Digital Equipment Corporation
Maynard, Massachusetts

digital

PDP-9, 9/L

INTERFACE MANUAL

DEC-09-H7AA-D

PDP-9
PDP-9/L

INTERFACE MANUAL

DIGITAL EQUIPMENT CORPORATION □ MAYNARD, MASSACHUSETTS

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INTRODUCTION

This manual provides the design engineer basic interface data for the PDP-9 and PDP-9/L computers manufactured by Digital Equipment Corporation of Maynard, Massachusetts. It is assumed that the reader is familiar with logic design, interface design, and basic PDP-9 programming.

Included in this manual are an introduction to DEC logic symbology; descriptions of the PDP-9 and PDP-9/L computers, with emphasis on input/output facilities; a complete description of interfacing techniques with detailed examples; some notes on terminal interfacing, margining, grounding; and general wiring rules. The I/O bus is summarized in Appendix A, a list of modules and their characteristics is presented in Appendix B, and a complete design example is given in Appendix C.

The following DEC reference documents provide additional design data: Logic Handbook (C-105), Industrial Handbook (C-110), PDP-9 User Handbook (F-95) and PDP-9/L User Handbook (DEC-9L-GRVA-D). The Logic Handbook and the Industrial Handbook provide complete specifications of DEC FLIP CHIP logic modules along with basic instructions in digital logic usage. The PDP-9 and PDP-9/L User Handbooks describe the instruction set for these computers and associated peripherals. Of particular interest are descriptions of the I/O instructions.

CHAPTER 1
INTRODUCTION TO DEC LOGIC

The logic circuits of the PDP-9 and PDP-9/L computers are assembled with DEC discrete component FLIP CHIP modules (B, R, S, and W series modules). Logic schematics (called block schematics at DEC) using these modules are usually drawn with DEC pre-MIL-STD-806B logic symbols. Except for shape representation, these logic symbols conform to MIL-STD-806B with additional features added for clarity. Both of these logic symbol standards are discussed below.

The most striking feature of DEC logic (and most puzzling to those not accustomed to it) is that a logic signal may be true (logical 1) either when it is high or when it is low depending on the logic designer's preference. In any given logic network, signals which are high-when-true and signals which are low-when-true will ordinarily exist. Not infrequently, the same logic signal will have two electrical representations, one high-when-true and the other low-when-true. In addition, the logic designer has the freedom of using the logic negation of a signal. This usage is indicated by a not sign (~), and overbar ($\overline{XXXX}$), or a minus sign preceding the signal name (Figure 1-1). Whether a signal is true-when-high or true-when-low is indicated by the type of diamond or arrow (open or solid) in DEC logic symbols or by the presence or absence of a small circle in MIL-STD-806B logic. This convention permits logic design without regard to the inversion properties of most DEC logic. It also permits assignment of logic packages to the realization of the design without requiring undue redesign to account for gate inversions.

Frequently in larger logic networks, it is convenient to show a named signal's source without a connection to its load which is located elsewhere (Figure 1-2). To facilitate this, a small circle may be drawn at the end of the source line when using MIL-STD-806 logic symbols in order to show that the signal is true-when-low.

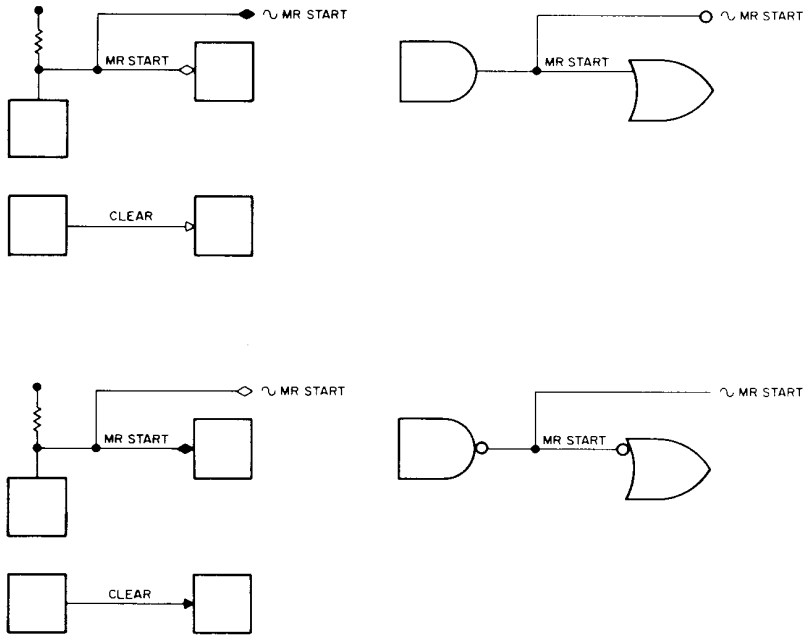


Figure 1-1 Digital Logic Signals

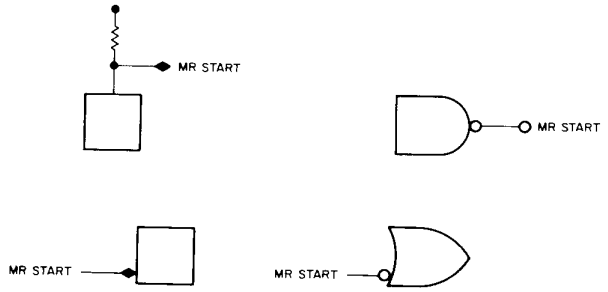


Figure 1-2 Sources and Loads Shown Without Connections

In DEC logic symbols, wired ANDs and wired ORs are not explicitly marked (Figure 1-3 and 1-4); they must be recognized. Due to the electrical properties of DEC's below ground logic (ground and -3V logic levels), a wired OR will usually occur at ground (high) and a wired AND at -3V (low). The B683 is an exception (refer to Appendix B).

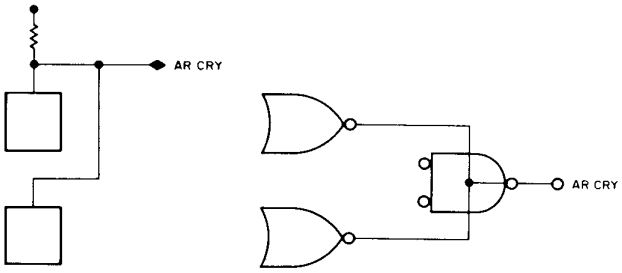


Figure 1-3 Wired AND

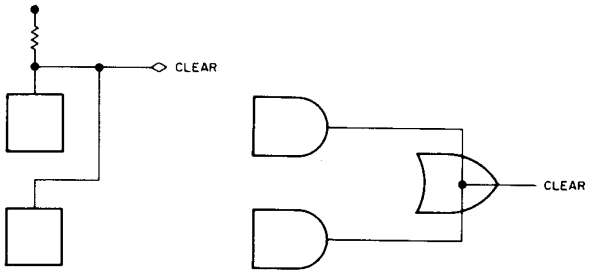


Figure 1-4 Wired OR

In DEC logic, most flip-flops are drawn with four outputs: one which is high when the flip-flop is in the 1 state, one which is low when the flip-flop is in the 1 state, one which is high when the flip-flop is in the 0 state, and one which is low when the flip-flop is in the 0 state. This convention allows the condition "the flip-flop is in the 1 (0) state" to be used with gates that require either high or low inputs without manipulating highs, lows, 1s and 0s. Although a flip-flop has four logical outputs, as noted above, it has only two electrical output connections, as the 1-high and 0-low connections are electrically equivalent (same output pin), as are the 1-low and 0-high connections. Except when the lines are quite short, connections to flip-flop outputs are not usually shown explicitly (Figure 1-5).

Figure 1-5 Flip-Flop Representation

In MIL-STD-806B logic drawings, DEC shows only the 1-high and 0-high output of a flip-flop, although all outputs are considered present for the purpose of logic design.

Mention should be made of the DEC diode-capacitor-diode (DCD) gate which is both an AND gate and a logic delay (Figure 1-6). This gate allows the output of a flip-flop to be sampled (with a DCD gate) at the same time the flip-flop state is changed. The flip-flop state seen by the DCD gate is the state prior to the change. The DCD gate generates an output pulse when the "level" input has been true (high) for approximately 400 ns and the "pulse" input has a 100 ns positive pulse or a positive-going (ground-going) level change with a rise time of less than 60 ns applied to it.

It is recommended that the DEC rectangular symbol for the DCD gate be used with either the older DEC logic symbols or with the MIL-STD-806B logic symbols in order to distinguish the quite different properties of the two inputs and to indicate the logic delay properties of the DCD gate. DEC logic sym-

bols are all rectangular in shape. The function of the symbol is indicated by a descriptive notation within the rectangle. Examples of the more common symbols are shown in Figures 1-7 through 1-15.

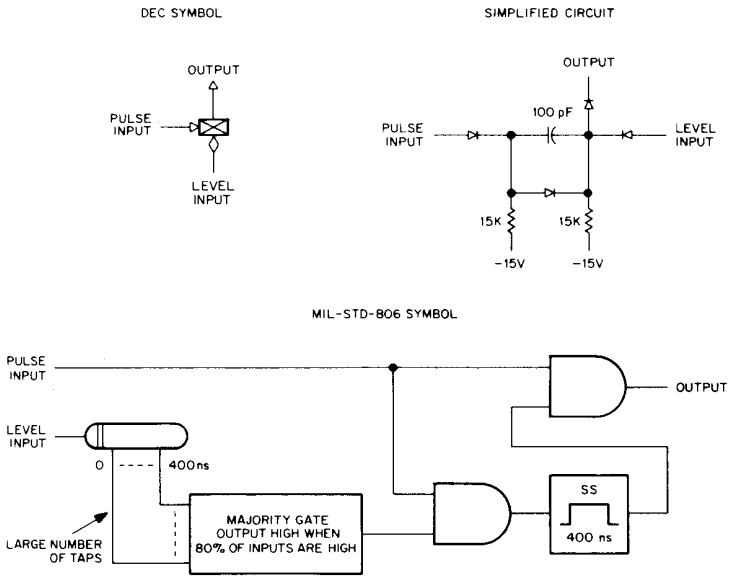


Figure 1-6 DCD Gate

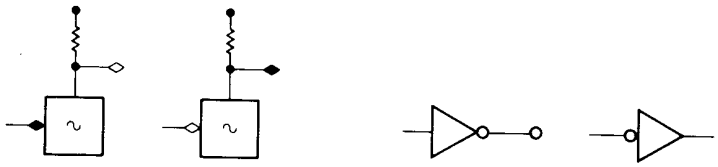


Figure 1-7 Inverter (NOT Gate)

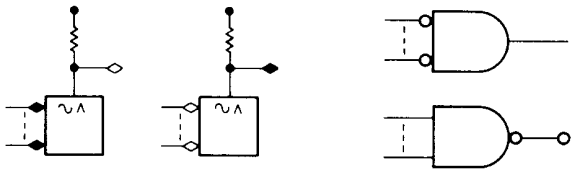


Figure 1-8 AND Gate

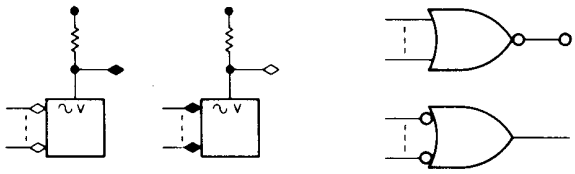


Figure 1-9 OR Gate

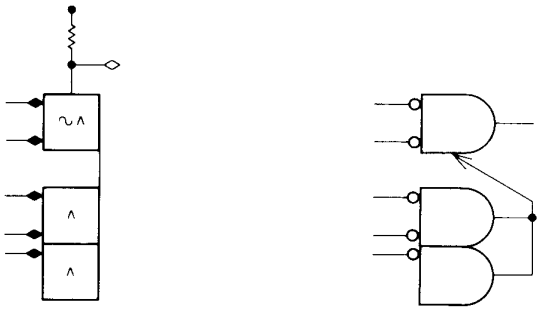


Figure 1-10 Expanded Gate

Figure 1-11 Pulse Amplifier

Figure 1-12 Monostable Multivibrator (Single Shot)

Figure 1-13 Monostable Multivibrator (Delay)

Figure 1-14 Delay

Figure 1-15 Clamped Load

DEC makes use of the electrical equivalence of various logic configurations. As an aid to understanding, symbols are drawn to represent the logic function intended by the designer rather than as a single standard symbol for each module type. Thus, a particular module type may appear as several different symbols. (See Figure 1-16.)

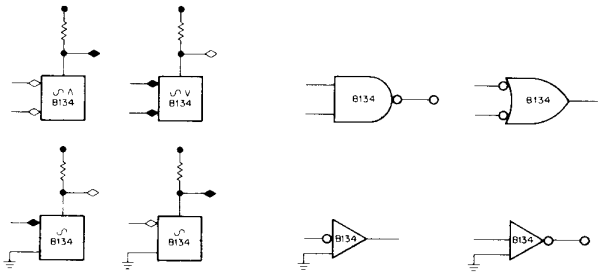


Figure 1-16 Different Uses of a Particular Module

Occasionally, the trailing edge of a signal will be used to cause some action, usually by triggering a DCD gate. This usage is illustrated in Figure 1-17. For additional details on the types of logic modules available see the DEC Logic Handbook (C-105) and the module descriptions in Appendix B.

Figure 1-17 DCD Usage

CHAPTER 2
THE PDP - 9 and PDP-9 / L COMPUTER SYSTEMS

2.1 PDP-9

The PDP-9 is a modular, medium scale digital computer. The basic system consists of a PDP-9 central processor with 8192 18-bit words of core storage (1 μs cycle time), a Teletype Model KSR33 Teletypewriter with keyboard and printer (10 cps), a paper tape reader (300 cps), and paper tape punch (50 cps). Also included are a real-time clock, hardware read-in, eight data channels, and a direct memory-access port. For details of expanded systems, see the PDP-9 User Handbook (F-95).

2.2 PDP-9/L

The PDP-9/L is a highly modular medium-scale digital computer. The basic system consists of a central processor with 4096 18-bit words of core storage (1.5 μs cycle time) and a Teletype Model ASR33 Teletypewriter and punch (10 cps) with keyboard and printer (10 cps). Also included are eight data channels and hardware read-in. No direct memory access port is available either in the basic or expanded version. For details of expanded PDP-9/L systems, see the PDP-9/L User Handbook DEC-9L-GRVA-D.

Both the central processor and the input/output facilities of the PDP-9 and PDP-9/L systems are very similar. Significant differences are pointed out in the text.

2.3 COMPUTER SUBSYSTEMS

The major subsystems of the two computers are the central processor unit (CPU), core memory, and the input/output facilities. These are described below.

2.3.1 Central Processor Unit

The PDP-9 and 9/L central processor unit (CPU) is a single address binary processor. This section describes the internal organization of the major CPU registers and is intended to give the user sufficient understanding of CPU instruction and data handling to prepare him for input/output interfacing techniques described later. For detailed descriptions of the CPU, refer to the PDP-9 or PDP-9/L maintenance manual.

The CPU employs a bus system on which data is transferred at dc levels between registers. In this bus system, all active registers use simple circuit designs for transfers which minimize timing problems.

The control elements and registers of the CPU that govern gating of information are described in the following paragraphs. (Refer to Figure 2-1.)

2.3.1.1 Control Elements and Registers

Instruction Register (IR) - The IR accepts the five most-significant bits of each instruction word fetched from memory. The four most significant bits constitute the operation code and, when decoded, indicate the entry point to the control memory microinstruction sequence necessary to effect system response. The fifth bit signals when the fetched instruction indicates indirect addressing.

Control Memory (CM) - The CM stores the sequence of internal microinstructions required to fetch and execute a program's instructions, to effect operation of the data channels, and to respond to operator commands initiated at the control console. It is a very fast, read-only, magnetic-core storage unit, prewired with the sequences.

Control Register (CR) - The CR provides gate control signals to the transfer buses and to the active registers. The register supplies new address information to the CM based on conditions sensed.

2.3.1.2 Major Registers - The major registers in the processor are as described in the following paragraphs.

Adder (ADR) - The 18-bit ADR functions as a fast adder for arithmetic operations and as the transfer path for inter-register transfers and shift operations. It also increments the PC and MB registers as required. Entry to the ADR is via the A bus and/or the B bus, under control of CR-developed gating control level. The ADR operates at a 5 mc rate to provide an inter-register transfer time of 200 ns.

Accumulator (AC) - The AC is an 18-bit register that retains the result of arithmetic/logical operations for the period between instructions. The AC can be cleared and complemented; its contents can be rotated right or left with the link. The contents of the memory buffer register can be added to the contents of the AC with the result left in the AC. The contents of both the MB and AC can be combined by the logical operation AND and exclusive OR, with the result remaining in the AC. The inclusive OR can be formed between the AC and the DATA switches on the operator console and the result can be left in the AC. For all program controlled transfers, information is transferred between core memory and an external device through the accumulator.

Link (L) - This 1-bit register is used to extend the arithmetic capability of the accumulator. In 1's complement arithmetic, the link is an overflow indicator; in 2's complement arithmetic, it logically extends the AC to 19 bits and functions as a carry register. The program can check overflow into the link from the accumulator to greatly simplify and speed up single and multiple precision arithmetic routines. The link can be cleared and complemented and its state sensed independent of the AC. It is included with the AC in rotate operations and in logical shifts.

Arithmetic Register (AR) - The AR functions with the AC to perform arithmetic and logic operations. It is not accessible to the programmer. Its operation is a function of the microinstruction sequence in the CM.

Multiplier-Quotient Register (MQ) - The optionally implemented extended arithmetic element (EAE) adds the logic of the MQ to the basic PDP-9. The MQ is 18 bits long and holds the multiplier during multiplication instructions and receives the low-order 18 bits of the resulting product. During division operations, it holds the low-order 18 bits of the dividend and, at the completion of the divide instruction, it contains the quotient. It can also be used as an extension of the AC for 36-bit shift operations and for data normalizing operations.

Program Counter (PC) - The PC determines the program sequence; that is, the order in which instructions are performed. This 13-bit register contains the address of the memory cell from which the next instruction is to be taken. Addition of the memory extension control option expands the PC to 15 bits for addressing up to 32,768 locations.

Memory Buffer Register (MB) - All information transferred into, or out of, core memory passes through the 18-bit MB. Information is read from a memory cell into the MB and is rewritten into the cell in one cycle time. Instructions and data are brought from core memory into the MB for processing. The MB also serves as a buffer for information transferred between core memory and the external device in data channel transfers. As an example of operation, the CPU would perform the instruction to add the contents of the MB to those of the AC by issuing the following microinstructions (see Figure 2-1).

MB OUT	/THIS OPENS THE MB TO THE /B BUS
AC OUT	/THIS OPENS THE AC TO THE /A BUS

The adder now adds the contents of the A and B buses, and the output of the adder is fed back to the input mixers of the major registers.

NO SHIFT	/THE OUTPUT OF THE ADDER IS /GATED ONTO THE "0" BUS (OR /INPUT GATES TO THE MAJOR /PROCESSOR REGISTERS)
AR IN	/THE "0" BUS (OR ADDER OUT- /PUT) IS TRANSFERRED TO THE /AR
AR OUT	/OPEN AR TO "A" BUS
NO SHIFT	/GATE ADDER OUTPUT TO "0" /BUS
AC IN	/TRANSFER DATA TO AC

2.3.2 Core Memory

2.3.2.1 PDP-9 Memory - PDP-9 core memory (Figure 2-1) operates with a complete cycle time of 1.0 μs. Each 8192-word core memory module contains a core stack, sense amplifiers, drivers, and a memory address (MA) register. The MA sets up the memory location (address) to be used for data retrieval or storage.

System core memory can be expanded from the basic 8,192 words up to 32,768 words in 8,192-word increments. Such expansion requires implementation

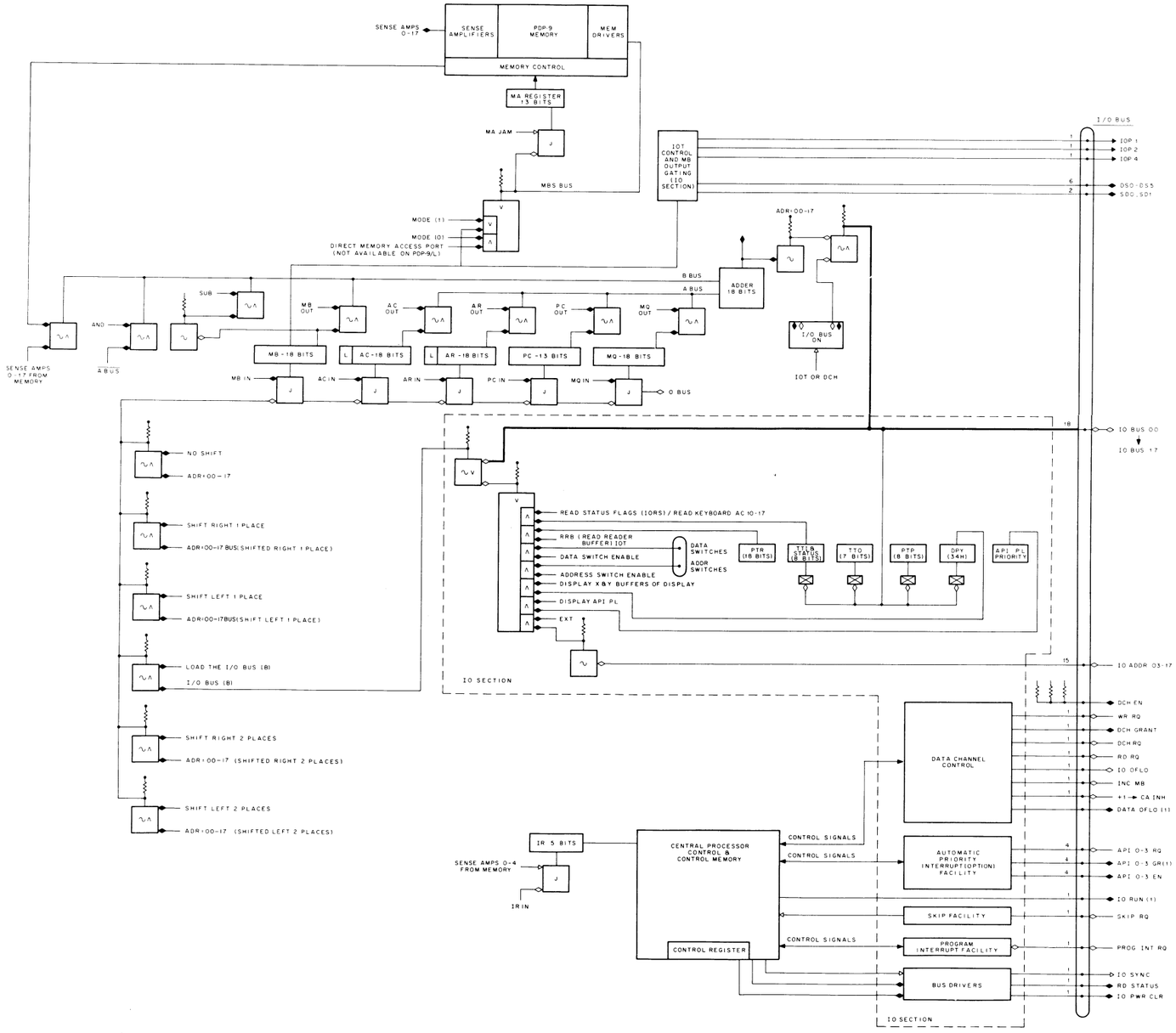


Figure 2-1 CPU Control Elements and Registers

of the optional Type KG09A Memory Extension Control, to extend PDP-9 addressing capability.

Each PDP-9 memory module has a two-port capability for data entry and retrieval. One port, connecting to the memory bus, services the processor; the other port allows a peripheral device direct and immediate access to memory for fast data transfers via a direct memory access (DMA) bus. A device request for DMA service has priority over a processor request, which is deferred until DMA operation terminates. The optional Type DM09A Multiplexer Adapter permits concurrent servicing of up to three DMA peripherals and assigns each a fixed priority.

2.3.2.2 PDP-9/L Memory - The PDP-9/L core memory is a 4-wire, 3D system with a cycle time of 1.5 μs. The basic PDP-9/L contains 4,096 18-bit words and is expandable in 4,096-word sections up to 32,768 words. The Type KG09A Memory Extension Control option is required for memory expansion above 8K. Each PDP-9/L memory has a one-port capability, i.e., no direct memory access is available.

2.3.3 Input/Output Facilities

One of the most useful features of both the PDP-9 and PDP-9/L computer systems is the flexible, high capacity input/output facility (Figure 2-1) with which the computers communicate to such DEC peripherals as displays, analog-digital and digital-analog converters, magnetic tape controllers, data communications equipment, disk systems and, for the PDP-9, drums. The design techniques developed for interfacing special systems are simple and inexpensive; for example, it is possible for the PDP-9 and PDP-9/L to communicate with their associated peripherals in two ways:

a. Under direct program instruction control (Program Controlled Transfers)

b. Under channel control (Channel Transfers)

Program controlled transfers are implemented under direct supervision of a stored program. Machine instructions, called IOT instructions, contained in this program carry out the necessary internal and external (device) signal conditioning to effect the desired information transfer. This method requires very little device interface logic and is the least expensive method for slow speed transfers (50,000 words per second for the PDP-9 and 33,000 words per second for the PDP-9/L). However, program controlled transfers require the use of major registers in the CP which must be cleared of vital information before a transfer occurs.

Channel transfers require more logic in the external device, but are less demanding of computer hardware and time. In general, they are used to move large blocks or arrays of data between machine and peripheral at rates of from 6 to 20 times those of program-controlled transfers.

The PDP-9 uses two distinct channel transfers, the data channel (DCH) and direct memory access (DMA) Figure 3-1. The data channel requires from three to four memory cycles to effect an 18-bit word transfer and uses some of the CP control logic. The PDP-9/L has only the data channel facility which is the same configuration as in the PDP-9; however, the 1.5 μs cycle time of the PDP-9/L slows transfer to two-thirds of the rate of the PDP-9 transfers.

Both computers communicate with peripheral devices by program control and data channel through the I/O bus which consists of two 36-pair cables with male connectors at both ends. Each peripheral is chain linked to a common interface point at the central processor. Signals between the bus and central processor are shown in Figure 2-1. Each signal is described in detail and some of the computer control logic which serves them is shown in the following section.

A summary of the physical properties of the I/O bus and descriptions of the signals it serves are given in Appendix A. The DMA channel of the PDP-9 has its own bus, and will be covered separately.

2.3.3.1 Program Controlled Transfers - When there are a small number of peripherals and no complex timing or stringent priority considerations in a computer system, data can be transferred by IOT instructions via the I/O bus to and from peripherals (most applications fall into this category). Hardware cost is low since the computer supplies most of the control, but computer time may be high.

There are four computer subsystems used in program-controlled transfers. These are: IOT instruction logic, read status logic, program interrupt and skip logic, and API logic. Each of these is described below.

IOT Instruction Logic - Input/output (IOT) instructions initiate the transmission of signals through the I/O bus to control peripheral devices, sense their status, and effect transfers between them and the processor. When an IOT instruction is transferred to the MB (Figure 2-1) the computer logic decodes it according to the format shown in Figure 2-2.

The PDP-9 IOT instruction has the following characteristics.

a. An operation code of 70_8.

b. An 8-bit selection code to allow the selection of up to 256 decoders. Outputs of these decoders are used by peripheral devices to enable various functions such as data transfers.

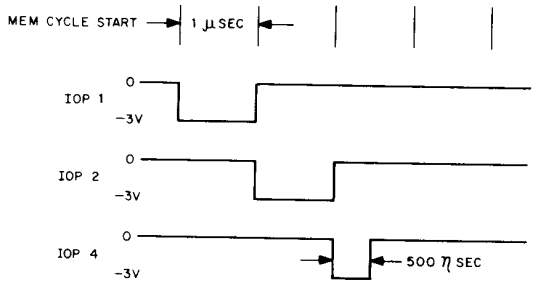


Figure 2-3 IOP Timing Diagram for PDP-9

c. If the device has requested an input transfer (to the computer) by grounding the RD RQ signal of the I/O bus, the contents of the 18 data lines, I/O

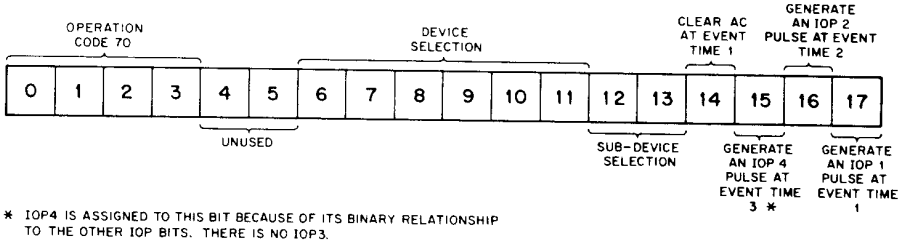


Figure 2-2 PDP-9 IOT Instruction Format

c. A command code (bits 14-17) capable of being microprogrammed to clear the AC and/or issue up to three pulses to the I/O bus (IOP1, IOP2 and IOP4).

When an IOT instruction is decoded in the IR, the following sequence occurs (Figure 2-1).

a. The bit pattern placed in MB bits 6 through 13 is buffered by the IOT control logic (where it emerges as DS0 through DS5 for MB6 through MB11, and SD0, SD1 for MB12 and MB13) and placed on the I/O bus cable. Assertion or binary 1 is -3V and binary 0 is ground. (The device logic used to respond is explained later.)

b. The microprogrammed signals IOP1, IOP2 and IOP4 are generated by the IOP control logic, if they are selected by the instruction, and appear in time sequences defined by the IOP timing diagram (Figures 2-3 and 2-4). They are used by the device to effect data transfers, sense the status of a device, or issue commands.

BUS 00-17, are jammed into the AC register of the CP. If, during the IOT instruction, the RD RQ line is not grounded, the computer will place the contents of its AC onto the 18 data lines. The proper timing to effect the transfer is given in Chapter 4.

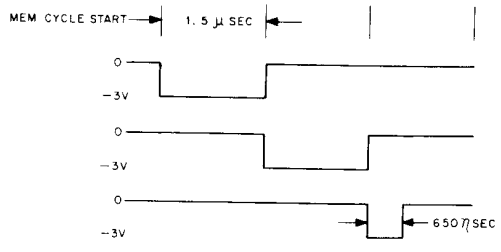


Figure 2-4 IOP Timing Diagram for PDP-9/L

There are five basic control circuits in the PDP-9 and PDP-9/L I/O sections, which handle the IOT instructions. Part of each circuit is described below. Characteristics of the driver or receiver modules are presented in Appendix B.

MB Bits 6 through 13 Buffering - Figure 2-5 shows how MB bits 6 through 13 of the CP are gated with the IOT (B) signal (always present during an IOT instruction) and then drive DEC Type B213 Bus Drivers down the I/O bus in the form of signals DS0 through DS5 for MB6 through MB11 and SD0, SD1 for MB12 and MB13. Any device on the bus must be able to decode these signals.

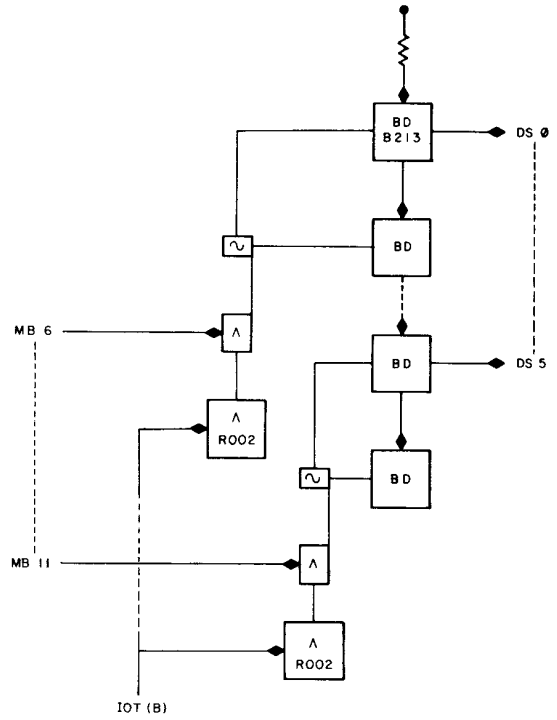


Figure 2-5 MB, DS or SD Signal Buffering

IOP Control Logic - The IOP control logic is shown in Figure 2-6. A 2-bit counter (IO0, IO1) is driven by the I/O CLK POS clock pulse during the IOT instruction. The counter pulses each of the three R602 Pulse Amplifiers in turn. If any one is enabled by the appropriate MB bit 15, 16, or 17, the associated flip-flop, IOP1, IOP2, or IOP4 is set. IOP1 and IOP2 are reset by the next I/O CLK POS pulse while IOP4 is reset by a delay.

Data Lines (I/O Bus 00 through I/O Bus 17) - Figure 2-7 indicates the modules which manipulate the data lines. I/O bus line 01 is illustrated as an example.

RD RQ - This ground signal, which must be issued by the device requesting data transfer to the computer, is gated with IO1 to the IOP counter and is used to generate an AC RD control pulse to the CP (see Figure 2-6).

I/O PWR CLR - Whenever it becomes necessary to reset a device to its initial conditions, I/O PWR CLR pulses, which are 400 ns (nominal width) negative-going signals, are issued. This occurs during power turn-on, actuation of the IO RESET switch, or the occurrence of a CAF (clear all flags) instruction. The output driver for I/O PWR CLR is shown in Figure 2-8.

Read Status Logic - The IOT instruction IORS = 700314 sends a pulse down the RD status line of the I/O bus. This signal can be used to place various device flags onto the data lines. The computer then reads the data on these lines into its AC for evaluation. These status bits can also be displayed on the register indicators by turning the console switch to position STATUS (STA on the PDP-9/L) and stopping the computer. In this situation, a train of pulses is placed on the RD status line. The output logic for the RD status line is shown in Figure 2-9.

Program Interrupt (PI) and SKIP Logic - To avoid forcing the computer to continually monitor slower devices for their ready conditions in program controlled transfers, program interrupt and SKIP facilities are built into these computers. The program interrupt logic allows a device to force the running computer into a break state (i.e., a break from normal program sequence) by grounding the PROG INT RQ signal of the I/O bus. Before entering this break state the computer completes its current instruction or higher order break (such as DCH request or API or real-time clock), stores the contents of the PC, link, state of extended memory, state of memory protect and content of extended PC in location 0 and executes the instruction in location 1 (see Figure 2-10). This instruction is usually a JMS to a SKIP routine.

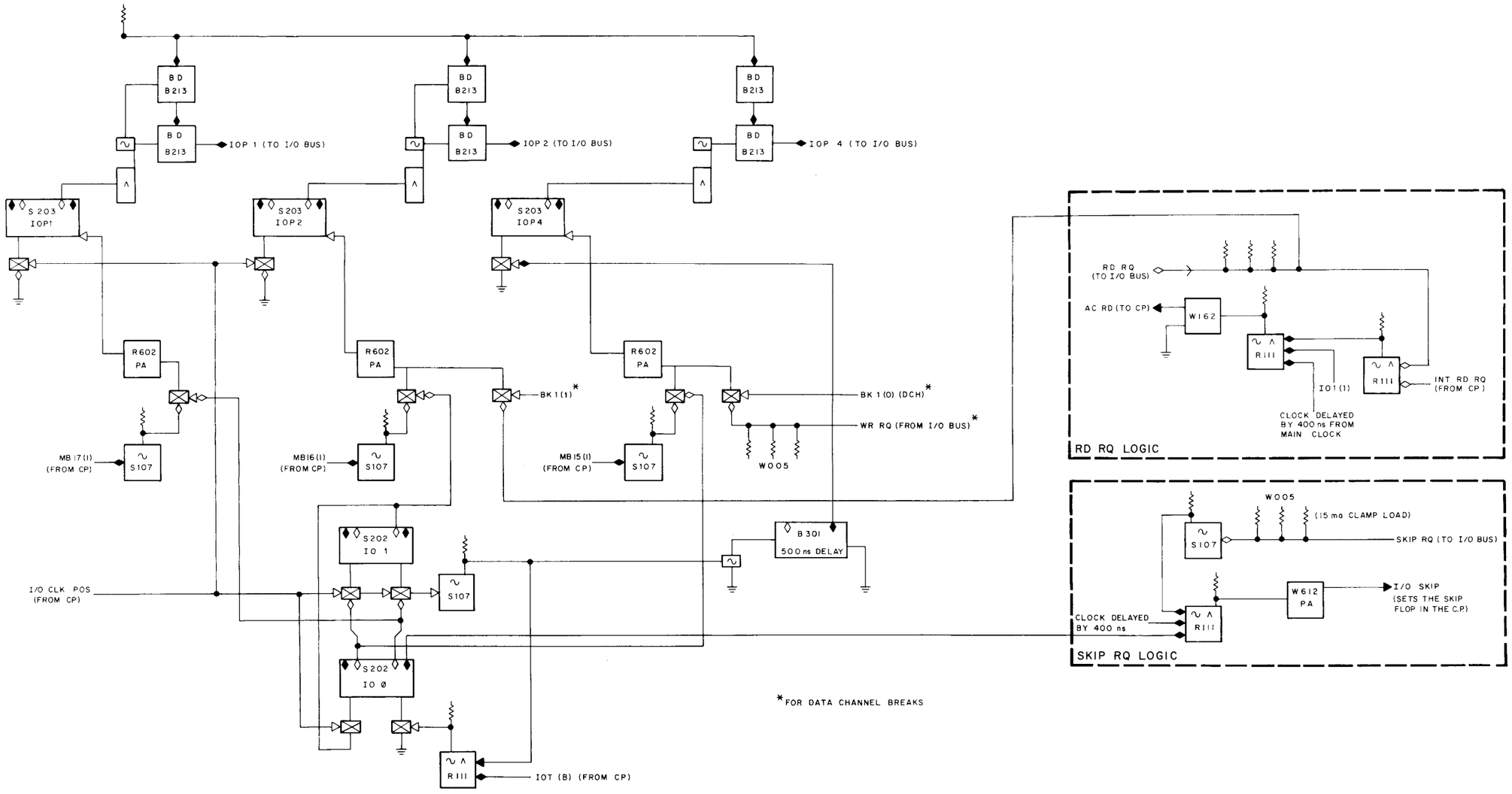


Figure 2-6 IOP Control Logic

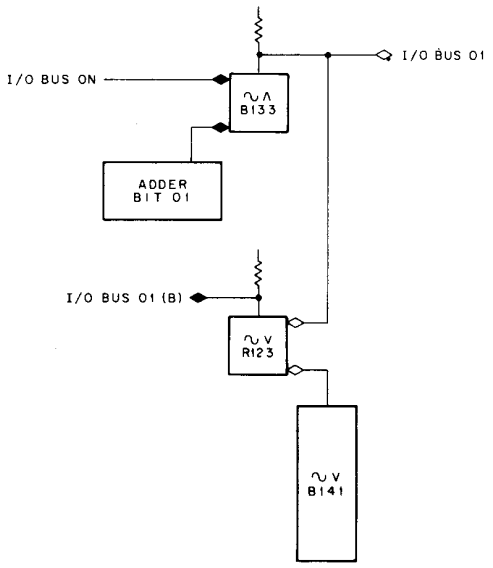


Figure 2-7 Typical Input/Output Logic for Data on I/O Bus Lines 00 through 17

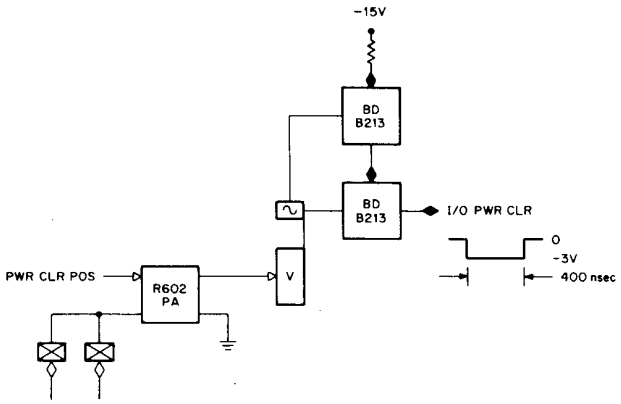


Figure 2-8 I/O PWR CLR Logic

The SKIP routines consist of a set of IOT instructions which send IOP1 pulses to all devices; thus interrogating each device which may be requesting the PI (many devices can tie onto the PROG INT RQ line). If a device returns the pulse via the SKIP RQ line of the I/O bus, the computer skips the next instruction. Thus, the device has been identified and can be serviced by the computer.

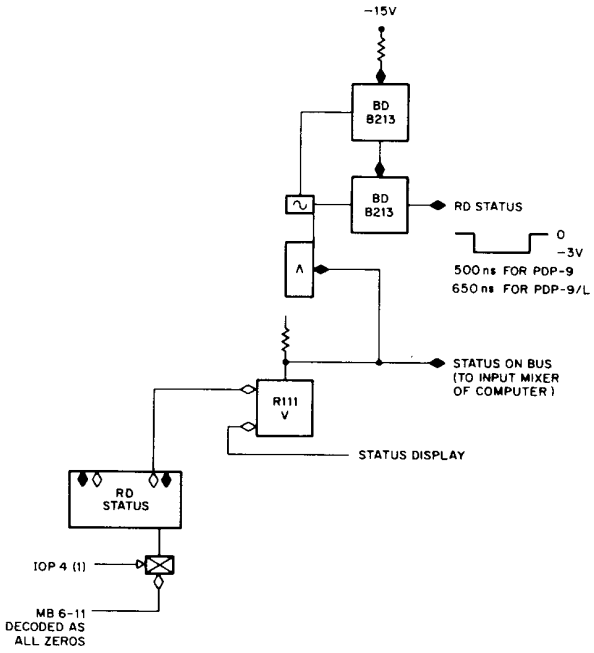


Figure 2-9 RD Status Logic

INFORMATION	L	EM	MP	EPC	PC
SIZE (BITS)	1	1	1	2	13

L = LINK CONTENT
EM = STATE OF EXTEND MODE
MP = STATE OF MEMORY PROTECT MODE
EPC = CONTENT OF THE EXTENSION TO PROGRAM COUNTER AND;
PC = CONTENT OF THE PROGRAM COUNTER.

THE INTERRUPT SERVICING SUBROUTINE MUST SAVE AND RESTORE THE CONTENTS OF THE ACCUMULATOR.

Figure 2-10 Program Interrupt Storage Word Format

The I/O logic used by the computers to effect the PI facility is shown in Figure 2-11. The flip-flop PIE (program interrupt enable) is set with the ION instruction (700042). Then, if CLK SYNC, DCH SYNC and PI disable are all low, the flag PROG SYNC can be set by I/O SYNC IN if a PROG INT RQ is initialized by some device. A control pulse called BK (1) then sets PROG SYNC which requests control memory to accept an odd address, which forces the computer to put the PC, link and extended memory address into location 0. The PC then goes to 1 and this becomes the address of the next instruction executed.

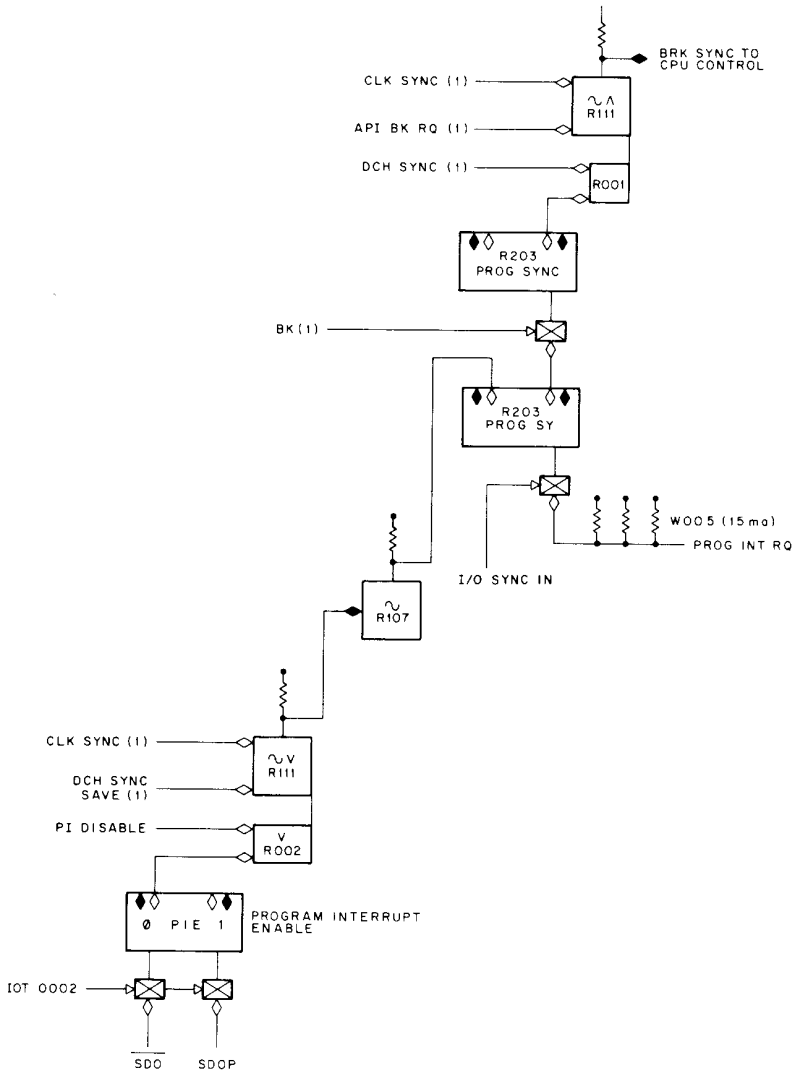


Figure 2-11 I/O PI Logic

Figure 2-6 shows the SKIP facility control logic. Here, the grounded SKIP RQ line is inverted, gated with bit I/O (1) of the counter, and finally triggers the W612 Pulse Amplifier which sets the CP SKIP flip-flop. This flip-flop forces the computer to add 2 to the PC instead of 1.

Automatic Priority Interrupt (API) System - The PI facility becomes inefficient on a system with a large number of peripherals which require a hierarchy of priorities or data rates of more than 50,000 words per second. In this case, central processor overhead time can be reduced with a multichannel interrupt system. Such an option is the KF09A Automatic Priority Interrupt Facility provided in the PDP-9 system. A complete description of this option is given in a separate manual, DEC-08-I5AA-D. However, Chapter 3 will outline the interfacing techniques required to use in the API.

2.3.3.2 Channel Controlled Transfers - The PDP-9 has two separate facilities for channel controlled transfers. There are data channel and direct memory access. The PDP-9/L, however, uses only the data channel facility which is identical to that in the PDP-9 except for timing.

Channel transfers, in general, differ from program-controlled transfers in that they are designed to manipulate blocks of data, rather than a word at a time (a block of data is defined as a series of data words stored in sequence in some device; i.e., core memory or disk). A block of data can be completely specified for any device by the address of its first word and the number of words in the block. Thus, to specify a block and its destination between any two devices, three variables are necessary.

These are:

a. Present first address;

b. First address of its destination;

c. Word count of the block.

Data Channel (DCH)

Each device on the DCH is assigned two locations in memory. The first location is defined as the word count (WC) register and is programmed to contain the 2's complement of the word count of the block. The second location is programmed to contain a value one less than the address in memory that will send or receive the first word of the block. This location is called the CA (current address) register.

After the computer has set up the WC and CA registers and has specified the address of the device's first word, it enables the device and returns to its main program. The device then informs the computer via the DCH RQ (data channel request) line when it wants to transfer each word and specifies on I/O ADDR lines (I/O address) its WC address. The CA register automatically becomes WC+1. At any given transfer, the WC and CA locations are incremented by the computer. Then, the word on the bus is passed into the address specified by the contents of CA. If, during the transfer, WC overflows; that is, the last word of the block has been reached, an I/O OFLO (overflow pulse) is transmitted to the device. During DCH transfers, the CP suspends execution of the main program. The MB register is used as a buffer between memory and device (see Figure 2-1).

DCH Logic - The I/O bus contains seven lines unique to the DCH, which are DCH RQ, DCH GR(1), DCH EN, ADD OFLO, I/O OFLO, INC MB and +1→CA INH. Other I/O bus signals used by the DCH include: IO PWR CLR, IO SYNC, IO ADDR 03 →IO ADDR17, WR RQ, and RD RQ.

The DCH RQ (request) line asks for a data channel break from the computer; the DCH GR (grant) signal represents the computer's permission to "go ahead." DCH EN (enable) is a -3V line that is linked from device to device to establish priority among the group tied to DCH. It can enable one device to post a DCH RQ or prevent it from doing so if a higher priority device has already requested it.

ADD OFLO (address overflow) and I/O OFLO (overflow) are signals issued by the computer to indicate overflow conditions. I/O PWR CLR (power clear) is used in each device to set all registers to their initial states (i.e., clear all data registers, interrupt flags, etc.). I/O SYNC (synchronize) is a timing pulse, I/O ADDR 03 to I/O ADDR 17 (address) specify word count registers assigned in memory to each device. RD RQ (read request) is a signal issued by a device to inform the computer that information must be transferred to computer memory. WR RQ (write request) is also issued by the device only to inform the computer that the transfer must be out of computer memory. INC MB causes a single cycle DCH break where the contents of the word located at the address specified on I/O ADDR lines is incremented by 1. +1 →CA INH, when grounded by a device, inhibits the computer from incrementing the CA during the DCH break.

I/O SYNC pulses (Figure 2-12) occur on computer CLK POS pulses only where no AM SYNC (DMA) is present, and where no IOT instruction is currently in progress (IOT(0)). Output drivers are B213 Bus Drivers.

DCH RQ Logic - If a DCH RQ ground level (Figure 2-13) is present on the enabling input to the DCH SYNC flag, then I/O CLK POS will set this flag provided IOT(0), CLK SYNC(0), etc. are present. This means that this flag is set if no IOT, RTC, PI or optional API operation is in progress. The DCH, therefore, cannot interrupt any of these operations. However, once set, DCH SYNC inhibits the CLK, and the API takes priority.

DCH SYNC sets DCH SYNC SAVE which ultimately requests the break state from the CP. DCH SYNC also drives a B213 Bus Driver which supplies DCH GRANT to the device. DCH GRANT requests that the device specify its WC address.

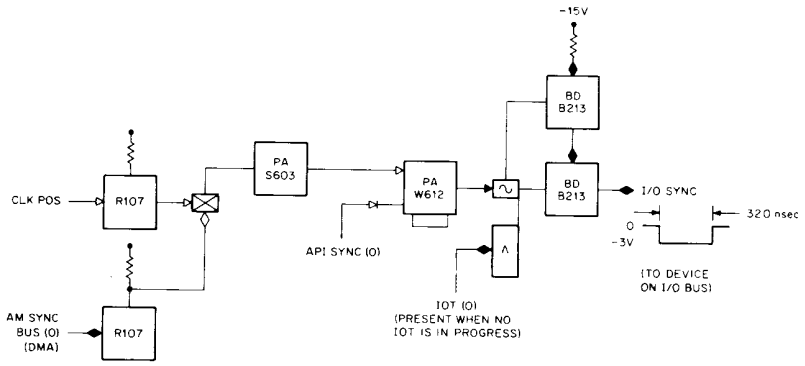


Figure 2-12 I/O Sync Logic for the Computers

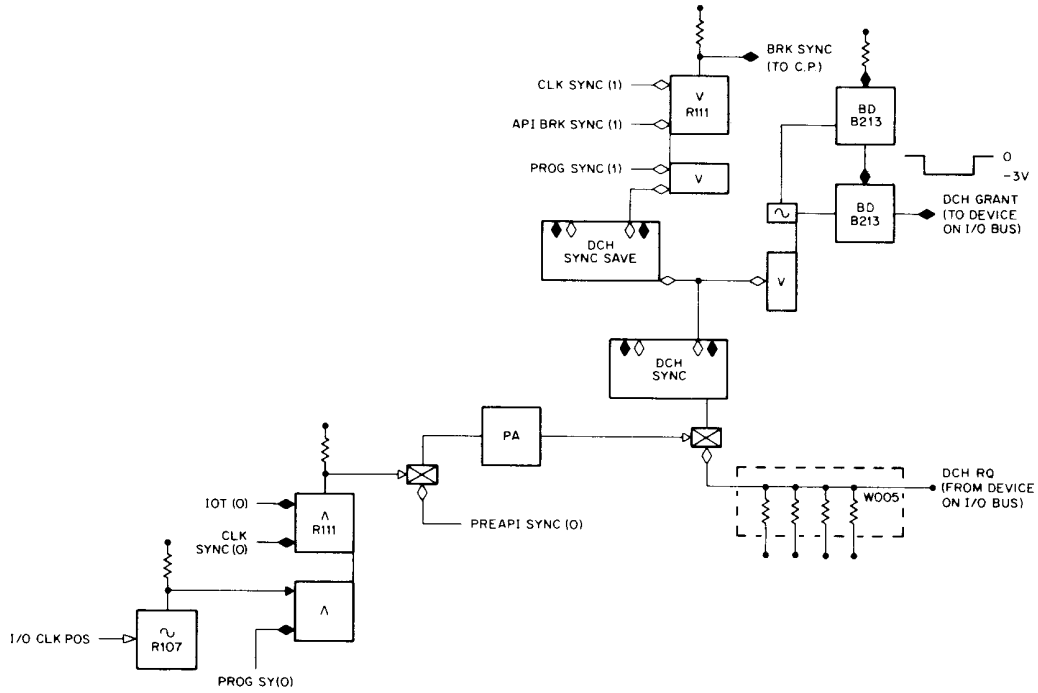


Figure 2-13 DCH RQ Logic for PDP-9 and PDP-9/L

IO OFLO Logic - The IO OFLO signal, derived from a B213 in the CP (Figure 2-14) occurs during the WC cycle of a data channel break if the WC address overflows to all zeros.

IO ADDR Input Logic - The IO ADDR input logic (Figure 2-15) consists of Type S103 Inverters and two 5-mA clamped loads from a W005 module. The output of this circuit is the IO ADDR XX(B) signal

which goes to the input mixer circuit shown in Figure 2-15.

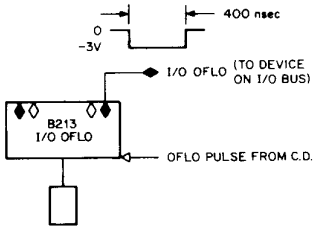


Figure 2-14 IO OFLO Output Logic

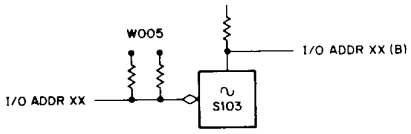


Figure 2-15 IO ADDR Input Logic to Computer

DATA OFLO Logic - The DATA OFLO signal is derived from a B213 flip-flop as shown in Figure 2-16. DATA OFLO is a 200 ns pulse, gated onto the I/O bus in the middle of the third add to memory DCH cycle, which signals an incorrect sum occurred. This happens when the contents of the MB and the contents of the I/O bus are of like signs and their sum has the opposite sign. If the contents of the MB and the contents of the I/O bus have opposite signs DATA OFLO cannot occurs. Thus,

DATA OFLO occurs when:

$$(MB) + (I/O\ Bus) > 2^{17} - 1$$

OR

$$(MB) + (I/O\ Bus) < -2^{17}$$

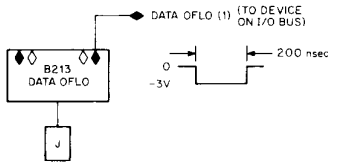


Figure 2-16 DATA OFLO Logic

+1 → CA INH and DCH EN Logic - The +1 → CA INH is a signal from the device to the computer. It is applied to an R002 Diode Gate and two 5-mA clamped loads. DCH EN is a -3V signal from the computer to the device and is produced by three 5-mA clamped loads. Both of these signals are shown on Figure 2-17.

INC MB Signal - The INC MB signal is distributed between I/O facilities and control memory. Loading for INC MB is the same as that for RD RQ, shown in Figure 2-6.

Direct Memory Access Channel (DMA)

The DMA logic of the PDP-9 is sufficiently complicated to require reference to the PDP-9 Maintenance Manual for logic schematics and explanations.

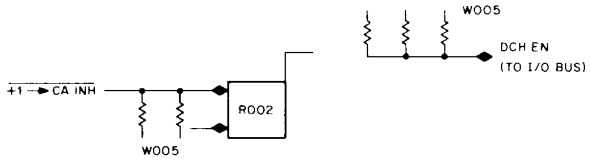


Figure 2-17 +1 → CA INH and DCH EN Logic

CHAPTER 3
INTERFACING TO THE PDP - 9 and PDP-9 / L COMPUTERS

This chapter presents techniques and examples for interfacing special devices to either the PDP-9 or PDP-9/L computer. The methods shown have been designed and implemented by DIGITAL engineers and by no means represent any design rule restrictions. In many applications modules or circuits other than those shown can be employed for the same desired function at the discretion of the design engineer. In all cases, however, the bus rules summarized in Appendix A of this document must not be violated.

Both the PDP-9 and PDP-9/L communicate with their associated peripherals through I/O bus cables. Three transfer techniques can be used:

a. Program controlled transfers for systems without optional API.

b. Program controlled transfers using the API facility.

c. Data channel transfers.

Program controlled transfers occur under direct control of IOT instructions. Data channel transfers are set up by IOT instructions, but are carried out independently. All transfers take place between the computer and its peripherals through a parallel I/O bus system (Figure 3-1). Each device interface has two sets of I/O cables; (these are two cables per set) an input set which comes from the computer or from the previous device, and an output set that goes to the next peripheral device on the line. Input cables are jumpered to the output cables within the device.

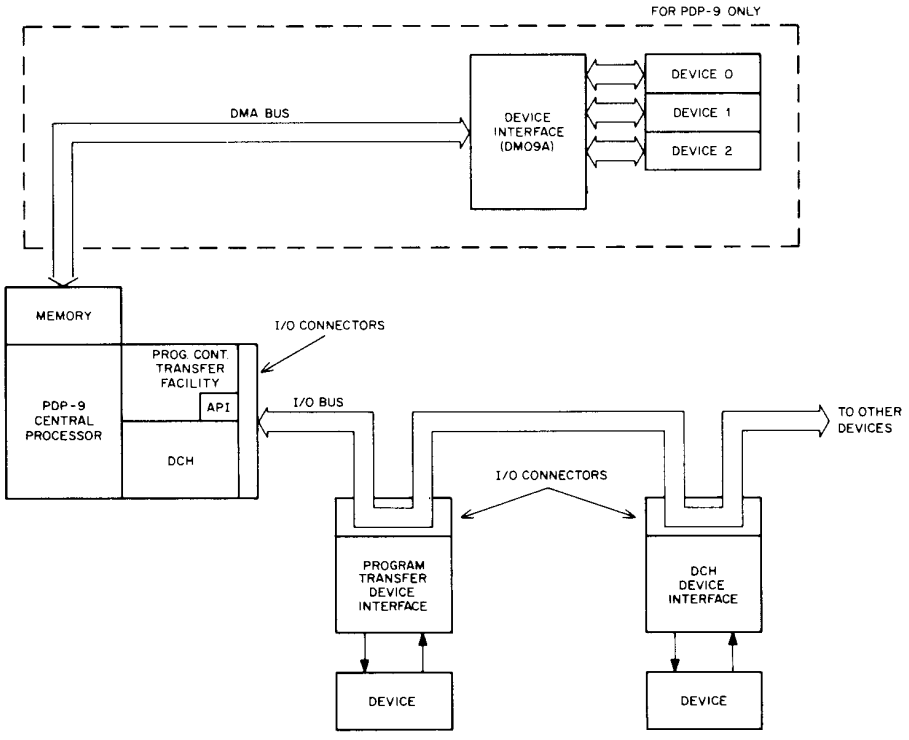


Figure 3-1 Interfacing to the PDP-9 and PDP-9/L Computers

3.1 PROGRAM CONTROLLED TRANSFERS

3.1.1 Signal Summary

The signals used with program controlled transfers in the computers were described in Chapter 2. The configuration of the PDP-9 and PDP-9/L I/O control logic which generated these signals was also shown. For characteristics of the modules driving, or receiving from the computer bus refer to either the Digital Logic Handbook (C-105) or Appendix B of this manual.

In summary, there are a total of seven sets of signals for non-API program controlled transfers. These are as follows:

DS0 through DS5, SD0, SD1

These signals correspond to the bit pattern in MB bits 6 through 13 during the IOT instruction and are used to address the device.

IOP1, IOP2 and IOP4

These control pulses decoded from MB bits 17, 16, and 15 are used by the device to effect transfers or sense control functions.

RD RQ

A signal which the device must place at ground if it requires a data transfer into the computer.

Data Lines

I/O Bus 00 through I/O Bus 17 carry an 18-bit word to or from the AC during program controlled transfers.

I/O PWR CLR

Clears all device flags committed to it.

PROG INT RQ

Causes the computer to go into a "break" state when enabled.

SKIP RQ

A ground on this line will force the computer to skip the next instruction after completion of the current IOT instruction.

3.1.2 Peripheral Interface Requirements

The bused system of input/output data transfers imposes the following requirements on peripheral equipment using the programmed data transfer facility.

a. Each device must have the ability to sample the select code generated by the computer during IOT instructions. When selected, it must be capable of producing sequential command pulses in accordance with the computer-generated IOP pulses. Circuits performing these functions in peripheral devices are called device selectors (DS). One double-sized module Type W109 provides all these functions.

b. Each device receiving output data from the computer must contain gating circuits at the input of a receiving register which are capable of strobing the data on the I/O bus into the register when triggered by a command pulse from the device selector. Such gates are called device input gates.

c. Each device supplying input data to the computer must contain gating circuits at the output of the transmitting register capable of strobing the information from the output register to the I/O bus, and furnishing a read request (RD RQ) level to the computer when triggered by a command pulse from the DS. Such gates are called device output gates.

d. Each device many contain a BUSY/DONE flag (flip-flop) and gating circuits that can supply a signal to the computer input/output skip bus upon command from the DS. The flag is set to indicate that the device is ready to transfer another byte of information.

Since the I/O bus is bidirectional, a signal called RD RQ must be supplied by the device to inform the computer that the desired direction of the data transfer is from the device to the AC. If RD RQ is not present, the computer assumes an outgoing transfer (from the computer).

3.1.3 I/O Bus Transfer

3.1.3.1 Loading a Device Buffer From The AC - Loading a device buffer from the AC (Figure 3-2) is usually accomplished by but is not restricted to the following two steps. The first IOT clears the device buffer and the second IOT ORs the contents of the AC into the cleared buffer. For such a transfer, the details are as follows:

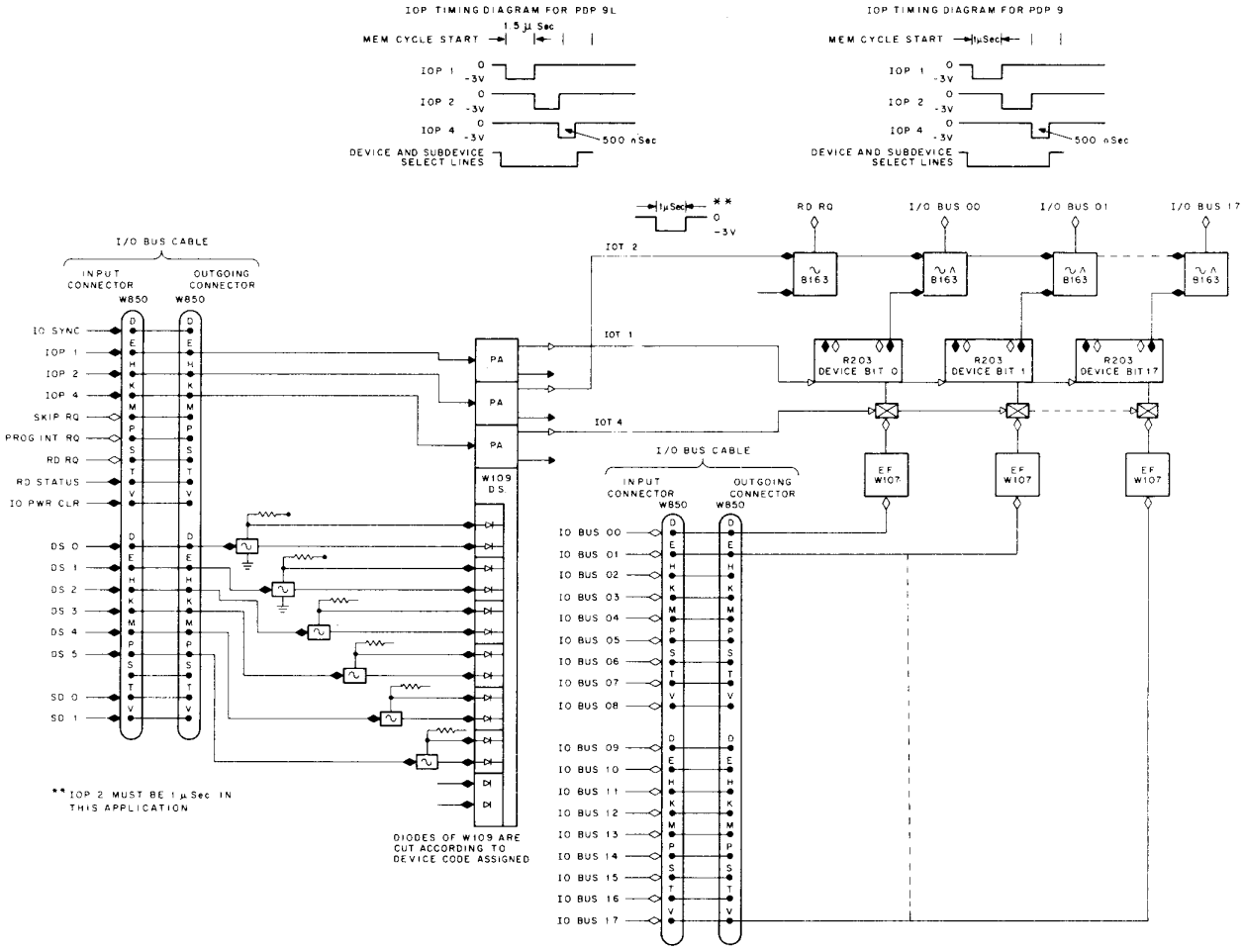


Figure 3-2 Reading and Writing on the PDP-9 and PDP-9/L I/O Buses

a. Prior to the end of the first cycle the AC is placed onto the I/O bus. Note that in any output transfer, IOP1 must not be used to transfer the AC to an external register.

b. IOT1 is generated in the Device Selector Module W109 and transmitted to all "clear" inputs of the flip-flops in the device buffer.

c. IOT4 is generated in the W109 and applied to the DCD input gates of the device buffer. Note that the input to the DCD gates for each bit must be buffered from the I/O bus by Type W107 Emitter Followers.

3.1.3.2 Reading a Device Buffer into the AC - Reading the content of a device buffer into the computer is accomplished in the following manner:

a. IOT pulse 2 is generated in the device selector module which is jumpered to produce a 1-μs pulse.

b. This 1-μs pulse is used to gate the device data buffer onto the I/O data bus.

c. Simultaneously, a read request positive pulse is generated (by a B163) on the RD RQ line.

d. The central processor receives the request signal and allows time for the data bus to settle completely.

e. The I/O bus is strobed into the AC.

The output of the W109 is a 1-μs pulse, and is regarded by the I/O bus system as a level. Either pulse or level notation may be used, provided this definition is kept in mind. Often, designers have used the W103 module and W640 modules to generate the 1-μs pulse. This combination has since been replaced with the W109 module.

Since the I/O bus is ORed into the AC the read IOT instruction is usually microprogrammed to clear the AC prior to reading (i.e., MB14=1). I/O waveforms are shown.

3.1.4 Other I/O Bus Facilities Used in AC Transfers

3.1.4.1 Program Interrupt (PI) Facility - When computer time is at a premium, it is advantageous for the computer to perform other tasks rather than to wait in a skip loop for the peripheral to complete its operation. The program interrupt facility allows the computer program to enter a subroutine at device request in order to service it. If more than one device is tied to the PI, a series of skip tests must be made to identify the requesting device.

Figure 3-3 shows the device hardware required for PI. The device flag is connected to the PROG INT RQ line with a B163 module or equivalent. When an interrupt is recognized by the computer, it stops execution of the main program, stores certain flags and the contents of the PC in memory location 000000. It then executes the instruction in location 000001, which should be a JMP to the skip subroutine. Interrupts occur only when the PI is enabled. The IOT instructions associated with the PI are:

```
IOF = 700002    /TURN OFF PI FACILITY
ION = 700042    /TURN ON PI FACILITY
```

3.1.4.2 I/O Skip Facility - The skip subroutine referred to above must identify the interrupting device. The I/O skip facility performs this function in the following way (see Figure 3-3).

When the IOT1 pulse is used in an I/O skip instruction (example CLSF = IOT 0001 = 700001), it is gated with the device flag flip-flop through a diode gate and returned to the computer on the I/O skip request bus line. A positive pulse, 1 μs wide, is returned to the processor if the tested flag is a binary 1. The skip flip-flop in the processor is set, and the instruction following the IOT instruction in the program sequence is not executed -- it is skipped. The signal on the skip line is sampled 600 ns after IOP1 is issued. A B163 Diode Gate or equivalent must be used in the device, to gate the SKIP RQ onto the bus.

The following program sequence represents a single output transfer to a device.

```
LAC Y       /LOAD AC WITH DATA

IOT SKIP    /TEST DEVICE STATUS
```

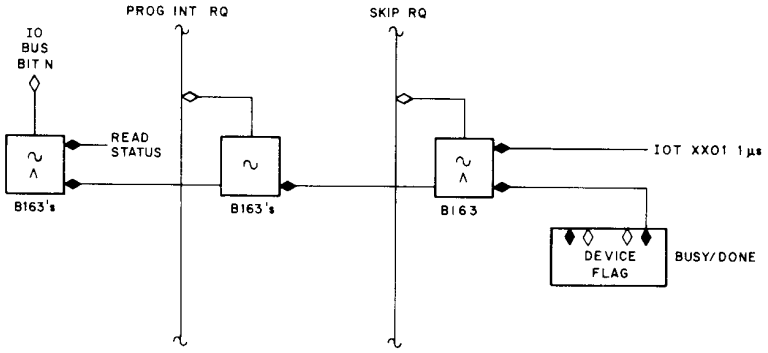


Figure 3-3 Device Flag Hardware

```
JMP. -1     /TEST DEVICE UNTIL READY
IOT WRITE   /TRANSMIT DATA TO DEVICE
```

An input transfer is represented by:

```
IOT SKIP    /TEST DEVICE STATUS
JMP .-1     /TEST UNTIL READY
IOT READ    /READ DEVICE BUFFER
DAC Y       /STORE AC IN Y
```

A skip subroutine might look like:

```
IOT SKIP D1 /TEST DEVICE 1
JMP .+2     /DEVICE 1 NOT INTERRUPTING
JMS SUB D1  /GO TO DEVICE 2 SERVICE SUB-
            /ROUTINE
IOT SKIP D2 /TEST DEVICE 2
JMP .+2     /DEVICE 2 NOT INTERRUPTING
JMS SUB D2  /GO TO DEVICE 3 SERVICE SUB-
            /ROUTINE
```

3.1.4.3 Read Status Facility - The IOT instruction IORS = 700314 loads the AC with a word comprised of various device flags and control flip-flops. External devices with assigned status bits use the read status level to gate their device flag onto the corresponding I/O bus line (Figure 3-3). The status word can be displayed in the REGISTER indicators by putting the console switch to status and stopping the computer. Figure 3-4 shows the bit positions associated with the commonly interfaced flags. The functions of the device flags normally interfaced to the IORS (input/output read status) facility are presented below.

Program Interrupt - a 1-bit indicates that the program interrupt control is enabled. A 0-bit indicates that it is disabled. The program interrupt control is automatically disabled upon granting of a program interrupt request.

Tape Reader - a 1-bit indicates that the reader was previously selected and has assembled a character in its buffer for transfer to the AC upon execution of a "read buffer" IOT instruction. This flag is also interfaced to the program interrupt control to request program interruption when the flag goes to the 1 state.

Tape Punch - a 1-bit indicates that the paper tape punch has punched a line of tape relating to the contents of the AC at the time of selection. The flag is also interfaced to the program interrupt control to request program interruption when the flag goes to the 1 state.

Teletype Keyboard - a 1-bit indicates that the keyboard buffer has assembled a character code relating to a struck key. The flag is cleared when the assembled code is read into the AC by an IOT instruction. The flag is also interfaced to the program interrupt control to request program interruption when the flag goes to the 1 state.

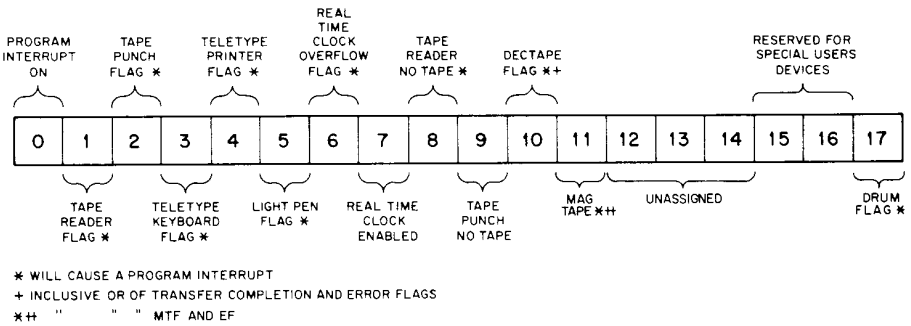


Figure 3-4 IORS Word-Status Bit Assignment

Teletype Printer - a 1-bit indicates that the teleprinter is ready to accept a character code from the AC. The flag is cleared when the teleprinter buffer is loaded and it remains so until the action called by the code has been executed. The flag is then again set to 1. The flag is also interfaced to the program interrupt control to request program interruption when the flag goes to the 1 state.

Light Pen - a 1-bit indicates that the Type 370 Light Pen has detected the presence of illumination, normally a CRT-displayed point. The pen is equipped with a manually operated shutter which should be opened only when the pen is positioned on the face of the CRT display. The flag is also interfaced to the program interrupt control to request program interruption when the flag goes to the 1 state.

Real-Time Clock Overflow - a 1-bit indicates that the real-time clock counter (stored in memory location 000007 of bank 0) has overflowed; i.e., the initialized clock count (in 2's complement form) has been incremented to zero. The flag is also interfaced to the program interrupt control to request program interruption when the flag goes to the 1 state.

Real-Time Clock Enabled - a 1-bit indicates that the real time clock is enabled and incrementing the contents of location 00007 by one at the rate of 60 times per second (or 50 times per second for 50 Hz powered PDP-9 systems). A 0-bit indicates that the real time clock is disabled. The flag is not interfaced to the program interrupt control.

Tape Reader No Tape - a 1-bit indicates that the paper tape reader has detected a no-tape condition and has halted. In the case of a tape break, since the break may be skewed, approximately 12 lines of previously read tape is considered invalid data when the no-tape flag is detected going to a 1. Although this flag is not interfaced to the program interrupt control, it does force the tape reader flag to go to the 1 state and hence request program interruption for the no-tape condition. A program may make use of the no-tape flag by executing an IORS instruction and testing the AC contents prior to each selection of the reader. An alternate method calls for a program-interrupt accessed subroutine to execute the IORS instruction and check the states of the tape-reader and tape-reader-no-tape flags to determine which flag initiated the interruption. While the no-tape flag is a 1, the tape reader will not respond to IOT selection; i.e., the reader is inhibited from reading tape lines. Depressing the FEED button on the tape reader after loading a tape for readin clears the no-tape flag.

Tape Punch No Tape - a 1-bit indicates that the supply of unpunched tape in the internal magazine has been exhausted except for approximately one inch. This length is adequate for punching several characters; it may be used also for splicing purposes. This flag does not request a program interruption. Users making use of this flag must include an execution of the IORS instruction and a test of the AC contents prior to each selection of the paper tape punch.

DECtape - a 1-bit indicates that the DECtape flag and/or the error flag (both contained in the TC02 DECtape control unit) are set. This flag is interfaced to the program interrupt control to request program interruption when the flag goes to the 1 state.

3.2 GENERAL USE OF IOP PULSES AND DEVICE SELECT CODES

The use of the three IOPs is summarized below:

IOP Pulse 1 - Normally used as an I/O skip instruction to test a device flag. May be used as a command pulse, such as to clear a register before loading it but not to initiate either load or read from a device.

IOP Pulse 2 - Usually used to transfer data from the device to the computer or to clear a register. May not be used to determine a skip condition. May be used to transfer data from computer to device.

IOP Pulse 4 - Usually used to transfer data from the computer to the device. May not be used to determine a skip condition or to effect transfer of data from a selected device to the processor.

It is important that the IOT device select codes are unique to each device. When designing a special system, the engineer will note which device codes are already taken by existing peripherals or options and which codes might be used by any future additions to his system. A summary of assigned codes is given in the User Handbook for the computer.

3.2.1 Timing Charts

Figure 3-5 and 3-6 are complete timing charts for non-API program controlled transfers in the PDP-9 and PDP-9/L. When applicable, all signals are measured at the computers.

3.3 PROGRAM CONTROLLED TRANSFERS USING THE API OPTION

The API option extends PDP-9 and PDP-9/L capabilities by providing servicing for as many as 28 I/O devices with minimum programming and maximum efficiency. Its priority structure permits high data-rate devices to interrupt the service routines of slower devices with a minimum of system "overhead." The option permits the device service routines to access directly from hardware-generated entry points, eliminating the need for time-consuming flag searches to identify the device that is causing the interrupt.

The option provides 32 unique channels, or entry points, for the device service routines, and 8 levels of priority. The four higher levels are for fast access to service routines in response to device-initiated service requests. Each of these levels can be multiplexed to handle up to eight devices assigned an equal priority. The four lower levels are assigned to program-initiated software routines for transferring control to programs or subroutines on a priority basis. Four of the 32 channels are reserved for these software levels.

Each device interfaced to the API option specifies (sends) its "trap address" or unique service routine entry point to the processor when granted an API break by the processor. Core memory locations 40_8 through 77_8 are assigned as these entry points. JMS or JMS I instructions contained in these locations provide linkage to the actual service routines.

Of the 28 hardware channels, 3 are assigned internally to the paper tape reader, real-time clock, and optional power-failure detection system. The API interface logic for these devices is wholly contained within the I/O wing of the PDP-9.

Each API priority takes precedence over lower API priorities, program interrupts (PI facility, basic PDP-9), and the main program. The highest priority program segment interrupts lower priority program

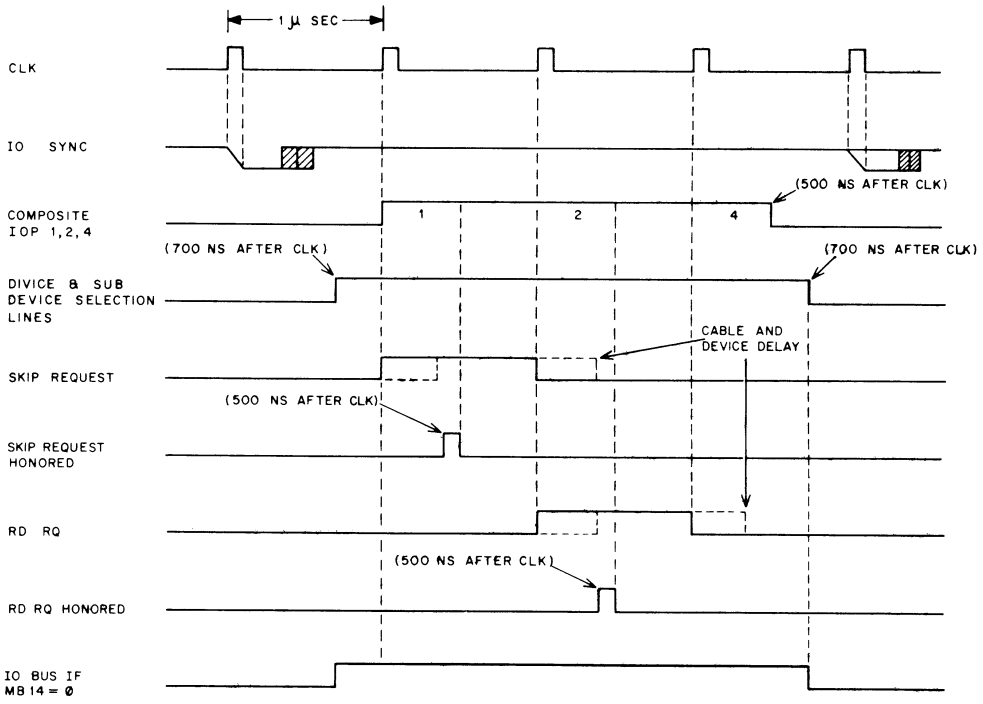


Figure 3-5 PDP-9 Program Controlled Transfer Timing

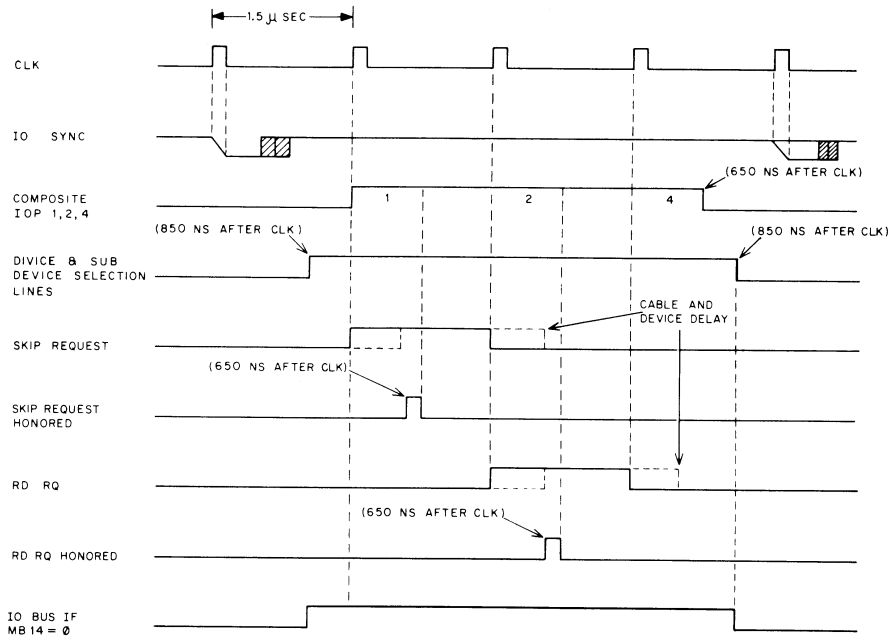


Figure 3-6 PDP-9/L Program Controlled Transfer Timing

segments when activated. Above all of these in priority, the DMA, DCH, and RTC program segments hold highest priority.

The entire API system may be enabled or disabled by a single IOT instruction. With the exception of the paper-tape reader channel, it is not possible to enable or disable a single channel. For a detailed description of API logic in the PDP-9, refer to document number DEC-09-15AA-D.

3.3.1 API Interface Logic

3.3.1.1 API I/O Bus Signals - The I/O bus contains 12 lines unique to the API; these include an API RQ (request), an API GR (1) (grant) and an API EN (enable) line for each of the four levels. Other I/O bus signals used by the API include I/O PWR CLR, I/O SYNC, and I/O ADDR 12-I/O ADDR 17. The API RQ lines are used by the device to request an interrupt from the computer at a particular priority level. The API GR is the computer's response to an API RQ. The API EN signal indicates to a device the status of another device on that interrupt level. (There can be as many as eight devices sharing any priority level.) I/O PWR CLR is used to establish initial conditions, I/O SYNC is used for timing, and the I/O ADDR 12 to I/O ADDR 17 specify the unique entry point or trap address to a device service routine.

3.3.1.2 The W104 Module - DEC makes a double-height FLIP CHIP module, the W104, to handle much of the timing and hardware interface demands of the API. Its equivalent circuit is shown in Figure 3-7.

The W104 serves to establish priorities among devices tied to the same priority level; it also accepts the request for interrupt from the device and implements the necessary timing to place the trap address onto the I/O ADDR lines. The functions of the W104 signal and data lines are described below.

a. I/O Address Lines - Each W104 module contains six address selection lines (pins AJ, AK, AL, AN, AS, AU) which are normally connected to the I/O ADDR lines of the I/O bus to form the trap address. For a standard API device, pin AJ is connected to line 12 (40_8) and pins AK-AU form the channel number. In some cases, trap addresses above 77_8 may be used, although standard PDP-9 peripherals should be restricted to 40_8-77_8. If a single device is required to generate a number of

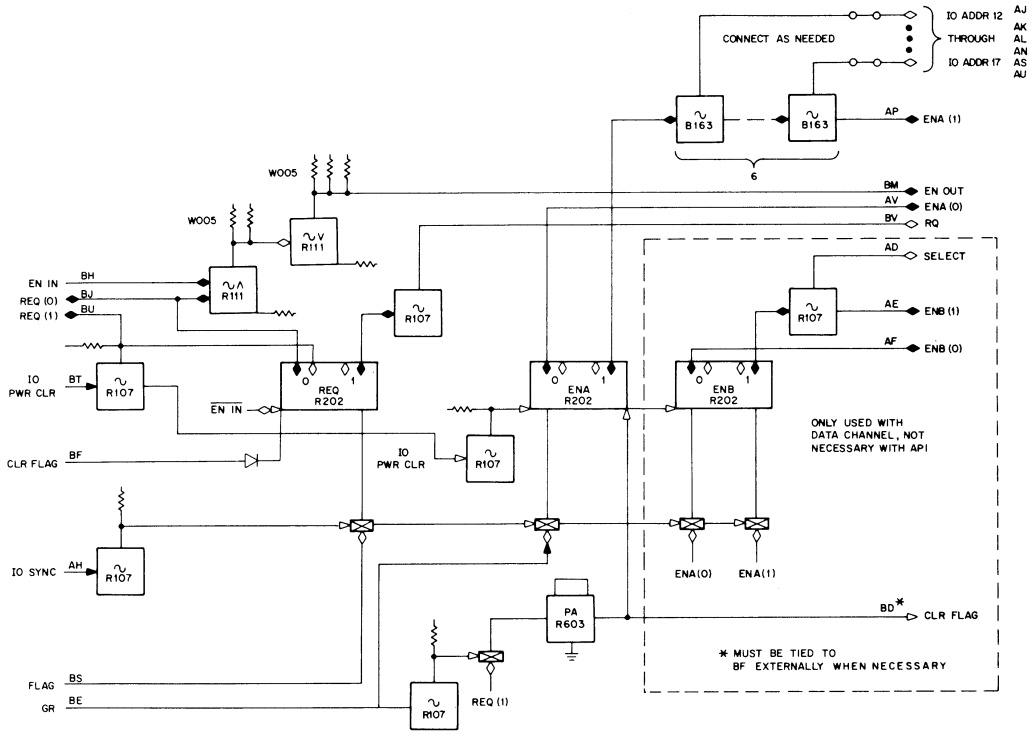


Figure 3-7 Equivalent Circuit of the W104 Module

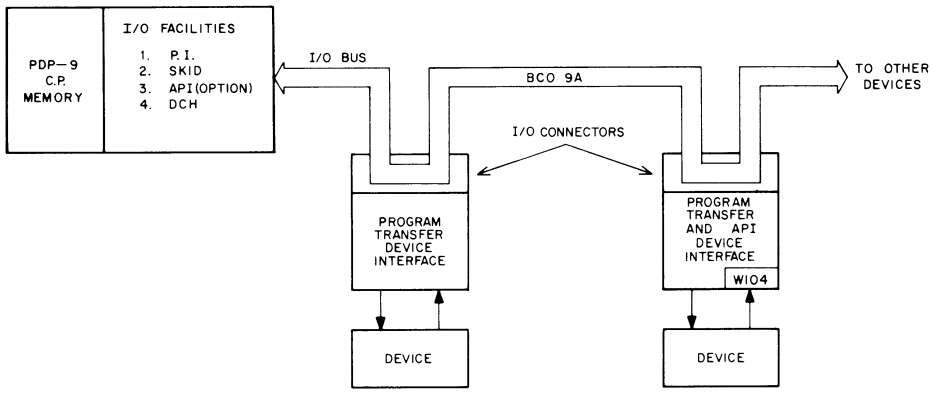
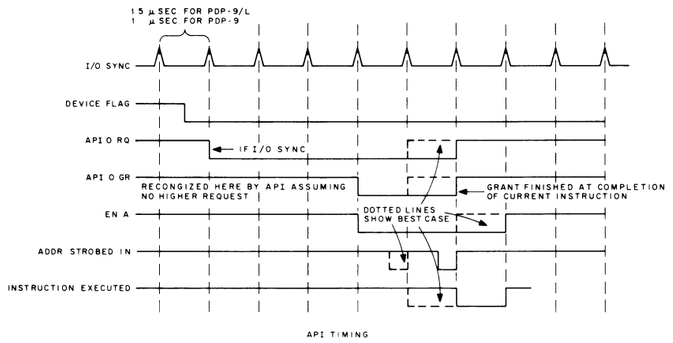


Figure 3-8 Using the API Facility of the PDP-9

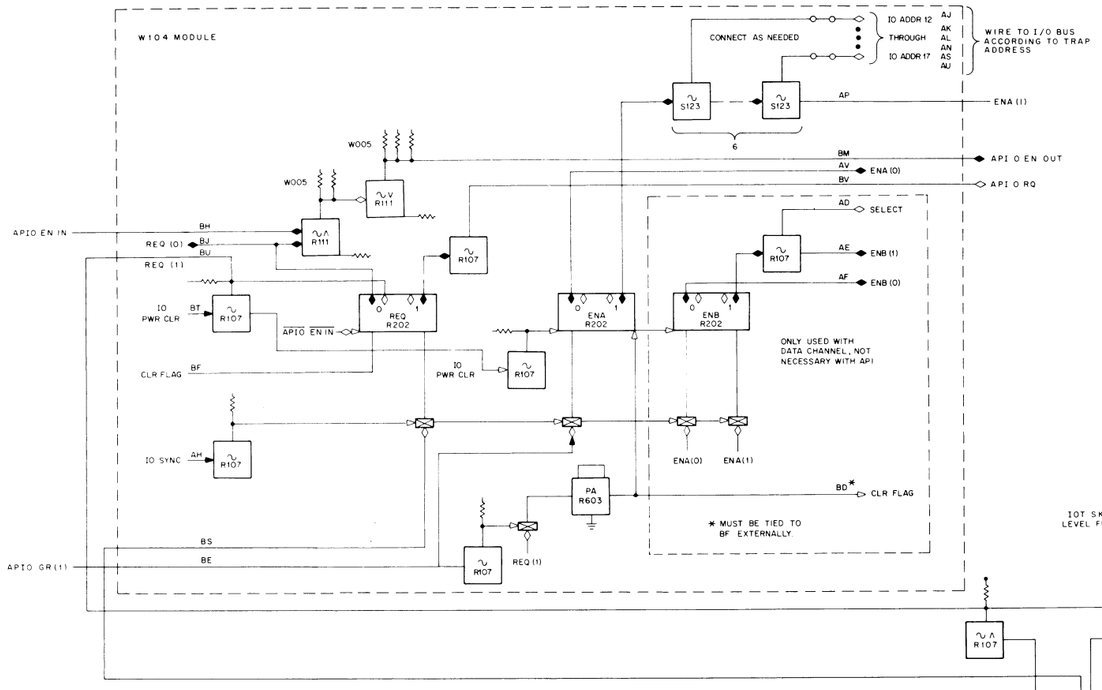
different addresses on the basis of a single flag, the W104 can be used to gate the address from a flip-flop register onto the IO ADDR lines. Figure 3-9 shows an example of this.

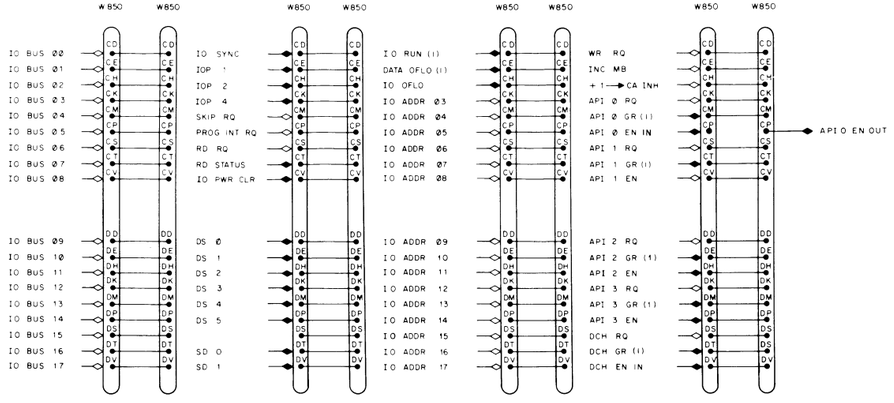
b. RQ Lines - This signal requests an interrupt on level "N" and must be tied to API "N" RQ of the device I/O bus.

c. GR Lines - This signal is tied to the API "N" GR I/O bus signal. This is the computer's response to an API "N" RQ. It is used by the W104 to post the IO ADDR levels and thus indicate its trap address to the computer. The trailing edge of GR generates the CLR FLAG pulse.



API TIMING





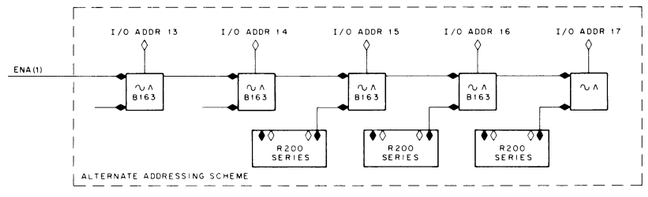


Figure 3-9 Interfacing a Single Flag Device to the API

d. EN IN Lines - When more than one device is tied to any API priority level, the API "N" EN incoming I/O bus signal (refer to Appendix A) is tied to the W104s EN IN line. The outgoing API "N" EN I/O bus signal is jumped to the EN OUT signal of the W104. Thus, if the device closest to the computer requests API on a certain level, its EN OUT signal will prevent all other devices on the same API level from requesting an interrupt.

3.3.1.3 Use of the W104 Module in a Device - Two examples showing the use of the W104 module are presented below. The first deals with a single-flag device while the second explains multiple-flag devices.

a. Single Flag Devices - The device using API connects to the W104 inputs called FLAG, REQ(1), and ENA(1). The other W104 signals usually go to the I/O bus or are not used. Figure 3-9 shows how a device flag is tied to the API lines of the I/O bus through the W104. In this case, API channel 0 is used. Note that the signal API 0 EN, usually jumpered between in-going and out-going cables, is cut and two new signals created; API 0 EN IN at the incoming cable and API 0 EN OUT at the outgoing cable. This was not done for API 1 EN to API 3 EN. Note also, that it is necessary that the PI facility operate when either API is shut off or when the W104 module is not plugged in (for this reason, PI logic is also shown in Figure 3-9). The circuitry shown in Figure 3-9 operates in the following way.

The DEVICE FLAG is set by some device state change, enabling the RQ flop of the W104. The next I/O SYNC pulse issued by the computer after a 400 ns delay will set RQ, which then posts API 0 RQ. The computer, some time later, issues API 0 GR(1) which sets ENA(1). ENA(1) places the trap address onto the IO ADDR lines (in one of the two configurations shown) and the computer executes the instruction of the specified address. The next I/O SYNC pulse after API GR(1) clears ENA. An IOT instruction clears the device flag and thus RQ of the W104. While the RQ flip-flop is set, API 0 EN OUT goes to ground. This signal is passed onto the next device as API 0 EN IN. At ground, it will prevent the next device's RQ flag and any others down the line from setting. A PROG INT RQ will be raised simultaneously with the API RQ. However, API takes priority and the PI will be ignored. If the API is disabled, however, the PI will be raised instead. Removing the W104 module from the configuration (remembering to jumper the API 0 EN I/O cable lines together) leaves the device PI facility intact.

b. Multiple Flag Devices- The hardware shown in Figure 3-10 allows multiple flags to use API and PI facilties similar to the way shown in Figure 3-9. Note that when the last flag is cleared, the request flag of the W104 is cleared.

Each device interfaced to the automatic priority interrupt system must specify its "trap address" or unique entry point to its service routine. Locations 40_8-77_8 are reserved at these service routine entry

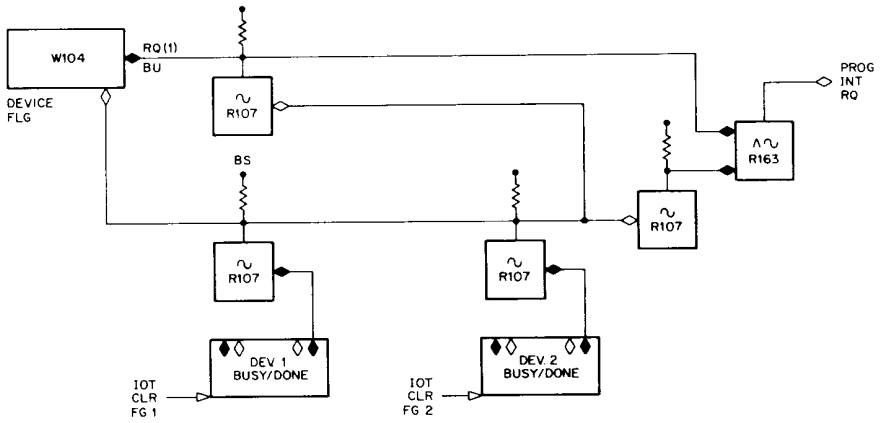


Figure 3-10 Multiple Flags Device Using Both API and PI Facilities

points. Trap addresses and channel numbers are related as follows:

$$(\text{TRAP ADDRESS})_8=(\text{CHANNEL NUMBER})_8+(40)_8$$

Locations 40_8-77_8 should contain JMS or JMSI instructions to provide linkage to the actual service routine.

Table 3-1 shows the relationship between channel number and trap address, the channel assignments for standard PDP-9 I/O devices, and their suggested priority levels. All devices listed in Table 3-1 are connected to the API as shown. The channel number-assignments should remain fixed for software compatibility but priority levels may be changed at the user's option.

Figure 3-11 shows an example of four devices tied to the API (only API-related lines are shown). In this example, the following relationship exists between device number and priority level.

Device	Priority Level
A	3
B	2
C	0
D	2

Table 3-1
Channel and Priority Assignments

Channel Number (Octal)	Trap Address	Standard Device	Suggested Priority Level	IO ADDR Bits 12-17
0	40	Software channel 0	4	100 000
1	41	Software channel 1	5	100 001
2	42	Software channel 2	6	100 010
3	43	Software channel 3	7	100 011
4	44	DECtape (TC02)	1	100 100
5	45	Magtape (TC59)	1	100 101
6	46	Drum (RM09)	1	100 110
7	47	Disk	1	100 111
10	50	Paper Tape Reader	2	101 000
11	51	Clock Overflow	3	101 001
12	52	Power Fail (KP09)	0	101 010
13	53	Parity (MP09)	0	101 011
14	54	Light Pen (34H)	2	101 100
15	55	Card Readers (CR01E, CR02A)	2	101 101
16	56	Line Printer (647)	2	101 110
17	57	A/D (AF01)	0	101 111
20	60	DB99A/DB98A	3	110 000
21	61	Data Link to System 360	3	110 001
22	62	Data Phone (DP09A)	2	110 010
23	63	Reserved for Systems Device		110 011
24	64			110 100
25	65			110 101
26	66			110 110
27	67			110 111
30	70			111 000
31	71			111 001
32	72			111 010
33	73	Teletype LT19		111 011
34	74	Control LT19		111 100
35	75	Unassigned		111 101
36	76			111 110
37	77			111 111

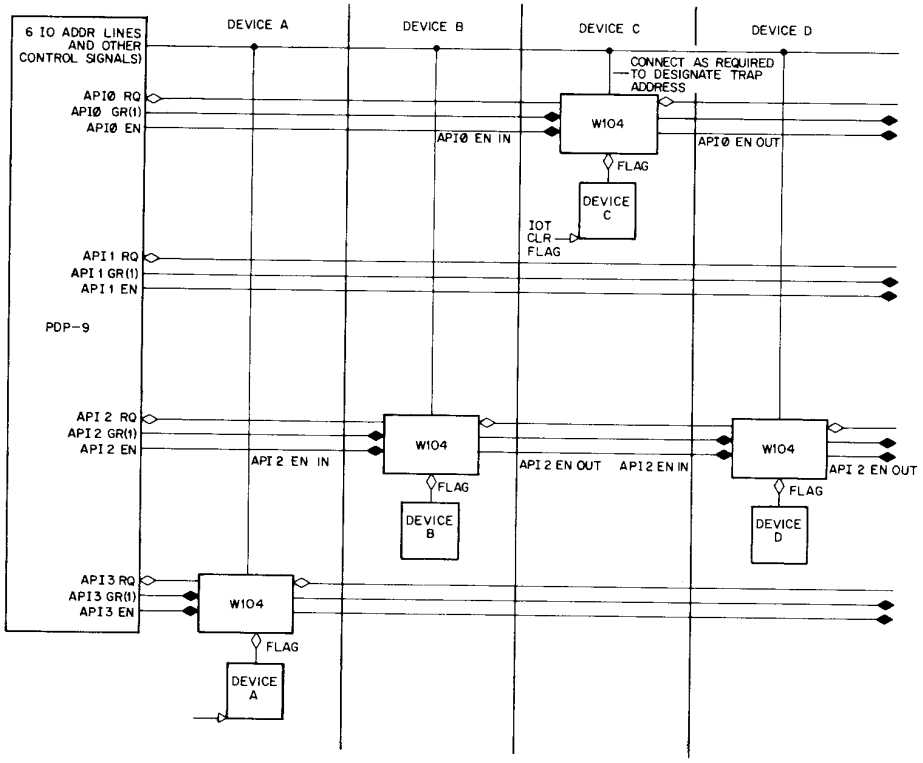


Figure 3-11 Multiple Devices on the Automatic Priority Interrupt System

If all four devices request service simultaneously, they are serviced in the following order: C, B, D, and A. Although B and D are on the same priority level, device B is serviced before D because it is closer to the computer on the I/O bus.

3.4 DATA CHANNEL TRANSFERS

The PDP-9 and PDP-9/L data channels, multiplexed to permit interfaced service to four peripheral devices, provide relatively high-speed interface to the core memory along the I/O bus. Requests for data from I/O devices are honored by the channel at the completion of the instruction in progress at the time the grant signal is issued. The channel is controlled by word count and address registers held in core memory; each request updates these registers, and transfers the data between the memory and the device.

Each of the four devices has a unique pair of sequential core memory registers associated with it. The system software assumes that these are registers 30_8-37_8. These registers must be initialized by the program before the peripheral device may begin transferring data through the channel. The first (word count) register, of lower numerical value, must be even, and is initialized to contain the 2's complement of the number of words to be transmitted. The second (address) register is initialized to contain one less than the first address of the data word block.

These registers may be examined at the end of channel operation to check for final address; if, for example, the device indicates that a short record was read. Peripheral devices normally issue a program interrupt or API request at the completion of the transfer when the word count register has counted up to 0.

The maximum transfer capacity of the channel is between 250,000 and 333,000 words for the PDP-9 (165,000 and 218,000 for PDP-9/L) depending on the mix of input and output rates. Each input transfer steals three processor cycles; each output transfer steals four processor cycles. The latency time

(maximum wait before service is granted after a request is made) under adverse conditions may be as high as 30 μs for PDP-9, or 40 μs for PDP-9/L (see latency section). Special care is necessary, however, when designing software for devices whose channel usage is greater than 50,000 words per second.

Priority among I/O devices making simultaneous requests is determined by their physical placement on the I/O bus; devices closer to the processor have priority over devices further away. The establishment of priority requires that each device quickly propagate an enable signal to the next device on the bus; a special module, the W104 Multiplexer, has been designed for this purpose.

3.4.1 Latency

Since data channel requests are only honored between instructions, the type of instruction in progress determines the waiting time until the interrupt is granted. The following considerations apply:

a. The IOT instruction is noninterruptible. The interrupt request is honored at the completion of the instruction which follows the IOT.

b. The EAE instructions delay interruption until they complete, which may be as long as 17 μs.

c. The XCT instruction is noninterruptible. The interrupt request is honored at the completion of the instruction referenced by the XCT.

d. Lower priority devices wait for the completion of data transfers on the requesting higher priority channel. Hence, if four requests come up simultaneously, the lowest may wait 12 μs for PDP-9, or 16 μs for PDP-9/L, and indefinitely if a higher priority device is taking successive breaks.

Long XCT chains or sequential IOT instructions can lock out channel requests for indeterminate periods of time. These are to be avoided in programs operating devices requiring short latency. EAE instructions requiring more than 12 μs are uncommon, but possible. Unfortunately, requests tend to stack up during these waiting periods, so that lower priority devices must wait even longer. I/O system design must insure that the latency time requirement of each peripheral is satisfied.

3.4.2 Data Channel Interface Logic

3.4.2.1 Device Requirements - Each device connected to the data channel must have the interface hardware outlined below. The first four requirements are essentially the same as those met by devices connected to the program interrupt. They insure that the device hardware may also be checked by maintenance routines using special IOT instructions. Requirements e, f, and g are met by the Type W104 Bus Multiplexer which is strongly recommended for use in the interface. The W104 is shown on Figure 3-7.

a. Each device must have the ability to decode the 6-bit selection code transmitted by the processor on the device selection lines. When selected, the device must be capable of producing internal command pulses in response to IOP pulses transmitted on the bus. The module performing such functions in the peripheral device is called the device selector. Furthermore, the device must have the ability to force selection of the device selector, regardless of the address on the selection lines. The Type W109 Device Selector module possesses this property.

b. Each device receiving output data from the computer must contain gating circuits at the input of the receiving register which are capable of strobing the I/O bus information into the register when triggered by a command pulse from the device selector. In addition, the device must supply a write request level to the channel during the period wherein it is selected.

c. Each device supplying input data to the computer must include gating circuits at the output of the transmitting register which are capable of gating this register onto the I/O bus when triggered by a command pulse from the device selector. In addition, the device must supply a read request level to the channel while it is selected.

d. Each device must contain a request flag (flip-flop) which is set whenever the device is ready to receive (or transmit) another word of information. This flag is normally cleared when the transfer is complete.

e. The device data flag is used to request a break through a synchronizing flip-flop, which drives the request line (DCH RQ). The device data flag must be cleared when the break is granted (DCH GR).

f. Each device must be capable of propagating the enable signal (DCH EN) to the next device to establish priority of devices along the bus in case of simultaneous requests. The next device must be enabled if the current device is enabled and is not itself requesting.

g. Each device must contain the gating circuits necessary to transmit the core memory address of the word count register assigned to the device. The address is transmitted by the selected device upon receipt of the grant signal (DCH GR) from the channel.

h. Each device must contain an "active" flip-flop which controls whether or not the device periodically requests data transfer through the channel. This flip-flop is normally turned on by the program with an IOT instruction and off by the IO OFLO signal transmitted to devices by the channel.

3.4.2.2 Interface Hardware

DCH IO Bus Signals - The I/O bus contains seven wires unique to the DCH. These are called DCH RQ, DCH GR(1), DCH EN, DATA OFLO(1), I/O OFLO, INC MB and +1 → CA INH. Other I/O bus signals used by the DCH include I/O PWR CLR, I/O PWR CLR, I/O SYNC, WR RQ, RD RQ and I/O ADDR 12 through I/O ADDR 17.

The DCH RQ line is used by the device to request a data channel break from the computer. DCH GR is the computer's response to the request.

The DCH EN signal is a -3V level from the computer and is daisy-chained from W104 module to W104 module of each device on the DCH. Each module can ground this level and inhibit any device further down the chain (away from the computer). In this way, priorities for devices are established.

The I/O OFLO line sends a pulse to the device from the computer whenever the WC register overflows (1's complement) during a DCH request.

The DATA OFLO(1) is a 200 ns pulse occurring during an add-to-memory DCH break whenever the sum of the contents of memory and contents on the I/O bus, which must be like signs (2's complement) has an opposite sign.

INC MB is a signal sent to the computer by the device to indicate that the device needs to increment the location it specifies on the I/O ADDR lines.

+1 → CA INH, when grounded, forces the CP to inhibit incrementing the CA during its DCH break.

I/O PWR CLR is used to clear the flip-flop in the device; I/O SYNC is a timing pulse derived from the main computer clock; and RD RQ and WR RQ inform the computer of the transfer direction.

I/O ADDR 12 to I/O ADDR 17 specify the address of the word count (WC) register previously set up by the computer.

The W104 Module - As with the API interface for program controlled transfers, the DCH uses the W104 double-height FLIP CHIP module to handle the timing and hardware demands of the DCH. The equivalent logic circuit of this module is shown in Figure 3-7. The signal lines associated with the W104 module are described below:

RQ Lines - The RQ signal of the W104 is tied to DCH RQ of the I/O bus. When the RQ flop of the W104 is set, a DCH RQ signal asks for a break from the computer.

GR Lines - This signal is tied to DCH GR of the I/O bus. The computer supplies the positive level in response to the DCH RQ. The negative edge sets ENA of the W104 which then gates the B163 onto the I/O ADDR line.

I/O ADDR Lines 12 through 17 - These lines of the W104 are connected to their corresponding signals of the I/O bus when a line corresponds to the code of the address of the CA register in memory.

EN IN and EN OUT Lines - The signal EN IN of the W104 is connected to DCH EN of the input I/O bus cable: EN OUT is tied to DCH EN of the output I/O bus cable. The EN OUT signal then goes via the I/O bus to the EN IN of the next device.

RQ Line - An RQ flag raised at any device causes a ground to propagate down the DCH EN line (away from the computer) and inhibit any other "RQ" flag below the active device, from being set.

I/O PWR CLR and I/O SYNC - These signals are connected to their equivalent on the I/O bus and are used for clearing registers and synchronizing to the computer, respectively.

3.4.3 Data Transfers to and From the Computer

The device flag is raised asynchronously by some state change in the device control. This flag is

synchronized by the W104 Data Multiplexer, which requests a data channel interrupt through the DCH RQ line. If more than one device on the channel is requesting a transfer to or from the computer, the multiplexer insures that the lower priority device is shut out by driving its enable (DCH EN) input line to ground (disable state). This request is recognized by the processor and, at the end of the current instruction, control is relinquished to the channel hardware.

Channel hardware begins operation by identifying the device requesting service. This is done by issuing a grant signal (DCH GR) to all connected devices. Upon receipt of the grant signal, the device which supplied to the DCH RQ transmits the core memory address to be incremented and rewritten. If, in this word count updating procedure, the count reaches 0, an I/O overflow signal is set to all devices. The device hardware interprets the overflow signals as a shut down command. No further transfers are made until the device is reinitialized by the programmer.

After incrementing the word count register, the channel reads the next sequential word from memory. This is taken as the current address register, which is incremented and rewritten into memory. The updated value is used to specify the location into (from) which the data is to be transferred.

3.4.3.1 Operations Unique to Reading - If the read request (RD RQ) signal is present and the write request (WR RQ) signal is not present, the transfer is taken as an into-computer data transfer (refer to Figure 3-12). At the beginning of the second (current address) cycle, IOP2 is issued. At this time the device is expected to gate its data onto the I/O bus for subsequent read-in by the channel. At the end of the second cycle, the data is read into the AR register. The third cycle stores the data word in the memory. This ends the sequence and the channel relinquishes control to the processor.

3.4.3.2 Operations Unique to Writing - If the write request (WR RQ) signal is present and the read request signal is not present, the transfer is taken as an out-of-computer data transfer (refer to Figure 3-12). During the middle of the third (data) cycle, the channel places the requested data onto the I/O bus for subsequent read-in by the device. The data remains available until the middle of the fourth cycle. At the beginning of the fourth cycle, IOP4 is issued instructing the device to clear its buffer and to gate the data on the bus into its receiving register. DCD gates must be used. The sequence then ends and the channel relinquishes control to the processor.

3.4.4 Expanding the DCH to Eight Devices

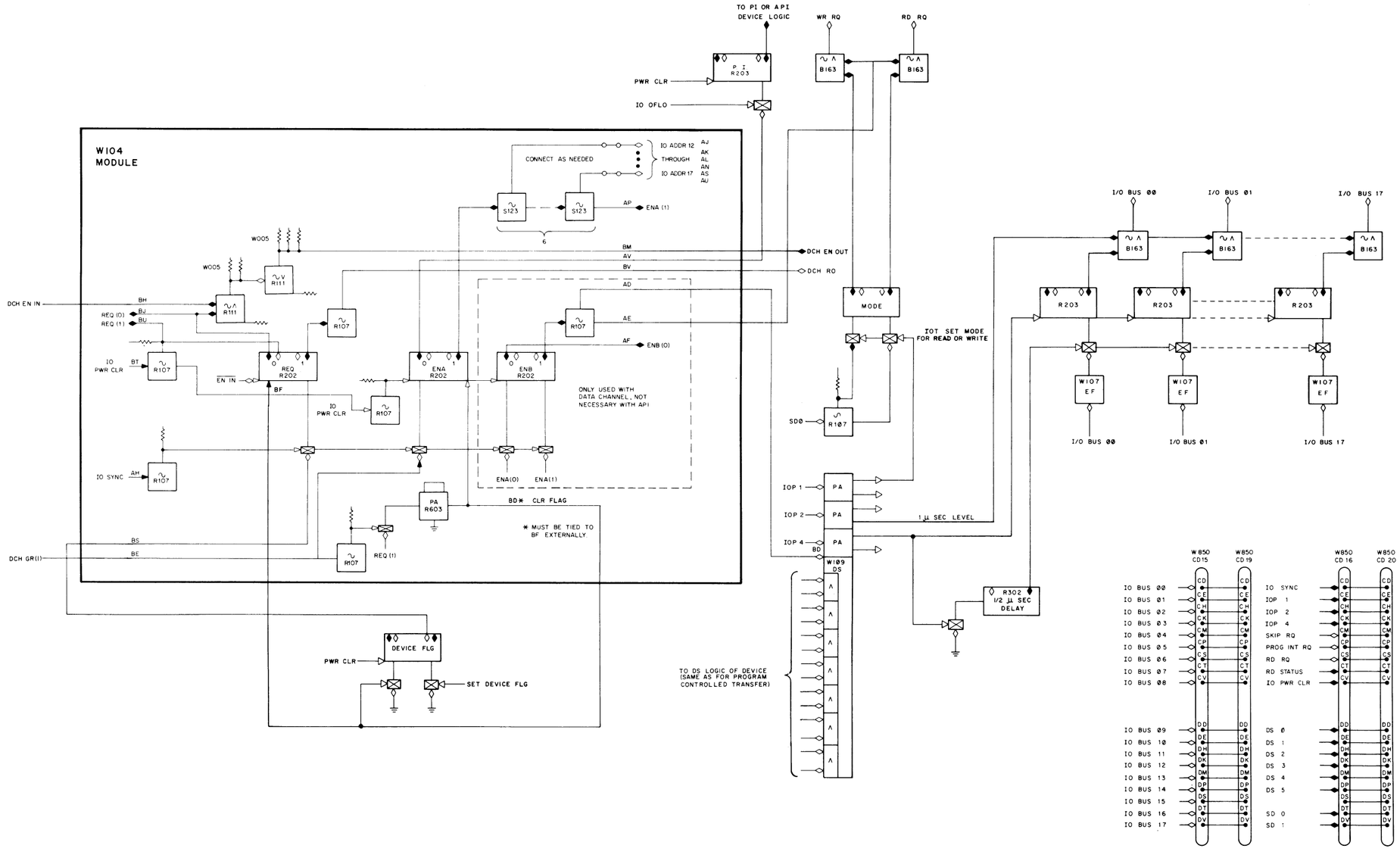
The number of devices connected to the data channel is limited by the combined transfer rate capability and the propogation delay of control and data signals. The most critical delay is that of the DCH EN. Approximately 600 ns are available between I/O SYNC and DCH GR during which DCH EN must be able to propogate through the W104 modules in all DCH devices. If only four devices are used, (requiring a total of four W104 modules), these is no propagation problem for I/O cable lengths of up to 50 feet. Furthermore, the system software has set aside WC and CA addresses for the four devices. If the total I/O cable length is less than 50 feet, up to eight W104s could be added to the data channel. In this case, the WC and CA registers for these extra devices would have to be assigned by the system designer.

3.4.5 Interface Design

The interface shown in Figure 3-12 can be used to either read or write from the computer into its data buffer. If the MODE flip-flop is set to enable the RD RQ gate, the computer will read the contents of the device register into the core address location CA+1. If MODE is set to enable the WR RQ gate, then the computer will write into the device data register the memory word contained in core memory location CA+1. The circuit operates as follows:

a. The MODE is selected by IOT instruction.

b. A change in state of the device (not shown) sets DEVICE FLAG, which enables the RQ flag of the W104. The pulse I/O SYNC sets RQ. The computer responds with DCH GR, setting ENA and thus gating onto the I/O ADDR lines the WC address. ENA(1) enables ENB which is set with the reset I/O SYNC pulse. The SELECT line goes to ground, enabling the W109. Meanwhile, the trailing edge of DCH GR produces CLR FLG which resets the DEVICE FLG. IOP 2 is issued (for a RD RQ) and the data buffer gated onto the bus. If a WR RQ was placed, the IOP4 is issued on the reset cycle. The register is cleared on the trailing edge and loaded 1/2 μs later by the delay. DCH timing diagrams are shown in Figure 3-15 and 3-16.



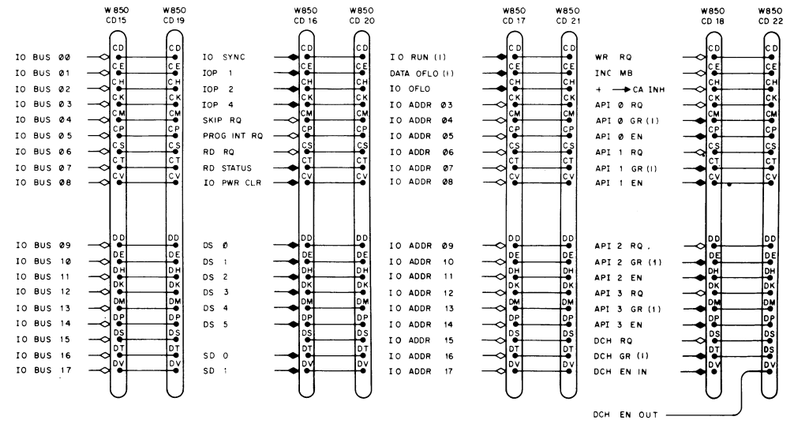


Figure 3-12 DCH Interface Logic for Reading and Writing

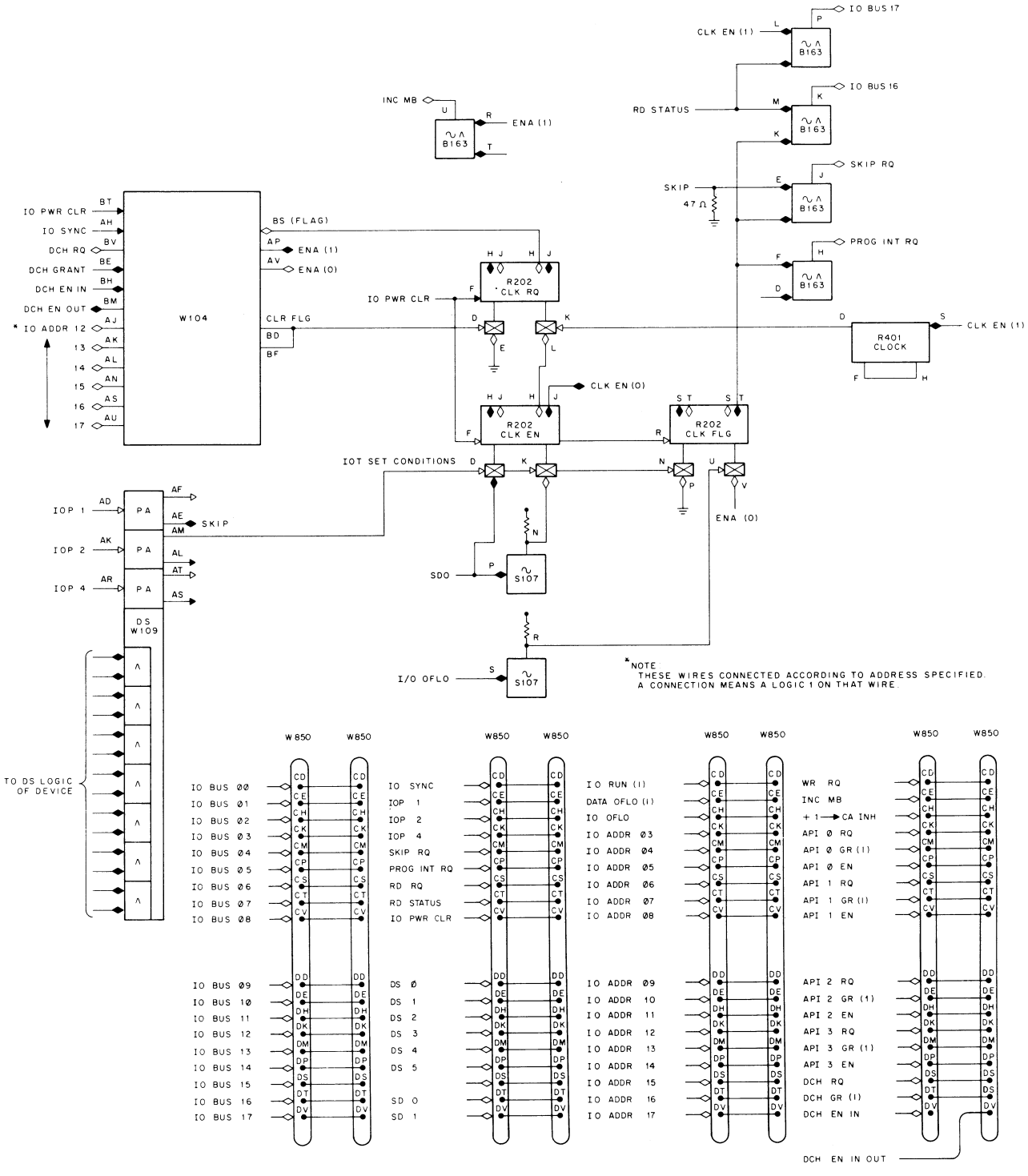


Figure 3-13 DCH Clock Using Memory Increment

c. If an I/O OFLO occurs, the PI flag, enabled by ENB, will be set. The computer and device are then informed that the block has been transferred.

3.4.6 Other DCH Features

3.4.6.1 Incremented Memory - The memory increment operation (Figure 3-13) is the first cycle only of a channel transfer. The word specified on the I/O ADDR lines is incremented. Maximum rate is 250,000 increments per second on the PDP-9 or 165,000 on the PDP-9/L, unless some latency condition interferes. A typical interface circuit using the increment memory facility is shown in Figure 3-13 Here, a clock pulses the device CLK RQ flag which, in turn, enables the W104. A DCH RQ is made, ENA is set by DCH GRANT and INC MB is gated onto the bus, along with the I/O ADDR lines. The location specified by the W104 on the I/O ADDR lines is incremented. If the specified register has reached, and overflow signal (I/O OFLO) sets CLK FLG which causes a PROG INT RQ, thus informing the computer of the overflow condition. Otherwise, the machine resumes normal operation until the next DCH RQ.

3.4.6.2 Add-to-Memory - The add-to-memory operation (Figure 3-14) is a combination of reading and writing. The data transmitted by the device is added to the word read from memory, and rewritten

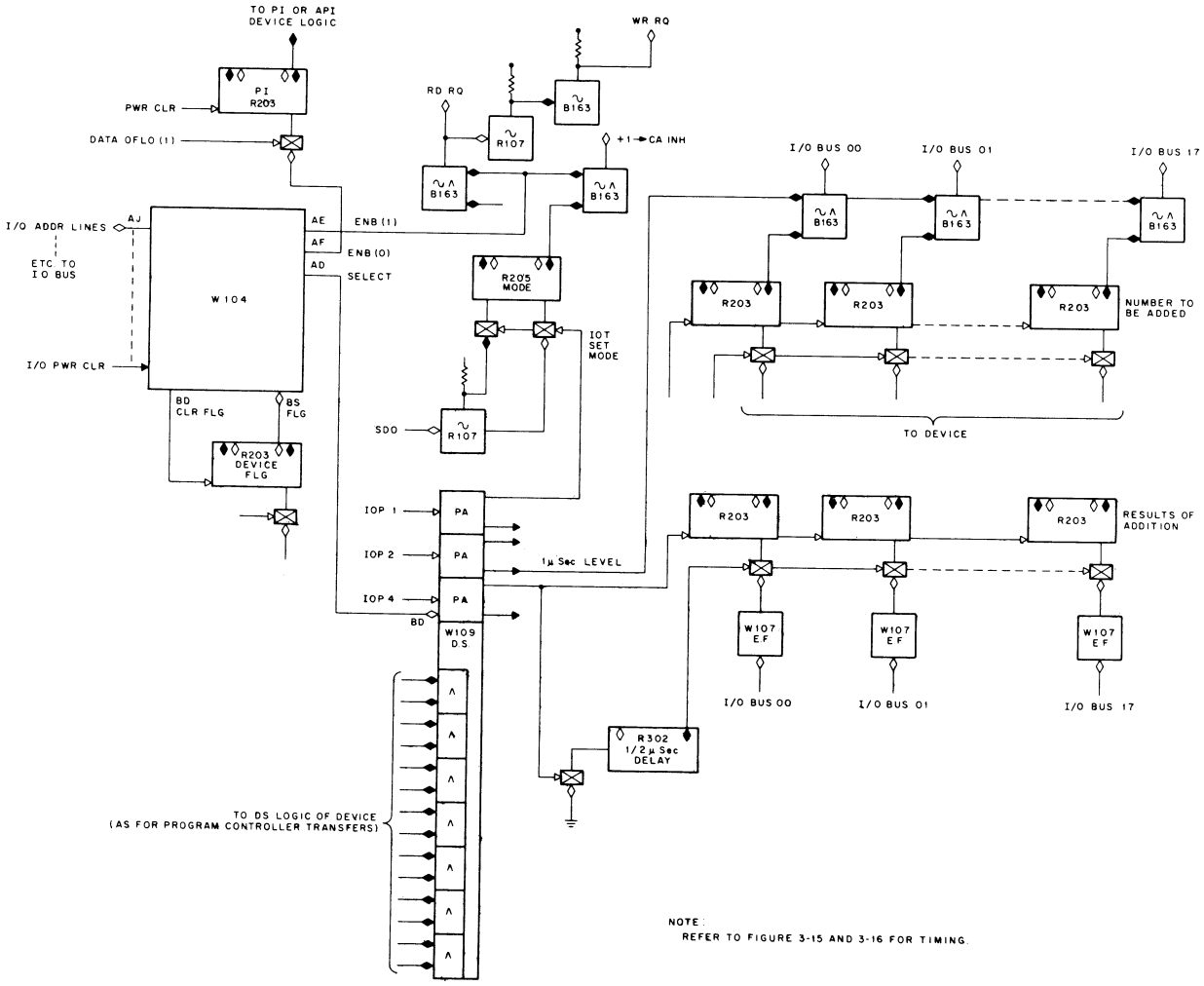


Figure 3-14 DCH Add-to-Memory Circuit With +1 →CA INH Mode

into memory. The sum is transmitted back along the I/O bus. Four cycles are required.

This is a 2's complement operation - the contents of the MB (and thus the location addressed) are assumed to be in 2's complement form.

The circuit shown in Figure 3-14 does not differ much from an ordinary DCH transfer. A DCH RQ is made. Both RD RQ and WR RQ are sent to the computer. A MODE flip-flop can be set to inhibit incrementing the CA contents during the third cycle. (For averaging, IOP 2 is used to gate the data to be added onto the bus and IOP4 strobes the sum into the second register.) If DATA OFLO(1) occurs, a PI is set.

3.4.6.3 +1 → CA INH - A feature that inhibit CA incrementing is extremely valuable when running diagnostics. By asserting the +1 → CA INH signal, the computer will continuously cycle around the same CA location during DCH breaks, since this prevents a one from being added to the CA register.

3.4.7 Standard Core Register Assignment for DCH

Table 3-2 shows the existing core register assignments for standard devices using DCH.

Table 3-2
Standard Core Register Assignment

Device	Word Count	Initial Address
DECtape	30	31
Magtape	32	33
Interprocessor Buffers	22, 23	24, 25
Not presently assigned	36	37

3.4.7.1 DCH Timing - Figures 3-15 and 3-16 indicate the timing of all DCH IO signals in the PDP-9 and PDP-9/L, respectively. These timing charts assume no latency after a DCH RQ is posted.

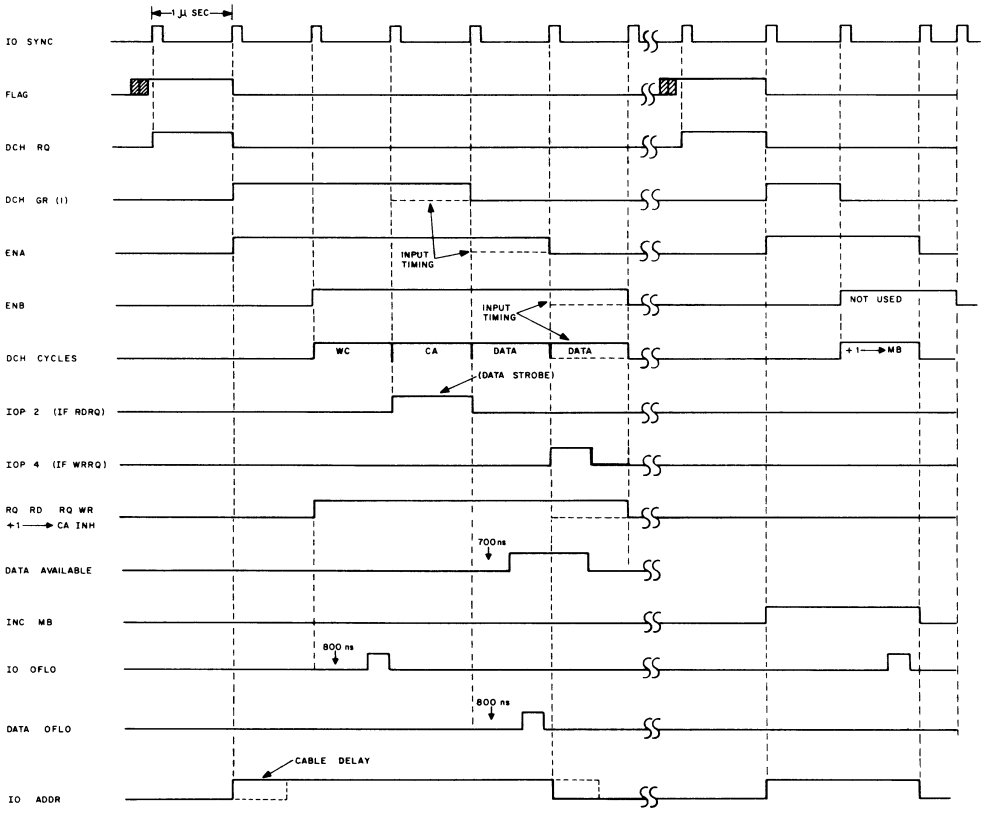


Figure 3-15 DCH IO Timing in the PDP-9

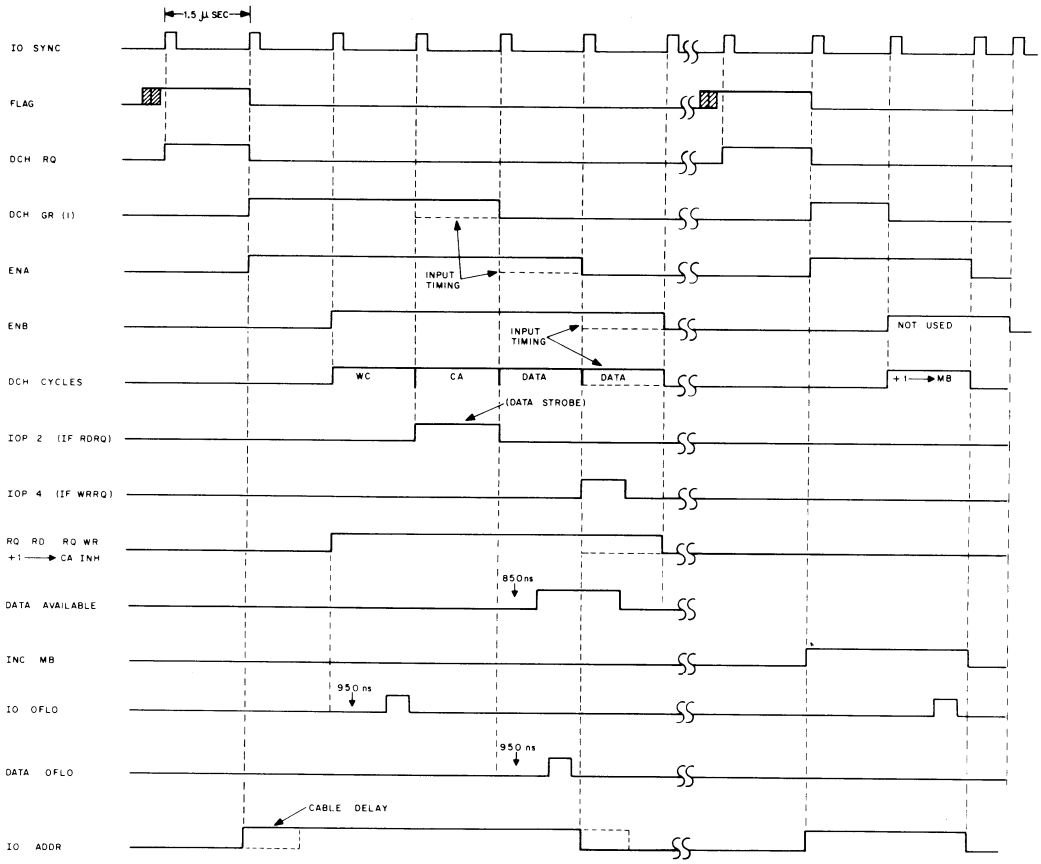


Figure 3-16 DCH IO Timing in the PDP-9/L

CHAPTER 4
DIRECT MEMORY ACCESS CHANNEL OF THE PDP - 9

The direct memory access (DMA) channel permits channel-interfaced devices to directly access system memory locations for the purpose of entering or retrieving data. DMA channel devices effect their data transfers by stealing memory cycles from the central processor (CP). A DMA request for access to memory always has priority over a CP request. The maximum data transfer rate for the DMA channel is 1×10^6 words per second.

While the CP is cycling without accessing memory (as in the execution of EAE arithmetic, EAE data shifting, or IOT instructions following the fetch of such instructions from memory), DMA and CP operations overlap; i.e., no time is lost to the CP by DMA requests for access to memory. Where the operations do not overlap, the CP operation is suspended until the DMA channel frees memory. The design of the PDP-9 system prohibits more than one memory bank of an expanded system from being active at any one time.

The Type DM09A Adapter-Multiplexer, offered as a standard PDP-9 option, is a compatible high-speed interface by which up to three devices may be multiplexed to the DMA channel. Although users may design and fabricate an interface for one device, the relative low cost and the additional benefit of DMA channel expansion make it a valuable addition to a PDP-9 system. The DM09A option is described later in this chapter.

4.1 DMA INTERFACE SIGNALS

Each memory bank of a PDP-9 system contains an input multiplexer which permits both the CP and a DMA channel device to gain access to memory locations. This multiplexer includes a synchronizer and priority system to assure that a device request for memory access will be granted if the CP and the device simultaneously request a memory cycle.

The CPs memory buffer (MB) register outputs (conveying addresses and data) are bused from memory bank to memory bank when they enter one part of the memory input mixer. The channel interface MB outputs are similarly bused to each memory bank and enter a second part of the mixer. The sense amplifier outputs from the memory banks are also bused together and drive both the CP and the channel interface.

The input mixer gates are strobed into the memory address (MA) register at the beginning of the read-half-cycle and are connected to the memory drivers during the write-half-cycle. An external device interface must provide data during the write-half of a normal read/restore memory cycle. Approximately 200 ns are available to receive and return the sense amplifier signals during a typical read/restore memory cycle.

The following signals constitute the DMA interface to the PDP-9 memory system. They consist of signals supplied by memory and signals which must be supplied by the appropriate channel control (DM09A or equivalent, see Figure 4-1).

AM RQ

Signal level sent by channel control to request a memory cycle. Ground level for assertion, -3V otherwise.

AM SYNC (1) B

Signal level returned to channel control by memory, signifying acceptance of cycle request. At ground level for assertion, -3V otherwise.

Clock

Clock pulse train of 120 ns, negative-going pulses. Sent by memory to synchronize internal operation of channel control to system timing. The time between pulses is the same as the processor cycle time.

AM GRANT

Negative-going 120 ns pulse sent by memory to channel control. Normally, the pulse is used to place device-supplied address word on channel control data lines for input to memory MA register. It may also be used to stop the transmission of the data word of the previous DMA transfer if successive requests are being made.

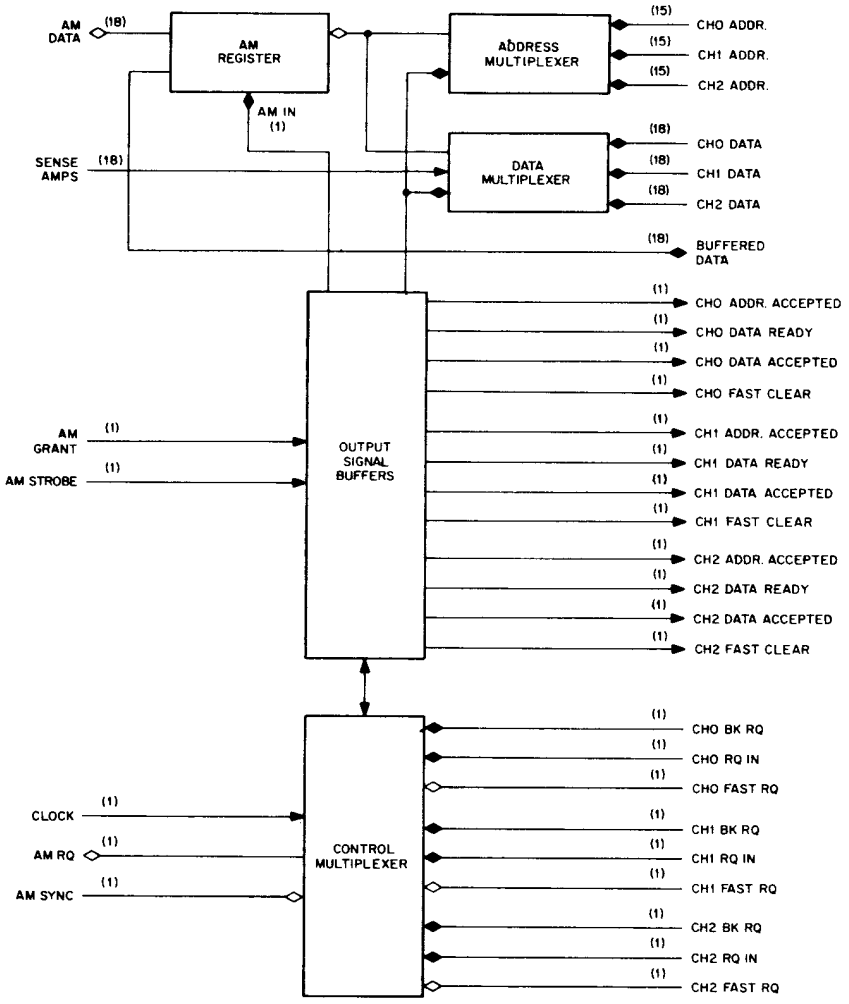


Figure 4-1 DM09A Option Block Diagram

AM STROBE

Negative-going 120 ns pulse sent by memory to channel control. Normally, pulse is used to place lines for input to previously addressed memory location. It may also be used to terminate the transmission of the address via the channel control data lines.

AM DATA

18 data lines convey device-supplied address and data words from channel control to memory. -3V for 0-bit, ground for 1-bit. Channel control must bus drive these lines to ensure signal integrity at memory.

Sense Amplifiers

18 data lines convey data word from previously addressed memory location to channel control. 320 ns negative-going pulses from the memory sense amplifiers. Negative pulse (-3V) indicates 1-bit, ground for 0-bit.

4.2 DM09A OPERATION

The DM09A Adapter-Multiplexer is a convenient interface through which up to three devices may gain access to memory locations via the DMA channel. The option satisfies the interface requirements of the channel, establishes a relatively simple interface for the devices, and allocates priority of service among the devices. The DM09A is designed to transfer data to memory at high speed (1 μs transfer time) and to devices at either of two speeds, depending upon the operational characteristics of their interface logic circuits. Devices having 10 mHz logic should request the fast (1 μs) transfer rate; devices having lower speed logic will operate at the slow (3 μs) transfer rate, (devices interfaced to the PDP-7, the PDP-9's predecessor, are typical of the latter category). The slow speed applies only to the DM09A and the affected device. Regardless of the transfer mode and direction, the DMA channel steals only one memory cycle per each data transfer.

Figure 4-1 is a simple block diagram of the DM09A, showing the major elements of the option and the interface signal lines to the memory bank(s) and to the devices.

Device signals supplied to the DM09A have the following characteristics:

CHX BK RQ

-3V for assertion, otherwise at ground

CHX RQ IN

-3V for device-to-memory transfer, ground for memory-to-device transfer

CHX DATA

-3V for 1-bit, ground for 0-bit

CHX ADDR

-3V for 1-bit, ground for 0-bit

CHX FAST RQ

-3V for slow mode transfer (to device only), ground for fast mode transfer.

Signals supplied by the DM09A to interfaced devices have the following characteristics:

CHX ADDR ACCEPTED

Negative-going 320 ns pulse. Occurrence signifies that device-supplied address has been strobed into memory system MA register.

CHX DATA READY

Negative-going 320 ns pulse. Occurrence signifies that data is present in AM register for entry into device buffer register. Pulse may be used to strobe the data in.

CHX DATA ACCEPTED

Negative-going 320 ns pulse. Occurrence signifies that device-supplied data word has been strobed into addressed memory location.

CHX FAST CLEAR

Negative-going 320 ns pulse. Occurs when DM09A is synchronized to memory. It should be used to clear device request. This pulse is generated for fast mode transfers only.

BUFFERED DATA

18 data lines supply data word read from device-addressed memory location in memory-to-device DMA transfer. -3V for 1-bit, ground for 0-bit.

The following discussion and the timing diagrams (Figures 4-2 and 4-3) serve to illustrate the operation of the DM09A and the manner in which devices must function to make use of the DMA channel.

A device can be initialized by program controlled transfers to indicate the direction of data transfer, the number of words to be transferred, and the address of the initial memory location which is to deliver or receive the first data word. A device flag can then be set to place -3V on the associated break request line (CHX BK RQ). If the DM09A is not currently active, the break request initiates the transition of the adapter-multiplexer request (AM RQ) to ground to request a memory cycle. The return of a ground level on the AM SYNC (DM09A synchronizing) line signifies that the memory system has accepted the DMA request for a cycle.

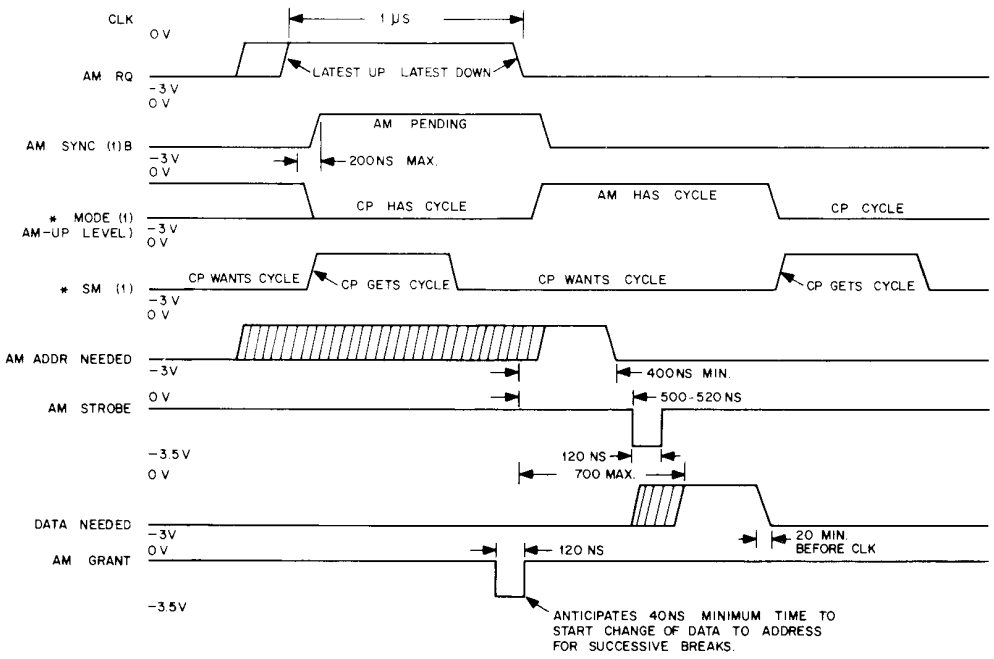


Figure 4-2 DMA Synchronization Cycle, Timing Diagram

Synchronization of DMA requests occurs at the beginning of the memory cycle preceding the cycle in which the data transfer is to take place. Thus, the maximum waiting time for the DMA channel is 2 μs where the first μs is the interval in which the device flag and the AM RQ can come up and the second μs is devoted to synchronizing the DMA. The synchronizing action also blocks processor access of memory to assure DMA priority access.

In a fast mode transfer, following the AM SYNC signal, the DM09A generates the CHX FAST CLEAR signal to clear the device flag and thus the CHX BK RQ line. This action affords another device or the active device the opportunity to anticipate completion of the data transfer and initiate another break request for successive data transfers if the respective device is capable of a 1-μs data transfer rate. In the case of output (to device) transfers at the slow rate, the CHX ADDR ACCEPTED signal (described below) serves to clear the device flag. Successive requests are not permitted for slow mode transfers; i.e., an active device or other DMA device must wait at least one memory cycle following a slow mode request before another slow mode request will be honored.

The device-supplied address (and data word, if request is for a device-to-memory transfer) must be present on the CHX ADDR and CHX DATA lines at the time of the break request. The trailing edge of AM GRANT generates AM IN to place the address in the AM register and, thus, on-line for entry into the memory address (MA) register of the PDP-9 memory system. Shortly thereafter, the DM09A generates the CHX ADDR ACCEPTED signal which tells the device that the address has been entered in memory. The device may use this signal to clear its address register or to setup the next address if successive requests are to be made. For a slow mode device, the CHX ADDR ACCEPTED signal occurs at an opportune time to clear the device request flag.

The AM STROBE signal occurs midway into the cycle, or 500-520 ns after the start of the transfer. If the CHX RQ IN line is at -3V (signifying a device-to-memory transfer), AM STROBE generates AM IN to enter the device-supplied data word in the AM register and, thus, on-line for entry into the addressed memory location. If CHX RQ IN is at ground potential (signifying a memory-to-device transfer), data present on the sense amplifier output lines are gated through the data multiplexer to the AM register.

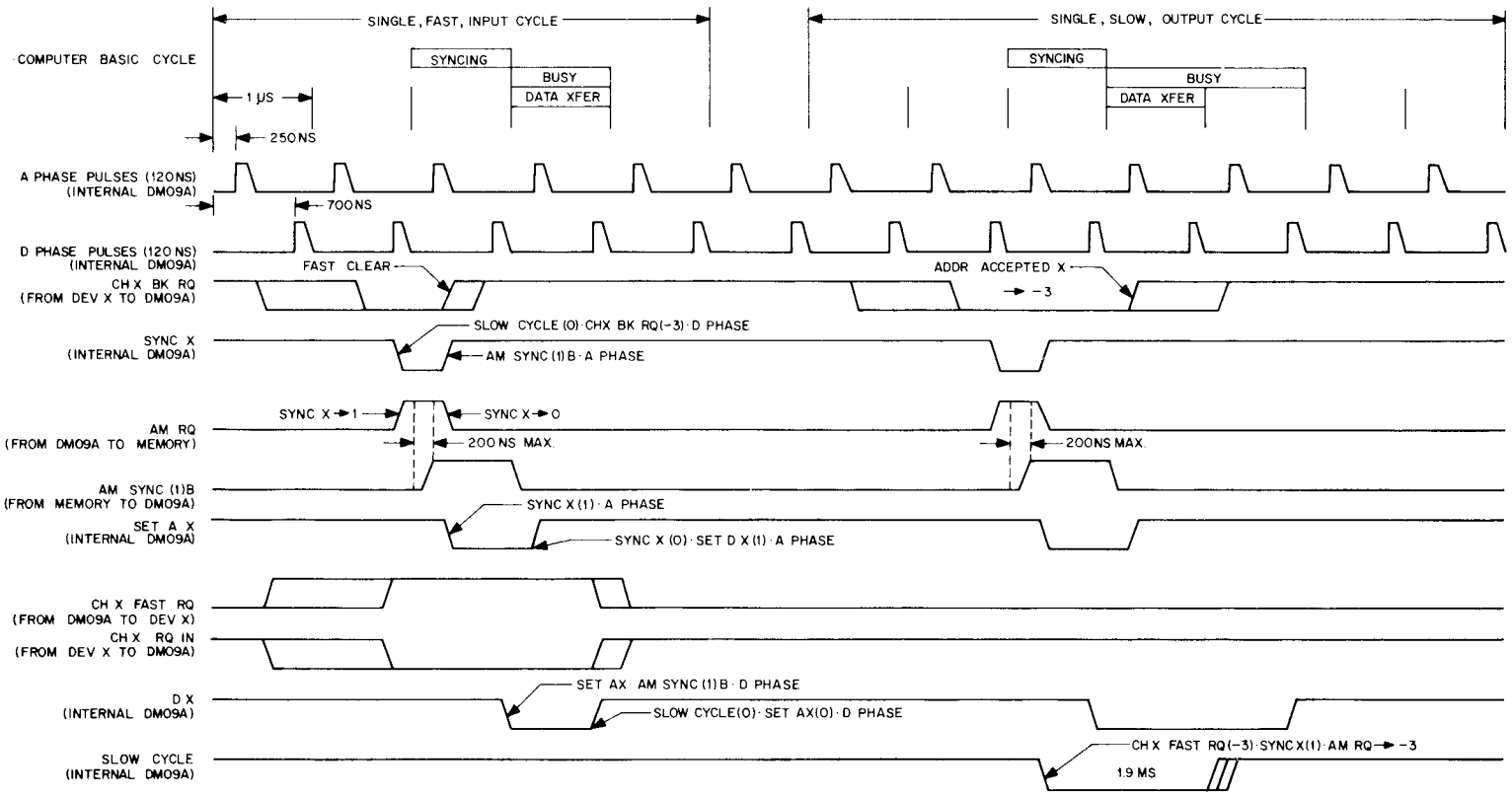


Figure 4-3 DM09 Data Cycle Timing Diagram

For a device-to-memory transfer, AM STROBE enters the contents of the AM register in the memory location previously addressed by the device address word. The DM09A then generates the CHX DATA ACCEPTED signal which signifies to the device that its data word has been entered in memory. CHX DATA ACCEPTED is generated only when a data transfer is made from the device to memory. The device may use this signal to clear its data buffer in preparation for a successive DMA transfer.

For a memory-to-device transfer, AM STROBE causes the DM09A to generate the CHX DATA READY signal, which tells the device that a data word is present on the buffered data lines at the output of the AM register. The device must read this data into a buffer register within 300 ns.

The CLK line supplies buffered clock pulses to the DM09A for the purpose of synchronizing its internal operations to those of the memory system.

In the fast mode, if a device flag (either that of a currently active device or another DMA device) initiates a CHX BK RQ after AM SYNC time but prior to AM GRANT time, successive DMA breaks will be granted.

4.2.1 Interfacing To The DM09A

External devices are interfaced to the DM09A option through one of three available cabling sections each of which contains the cable connectors specified below. These cables must be ordered with the external device option (not the DM09A) and cannot be more than 50 ft long.

2 - cables (W031 to W031) variable length - 18 AM Data Signals

2 - cables (W031 to W031) variable length - 18 Device Data Signals

2 - cables (W031 to W031) variable length - 15 Device Address Signals

1 - cable (W021 to W031) variable length - 7 Control Signals

When interfacing to the DM09A, the following procedures are suggested.

a. All address, data, and control request levels should be interfaced to the DM09A through Type R650 Bus Drivers.

For devices that have already been designed and do not follow the above suggestion, the DM09A option contains a number of prewired clamped load modules (Type W005). These clamped loads are used to terminate collector driven lines when necessary (no clamped loading in external device logic). One 5 mA clamped load is available for each address line, data line and all control levels of the three devices which can be interfaced to the DM09A. Therefore, the user may insert these optional clamped load modules as is necessary for his system.

b. Devices interfaced to the DM09A option should delay their request for a data transfer until their address (and data for an input transfer) has had time to settle on the cable lines, especially if the device is connected to the DM09A through long cable lengths.

c. Devices operating in the fast transfer mode must use the CHX fast CLR pulse to lower its RQ line and this must be accomplished within 300 ns to prevent multiple transfers.

d. When a device requests multiple fast mode transfers at a 1 mc rate, it is suggested that the CH X fast CLR pulse be gated off at the device so that the CH X BR RQ level is never removed until the last word has been transferred (see Timing Diagram in Section 3.4).

e. Negative pulses (120 ns and 320 ns) from W612 Pulse Amplifiers in the DM09A should be terminated with 100 ohms to ground. Collection driven levels should be terminated with 10 mA clamped loads.

f. Where the connector cable exceeds 15 ft, interface levels from B123 flip-flops, collector driven lines, and R650 Bus Drivers should be terminated with G795 modules.

4.2.2. DM09A Master Drawing List

The following table lists the DEC drawings for the DM09A.

Table 4-1
Engineering Drawings

Drawing Number	Title	Drawing Number	Title
C-UA-DM09-A-0	Unit Assembly	D-ML-DM09-A-4	Utilization Module List
A-PL-DM09-A-0	Parts List	A-PL-DM09-A-4	Module Parts List
C-AD-7005394-0-0	Busing Schedule	A-CP-DM09-A-5	Component List
A-PL-7005394-0-0	Parts List	D-BD-DM09-A-6	DM09A Block Diagram
D-BS-DM09-A-1	DMA Adapter Multiplexer Control	D-FD-DM09-A-7	DM09A Flow Diagram
		D-TD-DM09-A-8	DM09A Timing Diagram
D-BS-DM09-A-2	AM Register	D-CD-DM09-A-9	DM09A-Memory Interface
D-CD-DM09-A-3	Cable Diagram	K-WL-DM09-A-9	Wiring List Type DM09-A-

4.2.3 Summary of Data Transfer Rates and Latency Times

The data rates, the latency times (i.e., the time which a device must wait before its request for service is answered), and the representative degrees of efficiency for the PDP-9 and PDP-9/L modes of I/O service are presented in Table 4-2. The "direct" mode refers to program controlled transfers made to or from a single device without interruption by other I/O facilities.

Table 4-2
Data Transfer Rates and Latency Times

Mode	Data Rate Maximum/Typical		Latency Maximum/Typical		Efficiency
	PDP-9	PDP-9/L	PDP-9	PDP-9/L	
Direct	100 kHz	66 kHz			10%
PI	25 kHz/1 kHz	16.5 kHz/ .66 kHz	45 μs for one device 100+μs for two devices/ -100 μs	67.5 μs for one device 150+μs for two devices/150 μs	2%
API	35 kHz/ 10 kHz	23 kHz/ 6.6 kHz	30 μs/50 μs	45 μs/75 μs	3%
DCH	250 kHz/ 50 kHz	166 kHz/ 33 kHz	20 μs/5 μs	30 μs/7.5 μs	25%
DMA	1 MHz	Not Available	2 μs	Not Available	100%

CHAPTER 5
GENERAL WIRING RULES AND SUGGESTIONS

5.1 TYPICAL WIRING

In building logic assemblies the wiring interconnecting the logic modules forms an important part of the logic. Improper wiring may lead to unreliable operations of the logic. DEC logic will generate waveforms whose rising edges contain frequencies over 100 MHz. At these frequencies the inductance, mutual inductance, capacitance, and transmission line properties of the wiring become noticeable. To avoid potential problems, the following rules and guidelines are provided.

a. The propagation delay of typical wiring is 1.5 ns/ft (4.5 ns/m). Although this delay is usually small in comparison with gate delays, it is often significant when overshoot and reflections are considered.

b. The current carrying capacity of a wire is only V/Z_0 until the wave (change) has propagated along the wire three times (4.5 ns/ft, 13.5 ns/m). Typical wiring has a characteristic impedance (Z_0) of approximately 150 ohms, so that the current available at the end of the wire for rising waveforms is only 20 mA until reflections propagate, regardless of the source current available. Conversely, the initial voltage drop produced by a clamped load is IZ_0 or 1.5V for a 10 mA clamped load and 150 ohms characteristic impedance wiring.

c. The inductance and capacitance of the wiring combine to produce high frequency ringing on the transitions of waveforms. This ringing can be controlled by either resistively terminating the line with approximately 100 ohms if the circuit will drive it (B-series pulse amplifiers) or with the DEC level terminator circuit incorporated into the G796, G704, B163 and other modules. This clamp circuit inhibits the waveforms from reaching -3.5V and from going above ground.

d. The mutual inductance and capacitance of the wiring also causes high frequency cross-talk which may produce false operation of the logic. This can be reduced in the following ways: by minimizing the number of high frequency signal components through the substitution of slower R-series logic, instead of B-series; by clipping or clamping high frequency ringing with a level terminator circuit; by wiring with short wires and/or twisted pair, thereby reducing coupling.

5.2 GROUND SYSTEM

A good ground system is essential to reliable logic operation. The following is recommended: (1) Bus the ground and power pins A,B, and C in each module row with a type 932 Horizontal Bussing Strip. (2) Tie the ground bus strips to chassis ground ap-

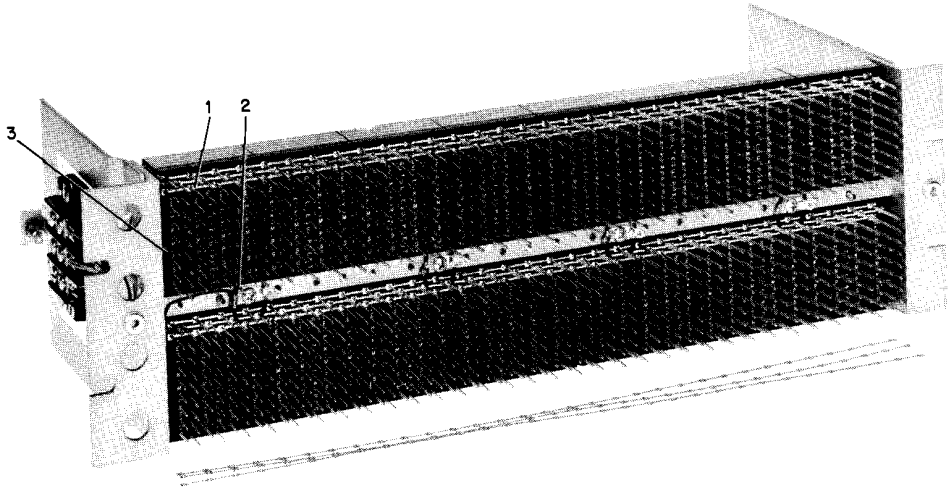


Figure 5-1 Logic Ground Mesh

proximately every two inches (once per H800 module block), using solid wire and white spaghetti insulation. (3) Wirewrap all grounded pins together for each vertical module row (pins C and other ground pins). This ground mesh (see Figure 5-1) will form a stable base for satisfactory logic performance.

5.3 SIGNAL WIRING RULES

The following signal wiring rules are meant as arbitrary guidelines for the construction of reliable logic assemblies, since under some conditions in the past, limits have been exceeded, while, under other conditions, the guidelines failed to prevent trouble. The best test of adequate wiring design is the ability of the signal waveforms to meet the following waveform requirements.

These rules DO NOT APPLY to B-series transistor inverters such as the B104, B105, B123 or B124; to transistor inverter flip-flops such as the B200, B201 or B204; or to the input circuits of the B301, B310, B360 or B620. The use of these modules since it requires very careful design and considerable experience is not recommended. Note that the R- and S-series pulses are to be treated as "levels" as the R-andS-series pulse amplifier output circuit is similar to an ordinary logic gate output circuit.

5.3.1 Control Area Pulses (high pulse wiring density)

If less than 6 in. total run length, use single wire; if 6 to 20 in. total run length and less than 6 loads total, use single wire; all other cases use twisted pair; in any case, terminate the end of the run in a 100 ohm pulse terminator as on the G700.

5.3.2 Register Loading Pulses (low pulse wiring density)

If distance from source to single load or to cable is less than 8 in., use single wire; if cable is used (cable length must not exceed 20 in.; maximum vertical distance between cable connectors is 1.5 in.), use G794-G794 or G799-G799 cables. If distance between load pins or between cable and load pin is less than 6 in., use single wire; if longer than 6 in., use twisted pair. All loads on a run must be located within an area 22 modules wide and 2 modules high; in any case, the end of the run must be terminated in a 100 ohm terminator as available in the G700.

5.3.3 Waveform Requirements

The following waveform requirements should be met by all levels and pulses.

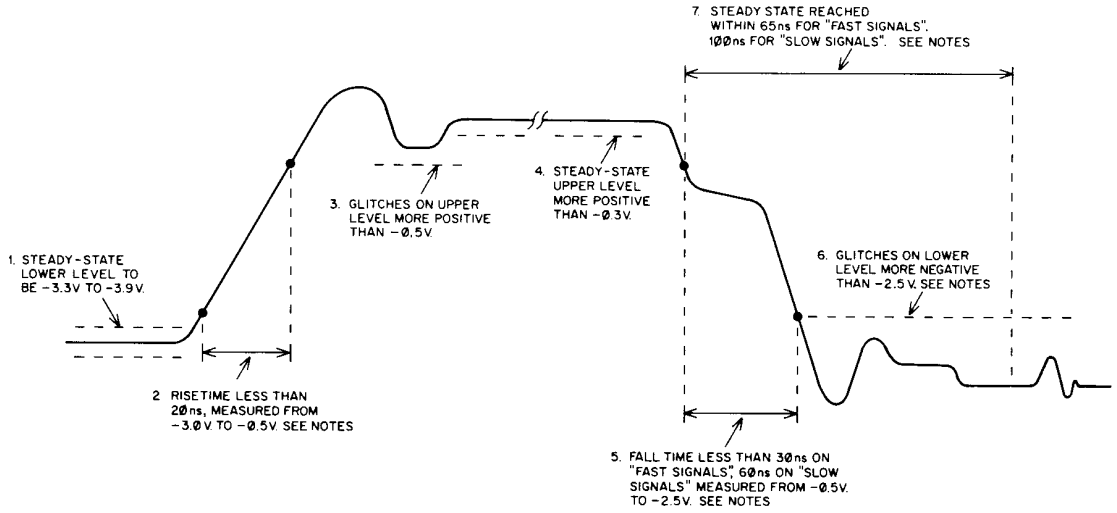


Figure 5-2 Waveform Requirements for B Series

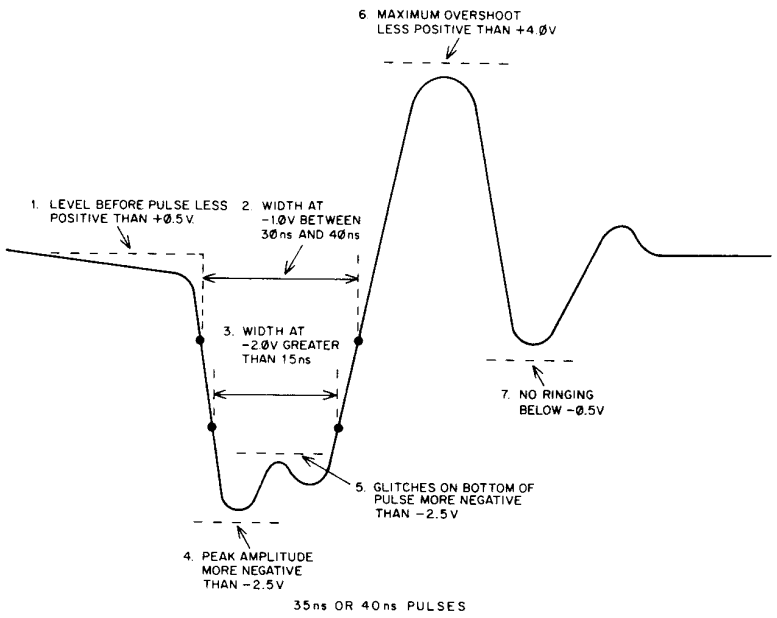


Figure 5-3 Waveform Requirements for B Series Modules

If 2. is not met, the source is overloaded.
If 3. is not met, the level is inadequately terminated.
If 4. is not met, the source is overloaded.
If 5, 6, 7. are not met, more clamped loads are needed.

If 1. is not met, recovery time is not long enough.
If 2, 3, 4. are not met, load is too heavy or wire is too long.
If 5, 6, 7. are not met, termination resistors should be added along line.

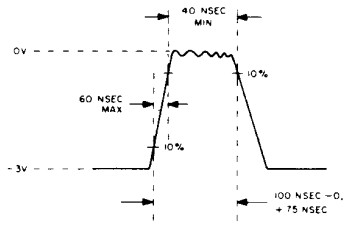


Figure 5-4 Standard R Series FLIP CHIP Waveform

5.4 LEVEL WIRING RULES FOR B-, R-, and S-SERIES LEVELS AND PULSES

a. Levels entirely in one cabinet (not going through a cable): If less than 20 in. total run length and less than 4 loads, the levels do not need to terminate; if less than 50 in. total run length and less than 4 loads and the level is ANDed with a pulse at the end of a run, they do not need to terminate but should be checked to determine that the pulse samples the level after ringing has settled down. If a short length run but more than 4 loads, terminate if the waveform does not meet waveform requirements below; all other cases terminate level with a level terminator circuit.

b. Interbay Levels (levels which run through a cable): Use G796-G796 cable between bays for all level cables. The levels do not need to terminate if: 1) source to cable run is less than 20 in. 2) cable to load run is less than 20 in. and there are less than 4 loads, 3) cable to load run is less than 50 in. and there are less than 4 loads and the level is ANDed with a pulse at the end of the run. Otherwise terminate with a level terminator circuit.

The standard level terminator is the G704 2 mA terminator circuit. It consists of a 2 mA clamped load which does not allow signal excursions below approximately -3.5V and a clamp diode which does not allow signal excursion above approximately ground. The single inputs of the B163 (pin D, E, K, L, R, S) contain similar circuits which may be used in lieu of G704 terminators if convenient. The G796-G796 cable assembly contains a standard 2 mA terminator circuit at each end. The R-series DCD gate contains a diode clamp which prevents input excursions above ground on both the level and pulse inputs. The DCD gate clamping feature is also an adequate terminator in most cases. R001 and R002 diodes are usable as ground clamp terminators with the cathode tied to ground and the anode tied to the level run, if no other terminator is available. A diode to ground should only be used if no other solution is practical. Additional clamped loads may have to be added to a long level line to maintain adequate fall time. For a terminator to be of any value, it must be within 10 in. beyond the last load in the run.

CHAPTER 6
USER TERMINAL INTERFACES

6.1 REQUIREMENTS

Teletypes and other user terminals must meet a minimum number of requirements to be used with the standard PDP-9 or PDP-9/L hardware-software system. (Violation of any particular requirement will necessitate the use of some hardware option, special interface or a modification of the standard software. In many cases, the change is quite simple, such as supplying extra NUL characters to allow a slow carriage to return.) PDP-9 and PDP-9/L software is designed for an ordinary (essentially unmodified) Teletype machine using the ASCII (USASCII) character codes. The requirements are as follows:

a. The terminal must have a 20 mA, neutral, full-duplex or an EIA interface.

b. The terminal must use self-synchronizing, asynchronous, serial-by-bit, serial-by-character data transmission, that is, ordinary, start-stop, teletype-style data transmission.

c. The printer or display portion of the terminal must respond to the control characters CR (carriage return, 015_8) and LF (line feed, 012_8) in the ordinary way. Response to other control characters is not required.

d. The printer or display must have "continuous paper-like" characteristics. That is, a special control should not be required to "advance-to-the-next page" (erase the present display).

e. No waiting time, beyond that provided by a CR LF sequence, should be required to return the printing carriage to the beginning of the line.

f. The printer or display should respond to at least the first 64 graphics of ASCII. (USASCII figures 040_8 to 077_8, and upper case 100_8 to 137_8). Any version of ASCII can be used with the user doing translation among equivalent graphics as necessary. All 95 graphics of USASCII can be used when available.

g. The keyboard must be able to generate at least one of the ALTMODE or ESC (PREFIX) codes (033_8, 175_8, 176_8).

h. The keyboard must be able to generate the "control" characters (000_8 to 037_8).

i. The keyboard must be able to generate at least the first 64 graphics of ASCII.

j. The terminal should not have any peculiar features i.e. (features not predictable from a reasonable interpretation of some revision of the ASCII standard).

Any terminal which meets the above requirements should be a usable terminal. It may not be as convenient to use as an ordinary Teletype with the PDP-9 (PDP-9/L) modifications but it will be adequate for many uses.

6.2 TELETYPE INTERFACE

Teletypes supplied by DEC for PDP-9 or PDP-9/L systems have the following as standard: local (off line) mode; slashed zero (Ø), upward arrow and left arrow characters; a separate ALTMODE, ESC, or PREFIX key and standard plug connector. When considered necessary by DEC engineering, various mechanical modifications will also be incorporated to provide improved reliability and user convenience.

Connections for 20 mA, neutral, full-duplex terminals (most Model 33 and 35 Teletypes and similar equipment) can be made as indicated on the drawings furnished with the machine by the manufacturer. A 283B plug can be connected as shown in Figure 6-1. Polarity must be as indicated. Connections for an EIA Interface (see EIA standard, Document Number RS-232-B) can be made as shown in Figure 6-2.

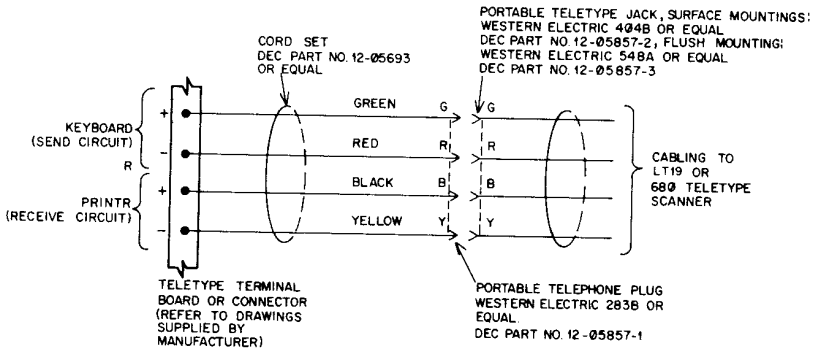


Figure 6-1 20 mA, Full Duplex Terminals

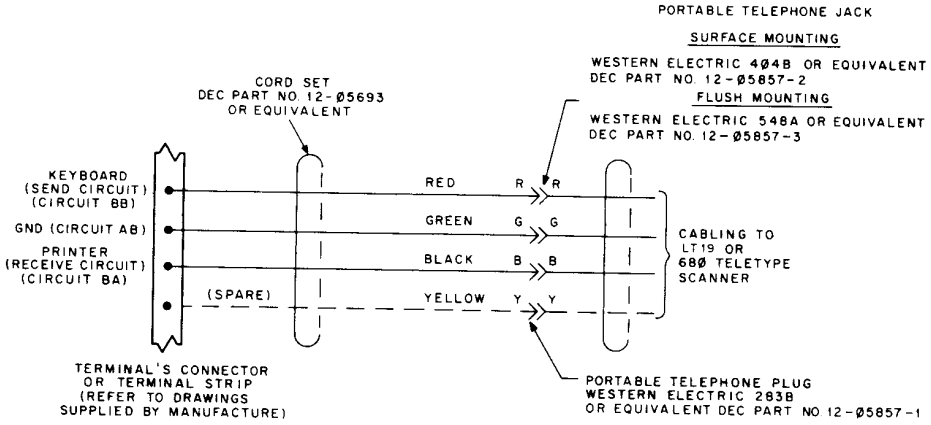


Figure 6-2 Connections for EIA Interface (EIA Standard RS-232-B) (Model 37 Teletypes and many other terminals)

CHAPTER 7
MARGIN CHECK BUS

Margin checking is a time-saving method of preventive and corrective maintenance, whereby the tolerance of a logic section to a change in nominal voltage gives an indication of circuit conditions. A decreasing tolerance to voltage changes (that is, the logic fails at smaller deviations from nominal voltage), indicates a degradation of circuit performance.

Margin checking in peripherals is generally done one logic row at a time. The method used for monitoring the margin voltage differs from previous DEC margin check methods. Since the PDP-9 and PDP-9/L systems are larger than the PDP-8 computer series, voltage drops in the margin lines are significant. For this reason, margin voltage monitoring is done as close to the logic as possible, by means of meter return lines. As shown in Figure 7-1, a simplified schematic of the margining system, voltage drops between the variable power supply and the section of logic under test have no effect on the meter reading, and any drop between the logic and meter is negligible since the meter current is small. As shown in Figure 7-1, the margin voltage line and the meter return line are connected together at the end of the system.

Figure 7-2 is a simplified schematic of the maintenance control panel. A few points concerning the circuitry follow:

a. The voltmeter is zero-center, and when the MC switch is OFF, it reads zero.

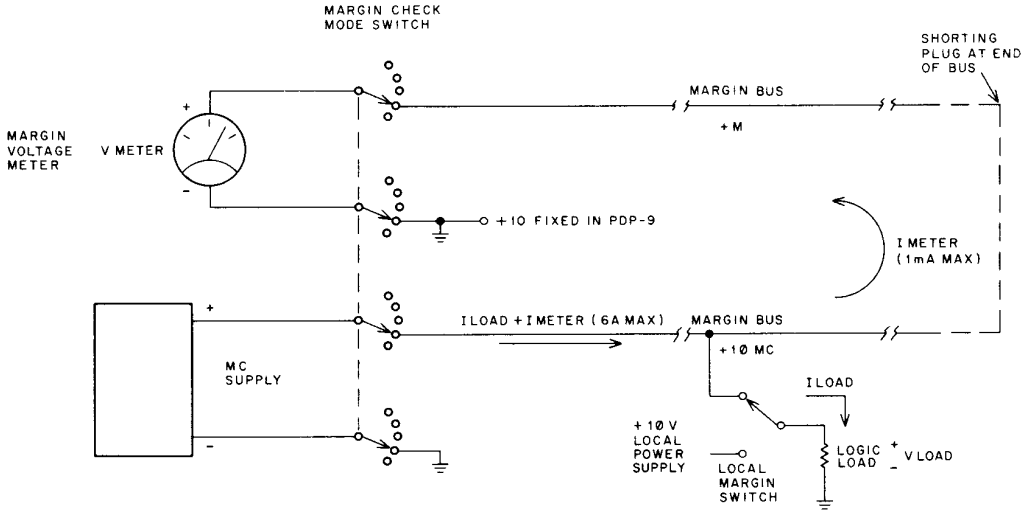


Figure 7-1 Margin Bus Voltage Drops

b. The variable supply has its output floating until a margin check is made. At this time the proper side of the supply is grounded.

c. The MC power supply provides the variable dc voltage for margin checking. Up to 5A is available at 20V from the margin check bus.

d. If the MC switch on a Maintenance Switch Panel is inadvertently left in the MC position, while the maintenance panel switch is OFF or margining in another mode, the correct fixed voltage is supplied to the logic through a margin voltage line. If this situation occurs, the following current is available +10V line, 4A; -15V line, 5A.

e. The voltmeter shows the difference between the variable supply and the fixed supply for each voltage level.

The cable used to connect the margin bus in the system has a male connector (Cinch-Jones P306CCT) at one end and female connector (S306CCT) at the other. The cable is called the BC10B margin check and remote control cable.

The power connector bracket used is DEC part number 7005467.

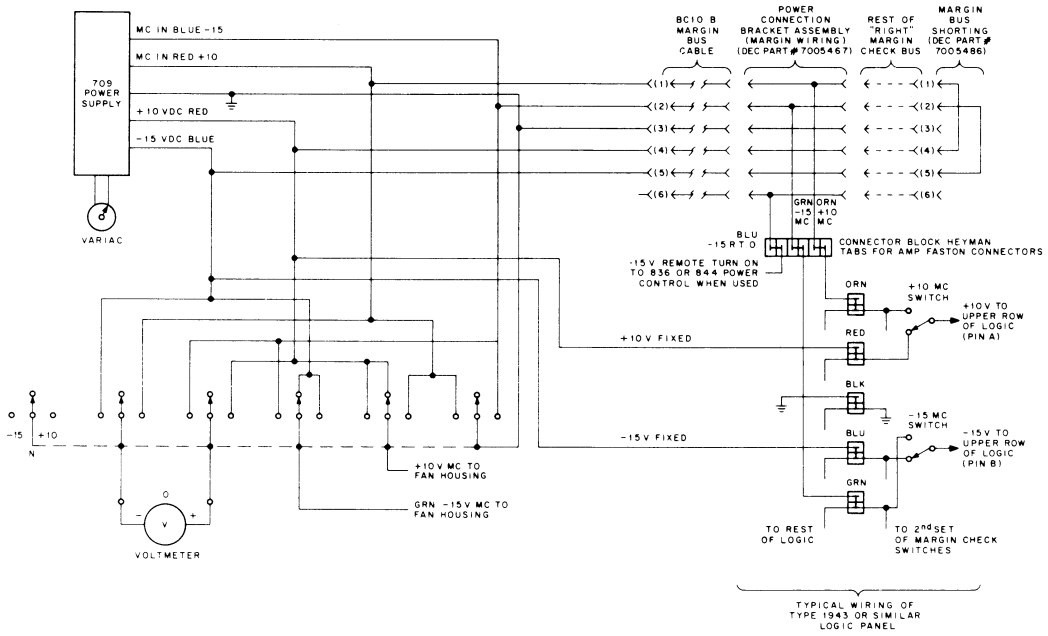


Figure 7-2 Margin Bus Circuit

CHAPTER 8
THE PDP - 9 and PDP-9 / L
GROUND MESH SPECIFICATIONS

To keep electrical noise and potential differences under control in the PDP-9 or PDP-9/L facility the following ground system is recommended. Other possible grounding methods may prove adequate but serious consequences of an inadequate ground system mean the user should consider carefully any alternate system he provides.

Each cabinet should be fitted with ground lug terminals connected together as shown in Figure 8-1 with #4 gage copper wire or equivalent. Ordinary stranded #4 gage wire is adequate for this purpose, although #4 gage welding cable (extra flexible stranding) may be preferred by some. Upon installation, the purchaser should supply a good earth ground connection to the central processor through #4 gage copper wire or equivalent. In general, an adequate earth ground is provided by a steel beam of a building frame or a large water pipe.

The type of the earth ground necessary depends on the use of the system. A system involving a digital-analog interface usually requires that the digital system ground be connected to the analog system ground at a single point, often at the analog-digital interface. A good ground connection is usually required in these cases. In small systems where no analog interface is involved, the grounding provided by a large electrical conduit may be adequate, although electrical conduit systems often are connected together poorly in terms of a low resistance path to ground. In large systems, additional connections to earth ground may also be advisable. All of these ground connections are additions to (not substitutes for) the ground leads carried along through the various signal buses (memory, I/O multiplexer and channel buses) and the ground conductors contained in the power (main) cables. The green wire in the power (mains) cable must also be returned to ground, usually through the conduit of the electrical distribution system.

When two cabinets are joined together, they should be bonded together electrically by running a #4 gage conductor or several copper mesh straps between the two cabinets.

Auxiliary units such as the line printer and card reader should be grounded to their associated control cabinets with #4 gage copper wire (#6 wire can be used in this case if desired).

In general, ground conductors should follow the path of the data buses through the system (i.e. in parallel to the memory buses, the I/O bus, the channel bus, etc.).

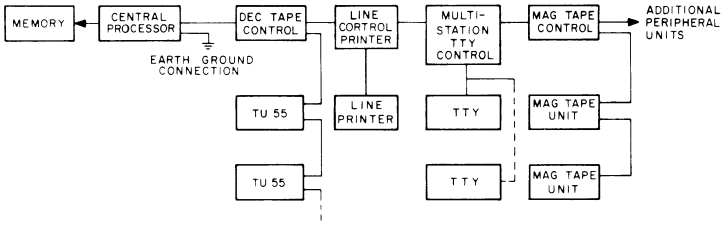


Figure 8-1 Typical Ground Mesh System

APPENDIX A
I/O BUS SUMMARY

This appendix describes the physical, electrical, and mathematical properties of the bus cable and its connectors, as well as each IO Bus signal, its origin, destination, and function.

The I/O Bus consists of cables and connectors which interface all I/O device controls to a common point at the computer (see Figure A-1). This bus provides signal lines for command and data transmissions initiated by programmed transfers, data channel transfers, program interrupt, API, read status and I/O skip facilities.

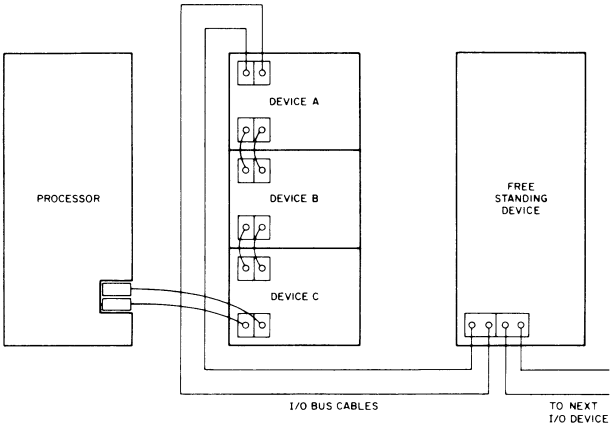


Figure A-1 IO Bus Connections

A.1 PHYSICAL CHARACTERISTICS

The PDP-9 (and PDP-9/L) I/O bus consists of two 36-pair cables with DEC Type W850 male connectors at either end. Cable specifications are given in Table A-1. The W850 connectors consist of two double-height FLIP CHIP boards. Figure A-2 shows a complete I/O bus cable assembly. The complete 2 cable assembly is designated as BC09A.

The size and weight of the cable and connectors require that retaining blocks be used to fasten the W850 connectors to the H800 female connector block of the 1943 panels. These retaining blocks are designated as the H003 and H004 connector retaining block kits, and are shown in Figure A-3.

Table A-1
I/O Cable Specifications

36-Pair Cable	Specifications	
Each Pair:	24 AWG 7 strands tinned copper Type B 600 V 105°C per MIL-W-16878D	
Twin:	1.0" LHL	
Cable:		
Core:	1 of Filler	
1st. Layer:	6 Pair	5.4" RHL
2nd. Layer:	12 Pair	5.4" RHL
Outer Layer:	18 Pair	7.5" LHL
Type:	.001" Mylar Tape Spiral Wrap 25: Overlap	
Jacket:	.035 wall Black 802 C Polyvinyl-chloride	
O.D.	Finished Nominal O.D. .580 plus or minus .020	

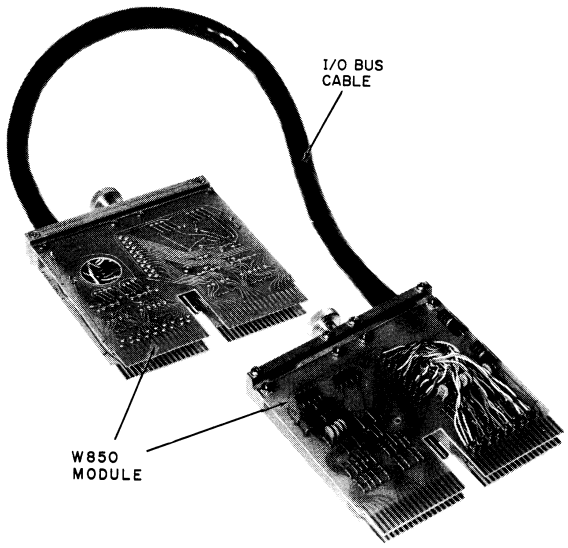


Figure A-2 I/O Cable Assembly

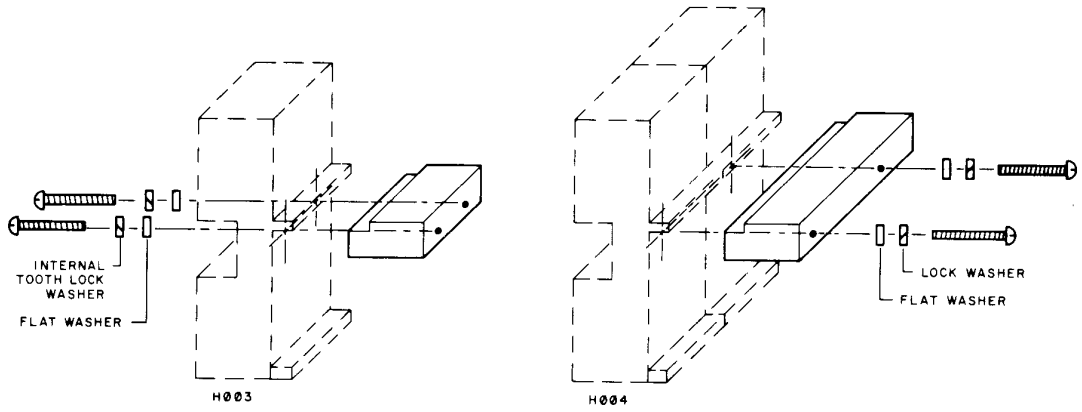


Figure A-3 H003, H004 Connector Retaining Block Kits

The H003 spans one H800 connector block and allows two cables to be plugged in. The H004 spans two H800 connector blocks and allows four cables to be plugged in. All necessary hardware and installation instructions are furnished with each kit. The H003 costs $5.20, and the H004 costs $11.00

A.2 ELECTRICAL CHARACTERISTICS

Electrical characteristics of the I/O cable are presented in Table A-2. The values shown are estimates; where such parameters are critical, it is recommended that the user perform his own measurements.

Table A-2
Electrical Characteristics of IO Cable

Characteristic Impedance	68 Ω
Delay	1.8 ns/ft
Rise Time	≈ 45 ns in 100 ft
Capacitance	≈ 25 pf/ft

A.3 W850 CONNECTOR

The W850 connectors have two-diode clamping circuits terminating the lines. A circuit schematic is shown in Figure A-4. At each interface, the normal power connection to pin B (-15V) must be made in all input W850 connectors. The output connector need not be supplied with power. A total of 400 mA is required per cable.

A.4 LOADING RULES

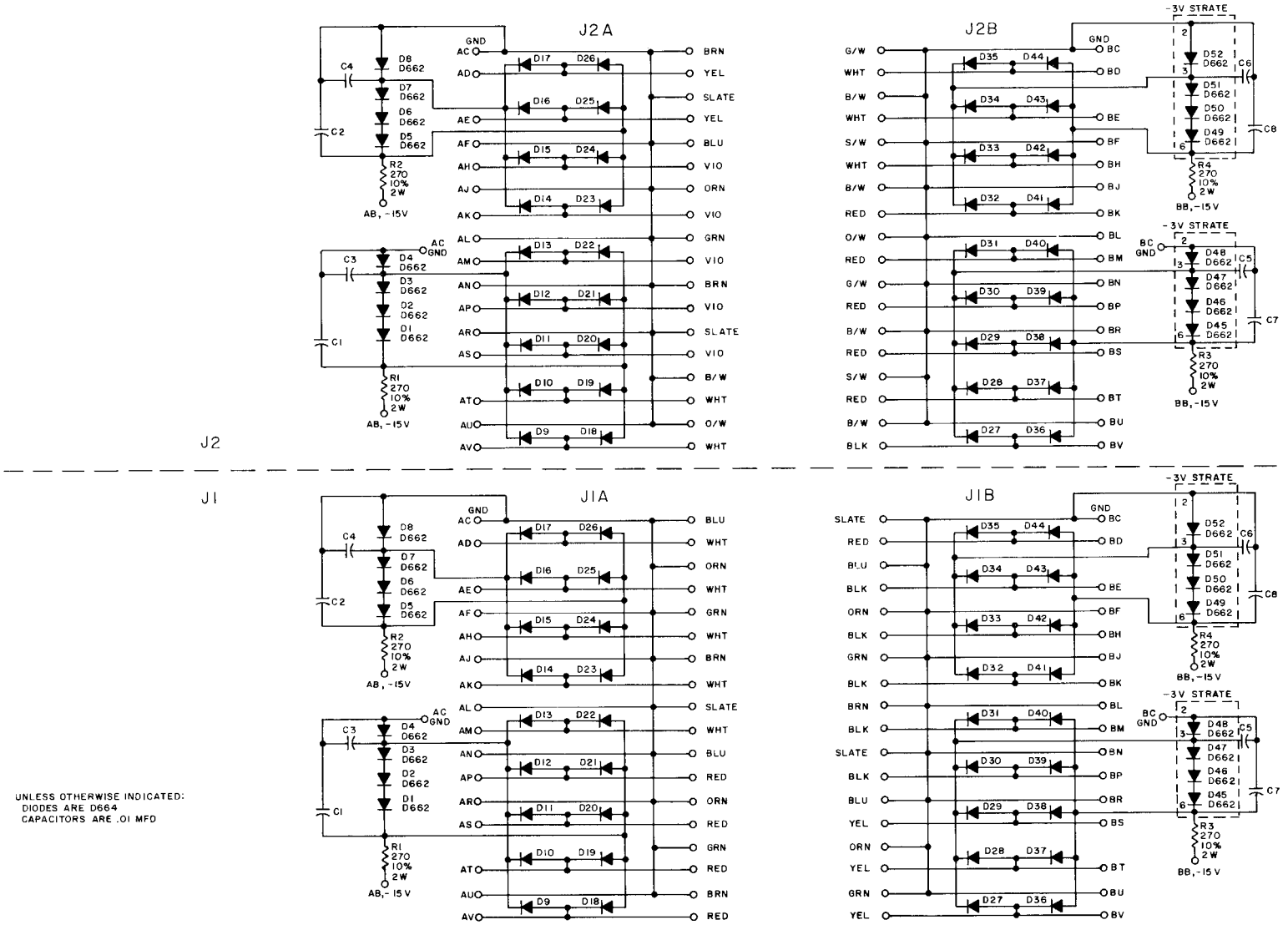
Each device must not draw more than 200 uA from the data lines I/O Bus 00 through I/O Bus 17. All other receiving lines must not draw more than 1 mA. All device output gates must be open collector gates capable of drawing 30 mA at ground. The B163 is an example of one such gate.

A.5 GENERAL RULES

All I/O bus interfaces must have two sets of I/O connectors: one set to receive incoming signals from the central processor or previous I/O device, and the other set to plug-in outgoing cables for the reset device on the I/O bus. On all 16 FLIP CHIP positions occupied by the I/O bus cables, pins C, F, J, L, N, R and U must be grounded. Even though some I/O signals may not be used by a particular device, all signals (including the spare) except the API "X" EN signals and DCH EN when they are used by the device must be strapped from the input connector position to the output connector positions, in order to feed signals to subsequent devices. No terminating resistors are required at the end of the I/O bus. Figure A-5 illustrates a typical I/O bus connection in a device using DCH.

A.6 INTERFACE SIGNALS

Descriptions of the functions of all I/O bus signal lines linking the central processor with the external I/O devices follow. Electrical characteristics and line terminating requirements are included. Figure A-6 illustrates the interface.



UNLESS OTHERWISE INDICATED:
DIODES ARE D664
CAPACITORS ARE .01 MFD

Figure A-4 I/O Connector W850

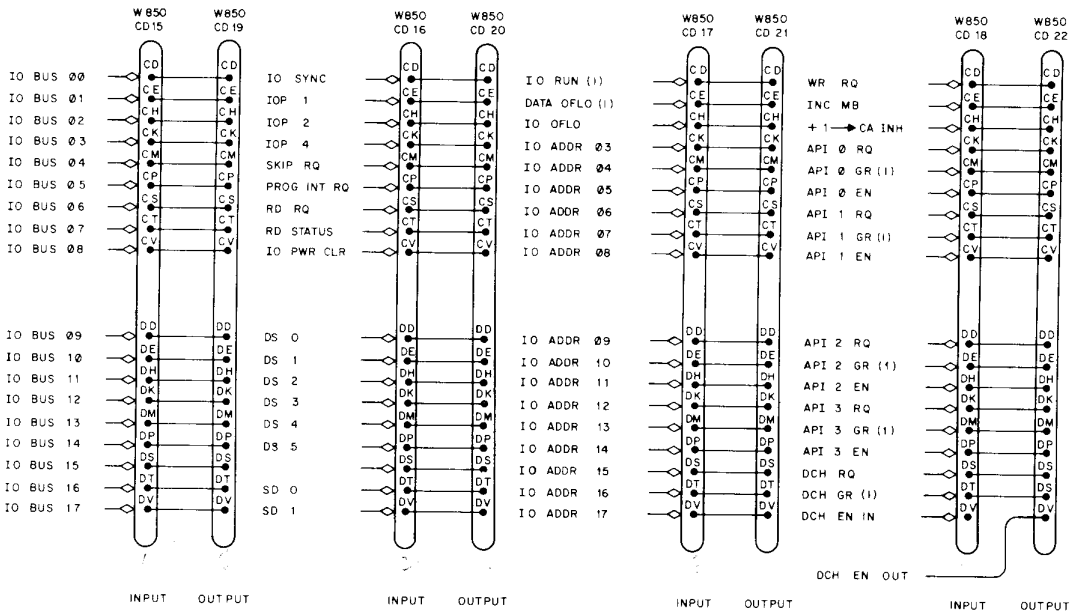


Figure A-5 Typical I/O Bus Connection in Device Using DCH

Data Lines I/O Bus 00 - I/O Bus 17

Eighteen data lines constitute the bidirectional facility for transferring data in bytes up to 18 bits in length between the central processor and all I/O devices. Transfers are made on a dc basis with the processor or device allowing bus settling time before data on the lines is strobed into the receiving register. The data lines convey transfers between the AC and a selected device information buffer register for programmed transfers; they convey data between the MB and a selected device buffer register for data channel operation. The bidirectional characteristic requires that the device use unclamped collectors for data transmission to the processor. Emitter followers must be used for data reception to avoid loading the bus on a dc basis which cannot be more than 200 uA per device. The data lines are terminated in the central processor by 15-mA clamped loads.

Output Control Signals

Eight output control signals are generated within the processor to effect specific functions in a selected device. The signals are bus driven at the CPU-I/O interface. They are:

a. IO PWR CLR - issued by power turn-on warm-up, by occurrence of a CAF instruction (mnemonic for clear all I/O flags), and by actuation of the I/O RESET key on the control console. The signal resets all flip-flops storing device-to-processor flag indications (e.g., ready, done, busy). It is developed as a 400 ns, nominal width, negative-going pulse.

b. IO SYNC - issued every memory cycle. The signal may be used to synchronize I/O device control timing to execution of the program in progress. The signal is developed as a 400 ns, nominal width, negative-going pulse.

c. IOP1, IOP2, IOP4 - microprogrammable signals to effect IOT instruction-specified operation within a selected I/O device. Processor automatically generates IOP2 and IOP4 for data channel input and output transfers, respectively. Although they may be used for any control function, the common uses of the IOPs are:

(1) IOP1 - normally used in I/O skip instruction to test a device flag. It may be used as a command pulse, but it cannot be used to initiate loading of or reading from a device buffer register.

(2) IOP2 - usually used to effect transfer of data from a selected device to the processor, or to clear a device register. It may not be used to determine a skip condition.

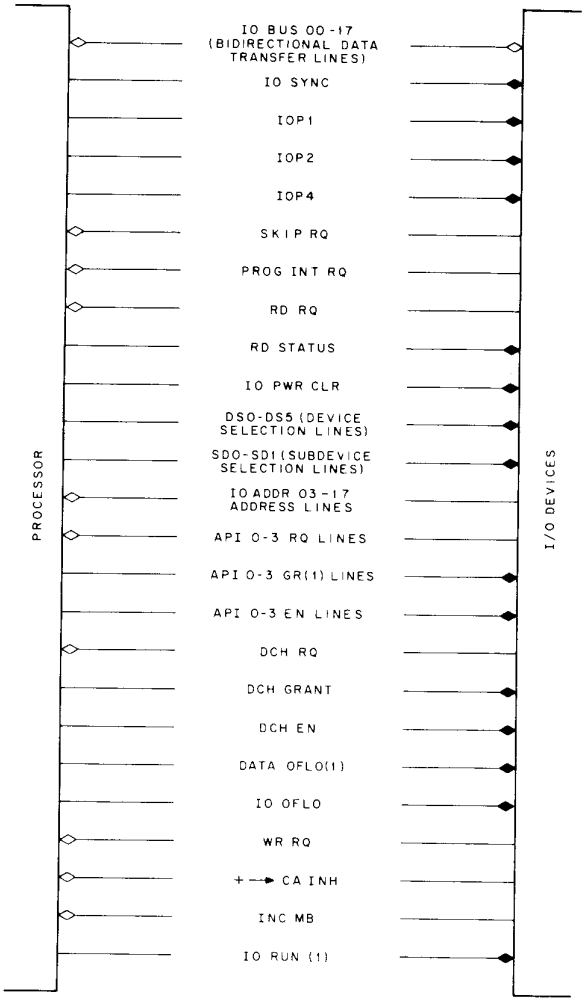


Figure A-6 I/O Bus Interface

(3) IOP4 - usually used to effect transfer of data from the processor to a selected device register. It may not be used to determine a skip condition or to effect transfer of data from a selected device to the processor.

The IOP 1 and 2 signals in the PDP-9 occur as 1 μs, nominal width, negative-going pulses, and IOP4 occurs as a 500 ns negative-going pulse. IOP 1 and 2 for the PDP-9/L are 1.5 μs negative-going; IOP4 is 650 ns negative-going.

d. RD Status - issued by execution of the IORs instruction (mnemonic for input/output read status). Loads the AC with an 18-bit word containing device flag indications for devices interfaced to read status facility. The signal occurs as a 500 ns, nominal width, negative-going pulse for the PDP-9, and 650 ns for the PDP-9/L. The signal also occurs when the REGISTER DISPLAY switch (console) is placed in the STATUS position and the processor is stopped.

e. IO OFLO - issued during the first cycle of a data channel transfer if the content (2's complement) of the word counter assigned to the currently active data channel device becomes zero when incremented. This indicates that the program specified number of words will have been transferred at completion of the data channel transfer in progress. It is normally used to turn off the respective device, preventing further data channel action by that device until a service subroutine reinitializes the channel word counter and current address registers, and the program turns on the device request flag. The overflow signal may also be used to initiate a program interrupt through the program interrupt or automatic priority interrupt facilities for access to the initializing subroutine. The signal occurs as a 400 ns nominal width, negative-going pulse.

f. DATA OFLO(1) - issued during the third cycle of a 4-cycle add-to-memory DCH break when the address incremented overflows. The DCH add to memory capability is a 2's complement arithmetic operation. The contents of the MB, and the contents of the I/O Bus during data transfer to the computer, are assumed to be in 2's complement form, Bit 0 being the sign bit.

DATA OFLO(1) is a 200 ns pulse, gated onto the I/O Bus in the middle of the third add to memory DCH cycle, which signals an incorrect sum occurred. This happens when the C(MB) and the C(I/O Bus) are of like signs and their sum has the opposite sign. If the C(MB) and the C(I/O Bus) have opposite signs DATA OFLO(1) cannot occur.

DATA OFLO occurs when:

$$(MB) + (I/O\ Bus) > 2^{17} - 1$$

OR

$$(MB) + (I/O\ Bus) < -2^{17}$$

Device Selection Levels DS0 - DS5 and SD0, SD1

Detection of the current instruction as an IOT causes the bit pattern placed in MB6-13 during the fetch

cycle of the instruction to be bus driven and sent via eight bus lines to the Type W109 Device Selection modules contained in the control logic for each device. These eight levels form a 6-bit device selection code, DS0 - DS5 (relating to MB6-11) and a subdevice or mode select code extension, SD0 and SD1 (relating to MB12-13). Assertion, or binary 1, is defined as a -3V. Negation, or binary 0, is defined as ground level. Each W109 is configured for response to only one of the 64 possible DS codes. Cooperating pairs of W109s permit unique response to any of the 256 DS-plus-SD codes. Each selection code configured in a device permits the internal generation of up to three associated commands through the W109 ANDing of IOPs and the device selection code.

IO RUN(1)

The IO RUN signal is available at the interface for use as the interface designer requires. This bus driven level switches to the -3V level and remains there while the RUN flip-flop in the CP is set. A ground level indicates that the RUN flip-flop has been cleared.

Input Control Levels

Six input control level signals arrive at the I/O control section in the central processor. These levels are at ground for assertion and at -3V for negation. Each signal line is terminated in the processor with a 15 mA clamped load. The line must be driven from the unclamped collector of a saturated transistor whose emitter is grounded. The individual functions of the input control levels are as follows.

a. SKIP RQ - the return of this level to the processor indicates that an IOT instruction test for a skip condition in a selected device has been satisfied (e.g., a test of ready status). The PC is subsequently incremented by one to effect a skip of the next instruction of the program in progress.

b. PROG INT RQ - a device delivers this level to request interruption of the program in progress. The program traps to location 00000 when no I/O transfer action of higher priority is in progress. The instruction resident in location 00001 is fetched and executed. This instruction is usually a JMP to a subroutine which determines through a search process (skip chain) the device making the program interrupt request. Access is then made of the appropriate service subroutine. Up to 64 devices may be interfaced to the program interrupt request line. The only limiting factor is the program overhead incurred in the search for the requesting device.

c. RD RQ - this level requests that the processor execute a read transfer of device-offered data word.

d. WR RQ - this level requests that the processor execute a data channel write transfer of a data word into the selected device's information register.

e. INC MB - this level requests that the processor increment by one the contents of the memory location addressed by the 15-bit address on the I/O bus address lines.

f. +1 → CA INH - this is a special signal line required by devices which automatically search for records, etc. Typical are DECtape and magnetic tape. The presence of the level inhibits normal incrementing of the device-assigned current address register during a data channel transfer.

Multiplexed Control Lines

Fifteen control lines, constituting five multiplexed subsets of three lines each, provide processor-device control information paths for the multiplexed data channel and the four priority levels on which the automatic priority interrupt option processes device channel requests for service. The functions of the lines in the subsets are as follows:

a. Request - a device transmits a service request to the processor via the appropriate request line. Each request line is terminated in the processor by a 15-mA clamped load. The line must be driven to ground for assertion by an unclamped collector of a saturated transistor whose emitter is grounded.

b. Grant - the processor indicates a grant of the service request by driving the associated grant line negative. All grant lines are buffered by bus driver modules in the processor.

c. Enable - the enable signal controls the priority order for answering service requests of devices interfaced to the data channel control or to one of the APIs 28 device channels. Each API channel may be uniquely assigned to one device for fast access of the appropriate service subroutine, or interfaced to any number of devices. The latter case requires a search subroutine to determine the requesting device. Priority for a channel (data or API) is allocated in descending order from the device nearest the processor I/O bus interface. Occurrence of an enable signal permits service of the requesting device with the highest channel priority and inhibits all lower priority devices from making requests during the interval of service.

A bus driver module in the processor buffers each enable line.

Address Lines

Fifteen lines, of which only the least significant six are normally used, constitute an input bus for the devices which must deliver address data to the processor. The lines are terminated in the processor by 15-mA clamped loads. Each line must be driven to ground for assertion by an unclamped collector of a saturated transistor whose emitter is grounded. Two uses for the address bus are as follows.

a. When a device interfaced to the multilevel, automatic priority interrupt option receives a processor grant of its interrupt request, it delivers to the processor a hardware-defined address, relating to its API channel assignment. This channel address indicates the unique entry point to the device's service subroutine. The instruction resident in the addressed memory location is always a JMS (or JMS I or XCT of a JMS), offering fast access to the appropriate service routine.

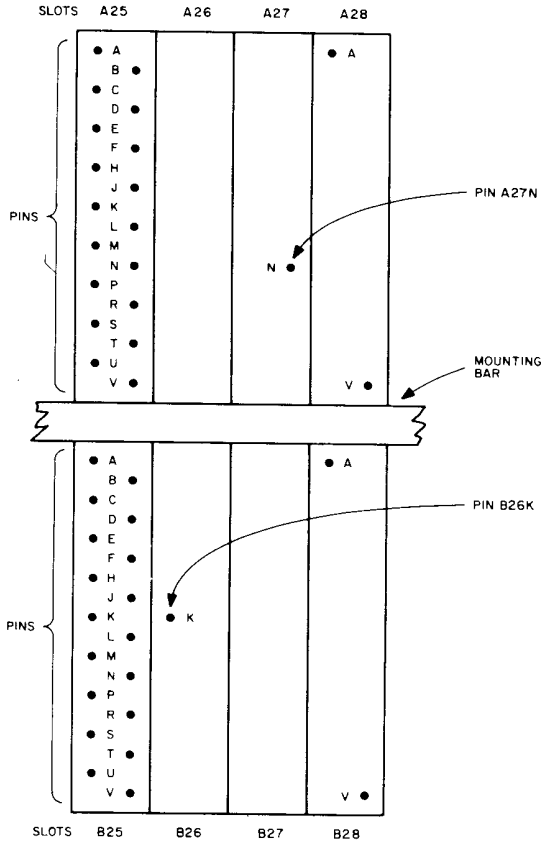


Figure A-7 Interface Connectors and Pins

b. When a data channel device receives a processor grant of its transfer request, it delivers to the processor a hardware-defined address, relating to the memory location of the assigned channel word counter register.

Connection to the address lines and data lines is made by AND gates without clamp loads. Each gate must be capable of driving 30 mA at ground.

I/O Bus Interface Summary

Table A-3 summarizes the I/O bus interface at the processor. Figure A-7 illustrates the key for determining the connector and associated pin for each bus line. Provision is made for two I/O bus connections at the computer; I/O block 1, and I/O block 2.

Reference Symbols:

CO - Collector Output, no clamped load, normally Type R111 or B163. Can drive a 30-mA load at ground. 0-mA load at -3V.

BD - Bus Driven output. Can drive 25-mA load at ground, 7-mA load at -3V. Usually a B123.

Level Terminator Operation - A Mathematic Treatise

Two-diode clamping circuits as explained below are adequate to terminate a transmission line such that little if any reflection occurs.

Consider the simplified example shown in Figure A-8. The transmission shown is a twisted pair, but any long signal line in a relatively uniform wiring network will act as a transmission line. Transmission lines will propagate independent forward (left-to-right) and backward (right-to-left) waves. These are described by the following incremental equations:

$$V_f(t,x) = V_{f_0}(t - x/c)$$
$$I_f(t,x) = \frac{Vf_0(t - x/c)}{Z_0} \quad \text{forward wave}$$

$$V_r(t,x) = V_{r0}(t + x/c)$$
$$I_r(t,x) = -\frac{Vf_0(t + x/c)}{Z_0} \quad \text{backward wave}$$

Where Z_0 is the charactistic impedance of the transmission line and c is the velocity of propagation along the transmission line. (The line is lossless and dispersionless.) The current in the line at any point is $I_f + I_r$ and the voltage at any point is $V_f + V_r$

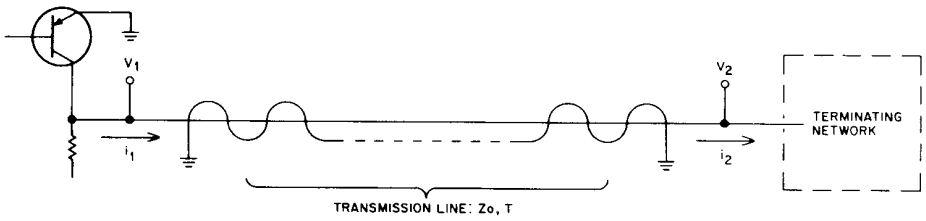


Figure A-8 Level Transmission Line

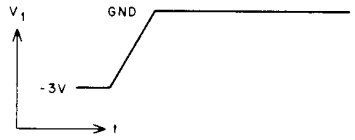


Figure A-9 Driving Waveform

where in both cases dc voltages and currents are ignored.

Consider the case where the transistor at the left end of the transmission line generates the voltage waveform shown in Figure A-9.

At a time T later, this waveform traveling as a forward wave will reach the terminal end of the line and will interact with the terminating network possibly causing a reflected backward wave. The following equation must be satisfied at the terminal node:

$$V_f = I_f Z_0$$
$$V_r = - I_r Z_0$$
$$V_2 = I_2 Z \text{ term}$$
$$I_2 = I_f + I_r$$
$$V_2 = V_f + V_r$$

where Z Term is the (incremental) impedance of the terminating network (as a function of V_2 and I_2).

If Z Term is an open circuit (the signal is unterminated), then $I_2 = 0$ so $I_r = - I_f$ and $V_r = V_f$ (the signal is completely reflected). The voltage in the middle of the line will have a 100% overshoot (Figure A-10 (a)).

If Z Term = Z_0, the $I_2 = I_f$, $V_2 = V_f$ and I_r and $V_r = 0$ (there is no reflection). There will be no overshoot (Figure A-10(b)). Unfortunately most logic circuits are unable to drive a load of Z_0 (typically 100 to 150Ω).

If the terminating network is a short circuit, then $V_2 = 0$, so $V_r = -V_f$, $I_r = I_f$, and $I_2 = ZI_f$ (the signal is completely reflected and inverted). The voltage in the middle of the line will have a 100% undershoot.

If the terminating network is an ideal clamp diode connected to ground, the incremental reflected wave will be identical to the open circuit case until V_2 reaches ground. Then it will be identical to the incremental wave found in the short circuit case (Figure A-10 (d)). In this case the overshoot is only 50% and lasts only the duration of the risetime of the forward wave.

If the terminating network is a real diode connected to -0.7V (to compensate for the forward voltage drop of the diode), the incremental terminating impedance will vary from an open circuit to a low impedance in a continuous fashion. The terminating impedance will be approximately equal to Z_0 over a significant part of the risetime. The overshoot in the middle of the line is now somewhat less than 50% but has a nonzero tail (Figure A-10 (e)).

The actual level terminating network has a positive going clamp at ground as discussed above and also a negative going clamp at -3.5V. These clamp diodes in conjunction with the miscellaneous dissipative losses in the transmission line and the source provide signals throughout the length of the line which do not have excessive overshoot, undershoot, or ringing.

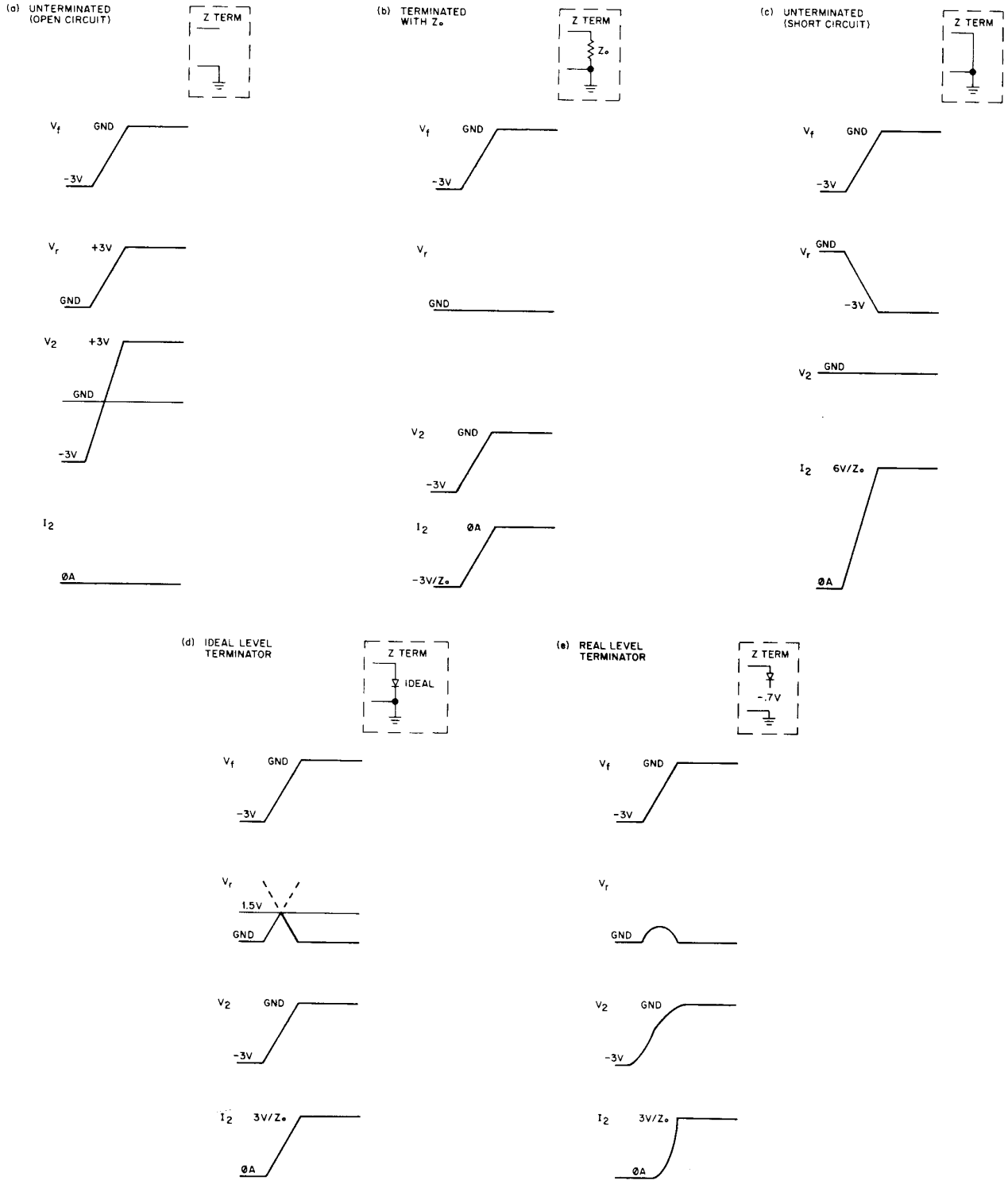


Figure A-10 Waveforms During Reflection

Table A-3
I/O Bus Interface Chart

I/O Block 1	I/O Block 2	Type	Assertion	Signal Name
A25D	A29D	CO	◇	IO BUS 00
A25E	A29E	CO	◇	IO BUS 01
A25H	A29H	CO	◇	IO BUS 02
A25K	A29K	CO	◇	IO BUS 03
A25M	A29M	CO	◇	IO BUS 04
A25P	A29P	CO	◇	IO BUS 05
A25S	A29S	CO	◇	IO BUS 06
A25T	A29T	CO	◇	IO BUS 07
A25V	A29V	CO	◇	IO BUS 08
A26D	A30D	BD	◆	IO SYNC
A26E	A30E	BD	◆	IOP 1
A26H	A30H	BD	◆	IOP 2
A26K	A30K	BD	◆	IOP 4
A26M	A30M	CO	◇	SKIP RQ
A26P	A30P	CO	◇	PROG INT RQ
A26S	A30S	CO	◇	RD RQ
A26T	A30T	BD	◆	RD STATUS
A26V	A30V	BD	◆	IO PWR CLR
A27D	A31D	BD	◆	IO RUN (1)
A27E	A31E	BD		ADD OFLO(1)
A27H	A31H	BD	◆	IO OFLO
A27K	A31K	CO	◇	IO ADDR 03
A27M	A31M	CO	◇	IO ADDR 04
A27P	A31P	CO	◇	IO ADDR 05
A27S	A31S	CO	◇	IO ADDR 06
A27T	A31T	CO	◇	IO ADDR 07
A27V	A31V	CO	◇	IO ADDR 08
A28D	A32D	CO	◇	WR RQ
A28E	A32E	CO	◇	INC MB
A28H	A32H	CO	◇	+1 → CA INH
A28K	A32K	CO	◇	API 0 RQ
A28M	A32M	BD	◆	API 0 GR(1)
A28P	A32P	BD	◆	API 0 EN
A28S	A32S	CO	◇	API 1 RQ
A28T	A32T	BD	◆	API 1 GR(1)
A28V	A32V	BD	◆	API 1 EN

NOTE

All pins C,F,J,L,N,R,U, should be connected together and wired into the ground mesh of the device.

Table A-3 (Cont)
I/O Bus Interface Chart

	I/O Block 1	I/O Block 2	Type	Assertion	Signal Name
1	B25D	B29D	CO	◇	IO BUS 09
	B25E	B29E	CO	◇	IO BUS 10
	B25H	B29H	CO	◇	IO BUS 11
	B25K	B29K	CO	◇	IO BUS 12
	B25M	B29M	CO	◇	IO BUS 13
	B25P	B29P	CO	◇	IO BUS 14
	B25S	B29S	CO	◇	IO BUS 15
	B25T	B29T	CO	◇	IO BUS 16
	B25V	B29V	CO	◇	IO BUS 17
2	B26D	B30D	BD	◆	DS 0
	B26E	B30E	BD	◆	DS 1
	B26H	B30H	BD	◆	DS 2
	B26K	B30K	BD	◆	DS 3
	B26M	B30M	BD	◆	DS 4
	B26P	B30P	BD	◆	DS 5
	B26S	B30S	–		SPARE
	B26T	B30T	BD	◆	SD 0
	B26V	B30V	BD	◇	SD 1
3	B27D	B31D	CO	◇	IO ADDR 09
	B27E	B31E	CO	◇	IO ADDR 10
	B27H	B31H	CO	◇	IO ADDR 11
	B27K	B31K	CO	◇	IO ADDR 12
	B27M	B31M	CO	◇	IO ADDR 13
	B27P	B31P	CO	◇	IO ADDR 14
	B27S	B31S	CO	◇	IO ADDR 15
	B27T	B31T	CO	◇	IO ADDR 16
	B27V	B31V	CO	◇	IO ADDR 17
4	B28D	B32D	CO	◇	API 2 RQ
	B28E	B32E	BD	◆	API 2 GR(1)
	B28H	B32H	BD	◆	API 2 EN
	B28K	B32K	CO	◇	API 3 RQ
	B28M	B32M	BD	◆	API 3 GR(1)
	B28P	B32P	BD	◆	API 3 EN
	B28S	B32S	CO	◇	DCH RQ
	B28T	B32T	BD	◆	DCH GR(1)
	B28V	B32V	BD	◆	DCH EN

NOTE

All pins C,F,J,L,N,R,U, should be connected together and wired into the ground mesh of the device.

APPENDIX B
PDP - 9 MODULE INFORMATION

This appendix provides descriptions of many of the Digital FLIP CHIP modules useful for building special hardware for PDP-9 systems. PDP-9 wiring rules are provided in Chapter 5 to aid the designer in producing reliable high-speed logic designs.

DEC builds three series of compatible below-ground logic (the B-, R- and S-series), two series of compatible above-ground logic (K- and M-series), an extensive line of modules to interface different types of logic (W-series), a line of special purpose modules (G-series), and a line of support hardware for its module line (H-series).

With few exceptions, the DEC compatible below-ground logic operates with logic levels of ground (±0.3V) (upper level) and -3V (-3.3V to -3.9V) (lower level) using diode gates which draw input current at ground and supply output current at ground.

The compatible above-ground logic generally operates with levels of ground (±0.4V, lower level) and +2.4 to +3.6V (upper level) using TTL or TTL-compatible circuits whose inputs supply current at ground and whose outputs sink current at ground.

The DIGITAL Logic Handbook, C-105, is recommended reading for those not already familiar with the basic principles of digital logic and the type of circuits used in DEC logic modules. Updated repair schematics for all modules used in the PDP-9 are furnished with each system.

B.1 MEASUREMENT DEFINITIONS

Timing is measured with input driven by a gate or pulse amplifier of the series under test and with output loaded with gates of the same series, unless otherwise specified. Percentages are assigned as follows: 0% is the initial steady-state level, 100% is the final steady-state level regardless of the direction of change.

Delay is the time difference between input change and output change, measured from 50% input change to 50% output change. Rise and fall delays for the same module usually are specified separately.

Risetime and falltime are measured from 10% to 90% of waveform change, either rising or falling.

Total transition time (TTT) is the time difference between 10% input change and 90% output change. Output rise and fall TTT are usually specified separately.

Typical propagation delay is the average delay per stage for many similar circuits connected in cascade and should be independent of the level (10%, 50%) at which it is measured.

Set-up time is the time during which an input must be held stable (e.g., the level input of a DCD gate) before another input is asserted (e.g., the pulse input of the DCD gate).

Input current is defined as positive when it is flowing into the input terminal.

Output current is defined as positive when it is flowing out of the output terminal.

All specifications are nominal or typical unless noted as Min or Max or with a tolerance.

B.2 B-SERIES MODULE INTERCONNECTIONS

Due to the high operating speed of B-series modules, the effects of wiring on logic operation should be considered. However, the use of diode-transistor circuitry similar to that used in the R-series modules provides good noise margins.

Occasionally, a logic design will require a minimum delay along a particular path. Logic elements which provide a guaranteed minimum delay such as the B212 flip-flop or the B311 delay should be used as regular decreases in delay are obtained in other modules due to continued improvements in technology.

Slow falltimes of logic levels may limit the speed of systems built with B-series modules to less than 10 MHz. In most cases, an estimate of falltime can be made by considering the total capacitance on

the logic line and the current available to drive the line negative. Figure B-1 shows the equivalent circuit.

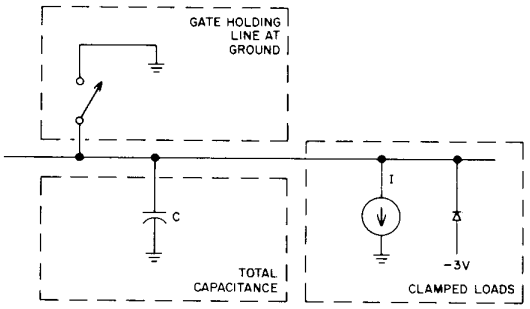


Figure B-1 Circuit to Estimate Falltime

The falltime is then given by

$$t_f(ns) = \frac{C\ (pF)}{I\ (mA)}\ \Delta V\ (V).$$

For B-, R-, S-series logic, as well as the "DEC" (below ground) portions of W-series modules, ΔV is around -3.5V. To be conservative, "I" should be taken as the current that can be sinked by the clamped loads at -3V. Thus a "10 mA" clamped load provides -7 mA of current to discharge capacitance at -3V. Inputs which require current at -3V must be deducted from the available current before calculating falltime (e.g., B684 inputs, indicator drivers). Input and output capacitances are typically as follows: input capacity 10 pF for each diode input, output capacity 8 pF for each collector output, a clamped load with a separate pin represents 8 pF of capacity, and wiring represents 1 to 1.5 pF per in. (.04 to .06 pF per mm).

Falltime calculations become inaccurate as the delay inherent in the wiring (1.5 ns per ft, 4.5 ns per m) approximates 1/10 the estimated falltime due to overshoots, reflections and ringing.

When wire lengths become relatively long, the distributed capacitance and inductance of the wiring will produce overshoots and ringing of the logic signal. The DEC level terminator circuit has been designed to control the amplitude of these effects to eliminate false operation of the logic. A simplified circuit of the level terminator is shown in Figure B-2.

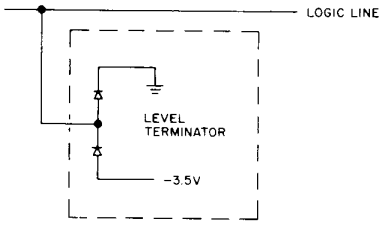


Figure B-2 Level Terminator, Simplified Circuit

The level terminator operates by clamping the signal excursions at ground and -3.5V. Occasionally, a clamped load is incorporated into the level terminator to improve falltime (e.g., G796, G704). A theoretical analysis of the level terminator operation when terminating a transmission line is provided in Appendix A.

Module Margining

The PDP-9 is provided with a system for checking the margin of power supply which will still allow a module to operate. A module should work properly within a prescribed range of supply voltage variation. Failure to do so may be due to a faulty module or to timing or loading problems in the logic design. To avoid permanent damage to the modules, the supply voltage should not exceed the range 0V to +20V (+10V supply) or 0V to -20V (-15V supply). Exceeding these limits (or tighter limits where specified) may cause permanent damage to the module. Typical power supply margins which allow proper operation are shown with each module.

Inter-Series Pulse Conversion

Table B-1 provides a helpful aid in the selection of modules to convert pulses from one series to another. For complete specifications refer to the appropriate module catalog.

DEC's Module Applications Group can supply numerous application notes and advice on unusual problems in this area.

Table B-1 Inter-Series Pulse Conversion

FROM \ TO		FLIP CHIP K 100/5 kHz 4/50 µs	FLIP CHIP M 6MHz 30 ns	Conversion To Below Ground →	FLIP CHIP B 10 MHz 25 ns	FLIP CHIP R (& S) 2 MHz 40 ns	LAB 100 5 MHz 50 ns	SYSTEM 1000 5 MHz 50 ns	LAB 3000 500 kHz 300 ns	SYSTEM 4000 500 kHz 60 ns	LAB 5000 10 MHz 25 ns	SYSTEM 6000 10 MHz 25 ns
FLIP CHIP K[2]			M602**	M652[1] W512 W510 1501	B611**	R601,** etc.	602**	1607**	3602**	4604**	5602**	6603**
FLIP CHIP M	50 ns	M302 K303[3]			DIRECT	R601,* etc.	DIRECT	DIRECT	Convert To 100 Series First	Convert To 1000 Series First	DIRECT	DIRECT
Conversion To Above GND ↑		M502[1], W603, W601, 668, 4686										
FLIP CHIP B	40 ns	Convert To R or M Series First	M602			R601,* etc.	W607 602 with Feedback	W607 1609	Convert To R or 100 Series First	Convert To R or 1000 Series First	DIRECT	DIRECT
FLIP CHIP R (& S)	100 ns 400 ns	K303[4] R302 R303	M602** †		B611**		W607** 602**	W607** 1607**	W640	W640	B611** 5602**	B611** 6603**
LAB 100	70 ns	302	M602 †		5602 B611 †	R601,* etc.		DIRECT	3602 with Feedback	4604 3602 with Feedback	5602 †	5602 6603 †
SYSTEM 1000	70 ns	1304	M602 †		6603 B611 †	R601,* etc.	DIRECT		4604 3602 with Feedback	4604 4606	6603 5602 †	6603 †
LAB 3000	400 ns	3301 K303	M602** †		Convert To R or 100 Series First	R601,* etc. †*	602 †	1609 602 †		DIRECT	Convert To 100 Series First	Convert To 100 or 1000 Series First
SYSTEM 4000	400 ns	4301 4303 K303	M602** †		Convert To R or 1000 Series First	R601,* etc. †*	1609 602 †	1608 1609 etc. †	DIRECT		Convert To 100 or 1000 Series First	Convert To 1000 Series First
LAB 5000	40 ns	Convert To 100 Series First	M602		DIRECT	R601,* etc.	602 with Feedback	1609 602 with Feedback	Convert To 100 Series First	Convert To 100 or 1000 Series First		DIRECT
SYSTEM 6000	40 ns	6304	M602		DIRECT	R601,* etc.	1609 602 with Feedback	1609 1608 with Feedback	Convert To 100 or 1000 Series First	Convert To 1000 Series First	DIRECT	

[1] M502 and M652 must be used for 40 ns pulses
[2] Convert to unslowed K-series first
[3] See Application note AP-K-016
[4] Use 400 ns Pulse

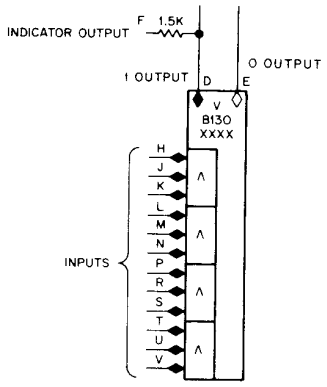
*Invert with higher speed inverter to obtain correct polarity
**Invert twice with higher speed series to obtain adequate risetime
†Direct except where pulse overlap or recovery problems occur

B.3 MODULES FOR PDP-9 or PDP-9/L INTERFACING

This section contains descriptions of R-, W, and B-series modules often used in PDP-9 interfaces. Many of these modules are listed in the Logic Handbook and are repeated here when they are referred to in interfacing examples; some are special DEC designs, not listed in the Logic Handbook, but available on request.

B130 THREE-BIT PARITY CIRCUIT

Standard Size FLIP CHIP Module, 18 Pins



Price - $50.00

This special module has two levels of high speed logic and complementary outputs. It is designed to compute the parity (odd or even) of the contents of a flip-flop register with a minimum of delay, but it can be used wherever there is a need for four 3-input negative diode AND gates feeding a 4-input OR gate.

Delay is typically 15 ns from 50% of the input transition to 50% of the output transition when output capacitive loading is very small.

INPUTS: The input load is 2 mA shared among the inputs of each AND gate which are at ground. Input load at -3V is less than 1 μA. When the inputs are connected to compute parity, the total load on each of the input lines is 2.67 mA or less. Pin D is at -3V whenever all three inputs to one or more of the AND gates are negative.

OUTPUTS: Each of the complementary outputs (pins D and E) can drive 10 mA at ground -7 mA at -3V (-6 mA at pin D when pin F is used). The output is a special emitter follower circuit.

An indicator output (pin F) is provided to drive an indicator driver circuit such as the W012-W250 indicator driver or the W020-4902 indicator driver with lamp.

POWER:

Pin	Voltage	Margin Range	Current
A	+10V	+4V to +16V	49 mA
B	-15V	-12V to -18V	92 mA
C	ground		

APPLICATION: The B130 can be connected to compute either even or odd parity by ORing the appropriate four of the eight possible 3-bit configurations together.

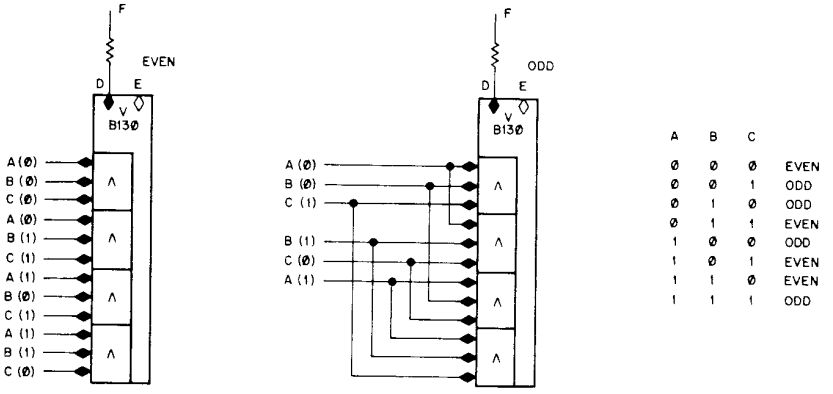
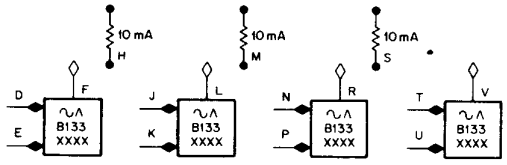


Figure B-3 B130 Connections, Odd and Even Parity

B133, B134, B135, B137, B163, B165, B167, B168 DIODE GATES

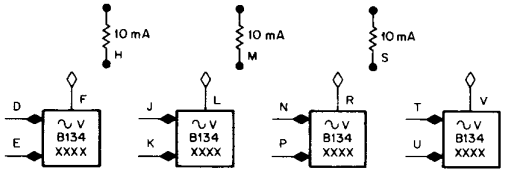
Standard Size FLIP CHIP Modules, 18 Pins

B133



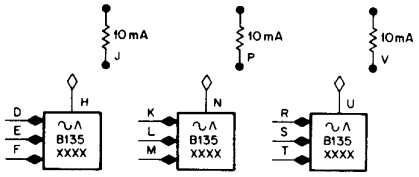
Price - $23.30

B134



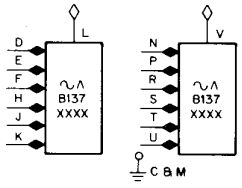
Price - $31.00

B135



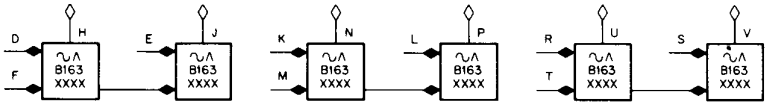
Price - $17.00

B137



Price - $13.00

B163

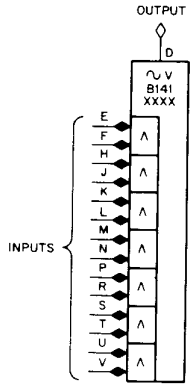


Price - $31.00

Note: Pins D, E, K, L, R, S include level terminator at input

B141 DIODE GATE

Standard Size FLIP CHIP Module, 18 Pins



Price $24.50

The B141 is a 2 mA diode gate used for performing AND/OR functions and register comparisons. It is typically used for register loading and driving I/O bus data lines. The B141 will operate from standard DEC 25 ns or 40 ns negative pulses, provided that adequate falltimes are maintained. It will also operate with standard DEC levels of ground and -3V. (Pulses 70 ns or wider are considered levels). Repetition rate may be limited to less than 10 MHz by slow falltimes.

INPUTS: Input load is 2 mA per input pair shared by the grounded inputs. When any pair is not being used, at least one of the two inputs must be grounded.

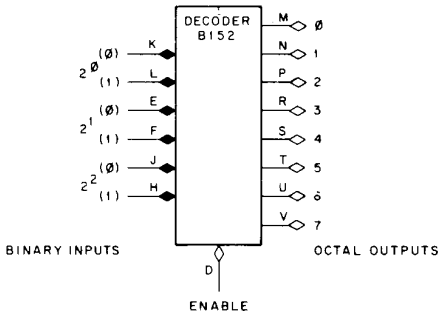
OUTPUT: Standard levels of -3V and ground. The output can drive 26 mA at ground (30 mA if slower rise and fall is adequate). Rise TTT is 15 ns or less; fall TTT is 50 ns or less. Fall delay is 20 ns or less. No clamped load is provided.

POWER:

Pin	Voltage	Margin Range	Current
A	+10V	0V to 20V	1.3 mA
B	-15V	-10V to -20V	19 mA
C	ground		

B152 BINARY TO OCTAL DECODER

Standard Size FLIP CHIP Module, 18 Pins



Price $34.00

This circuit decodes binary information from three flip-flops into octal form. The internal gates, including the enable gate, are high speed B-series 2 mA diode gates. Maximum repetition rate is slightly less than 10 MHz.

INPUTS: Standard levels of -3V and ground, with pulse widths 40 ns or greater. Each diode gate within the decoder draws 2 mA at ground which is shared among the input diodes which are at ground. The load at -3V is less than -1 μA for each diode input.

Binary: 4.7 mA or less when used as a decoder.

Enable: 2 mA when at ground. When the enable input is at ground, the selected output line is at ground and the deselected outputs are at -3V. When the enable input is at -3V, all outputs are at -3V.

OUTPUTS: Standard levels of -3V and ground. Each output can supply 26 mA at ground. A 5 mA or heavier clamped load must be used at each output. Output TTT with respect to binary inputs is 20 ns for rise and 35 ns for fall. With respect to the enable input, output TTT is 40 ns for both rise and fall (with 10 mA clamped loads). Simultaneous switching of outputs is not assured. If outputs are ORed together, the resultant output may contain spikes.

POWER:

Pin	Voltage	Margin Range	Current
A	+10V	0V to 20V	1.3 mA
B	-15V	-10V to -20V	19 mA
C	ground		

APPLICATION: In addition to a binary-to-octal decoder, the B152 may be used in any application where the internal gating structure is appropriate. The internal structure is shown below.

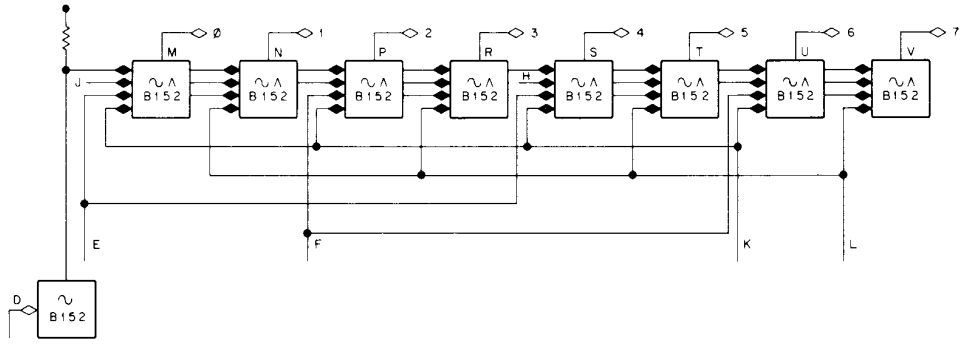
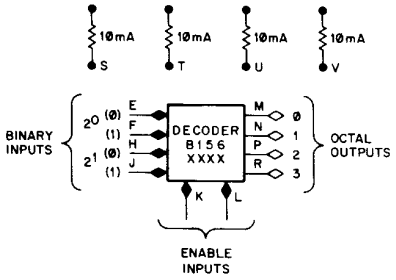


Figure B-4 Internal Gating Structure, B152 Module

B156 HALF BINARY-TO-OCTAL DECODER

Standard Size FLIP CHIP Module, 18 Pins



Price $25.00

The B156 module is used alone as a 2-bit decoder with two enable inputs, or it is used with another B156 to form a full 3-bit (binary-to-octal) decoder, with one combined enable line. Either way, each binary input combination results in one selected output held at ground if the decoder is enabled. No output will be selected if an enable input is held at ground. The decoder consists of four 4-input 2 mA diode gates with appropriate input connections. The B156 is often used as a high-speed decoder for unit-select or instruction-decoding applications.

INPUTS: Standard levels of -3V and ground, with pulse widths of 40 ns or greater. Each diode gate within the decoder draws 2 mA at ground which is shared among the input diodes which are at ground. When used as a decoder, the binary inputs draw 3 mA or less. When two B156s are used as a full binary-to-octal decoder, the binary inputs draw 4.7 mA or less. The load at -3V is less than -1 μA for each diode input.

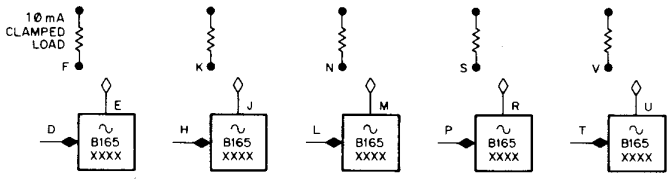
OUTPUTS: Standard levels of -3V and ground. Each output can supply 26 mA at ground. Output TTT is 30 ns maximum for rise and 45 ns maximum for fall when driving five 2 mA diode gates, a 10 mA clamped load, and 3 in. of connecting wire. Typical propagation time is 13 ns.

Simultaneous switching of B156 outputs is not assured. It outputs are ORed together, the resultant output may contain spikes.

POWER:

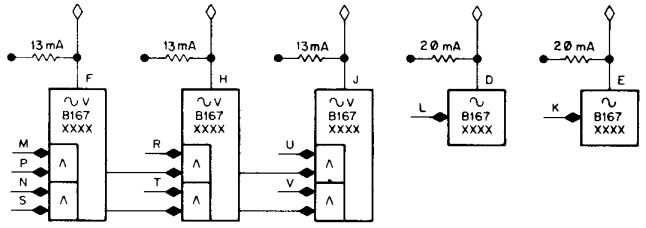
Pin	Voltage	Margin Range	Current
A	+10V	0V to 20V	.6 mA
B	-15V	-10V to -20V	56 mA
C	ground		

B165



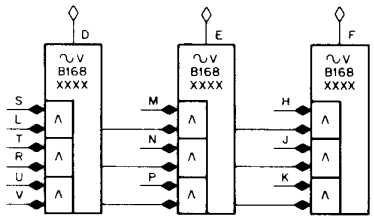
Price $21.20

B167



Price $34.00

B168



Price $31.00

The B-series 2 mA diode gates are used for perform- high speed AND/OR gating, register input gating, and general logic use. These gates operate from standard DEC 35-ns or 40-ns negative pulses (0V to -3V), provided that adequate falltimes are maintained (see technical notes below). These gates will also operate with standard DEC levels of ground and -3V. (Pulses 70 ns or wider are considered levels.) Collector outputs are provided in order to allow wired ORing at ground by paralleling outputs of gates. Simultaneous switching of outputs in decoding applications is not guaranteed; ORed outputs may contain spikes.

INPUTS: Each diode gate input is a 2 mA or greater load at ground, shared among the input diodes which are at ground. The loading at ground for all the diode gate inputs is given in Table B-2. The load at -3V is less than 1 μA for each diode input.

OUTPUTS: Each output of this series of gates can supply up to 26 mA at ground less that required by internal clamped loads. Risetimes and falltimes are listed in Table B-3.

Falltimes for logic levels may increase the effective width of standard pulse inputs, thus limiting the system repetition rate to less than 10 MHz. To calculate falltimes, follow the procedure detailed at the beginning of this chapter. The 10 mA clamped loads are adequate to maintain reasonable pulse width and pulse shape through several stages of gating, provided that capacitive loading is small and wire length are short. For other conditions, the 35 ns or 40 ns pulses should be regenerated with a pulse amplifier (B602, B611, etc.) after at most three stages of gating. Although these gates will not drive resistive terminators to ground at dc, satisfactory operation over long wires (65 ft, 20 m) can be obtained by terminating the far end of the driven line with a G796 or G704 level terminator.

Table B-2
Input Loading (at ground)

Module	2 mA	2.7 mA	3.2 mA	4 mA	6 mA	8.1 mA
B133	D and E, J and K, N and P T and U					
B134[1]	D,E,J,K,N,P,T,U					
B135	D and E and F, K and L and M, R and S and T					
B137	D and E and F and H and J and K, N and P and R and S and T and U					
B163	D,E,K,L,R,S[2]			F,M,T		
B165	D,H,L,P,T					
B167	N,M,T,R,V,U		K,L		S,P	
B168		H,J,K, N,M,P, T,U,S				L,R,V

[1]Each input to the B134 is a 2 mA load at ground; there is no load sharing between inputs.

[2]These inputs include a level terminator circuit and should only be used for signals which go from -3V to ground. Signals which attempt to go above ground (such as B611 outputs) are clamped at ground, and signals which attempt to go below -3V are clamped at -3V.

Table B-3
Technical Data

Type	Typical Propagation Delay* (ns)	Output Rise TTT Max.* (ns)	Output Fall TTT Max.* (ns)	+10V (pin A) Current Required (mA)	+10V (pin A) Margin Range	-15V (pin B) Current Required (ma)	-15V (pin B) Margin Range
B133	13	30	45	0.6	0V, 20V	48	-10V, -20V
B134	13	30	45	1.2	0V, 20V	54	-10V, -20V
B135	13	30	45	0.45	0V, 20V	44	-10V, -20V
B137	13	30	45	0.30	0V, 20V	4	-10V, -20V
B163	13	30	45	0.90	0V, 20V	30	-10V, -20V

Table B-3
Technical Data (Cont)

Type	Typical Propagation Delay* (ns)	Output Rise TTT Max.* (ns)	Output Fall TTT Max.* (ns)	+10V (pin A) Current Required (mA)	+10V (pin A) Margin Range	-15V (pin B) Current Required (ma)	-15V (pin B) Margin Range
B165	13	30	45	0.75	0V, 20V	68	-10V, -20V
B167	13	30	45	1.2	0V, 20V	107	-10V, -20V
B168	13	30	45	1.3	0V, 20V	24	-10V, -20V

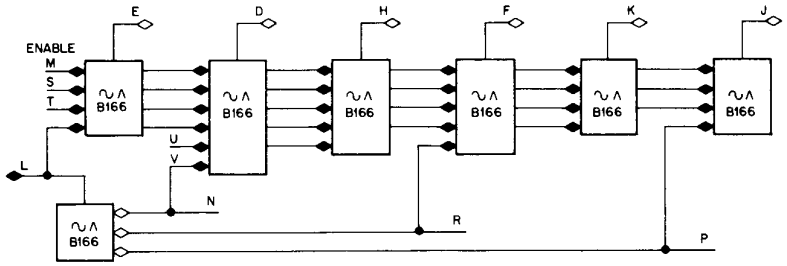
*Test Conditions: Five 2-mA diode gates as load, 10 mA clamped load total, 3 in. of connecting wire, gate under test driven by and driving standard 2 mA diode gates.

Pin C is ground on all modules. Both Pinc C and M of the B137 must be grounded.

POWER: Power and margins are listed in Table B-3. Margins assume 40-ns input pulses from a 2 mA diode gate with a 10 mA clamped load only. Operating margins are broader with wide pulses or with levels. With heavier loads, risetimes and falltimes are longer when the -15V supply is adjusted toward -10V due to decreased transistor drive and decreased clamped load current, causing narrower margins.

B166 COUNTING GATE

Standard Size FLIP CHIP Module, 18 Pins



Price $31.00

The B166 provides compact gating to implement an up counter or down counter using delayed flip-flops such as the B212. It is constructed out of 2 mA diode gates and will operate using standard DEC 35 ns or 40 ns negative pulses, provided adequate falltimes are maintained. This circuit will also operate with DEC standard levels of -3V and ground. (Pulses 70 ns or wider are considered levels.)

INPUTS: Each diode gate input is a 2 mA load at ground, shared among the input diodes which are at ground. The inputs to the positive NAND (whose output is pin L) each draw 2 mA at ground independent of the state of the other inputs. The load at -3V is less than 1 μA for each diode input.

OUTPUTS: Each diode gate output can supply up to 26 mA at ground. Output TTT of each diode gate is 30 ns maximum for rise and 45 ns maximum for fall. When driving five 2 mA diode gates, a 10 mA clamped load, and 3 in. of connecting wire. Typical propagation time is 13 ns. No internal clamped loads are supplied; external clamped loads must be supplied when necessary (usually for pin L at least).

POWER:

Pin	Voltage	Margin Range	Current
A	+10V	0V to 20V	1.3 mA
B	-15V	-10V to -20V	18 mA
C	ground		

APPLICATION: Part of a typical up-counter arrangement is shown in Figure B-5. The 3-bit section shown includes carry conditions from lower order stages and generates part of the carry condition for succeeding higher order stages. Notice that three input pins (N,R,P) are used for both the 1-high and 0-low states of a flip-flop. This is valid as these two signals are electrically equivalent.

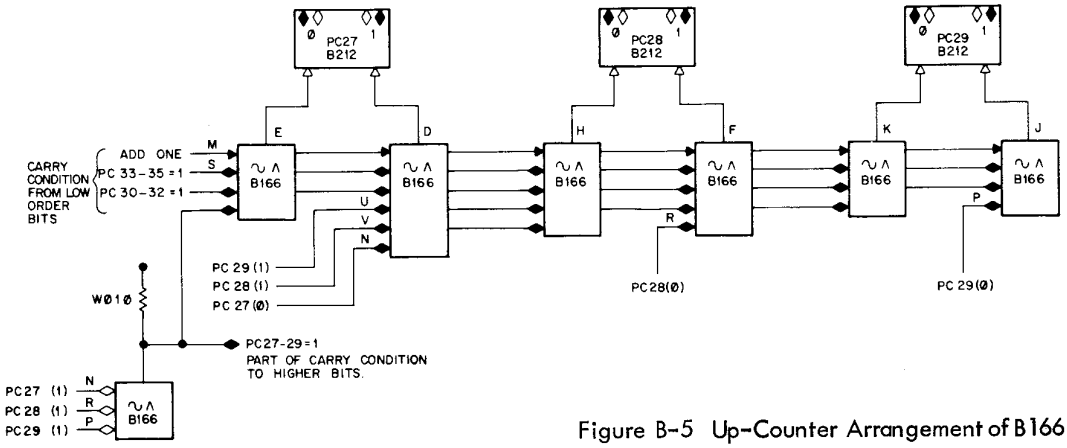
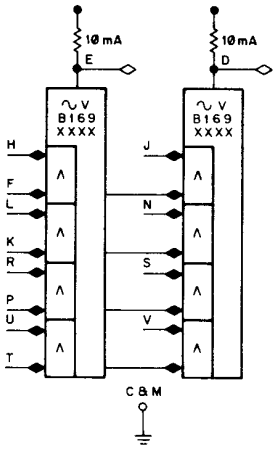


Figure B-5 Up-Counter Arrangement of B166 Module

B169 DIODE GATE

Standard Size FLIP CHIP Module, 18 Pins



Price $25.00

The B169 is a 2 mA diode gate used for performing AND/OR functions such as register input gating. The B169 will operate from standard DEC 35 ns or 40 ns negative pulses, provided that adequate fall-times are maintained. It will also operate with standard DEC levels of ground and -3V. (Pulses 70 ns or wider are considered levels.) Repetition rate may be limited to less than 10 MHz by slow falltimes.

INPUTS: Input load is 2 mA per input-AND pair shared by the grounded inputs. When any pair is not being used, at least one of the two inputs must be grounded.

OUTPUTS: Standard levels of -3V and ground. The output can drive 16 mA at ground (26 mA output minus 10 mA clamped load). If slower rise and fall is adequate, 22 mA can be driven. The internal clamped load will supply -7 mA at -3V. Typical TTT is 25 ns for output rise and 30 ns for output fall.

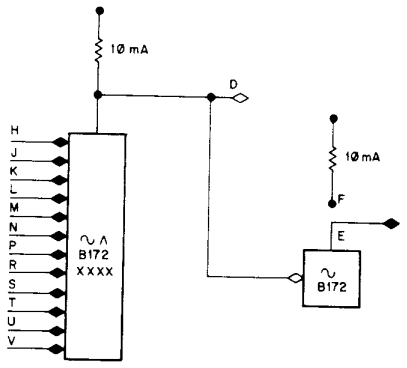
POWER:

Pin	Voltage	Margin Range	Current
A	+10V	+5V to +15V	.8 mA
B	-15V	-12V to -18V	42 mA
C,M	ground		

Both pins C and M must be grounded.

B172 DIODE GATE

Standard Size FLIP CHIP Module, 18 Pins



Price $18.00

The B172 provides a 12-input 2 mA diode gate with 2 mA diode inverter permanently connected to the output of the first gate.

INPUTS: The input load of the diode gates is 2 mA shared among the inputs which are at ground. Each diode input at ground represents 12 pF of capacitance. The input load at -3V is less than 1 μA plus 5 pF of capacitance at each input provided at least one input is at ground.

OUTPUTS: Pin D - This output can drive up to seven other 2 mA diode gates (14 mA at ground). The internal clamped load will supply -7 mA at -3V.

Pin E - This output can supply 26 mA at ground. The output capacitance is 3 pF. A 10 mA clamped load is available at pin F.

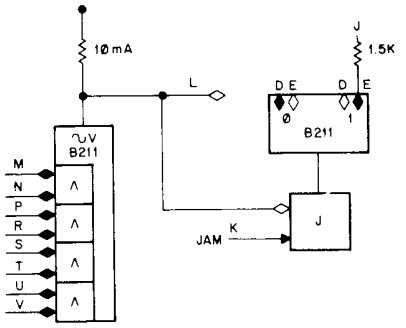
Typical propagation time through the first gate is 15 ns; through both gates, 25 ns. Rise TTT from input is 25 ns to pin D, 40 ns to pin E. Fall TTT from input is 40 ns to pin D, 35 ns to pin E. The output load for pin E is the clamped load at pin F for these measurements.

POWER:

Pin	Voltage	Margin Range	Current
A	+10V	0V to 20V	.3 mA
B	-15V	-10V to -20V	24 mA
C	ground		

B211 JAM FLIP-FLOP

Standard Size FLIP CHIP Module, 18 Pins



Price $43.00

The B211 provides a 2 mA diode gate AND/OR circuit driving a jam flip-flop similar to one half of a B213.

INPUTS: Diode gate - Standard DEC levels of -3V and ground. Input load is 2 mA per input pair shared by the grounded inputs. When any pair is not being used, at least one of its inputs must be grounded.

Jam - A standard DEC 40 ns or longer negative pulse or a level change greater than -1V in 12 ns will set or clear the flip-flop. Input load is -5 mA at -3V and 31 pF. Maximum repetition rate is 10 MHz. Rise and fall TTT from the jam input to the output is less than 40 ns.

Pin L - Standard DEC levels of -3V and ground. This pin may be used to expand the input capability of the flip-flop. Load at ground is 12 mA (10 mA clamped load plus 2 mA input load). The clamped load will supply -7 mA at -3V. The input must be settled at -3V or ground 20 ns before the jam input is pulsed. If pin L is at ground when the jam input is pulsed, pin E will go negative (the flip-flop will be set).

OUTPUTS: Flip-Flop Standard levels of -3V and ground. Each output can drive 36 mA at ground. The internally connected clamped load will supply -7 mA at -3V (-6 mA at pin E when the indicator output is used).

Indicator - A resistor output is provided to drive an indicator driver circuit such as the W012-W250 indicator driver or the W020-4902 indicator driver with lamp.

Pin L - The output of the diode gate may be used to perform additional logic provided that the set-up required above is met. The diode gate will drive 14 mA in addition to the internally connected loads.

POWER:

Pin	Voltage	Margin Range	Current
A	+10V	+5V to +15V	17 mA
B	-15V	-12V to -18V	82 mA
C	ground		

NOTE

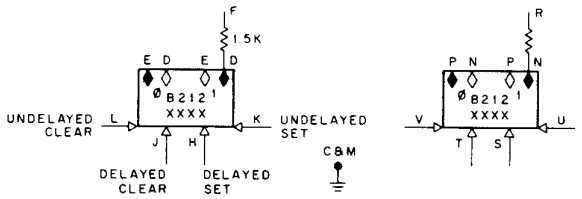
This description applies to B211 flip-flops revision E or later.

CAUTION

The B211 flip-flop may be damaged if its output is grounded when one or more of its inputs is active.

B212 DELAYED FLIP-FLOP

Standard Size FLIP CHIP Module, 18 Pins



Price $72.00

The B212 standard size FLIP CHIP module contains two clear-set flip-flops with buffered outputs and individual delayed and undelayed set and clear inputs.

INPUTS: Undelayed - Undelayed inputs must be driven from the collector of a diode gate and require an external clamped load. A total of five B212 undelayed inputs may be driven from one 2 mA diode gate collector if a 5 mA clamped load is used. For driving four or less B212 direct inputs a 10 mA clamped load may be used. Undelayed inputs require 5.5 mA at ground and 0 mA at -3V. The B212 will operate at 10 MHz; therefore, undelayed input pulses may occur at a 5 MHz repetition rate. The input to the 2 mA diode gate driving the B212 undelayed input should be a standard 40 ns or longer negative pulse. The state of the flip-flop after the simultaneous application of set and clear pulses is undefined.

Delayed - Delayed inputs contain an internal 2 mA clamped load and must be driven from the collector of a diode gate. Two delayed inputs may be driven from the collector of one 2-mA diode gate. The B212 delayed input requires 14 mA at ground for a 35 ns or 40 ns pulse and 2 mA at -3V. A longer pulse or level is loaded with 22 mA at ground. Maximum repetition rate for any delayed input is 5 MHz. The input to the diode gate driving the delayed input of the B212 must be a standard 35 ns or longer pulse. Output delay time is 40 ns minimum and 60 ns maximum measured from the input of the diode gate driving the delayed input.

OUTPUTS: Logic - Standard ground and -3V levels. Each output can drive 40 mA of external load at ground and -7 mA at -3V (-6 mA at pin D, N when the indicator output is used). A total of twenty 2-mA diode gates may be driven at 10 MHz provided that the wiring is kept very short.

Indicator Drive - Pins F and R apply the 1-low output through a 1.5 KΩ resistor to an indicator driver such as the W012-W250 or W020-4902.

POWER:

Pin	Voltage	Margin Range	Current
A	+10V	2.5V to 17.5V	50 mA
B	-15V	-10V to -20V	120 mA
C,M	ground		

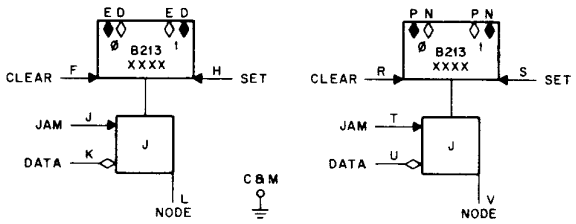
Pins C and M must both be grounded.

CAUTION

The B212 flip-flop may be damaged if its outputs are grounded when one or more of its inputs is at ground. To manually set or clear the flip-flop ground the input.

B213 JAM FLIP-FLOP

Standard Size FLIP CHIP Module, 18 Pins



Price $42.00

The B213 provides two jam transfer (C-D) flip-flops. It is often used in combination with the B169 diode gate to form a general purpose register; it is also useful as a complementary bus driver.

INPUTS: Data - Standard DEC levels of -3V and ground. Input load is 2 mA shared among those inputs (pin K or U and expansion inputs) which are at ground. The inputs must be settled at -3V or ground 20 ns before the jam input is pulsed.

Node - The node can be used to expand the data input using R001 or R002 diode networks. Short wires must be used between the node and diode networks. If any data input is at ground when the jam input is pulsed, pin D, N will go negative (the flip-flop will be set). If all data inputs are at -3V, pin E,P will go negative (the flip-flop will be cleared).

Jam - A standard DEC 40-ns negative pulse or a level change greater than -1V in 12 ns will set or clear the flip-flop. Input load is -5 mA at -3V and 31 pF. Maximum repetition rate is 10 MHz. Rise and fall TTT from the jam input to the output is less than 40 ns.

Direct Set or Clear - Standard DEC 40 ns negative pulses. Input load is -10 mA at -3V. The result of pulsing both the set and clear inputs is not defined. The set and clear inputs may be left open when not in use.

OUTPUTS: Standard DEC levels of -3V and ground. All outputs can drive 36 mA at ground or 2 base loads at 10 MHz. (A base load is -1 mA and 60 pF.) The internally connected clamped loads will supply -7 mA at -3V.

POWER:

Pin	Voltage	Margin Range	Current
A	+10V	+8V to +12V	32 mA
B	-15V	-12V to -18V	80 mA
C,M	ground		

Both pins C and M must be grounded.

CAUTION

The B213 flip-flop may be damaged if its outputs are grounded when one or more of its inputs is active.

APPLICATIONS: Redefining the B213 output pins provides a jam (C-D) flip-flop with a negative data input (See Figure B-6.)

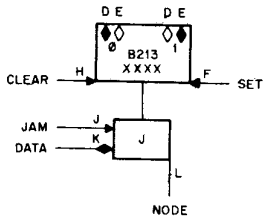


Figure B-6 B213 With Negative Data Input

The B213 can also be used as a dual complementary bus driver by connecting the jam input to a source of -3V such as a free clamped load. (See Figure B-7.)

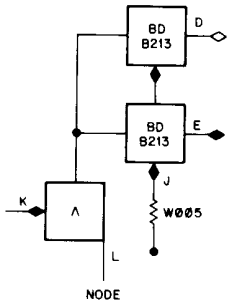
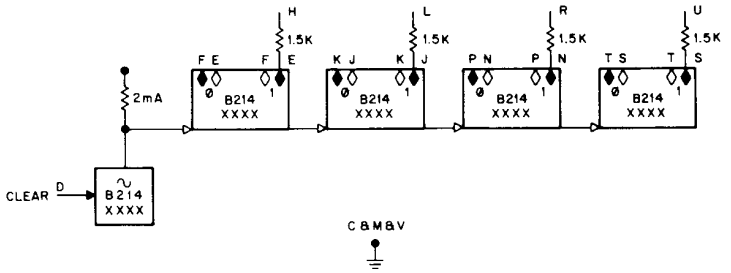


Figure B-7 B213 As Bus Driver

B214 FLIP-FLOPS

Standard Size FLIP CHIP Module, 18 Pins



Price $31.00

The B214 contains four unbuffered flip-flops. The module is pin-compatible with the B204, but has improved noise rejection and a 2 mA diode inverter clear input.

INPUTS: Each flip-flop may be individually set or cleared by grounding the 1-high or 0-high output. The collector of a 2 mA diode gate driven by a 35 ns or longer pulse may be used to ground a flip-flop output. Diode gates such as B113, B115, B117, etc., may also be used, but due to their slower operation they must be conditioned "on" for at least 70 ns to provide adequate drive. When switching, the output of the negative-going side must reach -1.4V to latch the flip-flop; the driving signal must be present until this occurs. A negative level at least 35 ns wide applied to the input of the inverter clears all four flip-flops. Clear input loading is 2 mA at ground. If the clear input of the B214 is allowed to fall, all flip-flops clear; then if one stage is driven to the 1 state, it holds that state as long as the driving signal is present. However, when the driving signal is removed the flip-flop falls back to the 0 state, if the clear signal is still present. If the clear input is not used, it must be grounded.

OUTPUTS: Each flip-flop output can drive 20 mA of external load at ground or -6 mA at -3V (-5 mA when the indicator output is used). For flip-flops driven by 2 mA diode gates with 35-ns pulse inputs, each side of the flip-flop can be loaded with five 2 mA diode gates and 100 pF.

The 1500Ω resistor outputs allow an indicator driver circuit such as the W012-W250 or W020-4902 to be used. The wire to the W012 or W020 should be short.

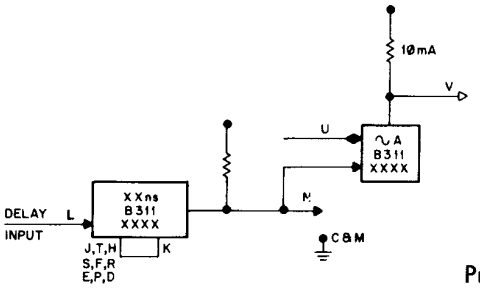
POWER:

Pin	Voltage	Margin Range	Current
A	+10V	0V to 20V	0.6 mA
B	-15V	-8V to -20V	50 mA
C,M,V	ground		

Pins C,M, and V must all be grounded.

B311 TAPPED DELAY LINE

Standard Size FLIP CHIP Module, 18 Pins



Price $64.00

The B311 consists of a tapped delay line with suitable buffering and a connected 2 mA diode gate. Delay time is selected by connecting pin K to a delay line tap (see delay control below.) This module has the same pin connections and can be used in the same slot as the B312 variable delay line module.

INPUTS: Delay Input - The standard input to pin L is a negative 35 ns pulse from a B611 PA. Loading is equivalent to a 75Ω resistance in series with a 68 pF capacitance. For levels, the static input load is -7 mA at -3V, 0 mA at ground, dynamic load is negligible. The input may be driven by a clamped load drawing 10 mA at ground. The B311 may be driven by a 2-mA diode gate with clamped load, but pulses will tend to become wider than normal.

Gate Input - Standard levels of -3V and ground. Loading is 2 mA shared by the gate inputs at ground, 0 mA at -3V. The gate is a 2 mA diode gate.

OUTPUTS: When the delay input is driven with 35 ns negative pulses, output N delivers negative pulses with no overshoot (ground to -3V) from 50 to 70 ns wide at the -1V points. If pin U is at -3V, pin V delivers positive pulses (-3V to ground) of the same width.

Pins N and V each drive 22 mA at ground in addition to the clamped loads and other gates tied internally. Each clamped load drives -7 mA at -3V.

DELAY CONTROL: The delay time is selected by connecting pin K to delay tap pins D, E, F, H, J, P, R, S, T of the same B311 card. No other use for pin K is intended. The wire from pin K to the tap should be as short as possible.

The delay from pin L to pin N measured at the -1V point on the waveforms can be predicted by the formula:

L to N delay = tap delay + 16 ± 3 ns.

where the tap delay is from the table below.

Pin K connected to Pin	Tap Delay
J	50 ns
T	75 ns
H	100 ns
S	125 ns
F	150 ns
R	175 ns
E	200 ns
P	225 ns
D	250 ns

The delay from pin N to pin V at the -1V point depends on the loads at pin N and pin V, but for a fanout of 2 or less from pins N and V and wire runs less than 3 in., 9 to 12 ns delay is typical.

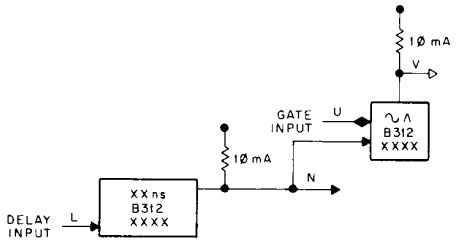
POWER:

Pin	Voltage	Margin Range	Current
A	+10V	+2.5V to +20V	10 mA
B	-15V	-10V to -20V	56 mA
C,M	ground		

Pins C and M must both be grounded.

B312 ADJUSTABLE DELAY LINE

Standard Size FLIP CHIP Module, 18 Pins



Price $65.00

The B312 is an adjustable delay line with suitable buffering driving a standard 2 mA diode gate. The delay is set by a screwdriver adjustment accessible from the handle end. This module has the same pin connections and can be used in the same slot as the B311 tapped delay line module.

INPUTS: Delay Input - The standard input is a negative 35 ns pulse from a B611 PA. Loading is equivalent to a 250Ω resistance to ground. For levels, the static input load is -12.5 mA at -3V, 0 mA at ground; dynamic load is negligible. The input may be driven by a clamped load drawing 15 mA at ground. The B312 may be driven by the output of a 2 mA diode gate with clamped load, but pulses will tend to become wider than normal.

Gate Input - Standard levels of -3V and ground. Loading is shared by the gate inputs at ground, 0 mA at -3V. The gate is a 2 mA diode gate.

OUTPUTS: When the delay input is driven with 35-ns negative pulses, output N delivers negative pulses with no overshoot (ground to -3V) from 40 to 80 ns wide at the -1V points. If pin U is at -3V, pin V delivers a positive pulse (-3V to ground) of the same width.

Pins N and V each drive 22 mA at ground in addition to the clamped loads and other gates tied internally. Each clamped load drives -7 mA at -3V.

DELAY CONTROL: The delay from pin L to pin N, measured at the -1V on the waveforms, can be adjusted from 20 ns to 215 ns. The delay from pin N to pin V at the -1V point depends on the loads at pin N and pin V, but for a fanout of 2 or less from pins N and V and wire runs less than 3 in., 9 to 12 ns delay is typical.

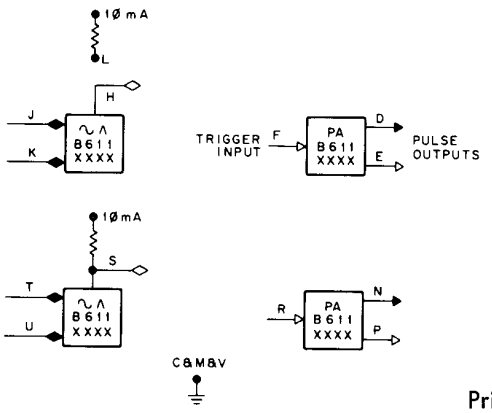
POWER:

Pin	Voltage	Margin Range	Current
A	+10V	+2.5V to +20V	4.7 mA
B	-15V	-10V to -20V	34.4 mA
C,M	ground		

Pins C and M must both be grounded.

B611 PULSE AMPLIFIER

Standard Size FLIP CHIP Module, 18 Pins



Price $42.00

The B611 contains two independent 10 MHz 35-ns pulse amplifiers for power gain and pulse standardization. Two 2-input diode gates increase the logic flexibility.

INPUTS: Gate Inputs - Input load is 2 mA shared by the grounded inputs of each gate. Load at -3V is less than 1 μA.

Trigger Inputs - The input to each pulse amplifier is a diode gate which is a 1 mA load at ground and no load at -3V. The PA is triggered by positive-going pulses or level transitions (-3V to ground) which are 25 ns or wider at the -1.5V point at the PA input. The PA produces output pulses for any spacing of input pulses above a minimum of 100 ns, provided that the input is at -3V for at least 50 ns before going to ground. The PA may be driven by any circuit which meets the above requirements. Gates may be collector ORed at the PA input, provided that the wiring is kept short, stray capacitance is minimized and the above rules are followed. Up to four PA inputs may be driven from one diode gate collector.

OUTPUTS: Gate Outputs - The diode gate output at pin S has a 10 mA clamped load connected internally and therefore can supply 16 mA drive at ground and -8 mA at -3V. The diode gate output at pin H has no internal clamped load and therefore can supply 26 mA at ground and no current at -3V. A 10 mA clamped load is available at pin L. These diode gates are suitable for driving the B611 PA input.

Pulse Outputs - The PA output is from the secondary of a transformer so that positive or negative pulses are available by grounding the appropriate pin. The PA output is capable of driving eighteen 2-mA diode gate loads if careful consideration is given to the wiring and termination. In general, a 100Ω termination at the last gate in the line provides the proper termination; each case should be examined to see if that is adequate. For a negative pulse output (pin E or P grounded), the pulse width is 30 to 40 ns, measured at the -1.5V point, the output amplitude is -3V, delay from PA input to output is 20 ns or less, and the transformer backswing is +4V, all of which are measured at the PA output. Corresponding values apply to a positive pulse output. There is approximately 1-ns additional delay through the PA for each diode gate collector that is ORed at the PA input.

NOTE

Transistors with low BV_{cbo} should not be driven by negative pulses from the B611. The +4V backswing from a negative pulse may cause breakdown.

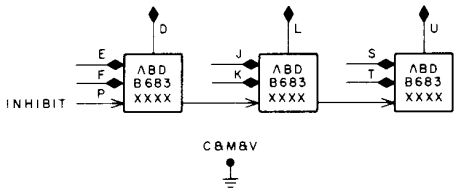
POWER:

Pin	Voltage	Margin Range	Current
A	+10V	0V to 20V	0.66 mA
B	-15V	-10V to -20V	134 mA
C,M,V	ground		

Pins C, M, and V must all be grounded. One side of each pulse transformer output used must be grounded (D or E, N or P).

B683 BUS DRIVER

Standard Size FLIP CHIP Module, 18 Pins



Price $50.00

The B683 is the level counterpart of the W102 pulsed-bus transceiver. It is designed to drive two 100Ω transmission lines terminated to ground in their characteristic impedance. A single, terminated 50Ω transmission line can be driven instead. The output impedance of the B683 is zero when the output is low (-3V) and infinite when high (ground), or when the power is off. Thus, two or more of these drivers may be attached to the same line in a "wired OR" fashion.

INPUTS: The input is that of a two input 2 mA diode AND gate. When both inputs are low, the output is also low. The input load is 2 mA shared by those inputs at ground, 0 for those inputs at -3V.

An inhibit input is provided on pin P. If this input is held at ground (for example, by the CROBAR relay contact on the 844 Power Control, possibly through an isolating diode) power-on, power-off transients are prevented from causing the outputs to go negative. This input normally is at -5.3V and must not be tied to any other potential if normal operation is expected. Load is 30 mA at ground.

OUTPUTS: The outputs will supply -60 mA to a 50Ω load at -3V. The output circuit will tolerate short circuit operation for a short time (tens of seconds) but this type of operation is not recommended. Typical TTT is 30 ns.

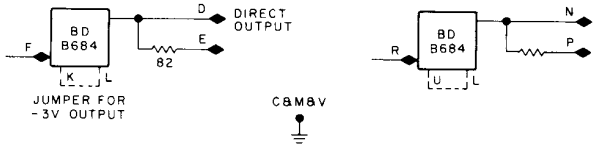
POWER:

Pin	Voltage	Margin Range	Current
A	+10V	0V to 20V	0.4 mA
B	-15V	-12V to -18V	350 mA
C,M,V	ground		

Pins C, M, and V must all be grounded.

B684 BUS DRIVER

Standard Size FLIP CHIP Module, 18 Pins



Price $52.00

The B684 contains two dual-purpose, non-inverting bus drivers. Each bus driver provides standard DEC levels of -3V and ground to a large number of diode gates and "inverter base loads" (an inverter base load is a load of -1 mA at -3V and 60 pF). Alternatively, the bus driver will drive a terminated cable of 90Ω characteristic impedance.

INPUTS: Standard levels of -3V and ground. Load is -1 mA at -3V, 0 mA at ground. Input wiring must be kept relatively short (less than 3 ft).

OUTPUTS: Direct - Standard levels of -3V and ground. The direct output will drive 40 mA at ground and -80 mA at -3V. A 100Ω cable terminated at each end by 100Ω resistors to ground can be driven by this output. The level control pins must be jumpered when the direct output is used.

Resistor - Levels of ground and -6V at the resistor output provide standard ground and -3V levels at the end of a 93Ω cable terminated with 100Ω to ground. The terminated cable will drive ± 10 mA at 10 MHz. The level control pins must be left open when driving terminated cable from the resistor output.

For driving 5 mA loads or less, an unterminated cable or open wire may be driven from the resistor output using ground and -3V levels. This connection allows heavy local load and light distant loads on one circuit.

Typical delay through the bus driver is 30 ns.

The output can be held at approximately ground, independent of the input and of power-on, power-off transients, by bringing the level control pin (K,U) to ground with the CROBAR relay contacts of an 844 Power Control (possibly through an isolating diode). Approximately 50 mA is required.

POWER:

Pin	Voltage	Margin Range	Current
A	+10V	-6V to +20V	80 mA[1]
B	-15V	-12V to -18V	120 mA[2]
C,M,V			

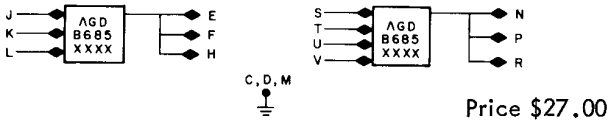
Pins C, M, and V must all be grounded.

[1] Plus the current required to bring the loads to ground.

[2] Plus the current required to bring the loads negative.

B685 DIODE GATE DRIVER

Standard Size FLIP CHIP Module, 18 Pins



Price $27.00

The diode gate driver circuit consists of a diode AND gate controlling a current-mode switch, the output of which is buffered with a complementary emitter follower of asymmetric drive capability. Both circuits are identical except that one diode AND gate has four inputs while the other has three. Both circuits are non-inverting.

INPUTS: The input load shared by the diode inputs is 2.5 mA at ground and 0 mA at -3V. The capacitive load of each input is 11 pF at ground and 4.5 pF at -3V. Propagation delay is about 20 ns.

OUTPUTS: Each output circuit drives up to 36 2 mA diode gates (or 80 mA) at ground, and sinks up to 8 mA at -3V. There are three pins per output. The output load should be split among the three pins to allow adequate signal transmission. Each output has a separate pin brought out for grounding.

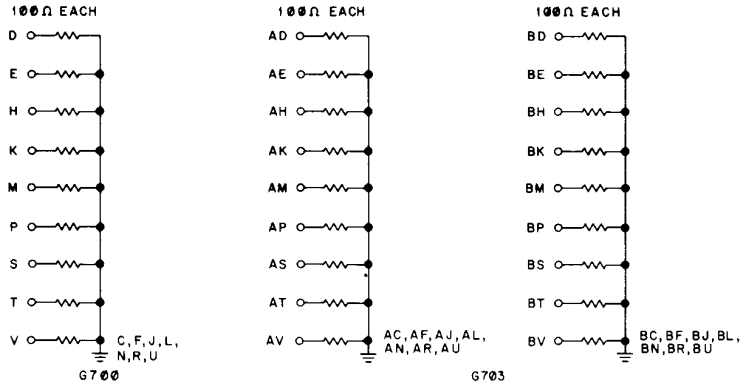
POWER:

Pin	Voltage	Margin Range	Current
A	+10V	+6V to +16V	65 mA
B	-15V	-10V to -20V	100 mA
C,D,M	ground		

Pins C, D and M must all be grounded.

G700, G703 100Ω TERMINATORS

Standard Size FLIP CHIP Module, 18 Pins



Price $8.00

The G700 provides nine 100Ω resistive terminators for use in terminating standard 9-circuit cables such as W021 cable assemblies. It is designed to plug into the same module locations as the cable assembly facilitiating future extension of the cable. The G700 is useful for terminating transformer-coupled pulse-amplifier outputs such as are found on the B611.

The G703 is a double width FLIP CHIP module with 36 pins. It provides 18 100Ω resistive terminators for use in terminating standard dual 9-circuit cables such as W851 cable assemblies. The G703 is notched to fit in a module location which has been provided with nylon cable retaining blocks such as the H003 or H004, which hold BC09A FLIP CHIP cables to module blocks. Thus, the G703 can be used to terminate a bus by plugging it into the same location that future bus extension cables plug into.

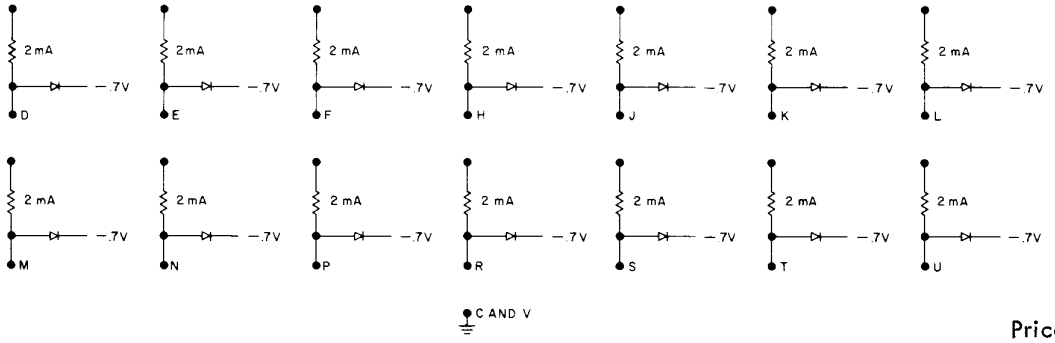
INPUTS: Each input pin has a 100Ω ±10% 1/4W carbon resistor to ground.

GROUNDS: All ground pins must be grounded. The "A" and "B" ground buses of the G703 are not internally connected.

POWER: No power is required. Power connections to pins A and B (G700) or AA, AB, BA and BB (G703) are optional. These pins are not connected to anything internally.

G704 2 mA LEVEL TERMINATOR

Standard Size FLIP CHIP Module, 18 Pins



Price $30.20

The G704 provides fourteen 2-mA level terminator circuits; that is, level terminator circuits combined with 2 mA clamped loads. It is used to control overshoots and ringing on long or heavily loaded level lines as described in the wiring guidelines (see Chapter 5).

INPUTS: Each circuit will prevent the signal to which it is connected from going below -3V (-3.5V) and from going above approximately ground. Thus, it can be used only on signal lines which have standard DEC levels of -3V and ground. The clamped load draws 2 mA at ground and will supply -1.6 mA at -3V.

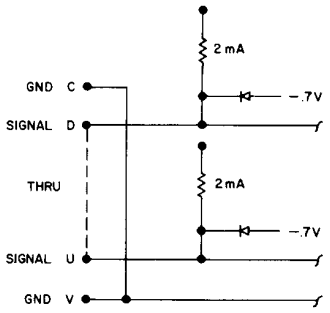
POWER:

Pin	Voltage	Margin Range	Current
A	not used - connection optional		
B	-15V	-7.5V to -20V	60 mA
C,V	ground		

Pins C and V must both be grounded.

G796 LEVEL TERMINATING CABLE CONNECTOR

Standard Size FLIP CHIP Module Without Handle, 18 Pins



DEC #7005469
G796-G796
Level Terminator Assembly is $75.00

The G796 cable connector provides an end for 14 circuit cables formed from 2 flat, flexible cables made of Flex Print or Tape Cable. A 2 mA level terminator (level terminator plus 2 mA clamped load) is connected to each signal line to control overshoot and ringing as described in Chapter 5. Only signals using DEC standard levels of -3V and ground can be transmitted through this cable. All signal lines are separated by at least one grounded line in the cable to reduce cross-talk.

SIGNAL CIRCUITS: Circuits suitable for transmission of DEC standard levels of -3V and ground are available at pins D, E, F, H, J, K, L, M, N, P, R, S, T, and U. Load is 4 mA at ground (2 mA at each end). -3.2 mA is supplied at -3V to discharge capacitance.

POWER: (at each end of the cable)

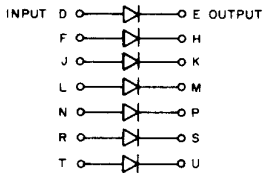
Pin	Voltage	Margin Range	Current
A	not used - connection optional		
B	-15V	-7.5V to -20V	60 mA
C,V	ground		

Pins C and V must both be grounded.

CABLE: The G796-G796 Tape Cable assembly is available as DEC part number 7005469. The length must be specified. Length is measured from the back end (handle end) of each cable connector.

R001, R002 DIODE NETWORKS

R001 Diode Network

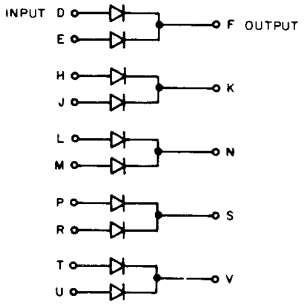


Price: $4.00

Diode networks can expand the logic capability of any R-series, W-series, or A-series module which has one or more node inputs, such as the R111 Diode Gate. They also permit ORing into an R-series flip-flop output terminal for setting or clearing from several sources.

Diode networks cannot be cascaded to perform other logic operations.

R002 Diode Network

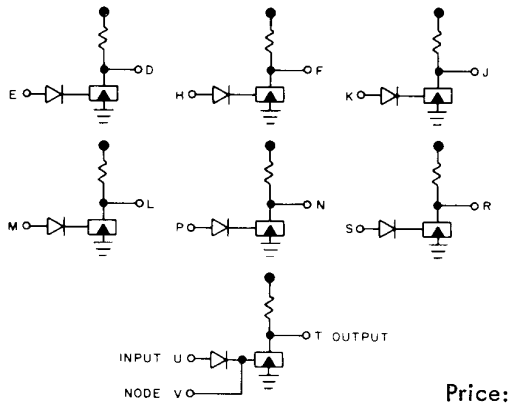


Price: $5.00

Propagation delay of R-series gates expanded by R001 or R002 diodes will increase typically 15 to 30 ns when gate output rises from -3V to 0V, but will not change noticeable when gate output falls from 0V to -3V. Diodes used are similar to type IN3606.

R107 INVERTER

R107 Inverter



Price: $24.00

The R107 inverter contains seven inverter circuits with single-input diode gates. Six of the circuits are used for single-input inversion; the seventh circuit can be used for gating by tying additional diode input networks to its node terminal. Clamped load resistors of 2 mA are a permanent part of each inverter.

INPUT: Diode - Standard levels of -3V and ground, 100 ns minimum duration. Input load is 1 mA, shared among the inputs that are at ground.

Node Terminal - Accepts only R001 or R002 Diode Networks or their equivalent. The combined length of all leads attached to the node terminal must not exceed 6 in. Input signal and load characteristics for diode networks are the same as those given for the diode input above.

OUTPUT: Standard levels of -3V and ground. Each inverter can drive 18 mA of load at ground. Output terminals of inverters may be connected in parallel.

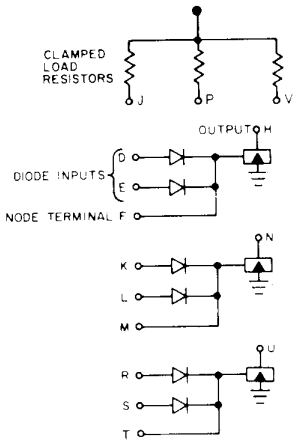
Some typical propagation delays are shown below. High frequency logic designs may benefit from the application note "Estimating Propagation Delays."

Fan-out	4	10	16
Output Rise	30 ns	35 ns	40 ns
Output Fall	60 ns	100 ns	140 ns

POWER: +10V(A)/0.7 mA, -15V(B)/30 mA.

R111 EXPANDABLE NAND/NOR GATE

Expandable NAND/NOR Gate



Price: $14.00

The R111 contains three diode gates, each connected to a transistor inverter. The gate operates as a NAND for negative inputs, and as a NOR for ground inputs. Each gate has three input terminals: two are connected to diodes, a third is connected directly to the node point of the diode gate. The third terminal allows the number of input diodes to be increased by adding external diode networks such as the R001 or R002. External diodes must be connected in the same direction as the diodes in the R111. Unused inputs may be left open.

INPUT: Diodes - Standard levels of -3V and ground, 100 ns minimum duration. Input load is 1 mA, shared among the inputs that are at ground.

Node Terminal - Accepts only R001 or R002 networks or their equivalent. The combined length of all leads attached to the node terminal must not be greater than 6 in. Input signal and load characteristics for the diode networks are the same as those given for the diode above.

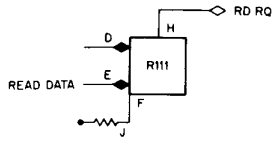
OUTPUT: Standard levels of -3V and ground. Each output can drive 20 mA of load at ground. Clamped load resistors are included in the module. Each clamped load resistor represents 2 mA of load. The output terminals of diode gates may be connected in parallel. Two gates in parallel (driven by the same signal) can drive 38 mA at ground (20 mA each, less the 2 mA clamped load). If they are not driven by the same signal, gates in parallel drive 20 mA at ground minus 2 mA for each clamped load used. Some typical propagation delays are shown below. High frequency logic designs may benefit from the application note "Estimating Propagation Delays."

Fan-out	4	10	16
Output Rise	30 ns	35 ns	40 ns
Output Fall	60 ns	100 ns	140 ns

POWER: +10V(A)/0.3 mA, -15V(B)/18 mA

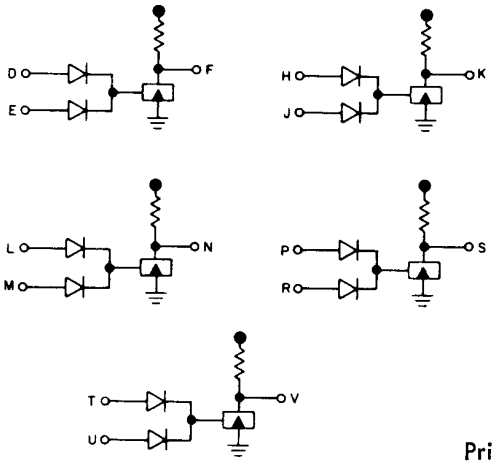
APPLICATION: The R111 is often used to drive the PDP-9 computer lines as in the example shown below.

By connecting the clamped load to the input node of the R111, this gate will drive 27 mA of load at ground.



NAND/NOR GATE

R113 NAND/NOR Gate



Price $20.00

The R113 contains five diode gates, each connected to a transistor inverter. The gate operates as a NAND for negative inputs, and as a NOR for ground levels.

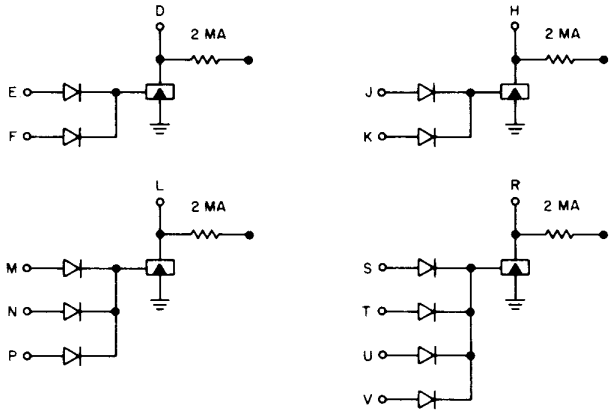
INPUTS: Standard levels of -3V and ground, 100 ns minimum duration. Input load is 1 mA shared among the inputs at ground. Unused inputs may be left open.

OUTPUT: Standard levels of -3V and ground. Each output can drive 18 mA of load at ground. Outputs terminals may be connected in parallel. Clamped loads included in the module are 2 mA each. Some typical propagation delays are shown below. High frequency logic designs may benefit from the application note "Estimating Propagation Delays."

Fan-out	4	10	16
Output Rise	30 ns	35 ns	40 ns
Output Fall	60 ns	100 ns	140 ns

POWER: 10V (A)0.5 mA, -15V (B)23 mA

R121 NAND/NOR Gate



Price $17.00

The R121 contains four R111-type circuits with 2 mA loads internally connected to each output. This module increases density at the expense of flexibility, since gate expanders R001 and R002 cannot be used.

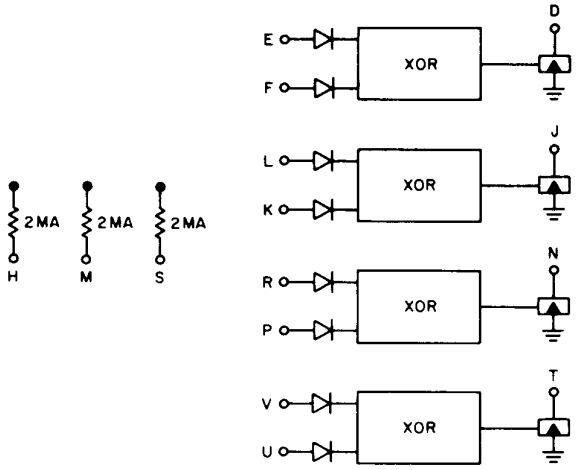
INPUT: Standard levels of -3V and ground, 100 ns minimum duration. Input load is 1 mA, shared among the inputs that are at ground.

OUTPUT: Standard level of -3V and ground. Each output has a permanently attached 2 mA clamped load resistor. Each output can drive 18 mA of load at ground. Delays are similar to R111 delays. See application note "Estimating Propagation Delay" for more information.

POWER: +10V(A)/0.4 mA, -15V/20 mA.

R131 EXCLUSIVE OR

R131 Exclusive OR



Price $35.00

This module provides a convenient way to compare two binary numbers or patterns. The output of each circuit is negative if its inputs are the same, and ground if they are different. If the outputs of several circuits are tied together, the common output line will be negative if every input pair matches, ground if any pair doesn't match.

During the transition from one input pattern to another with the same output, there is an interval during which the R131 output may be wrong for both patterns. Transitions between unequal inputs have a relatively short settling time, but transitions between equal inputs may produce transients to ground lasting 250 ns or more.

INPUTS: Standard levels of -3V and ground. Each input is a 2 mA load at ground.

OUTPUTS: Standard levels of -3V and ground. Each output can drive 18 mA at ground. Propagation delay for output rise is similar to R111 delay. Propagation delay for output fall is typically 300 ns longer than R111 delay.

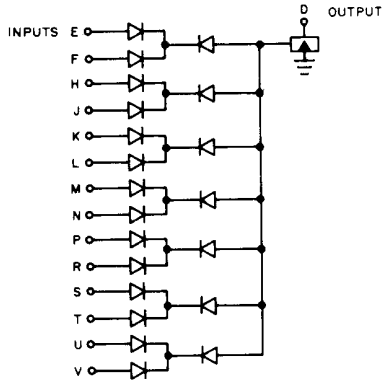
POWER: +10V(A)/0.8 mA; -15V(B)/36 mA.

TRUTH TABLE

Input E (K, P, U)	Output D(J, N, T)	Input F (L, R, V)
0V	0V	-3V
-3V	0V	0V
0V	-3V	0V
-3V	-3V	-3V

R141 AND/NOR GATE

R141 AND/NOR Gate



Price $13.00

The R141 AND/NOR Gate performs two levels of gating. The module contains a multiple = input diode gate with a transistor inverter for signal amplification. For negative input signals the R141 is seven 2-input AND gates which are NORed together. For ground inputs, it is seven 2-input OR gates NANDed together. This module is frequently used to mix multiple inputs to a pulse amplifier, or to compare the contents of two flip-flop registers.

The back-to-back diode circuits are possible because of an internal bias resistor connected to the input of each second stage diode. The bias holds the input of the second stage at -3V unless one of the first stage inputs is grounded. Propagation delay for output rise is similar to R111 delay. For output fall, delay is typically 100 ns longer than R111 delay under similar loading conditions, assuring sufficient pulse stretching to allow 70 ns inputs. Output is typically too wide, however, to allow 2 mc rates. Maximum rate depends upon R141 loading, and may be as low as 1 mc.

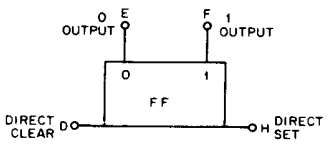
INPUT: Standard 100 ns pulses, standard levels of -3V and ground, or 70-ns negative pulses such as those generated by the W607 Pulse Amplifier. Input load is 1 mA per input pair shared by the grounded inputs. When any pair of inputs is not being used, at least one of the two must be grounded.

OUTPUT: Standard levels of -3V and ground. The output can drive 20 mA of external load at ground. It has no internal load.

POWER: +10V(A)/0.5 mA, -15V(B)/19 mA.

R200 FLIP-FLOP

R200 Flip-Flop



Price $9.50

The R200 is a basic flip-flop for use in set-reset applications. It can be set and cleared at any frequency up to 2 mc. A set input makes the 1 output go to -3V and the 0 output go to ground; a clear input makes the 0 output go to -3V and the 1 output go to ground.

INPUT: Direct Set and Clear - A standard 100 ns pulse or a ground level of 100 ns minimum duration activates the input; the load at ground is 1 mA. When not in use, the direct set and clear terminals must be at -3V. If both inputs are held at ground, both outputs are at -3V.

Collector Triggering - The flip-flop can also be set or cleared through its output by a diode network. The triggering circuit load is the external load on the output terminal being driven plus the internal load.

OUTPUT: Standard levels - Each output can drive 17 mA of external load at ground. The internal load is 4 mA. If more than 18 in. of wire is attached to an output, additional clamped loads (see the W002, W005) should be connected to decrease the output falltime. The load is sufficient if the positive transition at the opposite terminal reaches -1V within 80 ns after the flip-flop is pulsed.

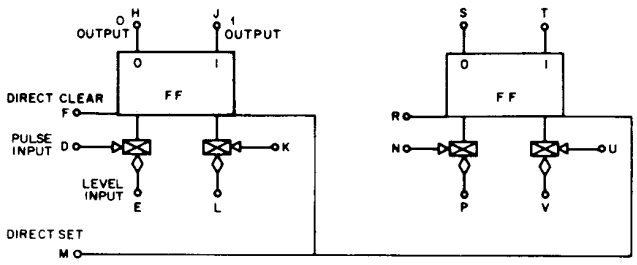
NOTE

Additional driving capability at -3V is required by some circuits outside the R-series. Auxiliary clamped loads W002 and W005 are available for this purpose.

POWER: +10V(A)/0.3 mA, -15V(B)/16 mA

R202 DUAL FLIP-FLOP

R202 Dual Flip-Flop



Price $25.00

The R202 Dual Flip-Flop contains two identical flip-flops. Each has a direct clear input, and two DCD gates. The R202 can perform in any one of the following applications without additional gating: up counter, down counter, shift register, ring counter, jam transfer buffer, and switch-tail ring counter.

INPUT: Direct Set and Clear - A standard 100 ns pulse or a ground level of 100 ns minimum duration activates the input; the load at ground is 1 mA for each clear input and 2 mA for the set input. When not in use, the direct terminals must be at -3V. If the flip-flop is in an up counter with carry gates enabled, direct clear pulses must be at least 400 ns long to suppress carry propagation. In like manner, a 400 ns set pulse must be used when the flip-flops are arranged as a down counter. If both inputs are held at ground, both outputs are at -3V.

DCD Gates, Level - Standard levels of -3V and ground. Because DCD gates are internally conditioned by the state of the flip-flop, a complement input may be formed by tying the 1 and 0 DCD gate inputs together. A DCD gate is enabled by a ground level and disabled by a -3V level. The conditioning level must be present for at least 400 ns before the gate is pulsed. The level input represents 2 mA of load at ground. When 1 and 0 DCD gates are connected in parallel to form a complement input, the total level is 3 mA at ground.

Pulse - Standard 100-ns pulses (-3V to ground) at any frequency up to 2 mc. It can also be driven by positive-going level changes (-3V to ground) with rise times of 60 ns maximum and duration of 100 ns minimum. Prior to operation the input must have been at -3V for at least 400 ns. The pulse input represents 3 mA of load at ground. When a pair of 1 and 0 DCD gates have a common pulse input, as in complementing or shifting, the total pulse load is 4 mA at ground.

Collector Triggering - The flip-flop can also be set or cleared through its outputs by a diode gate circuit or a diode network. The triggering circuit load is the external load on the terminal being driven by the circuit plus the internal load on that terminal (6 mA each).

OUTPUT: Standard levels - The carry propagate time is 70 ns. Each terminal can drive 15 mA of external load at ground and has an internal load of 6 mA. If more than 18 in. of wire is attached to an output, additional clamped loads (see the W002, W005) should be connected to decrease the output falltime. The load is sufficient if the positive transition at the opposite terminal reaches -1V within 80 ns after the flip-flop is pulsed.

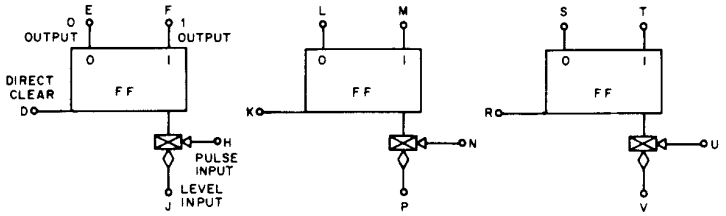
NOTE

Additional driving capability at -3V is required by some circuits outside the R-series. Auxiliary clamped loads W002 and W005 are available for this purpose.

POWER: +10V(A)/0.5 mA, -15V(B)/34 mA

R203 TRIPLE FLIP-FLOP

R203 Triple Flip-Flop



Price $28.00

The R203 Triple Flip-Flop contains three identical flip-flops. Each flip-flop has a direct clear input and a DCD gate for conditional read-in.

INPUT: Direct Clear - A standard 100 ns pulse or ground level of 100 ns minimum duration activates the input; the load at ground is 1 mA. When not in use, the direct clear terminal must be at -3V.

DCD Gates, Level - Standard levels of -3V and ground. A DCD gate is enabled by a ground level and disabled by a -3V level. The conditioning level must be present for at least 400 ns before the gate is pulsed. The level input represents 2 mA of load at ground.

Pulse - Standard 100 ns pulses (-3V to ground) at any frequency up to 2 mc. The flip-flop can also be driven by positive-going level changes (-3V to ground) with rise times of 60 ns maximum and duration of 100 ns minimum. Prior to operation the input must have been at -3V for at least 400 ns. The pulse input represents 3 mA of load at ground.

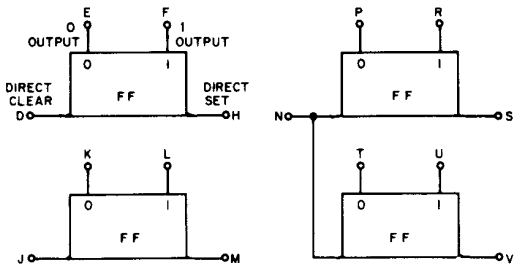
Collector Triggering - The flip-flop may also be set or cleared from its outputs by a diode gate circuit or a diode network. The triggering circuit load is the external load on the terminal being driven by the circuit plus the internal load on that terminal.

OUTPUT: Standard levels of -3V and ground. The 0 terminal can drive 15 mA of external load at ground; the internal load is 6 mA. The 1 terminal can drive 17 mA of external load at ground; the internal load is 4 mA. If more than 18 in. of wire is attached to an output, additional clamped loads (see the W002, W005) should be connected to decrease the output falltime. The load is sufficient if the positive transition at the opposite terminal reaches -1V within 89 ns after the flip-flop is pulsed.

POWER: +10V(A)/0.7 mA, -15V(B)/40 mA.

R204 QUADRUPLE FLIP-FLOP

R204 Quadruple Flip-Flop



Price $28.00

The R204 Quadruple Flip-Flop contains four flip-flops. Each has direct set and direct clear inputs. Two of the flip-flops share a common direct-clear input. The R204 is used in general control applications. A set input makes the 1 output -3V and the 0 output ground; a clear input makes the 0 output -3V and the 1 output ground.

INPUT: Direct Set and Clear - A standard 100 ns pulse or a ground level of 100 ns minimum duration activates the input; the load at ground is 1 mA per flip-flop. When not in use, the direct set and clear terminals must be at -3V. If both inputs are held at ground, both outputs will be at -3V.

Collector Triggering - The flip-flop can also be set or cleared through its outputs by a diode gate circuit or a diode network. The triggering circuit load is the external load on the terminal being driven by the circuit plus the internal load on that terminal. The internal load is 4 mA for each terminal.

OUTPUT: Standard levels of -3V and ground. Each terminal can drive 17 mA of external load at ground, and has an internal load of 4 mA. If more than 18 in. of wire is attached to an output, additional clamped loads (see the W002, W005) should be connected to decrease the output falltime. The load is sufficient if the positive transition at the opposite terminal reaches -1V within 80 ns after the flip-flop is pulsed.

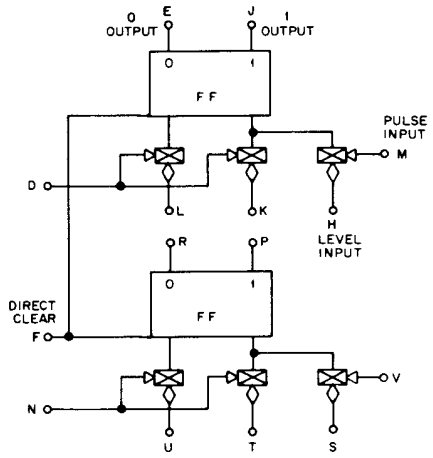
NOTE

Additional driving capability at -3V is required by some circuits outside the R-series. Auxiliary clamped loads W002 and W005 are available for this purpose.

POWER: 10V(A)/0.9 mA, -15V(B)/42 mA.

R205 DUAL FLIP-FLOP

R205 Dual Flip-Flop



Price - $29.00

The R205 contains two identical flip-flops with a common direct-clear input. Each has three DCD gates, and can be collector-triggered at either output by a diode-transistor gate or a diode network. The R205 can be used in any of the following applications without additional gating; up counter, down counter, shift register, ring counter, or jam transfer register.

INPUT: Direct Clear - A standard 100 ns pulse or a ground level of 100 ns minimum duration activates the input: the load at ground is 1 mA. When not in use, the direct clear terminal must be at -3V. If the flip-flop is used in an up counter with carry gates enabled, direct clear pulses must be at least 400 ns long to suppress carry propagation.

DCD Gates, Level - Standard levels of -3V and ground. Because DCD gates are internally conditioned by the state of the flip-flop, complement inputs may be formed by tying the 1 and 0 DCD gate inputs together. A DCD gate is enabled by a ground level and is disabled by a -3V level. The conditioning level must be present for at least 400 ns before the gate is pulsed. The level input represents 2 mA load at ground. When the 1 and 0 DCD gates are connected in parrallel to form a complement input, the total load is 3 mA at ground.

Pulse - Standard 100 ns pulses (-3V to ground) at any frequency up to 2 mc. It can also be driven by positive-going level changes (-3V to ground) with risetimes of 60 ns maximum and duration of 100 ns minimum. Prior to operation, the input must have been at -3V for at least 400 ns. The pulse input represents 3 mA of load at ground. When a pair of 1 and 0 DCD gates have a common pulse input as in complementing or shifting, the total pulse load is 4 mA at ground.

Collector Triggering - Triggering circuit load is the external load on the terminal being driven plus the internal load on that terminal. Internal load for the 1 terminal is 6 mA; for the 0 terminal, 8 mA.

OUTPUT: Standard levels - Carry propagation time is 70 ns. The 0 terminal can drive a 13-mA external load at ground; the 1 terminal, 15 mA at ground. Internal load on the 1 terminal is 6 mA; for the 0 terminal, 8 mA. If more than 18 in. of wire is attached to an output, additional clamped loads (see the W002, W005) should be connected to decrease the output falltime. The load is sufficient if the positive transition at the opposite terminal reaches -1V within 80 ns after the flip-flop is pulsed.

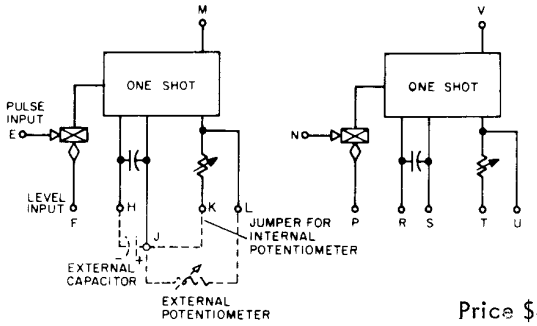
NOTE

Additional driving capability at -3V is required by some circuits outside the R-series. Auxiliary clamped loads W002 and W005 are available for this purpose.

POWER: +10V(A)/0.5 mA, -15V(B)/36 mA

R302 DELAY (ONE SHOT)

R302 Delay (One Shot)



Price $44.00

The R302 contains two delays (one-shot multivibrators) which are triggered by DCD gates. Each delay is independent and can be externally or internally controlled. When the input is triggered, the output changes from its normal ground level to -3V, for a predetermined, adjustable period of time and then returns to ground. The length of the delay is determined by the capacitor and potentiometer. External capacitors can be attached between terminals H and J (or R and S), J (S) being the more positive terminal. The 20 KΩ internal potentiometer can be used by putting a jumper between terminals J and K (or S and T). External potentiometers can be attached between terminals J and L (S and U). The total resistance between these terminals must not exceed 20Ω. A 20% change in power supply voltage will change the delay less than 2%. Delay jitter due to power supply ripple is less than 0.2%.

The expected delay of any combination (with more than a 500 pF capacitance) is determined by the resistance - capacitance network. The delay time will be in ns, the R in KΩ and C in pF. The total capacitance, C, equals 220 pF of internal capacitance plus any external capacitance use. The resistance, R, is equal to the resistance of the potentiometer plus 1 KΩ of internal resistance

(The minimum delay is 400 ns.) The minimum delay in ns for a given external capacitor is C, where C is equal to the external capacitance in pF plus a 220 pF internal capacitance. The recovery time is twice the minimum delay.

The delay range for typical capacitors used with the internal potentiometer is given below.

Total Capacitance Used (External + 220 pF Internal)	Minimum Delay Range	Recovery Time
Internal 220 pF only	400-4000 ns	800 ns
2000 pF	4-40 μs	8 μs
20 nF	40-400 μs	80 μs
200 nF	0.4-4 ms	0.8 ms
2000 nF	4-40 ms	8 ms
20 μF	40-400 ms	80 ms
200 μF	400-4000 ms	800 ms

Large electrolytic capacitors can have internal leakage enough to substantially modify time delay. For best results, use wet-slug tantalum electrolytics for delays of several seconds or more. While 4V ratings are adequate in most cases, 6 or 8V ratings may be desirable to further reduce leakage in other instances.

Remote Control Wiring: Noise picked up on wires leading to remote timing capacitors or rheostats tends to synchronize the end of the delay period (or it could cause false triggering in extreme cases). Even for 1 ft control wires, a grounded shield may be advisable if smooth control and freedom from jitter are essential.

INPUT: Level - Standard levels of -3V and ground. A DCD gate is enabled by ground level and disabled by a -3V level. The conditioning level must be present for at least 400 ns before the gate is pulsed. The level input represents 2 mA of load at ground.

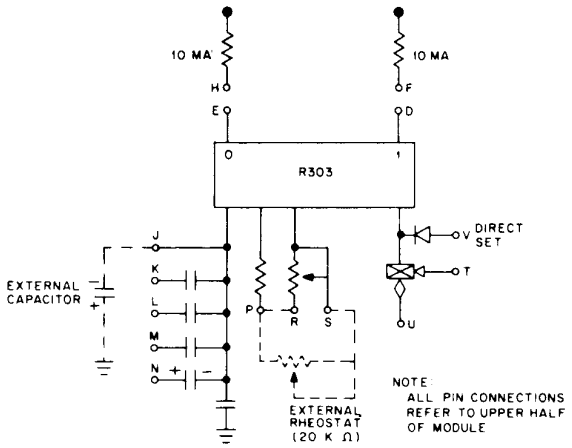
Pulse - Standard 100 ns pulses (-3V to ground). It can also be driven by positive-going level changes (-3V to ground) with risetimes of 60 ns maximum and minimum duration of 100 ns. Prior to operation, the input must have been at -3V for at least 400 ns. The pulse input represents 3 mA of load at ground. The delay cannot be set from its output terminal.

OUTPUT: Standard level of -3V for the duration of the delay time. The output can drive 18 mA of external load at ground. The internal load is 2 mA.

POWER: +10V(A)/0.6 mA; -15V(B)/88 mA

R303 INTEGRATING ONE SHOT

R303 Integrating One Shot



Price $45.00

The R303 contains a zero recovery time multivibrator and complementary output buffers. Its unusual characteristics include the ability to respond to inputs even while in the 1 state, so that successive inputs above a preset frequency can postpone the return to 0 indefinitely. This characteristic can be used, for example, to detect gaps in an otherwise continuous pulse train, or to determine whether an input pulse rate is above or below a preset frequency threshold. If the delay setting of this module exceeds the time it takes +10 and -15 to reach 90% of their final values on power turn-on, this module will initially go to the 1 state. The above conditions allow the R303 to be used for system initialization on power turn-on.

Delay is 3.5 μs to 0.7s. Jitter is less than 1.4% peak-to-peak. Delay time will change less than 2% for a change of 20% in supply voltage.

INPUTS: Direct Set - A standard 100 ns pulse or a ground level of at least 100 ns duration starts the delay. The load at ground is 1 mA. At least 90 to 99.5% of total delay (for 0 and 20 kΩ rheostat setting, respectively) will not be measured out until 13V is restored, a fact which may be important if this input is grounded for longer than 300 ns.

DCD Gate - Same as R302.

OUTPUTS: Each output can drive 18 mA at ground, 0 mA at -3V. Extra 10 mA clamped loads may be connected to change the driving capability at each output to 8 mA at ground, 7 mA at -3V. The 1 output will be at -3V during the delay period and at ground otherwise. The 0 output is grounded during the delay period and is at -3V otherwise.

POWER: +10V(A)/6 mA; -15V/75 mA

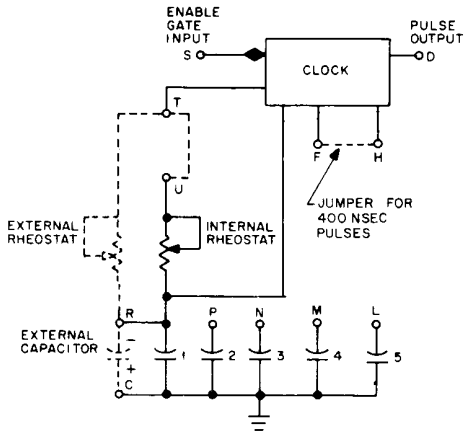
CONTROLS: To choose desired range of delay, ground the appropriate capacitor pin K through N (for minimum delay range, ground none of these). Ranges are separated by a factor of approximately ten. For extra long delays, connect an external capacitor from pin J to ground. To use the internal rheostate, connect pin P to pin R. For external control, connect a variable resistance no larger than 20,000Ω from pin P to pin S.

EXTERNAL CONTROL: Delay times may be controllec by external R and C in the same manner as described for R302. Substantially the same R and C are required in the R303 as in the R302 for a given delay, taking into account that a minimum capacitance ten times greater is built into the R303. If electrolytic capacitors are used, at least a 6V rating is required.

Capacitor Values (MFD): Internal - 0.0022, Pin K-0.027, Pin L -0.39, Pin M-3.9, Pin N-39.0

R401 VARIABLE CLOCK

R401 Variable Clock



Price $45.00

The R401 Variable Clock is a gateable clock that produces standard 100 or 400 ns pulses from a stable RC-coupled oscillator. The variable clock is often used as a primary source of timing for large systems.

The frequency of the R401 Clock is variable from 30 cps to 2.0 mc. Five capacitors provide coarse frequency control, and a built-in 20,000Ω potentiometer permits fine adjustment. Terminals for an external potentiometer or capacitor are available. The maximum size of the external potentiometer to be used is 20,000Ω.

Frequency Selection

Select Pin R	C_1 = 82 pF	300 kc to 2.0 mc
Pin P	C_2 = 1200 pF	30 kc to 375 kc
Pin N	C_3 = 0.015 MFD	3.5 kc to 40 kc
Pin M	C_4 = 0.15 MFD	300 cps to 4.5 kc
Pin L	C_5 = 2.2 MFD	30 cps to 340 cps

Lower frequencies may be obtained by adding an external capacitor between pins R and C. A 20% change in power supply voltage will change the PRF less than 1%. The pulse-to-pulse jitter is less than 0.2%.

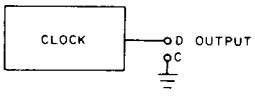
INPUT: The clock is enabled by -3V level or an open circuit at its enable gate input. The total transition time from the time the gate is enabled until the first pulse reaches 90% of its amplitude is approximately 45 ns. The pulses that follow appear at the frequency selected. The clock may be disabled by applying a ground level at the enable gate pin S. The enable gate loading is 4 mA at ground. Disable duration must exceed the period to which the clock is set.

OUTPUT: The output is a standard 100 ns pulse -3V to ground and may be changed to a 400 ns pulse by connecting pin F to pin H. The output can drive 70 mA of external load at ground. The internal load is 3 mA.

POWER: +10V(A)/1.3 mA; -15V(B)/19 mA

R405 CRYSTAL CLOCK

R405 Crystal Clock



Price - $100.00

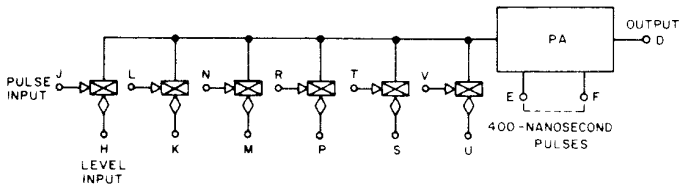
The Type R405 employs a series-resonant crystal oscillator, squaring circuit, and output pulse amplifier. The crystal clock's output frequency remains within 0.01% of specified value between 0°C and +55°C. The clock frequency is specified anywhere in the 5 kc to 2 mc range by the customer and is stamped on the crystal can.

OUTPUT: 100 ns pulse, -3V to ground. The output can drive 70 mA of external load at ground. Internal load is 3 mA.

POWER: +10V(A)/5.4 mA; -15V(B)/50 mA

R601 PULSE AMPLIFIER

R601 Pulse Amplifier



Price - $25.00

The R601 is a pulse amplifier that standardizes pulses in amplitude and width. Outputs may be either standard 100 or 400 ns pulses (-3V to ground). It has six DCD gates so that inputs from as many as six sources may be mixed. Input pulses can occur at any frequency up to 2 mc for 100 ns pulse outputs and up to 1 mc for 400 ns outputs. Delay through the pulse amplifier is approximately 50 ns.

DCD GATE INPUTS: Level - Standard levels of -3V and ground. A DCD gate is enabled by a ground level and disabled by a -3V level. The conditioning level must be present for at least 400 ns before the gate is pulsed. The level input represents 2 mA of load at ground.

Pulse - 100 ns or longer pulses, -3V to ground, at any frequency up to 2 mc. It can also be driven by positive-going level changes (-3V to ground) with rise times of 60 ns maximum and duration of 40 ns minimum. The input must have been at -3V for at least 400 ns prior to operation of any input. The pulse input represents 3 mA of load at ground.

OUTPUT: With terminals E and F connected together, the output is a standard 400 ns pulse (-3V to ground). With E and F open, the output is a standard 100 ns pulse (-3V to ground). The output is a standard 100 ns pulse (-3V to ground). The output (for either 100 or 400 ns pulses) can drive 70 mA of external load at ground. The internal load is 3 mA.

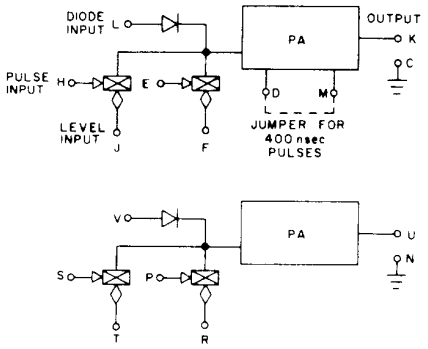
Pulse amplifier outputs may be paralleled for a logical OR.

Pulse lines and ground lines should be kept as short as possible.

POWER: +10V(A)/1.1 mA; -15V(B)/33 mA

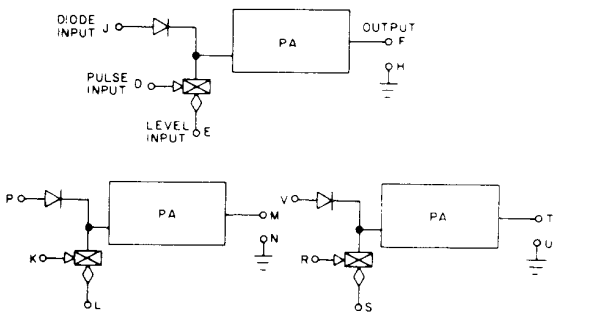
PULSE AMPLIFIERS

R602 Pulse Amplifier



Price $22.00

R603 Pulse Amplifier



Price $28.00

The R602 and R603 contain pulse amplifiers for power amplification and for standardizing pulses in amplitude and width. Each amplifier produces standard 100 ns pulses and one section of the R602 can also produce 400 ns pulses. DCD gates and a single diode input permit inputs from many sources to be mixed. Input pulses can occur at any frequency up to 2 mc for 100 ns pulses, and up to 1 mc for 400 ns pulses. Delay through the pulse amplifier is approximately 50 ns.

INPUTS: Level and Pulse - Same as R601.

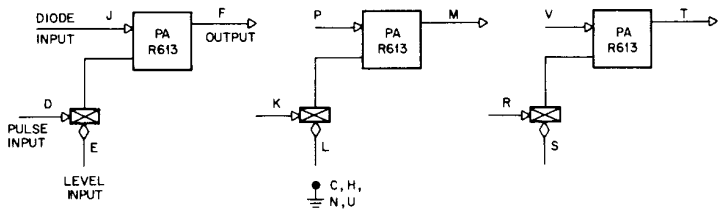
Diode - Standard 100 ns pulses (-3V to ground) or positive-going level changes (-3V to ground) with a rise time of 60 ns maximum. The input level must be returned to -3V for at least 400 ns before another input may occur at either the diode or the DCD gate input. The diode input represents a 1 mA load at ground.

OUTPUTS: Outputs are standard 100 ns pulse, -3V to ground (except pin K of R602, which may be changed to 400 ns pulses by connecting pin D to pin M). Each output can drive up to 70 mA load at ground. The internal load is 3 mA. Pulse amplifier outputs may be parallel to obtain a logical OR. Pulse line and grounds should be kept as short as possible.

POWER: R602: +10V(A)/2.2 mA; - 15V(B)/45 mA
R602: +10V(A)/3.3 mA; - 15V(B)/57 mA

R613 PULSE AMPLIFIER

Standard Size FLIP CHIP Module, 18 Pins



Price $42.00

The R613 is pin compatible with and functionally similar to the R603.

Each pulse amplifier produces a 200 ns R-series (positive) pulse. A DCD gate and a diode input permit considerable flexibility. Input pulses can occur at any rate up to 2 MHz. Delay through the pulse amplifier is typically 50 ns.

INPUTS: DCD Gate Level - DEC standard levels of -3V and ground. The DCD gate is enabled by a ground level and disabled by a -3V level. The conditioning level must be present for at least 200 ns before the gate is pulsed. The level input represents 2.5 mA of at at ground and 0 mA at -3V. The level input is prevented from going above ground by a diode clamp.

DCD Gate Pulse - 40 ns or longer pulses going from -3V to ground at any repetition rate up to 2 MHz. It can also be driven by positive going level changes (-3V to ground) with risetimes of 60 ns maximum and durations of 40 ns minimum. The input must have been at -3V for at least 200 ns prior to operation of any input. The pulse input represents 5 mA of load at ground, 0 mA at -3V. The pulse input is prevented from going above ground by a diode clamp.

Diode - DEC standard levels of -3V and ground. 40 ns or longer pulses or positive going level changes (-3V to ground) with a risetime of 60 ns maximum will trigger the PA. The input must be returned to -3V for at least 400 ns before another input is allowed to trigger the PA from either the DCD gate or diode input. The output produced by a ground level at the diode input will be at ground for 200 ns or as long as the input is at ground, whichever is longer. This feature can be used to apply a dc clear to flip-flops during an initial power-up period and also to apply clear pulses during normal operation. The diode input represents a 1 mA load at ground.

OUTPUTS: Outputs are positive pulses (-3V to ground) of from 190 ns to 350 ns duration or levels (see diode input above). Each output can supply 65 mA at ground. The internal clamped load supplies -3.5 mA at -3V. Output pulses may be ORed by paralleling PA outputs. The outputs are buffered so that the PA cannot be triggered by noise on the output line (or by another gate or PA). Pulse lines and ground should be kept as short as possible.

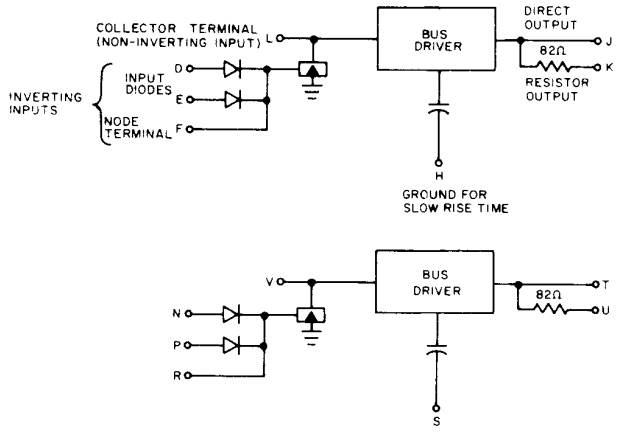
POWER:

Pin	Voltage	Margin Range	Current
A	+10V	+8V to +12V	3.3 mA
B	-15V	-12V to -18V	77 mA
C,H,N,U	ground		

Pins C,H,N, and U must all be grounded.

R650 BUS DRIVER

R650 Bus Driver



Price - $23.00

The R650 contains two inverting bus drivers for driving heavy current loads to either ground or negative voltages. The four input terminals make the R650 a versatile logic element as well. The diode inputs D and E (N and P) are the principal inputs. They form a NAND gate for negative inputs or a NOR gate for ground inputs. Gate inputs, such as the R001 or R002, can be added through the node terminal F (R). Other gating sources may be mixed with the gate inputs by using collector terminal L (V).

The bus drivers operate at frequencies up to 2 mc with typical risetimes and falltimes of 25 ns. The typical total transition times are 60 ns for output rise and 65 ns for output fall.

By grounding pin H (S) the risetimes and falltimes can be increased to avoid ringing on exceptionally long lines. The driver then operates at frequencies up to 500 kc with typical rise delay of 50 ns, fall delay of 50 ns, and total transition time of 800 ns for output rise and 700 ns for output fall. Terminal K (U) can be used for driving coaxial cable.

INPUT: Standard levels at frequencies up to 2 mc (up to 500 kc with H or S grounded). The diode inputs, including any diodes attached to the node terminal, represent 1 mA of load, shared by all grounded inputs. Collector terminal L (V) represents 10 mA of load at ground. External clamped loads should not be connected to this terminal. The combined length of all leads attached to the node terminal should not exceed 6 in. The combined length of all leads attached to the collector terminal should not exceed 18 in.

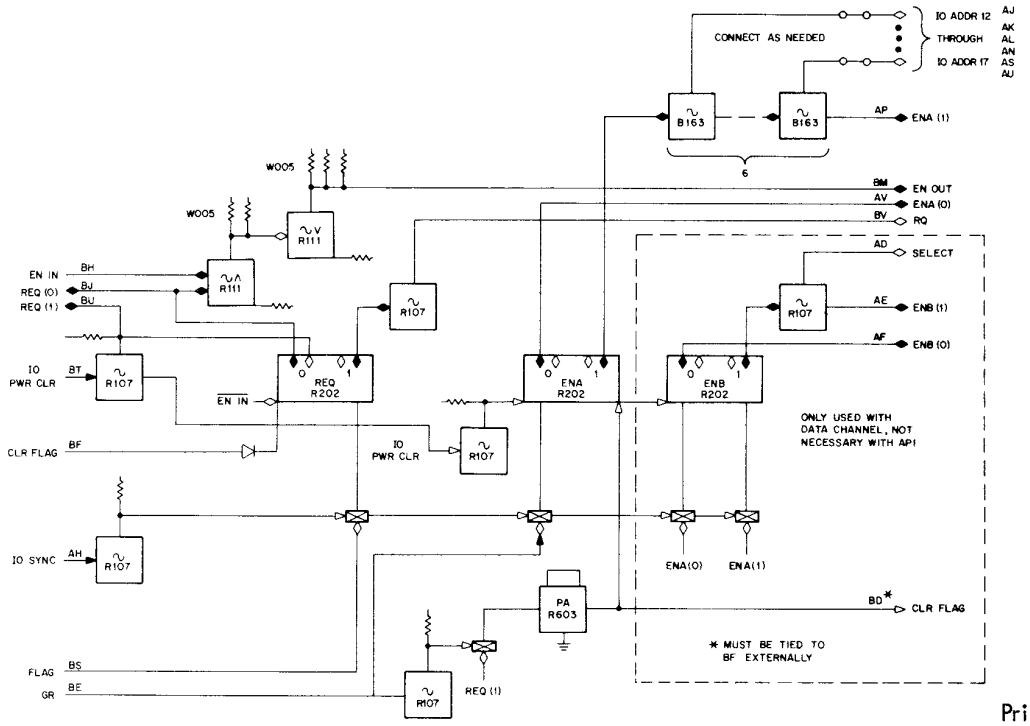
OUTPUT: Direct - Standard levels. The output can drive 20 mA of external load at either ground or -3V.

Resistor - Standard levels. The resistor output drives 90Ω coaxial cable such as RG-62-U. The output can drive 5 mA of external load at either ground or -3V.

POWER: +10V(A)/50 mA; -15V(B)/81 mA

W104 PDP-9 BUS MULTIPLEXER

Double Size FLIP CHIP Module, 36 Pins



Price $100.00

Equivalent Circuit of the W104 Bus Multiplexer

The W104 is a PDP-9 and PDP-9/L I/O Bus Multiplexer used in peripheral devices which operate on the data channel or the automatic priority interrupt channel.

INPUTS:

IO PWR CLR, IO SYNC - Must be standard levels of -3V and ground, 100 μs minimum duration. The load at ground is 1 mA.

EN IN must be a standard 100 μs pulse or ground level of 100 μs minimum duration. The load at ground is 2 mA maximum.

FLAG - Standard levels of -3V and ground. The DCD gate is enabled by a ground on FLAG. The conditioning level, FLAG, must be present 400 ns before the gate is pulsed by I/O SYNC. The level input represents 2 mA of load at ground.

GR - This signal enables the DCD gate of ENA. Its characteristics must be the same as FLAG. This input draws 3 mA at ground.

OUTPUTS:

CLR FLG - as an output from the R603 pulse amplifier at pin BD, it is a standard 100 ns pulse, -3V to ground. It can drive a 70 mA load at ground. Its own internal load is 3 mA.

ENB (1) and ENB (0) - These terminals can drive 15 mA and 14 mA, respectively, of external load at ground. ENB (1) has an internal load of 7 mA and ENB (0) of 6 mA. If more than 18 in. of wire is attached at these points, additional clamped loads

RQ (0); RQ (1) - These signals can be considered both inputs and outputs. As inputs they can be used to clear the RQ flip-flop. The triggering load is 7 mA maximum for REQ (0) and 9 mA for RQ (1).

SELECT, RQ - Standard levels of -3V and ground.

Each output can drive 27 mA of load at ground from open collector inverters.

ENA (0) - Standard levels - can drive 13 mA at ground and has an internal load of 8 mA.

ENA (1) - Can drive 3 mA of external load at ground. Internal load is 18 mA.

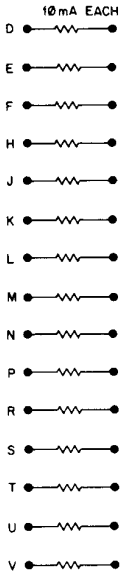
10 ADDR 12 - IO ADDR 17 - Each output can supply up to 26 mA at ground.

EN OUT - The clamped load resistor represents 15 mA of load. The output gate can drive an external load of 15 mA at ground.

POWER: +10V - 100 mA, -15V - 500 mA

W010 CLAMPED LOADS

Standard Size FLIP CHIP Module, 18 Pins



Price - $23.00

The W010 is pin compatible with the W002 and W005 clamped loads. It contains fifteen 10 mA clamped loads.

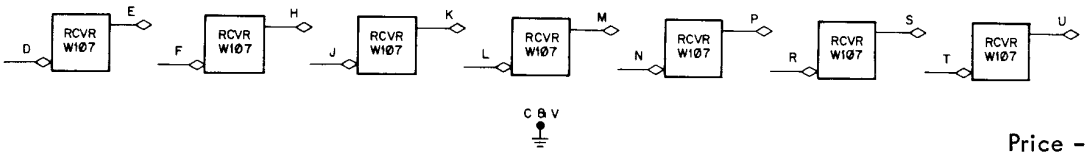
OUTPUTS: Each clamped load draws 10 mA at ground and can supply -7 mA at -3V.

POWER:

Pin	Voltage	Margin Range	Current
A	Not Used	Connections are optional	
B	-15V	-7.5V to -20V	180 mA
C	ground		

W107 I/O BUS RECEIVER

Standard Size FLIP CHIP Module, 18 Pins



Price - $36.00

The W107 contains seven identical non-inverting receiver circuits with high-impedance input for buffering signals from the PDP-9 or PDP-9/L I/O Bus. The W107 is pin compatible with the W500 emitter follower. (See Logic Handbook.)

INPUTS: Standard DEC levels of -3V and ground. Each input draws 0.22 mA at ground and less than 1 μA at -3V.

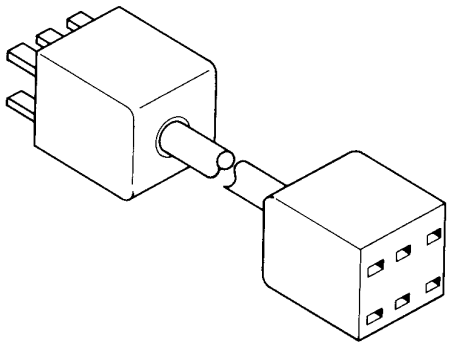
OUTPUTS: Standard DEC levels of -3V and ground. Each output can supply -7 mA at -3V and 36 mA at ground, in addition to the internal clamp load. The TTT is less than 150 ns for both rise and fall.

POWER:

Pin	Voltage	Margin Range	Current
A	+10V	2.5V to 17.5V	.14 mA
B	-15V	-10V to -20V	100 mA
C,V	ground		

Both pins C and V must be grounded.

BC10B MARGIN CHECK CABLE ASSEMBLY



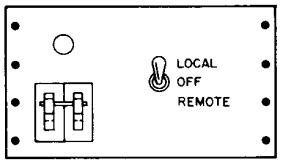
Price $20.00

The BC10B Margin Check Cable Assembly is the standard PDP-9 and PDP-9/L margin check bus cable. It consists of a Cinch-Jones P-306-CCT male plug at one end and Cinch-Jones S-306-CCT female plug at the other end. The cable is arranged as an extension cord; that is, all six pins at one end are connected to the corresponding pins at the other end.

The BC10B cable assembly is ordered by specifying BC10B-XX where XX is the length of the cable in feet. Standard lengths are 5, 7, 10, 15, 25, and 35 ft.

841 POWER CONTROL

841 Power Control



Price $201.00

The 841 Power Control provides remote and local on-off control, noise filtering, and power-on, power-off logic transient control.

The 841 requires 8 in. of space on a 16 in. plenum door. All connections are on the inside of the plenum door; all operating controls are on the outside of the door.

INPUTS: Line - The 841 will accommodate 115V or 230V ac 50-60 Hz power lines. A three conductor cord containing a safety ground wire should be connected to the pressure type terminal strip provided. The input supply need not have one side grounded, as both sides of the line are switched throughout.

Remote Control, ac - Power to the load is applied when the ac remote control input is energized. It must be of the same voltage as the line input. Male and female parallel-blade, U ground connectors are provided to facilitate connection of the ac remote control bus to all successive power controls.

Remote Control, dc - Power to the load is also applied when any of the four dc remote control inputs are at -15V. Load is approximately 1W. The dc remote control inputs are Heyman tabs suitable for AMP Faston solderless connectors.

If either of the ac or dc remote control inputs are energized and the local-remote switch is in the remote position, power will be applied to the load.

CONTROLS: Circuit Breaker - A 30A double-pole toggle-switch type circuit breaker controls all power to the load. The circuit breaker can be used as a master power switch.

Local-Off-Remote Switch - This three-position toggle switch controls the power control mode. In Local, the switched load is energized. In Off, the switched load is unenergized. In Remote, the switched load is energized under the control of the remote control inputs.

Console Switch - A single-pole switch can be inserted between the pair of Heyman tabs provided. When the switch is closed the switched load may be energized. The switch must break the line voltage and carry approximately 500 mA rms. If a console switch is not used, a jumper must be substituted.

Orange Jumpers - Two orange Faston jumpers must be supplied between the pair of orange Heyman tabs to operate the power control from 115 Vac. The jumpers should be removed for 230 Vac operation.

White Indicator - A white neon indicator is lit whenever line voltage is present at the line input terminals.

OUTPUTS: Unswitched - The two unswitched convenience outlets and unswitched Heyman tabs are energized whenever the circuit breaker is on.

Switched - The two switched convenience outlets and switched Heyman tabs are energized diagram Figure B-8. The switched power comes on immediately and goes off with a 4s delay.

Frame Ground - These Heyman tabs are connected to the chassis of the power control and the safety ground wire of the line cord.

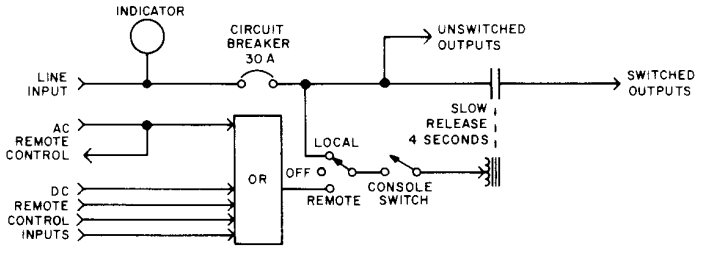
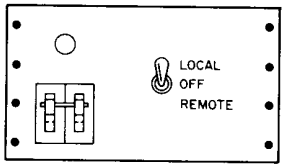


Figure B-8 841 Power Control Block Diagram

Type 844 POWER CONTROL Panel

844 Power Control Panel



Price $365.40

The 844 Power Control provides remote and local on-off control, noise filtering, and power-on, power-off logic transient control.

The 844 requires 8 in. of space on a 16 in. plenum door. All connections are on the inside of the plenum door. All operating controls are on the outside of the door.

INPUTS: Line - The 844 will accommodate 115V or 230 Vac 50-60 Hz power lines. A three conductor cord containing a safety ground wire should be connected to the pressure type terminal strip provided. The input supply need not have one side grounded as both sides of the line are switched throughout.

Remote Control, ac - Power to the load is applied when the ac remote control input is energized. It must be of the same voltage as the line input. Male and female parallel-blade, U ground connectors are provided to facilitate connection of the ac remode control bus to all successive power controls.

Remote Control, dc - Power to the load is also applied when any of the four dc remote controls inputs are at -15V. Load is approximately 1W. The dc remote control inputs are Heyman tabs suitable for AMP Faston solderless connectors.

If either of the ac or dc remote control inputs are energized and the local-remote is in the remote position, power will be applied to the load.

CONTROLS: Circuit Breaker - A 30A double-pole toggle-switch type circuit breaker controls all power to the load. The circuit breaker can be used as a master power switch.

Local-Off-Remote Switch - This three-position toggle switch controls the power control mode. In Local, the switched load is energized. In Off, the switched load is de-energized. In Remote, the switched load is energized under the control of the remote control inputs.

Console Switch - A single-pole switch can be inserted between the pair of Heyman tabs provided. When the switch is closed the switched load may be energized. The switch must break the line voltage and carry approximately 500 mA rms. If a console switch is not used, a jumper must be substituted.

Orange Jumpers - Two orange Faston jumpers must be supplied between the pairs of orange Heyman tabs to operate the power control from 115 Vac. The jumpers should be removed for 230 Vac operation.

White Indicator - A white neon indicator is lit whenever line voltage is present at the line input terminals.

OUTPUTS: Unswitched - The two unswitched convenience outlets and unswitched Heyman tabs are energized whenever the circuit breaker is on.

Switched - The two switched convenience outlets and switched Heyman tabs are energized when the console switch is on, and the local-off-remote switch is in local or remote. (See the block diagram Figure B-9). The switched power comes on immediately and goes off with a 4s delay.

Frame Ground - These Heyman tabs are connected to the chassis of the power control and the safety ground wire of the line cord.

Crobar* - These Heyman tabs are connected to a time delayed relay contact. The contact is closed when power is off. They open 4s after power-on and close immediately at power off. The contacts are rated at 115 Vac 5A.

*The term "crobar" is an extension of a concept originally used in radar power-supply technology and more recently used in integrated circuit power supplies. A crobar circuit (often spelled crowbar) was originally used to rapidly discharge a radar's high voltage power supply after a detected malfunction to avoid damaging (expensive) output components. In more recent integrated circuit power supplies, the term is used to describe a circuit which detects excessive output voltage and shorts it to

ground to avoid damaging integrated circuit components. The crobar function of the 844 provides a means which the logic designer may use to attempt to eliminate improper operation (glitches) in logic when power is being applied or removed.

The use of the word crobar (crowbar) for this function apparently comes from the "violent" means used to accomplish the function. (The operation of the crowbar circuits of a high power radar can be quite spectacular.) In semi-slang, the crobar is said to gronk the logic, in order to prevent false operation.

APPLICATION: To obtain maximum benefit from the crobar feature of the 844 in the large transient electric and magnetic field environment associated with turn-on and turn-off, it is advisable to connect the crobar contacts to the logic with coaxial cable, grounding the circuit only at the logic. In addition, noise energy on the crobar line should be absorbed by the use of load resistors, clamped loads, or diode clamps on the ungrounded side of the crobar circuit. The particular loading to be used depends on the voltage level during normal operation and the amount of noise which can be tolerated.

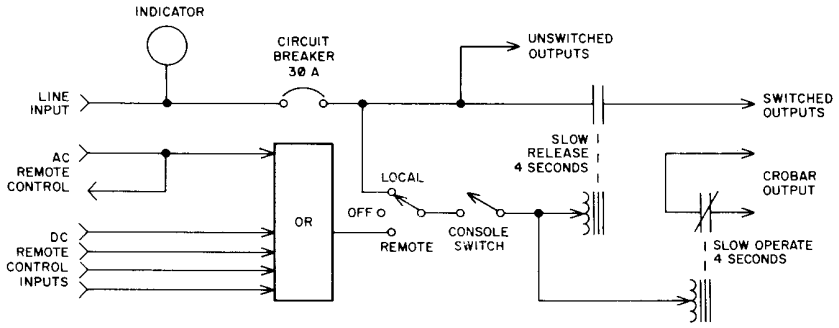


Figure B-9 844 Power Control Block Diagram

APPENDIX C
DESIGN EXAMPLE FOR STANDARD INTERFACE FOR THE PDP - 9 and PDP-9/L I/O DEVICES

The Standard Interface* for PDP-9 input/output devices is a general interface designed for a range of devices comprised of from one IOT command up to devices with 24 IOT commands (two device selectors), programmed data input and output, two data channels, and provisions for up to three levels to be connected to the Skip, Program Interrupt, and API facilities. This standard configuration utilizes 44 board slots in a standard Type 1943 Mounting Panel leaving 20 unused slots available to add additional logic.* The Standard Interface Panel is intended to be used in the following manner: (refer to prints C1→C5).

a. The engineer obtains the standard interface print set. A description of the interface and instructions to the engineer will accompany the print set.

b. The engineer marks up each print to suit his desired configuration and fills in the title blocks.

c. The engineer generates additional prints for the logic which is to be added in the spare locations or in additional panels.

d. The draftsman will draw the new prints and mark up sepias of the standard interface and generate a wire list for the additions only.

e. The wire list is made up.

*This is a design example only. This is not a DEC product.

C.1 IMPLEMENTING THE STANDARD INTERFACE

The following is a detailed step by step procedure to implement the various facilities of this interface.

Given: Single Device, NO SKIP, INT, or READ RQ.

1. Install the following modules.

1-W109	LOC	AB21
2-R107	LOC	A15, B15

2. Fill in the following blanks on the appropriate prints.

Print	Pin	Instructions
C-3	A21	Supply a device number to W109 at location AB21.
C-3	A21E	Complete label, IOT --- 01XA, by filling in blanks with device number.
C-3	A21L	Complete label, IOT --- 02XA, by filling in blanks with device number.
C-3	A21S	Complete label, IOT --- 04XA by filling in blanks with device number.

To add: 2 SKIPS, INT, RD RQ

1. Install the following modules:

1 - R107	LOC	A13
2 - R111	LOC	A12, B13

2. Fill in the blanks on the appropriate prints.

Print	Pin	Instructions
C-4	A13E	Connect to flag - 0V for assertion.
C-4	A13H	Connect to flag - 0V for assertion.
C-4	A12D	Complete label, IOT ---01XA by filling in blanks with device number.
C-4	A12K	Complete label, IOT ---01XB by filling in blanks with device number.
C-4	B13K	Additional gate for READ RQ, Neg. level for assertion. Connect as required.
C-4	B13L	Connect Read Data to appropriate IOT pulse.
C-4	A12S	Interrupt ENABLE ground here inhibits flag from giving interrupt.

To add:

One more Skip, two Interrupts:

1. Install the following modules:

2 - R111	LOC	B12

2. Fill in the blanks on the appropriate prints

Print	Pin	Instructions
C-4	A13K	Connect to flag 0V for assertion.
C-4	B12D	Complete label, IOT---. By filling in blanks with device number.
C-4	B12L	Connect to interrupt EN. Ground here inhibits flag from giving interrupt.
C-4	B12S	Connect to interrupt EN - Ground here inhibits flag from giving interrupt.

To add:

Subdevice selector:

1. Install the following modules:

1 - R107	LOC	B15
1 - R113	LOC	A16
1 - R001	LOC	B16

2. Fill in the blanks on appropriate prints

Print	Pin	Instructions
C-4	B16D	Connect to subdevice selector negative level for assertion.
C-4	B16F	Connect to subdevice selector negative level for assertion.
C-4	B16J	Connect to subdevice selector negative level for assertion.

To add:

One more device selector

1. Install the following modules:

1 - W109	LOC	AB22

2. Fill in the following blanks on the appropriate prints:

Print	Pin	Instructions
C-3	A22F	Complete label,IOT --- 01XB, by filling in blanks with device numbers.
C-3	A22M	Complete label,IOT --- 02XB, by filling in blanks with device numbers.
C-3	A22T	Complete label,IOT --- 04XB, by filling in blanks with device numbers.
C-3	A22	Supply a device number to W109 at LOC AB22.

To add:

API facility

1. Install the following modules:

1 - W104	LOC	AB14

2. Fill in the following blanks on the appropriate prints:

Print	Pin	Instructions
C-4	B14V	Complete label, API_REQ by filling in blank with API number.
C-4	B14M	Complete label, API_EN OUT, by filling in blank with API number.
C-4	B14E	Complete label, API_GR by filling in blank with API number
C-4	B14H	Complete label, API_EN IN by filling in blank with API number.

To implement API facility, user must remove jumper from I/O bus connector.

To add:

One DCH facility:

1. Install the following modules:

1 - W104	LOC	AB17
1 - R202	LOC	B19

2. Fill in the following blanks on the appropriate prints.

Prints	Pin	Instructions
C-6	B19L	Can be tied to ground
C-6	B19K	IOP pulse here for setting DCH EN.
C-6	B19U	Data channel REQUEST

For WR RQ, RD RQ, user must gate

ENB(1) through an R111

For increment memory, user must gate

ENA(1) through an R111

User must clip appropriate jumpers on W104 for correct IO ADDRESS and fill in DCH number on print C-6 6-C AB17.

To add:

One more DCH facility

1. Install the following modules:

1 - W104	LOC	AB18
1 - R202	LOC	A19

2. Fill in the following blanks on the appropriate prints.

Print	Pin	Instructions
C-6	A19L	Can be tied to ground
C-6	A19K	IOP pulse here to set DCH B EN.
C-6	A19U	Data channel REQUEST.

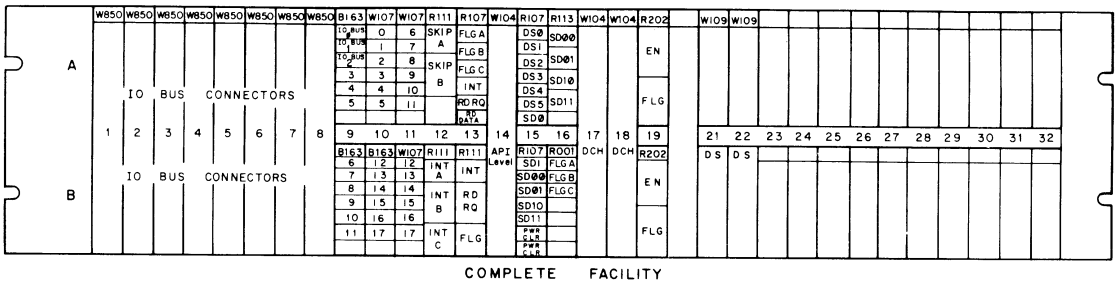
For WR RQ, RD RQ, user must gate

ENB(1) through an R111

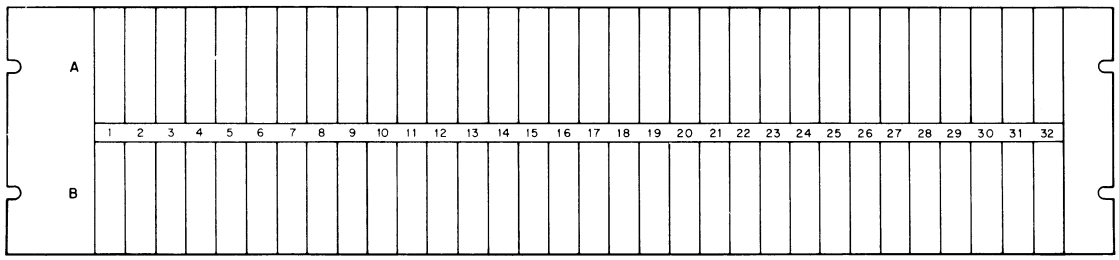
For increment MEMORY, user must gate

ENA(1) through an R111

User must clip appropriate jumpers on W104 for correct IO ADDRESS and fill in blank in DCH number on print C-6 6C AB1B.



COMPLETE FACILITY



NOTE: TO BE FILLED IN BY USER AS DESIRED.

FACILITY DESIRED	CARDS NEEDED	SLOT
SINGLE DEVICE NO SKIP OR READ RQ	1 W109, 2 R107	AB21, A15 B15
ADDS TWO SKIPS, ONE INTERRUPT, RD RQ	1 R107, 2R111	A13 A12 B13
ADDS DATA INPUT FROM IO BUS	3 W107	A10 A11 B11
ADDS DATA OUTPUT TO COMPUTER	3 B163, 1 R111	A09 B09 B10, B13
ADDS ONE MORE SKIP, TWO INTERRUPTS	1 R111	B12
ADDS SUB DEVICE SELECTOR	1 R107, 1 R113 1 R001	B15, A16 B16
ADDS API	1 W104	AB14
ADDS ONE MORE DEVICE SELECTOR	1 W109	AB22
ADDS 1 DCH FACILITY	1 W104, 1 R202	AB17, B19
ADDS 1 MORE DCH	1 W104, 1 R202	AB18, A19
COMPLETE FACILITY	2 W109, 3 R107 3 R111, 1 R113, 1 R001 3 W104 2 R202, 3 W107 3 B163	

Figure C-1 Complete Facility

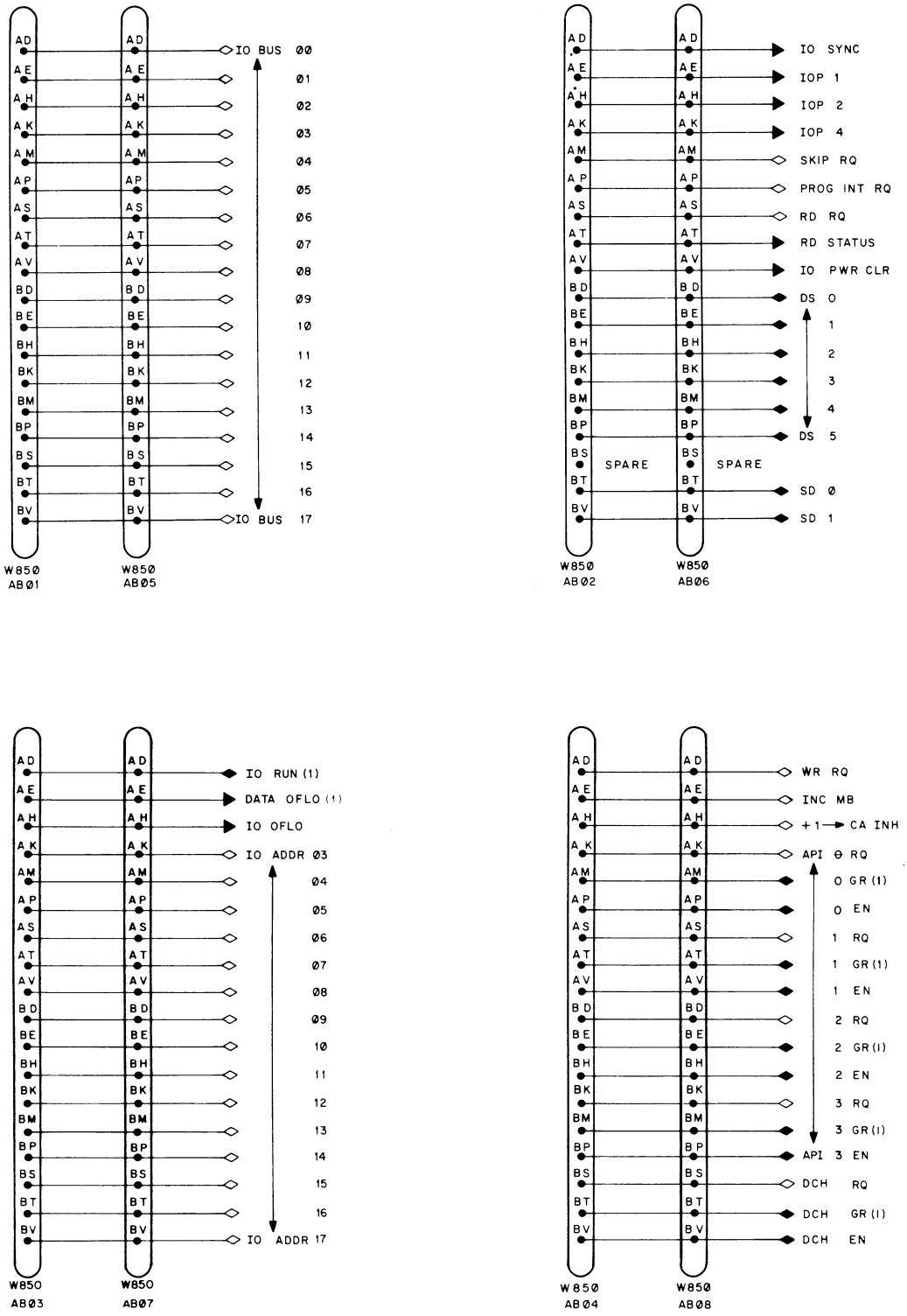


Figure C-2 I/O Bus Connectors

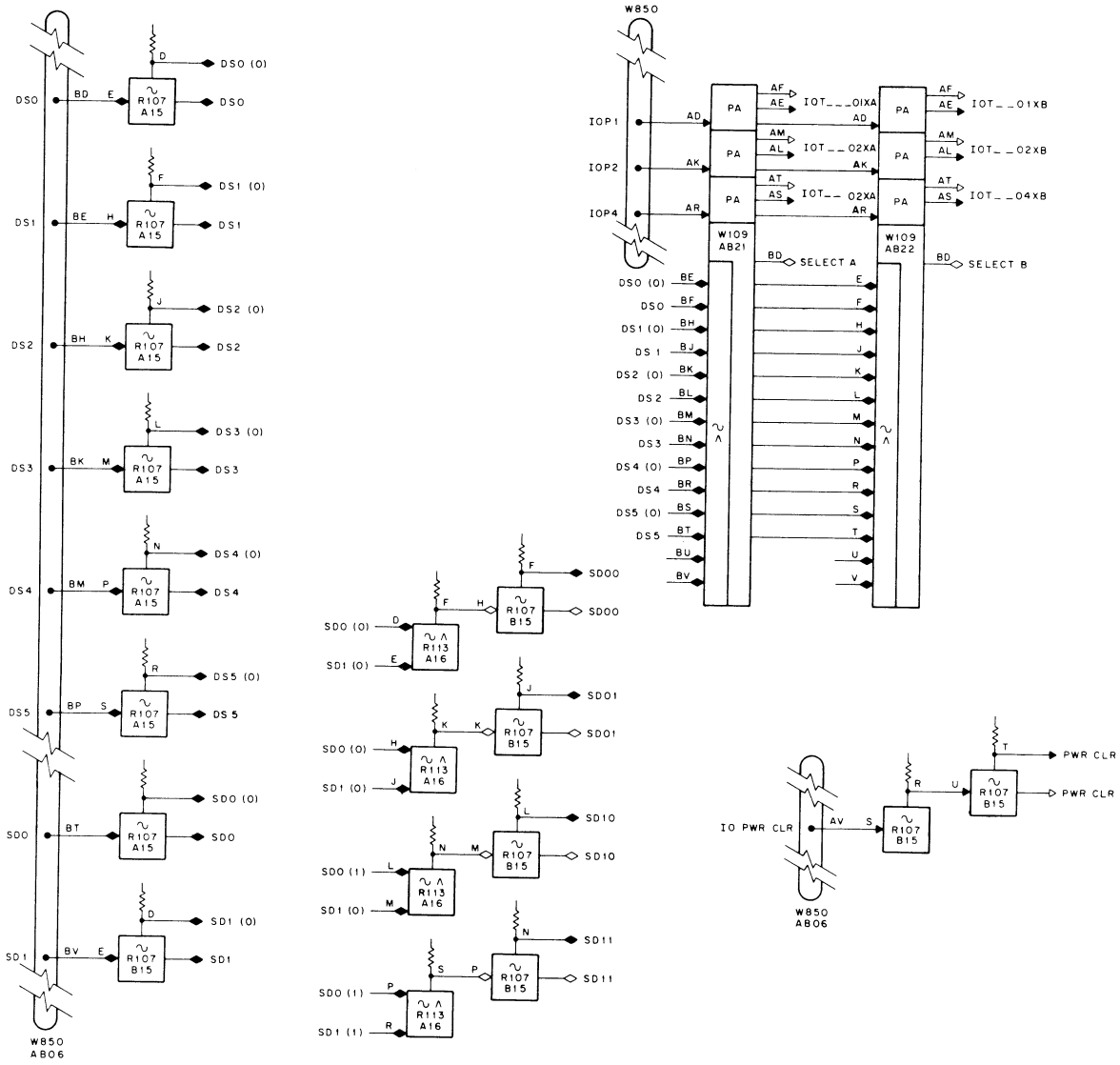


Figure C-3 Command Decode Logic

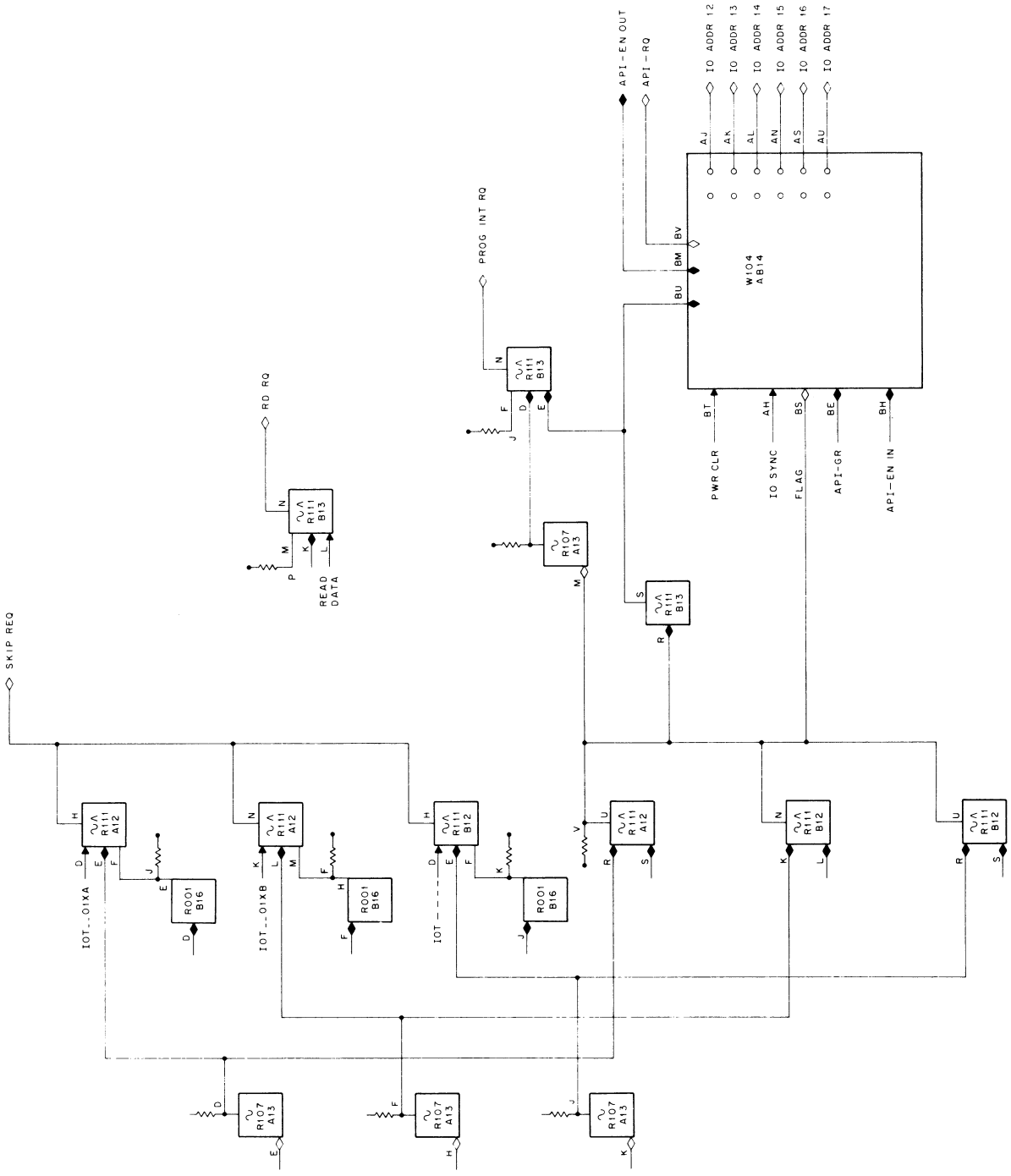


Figure C-4 SKIP, INT LOGIC

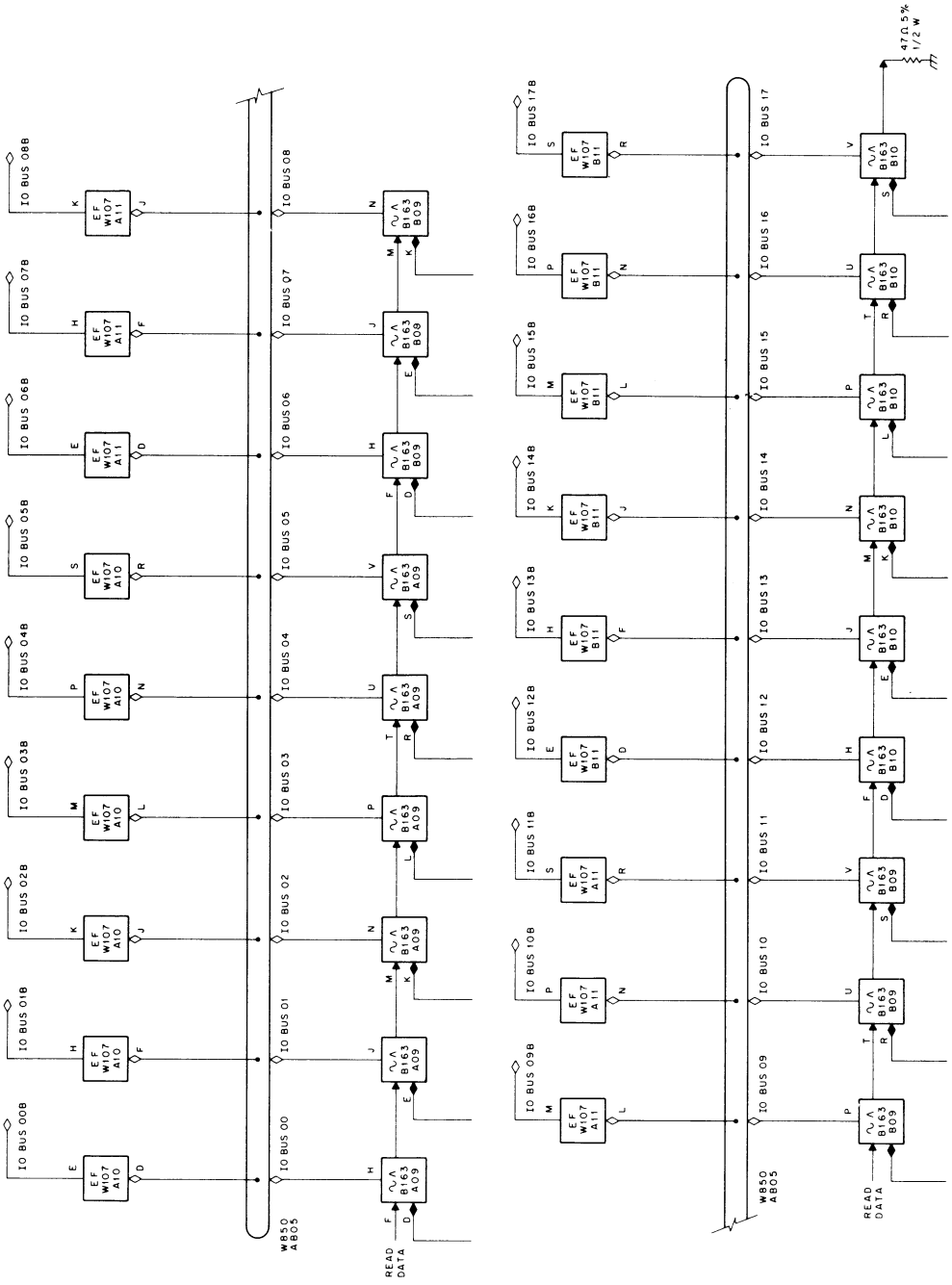


Figure C-5 I/O Bus RCVRS and Gates

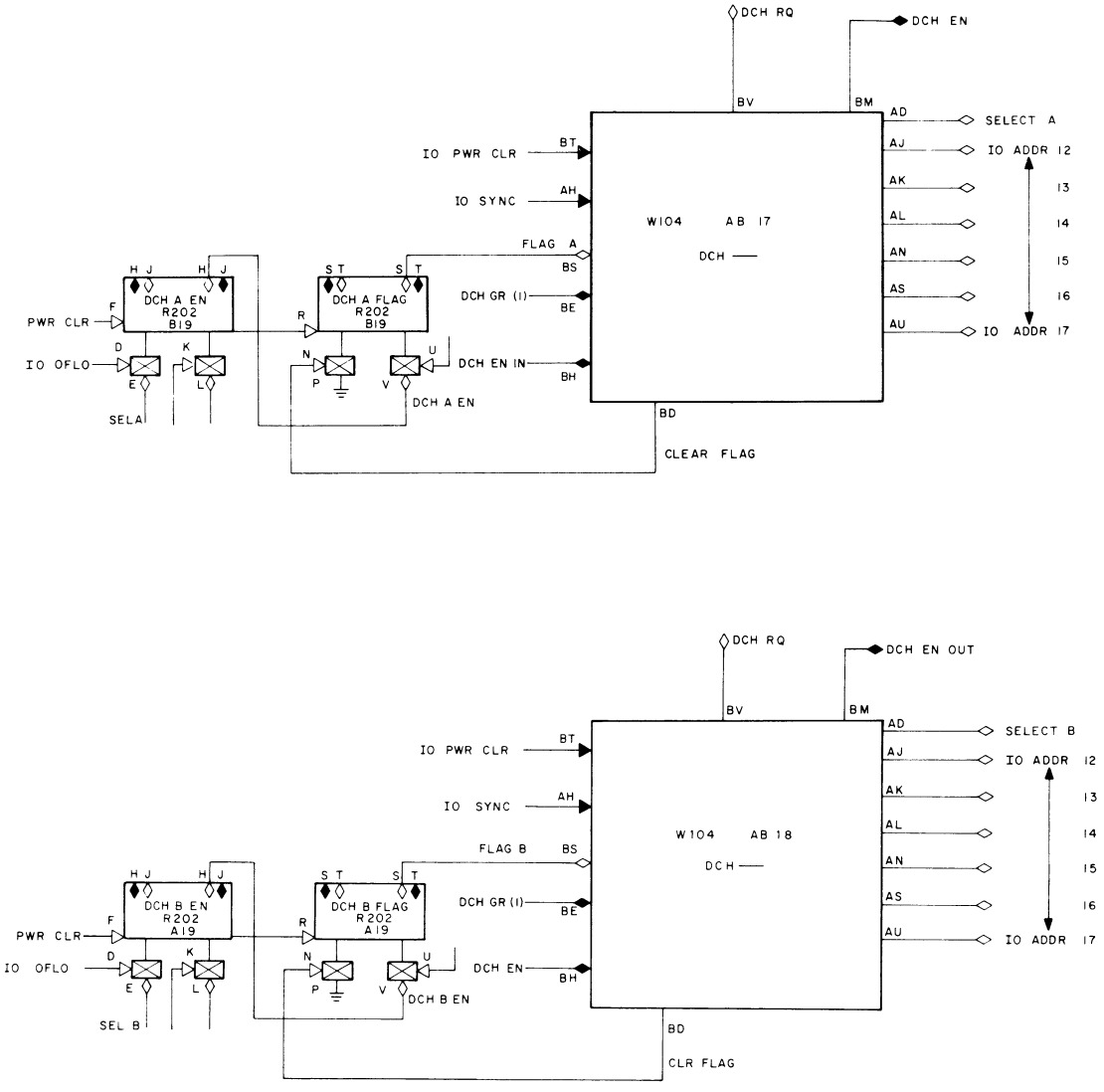


Figure C-6 DCH Logic