Digital Equipment Corporation
Maynard, Massachusetts

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DEC-8E-HR2B-D-KA8

POSITIVE I/O BUS INTERFACE OPTION

The information in this preliminary manual will become, in its final form, a part of the *PDP-8/E Maintenance Manual, Volume 2.*

PRELIMINARY

1st Preliminary Edition, August 1971

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1.0 INTRODUCTION

The Positive I/O Bus Interface, KA8-E, permits use of a PDP-8/I or PDP-8/L-type peripheral with the PDP-8/E. If the peripheral is a data break device, a Data Break interface, KD8-E, must also be in the system. The concept of data transfers and the interrelationship of the Positive I/O Bus Interface, the Data Break Interface, and the OMNIBUS are explained in Chapters 6 and 10 of the Small Computer Handbook - 1971. A detailed discussion of the CPU operation during a programmed I/O transfer is presented in Volume 1, Chapter 3, Section 6 of this maintenance manual. The reader should be thoroughly familiar with this referenced information to benefit from the detailed logic discussion presented in this chapter.

2.0 BLOCK DIAGRAM

Figure 2-1 is a functional block diagram of the Positive I/O Bus interface. When an IOT instruction has been placed on the OMNIBUS MD lines, the I/O PAUSE L signal is asserted by the CPU Timing Generator. If INTERNAL I/O L is not asserted by an internal peripheral, I/O PAUSE L causes the interface IOP Timing to assert the NOT LAST TRANSFER L signal. Thus, CPU timing is suspended at TP3 time. Simultaneously, IOP timing is initiated and the IOP signal that is subsequently generated enables the BIOP Pulse Generator to produce one or more pulses. These pulses are used by the peripheral in conjunction with BMB bits to decode IOT instructions.

The IOT instruction can clear and set flags and registers within the peripheral, or it can direct a data word transfer or a SKIP operation. Data words are transferred between the Data Gating logic and the CPU via the DATA 0-11 lines; between the peripheral and Data Gating, the data path depends on the direction of transfer, as shown in the block diagram. The OMNIBUS C-lines are asserted within the Data Gating logic in combinations that depend on the type and direction of transfer.

If a Skip operation is directed by the IOT instruction, the peripheral asserts the external SKIP L signal when conditions warrant. IOP Timing clocks the Skip Counter and either the DATA 10 or DATA 11 line, or both, is activated.

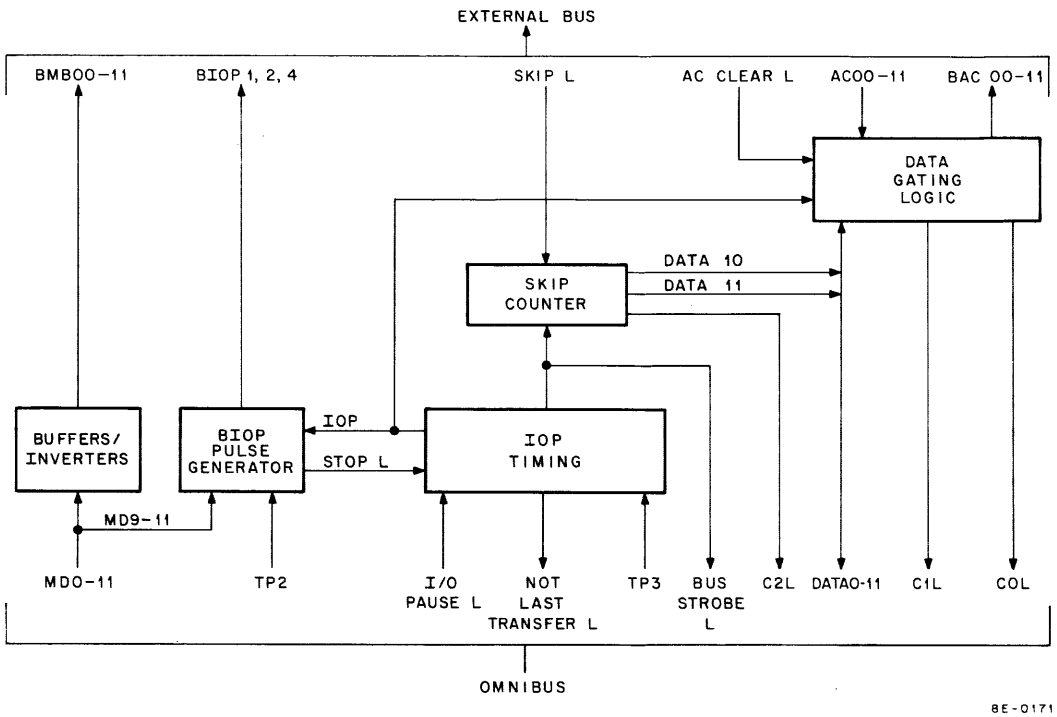

Figure 2-1 Block Diagram, Positive I/O Bus Interface

3.0 DETAILED LOGIC

3.1 BIOP Pulse Generator Logic

Figure 3-1 shows the BIOP pulse generator logic, which converts MD bits 9, 10, and 11 to BIOP pulses 4, 2, and 1, respectively. A logic 1 on any MD line conditions a corresponding NAND gate for enabling at TP2 time. When the NAND gate is enabled, it dc-sets a flip-flop that, in turn, conditions another NAND gate. Simultaneously, the flip-flop causes the STOP L signal to be negated. If an I/O transfer involving an external bus peripheral is in progress, the STOP L signal enables TP3 to initiate the IOP Timing operation. The IOP Timing logic (Paragraph 3.3) responds by asserting a signal (IOP) that enables the flip-flop-conditioned NAND Gate. The resulting signal is buffered and designated BIOP4, BIOP2, or BIOP1.

For example, if MD bit 9 is a logic 1, flip-flop IO4 is dc-set at TP2 time (note that the IO flip-flops are cleared at each TP1 time). The 0-output of the flip-flop causes STOP L to be asserted and, providing the IO1 and IO2 flip-flops are cleared (MD bits 10 and 11 are logic 0), the 1-output conditions NAND gate E24 for enabling by the IOP signal. When the IOP Timing asserts the IOP signal, E24 is enabled and the BIOP4 pulse is generated. The width of the pulse can be varied by adjusting a potentiometer in the IOP Timing logic, thereby asserting the IOP signal for the desired amount of time (see Paragraph 3.3). When the IOP signal is negated, E24 is disabled. Because the output of E24 is connected to the clock input of IO4, the flip-flop is cleared when E24 is disabled (note that the D inputs of the IO flip-flops are connected to ground; thus, a positive transition at a clock input clears the flip-flop). The 0-output of IO4 negates the STOP L signal and this action causes the IOP Timing logic to terminate the I/O dialogue.

This example stipulated that MD bits 10 and 11 were logic 0. Suppose, instead, that all three MD bits are logic 1. All three IO flip-flops are then set at TP2. The STOP L signal is asserted and the 1-output of IO1 conditions E11C for enabling by the IOP signal. Observe that the 0-output of IO1 disables both NAND gate E8B and NAND gate E24. Thus, the IOP signal enables E11C first and the BIOP1 pulse is generated. When the IOP signal is negated, E11C is disabled and IO1 is cleared. This action removes the disabling signal from E8B; however, E24 remains disabled because the 0-output of IO2 is one of its inputs. NAND gate E8B is now conditioned for enabling by the IOP signal. When this signal is again asserted by the IOP Timing logic, BIOP2 is generated. When BIOP2 ends, IO2 is cleared removing the disabling signal from E24. Now the BIOP4 pulse is generated, as detailed earlier.

Thus, the BIOP Pulse Generator logic operates in such a way that the BIOP pulses are not assigned specific time slots. If only one of the MD bits is a logic 1, then the corresponding BIOP pulse, whether 4, or 2, or 1, is generated at the first assertion of the IOP signal. If more than one MD bit is a logic 1, the least significant bit is selected first and its corresponding BIOP pulse is generated; the most significant bit is selected last.

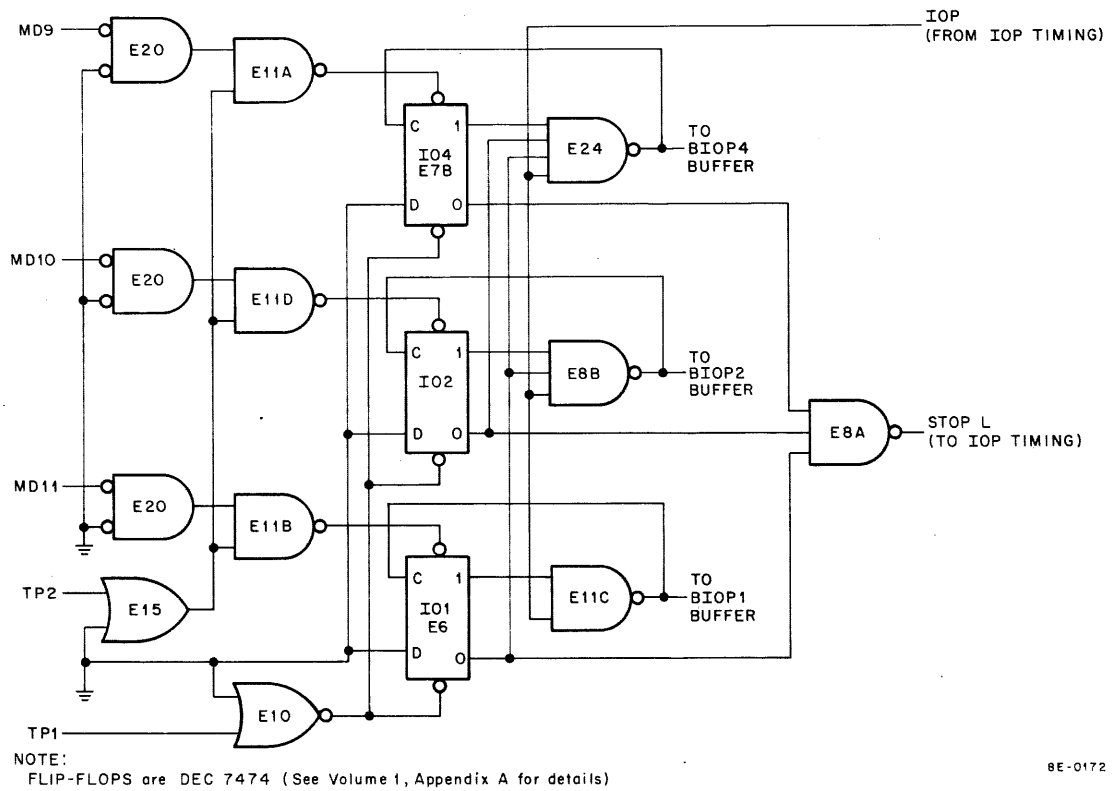

Figure 3-1 BIOP Pulse Generator Logic

3.2 BMB Buffers/Inverters

The preceding section discussed the BIOP pulse generator. A peripheral uses these BIOP pulses in conjunction with BMB bits to decode IOT instructions. The BMB bits are derived from the OMNIBUS MD bits, which are buffered and inverted by the interface. Figure 3-2 shows the buffer/inverter network.

BMB bits 03-08 are used in peripheral device selection logic. Both the true and the false states of these bits are derived from the corresponding MD bit; this minimizes the device selection network in the external peripheral. Although programmed transfer peripherals use the BMB bits only for device selection, data break peripherals receive output (from the CPU) data via the BMB 00-11 lines. Thus, all 12 BMB bits are derived, as shown in Figure 3-2.

3.3 IOP Timing Logic

Figure 3-3 shows the IOP Timing logic, which determines the duration of BIOP pulses and the separation between individual pulses, if more than one is programmed. Separation and duration can be individually varied by potentiometers that are indicated on the logic diagram and on the KA8-E etch as IOP SEP and IOP WIDTH. These potentiometers determine the triggered delay time of associated one-shot multivibrators, shown as part of DEC 74123 ICs. Briefly, the one-shots contained within a 74123 can be triggered by:

a. a positive transition at pin 2, if, prior to the transition, pin 1 is low and the clear (C) input is high (for the 'B' half of the IC, substitute pin 10 and pin 9 for pin 2 and pin 1, respectively),

b. a negative transition at pin 1, if, prior to the transition, pin 2 is high and C is high,

c. a positive transition at the C input, if, prior to the transition, pin 1 is low and pin 2 is high (see Appendix A for details about the DEC 74123 IC).

Figure 3-4 shows the IOP timing for a typical I/O transfer. The IOP signal is asserted twice during the time that I/O PAUSE is active; thus two BIOP pulses are generated by the BIOP Pulse Generator (the identity of the BIOP pulses does not affect the waveform relationship). The waveforms representing SEP and WIDTH are shown for the minimum allowable triggered delay time, viz., 200 nano-seconds for SEP and 600 nano-seconds for WIDTH. The potentiometer values allow these delay times to be increased to five times the minimum value. Refer to both figures while studying the following description.

If the I/O transfer involves an external bus peripheral (INTERNAL I/O L remains negated) and the BIOP Pulse Generator negates the STOP L signal, NAND gate E28 asserts the NOT LAST TRANSFER L signal; this signal indicates to the CPU Timing Generator the impending interruption of normal timing. At TP3 time the IOP Timing is initiated, while the CPU timing is suspended in TS3.

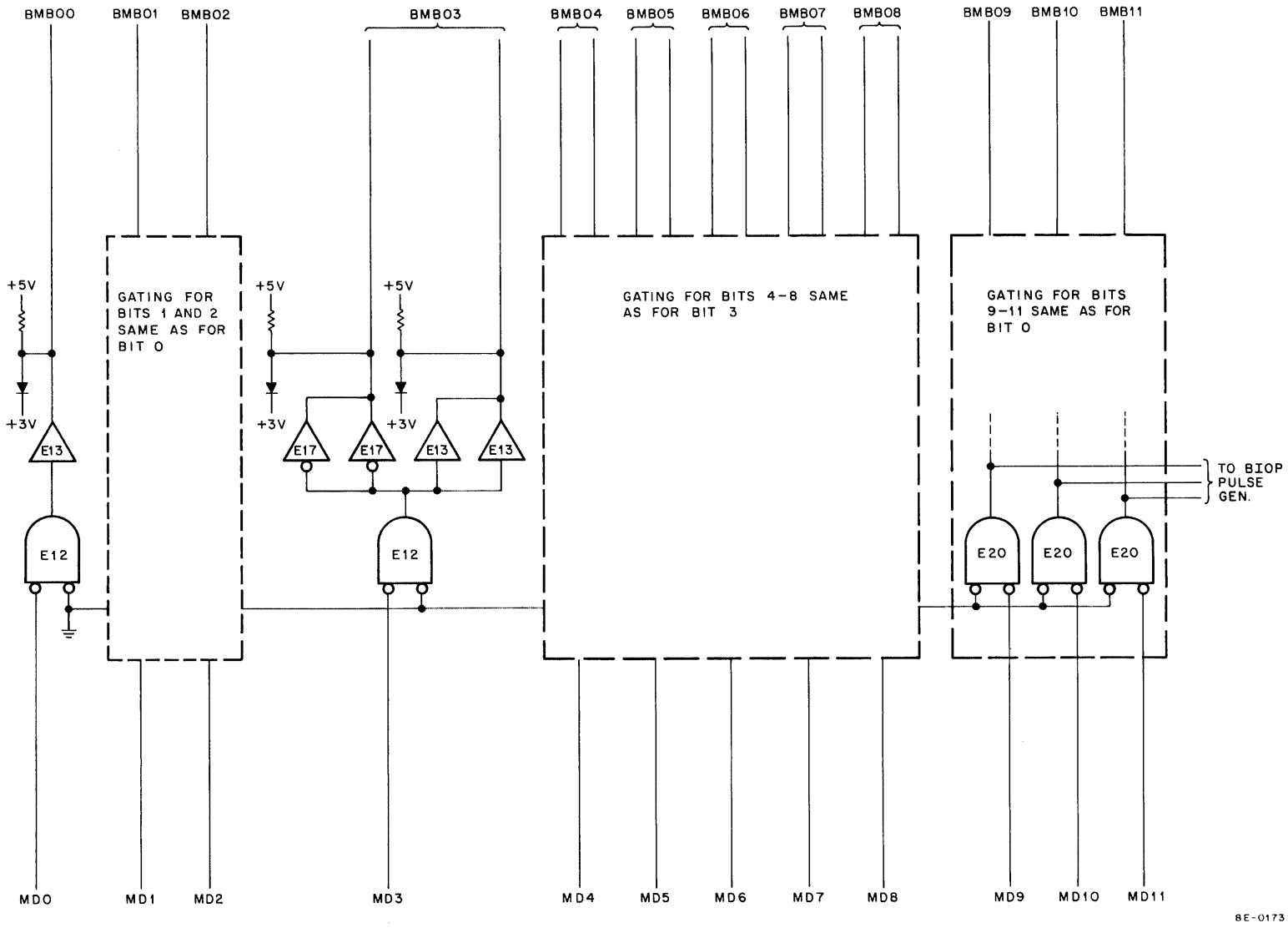

Figure 3-2 BMB Buffers/Inverters

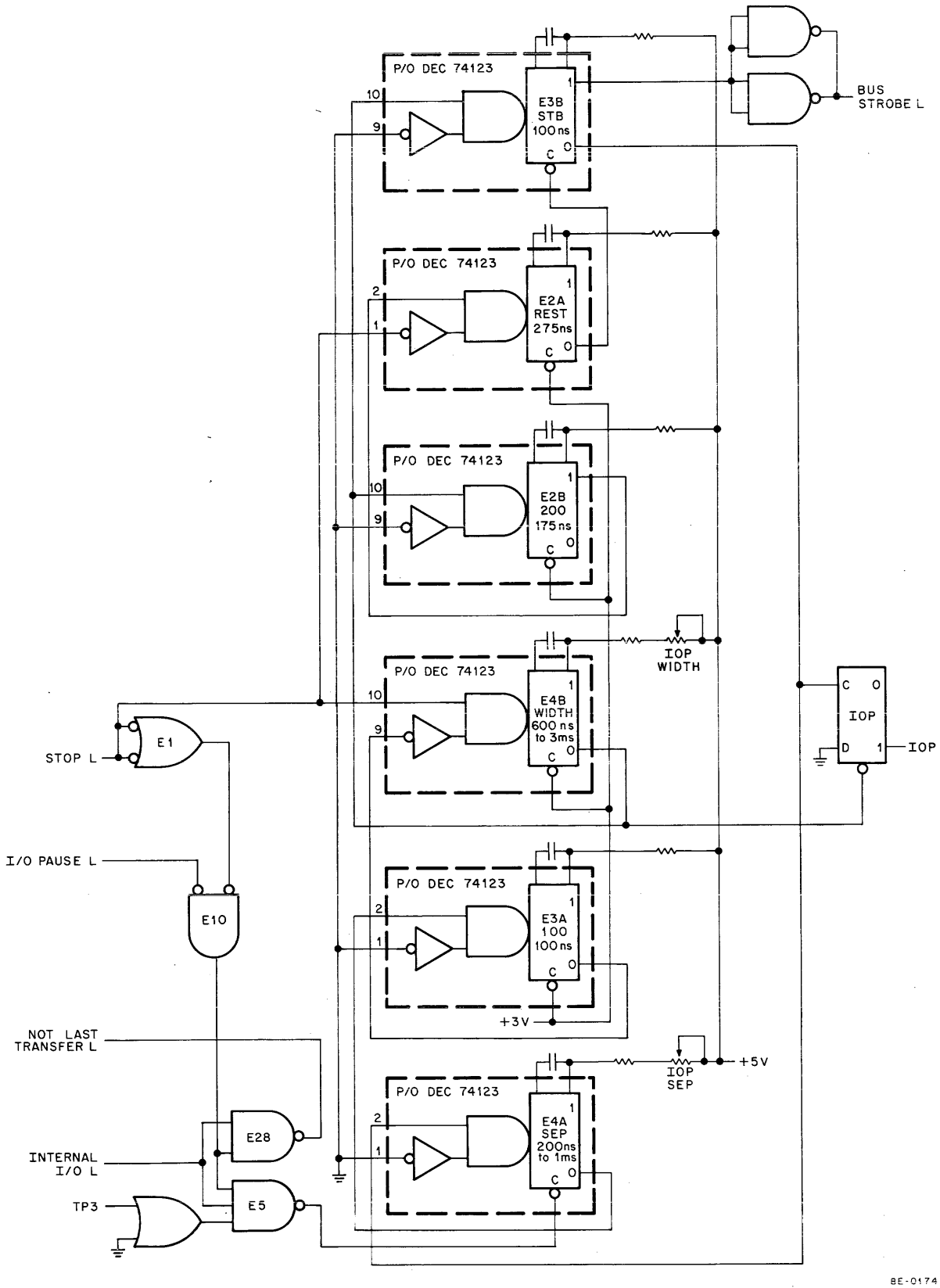

Figure 3-3 IOP Timing Logic

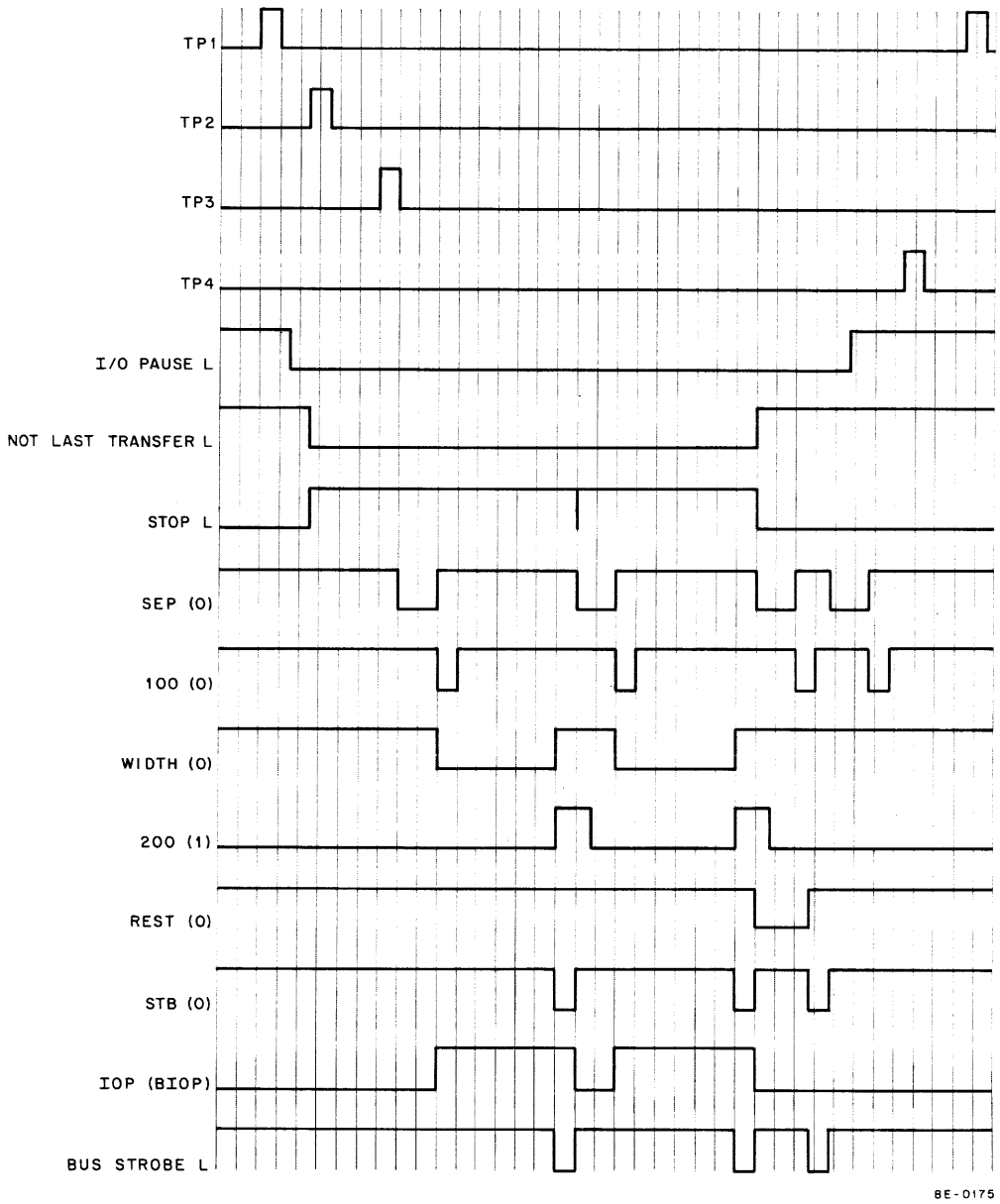

Figure 3-4 Waveforms, IOP Timing Logic

IOP timing begins when the SEP one-shot is triggered by the positive transition at its C-input. SEP (0) is used to trigger the 100 one-shot, which, in turn, triggers WIDTH. WIDTH (0) sets the IOP flip-flop and the resulting IOP signal enables the BIOP pulse generator to begin the BIOP pulse. The STB (Strobe) one-shot, triggered by the end of WIDTH (0), clears the IOP flip-flop; thus, the duration of the BIOP pulse is 100 nano-seconds longer than the duration of WIDTH (0). A BUS STROBE L signal is generated by STB (1) at the end of each BIOP pulse to execute the instruction represented by the BIOP pulse (BUS STROBE L causes the AC LOAD L signal to be asserted in the CPU; see Volume 1, Chapter 3, Section 6 for details). When the first BIOP pulse has ended, the sequence outlined begins anew, this time with STB (0) triggering the SEP one-shot. When the last BIOP pulse ends, the STOP L signal is asserted by the BIOP pulse generator. This signal ensures that the WIDTH one-shot is not triggered by the next transition of 100(0). Therefore, the IOP flip-flop remains clear through the remainder of the IOP timing. When REST (0) (the Re-start one-shot), which is triggered by the STOP L signal transition, goes positive after 275 nano-seconds, STB is triggered again, producing a final BUS STROBE L signal. This BUS STROBE terminates the I/O dialogue and reinstates the CPU timing.

The 100 one-shot is necessary for proper triggering of WIDTH. It provides a negative transition at pin 9 of WIDTH when SEP times out. If the negative transition were supplied by the 0-output of SEP, itself, WIDTH would trigger at the same time as SEP. On the other hand, if the negative transition were supplied by the 1-output of SEP, WIDTH would trigger at TP2 time, when the STOP L signal is negated. Consequently, the 100 one-shot is quite important to the timing operation.

The 200 one-shot is also important to the timing logic. Note on Figure 3-4 that the STOP L signal is shown to have a spike that is coincident with the trailing edge of the first BUS STROBE signal (if three BIOP pulses were generated, there would be two spikes shown). This spike is a representation of the tendency of the STOP L signal to go low at the end of the IOP signal (NAND gate E8A in the BIOP Pulse Generator becomes momentarily indecisive at this point in the timing). The 200 one-shot brackets this spike in time and, thus, prevents the REST one-shot from triggering prematurely.

3.4 Data Gating Logic

The data gating logic is shown in Figure 3-5. During a programmed I/O transfer, data is transferred to or from the CPU on the OMNIBUS DATA 0-11 lines. Output data (from the CPU) is gated from the DATA lines through an interface buffer/inverter network (illustrated in Figure 3-5 for bits 0 and 11) to the external bus BAC 00-11 lines. If the output transfer is to be accompanied by a clearing of the CPU AC Register, the peripheral is directed (by the BIOP pulse) to assert the OMNIBUS C0 L signal. The peripheral does this indirectly by grounding the external bus AC CLEAR line. The AC CLEAR L signal causes NAND gate E25D on the interface to assert the C0 L signal. If the AC Register does not have to be cleared, the C-lines remain negated throughout the transfer.

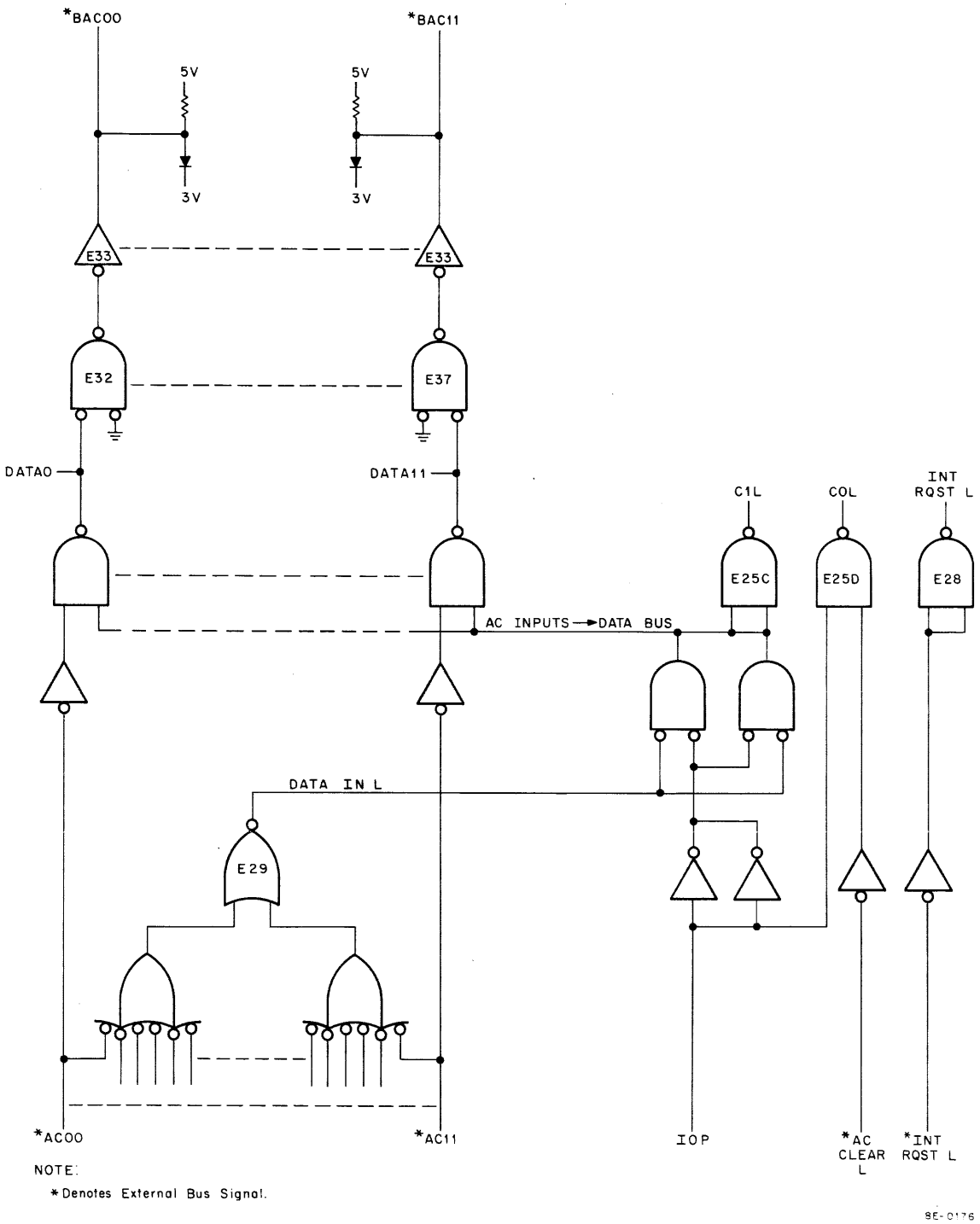

Figure 3-5 Data Gating Logic

On the other hand, an input transfer must always be accompanied by the assertion of at least one C line. Note that when a data word is transferred from the peripheral on the external bus AC 00-11 lines, the interface DATA IN L signal is asserted by NOR gate E29. If the data is placed on the AC lines during the BIOP pulse (as it must be), NAND gate E25C asserts the C1 L signal. Simultaneously, the AC INPUTS → DATA BUS signal gates the data onto the OMNIBUS DATA 0-11 lines. The result of these actions is an 'OR' operation of the AC contents and the data on the DATA 0-11 lines. The peripheral can cause a JAM input by grounding the AC CLEAR line, thereby asserting the C0 L signal. Thus, only the information on the DATA 0-11 lines is placed in the AC Register. Note that if data word 0000_8 is transferred from the peripheral, the DATA IN L signal is not asserted. To transfer 0000_8 the peripheral must ground the AC CLEAR line and, in effect, cause a JAM input of zeros.

These are the four types of data transfers that can be made by the PDP-8/I-type peripherals. Another form of I/O transfer, other than a 12-bit data word, that is, utilizes the interface SKIP logic to update the CPU PC Register. This type of transfer is discussed in Paragraph 3.5.

3.5 Skip Counter Logic

The peripheral, when directed by an IOT instruction, can cause a skip of 1, 2, or 3 program instructions. It initiates a skip operation by grounding the external bus SKIP line. The interface Skip logic, shown in Figure 3-6, asserts the OMNIBUS DATA 10 and/or DATA 11 lines, depending on the number of instruction skips required (during a SKIP operation the peripheral does not place data on the AC00-11 lines). At the same time, the OMNIBUS C-lines are manipulated to provide a path for the DATA bits through the CPU major register gating to the PC Register. The DATA bits are added to the contents of the PC register, increasing the program count in the register by 1, 2, or 3.

The timing diagram of a typical skip operation is shown in Figure 3-7. Refer to this diagram and to Figure 3-6 while studying the description that follows. The timing diagram shows that two BIOP pulses, 1 and 2, are generated during the IOT instruction. The imaginary peripheral that applies to this example decodes these 2 BIOP pulses and responds by grounding the SKIP line. Keep in mind that this is an example, only, and that this imaginary peripheral does not necessarily exist. The combination of BIOP1 and BIOP2 can produce a variety of operations, depending on how a peripheral decodes the pulses.

Nevertheless, when TP3 starts the IOP timing, this peripheral is directed to initiate a skip operation by asserting SKIP L. The SKIP line controls the D input of flip-flop E9, which is clocked when the STB one-shot is triggered. Because STB is triggered at the end of each BIOP pulse, E9 can be clocked twice during IOP timing. Note that the 100 one-shot dc-sets E9. Thus, E9 is set at the first triggering of the 100 one-shot, or (as is shown in Figure 3-7) during a previous IOP timing cycle. 100 and STB are triggered alternately thereafter. Thus, E9 is alternately cleared and set, as long as SKIP L is

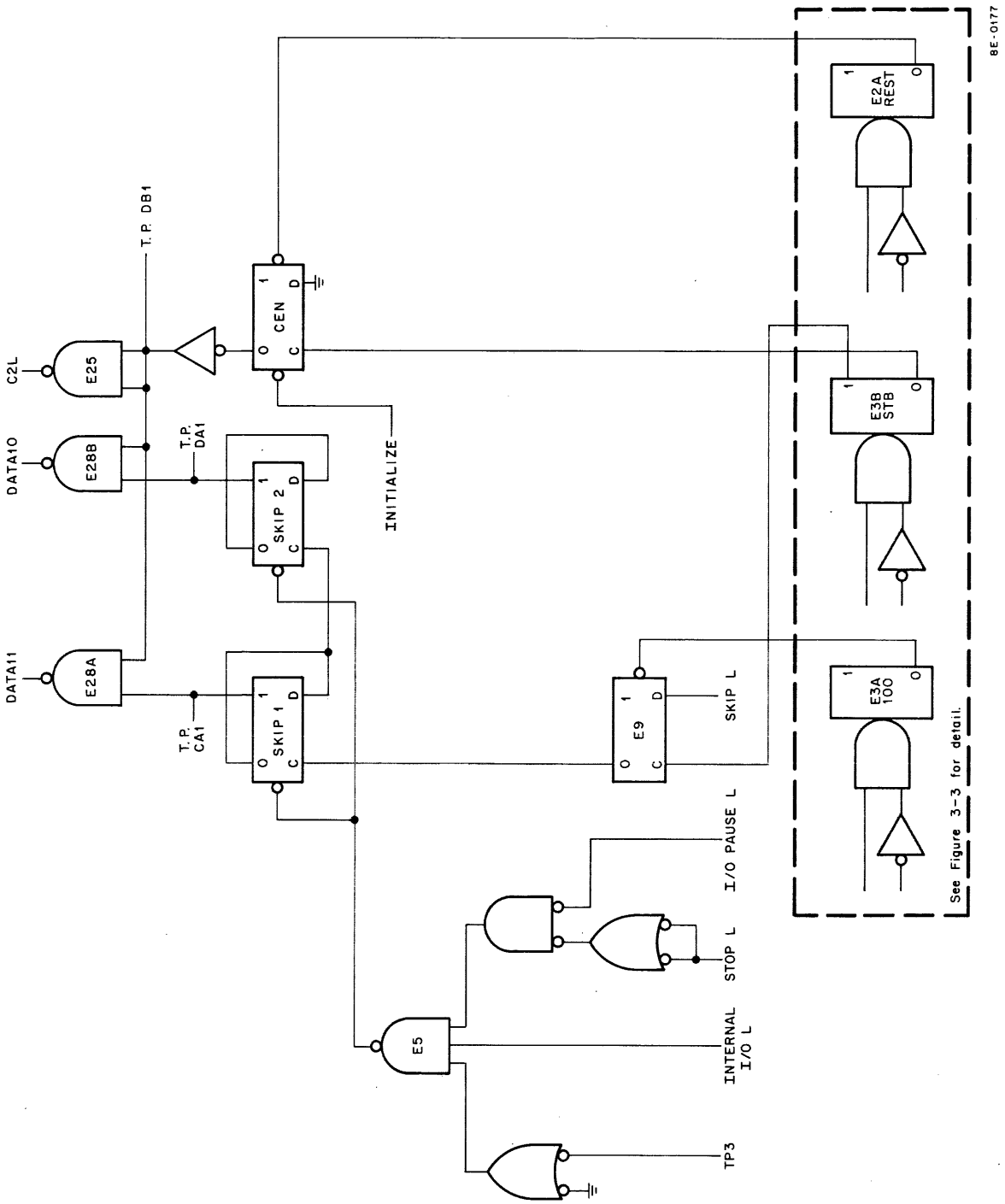

Figure 3-6 Skip Logic

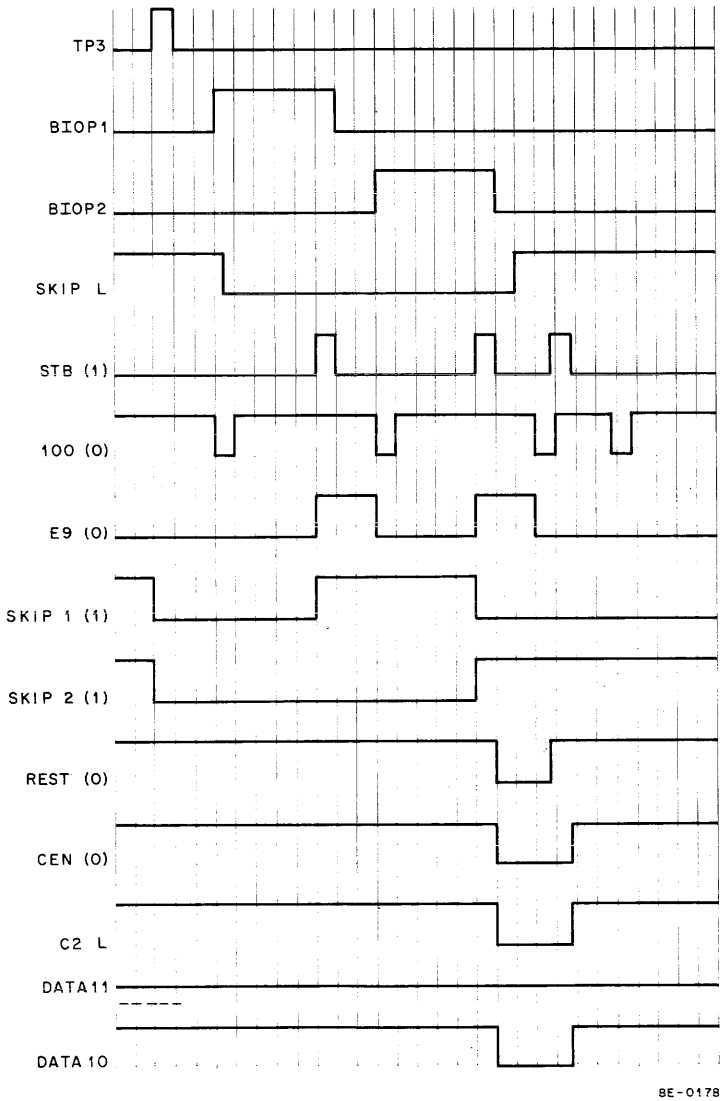

Figure 3-7 Timing, Skip Logic Application

asserted. Each time E9 is cleared, SKIP1, the first stage of the 2-stage binary counter, is clocked. In this example, the binary counter is clocked twice, indicating that two instructions are to be skipped. SKIP2 is set at the second triggering of STB. The C-line enable (CEN) flip-flop is dc-set by the REST one-shot, enabling NAND gates E25 and E28B (note that CEN is clocked by STB at the same time that it is dc-set by REST; the dc-input takes precedence in such a case). The assertion of C2L, while C1L and C0L are left negated, provides a path for DATA10 through major register gating to the PC Register. C2L and BUS STROBE (generated when REST times out) assert PC LOAD L and DATA 10 is added to the contents of the PC Register, updating it by two. Note that the SKIP line must be negated before STB is triggered by the trailing edge of REST (0). If not, the binary counter is erroneously clocked one more time.

4.0 MAINTENANCE

There are no specific maintenance procedures for the KA8-E, itself. Each DEC peripheral that connects to the KA8-E has an associated MAINDEC or exerciser program that enables the technician to maintain both the option and the KA8-E interface. Because all these peripherals use the one interface, a fault in the interface can be isolated by running a number of MAINDEC programs. If all programs result in errors, one can reasonably conclude that the KA8-E is at fault.

General information concerning corrective maintenance is included in Volume 1, Chapter 4. The technician will find this material helpful. The interface schematic, E-CS-M8350, indicates important test points, IC locations, and pin numbers and should be used whenever maintenance is being performed.

The KA8-E connects directly to a single peripheral via three cables that are supplied with the interface (see the Small Computer Handbook - 1971, Chapter 10 for cabling rules and suggestions). Each cable connects to the interface with a 40-pin Berg connector and to the peripheral with a DEC M953A cable connector. From-To information for the cable is given in Table 4-1 (the cables are identical; see Chapter 10 of the Small Computer Handbook - 1971 for details concerning proper connection of the cables).

5.0 SPARE PARTS

To be supplied.

Table 4-1
KA8-E Cable Information

From (M953A Cable Conn.)	To (Berg Conn.)	From (M953A Cable Conn.)	To (Berg Conn.)
Gnd	A	Gnd	Y
Gnd	B	M2	Z
Gnd	C	Gnd	AA
B1	D	L1	BB
Gnd	E	Gnd	CC
D2	F	P2	DD
Gnd	H	Gnd	EE
D1	J	M1	FF
Gnd	K	Gnd	HH
E2	L	S2	JJ
Gnd	M	Gnd	KK
E1	N	P1	LL
Gnd	P	Gnd	MM
H2	R	T2	NN
Gnd	S	Gnd	PP
H1	T	S1	RR
Gnd	U	Gnd	SS
K2	V	V2	TT
Gnd	W	Gnd	UU
J1	X	Gnd	VV

Pins A2, B2, U1, and V1 on M953A not used.
Pins A1, C1, F1, K1, N1, R1, T1, C2, F2, J2, L2, N2, R2, and U2 on M953A are ground pins.

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MASTER DRAWING LIST

MAINTENANCE MANUALS NO.	MAINTENANCE MANUALS TITLE	UNIT VARIATIONS KA8-E
	KA8-E POSITIVE I/O BUS INTERFACE	X

USED ON OPTIONS

REVISIONS

REV.	DATE	CHG. NO.	APP'D.
A	3/23/71	00001	L.K.
B	7/71	MISC-86	A.V.
C	8/71	KA8E-2. revs	

DRN. K. GULICK	DATE 1/18-71	digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS
CHK'D K. GULICK,	DATE 1/18-71	
ENG. L. KLOTZ	DATE 3-5-71	TITLE POSITIVE I/O BUS INTERFACE
PROJ. ENG. R. VOGELSANG	DATE 3-5-71	
PROD. L. SAYLOR	DATE 3-5-71	
FIRST USED ON PDP8/E		SIZE A · CODE ML · NUMBER KA8-E · REV. C
SCALE NONE		
SHEET 1 OF 2		DIST.

DRA 131

Dec 16-(325)-1048-N471

PRINT SET KA8-E	DWG. NO.	REV. LET.	NO. OF SHEETS	TITLE	OPTION NO.
–	A-PL-KA8-E-Ø	A	1	POSITIVE I/O BUS INTERFACE (PARTS LIST)	
X	E-CS-M8350-Ø-1	#	3	POSITIVE I/O BUS INTERFACE	
–	A-SP-KA8-E-1	REF	2	KA8-E/KD8-E MANUFACTURING TEST PROCEDURE	

TITLE				
POSITIVE I/O BUS INTERFACE	SHEET 2 OF 2	SIZE A · CODE ML	NUMBER KA8-E	REV. C

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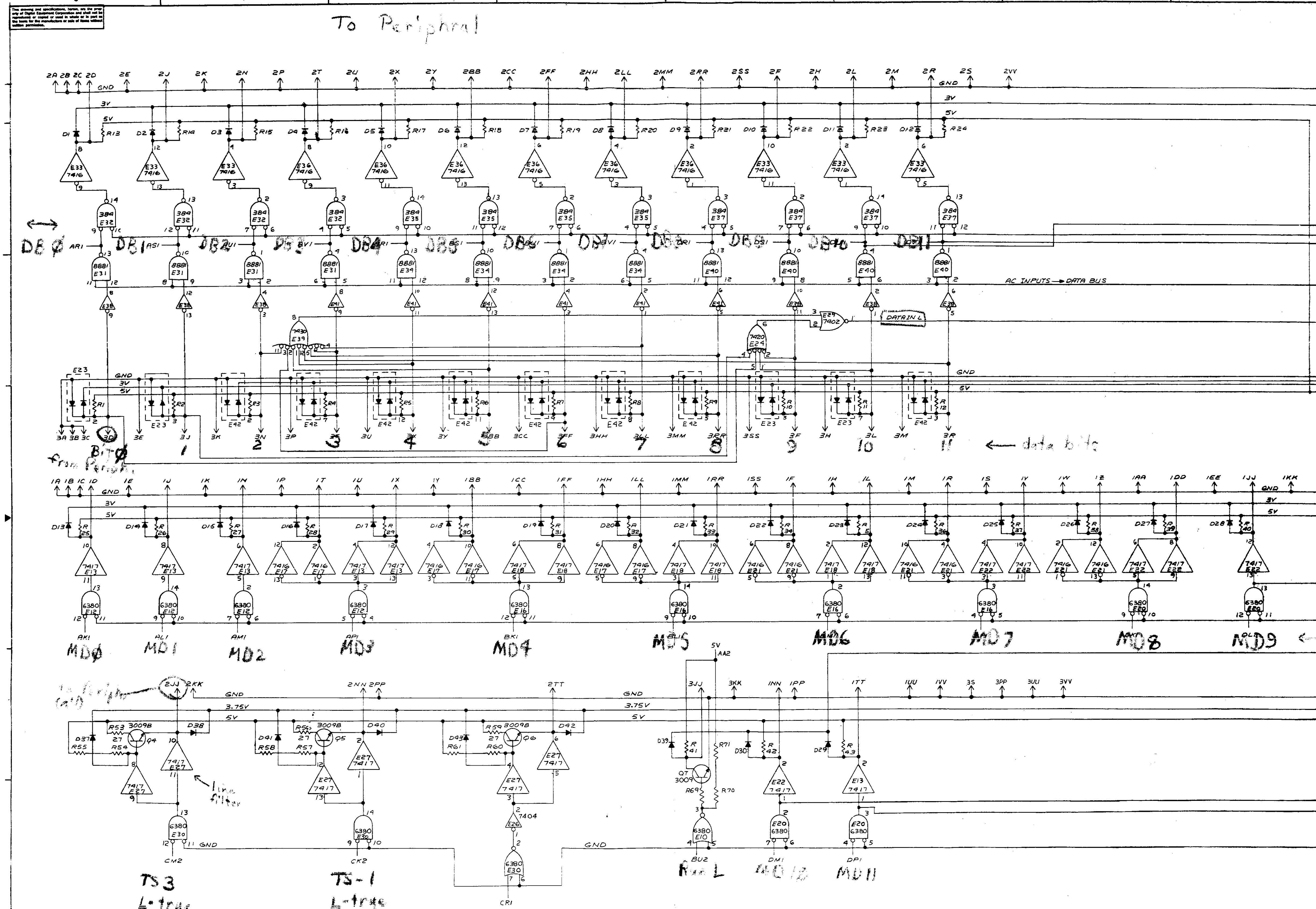

FIRST USED ON OPTION/MODEL: PDP 8/E

UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
DECIMALS ±.005 FRACTIONS ± 1/64 ANGLES ± 0°30'
FINAL SURFACE QUALITY √
REMOVE BURRS AND BREAK SHARP CORNERS

digital EQUIPMENT CORPORATION, MAYNARD MASSACHUSETTS

TITLE: POSITIVE I/O BUS INTERFACE

SIZE: C | CODE: CS | NUMBER: M8350-Ø-1 | REV.: A