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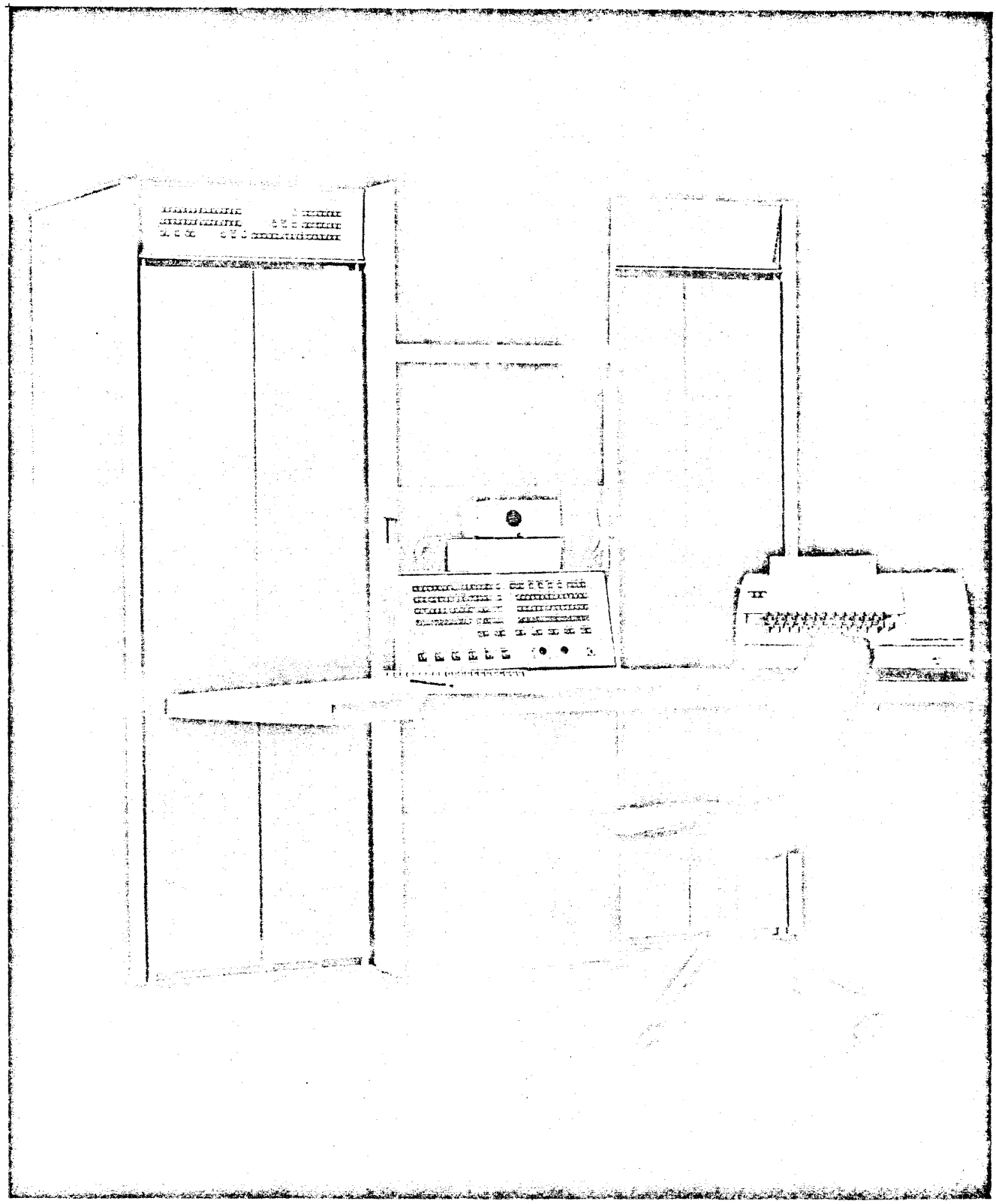


Figure 1-1 Programmed Data Processor-7

CHAPTER 1

INTRODUCTION AND DESCRIPTION

The Digital Equipment Corporation (DEC) Programmed Data Processor-7 (PDP-7) is a general purpose, stored-program, solid-state digital computer designed for use in laboratories, computing centers, or process control systems. The PDP-7 is single-address, fixed 18-bit word-length, binary computer using 1's complement arithmetic and 2's complement notation to facilitate multiprecision arithmetic. A basic PDP-7 contains a 4096- or 8192-word, random access, ferrite-core memory which can be expanded in increments of 4096 words to a maximum capacity of 32,768 words by the use of additional memory modules and a DEC Type 148 Core Memory Extension Control. High-capacity, flexible input/output circuits permit the computer to operate with all modern types of data processing equipment and many types of process-control instruments.

The basic PDP-7 includes the processor (with operator console), 4096-word core memory, input/output control with a device selector that permits selection of up to 64 I/O devices and is expandable, information collector, information distributor, and real-time clock. The processor provides facilities for program interrupt, data interrupt (for use with high-speed I/O devices), I/O status check, I/O skip, and I/O trap (which provides the basic hardware necessary for a time-shared or multiuser system). The input/output equipment supplied with a basic PDP-7 system consists of a high-speed perforated tape reader (300 char/sec); a high-speed paper tape punch (63.3 char/sec); and a Model 33 KSR Teletype unit (10 char/sec).

The PDP-7 is completely self-contained and requires no special power sources, air-conditioning, or floor bracing. The PDP-7 draws its primary power from a single source of 115v, 60-cps, single-phase power, and from this source produces all required operating voltages. Upon request, PDP-7 systems can be supplied to operate from 220v, 50- or 60-cps supplies. Built-in provisions for varying the +10 and −15v supplies that power the logic permit the operation of the logic to be checked under marginal conditions. The computer is constructed with standard DEC FLIP CHIP™ modules and power supplies.

™FLIP CHIP is a trademark of the Digital Equipment Corporation

This manual provides information required for maintaining a basic PDP-7 system. The manual also provides information concerning the following commonly used options: Type 177 Extended Arithmetic Element, Type 172 Automatic Priority Interrupt, and Type 173 Data Interrupt Multiplexer.

COMPUTER ORGANIZATION

The computer consists of a processor (with operator console), a core memory, interface equipment, and input/output equipment. Figure 1-2 illustrates the interrelationship of these elements. All arithmetic, logic, and system control operations are performed by the processor. Temporary information storage is provided by the various registers of the processor and by associated input/output devices. Permanent information storage (longer than one instruction time) is provided by the core memory. During each computer cycle lasting 1.75 μsec, the core memory automatically performs a read operation and a write operation under the control of timing signals produced by the processor. Interface circuits permit connections to a variety of peripheral equipment, and are responsible for detecting all I/O select codes and for providing necessary input or output gating. Individually programmed data transfers between the processor and peripheral equipment take place through the accumulator. The data break facility permits single or multiple data transfers to be initiated by a high-speed I/O device; each transfer using the data break is completed in a single computer cycle. The interface circuits also permit peripheral equipment to perform certain control functions, such as instruction skipping or the initiation of a program interrupt to transfer program control.

Processor

The processor performs logical and arithmetic functions, controls the storage and retrieval of information on core memory and controls the flow of information to and from peripheral equipment. The processor consists of control logic and six major registers. Associated with the processor is the operator console, which permits the information contents of memory and of the major registers to be manually established, modified, or examined.

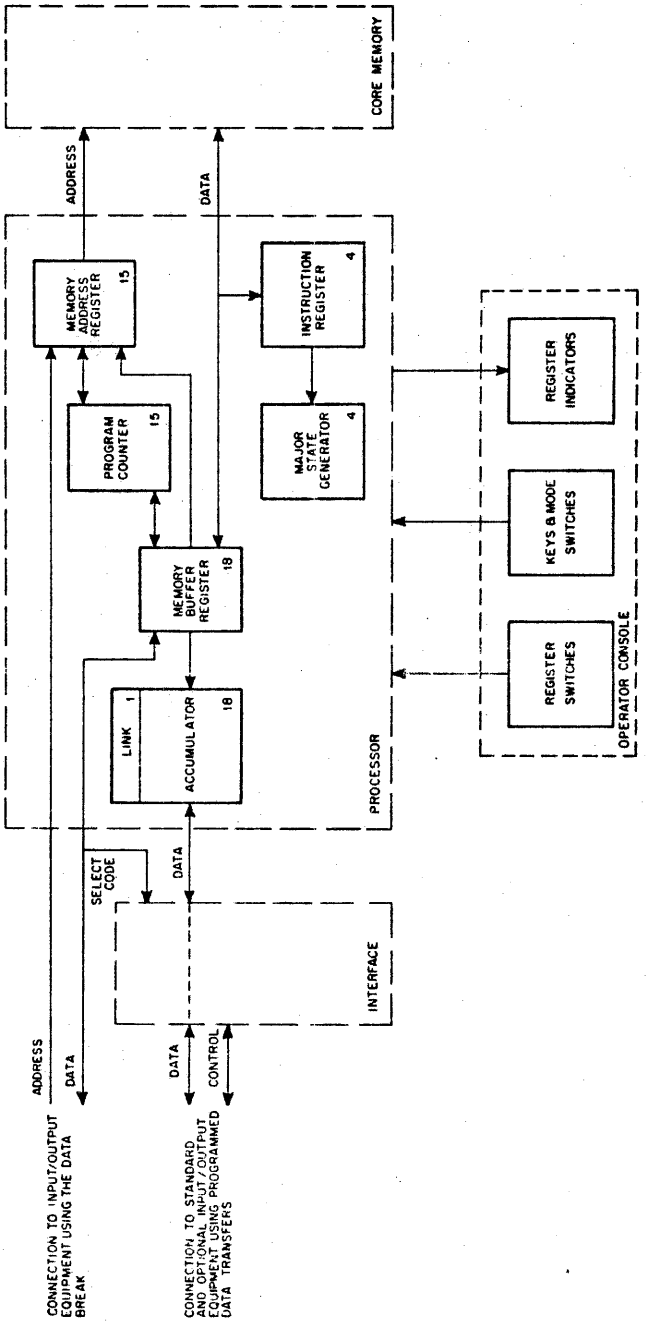


Figure 1-2 Major Registers, Simplified Block Diagram

Accumulator (AC) and Link (L)

The AC is an 18-bit register which performs arithmetic and logical operations on the data and serves as a transfer register for programmed information transfers between core memory and peripheral equipment. The link is a 1-bit register which extends the arithmetic facility of the AC and simplifies the programming of arithmetic operations. The link serves primarily as a carry or overflow register for the AC.

Memory Address Register (MA)

This 13-bit register holds the address of the core memory location currently being used. Two additional bits are wired into the basic PDP-7 but are used only if the memory storage capacity is extended beyond 8192 words by means of the memory extension options.

Memory Buffer Register (MB)

This 18-bit register serves as a buffer for all information passing to or from core memory from the processor or external devices using the data break.

Instruction Register (IR)

This 4-bit register holds the operation code of the instruction currently being performed.

Program Counter (PC)

This 13-bit register holds the address of the memory location from which the next instruction is to be taken. As in the MA, two additional bits are provided, but are used only in conjunction with the memory extension options.

Major State Generator

The major state generator is a multistate device which can assume any one of four stable states, each corresponding to one of the four major control states of the processor. One or more states are entered to execute a programmed instruction, but only one state exists at any one time.

Operator Console

All manual controls and all processor readouts and indicators are located on the operator console. These may be classified as follows:

1. Register switches, used to preset a binary number for transfer into an associated register. To facilitate presetting numbers specified in octal notation, the switches associated with each register are grouped in threes. The order of significance is from right (least significant) to left (most significant).

2. Keys and mode switches, used to initiate specific computer functions.

3. Register indicators, used to display the contents of an associated register. A lighted indicator lamp denotes a binary 1 in the associated bit of the register.

4. Primary power switches.

Core Memory

The high-speed random-access core memory of the basic PDP-7 is a 4096-word coincident-current core module with a read/write cycle time of 1.75 μsec. In each cycle, the memory reads an 18-bit word stored in the memory location specified by the MA, transfers the word into the MB, and rewrites the word into the same memory location. Extension of the core memory capacity to 8192 words may be accomplished merely by the addition of another 4K memory module, and requires no modifications to the processor. Extension of memory capacity beyond 8K requires the use of the memory extension options (memory modules and memory extension control).

Interface

The interface control links the processor to input and output stations, calls the stations, and collects and distributes the input/output data. It also controls the interleaving of high-speed data transfers between programmed instructions during the data break (cycle stealing); senses

the status of I/O devices and permits the status sensed to cause an instruction to be skipped; initiates program control transfers; and, in multiuser or time-shared systems, traps illegal instructions.

No additional interface equipment is required for the connection of standard DEC peripheral equipment to the PDP-7. If special-purpose devices are to be connected to the PDP-7, a suitable interface may easily be constructed using the standard line of FLIP CHIP modules manufactured by DEC.

Input/Output

The standard input/output equipment provided with a basic PDP-7 consists of a Model 33 KSR Teletype unit and DEC Type 649 Teletype Control, a Digitronics Type 2500 Perforated Paper Tape Reader and DEC Type 444B Reader Control, and a Teletype BRPE Perforated Tape Punch and DEC Type 75D Punch Control.

Teletype and Control

The Teletype unit is a standard machine operating from serial 11-unit code characters at a rate of 10 char/sec. The Teletype provides a means of supplying data to the computer by means of a keyboard, and of typing output data from the computer on a page-size paper roll. The Teletype control converts serial characters from the keyboard into parallel form for acceptance by the computer, and converts parallel computer output data into serial form for acceptance by the printer. The keyboard and printer, and their associated control circuits, form two separate and distinct information channels, though information typed on the keyboard is always printed by the printer.

Perforated Paper Tape Reader and Control

The reader senses information contained on 8-channel, fanfold paper tape photoelectrically, at a rate of 300 char/sec. The control contains a data register, a flag, and logic circuits which permit reader operation to be controlled by the stored program.

Perforated Paper Tape Punch and Control

The high-speed paper tape punch perforates 8-channel, fanfold paper tape at the rate of 63.3 char/sec. The control contains a data register, a flag, and control logic. All punching operations are performed under the control of the stored program.

Processor Options

The processor options described in this manual are the Type 177 Extended Arithmetic Element, The Type 172 Automatic Priority Interrupt, and the Type 173 Data Interrupt Multiplexer.

Extended Arithmetic Element

The extended arithmetic element (EAE) facilitates high-speed multiplication, division, shifting, normalizing, and register manipulation. Installation of the EAE adds an 18-bit multiplier-quotient register (MQ) and a 6-bit step counter register (SC) to the computer. The contents of the MQ are continuously displayed on the operator console. The EAE operates asynchronously with respect to the computer cycle, thereby permitting computations to be performed in the minimum possible time. Further, EAE instructions are microcoded so that several operations can be performed by one instruction. Average multiplication time is 6.1 μsec, average division time is 9 μsec.

Automatic Priority Interrupt

The automatic priority interrupt (API) increases the capacity of the PDP-7 to handle data transfers of information to and from I/O devices by directly identifying an interrupting device without the need to scan flags. The API is particularly useful in ensuring rapid servicing of I/O devices which retain their information for a limited period (such as the real-time clock or analog-to-digital converters). The API provides 16 automatic interrupt channels arranged in a priority sequence in which channel 0_8 has the highest priority and channel 17_8 the lowest. The priority chain guarantees that if two or more I/O devices request an interrupt concurrently, the first interrupt is granted to the device with the highest priority. The requests of the other devices are registered and are later serviced in order of priority. Multilevel interrupts are permissible, where a device of higher priority supersedes an interrupt already in progress.

Data Interrupt Multiplexer

The data interrupt multiplexer permits the single data break facility of the PDP-7 to be used by up to four high-speed I/O devices. Each device must supply 18 data lines, 15 address lines, a transfer direction signal, and a break request signal. When a data break is granted by the processor, each information transfer is completed within one computer cycle. The maximum combined transfer rate is 570,000 18-bit words/sec.

FUNCTIONAL DESCRIPTION

The PDP-7 performs arithmetic or logical operations upon data stored in the core memory. The nature and sequence of these operations is determined either by a series of instructions, also stored in memory (programmed operation), or by operation of keys and switches on the operator console (manual operation). Manual operation is restricted to the following: starting and stopping programmed operation; continuing programmed operation after a temporary halt; setting the starting address (memory location) of a program into the memory address register; depositing information in manually selected memory cells; examining the contents of manually selected memory cells; and the selection of special modes. For maintenance or debugging purposes, a deposit or examine operation may be repeated manually to permit visual monitoring by means of the register indicator lamps on the operator console or by signal tracing with an oscilloscope.

During programmed operation, the processor retrieves from memory the first instruction specified by the program, executes the instruction during one or more computer cycles (each cycle lasting 1.75 μsec), and then proceeds to retrieve and execute the remaining instructions specified by the program sequence. All arithmetic, logical, or control operations of which the computer is capable are performed as a function of three major determinants: the instruction retrieved from memory; the major control state established; and timing pulses produced by the processor.

Instructions

Instructions are of two types: memory reference and augmented. All instructions contain an operation code (specifying the nature of the instruction) in bits 0 through 3.

Memory reference instructions cause information to be stored in or retrieved from memory, and contain a memory address as well as an operation code. All memory reference instructions

require one computer cycle in which the instruction is retrieved, and all except the jump instruction require a second cycle in which to execute the instruction specified by the operation code. The jump does not cause storage or retrieval of information, but transfers control of the processor from one block of consecutive memory locations (containing instructions) to a different block of consecutive locations. The jump instruction is normally completed in one computer cycle. If indirect addressing is employed, two cycles are required for the jump and three cycles for other memory reference instructions.

Augmented instructions do not require reference to memory. Since no address is required, bits 4 through 17 are decoded to initiate various operations to extend or augment the operation code. Because no storage or retrieval operations are performed, most augmented instructions can be completed in one computer cycle. Augmented instructions are divided into three classes:

1. Instructions having an operation code of 64_8 are EAE instructions.

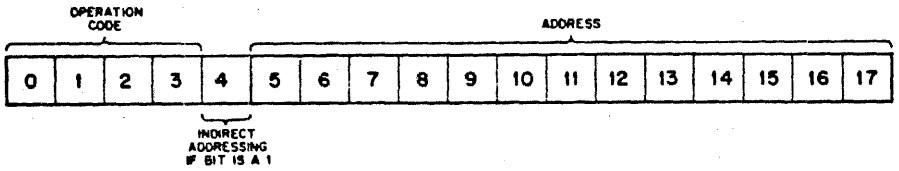
2. Instructions having an operation code of 70_8 are input/output transfer (IOT) commands, and are used to control or test the status of I/O devices, or to effect an information transfer.

3. Instructions having an operation code of 74_8 are operate (OPR) commands, and are used for basic processor data manipulation such as instruction skipping as a function of register condition, shifting, rotating, etc.

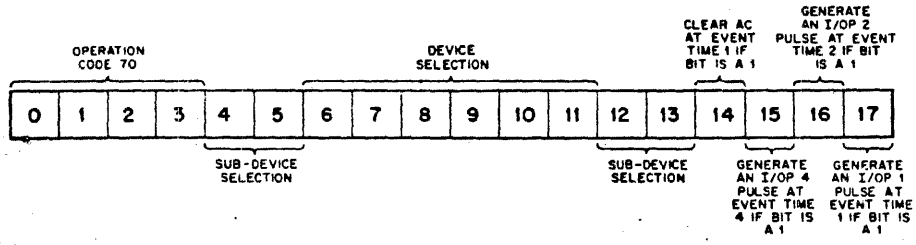
The formats of the various types of instruction words are illustrated in Figure 1-3. Appendix 1 contains a list of the instructions performed by the PDP-7.

Major Control States

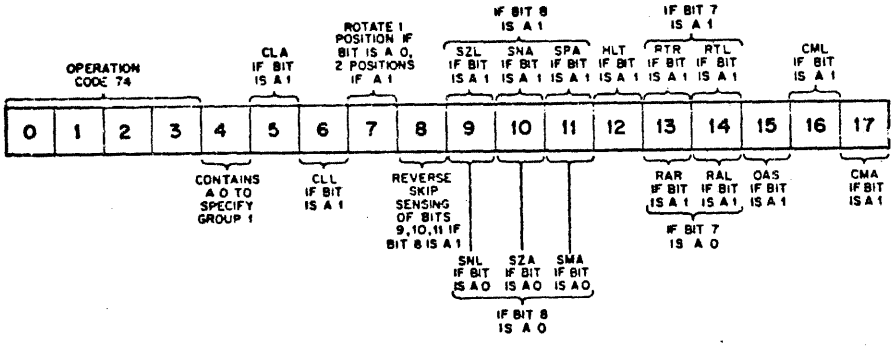
The computer operates in one of four major control states during each machine timing cycle. One or more states are entered to execute an instruction. The states are fetch, execute, defer, and break and are determined by the major state generator. Only one state exists at a time and all states, except break, are determined by the programmed instruction being executed.



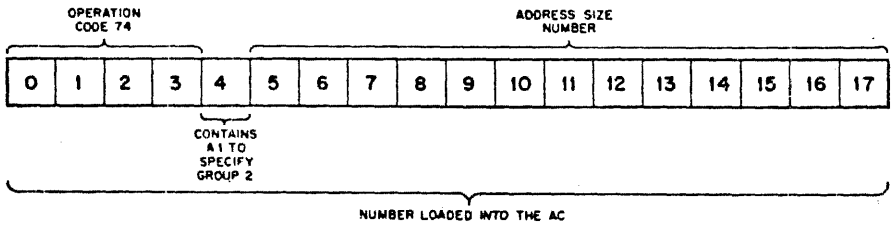
Memory Reference Instruction Bit Assignments



IOT Instruction Bit Assignments



Group 1 Operate Instruction Bit Assignments



Group 2 (LAW) Operate Instruction Bit Assignments

Figure 1-3 Instruction Word Format

Fetch (F)

A new instruction is obtained when this state is entered. The contents of the memory cell specified by the PC are placed in the MB, and the operation code (bits 0-3) of this instruction word is placed in the IR. The contents of the PC are then incremented by 1. If a single-cycle instruction is fetched, the operations specified are performed during the last part of the fetch cycle; then the next cycle is a fetch state for the next instruction. If a 2-cycle instruction is fetched, the succeeding control state is either defer or execute.

Defer (D)

When bit 4 of a memory reference instruction is a 1, the defer state is entered following the fetch state, to perform the indirect addressing. The memory location addressed by the instruction contains the address of the operand, and access to the operand is deferred to the next memory cycle (execute).

Execute (E)

This state is established only when a memory reference instruction is being executed. The contents of the memory cell addressed are brought into the MB, and the operation specified by the contents of the IR is performed.

Break (B)

When this state is established, the sequence of instructions is broken for a data interrupt or a program interrupt. In both cases, the break occurs only at the completion of the current instruction. The data break interrupt allows information to be transferred between core memory and an external device. When this transfer has been completed, the program sequence is resumed from the point of the break. The program interrupt causes the sequences to be altered. The contents of the PC and the contents of the link are stored in core memory location 0000, and the program continues from location 0001.

Timing

Seven times (designated T1 through T7) occur in sequence during each computer cycle. At each time, two pulses are generated, of which one is 40 nsec and the other is 70 nsec wide.

These time pulses cause gating circuits to perform sequential or synchronized logical or control operations. The narrow pulses are used for operations where timing is critical, such as the simultaneous sampling and incrementing of a register; the wider pulses are used to initiate gating operating where timing is less critical. The intervals between successive pairs of timing pulses permit gates and registers to settle before any new operation is initiated. During each computer cycle, memory reading occurs between times T2 and T3; memory writing starts at time T4 and occupies the remaining portion of the cycle.

PHYSICAL DESCRIPTION

The basic PDP-7 is housed in three standard DEC metal computer cabinets bolted together to form an intergrated console. In each cabinet, double doors at the front (held closed by magnetic latches) provide access to the wiring side of all module mounting panels. Double rear doors provide access to a plenum door on which the power supplies are mounted; the plenum door is latched by a spring-loaded pin at the top. Opening the plenum door permits access to the modules. A fan, mounted in the bottom of each cabinet, draws air through a dust filter to cool the modules. The airstream passes over the modules and is exhausted through louvered openings in the top of the cabinet, at the front. Four casters permit mobility of the computer.

Figure 1-4 shows the locations of components in the basic PDP-7. Note that the perforated tape reader and punch are mounted in the center bay above the operator console. The Teletype unit may be mounted on its own stand (supplied with the equipment) or may be placed on the console table. For additional physical data, refer to the table of physical data given below, and to the Installation section of this manual.

SPECIFICATIONS

Physical

Cabinet Height	69-1/8 inches
Cabinet Width	61-3/4 inches
Table Width	68-15/16 inches
Cabinet Depth	33-9/32 inches
Table Depth	19-7/8 inches

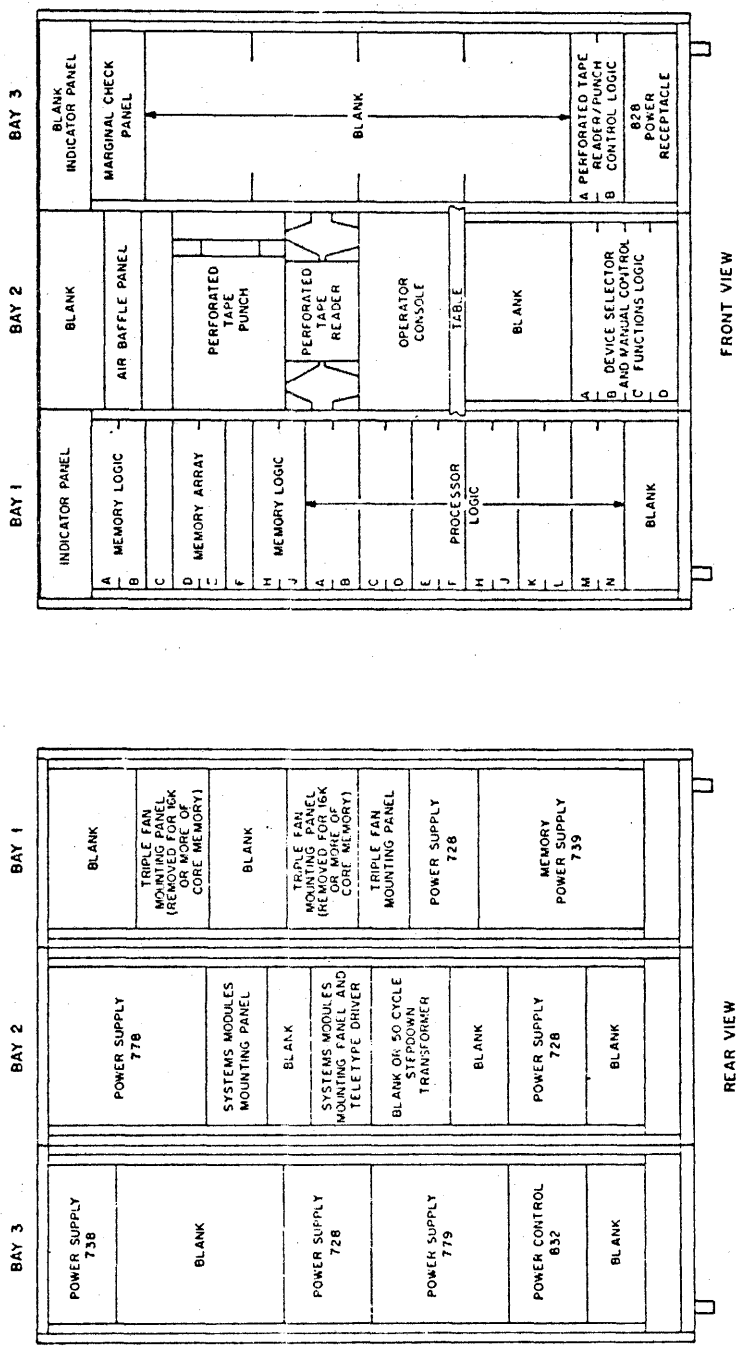


Figure 1-4 Basic PDP-7 Component Locations

Cabinet Door Clearance	14-7/8 inches at back
Cabinet Weight (3 cabinets)	1100 lbs
Teletype Height	8-3/8 inches
Teletype Width	18-5/8 inches
Teletype Depth	18-1/2 inches
Teletype Weight	40 lbs

Electrical

Power Requirements	115v, 60 cps, single phase, 17 amp for standard PDP-7 (can be constructed for 220v or 50 cps upon special request)
Power Dissipation	2200w
Digital Signal Levels	ground and −3v

Ambient Conditions

Operating Temperature	50 to 122° F
Operating Humidity	0 to 90% relative humidity
Storage Temperature	32 to 122° F
Storage Humidity	less than 90%
Heat Dissipation	7150 Btu/hr

Functional

Cycle Time	1.75 μsec
Word Length	18 bits
Core Memory Size	4096 or 8192 words, expandable to 32,768 in increments of 4096 words.
Instructions	16 basic instructions (13 memory reference and 3 augmented). The augmented instructions are microprogrammed to produce more than 175 commands.

Input/Output Capability	64 different devices can be individually selected and addressed by 3 command pulses.

PERTINENT DOCUMENTS

Publications

The following publications serve as source material and complement the information in this manual.

1. Digital FLIP CHIP Modules catalog, C-105, printed by DEC. This book presents information pertaining to the function and specifications of the FLIP CHIP modules and module accessories used in the PDP-7.

2. System Modules catalog, C-100, printed by DEC. This book presents information pertaining to the function and specifications of the basic system modules and module accessories used in the PDP-7.

3. Programmed Data Processor-7 Users Handbook, F75, printed by DEC. Programming, instruction format, and general computer function are presented in this document.

4. PDP-7 Software Package. Perforated program tapes and descriptive matter for the Program Assembly Language (PAL), utility subroutines, and the maintenance programs (Maindec) are contained in this package prepared by DEC. The content of the package is listed in Table 1-1.

5. Instruction manuals and Maindec programs for appropriate input/output devices are prepared by DEC.

6. Technical Manual, Keyboard Send and Receive Sets (KSR), Bulletin 273B (Vols. 1 and 2). This manual covers operation and maintenance of the Teletype unit.

7. Parts, Model 33 Page Printer Set, Bulletin 1184B. This illustrated parts breakdown can be used as a guide to disassembly, reassembly, and ordering parts of the Teletype unit.

8. Technical Manual, High-Speed Tape Punch Set (BRPE), Bulletin 215B. This manual covers operation and maintenance of the tape punch unit.

9. Parts, High-Speed Punch Tape Set (BRPE), Bulletin 1154B. This illustrated parts breakdown can be used as a guide to disassembly, reassembly, and ordering parts of the tape punch unit.

10. Digitronics Perforated Tape Reader Model 2500 manual. This book covers the installation, use, theory of operation, and maintenance of the tape reader unit.

TABLE 1-1 PROGRAM LIBRARY

Number	Name	Number	Name
Digital-7-1-S	Symbolic Tape Editor	Digital-7-23-10	Buffered Input/ Output Package
Digital-7-2-S	FORTRAN II System - 8K	Digital-7-24-10	Pen Follow Subroutine
Digital-7-3-S	Assembler - Basic and Extended	Digital-7-25-10	Character Display Subroutine
Digital-7-4-S	DDT (Debugging Tape)	Digital-7-30-A	Floating Point Package
Digital-7-10-0	Teletype Output Package	Digital-7-31-A	Multiply Subroutine
Digital-7-11-10	Tic Toc	Digital-7-32-A	Divide Subroutine
Digital-7-12-1	F F Loader	Digital-7-33-A	Double Precision Integer Package
Digital-7-13-1	Readin Mode Loader	Digital-7-34-A	Unsigned Multiply Subroutine
Digital-7-14-0	Octal Print Subroutine	Digital-7-35-A	Unsigned Divide Subroutine
Digital-7-15-0	Decimal Integer Print	Digital-7-40-U	Master Tape Duplicator
Digital-7-20-10	PDP-7 DECtog		
Digital-7-21-10	PDP-7 DECtrieve		
Digital-7-22-10	PDP-7 DECtape Subroutine		

TABLE 1-1 PROGRAM LIBRARY (continued)

Number	Name	Number	Name
Digital-7-41-U	Tape Reproducer	Digital-7-53-M	Reader and Punch Test
Digital-7-43-U	CAL Handler Type I	Digital-7-54-M	Maindec 401 (Instruction Test)
Digital-7-44-U	CAL Handler Type III	Digital-7-55-M	Maindec 402 (Checkerboard)
Digital-7-45-M	Type 57A Compiler	Digital-7-56-M	Maindec 403 (Address Test)
Digital-7-50-M	Teleprinter Input/ Output Test	Digital-7-57-M	Maindec 410 (RPB Test)
Digital-7-51-M	Clock Interrupt Test Program		
Digital-7-52-M	CONTEST II		

One copy each of publications 3 through 10 is supplied with each PDP-7 system. Copies of items 1 or 2 or additional copies of items 3 through 10 can be obtained from the nearest DEC district office or from:

Field Service Department
Digital Equipment Corporation
146 Main Street
Maynard, Massachusetts 01754
U.S.A.

Additional copies of items 6 through 9 can be procured from:

Teletype Corporation
5555 Touhy Avenue
Skokie, Illinois 60076
U.S.A.

Drawings

The engineering drawings listed in the table of contents are reproduced in Section 11 as an aid to understanding and maintaining the PDP-7. All the logic diagrams are included, but schematics are given only for those modules not described in the DEC System or FLIP CHIP

Module Catalogs. A complete set of formal engineering drawings and module schematics is supplied separately with each PDP-7 system. Should any discrepancy exist between the drawings in this manual and those supplied with the equipment, assume the formal drawings to be correct.

ABBREVIATIONS

Listed below are the most commonly used abbreviations of registers, key operations, components, instructions, and signal names. Instruction mnemonics not included in this list will be found in Appendix 1, Instruction Summary. Signal names not included in this list will be found in Appendix 3, Signal Glossary. This appendix contains an alphanumerical list of all signal names which appear on the engineering drawings, together with the number of the drawing on which each signal is generated.

AC	Accumulator
ACS	Accumulator Switches
ADDR	Address
API	Automatic Priority Interrupt
AS	Address Switches
B	Break (state)
BD	Bus Driver
BGN	Begin
BK RQ	Break Request
C	Complement
CAL	Call Subroutine
CHAN REQ	Channel Request
CHAR	Character
CLA	Clear Accumulator
CLK	Clock
CLR	Clear
CONT	Continue
CP	Central Processor
CRY	Carry
CY or CYC	Cycle
D	Defer (state)
DA	Data Address
DAC	Deposit Accumulator Contents
DCD	Diode-Capacitor-Diode Gate
DI	Data Information
DIV	Divide
DLY	Delay
DP	Deposit
DS	Device Selector
DPN	Deposit Next
E	Execute (state)
EAE	Extended Arithmetic Element
EMA	Extended Memory Address Register
EMB	Extended Memory Buffer Register

EN or ENB	Enable
EPC	Extended Program Counter
EX	Examine
EXN	Examine Next
F	Fetch (state)
FLG	Flag
HLT	Halt
IC	Information Collector
ID	Information Distributor
INH	Inhibit
INT RQ	Interrupt Request
INVTD	Inverted
I/OP	Input/Output Pulse
IOT	Input/Output (information) Transfer
IR	Instruction Register
ISZ	Index and Skip if Zero (instruction)
JMP	Jump (instruction)
JMS	Jump to Subroutine (instruction)
KBD	Keyboard
L	Link
LAC	Load Accumulator
LUI	Line Unit In (Teletype keyboard buffer)
LUO	Line Unit Out (Teletype printer buffer)
MA	Memory Address Register
MB	Memory Buffer Register
MQ	Multiplier Quotient Register
MS	Major States
MUL	Multiply
OP	Output
OPR	Operate (class of instruction)
OV	Overflow
PA	Pulse Amplifier
PB	Punch Buffer Register
PC	Program Counter
PI	Program Interrupt
PIC	Program Interrupt Control
PIE	Program Interrupt Enable
POV	Possible Overflow
PROG	Program
PUN	Punch (tape)
PWR CLK	Power Clock
PWR CLR	Power Clear
RB	Reader Buffer Register
RD FLG	Reader Flag
RDR	Reader
RPT	Read Paper Tape
RQ	Request
RTN	Return
SA	Sense Amplifier
SAD	Skip if Accumulator Differs
SEL	Select
SKP	Skip
SP	Special Pulse
STB	Strobe
SW	Switch
SYNC	Synchronize
TAD	Two's Complement Add
T	Timing Pulse (70-nsec)
TP	Timing Pulse (40-nsec)

XCT	Execute (instruction)
XOR	Exclusive OR

SYMBOLS AND TERMINOLOGY

Digital Logical Symbols

A complete list of the digital logic symbols used in the engineering drawings of this manual can be found in Appendix 1.

Conventions and Notations

Conventions and notations on engineering drawings and in text describing the PDP-7 are used as follows:

V	Programming notation for the inclusive OR function.
$\forall$	Programming notation for the exclusive OR function.
$\wedge$	Programming notation for the AND function.
$\Rightarrow$	Programming notation for an information transfer.
+	Design notation for the inclusive OR function and program notation for addition.
.	Design notation for the AND function.
$\longrightarrow$	Design notation for an information transfer accomplished by a single signal (used without parentheses).
( )	The contents of a storage device.
C(A) V C(B) $\Rightarrow$ C(A) or A V B $\Rightarrow$ A	The contents of register B are OR combined with the contents of register A and the result is stored in register A.
A2(1) or A_2^1	Bit 2 of register A is the state corresponding to a binary 1, or contains a 1.
+1 $\longrightarrow$ A	The contents of register A are incremented by 1.
0 $\longrightarrow$ A	Register A is cleared or set to contain all 0's.
A $\dashrightarrow$ B	The contents of register A are jam transferred into register B.

Other terms used in this manual are defined as follows:

absolute address - a number used directly to specify any memory location. Twelve bits are required to address 4K, 13 bits to address 8K, 14 bits to address 16K, and 15 bits to address 32K.

address of the operand - the location of a core memory register currently containing the operand.

clear - to clear a register is to establish the state corresponding to binary 0 in all bits of that register.

clock break - an interruption of the main program, lasting one computer cycle. During this cycle, a real time clock increments the contents of memory location 7_8 by 1. When the clock is enabled by a programmed instruction, a clock break occurs every 1/60 sec. If memory location 7_8 overflows, the clock flag is set and may cause a program break.

command - a signal that causes a specific operation to occur as the complete or partial execution of an instruction or microinstruction.

cycle stealing - a suspension of the main program for one computer cycle caused by the clock break or data break facilities to effect an operation or transfer information with core memory.

data break - an interruption of the main program lasting one computer cycle. During this cycle an information transfer takes place between core memory and a high-speed I/O device. The data break is requested by the I/O device when it is ready for the transfer, and the break occurs as soon as the processor reaches an "instruction done" situation.

effective address - the address of the operand as specified by an instruction word or by an absolute address.

flag - a flip-flop or signal that indicates a specific equipment status or condition. Flag signals are used to identify an I/O device which requires servicing, as well as for other purposes.

instruction - an 18-bit word which is stored in memory and is identified by a distinct operation code in the four most significant bits. When retrieved from memory, an instruction word causes specific operations to be performed by the processor.

microinstruction - a command to perform a specific operation, identified by the placement of 1's and 0's in bits of an instruction word other than those which contain the operation code. Several microinstructions can be combined within a single instruction word. In effect, the entire word is used as an operation code, and is decoded by gating circuits within the processor to produce multiple command pulses.

operand - a stored binary number to be operated upon.

program interrupt - an interruption of the main program initiated by peripheral equipment which requires servicing. When the processor reaches an "instruction done" situation, control of the processor is transferred to a subroutine which identifies the interrupting device. The transfer of control takes place during the break cycle. After the interrupting device has been identified, a further subroutine services it and then transfers control of the processor back to the main program.

set - to set a flip-flop is to establish the state corresponging to binary 1.

subroutine - a series of stored instructions which is not part of the main program but may be reached by means of a JMS instruction. A subroutine may contain instructions that service peripheral equipment, or instructions for an operation that must be repeated many times. At the conclusion of a subroutine, control of the processor may be returned to the main program.

CHAPTER 2

LOGIC FUNCTIONS

Both manual and programmed operation of the PDP-7 are required for the performance of any complete task. Manual operation is normally limited to the following: storing a brief loader program; modifying or examining data or addresses in a program that is already stored; or establishing the starting conditions for programmed operation. In programmed operation, data and the sequence of instructions which constitutes the program are loaded into the core memory; the starting address of the program is manually established; and the computer is manually started. The computer then successively executes the instructions specified by the program. For maintenance purposes and to facilitate debugging, provision is made for advancing the program one cycle at a time or one instruction at a time.

This chapter describes the sequence of events that takes place during each of the manual operations or instructions that the PDP-7 can perform. Reference is made throughout the descriptions to the flow diagrams.

FLOW DIAGRAM INTERPRETATION

Two flow diagrams are provided: one, contained in engineering drawing 20, shows the events that take place during each of the possible manual operations; the other, contained in engineering drawing 21, shows the events that take place during the execution of programmed instructions. The two flow diagrams are similar in their arrangement. At the extreme left are shown the timing pulses which initiate events at various times in the cycle. In the flow diagram of manual operations, these timing pulses are designated KEY MANUAL and SP0 through SP4. In the flow diagram of programmed operations, the timing pulses are designated T1 through T7. Times (in μsec or nsec) appearing in boxes that straddle the horizontal boundary line separating two timing pulses represent the time interval that elapses between the occurrence of those two pulses.

Events initiated by a specific timing pulse are shown in rectangular boxes placed between the boundary lines associated with that pulse. It is important to note that all such events are

initiated simultaneously by the timing pulse if they form part of the event sequence. For example, in following the deposit (DP) sequence on engineering drawing 20, at time SP2 the event AS1 → PC is followed in the sequence by DAC → IR and ACS1 → AC. The vertical separation does not imply that the AS1 → PC operation precedes the other two; on the contrary, they are all initiated simultaneously. The vertical separation merely facilitates the illustration of branches to other possible sequences.

Events in a sequence which is not specifically designated by a key name or instruction name are assumed to be common to all sequences (e.g., 0 → MA at time SP1, engineering drawing 20). Where a common sequence branches into two or more sequences, depending on the operation in progress, the operation associated with a given sequence is identified immediately below the branch. For example, at time SP2 the event AS1 → PC occurs in a sequence common to both examine (EX) and deposit (DP) operations. The sequence then branches; if an examine operation is in progress, pulse SP2 initiates the event LAC → IR, but if a deposit operation is in progress LAC → IR does not occur; instead, pulse SP2 initiates events DAC → IR and ACS1 → IR. Similarly, several separate sequences may be followed by a common sequence. Thus, on engineering drawing 20, each of the separate sequences associated with the START, CONTINUE, EXAMINE, and DEPOSIT operations is followed by the event 1 → TP1 which takes place at time SP4.

Note that some of the events specified in the rectangles of the flow diagram are unconditional; that is, they invariably occur at the specified time when the operation with which they are associated is in progress. Thus, when the START key is pressed, the event AS1 → PC always takes place at time SP2. Other events are conditional upon the state of control flip-flops or register bits. Conditional events are represented in the rectangles by a statement of the required condition which is separated from the conditional event by a colon. Thus, at time SP2 of a read-in operation (engineering drawing 20), the statements in the rectangle indicate that if the read paper tape (RPT) flip-flop is in the 0 state, the contents of the address switch register are transferred to the PC (RPT (0): AS1 → PC). However, if the RPT flip-flop is in the 1 state, 1 is added to the contents of the PC and the operation code DAC (deposit content of accumulator in specified memory cell) is set into the instruction register (RPT (1): + 1 → PC DAC → IR).

On engineering drawing 21, the seven time pulses that occur during each computer cycle are shown at the left. The column immediately to the right contains the events associated with

memory which occur during every computer cycle, regardless of the major control state established. Certain conditional events, whose occurrence is dependent on factors other than the major state, are also contained in this column designated Events Common. The other events on this drawing are grouped according to the major state established. Each major state (fetch, defer, execute, and break) lasts for one computer cycle. All programmed instructions start in the fetch state.

The exact mechanism by which the CP performs a function specified by an event shown on the flow diagram is found by referring to the appropriate engineering logic diagram and the corresponding circuit description. When tracing a transfer function, it is best to begin by examining the input and control gating of the register to which the transfer is being made. Thus, to trace the function AS1→ PC, first examine the logic diagram of the PC; it will be found that a set of input gates is triggered by a pulse designated AS1→ PC. To find out how this pulse is generated, examine the logic drawing of the PC control. When there is doubt where a pulse or level is generated, consult Appendix 3. This appendix lists all command pulses and control levels in alphanumerical order of their designations, together with the number of the engineering logic diagram on which are shown the circuits which generate any given signal.

> NOTE: It is very important that maintenance personnel familiarize themselves as soon as possible with the flow diagrams of manual operations, CP operations, and EAE operations. These flow diagrams hold the key to an understanding of system operation and provide much information that is valuable when troubleshooting.

PRELIMINARY OPERATIONS

Circuit protection and primary control of all power entering the computer is governed by the circuit breaker mounted on the 2-step power control unit located at the rear of the cabinet. Manual control of primary power is governed by the lock switch and POWER switch located on the console panel. With the lock switch in the unlocked position, turning on the POWER switch energizes a relay in the power control unit, which, in turn, energizes the computer logic power supply immediately. A second relay in the power control unit imposes a delay of 5 sec before the memory power supply is energized. This delay ensures that all ac transients in the computer have completely decayed before the memory is energized. Similarly, when

the POWER switch is turned off, the memory power supplies are deenergized immediately; and the computer logic power is maintained for 5 sec longer. In each case, the delay ensures that switching transients cannot cause current surges which would destroy information stored in the core memory.

During the 5-sec turnon delay period, an integrating circuit enables a variable clock. While the clock is enabled, it emits standard negative pulses at a repetition rate of 200 kc. These PWR CLK (power clock) pulses repeatedly clear the RUN and memory control flip-flops and trigger two NAND gates, which are enabled by the 0 condition of the RUN flip-flop. The output pulses from the gates trigger two pulse amplifiers, which produce the PWR CLR NEG (power clear negative) and PWR CLR POS (power clear positive) pulses. These PWR CLR pulses are supplied to the interface to establish initial conditions in peripheral equipment. Thus, if any flip-flops are set by switching transients during the first 5 sec after power turnon, they are immediately cleared by the PWR CLK or PWR CLR pulses. This establishes correct initial conditions and ensures that a stored program cannot be accidentally started or disturbed.

The lock switch, in its unlocked position, connects all the console keys and switches to the −15v supply, thereby permitting them to generate the levels required to start the computer and to perform manual operations. When a program has been started manually, the lock switch may be turned to its locked position. This grounds all the console keys and switches to prevent manual interference with the program. A second deck of the lock switch bypasses the POWER switch, so that power cannot be accidentally turned off while a program is running.

MANUAL OPERATIONS

Keys and switches on the operator console have three functions: they permit information to be stored in core memory; they permit the contents of a specified core memory cell to be displayed for visual examination; and they permit the execution of a program to be started and stopped.

Operation of the START, CONTINUE, EXAMINE/EXAMINE NEXT, DEPOSIT/DEPOSIT NEXT, or READ-IN keys generates the KEY MANUAL level transition to start the special pulse generator. The special pulse generator produces five timing pulses, designated SP0 through SP4, which initiate all functions performed as part of a manual operation. All five keys cause the RUN flip-flop to be cleared at time SP0 in order to stop any operations already in progress.

(Note that although it is not logical to press the START key when a program is running, it could be accidentally pressed and must therefore be made to stop current operations.) After the clearing of the RUN flip-flop, there is a 10-μsec pause to allow the completion of any EAE operations in progress. Thereafter, the sequence of operations depends upon which key was operated.

START Key

The START key initiates execution of a program which has been loaded into memory. After starting the special pulse generator and clearing the RUN flip-flop, the key causes the following events to take place:

1. At time SP1, the memory address register (MA) is cleared in preparation for entering the starting address of the program from the ADDRESS switches. A complete clear is required, because only binary 1's are transferred to the MA.

2. At time SP1, a BGN pulse is generated which clears the instruction register (IR), the read paper tape (RPT) and other special mode flip-flops, and establishes initial conditions in the registers of I/O devices. The multi-state device of the major state generator is forced into the fetch state in preparation for extracting the first programmed instruction from memory, and the program counter (PC) is cleared.

3. At time SP2, binary 1's of the starting address preset on the ADDRESS switches are transferred into the PC.

4. At time SP3, the RUN flip-flop is set to the 1 state, thereby conditioning a NAND gate between the special pulse generator and the main timing chain. Timing pulse SP4 triggers this gate and causes the main timing chain to generate timing pulse T1. Thereafter, the CP operates under control of timing pulses generated by the main timing chain and successively executes programmed instructions until the RUN flip-flop is set to the 0 state.

CONTINUE Key

The CONTINUE key causes the CP to continue execution of a program after a temporary halt. Pressing the key clears the RUN flip-flop during SP0 and the MA during SP1. Since a halt may take place at the end of any memory cycle, the CP must continue with the type of cycle that was predetermined by the cycle in which the halt was requested. Thus, the only further action required by the CONTINUE key is to set the RUN flip-flop to 1 at time SP3 and to cause timing pulse SP4 to initiate operation of the main timing chain. The CP then continues execution of the program from the point at which it was halted.

STOP Key

The STOP key provides a means of halting a program at the conclusion of a memory cycle. Pressing the key conditions a gate which is triggered at time T5 of the memory cycle. The output pulse produced by the gate clears the RUN flip-flop, thereby preventing timing pulse TP7 from re-entering the timing chain to initiate a new cycle. The CP, therefore, halts at the conclusion of the memory cycle during which the RUN flip-flop was cleared.

DEPOSIT/DEPOSIT NEXT Key

The DEPOSIT/DEPOSIT NEXT key, when momentarily set to DEPOSIT, causes a binary number that has been preset on the ACCUMULATOR switches to be deposited in the memory cell specified by the ADDRESS switches. When momentarily set to DEPOSIT NEXT, the key causes a binary number preset on the ACCUMULATOR switches to be deposited in the memory cell specified by the PC. Setting the key to DEPOSIT clears the RUN flip-flop at time SP0 and the MA at time SP1. A memory cycle which will perform the operation is then initiated as follows:

1. At time SP1, a BGN pulse is generated to clear special mode and I/O device flip-flops; the PC is cleared; and the major state generator is forced to the execute state. (Refer to the key function flow diagram on engineering logic diagram 20.)

2. At time SP2, the binary 1's contained in the ADDRESS switches are transferred to the PC. Then the binary 1's contained in the ACCUMULATOR switches are transferred to the accumulator register (AC), and the operation code for DAC (deposit AC) is set into the IR.

3. At time SP3, the contents of the PC are transferred into the MB. This step is necessary because after time SP4, the processor will enter an execute cycle in which the contents of the MB are transferred to the MA at time T1. The fact that the status of the link, trap flag, and extend mode are also set into the MB is of no importance in a deposit operation, because those bits of the MB are not sampled by the MA.

4. At time SP4, the contents of the PC are incremented by 1 to facilitate a further manual operation at the next location after completing the deposit operation. Timing pulse SP4 then starts the main timing chain. Note, however, that the RUN flip-flop remains in the 0 state, and that in consequence, the CP will halt at the end of the execute cycle.

5. At time T1 of the execute cycle, since this is not a CAL (call subroutine) instruction, the contents of the MB are transferred to the MA (CP flow diagram, engineering logic diagram 20).

6. At time T3 of the execute cycle, the contents of the AC are transferred to the MB; and during the remaining portion of the cycle, this data is written into the specified memory cell. Since the RUN flip-flop is not set, the CP halts after time T7, and the deposit operation is complete.

Setting the key to DEPOSIT NEXT causes the CP to perform an operation that is almost identical to a deposit operation. The difference is that the PC is not cleared at SP1, nor are the contents of the ADDRESS switches set into the PC at time SP2. The number preset on the ACCUMULATOR switches is therefore deposited in the memory cell specified by the PC instead of by the ADDRESS switches. Note that the contents of the PC are incremented at time SP4. Therefore, after an initial deposit operation, use of the DEPOSIT NEXT position causes deposits to be made at consecutive memory locations without resetting the ADDRESS switches.

EXAMINE/EXAMINE NEXT Key

The EXAMINE/EXAMINE NEXT key, when momentarily set to EXAMINE, causes the contents of the memory cell specified by the ADDRESS switches to be transferred to the MB and AC.

When the transfer is complete, the contents of the MB, MA, and AC may be visually checked by means of the associated indicator lamps.

The MB and AC contain the contents of the specified memory cell; the MA contains the address preset on the ADDRESS switches; and the PC contains the address of the next consecutive memory cell. Thus, a number of consecutive memory cells may be examined without resetting the ADDRESS switches between each operation. When momentarily set to EXAMINE NEXT, the key causes the contents of the memory cell specified by the PC to be transferred to the AC for visual examination.

Setting the key to EXAMINE clears the RUN flip-flop during time state SP0 and the MA at time SP1. A memory cycle which will perform the operation is then initiated as follows:

1. At time SP1, a BGN pulse is generated to clear special mode and I/O device flip-flops; the PC is cleared; and the major state generator is forced to the execute state. (Refer to the key function flow diagram on engineering logic diagram 20.)

2. At time SP2, the address specified by the ADDRESS switches is transferred to the PC, and the operation code for LAC (load AC) is set into the IR.

3. At time SP3, the contents of the PC are transferred to the MB. (This step is necessary for the reason stated under DEPOSIT/DEPOSIT NEXT Key, No. 3.)

4. During time state SP4, the contents of the PC are incremented by 1, and timing pulse SP4 starts the main timing chain.

5. At time T1 of the execute cycle, since the instruction is not CAL, the address contained in the MB is transferred to the MA, and the AC is cleared.

6. At time T3, the contents of the addressed memory cell are read into the MB, and an XOR (exclusive OR) operation is performed on the MB and AC. Since the AC was previously cleared, this results in a direct transfer of the contents of the MB into the AC, where they are available for visual examination. Since the RUN flip-flop is not set, the CP halts at time T7, and the EXAMINE operation is complete.

Setting the key to EXAMINE NEXT causes the CP to perform an operation which is almost identical to an EXAMINE operation. The difference is that the PC is not cleared at time SP1, nor are the contents of the ADDRESS switches set into the PC at time SP2. The word loaded into the AC for examination is therefore brought from the cell specified by the PC instead of by the ADDRESS switches. Note that the contents of the PC are incremented at time SP4 to permit examination of consecutive locations without resetting the ADDRESS switches.

REPEAT Switch

Turning on the REPEAT switch causes the CP to repeat the operation specified by one of the manual keys, at intervals determined by the setting of the SPEED controls on the console panel, for as long as the key is held down. After completing a DEPOSIT or EXAMINE operation, use of the REPEAT switch in conjunction with a DEPOSIT NEXT or EXAMINE NEXT operation permits deposition in, or examination of, successive memory cells without specifying each address.

Turning on the REPEAT switch causes timing pulse SP4 to trigger a one-shot which produces a delay. The length of the delay is adjustable by means of the coarse and fine SPEED controls on the operator console. When the one-shot reverts to its stable state, the level transition that appears at the output terminal is applied to the special pulse generator and initiates time state SP0 once more. The CP then repeats the operation associated with the manual key that is pressed.

READ-IN Key

The READ-IN key permits information punched in binary format on paper tape to be loaded into memory at successive memory locations, starting at the address specified by the ADDRESS switches. When in the binary mode, tape holes 1 through 6 of each line of tape contain one-third of an 18-bit word; hole 7 is not punched until the last line of the last character that is to be read, and hole 8 is always punched to cause the line to be read. When the READ-IN key is pressed, the processor selects the reader in binary mode, then waits for the reader to read three lines of tape and assemble these in the reader buffer in the form of an 18-bit word (and also waits until the READ-IN key is released). When the reader buffer is full, its contents are transferred to the AC and then deposited in memory. The process of reading three lines of tape, assembling the information into an 18-bit word, and depositing words at consecutive

memory locations continues until the reader encounters a line of tape in which hole 7 is punched. The reader then stops and the processor executes the last 18-bit word read and deposited (the hole 7 being in the last line of this word).

Pressing the READ-IN key causes the RUN flip-flop to be cleared at time SP0 and the MA to be cleared at time SP1. The following sequence of events then takes place:

1. At time SP1, a BGN pulse clears the special mode flip-flops, including the RPT (read paper tape) flip-flop to establish initial conditions. The PC is cleared, and the major state generator is forced to the execute state.

2. At time SP2, the address specified by the ADDRESS switches is set into the PC, and the operation code for DAC is set into the IR.

3. At time SP3, the RPT flip-flop is set to 1.

4. At time SP4, the AC is cleared and the contents of the PC are transferred to the MB. At this time a command is generated that selects the reader in binary mode and causes it to read three lines of tape successively into the reader buffer. When the reader buffer is full, the reader flag is set to 1.

5. The processor now waits for three conditions to be fulfilled:

   a. The RPT flip-flop is in the 1 state (this condition was fulfilled at time SP3).

   b. The reader flag is set to 1 (indicating that the reader buffer is full).

   c. The READ-IN key is released. If the processor were not forced to wait for this condition to be fulfilled, the rapid action of the reader might cause several words to be deposited at the starting address, with consequent loss or invalidation of information.

The levels representing assertion of these three conditions are combined in

a gate; whichever of the three conditions is fulfilled last causes a level transition to occur at the output of the gate. This transition starts the main timing chain and initiates a computer cycle in the execute state.

6. The events in the execute cycle follow the pattern already described for a deposit operation. However, the CP does not stop at time T7 because timing pulse TP7, combined with the 1 state of the RPT flip-flop, causes the generation of timing pulse SP0 of a second readin operation. However, the RUN flip-flop is cleared at time SP0.

7. At time SP1 of a second (or subsequent) readin operation, no BGN pulse is generated, because the READ-IN key has been released. Further, since the RPT flip-flop remains set, the PC is not cleared at time SP1 and the contents of the ADDRESS switches are not transferred to the PC at time SP2. Instead, the contents of the PC are incremented by 1 at time SP2. Thus, 18-bit words transferred from the reader buffer to the AC are deposited at consecutive memory locations.

8. When the reader encounters a line of tape which has hole 7 punched, the assertion level produced by hole 7 causes the RPT flip-flop to be cleared and the RUN flip-flop to be set at time T5.

9. At time T7, since the computer is in the execute state and the RUN flip-flop is set, timing pulse TP7 forces the major state generator to the fetch state and restarts the main timing chain. At time T1 of the ensuing fetch cycle, the contents of the PC are transferred to the MA. Therefore, since at that time the PC contained the memory address of the last word read from paper tape, the processor executes that word. The word may be any instruction, but sensible choices for the programmer would be either a HLT (halt) instruction to allow manual control of the program before starting or a JMP (jump) instruction that would provide entry to the start of the program.

SINGLE INSTRUCTION Switch

The SINGLE INSTRUCTION switch, in combination with an F SET level ("instruction done" situation), generates a RUN STOP signal that resets the RUN flip-flop and halts the CP at the end of the current memory cycle. However, the F SET ("instruction done") level is generated only during the cycle that completes the execution of an instruction and does not appear during a fetch or defer cycle which must be followed by an execute cycle. Thus, when the SINGLE INSTRUCTION switch is turned on, the CP halts after completing each instruction; and the next instruction must be initiated by pressing the CONTINUE key. When the SINGLE STEP and SINGLE INSTRUCTION switches are both turned on, the SINGLE STEP switch takes precedence; and the CP halts after each memory cycle.

PROGRAMMED OPERATIONS

The normal mode of PDP-7 operation is the execution of programmed instructions. Programmed operation can be modified by a program interrupt (produced by peripheral equipment to transfer control of the CP from the main program to a subroutine). The main program can also be temporarily interrupted by means of a data break or a clock break. During a data break, lasting one memory cycle, a high-speed peripheral device, which has a 15-bit address register as well as an 18-bit data register, can transfer information to or from memory. During a clock break, also lasting one memory cycle, a real-time clock may add 1 to the contents of memory location 7. If an overflow occurs, a program break is initiated; otherwise, the main program is resumed.

When a program is to be executed, the starting address of the program is preset on the ADDRESS switches, and the START key is momentarily pressed. The CP thereupon fetches the first instruction from the specified address and executes it, at the same time adding 1 to the contents of the PC. Succeeding instructions are obtained from numerically consecutive memory locations, unless a JMP or JMS instruction changes the contents of the PC so that instructions are obtained from another block of numerically consecutive locations in a different section of memory.

Programming is simplified and memory space is conserved if the programmer arranges the instructions for some operation that must be performed many times during the course of the program in the form of a subroutine. A subroutine is a group of instructions contained in a numerically

consecutive block of memory locations that do not form part of the main program sequence. These subroutines may be entered from any part of the main program by means of a JMS (jump to subroutine) instruction which stores in memory the location of the next main program instruction (that is, the contents of the PC). The next instruction to be executed is the first instruction of the subroutine. Exit from the subroutine and return to the main program sequence is obtained by means of a JMP I (jump indirect) instruction, which directs the CP to the location containing the next main program instruction and causes the instruction found in that location to be executed.

Instructions

The following explanations of the functions performed during the execution of each instruction assume that the PDP-7 is energized and is operating normally and that the address of the next instruction to be performed is held in the PC. Therefore, each instruction explanation begins at the start of the fetch cycle.

The instructions performed by the PDP-7 are of two kinds: memory reference instructions and augmented instructions. A memory reference instruction contains an operation code in bits 0 through 3, and the location in memory of the word upon which the operation is to be performed in bits 5 through 17. If bit 4 is a 1, it is an indication that the address contained in the instruction word is not that of the operand itself, but is the location containing the address of the operand. This facility is known as indirect addressing. Indirect addressing has many uses; for example, it may be used with a jump instruction to permit re-entry into the main program from a subroutine; it permits a memory location outside the current 8K field to be addressed when the extend mode is enabled; and it permits a programmer to gain access to an operand whose absolute address is determined by the program itself but is known to be contained in a specific memory location.

An augmented instruction requires no reference to memory. An operation code in bits 0 through 3 identifies the instruction as an OPR/LAW, IOT, or EAE instruction. The contents of the remaining bits specify operations to be performed by timing pulses T5, T6, and T7 during a single computer cycle. More than one such microinstruction may be combined into a single instruction provided that there is no logical conflict between the operations specified.

The following paragraphs describe the memory reference instructions first and then the augmented instructions. The load accumulator (LAC) and operate (OPR) instructions are described in detail, as representative of the memory reference instructions and augmented instructions, respectively. Remarks on the remaining instructions are confined to important points that may not be obvious from the flow diagram. All of the explanations assume that direct addressing is employed (bit 3 contains a 0). An explanation of the use of the auto-indexing locations and of the use of a defer cycle to permit indirect addressing follows the descriptions of the memory reference instructions. The descriptions of both memory reference and augmented instructions also assume that no I/O device has requested a break of any kind. The conditions under which a break may be granted and the events that take place during the ensuing break cycle are described after the explanation of the augmented instructions.

Memory Reference Instructions

Load Accumulator (LAC) - The LAC instruction is a memory reference instruction which requires a fetch cycle and an execute cycle. During the fetch cycle, the address of the LAC instruction is transferred from the PC to the MA, and the contents of the PC are incremented by 1. A read operation transfers the contents of the memory cell addressed into the MB and bits 0 through 3 are transferred directly into the IR as the operation code of the instruction to be executed. The contents of the MB are then rewritten into the memory cell from which they were read. Finally, the major state generator is set to the execute state. During the execute cycle, the operand is extracted from memory and loaded into the accumulator. The following detailed description of the sequence should be read while referring to the flow diagram and to the specified engineering logic diagrams.

At time T1 of any fetch cycle, the instruction register must be cleared. The F level is NAND combined with the T1 pulse (B5, 24); and the gate output, after amplification and inversion, is applied to the direct clear inputs of the four IR flip-flops. (In a similar manner, the IR is cleared at time T1 of a break cycle and at time T2 of certain execute cycles. The IR is not cleared during a defer cycle.) Also at time T1, the F negative level is NAND combined with the T1 pulse (A7, 25) to produce a PC1→ MA pulse. This pulse is applied to a set of MA input gates (29) and opens those which are already conditioned by a negative level from a PC flip-flop in the 1 state.

Note that the PC1→MA pulse is applied only to bits 5 through 17 of the MA register. Bits 3 and 4 of this register are used only in conjunction with memories of 16K capacity or more and must receive a separate transfer pulse (EPC1→ EMA) from the memory extension control unit. The F level and T1 pulse are also NAND combined in the PC control logic (C6, 25) to produce a +1→ PC pulse which increments the contents of the PC by 1. The +1→ PC pulse complements bit 17 of the PC register (D8, 29), and is also applied to a gated pulse amplifier. If this gate was already conditioned by a PC17 (1) level, a carry pulse complements bit 16. The carry is propagated toward bit 5 by a series of gated pulse amplifiers and stops when it first encounters a bit in the 0 state. The flip-flops have a controlled internal delay so timed that the MA input gates open and close before the incrementing pulse causes any flip-flop to change state. It is this internal delay which permits the PC register to be sampled and incremented by simultaneous pulses without transferring the incremented, rather than the original, contents to the MA.

At time T2 of every computer cycle, the MB is cleared and a read operation is prepared. Time pulse T2 is applied to an isolating gate (B3, 25), and the output of the gate causes a pulse amplifier to produce the 0→PC pulse. The TP2 pulse sets the READ flip-flops of the memory control (27) to 1 and is NAND combined with the MA4 (0) level to produce the TP2 · SEL 0, 1 pulse (A8, 27). Note that the MA4 bit is always 0 unless more than 8K of memory capacity is in use. The MA5 bit is decoded by the memory control to produce either a SEL 0 or a SEL 1 level which is used to select one of the two 4K memory stacks in the standard 8K field. The SEL level is combined with the 1 output of the READ flip-flops to produce an appropriate SEL · READ LEVEL, which is applied to memory. The action of the memory is discussed in detail in Chapter 4. The effect of the SEL and SEL · READ levels is to enable the half-select X and Y read circuits in memory. The TP2 · SEL 0, 1 pulse is applied to a delay network in memory to produce a strobe pulse which is applied to the sense amplifiers of the memory. This strobe pulse clears the READ 2 flip-flop and is returned to the main timing chain as the STB RTN pulse, which initiates the generation of T3 and clears the READ 1 flip-flop.

When the strobe pulse occurs, the memory sense amplifiers compare the signal level in the sense winding of each core plane with a reference level. In planes where coincident read currents have caused a core in the 1 state to change to the 0 state, the sense signal is greater than the reference level; and the associated sense amplifiers (SA) produce standard negative pulses.

These SA pulses are applied to the MB input gates (30) and set the corresponding MB flip-flops. The SA→MB input gates are normally enabled by an $\overline{\text{MB STB INH}}$ negative level generated in the MB control (25). Thus, the contents of the addressed memory cell are transferred to the MB unless the gates are specifically inhibited by the control logic. The conditions under which inhibition occurs are discussed in Chapter 3 under the heading of Memory Buffer Register Control. During a fetch cycle, when the MB is loaded with an instruction word consisting of an operation code and the address of the operand, the four most significant bits (which contain the operation code) are transferred directly into the IR, as well as into the MB. The negative pulses from sense amplifiers SA0 through SA3 are applied to IR input gates that are conditioned by the fetch level (B7, 24), and set the IR flip-flops accordingly.

After the strobe pulse has occurred, the contents of the various registers are as follows:

ADDRESS switches	Z (address of the first instruction, which in this example is LAC Y)
PC	Z+1
MA	Z
MB	MB0 through MB3 contain octal 20 (= LAC) MB4 (0) (= no indirect address) MB6 through MB17 contain Y (address of operand)
IR	IR0 through IR3 contain octal 20 (= LAC)

In the instruction register, the states of IR0 (0) and IR1 (1) are decoded to produce an IA1 level and a $\overline{\text{IA3}}$ level. The states of IR2 (0) and IR3 (0) are decoded to produce an IB0 level. The $\overline{\text{IA3}}$ level, which identifies the instruction as a memory reference instruction, is NAND combined with the existing fetch (F) and MB4 (0) levels (C1, 24) to establish a SET level. This ground level conditions the DCD gate (B3, 24) associated with a pulse amplifier which sets an execute (E) state into the major state generator at time T7. At the same time the ground level disables input L of module J21 to prevent any break request from being granted until the instruction has been executed.

At time T4, timing pulse TP4 sets the INH flip-flop of the memory control logic (C6, 27), thereby enabling the inhibit supply of the memory. At time T5, both WRITE flip-flops are also set and, in conjunction with the SEL 0 level, established coincident writing currents through the cores

of memory cell Z. All cores of the addressed cell are driven by full-select write currents. However, those in planes which correspond to MB bits containing a 0 are inhibited from changing state by a half-select inhibit current in the read direction. Thus, the contents of the MB are written back into the cell from which it was read.

At time T6, timing pulse TP6 resets the WRITE 1, WRITE 2, and INH flip-flops. The writing operation is now complete.

At time T7, timing pulse TP7 INVTD is applied to the DCD gates of the major state generator (24) and, in combination with the E SET level established during T3, sets the execute (E) state. The RUN flip-flop is still set, and the RUN (1) level is NAND combined with timing pulse T7 (A8, 25) to produce a 0→MA pulse which clears all the flip-flops of the MA. The RUN (1) level is also combined with a $\overline{\text{SLOW CYC}}$ (not slow cycle) level to condition a DCD gate at the entry to the main timing chain (D1, 22). The TP7 pulse (delayed 150 nsec) is combined with a $\overline{\text{STOP CP TC}}$ (not stop central processor timing chain) level which signifies that the extended arithmetic element does not require an interruption. The resulting pulse triggers the DCD gate and energizes a pulse amplifier (D2, 22). The output of this pulse amplifier causes the generation of timing pulse TP1, thereby initiating the second (execute) computer cycle.

At time T1 of the execute cycle, the absence of an IA0 signal at terminal S of module D5 (C1, 25) results in the production of a $\overline{\text{CAL}}$ (not CAL instruction) level. This level is NAND combined in the MA control (A7, 25) with the T1 timing pulse and another negative level resulting from the absence of a defer (D) level. The output of the NAND gate is applied to a pulse amplifier which produces an MB1→ MA pulse. This pulse opens all MA input gates which are already conditioned by a negative level from an MB flip-flop in the 1 state; thus the address of cell Y (containing the operand) is set into bits 5 through 17 of the MA. The (E) level of the major state generator is NAND combined with the IA1 level produced by the IR, and the output of the gate is inverted to produce an E · IA1 level (D2, 26). The E · IA1 level is NAND combined with the IB0 level and inverted to produce an E · LAC level. The E · LAC level enables a NAND gate which is opened by time pulse T1 to trigger a pulse amplifier in the AC control logic (A6, 26). This pulse amplifier produces a 0→AC pulse which clears all the flip-flops of the accumulator.

During the execute cycle, the contents of memory cell Y are read into the MB and then rewritten into memory in exactly the same manner as for cell Z (during the fetch cycle). Therefore, the following paragraphs describe only those events peculiar to the execute cycle. After the strobe occurs, the contents of the various registers are as follows:

PC	Z+1
MA	Y
MB	Contents of cell Y
IR	Octal 20 (= LAC)
AC	All zeros

At time T3 of the execute cycle, the E · IA1 level is combined with the T3 timing pulse. The resulting pulse is applied to pulse amplifier PA2 of module H2 in the AC control logic, and the output of the pulse amplifier is an XOR→AC pulse. This pulse is applied to a set of accumulator register input gates which are normally used to complement the accumulator in an exclusive OR operation. However, since the accumulator was cleared at time T1 (of the execute cycle), no carry pulses can be generated; and the effect is a simple transfer of memory buffer 1's into the corresponding bits of the accumulator.

After the operand has been rewritten into memory cell Y (starting at time T4) the MA is cleared, and the interrupt control is interrogated to determine the state to be set into the major state generator for the next cycle. If any I/O device has initiated a break request, the interrupt control logic (32) establishes a negative BK RQ (break request) level which is applied to terminal K of module H20 in the major state generator. Then, provided that neither a D SET nor an E SET level has previously been established by the nature of the instruction, a B SET ground level appears at terminal N of the module. This level, in combination with timing pulse TP7 INVTD, sets the major state generator to the break (B) state so that the I/O device may be serviced. If there is no break request, the $\overline{\text{BK RQ}}$ combines with $\overline{\text{D SET}}$ and $\overline{\text{E SET}}$ levels to produce an F SET level; and, at time T7, a new fetch cycle is initiated to extract the next instruction from memory address Z+1. Note that a break request is never granted until the current instruction has been executed. Thus, a break can be granted only after completion of a 1-cycle instruction; after the execute cycle of a multicycle instruction; or after a break cycle to continue a block transfer or other operation involving several break cycles.

Exclusive OR (XOR) - The exclusive OR logical operation is performed between the contents of the AC and the contents of the MB and requires a fetch cycle and an execute cycle. During the fetch cycle, the operation code 24 is set into the IR; and the address of the operand is set into bits 5 through 17 of the MB. At time T1 of the execute cycle, the address of the operand is transferred from the MB to the MA. At time T2, the MB is cleared; and a read operation sets the operand into bits 0 through 17 of the MB. The E negative level of the major state generator is NAND combined in the AC control with the IA1 negative level produced by the IR decoder. The resulting E · IA1 negative level is combined in the AC control with timing pulse T3 to produce a negative XOR→AC pulse. This pulse opens AC input gates already conditioned by MB bits in the 1 state and complements the associated AC bits. When the AC has previously been cleared (as in the LAC instruction), the XOR→AC command can be used for a simple transfer of binary 1's from MB to AC.

One's Complement Add (ADD) - The ADD instruction adds the contents of the MB to the contents of the AC in 1's complement arithmetic and requires a fetch cycle and an execute cycle. During the fetch cycle, the operation code 30 is set into the IR; and the address of the operand is set into bits 5 through 17 of the MB. At time T1 of the execute cycle, the address of the operand is transferred from the MB to the MA. At time T2, the MB is cleared; and a read operation sets the operand into bits 0 through 17 of the MB. At time T3, the E · IA1 negative level causes an XOR operation to be performed in the manner already described. In the AC control, the E negative level is further combined with the IB2 level produced by the IR decoder to produce an E · ADD level. The E · ADD level, in combination with timing pulse T4, produces a negative AC CRY (accumulator carry) pulse. This carry pulse opens accumulator input gates in which the state of each AC bit is compared with the state of the corresponding MB bit. Carries are propagated where necessary. A carry pulse generated by bit AC0 causes a negative END CRY (end carry) pulse to be generated. The END CRY pulse is applied to the complementing input of the AC17 flip-flop; if this is already in the 1 state, further carries are propagated toward bit AC0.

Two's Complement Add (TAD) - The TAD instruction adds the contents of the MB to the contents of the AC in 2's complement arithmetic and requires a fetch cycle and an execute cycle. During the fetch cycle, the operation code 34 is set into the IR; and the address of the operand is set

into bits 5 through 17 of the MB. At time T1 of the execute cycle, the address of the operand is transferred from the MB to the MA. At time T2, the MB is cleared; and a read operation sets the operand into bits 0 through 17 of the MB. At times T3 and T4, XOR and carry operations are performed as described for the ADD instruction. At time T5, an overflow from bit AC0 causes generation of a TAD CRY (2's complement carry) pulse which sets the LINK flip-flop to 1. The effect of the link depends upon what instruction follows; it may be sensed by an augmented instruction to cause a skip, for example.

Execute (XCT) - The XCT instruction causes the CP to execute the instruction contained in the memory cell addressed. The instruction requires a fetch cycle plus the cycles required to perform the instruction contained in the cell. During the fetch cycle of an XCT instruction, the operation code 40 is set into the IR; and the address of the instruction to be performed is set into bits 5 through 17 of the MB. At time T1 of the execute cycle, the address of the instruction is transferred from the MB to the MA. At time T2, the IR is cleared, and a fetch state is forced. Between times T2 and T3, the contents of the addressed memory cell are read into the MB; and the four most significant bits (containing the operation code) are set into the IR. The CP then executes the instruction which was contained in the cell addressed by the XCT instruction. Note that even if the subject instruction is a memory reference instruction, the effective address of the operand is available without reference to the PC, so that the program sequence is unaltered. In other words, the CP acts as if it were performing the subject instruction in place of the XCT instruction, then proceeds to the instruction following the XCT instruction.

Index and Skip if Zero (ISZ) - The ISZ instruction increments the contents of the addressed cell by 1, using 2's complement arithmetic. If the incremented number is 0, the next instruction is skipped. The ISZ instruction requires a fetch cycle and an execute cycle. During the fetch cycle, the operation code 44 is set into the IR; and the address of the operand is set into bits 5 through 17 of the MB. At time T1 of the execute cycle, the address of the operand is transferred from the MB to the MA. Between times T2 and T3, a read operation sets the operand into the MB. The E level derived from the major state generator is combined in the MB control with the IA2 and IB1 levels produced by the IR decoder. The resulting E · ISZ level conditions a gate which is opened by timing pulse TP3 to produce a +1→MB negative pulse. This pulse complements the least significant bit of the MB and is also applied to the MB gates which

propagate carry pulses. If the MB overflows (which can only happen when the contents of the MB become 0), bit MB0 generates a carry pulse which is combined in the PC control with the E · ISZ level. As a result, a negative pulse is generated which increments the contents of the PC by 1. Starting at time T4, the incremented contents of the MB are written back into the memory cell addressed by the ISZ instruction. Note that at time T1 of the fetch cycle, the address of the ISZ instruction was set into the MA; and the contents of the PC were incremented in the normal manner. If the incremented contents of the MB were not 0 and therefore produced no overflow at time T3 of the execute cycle, the next instruction is fetched and executed. An overflow from the MB, however, causes the contents of the PC to be incremented again, so that the instruction immediately following ISZ in the program is skipped.

Logical AND (AND) - The logical AND operation is performed by a transfer of 0's from the MB to the AC. Thus, at the end of the operation, all bits of the AC have been cleared except those bits which contained a 1 both in the AC and in the operand before the operation started. The AND instruction requires a fetch cycle and an execute cycle. During the fetch cycle, operation code 50 is set into the IR; and the address of the operand is set into bits 5 through 17 of the MB. During the execute cycle, the address of the operand is transferred from the MB to the MA at time T1. Between times T2 and T3, the operand is read into the MB. The E level derived from the major state generator is combined in the AC control with the IA2 and IB2 levels from the IR decoder to produce an E · AND level. This level conditions a NAND gate, which at time T5 is triggered to produce an MB0→AC pulse. The MB0→AC pulse clears all AC bits corresponding to MB bits which are in the 0 state. AC bits which are already in the 0 state remain 0's, regardless of the state of the corresponding MB bit. AC bits which are in the 1 state remain 1's only if they correspond to MB bits in the 1 state.

Skip if AC is Different From Operand (SAD) - The SAD instruction sets the operand into the MB and performs an XOR operation between the MB and the AC. No carry pulses are propagated, so that if the initial contents of the AC are identical to that of the MB, the end contents of the AC will be 0, and the next instruction will be performed. If any one bit of the AC differs from the corresponding bit in the MB, the next instruction is skipped. The SAD instruction requires a fetch cycle and an execute cycle. During the fetch cycle, the operation code 54 is set into the IR; and the address of the operand is set into bits 5 through 17 of the MB. The

contents of the PC are incremented in the normal manner. At time T1 of the execute cycle, the address of the operand is transferred from the MB into the MA; and a read operation sets the operand itself into the MB. The E level derived from the major state generator is combined in the AC control with the IA2 and IB3 levels from the IR decoder to produce an E · SAD level. The E · SAD level conditions a gate which is opened at time T3 to produce a negative XOR pulse. The XOR pulse causes MB bits in the 1 state to complement the corresponding bits of the AC. No carry pulses are propagated, so that if the initial contents of the AC are identical to that of the MB, the resultant contents of the AC are all 0's. A 17-input AND gate in the AC control samples the status of all the AC flip-flops at time T5 and generates an AC=0 level only if all flip-flops are in the 0 state. The AC=0 level is combined in the PC control with the E · SAD level to generate a +1→PC pulse which increments the contents of the PC by 1. Thus, if the initial contents of the AC were identical to that of the operand, the next instruction is skipped. If any one AC flip-flop is in the 1 state after the XOR operation (indicating that the contents of the AC were different from that of the operand), the AC=0 level is not produced by the AC control gate, and the +1→PC pulse is not generated. The CP, therefore, proceeds to the next instruction and executes it. The XOR operation is repeated at time T6 to restore the original contents of the AC.

Deposit AC in Memory (DAC) - The DAC instruction deposits the contents of the AC in memory at the address specified in the instruction. The instruction requires a fetch cycle and an execute cycle. During the fetch cycle, the operation code 04 is set into the IR, and the address of which the contents of the AC are to be deposited is set into bits 5 through 17 of the MB. At time T1 of the execute cycle, the address for the deposit is transferred from the MB to the MA. The E level derived from the major state generator is combined in the MB control with the IA0 and IB1 levels from the IR decoder to produce an E · DAC level. This level causes an AC1→MB pulse to be generated at time T3. The AC1→MB pulse opens the gates connecting the output of the AC to the input of the MB. A write operation (starting at time T4) deposits the new contents of the MB into memory at the address specified by the DAC instruction. Note that although read currents are applied to the addressed cell, the combination of the E and IA0 levels in the MB control produces an MB STB INH (MB strobe inhibit) level that inhibits the gates between the sense amplifiers and the input of the MB. Therefore, the original contents of the addressed cell are not transferred into the MB, and so are lost. Note also that when a pseudo-DAC instruction is used for loading information from perforated tape, the RPT(1) level causes the generatic

of a SEL → RRB pulse at time T2, which transfers the contents of the reader buffer into the AC. For further details, refer to the description of the READ-IN key in the Manual Operations paragraph. At the end of a readin operation, the combination of the RPT (1) level and a reader hole 7 signal clears the RPT flip-flop and sets the RUN flip-flop at time T5. The fetch state is then established for the execution of the next instruction. However, if the readin operation is to continue, the RPT (1) level causes the MB to be cleared at time T7 and starts the special pulse generator.

Deposit Zero in Memory (DZM) - The DZM instruction clears the memory cell at the address specified in the instruction and requires a fetch and an execute cycle. During the fetch cycle, the operation code 14 is set into the IR; and the address for the deposit is set into bits 5 through 17 of the MB. At time T1 of the execute cycle, the address for the deposit is transferred from the MB to the MA. At time T2, the MB is cleared; and a read operation is initiated in the normal manner. The E level derived from the major state generator is combined in the MB control with the IA0 level from the IR decoder, thereby inhibiting the gates between the memory sense amplifiers and the MB. Information previously stored in the addressed cell is read, but does not reach the MB and is therefore lost. A normal write operation takes place, starting at time T4; but since the MB was cleared, 0 is written into the addressed cell. At the end of the execute cycle, the fetch state is established in preparation for execution of the next instruction.

Jump to Subroutine (JMS) - The JMS instruction permits exit from the main program into a subroutine and requires a fetch and an execute cycle. During the fetch cycle, the operation code 10 is set into the IR; and an address (Y) is set into bits 5 through 17 of the MB. At time T1 of the execute cycle, address Y is transferred from the MB into the MA. At time T2, the MB is cleared and the input gates are inhibited; so that the normal read operation destroys the original contents of cell Y. At time T3, the current program count and the status of the link are transferred to the MB; the PC is then cleared. This information is written into cell Y and is available there when re-entry into the main program is desired. At time T4, the address Y is transferred from the MA to the PC; and, at time T5, the contents of the PC are incremented by 1. The end contents of the PC are Y+1, the address from which the first instruction of the subroutine is fetched.

Call Subroutine (CAL) - The CAL instruction is equivalent to the instruction JMS 20. During the fetch cycle, the operation code 00 is set into the IR; and the IR decoder produces IA0 and IB0 levels. These are combined in the MB control with a $\overline{B}$ (not a break state) level to produce a CAL level. At time T1 of the execute cycle, the CAL level is combined in the MA control with the E level derived from the major state generator and generates a 20→MA pulse. This pulse sets octal 20 into the MA by setting flip-flop MA13 to the 1 state. The 20→MA pulse also sets flip-flop IR2, thereby setting operation code 10 (JMS) into the IR. Thereafter, the CP proceeds to execute the JMS instruction, depositing the link status and current program count at memory location 20 and taking the first instruction of the subroutine from memory location 21, as described in the explanation of the JMS instruction.

Jump (JMP) - The JMP instruction transfers control of the CP to a sequence of consecutive memory locations that begins at the address specified in the instruction. The JMP instruction requires only one cycle (fetch), during which the operation code 60 is set into the IR; and the memory location from which the next instruction is to be taken is set into bits 5 through 17 of the MB. The IA3 and IB0 levels derived from the IR decoder are combined in the major state logic to produce a JMP level which conditions two gates in the PC control. At time T5, one of these gates is triggered to produce a 0→PC pulse which clears the PC. At time T6, the second gate is triggered to produce an MB1→ PC pulse which transfers the address specified by the JMP instruction into the PC. The major state generator is then set to fetch, and, during the following cycle, the next instruction is fetched from that address.

Indirect Addressing and Auto-Indexing

When bit 4 of a memory reference instruction contains a 1, the CP interprets the contents of bits 5 through 17 as the memory location where the address of the operand may be found. At time T7 of the fetch cycle, the major state generator is set to defer instead of to execute. At time T1 of the defer cycle, the contents of the MB are transferred to the MA (unless the instruction is CAL). The MB is then cleared, and a read operation sets the contents of the addressed cell into the MB, which now holds the effective address of the operand. If this address is one of the eight auto-indexing locations 10_8 through 17_8, decoding gates in the MA generate a pulse which increments the contents of the MB by 1 at time T3. If the instruction containing the indirect address was a JMP instruction, the PC is cleared at time T5; the effective address of

the next instruction is transferred from MB to PC at time T6; and the major state generator is set to fetch at time T7. If the instruction was not a JMP, no action occurs at times T4 through T6. The major state generator is set to execute at time T7. At time T1 of the execute cycle, the effective address of the operand is transferred from MB to PC. The machine then performs the operation specified by the instruction upon the operand contained in the indirectly addressed cell.

The eight auto-index locations may contain either the effective address of an operand or an instruction, depending on the program requirements. When used as direct addresses, they are identical to other memory locations. When used as indirect addresses, however, their contents are incremented by 1 each time they are addressed. Thus, use of the auto-indexing locations facilitates the repetition of an arithmetic process on a series of numbers without performing separate arithmetic operations on the addresses concerned. The PDP-7 Users Handbook explains the uses of the auto-index locations from the programmer's viewpoint.

Augmented Instructions

The augmented instructions are of three types: EAE instructions with the operation code 64, discussed with the EAE logic functions; IOT (input/output transfer) instructions with the operation code 70; and OPR/LAW (operate/law) instructions with the operation code 74. These instructions do not need a memory reference and are therefore completed in one cycle (fetch). Bits 4 through 17 are decoded to produce command pulses for the various possible operations. Since these take place at different times, several operations may be combined in a single instruction.

Operate (OPR) - The bit assignment of an OPR instruction is shown in Figure 1-3. It will be seen that bit 5 is used in one instruction only, i.e., clear accumulator (CLA) for which the octal code is 750000. All other instructions of the OPR class have octal codes beginning with 74. The functions performed at times T1 through T4 of an operate instruction are exactly the same as those which occur in the fetch cycle of any other kind of instruction. The IA3 and IB3 levels from the IR decoder are combined in the AC control with the MB4 (0) level to produce the OPR level. This level conditions two gates: one is triggered at time T5 to perform one set of operations and the other gate is triggered at time T7 to perform the second set of operations. The first set of commands consist of the following:

1. If bit 5 is a 1, the AC is cleared.

2. If bit 6 is a 1, the link is cleared.

3. If bits 7 and 13 are 1's, the AC is rotated one place right (and will be rotated again during time T7).

4. If bits 7 and 14 are 1's, the AC is rotated one place left (and will be rotated again during time T7).

5. If bit 12 is a 1, the RUN flip-flop is cleared and the program is halted at the conclusion of the current memory cycle.

6. If bit 8 is a 0, any one of the following conditions increments the contents of the PC to skip the next instruction: link is not 0 (bit 9 is a 1); AC is not 0 (bit 10 is a 1); AC is negative (bit 11 is a 1).

7. If bit 8 is a 1, the conditions that produce a skip are inverted (link is 0, AC is 0, or AC is positive).

The second set consists of the following operations which take place in time T7:

1. If bit 13 is a 1, the AC is rotated one place right.

2. If bit 14 is a 1, the AC is rotated one place left.

3. If bit 15 is a 1, the contents of the accumulator switch register are inclusively OR combined with the contents of the AC.

4. If bit 16 is a 1, the link is complemented.

5. If bit 17 is a 1, the AC is complemented.

Note that because of the nature of the rotate operations, a rotate operation may not be combined with any other operation of the same set. For example, a single instruction may clear the link (first set) and rotate the AC one place (second set); but a 2-place rotation (both sets) precludes the instruction from performing any other operation.

Law (LAW) - The LAW instruction is a special case of an operate class instruction and has the operation code 76. The IR decoder produces IA3 and IB3 levels which are combined in the AC control with the MB4 (1) level to produce an OP LAW level. This level conditions two AC control gates: one is triggered at time T5 to clear the AC and the other at time T6 to perform an XOR operation between MB and AC. This effectively places the entire instruction in the AC. Thus, an address-sized number (15 bits), preceded by the operation code, can be loaded into the AC without using an extra memory location. The various uses of the LAW instruction are described from the programmer's viewpoint in the PDP-7 Users Handbook.

Input/Output Transfer (IOT) - IOT instructions are augmented instructions which can be microprogrammed to address an I/O device and to generate up to three time pulses to initiate and control the operation of the device. When an IOT instruction is executed, if bit 14 is a 1, the AC is cleared at time T5; if bit 17 is a 1, an IOP1 pulse is also generated at this time. If bit 16 is a 1, an IOP2 pulse is generated at time T7. If bit 15 is a 1, an IOP4 pulse is generated at time T1 of the following cycle. For a description of the device selection and control processes, refer to Chapter 3.

Break Cycle

A break cycle provides a temporary interruption of the main program during which information may be transferred to or from a high-speed peripheral device or a subroutine may be initiated to service a slow peripheral device. Reference to the flow diagram (21) shows that a break cycle may be entered under the following conditions (which indicate an "instruction done" situation):

1. After the fetch cycle of an OPR, LAW, IOT, or directly addressed JMP instruction.

2. After the defer cycle of an indirectly addressed JMP instruction.

3. After the execute cycle of a directly or indirectly addressed memory reference instruction.

4. After a break cycle to continue a block transfer or other operation involving several break cycles.

When a break request from peripheral equipment is granted, one of three possible sequences takes place during the break cycle. If two or more break requests appear simultaneously, break sequences are granted in the following descending order of priority: data break, clock break, and program break.

Data Break

A data break may be granted to a high-speed I/O device containing registers which can simultaneously supply or accept a 15-bit address word, an 18-bit data word, a break request signal, and a direction-of-transfer signal. When a data break is granted, the IR is cleared; and the address specified by the I/O device is set into the MA at time T1 of the break cycle. If the I/O device specifies an outward transfer, the contents of the addressed memory cell are read into the MB between times T2 and T3 and are available there for sampling by the input register of the I/O device. If an inward transfer is specified, the gates between the sense amplifiers and the MB are inhibited. As a result, any information contained in the cell is destroyed, and the cell is cleared. At time T3 of the break cycle, the input gates linking the MB directly to the output register of the I/O device are triggered; and the incoming data is set into the MB. A normal write operation, starting at time T4, writes the data into the memory cell. Use of the Type 173 Data Interrupt Multiplexer permits up to four high-speed I/O devices to share the data interrupt channel. (Refer to Chapter 6 for further details.) After completion of the high-speed transfer, a fetch state is established for continuation of the program, unless a further break request exists. In this case, another break cycle follows.

Clock Break

A real-time clock, which can be enabled or disabled under program control by the appropriate IOT instruction, is included in each PDP-7 system. When the clock is enabled, each clock pulse initiates a break request. When the break is granted, the IR is cleared at time T1 of the break cycle. The clock address 7_8 is set into the MA and the clock count request flip-flop is cleared. Between times T2 and T3, the contents of memory location 7_8 (the clock count) are read into the MB; and, at time T3, the contents of the MB are incremented by 1. A normal write operation, starting at time T4, deposits the incremented clock count in memory location 7_8. If incrementing the MB did not cause an overflow, a fetch state is established at time T7 to

continue the main program (unless there is a further break request). If incrementing the clock count caused the MB to overflow, a carry pulse is generated by bit MB0. This carry pulse sets the clock flag to 1, thereby initiating a program break. Possible programming uses of the real-time clock are described in the PDP-7 Users Handbook.

Note that when the automatic priority interrupt (API) option is included in the PDP-7 system, the real-time clock is removed and the API is connected in its place. The real-time clock may then utilize one of the API channels. For further details of the API, refer to Chapter 6.

Program Break

Slow I/O devices, such as the Teletype or paper tape reader, require an interval of several milliseconds between the time one information transfer is performed and the time when the device is ready for the next transfer. During this interval, the PDP-7 can perform many hundreds of programmed instructions. When one or more such devices have been enabled by the programmed instructions, the program break facility permits the CP to continue execution of the main program until such time as a device indicates, by setting its flag, that it is ready to send or receive information. The setting of any device flag generates a program break request, and at the first "instruction done" situation the CP enters a break cycle in which the address of the next main program instruction, together with the status of the link, trap flag, and extend mode are stored at location 0. Control of the processor is then transferred to a subroutine starting in location 1, which scans all the device flags to discover which device caused the interrupt. Identification of the interrupting device may provide entry to a further subroutine for servicing the device. At the conclusion of the servicing subroutine, the main program may be reentered by a jump indirect to location 0, which transfers program control to the address stored at location 0.

A program break is granted when all of the following conditions are fulfilled:

1. The program interrupt facility has previously been enabled by a programmed ION instruction.
2. The setting of a device flag has generated a program break request.
3. There is no data break in progress or waiting.

4. There is no clock (or API) break in progress or waiting.

5. There is no program break in progress.

At time T1 of the break cycle, the IR is cleared, and at time T2 the MB is cleared. The memory generates read currents which clear location 0, but the MB input gates are inhibited so that any information previously contained in that location is destroyed. At time T3 the link status is set into bit MB0, the extend mode status into bit MB1, and the trap flag status bit into MB2. The contents of bits PC3 through PC17 are transferred to the corresponding bits of the MB and the PC is cleared. At time T4, the contents of the MA are transferred to the PC; note, however, that the MA was cleared at time T7 of the previous cycle and was not reloaded, so its contents are still 0. Also at time T4, a normal write operation is begun which deposits the contents of the MB in memory at location 0. At time T5, the contents of the PC are incremented by 1, so that the next instruction will be taken from location 1 in which a subroutine starts. The program interrupt enable flip-flop is cleared to prevent any other program breaks until the interrupt is enabled by a programmed instruction at the conclusion of subroutine operations. Note, however, that data breaks and clock (or API) breaks may still be granted. If the program is operating in the trap mode and the program break was initiated by the trapping of an illegal instruction, the contents of the PC are again incremented by 1 at time T5. Thus, control of the CP is transferred to a subroutine starting in memory location 2 in order to identify the trapped instruction and take appropriate action. If no data break or clock break request has been originated during the break cycle, a fetch state is established at time T7 and the first subroutine instruction is fetched during the ensuing fetch cycle. If a data or clock break request exists, a further break cycle is granted before the subroutine is entered.

Trap Mode

When the PDP-7 forms part of a real-time or multiuser system, the trap mode permits the use of sophisticated programming in the main program and guarantees this against interference from other users operating in a different section of memory. When the main program is operating in real time, it is particularly important to ensure that the processor cannot be halted, involved in lengthy operations, or thrown into a loop from which it cannot escape. The I/O trap provides the basic hardware necessary to provide protection against such disturbances.

When the trap mode is enabled by turning on the TRAP switch and by a programmed ITON (I/O Trap On) instruction, the following illegal instructions are trapped: all IOT instructions; all HLT (halt) instructions; and all XCT (execute) instructions. When an illegal instruction is detected, the trap flag is set, thereby preventing execution of the instruction. Instead, a program break request is initiated. When the break is granted, control of the CP is transferred to a subroutine starting at memory location 2, which initiates procedures for identifying the trapped instruction and for taking appropriate action. The reason for trapping halt instructions is obvious; IOT instructions are trapped because, if not well planned, they could involve the CP in lengthy operations to the detriment of the real-time operations; XCT instructions are trapped because if the subject instruction were also an XCT, a loop situation could arise in which the CP would never encounter an "instruction done" situation, so that all control would be lost.

CHAPTER 3

PROCESSOR

This chapter describes in detail the logic elements which perform the logic functions described in Chapter 2. Descriptions of registers consider the effect of the various control signals applied; descriptions of control elements consider the output signals and explain the conditions under which each of these is generated. Many types of FLIP CHIP modules consist of a number of similar components (e.g., Type W607 contains three identical pulse amplifiers). Where necessary the individual components of a module are identified by their input and output terminal letters (e.g., NOR gate NPR of module J5). In addition, references to the zone of the engineering drawing in which the component is located aid in identification of a particular component.

All logic circuit elements of the processor are shown on the block diagram of Figure 3-1. These elements consist of the major registers and their associated control elements, the timing generators for the computer system, the manual controls, and the special program feature controls (data break control, program interrupt control, I/O skip, I/O trap, etc.).

MAJOR REGISTERS

AC Register (30, 31)

The AC is the major arithmetic register of the CP and is involved in most of the mathematical, logical, and I/O transfer operations performed by the computer. This register consists of 18 Type B210 Accumulator FLIP CHIP modules at locations 1EF2 through 1EF19. The AC has a storage capacity of 18 bits. Each flip-flop of the AC can be individually set or cleared, in programmed operation, by means of gated signals from other registers or from external equipment. The flip-flops can also be set (but not cleared) by means of the ACCUMULATOR switches on the operator console. The AC may also be cleared collectively, or its contents incremented by 1, complemented, rotated, or shifted right or left. The status of each flip-flop in the register is shown by an indicator on the operator console.

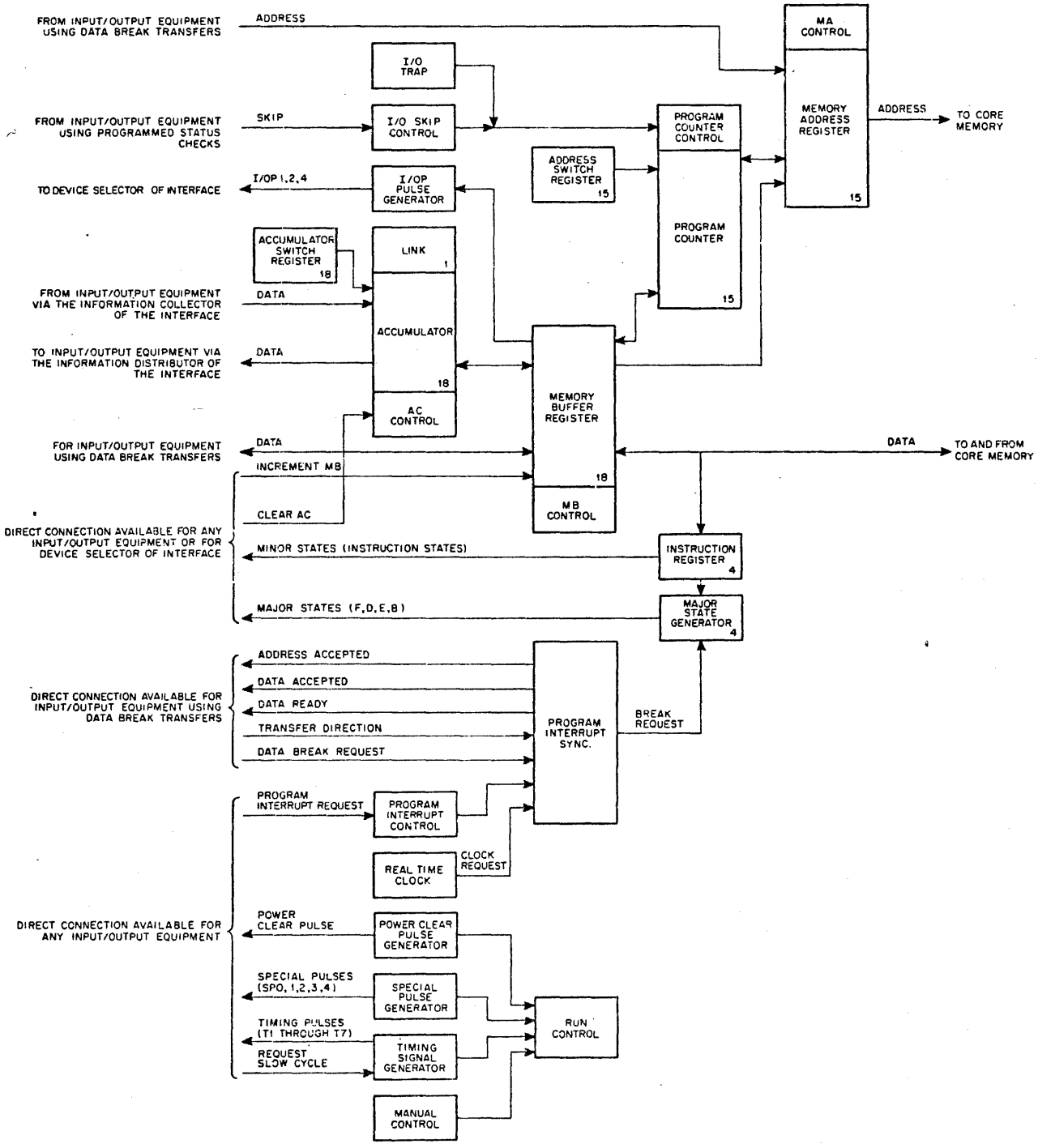


Figure 3-1 Processor Detailed Block Diagram

Each Type B210 module is a double-height module containing one buffered-output flip-flop, a carry pulse amplifier, and all the required transistor gating elements. The flip-flop is set or cleared by a positive pulse from a gating circuit; the gates are conditioned by negative levels and are triggered by negative pulses.

All bits of the accumulator are cleared collectively by a 0 → AC pulse applied to input terminal EV of a transistor gate connected to the direct clear input (ES) of the flip-flop.

Each bit of the AC may be individually set by a positive pulse from the information collector applied to terminal EU, which is connected to the direct set terminal (ET) of the flip-flop. An unused transistor gate permits a bit to be set by application of a negative pulse to terminal FL.

Rotate right operations are performed by a pair of transistor gates to which the RAR pulse is applied (at terminals EN and EJ). These gates set or clear the associated flip-flop according to the status of the adjacent flip-flop of greater significance. The (1) level of this flip-flop is applied to terminal EH, and the (0) level to terminal EM.

Rotate left operations are performed by a similar pair of gates to which the RAL pulse is applied (at terminals EL and ER). These gates are conditioned by the (1) level (terminal EK) and the (0) level (terminal EP) of the adjacent flip-flop of less significance.

Each bit of the AC may be cleared by a 0 in the corresponding bit of the MB. The MB (0) level is applied to terminal FH and clears the AC flip-flop when an MB0 → AC pulse is applied to terminal FF.

Each bit of the AC may be set by a 1 in the corresponding bit of the accumulator switch register. The (1) level from the corresponding ACCUMULATOR switch is applied to terminal FK, and the ACS1 pulse to terminal FJ.

Complementing is accomplished by applying a positive pulse to both the direct set and direct clear inputs of the flip-flop, through isolating diodes. Complementing is performed by any one of the following:

1. A negative C → AC pulse is applied to terminal FT; a transistor inverts the pulse.

2. A positive pulse from the XOR NAND gate; this gate is conditioned by an MB (1) level applied to terminal FV, and is triggered by a negative XOR → AC pulse applied to terminal FU. The output of the gate complements the AC flip-flop.

3. By a carry pulse from the adjacent AC bit of less significance. The negative carry pulse is applied to terminal FP and is inverted by a transistor.

Carry pulses from one bit to the adjacent bit of greater significance are generated by a pulse amplifier contained in the Type B210 module. A carry from bit ACx to bit ACx-1 is generated under the following conditions:

1. When bit ACx contains a 1, and a carry pulse is received from bit ACx+1. The negative ACx (1) level conditions terminal FD of a NAND gate; the incoming carry complements bit ACx and triggers the NAND gate. The output of the gate triggers the carry pulse amplifier which transmits a carry pulse to bit ACx-1.

2. During an ADD or TAD instruction, an XOR operation is first performed between the MB and the AC. After the XOR operation, an AC CRY pulse is applied to all bits of the AC at terminal FR of a NAND gate. If the level inputs of this gate are conditioned by an MBx (1) level applied to terminal FV and an ACx (0) level applied to terminal FE, the AC CRY pulse causes the gate to trigger the carry pulse amplifier and a carry is transmitted to bit ACx-1. The resulting changes of state in flip-flops of greater significance may result in additional carries being propagated as described in 1 (above).

Link (26)

The link (L) is an extension of the AC and is used for data overflow. The link consists of a single Type B210 Accumulator module at location 1EF1. Storage capacity is a single bit. The link is capable of the same functions as the AC and can be operated independently of, or in conjunction with, the AC. The status of the link is shown by an indicator on the operator console.

The link is cleared by any one of the following conditions:

1. By a BGN pulse at time SP1 of any key operation

2. By a microprogrammed rotate right command, if bit AC17 is 0

3. By a microprogrammed rotate left command, if bit AC0 is 0

4. By a microprogrammed clear link command (bit MB6 is 1) at time T5 of the computer cycle

The link is set by any one of the following conditions:

1. By an EAE SET L pulse originating in the extended arithmetic element

2. By a microprogrammed rotate right command, if bit AC17 is 1

3. By a rotate left command, if bit AC0 is 1

4. By timing pulse TP1 of the computer cycle, if the AC overflowed during the previous cycle

The link is complemented:

1. By an AC0 CRY (overflow) during a EAE multiply or divide operation

2. By a TAD CRY pulse generated: by an AC overflow during 2's complement addition; by a microprogrammed complement link command in an operate instruction; or by a complement link command originating in the EAE

Program Counter (29)

The PC governs the core memory address from which the next instruction will be drawn. This register consists of 15 Type B201 Flip-Flops at locations 1D18 through 1D32 and 7 Type B620 Carry Pulse Amplifiers at locations 1E21 through 1E27. The PC has a storage capacity of 15 bits. In normal (nonextended) operations, only 13 of these are used. The 13 flip-flops containing these 13 least significant bits can be individually set either by gated signals in automatic

operation or by the ADDRESS switches in manual operation. The PC can only be cleared collectively. The inclusion of complementing gates and carry pulse amplifiers permits the contents of the PC to be incremented by 1 injected into the least significant bit. The status of each flip-flop is shown by an indicator on the operator console.

Memory Address Register (29)

The (MA) contains the address of the core memory cell currently selected for reading or writing. This register consists of 15 Type B201 Flip-Flops at locations 1A18 through 1A32. The MA has a storage capacity of 15 bits. Each flip-flop of the MA can be individually set by gated signals from other registers but can only be cleared collectively. The status of each flip-flop is shown by an indicator on the operator console.

Memory Buffer Register (30)

The (MB) serves as a data buffer between the processor and the core memory. This register consists of 18 Type B201 Flip-Flops at locations 1C2 through 1C19 and 9 Type B620 Carry Pulse Amplifiers at even-numbered locations 1B2 through 1B18. The MB has a storage capacity of 18 bits. The register flip-flops can be individually set by gated signals but can only be cleared collectively. The circuitry of the MB is very similar to that of the MA with the addition of the pulse amplifiers and complementing gates which allow the contents of the MB to be incremented by 1, injected into the least significant bit. The status of each flip-flop is shown by an indicator on the operator console.

Major State Generator (24)

The multistate device which generates the four major state levels is composed of four NAND gates: three are contained in a Type B115 FLIP CHIP module at location H18, and the fourth in another similar module at location J17. When disabled, each NAND gate produces a negative level at its output terminal; when fully enabled by three negative levels, the gate produces a ground output level. The gates are so interconnected that the output signal of each gate is applied to one input terminal of each of the other three gates. Thus, if the fetch produces a ground output, this signal disables the other three gates, so that each produces a negative output. These three negative output signals are returned to the input terminals of the

fetch gate to maintain it in the fully enabled state. If a positive pulse is now applied to the output of the execute gate, this pulse keeps the defer and break gates disabled, but also disables the fetch gate. Terminals F and E of the execute gate remain enabled by the negative levels from the defer and break gates, but terminal D makes a transition from ground to −3v when the fetch gate is disabled. The execute gate is now enabled by three negative input levels, so that its ground output level is maintained after the setting pulse is ended. Setting pulses for the multistate device are provided by two Type R602 FLIP CHIP modules in locations J18 and H19. Each module contains two pulse amplifiers, which produce a standard positive 100-nsec pulse. Each pulse amplifier is provided with two DCD gates enabled by the combination of a ground level and a positive pulse. In principle, any state can be entered from any other state; however, certain necessary modifications to this principle are made by the major state gating.

During the execution of programmed instructions, the conditions established during any given cycle determine the major state for the next cycle. At time T7, those conditions are implemented by combining an F SET, D SET, E SET, or B SET level with timing pulse TP7 to produce a pulse that sets the multistate device. However, when starting a program, or when performing a manual operation, a fetch or execute state may be established by other means.

A fetch state is established by one of the following sets of conditions:

1. When the START key is depressed, the positive START level generated by the key circuits is combined with timing pulse SP1 of the key cycle. The resulting pulse triggers pulse amplifier PA1 in module J18 (B2, 24) which sets the multistate device to the fetch state.

2. A PI1 → MA pulse, inverted in module J30, triggers pulse amplifier PA2 of module J19 and establishes a fetch state.

3. When a program is running in the trap mode, and an illegal XCT instruction is trapped, a positive TRAP FLAG (0) level (produced only when the TRAP FLAG flip-flop is set) is combined with the XCT CY (1) signal. This establishes a fetch state immediately, to avoid implementing the illegal instruction.

4. During normal operation, an F SET level is combined in a DCD gate with timing pulse TP7 INVTD B; and the resulting output of the gate triggers pulse amplifier PA1 of module J18 to establish a fetch state.

The positive F SET level is generated by a NAND gate in module J21 (D1, 24) and appears at output terminal H of the gate. This gate normally produces a negative $\overline{\text{F SET}}$ level; however, when all three inputs are enabled by negative $\overline{\text{D SET}}$, $\overline{\text{E SET}}$, and $\overline{\text{BK RQ}}$ levels, the ground F SET level appears at the output. The $\overline{\text{D SET}}$ level indicates that the current instruction does not contain an indirect address which would require a defer cycle to follow the fetch. The $\overline{\text{E SET}}$ level indicates that the current cycle is not a defer cycle which would require an execute cycle to follow it. The $\overline{\text{BK RQ}}$ level indicates that no I/O device is in need of servicing.

An execute state is established under the following conditions:

1. When any operation key other than the START key is depressed, a negative $\overline{\text{START}}$ level derived from the key circuits enables a NAND gate in module J22 (B3, 24). When the BGN pulse of the key cycle is added, the gate triggers pulse amplifier PA2 of module J18 and establishes the execute state.

2. During programmed operation, an E SET level conditions one input of a DCD gate; and timing pulse TP7 INVTD B causes the gate to trigger the associated pulse amplifier and establish the execute state.

The ground E SET level is generated by one of three NAND gates located in modules J21, H20, and K19 (C1, 24). A ground E SET level appears at terminal H20U if all of the following conditions are met: the current cycle is operating in the fetch state; the operation code stored in the IR produces an $\overline{\text{IA3}}$ level (indicating that the instruction is not a single-cycle law, operate, or IOT instruction); and bit MB4 is 0 (indicating that the instruction contains the direct address of the operand). The ground E SET level appears at terminal J21F if the current cycle is operating in the defer state and the operation code produces an $\overline{\text{IA3}}$ level. The ground E SET level appears at terminal K19R if the RPT flip-flop is set (during a readin operation).

A defer state is established during the fetch cycle of any memory reference instruction or JMP instruction which contains a 1 in bit 4. The negative F level and MB4 (1) levels are combined in NAND gate JKL of module J21, and the output of the gate is inverted in inverter PRS of module J20. The output of this inverter and the output of NOR gate NPR of module J21 are both applied to inverter TUV in module J20. Note that both the NAND gate and the NOR gate must give negative outputs to produce the ground D SET level at terminal J20U. The NOR gate gives a negative output when the IA3 level from the IR decoder is at ground (this condition is not fulfilled when the IR contains 60 JMP, 64 EAE, 70 IOT, or 74 OPR/LAW), or when the $\overline{\text{IB0}}$ level is at ground (this condition is equivalent to an IB0 assertion and occurs when a JMP code is held in the IR).

A break state is established if a break request conditions NAND gate KLMN of module J21 (D1, 24), provided that neither a D SET nor an E SET level has already been established for the following cycle. These conditions can be fulfilled at time T7 of the fetch cycle of an OPR, LAW, IOT or directly addressed JMP instruction; during the defer cycle of an indirectly addressed JMP instruction; during the execute cycle of any multicycle instruction; and during a break cycle.

Instruction Register (24)

The IR flip-flops, together with the input gates and the output decoder, are shown at the right of engineering drawing 24. All four flip-flops are cleared simultaneously by the output pulse of pulse amplifier RNPM in module J16. This pulse amplifier is triggered by any one of the following conditions:

1. A BGN pulse applied to inverter input terminal H15E (C5, 24)

2. A timing pulse T1 applied to NAND gate NPR of module H16, when the gate is conditioned by an F (fetch) level

3. A timing pulse T1 applied to NAND gate JKL of module H16, when the gate is conditioned by a B (break) level

4. A timing pulse T2 applied to NAND gate DEF of module H16, when the gate is conditioned by an E·XCT level. (The E·XCT level is generated by combining the IA2 and IB0 levels from the IR decoder with the E (execute) level in NAND gate RSTU of module J17. The output of the gate is inverted and the E·XCT level appears at terminal H17U, provided that the trap flag is not set.)

A 4-bit operation code may be set into the IR in one of the following ways:

1. When an F level conditions the four input gates in module H13, a binary 1 pulse from any one of sense amplifiers SA0 through SA3 sets the corresponding IR flip-flop to 1.

2. During execution of a CAL instruction, the 20 → MA pulse generated in the MA control is applied to inverter input terminal J15D (C8, 24). The inverted pulse sets flip-flop IR2 to 1, thereby substituting a JMS (octal 10) operation code for the CAL (octal 00) code held in the IR.

3. During a deposit, deposit next, or read paper tape operation, a DP+DPN+READ-IN+RPT (1) level conditions NAND gate STU in module J12. The gate is triggered by timing pulse SP2 of the key cycle and sets operation code 04 (DAC) into the IR by setting flip-flop IR3 to 1.

4. During an examine or examine next operation, an EX+EXN level conditions NAND gate LMN in module J12. This gate is triggered by timing pulse SP2 of the key cycle and sets operation code 20 (LAC) into the IR by setting flip-flop IR1 to 1.

The operation code is decoded by two sets of NAND gates and inverters. The gates of module H14 and the inverters of module H15 decode the outputs of flip-flops IR0 and IR1. Gating levels IA0 through IA3 and $\overline{IA3}$ appear at terminals H15J, M, R, U, and T, respectively. The gates of module J14 and the inverters of module J15 decode the outputs of flip-flops IR2 and IR3. Gating levels IB0 through IB3 appear at inverter output terminals J15J, M, R, and U, respectively.

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pulse, which triggers a Type R302 one-shot in module K20 (D2, 22). The DCD input gate of this one-shot is conditioned by a positive SLOW CYC level; and, at the conclusion of the delay period, the level transition which appears at output terminal K20M initiates generation of pulse TP1 of a new cycle.

Every IOT instruction fetched from memory causes the minor state generator to produce negative IA3 and IB2 levels. These levels are applied to input terminals R and P, respectively, of module J23 (C4, 23), where they are NAND combined with the I/O TRAP (0) level. Thus, provided that the I/O TRAP flip-flop has not been set, the gate gives an output which is inverted and appears as a negative IOT level at terminal H23K. Each I/O device that requires a slow cycle must generate a negative REQUEST SLOW CYC level. This level is NAND combined with the IOT level in module J22 (D5, 23) to produce the positive SLOW CYC and negative $\overline{\text{SLOW CYC}}$ levels. The inverter in module H22, in turn, produces the negative SLOW CYC and positive $\overline{\text{SLOW CYC}}$ levels. These four levels control the gates that determine the signal paths through the timing chain for normal and slow cycles (engineering logic diagram 22). The total delay of the slow cycle is factory adjusted to accommodate the slowest I/O device in use.

When the tape reader is loading information into memory, each tape character is read into the reader buffer as the result of an operation in the READ-IN mode which utilizes timing pulses SP0 through SP4 of one key cycle. However, the reader buffer assembles an 18-bit computer word by storing three type characters successively in different sections of the buffer. The information transfer between reader buffer and processor must be delayed until the reader buffer is full. During readin, therefore, the RUN flip-flop is not set during the key cycle. Instead, a negative READ-IN level (generated by releasing the $\overline{\text{READ-IN}}$ key after initiating the operation) and a negative RPT (1) level condition the NAND gate in module K14 (D2, 22). When the reader starts to read the third tape character, the RD FLAG flip-flop is set, indicating that the reader is ready to transfer information, and the negative RD FLAG level conditions the third input of the gate. The last level to appear causes a positive-going level transition at terminal K14H, thereby initiating a timing cycle during which the complete word is transferred from the reader buffer into the processor. When the transfer is complete, the reader flag is reset, and the timing signal generator is halted until another word is ready for transfer.

Run Control (23)

The RUN flip-flop controls the continuous succession of normal computer timing cycles. When the flip-flop is set to 1, and there is no slow cycle or stop timing request, timing pulse TP7 of the current cycle (delayed by 150 nsec) is permitted to reenter the timing chain and generate timing pulse TP1 of the next cycle. When the RUN flip-flop is reset to 0, it disables a gate in the reentry path and stops the computer, unless other conditions permit a new cycle to be initiated. (Refer to the description of the timing signal generator for details.) The CP may be halted by the program but must then be restarted by a manual START or CONTINUE operation.

The RUN flip-flop is an unbuffered flip-flop contained in a FLIP CHIP Type R201 module which also contains two DCD gates for clear inputs and three for set inputs. The flip-flop is reset to 0 by the following events:

1. When power is turned on after a shutdown, PWR CLK negative pulses are inverted in module H22 and applied to a DCD clear input (terminal H26E) in order to establish initial conditions.

2. When any console key is depressed to initiate an operation, the SP0 timing pulse is applied to direct clear input terminal H26K, thereby causing any operation already in progress to be halted at the end of the current memory cycle.

3. A negative RUN STOP level generated by the STOP, SINGLE STEP, or SINGLE INSTRUCTION key (20) is inverted in module H22. The inverted signal appearing at terminal H22R conditions level input terminal H26J of a DCD gate. Timing pulse T5 is inverted in module J26, and the inverted pulse, applied to terminal H26H, triggers the gate and clears the RUN flip-flop.

4. A positive HLT pulse is applied to terminal H26E to trigger a DCD gate and clear the RUN flip-flop. The HLT command is generated by NAND combination (in module J24) of the I/O TRAP (0) level, an MB12 (1) level, and an IOP 1 pulse. The MB12 (1) level is derived from the execution of an OPR

instruction containing a HLT microinstruction. The RUN flip-flop is cleared at time T5. The CP halts after time T7 of the same cycle.

The RUN flip-flop is set under the following conditions:

1. Depressing the START or CONTINUE key generates a negative START+CONT level (20), which is NAND combined in module J25 with the SP3 timing pulse. The positive pulse produced by the gate is applied to terminal H26S. where it triggers a DCD gate and sets the RUN flip-flop.

2. During a readin operation, a positive RPT (1) level conditions terminal H26V of a DCD set gate. The pulse input of this gate (H26U) is triggered when a RDR HOLE 7 level is NAND combined with timing pulse T5 of the cycle in which a hole 7 was detected. (A hole 7 indicates that the processor is to interpret and execute the last word read.)

I/O Pulse Generator

Timing pulses for the control of I/O devices are generated in modules K30 and K31 (A8, 22). Module K30 is a FLIP CHIP Type B115 containing three NAND gates; the output of each gate triggers an associated pulse amplifier in module K31 to produce a standard negative 40-nsec pulse. Any instruction of the IOT class generates a negative IOT level, which is applied to all three NAND gates. The subsequent generation of I/O pulses depends on the state of memory buffer bits MB15, MB16, and MB17. If bit MB15 is 1, an IOP 4 pulse is generated at time T1 of the computer cycle; if bit MB16 is 1, an IOP 2 pulse is generated at time T7; if bit MB17 is 1, an IOP 1 pulse is generated at time T5. These pulses are routed to the device selector; there they are combined with device selection levels to generate IOT command pulses that control the operation of the selected I/O device or trigger control gates in the CP.

Manual Controls (WD-D-7-0-37)

The manual controls provide means of energizing and de-energizing the computer; selecting modes of operation; manually inserting data into registers and core memory; and visually examining the status of the most important registers. Wiring connections to the keys and switches

on the operator console panel are shown on engineering drawing WD-D-7-0-37. The logic for gating signals produced by the keys and switches is shown on engineering drawing BS-D-7-0-20.

Interlock and POWER Switches - One deck of the key switch is connected in parallel with the POWER switch and is closed when the switch is in the locked position. Thus, with the key switch in the locked position, it is impossible to ruin a program because accidentally turning off the POWER switch does not interrupt the primary power circuits. To shut down the computer, the key switch must be placed in the unlocked position and the POWER switch in the off position. A second deck of the lock switch supplies either ground or −15v to the key and mode switches. In the locked position, the key switch grounds all key switches to disable them. thereby preventing accidental interference with a program that is running.

Key Circuits - When the computer is energized and the lock switch is in the unlocked position, operating any of the keys or turning on the SINGLE STEP, SINGLE INSTRUCTION, or REPEAT switches supplies −15v to a terminal on connector 2B29 or 2B32. The gating circuits shown on engineering drawing 20 combine key signals to generate various levels. These levels start the special pulse generator and condition control gates, as necessary, to cause the event sequences shown in the flow diagram included on the drawing.

Indicator Circuits - Indicators on the operator console are 28v incandescent lamps driven by Type 4903 Light Bracket Assemblies or Type 4904 Short Light Bracket Assembles. These assemblies contain a number of transistor switches, each connected between an indicator and ground. One side of each indicator is connected to the −15v supply. A common ground potential is connected to the emitter of each transistor through parallel-connected diodes, which provide the appropriate base-emitter bias. Each transistor switch is turned on by a negative signal level derived from a flip-flop and connected to the base through a resistor. When a flip-flop is in the 0 state, it supplies a ground potential that cuts off the transistor switch and extinguishes the associated indicator lamp. When a flip-flop is in the 1 state, it supplies a negative potential to the transistor switch; and the indicator lamp lights. The potential applied to a lighted indicator lamp is approximately 14v, which provides adequate visibility while ensuring very long lamp life.

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the AC contains a binary number, and the XOR transfer is followed by the propagation of carry pulses and then by an end-around carry of an overflow from bit AC0, the contents of the MB are added to the contents of the AC in 1's complement arithmetic. If the overflow from bit AC0 is set into the link instead of into bit AC17, then the contents of the MB are added to the contents of the AC in 2's complement arithmetic. The XOR → AC pulse is generated by any one of the following conditions:

1. An XOR pulse originating in the EAE is applied to terminal J3E (A6, 26) and initiates an XOR command.

2. During execution of any LAW instruction, a negative OP LAW level conditions AND gate MN of module J3. The gate is triggered by timing pulse T6 and initiates the XOR command.

3. During the execute cycle of a LAC, XOR, ADD, or TAD instruction, a negative E · IA1 level conditions AND gate HJ of module J3. The gate is triggered by timing pulse T3 and initiates an XOR command.

4. During the execute cycle of a SAD instruction, a negative E · SAD level is generated by combining the E level from the major state generator with the IA2 and IB3 levels from the IR decoder in NAND gate RSTU of module H12 (B1, 26). The output of the gate, inverted, is the E · SAD level and conditions AND gates PR and KL of module J3 (A5, 26). Gate KL is triggered by timing pulse T3 and initiates an XOR command; a second XOR command is initiated when gate PR in module J3 is triggered by timing pulse T6.

The AC CRY (AC carry) command pulse is generated by pulse is generated by pulse amplifier circuit FDEC in module H5. During the execute cycle of either a TAD or an ADD instruction, the E · TAD or E · ADD ground level is applied to NOR gate NPR of module J5 (B6, 26) to generate the E · TAD + ADD negative level. This level conditions NAND gate DEF of module J4. The gate is triggered by timing pulse T4, and the positive pulse appearing at terminal J4F triggers the pulse amplifier which generates the AC CRY pulse. The pulse amplifier may also be triggered by a positive EAE CRY pulse originating in the EAE.

The END CRY (end-around-carry) command is generated by pulse amplifier circuit FDEC in module H3 and causes an overflow from bit AC0 to be added to bit AC17, with further carry pulses as necessary. A negative E · ADD level conditions NAND gate TUV in module J4. If bit AC0 contained a 1 before the carry operation, and changes to 0 as the result of carry pulses from less significant bits, an AC0 CRY pulse is generated. This pulse, after inversion, triggers the pulse amplifier STU in module H8, and the output pulse from this amplifier triggers NAND gate TUV in module J4, thereby initiating generation of the END CRY pulse. The END CRY pulse complements bit AC17, further carry pulses being generated as necessary.

The TAD CRY (2's complement addition carry) command pulse is generated by pulse amplifier circuit RNPM in module H3. This pulse complements the link whenever one of the following conditions occurs:

1. An EAE CML (EAE complement link) command pulse originating in the EAE triggers the pulse amplifier that generates the TAD CRY pulse.

2. An OPR instruction, microprogrammed to complement the link, contains a 1 in bit 16. The MBB16 (1) level conditions NAND gate TUV in module J5 (B5, 26), and the gate is triggered by an OP 2 pulse. A TAD CRY pulse is then generated at time T7 of the computer cycle.

3. During the execute cycle of a TAD instruction, a negative E · TAD level conditions NAND gate NPR in module J4 (B6, 26). If the AC overflows, this gate is triggered by the AC0 CRY (B) pulse and initiates generation of the TAD CRY pulse.

The C → AC command pulse is generated by pulse amplifier circuit RNPM in module H5. This pulse complements each individual bit of the AC and occurs when an EAE CMA (EAE complement AC) command pulse, originating in the EAE, triggers the pulse amplifier. The C → AC pulse also occurs at time T7 during the execution of an OPR instruction which is microprogrammed for a CMA operation by the insertion of a 1 in bit 17. The MB17 (1) level conditions NAND gate JKL in module J4 (B6, 26), and the gate is triggered at time T7 by an OP 2 pulse. The OP 2 pulse is generated by NAND-combining the negative OPR level with timing pulse T7 in gate NPR of module J8 (C2, 26), and applying the resulting pulse to pulse amplifier LNM in module H8.

The RAR and RAL command pulses are generated at terminals N and D, respectively, of pulse amplifier module H4. Each of the two pulse amplifiers is triggered by a NAND gate, which is conditioned by an MBB13 (1) level (for RAR) or an MBB14 (1) level (for RAL). These gates are strobed by an AC ROTATE pulse at time T5 and initiate generation of the RAR or RAL pulse. If the instruction word contains a 1 in bit 7, the MBB7 (1) level conditions a NAND gate which is triggered by an OP 1 pulse at time T7 and produces an additional AC ROTATE pulse. Thus, one RAR or RAL pulse is generated at time T5 for a 1-place rotate operation; if a 2-place rotate is microprogrammed, a second RAR or RAL pulse occurs at time T7. Rotate command pulses originating in the EAE are applied to the input terminal of the RAR or RAL pulse amplifier (terminals H4R and H4F, respectively) and initiate generation of the RAR or RAL command pulses.

The MB0 → AC command pulse is generated by pulse amplifier circuit RNPM in module H6 and appears at terminal H6N. This command pulse causes MB bits in the 0 state to set the corresponding bits of the AC to the 0 state. During the execute cycle of a logical AND instruction, the E level from the major state generator is combined with the IA2 and IB2 levels from the IR decoder in NAND gate KLMN of module H12 (C1, 26) and produces a negative E · AND level. The E · AND level conditions NAND gate NPR in module J6 (C6, 26), which is triggered by timing pulse T5 and causes generation of the MB0 → AC pulse.

The ACS1 → AC command pulse is generated by pulse amplifier FDEC in module H6 and appears at terminal H6D. This command pulse causes the contents of the ACCUMULATOR switches on the console to be transferred into the AC. The ACS1 → AC pulse is generated at time SP2 of a DEPOSIT or DEPOSIT NEXT key cycle. This command pulse may also be generated during the execution of an OPR instruction containing a 1 in bit 15. The MBB15 (1) level conditions NAND gate JKL in module J6, and the gate is triggered by an OP 2 pulse at time T7, thereby causing generation of the ACS1 → AC pulse.

The ADD OV level is generated whenever the AC overflows during an ADD instruction. This level conditions a link input gate which is strobed by timing pulse TP1 of the following cycle and sets the link to 1 if there has been an overflow. The ADD OV level appears at the junction of terminals D7F, D7L, D8J, and D8E. All four of the inverters connected to these terminals must produce a negative output level for an ADD OV negative level to be established. The

posibility of an overflow is detected by applying the AC0 (0) status to NAND gate NPR in module D9 (B4, 26). If this bit contains a 0 after data has been XOR transferred to the AC, but before the carry pulses are generated, there is the possibility of an overflow. The gate is strobed by timing pulse T4 and, if bit AC0 contains a 0, the POV flip-flop is set. The buffered IR3 (0) level and the POV (1) level now fulfill two of the conditions for the production of an ADD OV level. However, the states of bit MB0 and bit AC0 must now be sensed to determine whether an overflow has in fact occurred. The comparison is made by the two NAND gates in module D7. If, after the carry, bit MB0 and bit AC0 both contain a 1, there has been transfer of a 1 with no overflow. Terminal D7L, therefore, remains at ground potential and prevents generation of a negative ADD OV level. Similarly, if bits MB0 and AC0 both contain a 0 after the carry, no transfer at all has taken place between these bits; and terminal D7F remains at ground potential. However, if bit MB0 contains a 1 and bit AC0 contains a 0 after the carry, an overflow has taken place. Both NAND gates are disabled under these conditions, and the ADD OV level is generated by a negative output level from all four inverters. The ADD OV level conditions a link input gate which is strobed by the following timing pulse TP1 and sets the link. A few nsec later, timing pulse T1 resets the POV flip-flop.

The OP SKP (operation skip) negative level is generated at terminal H10F and conditions a gate in the PC control that increments the contents of the PC when an OPR instruction contains any one of six possible skip microinstructions. The OP SKP level will be generated and the contents of the PC incremented at time T5 if any one of the following sets of conditions is fulfilled:

1. Bit 8 is 0, bit 9 is 1, link is set.
2. Bit 8 is 0, bit 10 is 1, contents of AC are zero.
3. Bit 8 is 0, bit 11 is 1, bit AC0 is 1 (sign negative).
4. Bit 8 is 1, bit 9 is 1, link is not set.
5. Bit 8 is 1, bit 9 is 1, contents of AC are not zero.
6. Bit 8 is 1, bit 9 is 1, bit AC0 is 0 (sign positive).

The AC=0 and AC≠0 levels are generated by the NAND gates contained in modules J8, J9, and J10 (A1, B1, 26), which sample the contents of each individual bit of the AC and give a ground level at terminal J10V if, and only if, all bits are 0.

Note that when more than one skip condition is specified in a single instruction, the combined skip condition is the inclusive OR of the individual conditions when bit 8 contains a 0. However, when bit 8 contains a 1, the combined skip condition is the AND of the individual conditions specified in bits 9 through 11.

Program Counter Register Control (25) - All of the command pulses which clear the PC, increment its contents, or cause a transfer of information into the PC from other registers are generated in the control logic circuits shown at the bottom right of engineering drawing 25. This logic element consists of six pulse amplifiers which generate the command pulses, together with diode gates and inverters which determine the conditions under which each pulse amplifier is triggered.

The pulse amplifier circuit FDEC at location D17 generates a 0 → PC command pulse which clears bits 5 through 17 of the PC. Bits 3 and 4 are used in conjunction with an extended memory and are cleared by a pulse from the Type 148 Extend Mode Control option. Bits 5 through 17 of the PC are cleared by any one of the following conditions:

1. At time SP1 of a key cycle, after operation of the START, EXAMINE, or DEPOSIT key

2. At time T5 of the fetch cycle of a JMP instruction, in preparation for the transfer of a new address from the MB

3. At time T3 of the execute cycle of a JMS instruction or at time T3 of a program break cycle

4. At time SP1 of a key cycle during a readin operation, provided that the RPT flip-flop is in the 0 state.

The pulse amplifier circuit RNPM at location D16 generates an AS1 → PC command pulse which causes the contents of the ADDRESS switch register to be transferred into the PC. The command pulse is generated by either of the following conditions:

1. At time SP2 of a key cycle, after operation of the START, EXAMINE, or DEPOSIT key

2. At time SP2 of a key cycle during a readin operation, provided that the RPT flip-flop is in the 0 state.

The pulse amplifier circuit FDEC at location D16 generates an MB1 PC command pulse which causes the contents of bits 5 through 17 of the MB to be transferred into the PC. Bits 3 and 4 receive a similar command pulse from the extend mode control. The MB1 → PC pulse is generated at time T6 of the fetch cycle of a JMP instruction; the information transferred is the address from which the next instruction is to be fetched.

The pulse amplifier circuit RNPM at location D17 generates the MA1 → PC command pulse at time T4 of the execute cycle of a JMS instruction, or at time T4 of a program break cycle. The contents of the MA are the address at which the current program count is to be deposited; this address is 0 for the program break.

The +1 → PC pulse increments the contents of the PC by 1 and is generated by two cascaded pulse amplifiers: FDCE at location J16 and SPNM at location F26. The second pulse amplifier introduces a delay of 20 nsec between the time at which the flip-flop outputs are sampled by the PC → MA pulse, and the time at which the contents of the PC are incremented during a fetch cycle. The gating associated with these two pulse amplifiers causes the incrementing pulse to be generated by new instructions and during skip, jump, and special mode operations. The incrementing pulse is generated in the following circumstances:

1. At time SP2 of a read paper tape operation

2. At time SP4, following operation of the EXAMINE or DEPOSIT key

3. At time T1 of a fetch cycle

4. At time T5 of the execute cycle of a SAD instruction if the contents of the AC are not 0. The E · SAD and AC≠0 levels which condition the NAND gate in module D14 are both generated in the AC control.

5. At time T5 of the execute cycle of a JMS instruction, or at time T5 of a program break cycle. The E · JMS component of the level which conditions

terminal E of module D12 is generated by the major state generator and IR decoder (24); the PROG · B component is generated in the interrupt control (32).

6. During the execute cycle of an ISZ instruction, at time T3, if a carry pulse is generated by bit MB0 of the MB, indicating that the contents of the MB are 0.

7. At time T5 of an OPR instruction microprogrammed for one of the six possible skip operations, if the conditions for the skip are fulfilled. The OP SKP (operation skip) level and the OP 1 pulse applied to terminals P and R of module D12 are both generated in the AC control.

8. At time T6 of a program break cycle after an illegal instruction is trapped, when the system is operation in the trap mode. The positive TRAP pulse that is applied directly to pulse amplifier input J16F is generated by a one-shot when the TRAP FLAG flip-flop is set.

9. During an I/O device identification operation, when the flag of the selected device is set.

Memory Address Register Control (25) - All of the command pulses which cause a flow of information into the MA are generated by the control circuits shown at the top right of engineering drawing 25. This control element consists of two Type B602 FLIP CHIP modules, each containing two 40-nsec pulse amplifiers; a Type B113 FLIP CHIP module containing four diode gates and associated inverters; and a Type B115 FLIP CHIP module containing three diode gates and associated inverters.

The pulse amplifier circuit RNPM at location A15 generates standard negative pulses which clear the entire MA under either of the following conditions:

1. At time SP1 of a key cycle after operation of any key except the STOP key.

2. At time T7 of each computer cycle, provided that the RUN flip-flop is in the 1 state. This action prepares the MA for the insertion of a new address at time T1 of the following cycle.

The pulse amplifier circuit RNPM at location A17 generates a PC1 → MA pulse which transfers information from the PC to the MA at time T1 of every fetch cycle. The address set into the MA by this action is that of the next instruction to be executed.

The pulse amplifier circuit FDEC at location A17 generates a MB1 → MA pulse which transfers information from bits 5 through 17 of the MB into the corresponding bits of the MA. The transfer occurs at time T1 of a defer or execute cycle, provided that the instruction below executed is not CAL (call subroutine). Either a D ground level at terminal A14D or an E ground level at terminal A14E conditions terminal A14L with a negative level. A negative $\overline{\text{CAL}}$ level derived from the MB control conditions terminal A14M. When timing pulse T1 reaches terminal A14K, the positive pulse which appears at terminal N triggers the MB1 → MA pulse amplifier.

The pulse amplifier circuit FDEC at location A15 generates a 20 → MA pulse which sets octal 20 into the MA during the defer or execute cycle of a CAL instruction. The NAND gate RSTU of module A14 is conditioned by a negative D or E level and by a negative CAL level derived from the MB control. When timing pulse T1 reaches terminal R, the positive pulse which appears at terminal U triggers the 20 → MA pulse amplifier.

Memory Buffer Register Control (25) - All the command pulses which clear the MB, increment its contents, and cause or inhibit a transfer of information into the MB are generated by the logic circuits shown at the left of engineering drawing 25. Four pulse amplifiers contained in two Type B602 FLIP CHIP modules and one Type B620 Pulse Amplifier generate command pulses. A Type B684 Bus Driver provides negative or ground levels, which condition or inhibit the gates connecting the MB to the memory sense amplifiers. Diode gates and inverters combine various levels and timing pulses to select the conditions under which each command pulse is generated.

The 0 → MB command pulse clears the entire MB register and is generated by the pulse amplifier circuit RNPM at location D1. This pulse amplifier is triggered by the BGN pulse of a key cycle, at time T2 of every computer cycle, and at time T7 of an execute cycle initated by a readin operation.

The Type B684 bus driver at location A10 produces a negative $\overline{\text{MB STB INH}}$ (not MB strobe inhibit) level continuously, thereby permitting the logic 1 pulses generated by core memory sense amplifiers to set the corresponding MB flip-flops during the read operation in every cycle. During certain operations, however, the contents of a memory cell are not transferred into the MB. For these operations, a ground MB STB INH level inhibits the gates between the sense amplifiers and the MB. Any one of the following conditions causes generation of the MB STB INH level:

1. During a program break cycle, the negative PROG · B level generated by the interrupt control is applied to terminal T of diode gate module H21 and is inverted.

2. A high-speed I/O device requesting a break cycle to deposit information in memory generates a negative DATA-IN level, which conditions terminal H21K. When the data break is granted, the negative DATA · B level produced by the interrupt control conditions H21J and causes the NAND gate to produce a ground level at the input of the bus driver.

3. During the execute cycle of a JMS or DZM instruction, the E level from the major state generator conditions terminal H21E; and the IA0 level produced by the IR decoder conditions terminal H21D. The NAND gate then produces a ground level output which is applied to the bus driver.

The +1 → MB command pulse increments the contents of the MB by 1 and is generated by two cascaded pulse amplifiers: FDEC of module C1 and EHD of module F26. These pulse amplifiers are triggered by any one of the following conditions:

1. Time T3 of a defer cycle, when the contents of the MA are one of the auto-indexing locations 10 through 17. All of these locations, but only these, are defined by a 0 in MA bits 5 through 13 and a 1 in bit 14. The MA5-13 (0) and MA14 (1) levels are combined in module D6 with the D level from the major state generator and condition input terminal P of a NAND gate in module D2. When timing pulse T3 is applied to terminal D2N, the gate is triggered, and its positive output pulse causes the pulse amplifiers to generate the +1 → MB pulse.

2. When a real-time clock is in use and is enabled by the program, the CLOCK · B level produced by the interrupt control when a clock break is granted conditions NAND gate JKL in module D2. Timing pulse T3 triggers the gate and causes generation of the +1 →MB pulse.

3. During the execute cycle of an ISZ instruction, the E level from the major state generator and the IA2 and IB1 levels produced by the IR decoder are NAND combined in module D5. The output of the gate is inverted and conditions NAND gate DEF in module D2. When timing pulse T3 is applied to terminal D2D, the gate is triggered and causes generation of the +1 → MB pulse.

The AC1 → MB command pulse is generated by pulse amplifier circuit RNPM of module C1 and causes the contents of the AC to be transferred into the MB. This command is generated only during the execute cycle of a DAC instruction. The E level from the major state generator is NAND combined in module D5 with the IA0 and IB1 levels produced by the IB decoder. The output of the gate is inverted and conditions NAND gate TUV in module D2. When timing pulse T3 is applied to terminal T, the gate is triggered and causes generation of the AC1 MB pulse.

The PC1→ MB command pulse is generated by pulse amplifier circuit FDEC in module D1 and causes the contents of the PC to be transferred into the MB. This command is generated by any one of the following conditions:

1. During a read paper tape operation, the RPT (1) level conditions NAND gate DEF in module D9. Timing pulse SP4 triggers the gate, and the positive pulse which appears at terminal F triggers the pulse amplifier.

2. During an examine or deposit operation, the EX+EXN+DP+DPN level generated by the key circuits conditions NAND gate JKL in module D3. Timing pulse SP3 of the key cycle triggers the gate and causes generation of the PC1→ MB pulse.

3. During a program break cycle or the execute cycle of a JMS instruction, the E · JMS+PROG·B level conditions NAND gate DEF of module D3.

Timing pulse T3 triggers the gate and causes generation of the PC1→MB pulse. The derivation of the conditioning level was explained in condition 5 for the +1→PC pulse (PC control).

I/O Skip Control and I/O Trap

I/O Skip Control (32) - The I/O skip control element provides a means of skipping an instruction as a function of the performance of an IOT instruction microprogrammed to sense the state of a device flag. The flag sensing gates are shown at the botton right of engineering drawing 32. Each of the diode gates contained in modules L13 and M13 is conditioned by a negative level generated by the flag of the associated device. The gate is strobed by an IOT command pulse generated in the device selector; and, if the device flag is set, an IO SKP pulse is generated, which causes the contents of the PC to be incremented by 1. (Refer to the description of the PC control and engineering drawing 25.) The IOT command pulse occurs at time T5 and is generated by combining the device selection signal decoded from bits MB6 through MB11 with an I/OP 1 pulse initiated by a 1 in bit MB15.

I/O Trap (23) - The I/O trap permits time-sharing of the processor by two programs running in different memory fields by ensuring that instructions which would halt the machine, or would cause interference between the two programs, are not executed. Specifically, the I/O trap monitors the program for IOT instructions, for XCT instructions whose subject instruction is also an XCT (such instructions could put the machine into a loop from which it could not escape), and for instructions of the operate class containing a microprogrammed HLT command. Whenever one ot these illegal instructions is detected by the trap, a program break is substituted for the trapped instruction. The contents of the PC, together with the status of the link, the extend flag, and the trap flag, are stored in location 0. Control of the CP then transfers to location 2, and the subsequent sequence of events depends on the nature of the trapped instruction.

To enable the trap mode, the I/O TRAP flip-flop (B5, 23) is set by NAND-combining a negative I/O TRAP SW level, a negative trap enable level (MB12 (1) · MB13 (1)), and a negative IOT 0002 command pulse. The I/O TRAP (1) level conditions the various gates which detect conditions requiring that the TRAP FLAG flip-flop be set.

The TRAP FLAG flip-flop is set when the I/O TRAP flip-flop is set and any one of the following sets of conditions occurs:

1. Any IOT instruction is detected. The minor states IA3·IB2 are produced by all IOT instructions and are NAND combined in module J23 (C4, 23) with the I/O TRAP (1) level. Timing pulse T3 strobes this gate to produce a positive output pulse, which sets the TRAP FLAG flip-flop.

2. A microprogrammed HLT command is detected. The HLT command is generated by an OP1 pulse in combination with an MB12 (1) level; both these signals are NAND combined in module J24 (B5, 23) with the I/O TRAP (1) level. The gate produces a positive ILL HLT pulse which sets the TRAP FLAG flip-flop.

3. If an execute (E) state is set into the major state generator, and the IR contains the operation code for execute, an E · XCT level is produced. This level is NAND combined with timing pulse T2 in module L24 (C8, 23), thereby setting the SCT CY flip-flop to 1. The SCT CY (1) level is NAND combined in module H24 (B8, 23) with the I/O TRAP (1) level, and with the IA2 and IB0 minor state levels produced by the IR. Timing pulse T2 strobes the gate to produce a positive ILL XCT pulse which sets the TRAP FLAG flip-flop. The XCT CY flip-flop is reset to 0 by timing pulse TP7 of the same memory cycle.

The setting of the TRAP FLAG flip-flop produces a negative TRAP FLAG (1) level, which is applied to the program interrupt control and generates a PROG RQ level. (For details of how this level causes a program break, refer to the discussion of the program interrupt control, below.) When a program break is granted by the break control, a PROG · B level is generated. This level is NAND combined with timing pulse T4 of the break cycle in modules J22 and K19 to reset the TRAP FLAG and I/O TRAP flip-flops, respectively.

The resetting of the TRAP FLAG flip-flop generates a positive-going level transition at its output terminal E; this transition triggers the one-shot in module L32 (B3, 23) into its astable state. The negative level which then appears at output terminal M of the one-shot increments the contents of the PC at time T6 of the break cycle.

Break Control (32)

The break control contains all the logic elements required for causing an interruption of the main program to permit an external or auxiliary device to be serviced, and for returning to the program sequence when the servicing operation has been completed. The break control provides for the following three distinct classes of interruption:

1. A data channel break, which lasts for one computer cycle and permits an exchange of information between the central processor and a high-speed I/O device capable of transferring 15 address bits and 18 data bits in parallel.

2. A clock channel break, which also lasts for one computer cycle and permits a real-time clock to add 1 to the contents of memory location 7_8.

3. A program break, which stores the current program count in memory location 0 and initiates a subroutine (beginning in location 1) to find and service a slow I/O device which has requested a break. In the following discussion of the break control, component and signal references are to engineering logic diagram 32, unless otherwise stated.

Data Channel Control - A data break request, since the break never lasts for more than one computer cycle, takes priority over all other forms of break request. A high-speed I/O device may originate a data break request by placing a −3v DATA RQ level on the request line connecting the device to the computer. In the interrupt control, the DATA RQ level is NAND combined with timing pulse T5 (DLY) of a current computer cycle; and the resulting positive pulse sets the DATA SYNC flip-flop (A1, 32) to 1. The positive DATA SYNC (1) output of the flip-flop is NOR combined with similar levels from the CLOCK SYNC and PROG SYNC flip-flops. If any one of these flip-flops is set to 1, a negative BK RQ level appears at terminal L15J (A8, 32) and is transmitted to the major state generator. Completion of the current instruction permits the major state generator to produce a negative B (break) level which is applied to the interrupt control. The B level is NAND combined with the DATA SYNC (1) level to produce a negative DATA · B level at terminal L23J (A2, 32). At time T1 of the break cycle, the DATA · B level is NAND combined with timing pulse T1 to produce a DATA ADDR→MA pulse at terminal L16H (C1, 32). This pulse causes the memory address contained

in the address register of the I/O device to be transferred into the CP memory address register. At time T3, the DATA · B level is NAND combined with timing pulse T3 to produce a negative MB INFO →OUT pulse at terminal L16U. This pulse indicates to the I/O device that information for outward transfer is available in the memory buffer. If the requesting device is transmitting a negative DATA IN level, this is NAND combined with DATA·B and T3 to produce a negative DATA INFO→ MB pulse at terminal L16N (C1, 32). This pulse opens the data channel interrupt input gates of the memory buffer. During the remaining portion of the break cycle, the memory performs a normal write operation, depositing the received information (or rewriting the transmitted information) in memory. If the device has no further information to transmit or accept, the DATA RQ line goes to ground level. This $\overline{\text{DATA RQ}}$ ground level is inverted and combined with the T5 DLY pulse in NAND gate NPR of module L17 to reset the DATA SYNC flip-flop to 0. As a result, a $\overline{\text{BK RQ}}$ negative level is applied to the major state generator and permits it to enter the fetch state so that the main program can continue.

Clock Channel Control - The real-time clock consists of a Schmitt trigger (Type W501 FLIP CHIP module) which produces square pulses when fed from a source of 6.3v, 60 cps. The output pulses of the Schmitt trigger are applied to the pulse amplifier in location L25, which produces standard 70-nsec negative pulses (B3, 32). The clock is enabled by a CLON instruction (700044_8); the device selector decodes the instruction and produces an IOT 0004 pulse which clears the CLK FLAG flip-flop. This pulse is NAND combined with MB12 (1) to set the CLOCK ENABLE flip-flop to 1. The next clock pulse is NAND combined with the CLOCK ENABLE (1) level and sets the CLK COUNT RQ flip-flop. Timing pulse T5 of the current cycle, delayed by 50 nsec, is NAND combined with the CLK COUNT RQ (1) level and sets the CLK SYNC flip-flop. The CLK SYNC (1) level is applied to module L22 and generates a BK RQ level that initiates a break cycle at the earliest opportunity. If no data break is in progress, the CLK SYNC (1) and B levels are NAND combined to produce a CLOCK·B level at terminal L23M (A3, 32). At time T1 of the clock break cycle, the CLOCK·B level is combined with timing pulse T1 in NAND gate DEF of module 1L24 (B1, 32). The output of the gate triggers a pulse amplifier which generates a 7 →MA negative pulse. This pulse clears the CLK COUNT RQ flip-flop and sets bits MA15, MA16, and MA17 to 1, thereby addressing location 7 of the memory. At time T3 of the break cycle, the CLOCK·B is NAND combined with the timing pulse T3 to produce a +1→ MB pulse (MB control, 25). If the resulting increment causes the

memory buffer to overflow, an MBO CRY pulse is generated (30) and is combined with the CLOCK·B level (C2, 32) to set the CLK FLAG flip-flop to 1. The setting of the CLOCK FLAG flip-flop is one of the conditions which can cause a program break, as described below. If there is no overflow and the clock flag is not set, timing pulse T5 of the break cycle (delayed by 50 nsec) is combined with the CLK COUNT RQ (0) level to clear the CLK SYNC flip-flop. During the remaining portion of the clock break, the incremented contents of the memory buffer are written into memory location 7. If no other break request has been originated before time T5, the major state generator is set to fetch at time T5, and the processor continues the main program. However, while the CLK ENABLE flip-flop remains set, a clock break will occur every 1/60 sec. A CLOF instruction (700004_8) is required in order to disable the clock; the IOT 0004 pulse clears the CLK FLAG flip-flop and is combined with the MB12 (0) level to clear the CLK ENABLE flip-flop.

Note that when the Type 172 Automatic Priority Control (API) option is included in the system, it replaces the standard real-time clock. The real-time clock and the associated CLK ENABLE and CLK FLAG flip-flops are removed, since the API contains corresponding logic. The negative INT RQ level from the API is connected to terminal E of the CLK COUNT RQ flip-flop; and the same level, inverted in module J20, is connected to terminal F.

Program Break Control - A program break may be initiated by the Teletype, the punch, the tape reader, and other slow-speed peripheral equipment. The break may be requested whenever the setting of the associated flag indicates that a device is ready for an information transfer, or the status of the device requires some other kind of action. The setting of the real-time clock flag (indicating that the contents of memory location 7 have overflowed) or the trap flag (indicating that an illegal instruction has been trapped) can also initiate a program break. However, the program interrupt control (PIC) may be disabled by the program to delay the granting of a program break until a particular sequence of operations has been completed.

The PIC is enabled by an ION instruction (700042_8). The device selector decodes the instruction to produce an IOT 0002 pulse. This is combined in NAND gate TUV of module L21 (B4, 32) with the MB12 (1) level, and sets the PIE (program interrupt enable) flip-flop. Similarly, an IOF instruction (700002_8) clears the PIE flip-flop. The (1) level of any device flag which has been set enters the interrupt control through one of the 7-channel gates in locations L14

and M14. Providing that the PIE flip-flop has been set and that the major state generator is not already in a break state, the flag generates a PROG·RQ level (FLAG·PIE (1) $\overline{B}$ = PROG RQ, see A8, 32).

At time T5 of the current cycle, the PROG RQ level is NAND combined with timing pulse T5 DLY and sets the PROG SYNC flip-flop. The setting of this flip-flop produces a negative BK RQ level which is applied to the major state generator. When the CP reaches an "instruction done" situation, the major state generator establishes a break state, and the B (break) level is combined with the PROG SYNC (1) level. Provided that neither a data break nor a clock break has been requested in the meantime, a negative PROG·B level appears at terminal L23U (A5, 32). The PROG·B level is used in the I/O trap logic and, at time T5, is combined with the T5 timing pulse to reset the PIE flip-flop. The PIE (0) level, inverted, clears the PROG SYNC flip-flop. Since the PIE flip-flop can only be set to 1 by another ION instruction, a second level of interrupt is prevented. The flow diagram (21) shows the complete sequence of events which takes place during the break cycle of a program break.

INTERFACE

All information transfers between the CP and I/O equipment (other than devices which use the data break facility) take place under program control by way of the interface equipment and the accumulator register. Selection of an I/O device and generation of control pulses takes place in the interface logic. Gating circuits to control information flow are located at the input of the receiving register. The interface logic consists of three elements:

1. A device selector which decodes the IOT instruction to be executed, addresses the appropriate I/O device, and generates up to three IOT command pulses for control purposes.

2. An information collector which gates incoming information into the accumulator register.

3. An information distributor, consisting of bus drivers capable of driving an output bus system through which information is transferred from the accumulator register to I/O devices.

Device Selector (36)

The device selector (engineering drawing 36) contains a decoder module, a gate module, and a pulse amplifier module for each I/O device. In the standard PDP-7 system, 20 sets of device selector equipment are supplied, of which 6 are unassigned. The decoder module decodes bits MB6 through MB11 of an IOT instruction word held in the MB and produces a ground device-enabling level and a negative gating level. The negative level enables the gates of the associated gating module which route any IOP pulses generated to the addressed device. The positive pulse which appears at the output of each gate is applied to a pulse amplifier which generates a standard 70-nsec command pulse for controlling the operation of the addressed device. The following discussion of the device selector is based on Figure 3-2, which shows the logic of the selection equipment associated with one I/O device.

The decoder consists of a Type B171 FLIP CHIP Diode Gate containing twelve diode inputs and two inverters. The input terminals of the module are connected to the bus drivers associated with the (1) and (0) levels of memory buffer bits MB6 through MB11. A device assertion level is obtained by clipping out diodes associated with unasserted levels of the selection code (e.g., if the selection code were 010101, the diodes removed would be the (1) level diodes of bits MB6, MB8, and MB10, and the (0) level diodes of bits MB7, MB9, and MB11). The positive assertion level for the selected device appears at terminal D of the decoder module, and may be routed to the device for enabling purposes. The negative level appearing at terminal E is applied to the gating module.

The gating module consists of a Type R111 FLIP CHIP Diode Gate containing three inverters, each having two diode inputs. The negative assertion level for the device enables one input of each of the inverters; the second input of each inverter is connected to one IOP timing pulse bus. An IOP1 pulse appears at time T5 of the computer cycle in which the IOT instruction is executed, if bit 17 of the instruction word contains a 1; an IOP2 pulse appears at time T7 of the same cycle, if bit MB16 contains a 1; and an IOP4 pulse appears at time T1 of the following computer cycle if bit MB15 of the instruction word contains a 1. The selection of a device causes any IOP pulses generated to be applied to the pulse amplifer module of the corresponding device selector channel.

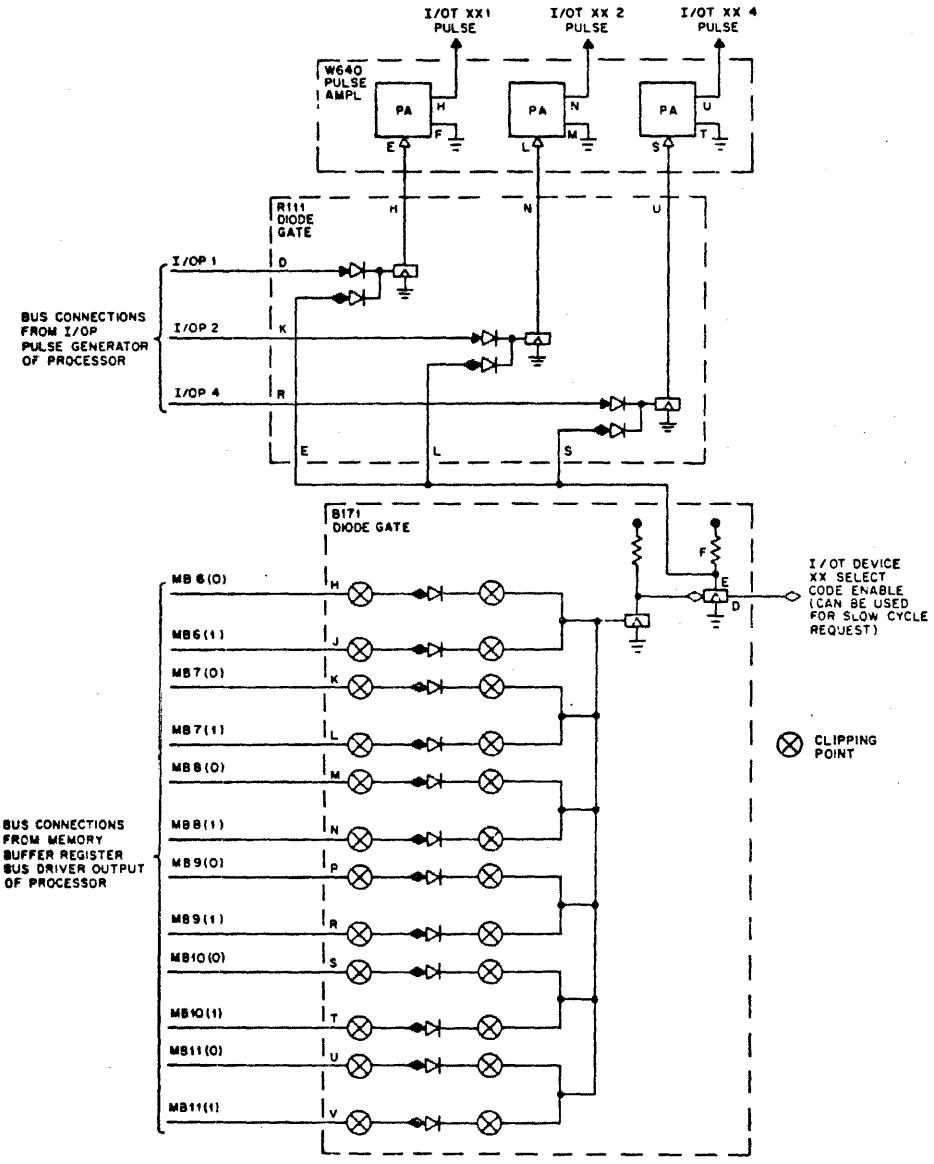


Figure 3-2 Device Selector Logic Diagram

Positive pulses from the gating module of a selected device are applied to corresponding pulse amplifiers contained in a Type W607 or Type W640 FLIP CHIP module. The pulse amplifiers of a Type W607 module produce standard −2.5v, 70-nsec output pulses. Those of a Type W640 module normally produce a −2.5v, 400-nsec pulse, but by jumpering the appropriate terminals on the module, the pulse length can be extended to 1 μsec if the nature of the I/O device requires it. Each module contains three pulse amplifiers. One of these, triggered by an IOP1 pulse, produces an IOT XX01 pulse (where XX is the device number), which may be used to sense the status of a device flag. The second, triggered by an IOP2 pulse, produces an IOT XX02 pulse which may be used to clear the device flag and read the contents of the device buffer register into the accumulator register. The third pulse amplifier, triggered by an IOP4 pulse, produces an IOT XX04 pulse which may be used to transfer data from the accumulator register through the information distributor into the device buffer. All three pulses may also be used to initiate control functions within the selected device.

Information Collector (33)

The information collector consists of 18 7-channel NAND gates Type R141, each of which is associated with one bit of the AC. Each channel has an upper half and a lower half corresponding, respectively, to bits 0-8 and 9-17 of the AC. If an I/O device occupies only one-half of a channel, the other half may be used for other purposes. From engineering drawing 32 it will be seen that in the basic PDP-7 system, the paper tape reader occupies the whole of channel 1; the associated gates are strobed by an IOT command pulse 0102 generated in the device selector. The status register (for flag monitoring) occupies the upper half of channel 2; the lower half of this channel is not used. The MQ register of the EAE occupies all of channel 3; the Teletype LUO occupies the lower half of channel 6; and the EAE step counter occupies the lower half of channel 7. Provision is made to accommodate an optional DECtape machine on channel 4, a magnetic drum device on channel 5, and tape status and drum status signals in the upper halves of channels 6 and 7, respectively. The information collector can be expanded almost indefinitely by adding gate modules. The first expansion, which adds six channels, requires 18 Type R141 Diode Gate modules and 6 Type W607 Pulse Amplifier modules. Additional expansions, in increments of six channels, require only Type 141 Gate modules.

Information Distributor (34)

The information distributor of the basic PDP-7 system consists of 9 Type R650 Bus Drivers and 16 Type W021 Cable Connectors to distribute the bus driver output signals. Note that each Type R650 module contains two inverters and two bus drivers. Negative logic 1 assertion levels from the AC appear as ground logic 1 assertion levels on the distribution buses. The information distribution can be expanded almost indefinitely by adding W021 Connectors, with additional bus drivers if the maximum load (5 ma) on the standard drivers is likely to be exceeded.

MB Bus Drivers (28)

The 1 and 0 levels of the MB flip-flops are available for distribution within the CP and to external devices connected to the data channel. Nine Type B684 FLIP CHIP Bus Driver modules are used for the 1 levels, and nine for the 0 levels. Each module contains two bus drivers, and each bus driver can supply up to 40 ma of load.

CHAPTER 4

CORE MEMORY

Data and instruction storage and retrieval are performed in the PDP-7 by the core memory. The standard PDP-7 is equipped with a DEC Type 149A Memory Module which can store 4096 18-bit words and which requires a 12-bit address. The addition of a DEC Type 147 Core Memory Module expands the memory capacity of the Type 149A Memory Module of the standard PDP-7 to 8192 words. No auxiliary equipment is required since the extra address bit required for selecting addresses in either 4K memory array is provided by the existing 15-bit memory address register (MA). Memory capacity can be further expanded by increments of 4096 or 8192 words to a maximum of 32,768 words. Expansion beyond 8K requires the use of a DEC Type 148 Memory Extension Control and of the remaining two bits of the MA. All information enters and leaves core memory via an input/output register designated the memory buffer register (MB). This manual describes the operation of the 8K memory; the basic principles and methods of access to this memory are equally applicable to larger or smaller capacities. For information on methods of accessing extended memories, refer to the maintenance manual for the Type 148 Memory Extension Control.

MEMORY ORGANIZATION

Each 4K core memory module used in the PDP-7 is a simple, coincident-current, ferrite-core array assembled from core planes 64 cores wide by 64 cores deep. Each module is operated by read, write, and inhibit currents originating in transistor power supplies and gating circuits. Figure 4-1 shows the interrelationship of the elements which constitute the core memory system. The MA and MB are located in the central processor (CP). Timing signals which control memory functions are derived from the CP timing signal generator in order to synchronize memory operations with CP operations. The memory cycles continuously perform a read operation during time states T2 and T3 and a write operation during time states T5 and T6. This permits random bidirectional access to any memory cell within one 1.75-μsec computer cycle. Both reading and writing operations are performed during each cycle, since reading from a memory cell destroys the content. Thus, if the information is not to be lost, it must immediately

be rewritten into the same cell from the MB. The only exceptions to this rule occur during a data break in which the direction of transfer is into the computer core memory and during the execution of DAC, JMS, or DZM instructions.

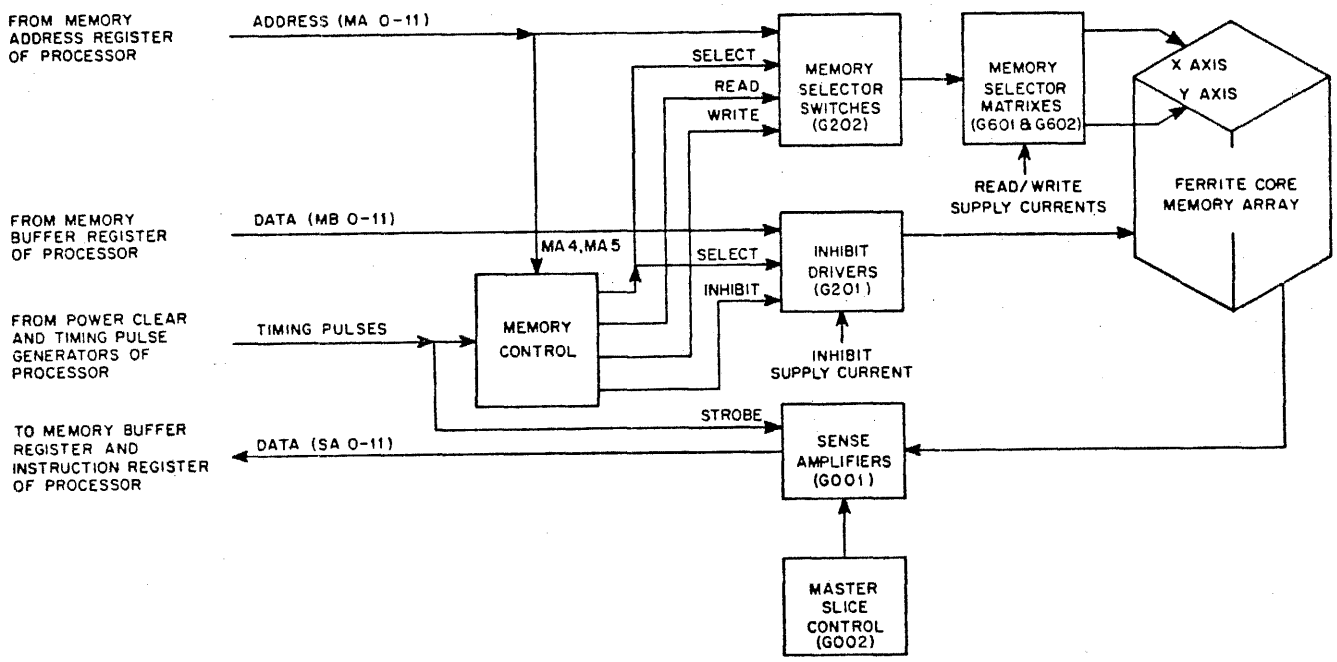


Figure 4-1 Core Memory System Block Diagram

CIRCUIT OPERATIONS

Ferrite-Core Memory Array

The standard memory array consists of 18 planes, each having 4096 ferrite cores arranged in a 64 by 64 square. Each core can assume one of two stable magnetic states corresponding to binary 1 and binary 0. Each core is traversed by four windings. An X read/write winding passes through all the cores in one horizontal row; a Y read/write winding passes through all the cores in one vertical row; the sense and inhibit windings each pass through all the cores in the plane. An example of this winding is in Figure 4-2 for a 4 by 4 core plane. In Figure 4-2, passing a current from right to left (write direction) of the diagram through the X2 winding

produces a magnetic field that tends to change all the cores in that row from the 0 to the 1 state. Passing a current from bottom to top of the diagram through the Y3 winding produces a similar effect on the cores in that row. Neither the X current nor the Y current is, by itself, strong enough to change the state of any core. However, if both X2 and Y3 currents are turned on, the magnetic fields due to the two currents are mutually reinforcing in one core through which both windings pass. The combined strength of both fields causes this, and only this, core (in each plane) to change state to the 1 condition. In the PDP-7 system, an array consists of 18 planes, with all the corresponding address windings connected in common so that each plane can be considered equivalent to one bit of a storage cell. Thus, in the previous example, the core located at coordinates X2Y3 on each plane will change to the 1 condition unless it is prevented from doing so by an inhibit current.

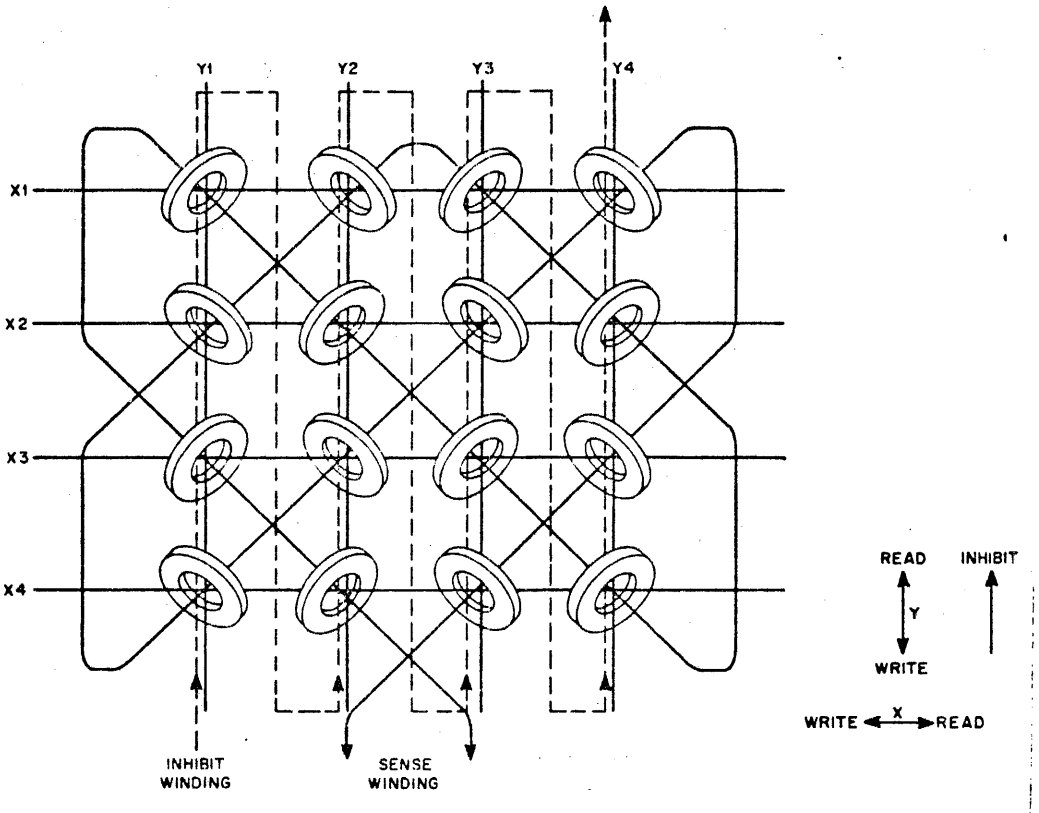


Figure 4-2 Simple Core Memory Plane Showing Read/Write, Sense, and Inhibit Windings

If the storage cell consisting of X2Y3 cores is to contain 0's as well as 1's, the cores in the planes which correspond to 0 bits must be prevented from changing state when the writing currents are turned on. This is accomplished by passing a current through the inhibit windings of those planes. The magnetic field due to the inhibit current has a direction and amplitude which partially cancels the fields due to the writing currents. Thus, even though both X and Y writing currents are present in all the X2Y3 cores, those cores in planes where an inhibit is also present will remain in the 0 condition. After setting or resetting cores, all of the read/write and inhibit currents are turned off without affecting the state of any cores.

To read the information stored in the X2Y3 cell, currents must be passed through all the X2 and Y3 windings in the opposite direction, thereby tending to change all the X2Y3 cores to the 0 condition. Cores X2Y2 of all planes which were inhibited during writing, and are thus already in the 0 state, induct only a very small signal into the sense windings. However, X2Y3 cores which were in the 1 state will change back to the 0 state when both the X2 and the Y3 read currents are turned on. The resulting flux change will induce a relatively large signal into the associated sense windings. After amplification, these binary 1 signals complete the information transfer by setting the corresponding MB flip-flops.

Memory Selectors Type G202 and Memory Selector Matrixes Types G601 and G602

The memory selectors decode the information contained in the MA and perform memory cell selection; the memory matrixes, controlled by the memory selectors, route read and write current pulses to the selected memory cell. In each memory array, address bits MA6 through MA11 select read and write lines in the matrix of the Y axis; bits MA12 through MA18 select read and write lines in the matrix of the X axis. Drawing E-149-0-49 shows the circuits for Y axis selection. Note that address bits MA6 through MA8 are decoded by the four Memory Selector Type G202 modules shown at the left of the diagram and known as drive selectors. Address bits MA9 through MA11 are decoded by the four G202 modules shown at the bottom of the diagram and known as ground selectors. The selector modules provide pulses to open gates in the Memory Selector Matrix Type G601 and G602 modules. A similar arrangement of memory selectors and memory selector matrix modules provides selection of read/write lines

on the X axis, as shown in drawing E-149-0-48. A schematic diagram of a memory selector is contained in drawing RS-B-G202. Schematic diagrams of the matrixes are contained in drawings RS-D-G601 and RS-D-G602.

The following discussion of the core selection process is based on the simplified schematic diagram of Figure 4-3. This diagram shows the logic switching circuits involved in the generation of read and write currents for cell 46 on the Y axis. When cell Y46 is to be read, the address set into the MA contains MA6(1), MA7 (0), MA8 (0), MA10 (1), and MA11 (0) which are applied as negative assertion levels to the selector module. Negated ground levels corresponding to $\overline{\text{MA8 (1)}}$ and $\overline{\text{MA11 (1)}}$ are also applied to the selector modules. The MA6 (1) and MA7 (0) negative levels enable transistor switches Q4 and Q5, respectively, of the drive selector module at location A10; similarly, the MA9 (1) and MA10 (1) levels enable transistor switches Q4 and Q5 of the ground selector module at location A13. The MA8 (0) and MA11 (0) levels are both negative, thereby enabling transistor switch Q7 in both modules. Transistor switch Q2 in each module is disabled by a negated ground level corresponding to $\overline{\text{MA8 (1)}}$ and $\overline{\text{MA11 (1)}}$. These levels are established as soon as the cell address is loaded into the MA during time state T1 of the computer cycle.

At time T2, timing pulse TP2 sets the READ 2 flip-flops (Figure 4-4). The setting of the READ 1 flip-flop, in combination with the state of the field select bits MA4 and MA5, causes a SEL 1 · READ 1 level to be applied to the G202 Pulser Selector, which in turn applies a pulse to the read pulser, thereby connecting read drive bus 4 to the positive supply. Simultaneously, the READ 2 (1) level enables transistor switch Q4 in both drive and ground selectors. The surge of current through the transistors causes pulses to be generated which open pulse gates PG1 and PG4. A read half-select current then flows from the read/write memory current supply through the read pulser, pulse gate PG1, diode D1, the cores of cell Y46, diode D3, and pulse gate PG4 to the read/write common negative line. This half-select read current is factory adjusted to approximately 330 ma. At time T3, the READ flip-flops are both cleared in preparation for a write operation.

At time T4, timing pulse TP4 sets the WRITE 1 and WRITE 2 flip-flops, thereby enabling the write pulser and transistor switch Q8 in the drive and ground selector modules. The resulting pulses connect write drive bus 4 to the positive read/write current supply and opens pulse gates

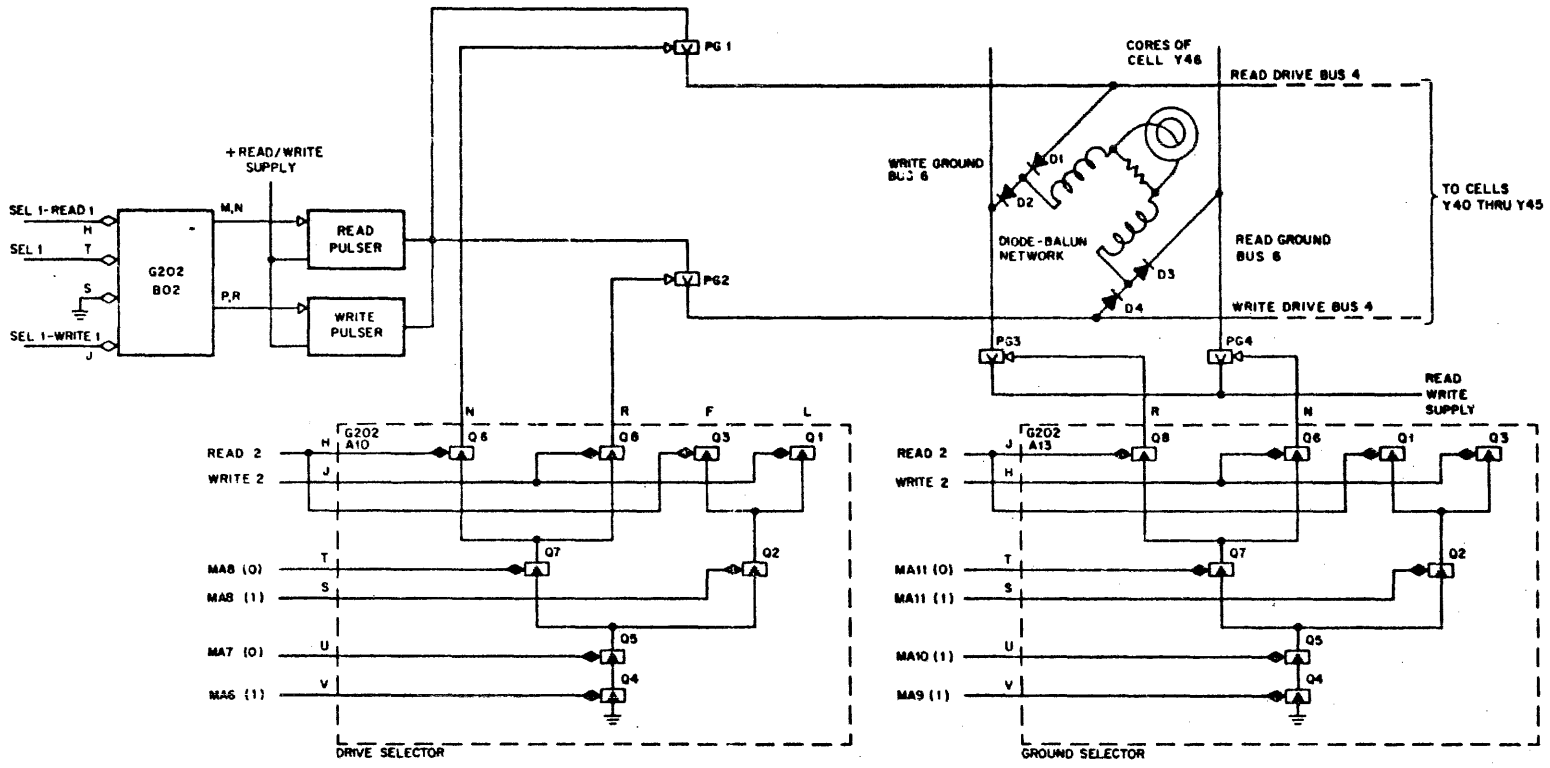


Figure 4-3 Typical Core Selection Circuit and Drive Current Path

PG2 and PG3. A write half-select current then flows from the supply, through pulse gate PG2, diode D4, the drive lines of the cores of cell Y46 (in the opposite direction to the read pulse), diode D2, and pulse gate PG3 to the read/write common negative line.

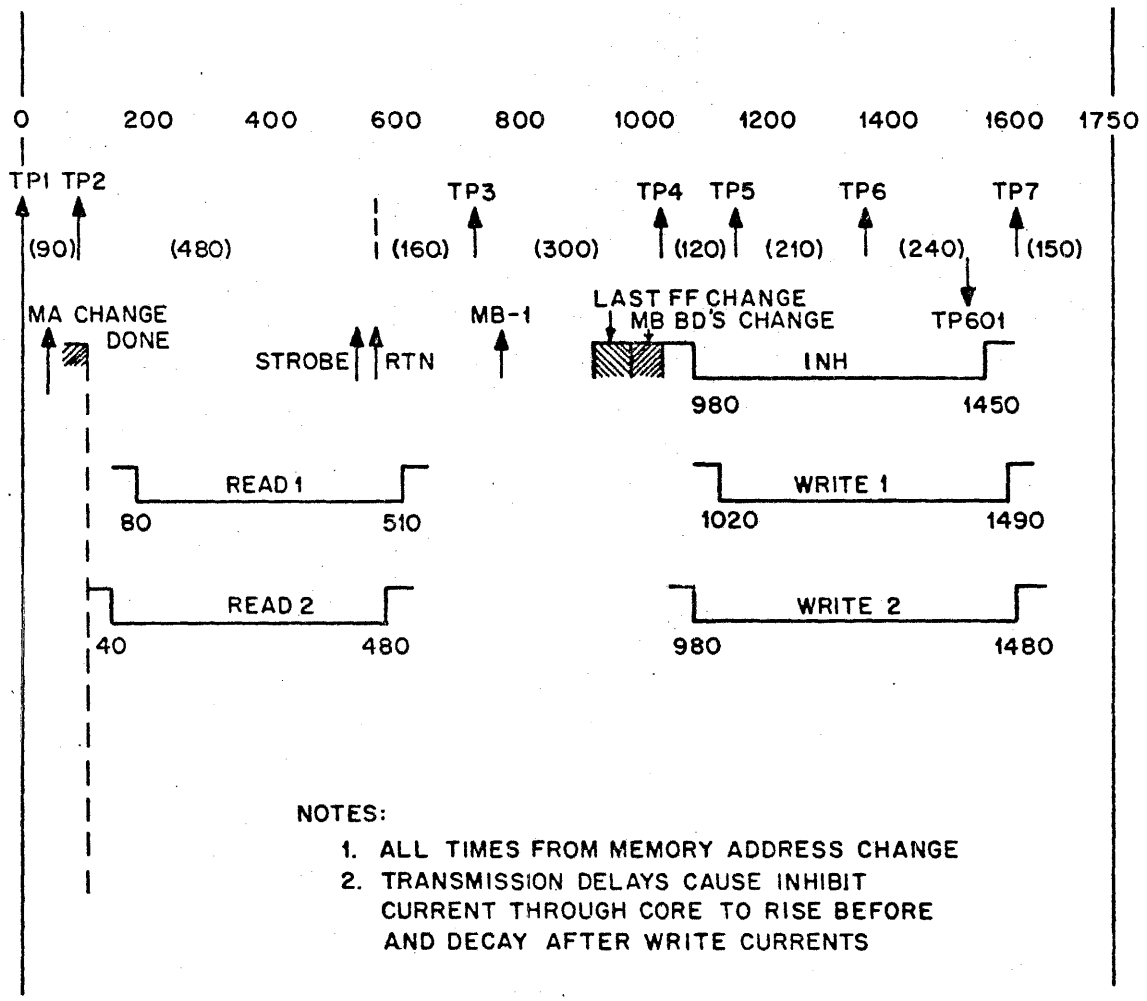


Figure 4-4 Memory Control Timing

Inhibit Drivers Type G201

The PDP-7 memory is wired for 19 Inhibit Driver modules Type G201. Each of these modules energizes the inhibit winding of one memory plane. Note, however, that the 19th plane is not used in the PDP-7 system unless the Type 176 Parity Checking option is in use, in which case a 19th plane and an inhibit driver module are added and used for a parity bit. A schematic diagram of an inhibit driver is shown in drawing RS-B-G201, and the connection of the inhibit drivers in the memory system is shown in engineering logic diagram BS-E-149-0-45. Figure 4-5 shows the internal logic circuits of an inhibit driver. A negative INH B level is applied to the module at terminals F and J and is NAND combined with the negative 0 level of the associated MB bit in transistor switches Q5 and Q2. The combined signal output of transistor switch Q5 enables pulse gate 1, which provides the principle on/off switching for the inhibit current. The INH B · MB (0) signal and the appropriate array SEL signal are NAND combined in transistor gate Q2 or Q3. If a negative SEL 0 level is present, transistor Q3 conducts and enables pulse gate 2, thereby routing the inhibit current into the inhibit winding associated with bit X of memory array 0. If a negative SEL 1 level is applied to transistor gate Q4, pulse gate 3 is enabled and routes the inhibit current into the corresponding bit inhibit winding of memory array 1. The memory control logic ensures that SEL 0 and SEL 1 levels can never be applied simultaneously. Inhibit current is applied to the inhibit winding of the cores through a balun which balances the winding with respect to ground, thereby minimizing the effects of stray capacitance and permitting increased operational speeds in the memory. Each Type G201 Inhibit Driver can sustain a current of 350 ma for 500 nsec; however, in the PDP-7 system, the inhibit current is normally set at approximately 290 ma.

Sense Amplifiers Type G001 and Master Slice Control Type G002

The PDP-7 memory contains 19 Sense Amplifier modules Type G001 and one Master Slice Control module Type G002. Eighteen of the sense amplifiers supply a standard negative pulse to the MB when an associated core changes from the 1 state to the 0 state during a read operation. The 19th sense amplifier provides a parity bit when the Type 176 Parity Checking option is in use. The master slice control supplies all the sense amplifiers with closely controlled reference

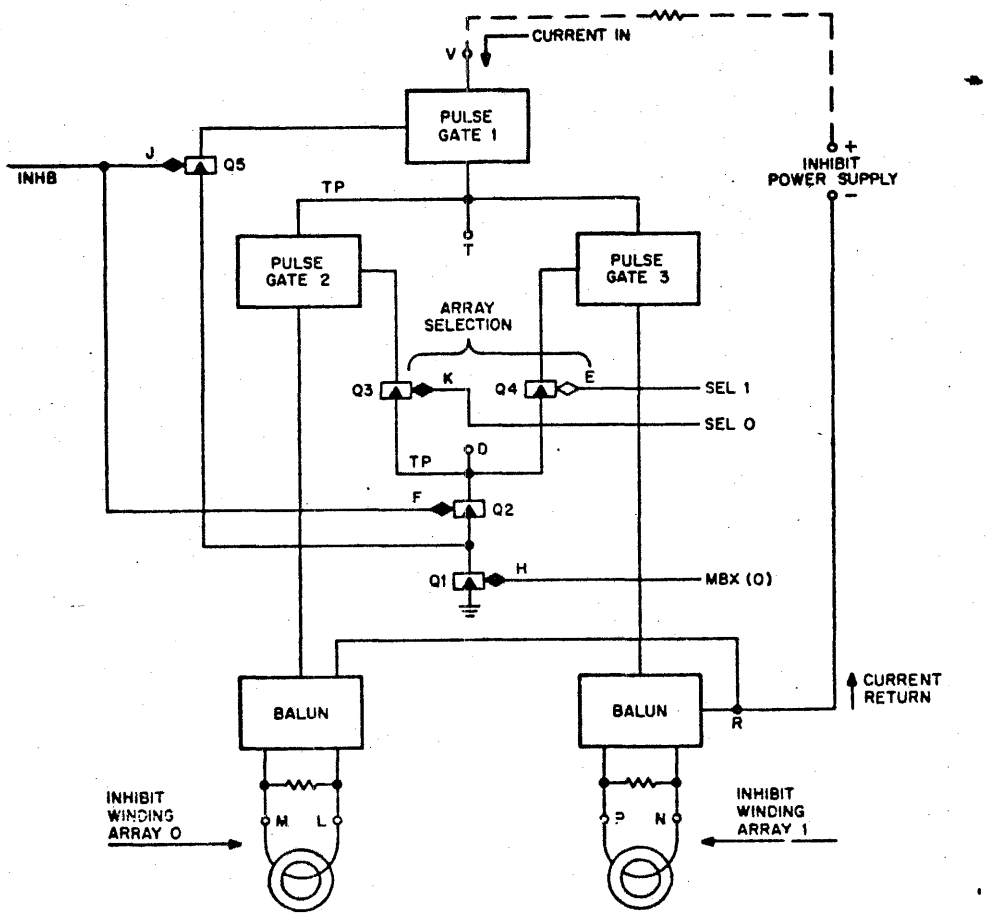


Figure 4-5 Inhibit Logic for One Memory Cell

voltages for use in clamping and comparator stages. Drawings RS-B-G001 and RS-B-G002 contain schematic diagrams of the sense amplifier and the master slice control, respectively. The connection of these modules in the memory system is shown in drawing BS-E-149-0-45.

Each sense amplifier contains a 2-stage dc preamplifier, a rectifying slicer, an output gate, and a pulse amplifier. The first stage of the dc preamplifier has two separate gated difference amplifiers, which share a common push-pull output stage. One input difference amplifier accepts a pulse input from the sense winding of the associated plane in memory array 0, together with a SEL 0 ground level which gates on the difference amplifier. The other input difference amplifier accepst a pulse from the corresponding plane in memory array 1 and a SEL 1 enabling level. The enabling levels are provided by the memory control logic and ensure maximum stability. The slicer suppresses nodes induced into the sense winding of a memory plane by the

read/write current pulses. Therefore, only the much larger signal produced by a core changing state can produce an output from the sense amplifier.

In order to obtain an output pulse of the correct shape and duration, a strobe pulse is applied to the output gate of the sense amplifier. The strobe pulse is obtained by combining timing pulse TP2 of the computer timing chain with a field selection signal, applying the resulting pulse to a delay network, and reshaping the delayed pulse in a pulse amplifier.

The strobe pulse is precisely timed with respect to the read current pulse, so that sensing occurs at the instant when the signal induced into the sense winding reaches maximum peak amplitude (Figure 4-4). If a core changes state, the slicer enables the output gate, and the strobe pulse causes the gate to produce a 40-nsec output pulse. This pulse is reshaped in the pulse ampifier and appears at the output terminal of the module as a standard negative pulse which sets an MB flip-flop.

The master slice control module contains three reference voltage diode networks, each with an associated emitter follower output voltage control. The adjustment range of the first stage clamp potential is from 5.0 to 6.5v; that of the second stage clamp potential is from 11.5 to 12.4v; and that of the slice level is from 5.0 to 10.0v. The first and second stage clamp levels are factory preset at 6.5v and 11.4v, respectively, under a 50-ma load. The slice level is normally preset to 6.8v and may be adjusted so that the sense amplifier gives symmetrical deviations when the sense amplifier +10v supply is varied to the upper and lower marginal levels.

Memory Control

The memory control logic generates signals which perform memory array selection and initiate the generation of read, write, and inhibit currents at the appropriate times in the computer cycle. The logic diagram of the memory control is contained in drawing BS-D-7-0-27, and all references in the following discussion of the memory control are to this diagram unless otherwise stated.

Address bits MA4 and MA5 are decoded by NAND gates in modules C21 and C22 and produce SEL 0, SEL 1, SEL 2, and SEL 3 control signals. Each of these signals enables the sense amplifier gates associated with a particular 4K memory array. When memory capacity is limited to 8K, bit MA4 is always 0, and bit MA5 selects one of the arrays in the 8K field designated. At time T2 of the computer cycle, timing pulse TP2 sets the READ 1 and READ 2 flip-flops. The READ 1 ground level output is combined with the MA5(0) or MA5(1) level to produce a SEL · READ (1) B level which enables the read current pulser in the address selection circuits. The negative READ 2 (1) level is applied to the drive selectors and ground selectors. At time T3, the STROBE 0, 1 pulse clears the READ 2 flip-flop first in order to disable the read/write current pulsers; 30 nsec later, the STROBE RTN pulse clears the READ 1 flip-flop to disable all the read gates in the drive and ground selectors. The setting of the WRITE flip-flops resulsts in similar actions, except that the WRITE 2 flip-flop opens the write gates in the memory selectors, thereby reversing the direction of the current pulse through the memory cores.

The memory control logic includes bus drivers which provide adequate current to drive the memory selectors and to gate the inhibit drivers. The NAND gates in module C29 (AB, 27) combine address bit MA4 with timing pulse TP2 for the generation of a separate strobe pulse for each of two 8K memory fields. When memory capacity is limited to 8K, the TP2 · SEL 0, 1 pulse is used. The resulting strobe pulse is applied to both 4K arrays of the 8K memory field.

Memory Current Sources

A Type 739 Power Supply is used in conjunction with the Core Memory Type 149B. The Type 739 unit contains two independent, floating power supplies. One supply provides read/write current, and the other provides inhibit current for a complete PDP-7 system, regardless of the capacity of the memory. A Type 728 Power Supply provides +10v and -15v to energize the memory logic. Both the 728 and 739 units are located at the rear of equipment bay 1, behind the memory. Circuit schematic diagrams for the 739 are shown in engineering drawings RS-C-739B, RS-B-W505, and RS-B-G800. Engineering drawings RS-B-728 shows the circuit schematic for the Type 728 Power Supply.

CHAPTER 5

INPUT/OUTPUT

Peripheral equipment may either be asynchronous with no timed transfer rates or synchronous with a timed transfer rate. Devices such as the CRT displays, teleprinter-keyboard, and the line printer can be operated at any speed up to a maximum without loss of efficiency. These asynchronous devices are kept on and ready to accept data; they do not turn themselves off between transfers. Devices such as magnetic tape, DECtape, the serial drum, and card equipment are timed-transfer devices and must operate at or very near their maximum speeds to be efficient.

Some of the timed-transfer devices can operate independently of the central processor after they have been set in operation by transferring a continuous block of data words through the PDP-7 data interrupt facility. Once the program has supplied information about the location and size of the block of data to be transferred, the device itself takes over the work of actually performing the transfer. The data interrupt facility logic is described in Chapter 2 and the circuit operations in Chapter 3.

Separate parallel buffers are provided on each input/output device attached to the basic PDP-7. The high-speed perforated Tape Reader Control Type 444B contains an 18-bit buffer and binary word assembler. The high-speed perforated Tape Punch Type 75D, and the teleprinter and the keyboard of the Teletype and Control Type 649 each contain separate 8-bit buffers. These devices are described in this chapter.

Separate parallel buffers are also incorporated as part of DEC standard I/O peripheral equipment options. Information is transferred between the accumulator and a device buffer during the execution time of a single-cycle IOT instruction. Because the maximum time the accumulator is associated with any one external buffer is 1.75 μsec, many standard I/O devices can operate simultaneously under control of the PDP-7.

Figure 5-1 shows the data path between device buffers and the AC through the information collector or information distributor.

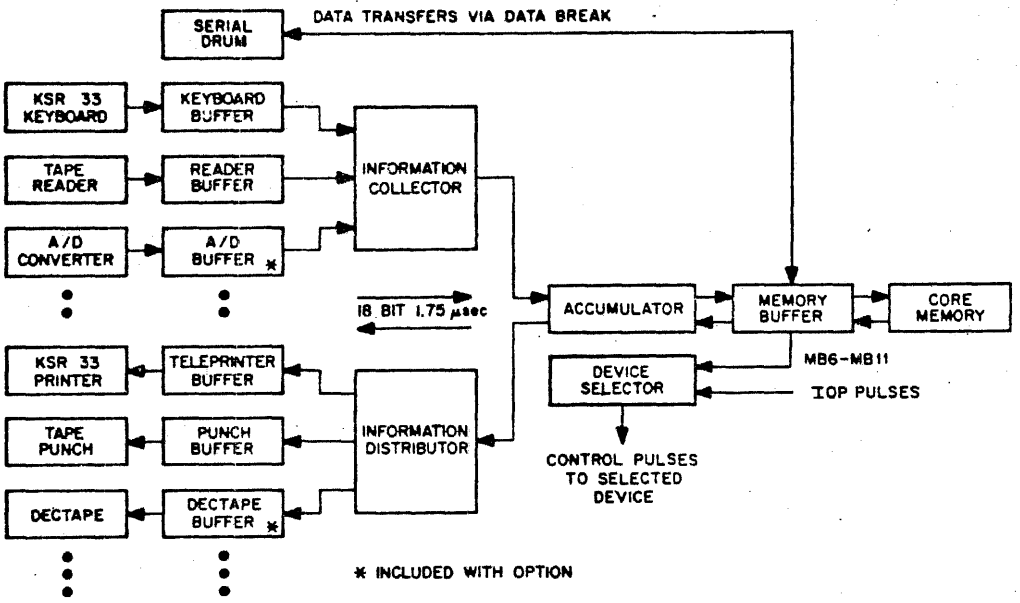


Figure 5-1 Input/Output Information Flow

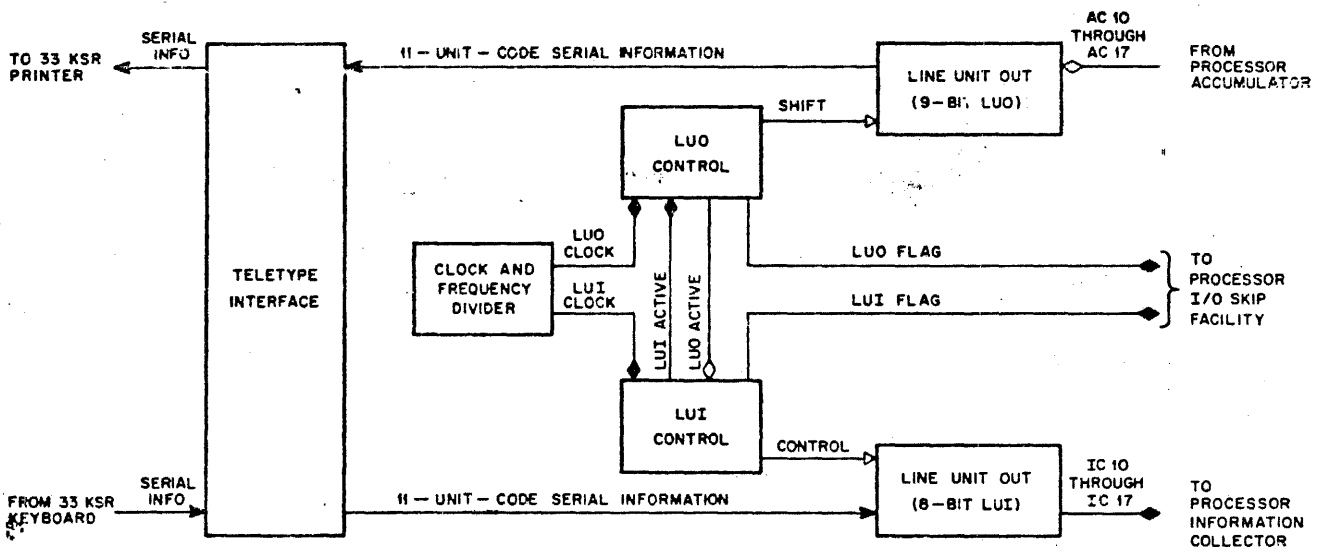


Figure 5-2 Block Diagram of Keyboard/Printer Control Type 649

TELETYPE (MODEL 33 KSR) AND CONTROL TYPE 649

The Teletype Model 33 KSR is a keyboard send-receive unit, utilizing a 3-row keyboard and an 8-level code operating on serial information at speeds up to 100 words/min. Internal jumper connections are made within the Teletype, as specified in the TTY manual, for full duplex operation with local copy provisions. No other modifications are made to the Teletype for use with the PDP-7. The Type 649 Control, used with the Teletype, provides conversion in both directions between the serial information used by the Teletype and the parallel information used by the processor. The logical organization of the Teletype and control is shown in Figure 5-2. (Note that in the figure the Type 649 Control is shown in two separate blocks: Teletype Receiver and Teletype Transmitter.) Information is manually injected by means of the Teletype keyboard and is carried in serial form to the Teletype receiver where it is assembled into parallel form. The receiver is also known as an incoming line unit (LUI). From the receiver, the parallel information is passed to the CP via the information collector. Information from the CP is transferred in parallel form to the Teletype transmitter, where it is shifted into the printer in serial form. The transmitter is also known as an outgoing line unit (LUO).

Block Diagram Discussion

Teletype Keyboard

Information is typed out on the keyboard in the same manner as on an ordinary typewriter. As each key is pressed, a code combination is set up to correspond with the selected character. This is converted to serial form by a distributor arrangement which relates a given bit position to a given time interval in the distributor cycle.

Teletype Printer

Serial information entering the printer is automatically typed on a page-width roll. The Teletype printer uses the same information code as the Teletype keyboard.

Teletype Receiver (LUI)

The serial information generated by the keyboard must be converted into parallel form before it can be accepted by the CP. This is accomplished by the Teletype receiver. Each successive

bit of information comprising each character is fed to the input of the flip-flop register in the receiver. Initially, the bit is deposited in the least significant flip-flop. When the next bit appears, a shift pulse occurs and each previously deposited bit is transferred to the flip-flop which is one order higher, while the new bit is deposited in the least significant flip-flop. This process continues until all the bits of the character being transferred have been deposited in the receiver flip-flop register, at which time a flag is raised and can be sensed by the program. The contents of the receiver are transferred to the AC via the IC.

Teletype Transmitter (LUO)

The parallel information utilized by the computer must be converted to serial form before it can be handled by the Teltype printer. This is accomplished by the Teletype transmitter which is fed an 8-bit character by the AC of the CP via the ID of the interface. The eight bits are first deposited in the flip-flop register of the transmitter. This register contains nine flip-flops, the least significant eight being used for temporary storage of the character and the ninth being the transfer flip-flop. A shift pulse transfers each successive bit of the character to the next higher order flip-flop, a move at a time, putting each bit sequentially into the transfer flip-flop. From the transfer flip-flop the bits are applied to the Teletype printer, through an output circuit.

Clock and Frequency Divider

Operation of the Teletype receiver (LUI) requires an input clock signal whose frequency is eight times the baud frequency of the Teletype keyboard unit. This signal is used to control the strobing of Teletype information into the receiver during the center of each baud (which is the most reliable time for sensing) and to control the shifting of information through the flip-flops of the receiver. The Teletype transmitter (LUO) requires an input clock signal whose frequency is twice the frequency of the transmitter. Clock pulses are produced by a 14.08-kc crystal clock driving a 6-element binary counter which serves as a frequency divider to provide the required pulse frequencies.

Logical Functions

Keyboard and Printer

The Teletype Model 33 KSR (keyboard-send-receive) can be used to type in or print out information at a rate of up to 10 char/sec. Signals transferred between the 33 KSR and the keyboard printer control logic are standard serial, 11-unit-code Teletype signals. The signals consist of marks and spaces which correspond to idle and bias current in the Teletype and 0's and 1's in the control and computer. The start mark and subsequent eight character bits are 1 unit of time duration and are followed by a 2-unit stop mark.

Teletype Code

Each of the (64 type) characters and 32 control characters is represented by an 8-bit standard ASCII code. The Teletype 8-level code is listed in the Appendix. The teleprinter input and output functions are logically separate, and the programmer should think of the printer and keyboard as individual devices.

Keyboard Control

The keyboard control contains an 8-bit buffer (LUI) which assembles and holds the code for the last character struck on the keyboard. The keyboard flag becomes a 1 to signify that a character has been assembled and is ready for transfer to the accumulator. This flag is connected to the computer program interrupt and input/output skip facility and may be cleared by command.

Teleprinter Control

The teleprinter control contains an 8-bit buffer (LUO) which receives a character to be printed from AC bits 10 through 17. The LUO receives the 8-bit code from the AC in parallel and transmits it to the teleprinter serially. When the last bit has been transmitted, the teleprinter flag is set to 1. This flag is connected to the computer program interrupt and input/output skip facility. It is cleared by programmed command.

Teletype Instructions

The following instructions are used for the Teletype:

KSF	700301	Skip if the keyboard flag is set to 1. If the flag is 0, the next instruction is executed. If it is 1, the next instruction is skipped. The flag is set only when a character has been completely assembled by the buffer.
KRB	700312	Read the keyboard buffer. The contents of the buffer are placed in bits 10-17 of the AC and the keyboard flag is cleared.
TSF	700401	Skip if the teleprinter flag is set.
TLS	700406	Load printer buffer and select. The contents of AC10-17 are placed in the buffer and printed. The flag is cleared before transmission takes place and is set when the character has been printed.

Circuit Operations

Teletype Keyboard and Printer

Complete technical information on these units may be found in the applicable instruction manuals supplied with the computer. (Refer to the list of pertinent documents in Chapter 1 of this manual.)

Keyboard/Printer Control

The keyboard printer control provides the required conversion between the parallel information used by the CP and the serial information used by the Teletype unit. It also provides the program flags which cause a program interrupt or an instruction skip based on the availability of the Teletype unit. It thus controls the rate of information flow between the processor and the Teletype as a function of the program. The control is shown on engineering drawing BS-D-649-0-2 It consists of a Type 4706 Eight-Bit Teletype Receiver (LUI) at location R2B2, a Type 4707

Eight-Bit Teletype Transmitter (LUO) at location R2B1, a Type 4225 Clock at location R2B4, a Type 4225 Eight-Bit Binary Counter at location R2B3, and the KSR 33 Driver attached to the back panel wiring of the keyboard/printer control logic panel.

Receiver (LUI) - The receiver accepts serial information from the Teletype keyboard and converts it to parallel form by means of an 8-bit flip-flop register. Each typed character consists of eight bits plus 1-unit start space and a 2-unit stop mark. As each character is typed on the keyboard, the serial pulses making it up are fed to the KSR 33 driver and to the input of the flip-flop register (input of the least significant flip-flop). Shift pulses (of the same frequency as the bit frequency of the transmitted character) move each of the stored bits to the next higher order flip-flop each time another bit (pulse) appears. When the register is filled, the character is complete and an LUI FLG signal is produced by the keyboard flag flip-flop. When the character is transferred to the AC, the IOT 0302 pulse clears the flag.

> NOTE: An indicator lamp and a cut-out toggle switch are provided on the handle end of the 4706 module to provide maintenance personnel with a visual indication of the flag signal and a means of disabling the signal to prevent the reading of new characters by the program.

An LUI ACTIVE signal, generated by the active flip-flop, is used to disable the transmitter (LUO) when the receiver is in use so that the LUO cannot be operated until 1.5 Teletype units of time have elapsed after the last LUI operation has been sensed by the AC.

Transmitter (LUO) - The transmitter accepts parallel information from the CP (through the ID) and converts it to serial form by means of a 9-bit flip-flop register. The eight bits of each transferred character are first loaded simultaneously in the eight least significant flip-flops. A series of shift pulses, at a frequency of 220 cps, successively shift each bit in turn into the ninth (most significant) flip-flop. This is the transfer flip-flop. From the transfer flip-flop, the bits are passed to the line driver, the KSR driver, and to the Teletype printer. When the transfer of all bits of the character has been completed, a LUO FLG sign 1 is put out by the teleprinter flag flip-flop. When the next character is ready to be loaded into the register from the CP, the IOT 0402 pulse clears the flag and an IOT 0404 pulse reloads the register.

NOTE: An indicator lamp and a cut-out toggle switch are provided on the handle end of the 4707 module to provide maintenance personnel with a visual indication of the flag signal and a means of disabling the signal to prevent the writing of new characters by the program.

A LUO ACTIVE signal, generated by the control, is used to disable the receiver (LUI) when the transmitter is in use. The flip-flop register is provided with a power clear signal to reset all flip-flops when the computer is initially turned on.

Clock and Frequency Divider - A 14.08-kc crystal clock producing 400-nsec positive pulses provides the master timing source for the Teletype system. Although the actual frequencies required by the keyboard and printer are respectively 880 and 220 cps, the higher frequency of 14.08 kc is used to insure operational stability. The necessary frequency reduction is accomplished with a binary counter, consisting of six flip-flops connected in a counting chain. Each flip-flop changes state whenever the next lower flip-flop changes from 1 to 0. Thus, the pulse frequency of a given flip-flop output is half that of its input. Since the LUI clock input is tapped off at the fourth flip-flop, the 14.08-kc clock frequency will have been divided by 2^4, or 16, giving the required frequency of 880 cps. Similarly, the LUO clock signal is tapped off at the sixth flip-flop, and the original clock frequency will be divided by 2^6, or 64, giving the required frequency of 220 cps.

PERFORATED TAPE READER AND CONTROL TYPE 444B

A Digitronics Model 2500 Perforated Tape Reader and a DEC Type 444B Reader Control are standard equipment supplied with every PDP-7 system. The tape reader is a timed-transfer device which senses the holes punched in 5, 7, or 8-channel paper or Mylar-base tape at a maximum rate of 300 lines/sec. When used in the PDP-7 system, the standard input medium is 8-channel tape. The reader control contains an 18-bit output register which is loaded by the reader, together with all the logic elements necessary for starting and stopping the reader under program control, and sensing the state of the output register.

The reader is normally mounted in the center of bay 2, immediately above the operator console. The reader control occupies one half of a mounting panel near the bottom of bay 3 (the other half of the panel is occupied by the punch control).

The mechanical and electrical operation of the reader is fully described in the manufacturer's manual which is supplied with the PDP-7 system and is identified in the list of Pertinent Documents in Chapter 1 of this manual. Therefore, the following paragraphs describe only the logical functions of the reader and control, and the operation of the Type 444B Reader Control.

Logical Functions

Operation of the reader is controlled entirely by the program. When the reader is selected by the appropriate IOT instruction, the brake is released and the clutch engages the capstan to move the tape past the photocells. The feedhole is sensed first, and generates a level transition which causes sensing of the information channels. The sensing of information channels is delayed until the holes have advanced far enough to ensure that punched holes transmit the maximum possible amount of light to the photocells and that tape skew due to worn guides will not cause loss of information. For each hole punched in a given line of tape, a corresponding bit of the RB (reader buffer) is set to 1. Information can be read from the tape and assembled in the reader buffer in either of two modes: alphanumeric, or binary.

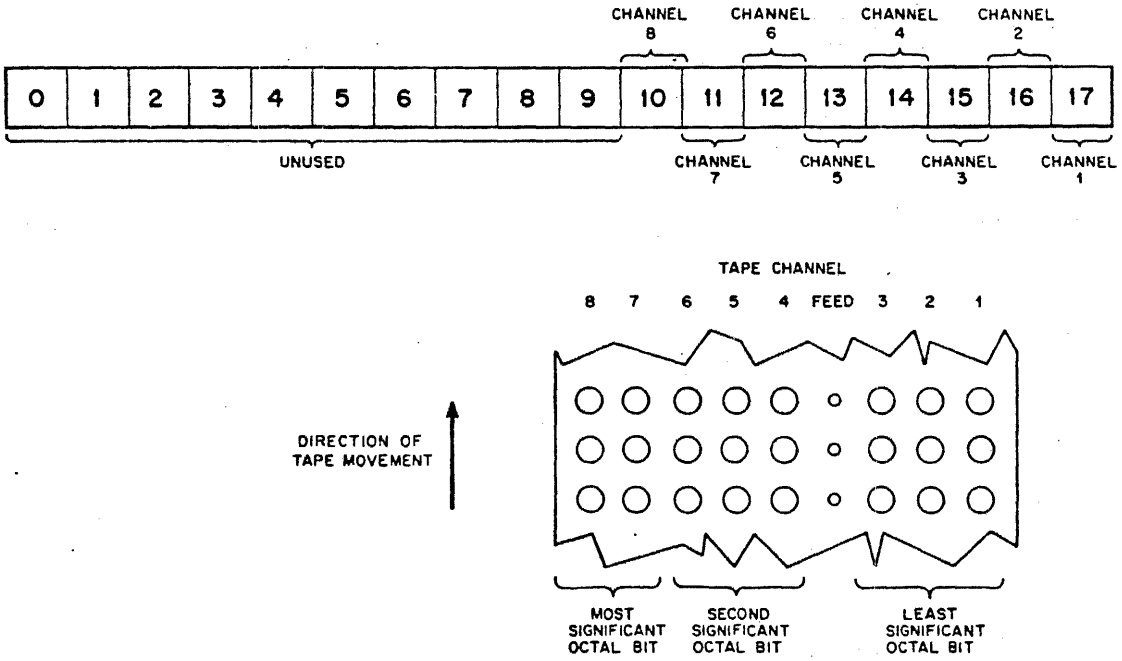
Alphanumeric Mode

The alphanumeric mode, used for reading eight channels of information, is selected by an RSA instruction of the IOT class. Each select instruction causes one line of tape to be read and the information to be placed in bits 10-17 of the RB. See Figure 5-3.

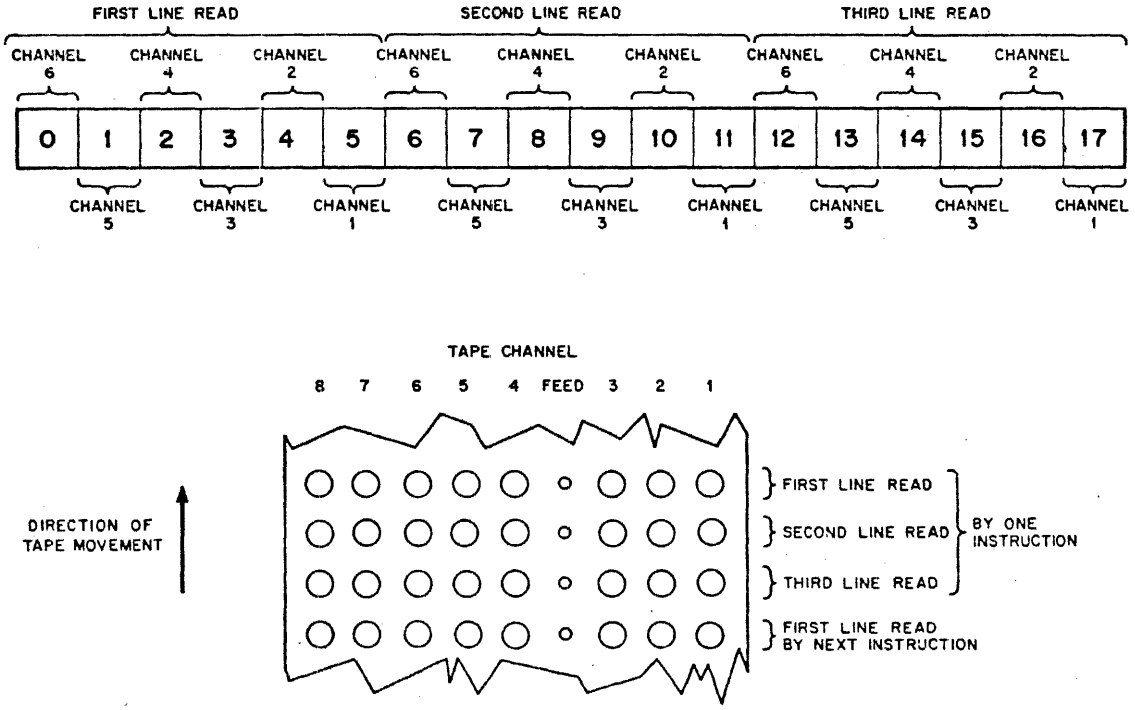
Binary Mode

The binary mode, used for reading 18-bit binary words, is selected by an RSB instruction of the IOT class. One binary word occupies three lines of tape. Each select instruction causes three successive lines of tape to be read, each line containing six bits of binary information. The first line, containing the most significant bits, is read into bits 12 through 17 of the RB.

The RB performs as a 3-stage, 6-bit shift register. When the first line of tape has been read, a shift pulse causes the contents of RB12-17 to be shifted bodily into RB6-11, and at the same time reads the second line of tape into RB12-17. A second shift pulse shifts the contents of the first line of tape into bits RB0-5, the contents of the second line of tape into RB6-11, and



Alphanumeric Mode



Binary Mode

Figure 5-3 Tape Format and Reader Buffer Register Bit Assignments

reads the third line of tape into RB12-17. The complete binary character is now assembled in bits RB0-17 and the reader flag is set, indicating that the reader buffer is full. When reading in binary mode, hole 7 is never punched; hole 8 is ignored, but a character is not read unless this hole is punched. The tape format for binary mode is shown in Figure 5-3.

When a program is being stored by use of the READ-IN key, the processor forces the reader into the binary mode and executes a pseudo-DAC instruction each time the reader flag is set. If a hole 7 is punched, the processor interprets this as an instruction to stop the reader and to execute the last 18-bit word read.

Perforated Tape Reader Instructions

RSA	700104	Select reader in alphanumeric mode. One 8-bit character is read and placed in the reader buffer. The reader flag is cleared before the character is read. When transmission is complete, the flag is set.
RSB	700144	Select reader in binary mode. Three 6-bit characters are read and assembled in the reader buffer. The flag is immediately cleared and later set when character assembly is completed.
RSF	700101	Skip if reader flag is set.
RCF	700102	Clear reader flag; then inclusively OR reader buffer into AC.
RRB	700112	Clear reader flag. Clear AC and then transfer contents of reader buffer to AC.

Circuit Operations

The logic of the Type 444B Reader Control is shown on engineering drawing BD-D-444B-0-2. The reader control contains two major groups of logic elements: the reader buffer (RB) and the control logic.

Reader Buffer (RB)

The reader buffer provides temporary storage for alphanumeric or binary characters read by the tape reader. The RB contains two Type R203 FLIP-CHIP Triple Flip-Flops, each flip-flop having a direct clear and a DCD set input. These modules are used in bits RB0 through RB5. For bits RB6 through RB17, Type R202 FLIP-CHIP Double Flip-Flops are used, each flip-flop having a direct clear input and DCD set and clear inputs. When reading in alphanumeric mode, bits RB10 through RB17 are used. Tape characters are read directly into these flip-flops, and the remaining bits are not used. When reading in binary mode, the input gating causes the register to function as a 3-stage, 6-bit shift register. A simplified diagram of this configuration is shown in Figure 5-4. After the first line of tape has been read into bits RB12 through RB17, an RD SHIFT 1 is applied to all the DCD input gates of bits RB6 through RB17. Bit RB12 then determines the condition of bit RB6, and RB17 that of RB11, with a corresponding transfer in intermediate bits. Simultaneously, the second line of tape is read into RB12 through RB17. When the third line of tape is ready for reading, RD SHIFT 1 and RD SHIFT 2 pulses are generated simultaneously and applied to the DCD input gates. The RD SHIFT 2 pulse shifts the contents of bits RB6 through RB11 into bits RB0 through RB5. The RD SHIFT 1 pulse operates in the same manner as before.

The (1) output of each RB flip-flop (ground level) is inverted and appears on terminals of the W020 connector in location B1 and of the W021 connectors in locations B2 and B3. Three Type R107 Inverters, each containing seven inverters, are used for this purpose. The connector at location B1 routes the levels to indicators; the connectors at B2 and B3 provide connections to the IC.

Control Logic

The control logic circuits generate all the levels and pulses required for starting and stopping the reader and for producing shifts when reading in binary mode.

At power turnon, PWR CLR negative pulses from the CP are applied to inverter JK in module B9 (D1, 444B-0-2) and clear the RD MODE, RD RUN, and RD FLAG flip-flops. This same clearing action is also initiated by a BGN pulse at time SP1 of a manual operation, or by an IOT 0102 pulse from the device selector. This clearing action establishes initial conditions.

The reader is started by an IOT 0104 command pulse applied to inverter HF in module B9 (C2, 444B-0-2). This pulse appears whenever the reader is selected, and triggers a pulse amplifier which produces a START pulse at terminal A4K. The START pulse performs three functions:

1. It clears all the reader buffer flip-flops, together with the RD FLAG, RD1 and RD2 flip-flops.

2. It sets the RD RUN flip-flop to 1, thereby starting the tape reader.

3. If bit 12 of the MB contains a 1, the START pulse triggers a DCD gate that sets the RD MODE flip-flop to 1. When this flip-flop is in the 0 state, a ground $\overline{\text{BINARY}}$ level is produced at inverter output terminal B8L (C3, 444B-0-2) to select the alphanumeric mode. When the RD MODE flip-flop is set to 1, a negative BINARY level appears at terminal B8L to select the binary mode. Note that the RD MODE flip-flop may also be set to 1 when an RPT (1)B level is established by a manual readin operation.

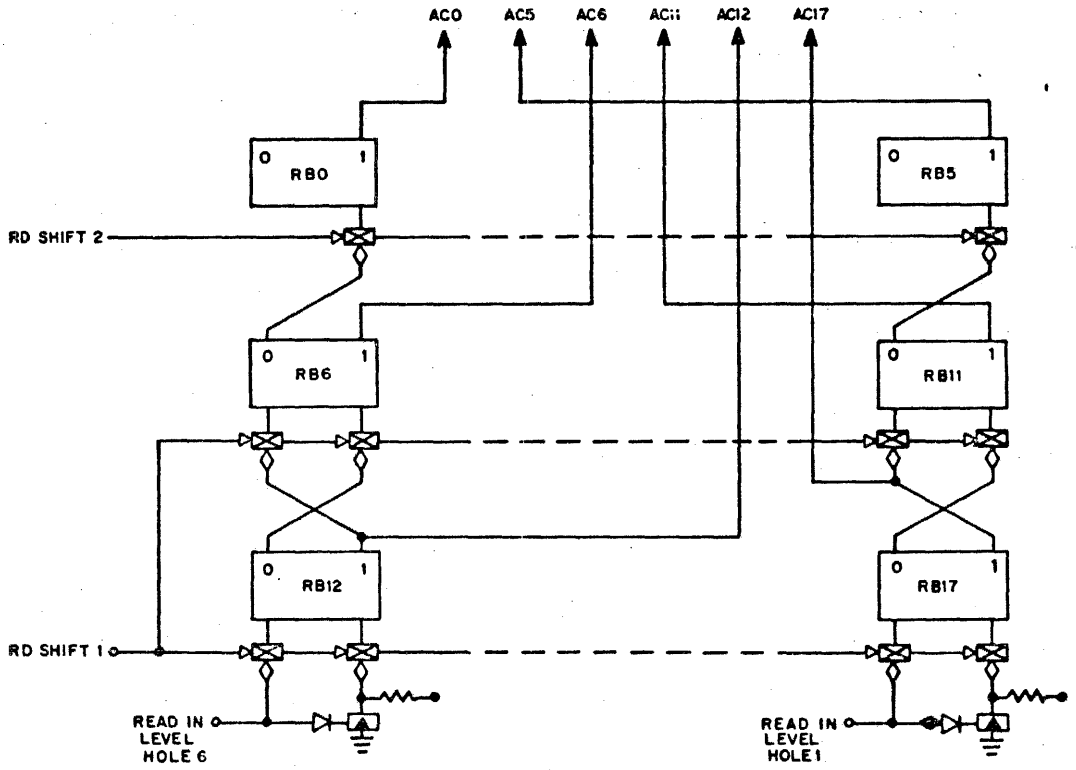


Figure 5-4 Reader Buffer In Binary Mode

Negative levels produced by 1's in the first six bits of the tape are inverted and condition the set DCD gates of flip-flops RB12 through RB17. Ground levels produced by 0's are directly applied to the reset DCD gates. The levels produced by holes 7 and 8 condition an additional set of NAND gates which do not open unless strobed by an ALPHA-N pulse. The level transition produced by the feed hole causes Schmitt trigger FLR in module A3 to change state. If the RD RUN flip-flop is set to 1, the output of the Schmitt trigger sets the delay one-shot in module B4. The purpose of this one-shot is to delay the instant at which the reader buffer samples the output of the photocells until the center line of the tape holes coincides with the center of the feed hole. There are two reasons for this. Using a correctly aligned tape, sampling at the leading edge of the feed hole would take place before the other holes were centralized over the photocells, so that the output of the photocells would not yet have reached its maximum value. More important, if worn tape guides have caused skew in the tape, sampling at the leading edge of the feed hole might cause loss of information from holes 7 and 8, as shown in Figure 5-5. Delaying the sampling instant ensures that under tolerable conditions of skew all photocells produce some output, so that no information is lost.

When reading alphanumeric mode, the RD STRB output pulse from the one-shot triggers a DCD gate conditioned by a ground $\overline{\text{BINARY}}$ level, and the output of the gate causes an RD SHIFT 3 signal to appear at pulse amplifier output terminal A4U. This pulse, inverted, becomes the ALPHA-N negative pulse which strobes the hole 7 and hole 8 NAND gates. At the same time, the RD STRB pulse triggers two other DCD gates conditioned by a $\overline{\text{BINARY}}$ level. One of these gates causes generation of an RD SHIFT 1 pulse at pulse amplifier output terminal B5K; the other causes generation of a RD SHIFT 2 pulse at terminal B5U. These RD SHIFT pulses strobe all the DCD input gates of the RB flip-flops and read a line of tape into bits RB10 through RB17. The ALPHA-N pulse, inverted, sets the RD FLAG flip-flop.

When reading in binary mode, the DCD gate A4P,R is disabled by the negative BINARY level, and therefore the ALPHA-N pulse is not generated. Since the NAND gates for holes 7 and 8 are not strobed, these holes are not read. However, hole 8 is always punched, and the negative level, inverted, permits generation of the RD SHIFT signals by conditioning DCD gates A5E,F and A5S,T.

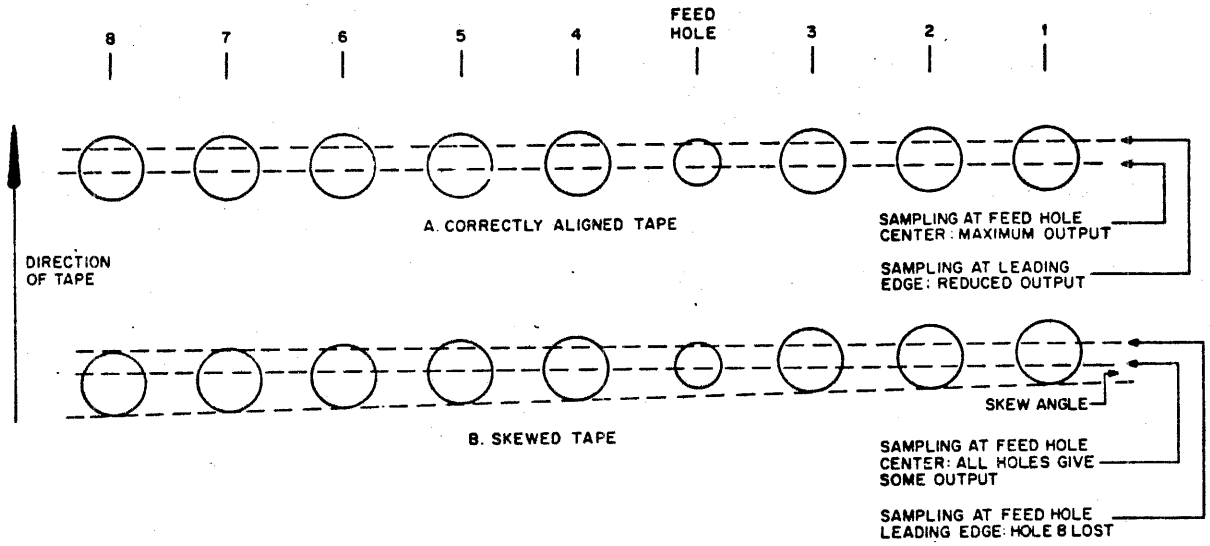


Figure 5-5 Effect of Delayed Sampling

The RD SHIFT 2 pulse that accompanies the reading of the first line of tape sets the RD 1 flip-flop. The output of this flip-flop conditions the DCD set gate of the RD 2 flip-flop, and when the RD SHIFT 2 pulse of the second line of tape appears, the flip-flop is set. The RD 2(1) output conditions the DCD set gate of the RD FLAG flip-flop, and when the third line of tape is read, the accompanying RD SHIFT 2 pulse sets the RD FLAG flip-flop.

The setting of the RD FLAG flip-flop indicates to the CP that the reader buffer is full. The positive-going level transition produced by the RD FLAG flip-flop clears both the RD MODE and the RD RUN flip-flops. Clearing the RD MODE flip-flop reestablishes the alphanumeric mode; clearing the RD RUN flip-flop stops the reader.

TAPE PUNCH AND PUNCH CONTROL TYPE 75D

The Teletype Tape Punch Set (BRPE) and the DEC Type 75D Punch Control are supplied with each PDP-7 as standard equipment. The tape punch is a timed-transfer device capable of

punching 5-, 7-, or 8-channel tape at a maximum rate of 63.3 char/sec. In the PDP-7 system the standard output medium is 8-channel tape. The punch control contains an 8-bit data register, which is loaded from the AC through the information distributor. It also contains all the logic elements necessary for starting and stopping the tape punch and supplying it with the applicable data.

The tape punch is mounted in the center bay, above the tape reader. The punch control is located near the bottom of bay 3.

The mechanical and electrical operation of the tape punch is fully described in the manufacturer's manual supplied with the PDP-7 (refer to the list of Pertinent Documents, in Chapter 1 of this manual). Consequently, the following paragraphs describe only the logical functions of the tape punch, and the operation of the punch control.

Logical Functions

Operation of the tape punch is normally controlled entirely by the program. However, the operator may punch leader tape (feed hole only punched) by pressing the PUNCH FEED button on the console or he may force on the punch power by setting the console PUNCH switch. When the tape punch is selected by the first punch IOT instruction, the punch is turned on and after a 1-sec delay (during which the punch motor comes up to speed), punching begins. Subsequent punch instructions are executed immediately. The punch control functions as a buffer, a control unit, and a solenoid and motor driver for the tape punch. When a tape punch operation is selected by an IOT instruction, a pulse establishes the operating mode of the control (alphanumeric or binary) and causes certain of the 1's stored in AC to be transferred to the buffer register of the punch control via the information distributor. If the mode is alphanumeric, the 1's are transferred from AC bits 10-17. If the mode is binary, the 1's are transferred from AC bits 12-17. The flip-flops containing 1's then enable a series of gates which trigger solenoid drivers and upon receipt of the punch command, a hole is punched in the tape in each channel where a corresponding 1 was present in the AC. When a line of tape has been punched, the buffer register and PUN ACTIVE flip-flops are cleared, and the PUN FLAG is set to indicate to the CP that the punch is ready for a further punching instruction. After the last punch command, the motor remains energized for an additional 5 sec.

Alphanumeric Mode

The alphanumeric mode is used for punching 8-channel tape, and is selected by a PSA instruction of the IOT class. Each select instruction causes one line of tape, consisting of eight bits, to be punched. A hole is punched in each tape channel whose corresponding bit in the AC is a 1. A feed hole is always punched.

Binary Mode

The binary mode is used for punching 18-bit words and is selected by a PSB instruction of the IOT class. Holes are punched corresponding to bits 12-17 of the PB. Bit 11 (hole 7) is never punched and bit 10 (hole 8) is always punched. This establishes the standard format for binary information on tape. Since only six data bits are punched at a time, a complete 18-bit word requires three lines on the tape and consequently involves three separate PSB instructions.

Tape Punch Instructions

PSA	700204	Punch a line of tape in alphanumeric mode. The punch flag is immediately cleared and then set when punching is complete.
PSB	700244	Punch a line of tape in binary mode. The punch flag is immediately cleared and then set when punching is complete.
PSF	700201	Skip if the following instruction if the punch flag is set.
PCF	700202	Clear the punch flag.

The following instruction will clear the accumulator and cause a line of tape to have only the feed hole punched:

PSA +10	700214	Clear AC and punch.

The following instruction as used on the PDP-4 is also available, but is generally replaced with the more direct PSA.

PLS	700206	Same as PSA.

Circuit Operations

Punch Control Type 75D may be divided into the following major functional circuit groups: control logic, punch buffer and solenoid drivers, and motor logic. These elements are all shown on engineering drawing BS-D-75D-0-2.

Control Logic

The operation of the punch is entirely under program control, and the control logic contains all the circuits which interpret a punch instruction and indicate to the CP when a punching operation is complete. PWR CLR pulses generated in the CP at turnon are applied to terminal D of the connector in module B30. These pulses, inverted, trigger a pulse amplifier in module B22, which clears the punch buffer. The buffer clearing pulses appear at terminal B22K. The buffer is also cleared if an IOT 0202 command pulse and an MB15 (0) level cause a pulse to appear at terminal B22U. In both cases the PUN MODE flip-flop is also cleared.

The elements which respond to program control are the PUN MODE flip-flop, which determines whether alphanumeric or binary characters will be punched on the tape; the PUN ACTIVE flip-flop, which starts and stops the motor; and the PUN FLAG, which is set to 0 at the beginning of a punching operation and is set to 1 when the punching of a character is complete.

The PUN MODE flip-flop is cleared by an IOT 0202 command pulse. The flip-flop is set by an IOT 0204 pulse, produced by an instruction to punch, if bit 12 of the instruction contains a 1, specifying binary mode. When set, the PUN MODE flip-flop forces a 0 into bit 11 of the punch buffer (hole 7) and a 1 into bit 10 (hole 8). When the PUN MODE flip-flop is in the 0 state (for alphanumeric mode) bits 10 and 11 of the punch buffer are set by the corresponding bits of the AC.

The PUN FLAG and PUN ACTIVE flip-flops are cleared by an IOT 0204 pulse, produced by an instruction to punch. When a character has been punched, a PUN DONE level is produced which clears both these flip-flops and the buffer register. The PUN FLAG (1) level appears

at terminal T of the W021 connector in location B30, and is routed to the break control in the CP. The PUN ACTIVE (1) level is utilized in the motor logic.

Punch Buffer, Solenoid Drivers, and Synchronization

The punch buffer (PB) is an 8-bit register which provides temproary storage for information supplied by the AC. The PB (1) levels condition the solenoid driver input gates. Flip-flops PB10 through PB17 are cleared by PWR CLR pulses at power turnon, by an IOT 0202 command pulse, and by the PUN DONE signal produced after the punching of each character. The DCD set gate of each flip-flop is conditioned by the state of the corresponding bit of the AC and is triggered by an IOT 0204 pulse. Thus, binary 1's are transferred from the AC into the PB. The solenoid drivers are controlled by 2-input NAND gates.

One input of each gate is conditioned by the corresponding PB (1) level; the other input is enabled by a 5-msec signal generated in the synchronization circuits. During this 5-msec period each gate that is fully enabled causes the associated solenoid driver to energize the solenoid, and a hole is punched in the corresponding tape position. The solenoid driver for the feed hole punch receives only the synchronizing signal and produces a feed hole for every operation.

The synchronizing signal is generated by a magnetic pickup on the punch drive shaft and appears when the punch cams are at or near top dead center. The timing of the signal is adjustable. The synchronizing signal triggers the Schmitt trigger in module A19, and the level transition which appears at terminal A19F triggers the 5-msec one-shot in module A20, provided that the DCD input gate is conditioned by a PUN READY level. In its quiescent state, this one-shot produces a ground PUN DONE level at terminal A20V which is applied through the bus drivers in module A21 to the solenoid driver input gates. When the synchronizing signal arrives, the level at terminal A20V changes to -3v and causes the bus drivers to enable the solenoid driver input gates for 5 msec, after which punching of a character is complete and the PUN DONE level reappears. The resulting positive-going level transition clears the punch buffer and the PUN ACTIVE flip-flop, and sets the PUN FLAG.

Motor Logic

The punch is turned on and off under program control, but the motor requires 1 sec to attain full speed. To eliminate delay in the execution of successive punch instructions, it is desirable to keep the motor running for 5 sec after a line of tape has been punched, so that a further punch instruction can be executed immediately. The motor logic provides the required control signals for this purpose.

The Type R302 delay one-shot at location B28 delays the execution of the first punch instruction for 1 sec to allow the motor to come up to speed, and the Type 4303 Integrating One-Shot at location R2B4 keeps the motor running for 5 sec after execution of the last punch instruction. These functions are accomplished as follows:

1. If the PUN ACTIVE flip-flop is set by a punch IOT instruction, or if the console TAPE FEED pushbutton is pressed, a PUN RQ level is produced at terminal B27H and sets the integrating one-shot to its unstable state. The negative level produced at the (1) terminal of the integrating one-shot is inverted and causes a relay driver to energize relay K1, thereby starting the motor.

2. Punching cannot begin until a ground PUN READY level appears at NAND gate output terminal B27N and conditions the DCD input gate of the 5-msec one-shot of the synchronizing one-shot (refer to the explanation of the synchronizing logic). The PUN READY level appears only when all three inputs of NAND gate KLMN of module B27 are conditioned by the negative levels. One of these inputs is conditioned by the PUN RQ level. A second input is conditioned by the negative (1) level of the integrating one-shot. The third input is conditioned by the inverted (0) level of the 1-sec delay one-shot at location B28. When the integrating one-shot is set and starts the motor, the positive-going level transition appearing at the (0) terminal triggers the 1-sec delay one-shot into its unstable state. The output of the delay one-shot, inverted, disables the NAND gate in module B27 to prevent a PUN READY level from being generated while the motor is gathering speed.

3. After 1 sec, when the motor has attained full speed, the delay one-shot reverts to its stable state. The ground level which appears at the output terminal B28M is inverted and causes a negative level to be applied to terminal B27N. All three inputs of the NAND gate are now conditioned, and a ground PUN READY level appears at the output of the gate.

4. After a character has been punched, the PUN DONE level transition clears the PUN ACTIVE flip-flop, thereby producing a ground $\overline{\text{PUN RQ}}$ level that disables NAND gate KLMN of module B27 and removes the level that held the integrating one-shot in its unstable state. The PUN READY level disappears immediately, preventing further punching. However, the integrating one-shot does not yet change state, and therefore the motor continues to run. At the end of its 5-sec timing period, the integrating one-shot reverts to its stable state, thereby causing relay K1 to be de-energized and the motor to be stopped. Note that the 5-sec timing period of the integrating one-shot does not begin until clearance of the PUN ACTIVE flip-flop removes the PUN RQ signal that holds the integrating one-shot in the unstable state. If a further PUN RQ signal is generated before the end of the timing period, timing action is immediately halted. Thus, the integrating one-shot does not revert to its stable state and stop the motor until a full 5-sec period has elapsed since the last punch instruction was completed.

CHAPTER 6

OPTIONAL EQUIPMENT

AUTOMATIC PRIORITY INTERRUPT TYPE 172

The optional Automatic Priority Interrupt (API) Type 172 connects up to 16 I/O devices to the program interrupt facility of the PDP-7 processor and allows each device to initiate a program interrupt based on a prewired priority. The API provides direct identification of an interrupting device so that the interrupt subroutine is not required to determine this by scanning device flags. The API also executes multilevel interrupts in which a high-priority device may be granted an interrupt that supersedes an interrupt already in progress. These functions permit more devices to be serviced with greater speed and efficiency.

The API occupies three mounting panels, whose location depends to some extent upon what other options are included in the PDP-7 system. The location of each module within the panels is shown in the API module map, engineering drawing ML-D-172-0-5.

Block Diagram Discussion

The API consists of a control element, a priority chain, and an address selector. The real time clock of the processor is assigned to channel 17_8 of the API. The relationship of these elements to each other and to the processor is shown in Figure 6-1.

When the API option is included in a PDP-7 system, it is connected in place of the real-time clock of the basic system and has a corresponding priority (lower than data break interrupt requests, but higher than program interrupt requests). An interrupt request from a device connected to the API is granted if the following conditions are met:

a. The API is in the enabled condition (by program control).
b. The requesting channel is in the enabled condition (by program control).
c. There is no data interrupt request present or data interrupt in progress.
d. There is no interrupt in progress on a higher priority channel.
e. There is no interrupt in progress on the requesting channel.

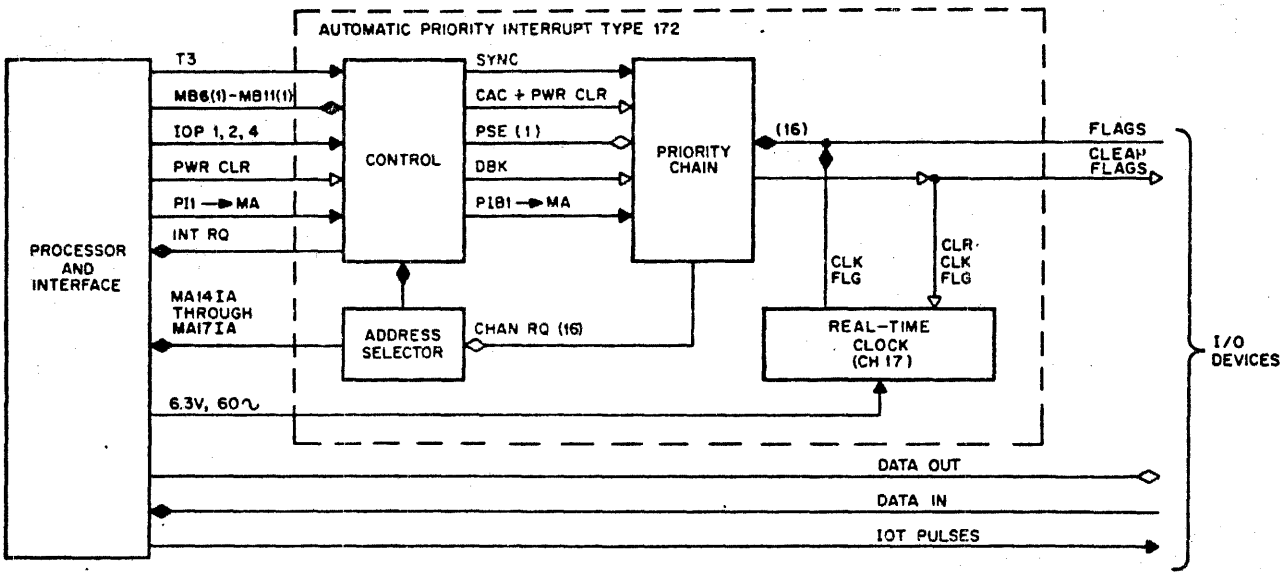


Figure 6-1 Automatic Priority Interrupt Type 172 Block Diagram

Each channel in the API system is assigned a unique, fixed core memory location (40_8 through 57_8). When an interrupt is granted, the next instruction is taken from the memory location assigned to the requesting channel.

Control

The control element contains all the logic required for enabling or disabling the entire priority system or selected channels, in response to IOT instructions. The control element also generates the interrupt request (INT RQ) level signal, which causes the processor to grant an API interrupt (equivalent to a clock break in the basic system) at the first available opportunity.

Priority Chain

The priority chain contains a set of three flip-flops for each channel, designated bXX1, bXX2, and bXX3, where XX represents the channel number. Each bXX1 flip-flop, when set, enables the associated API channel. Setting and clearing of these flip-flops is accomplished by IOT instructions in conjunction with the content of bits 2 through 17 of the accumulator. At time T3, a SYNC pulse opens gates which are conditioned by a bXX1 (1) level and a CH FLG (channel flag) level. The output pulses from gates associated with enabled requesting channels set the associated bXX2 flip-flops. The bXX2 (1) output from the highest priority flip-flop generates a CHAN RQ (channel request) level for the associated channel, and disables gates which

prevent a CHAN RQ level from being generated by channels of lower priority. Only one channel at a time can generate a CHAN RQ level. The channel request level generated by the requesting channel which carries the highest priority is applied to the address selector element, which generates the memory address assigned to that channel and an INT RQ (interrupt request) level. When the processor grants an API break, it generates a PI1 → MA pulse. The PI1 → MA pulse sets the address generated by the address selector into the MA of the processor, and transmits it to the API where it sets the bXX3 (hold break) flip-flop of the requesting channel. The level transition that occurs when the bXX3 flip-flop is set to 1 clears the device flag. This flip-flop remains set until a DBK (debreak) pulse is generated by the control element. It is also cleared by a CAC (clear all channels) instruction.

Address Selector

The address selector consists of four NOR gates which set 1's or 0's into bits 14 through 17 of the MA to produce the memory address of the channel in which a CHAN RQ level is generated. The channel address is transferred into the MA at time T1 of the API break cycle. Circuits are also contained in the API address selector that assure that MA12IA is always a 1 and MA13IA is always a 0 when the API is granted an interrupt; hence the memory address range of $40_8 - 57_8$.

Real-Time Clock

The real-time clock consists of a Schmitt trigger, a pulse amplifier, and a clock flag flip-flop. The Schmitt trigger input receives a 6.3 vac, 60 cps signal from a processor power supply, and the trigger output is coupled to the pulse amplifier, which produces 100-nsec pulses at the rate of 60 per second. Each clock pulse sets the clock flag flip-flop and, if its channel is enabled, requests an API break. One channel (CH 17_8) is assigned to the real-time clock and one is assigned for overflow from the core memory location containing the clock count.

Logical Functions

Channel Allocation

The API provides 16 automatic interrupt channels arranged in a priority chain so that channel 00_8 has the highest priority and channel 17_8 has the lowest priority. Each channel is assigned a

unique, fixed memory location in the range 40_8 (CH 00_8) through 57_8 (CH 17_8). Each I/O device is assigned a unique channel in order of device operating speed. The higher-speed devices are assigned to the higher-priority channels. The priority chain guarantees that if two or more devices request an interrupt concurrently, the first interrupt is granted to the device with the highest priority. When this device has been serviced, further interrupts are granted to the other devices, in order of priority.

Multi-Instruction Subroutine Mode

This mode is generally used to service an I/O device that requires control information from the PDP-7. Such devices are alarms, slow electomechanical devices, teleprinters, punches, etc. Each device requires a servicing subroutine that includes instructions to manipulate data and give further instructions, such as continue, halt, etc., to the interrupting device. When an interrupt is granted, the contents of the channel memory location are transferred to the MB and executed. If the instruction executed is JMS Y, the system operates in the multi-instruction subroutine mode. The contents of the program counter and the condition of the link are stored in location Y, and the device-servicing subroutine starts in Y + 1. (Note that it is often useful to store the content of the AC before servicing the device and to restore the AC prior to exiting from the servicing routine.)

The interrupt flag is normally lowered by the 172, but can be lowered by an IOT instruction if desired. Program control now rests with the servicing routine.

A return to the main program is accomplished by an instruction sequence that restores the AC and link, issues a debreak IOT, and gives a jump indirect to location Y (where the contents of the PC prior to interrupt are stored). The debreaking IOT requires no channel designator, since the interrupt priority chain automatically releases the correct channel and returns it to the receptive state. This IOT normally inhibits all other interrupts for one memory cycle to ensure that the jump indirect Y is executed immediately.

The following program example illustrates the action that takes place during the multi-instruction subroutine mode. Assume an interrupt on channel 03.

Memory Location	Instruction	Operation
1000	ADD 2650	Instruction being executed when interrupt request occurs.
0043	JMS 3000	Instruction executed as a result of interrupt on channel 03. The JMS determines multi-instruction mode.
3000	---	The link, condition of the extend mode, and the PC are stored in location 3000.
3001	DAC 3050	First instruction of servicing routines stores AC.
3002	---	Instructions servicing the interrupting in/out device.
3003	---	
3004	---	
3005	---	
3006	---	
3007	LAC 3050	Restores AC for main program.
3010	DBR	Debreaking IOT releases channel.
3011	JMP I 3000	Return to main program sequence.
1001	---	Next instruction executed from here unless another priority interrupt is waiting.

Single-Instruction Subroutine Mode

In some instances, it is desirable for the PDP-7 to receive information from an external device but not to send control information to the device, such as in the counting of real-time clock pulses to determine elapsed time. The single-instruction subroutine mode simplifies programming a counter.

An interrupt request is subject to the same conditions as in the multi-instruction mode, and the appropriate memory location is addressed as described previously. Then the single-instruction subroutine mode is entered if the channel memory location does not contain a JMS instruction. Normally the instruction is ISZ. In any case, since the single instruction constitutes the entire subroutine, the interrupt system automatically lowers the interrupt flag, debreaks the interrupting channel, and returns the channel to the receptive condition.

If the ISZ instruction is used, the 172 acknowledges only the incrementing operation and neglects the skip to avoid changing the contents of the program counter. If an overflow results from the incrementing, a flag is set. This flag can be entered in another channel or the interrupt system to cause a further program interrupt.

The following program coding illustrates operation in the single instruction subroutine mode. Assume an interrupt on channel 06.

Memory Location	Instruction	Operation
1200	DAC 1600	Operation being executed when interrupt occurs.
0046	ISZ 3200	Instruction executed as a result of break on channel 06. If overflow, flag is set, PC not changed.
1201	LAC 1620	Next instruction in sequence of main program.

Automatic Priority Interrupt Instructions

The following instructions are added to the PDP-7 with the installation of the Type 172 API option. Some instructions, for example CAC and ASC, can be microprogrammed.

Octal Code	Mnemonic	Operation
CAC	705501	Clear all channels. Turn off all channels.
ASC	705502	Enable selected channel(s). AC bits 2 through 17 are used to select the channel(s).
DSC	705604	Disable selected channel(s). AC bits 2 through 17 are used to select the channel(s).
EPI	700004	Enable automatic priority interrupt system. Same as real-time clock CLON.
DPI	700044	Disable automatic priority interrupt system. Same as real-time clock CLOF.
ISC	705504	Initiate break on selected channel (for maintenance purposes). AC bits 2 through 17 are used to select the channel.
DBR	705601	Debreak. Returns highest priority channel to receptive state. Used to exit from multi-instruction subroutine mode.

AC bits 0 to 1 are available for expansion of the basic automatic priority interrupt system to 4 groups of 16 channels.

Circuit Operations

Control

The control circuits generate seven conditioning levels and ten command pulses for the operation of the API system. The logic circuits which produce these signals are shown on engineering drawing BS-D-172-0-2.

The PWR CLR + CAC positive pulse provides a means of collectively clearing all flip-flops contained in the API, either automatically at power turn-on or under program control. The PWR CLR + CAC positive pulse appears at pulse amplifier output terminal E3K. This pulse amplifier is triggered either by PWR CLR POS pulses applied to DCD gate E3E, F, or by IOP1 pulses generated in the processor and inverted by inverter LMN of module E7 (C1, 172-0-2). The inverted pulse is applied to DCD input E3H; and, if the level input of this gate is conditioned by an IO 55 level, the pulse amplifier is triggered and generates the PWR CLR + CAC pulse.

The IO 55 and IO 56 levels are the basic enabling and disabling levels for the entire API system. These levels are generated by decoding the content of bits 6 through 11 of the MB in NAND gates at locations F3 and F4. The IO 55 assertion levels appear at terminals F3E (negative) and F3D (ground). The IO 56 levels appear at terminals F4E (negative) and F4D (ground).

The PSE (1) (priority system enable) negative level conditions the NAND gates associated with channel 00. The PSE (1) ground level conditions a DCD gate, which resets flip-flop b003 in the priority chain when triggered by a COMMON DEBREAK pulse. The PSE (1) levels are generated by the PS ENABLE flip-flop, which is set by an EPI (enable priority interrupt) instruction and reset by a DPI (disable priority interrupt) instruction. These IOT instructions contain a 1 and a 0, respectively, in bit 12, which condition NAND gates JKL and DEF in module A12. An IOT 0004 command pulse, generated in the device selector, triggers whichever gate is conditioned and sets or resets the flip-flop. The PS ENABLE flip-flop must be set by an EPI instruction before the API can initiate an interrupt from any channel.

The ASC 5502 command pulse appears at pulse amplifier output terminal E3U. This pulse amplifier is triggered by an IOP2 pulse generated in the CP and inverted by inverter PRS of module E7. The inverted pulse is applied to DCD input E3P and triggers the pulse amplifier when the gate is conditioned by an IO 55 ground level. The ASC 5502 pulse sets all bXX1 flip-flops of the priority chain whose DCD set gates are conditioned by a 1 in the corresponding bit of the AC.

The DSC 5604 command pulse appears at pulse amplifier output terminal E5K. This pulse amplifier is triggered by an inverted IOP4 pulse applied to DCD input 5E, when the DCD gate is conditioned by an IO 56 ground level. The DSC 5604 pulse resets all bXX1 flip-flops of the priority chain whose DCD reset gates are conditioned by a 1 in the corresponding bit of the AC.

The ISC 5504 command pulse appears at pulse amplifier output terminal E4K. This pulse amplifier is triggered by an inverted IOP4 pulse applied to DCD input terminal E4E, when the gate is conditioned by an IO 55 ground level. The ISC 5504 pulse sets the bXX2 flip-flop of any channel selected by the insertion of a 1 in the corresponding bit of the AC. The setting of the bXX2 flip-flop initiates a break request by the selected channel (or by the highest priority channel if more than one has been selected). This command initiates a break request on the selected channel or on the highest priority channel selected, independent of the channel enable/disable conditions. The channel MUST be disabled if there is no device connected to it. If a device is connected to the channel, the channel can be enabled, but the program must consider the status of the external device. The ISC instruction allows diagnostic routines to initiate a break on any channel, independent of external operations.

The negative INSURE DEBREAK level is generated by the INSURE DEBREAK flip-flop and appears at terminal A15J when the flip-flop is set to 1. This level is applied to terminal J30P of the break control in the CP (drawing BS-D-7-0-32) and forces a $\overline{\text{BK RQ}}$ condition for one cycle at the end of an API break. This ensures that an indirectly addressed JMP instruction providing exit from a break routine will be executed immediately. The INSURE DEBREAK flip-flop is set by any instruction that generates a DBK (debreak) command and is reset to 0 by timing pulse T3 of the following cycle.

The DEBR (debreak) command pulse appears at pulse amplifier output terminal E5 (C3, 172-0-2). This pulse not only sets the INSURE DEBREAK flip-flop, but also triggers a pulse amplifier to produce a COMMON DEBREAK command pulse in the priority chain. The DEBR command pulse is generated by either of the following conditions:

a. An IOP1 pulse, inverted, is combined with an IO 56 ground level in DCD gate PR of module E5 to trigger the pulse amplifier.

b. The INT RECOGNIZED flip-flop is set during time T1 of the API break cycle by a PI1--MA pulse generated in the break control of the CP. The INT RECOGNIZED (1) negative level conditions one input of the NAND gate in module E8. If two other inputs are conditioned by an F (fetch) level and a $\overline{\text{JMS}}$ level, then at time T5 of the fetch cycle the gate is triggered and causes the pulse amplifier to generate the DBK pulse. If the following cycle is also to be a fetch, the F SET level from the major state generator is combined with timing pulse T7 of the current cycle to reset the INT RECOGNIZED flip-flop.

The OVERFLOW FLAG (1) level is generated during an API break in which the instruction in the assigned memory location of the requesting channel is ISZ. If the indexing operation causes an overflow, an MBO CRY (B) pulse triggers gate NPR of module A12 and sets the OVERFLOW FLAG flip-flop. The (1) output is applied to another channel of the priority chain and initiates a break request. The OVERFLOW FLAG flip-flop is cleared when the interrupt is granted.

A SYNC command pulse appears at pulse amplifier output terminal E9N. This pulse amplifier is triggered by NAND gate RNPV of module E8 which is operated at time T3 of each cycle in which the $\overline{\text{INT REC}}$ level and the $\overline{\text{IO DEVICE 56}}$ are both present. The presence of these levels assure that no SYNC pulse will be issued when the API tries to debreak (DEBR) and return to the main program sequence. The SYNC command pulse sets the bXX2 flip-flop of all API channels which have been enabled and are requesting an interrupt with a CH FLAG level.

The PIB1 → MA pulse appears at pulse amplifier output terminal E9H. This pulse amplifier is triggered when a PI1 → MA pulse appears, indicating that an interrupt has been granted. The

PI1 → MA pulse is generated in the processor break control circuits at time T1 of the break cycle, and forces the major state generator to the fetch state. This pulse appears at terminal IL 25H and is identical to the CLOCK 7 → MA pulse of the basic PDP-7 system (B2, BS-D-7-0-32). The PI B1 → MA pulse is applied to all channels of the priority chain, thereby setting flip-flop bXX3 of the highest priority enabled. Setting of this flip-flop turns on the channel and clears the flag of the device to which an interrupt has been granted.

Address Selector

The address selector circuits generate negative levels which condition the input gates of bits 14 through 17 of the MA, thereby setting the memory address assigned to the requesting channel into the MA. The address selector circuits also generate the INT RQ level which sets the API SYNC (CLK SYNC in the basic system) flip-flop of the break control (engineering drawing BS-D-7-0-32). The CHAN RQ (channel request) levels of all channels in the priority chain are applied to the four NOR gates in modules A16, A17, A18, and A19. Only the highest priority requesting channel generates a CHAN RQ level, so that only one address at a time can be set up. In addition to the four MA addressing levels generated by the NOR gates, an MA12IA level is generated with each address by disconnecting the ground jumper on terminal P of module C27 in the MA (B6, BS-D-7-0-29). This wiring modification, in conjunction with the fact that MA13IA is never set to 1 by the PIB → MA pulse (B6, BS-D-7-0-29) produces the desired range of memory locations ($40_8 - 57_8$).

The INT RQ (interrupt request) level appears at terminal A14M. Any address selected by a selected channel causes one or more of the NOR gates to apply a ground output level to the NOR gate in module A20. The INT RQ level is then generated from A20D, unless the PS ENABLE flip-flop is in the 0 state. In that case, the negative PSE (0) level is inverted in module A14 and grounds the INT RQ line.

Priority Chain

Each channel of the priority chain consists of three flip-flops, four NAND gates, an inverter, and a pulse amplifier connected in a configuration that is identical in each channel. The logic of the priority chain is shown on engineering drawing BS-D-172-0-3. Only channel 01 is described below, since all other channels operate in an identical manner.

Channel 01 is enabled when flip-flop b011 is set. The setting pulse is provided by a DCD gate conditioned by a 1 in bit 3 of the AC and triggered by an ASC 5502 command pulse from the control element. Similarly, the channel is disabled when flip-flop b011 is reset by the combination of a 1 in bit 3 of the AC and a DSC 5604 command pulse from the control element. When channel 01 is enabled under program control, the b011 (1) level conditions one input of NAND gate KLMN in module E14 (C2, 172-0-3). Another input is conditioned by a CH 1 FLG (channel 1 flag) level generated in the associated I/O device. At time T3 of the computer cycle, the NAND gate is triggered by a SYNC pulse from the control element; and the output of the gate sets flip-flop b012. This flip-flop may also be set by the combination of a 1 in bit 3 of the AC and an ISC 5504 command pulse from the control element. Use of the ISC instruction causes a break to be initiated on the selected channel without a prior enabling instruction.

NAND gate KLMN in module C10 is conditioned by three levels. The input at terminal M is a negative level indicating that channel 01 is enabled and that the associated device has requested a break. The input at terminal L is a negative level indicating that there is no break already in progress on this channel. The input at terminal K is a negative level indicating that no break is in progress on a channel or higher priority, and that the API system as a whole is enabled. If these conditions are all met, then the gate becomes fully enabled and generates a CHAN 01 RQ (channel 01 request) ground level at terminal C10N. The CHAN 01 RQ level is applied to the control element, where it generates the memory address assigned to channel 01, as well as an interrupt request level, which is applied to the break control of the CP. When the interrupt is granted, the break control generates a command pulse which sets the API address levels into the MA, and causes the control element to generate a PIB1 pulse. This pulse triggers NAND gate DEFH in module C10, since the gate is already conditioned by the priority level and a b012 (1) level. The output of the gate sets the b013 flip-flop to 1. The positive-going level transition which appears at terminal B10S of this flip-flop triggers a pulse amplifier in module B9, and produces a CLR FLG 1 pulse at terminal B9U. This pulse clears the I/O device flag to indicate that an interrupt has been granted.

Note that any bXX2 flip-flop, which is in the 1 state, produces a ground level at terminal H, thereby disabling the associated NAND gate RSTU. The inverted output of a disabled RSTU gate disables inputs D, K, and R of the three NAND gates associated with the next channel of

lower priority. This prevents the lower priority channel from generating either a CHAN RQ or a CLR FLG signal. When the flags of several devices are set concurrently, the bXX2 flip-flop in each of these channels is set by the SYNC pulse. However, the CHAN RQ levels appear one by one, in order of channel priority.

All flip-flops in all channels are cleared by a CAC+PWR CLR pulse generated in the control element at power turn-on or when a CAC (clear all channels) instruction is executed.

While an interrupt is in progress on channel 01, the b013 flip-flop remains set. At the end of the interrupt, both flip-flops b013 and b012 are reset to 0. Flip-flop b013 is reset by a COMMON DEBREAK pulse from the control element, and flip-flop b012 is reset by the level transition of b013. Note that the COMMON DEBREAK pulse triggers a DCD gate condition by a ground level from the channel of next higher priority. Therefore, although the COMMON DEBR pulse is applied to all channels, only the channel to which the interrupt was granted is cleared.

DATA INTERRUPT MULTIPLEXER TYPE 173

Data Interrupt Multiplexer Type 173 consists of 60 FLIP CHIP modules contained in two mounting panels. When this option is added to a standard PDP-7 system, the location of the mounting panels is somewhat dependent upon the number and type of other optional equipment in the system. When the 173 option is designed into a specific PDP-7 system, convenience may require that the multiplexer be located in a specific portion of the console. Module map ML-D-173-0-5 shows the locations of modules within the panels. Data Interrupt Multiplexer Type 173 permits the direct transfer of information between the PDP-7 core memory and one of four high-speed I/O devices which can supply 15 address lines, 18 data lines, a request line, and a transfer direction line. The multiplexer services the devices in a preset priority order and routes the address and data supplied by each device into the data interrupt channel of the standard PDP-7 system. The data interrupt channel has priority over all other interrupt requests. When a data break is granted by the central processor on completion of the current instruction, the transfer takes place during one computer cycle, under the control of the I/O device. The maximum combined transfer rate of four devices connected to the CP through the multiplexer is 570,000 18-bit words per second.

Logical Functions

Figure 6-2 shows a block diagram of the logical elements of the data interrupt multiplexer and their relationship to the central processor. When one or more of the devices connected to the multiplexer generate a channel DATA RQ level (−3 volts), the multiplexer control transmits to the CP a DATA RQ level which causes the DATA SYNC flip-flop in the interrupt control to be set at time T5 DLY (delayed) of the current cycle. At time T6 of the same cycle, the multiplexer control selects the device having the highest priority. When the central processor reaches an "instruction done" situation and grants a break cycle, the following events take place:

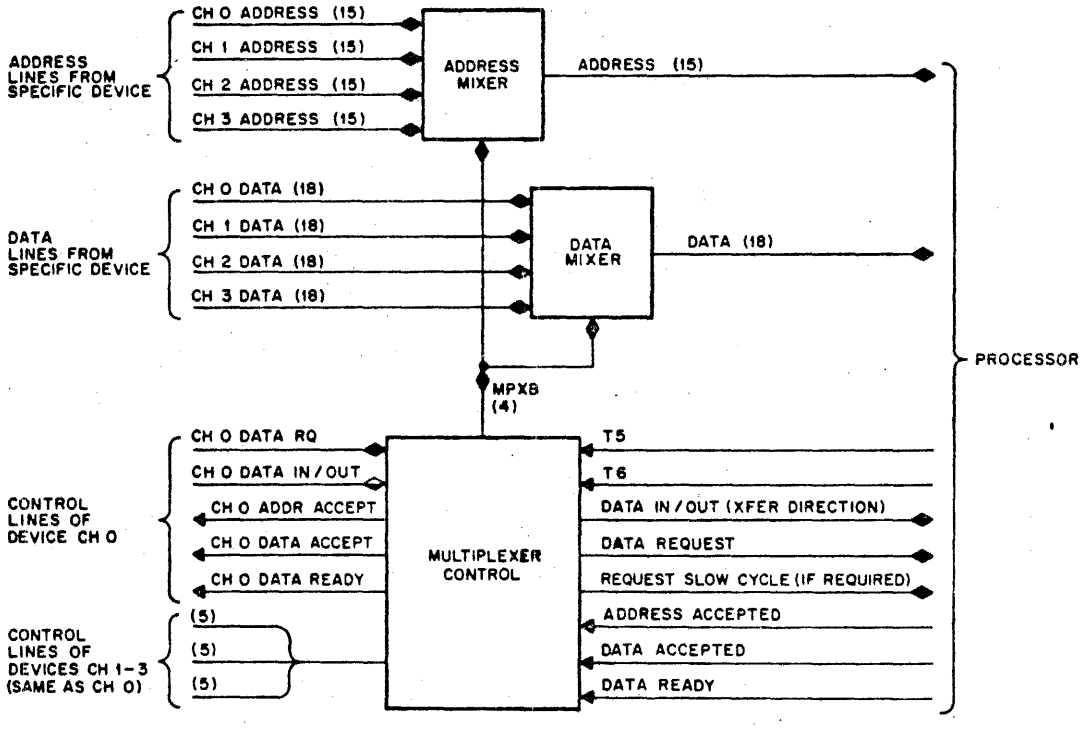


Figure 6-2 Data Interrupt Multiplexer Type 173 Block Diagram

a. At time T1 of the break cycle, the processor transfers the address supplied by the requesting device into the MA, and the multiplexer returns a negative ADDR ACC (address accepted) pulse to the requesting device.

b. At time T3, if an in transfer has been specified, the processor transfers the data supplied by the device into the MB, and the multiplexer returns a DATA ACC (data accepted) pulse to the requesting device.

c. At time T3, if an out transfer has been specified, the information that was stored in the addressed memory cell is held in the MB, and the multiplexer returns a DATA RDY (data ready) pulse to the requesting device, indicating that the requested data is ready for sampling.

d. At time T5 the multiplexer priority chain is cleared and the processor interrogates the DATA RQ line.

e. If the DATA RQ line is still at −3 volts, the processor grants another break cycle, and the events described in a through d are repeated until all requesting devices have been serviced in order of priority. If the DATA RQ line is at ground, indicating that there is no further data request, the processor fetches and executes the next programmed instruction.

Circuit Operations

The following discussion of the detailed operation of Data Interrupt Multiplexer Type 173 is based on engineering logic drawings BS-D-173-0-2 and BS-D-173-0-3. References to these drawings are given in full. Reference is also made to the break control of the central processor, shown on engineering logic diagram D-7-0-32; such references are identified by the number 32 in parentheses.

Data Interrupt Multiplexer Control

Each of the four I/O devices which may be connected to the multiplexer must supply a −3 volt CH X DATA RQ level when it is ready to receive or transmit data. The four request lines are OR combined in module A3 of the multiplexer (C5, D-173-0-2). A data request from any or all of the four I/O devices results in the transmission of a negative DATA RQ level to the break control of the central processor. This DATA RQ level is AND combined with timing pulse T5 DLY to set the DATA SYNC flip-flop (A1, 32). In the break control, the DATA SYNC (1) level is inverted in NOR gate NPRSV of module L22 (A7, 32) to produce a negative BK RQ level which is applied to the major state generator. When the processor reaches an "instruction done" situation, the major state generator establishes a break state. The B (break) and DATA SYNC (1) levels are combined to produce a DATA·B level.

In the multiplexer, the CH X DATA RQ level conditions a gate which is triggered by timing pulse T6 of the current computer cycle to set the associated MPX flip-flop. There are four flip-flops, designated MPX0 through MPX3. The inverted (1) level of each flip-flop holds all flip-flops of lower priority in the 0 state by pull-over action. Thus, only one flip-flop at a time can be set, and if two or more I/O devices have generated a DATA RQ level concurrently, the MPX flip-flop which is set at time T6 will be that associated with the device of highest priority.

The MPX (1) level performs five functions, as follows:

a. It conditions the address mixer gates which connect the address lines of the requesting device to the MA.

b. It conditions the data mixer gates which connect the data lines of the requesting device to the MB.

c. It is NAND combined in module A6 with the CH RQ IN level to produce a DATA IN level for transmission to the break control of the processor.

d. It is applied to one input of a two-input diode AND gate in a Type R141 module at location A5. The outputs of the seven gates in this module are NOR combined. As supplied, the second input of each gate is disabled by a ground connection; however, if any of the four I/O devices requires a slow cycle, the associated gate may be conditioned by the CH DATA RQ and MPXB negative levels to generate a negative RQ SLOW CYC level for transmission to the processor timing circuits.

e. It is applied to the input of a bus driver, whose output conditions three NAND gates contained in a Type R111 module. The Type R111 modules for channels 0 through 3 are at locations C12 through C15, respectively. In each channel, one NAND gate is triggered by an ADDR ACC (address accepted) pulse from the processor; the output of the gate causes an associated Type W607 pulse amplifier to transmit a CHX ADDR ACC (channel address accepted) pulse to the requesting device. The second of these gates is triggered

by a DATA ACC (data accepted) pulse during an inward transfer, and causes the associated pulse amplifier to transmit a CHX DATA ACC pulse to the requesting device. The third gate is triggered during an outward transfer by a DATA RDY (data ready) pulse, and causes the associated pulse amplifier to transmit a CHX DATA RDY pulse to the requesting device. The three control pulses (ADDR ACC, DATA ACC, and DATA RDY) are generated in the processor (as the DATA ADDR → MA, DATA INFO → MB, and MB INFO → OUT pulses, respectively) and are transmitted to the multiplexer control.

At time T5, timing pulse T5 (inverted) is applied to the direct clear inputs of all four MPX flip-flops and resets them to 0. If no other I/O device has generated at CH DATA RQ level in the meantime, the DATA RQ line is at ground and permits timing pulse T5 DLY to clear the DATA SYNC flip-flop in the break control. At the conclusion of the break cycle, the processor will then fetch and execute the next programmed instruction. If, however, a further CH DATA RQ level has been generated, the DATA SYNC flip-flop will remain set and the processor will grant further data break cycles until all requesting devices have been serviced in order of priority.

Address Mixer and Data Mixer

The address mixer consists of 15 Type R141 Diode Gate modules at locations B10 through B24, and 3 Type B105 Inverter modules each containing 5 inverters. Each Type 141 module contains seven two-input diode AND gates whose outputs are NOR combined. Three of these diode AND gates are unused. In the remaining four gates, one input is conditioned by one of the MPXB levels; the other input is conditioned by an address line from the associated device. The ground level that appears at terminal D of the Type R141 module when one of its gates is enabled is applied to an inverter of the Type B105 module. The resulting negative level conditions the input gate of the corresponding bit of the MA.

The data mixer is similar in operation to the address mixer, except that the input gates are conditioned by the device data lines and that there are 18 bits instead of 15. The Type 141 modules are located at positions A7 through A24, and the Type B105 modules at positions B3, B4, C1,

and C2. Each inverter in each mixer is equipped with a 15-milliampere clamped load; these loads are contained in Type W005 modules at locations C6 through C8.

EXTENDED ARITHMETIC ELEMENT TYPE 177

The Extended Arithmetic Element (EAE) Type 177 is a standard option for the PDP-7 to facilitate high-speed multiplication, division, shifting, and register manipulation. The EAE contains an 18-bit multiplier quotient register (MQ), a 6-bit step counter register (SC), two sign registers and the EAE control logic. The two panels of EAE logic are installed just below the operator console in bay 2 of the PDP-7 computer. The content of the MQ register is continually displayed on the operator console just below the ACCUMULATOR indicators.

The Extended Arithmetic Element hardware operates asyncronously to the basic computer cycle, permitting computations to be performed in the minimum possible time. Further, since the EAE instructions are microprogrammed, it is usually possible to simplify programming and shorten computation time by microcoding exactly the arithmetic operation desired.

Logical Functions

Instructions

The EAE instructions are broken up into two parts: The first part permits register manipulation as microprogrammed in the instruction while data is being fetched; the second part is the specified operation itself. Signed and unsigned multiplication would, for example, differ in the microprogrammed first part where the sign manipulation is done. The bit configuration for the EAE instructions is shown in Figure 6-3 and defined in Table 6-1. The set-up phase of the instruction is broken up into three event times. Microprogramming for all but the set-up commands uses only the first two event times. The bits corresponding to the third event time then specify the step count of commands such as multiply, divide, and the shifts. The unassigned operation code (010) should not be used as it is reserved for future EAE expansion.

TABLE 6-1 EAE BIT ASSIGNMENTS AND OPERATIONS

Bit Positions	Bits	Function
0, 1, 2, 3	1101	EAE operation code.
4	1	Place the AC sign in the link. Used for signed operations.
5	1	Clear the MQ.
6	1	Read the AC sign into the EAE AC sign register prior to carrying out a stepped operation. Used for the signed operations multiply and divide.
6, 7	10	Take the absolute value of the AC. Takes place after the AC sign is read into the EAE AC sign.
7	1	Inclusive OR the AC with the MQ and read into MQ. (If bit 5 is a 1, this reads the AC into the MQ).
8	1	Clear the AC.
9, 10, 11	000	Setup. Specifies no stepped EAE operation, and enables the use of bits 15, 16, and 17. It is used as a preliminary to multiplying, dividing, and shifting signed numbers. Execution time is one cycle.
9, 10, 11	001	Multiply. Causes the number in the MQ to be multiplied by the number in the memory location following this instruction. If the EAE AC sign register is 1, the MQ will be complemented prior to multiplication. The exclusive OR of the EAE AC sign and the link will be placed in the EAE sign register (the sign of product and quotient). The product is left in the AC and MQ, with the lowest order bit in MQ bit 17. The program continues at the location of this instruction plus two. At the completion of this instruction the link is cleared and if the EAE sign was 1, the AC and MQ are

TABLE 6-1 EAE BIT ASSIGNMENTS AND OPERATIONS (continued)

Bit Positions	Bits	Function
9, 10, 11	001 (continued)	complemented. The step count of this instruction should be 22 (octal) for a 36-bit multiplication, but can be varied to speed up the operation. The execution time is 4.2 to 8.7 μsec, depending on number of 1 bits in the MQ.
9, 10, 11	010	This is an unused operation code reserved for possible future expansion.
9, 10, 11	011	Divide. Causes the 36-bit number in the AC and MQ to be divided by the 18-bit number in the register following the instruction. If the EAE AC sign is 1, the MQ is complemented prior to starting the division. The magnitude of the AC is taken by microprogramming the instruction. The exclusive OR of the AC sign and the link are placed in the EAE sign. The part of the dividend in the AC must be less than the divisor or overflow occurs. In that case the link is set at the end of the divide; otherwise, the link is cleared. At the completion of this instruction, if the EAE sign was a 1, the MQ is complemented; and if the EAE AC sign was 1, the AC is complemented. Thus the remainder has the same sign as the dividend. The step count of this instruction is normally 23 (octal) but can be decreased for certain operations. The execution time is 3.5 μsec in the case of divide overflow or from 9.0-12.6 μsec otherwise.
9, 10, 11	101	Long right shift. Causes the AC and MQ to be shifted right together as a 36-bit register the number of times specified in the step count of the instruction. On each step the link fills AC bit-0, AC bit-17 fills MQ bit-0, and MQ bit-17 is lost. The link remains unchanged. The time is 0.1 n + 1.6 μsec, where n is the step count.

TABLE 6-1 EAE BIT ASSIGNMENTS AND OPERATIONS (continued)

Bit Positions	Bits	Function
9, 10, 11	110	Long left shift. Causes the AC and MQ to be shifted left together the number of times specified in the step count of the instruction. On each step, MQ bit 17 is filled by the link; the link remains unchanged. MQ bit 0 fills AC bit 17 and AC bit 0 is lost. The time is 0.1 n + 1.6 μsec, where n is the shift count.
9, 10, 11	100	Normalize. Causes the AC and MQ to be shifted left together until either the step count is exceeded or AC bit 0 ≠ AC bit 1. MQ bit 17 is filled by the link, but the link is not changed. The step count of this instruction would normally be 44 (octal). When the step counter is read into the AC, it contains the number of shifts minus the initial shift count as a 2's complement 6-bit number. The time is 0.1 n + 1.6 μsec, where n is the number of steps in the shift counter or the number required to effect normalization, whichever is less.
9, 10, 11	111	Accumulator left shift. Causes the AC to be shifted left the number of times specified in the shift count. AC bit 17 is filled by the link, but the link is unchanged. The time is 0.1 n + 1.6 μsec, where n is the step count.
12-17		Specify the step count except in the case of the setup command, which does not change the step counter.
15	1	On the setup command only, causes the MQ to be complemented.
16	1	On the setup command only, causes the MQ to be inclusive ORed with the AC and the result placed in AC. (If the AC has been cleared, this will place the MQ into the AC).
17	1	On the setup command only, causes the AC to be inclusive ORed with the SC and the results placed in AC bits 12-17. (If the AC has been cleared, this will place the SC into the AC).

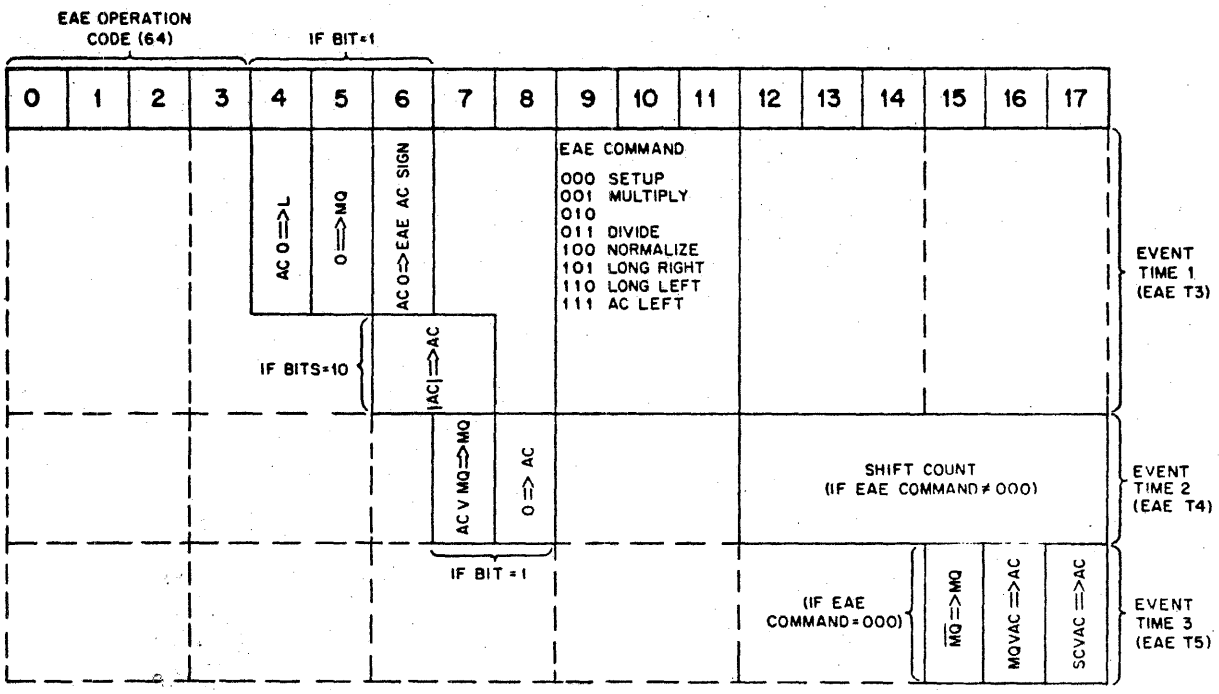


Figure 6-3 EAE Instruction Bit Assignment

Execution of Instructions

EAE instructions which do not require reference to memory take one computer fetch cycle plus the time required to complete the EAE operations. The processor timing chain is stopped at the end of the fetch cycle, and is restarted when EAE operations are complete.

EAE instructions which require reference to memory (to fetch an argument) occupy a fetch cycle and a hybrid cycle, plus the time required to complete the EAE operations. During the fetch cycle, the EAE instruction is fetched from memory and partially executed. During the first portion of the augment fetch cycle, the normal events of a fetch cycle occur; that is, at time T1 the IR is cleared, the content of the PC is transferred to the MA and is then incremented by 1; at time T2 the MB is cleared and a read operation is initiated, the content of the addressed cell being strobed into the MB between times T2 and T3, and the READ flip-flops being cleared at time T3. These events result in the argument being retrieved from the memory location immediately following the location which contained the EAE instruction. At time T3 of the hybrid cycle a START MUL, DIV pulse generated in the EAE forces the major state generator to the execute state and at the same time forces the operation code for DZM (14_8, or IA0, IB3) into the instruction register. During the remainder of this cycle, the processor writes the content

of the MB back into memory; then the EAE generates a STOP CP TC level which prevents timing pulse TP7 from being returned to the start of the processor timing chain and so stops the timing circuits of the processor. EAE operations are then timed and counted by logic elements of the EAE and multiplication or division starts. At the conclusion of these operations, a START CP TC pulse restarts the processor timing chain, permitting the processor to fetch and execute the next instruction.

Sheet 1 of the EAE Flow Diagram, engineering drawing FD-D-177-0-2, shows the possible sequences of events during a fetch cycle in which an EAE instruction is fetched, and the events which take place at times T2 and T3 of an ensuing hybrid cycle (in which an argument is fetched). Sheet 2 of the EAE Flow Diagram shows the events which take place under control of the EAE timing, during the period when the processor timing chain is inhibited. Operations concerned with starting and ending the EAE sequence are shown in the top right portion of the diagram; the last point in the START/END sequence, designated ENTRY, may lead into the Multiply, Divide, or Shift sequences. Multiply or Divide sequences also entail entry into the ADDER/SUBTRACTOR sequence. The counting process performed by the step counter register is shown at the bottom left of this flow diagram, and the events which take place when the SC register overflows (indicating that all required steps have been performed) are shown at the bottom right.

Program examples of the use of the EAE are given in the PDP-7 Users Handbook, F-75.

Circuit Operations

The logical circuits of the EAE are shown on block schematic engineering drawings BS-D-177-0-4 through BS-D-177-0-9. Drawing BS-D-7-0-40 shows special control signal interface between the processor and the EAE option. Refer to these drawings when analizing the circuit operations of this option.

CHAPTER 7

INTERFACE

INTERFACE CONNECTIONS AND SIGNAL IDENTIFICATION

All signals passing between the processor of the PDP-7 and the peripheral equipment are routed through the interface section of the computer. Interface connections are made either by coaxial cable or by ribbon cables terminated in a Type W021 Signal Cable Connector. This cable connector is described in detail in the Digital FLIP CHIP Modules Catalog, C-105. The cable connector plugs into the appropriate FLIP CHIP module receptacle. Interface cable connections made to the module mounting panels of the processor are shown on engineering drawing CL-D-7-0-38 with detailed signal and terminal identification information. The interface is so designed that the information collector and information distributor can be expanded (with suitable bus drivers) almost indefinitely to support any desired array of peripheral equipment, up to the most expansive computing system imaginable.

All logic signals that pass between the PDP-7 and the I/O equipment are standard DEC levels or standard DEC pulses. Logic signals are assigned mnemonic names that indicate the condition represented by assertion of the signal. Standard levels are either ground potential (0.0 to 0.3v) designated by an open diamond (———◇) or are −3v (−3.0 to −4.0v) designated by a solid diamond (———◆). Standard pulses in the positive direction are designated by an open triangle (———▷), and negative pulses are designated by a solid triangle (———▶). Pulses originating in R series modules are positive-going pulses which start at −3v, go to ground for 100 nsec, then return to −3v. Pulses originating in W series modules are bipolar, are always referenced to ground, are 2.5v in amplitude (2.3 to 3.0v) with a 2v overshoot, and are of 400-nsec duration (or 1 μsec if selected on the W640).

Tables 7-1 and 7-2 provide cable connections and logic circuit identification for basic PDP-7 interface signals.

TABLE 7-1 OUTPUT SIGNALS

Signal	Symbol	Signal Origin				
		Interface Connection	Terminal	Module Type	Logic	Block Schematic Drawing
ACB0(1)	—◇	1L1D- 1L9D	1K3J	R650	Information Distributor	BS-D-7-0-34
ACB1(1)	—◇	1L1E- 1L9E	1K3T	R650	Information Distributor	BS-D-7-0-34
ACB2(1)	—◇	1L1H- 1L9H	1K4J	R650	Information Distributor	BS-D-7-0-34
ACB3(1)	—◇	1L1K- 1L9K	1K4T	R650	Information Distributor	BS-D-7-0-34
ACB4(1)	—◇	1L1M- 1L9M	1K5J	R650	Information Distributor	BS-D-7-0-34
ACB5(1)	—◇	1L1P- 1L9P	1K5T	R650	Information Distributor	BS-D-7-0-34
ACB6(1)	—◇	1L1S- 1L9S	1K6J	R650	Information Distributor	BS-D-7-0-34
ACB7(1)	—◇	1L1T- 1L9T	1K6T	R650	Information Distributor	BS-D-7-0-34
ACB8(1)	—◇	1L1V- 1L9V	1K7J	R650	Information Distributor	BS-D-7-0-34
ACB9(1)	—◇	1M1D- 1M9D	1K7T	R650	Information Distributor	BS-D-7-0-34
ACB10(1)	—◇	1M1E- 1M9E	1K8J	R650	Information Distributor	BS-D-7-0-34
ACB11(1)	—◇	1M1H- 1M9H	1K8T	R650	Information Distributor	BS-D-7-0-34
ACB12(1)	—◇	1M1K- 1M9K	1K9J	R650	Information Distributor	BS-D-7-0-34
ACB13(1)	—◇	1M1M- 1M9M	1K9T	R650	Information Distributor	BS-D-7-0-34
ACB14(1)	—◇	1M1P- 1M9P	1K10J	R650	Information Distributor	BS-D-7-0-34
ACB15(1)	—◇	1M1S- 1M9S	1K10T	R650	Information Distributor	BS-D-7-0-34

TABLE 7-1 OUTPUT SIGNALS (continued)

Signal	Symbol	Signal Origin				
		Interface Connection	Terminal	Module Type	Logic	Block Schematic Drawing
ACB16(1)	⟶◇	1M1T- 1M9T	1K11J	R650	Information Distributor	BS-D-7-0-34
ACB17(1)	⟶◇	1M1V- 1M9V	1K11T	R650	Information Distributor	BS-D-7-0-34
IOT 7001	⟶▶	2D13D	2C13H	W640	Device Selector	BS-D-7-0-36
IOT 7002	⟶▶	2D11D	2C13N	W640	Device Selector	BS-D-7-0-36
IOT 7004	⟶▶	2D11E	2C13U	W640	Device Selector	BS-D-7-0-36
IOT 7101	⟶▶	2D13E	2C14H	W640	Device Selector	BS-D-7-0-36
IOT 7102	⟶▶	2D11H	2C14N	W640	Device Selector	BS-D-7-0-36
IOT 7104	⟶▶	2D11K	2C14U	W640	Device Selector	BS-D-7-0-36
IOT 7201	⟶▶	2D13H	2C15H	W640	Device Selector	BS-D-7-0-36
IOT 7202	⟶▶	2D11M	2C15N	W640	Device Selector	BS-D-7-0-36
IOT 7204	⟶▶	2D11P	2C15U	W640	Device Selector	BS-D-7-0-36
IOT 7301	⟶▶	2D13K	2C16H	W640	Device Selector	BS-D-7-0-36
IOT 7302	⟶▶	2D11S	2C16N	W640	Device Selector	BS-D-7-0-36
IOT 7304	⟶▶	2D13M	2C16U	W640	Device Selector	BS-D-7-0-36
IOT 7401	⟶▶	2D11T, 2D13P	2C17H	W640	Device Selector	BS-D-7-0-36
IOT 7402	⟶▶	2D11V	2C17N	W640	Device Selector	BS-D-7-0-36

TABLE 7-1 OUTPUT SIGNALS (continued)

Signal	Symbol	Signal Origin				
		Interface Connection	Terminal	Module Type	Logic	Block Schematic Drawing
IOT 7404	→	2D12K, 2D13S	2C17U	W640	Device Selector	BS-D-7-0-36
IOT 7501	→	2D14D	2C18H	W640	Device Selector	BS-D-7-0-36
IOT 7501(B)	→	2D14M, 2D15D	2C18H	W640	Device Selector	BS-D-7-0-36
IOT 7502	→	2D14E, 2D15H	2C18N	W640	Device Selector	BS-D-7-0-36
IOT 7504	→	2D14H	2C18U	W640	Device Selector	BS-D-7-0-36
IOT 7601	→	2D15K	2C19H	W640	Device Selector	BS-D-7-0-36
IOT 7602	→	2D15M	2C19N	W640	Device Selector	BS-D-7-0-36
IOT 7604	→	2D14K	2C19U	W640	Device Selector	BS-D-7-0-36
MBB0(1)	→	2C3D	1B22D	B684	MB Bus Drivers	BS-D-7-0-35
MBB1(1)	→	2C3E	1B22N	B684	MB Bus Drivers	BS-D-7-0-35
MBB2(1)	→	2C3H	1B23D	B684	MB Bus Drivers	BS-D-7-0-35
MBB3(1)	→	2C3K	1B23N	B684	MB Bus Drivers	BS-D-7-0-35
MBB4(1)	→	2C3M	1B24D	B684	MB Bus Drivers	BS-D-7-0-35
MBB5(1)	→	2C3P	1B24N	B684	MB Bus Drivers	BS-D-7-0-35
MBB6(1)	→	2C3S	1B25D	B684	MB Bus Drivers	BS-D-7-0-35
MBB7(1)	→	2C3T	1B25N	B684	MB Bus Drivers	BS-D-7-0-35

TABLE 7-1 OUTPUT SIGNALS (continued)

Signal	Symbol	Signal Origin				
		Interface Connection	Terminal	Module Type	Logic	Block Schematic Drawing
MBB8(1)	——◆	2C3V	1B26D	B684	MB Bus Drivers	BS-D-7-0-35
MBB9(1)	——◆	2C3D	1B26N	B684	MB Bus Drivers	BS-D-7-0-35
MBB10(1)	——◆	2C4E	1B27D	B684	MB Bus Drivers	BS-D-7-0-35
MBB11(1)	——◆	2C4H	1B27N	B684	MB Bus Drivers	BS-D-7-0-35
MBB12(1)	——◆	2C4K	1B28D	B684	MB Bus Drivers	BS-D-7-0-35
MBB13(1)	——◆	2C4M	1B28N	B684	MB Bus Drivers	BS-D-7-0-35
MBB14(1)	——◆	2C4P	1B29D	B684	MB Bus Drivers	BS-D-7-0-35
MBB15(1)	——◆	2C4S	1B29N	B684	MB Bus Drivers	BS-D-7-0-35
MBB16(1)	——◆	2C4T	1B30D	B684	MB Bus Drivers	BS-D-7-0-35
MBB17(1)	——◆	2C4V	1B30N	B684	MB Bus Drivers	BS-D-7-0-35
MBB6(0)	——◆	2C1D	B9D	B684	MB Bus Drivers	BS-D-7-0-35
MBB7(0)	——◆	2C1E	B9N	B684	MB Bus Drivers	BS-D-7-0-35
MBB8(0)	——◆	2C1H	B11D	B684	MB Bus Drivers	BS-D-7-0-35
MBB9(0)	——◆	2C1K	B11N	B684	MB Bus Drivers	BS-D-7-0-35
MBB10(0)	——◆	2C1M	B13D	B684	MB Bus Drivers	BS-D-7-0-35
MBB11(0)	——◆	2C1P	B13N	B684	MB Bus Drivers	BS-D-7-0-35

TABLE 7-1 OUTPUT SIGNALS (continued)

Signal	Symbol	Signal Origin				
		Interface Connection	Terminal	Module Type	Logic	Block Schematic Drawing
MBB12(0)	——◆	2C1S	B15D	B684	MB Bus Drivers	BS-D-7-0-35
BGN(B)	——▶	---	2C28U	W640	Timing	BS-D-7-0-22
NEG PWR CLR	——▶	---	2C28H	W640	Spec. Cyc.	BS-D-7-0-20
PWR CLR	——▷	---	1C28P	W640	Spec. Cyc.	BS-D-7-0-20
DATA ADDR ACC	——▶	---	1L16H	W607	Interrupt Control	BS-D-7-0-32
DATA ACC	——▶	---	1L16N	W607	Interrupt Control	BS-D-7-0-32
DATA RDY	——▶	---	1L16U	W607	Interrupt Control	BS-D-7-0-32

TABLE 7-2 INPUT SIGNALS

Signal	Symbol	Signal Destination				
		Interface Connection	Terminal	Module Type	Logic	Block Schematic Drawing
RB0	——◆	1N15D	1M15F	R141	Information Collector	BS-D-7-0-33
RB1	——◆	1N15E	1M16	R141	Information Collector	BS-D-7-0-33
RB2	——◆	1N15H	1M17F	R141	Information Collector	BS-D-7-0-33
RB3	——◆	1N15K	1M18F	R141	Information Collector	BS-D-7-0-33
RB4	——◆	1N15M	1M19F	R141	Information Collector	BS-D-7-0-33
RB5	——◆	1N15P	1M20F	R141	Information Collector	BS-D-7-0-33

TABLE 7-2 INPUT SIGNALS (continued)

Signal	Symbol	Signal Origin				
		Interface Connection	Terminal	Module Type	Logic	Block Schematic Drawing
RB6	——◆	1N15S	1M21F	R141	Information Collector	BS-D-7-0-33
RB7	——◆	1N15T	1M22F	R141	Information Collector	BS-D-7-0-33
RB8	——◆	1N15V	1M23F	R141	Information Collector	BS-D-7-0-33
RB9	——◆	1N16D	1M24F	R141	Information Collector	BS-D-7-0-33
RB10	——◆	1N16E	1M25F	R141	Information Collector	BS-D-7-0-33
RB11	——◆	1N16H	1M26F	R141	Information Collector	BS-D-7-0-33
RB12	——◆	1N16K	1M27F	R141	Information Collector	BS-D-7-0-33
RB13	——◆	1N16M	1M28F	R141	Information Collector	BS-D-7-0-33
RB14	——◆	1N16P	1M29F	R141	Information Collector	BS-D-7-0-33
RB15	——◆	1N16S	1M30F	R141	Information Collector	BS-D-7-0-33
RB16	——◆	1N16T	1M31F	R141	Information Collector	BS-D-7-0-33
RN17	——◆	1N16V	1M32F	R141	Information Collector	BS-D-7-0-33
MQ1 ——▶ AC	——▶	1N32S	1M15K	R141	Information Collector	BS-D-7-0-33
MQ	——◆	N19D	1M15L	R141	Information Collector	BS-D-7-0-33
MQ1	——◆	N19E	1M16L	R141	Information Collector	BS-D-7-0-33
MQ2	——◆	N19H	1M17L	R141	Information Collector	BS-D-7-0-33

TABLE 7-2 INPUT SIGNALS (continued)

Signal	Symbol	Signal Destination				
		Interface Connection	Terminal	Module Type	Logic	Block Schematic Drawing
MQ3	——◆	N19K	1M18L	R141	Information Collector	BS-D-7-0-33
MQ4	——◆	N19M	1M19L	R141	Information Collector	BS-D-7-0-33
MQ5	——◆	N19P	1M20L	R141	Information Collector	BS-D-7-0-33
MQ6	——◆	N19S	1M21L	R141	Information Collector	BS-D-7-0-33
MQ7	——◆	N19T	1M22P	R141	Information Collector	BS-D-7-0-33
MQ8	——◆	N19V	1M23L	R141	Information Collector	BS-D-7-0-33
MQ9	——◆	N20D	1M24L	R141	Information Collector	BS-D-7-0-33
MQ10	——◆	N20E	1M25L	R141	Information Collector	BS-D-7-0-33
MQ11	——◆	N20H	1M26L	R141	Information Collector	BS-D-7-0-33
MQ12	——◆	N20K	1M27L	R141	Information Collector	BS-D-7-0-33
MQ13	——◆	N20M	1M28L	R141	Information Collector	BS-D-7-0-33
MQ14	——◆	N20P	1M29L	R141	Information Collector	BS-D-7-0-33
MQ15	——◆	N20S	1M30L	R141	Information Collector	BS-D-7-0-33
MQ16	——◆	N20T	1M31L	R141	Information Collector	BS-D-7-0-33
MQ17	——◆	N20V	1M32L	R141	Information Collector	BS-D-7-0-33
DT10	——◆	N21D	1M15N	R141	Information Collector	BS-D-7-0-33

TABLE 7-2 INPUT SIGNALS (continued)

Signal	Symbol	Signal Destination				
		Interface Connection	Teminal	Module Type	Logic	Block Schematic Drawing
DT11	——◆	N21E	1M16N	R141	Information Collector	BS-D-7-0-33
DT12	——◆	N21H	1M17N	R141	Information Collector	BS-D-7-0-33
DT13	——◆	N21K	1M18N	R141	Information Collector	BS-D-7-0-33
DT14	——◆	N21M	1M19N	R141	Information Collector	BS-D-7-0-33
DT15	——◆	N21P	1M20N	R141	Information Collector	BS-D-7-0-33
DT16	——◆	N21S	1M21N	R141	Information Collector	BS-D-7-0-33
DT17	——◆	N21T	1M22N	R141	Information Collector	BS-D-7-0-33
DT18	——◆	N21V	1M23N	R141	Information Collector	BS-D-7-0-33
DT19	——◆	N22D	1M24N	R141	Information Collector	BS-D-7-0-33
DT110	——◆	N22E	1M25N	R141	Information Collector	BS-D-7-0-33
DT111	——◆	N22H	1M26N	R141	Information Collector	BS-D-7-0-33
DT112	——◆	N22K	1M27N	R141	Information Collector	BS-D-7-0-33
DT113	——◆	N22M	1M28N	R141	Information Collector	BS-D-7-0-33
DT114	——◆	N22P	1M29N	R141	Information Collector	BS-D-7-0-33
DT115	——◆	N22S	1M30N	R141	Information Collector	BS-D-7-0-33
DT116	——◆	N22T	1M31N	R141	Information Collector	BS-D-7-0-33

TABLE 7-2 INPUT SIGNALS (continued)

Signal	Symbol	Signal Destination				
		Interface Connection	Terminal	Module Type	Logic	Block Schematic Drawing
DTI17	——◆	N22V	1M32N	R141	Information Collector	BS-D-7-0-33
CA5	——◆	N23P	1M20R	R141	Information Collector	BS-D-7-0-33
CA6	——◆	N23S	1M21R	R141	Information Collector	BS-D-7-0-33
CA7	——◆	N23T	1M22R	R141	Information Collector	BS-D-7-0-33
CA8	——◆	N23V	1M23R	R141	Information Collector	BS-D-7-0-33
CA9	——◆	N24D	1M24R	R141	Information Collector	BS-D-7-0-33
CA10	——◆	N24E	1M25R	R141	Information Collector	BS-D-7-0-33
CA11	——◆	N24H	1M26R	R141	Information Collector	BS-D-7-0-33
CA12	——◆	N24K	1M27R	R141	Information Collector	BS-D-7-0-33
CA13	——◆	N24M	1M28R	R141	Information Collector	BS-D-7-0-33
CA14	——◆	N24P	1M29R	R141	Information Collector	BS-D-7-0-33
CA15	——◆	N24S	1M30R	R141	Information Collector	BS-D-7-0-33
CA16	——◆	N24T	1M31R	R141	Information Collector	BS-D-7-0-33
CA17	——◆	N24V	1M32R	R141	Information Collector	BS-D-7-0-33
DATA FLG/ LP FLAG	——◆	N25D	1M15T	R141	Information Collector	BS-D-7-0-33
BLOCK FLG/STOP FLAG	——◆	N25E	1M16T	R141	Information Collector	BS-D-7-0-33

TABLE 7-2 INPUT SIGNALS (continued)

Signal	Symbol	Signal Destination				
		Interface Connection	Terminal	Module Type	Logic	Block Schematic Drawing
ERR-FLG	——◆	N25H	1M17T	R141	Information Collector	BS-D-7-0-33
OFF END	——◆	N25K	1M18T	R141	Information Collector	BS-D-7-0-33
TIMING ERR	——◆	N25M	1M19T	R141	Information Collector	BS-D-7-0-33
REVERSE	——◆	N25P	1M20T	R141	Information Collector	BS-D-7-0-33
GO	——◆	N25S	1M21T	R141	Information Collector	BS-D-7-0-33
MARK TRK ERR	——◆	N25T	1M22T	R141	Information Collector	BS-D-7-0-33
UNABLE	——◆	N25V	1M23T	R141	Information Collector	BS-D-7-0-33
TT1	——◆	N26E	1M25T	R141	Information Collector	BS-D-7-0-33
TT2	——◆	N26H	1M26T	R141	Information Collector	BS-D-7-0-33
TT3	——◆	N26K	1M27T	R141	Information Collector	BS-D-7-0-33
TT4	——◆	N26M	1M28T	R141	Information Collector	BS-D-7-0-33
TT5	——◆	N26P	1M29T	R141	Information Collector	BS-D-7-0-33
TT6	——◆	N26S	1M30T	R141	Information Collector	BS-D-7-0-33
TT7	——◆	N26T	1M31T	R141	Information Collector	BS-D-7-0-33
TT8	——◆	N26V	1M32T	R141	Information Collector	BS-D-7-0-33
DR LATE	——◆	N27D	1M15V	R141	Information Collector	BS-D-7-0-33

TABLE 7-2 INPUT SIGNALS (continued)

Signal	Symbol	Signal Destination				
		Interface Connection	Terminal	Module Type	Logic	Block Schematic Drawing
PARITY ERR	——◆	N27E	1M16V	R141	Information Collector	BS-D-7-0-33
READ COMP ERR	——◆	N27H	1M17V	R141	Information Collector	BS-D-7-0-33
EOF	——◆	N27K	1M18V	R141	Information Collector	BS-D-7-0-33
WRITE LOCK	——◆	N27M	1M19V	R141	Information Collector	BS-D-7-0-33
LOAD POINT	——◆	N27P	1M20V	R141	Information Collector	BS-D-7-0-33
END POINT	——◆	N27S	1M21V	R141	Information Collector	BS-D-7-0-33
TRD WR/LR	——◆	N27T	1M22V	R141	Information Collector	BS-D-7-0-33
REWIND	——◆	N27V	1M23V	R141	Information Collector	BS-D-7-0-33
MISS CHAR	——◆	N6V	M24V	R141	Information Collector	BS-D-7-0-33
SC1	——◆	N26K	M27V	R141	Information Collector	BS-D-7-0-33
SC2	——◆	N26M	M28V	R141	Information Collector	BS-D-7-0-33
SC3	——◆	N26P	M29V	R141	Information Collector	BS-D-7-0-33
SC4	——◆	N26S	M30V	R141	Information Collector	BS-D-7-0-33
SC5	——◆	N26T	M31V	R141	Information Collector	BS-D-7-0-33
SC6	——◆	N26V	M32V	R141	Information Collector	BS-D-7-0-33
DA3(1)	——◆	B31K	A18M	B201	MA	BS-D-7-0-29
DA4(1)	——◆	B31M	A19M	B201	MA	BS-D-7-0-29

TABLE 7-2 INPUT SIGNALS (continued)

Signal	Symbol	Signal Destination				
		Interface Connection	Terminal	Module Type	Logic	Block Schematic Drawing
DA5(1)	——◆	B31P	A20M	B201	MA	BS-D-7-0-29
DA6(1)	——◆	B31S	A21M	B201	MA	BS-D-7-0-29
DA7(1)	——◆	B31T	A22M	B201	MA	BS-D-7-0-29
DA8(1)	——◆	B31V	A23M	B201	MA	BS-D-7-0-29
DA9(1)	——◆	C31D	A24M	B201	MA	BS-D-7-0-29
DA10(1)	——◆	C31E	A25M	B201	MA	BS-D-7-0-29
DA11(1)	——◆	C31H	A26M	B201	MA	BS-D-7-0-29
DA12(1)	——◆	C31K	A27M	B201	MA	BS-D-7-0-29
DA13(1)	——◆	C31M	A28M	B201	MA	BS-D-7-0-29
DA14(1)	——◆	C31P	A29M	B201	MA	BS-D-7-0-29
DA15(1)	——◆	C31S	A30M	B201	MA	BS-D-7-0-29
DA16(1)	——◆	C31T	A31M	B201	MA	BS-D-7-0-29
DA17(1)	——◆	C31V	A32M	B201	MA	BS-D-7-0-29
DI0(1)	——◆	A1D	C2M	B201	MB	BS-D-7-0-30
DI1(1)	——◆	A1E	C3M	B201	MB	BS-D-7-0-30
DI2(1)	——◆	A1H	C4M	B201	MB	BS-D-7-0-30
DI3(1)	——◆	A1K	C5M	B201	MB	BS-D-7-0-30
DI4(1)	——◆	A1M	C6M	B201	MB	BS-D-7-0-30
DI5(1)	——◆	A1P	C7M	B201	MB	BS-D-7-0-30
DI6(1)	——◆	A1S	C8M	B201	MB	BS-D-7-0-30
DI7(1)	——◆	A1T	C9M	B201	MB	BS-D-7-0-30
DI8(1)	——◆	A1V	C10M	B201	MB	BS-D-7-0-30
DI9(1)	——◆	A2D	C11M	B201	MB	BS-D-7-0-30
DI10(1)	——◆	A2E	C12M	B201	MB	BS-D-7-0-30
DI11(1)	——◆	A2H	C13M	B201	MB	BS-D-7-0-30
DI12(1)	——◆	A2K	C14M	B201	MB	BS-D-7-0-30
DI13(1)	——◆	A2M	C15M	B201	MB	BS-D-7-0-30

TABLE 7-2 INPUT SIGNALS (continued)

Signal	Symbol	Signal Destination				
		Interface Connection	Terminal	Module Type	Logic	Block Schematic Drawing
DI14(1)	——◆	A2P	C16M	B201	MB	BS-D-7-0-30
DI15(1)	——◆	A2S	C17M	B201	MB	BS-D-7-0-30
DI16(1)	——◆	A2T	C18M	B201	MB	BS-D-7-0-30
DI17(1)	——◆	A2V	C19M	B201	MB	BS-D-7-0-30
DATA RQ	——◆	---	L23D	B105	Interrupt Control	BS-D-7-0-32
57A SLOW CYC	——◆	2D15S	2B26	B171	Device Selector	BS-D-7-0-36

LOADING AND DRIVING CONSIDERATIONS

All interface circuits within the PDP-7 consist of series Rand W FLIP CHIP modules. When interconnecting these circuits with those in the peripheral equipment, it is important to keep the load on each circuit within its driving ability. Driving and loading capabilities of most DEC modules used in the PDP-7 and in standard DEC optional equipment are specified in detail in the Digital FLIP CHIP Modules Catalog, C-105.

All inputs to series R modules consist of either diode gate or diode-capacitor-diode (DCD) gate circuits. All inputs draw current in the same direction. Each diode gate input at ground level draws 1 ma. A diode gate with an internal clamped load resistor can drive an 18-ma external load. A flip-flop consists of two cross-connected diode gates. The direct set and clear terminals draw 1 ma. The output capability is 20 ma, less 2 ma for the load resistor permanently connected in the flip-flop, and 1 ma required to condition the opposite side of the flip-flop. The flip-flop can, therefore, drive a 17-ma external load.

The DCD gate circuits on flip-flops and pulse amplifiers draw 2 ma at the level inputs and 3 ma at the pulse inputs when the level is conditioned; 1 ma when the level input is disabled. When

two DCD gates are driving both sides of the same flip-flop, the load on both pulse inputs totals only 4 ma. When the level inputs are tied together as in a complement configuration, the total input load is only 3 ma.

Capacitive loading adversely affects the performance of series R modules; therefore, where long lines are being driven, extra clamped loads should be added to sufficiently discharge the cable capacitance. As a general rule, an extra 2 ma of clamped load current should be added for every foot of wire beyond 1-1/2 ft. An exception to this rule is the R650 Bus Driver module. This module is designed to drive coaxial cable of 100-ohm characteristic impedance through a series driving resistor. If coaxial cable is not used, the direct output may be used, provided that the lines are short. If reflections occur on the line, the resistive output of the bus driver may be used to correct the problem. Shunt termination on the far end of the transmission line is not recommended.

The R650 Bus Driver has two types of outputs: the fast and the slow (or ramp) output. Using the fast output, the bus driver operates as a fast amplifier. When the ramp output is used, an integrating capacitor is inserted between the input of the bus driver and the output stage, causing the output lines to move from ground to −3v or in the reverse direction in approximately 800 nsec. This connection, which is desirable to reduce crosstalk between lines, is used on the ACB (buffered accumulator) lines.

The W640 Pulse Amplifier modules should be carefully terminated. If sufficient noise is generated at the output of these modules, regeneration may result. For this reason, it is recommended that output lines of W640 Pulse Amplifier modules be well shielded. The outputs of W640 modules may be either 400 nsec or 1 μsec in width. All connections on the standard PDP-7 use the 400 nsec pulse width.

All input signals to the PDP-7 are received by diode gates or inverters. Diode gates inputs draw 1 ma of current from the driving circuit, shared among all inputs at ground potential. Inverter inputs draw 2 ma when the signal is at −3v and provide no load when the signal is at ground potential.

Timing is, in general, determined by the machine itself. However, the following timing considerations apply to the modules. The R111 Diode Gate sets up in approximately 50 nsec in

either direction under normal load conditions. Fall times are faster with heavier loads, and the best method to speed up a slow R111 Diode Gate is to connect an external load across the input to ground. The DCD gates set up in 400 nsec, as measured from the end of the preceding 100-nsec pulse; and the pulse input must return to −3v for 400 nsec before the next pulse is applied. Series R pulses are 100 nsec in width, measured from the 10% point of the leading edge to the 90% point of the trailing edge. Fall time is not critical on these pulses, provided that the pulse has returned to −3v in time to come up for the next pulse.

All output signals from the PDP-7, routed through the interface, have been provided with adequate buffering to meet the input requirements of all normal I/O equipment. Whenever it becomes necessary for the user to draw out other signals (besides those connected in the standard interface), care must be taken to ensure that the input loads presented to the sources of these signals does not exceed their driving ability. When it is evident that the source would be overloaded, a suitable driver must be provided between the signal source and the I/O device employing the signal.

> NOTE: Numbers in parentheses included in headings of the remainder of this chapter designate the last digit of the block schematic engineering drawing for the logic circuit or signal discussed.

INFORMATION COLLECTOR (IC) (33)

The IC reads data or status information into the AC from various peripheral devices. Seven IC channels or levels, are available in the basic machine. Each of these channels are wired to a signal cable connector corresponding to an upper half (bits 0-8) and a lower half (bits 9-17) of the AC. On the basic machine the paper-tape reader occupies one complete channel, the Teletype occupies the lower half of a channel and the status register occupies (nominally) one channel. If no card reader, card punch, or line printer is connected to the system, the lower half of the status register channel may be used for other purposes. Thus, in the basic machine, the equivalent of five free channels is available for additional IC inputs. Channel availability of the IC is specified as follows:

Level	Use
1	All 18 connections employed for RB
2	First 9 connections employed for status signals of IORS instruction (IOT 0314)
3, 4, 5	All 18 connections open and assignable
6	First 10 connections are open and last 8 connections are assigned to Teletype unit
7	First 12 connections are open and last 6 connections are assigned to the step counter (SC) of the Type 177 EAE option

Each level, or channel of the IC consists of one 2-input negative AND gate (two series-connected transistors) for each of the 18 possible bits of an input word. The two inputs are usually supplied by a data signal and an IOT pulse which is common to each bit of the input word. The output from the seven channels for each bit are NOR combined to set the appropriate accumulator flip-flop. One bit for each of the seven channels is provided by a Type R141 Diode Gate module; the entire IC being constructed of 18 of these modules.

When designing a PDP-7 system, it is necessary to consider the number of collector channels required by peripheral equipment. If more than seven channels are required, the IC will have to be expanded to accommodate the additional information. The expansion requires 18 Type R141 Diode Gate modules, six Type W607 Pulse Amplifier modules and the appropriate mounting panel and hardware. This expansion is connected into one full channel of the standard IC and adds six additional information channels. Further expansion requires only additional R141 modules, each group of 18 adding an additional seven channels. Figure 7-1 represents the channel assignments for the standard IC.

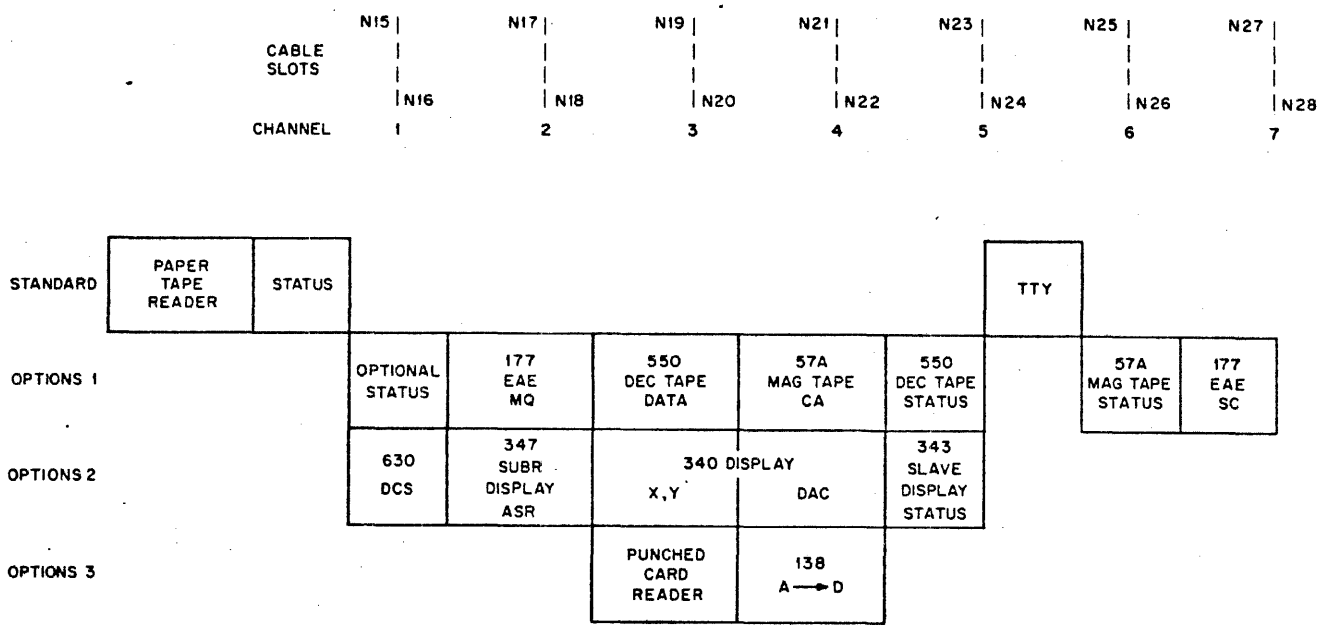


Figure 7-1 Channel Assignments for the Information Collector

INFORMATION DISTRIBUTOR (ID) (34)

The ID provides a series of buffered output channels for connecting peripheral devices to the output of the AC. These output channels are powered by 18 Type R650 Bus Driver modules ... one for each bit of the AC. In the basic ID, each of these modules has terminals H and S connected to ground. This causes an output ramp with a rise time of about 800 nsec. Without these terminals grounded, the rise time is about 50 nsec. Each R650 output will deliver about 20 ma to ground. Extension of the ID increases the rise time of the output ramp, as a result of increased loading. Consequently, the previously-mentioned ground connections should be removed when the ID is expanded in order to maintain a satisfactory rise time in the output. The prewired connections to the interface cable receptacles of the ID are listed in Table 7-3.

Data contained in the AC is available as static levels to supply information to I/O devices. These static levels can be strobed into an I/O device register by IOT pulses from the device selector. The static level of each ACB output signal is at −3v when the bit contains a binary 0 and at ground potential when that bit contains a binary 1. The ACB signals are applied to the interface connections through Type R650 Bus Driver modules.

TABLE 7-3 PREWIRED INFORMATION DISTRIBUTOR CONNECTIONS

Wire Color	Signal Name	Connector Terminal
	To Data Multiplexer (C10)	
W/BLK	GND	N1C
W/BRN	T5	N1D
W/RED	GND	---
W/ORN	T6	N1E
W/YEL	GND	N1F
W/GRN	DATA RQ	N1H
W/BLU	GND	N1J
W/VIO	DATA IN	N1K
W/GRY	GND	N1L
WHT	ADDR ACC	N1M
W/BLK	GND	N1N
W/BRN	DATA ACC	N1P
W/RED	GND	N1R
W/ORN	DATA RDY	N1S
W/YEL	GND	---
W/GRN	RQ SLOW CY	N1T
W/BLU	GND	N1U
W/VIO	---	N1V
W/GRY	GND	---
	To API	
W/BLK	GND	N2C
W/BRN	F SET	N2D
W/RED	GND	---
W/ORN	FETCH	N2E
W/YEL	GND	N2F
W/GRN	IA0	N2H

TABLE 7-3 PREWIRED INFORMATION DISTRIBUTOR CONNECTIONS (continued)

Wire Color	Signal Name	Connector Terminal
	To API (continued)	
W/BLU	GND	N2J
W/VIO	IB2	N2K
W/GRY	GND	N2L
WHT	MA 12 IA	N2M
W/BLK	GND	N2N
W/BRN	MA 14 IA	N2P
W/RED	GND	N2R
W/ORN	MA 15 IA	N2S
W/YEL	GND	---
W/GRN	MA 16 IA	N2T
W/BLU	GND	N2U
W/VIO	MA 17 IA	N2V
W/GRY	GND	---
	To DECtape	
W/BLK	GND	N3C
W/BRN	IOT 7501 (B)/IOT 0701	N3D
W/RED	GND	---
W/ORN	IOT 7541 (B)	N3E
W/YEL	GND	N3F
W/GRN	IOT 7502/IOT 0702	N3H
W/BLU	GND	N3J
W/VIO	IOT 7601/IOT 0601	N3K
W/GRY	GND	N3L
WHT	IOT 7602/IOT 1004	N3M
W/BLK	GND	N3N
W/BRN	RUN (1) B	N3P

TABLE 7-3 PREWIRED INFORMATION DISTRIBUTOR CONNECTIONS (continued)

Wire Color	Signal Name	Connector Terminal
	To DECtape (continued)	
W/RED	GND	N3R
W/ORN		N3S
W/YEL	GND	---
W/GRN		N3T
W/BLU	GND	N3U
W/VIO		N3V
W/GRY	GND	---
	To API	
W/BLK	GND	N4C
W/BRN	INS DBK (1)	N4D
W/RED	GND	---
W/ORN	T3	N4E
W/YEL	GND	N4F
W/GRN	T5	N4H
W/BLU	GND	N4J
W/VIO	T7	N4K
W/GRY	GND	N4L
WHT	INT REC	N4M
W/BLK	GND	N4N
W/BRN	INT REC NOT	N4P
W/RED	GND	N4R
W/ORN	INT RQ	N4S
W/YEL	GND	---
W/GRN	MB0 CRY (B)	N4T
W/BLU	GND	N4U
W/VIO	PI1 ⟶ MA	N4V
W/GRY	GND	---

TABLE 7-3 PREWIRED INFORMATION DISTRIBUTOR CONNECTIONS (continued)

Wire Color	Signal Name	Connector Terminal
	To 57A	
W/BLK	GND	N5C
W/BRN	ERF-ERF ENB/V EDGE FLAG	N5D
W/RED	GND	---
W/ORN	WCO-WCO ENB/H EDGE FLAG	N5E
W/YEL	GND	N5F
W/GRN	TCR	N5H
W/BLU	GND	N5J
W/VIO	T READY	N5K
W/GRY	GND	N5L
WHT	ADDR ACC	N5M
W/BLK	GND	N5N
W/BRN	DATA RDY	N5P
W/RED	GND	N5R
W/ORN	DATA RQ	N5S
W/YEL	GND	---
W/GRN	JOB DONE	N5T
W/BLU	GND	N5U
W/VIO		N5V
W/GRY	GND	---
	To DS for 57A	
W/BLK	GND	N6C
W/BRN	IOT 7001	N6D
W/RED	GND	---
W/ORN	IOT 7101	N6E
W/YEL	GND	N6F
W/GRN	IOT 7201/IOT 1001	N6H

TABLE 7-3 PREWIRED INFORMATION DISTRIBUTOR CONNECTIONS (continued)

Wire Color	Signal Name	Connector Terminal
	To DS for 57A (continued)	
W/BLU	GND	N6J
W/VIO	IOT 7301/IOT 0501	N6K
W/GRY	GND	N6L
WHT	IOT 7304	N6M
W/BLK	GND	N6N
W/BRN	IOT 7401	N6P
W/RED	GND	N6R
W/ORN	IOT 7404/IOT 0502	N6S
W/YEL	GND	---
W/GRN	REWIND	N6T
W/BLU	GND	N6U
W/VIO	MISS CHAR	N6V
W/GRY	GND	---
	To 340	
W/BLK	GND	N7C
W/BRN	BLOCK FLAG/STOP FLAG	N7D
W/RED	GND	---
W/ORN	DATA FLAG/LP FLAG	N7E
W/YEL	GND	N7F
W/GRN	DATA RQ	N7H
W/BLU	GND	N7J
W/VIO	DATA IN	N7K
W/GRY	GND	N7L
WHT	ADDR ACC	N7M
W/BLK	GND	N7N
W/BRN	BGN	N7P

TABLE 7-3 PREWIRED INFORMATION DISTRIBUTOR CONNECTIONS (continued)

Wire Color	Signal Name	Connector Terminal
	To 340 (continued)	
W/RED	GND	N7R
W/ORN	DATA RDY	N7S
W/YEL	GND	---
W/GRN	ERF-ERF ENB/V EDGE FLAG	N7T
W/BLU	GND	N7U
W/VIO	WCO-WCO ENB/H EDGE FLAG	N7V
W/GRY	GND	---
W/BLK	IOT 7301/IOT 0501	N8D
W/BRN	IOT 7404/IOT 0502	N8E
W/RED	IOT 7601/IOT 0601	N8H
W/ORN	GND	---
W/YEL	IOT 7501(B)/IOT 0701	N8M
W/GRN	IOT 7502/IOT 0702	N8P
W/BLU	IOT 7201/IOT 1001	N8S
W/VIO	IOT 1002	N8T
W/GRY	IOT 7602/IOT 1004	N8V
WHT	GND	---

DEVICE SELECTOR (DS) (36)

The DS generates IOT pulses that control information transfers between the processor and peripheral equipment. The DS consists of a series of Type B171 Diode Gate, Type R111 Diode Gate, and Type W640 Pulse Amplifier modules. The DS is expandable, as are the IC and ID. The IOT pulse code assignment is given in Table 7-4.

TABLE 7-4 IOT PULSE CODE ASSIGNMENTS

00 1 RT Clock 2 Prog. Interrupt 4 RT Clock	10 Symbol Generator Type 33	20 Memory Increment Type 197	30	40	50	60 Serial Drum Type 24	70 Auto Magnetic Tape Control Type 57A
01 Standard Perforated Tape Reader and Control Type 444B	11 Analog-to-Digital or Digital-to-Analog Converters	21 Relay Buffer Type 140	31	41	51 Digital-to-Analog Converter Type 180	61 Serial Drum Type 24	71 Tape Control Type 57A
02 Standard Perforated Tape Punch Type 75D	12 A-D-A	22 Inter-Processor Buffer Type 195	32	42	52 D-to-A Converter Type 180	62 Serial Drum Type 24	72 Tape Control Type 57A
03 1 Keyboard 2 Keyboard 4 IORS	13 A-D-A Stimulus Flag	23 Inter-Processor Buffer Type 195	33 1 33 KSR Skip 2 Clear All Flags 4 Open	43	53 D-to-A Converter Type 180	63 Automatic Line Printer Type 64	73 Tape Control Type 57A
04 Teleprinter	14	24 Incremental Plotter Control Type 350	34	44	54	64 Card Punch (IBM 523) Control Type 40	74 Tape Control Type 57A
05 Displays Types 34A, 30D, or 340	15 2nd DECtape Control Type 550	25 Plotter	35	45	55 Automatic Priority Interrupt Type 172	65 Automatic Line Printer Type 647	75 DECtape Control Type 550
06 Displays	16 2nd DECtape Control Type 550	26 Plotter	36	46	56 API Type 172	66 Automatic Line Printer Type 647	76 DECtape Control Type 550
07 Display and Light Pen	17 Boundary Register Type KA70A	27 Memory Parity Type 176	37	47	57	67 Card Reader Type CR 01B or Type 421	77 Memory Extension Type 148

PWR CLR AND NEG PWR CLR (20)

These signals are 400-nsec pulses produced by W640 Pulse Amplifiers at location 2C28. These pulses are made available to I/O equipment through connections made at the device selector of the interface. External equipment can make use of these pulses for clearing operations during the power turnon period. The pulses are generated during the 1-sec interval after the POWER switch is set to on.

BGN(B) (20)

The buffered BGN (Begin) signal is supplied to external equipment through a connection in the device selector of the interface. This signal is a 400-nsec, −3v pulse generated by a W640 Pulse Amplifier at location 2C28 during timing pulse SP1·CONTINUE NOT. The signal is used in I/O equipment to clear registers and reset control flip-flops to initial conditions when the START key on the operator console is used.

RUN STOP (20)

The RUN STOP signal is supplied to external equipment through a connection in the device selector of the interface. This signal is a −3v level used to indicate to I/O devices that the STOP key on the operator console has been operated to halt the program.

RUN(1) (23)

The 1 output of the RUN flip-flop is supplied to external equipment through the interface circuits. This signal is at −3v when the computer is performing instructions and is at ground potential when the program is halted. Magnetic tape and DECtape equipment make use of this signal to stop transport motion when the PDP-7 halts, and thus prevents the tape from running off the end of the reel.

MB (36)

Bits 6-11 of an IOT instruction held in the MB are used to select the I/O device to be serviced in a programmed data transfer. Complementary output signals from MB flip-flops 6-11 supply the input to the device selector which generates the appropriate IOT pulses according to instruction bits contained in the MB.

IOT (36)

IOT pulses are generated in the device selector as a function of the contents of MB bits 6-11. These pulses are used in I/O devices for various functions such as: clearing flags, gating data, setting operation modes, etc. The last digit of any IOT pulse designation corresponds to the number of the IOP pulse which causes generation of that IOT pulse (e.g., combination of a device code XX with an IOP 4 pulse produces an IOT XX04 pulse).

ACB (34)

Information contained in the AC which is to be transferred to external equipment under program control, is buffered in the information distributor by 18 Type R650 Bus Drivers. Each of these bus driver circuits produces a positive ACB level when the associated AC bit is a 1.

REQUEST SLOW CYCLE (36)

The REQUEST SLOW CYCLE ground level signal is supplied by the device selector to request that all IOT instructions that address a specific device be a computer slow cycle. This signal is added at the time a slow I/O device is added to the computer system. The IOT instructions for this device are decoded in a Type B171 Diode Gate module. The ground level output at terminal D when the device is selected, is used to request the slow cycle by connection to the input of another Type B171 module. This latter module is used as a ground level NOR gate for all such request signals, and negative output on terminal D of this module is applied to the processor timing circuits (zone D6 of drawing 22). The Type B171 module which receives the SLOW CYCLE REQUEST signals from various devices is located at B26 of the DS. Locations C26 and C27 are available for expansion of this facility (to OR in the slow cycle requests) if more than 12 I/O devices requiring slow cycle operation are connected to the computer.

PROGRAM INTERRUPT REQUEST (32)

The flag of an external device can be used to request a program interrupt. At the time the device requires servicing, the condition of the flag, connected to the Type R141 module in location L14 or M14 of the processor, can be used to request a program break. (The flag of the external device should also be connected to the I/O skip facility so that the IOT 01 pulse

can be sensed by the interrupt program to determine the device requesting the program break.) The PROGRAM INTERRUPT signal level is the NOR of requests from many devices that require programmed attention. At the time the program break is entered, a program subroutine is initiated to determine which device, of many, is to be serviced; then to perform the appropriate service operation (usually by supplying or receiving data under program control). The flags shown connected to the R141 module in location M14 on drawing 32 are only suggested, and are changed if these devices (the display, DECtape, etc.) are not included in the system.

DATA RQ (24)

A high-speed I/O device may originate a data break request by placing a −3v DATA RQ level on the request line connecting the device to the computer. In the interrupt control, the DATA RQ level is synchronized with timing pulse T5 of the current computer cycle, and sets the DATA SYNC flip-flop to 1. This causes a BK RQ level to be transmitted to the major state generator. Completion of the current instruction permits the major state generator to enter a break state, producing a (B) level. This (B) level is combined with the DATA SYNC level to produce a negative DATA·B level.

An external device connected to the data break facilities of the computer must supply a DATA RQ level, a 15-bit core memory address for the transfer, a signal indicating the direction of the transfer as into or out of the computer core memory, and input or output connections to the MB for 18 data bits. The DATA RQ level is sent to the computer at the time the data is ready for a transfer into the PDP-7 or when the data register in the external device is ready to receive information from the PDP-7. This request level must be −3v for assertion, meaning a request for a data break, and drives a transistor base requiring 2 ma of input current.

DA (Data Address) (29)

The data address given by an I/O device is transferred to the MA by connections made at the DA level input of a NOR gate in each module of the MA. Transfer of the address is accomplished during a DATA ADDR ACC pulse of a break cycle.

DATA ADDR ACC (32)

At time T1 of the break cycle, the DATA·B level is NAND combined with timing pulse T1 to produce a DATA ADDR ACC pulse (called DATA ADDR ⟶ MA pulse in early systems). This pulse causes the memory address contained in the address register of the I/O device to be transferred into the processor MA. This pulse is also transmitted to the external device as an acknowledgment that its address has been accepted.

DATA IN (Transfer Direction) (32)

This signal, specifying the direction of data transfer for a data break, is received by the computer from the requesting device. Transfer direction is referenced to the computer core memory, not to the device. This signal is a −3v level to determine the transfer direction as in, or is ground to determine an out transfer.

DI (Data Information) (30)

The 18 DI lines establish the data to be transferred into the MB from an external derice during c data break in which the direction of transfer is into the PDP-7. The DI signal levels must be presented to 2-input negative NAND diode gates at the binary 1 input of the MB and are transferred into the MB by the DATA ACC pulse. This information in the MB is then written into core memory during a normal write operation. The DI signals must be −3v to designate a binary 1 or must be ground potential to specify a binary 0, and must be available at the time the break request is made.

DATA ACC (32)

During a data break cycle when the external device is requesting a transfer into the PDP-7, time T3 and the DATA · B level produce a negative DATA ACC (called DATA INFO ⟶ MB in early systems) pulse. This pulse strobes the data input gates of the MB to transfer a data word from an external device into the MB. This pulse is also provided as an output for device synchronization. Starting at time T5, the information in the MB is written into core memory by the normal write operation.

MBB (28 and 36)

Data break transfer from core memory to an I/O device is made via the MB; whose output is buffered for this purpose by 18 Type R684 Bus Drivers. Each bus driver is capable of driving a 40-ma load. Gating of the information is accomplished at the receiving end by the DATA RDY pulse. The MBB output terminals are located in the device selector.

DATA RDY (32)

During time T3 of a data break cycle in which the transfer direction is out, the DATA • B level and time 3 causes a negative DATA RDY (in early systems called MB INFO ⟶ OUT) pulse to be generated. This pulse may be used to strobe the MBB information into the external device buffer; for this purpose the signal may be delayed within the device to strobe the data into the buffer after an appropriate setup time. Note that the transfer must be made prior to time T2 of the next computer cycle.

CHAPTER 8

INSTALLATION

SITE PREPARATION

Space Considerations

Space must be provided at the installation site to accomodate the PDP-7 and all peripheral equipment and to allow freedom of access to all doors and panels for maintenance. In larger systems, consideration should be given to human engineering factors which minimize the effort required by an operator seated at the operator console to obtain visual or physical access to all controls, indicators, input bins, and output hoppers of all equipment in the system. A basic 3-cabinet PDP-7 requires a floor space 68-15/16 inches wide and 76-5/32 inches deep with a minimum service clearance of 14-7/8 inches at the back. A 4-cabinet PDP-7 requires a space 85-3/32 inches wide, and a 5-cabinet PDP-7 requires a space 101-1/4 inches wide, both with the same depth and service clearance as that given above. An additional width of 19-3/4 inches is required for each additional computer cabinet which is bolted to the main frame or console cabinet. Figure 8-1 indicates the space requirements, cable access, and floor loading for a 3-cabinet PDP-7. This diagram can also be used in planning the installation of all I/O equipment housed in standard DEC computer cabinets if it is borne in mind that other cabinets do not have the table at the front of the operator console and that 1-1/4-inch end panels must be added to the side of each multiple-cabinet configuration constructed of 19-3/4 inch cabinets bolted together. The standard Teletype Keyboard Send Receive set requires a floor space approximately 18-5/8 inches wide by 18-1/2 inches deep. Signal cable length restricts the location of the Teletype to within 18 inches of the side of the computer.

Environmental Conditions

No special environmental condition need be met for proper operation of the PDP-7. Ambient temperature at the installation site can vary between 50 and 122 degrees Fahrenheit (between 10 and 50 degrees centigrade) with no adverse effect on computer operation. However, to extend the life expectancy of the system, it is recommended that the ambient temperature at

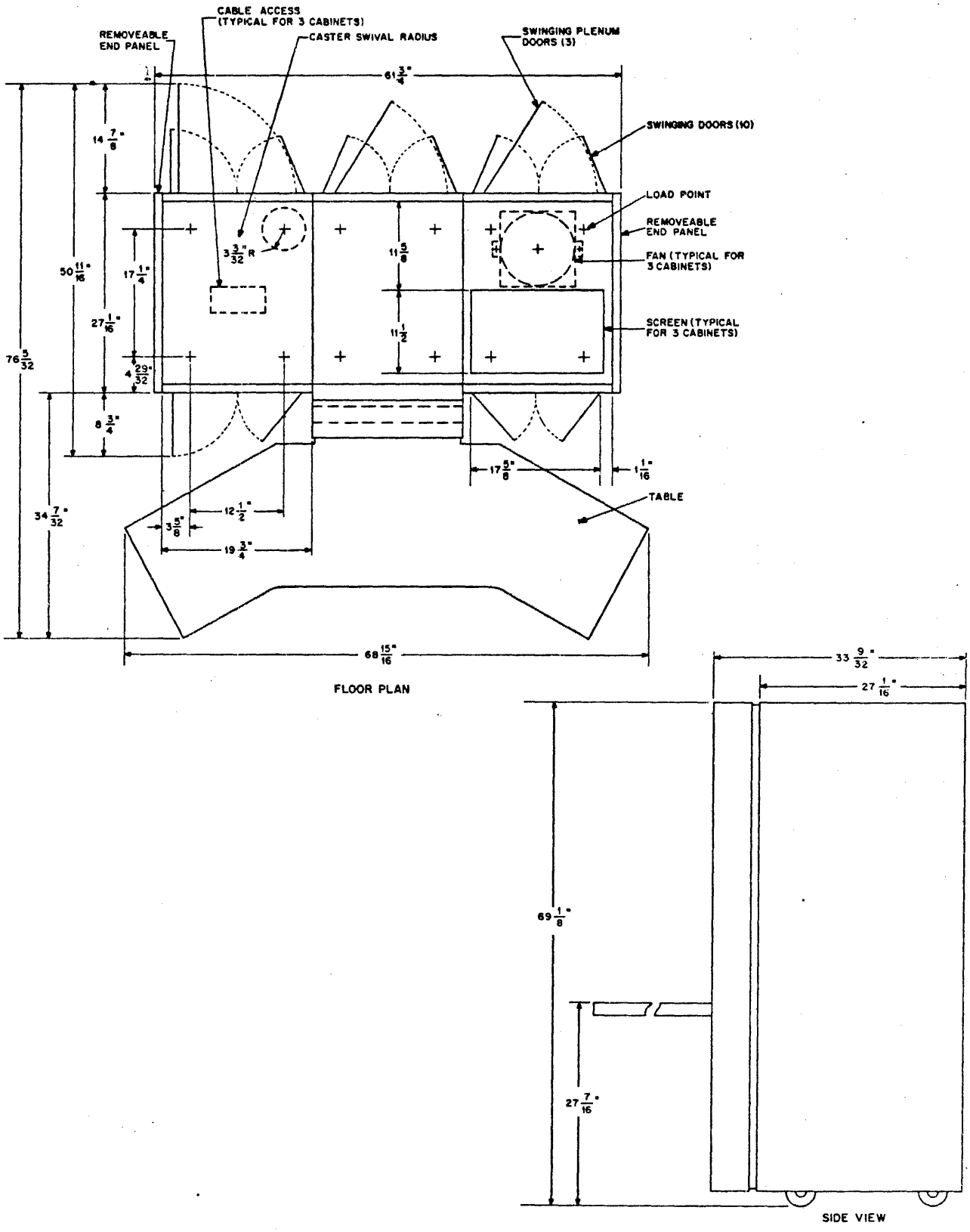


Figure 8-1 Installation Outline Drawing

the installation site be maintained between 70 and 85 degrees Fahrenheit (between 21 and 30 degrees centigrade). During shipping or storing of the system, the ambient temperature may be permitted to vary between 32 and 122 degrees Fahrenheit (between 0 and 50 degrees centigrade). Although all exposed surfaces of all DEC cabinets and hardware are treated to prevent corrosion, exposure of systems to extreme humidity for long periods of time should be avoided to prevent rusting.

Power Requirements

A source of 115-volt (±17 volts), 60-cycle (±0.5 cycle), single-phase power capable of supplying at least 30 amperes must be provided to operate a standard PDP-7. To allow connection to the power cable of the computer, this source should be provided with a Hubbel Twistlock flush receptacle (or its equivalent) rated at 30 amperes at 250 volts. Power dissipation of a standard PDP-7 is approximately 2200 watts, and the heat dissipation is approximately 6600 Btu/hour. Upon special request, a PDP-7 can be constructed to operate from a 220-volt (±33 volts), 60-cycle (±0.5 cycle), single-phase power source or from a 100-volt (±15 volts), 50-cycle (±0.5 cycle), single-phase power source.

PREPARATION FOR SHIPMENT

The following shipping practices are followed by the factory in preparing a system for delivery to a customer and should be adhered to by the customer in any future shipment or relocation. Usually a shipment consists of at least three parcels containing the computer main frame, the Teletype, and a carton containing related documentation, cables, and other miscellaneous material. Shipping weight of a standard 3-cabinet main frame is approximately 1150 pounds. Shipping weight of the Teletype equipment is approximately 60 pounds, and the miscellaneous equipment carton weighs up to 100 pounds.

The cabinet of a PDP-7 system is prepared for shipment as follows:

a. The cabinet is placed upon a sturdy wooden pallet and held in place by passing a bolt through the center of the tubular frame on each side of the bottom of the cabinet. This bolt is secured by a nut on the underside of the pallet.

b. The console table is removed from the cabinet by removing the two mounting pins which attach the table extension arms to the side of the cabinet at the back; then the pins are returned to their position in the cabinet.

c. Modules are taped within the mounting panels, and the power cables are coiled and taped to the floor of the cabinet. The plenum door is then bolted shut.

d. The console table is cushioned by packing material and attached to the outside of the cabinet by metal straps. A wooden protector plate, wrapped in packing material, is strapped to the front of the cabinet to cover the operator console.

e. A full-height plastic bag is placed over the entire cabinet.

f. A wooden cover plate with appropriate packing material is placed on top of the cabinet, and metal shipping straps are run vertically around the cabinet, over the cover plate, and under the pallet. When preparing the cabinet for overseas shipment, boards are nailed between the cover plate and the pallet to form a shipping crate which totally encloses the cabinet.

Teletype Shipping Procedure

The Teletype is packaged in the original manufacturer's shipping carton and is prepared for shipment to the customer as follows:

a. The Teletype is disconnected from the computer cabinet.

b. The back panel of the stand is removed, all cables are disconnected, and the power pack is removed.

c. The Teletype console is removed from the stand and attached to a wooden pallet by four shipping screws. The pallet is then placed in the shipping carton and corrugated packing material is placed on all sides of the console.

d. The stand is placed in the shipping carton above the Teletype console. The power pack is individually wrapped in shipping material and packed within the stand; then the back of the stand is attached by means of the two normal mounting screws.

e. Additional packing material is added and the carton is sealed.

INSTALLATION PROCEDURE

No special tools or equipment are required for installation of a PDP-7 system. A fork-lift truck or other pallet-handling equipment and normal hand tools, including shears to cut the shipping straps, should be available for receiving and installing the equipment. To install the computer:

1. Place the computer cabinet package within the installation site near the final location. Cut the shipping straps and remove all packing material. Remove the console table from the side of the cabinet, and remove the protector plate from the front of the cabinet. Open the rear doors, remove the shipping bolts which hold the plenum doors closed, and open the plenum doors. Remove the bolt which holds each side of the cabinet to the pallet. Slide the cabinet off of the pallet, using a ramp (approximately 4-3/4 inches high) from the floor to the top of the pallet. Move the cabinet to its final location within the installation site (this location must be within 18 feet of the primary power connector within the site).

2. Remove the tape which holds the modules in place within the mounting panels and the tape which holds the power cables to the floor of the cabinet. Assure that all modules are securely mounted in their connectors.

3. Remove the pins from the table mounting guide at each side of the back of the cabinet; install the console table by passing the extension arms through the openings in the front of the cabinet and into the guides at the back of the cabinet; then replace the pins by passing them through the extension arms and guides.

4. Open the Teletype carton and remove the packing material. Remove and unwrap the power pack. Remove the stand from the shipping carton. Remove the Teletype console from the carton, holding it by means of the wooden pallet attached to the bottom. Remove the Teletype console from the pallet and mount it on the stand or console table, as desired. Snap the power pack in place within the top front of the stand, and connect the Teletype console to the power pack (a 6-lead cable attached at the console is connected to the power pack by means of a white plastic Molex 1375 female connector which mates with a male output plug on the power pack). Pass the 3-wire power cable and the 7-conductor signal cable (which is terminated in a female Amphenol 143-022-04 connector) through the opening at the lower left-hand corner of the Teletype stand; then replace the back cover of the stand by means of the two mounting screws.

5. Adjust the stabilizing feet on the four corners of the computer cabinet and on any I/O equipment. Adjust the leveling devices on the feet of the Teletype stand.

6. Remove the fan and filter assemblies from the bottom of the computer cabinet by disconnecting the captive screw at each side of the filter housing. Slide the rear portion of the cable port toward the rear door. Pass the larger diameter computer power cable out through the cable port, pass the Teletype signal and power cables into the cabinet through the cable port, and pass any other I/O equipment signal cables through the cable port; then replace the back half of the cable port and the fan and filter assembly.

7. Connect the 3-prong male connector of the Teletype power cable to the female connector at the end of the smaller diameter power cable within the computer cabinet. Connect the male connector of the Teletype signal cable to the mating connector at location R3B on the rear door of bay 2. Be sure that the computer lock switch is turned fully counterclockwise and that the

POWER switch is set to the down position; then connect the computer power cable to the primary power source.

8. Set the POWER switch to the up position and note that the POWER indicator lights. Computer logic power should go on immediately, and memory power after approximately 5 seconds.

9. Install the printer paper roll in the Teletype printer/keyboard, insert a blank tape in the tape punch.

10. Set the Teletype LINE/OFF/LOCAL switch to LINE and strike several keys, noting whether or not the printer operates. Make the same check with the switch in the LOCAL position. After completion of the checks, set the LINE/OFF/LOCAL switch to OFF.

11. Set the PUNCH feed switch on the operator console to the up position. Observe that the punch motor runs, then return PUNCH feed switch to the down position.

12. Press and hold the punch FEED pushbutton. The motor should start the instant the pushbutton is pressed. After one second, the punch should punch feed-holes only in the tape and should continue punching feed-holes as long as the pushbutton is pressed. When the pushbutton is released, punching and tape movement should stop, but the punch motor should continue to run for approximately 5 seconds.

13. Load the RIM loader program by placing the RIM loader tape in the reader as described in Chapter 9 of this manual, setting the READY/LOAD switch to the READY position, and then pressing the READ-IN key. After completion of the loading operation, check the contents of the appropriate memory cell for accuracy. The procedure for checking the contents of a cell is described in Chapter 9, and Table 9-8 indicates the addresses used and the contents of each address.

14. Set the POWER switch to the down position and observe that the computer cycles down. Memory power should go off immediately, and computer logic power after approximately 5 seconds.

This completes the installation of a standard PDP-7 system. Before commencing normal use, verify the operating capability of the system. Perform the Power Supply Checks as described under Preventive Maintenance in Chapter 10 of this manual and run all Maindec dianostic programs supplied with the PDP-7 system as described in the associated documents.

CAUTION

Whenever the PDP-7 system is operating, make sure that the area is clear atop of the cabinet. The vents located at this point are vital to the proper cooling of the computer. Never use this space as a storage shelf.

CHAPTER 9

OPERATION

CONTROLS AND INDICATORS

Manual control of the PDP-7 and its peripheral equipment is effected by controls, switches, and keys located on the operator console and the individual peripheral devices. Visual indication of computer status and content of registers and control flip-flops is given on the operator console where this information relates to the central processor. Similar information relating to the memory and peripheral equipment is given on a separate indicator panel.

Operator Console Controls and Indicators

The controls and indicators of the operator console are shown in Figure 9-1.

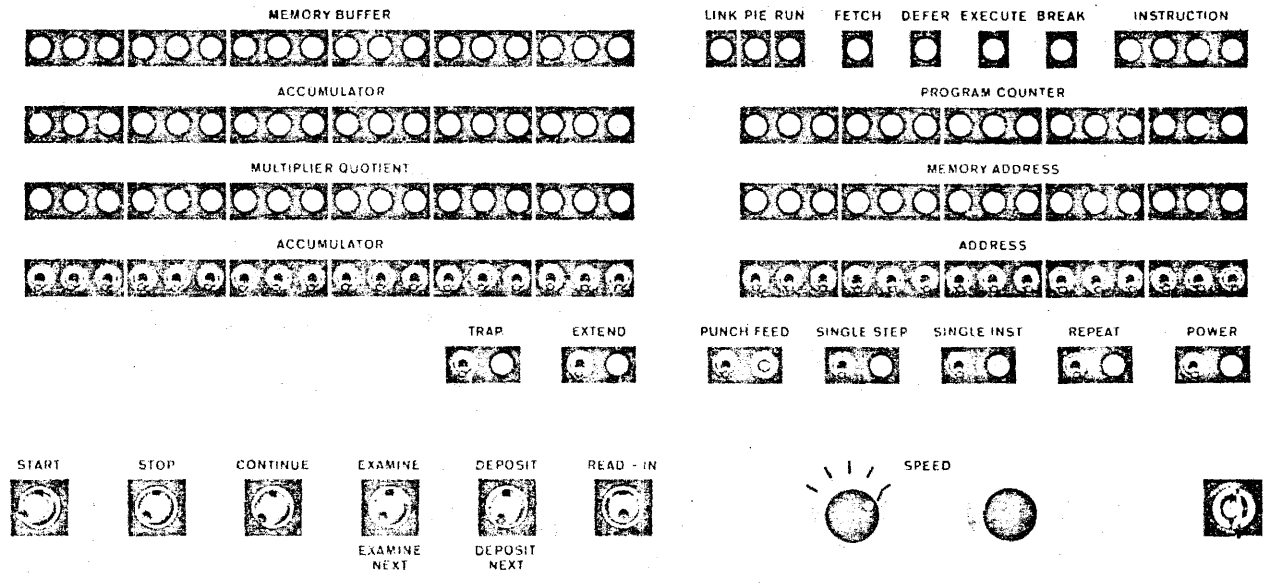


Figure 9-1 Operator Console

Indicators

The contents of the various registers, the current major state of the computer, and the states of various flip-flops are shown by the indicators on the operator console. Lighted indicator lamps denote the presence of binary 1's in the associated register bits and flip-flops. Table 9-1 lists the indicators mounted on the operator console and explains their functions.

TABLE 9-1 OPERATOR CONSOLE INDICATORS

Indicator	Function
MEMORY BUFFER Indicators	Indicate the contents of the MB. Usually the contents of the MB denote the word read or written at the core memory address held in the MA.
ACCUMULATOR Indicators	Indicate the contents of the AC. The contents of the AC are the result of an arithmetic operation, a control word for output to an external control, data read in from some peripheral device, or data for transfer out to a peripheral device.
MULTIPLIER QUOTIENT Indicators	Indicate the contents of the MQ. The MQ holds the multiplier at the beginning of a multiplication operation and the least significant half of the product at the conclusion. It also holds the least significant half of the dividend at the start of a divide operation and at the end holds the quotient.
PROGRAM COUNTER Indicators	Indicate the contents of the PC. The PC holds the address in core memory from which the next instruction is to be taken.
MEMORY ADDRESS Indicators	Indicate the contents of the MA. The contents of the MA denote the core memory address of the word currently or previously read or written. The address of each new word is set into the MA during time state T1 of the computer cycle.

TABLE 9-1 OPERATOR CONSOLE INDICATORS (cont)

Indicator	Function
FETCH, EXECUTE, DEFER BREAK Indicators	Give the major operating state of the computer during the next memory cycle.
INSTRUCTION Indicators	Give the current operating instruction of the computer in binary code. This may be 1 of 16 possible combinations.
LINK Indicator	Indicates the status of the link. The link is used as an extension of the AC, as an overflow register in 1's complement arithmetic operations, and as a carry register in 2's complement arithmetic operations.
RUN Indicator	Indicates that the RUN flip-flop is set to 1. When this indicator is lit, the timing circuits are enabled, and the computer is performing an instruction.
PIE Indicator	Indicates Program Interrupt Enabled. This occurs whenever the regular program is halted for some reason, such as a program break to transfer information between the computer and the I/O devices.

Switch Registers

The switch registers provide a means of manually inserting data and addresses into the processor. On each switch, the upper position selects a binary 1 for the associated bit and the lower position selects a binary 0. Table 9-2 lists the switch registers and explains their functions.

TABLE 9-2 OPERATOR CONSOLE SWITCH REGISTERS

Control	Function
ACCUMULATOR Switches	Provide a means of manually setting information through the AC into core memory. The 18-bit switch register also functions as a set of sense switches which may be sensed by the program.
ADDRESS Switches	Provide a means of manually specifying an address of a given core memory cell. This may be done either to establish the starting point of a program or as part of an examine or deposit operation. The upper position indicates binary 1, the lower indicates 0.

Switch Controls and Indicators

Switch controls and indicators, or pushbutton controls are used to initiate certain modes of operation in the computer. In these controls, a switch position does not denote a bit content and the indicator is not necessarily lighted by the associated switch. Table 9-3 lists the switch controls and indicators and explains their functions.

TABLE 9-3 OPERATOR CONSOLE SWITCH CONTROLS AND INDICATORS

Control or Indicator	Function
POWER Switch and Indicator	The switch controls primary power to the computer and all external devices attached to it. The on position is up. The indicator lights when primary power is turned on.
REPEAT Switch and Indicator	The switch causes the operation initiated by pressing the CONTINUE, DEPOSIT NEXT, or EXAMINE NEXT key to be repeated as long as the key is held in the on (up) position. This switch triggers a one-shot with an adjustable delay. The signal from this

TABLE 9-3 OPERATOR CONSOLE SWITCH CONTROLS AND INDICATORS (cont)

Control or Indicator	Function
REPEAT Switch and Indicator (cont)	one-shot restarts the cycle each time it has reached completion. The indicator lights when the mode is enabled.
SPEED Controls	Vary the repeat interval from 40 microseconds to 7 seconds. The left-hand knob is a 5-position coarse control; the right-hand knob is a continuously variable fine control. Slowest speed is obtained with both knobs rotated to the extreme counterclockwise position.
SINGLE STEP Switch and Indicator	The switch causes the computer to stop at the end of each memory cycle. This switch generates a RUN STOP signal that resets the RUN flip-flop to 0. Repeated operation of the CONTINUE key momentarily overrides the RUN STOP signal so that the program is advanced one step at a time. The indicator lights when the mode is enabled.
SINGLE INST Switch and Indicator	The switch, when in the up position, causes the computer to stop at the end of each instruction. This switch, in combination with an F Set level, generates a RUN STOP signal that resets the RUN flip-flop and halts the computer at the end of the current memory cycle. If the CONTINUE key is depressed while this switch is on, the RUN STOP signal is temporarily overridden; and the program is run one instruction at a time. When both switches are on, SINGLE STEP takes precedence over SINGLE INSTRUCTION. The Indicator lights when the mode is enabled.

TABLE 9-3 OPERATOR CONSOLE SWITCH CONTROLS AND INDICATORS (cont)

Control or Indicator	Function
PUNCH FEED Switch	Controls perforated tape punch power. When this switch is in the down position, punch power is under program control. When this switch is in the up position, punch power is on (independent of the program).
PUNCH FEED Pushbutton	Causes tape to be punched with feed holes only. Approximately 2 feet of such "leader" should be punched before the punch is placed under program control.
EXTEND Switch and Indicator	The switch enables the extend mode of the optional Type 148 Memory Extension Control to be used with all console keys and switches performing memory reference functions. The indicator lights when the mode is enabled.
TRAP Switch and Indicator	The switch permits the trap mode to be engaged by an ITON instruction in the program. When in use, the trap prevents the computer from carrying out harmful or undesirable instructions which might be given when the computer is operating in a time-shared mode. When such an illegal instruction appears, it sets a trap flag; and a program break is initiated. The indicator lights when the mode is enabled.

Keys

The following manual keys are used to initiate basic general operations of the processor. (Note: The starting cycle is initiated by activating any manual key.) Table 9-4 lists the keys and their functions.

TABLE 9-4 OPERATOR CONSOLE MANUAL KEYS

Control or Indicator	Function
START Key	When depressed, initially clears the RUN flip-flop, delays 10 microseconds to allow all operations both internal and external to cease, then sets the computer to the Fetch State, loads the program counter with the contents of the 15 bit address switch register, sets the RUN flip-flop and starts the computer time chain. Thus operation of the program is started, at the address specified by the contents of the ADDRESS switches (AS).
STOP Key	Stops the computer program when depressed by clearing the run flip-flop during time five (T5) of the main computer cycle.
CONTINUE Key	Causes the computer to resume operation, at the point at which it was stopped. Beside the normal off (level) and (down) positions, this key also has a latched on position, obtained by lifting the key.
EXAMINE/EXAMINE NEXT Key	When the EXAMINE/EXAMINE NEXT control is raised the EXAMINE function is initiated. The effect of this key is to place the contents of the core memory cell, specified by the ADDRESS switches, into the AC and MB. This operation is performed by clearing the PC and forcing the computer into the execute cycle of an LAC instruction. At the completion of the operation, the MA contains the contents of the ADDRESS switches, and the PC contains the address of the next consecutive memory cell. When the EXAMINE/EXAMINE NEXT control is pressed the EXAMINE NEXT function is initiated. This function is

TABLE 9-4 OPERATOR CONSOLE MANUAL KEYS (cont)

Control or Indicator	Function
EXAMINE/EXAMINE NEXT Key (cont)	similar to that of the EXAMINE function, except that the PC is not cleared but is used to load the MA directly rather than from contents of the ADDRESS switches. At the completion of the operation, the contents of the various registers is the same as for an examine operation.
DEPOSIT/DEPOSIT NEXT Key	When the DEPOSIT/DEPOSIT NEXT control is raised the DEPOSIT function is initiated. This key places the contents of the ACCUMULATOR switches into the core memory cell whose address is specified by the ADDRESS switches. This operation is performed by forcing the computer into the execute cycle of a DAC instruction. At the completion of the operation, the contents of the ACCUMULATOR switches is in the AC and MB, and the MA contains the contents of the ADDRESS switches. The PC contains the address of the next consecutive memory cell. When the DEPOSIT/DEPOSIT NEXT control is pressed, the DEPOSIT NEXT function is initiated. This function is similar to that of the DEPOSIT function, except that it places the contents of the ACCUMULATOR switches into the core memory cell whose address is specified by the contents of the PC. The contents of the PC are then incremented by 1. At the completion of the operation, the contents of the various registers are the same as for a deposit operation.
READ-IN Key	Is used to read paper tape punched in the binary mode into a block of core memory. The first address of the memory block must be specified by the contents of the ADDRESS switches. When the key is depressed the

TABLE 9-4 OPERATOR CONSOLE MANUAL KEYS (cont)

Control or Indicators	Function
READ IN Key (cont)	address specified in the ADDRESS switches is placed in the PC and MB. The execute state is set in the major states and a DAC instruction is set in the IR. The read paper tape flip-flop (RPT) is set, the reader is selected in the binary mode, and the first three lines are read from tape. The reader then halts. The condition that the KEY LEVEL is present is required to establish initial conditions. This level must be absent in order that information may be placed in consecutive core locations. When the key is released the remainder of the tape will be read. The readin mode may be terminated by having a hole 7 punched in the last line on the tape, or by pressing the STOP or EXAMINE key.
LOCK Switch	Prevents accidental disturbance of a program in progress. With this switch turned clockwise, all console switches and keys, except the ACCUMULATOR and ADDRESS switches, are disabled. In the counterclockwise positon, all controls operate normally.

Teletype Controls

The Teletype is shown in Figure 9-2. Table 9-5 lists the Teletype controls and explains their functions.

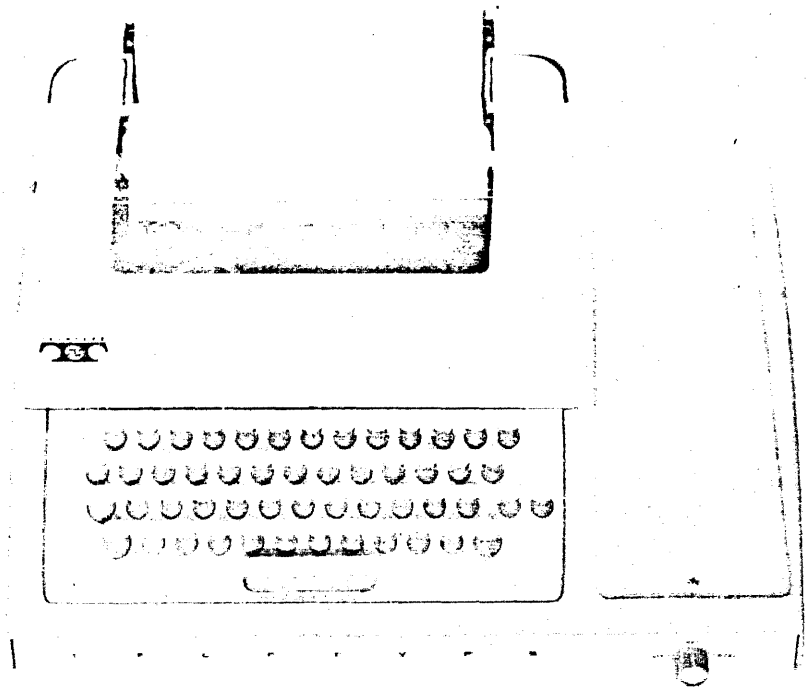


Figure 9-2 Teletype Console

TABLE 9-5 TELETYPE CONSOLE CONTROLS

Control	Function
KEYBOARD	Provides a means of supplying input data, in the form of typed characters, to the computer and/or the page printer, depending on the setting of the LINE/OFF/LOCAL switch.
LINE/OFF/LOCAL Switch	Controls the application of primary power to the Teletype and controls data connection between the Teletype and the central processor. In the LINE position, the Teletype is energized and connected as an I/O device of the computer. In the OFF position, the Teletype is de-energized. In the LOCAL position, the Teletype is energized for off-line operations; and the signal connections to the processor are broken. Both line and local use of the Teletype requires that the computer be energized through the POWER switch.

Tape Reader Controls

The tape reader is shown in Figure 9-3. Table 9-6 lists the tape reader controls and explains their functions.

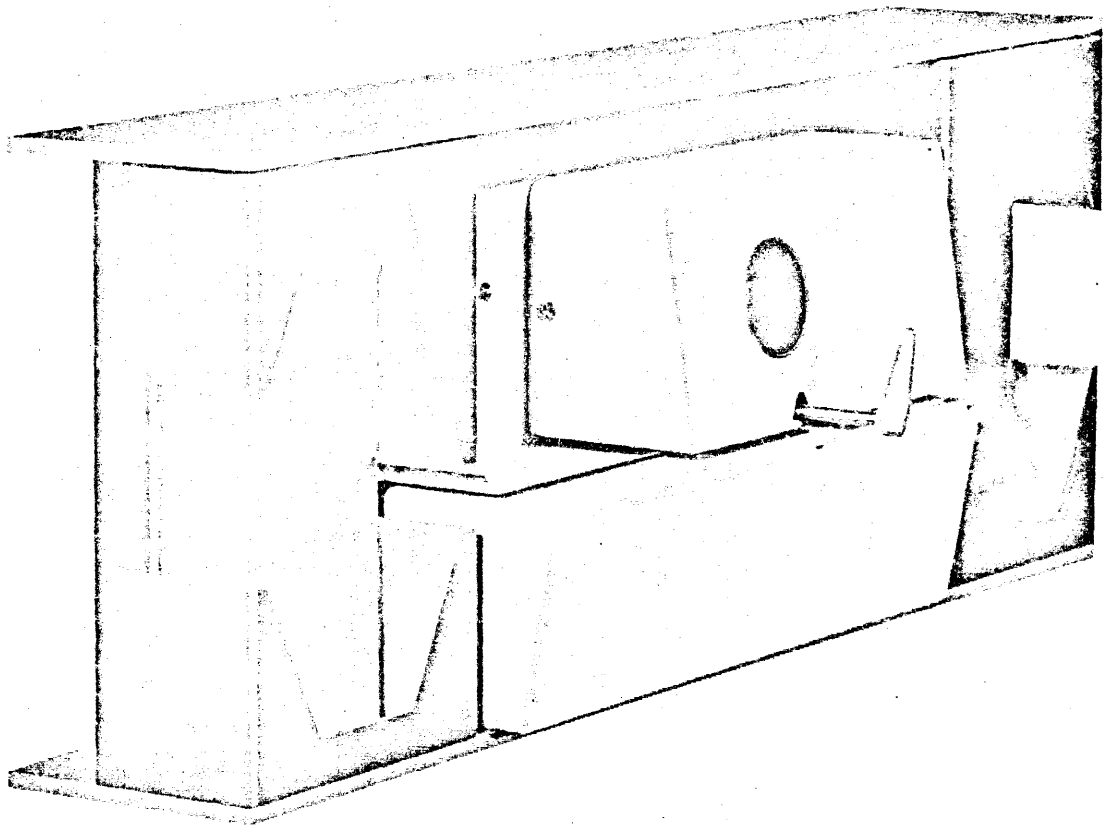


Figure 9-3 Perforated Tape Reader

TABLE 9-6 TAPE READER CONTROLS

Control	Function
POWER ON Switch	Applies power to the power supply, capstan drive motor, and fan motor.
READY/LOAD Switch and Tape Width Selector Knob	In its clockwise position, the READY/LOAD switch de-energizes the brake and pinch roller to allow tape insertion. The knob may be moved in or out to handle different tape levels.

Indicator Panel

The indicator panel is shown on Figure 9-4. Table 9-7 lists the indicator panel indicators and their functions.

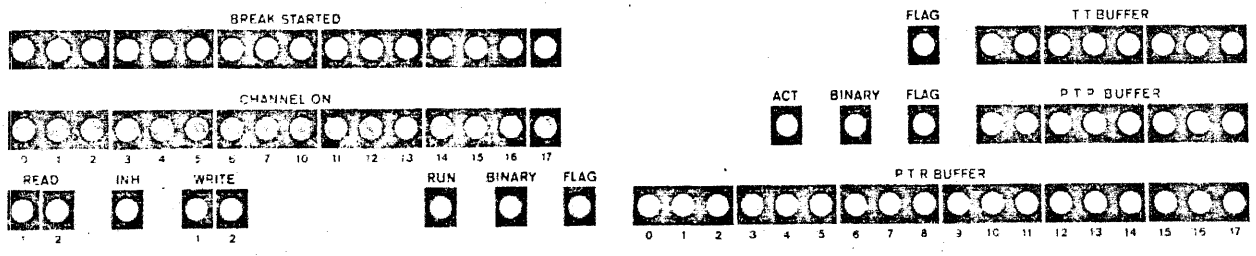


Figure 9-4 Indicator Panel

TABLE 9-7 INDICATOR PANEL INDICATORS

Indicator	Function
BREAK STARTED Indicators	Indicate which channels of the Automatic Priority Interrupt option are requesting an interrupt.
CHANNEL ON Indicators	Indicate which channels of the Automatic Priority Interrupt option have been enabled by the program.
READ Indicators	Indicate the status of the READ 1 and READ 2 flip-flops. Since a read operation occurs during each cycle, these should appear to glow faintly whenever the computer is cycling, but should go out when the computer is stopped.

TABLE 9-7 INDICATOR PANEL INDICATORS (cont)

Indicator	Function
INH Indicator	Indicates the status of the INH (inhibit) flip-flop in the memory control. Since inhibit current flows during each cycle, this indicator should appear to glow faintly whenever the computer is cycling, but should go out when the computer is stopped.
WRITE Indicators	Indicates the status of the WRITE 1 and WRITE 2 flip-flops. Since a write operation occurs during each cycle, these indicators should appear to glow faintly whenever the computer is cycling, but should go out when the computer is stopped.
FLAG Indicator (TT BUFFER)	Indicates the status of the Teletype KEYBOARD FLAG flip-flop. When this indicator is lit, the Teletype LUI is ready for a data transfer.
TT BUFFER Indicators	Indicate the contents of each of the eight bits of the Teletype buffer (LUI).
ACT Indicator	Indicates the status of the PUN ACTIVE flip-flop. This indicator is lit during tape punching operations.
BINARY Indicator	Indicates the status of the PUN MODE flip-flop in the punch buffer. When this indicator is lit, tape is being punched in the binary mode.
FLAG Indicator (PTP BUFFER)	Indicates the status of the PUN FLAG flip-flop. When this indicator is lit, the punch buffer is ready for a data transfer.

TABLE 9-7 INDICATOR PANEL INDICATORS (cont)

Indicator	Function
PTP BUFFER Indicators	Indicate the contents of the punch control buffer. When tape is being punched in binary mode, only the six least significant indicators are read.
RUN Indicator	Indicates the status of the RD RUN flip-flop. When this indicator is lit, the reader is reading tape.
BINARY Indicator	Indicates the status of the RD MODE flip-flop. When this indicator is lit, the reader is reading tape in the binary mode.
FLAG Indicator (PTR BUFFER)	Indicates the status of the RD FLAG flip-flop. When this indicator is lit, the tape reader is ready for a data transfer.
PTR BUFFER Indicators	Indicates the contents of the reader buffer. When the reader is operating in binary mode, the indicators are read as a 3-stage, 6-bit shift register.

OPERATING PROCEDURES

Many means are available for loading and unloading PDP-7 information. The means used are, of course, dependent upon the form of the information, time limitations, and the peripheral equipment connected to the computer. The following procedures are basic to any use of the PDP-7, and although they may be used infrequently as the programming and use of the computer become more sophisticated, they are valuable in preparing the initial programs and learning the function of machine input and output transfers.

Manual Data Storage and Modification

Programs and data can be stored or modified manually by means of the facilities on the operator console. Chief use of manual data storage is made to load the readin mode loader program into the computer core memory. The readin mode (RIM) loader is a program used to automatically load programs into PDP-7 from perforated tape in RIM format. This program and the RIM tape format are described in the PDP-7 Users Handbook F-75 and in Digital Program Library descriptions. The RIM program is listed in Table 9-8 for rapid reference and can be used as an exercise in manual data storage. To store data manually in the PDP-7 core memory:

1. Turn the lock switch counterclockwise and set the POWER switch to the up position.

2. Set the ADDRESS switches to correspond with the address of the first word to be stored. (In the case of the RIM loader program, this is 17762_8).

> NOTE: Whenever an address in core memory is given in this section, it is intended to apply to an 8K memory. To translate this to the correct 4K memory address, subtract 10000_8.

3. Set the ACCUMULATOR switches to correspond with the binary content of the first word. (In the case of the RIM loader program, this is zero.)

4. Momentarily lift the DEPOSIT/DEPOSIT NEXT key to deposit the word in memory.

5. Note the contents of the four storage registers (AC, MB, MA, and PC) as given by their respective indicators after completion of the deposit operation. The AC and MB must both contain the data word just deposited, the MA must contain the address of the core memory cell in which the word was deposited, and the PC must contain the address of the next consecutive core memory cell (MA+1).

6. Store all additional data words by momentarily depressing the DEPOSIT/DEPOSIT NEXT key to the DEPOSIT NEXT position after each successive

data word had been set up on the ACCUMULATOR switches. The contents of the PC will be incremented by 1 during each deposit next operation, thus setting up the address of the core memory cell to be used for the next operation. The RIM loader contains the following program:

TABLE 9-8 READIN MODE (RIM) LOADER PROGRAM

Address (octal)	Content (octal)	Tag	Mnemonic	Comments
17762/	0	R,	0	/READ ONE BINARY WORD
17763/	700101		RSF	
17764/	617763		JMP .-1	/WAIT FOR WORD TO COME IN
17765/	700112		RRB	/READ BUFFER
17766/	700144		RSB	/READ ANOTHER WORD
17767/	637762		JMP I R	/EXIT SUBROUTINE
17770/	700144	GO,	RSB	/ENTER HERE, START READER /GOING
17771/	117762	G,	JMS R	/GET NEXT BINARY WORD
17772/	057775		DAC OUT	
17773/	417775		XCT OUT,	/EXECUTE CONTROL WORD
17774/	117762		JMS R	/GET DATA WORD
17775/	0	OUT,	0	/STORE DATA WORD
17776/	617771		JMP G	/CONTINUE

7. To recheck a loaded program, set the ADDRESS switches to the starting address and momentarily set the EXAMINE/EXAMINE NEXT key to the EXAMINE position. After the first cell has been checked, the remaining cells may be examined in sequence simply by repeatedly setting the switch to the EXAMINE NEXT position without adjusting the ADDRESS switches. The contents of any cell can be altered by repeating steps 2 through 4, using the address of the cell in question.

Loading Binary Data Using READ-IN Key

Binary format tapes (including the RIM loader tape) can be loaded directly into the computer without the need of a prestored program. This is accomplished as follows:

1. Turn the computer lock switch counterclockwise and set the POWER switch to the up position.

2. Set the tape reader POWER ON switch to ON.

3. Set the READY/LOAD switch to LOAD (clockwise) and insert the binary tape. The tape is placed in the right-hand loading bin of the reader, and, during reading, travels to the left-hand bin. When the tape is properly positioned, there will be three bit positions to the rear of the sprocket wheel and five bit positions to the front.

4. Set up the starting address of the tape (found on the leader) on the ADDRESS switches.

5. Press and release the computer READ-IN key.

6. Set the tape reader READY/LOAD switch to READY. The tape will be read automatically.

Loading Data Under Program Control

Information (in other than binary format) can be stored or modified in the computer automatically, only by executing programs previously stored in memory. For example, having the RIM loader stored in the core memory allows RIM format tapes to be loaded as follows:

1. Turn the computer lock switch counterclockwise and set the POWER switch to the up position.

2. Set the tape reader POWER ON switch to ON.

3. Set the READY/LOAD switch to LOAD and insert the tape into the tape reader.

4. Set up the starting address of the RIM loader program (17770) by means of the ADDRESS switches.

5. Press and release the computer START key.

6. Set the tape reader READY/LOAD switch to READY. The tape will be read automatically. The program contained on the tape may be initialized and started automatically after being loaded. This occurs because some tapes in RIM format are concluded with address 0000 and a data word equal to one less than the starting address of the program just read. Therefore, after the last tape character is read, the program starting address is taken by the program counter as the address of the next instruction to be executed.

Assembling Programs With PAL

Programs prepared in binary format and written in PAL, symbolic language can be assembled into binary, machine-language program tapes by PAL as described in appropriate Digital Program Library documents. Basically, this operation is accomplished as follows:

1. Energize the computer by turning the lock switch counterclockwise and setting the POWER switch to the on (up) position.

2. Energize the tape reader by setting the POWER ON switch to ON.

3. Store the RIM loader program, either manually or by use of the READ-IN key, as previously described.

4. Load the PAL assembler program by means of the assembler tape. Since the assembler tape is in RIM format, it can be loaded by the method described under Loading Data Under Program Control. When the tape has been run, the AC should contain all 0's. If it does not, a checksum error has been detected; and the program has been improperly stored. When this occurs, the tape must be rerun until the AC does finally contain all 0's at the conclusion of the loading process. When this result is achieved, the program has been properly stored. Repeated errors indicate defects in either the assembler tape or the PDP-7 system.

5. Set the tape reader READY/LOAD switch to the LOAD position, and insert the PAL symbolic language tape (which is to be converted into machine-language, binary format) into the tape reader.

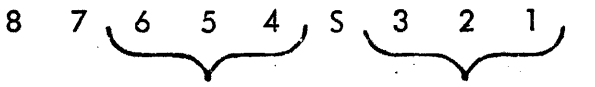
6. Set up the starting address of the PAL assembler program (0020) on the ADDRESS switches of the operator console. (Set accumulator switch 10 up to indicate ASCII, or down to indicate FIODEC.)

7. Press and release the CONTINUE key.

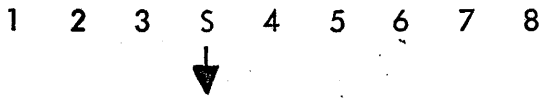
8. When assembly is complete, the assembler will stop with all 1's in the AC.

Teletype Code

The 8-bit code used by the Model 33 KSR Teletype unit is the American Standard Code for Information Interchange (ASCII) modified. To convert the ASCII code to Teletype code add 200 octal (ASCII - 200_8 = Teletype). This code is read in the reverse of the normal octal form used in the PDP-7 since bits are numbered from right to left, from 1 through 8, with bit 1 having the most significance. Therefore, perforated tape is read:



Tape is loaded into the reader:



The Model 33 KSR set can generate all assigned codes except 340 through 374 and 376. Generally, codes 207, 212, 215, 240 through 337, and 377 are sufficient for Teletype operation. The Model 33 KSR set can detect all characters, but does not interpret all of the codes that it can generate as commands. The standard number of characters printed per line is 72. The sequence for proceeding to the next line is a carriage return followed by a line feed (as opposed to a line feed followed by a carriage return). Key or key combinations required to produce octal codes from 200 through 337, 375, and 377 are indicated in Table 9-9 with the associated ASCII character.

TABLE 9-9 TELETYPE CODE

Octal Code	Character Name	ASCII Character	Teletype Character	Key or Key Combinations
220	Null/Idle	NULL	---	CTRL @
201	Start of Message	SOM	---	CTRL A
202	End of Address	EOA	---	CTRL B
203	End of Message	EOM	---	CTRL C
204	End of Transmission	EOT	---	CTRL D
205	Who Are You	WRU	---	CTRL E
206	Are You	RU	---	CTRL F
207	Audible Signal	BELL	---	CTRL G
210	Format Effector	FE	---	CTRL H
211	Horizontal Tabulation	H TAB	---	CTRL I
212	Line Feed	LF	---	CTRL J
213	Vertical Tabulation	V TAB	---	CTRL K
214	Form Feed	FF	---	CTRL L
215	Carriage Return	CR	---	CTRL M
216	Shift Out	SO	---	CTRL N
217	Shift In	SI	---	CTRL O
220	Device Control Reversed for Data Line Escape	DC0	---	CTRL P
221	Device Control On	DC1	---	CTRL Q
222	Device Control (TAPE)	DC2	---	CTRL R
223	Device Control Off	DC3	---	CTRL S
224	Device Control (~~TAPE~~)	DC4	---	CTRL T
225	Error	ERR	---	CTRL U
226	Synchronous Idle	SYNC	---	CTRL V
227	Logical End of Media	LEM	---	CTRL W
230	Separator, Information	S0	---	CTRL X
231	Separator, Data Delimiters	S1	---	CTRL Y
232	Separator, Words	S2	---	CTRL Z
233	Separator, Groups	S3	---	SHIFT CTRL K

TABLE 9-9 TELETYPE CODE (cont)

Octal Code	Character Name	ASCII Character	Teletype Character	Key or Key Combinations
234	Separator, Records	S4	---	SHIFT CTRL L
235	Separator, Files	S5	---	SHIFT CTRL M
236	Separator, Misc.	S6	---	SHIFT CTRL N
237	Separator, Misc.	S7	---	SHIFT CTRL O
240	Space	SP	Space	Space Bar
241	Exclamation Point	!	!	SHIFT !
242	Quotation Marks	"	"	SHIFT "
243	Number Sign	#	#	SHIFT #
244	Dollar Sign	$	$	SHIFT $
245	Percent Sign	%	%	SHIFT %
246	Ampersand	&	&	SHIFT &
247	Apostrophe	'	'	SHIFT '
250	Parenthesis, Beginning	(	(	SHIFT (
251	Parenthesis, Ending	)	)	SHIFT)
252	Asterisk	*	*	SHIFT *
253	Plus Sign	+	+	SHIFT +
254	Comma	,	,	,
255	Hyphen	-	-	-
256	Period	.	.	.
257	Virgule	/	/	/
260	Numeral 0	0	0	0
261	Numeral 1	1	1	1
262	Numeral 2	2	2	2
263	Numeral 3	3	3	3
264	Numeral 4	4	4	4
265	Numeral 5	5	5	5
266	Numeral 6	6	6	6
267	Numeral 7	7	7	7

TABLE 9-9 TELETYPE CODE (cont)

Octal Code	Character Name	ASCII Character	Teletype Character	Key or Key Combinations
270	Numeral 8	8	8	8
271	Numeral 9	9	9	9
272	Colon	:	:	:
273	Semicolon	;	;	;
274	Less Than	<	<	SHIFT <
275	Equals	=	=	SHIFT =
276	Greater Than	>	>	SHIFT >
277	Interrogation Point	?	?	SHIFT ?
300	At	@	@	SHIFT @
301	Letter A	A	A	A
302	Letter B	B	B	B
303	Letter C	C	C	C
304	Letter D	D	D	D
305	Letter E	E	E	E
306	Letter F	F	F	F
307	Letter G	G	G	G
310	Letter H	H	H	H
311	Letter I	I	I	I
312	Letter J	J	J	J
313	Letter K	K	K	K
314	Letter L	L	L	L
315	Letter M	M	M	M
316	Letter N	N	N	N
317	Letter O	O	O	O
320	Letter P	P	P	P
321	Letter Q	Q	Q	Q
322	Letter R	R	R	R
323	Letter S	S	S	S

TABLE 9-9 TELETYPE CODE (cont)

Octal Code	Character Name	ASCII Character	Teletype Character	Key or Key Combinations
324	Letter T	T	T	T
325	Letter U	U	U	U
326	Letter V	V	V	V
327	Letter W	W	W	W
330	Letter X	X	X	X
331	Letter Y	Y	Y	Y
332	Letter Z	Z	Z	Z
333	Bracket, Left	[	[	SHIFT K
334	Reverse Virgule	\	\	SHIFT L
335	Bracket, Right	]	]	SHIFT M
336	Up Arrow (exponentation)	↑	↑	↑
337	Left Arrow	←	←	SHIFT ←
340 through 374 are not available				
375	Unassigned Control	(1)	---	ALT MODE
376	Not Available			
377	Delete/Idle/Rub Out	DEL	---	RUB OUT

Local Teletype Operation

The Teletype can be used as an ordinary typewriter in the following manner:

1. Set the computer lock switch to the counterclockwise position.
2. Set the computer POWER switch to the up position.
3. Set the Teletype LINE/OFF/LOCAL switch to the LOCAL position.
4. Type out the desired information on the Teletype keyboard.

PROGRAMMING

Refer to the PDP-7 Users Handbook F-75 for information on basic programming of the system. Refer to individual Digital Program Library documents for specific information on the format, specifications, and procedure for using a particular program language, such as PAL or FORTRAN.

CHAPTER 10

MAINTENANCE

Maintenance of the PDP-7 consists of procedures repeated periodically as preventive maintenance and tasks performed as corrective maintenance in the event of equipment malfunction. Maintenance activities require use of the equipment listed in Table 10-1, or equivalent, as well as the use of standard hand tools, cleansers, and test cables and probes.

TABLE 10-1 MAINTENANCE EQUIPMENT

Equipment	Manufacturer	Designation
Multimeter	Triplett or Simpson	Model 630-NA or 260
Oscilloscope	Tektronix	Type 547
Plug-in Unit	Tektronix	Type CA
Clip-on Current Probe	Tektronix	Type P6016
X 10 Probe	Tektronix	P6008
Recessed tip, 0.065 inch for wire wrap terminals	Tektronix	206-052
Current Probe Amplifier	Tektronix	Type 131
Hand Unwrapping Tool	Gardner-Denver	500130
Hand-Operated Wire-Wrap Tool with a 26263 Bit for 24 AWG wire and 18840 sleeve	Gardner-Denver	14H1C
FLIP CHIP Module Extender*	DEC	Type W980
Paint Spray Can*	DEC	DEC Blue 5150-S65
Air Filter*	Research Products Corp.	EZ Clean 2-inch Type MV
Filter-Kote*	Research Products Corp.	By Name
Teleprinter Input/Output Test*	DEC	Digital-7-50-M
Clock Interrupt Test Program*	DEC	Digital-7-51-M
CONTEST II*	DEC	Digital-7-52-M

*One is supplied with the equipment

TABLE 10-1 MAINTENANCE EQUIPMENT (continued)

Equipment	Manufacturer	Designation
Reader and Punch Test*	DEC	Digital-7-53-M
Maindec 401 (Instruction Test)*	DEC	Digital-7-54-M
Maindec 402 (Checkerboard)*	DEC	Digital-7-55-M
Maindec 403 (Address Test)*	DEC	Digital-7-56-M
Maindec 410 (RPB Test)*	DEC	Digital-7-57-M

*One is supplied with the equipment

The Maindec routines are diagnostic programs designed to exercise or test specific functions within the computer system. Maindec routines are prepared as perforated-paper program tapes in readin mode format. Each tape is accompanied by a detailed description of the program contained on the tape, procedures for using the program, and information on analyzing the program results to locate specific circuit failures. Use of these routines is indicated at the appropriate points in this manual as they apply to preventive or corrective maintenance of the standard PDP-7 system.

Turn off all power before extracting or inserting modules. Access to controls on the module for use in adjustment, or access to points used in signal tracing can be gained by removing the module (use a straight, even pull to prevent twisting of the printed-wiring board), connecting a Type W380 FLIP CHIP Module Extender into the vacated module connector in the mounting panel, and then inserting the module into the extender.

CAUTION

FLIP CHIP modules may be harmed by removing or inserting them with power on. Failure is not caused by the transient voltage but rather by brushing the free module against one plugged in. Failure to one or both modules may result. Do not remove FLIP CHIP modules with power on.

The procedures presented here assume that the reader understands the function of the keys, switches, and indicators on the operator console and is familiar with machine programming as described in the PDP-7 Users Handbook F-75.

In addition to the controls and indicators on the operator console, the indicator panel, and on the Teletype unit (described in Tables 9-1 through 9-5); maintenance operations use controls and indicators on the marginal-check panel (which is mounted at the top of bay 3, in the front of the computer) and on the Type 832 Power Control. The function of these controls and indicators is described in Table 10-2, and the marginal-check panel is shown in Figure 10-1.

TABLE 10-2 MAINTENANCE CONTROLS AND INDICATORS

Control or Indicator	Function
	Marginal-Check Panel
Voltmeter	Indicates the output voltage of the marginal-check poser supply in either polarity.
Toggle switches (four)	The bottom switch applies a −15v marginal-check voltage to the Teletype control. The active position for the switch is up. The second switch from the bottom applies a +10v marginal-check voltage to the Teletype control. The active position is up. The other two switches are not used.
Selector switch	Controls the output of the marginal-check power supply. In the +10 MC position, the output is positive and is connected to the orange +10 MC connector. In the −15MC position, the output is negative and is connected to the green −15 MC connector. The center position is off and disconnects the output from the marginal-check power supply.
Elapsed time meter	Indicates the cumulative total number of hours during which the computer has been energized, and so provides a unit of measure that is more appropriate than calendar time for determining preventive maintenance schedules.

TABLE 10-2 MAINTENANCE CONTROLS AND INDICATORS (continued)

Control or Indicator	Function
	Marginal-Check Panel (continued)
Control Knob	Controls the output of rhe marginal-check voltage to any level between 0 and 20v.
	832 Power Control
Circuit breaker	Protects the computer power source from overload due to failure of the computer power circuits.
REMOTE/OFF/LOCAL switch	Allows control of the computer primary power from the back of the machine during maintenance. In the REMOTE position, application and removal of computer power is controlled by the lock and POWER switches on the operator console. In the OFF position the computer is de-energized, regardless of the position of switches on the operator console. In the LOCAL position the computer is energized regardless of the position of operator console switches or door interlocks.
MEM. POWER switch	Controls the application and removal of operating voltages for the memory circuits.

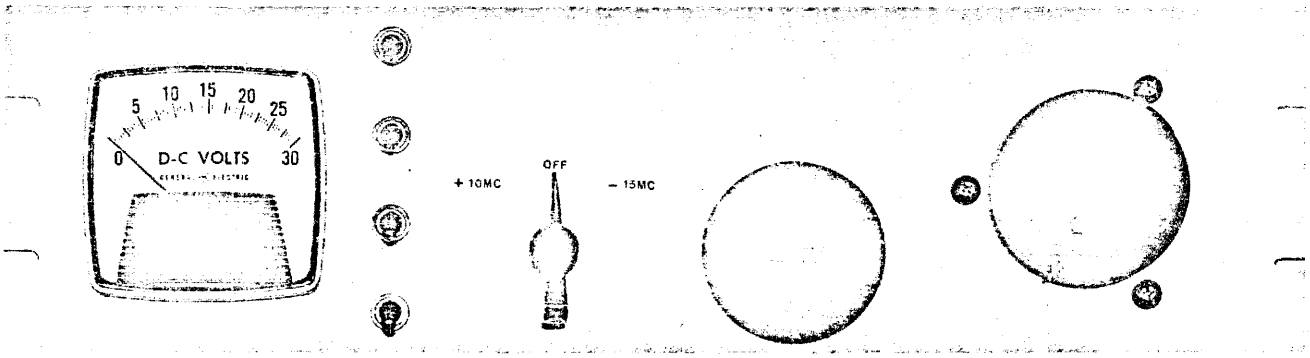


Figure 10-1 Marginal-Check Panel

PREVENTIVE MAINTENANCE

Preventive maintenance consists of tasks performed periodically during the operating life of the equipment to ensure that it is in satisfactory operating condition. Faithful performance of these tasks helps to forestall incipient failures by discovering progressive deterioration and correcting minor damage at an early stage. Data obtained during the performance of each preventive maintenance task should be recorded in a log book. Analysis of this data indicates the rate of circuit operation deterioration and provides information for determining when components should be replaced to prevent failure of the system. Preventive maintenance tasks consist of mechanical checks, which include cleaning and visual inspections; marginal checks, which aggravate border-line circuit conditions or intermittent failures so that they can be detected and corrected; and checks of specific circuit elements such as the power supply, sense amplifiers and master slice control, and memory selectors.

All preventive maintenance tasks should be performed as a function of conditions at the installation site. Perform the mechanical checks at least once each month or as often as required to allow efficient functioning of the air filter. All other tasks should be performed on a regular schedule, at an interval determined by the reliability requirements of the system. A typical recommended schedule is every 600 equipment operating hours or every four months, whichever is completed first. The most important schedule to maintain is that of the simplest procedure--the mechanical checks. Many hours of computer down time can be avoided by rigid adherence to a schedule based upon the condition of the air filter. Machine failures can occur due to overheating caused by the air filters becoming so dirty that no cooling air can be drawn into the cabinet by the fans.

Mechanical Checks

Assure good mechanical operation of the equipment by performing the following steps and the indicated corrective action for any substandard condition found:

1. Clean the exterior and the interior of the equipment cabinet using a vacuum cleaner or clean cloths moistened in nonflammable solvent.

2. Clean the air filters of the bottom of the cabinets. Remove each filter by removing the fan and housing, which are held in place by two knurled

and slotted captive screws. Wash each filter in soapy water and dry it in an oven or by spraying with compressed gas. Spray each filter with Filter-Kote (Research Products Corporation, Madison, Wisconsin).

3. Lubricate door hinges and casters with a light machine oil. Wipe off excess oil.

4. Visually inspect the equipment for completeness and general condition. Repaint any scratched or corroded areas with DEC blue tweed paint number 5150-S65.

5. Inspect all wiring and cables for cuts, breaks, fraying, wear, deterioration, kinks, strain, and mechanical security. Tape, solder, or replace any defective wiring or cable covering.

6. Inspect the following for mechanical security: keys, switches, control knobs, lamp assemblies, jacks, connectors, transformers, fans, capacitors, elapsed time meter, etc. Tighten or replace as required.

7. Inspect all module mounting panels to assure that each module is securely seated in its connector.

8. Inspect power supply capacitors for leaks, bulges, or discoloration. Replace any capacitors giving these signs of malfunction.

Power Supply Checks

Perform the following power supply output checks outlined in Table 10-3. Use a multimeter to make the output voltage measurements with the normal load connected. Use the oscilloscope to measure the peak-to-peak ripple content on all dc outputs of the supply. The +10 and -15v supplies are not adjustable; therefore, if any output voltage or ripple content is not within specifications, the power supply giving these indications should be considered defective and troubleshooting procedures should be initiated. Refer to the engineering drawing listed in the table.

TABLE 10-3 POWER SUPPLY OUTPUT CHECKS

Measurement Terminals at Power Supply Output	Nominal Output (Volts dc)	Acceptable Output Range (Volts)	Maximum Output Current (Amperes)	Maximum Peak-to-Peak Output Ripple (Volts)
		Type 728 Power Supply (RS-B-728)		
Red (+) to Yellow (-)	+10	+9.5 to 11.5	7.5	0.7
Yellow (+) to Blue (-)	-15	-14.5 to 16.5	8.5	0.4
		Type 778 Power Supply (RS-B-778)		
Red (+) to Blue (-)	-15	-14.5 to 16.5	8.5	0.6
		Type 779 Power Supply (RS-B-779)		
Orange (+) to Yellow (-)	+10	+9.6 to 11.0	7.5	1.0
Yellow (+) to Blue (-)	-15	-14.5 to 16.0	8.0	0.4
Red (+) to Yellow (-)	+15	+14.5 to 16.0	7.5	1.1
Yellow (+) to Green (-)	+15	+14.5 to 16.0	7.5	1.1

Check the operation of the variable-output Type 738 Power Supply which produces the marginal-check voltages. With all of the normal/marginal switches in the normal (down) position, make the following measurements at the color-coded connector at the right side of any convenient module mounting panel:

1. Connect a multimeter between the yellow (-) and black (+) terminals; set the +10 MC/OFF/-15 MC switch to the -15 MC position, and turn the control knob clockwise to assure that at least -20 volts can be produced by the supply (as indicated on the multimeter). Record the indication given on both the marginal check voltmeter on the panel and on the multimeter.

These indications should be equal ±1 volt. Connect the oscilloscope to the yellow terminal, and measure the peak-to-peak ripple content to assure that it is no more than 1.0 volt. Turn the control knob fully counterclockwise; set the +10 MC/OFF/-15 MC switch to the OFF position, and disconnect the multimeter and oscilloscope.

2. Connect the multimeter between the green (+) and black (-) terminals; set the +10 MC/OFF/-15 MC switch to the +10 MC position, and turn the control knob clockwise to assure that at least +20 volts can be produced by the supply. Turn the control knob fully counterclockwise, set the +10 MC/OFF/-15 MC switch to the OFF position, and disconnect the multimeter.

The Type 739 Power Supply output is not measured during this check, since it is monitored and adjusted during the Memory Current Check.

Marginal Checks

Marginal checking utilizes the Maindec diagnostic programs to test the functional capabilities of the computer with the module-operating voltages biased above and below the nominal levels. Biasing the operating voltages aggravates borderline circuit conditions within the modules to produce failures which are detected by the program. When the program detects an error, it usually provides a printout or visual indication which is helpful in locating the source of the fault, and then halts. Therefore, marginal components can be replaced during scheduled preventive maintenance to forestall possible future equipment failure. The biased operating voltages at which circuits fail are recorded in the maintenance log. By plotting the bias voltages obtained during each scheduled preventive maintenance, progressive deterioration can be observed and expected failure dates can be predicted. In this manner these checks provide a means of planned replacement. These checks can also be used as a troubleshooting aid to locate marginal or intermittent components, such as deteriorating transistors.

Raising the operating voltages above +10v increases the transistor cutoff bias that must be overcome by the previous driving transistor, therefore low-gain transistors fail. Lowering the bias voltage below +10v reduces transistor base bias and noise rejection and thus provides a

test to detect high-leakage transistors. Lowering this voltage also simulates high-temperature conditions (to check for thermal run away). Raising and lowering the -15v supply increases and decreases the primary collector supply voltage for all modules and so affects output signal voltage.

Since marginal voltages attainable vary for different circuit changes and/or system configurations, determine the expected marginal-check voltages for a specific system from the initial factory test records and any subsequent test records in the maintenance log. A record of margins obtained at the factory for a specific system is provided with each system and serves as a base for all preventive and corrective maintenance procedures. With time and normal circuit operation deterioration, margins will decrease. This decrease does not affect reliable operation of the machine until there is little or no margin at all. The normal slow rate of margin decay can be used to predict the time at which the system should be refurbished to prevent sudden failure. Margins do provide a measure of circuit performance and so can be used to certify correct or defective operation. However, failure of a system to obtain the same margins year after year does not constitute a defect in the operation of the system. For example, if a specific margin decreases at the rate of 0.5v per year, no trouble is indicated. If this margin suddenly decreases by 0.7v in six months, troubleshooting procedures should be undertaken to determine the cause of this rapid change.

CAUTION

Do not increase the −15v margin beyond −18v. Failure to observe this precaution may cause serious damage to the logic elements.

Marginal check voltages are supplied to the various sections of the processor through connections made to the module connectors in each mounting panel. Each marginal check voltage may be adjusted throughout the range of 0 to 20v by means of the control knob and voltmeter located on the marginal-check control panel. The selector switch on this panel selects either the +10 or the −15 marginal-check voltage. Power supply leads to the module connectors in the mounting panels are color-coded as follows:

Orange	+10v marginal-check supply
Red	+10v normal power supply
Black	Ground
Blue	-15v normal power supply
Green	-15v marginal-check supply

Marginal check and normal supply voltages are distributed to each of two module rows in each mounting panel by means of two SPDT switches on the marginal check panel of each assembly. There are two positions for each SPDT switch: normal (down) and marginal-check (up). Therefore the modules in one mounting panel (two rows) may be marginally checked while all other rows maintain normal voltage. In each module mounting panel, the upper switch controls the +10v supply and the lower controls the -15v supply (with mounting panel viewed from the connector side and switches on the left).

To perform the checks:

1. Assure that all normal/marginal-check switches on each module mounting panel are in the normal (down) position (normal +10v and -15v power supplies are being used).

2. Set the +10 MC/OFF/-15 MC selector switch on the marginal-check control panel to the +10 MC position.

3. Adjust the output of the marginal-check power supply so that the marginal-check voltmeter indicates 10v.

4. Set the +10 normal/marginal switch for the first panel row to be checked to the marginal-check (up) position.

5. Start computer operation in a diagnostic program or routine which fully utilizes the circuits in the panel to be tested. If no program is suggested by the normal system application, select an appropriate Maindec program from Table 10-4. To completely test the PDP-7, all Maindec programs listed in Table 10-4 should be performed at elevated and reduced voltages for each supply terminal (+10, -15) and for each module mounting panel indicated in the table.

6. Decrease the marginal-check power supply output until normal system operation is interrupted. Record the marginal-check voltage. At this point marginal transistors can be located and replaced, if desired. Readjust the marginal-check power supply output to the nominal +10v level.

7. Restart computer operation. Increase the marginal-check supply output until normal computer operation is interrupted, at which point record the marginal-check voltage. Transistors can again be located and replaced. Readjust the marginal-check power supply to the nominal +10v level.

8. Return the normal/marginal switch to the normal (down) position.

9. Repeat steps 4 through 8 for each of the other panels to be checked by biasing the +10v line.

10. Set the +10 MC/OFF/-15 MC selector switch on the marginal-check power supply to the -15 MC position and adjust the output until the marginal-check voltmeter indicates 15v.

11. Set the -15 normal/marginal switch to the marginal-check (up) position for the first panel row to be checked, then repeat step 5.

12. Repeat steps 6 and 7, readjusting the marginal-check power supply to the nominal -15v level at the end of each step. Return the normal/marginal switches to the normal (down) position.

13. Repeat steps 10 through 12 for each other module mounting panel row to be tested by biasing the -15v line.

14. Set the +10 MC/OFF/-15 MC selector switch to the OFF position.

TABLE 10-4 MARGINAL TEST PROGRAMS

Mounting Panel Row Tested	Diagnostic (MAINDEC) Test					
	Clock Interrupt Test Digital-7-51-M	Memory Checkerboard Test 402 Digital-7-55-M	Address Test 403 Digital-7-56-M	Contest II Digital-7-52-M	Reader and Punch Test Digital-7-53-M	Teleprinter Test Digital-7-50-M
CP 1A		+10				
CP 1B		+10		+10, -15		
CP 1C		+10		+10, -15		
CP 1D				+10, -15		
CP 1E	* ** +10, -15			+10, -15	+10, -15	+10, -15
CP 1F				+10, -15		
CP 1H				+10, -15		
CP 1J				+10, -15		
CP 1K				+10, -15		
CP 1L	* ** +10, -15			+10, -15		
CP 1M	* ** +10, -15			+10, -15	+10, -15	+10, -15

* This check made with third (from the top) toggle switch on marginal-check panel in the ON (up) position.
**This check made with bottom toggle switch on marginal-check panel in the ON (up) position.

TABLE 10-4 MARGINAL TEST PROGRAMS (continued)

Mounting Panel Row Tested	Diagnostic (MAINDEC) Test					
	Clock Interrupt Test Digital-7-51-M	Memory Checkerboard Test 402 Digital-7-55-M	Address Test 403 Digital-7-56-M	Contest II Digital-7-52-M	Reader and Punch Test Digital-7-53-M	Teleprinter Test Digital-7-50-M
CP 1N						
MEM 1A		+10	+10			
MEM 1B		+10	+10			
MEM 1H		+10	+10			
MEM 1J		+10	+10			
DS 2A	* ** +10, -15				+10, -15	+10, -15
DS 2B	* ** +10, -15				+10, -15	+10, -15
DS 2C	* ** +10, -15				+10, -15	+10, -15
Reader/Punch 3A	* ** +10, -15				+10, -15	
Reader/Punch 3B	* ** +10, -15				+10, -15	
Teletype Control	* ** +10, -15					* ** +10, -15
Teletype Control						+10, -15

* This check made with third (from the top) toggle switch on marginal-check panel in the ON (up) position.

[illegible] toggle switch on marginal-check panel in the ON (up) position.

Memory Current Check

Measure the read/write and inhibit currents in the core memory. These currents should be approximately equal to the values specified on the memory array label (approximately 330 ma and 290 ma, respectively). This label indicates the optimum memory setting determined at the factory. Allow the equipment to warm up for approximately 1 hr before making measurements. Whenever possible this check should be performed at an ambient temperature of 25°C. Compensate measured read-write and inhibit currents by subtracting 1 ma for every degree of ambient temperature above 25°C. (Add 1 ma for each degree below 25°C.) The memory current check and sense amplifier check procedures must not be performed when the equipment temperature is below 20°C.

Measure the read/write current using the oscilloscope and clip-on current probe at the read side of a fully selected drive line of the X or Y axis G202 Memory Selector Switch. The READ terminals are either L and P, or M and N of a G202 module. Refer to the G202 module schematic. Synchronize the oscilloscope with the negative transition of the READ signal found at location 1B202H. Adjust the read/write current to 330 ma or to the value specified on the memory array label by rotation of R16 in the G808 read/write power supply control module.

In a similar manner, measure the inhibit current by connecting the clip-on current probe at a proper terminal of the inhibit connector located at 1B10. See drawing G201 for the appropriate inhibit terminal. Synchronize the oscilloscope on the negative transition of the INH(B) line found at location 1B10J. Adjust the inhibit current to 290 ma or to the value indicated on the memory array label.

To obtain consistent measurements, the current probe should be positioned to indicate read current as a negative pulse, and write and inhibit currents as positive pulses as displayed on the oscilloscope. All current amplitude measurements should be made just before the knee in the curve of the trailing edge of a pulse. Note that read and write currents are measured from base line to peak amplitude, not from peak to peak.

Sense Amplifier Check

The G001 Sense Amplifier modules are adjusted for optimum efficiency through marginal checking techniques. Perform the marginal checks using the Memory Checkerboard Program, Maindec 402. See Table 10-4 for marginal power supply used, and set the SPDT switches accordingly. Check and adjust each SA circuit so that approximately equal positive and negative margins can be obtained, using the +10v marginal power supply.

Sense amplifiers are located at 1H and 1J, 1 through 19. The master slice control is located at 1H20.

CORRECTIVE MAINTENANCE

The PDP-7 is constructed of highly reliable transistorized FLIP CHIP modules. Use of these circuits and faithful performance of the preventive maintenance tasks ensure relatively little equipment downtime due to failure. Should a malfunction occur, the condition should be analyzed and corrected as indicated in the following procedures. No test equipment nor special tools are required for corrective maintenance other than a broad bandwidth oscilloscope and a standard multimeter. However, a clip-on current probe such as the Tektronix Type P6016 with a Type 131 Current Probe Amplifier is very helpful in monitoring memory currents. The best corrective maintenance tool is a thorough understanding of the physical and electrical characteristics of the equipment. Persons responsible for maintenance should become thoroughly familiar with the system concept, the logic drawings, the operation of specific module circuits, and the location of mechanical and electrical components.

It is virtually impossible to outline any specific procedures for locating faults within complex digital systems such as the PDP-7. However, diagnosis and remedial action for a fault condition can be undertaken logically and systematically in the following phases:

1. Preliminary investigation to gather all information and to determine the physical and electrical security of the computer.

2. System troubleshooting to locate the fault to within a module through the use of control panel troubleshooting, signal tracing, or aggravation techniques.

3. Circuit troubleshooting to locate defective parts within a module.

4. Repairs to replace or correct the cause of the malfunction.

5. Validation tests to assure that the fault has been corrected.

6. Log entry to record pertinent data.

Preliminary Investigation

Before commencing troubleshooting procedures, explore every possible source of information. Ascertain all possible information concerning any unusual function of the machine prior to the fault and all possible data about the symptoms given when the fault occurred, such as the program in progress, condition of operator console indicators, etc. Search the maintenance log to determine if this type of fault has occurred before or if there is any cyclic history of this kind of fault, and determine how this condition was previously corrected. When the entire machine fails, perform a visual inspection to determine the physical and electrical security of all power sources, cables, connectors, etc. Assure that the power supplies are working properly and that there are no power short circuits by performing the Power Supply Checks as described under Preventive Maintenance. Check the condition of the air filter in the bottom of the cabinet. If this filter becomes clogged, the temperature within the cabinet might rise sufficiently to cause marginal semiconductors to become defective.

System Troubleshooting

Do not attempt to troubleshoot the system without first gathering all information possible concerning the fault, as outlined in the Preliminary Investigation.

Maindec Diagnostic Programs

The Maindec Diagnostic Programs listed in Table 10-1 are provided for locating sources of malfunction within the processor, memory, and I/O equipment. Since these divisions encompass the complete PDP-7 system, any trouble may be located generally by the Maindec programs, and a local program loop may be devised to pinpoint the malfunction to a specific module.

Maindecs 401, 402, and 403 specifically test processor and memory functions. Maindec 410 tests functioning of the reader and punch buffer. These diagnostic programs are particularly useful under marginal checking conditions.

Maindec 401 tests the instruction cycling, processor registers, and controls (including the PC). Maindec 402 tests memory core storage by producing bit patterns in the cores that will cause worst-noise conditions within the core array. Defective cores are detected in this manner. Maindec 403 tests address selection, and is, therefore, a powerful means of troubleshooting the entire memory address system, including the MA register, MB register, memory selector switches, and all controls associated with these functions.

Each Maindec diagnostic program instruction manual contains full particulars for loading the program, interpreting the results, and operating the PDP-7 for diagnostic testing. Chapter 9 of this maintenance manual also contains instructions for loading and starting Maindec programs.

Commence troubleshooting by performing that operation in which the malfunction was initially observed, using the same program. Thoroughly check the program for proper control settings. Careful checks should be made to assure that the PDP-7, and not the peripheral equipment, is actually at fault before continuing with corrective maintenance procedures. Faults in equipment, check with transmits or receive information, or improper connection of the system frequently gives indications very similar to those caused by computer malfunction. Faulty ground connections between peripheral equipment and the computer are a common source of trouble. From

that portion of the program being performed and the general condition of the indicators, the logical section of the machine at fault can usually be determined.

If the fault has been isolated to the computer but cannot be immediately localized to a specific logic function, it can usually be determined to be within either the core memory or the processor logic circuits. Proceed to the Memory Troubleshooting or Logic Troubleshooting procedures. When the location of a fault has been narrowed to a logic element, continue troubleshooting to locate the defective module or component by means of signal tracing. If the fault is intermittent, a form of aggravation test should be employed to locate the source of the fault.

Memory Troubleshooting

If the entire memory system fails, use the multimeter to check the outputs of the 739 Power Supply. Measure the voltages at the terminal strip as indicated on engineering drawing RS-B-739. Do not attempt to adjust this supply. If the supply is defective, troubleshoot it and correct the cause of the trouble; then adjust the output voltage by performing the Memory Current Check. If the power supply is functioning properly, proceed as follows:

The following test set-up permits sequential addressing (in binary form) of the core memory through the MA register and read/write memory selectors.

1. De-energize the computer.
2. Connect a jumper from 1K21H to ground.
3. Restore computer power and press the START key.

This discussion references the X and Y axis selection drawings, BS-E-149-0-46 and BS-E-149-0-47 and the memory control drawing BS-D-7-0-27. Looking at the X and Y axis drawings, note that a core address is selected by a combination of two G202 switch selectors: one on the left side of the array; the other on the bottom of the array. READ or WRITE transitions, buffered by the BD module at location 1B30, trigger all G202 selectors which generate and distribute the actual read/write current to specific cores. In each axis, selection of the two G202 switches is accomplished by the bit configuration in the MA register. The actual

read/write current pulses flow from the positive supply line, through a left G202 selector, through a horizontal core matrix line, through the core and diodes, down a vertical core matrix line to a bottom G202 selector, and into the negative return line.

A train of current spikes will be seen, and missing spikes will then represent malfunctioning addresses. Read currents are at terminals E and M; write currents are at terminals K and P of each drive selector. Before loading a Maindec Address program to find specific address malfunction, trace the read/write gating pulses from the BD module at 1B30 and all the H and J terminals of every G202 module. A G202 Switch Selector module cannot select without the gating pulse. If the read/write currents are not as specified on the memory array labels, adjust the Type G800 control module current accordingly.

Perform the Memory Address Test program (Maindec 403) to locate defective core memory addresses. Complete the entire program and record all addresses which fail. Inspect the record of failure addresses for common bits. Refer to engineering drawings BS-E-149-0-46 and BS-E-149-0-47, and check the memory selectors that decode common bits of the failing addresses. Also check the associated resistor board and memory matrix module.

If an address is dropping bits, use the operator console to deposit all binary 1's in that address. Then examine the contents of the address to determine which bit position is not being set (contains a 0). Check the sense amplifier, inhibit driver, and resistor board for the associated bit. Also check the memory inhibit current as described in the Memory Current Check.

If an address is picking up bits, use the operator console to deposit all binary 0's in that address, and proceed as described in the previous paragraph.

To locate the cause of a specific address failure, use the oscilloscope and current probe to trace read and write current while performing a repetitive program such as the Memory Address Test program or the Memory Checkerboard Test program.

Perform the Memory Checkerboard Test program (Maindec 402) to troubleshoot all other memory conditions.

Logic Troubleshooting

If the instructions do not seem to be functioning properly, perform the Instruction Test program (Maindec 401). This test halts to indicate instructions that fail. Wnen an instruction fails, as indicated by the operator console indicators when the program stops, or by the diagnostic printout that follows the error halt, consult the descriptive manual for the Maindec 401 to obtain an interpretation that will localize the fault.

If the computer interrupt system or the Teletype teleprinter do not seem to be functioning properly, perform the Teleprinter Test Program, Digital 7-50-M. If the tape reader or punch operation is questionable, perform the Reader and Punch Test (Digital-7-53-M) or the RPB Test (Maindec 410).

Refer to the Teletype and Digitronics documents for detailed maintenance information on the Model 33 KSR set, BRPE Tape Punch Set, and Model 2500 Perforated Tape Reader.

Signal Tracing

If the fault has been located within a functional logic element, program the computer to repeat some operation in which all functions of that element are utilized. Use the oscilloscope to trace signal flow through the suspected logic element. Oscilloscope sweep can be synchronized by control signals or clock pulses, which are available on individual module terminals at the wiring side (front) of the equipment. Circuits transferring signals with external equipment are most likely to encounter difficulty. Trace output signals from the interface connector back to the origin, and trace input signals from the connector to the final destination. The signal tracing method can be used to certify signal qualities such as pulse amplitude, duration, rise time, and the correct timing sequence. Refer to the table on engineering drawing BS-D-7-0-22 to check or adjust the timing of circuits in the main timing chain or special timing chain generators. If an intermittent malfunction occurs, signal tracing must be combined with an appropriate form of aggravation test.

Aggravation Tests

Intermittent faults should be traced through aggravation techniques. Intermittent logic malfunctions are located by the performance of marginal-check procedures as described under Preventive Maintenance.

Intermittent failures caused by poor wiring connections can often be revealed by vibrating modules while running a repetitive test program. Often, tapping a wooden rod held against the handles of a suspect panel of modules is a useful technique. By repeatedly starting the test program and vibrating fewer and fewer modules, the malfunction can be localized to within one or two modules. After isolating the malfunction in this manner, check the seating of the modules in the connector; check the module connector for wear or misalignment, and check the module wiring for cold solder joints or wiring kinks.

Circuit Troubleshooting

The procedure followed for troubleshooting and correcting the cause of faults within specific circuits depends upon the downtime limitiations of equipment use. Where downtime must be kept at a minimum, it is suggested that a provisioning parts program be adopted to maintain one spare module, power supply, or standard component which can be inserted into the cabinet when system troubleshooting procedures have traced the fault to a particular component. Static and dynamic bench tests can then be performed without interfering with system operation. Where downtime is not critical, the spare parts list can be reduced and module troubleshooting procedures can be performed with the modules in-line (within the system). Altnough in-line module troubleshooting extends the downtime of the system, it is economical of personnel time because the module can be program exercised to locate the cause of the fault more rapidly.

Module Circuits

Basic functions and specifications for standard system modules used in the PDP-7 are presented in the FLIP CHIP Modules catalog, C-105. Circuit schematics are provided in Chapter 11 of the manual for all modules not described in the catalog. Schematic diagrams of all modules are provided in the set of formal engineering supplied with each system. The following design considerations may also be helpful in troubleshooting standard modules.

1. Forward-biased silicon diodes are used in the same manner as Zener diodes, usually to provide a voltage differential of 0.75v. For instance, a series string of four diodes is used to produce the -3 vdc clamp voltage used in most modules.

2. The state of DEC flip-flops is changed by an incoming pulse which turns off the conducting transistor amplifier. Since these flip-flops use PNP transistors, the input pulse must be positive and must be coupled to the base of the transistor. Flip-flop modules that accept negative pulses to change the state invert this pulse by means of a normal transistor inverter circuit.

3. Fixed-length delay lines such as the W300 are extremely reliable and very seldom malfunction. However, if a malfunction should occur, these delay lines should not be replaced on the printed-wiring board. In such cases the entire module should be returned to DEC for repair.

4. The W607 and W640 modules both contain three independent pulse amplifiers, each with its own input inverter. Output pulse duration is determined by the time required to saturate the interstate coupling transformer. No multivibrators or other RC timing circuits are used in the pulse amplifiers.

In-Line Dynamic Tests

To troubleshoot a module while maintaining its connection within the system:

1. De-energize the computer.

2. Remove the suspect module from the mounting panel.

3. Insert a W980 FLIP CHIP Module Extender into the mounting panel connector which normally holds the suspect module.

4. Insert the suspect module into the module extender. All components and wiring points of the module are now accessible.

5. Energize the computer and establish the program conditions desired for troubleshooting the module. Trace voltages or signals through the module, using a dc voltmeter or an oscilloscope, until the source of the fault is located.

In-Line Marginal Checks

Marginal checks of individual modules can be performed within the computer to test specific modules of questionable reliability, or to further localize the cause of an intermittent failure which has been localized to within one module mounting panel by the normal marginal checking method. These checks are performed with the aid of a modified W980 FLIP CHIP Module Extender. To modify an extender for these checks:

1. Disconnect module receptacle terminals A, B, and C from the male plug connection terminals. This can be accomplished by cutting the printed wiring for these lines near the plug end and removing a segment of this wiring in each line.

2. Solder a 3-ft test lead to the printed wiring for terminals A, B, and C. Make this solder joint close to the receptacle end of the extender, certainly on the receptacle side of the wiring break. Observe the normal precautions when making this connection to assure that excessive heat does not delaminate the printed-wiring board and that neither solder nor flux provides conduction between lines.

3. Attach a spade lug, such as an AMP 42025-1 Power Connector to the end of each test lead and label each lead to correspond to the A, B, or C terminal of the receptacle to which it is connected.

To marginal check a module within the computer:

1. De-energize the computer.

2. Remove the module to be checked from the module mounting panel; replace it with the modified extender, and insert the module in the extender.

3a. If the +10v marginal check is to be performed, connect test lead A to the +10v orange connector terminal at end of the panel. Connect test lead B to the normal -15v blue connector terminal and test lead C to black ground connector.

3b. When performing the -15v marginal check, connect test lead A to the normal +10v red connector, test lead B to the -15v green connector terminal, and test lead C to the black ground terminal. Keep all SPDT switches in the down position.

4. Restore computer power, adjust the marginal-check power supply to provide the nominal voltage output, and start operation of a routine which fully utilizes the module being checked. The procedures and routines suggested in Preventive Maintenance for use in marginal checking the computer can be used as a guide to marginal checking modules.

5. Increase or decrease the output of the marginal-check power supply until the routine stops, indicating module failure. Record each bias voltage at which the module fails. Also record the condition of all operator console controls and indicators when a failure occurs. This information indicates the module input conditions at the time of the failure and is often helpful in tracing the cause of a fault to a particular component part.

6. Repeat steps 4 and 5 for each of the three bias voltages. If margins of ±5v on the +10 vdc supplies can be obtained, and the -15 vdc supply can be adjusted between -7v and -18v without module failure, a module can be assumed to be operating satisfactorily. If the module fails before these margins are obtained, use normal signal tracing techniques within the module to locate the source of the fault.

Static Bench Tests

Visually inspect the module on both the component side and the printed-wiring side to check for short circuits in the etched wiring and for damaged components. If this inspection fails to reveal the cause of trouble or to confirm a fault condition observed, use the multimeter to measure resistances.

CAUTION

Do not use the lowest or highest resistance ranges of the multimeter when checking semiconductor devices. The X10 range is suggested. Failure to heed this warning may result in damage to components.

Measure the forward and reverse resistances of diodes. Diodes should measure approximately 20 ohms forward and more than 1000 ohms reverse. If readings in each direction are the same, and no parallel paths exist, replace the diodes.

Measure the emitter-collector, collector-base, and emitter-base resistances of transistors in both directions. Most catastrophic failures are due to short circuits between the collector and the emitter or are due to an open circuit in the base-emitter path. A good transistor indicates an open circuit in both directions between collector and emitter. Normally 50 to 100 ohms exist between the emitter and the base or between the collector and the base in the forward direction, and open-circuit conditions exist in the reverse direction. To determine forward and reverse directions, a transistor can be considered as two diodes connected back-to-back. In this analogy PNP transistors are considered to have both cathodes connected together to form the base, and both the emitter and collector assume the function of an anode. In NPN transistors the base is assumed to be a common-anode connection, and both the emitter and collector are assumed to be the cathode.

Multimeter polarity must be checked before measuring resistances, since many meters (including the Triplett 630) apply a positive voltage to the common lead when in the resistance mode. Note that although incorrect resistance readings are a sure indication that a transistor is defective, correct readings give no guarantee that the transistor is functioning properly. A more reliable indication of diode or transistor malfunction is obtained by using one of the many inexpensive in-circuit testers commercially available.

Damaged or cold-solder connections can also be located using the multimeter. Set the multimeter to the lowest resistance range and connect it across the suspected connection. Poke at the wires or components around the connection, or alternately rap the module lightly on a wooden surface, and observe the multimeter for open-circuit indications.

Often the response time of the multimeter is too slow to detect the rapid transients produced by intermittent connections. Current interruptions of very short duration, caused by an intermittent connection, can be detected by connecting a 1.5v flashlight battery in series with a 1500-ohm resistor across the suspected connection. Observe the voltage across the 1500-ohm resistor with an oscilloscope, while probing the connection.

Dynamic Bench Tests

In general, a module which fails marginal in-line tests, or is suspect for other reasons, should be returned to DEC for repair or replacement. Many modules require special equipment for dynamic testing, since the timing of pulse amplifiers and delay modules must be rigorously maintained within narrow limits. Dynamic tests, therefore, should be oriented only toward discovery of defective semiconductors. Dynamic tests may be carried out by means of a Type H901 Patchcord Mounting Panel connected to the computer power supply outputs by means of Type 914 Power Jumpers. Simulated ground-level signals may then be applied to the module under test, using Type 911 Patchcords, and output terminals of the module under test can be monitored by an oscilloscope connected to terminals on the front of the Type H901 panel. (Simulated negative-level signal inputs are not required, since FLIP CHIP module input terminals are internally clamped at -3v, so open input terminals simulate a -3v signal input.)

Repair

Repairs to FLIP CHIP modules should be limited to the replacement of semiconductors. In all soldering and unsoldering operations in the repair and replacement of parts, avoid placing excessive solder or flux on adjacent parts or service lines. When soldering semiconductor devices (transistors, crystal diodes, and metallic rectifiers) which may be damaged by heat, the following special precautions should be taken:

1. Use a heat sink, such as a pair of pliers, to grip the lead between the device and the joint being soldered.

2. Use a 6v soldering iron with an isolation transformer. Use the smallest soldering iron adequate for the work.

3. Perform the soldering operation in the shortest possible time, to prevent damage to the component and delamination of the module etched wiring.

When any part of the equipment is removed for repair and replacement, make sure that all leads or wires which are unsoldered, or otherwise disconnected, are legibly tagged or marked for identification with their respective terminals. Replace defective components only with parts of equal or better quality and equal or narrower tolerance.

Spare Parts

Each user of the PDP-7 system should establish a spare parts stock which is in accordance with the extent of the available repair facilities. The following considerations will be of help in determining what spare parts should be stocked.

Teletype

Users who do not have maintenance personnel trained in the maintenance and repair of Teletype units should keep a complete Model 33 Keyboard Send Receive Teletype near the computer. If the on-line unit becomes defective, the spare should be substituted to avoid computer downtime. However, many users do have facilities for the maintenance of Teletype units. It is suggested that such users should stock the spare parts listed in Table 10-5 and the Teletype maintenance tools listed in Table 10-6.

FLIP CHIP Modules

All users should stock a minimum of one spare module of every type used in the PDP-7 system. A list of these modules is given in Table 10-7. When a marginal check or other troubleshooting procedure reveals a faulty module, that module should be withdrawn from the unit and the spare substituted in its place. The defective module should be returned to DEC for repair or replacement. Module repair service is offered by DEC at a very moderate cost.

Users who have adequate maintenance personnel and facilities may wish to repair defective modules, at least to the extent of replacing defective semiconductors; more extensive repairs are not recommended. Such users should stock the semiconductors and integrated circuits listed in Table 10-8 as a minimum. Experience with the system will show what other semiconductors could usefully be stocked.

Miscellaneous Parts

Table 10-9 contains a list of miscellaneous parts useful in the maintenance of the PDP-7.

TABLE 10-5 SPARE PARTS FOR PRINTER KEYBOARD-MODEL KSR 33

Quantity	Item	Part No.	Vendor*
1	Circuit board	181821	Teletype Corp.
2	Tape fee sprocket	183071	Teletype Corp.
2	Lever, universal	180086	Teletype Corp.
1	Fuse (3.2 amp)	120167	Teletype Corp.
2	Distributor brush	180979	Teletype Corp.
1	Dust cover	183067	Teletype Corp.
1	Dust cover spring	183068	Teletype Corp.
1	Power pack assembly	182134	Teletype Corp.
1	Belt gear	181420	Teletype Corp.

*All items are available from the Digital Equipment Corporation or from the Teletype Corporation.

TABLE 10-6 TELETYPE MAINTENANCE TOOLS

Quantity	Item*	Part No.
1	8 oz scale	110443
1	32 oz scale	110444
1	64 oz scale	82711
1	set of gauges	117781
1	offset screwdriver	94644
1	offset screwdriver	94645
1	8 crochet hook	151952
1	12 crochethook	151959
1	spring hook push	142555
1	spring hook pull	142554
1	screw holder	151384
1	handwheel adaptor	181465
1	handwheel	161430
1	contact adjustment tool	156170
1	gauge	180587

*All items available from Digital Equipment Corporation or Teletype Corporation.

TABLE 10-6 TELETYPE MAINTENANCE TOOLS (continued)

Quantity	Item*	Part No.
1	gauge	180588
1	bending tool	180993
1	gauge	183103
1	extractor	182697
1	tweezer	151392
1	tommy wrench	6617
1	tommy wrench	73404
1	key lever remover	151383

*All items available from Digital Equipment Corporation or Teletype Corporation.

TABLE 10-7 PDP-7 MODULE LIST

Type	Name
B104	Inverter
B105	Inverter
B113	Diode Gate (2-input negative NAND)
B115	Diode Gate (3-input negative NAND)
B117	Diode Gate (6-input negative NAND)
B124	Inverter
B171	Diode Gate (6-input negative NAND for DS)
B201	Flip-Flop
B204	Four Flip-Flops
B210	PDP-7 Accumulator
B360	Delay with Pulse Amplifier
B602	10 MC Pulse Amplifier
B620	Carry Pulse Indicator
B684	Two Bus Drivers
G001	DC Sense Amplifier
G002	Master Slice Control
G201	Inhibit Driver
G202	Memory Selector
G601	Memory Selector Matrix
G602	Memory Selector Matrix

TABLE 10-7 PDP-7 MODULE LIST (continued)

Type	Name
G800	Control for 739 Power Supply
R002	Diode Network
R107	Inverter
R111	Diode Gate (2-input negative NAND)
R141	Diode Gate (7 two-input negative AND gate NOR combined)
R201	Flip-Flop
R202	Dual Flip-Flop
R203	Triple Flip-Flop
R302	Delay (one-shot or monostable multivibrator)
R601	Pulse Amplifier
R602	Pulse Amplifier
R603	Pulse Amplifier
R650	Bus Driver
W005	Clamped Load Resistors
W020	Indicator Cable Connector
W021	Signal Cable Connector
W040	Solenoid Driver
W501	Schmitt Trigger
W505	Low Voltage Detector
W607	Pulse Amplifier
W640	Pulse Amplifier
1404	Variable Clock
4225	Eight-Bit BCD or Binary Counter
4303	Integrating One-Shot
4407	Crystal Clock
4706	Eight-Bit Teletype Receiver
4707	Eight-Bit Teletype Transmitter
728	Power Supply (+10 and -15)
738	Power Supply (0-20 marginal check supply)
739	Power Supply
778	Dual 15-V Power Supply
779	Power Supply (one 10v and three 15v floating supplies)
832	Two-Step Power Control

TABLE 10-8 SUGGESTED SPARE SEMICONDUCTORS*

FLIP CHIP Series	Transistors	Diodes
A Series Modules	C1-106	D-007
	DEC999	D-662
	2N1304	D-664
	2N1305	
	2N1305B	
	2N1305W	
	DEC2219	
	DEC2894-1	
	DEC2894-3	
	DEC3009	
	NS-3033-3	
	NS-3033-5	
	NS-3033-9	
	2N3608	
	2N456A	
B Series Modules	SDA-8	D-662
	16J1	D-664
	DEC2894-1	D-668
	DEC2894-3	1N750A
	2N2904	6.8AZ5
	2N3009	
R Series Modules	DEC2894-1	D-662
	DEC2894-3	D-664
	DEC3009	1N74B
	DEC3639	
W Series Modules	16J1	D-003
	2N398A	D-007
	2N1184B	D-662
	DEC1305	D-664
	DEC2894-1	D-668
	DEC2894-3	D-670
	DEC3009	1N1217
	2N3568	
	4JX1C741	

*A quantity of four of each transistor and diode is recommended until the user can determine quantities by ause-rate figure.

TABLE 10-8 SUGGESTED SPARE SEMICONDUCTORS* (continued)

FLIP CHIP Series	Transistors	Diodes
G Series Modules	SDA-6 SDA-8 DEC999 DEC1008 DEC2894-1 2N3110	D-662 D-664 D-670 1N429

*A quantity of four of each transistor and diode is recommended until the user can determine quantities by a use-rate figure.

Validation Test

Following the replacement of any electrical component of the equipment, a test should be performed to assure the correction of the fault condition and to make any adjustments of timing or signal levels affected by the replacement. This test should be taken from the preventive maintenance procedure most applicable to the portion of the system in which the error was found. For example, if a filter capacitor is replaced in a section of the 728 Power Supply, the ripple check for that section should be repeated as specified under Power Supply Checks. If repairs or replacements are made in an area which is not checked during preventive maintenance, the appropriate diagnostic program (Maindec) should be run or an appropriate operational test should be devised. For example, if a flip-flop is repaired or replaced, the register or control function performed by the flip-flop should be completely checked by manual setting and clearing, by improvised programmed exercise of the function, or by performance of the appropriate diagnostic program.

When time permits, it is suggested that the entire preventive maintenance task be performed as a validation test. The reasons for this are:

1. If one fault has been detected and corrected, other components may be marginal.

2. While the equipment is down and available, preventive maintenance can be performed and need not be scheduled again for four months (or the normal period).

Log Entry

Corrective maintenance activities are not completed until they are recorded in the maintenance log. Record all data indicating the symptoms given by the fault, the method of fault detection, the component at fault, and any comments which would be helpful in maintaining the equipment in the future.

CHAPTER 11

ENGINEERING DRAWINGS

This appendix contains reduced copies of DEC block schematics, circuit schematics, and other engineering drawings nceessary for understanding and maintaining this equipment. Only those drawings which are essential and are not available in the referenced pertinent documents are included. Should any discrepancy exist between the drawings in this chapter and those supplied with the equipment, assume that the latter drawings are correct. A complete listing of the drawings in this appendix is presented in the table of contents.

DRAWING NUMBERS

DEC engineering drawing numbers contain five groups of information, separated by hyphens. A drawing number such as BS-D-9999-1-5 consists of the following information reading from left to right: a 2- or 3-letter code specifying the type of drawing (BS); a 1-letter code specifying the original size of the drawing (D); the type number of the equipment (9999); the manufacturing series of the equipment (1); and the drawing number within a particular series (5). The drawing type codes are:

BS, block schematic or logic diagram
CL, cable list
FD, flow diagram
ML, module list
RS, replacement schematic
WD, wiring system

CIRCUIT SYMBOLS

The block schematics of DEC equipment are multipurpose drawings that combine signal flow, logical function, circuit type and physical location, wiring, and other pertinent information. Individual circuits are shown in block or semiblock form, using special symbols that define the circuit operation. These symbols are similar to those appearing in both the FLIP CHIP Modules Catalog and the System Modules Catalog but are often simplified. Figure A1-1 illustrates some of the symbols used in DEC engineering drawings.

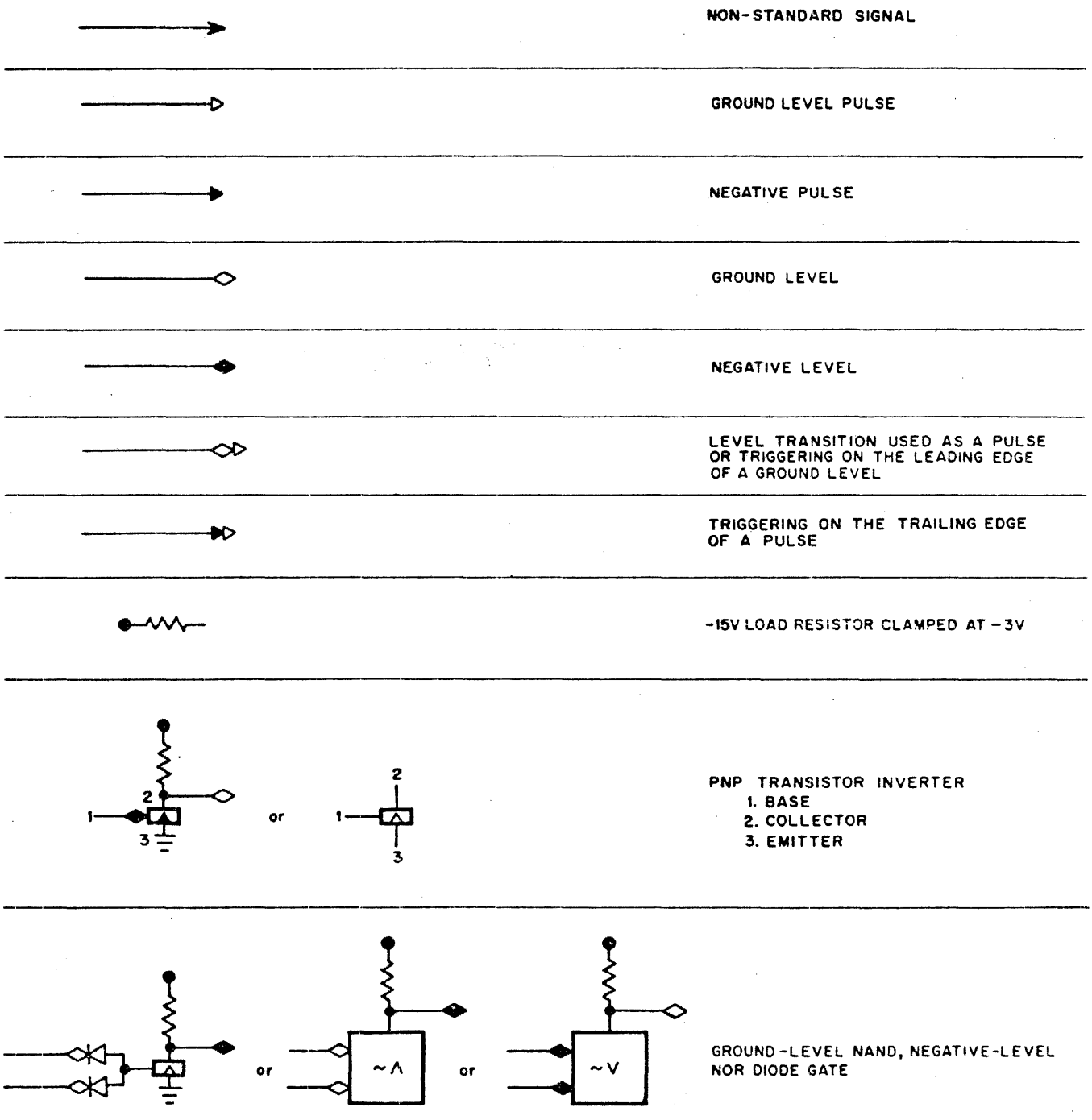
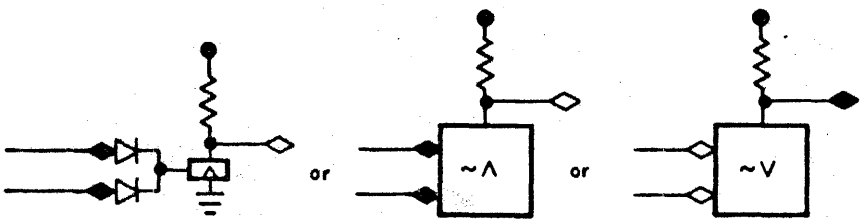
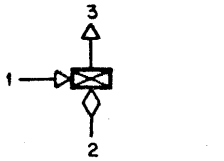


Figure 11-1 DEC Symbols



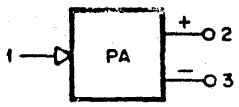
GROUND-LEVEL NOR, NEGATIVE-LEVEL NAND DIODE GATE



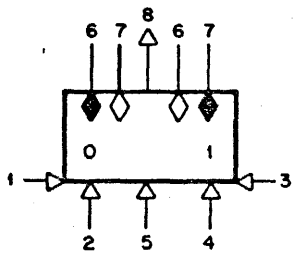
DIODE-CAPACITOR-DIODE GATE

1. PULSE INPUT
2. CONDITIONING LEVEL INPUT
3. PULSE OUTPUT

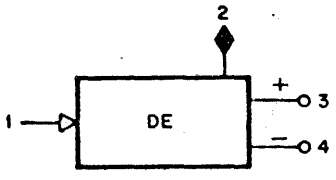
PULSE INVERTER



PULSE AMPLIFIER
1. PULSE INPUT, POLARITY INDICATED BY INPUT SIGNAL
2,3. TRANSFORMER-COUPLED PULSE OUTPUT. EITHER TERMINAL MAY BE GROUNDED



FLIP-FLOP (MOST FLIP-FLOPS HAVE ONLY SOME OF THE FOLLOWING):
1. DIRECT-CLEAR INPUT
2. GATED-CLEAR INPUT
3. DIRECT-SET INPUT
4. GATED-SET INPUT
5. COMPLEMENT INPUT
6. OUTPUT LEVEL, -3 V IF 0, 0 V IF 1
7. OUTPUT LEVEL, 0 V IF 0, -3 V IF 1
8. CARRY PULSE OUTPUT, UPON BEING CLEARED



DELAY (ONE-SHOT MULTIVIBRATOR)
1. INPUT PULSE
2. OUTPUT LEVEL, -3V DURING DELAY
3,4. TRANSFORMER-COUPLED PULSE OUTPUT. EITHER TERMINAL MAY BE GROUNDED

Figure 11-1 DEC Symbols (continued)

LOGIC SIGNAL SYMBOLS

DEC standard logic signal symbols are shown at the input of most circuits to specify the enabling conditions required to produce a desired output. These symbols represent either standard DEC logic levels, standard DEC pulses, standard FLIP CHIP pulses, or level transitions.

Logic Levels

The standard DEC logic level is either at ground (0 to −0.3v) or at −3v (−2.5 to −3.5v). Logic signals are generally given mnemonic names which indicate the condition represented by assertion of the signal. An open diamond (—◇) indicates that the signal is a DEC logic level and that ground represents assertion; a solid diamond (—◆) indicates that the signal is also a DEC logic level and that −3v represents assertion. All logic signals applied to the conditioning level inputs of capacitor-diode gates or diode-capacitor-diode gates must be present for a specified length of time (depending on the module used) before an input pulse will trigger operation of the gate.

Standard Pulses

DEC standard pulses are 2.5v in amplitude with reference to either ground or −3v, depending upon the type of module used. The width of standard pulses is either 40, 70, or 400 nsec as required for specific circuit configurations. The standard 2.5v negative pulse (−2.3 to −3.5v) is indicated by a solid triangle (—▶) and is always referenced with respect to ground, as shown in Figure A1-2.

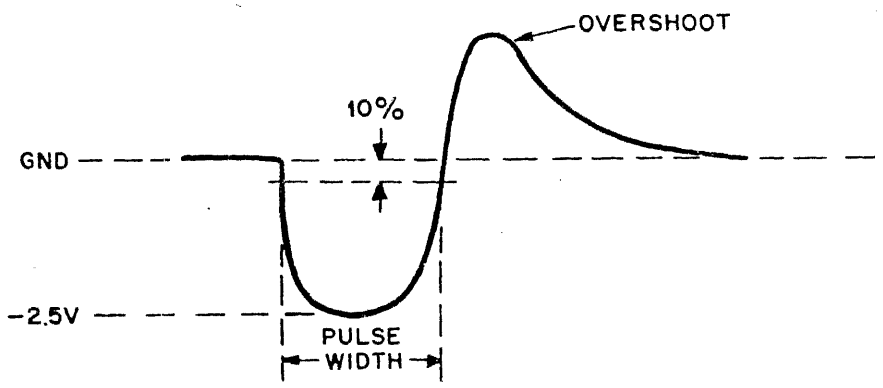


Figure 11-2 Standard Negative Pulse

The standard positive pulse is the inverse of the negative pulse and is indicated by an open triangle (——▷). The positive pulse goes either from – 3v to ground or goes from ground to +2.5v (+2.3 to +3.0v).

FLIP CHIP Standard Pulses

Two types of pulses, R series and B series, are utilized in FLIP CHIP circuit operation. The pulse produced by R-series modules starts at – 3v, goes to ground (– 0.2v) for 100 nsec, then returns to – 3v. This pulse is shown in Figure A1-3.

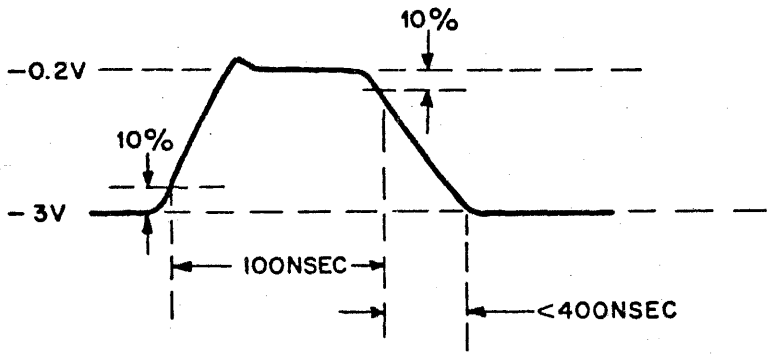


Figure 11-3 FLIP CHIP R-Series Pulse

The B-series negative pulse is 2.5v in amplitude and 40 nsec in duration and is similar to the one shown in Figure A1-2. If this pulse is applied to the base of an inverter, the inverter output will be a narrow pulse, similar in shape to the R-series standard pulse. The B-series positive pulse, which goes from ground to +2.5v, is the inverse of the B-series negative pulse.

Level Transitions

Occasionally, the transition of a level is used at an input where a standard pulse is otherwise expected and a composite symbol (——◆▷) is drawn to indicate this fact. The triangle is drawn open or solid depending respectively on whether the positive (– 3v to ground) or the negative (ground to – 3v) transition triggers circuit action. The shading of the diamond either is the same as that of the triangle to indicate triggering on the leading edge of a level, or is opposite that of the triangle to indicate triggering on the trailing edge. Nonstandard signals (power supply outputs, calibration reference levels, etc.) are indicated by an arrowhead (——▶) pointing in the direction of signal flow.

COORDINATE SYSTEM

Each engineering logic drawing is divided into 32 zones (4 horizontal and 8 vertical) by marginal map coordinates. Figure references in the text are usually followed by a letter and a digit specifying the zone in which the referenced circuit is located. Physical reference to a drawing area such as "lower left" or "upper center" may also be used.

MODULE IDENTIFICATION

Two designations appear in or near each circuit symbol or inside the dotted line surrounding multiple circuit symbols shown on engineering drawings. The upper designation consists of four characters which specify the module type. Modules are identified by this designation in the Digital System Modules Catalog while FLIP CHIP modules are described in the FLIP CHIP Modules Catalog. Modules not described in the catalogs are described in this manual or in other referenced pertinent documents.

The lower designation is the module location code. The leftmost character of this designation is a number indicating the cabinet in which the module is located. The next character is a letter indicating the mounting panel in which the module is located. The last character consists of one or two numbers specifying the module location within the mounting panel. As an example, the designation 1A22 indicates that this module is mounted in location 22 of mounting panel A in cabinet 1. Terminal J of this module is designated at 1A22J.

Module mounting panels which can accommodate more than one row of modules may be used in the construction of certain equipment. For this equipment, a letter is assigned to each row of modules within a mounting panel. When a particular device is contained within one cabinet, the number 1 may be omitted from the reference designations appearing on the associated drawings for that device.

Certain modules are indicated on engineering drawings by the normal 4-digit type number followed by the suffix R or by a number and R. These modules contain removable jumpers that connect certain output terminals to clamped load resistors. The suffix R indicates that all clamped load resistors on that particular module are used; and since replacement modules are shipped with all clamped load resistors connected, a new module can be substituted for the

old without any modifications. A suffix such as 2R indicates that the two clamped load resistors connected to output terminals designated by letters closest to the beginning of the alphabet are to remain connected. All remaining jumpers connecting clamped load resistors to output terminals are to be removed. As an example, the designation 1103-3R indicates that the jumpers associated with output terminals H, L, and P of a Type 1103 Inverter module are to remain connected, while the jumpers associated with output terminals T, W, and Z, are to be removed. The standard Type 1103 is thereby modified into a Type 1103-3R.

EXAMPLE

Figure A1-4 illustrates DEC symbols and nomenclature. The circuit shown is a Type 4303 Integrating Single Shot used to control the enabling time of several gates. The module is located in the twelfth position from the left (when viewed from the front or wiring side) of mounting panel B (the second row of modules from the top) in cabinet 1. The symbol marked DELAY is a monostable multivibrator with two complementary outputs, terminals U and W. The output at terminal U is connected to terminals 2D18F and 1B15M while the output at terminal W is connected to terminal 1D02F.

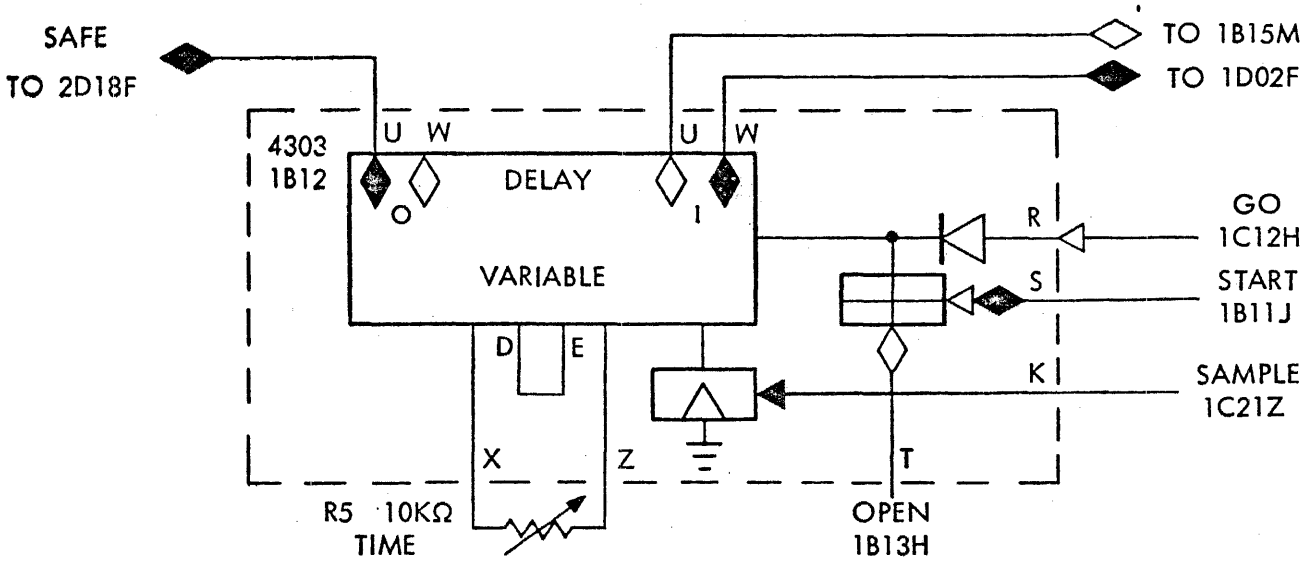
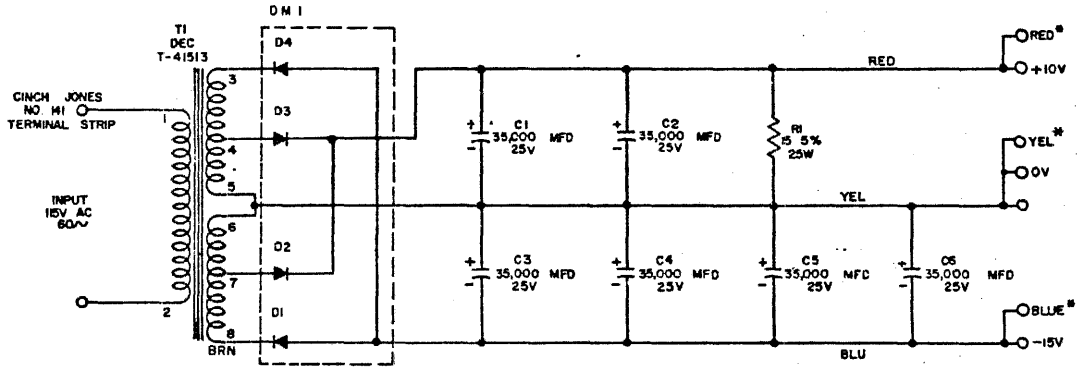


Figure 11-4 Typical DEC Logic Block Diagram



* HEYMAN MFG. CO.
TAB TERMINALS

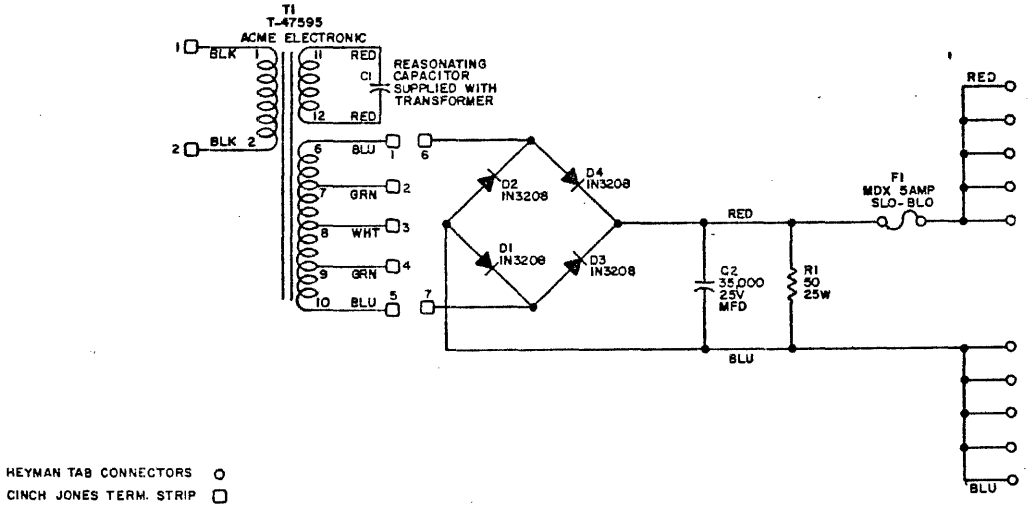
NOTE:
IN ORDER TO KEEP OUTPUT VOLTAGE WITHIN THE FOLLOWING LIMITS:
+10V: +9.5 TO +11V
-15V: -14.5 TO -16V
THE LOADING SHOULD BE WITHIN THE FOLLOWING LIMITS:

BOTH SIDES LOADED	+10 V	0	TO	7.0 AMPS
	-15 V	1.0	TO	8.0 AMPS
ONE SIDE LOADED	+10 V	0	TO	7.5 AMPS
	-15 V	1.0	TO	8.5 AMPS

SUM OF THE OUTPUT CURRENTS ARE LIMITED BY THE FOLLOWING EQUATION: $5I_{10} + 6I_{15} \leq 53$

TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
IN3208	IN3208		

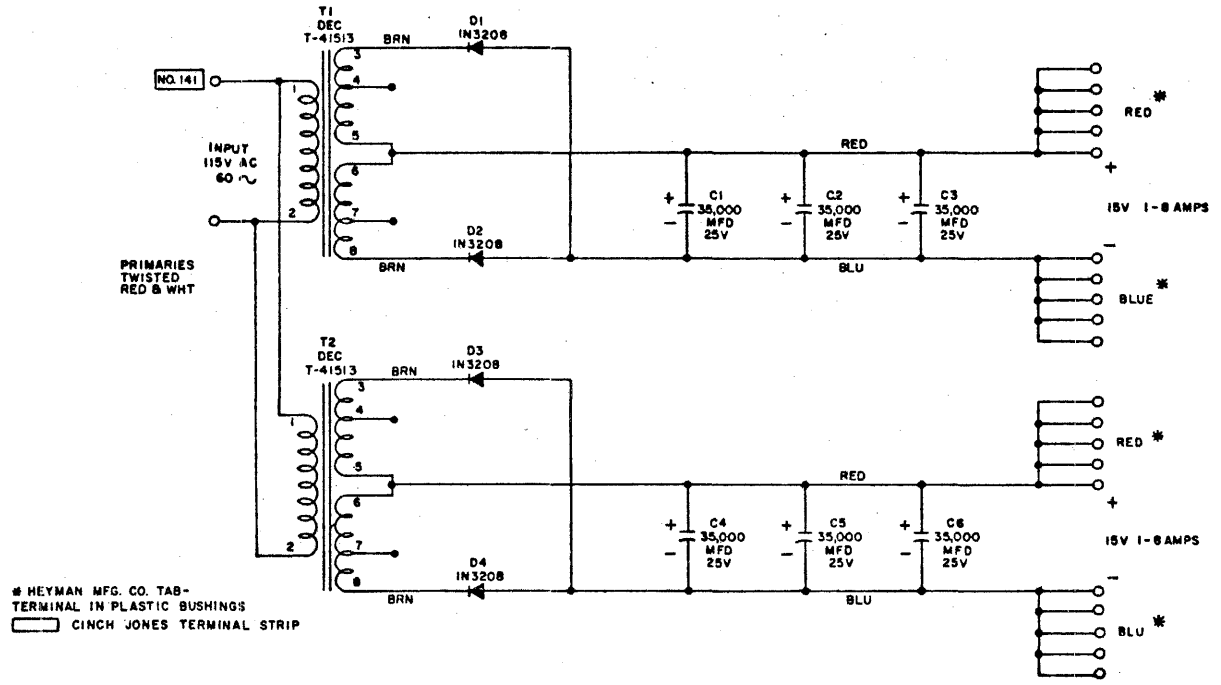
Power Supply (+10 and -15) RS-B-728



HEYMAN TAB CONNECTORS ○
CINCH JONES TERM. STRIP □

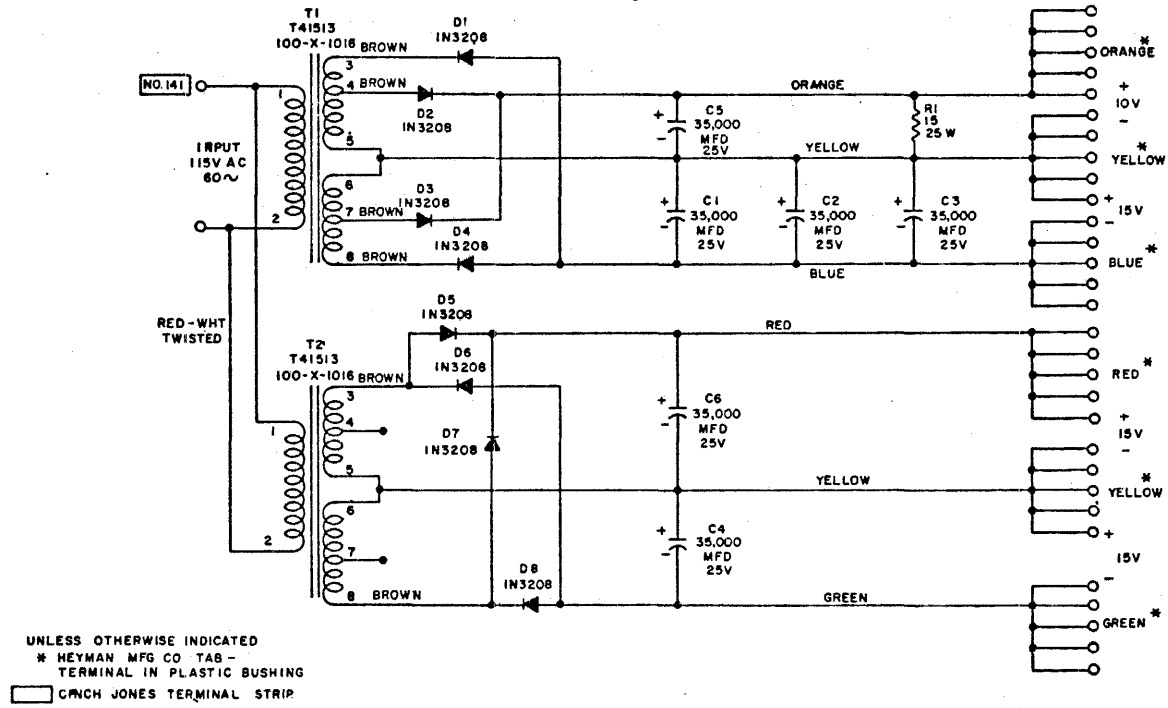
TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA

Power Supply (0-20 marginal check supply) RS-B-738



TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
IN3208	IN3208		

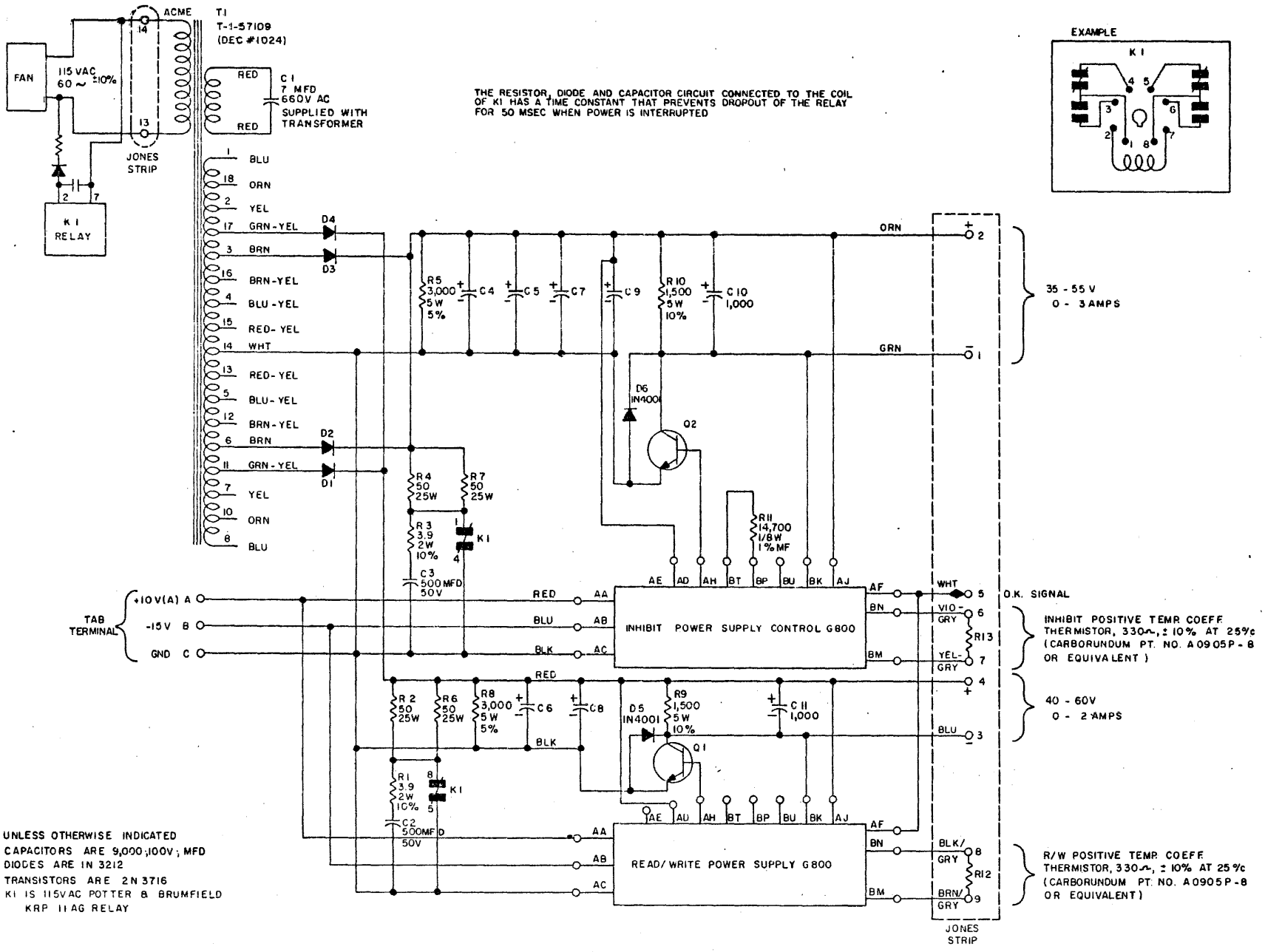
Dual 15-Volt Power Supply RS-B-778



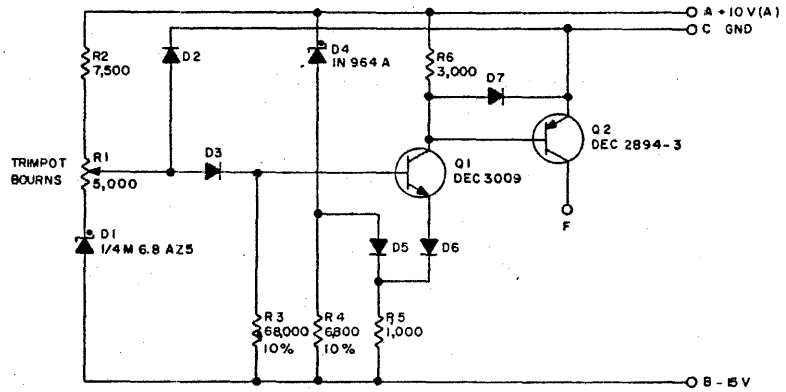
UNLESS OTHERWISE INDICATED
* HEYMAN MFG CO TAB-
TERMINAL IN PLASTIC BUSHING
CINCH JONES TERMINAL STRIP

TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
IN3209	IN3208		

Power Supply (one 10v and three 15v floating supplies) RS-B-779



Power Supply (Memory) RS-C-739

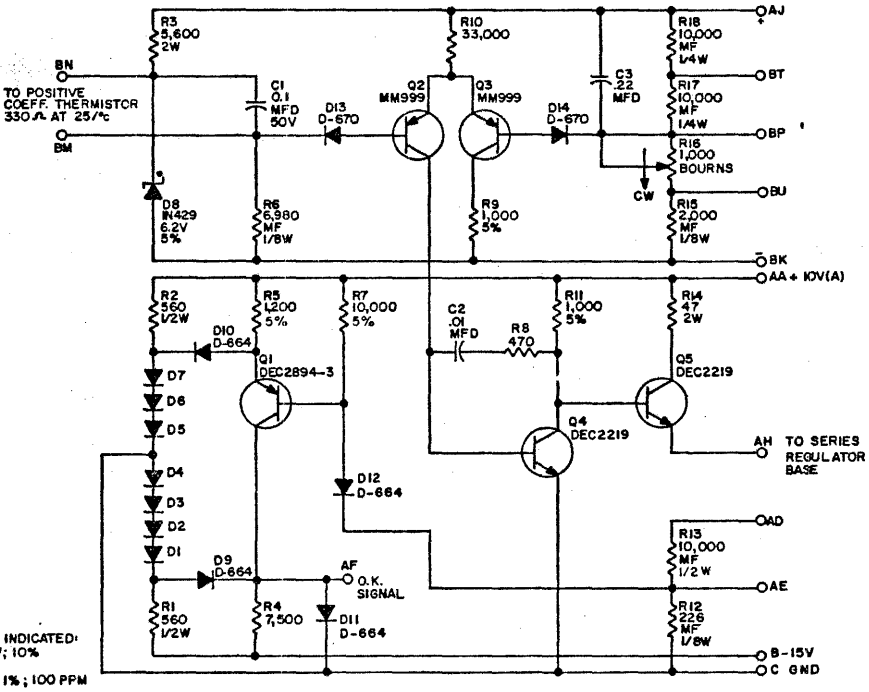


UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W, 5%
DIODES ARE D-664

TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
D 664	IN 3606		
IN 964 A	IN 964 A*		
1/4M 6.8 AZ 5	IN4099		
DEC 2894-3	DEC 2894		
DEC 3009	2N 3009		

NOTES
*13 V, 10%

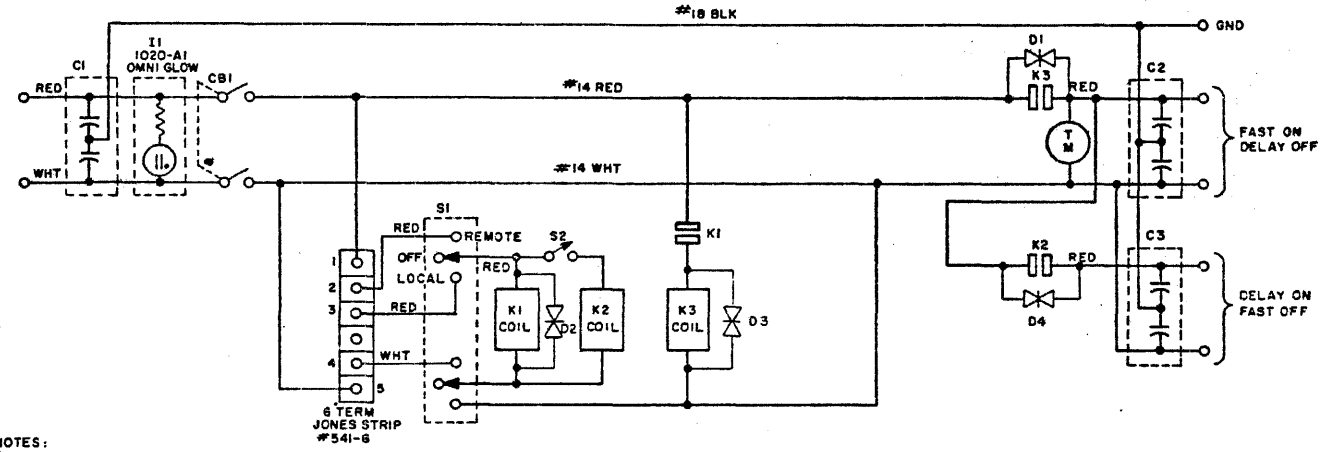
Low-Voltage Detector (for 739) RS-B-W505



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W; 10%
DIODES ARE D-662
MF RESISTORS ARE 1%; 100 PPM

TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
DEC2219	DEC2219	D-662	IN645
DEC2894-3	DEC2894	D-664	IN3606
		D-670	IN3653
MM999	DEC999	IN429	IN429 6.2V,5%

Control for 739 Power Supply RS-B-G800

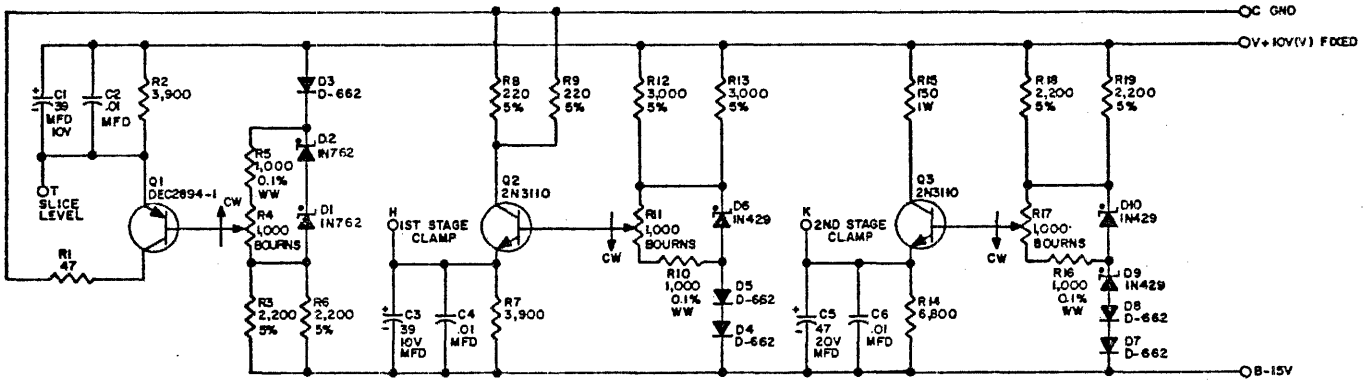


NOTES:

D1,D2,D3,D4 THYRECTOR GENERAL ELECTRIC 20SP 484,115V
C1 CAPACITOR 2 X.1 MFD 1000VDC #YAT 10011
CORNELL DUBLIER.
C2 & C3 CAPACITOR BATHTUB-DEC PURCH. SPEC #CAF-0001
2X.1MFD 600VDC CORNELL DUBLIER.
S1 TOGGLE SWITCH #ST52P.
S2 TOGGLE SWITCH SPDT 2 POS #7505-K3
K1 RELAY #1040-8-687 NORMALLY OPEN 115VAC COIL 3-5 SEC DELAY
QUICK OPERATE, SLOW RELEASE.
K2 RELAY #1040-8-58 NORMALLY OPEN 115 VAC COIL 3-5 SEC DELAY
SLOW OPERATE QUICK RELEASE.
K3 RELAY #EM-1 115 VAC EBERT ELECTRONICS.
CB1 CIRCUIT BREAKER #190-220-101 20AMPS 250V, 60 CYC-CURVE 4

TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA

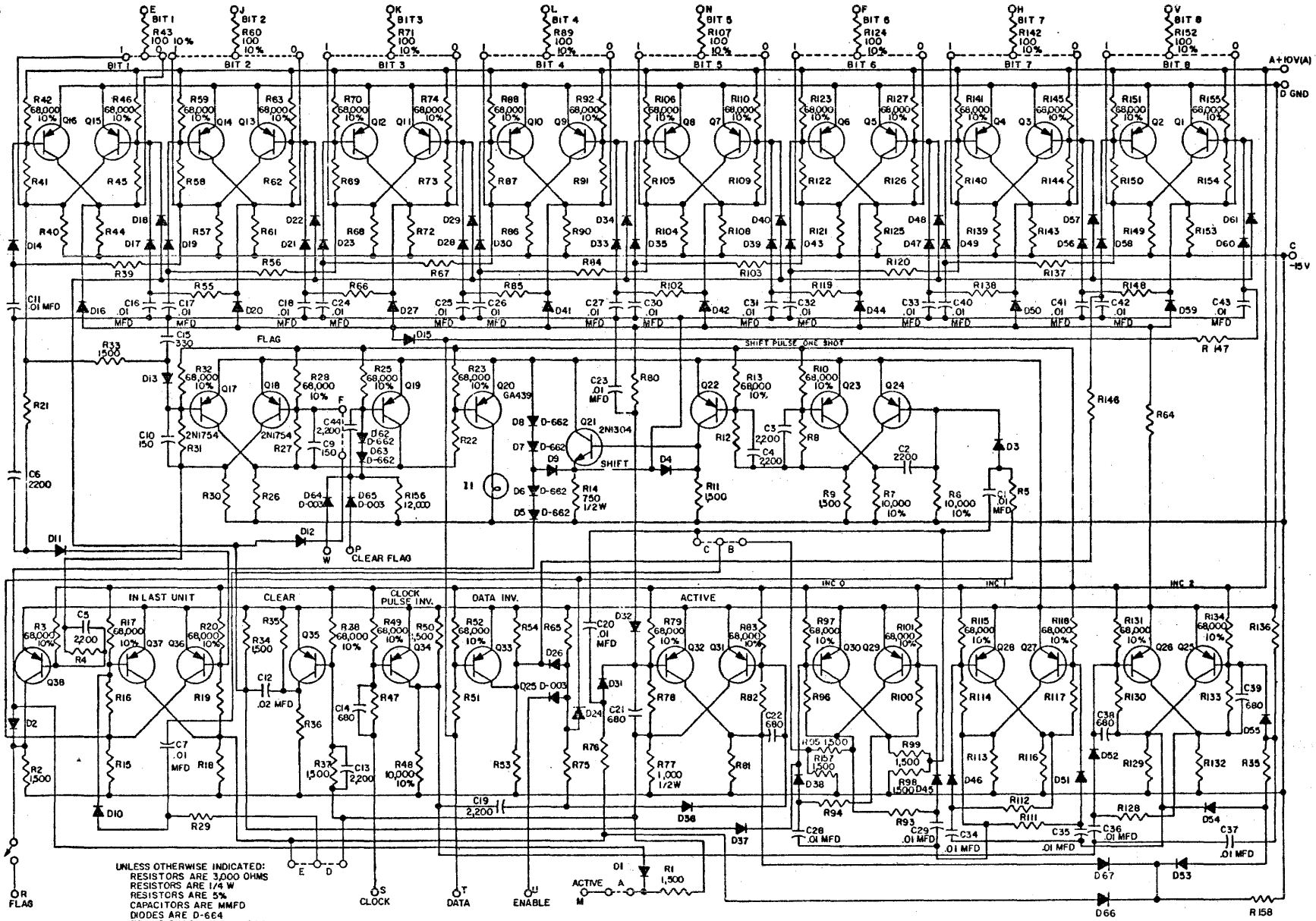
Two-Step Power Control RS-B-832



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W, 10%
R5, R10 & R16 ARE TEL-LAB

TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
DEC2894-1	DEC2894		
2N3110	2N3110		
D-662	IN645		
IN429	IN429 6.2V 5%		
IN762 *	IN762 *		

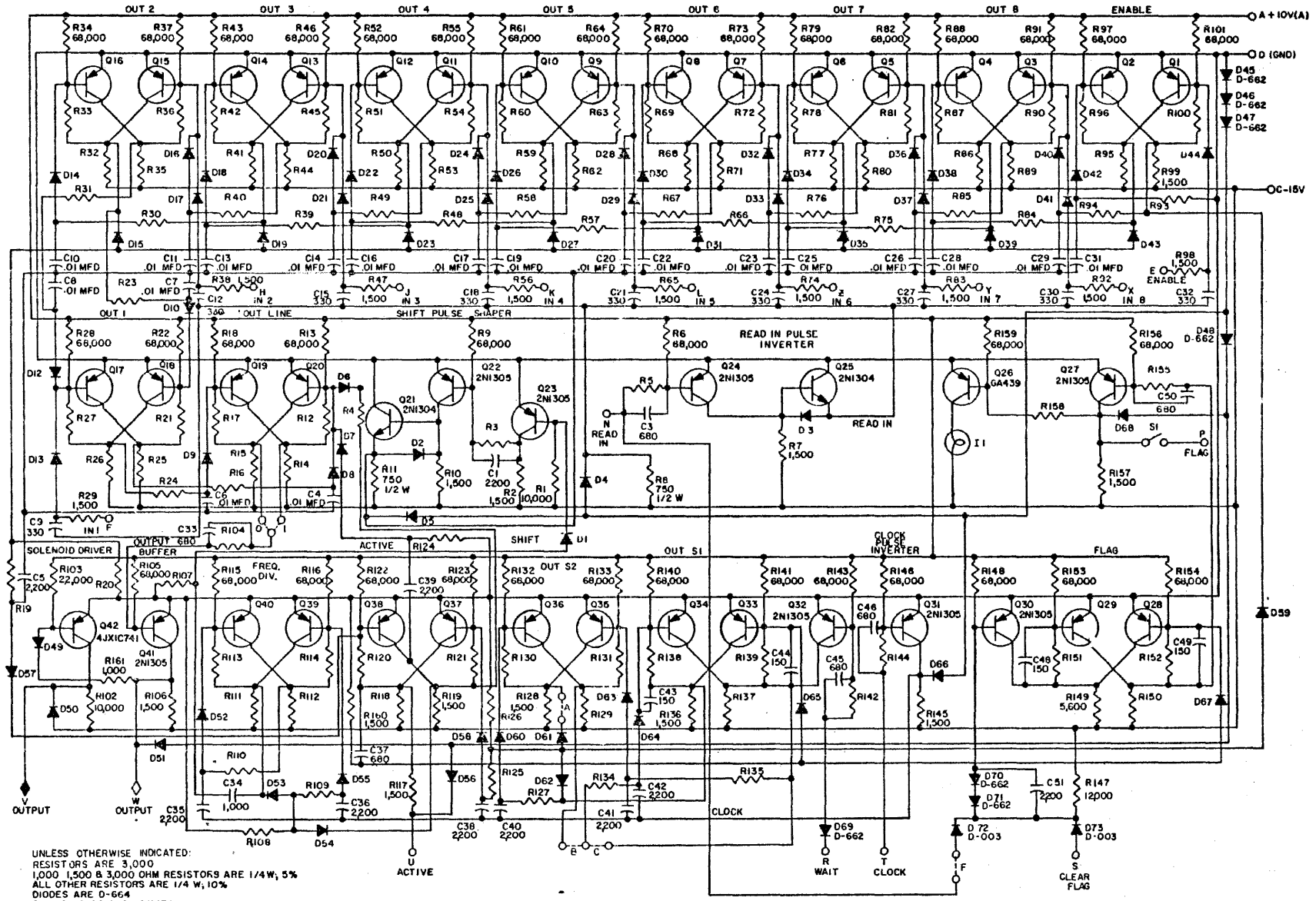
NOTES
* 5.5V 250 Ohm, 5%



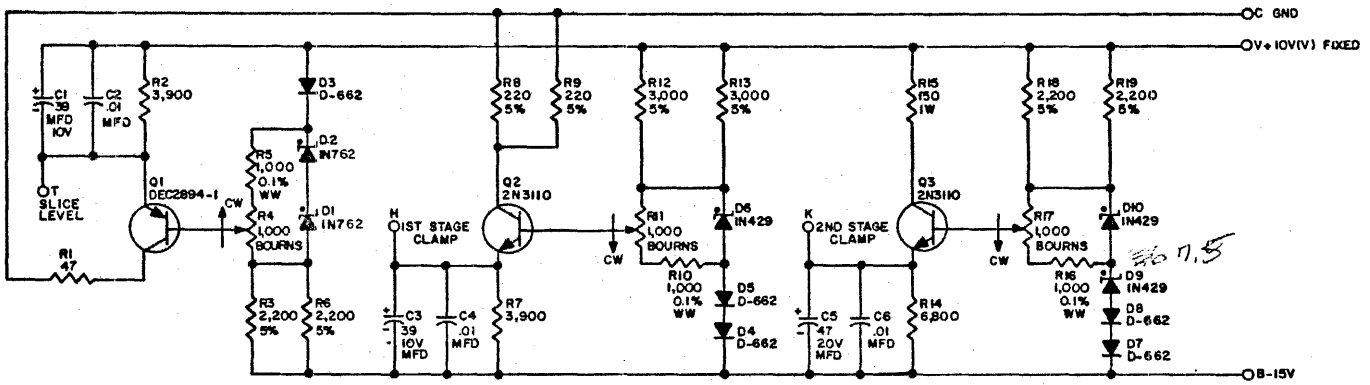
REF 83-4706

TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
2N1305	2N1305		
GA439	2N527		
D-003	IN914		
D-662	IN645		
D-664	IN3606		

Eight-Bit Teletype Receiver RS-C-4706



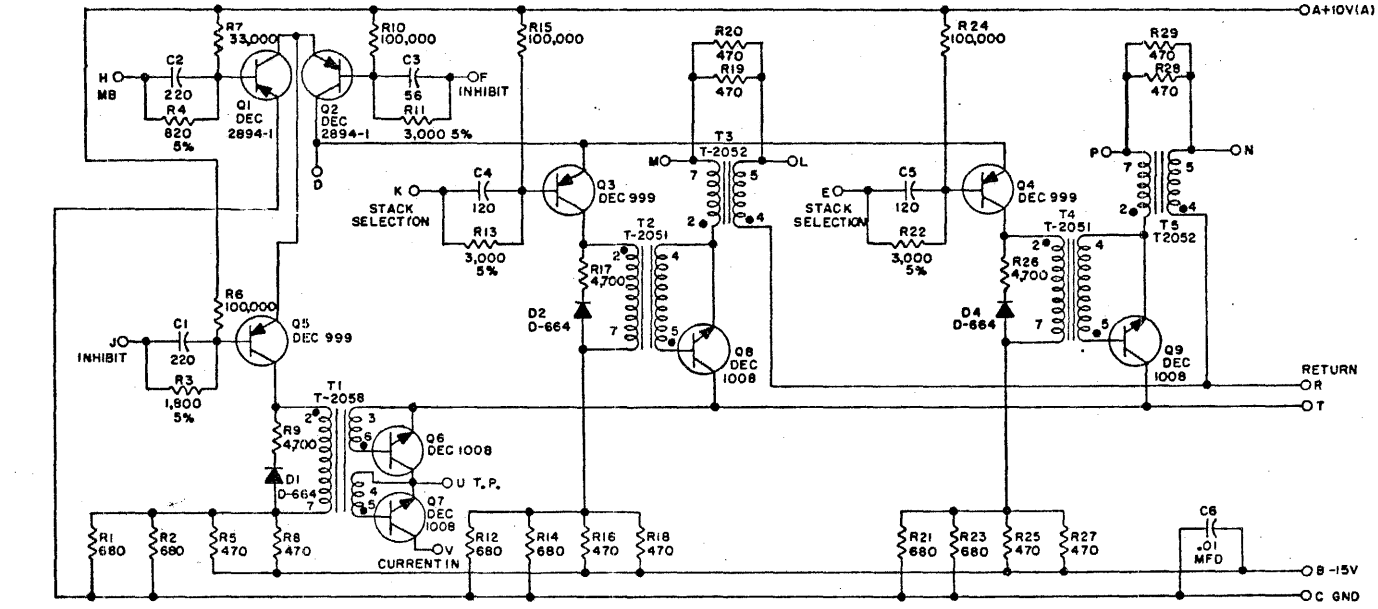
TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
2N1754	2N1754	D-664	IN3606
2N1304	2N1304	4JX1C741	2N527
2N1305	2N1305	D-003	IN994
GA439	2N527		
D-662	IN645		



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W;10%
R5, R10 & R16 ARE TEL-LAB

TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
DEC2894-1	DEC2894		
2N3110	2N3110		
D-662	IN645		
IN429	IN429 6.2V 5%		
IN762 *	IN762 *		

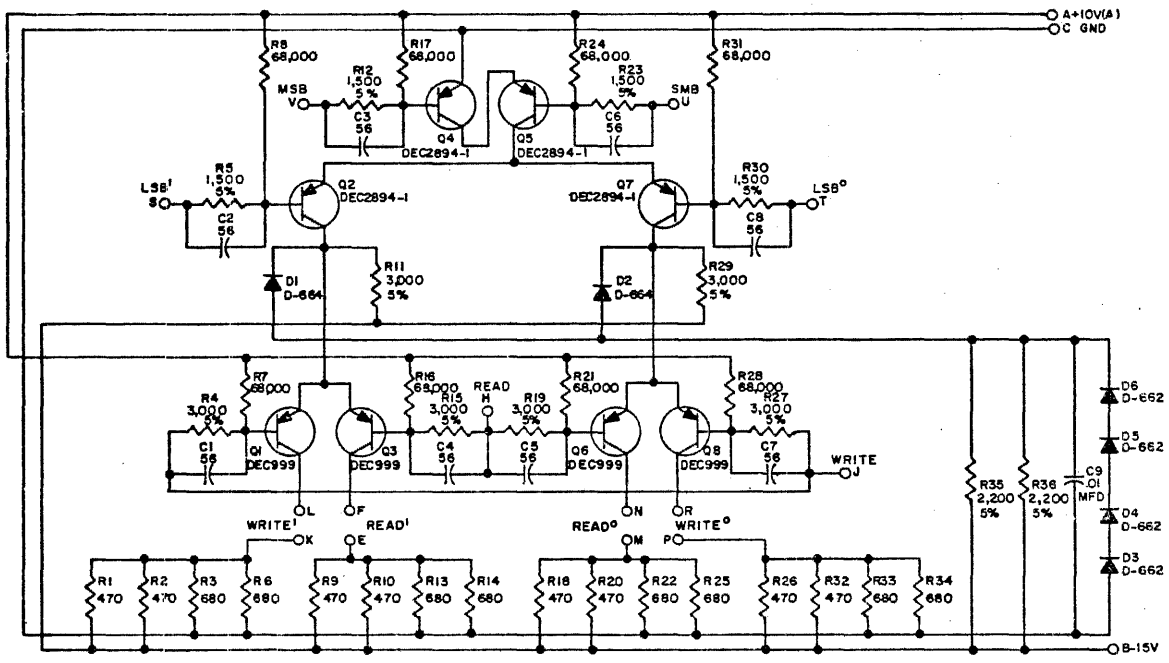
Master Slice Control RS-B-G002



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W; 10%
CAPACITORS ARE MMFD.

TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
DEC 2894-1	DEC2894		
DEC 1008	MM1008		
DEC 999	MM999		
D-664	IN3606		

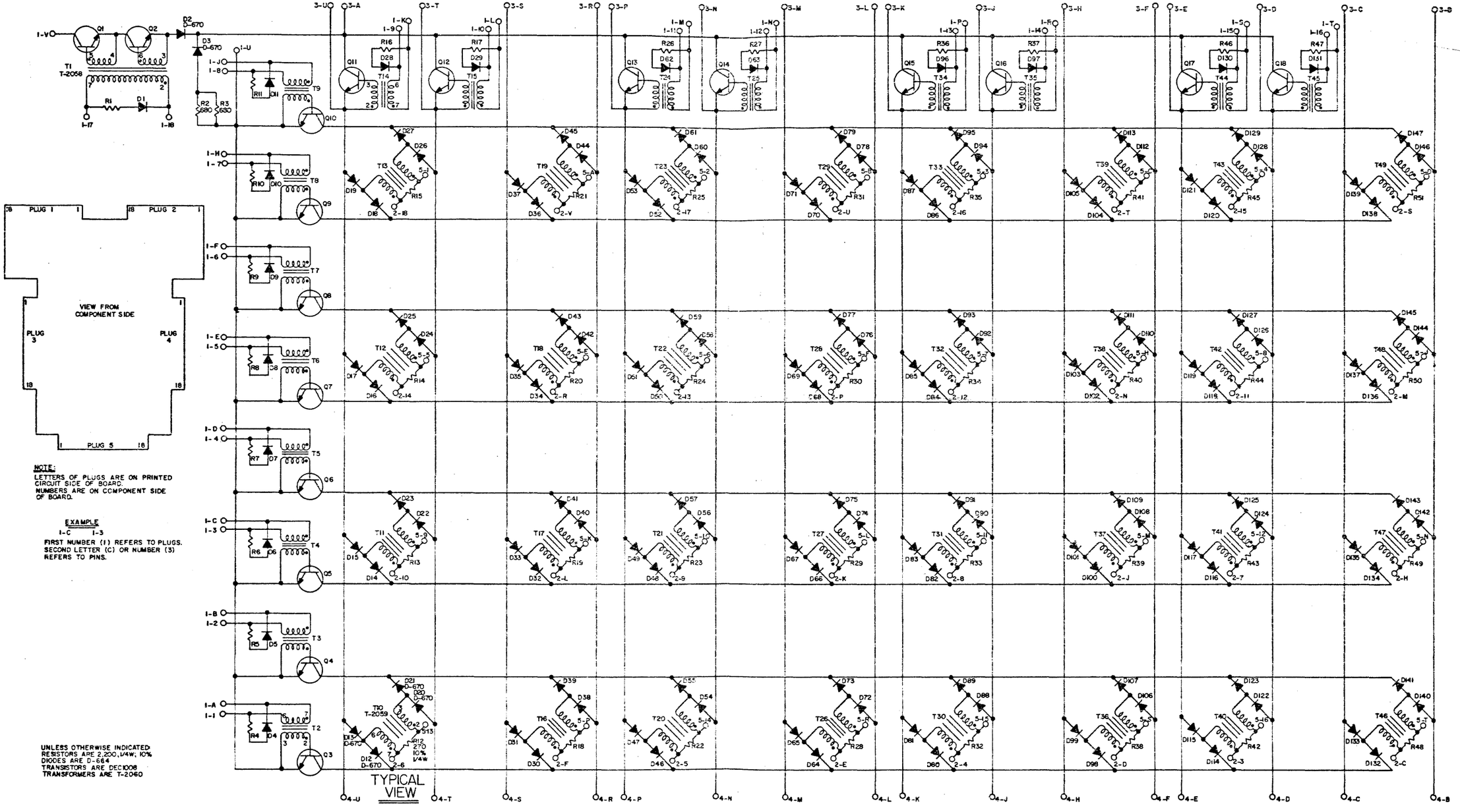
Inhibit Driver RS-B-G201



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W; 10%
CAPACITORS ARE MMFD

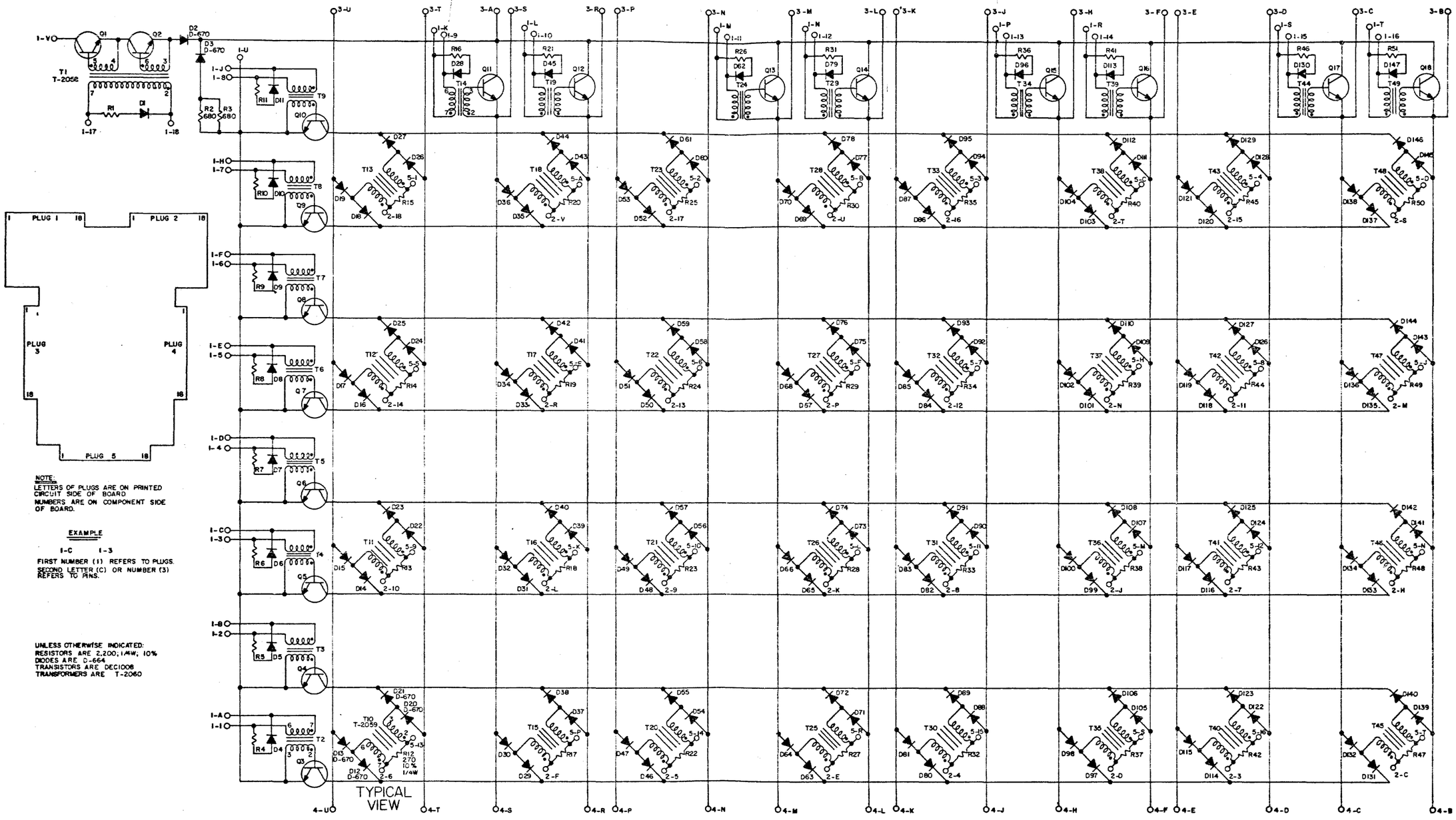
TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
DEC2894-1	DEC2894		
DEC999	DEC999		
D-662	1N645		
D-664	1N3606		

Memory Selector RS-B-G202



TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
DEC1008	MM1008		
D-664	IN914		
D-670	IN3633		

Memory Selector Matrix RS-D-G601



NOTE:
LETTERS OF PLUGS ARE ON PRINTED CIRCUIT SIDE OF BOARD
NUMBERS ARE ON COMPONENT SIDE OF BOARD.

EXAMPLE

1-C 1-3

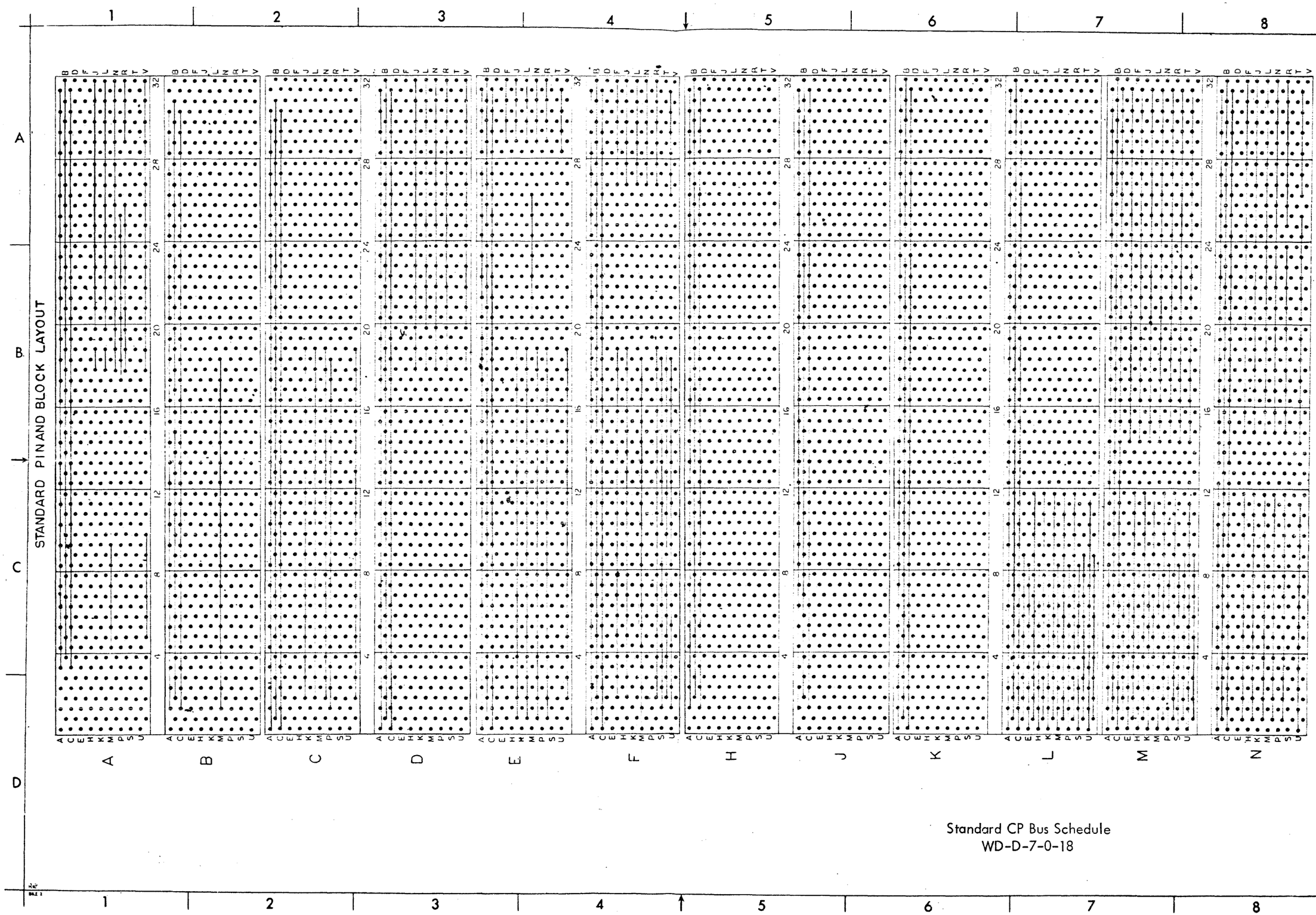
FIRST NUMBER (1) REFERS TO PLUGS.
SECOND LETTER (C) OR NUMBER (3) REFERS TO PINS.

UNLESS OTHERWISE INDICATED:
RESISTORS ARE 2,200; 1/4W; 10%
DIODES ARE D-664
TRANSISTORS ARE DEC1008
TRANSFORMERS ARE T-2060

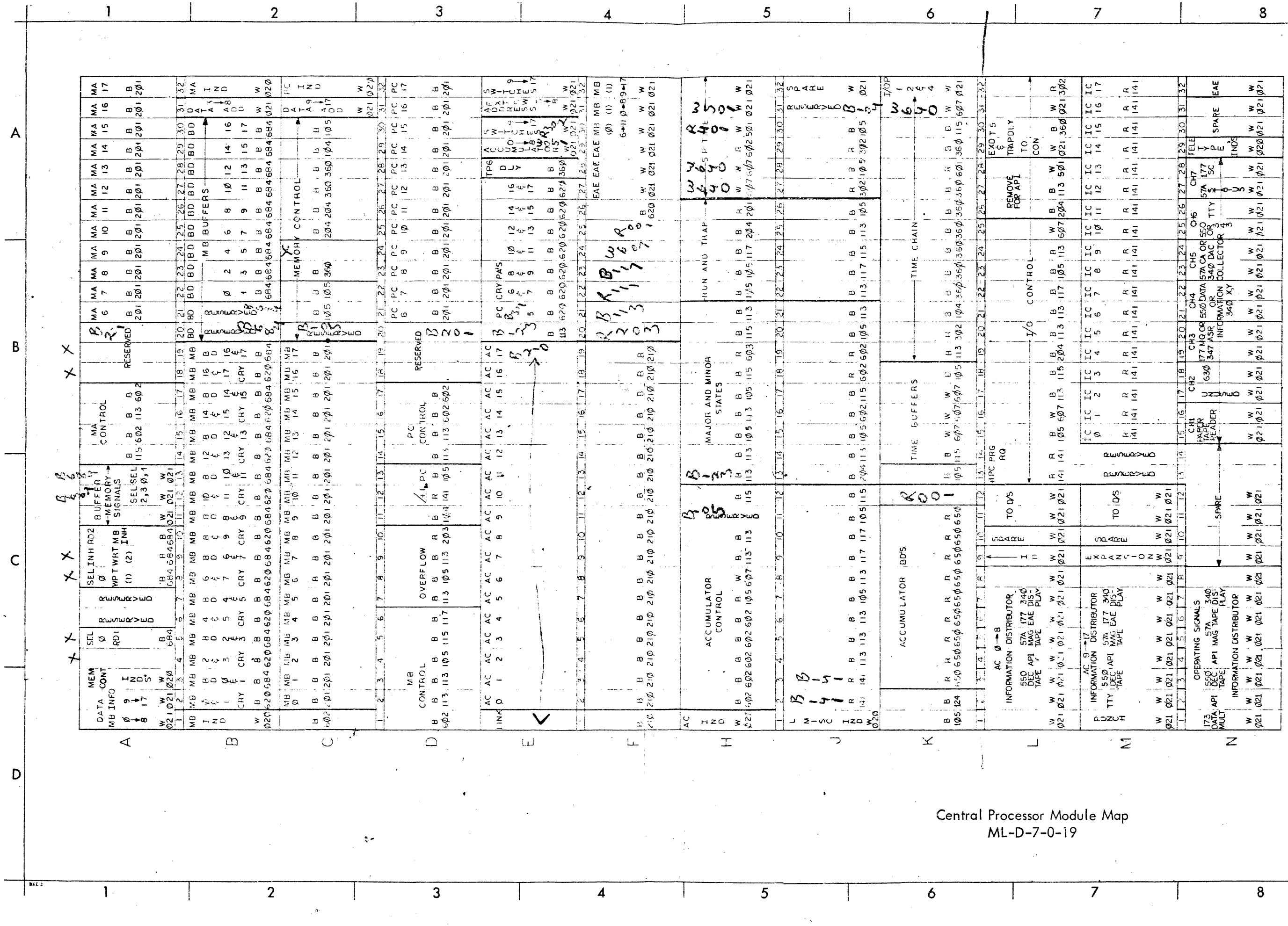
TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
DEC1008	MM1008		
D-664	1N3606		
D-670	1N3638		

Memory Selector Matrix RS-D-G602

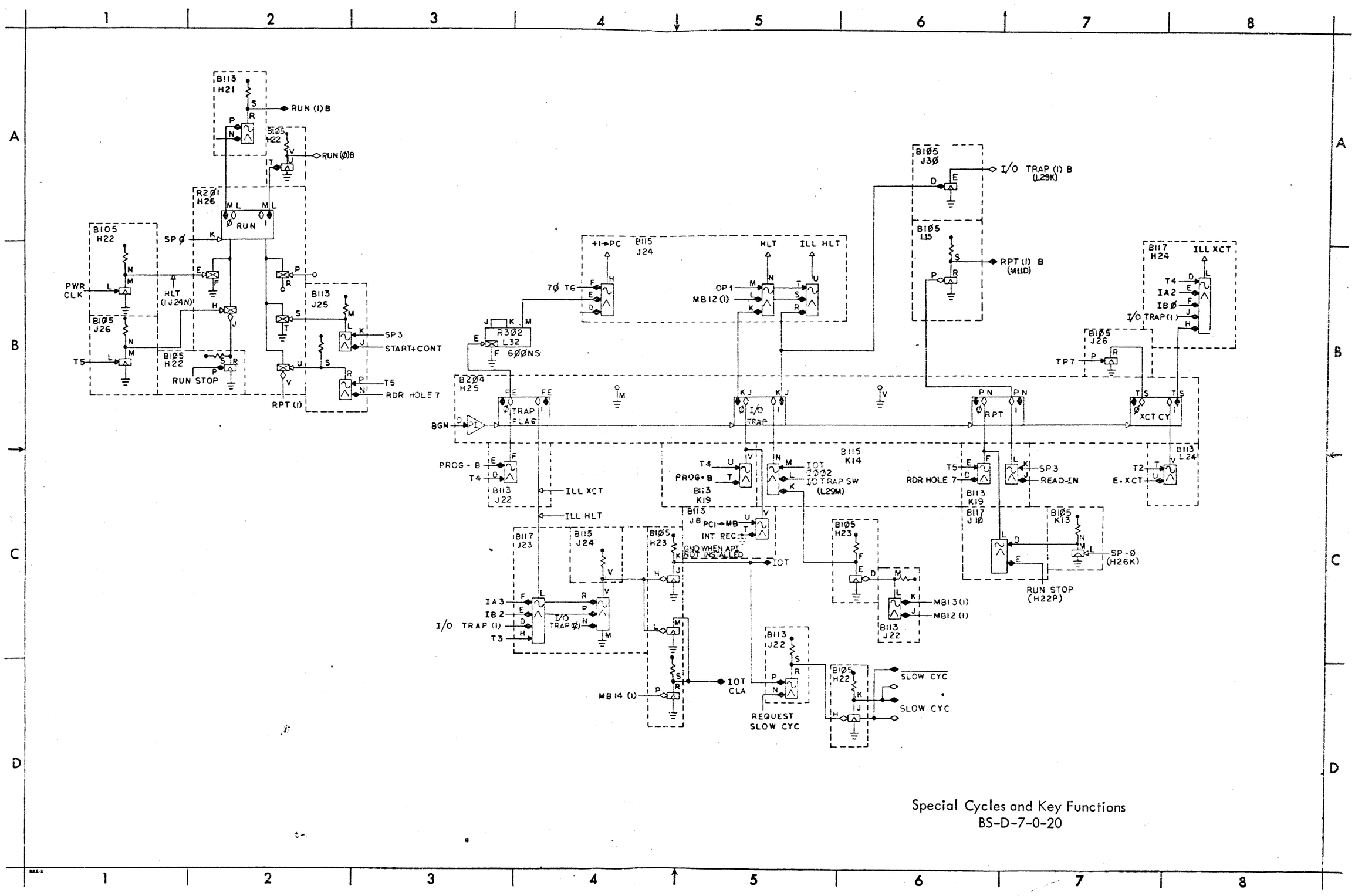
STANDARD PINAND BLOCK LAYOUT



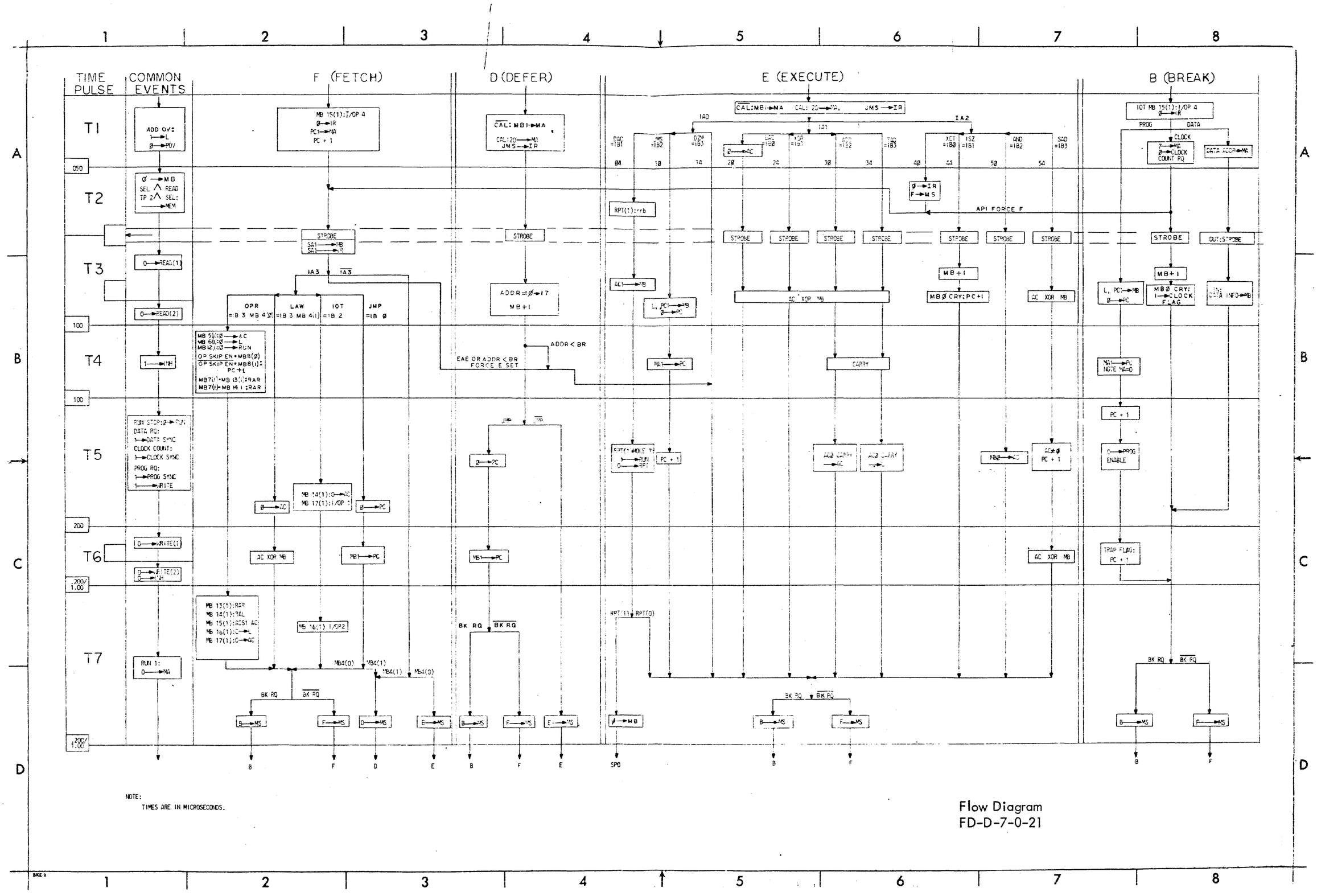
Standard CP Bus Schedule
WD-D-7-0-18



Central Processor Module Map
ML-D-7-0-19

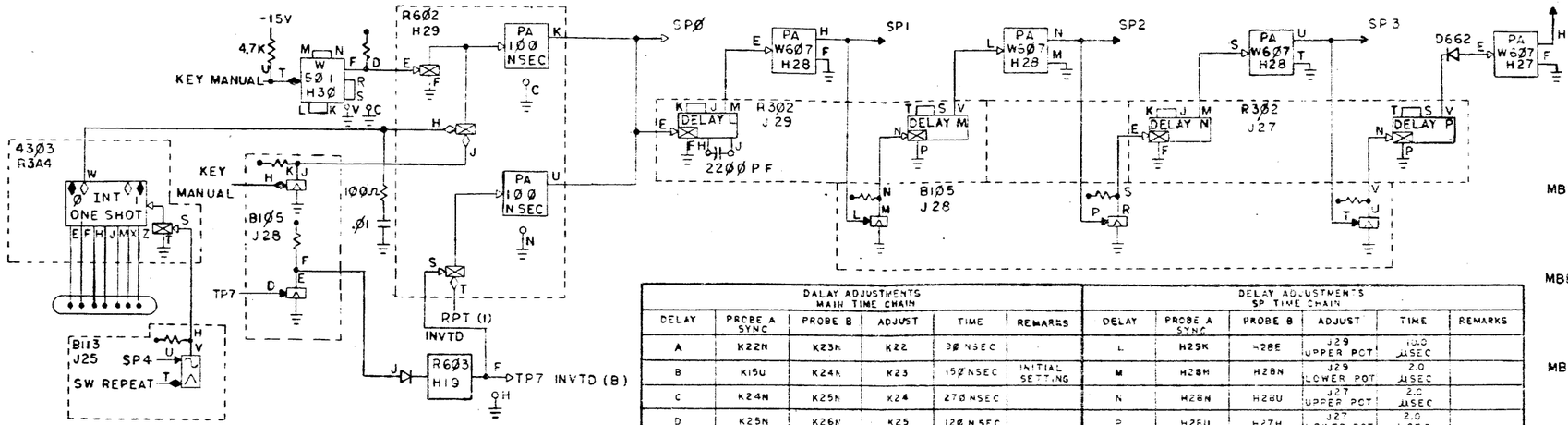


Special Cycles and Key Functions
BS-D-7-0-20

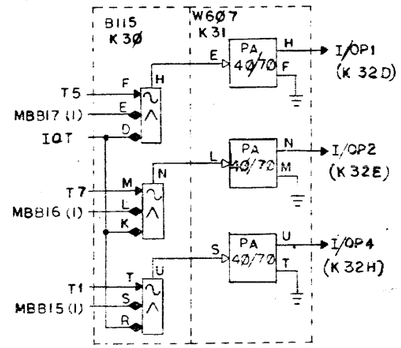


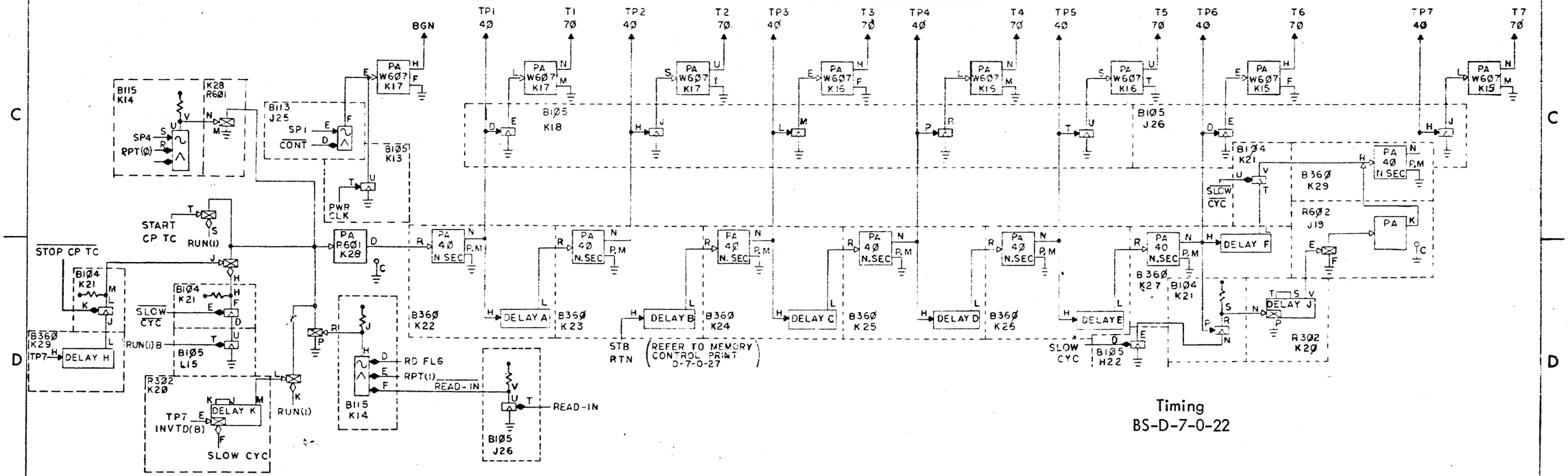
NOTE:
TIMES ARE IN MICROSECONDS.

Flow Diagram
FD-D-7-0-21

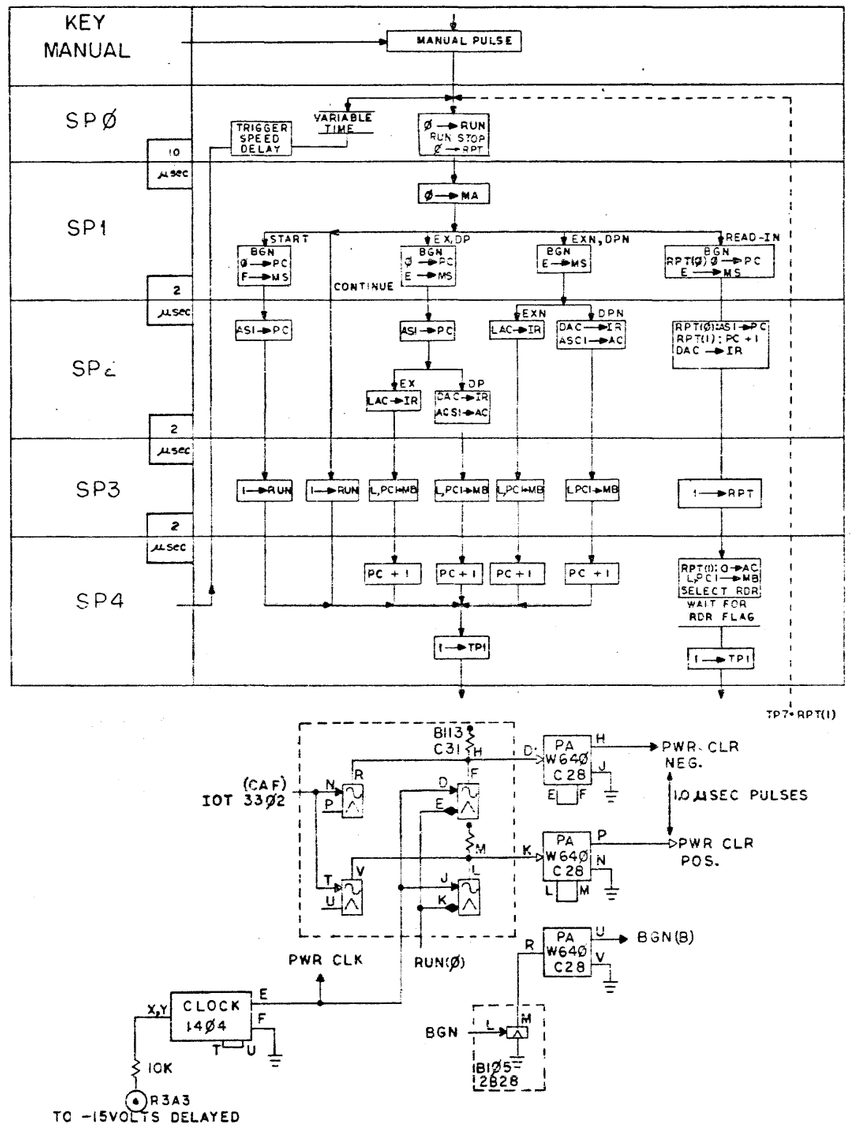


DALAY ADJUSTMENTS MAIN TIME CHAIN						DELAY ADJUSTMENTS SP TIME CHAIN					
DELAY	PROBE A SYNC	PROBE B	ADJUST	TIME	REMARKS	DELAY	PROBE A SYNC	PROBE B	ADJUST	TIME	REMARKS
A	K22N	K23N	K22	3Ø NSEC		L	H25K	H28E	J29 UPPER POT	10.0 μSEC	
B	K15U	K24N	K23	15Ø NSEC	INITIAL SETTING	M	H28H	H28N	J29 LOWER POT	2.0 μSEC	
C	K24N	K25N	K24	27Ø NSEC		N	H28N	H28U	J27 UPPER POT	2.0 μSEC	
D	K25N	K26N	K25	12Ø NSEC		P	H28U	H27H	J27 LOWER POT	2.0 μSEC	
E	K26N	K27N	K26	21Ø NSEC							
F	K27N	K29N	K27	24Ø NSEC							
H	K29N	K22N	K29	15Ø NSEC							
OVERALL	K22N	——	K23	1.75 μSEC	FINAL						
J	K27N	K29N	K2Ø LOWER POT	1.Ø μSEC							
K	K29N	K22N	K2Ø UPPER POT	1.Ø μSEC							
DELAYS J & K REQUIRE SLOW CYC REQUEST											

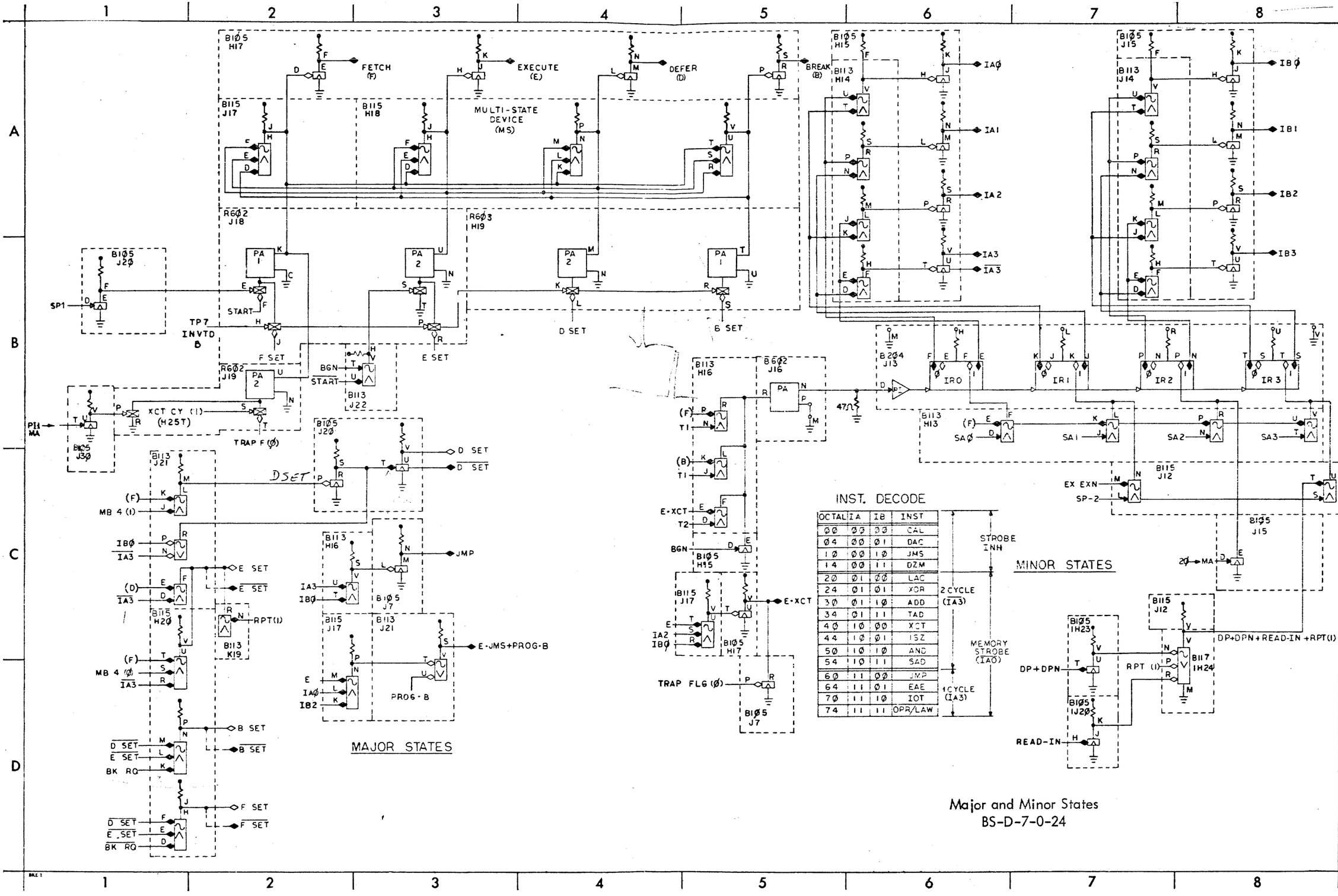




Timing
BS-D-7-0-22



Run and Special Modes
BS-D-7-0-23



OCTAL	IA	IB	INST
ØØ	ØØ	ØØ	CAL
Ø4	ØØ	Ø1	DAC
1Ø	ØØ	1Ø	JMS
14	ØØ	11	DZM
2Ø	Ø1	ØØ	LAC
24	Ø1	Ø1	XOR
3Ø	Ø1	1Ø	ADD
34	Ø1	11	TAD
4Ø	1Ø	ØØ	XCT
44	1Ø	Ø1	ISZ
5Ø	1Ø	1Ø	AND
54	1Ø	11	SAD
6Ø	11	ØØ	JMP
64	11	Ø1	EAE
7Ø	11	1Ø	IOT
74	11	11	OPR/LAW

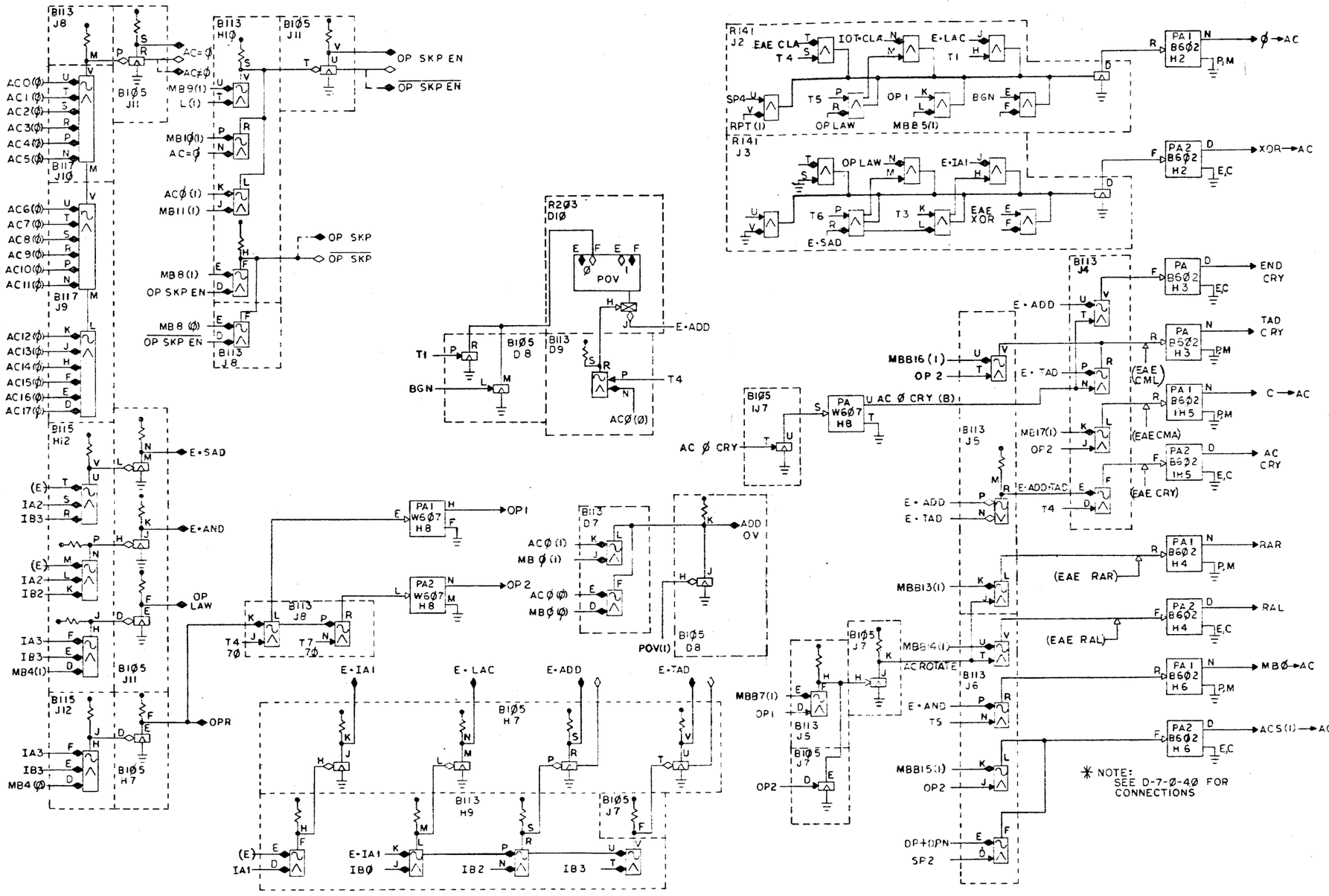
Major and Minor States
BS-D-7-0-24

MB CONTROL

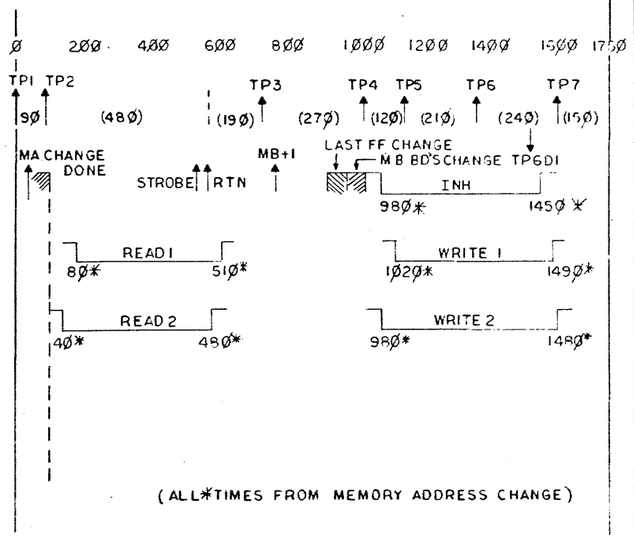
MA CONTROL

PC CONTROL

MA, MB, and PC Control
BS-D-7-0-25



AC Control and Link
BS-D-7-0-26



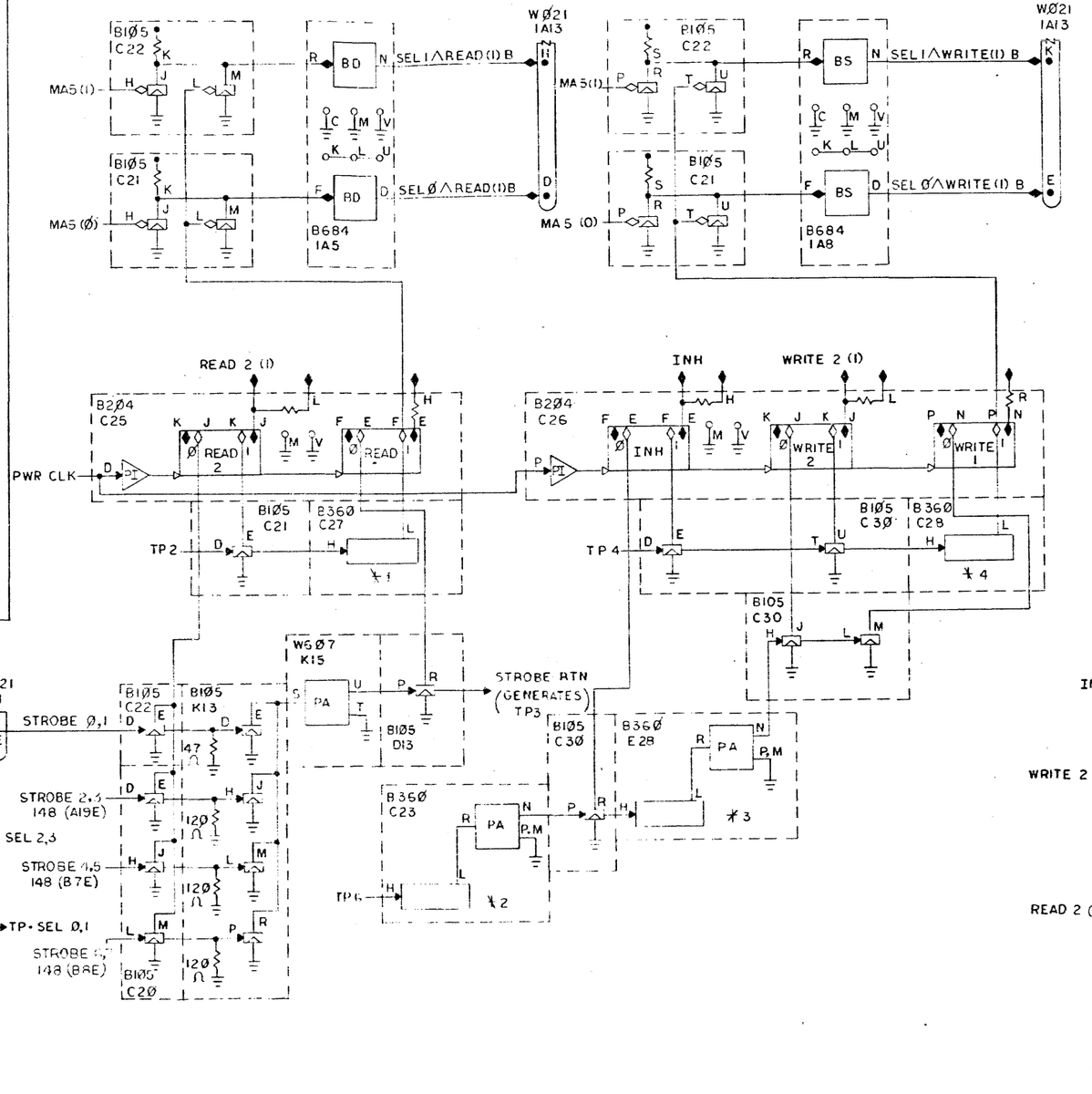
MEMORY CONTROL TIMING

* DELAY ADJUSTMENT (SYNC ON PROBE 1)

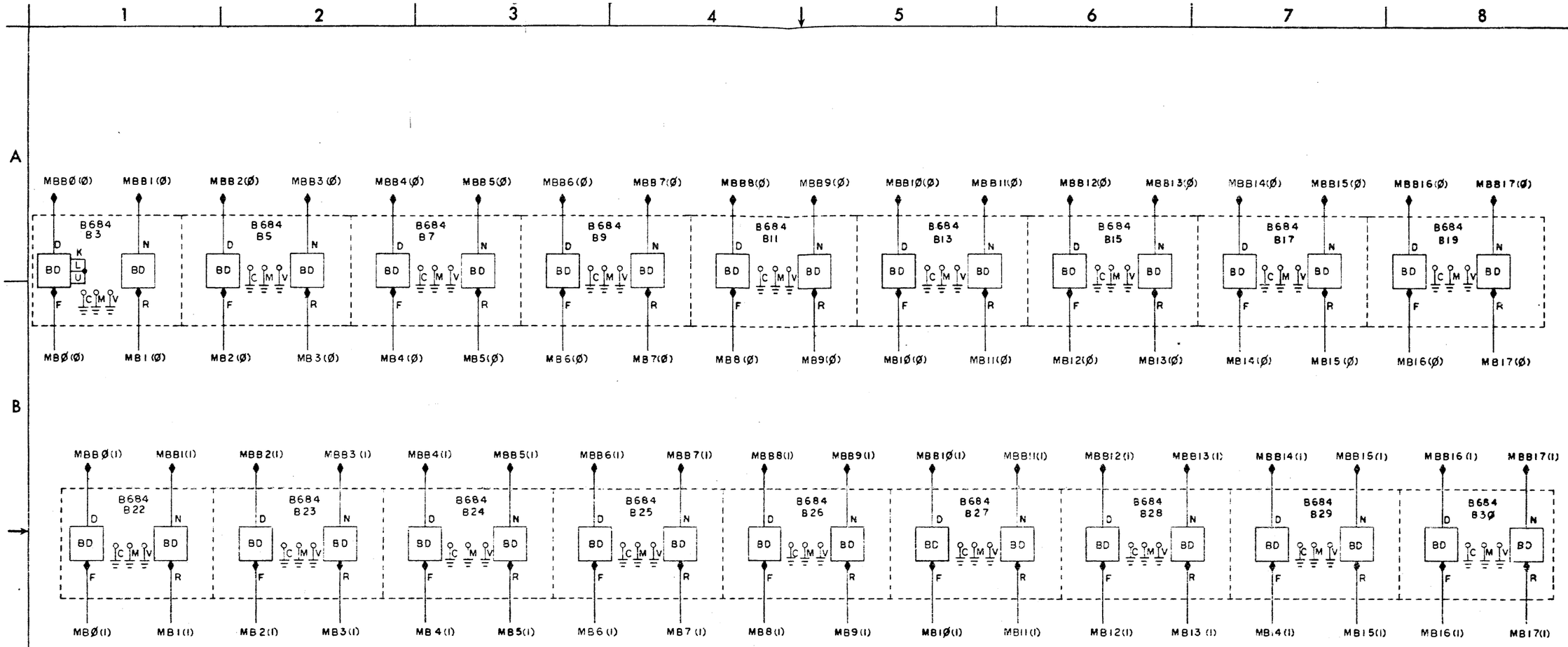
#	PROBE 1	PROBE 2	CONDITION
1	AI3S	AI3D	40 NS
2	C23H	AI3V	190 NS
3	C23N	E28N	30 NS
4	AI3T	AI3 E	40 NS

NOTE FOR AN 8K MEMORY

	MEM	CP
SEL Ø=MA5 (Ø) WIRE:	H22R - A2ØE	
SEL 1=MA5 (1) WIRE:	H21R - A2ØD	

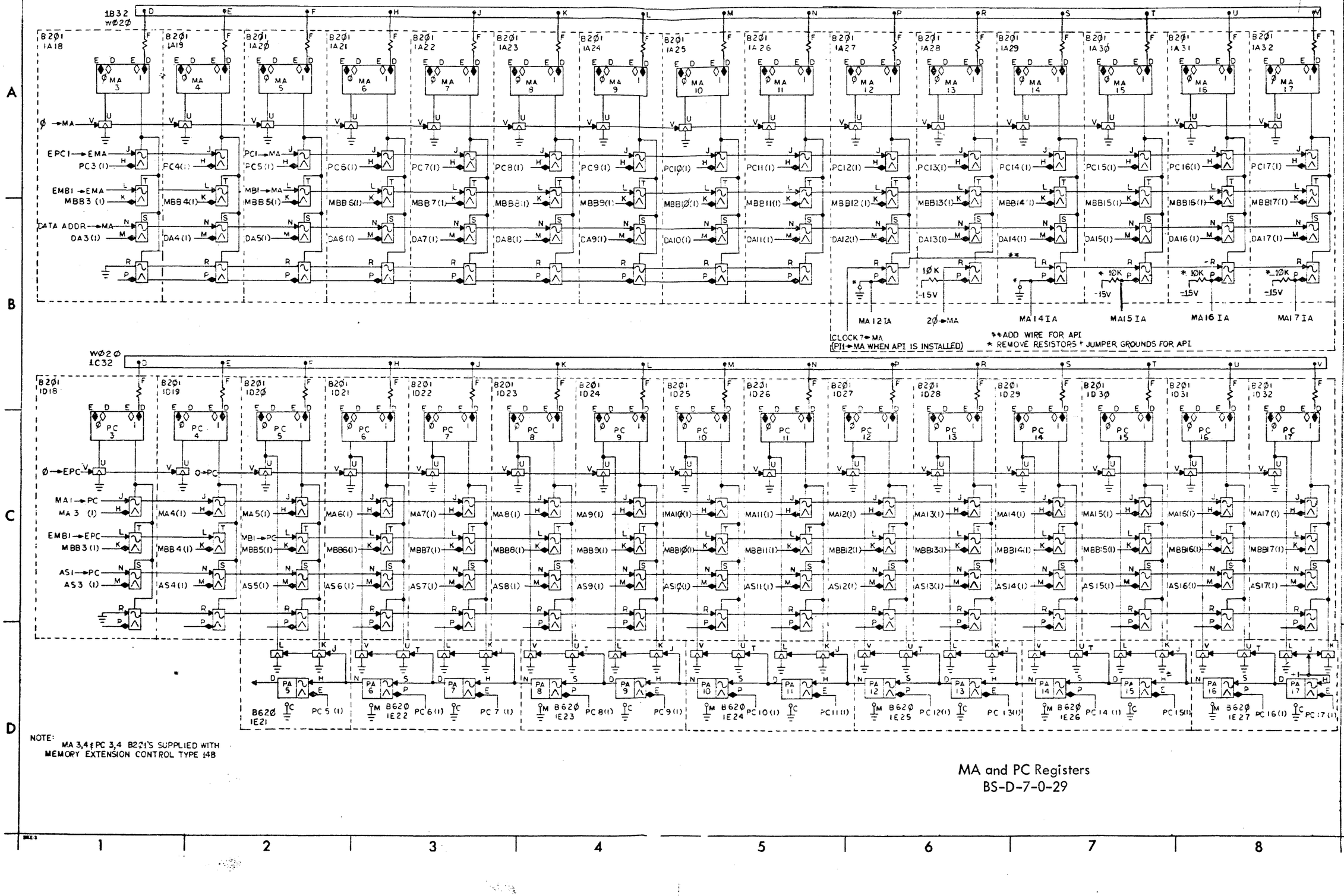


Memory Control
BS-D-7-0-27



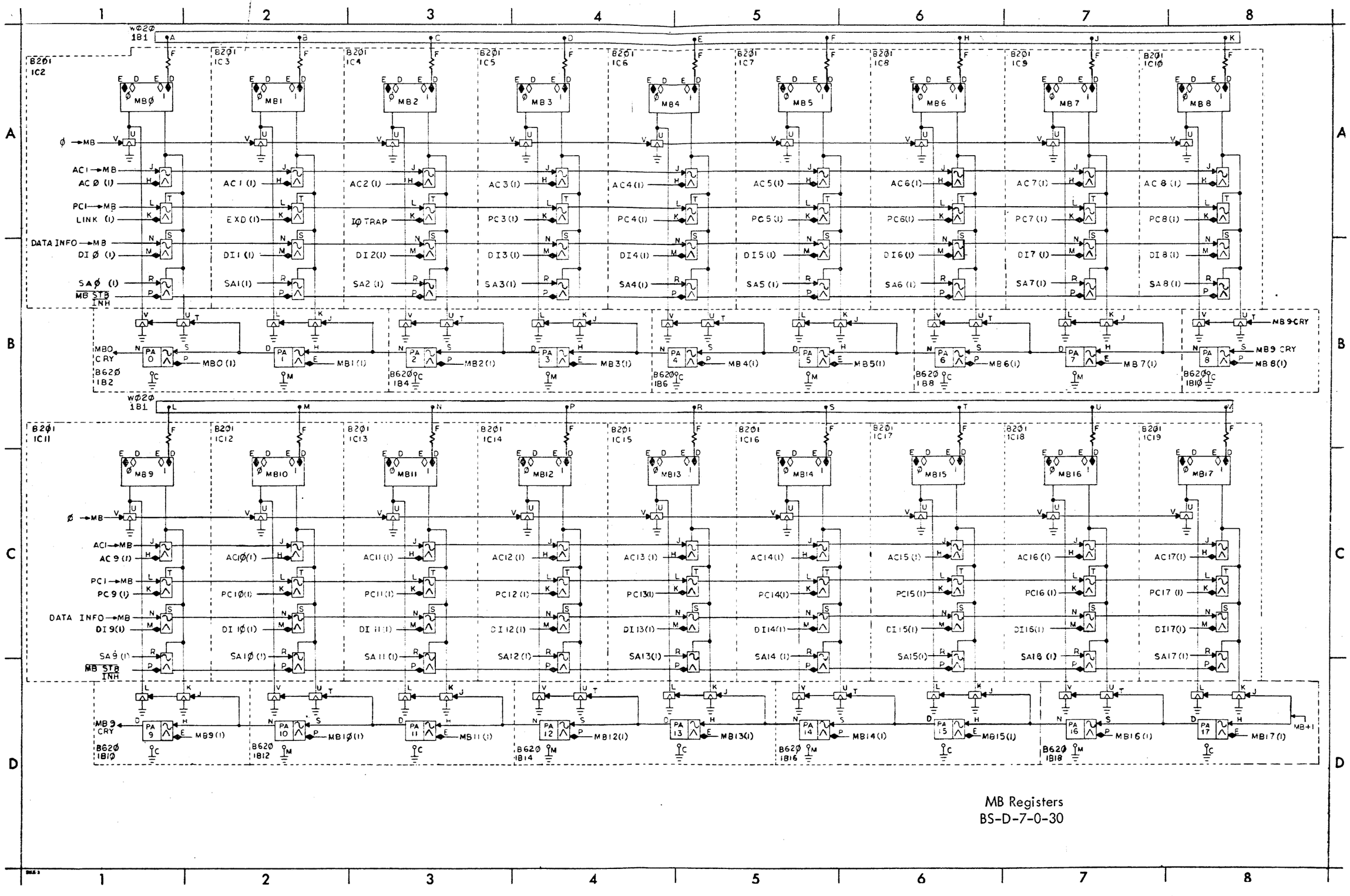
NOTE:
ALL B684'S HAVE
PINS K,L&U JUMPERED
AS SHOWN IN B3.

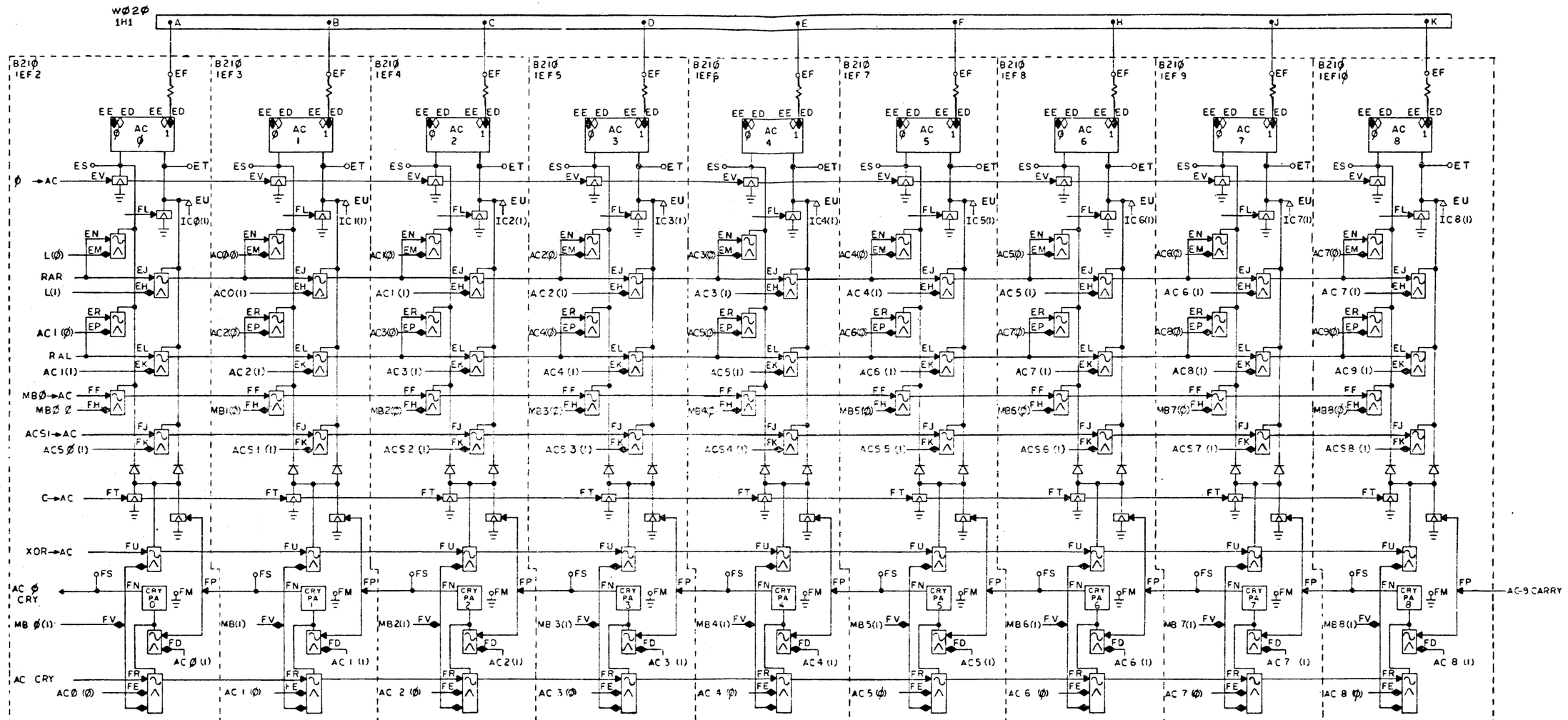
MB Bus Drivers
BS-D-7-0-28



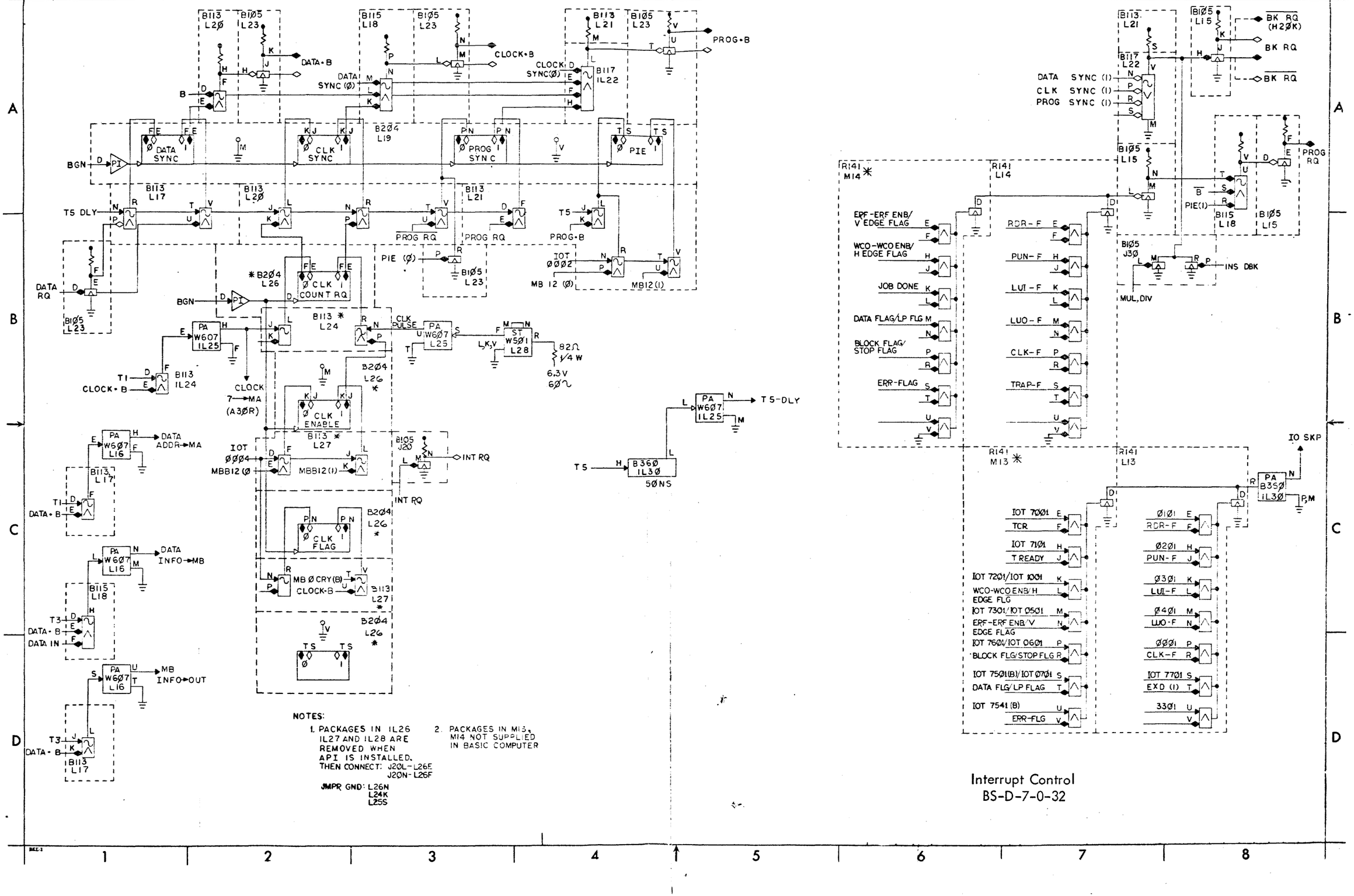
NOTE:
MA 3,4 & PC 3,4 B2Ø1'S SUPPLIED WITH MEMORY EXTENSION CONTROL TYPE 148

MA and PC Registers
BS-D-7-0-29

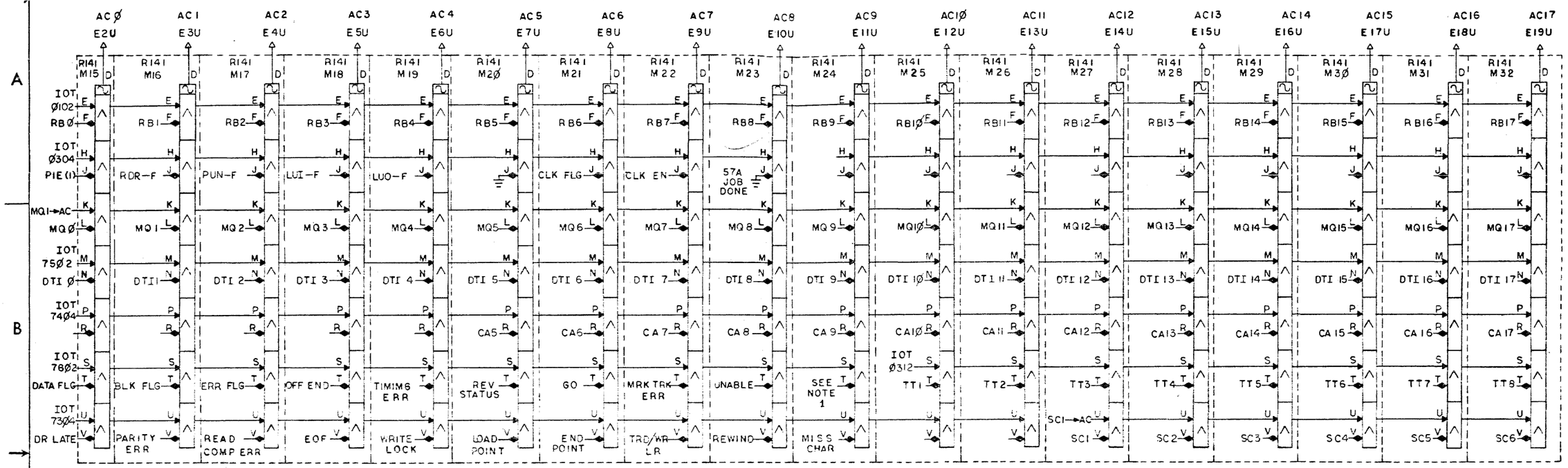

1
2
3
4
5
6
7
8
A
B
C
D
MB Registers
BS-D-7-0-30



AC Registers (Sheet 1)
BS-D-7-0-31

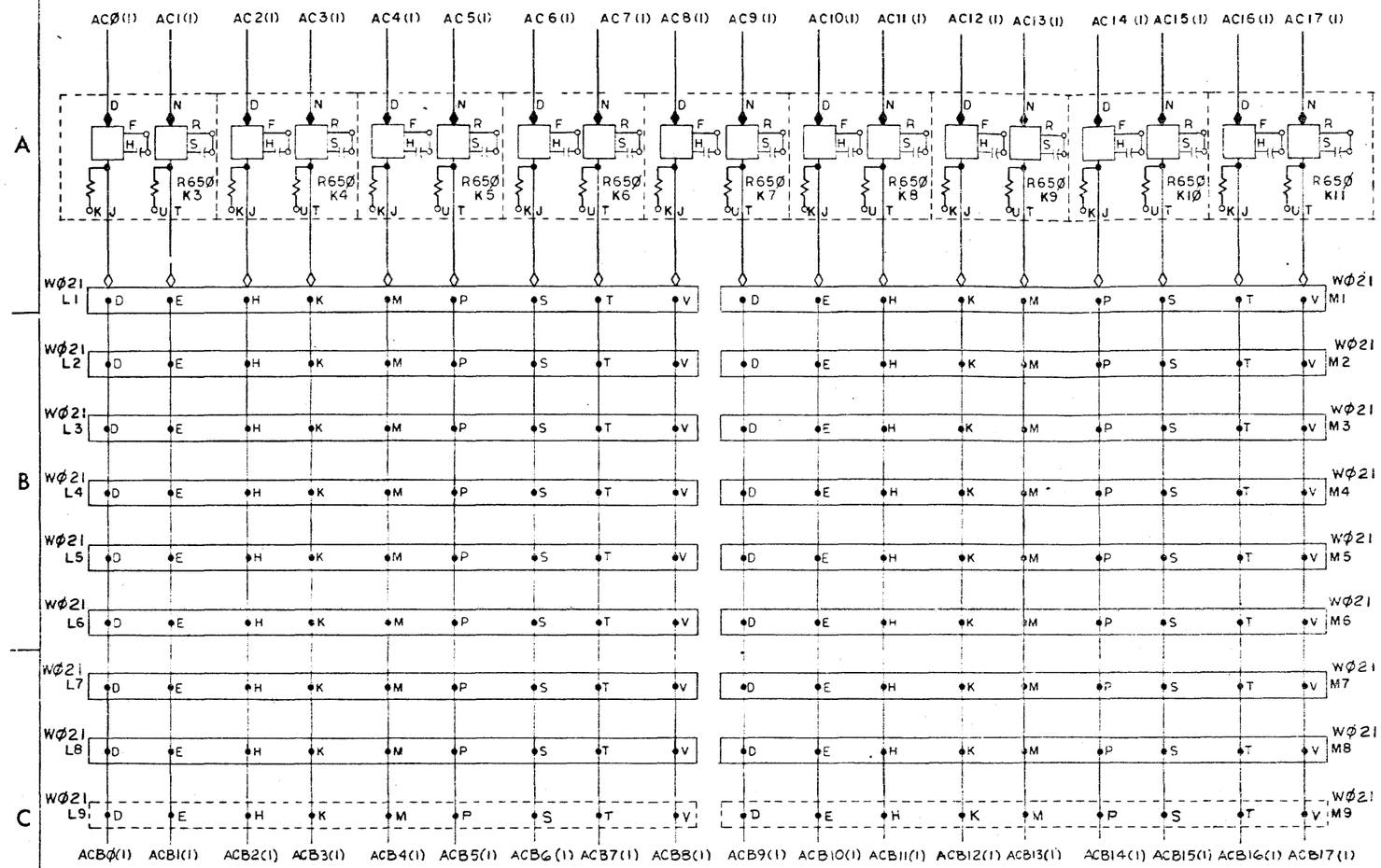


Interrupt Control
BS-D-7-0-32



NOTE:
1. UNGROUND THIS POINT WHEN SOLID STATE TRANSPORT IS INSTALLED

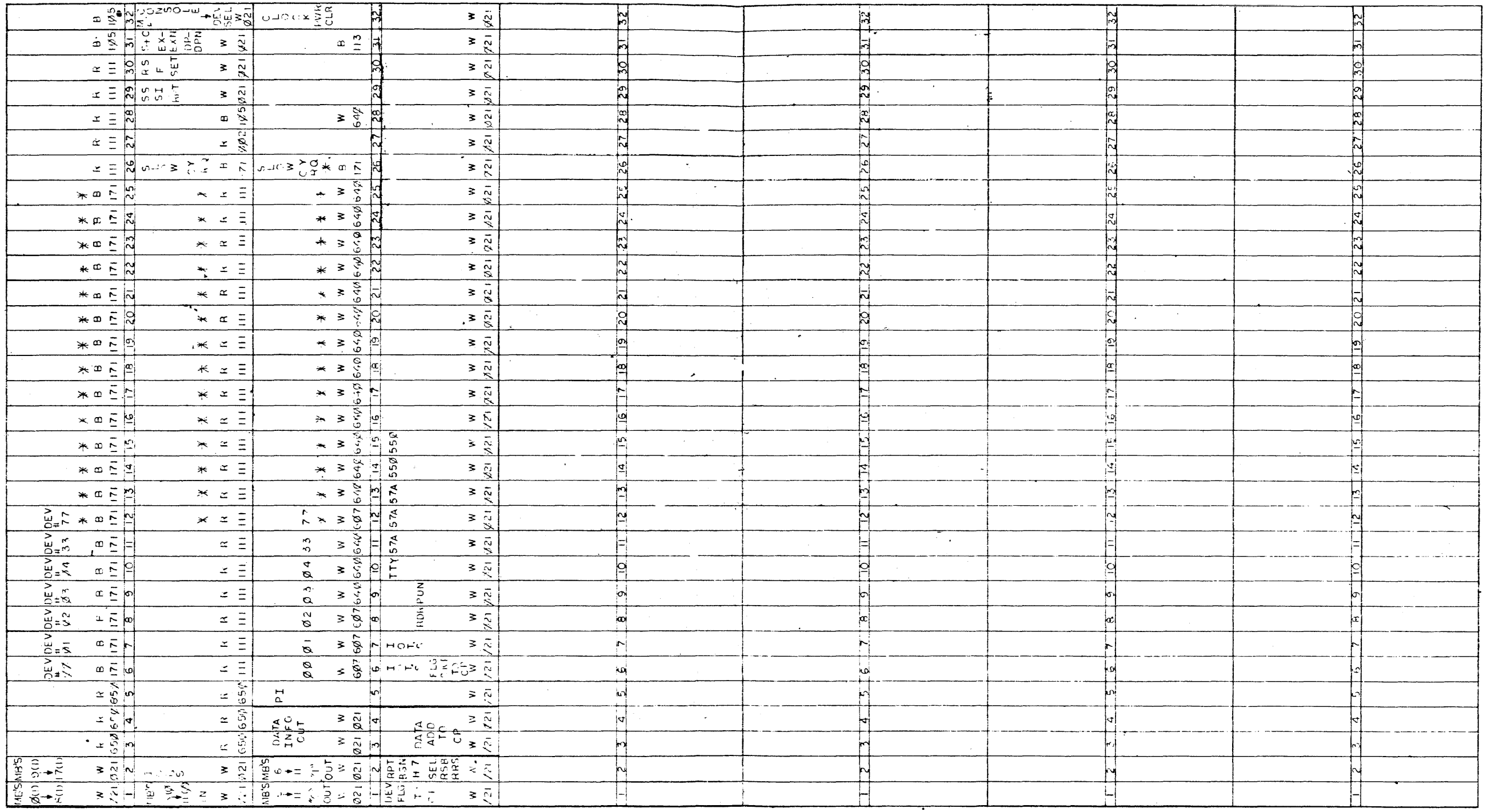
Information Collector
BS-D-7-0-33



ID EXPANSION

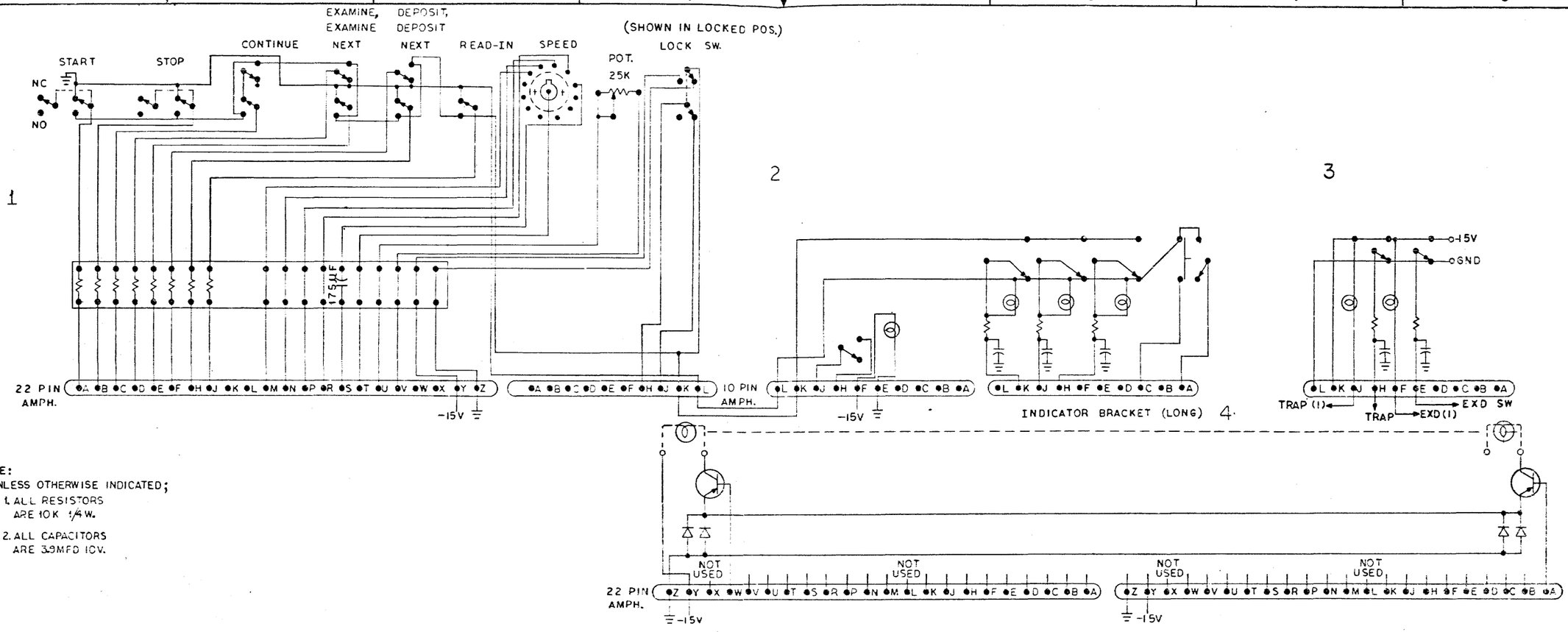
Information Distributor
BS-D-7-0-34

DEVICE SELECTOR
MODULE MAP



NOTE:
* OPTIONAL, NOT SUPPLIED

Device Selector Module Map
ML-D-7-0-35



NOTE:
UNLESS OTHERWISE INDICATED;
1. ALL RESISTORS ARE 10K 1/4 W.
2. ALL CAPACITORS ARE .39MFD 10V.

CONSOLE

MEMORY BUFFER	#4	L P R	STATES	IR	#4
ACCUMULATOR	#4	PROGRAM COUNTER			#4
MULTIPLIER QUOTIENT	#4	MEMORY ADDRESS			#4
ACCUMULATOR SWITCHES	#5	ADDRESS SWITCHES			#5
TRAP / EXTEND	#3	PUN FD / SS / SI / REP / PWR			#2
KEYS		SPEED		LOCK SW	#1

Console Panel Wiring Diagram
WD-D-7-0-37

W021 SIGNAL CABLE CONNECTORS

A1

DI Ø(1)	D
DI 1(1)	E
DI 2(1)	H
DI 3(1)	K
DI 4(1)	M
DI 5(1)	P
DI 6(1)	S
DI 7(1)	T
DI 8(1)	V

A2

DI 9(1)	D
DI 10(1)	E
DI 11(1)	H
DI 12(1)	K
DI 13(1)	M
DI 14(1)	P
DI 15(1)	S
DI 16(1)	T
DI 17(1)	V

A4-MEM IND 5'6"

	D
	E
	H
	K
	M
	P
	S
	T
	V

1A11-1H23 1'5"

TP 2•SEL Ø, 1	D
STROBE Ø, 1	E
	H
	K
	M
	P
	S
	T
	V

A12

	D
	E
	H
	K
	M
	P
	S
	T
	V

A3

READ(1) IND	A
READ(2) IND	B
	C
INHIBIT IND	D
	E
WRITE(1) IND	F
WRITE(2) IND	H
	J
	K
	L
	M
	N
	P
	R
	S
	T
	U
	V

B1-CONSOLE 8'5"

MB Ø IND	A
MB 1 IND	B
MB 2 IND	C
MB 3 IND	D
MB 4 IND	E
MB 5 IND	F
MB 6 IND	H
MB 7 IND	J
MB 8 IND	K
MB 9 IND	L
MB 10 IND	M
MB 11 IND	N
MB 12 IND	P
MB 13 IND	R
MB 14 IND	S
MB 15 IND	T
MB 16 IND	U
MB 17 IND	V

B32-CONSOLE 3'10"

	A
	B
	C
MA 3 IND	D
MA 4 IND	E
MA 5 IND	F
MA 6 IND	H
MA 7 IND	J
MA 8 IND	K
MA 9 IND	L
MA 10 IND	M
MA 11 IND	N
MA 12 IND	P
MA 13 IND	R
MA 14 IND	S
MA 15 IND	T
MA 16 IND	U
MA 17 IND	V

C32-CONSOLE 3'7"

	A
	B
	C
PC 3 IND	D
PC 4 IND	E
PC 5 IND	F
PC 6 IND	H
PC 7 IND	J
PC 8 IND	K
PC 9 IND	L
PC 10 IND	M
PC 11 IND	N
PC 12 IND	P
PC 13 IND	R
PC 14 IND	S
PC 15 IND	T
PC 16 IND	U
PC 17 IND	V

H1-CONSOLE 7'0"

AC Ø IND	A
AC 1 IND	B
AC 2 IND	C
AC 3 IND	D
AC 4 IND	E
AC 5 IND	F
AC 6 IND	H
AC 7 IND	J
AC 8 IND	K
AC 9 IND	L
AC 10 IND	M
AC 11 IND	N
AC 12 IND	P
AC 13 IND	R
AC 14 IND	S
AC 15 IND	T
AC 16 IND	U
AC 17 IND	V

J1-CONSOLE 7'6"

	A
	B
LINK IND	C
PIE(1)	D
RUN(1)B	E
	F
FETCH	H
	J
DEFER	K
	L
EXECUTE	M
	N
BREAK	P
	R
IR Ø IND	S
IR 1 IND	T
IR 2 IND	U
IR 3 IND	V

W020 INDICATOR CABLE CONNECTORS

1A13-1B29 3'6"

SEL Ø•READ(1)B	D
SEL Ø•WRITE(1)B	E
SEL 1•READ(1) B	H
SEL 1•WRITE(1)B	K
	M
	P
READ(2)B	S
WRITE(2)B	T
INH B	V

B31

	D
	E
	H
DA 3(1)	K
DA 4(1)	M
DA 5(1)	P
DA 6(1)	S
DA 7(1)	T
DA 8(1)	V

C31

DA 9(1)	D
DA 10(1)	E
DA 11(1)	H
DA 12(1)	K
DA 13(1)	M
DA 14(1)	P
DA 15(1)	S
DA 16(1)	T
DA 17(1)	V

E29-CONSOLE 2'10"

ACS Ø(1)	D
ACS 1(1)	E
ACS 2(1)	H
ACS 3(1)	K
ACS 4(1)	M
ACS 5(1)	P
ACS 6(1)	S
ACS 7(1)	T
ACS 8(1)	V

E30-CONSOLE 2'10"

ACS 9(1)	D
ACS 10(1)	E
ACS 11(1)	H
ACS 12(1)	K
ACS 13(1)	M
ACS 14(1)	P
ACS 15(1)	S
ACS 16(1)	T
ACS 17(1)	V

E31-CONSOLE 3'0"

	D
	E
	H
AS 3(1)	K
AS 4(1)	M
AS 5(1)	P
AS 6(1)	S
AS 7(1)	T
AS 8(1)	V

E32-CONSOLE 3'0"

AS 9(1)	D
AS 10(1)	E
AS 11(1)	H
AS 12(1)	K
AS 13(1)	M
AS 14(1)	P
AS 15(1)	S
AS 16(1)	T
AS 17(1)	V

EAE F27-2C8 2'7"

CRY DET	D
T2	E
T3	H
T4	K
T5	M
AC 17(Ø)	P
T7	S
IA 3	T
IB 1	V

EAE F28-2C9 2'7"

LINK(1)	D
LINK(Ø)	E
AC 1(1)	H
AC 1(Ø)	K
AC 2(1)	M
AC 2(Ø)	P
MQ Ø(1)	S
MQ Ø(Ø)	T
AC 17(1)	V

EAE F29-2C10 2'6"

INPUT (C-AC)	D
INPUT (TAG-CRY)	E
INPUT (AC-CRY)	H
EAE RAR	K
EAE RAL	M
EAE XOR	P
EAE CLA	S
SET LINK	T
CLEAR LINK	V

1F30-2B1 2'6"

MBB 6(Ø)	D
MBB 7(Ø)	E
MBB 8(Ø)	H
MBB 9(Ø)	K
MBB 10(Ø)	M
MBB 11(Ø)	P
MBB 12(Ø)	S
	T
	V

1F31-2A1 2'3"

MBB Ø(1)	D
MBB 1(1)	E
MBB 2(1)	H
MBB 3(1)	K
MBB 4(1)	M
MBB 5(1)	P
MBB 6(1)	S
MBB 7(1)	T
MBB 8(1)	V

1F32-2A2 2'4"

MBB 9(1)	D
MBB 10(1)	E
MBB 11(1)	H
MBB 12(1)	K
MBB 13(1)	M
MBB 14(1)	P
MBB 15(1)	S
MBB 16(1)	T
MBB 17(1)	V

1H31-2B31 4'10"

START + CONT	D
EX + EXN	E
DP + DPN	H
EX +EXN +DP +DPN	K
START +EX +DP	M
CONTINUE NOT	P
KEY MANUAL	S
READ IN	T
BGN	V

1H32-2B30 4'9"

RUN STOP	D
F SET	E
REPEAT	H
RQ SLOW CY	K
PWR CLK	M
	P
	S
RUN(Ø)B	T
START NOT	V

J32

	D
	E
	H
	K
	M
	P
	S
	T
	V

1K32-2B2 2'3"

I/OP 1	D
I/OP 2	E
I/OP 4	H
IOT	K
	M
	P
	S
	T
	.

CP Cables Out 1L1 to 1M12 (Sheet 1)
CL-D-7-0-38

W021 SIGNAL CABLE CONNECTORS

M10

	D
	E
	H
	K
	M
	P
	S
	T
	V

IM11-2D2
2'9"

RPT 1(B)	D
BGM	E
HOLE 7	H
SEL - RSB	K
SEL - RRB	M
	P
	S
	T
	V

IM12-2D7
3'3"

TSF	D
TTS	E
IOT 7701	H
	K
	M
	P
	S
	T
	V

173 DATA MULTIPLEXER
N1

T5	D
T6	E
DATA REQ	H
DATA IN	K
DATA ADR-MA	M
DATA INFO-MB	P
MB INFO OUT	S
RQ SLOW CY	T
	V

API
N2

F SET	D
FETCH	E
IA Ø	H
IB 2	K
MA 12 IA	M
MA 14 IA	P
MA 15 IA	S
MA 16 IA	T
MA 17 IA	V

W020 INDICATOR CABLE CONNECTORS

	N5	N6	N7	N8	N9	N10	N11	N12
A	A	A	A	A	A	A	A	A
B	B	B	B	B	B	B	B	B
C	C	C	C	C	C	C	C	C
D	D	D	D	D	D	D	D	D
E	E	E	E	E	E	E	E	E
F	F	F	F	F	F	F	F	F
H	H	H	H	H	H	H	H	H
J	J	J	J	J	J	J	J	J
K	K	K	K	K	K	K	K	K
L	L	L	L	L	L	L	L	L
M	M	M	M	M	M	M	M	M
N	N	N	N	N	N	N	N	N
P	P	P	P	P	P	P	P	P
R	R	R	R	R	R	R	R	R
S	S	S	S	S	S	S	S	S
T	T	T	T	T	T	T	T	T
U	U	U	U	U	U	U	U	U
V	V	V	V	V	V	V	V	V

550 DECTAPE
N3

IOT 7501(B)/IOT 0701	D
IOT 7541(B)	E
IOT 7502/IOT 0702	H
IOT 7601/IOT 0601	K
IOT 7602/IOT 1004	M
RUN(1)B	P
	S
	T
	V

API
N4

IMS DBK(1)	D
T-3	E
T-5	H
T-7	K
INT REC	M
INT REC NOT	P
INT RQ	S
MB(Ø)CRY(B)	T
PI 1 ⟶ MA	V

57A MAG TAPE
N5

ERF-ERF ENB V EDGE FLAG	D
WCO-WCO ENB H EDGE FLAG	E
TCR	H
T READY	K
DATA ADDR.MA	M
MB INFO OUT	P
DATA REQ	S
JOB DONE	T
	V

57A MAG TAPE
N6

IOT 7001	D
IOT 7101	E
IOT 7201/IOT 1001	H
IOT 7301/IOT 0501	K
IOT 7304	M
IOT 401	P
IOT 7404/IOT 0502	S
REWIND	T
MISS CHAR	V

340 DISPLAY
N7

BLOCK FLG STOP FLG	D
DATA FLG LP FLAG	E
DATA REQ	H
DATA IN	K
DATA ADDR-MA	M
BGM	P
MB INFO OUT	S
ERF-ERF ENB V EDGE FLAG	T
WCO-WCO ENB H EDGE FLAG	V

N8

IOT 7301/IOT 0501	D
IOT 7404/IOT 0502	E
IOT 7601/IOT 0601	H
	K
IOT 7501(B)/IOT 0701	M
IOT 7502/IOT 0702	P
IOT 7201/IOT 1001	S
IOT 1002	T
IOT 7602/IOT 1004	V

N9

	D
	E
	H
	K
	M
	P
	S
	T
	V

N10

	D
	E
	H
	K
	M
	P
	S
	T
DATA IN	V

N11

	D
	E
	H
	K
	M
	P
	S
	T
	V

N12

	D
	E
	H
	K
	M
	P
	S
	T
	V

PAPER TAPE READER
N15-383
4'2"

RB Ø(1)	D
RB 1(1)	E
RB 2(1)	H
RB 3(1)	K
RB 4(1)	M
RB 5(1)	P
RB 6(1)	S
RB 7(1)	T
RB 8(1)	V

PAPER TAPE READER
N16-383
4'3"

RB 9(1)	D
RB 10(1)	E
RB 11(1)	H
RB 12(1)	K
RB 13(1)	M
RB 14(1)	P
RB 15(1)	S
RB 16(1)	T
RB 17(1)	V

N17

	D
	E
	H
	K
	M
	P
	S
	T
	V

630
N18

IC 9-2	D
IC 10-2	E
IC 11-2	H
IC 12-2	K
IC 13-2	M
IC 14-2	P
IC 15-2	S
IC 16-2	T
IC 17-2	V

177 MQ OR 347 ASR
N19-2C5
3'4"

MQ Ø	D
MQ 1	E
MQ 2	H
MQ 3	K
MQ 4	M
MQ 5	P
MQ 6	S
MQ 7	T
MQ 8	V

177 MQ OR 347 ASR
N20-2C5
3'4"

MQ 9	D
MQ 10	E
MQ 11	H
MQ 12	K
MQ 13	M
MQ 14	P
MQ 15	S
MQ 16	T
MQ 17	V

550 DATA OR 340 X, Y
N21

DTI Ø	D
DTI 1	E
DTI 2	H
DTI 3	K
DTI 4	M
DTI 5	P
DTI 6	S
DTI 7	T
DTI 8	V

550 DATA OR 340 X, Y
N22

DTI 9	D
DTI 10	E
DTI 11	H
DTI 12	K
DTI 13	M
DTI 14	P
DTI 15	S
DTI 16	T
DTI 17	V

57A CA OR 340 DAC
N23

IC Ø-5	D
IC 1-5	E
IC 2-5	H
IC 3-5	K
IC 4-5	M
CA 5	P
CA 6	S
CA 7	T
CA 8	V

57A CA OR 340 DAC
N24

CA 9	D
CA 10	E
CA 11	H
CA 12	K
CA 13	M
CA 14	P
CA 15	S
CA 16	T
CA 17	V

550 OR TTY
N25

DATA FLG/LP FLAG	D
BLOCK FLAG/STOP FLAG	E
ERR-FLG	H
OFF END	K
TIMING ERR	M
REVERSE	P
GO	S
MARK TRACK ERR	T
UNABLE	V

550 OR TTY
N26-R286

IC 9-6	D
TT 1	E
TT 2	H
TT 3	K
TT 4	M
TT 5	P
TT 6	S
TT 7	T
TT 8	V

CP Cables Out 1L1 to 1M12 (Sheet 2)
CL-D-7-0-38

W021 SIGNAL CABLE CONNECTORS

L10

D
E
H
K
M
P
S
T
V

IL11-2D6
3'12"

CLSF	D
IOT 0002	E
IOT 0004	H
IOT 0304	K
RSF	M
IOT 0102	P
PSF	S
KSF	T
KRB	V

IL12-2D1
3'3"

RDR-F	D
PUN-F	E
LUI-F	H
LUO-F	K
RQ SLOW CY	M
	P
	S
	T
	V

L29-CONSOLE

LUI-F	D
	E
	H
	K
I/O TRAP(1)B	M
I/O TRAP SW	P
	S
	T
	V

L31

D
E
H
K
M
P
S
T
V

W020 INDICATOR CABLE CONNECTORS

A	B	C	D	E	F	H	J	K	L	M	N	P	R	S	T	U	V		

ACB 0(0)
ACB 1(0)
ACB 2(0)
ACB 3(0)
ACB 4(0)
ACB 5(0)
ACB 6(0)
ACB 7(0)
ACB 8(0)

	L1	L2	550 DEC TAPE L3	API L4	57A MAG TAPE L5	177 EAE L6	340 DISPLAY L7	L8	L9		
D	D	D	D	D	D	D	D	D	C	D	D
E	E	E	E	E	E	E	E	E	E	E	E
H	H	H	H	H	H	H	H	H	H	H	H
K	K	K	K	K	K	K	K	K	K	K	K
M	M	M	M	M	M	M	M	M	M	M	M
P	P	P	P	P	P	P	P	P	P	P	P
S	S	S	S	S	S	S	S	S	S	S	S
T	T	T	T	T	T	T	T	T	T	T	T
V	V	V	V	V	V	V	V	V	V	V	V

ACB 9(0)
ACB 10(0)
ACB 11(0)
ACB 12(0)
ACB 13(0)
ACB 14(0)
ACB 15(0)
ACB 16(0)
ACB 17(0)

	PUNCH IM1-3B31 6'6"	TTY IM2-R2B5 7'2"	550 DECTAPE M3	API M4	57A MAG TAPE M5	177 EAE M6	340 DISPLAY M7	M8	M9		
D	D	D	D	D	D	D	D	D	D	D	D
E	E	E	E	E	E	E	E	E	E	E	E
H	H	H	H	H	H	H	H	H	H	H	H
K	K	K	K	K	K	K	K	K	K	K	K
M	M	M	M	M	M	M	M	M	M	M	M
P	P	P	P	P	P	P	P	P	P	P	P
S	S	S	S	S	S	S	S	S	S	S	S
T	T	T	T	T	T	T	T	T	T	T	T
V	V	V	V	V	V	V	V	V	V	V	V

CP Cables Out 1L1 to 1M12 (Sheet 3)
CL-D-7-0-38

BAE 2

W021 SIGNAL CABLE CONNECTORS

57A STATUS
N27

DR LATE	D
PARITY ERR	E
READ COMP ERR	H
EOF	K
WRITE LOCK	M
LOAD POINT	P
END POINT	S
TRD/WR LR	T
REWIND	V

177 SC
M26-2C7
3'1"

T-6	D
EAE SHIFT	E
IC 11-7	H
SC 1	K
SC 2	M
SC 3	P
SC 4	S
SC 5	T
SC 6	V

N29

	D
TT 1	E
TT 2	H
TT 3	K
TT 4	M
TT 5	P
TT 6	S
TT 7	T
TT 8	V

N30

	D
	E
	H
	K
	M
	P
	S
	T
	V

N31

	D
	E
	H
	K
	M
	P
	S
	T
	V

W020 INDICATOR CABLE CONNECTORS

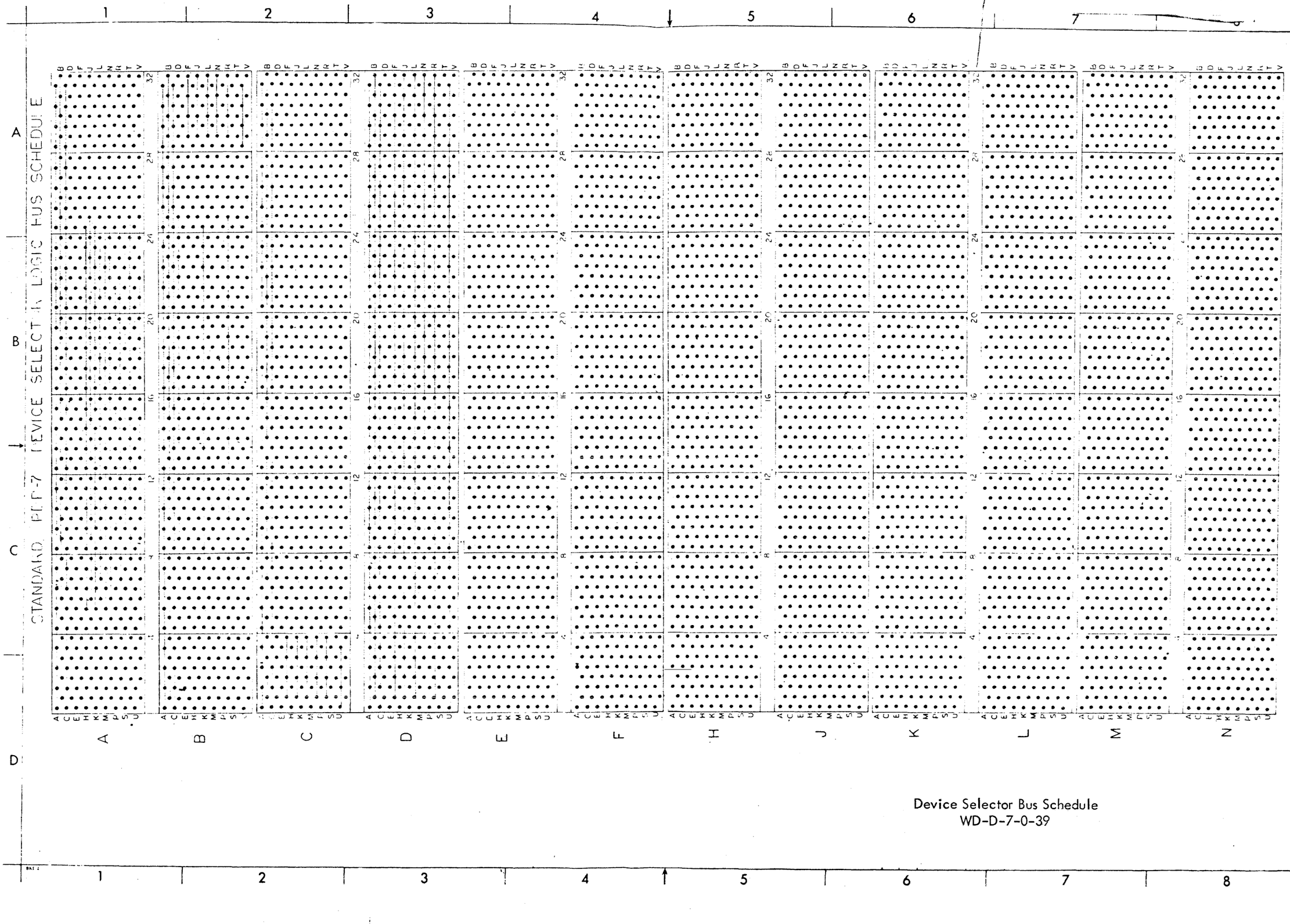
	A
	B
	C
	D
	E
	F
	H
	J
	K
	L
	M
	N
	P
	R
	S
	T
	U
	V

EAE
N32-2B3
2'5"

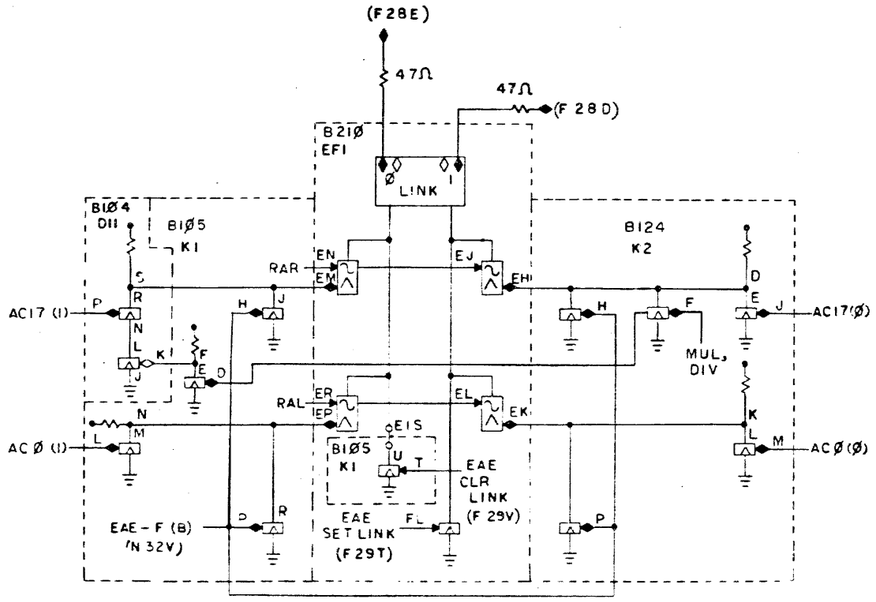
STOP CPTC	D
LEFT SHIFT	E
START CPTC	H
LEFT ROTATE	K
SC 1-AC	M
START MUL, DIV	P
MQ 1-AC	S
MUL, DIV	T
EAE-F(8)	V

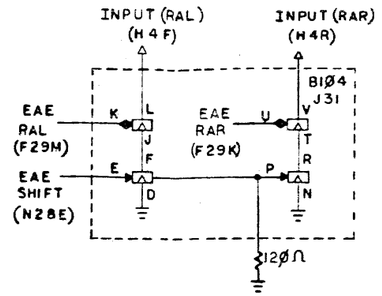
CP Cables Out 1L1 to 1M12 (Sheet 4)
CL-D-7-0-38

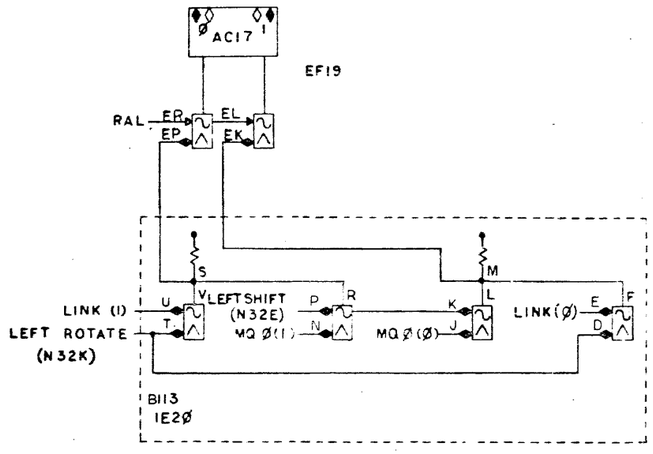
STANDARD PDP-7 DEVICE SELECTOR BUS SCHEDULE

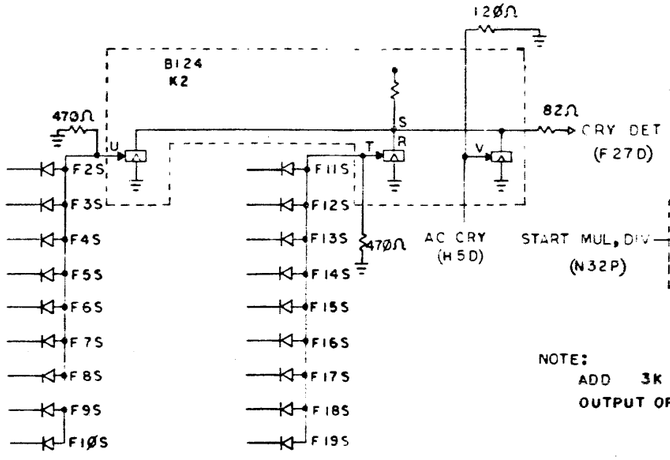


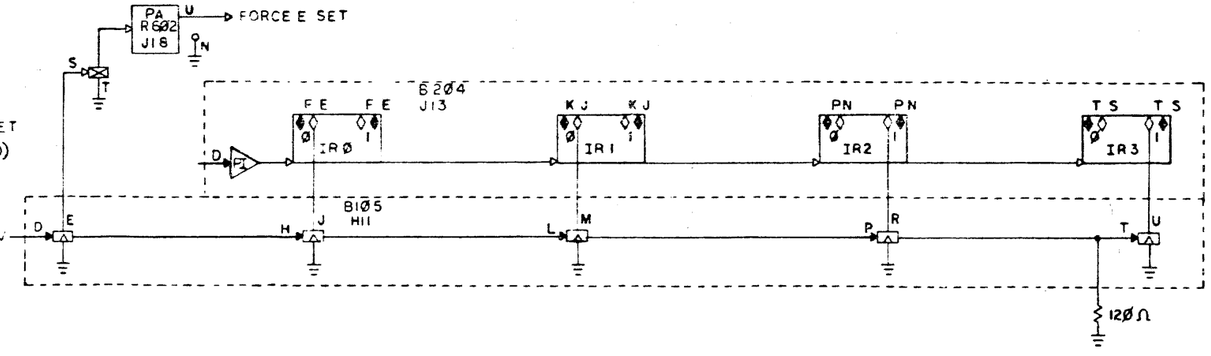
Device Selector Bus Schedule
WD-D-7-0-39





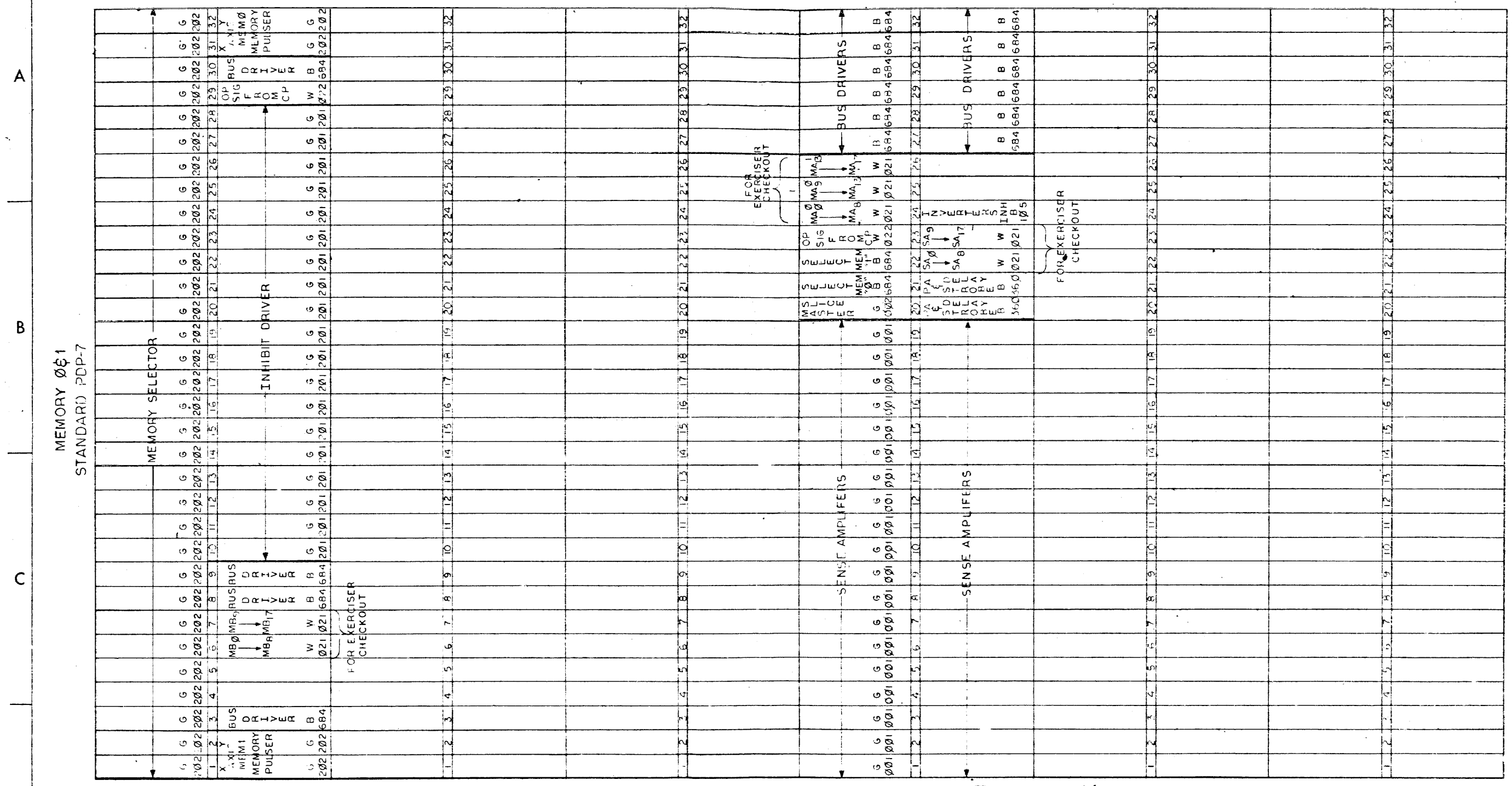






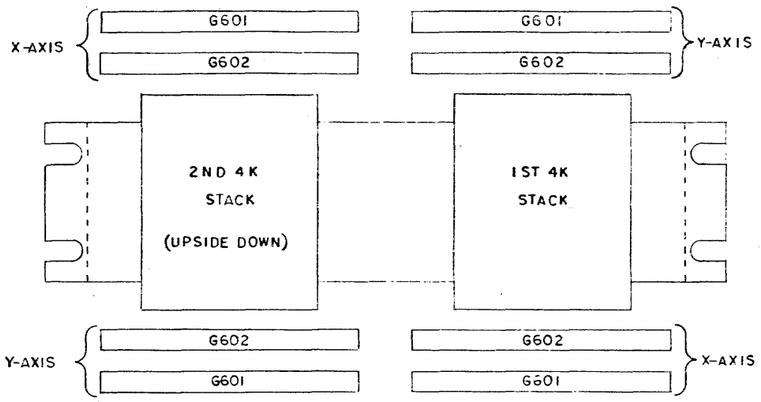
NOTE:
ADD 3K TO -15V ON ONE AND ZERO OUTPUT OF B210'S BITS LINK 1,2,17.

Central Processor Modification for EAE
BS-D-7-0-40

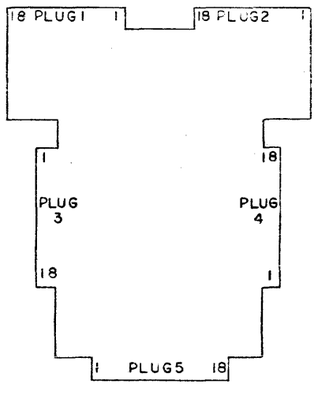


Standard Memory Module Map
ML-D-149-0-50

FRONT PANEL VIEW



G602 OR G601



VIEW FROM COMPONENT SIDE.

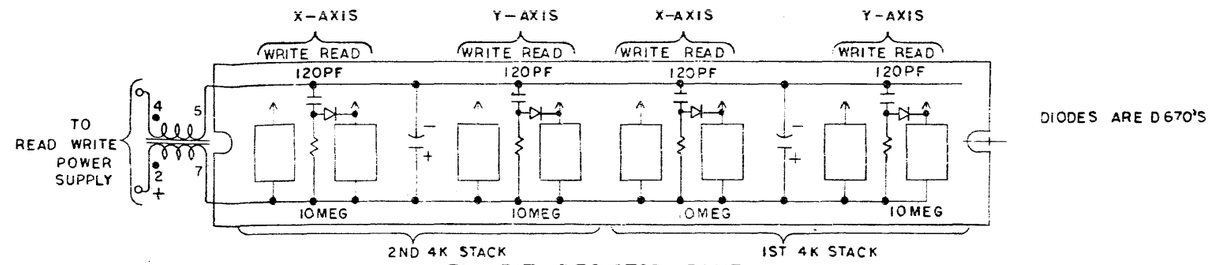
NOTE:
LETTERS OF PLUGS ARE ON PRINTED CIRCUIT SIDE OF BOARD.
NUMBERS ARE ON COMPONENT SIDE OF BOARD.

EXAMPLE

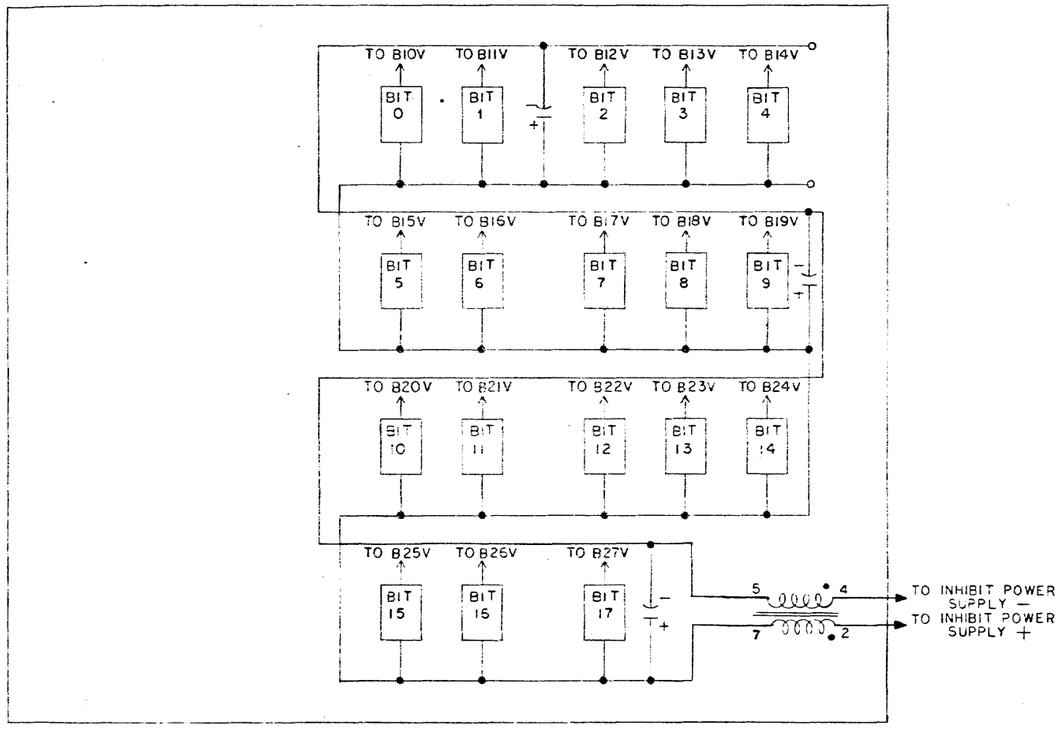
1-C 1-3

FIRST NUMBER (1) REFERS TO PLUG
SECOND LETTER (C) OR NUMBER (3) REFERS TO PINS.

FRONT PANEL VIEW OF READ WRITE RESISTORS



INHIBIT RESISTOR PANEL



NOTE:
1. CAPACITORS ARE 1 MFD, 150V.
2. RESISTORS ARE 125 OHMS ± 1%, 25 WATTS NON-INDUCTIVE.

Resistor Panels
WD-D-149-0-51

TOP

CONN	1	2		6	7
PIN	SENSE	SENSE		INH RET	INH DRV
A	0	0′		0	0
B	1	1′		1	1
C	2	2′		2	2
D	3	3′		3	3
E	4	4′		4	4
F	5	5′		5	5
H	6	6′		6	6
J	7	7′		7	7
K	8	8′		8	8
L	9	9′		9	9
M	10	10′		10	10
N	11	11′		11	11
P	12	12′		12	12
R	13	13′		13	13
S	14	14′		14	14
T	15	15′		15	15
U	16	16′		16	16
V	17	17′		17	17
W	* 18	* 18′		* 18	* 18
X					
Y					
Z					
WIRE COLOR	WHITE **	RED **	CONNECTORS MOUNTED ON CASTING ASSEMBLY	WHITE **	BLACK **

CONNECTOR CONFIGURATION FOR SENSE AND INHIBIT WINDINGS

TOP

GREY BLACK GREY BLACK

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	
DWG NO.	73	53	33	13	72	52	32	12	71	51	31	11	70	50	30	10			J05-1Y
A-149-0-43	63	43	23	03	62	42	22	02	61	41	21	01	60	40	20	00			
	A	B	C	D	E	F	H	J	K	L	M	N	P	R	S	T	U	V	

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	
DWG NO.	77	57	37	17	76	56	36	16	75	55	35	15	74	54	34	14			J05-2Y
A-149-0-44	67	47	27	07	66	46	26	06	65	45	25	05	64	44	24	04			
	A	B	C	D	E	F	H	J	K	L	M	N	P	R	S	T	U	V	

FRONT VIEW OF STACK

SOCKETS ARE MOUNTED ON FRONT MOUNTING PLATE

	V	U	T	S	R	P	N	M	L	K	J	H	F	E	D	C	B	A	
DWG NO.			04	24	44	64	05	25	45	65	06	26	46	66	07	27	47	67	J05-2X
A-149-0-42			14	34	54	74	15	35	55	75	16	36	56	76	17	37	57	77	
	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

	V	U	T	S	R	P	N	M	L	K	J	H	F	E	D	C	B	A	
DWG NO.			00	20	40	60	01	21	41	61	02	22	42	62	03	23	43	63	J05-1X
A-149-0-41			10	30	50	70	11	31	51	71	12	32	52	72	13	33	53	73	
	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

BROWN YELLOW BROWN YELLOW

CONNECTOR CONFIGURATION AND ADDRESS LOCATION OF R/W WINDING, READ DRIVE END

TOP

BLACK GREY BLACK GREY

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	
DWG NO.			10	30	50	70	11	31	51	71	12	32	52	72	13	33	53	73	J02-1Y
A-149-0-39			00	20	40	60	01	21	41	61	02	22	42	62	03	23	43	63	
	A	B	C	D	E	F	H	J	K	L	M	N	P	R	S	T	U	V	

	J	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	
DWG NO.			14	34	54	74	15	35	55	75	16	36	56	76	17	37	57	77	J02-2Y
A-149-0-40			04	24	44	64	05	25	45	65	06	26	46	66	07	27	47	67	
	A	B	C	D	E	F	H	J	K	L	M	N	P	R	S	T	U	V	

BACK VIEW OF STACK

SOCKETS ARE FLOATING ***

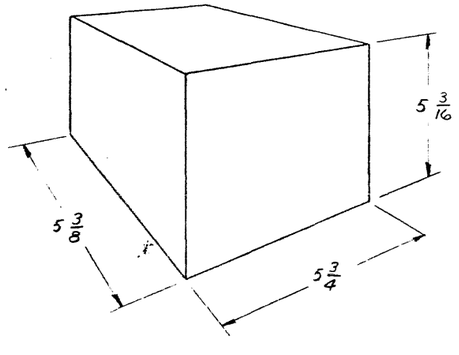
	V	U	T	S	R	P	N	M	L	K	J	H	F	E	D	C	B	A	
DWG NO.	67	47	27	07	66	46	26	06	65	45	25	05	64	44	24	04			J02-2X
A-149-0-38	77	57	37	17	76	56	36	16	75	55	35	15	74	54	34	14			
	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

	V	U	T	S	R	P	N	M	L	K	J	H	F	E	D	C	B	A	
DWG NO.	63	43	23	03	62	42	22	02	61	41	21	01	60	40	20	00			J02-1X
A-149-0-37	73	53	33	13	72	52	32	12	71	51	31	11	70	50	30	10			
	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

YELLOW BROWN YELLOW BROWN

CONNECTOR CONFIGURATION AND ADDRESS LOCATION OF R/W WINDING, READ RETURN END

ALUMINUM HOUSING FOR STACK



HOUSING CONSISTS OF HALVES BOLTED TOGETHER FOR EASY DISASSEMBLY

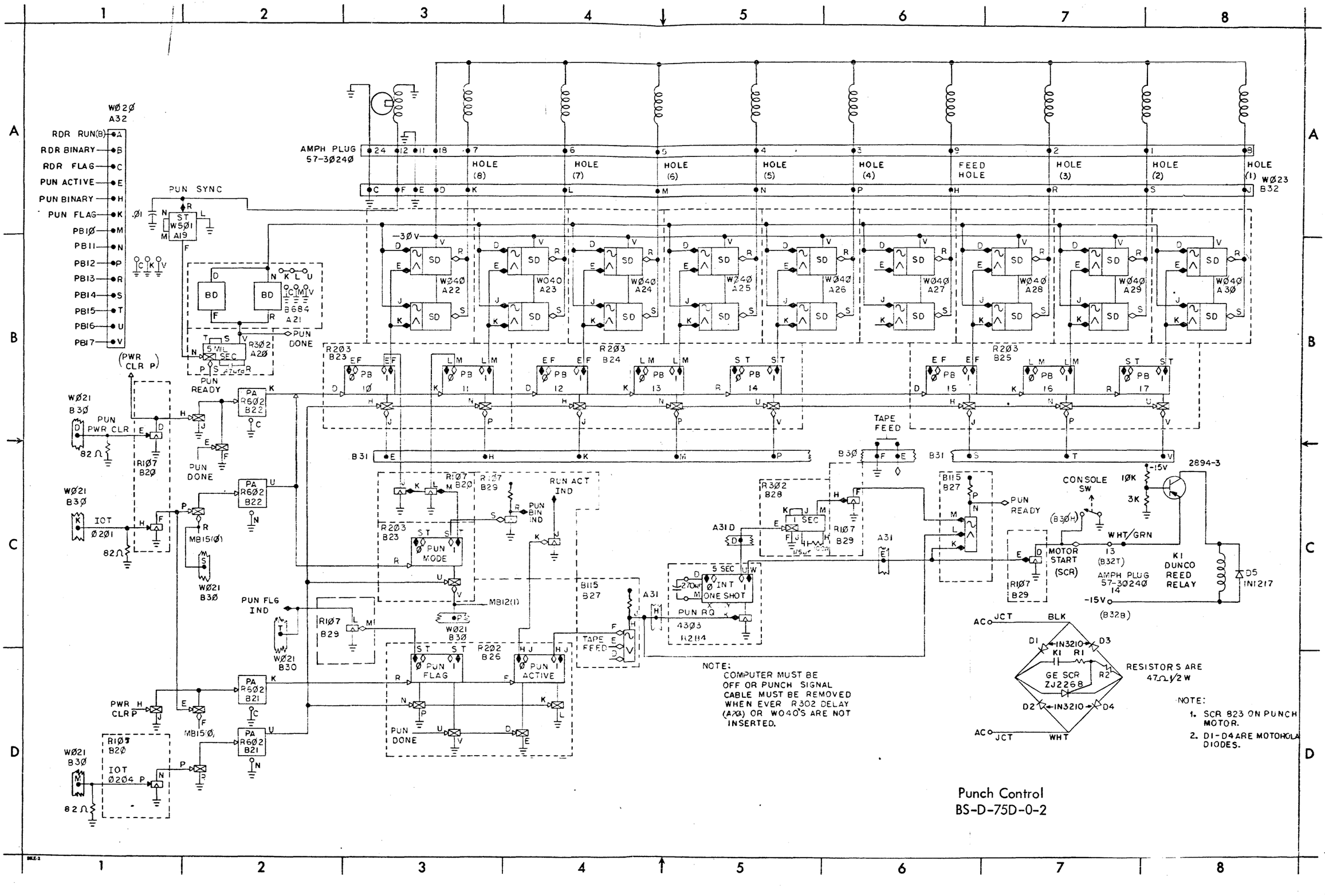
NOTES:

* FOR STACK WITH 19 PLANES, THESE PINS ARE USED FOR 19TH SENSE AND INHIBIT WINDINGS.

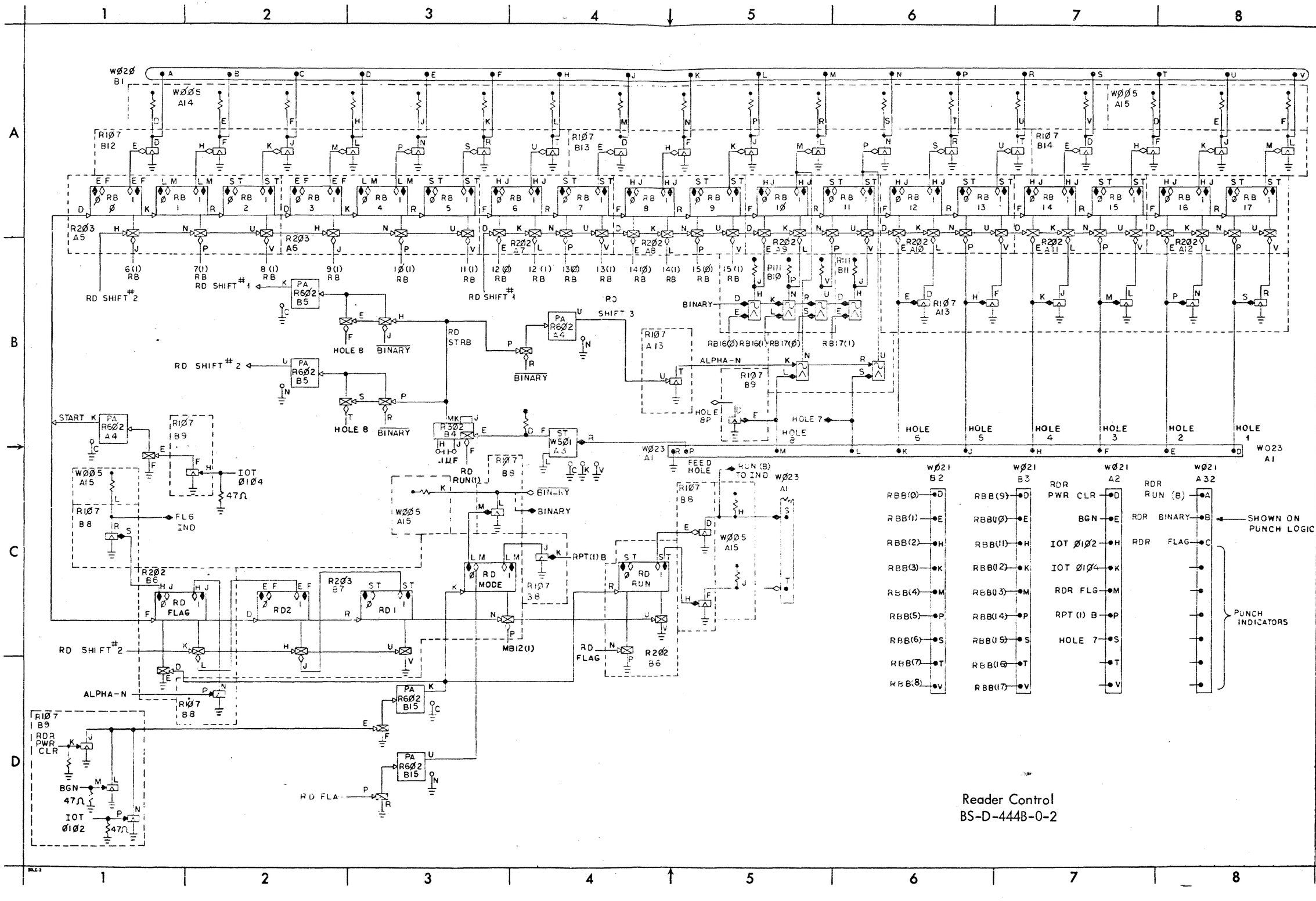
** EACH PAIR OF SENSE WINDINGS WILL BE TWISTED. EACH PAIR OF INHIBIT WINDINGS WILL BE TWISTED.

*** LENGTH OF CABLES FROM SOCKETS TO REAR MOUNTING PLATES IS 10 INCHES.

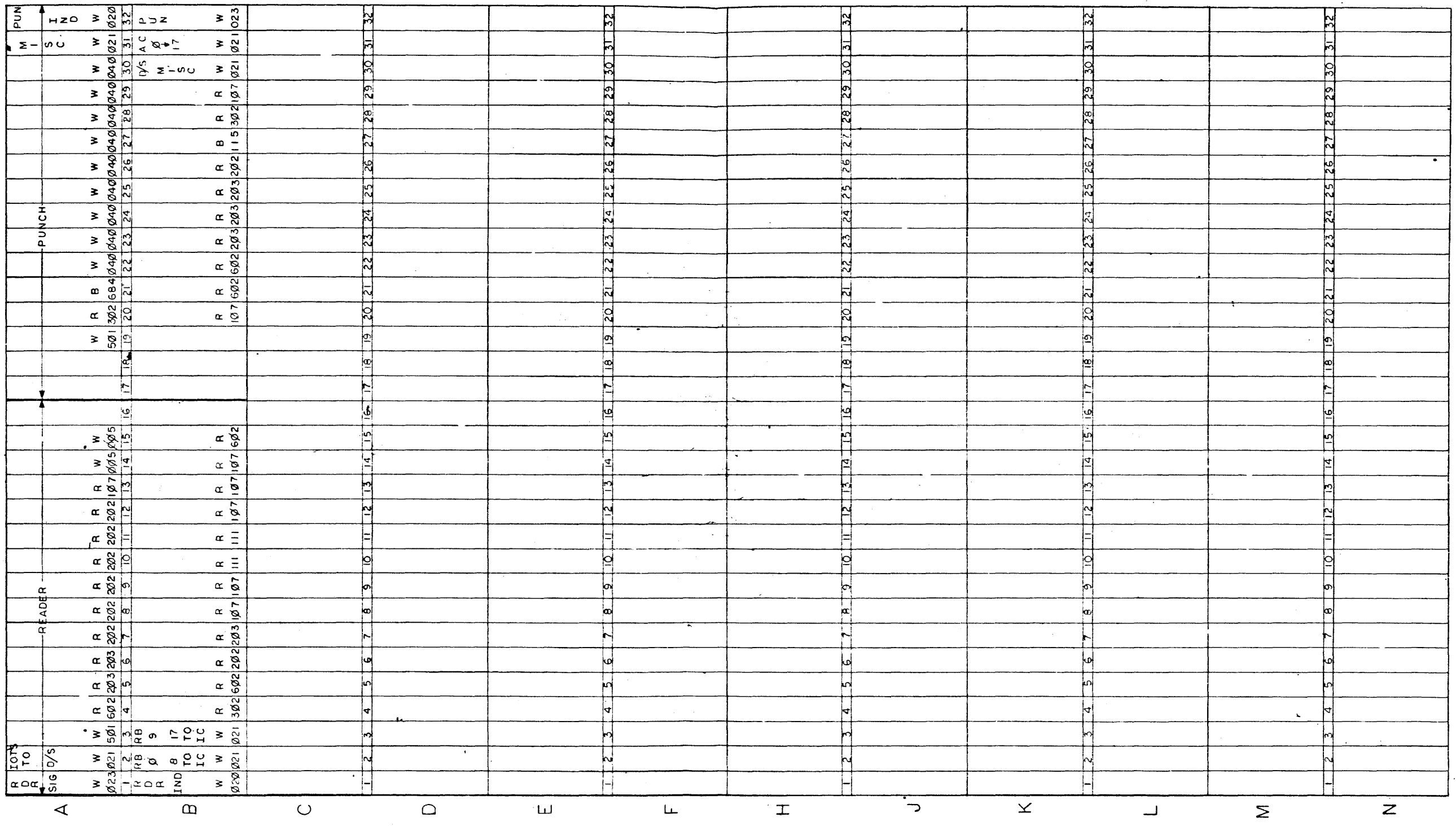
Memory Stack Connector Configuration
CL-D-149-0-52



Punch Control
BS-D-75D-0-2

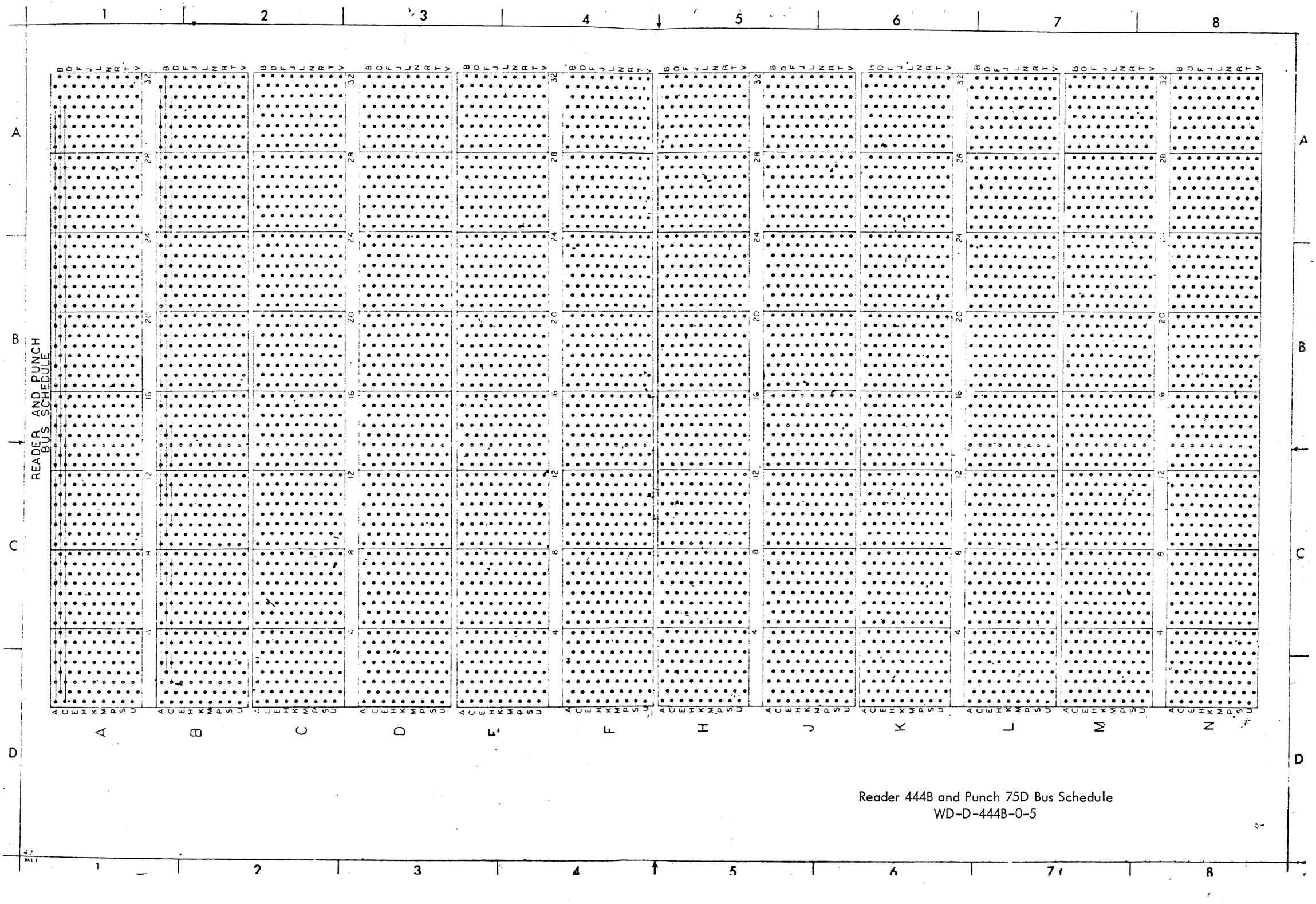

WØ2Ø B1
WØØ5 A14
WØØ5 A15
RIØ7 B12
RIØ7 B13
RIØ7 B14
R2Ø3 A5
R2Ø3 A6
R2Ø3 B7
R2Ø2 B6
RD SHIFT #1
RD SHIFT #2
PA R6Ø2 B5
PA R6Ø2 A4
PA R6Ø2 A7
PA R6Ø2 A8
PA R6Ø2 A9
PA R6Ø2 A10
PA R6Ø2 A11
PA R6Ø2 A12
PA R6Ø2 B15
RIØ7 A13
RIØ7 B9
RIØ7 B8
RIØ7 B7
RIØ7 B10
RIØ7 B11
R3Ø2 B4
WSØI A3
WØ23 A1
WØ21 B2
WØ21 B3
WØ21 A2
WØ21 A32
HOLE 8
BINARY
RD STRB
RD SHIFT 3
ALPHA-N
START K
IOT Ø1Ø4
47Ω
FL6 IND
RD RUN(1)
RD MODE
RD RUN
RD FLAG
RD2
RD1
RPT(1) B
MB12(1)
HOLE 8P
HOLE 7
HOLE 6
HOLE 5
HOLE 4
HOLE 3
HOLE 2
HOLE 1
FEED HOLE
RUN (B) TO IND
RDR PWR CLR
BGN
IOT Ø1Ø2
RDR BINARY
RDR FLAG
RDR RUN (B)
SHOWN ON PUNCH LOGIC
PUNCH INDICATORS
Reader Control
BS-D-444B-0-2

READER & PUNCH
MODULE MAP

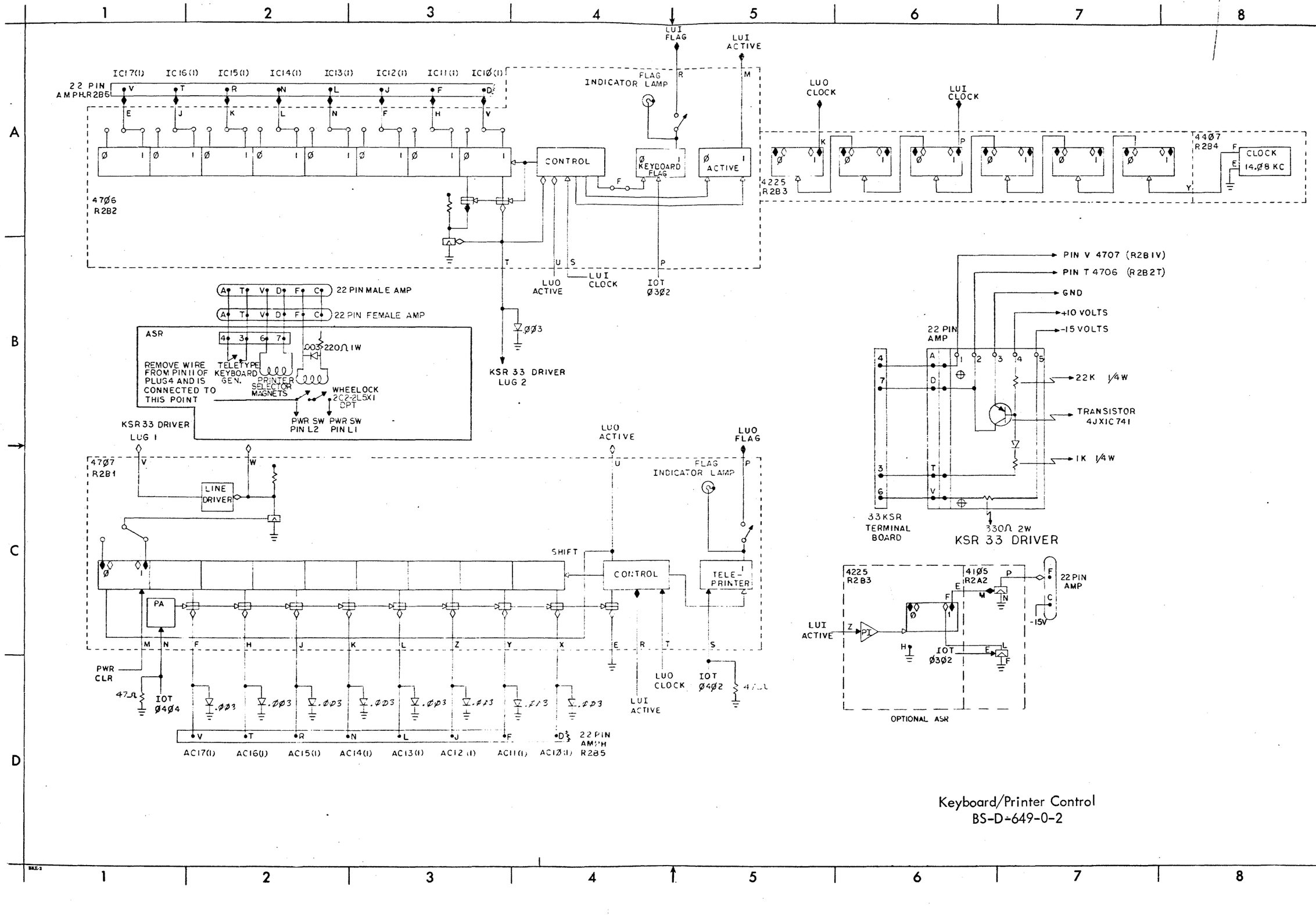


Reader 444B and Punch 75D Module Map
ML-D-444B-0-3

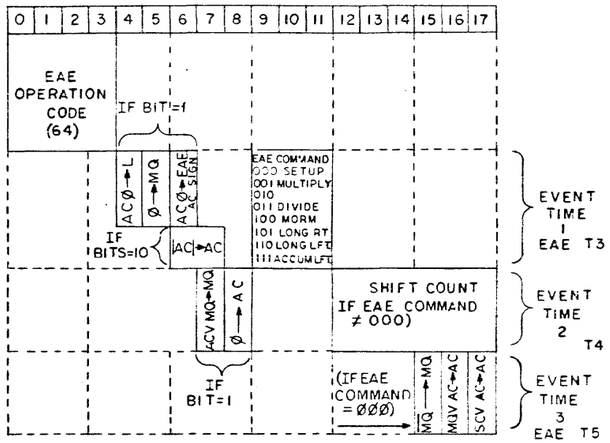
READER AND PUNCH
BUS SCHEDULE



Reader 444B and Punch 75D Bus Schedule
WD-D-444B-0-5



Keyboard/Printer Control
BS-D-649-0-2



EAE INSTRUCTION BIT ASSIGNMENT

T1		
T2	STROBE EAE: 1→EAE-F	Ø→EAE-F MUL•MQ 17(1): 1→STOP SHIFT, 1→ADD DIV: 1→SUB, 1→STOP SHIFT
T3	Ø→STOP SHIFT, Ø→ADD, Ø→SUB MB4(1): ACØ→L SET/CLR→LINK MB5(1): Ø→MQ MB6(1): ACØ→EAE AC SIGN MB6(1) • MB7(Ø) • ACØ(1): $\overline{AC}$→AC OTHER: $\overline{MB12\text{-}17 \rightarrow J}$→SC12-17	MUL V DIV: START MUL, DIV, Ø→LINK
T4	MB7(1): AC1→MQ MB8(1): Ø→AC	
T5	SETUP • MB15(1): {1→MQ, Ø→MQ} ($\overline{MQ}$→MQ) SETUP • MB16(1): MQ1→AC SETUP • MB17(1): SC1→AC MB9(Ø) • MB10(Ø) • MB11(1): 1→MUL MB9(Ø) • MB10(1): 1→DIV, 1→DIV FIRST SC 12-17=77: 1→FULL MB8(Ø) • NORMALIZE • ACØ ⊻ AC1: 1→FULL MUL, DIV: INHIBIT BK RQ CN CP EAE AC SIGN ⊻ LINK→EAE SIGN	
T6	MB9(1): START SHIFT	
T7	SETUP: CLR (MUL V DIV)•EAE AC SIGN (1): $\overline{MQ}$→MQ 1→NORM	

DELAY ADJUSTMENT

INITIAL: SET ALL DELAYS TO MAXIMUM EXCEPT:

1. D3Ø (D-177-Ø-5 D3)
   5Ø NS INPUT (D3ØH) TO OUTPUT (D3ØL)
2. D31 (D-177-Ø-5 C2)
   ADJUST FOR MINIMUM
3. A27 (D-177-Ø-6 D5)
   ADJUST FOR MINIMUM

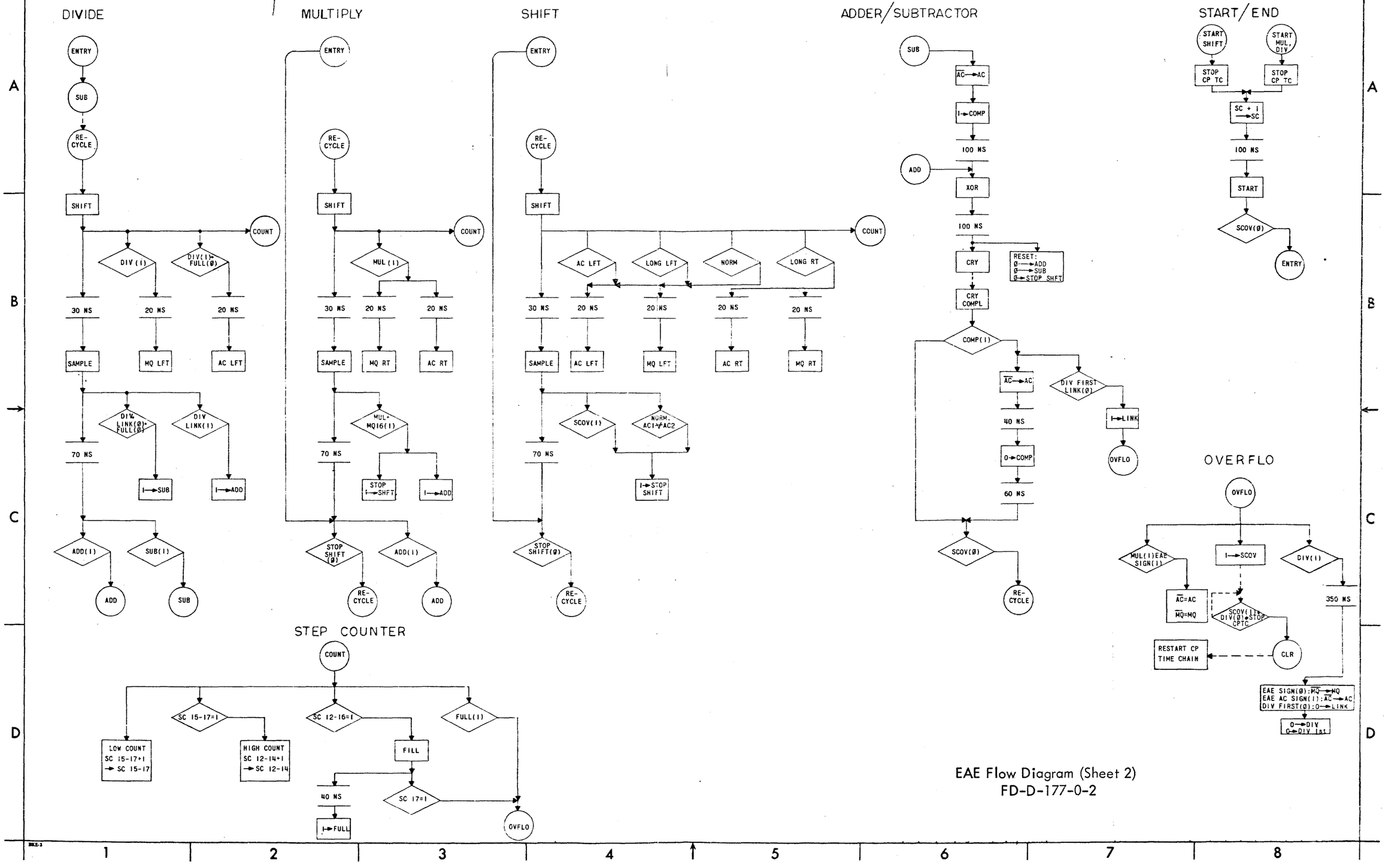
FINAL: ADJUST DELAYS AS SHOWN ON INDIVIDUAL PRINTS.
THE ORDER OF ADJUSTMENT IS INDICATED THERE.

WIRING NOTE:

WHEN EAE IS INSTALLED, WIRE:

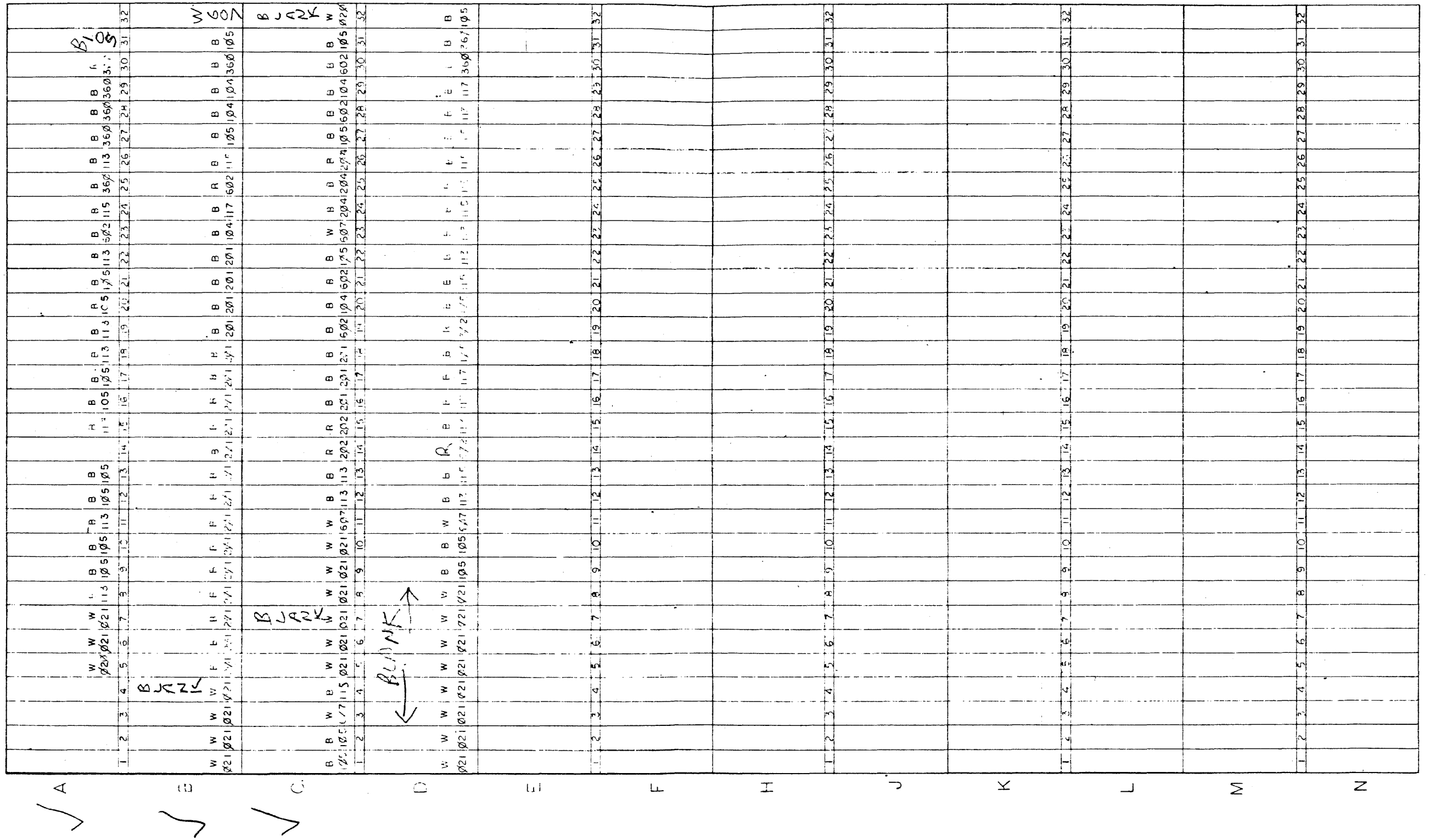
1. GROUNDS FROM LOWEST PIN IN EAE TO DEVICE SELECTOR HIGHEST PINS
2. BGN: EAE (D2ØL) TO DS(B31V)
3. 1→MQ EAE (A23N) TO EAE (A12T)

EAE Flow Diagram (Sheet 1)
FD-D-177-0-2

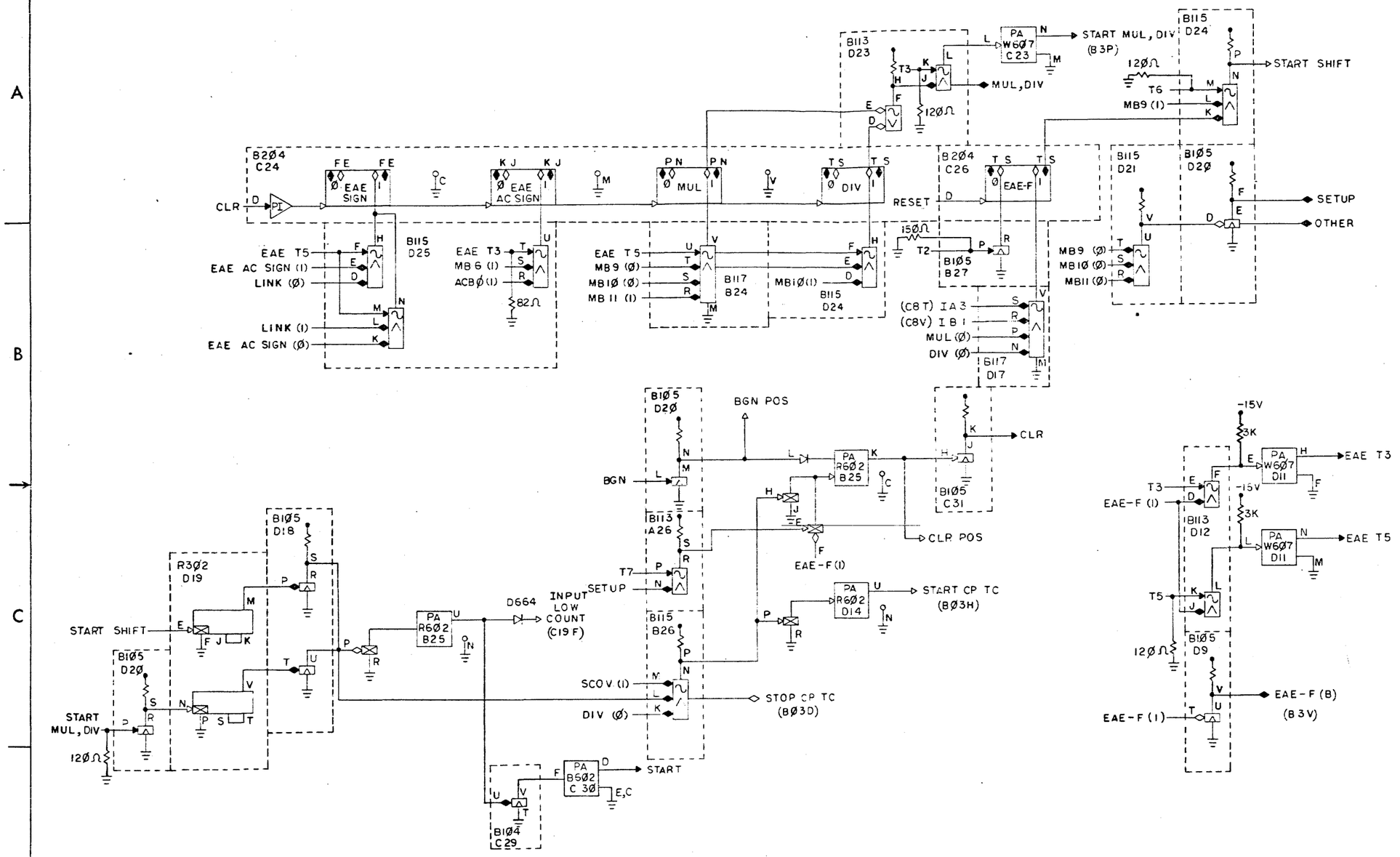


EAE Flow Diagram (Sheet 2)
FD-D-177-0-2

EAE MODULE MAP



EAE Module Map
ML-D-177-0-3



NOTE:

1. DELAY ADJUSTMENT

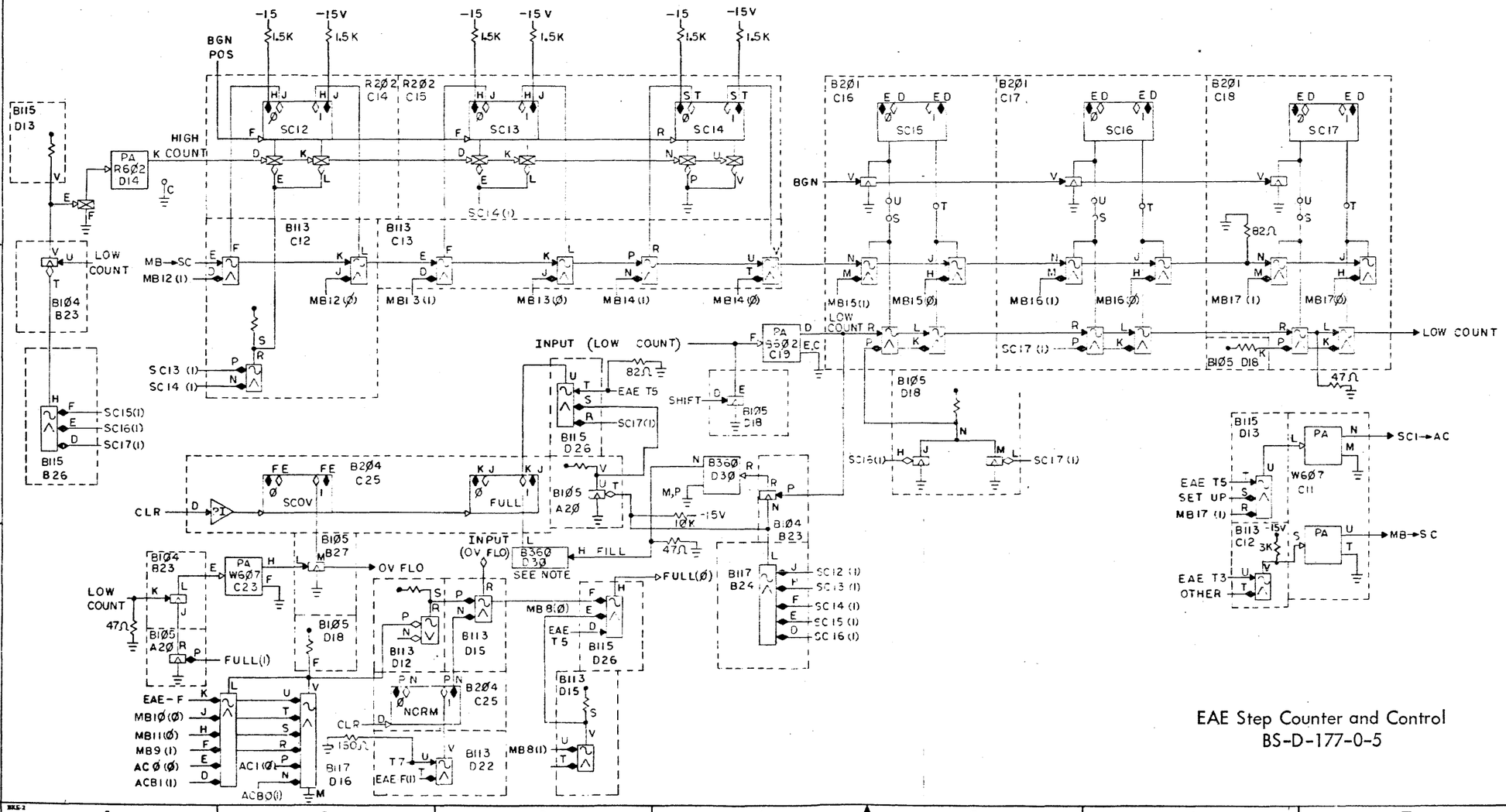
	DLY	PROBE 1	PROBE 2	SYNC	CONDITION
8.	DI9 UPPER	CP K21J	CP K21K	PROBE 1	LEVEL TO FALL ICONS AFTER PULSE WHILE SHIFTING
9.	DI9 LOWER	CP K21J	CP K21K	PROBE 1	AS ABOVE WHILE MULTIPLYING

EAE States
BS-D-177-0-4

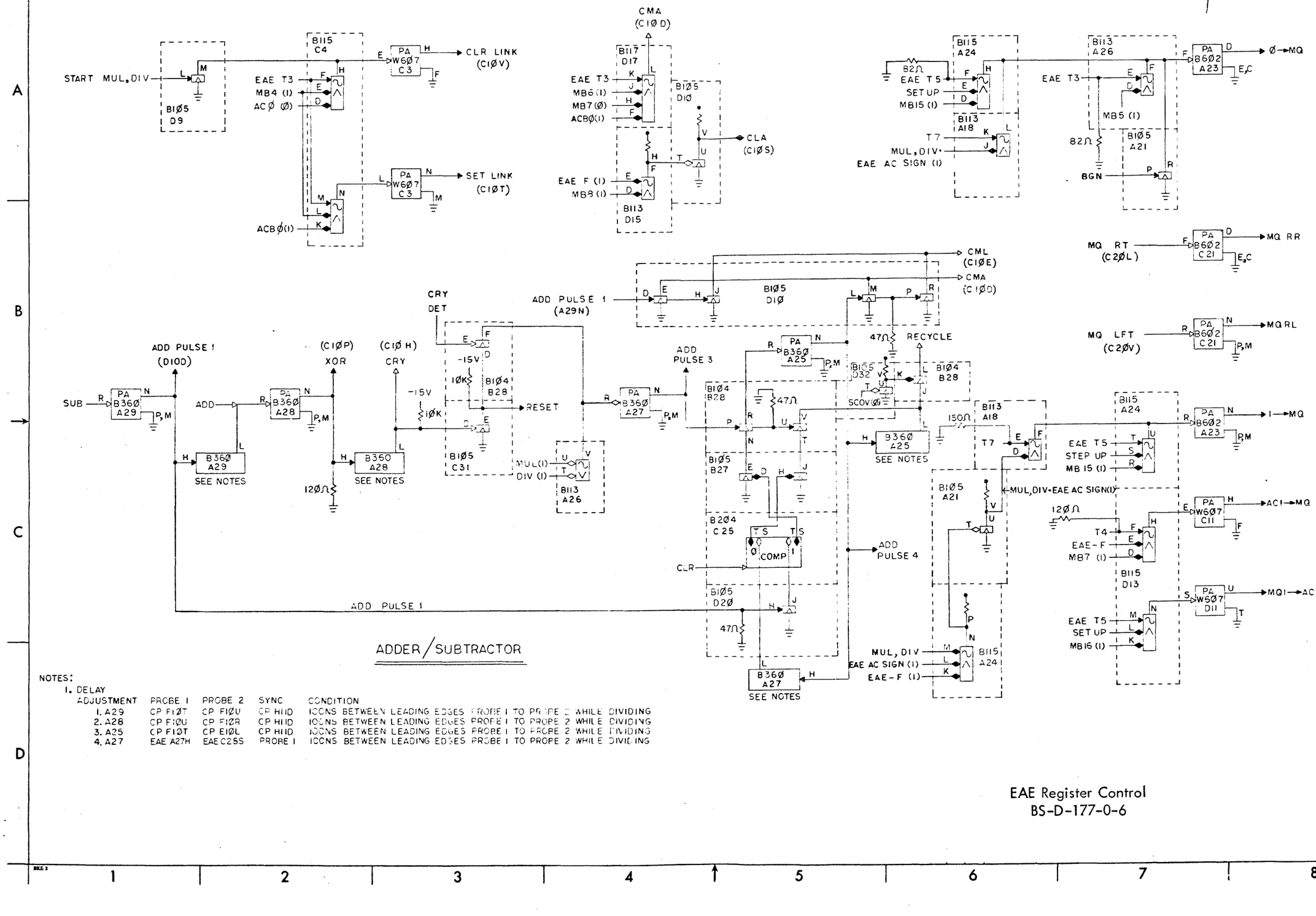
BKE-2

NOTE:
1. DELAY ADJUSTMENT

DLY	PROBE 1	PROBE 2	SYNC	CONDITION
10.D30	EAE D30H	EAE C25J	PROBE 1	PULSE 50NS BEFORE LEVEL CHANGE BEGINS



EAE Step Counter and Control
BS-D-177-0-5



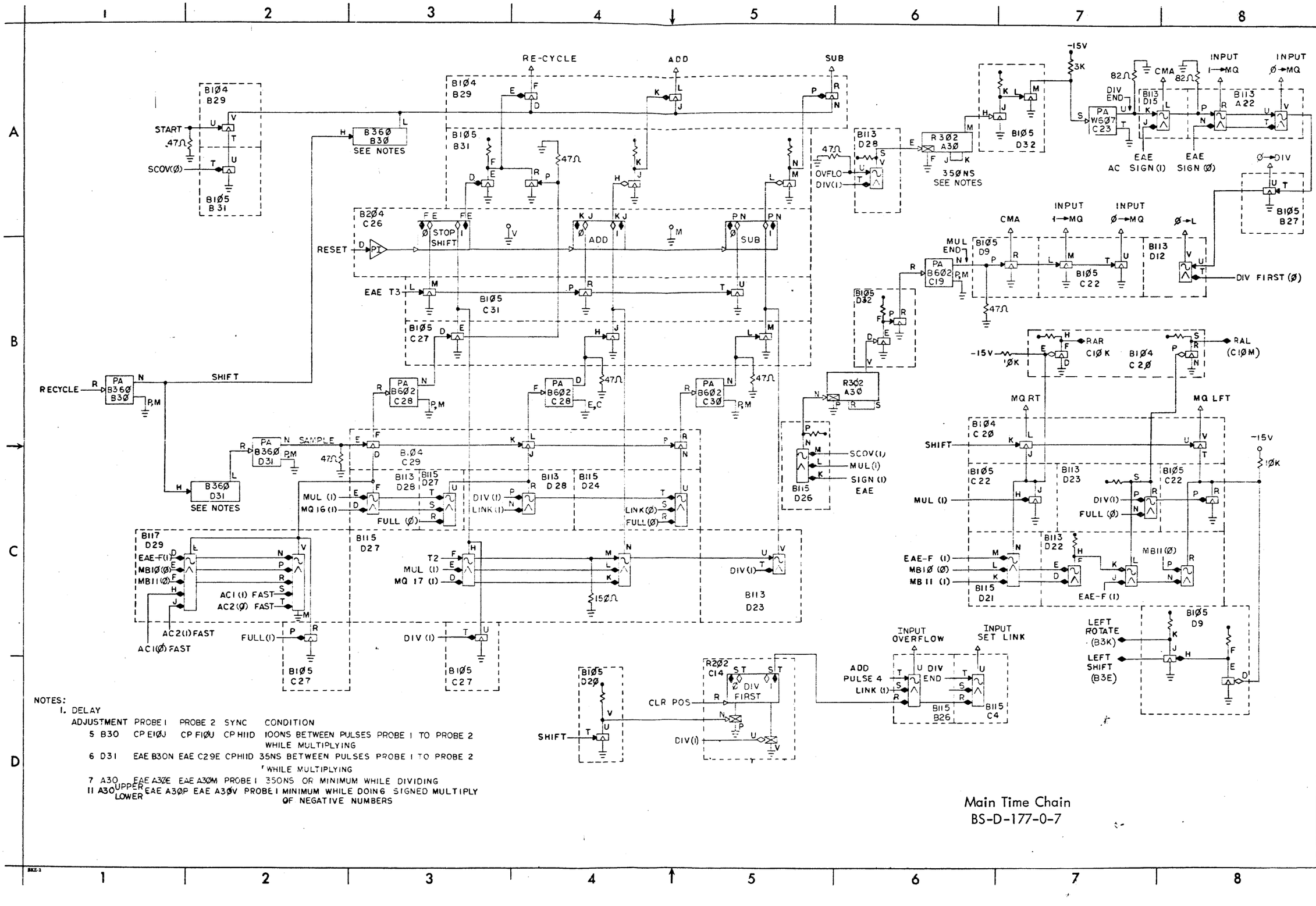
ADDER / SUBTRACTOR

NOTES:

1. DELAY ADJUSTMENT

	PROBE 1	PROBE 2	SYNC	CONDITION
1. A29	CP FIØT	CP FIØU	CP HIID	ICONS BETWEEN LEADING EDGES PROBE 1 TO PROBE 2 WHILE DIVIDING
2. A28	CP FIØU	CP FIØR	CP HIID	ICONS BETWEEN LEADING EDGES PROBE 1 TO PROBE 2 WHILE DIVIDING
3. A35	CP FIØT	CP EIØL	CP HIID	ICONS BETWEEN LEADING EDGES PROBE 1 TO PROBE 2 WHILE DIVIDING
4. A27	EAE A27H	EAEC25S	PROBE 1	ICONS BETWEEN LEADING EDGES PROBE 1 TO PROBE 2 WHILE DIVIDING

EAE Register Control
BS-D-177-0-6

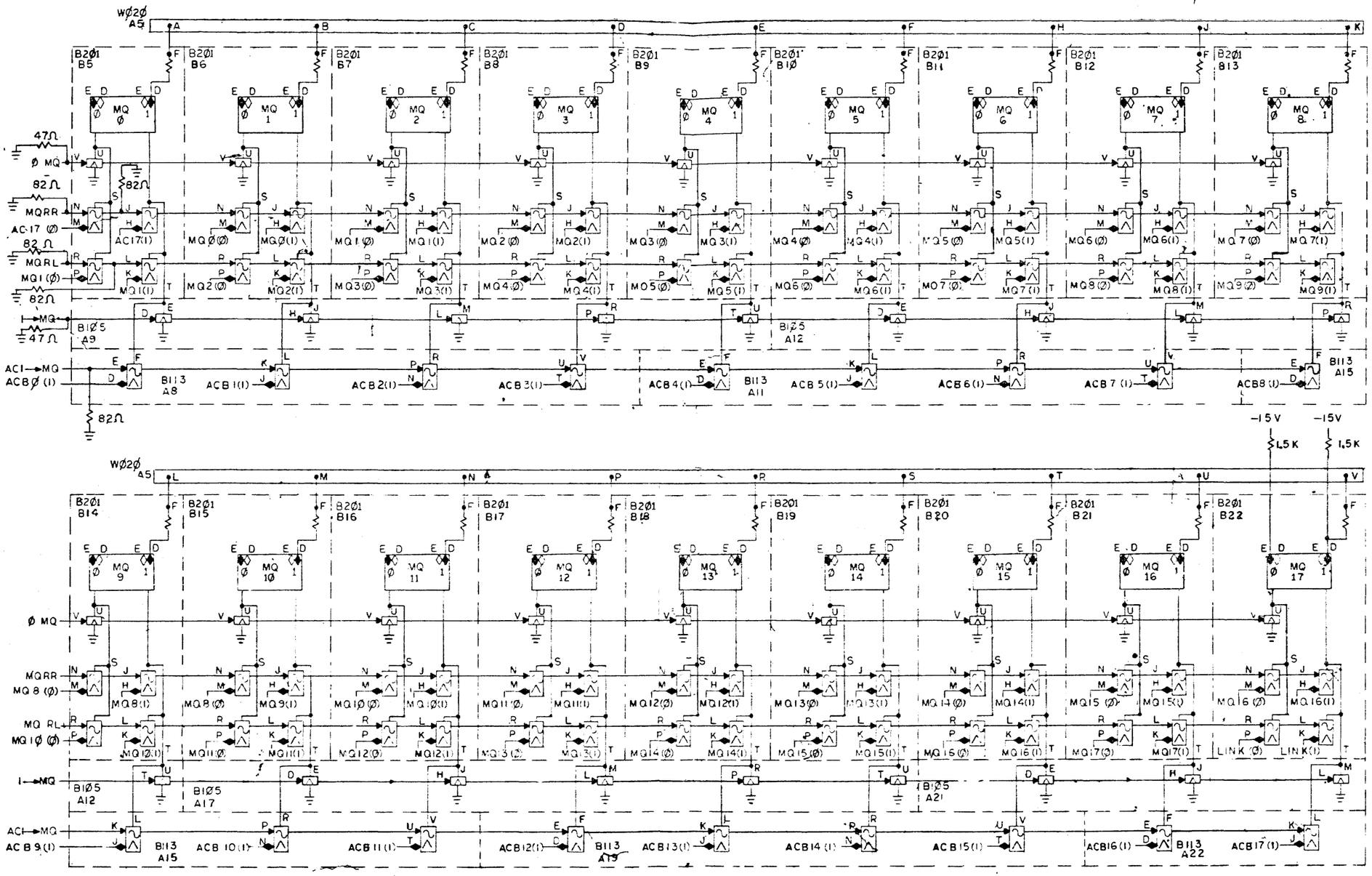


NOTES:

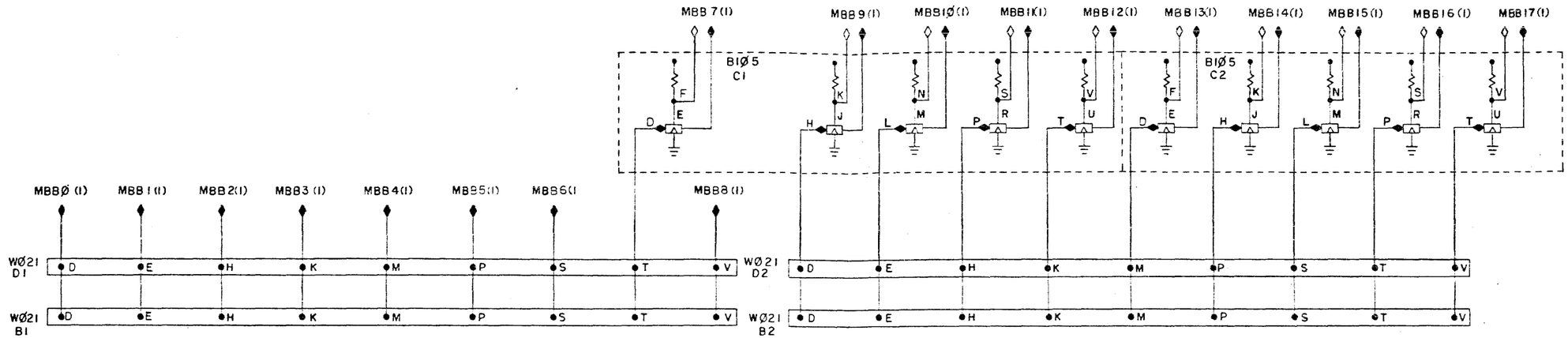
1. DELAY

ADJUSTMENT	PROBE 1	PROBE 2	SYNC	CONDITION
5 B30	CP EIØJ	CP FIØU	CP HIID	100NS BETWEEN PULSES PROBE 1 TO PROBE 2 WHILE MULTIPLYING
6 D31	EAE B30N	EAE C29E	CPHIID	35NS BETWEEN PULSES PROBE 1 TO PROBE 2 WHILE MULTIPLYING
7 A30	EAE A30E	EAE A30M	PROBE 1	350NS OR MINIMUM WHILE DIVIDING
11 A30 UPPER / LOWER	EAE A30P	EAE A30V	PROBE 1	MINIMUM WHILE DOING SIGNED MULTIPLY OF NEGATIVE NUMBERS

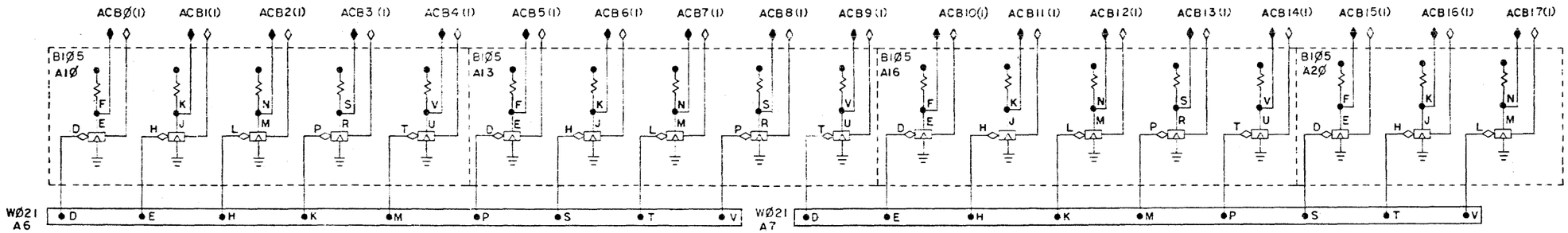
Main Time Chain
BS-D-177-0-7



MQ Register
BS-D-177-0-8



* NOTE:
MBBS ARE SERIES TERMINATED AT DRIVE END.



AC Inverters
BS-D-177-0-9

W021 SIGNAL - CABLE CONNECTORS

EAE CABLE TO ID
LENGTH
2AØ6 → ILO6

ACBØ (Ø)	D
ACBØ1 (Ø)	E
ACBØ2 (Ø)	H
ACBØ3 (Ø)	K
ACBØ4 (Ø)	M
ACBØ5 (Ø)	P
ACBØ6 (Ø)	S
ACBØ7 (Ø)	T
ACBØ8 (Ø)	V

EAE CABLE TO ID
LENGTH
2AØ7 → IMØ6

ACBØ9 (Ø)	D
ACB1Ø (Ø)	E
ACB11 (Ø)	H
ACB12 (Ø)	K
ACB13 (Ø)	M
ACB14 (Ø)	P
ACB15 (Ø)	S
ACB16 (Ø)	T
ACB17 (Ø)	V

MQ INDICATOR
CABLE 2AØ5

MQØØ IND	A
MQØ1 IND	B
MQØ2 IND	C
MQØ3 IND	D
MQØ4 IND	E
MQØ5 IND	F
MQØ6 IND	H
MQØ7 IND	J
MQØ8 IND	K
MQØ9 IND	L
MQ1Ø IND	M
MQ11 IND	N
MQ12 IND	P
MQ13 IND	R
MQ14 IND	S
MQ15 IND	T
MQ16 IND	U
MQ17 IND	V

EAE CHECK OUT
INDICATOR CABLE
2C32

STOP	A
SHIFT	B
ADD	C
SUB	D
EAE F	E
MUL	F
DIV	H
EAE SIGN	J
EAE AC SIGN	K
FULL	L
SCOV	M
SC 12	N
SC 13	P
SC 14	R
SC 15	S
SC 16	T
SC 17	U

EAE SINGLE STEP SW

W020 INDICATOR CABLE CONNECTORS

MB BITS FROM CP
2B01 → IF31

MBBØ (I)	D
MBBØ1 (I)	E
MBBØ2 (I)	H
MBBØ3 (I)	K
MBBØ4 (I)	M
MBBØ5 (I)	P
MBBØ6 (I)	S
MBBØ7 (I)	T
MBBØ8 (I)	V

*1

MB BITS FROM CP
2B01 → IF32

MBBØ9 (I)	D
MBB1Ø (I)	E
MBB11 (I)	H
MBB12 (I)	K
MBB13 (I)	M
MBB14 (I)	P
MBB15 (I)	S
MBB16 (I)	T
MBB17 (I)	V

*

CP CONTROL SIGNALS
FROM EAE
2B03 → IN32

STOP CP TC	D
LEFT SHIFT	E
START CP TC	H
LEFT ROTATE	K
SC1 - AC	M
START MUL, DIV	P
MQ1 - AC	S
MUL, DIV	T
EAE - F (B)	V

*2

EAE CABLES TO DS
2DØ1 → 2AØ1

MBØ (I)	D
MBØ (I)	E
MBØ2 (I)	H
MBØ3 (I)	K
MBØ4 (I)	M
MBØ5 (I)	P
MBØ6 (I)	S
MBØ7 (I)	T
MBØ8 (I)	V

EAE CABLES TO DS
2DØ2 → 2AØ2

MB 9 (I)	D
MB10 (I)	E
MB11 (I)	H
MB12 (I)	K
MB13 (I)	M
MB14 (I)	P
MB15 (I)	S
MB16 (I)	T
MB17 (I)	V

EAE CABLE TO IC (MQ)
2CØ5 → IND

MQ Ø (I)	D
MQØ1 (I)	E
MQØ2 (I)	H
MQØ3 (I)	K
MQØ4 (I)	M
MQØ5 (I)	P
MQØ6 (I)	S
MQØ7 (I)	T
MQØ8 (I)	V

EAE CABLE TO IC (MQ)
2CØ6 → IN2Ø

MQØ9 (I)	D
MQ1Ø (I)	E
MQ11 (I)	H
MQ12 (I)	K
MQ13 (I)	M
MQ14 (I)	P
MQ15 (I)	S
MQ16 (I)	T
MQ17 (I)	V

EAE CABLE TO IC
STEP COUNTER BITS
2CØ7 → IN28

T6	D
SHIFT	E
	H
SC 2 (I)	K
SC13 (I)	M
SC14 (I)	P
SC 15 (I)	S
SC16 (I)	T
SC17 (I)	V

*4

EAE CABLE TO CP
2CØ8 → IF27 (WØ28)

CRY DET	D
T2	E
T3	H
T4	K
T5	M
AC17 (Ø)	P
T7	S
IA3	T
IBI	V

82Ω IN SERIES

EAE CABLE TO CP
2CØ9 → IF28

LINK (I)	D
LINK (Ø)	E
AC1 (I)	H
AC1 (Ø)	K
AC2 (I)	M
AC2 (Ø)	P
MQ Ø (I)	S
MQ Ø (Ø)	T
AC17 (I)	V

47Ω IN SERIES
47Ω IN SERIES

EAE TO CP
(WØ28) 2C1Ø → IF29

CMA	D
CML	E
CRY	H
RAR	K
RAL	M
XOR	P
CLA	S
SET LINK	T
CLR LINK	V

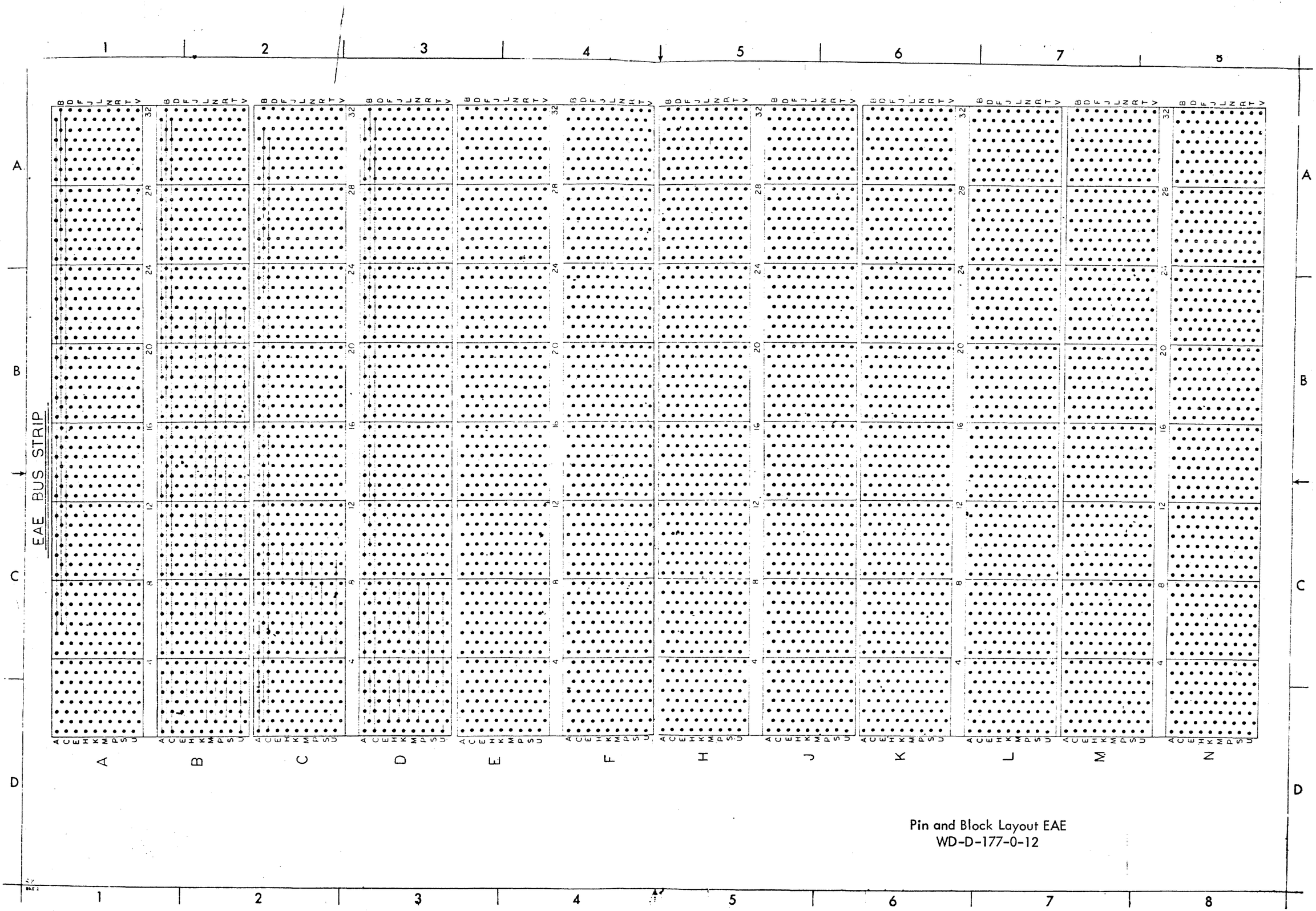
*2
47Ω IN SERIES
47Ω IN SERIES
47Ω IN SERIES

NOTES:

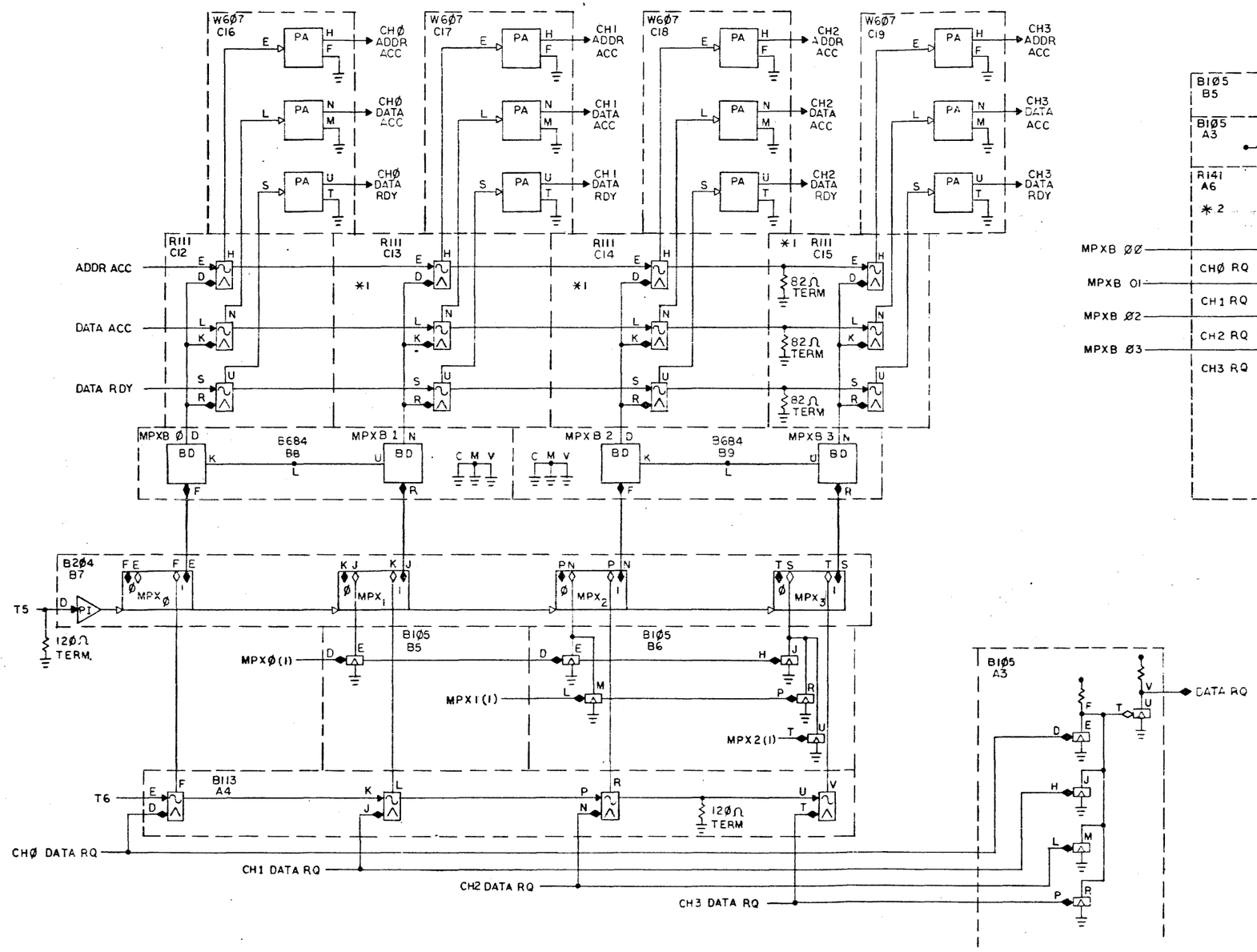
1. CABLE CONNECTOR IS TYPE WØ28 WITH 47 OHM SERIES RESISTORS.
2. REMOVE JUMPER CARD IN CENTRAL PROCESSOR.
3. WHEN EAE IS INSTALLED, THE CABLES GOING TO 2AØ1, 2AØ2 OF THE DEVICE SELECTOR ARE MOVED TO EAE 2BØ1, AND 2BØ2
4. EAE CABLES TO CP WØ28 CONNECTORS WITH SERIES RESISTORS AS SPECIFIED

EAE Cable Schedules
CL-D-177-0-10

EAE BUS STRIP



Pin and Block Layout EAE
WD-D-177-0-12

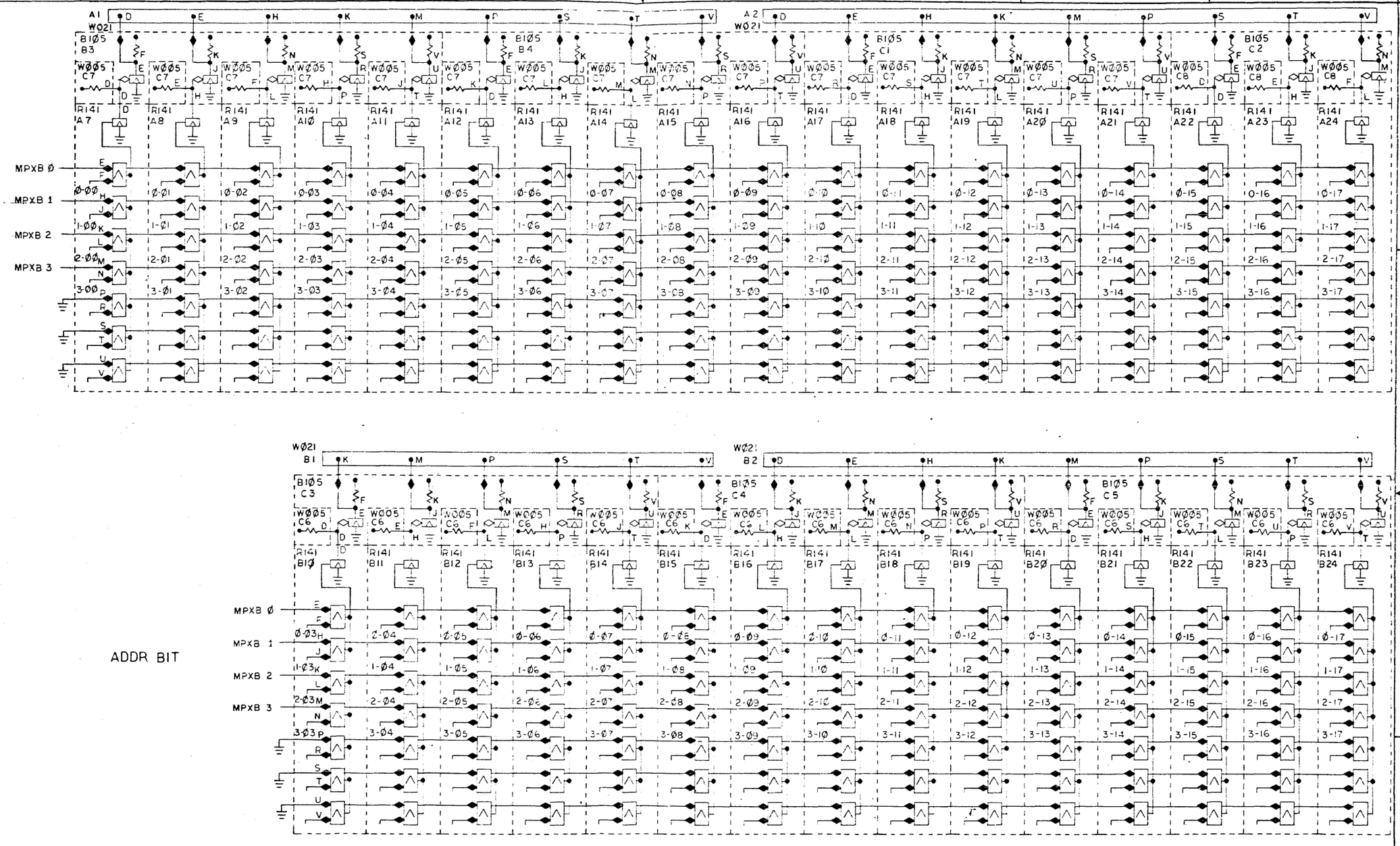


* NOTES
1. PINS E, L & R ON RIII ARE BUSSED
2. A5, A6 ARE BUSSED WITH A7–A24 ON D-173-0-3

Data Interrupt Multiplexer Control
BS-D-173-0-2

DATA BIT

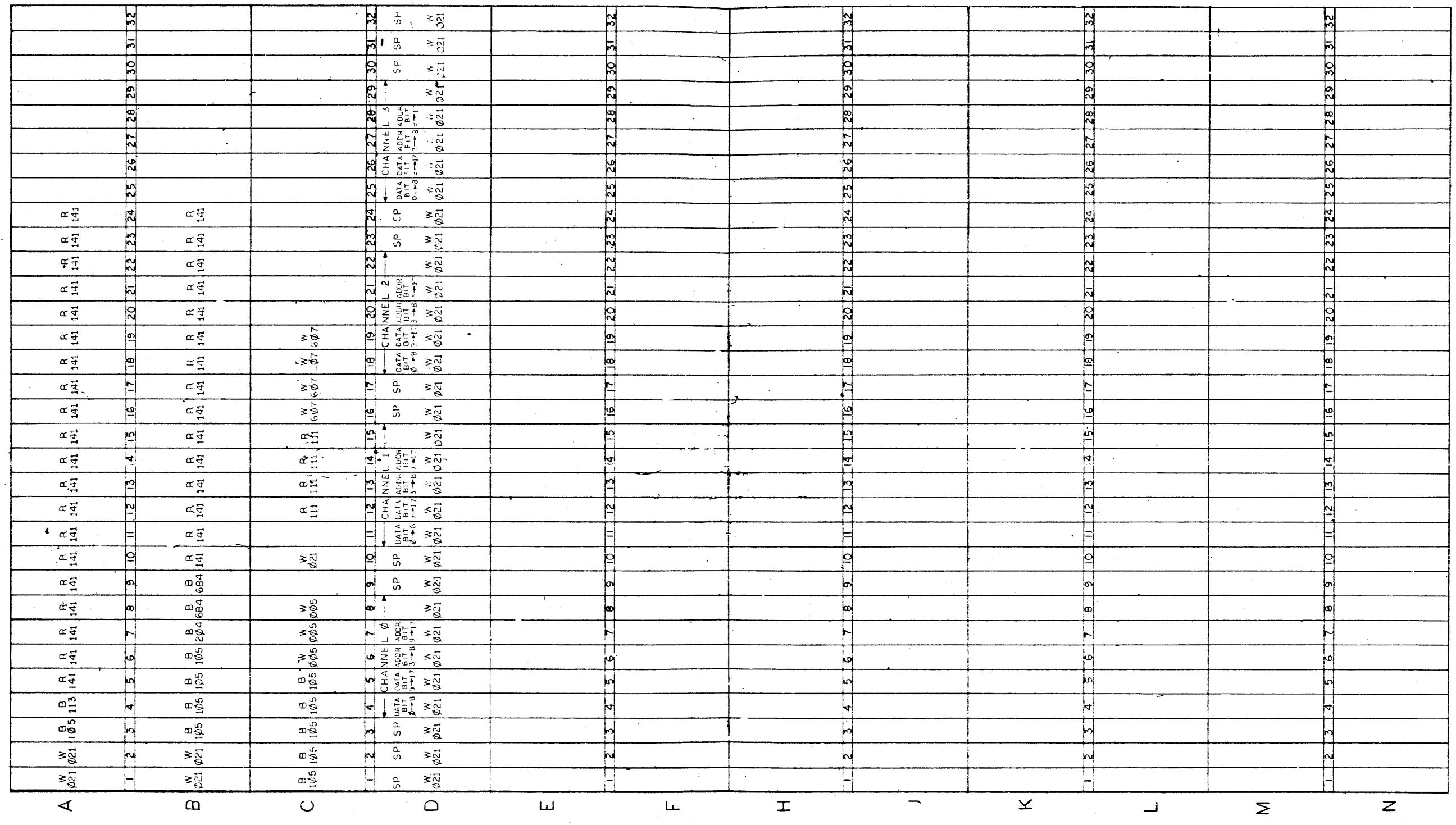
ADDR BIT



NOTE:

1. ALL R141'S ARE PINED AS SHOWN IN A7 & BIØ.
2. PINS E,H,K,M,P,S,U ON R141 ARE BUSSED

Data Interrupt Multiplexer Data Inputs/Data Addresses
BS-D-173-0-3



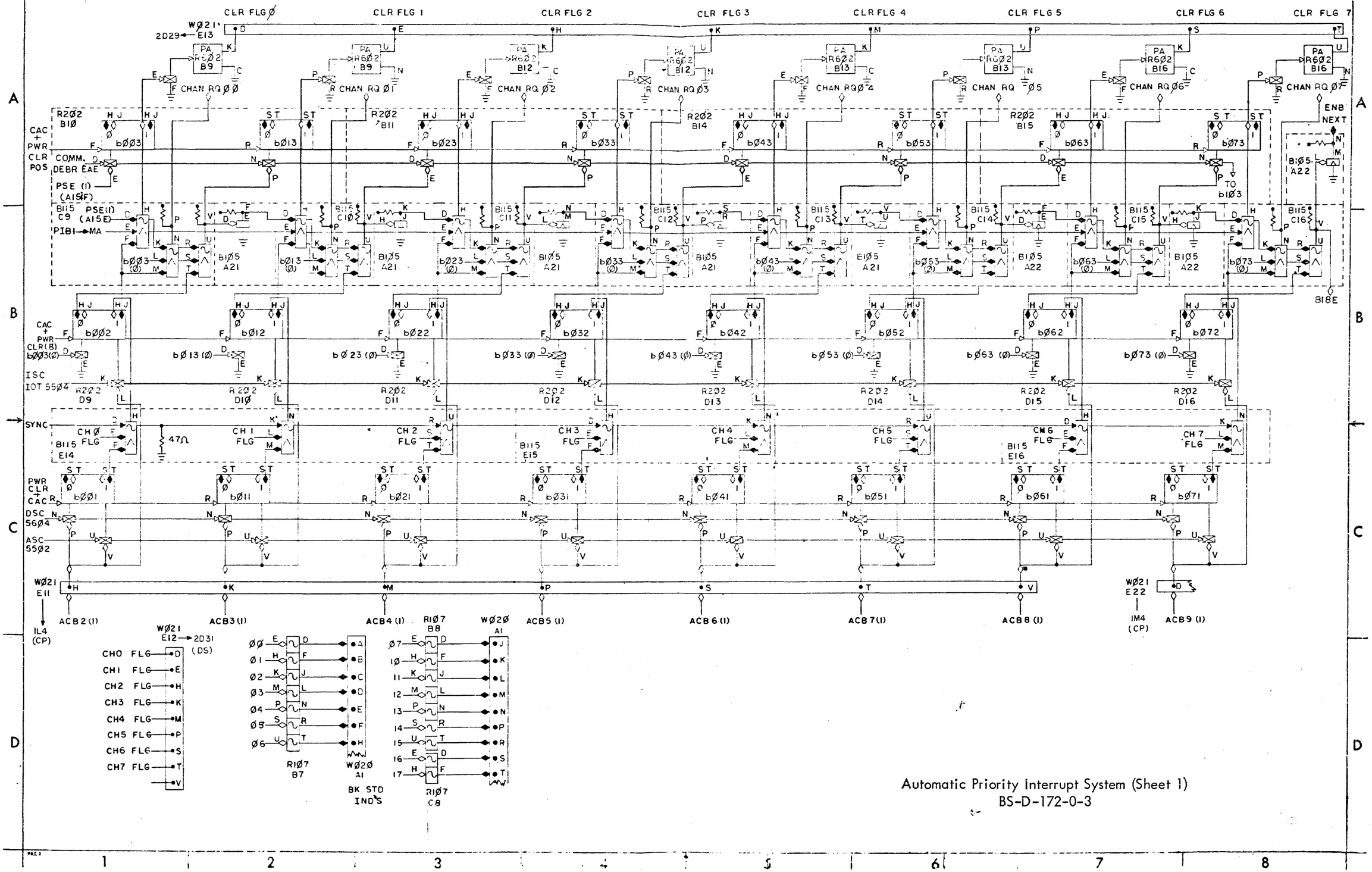
Data Interrupt Multiplexer Module Map
ML-D-173-0-5

Bus Schedule
WD-D-173-0-8

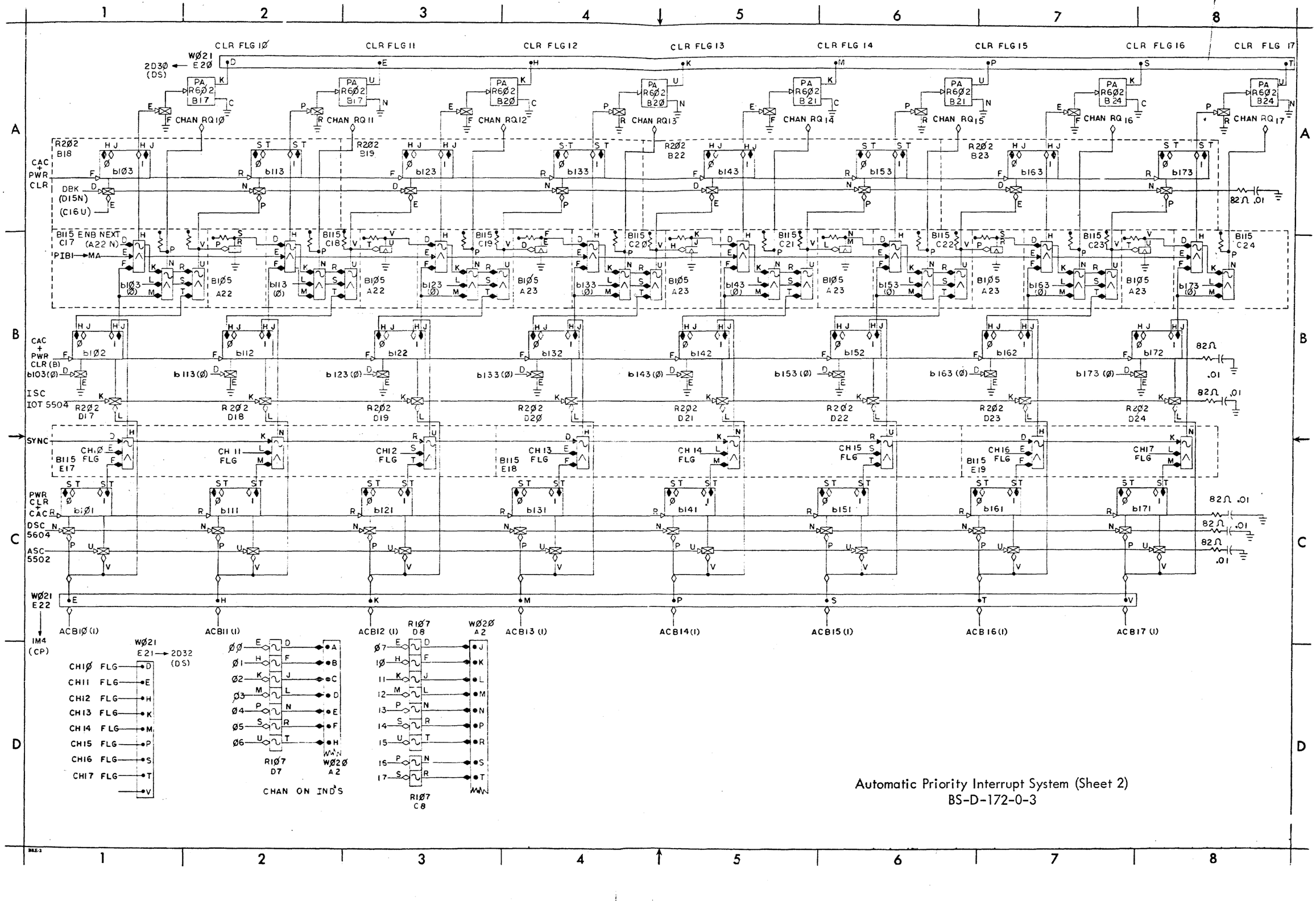
ASSIGNMENT OF MAIN MEMORY LOCATIONS TO CHANNELS

MAIN MEMORY ADDRESS	CHANNEL NUMBER
0040_8	0
0041_8	1
0042_8	2
0043_8	3
0044_8	4
0045_8	5
0046_8	6
0047_8	7
0050_8	10
0051_8	11
0052_8	12
0053_8	13
0054_8	14
0055_8	15
0056_8	16
0057_8	17

Automatic Priority Interrupt Control
BS-D-172-0-2

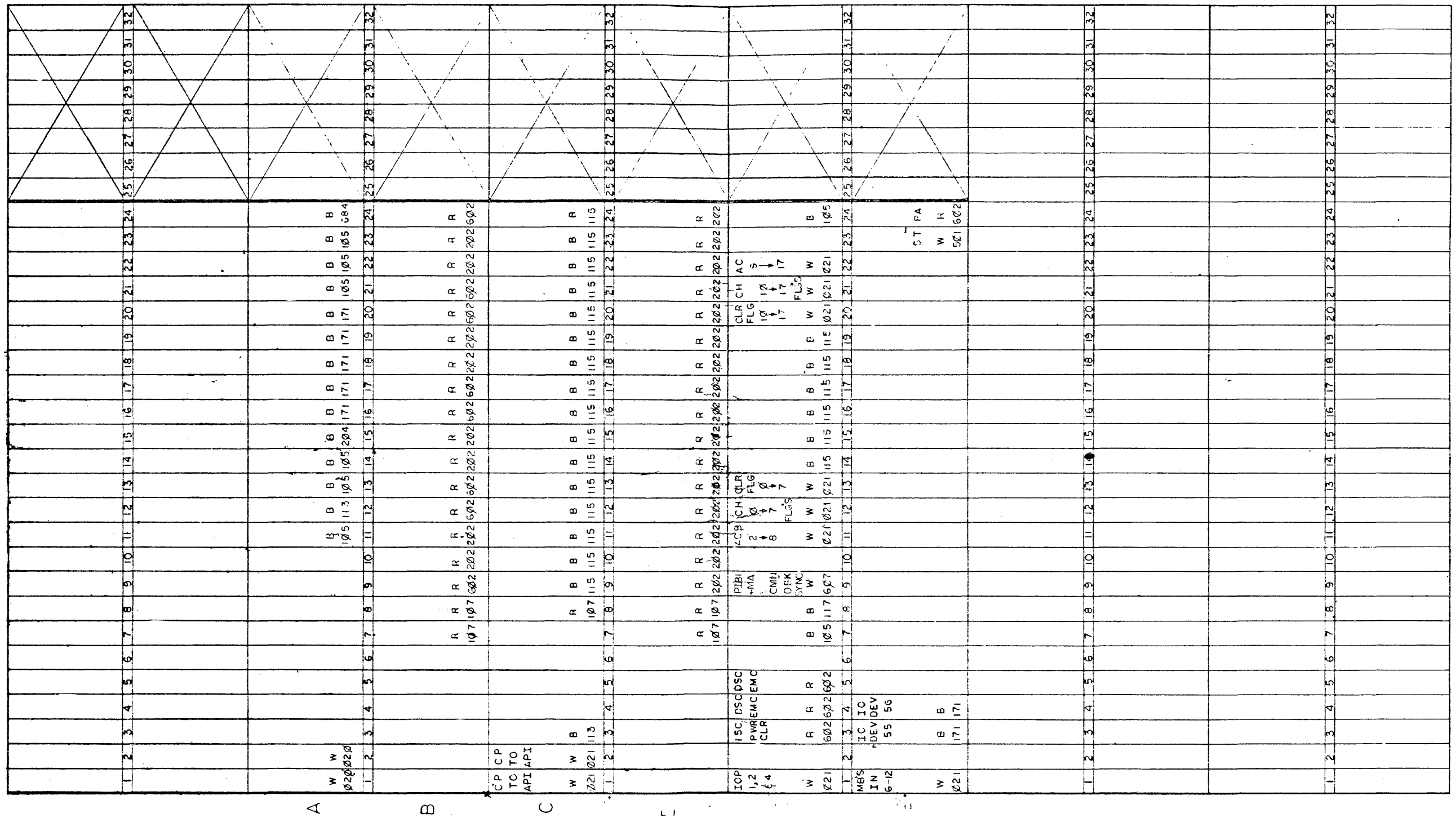


Automatic Priority Interrupt System (Sheet 1)
BS-D-172-0-3



Automatic Priority Interrupt System (Sheet 2)
BS-D-172-0-3

AUTOMATIC PRIORITY
INTERRUPT SYSTEM
BACK DOOR LOGIC



Module Map
ML-D-172-0-5

Pin and Block Layout
WD-D-172-0-6

APPENDIX 1

INSTRUCTION SUMMARY

MEMORY REFERENCE INSTRUCTIONS

Mnemonic Symbol	Octal Code	Machine Cycles	Operation Executed
CAL	00	2	Call subroutine. The address portion of this instruction is ignored. The action is identical to JMS 20.
DAC Y	04	2	Deposit AC. The content of the AC is deposited in the memory cell at location Y.
JMS Y	10	2	Jump to subroutine. The content of the PC and the content of the L is deposited in memory cell Y. The next instruction is taken from cell Y + 1.
DZM Y	14	2	Deposit zero in memory. Zero is deposited in memory cell Y.
LAC Y	20	2	Load AC. The content of Y is loaded into the AC.
XOR Y	24	2	Exclusive OR. The exclusive OR is performed between the content of Y and the content of the AC, with the result left in the AC.
ADD Y	30	2	Add (1's complement). The content of Y is added to the content of the AC in 1's complement arithmetic and the result is left in the AC.
TAD Y	34	2	Two's complement add. The content of Y is added to the content of the AC in 2's complement arithmetic and the result is left in the AC.

MEMORY REFERENCE INSTRUCTIONS (continued)

Mnemonic Symbol	Octal Code	Machine Cycles	Operation Executed
XCT Y	40	1+	Execute. The instruction in memory cell Y is executed.
ISZ Y	44	2	Increment and skip if zero. The content of Y is incremented by one in 2's complement arithmetic. If the result is zero, the next instruction is skipped.
AND Y	50	2	AND. The logical operation AND is performed between the content of Y and the content of the AC with the result left in the AC.
SAD Y	54	2	Skip if AC is different from Y. The content of Y is compared with the content of the AC. If the numbers are different, the next instruction is skipped.
JMP Y	60	1	Jump to Y. The next instruction to be executed is taken from memory cell Y.

EAE INSTRUCTION LIST

Mnemonic Symbol	Octal Code	Operation Executed
EAE	640000	Basic EAE command. No operation.
LRS	640500	Long right shift.
LRSS	660500	Long right shift, signed (AC sign = link).
LLS	640600	Long left shift.
LLSS	660600	Long left shift, signed (AC sign = L).
ALS	640700	Accumulator left shift.
ALSS	660700	Accumulator left shift, signed (AC sign = L).

EAE INSTRUCTION LIST (continued)

Mnemonic Symbol	Octal Code	Operation Executed
NORM	640444	Normalize, unsigned. Maximum shift is 44_8.
NORMS	660444	Normalize, signed (AC sign = L).
MUL	653122	Multiply, unsigned. The number in the AC is multiplied by the number in the next core memory address.
MULS	657122	Multiply, signed. The number in the AC is multiplied by the number in the next core memory address.
DIV	640323	Divide, unsigned. The 36-bit content of both the AC and MQ is divided by the number in the next core memory location.
DIVS	644323	Divide, signed. The content of both the AC and MQ as a 1's complement signed number is divided by the number in the next core memory location.
IDIV	653323	Integer divide, unsigned. Divide the number in the AC as an 18-bit unsigned integer by the number in the next core memory location.
IDIVS	657323	Integer divide, signed. Same as IDIV but the content of the AC is a 17-bit signed number.
FRDIV	650323	Fraction divide, unsigned. Divide the 18-bit fraction in the AC by the 18-bit fraction in the number in the next core memory location.
FRDIVS	654323	Fraction divide, signed. Same as FRDIV, but the content of the AC is a 17-bit signed number.
LACQ	641002	Replace the content of the AC with the content of the MQ.
LACS	641001	Replace the content of the AC with the content of the SC.
CLQ	650000	Clear MQ.

EAE INSTRUCTION LIST (continued)

Mnemonic Symbol	Octal Code	Operation Executed
ABS	644000	Place absolute value of AC in the AC.
GSM	664000	Get sign and magnitude. Places AC sign in the link and takes the absolute value of AC.
OSC	640001	Inclusive OR the SC into the AC.
OMQ	640002	Inclusive OR AC with MQ and place results in AC.
CMQ	640004	Complement the MQ.
LMQ	652000	Load MQ

INPUT/OUTPUT TRANSFER INSTRUCTIONS

Mnemonic Symbol	Octal Code	Operation Executed
		Program Interrupt
IOF	700002	Interrupt off. Disable the PIC.
ION	700042	Interrupt on. Enable the PIC.
ITON	700062	Interrupt and trap on. Enable PIC and trap mode.
		Real Time Clock
CLSF	700001	Skip the next instruction if the clock flag is set to 1.
CLOF	700004	Clear the clock flag and disable the clock.
CLON	700044	Clear the clock flag and enable the clock.
		Perforated Tape Reader
RSF	700101	Skip if reader flag is a 1.

INPUT/OUTPUT TRANSFER INSTRUCTIONS (continued)

Mnemonic Symbol	Octal Code	Operation Executed
		Perforated Tape Reader (continued)
RCF	700102	Clear reader flag, then inclusively OR the content of reader buffer into the AC.
RRB	700112	Read reader buffer. Clear reader flag and AC, and then transfer content of reader buffer into AC.
RSA	700104	Select reader in alphanumeric mode. One 8-bit character is read into the reader buffer.
RSB	700144	Select reader in binary mode. Three 6-bit characters are read into the reader buffer.
		Perforated Tape Punch
PSF	700201	Skip if the punch flag is set to 1.
PCF	700202	Clear the punch flag.
PSA or PLS	700204 700206	Punch a line of tape in alphanumeric mode.
PSB	700244	Punch a line of tape in binary mode.
		I/O Equipment
I/ORS	700314	Input/output read status. The content of given flags replace the content of the assigned AC bits.
TTS	703301	Test Teletype and skip if KSR 33 is connected to computer.
CAF	703302	Clear all flags.
SKP7	703341	Skip if processor is a PDP-7.

INPUT/OUTPUT TRANSFER INSTRUCTIONS (continued)

Mnemonic Symbol	Octal Code	Operation Executed
		Teletype Keyboard
KSF	700301	Skip if the keyboard flag is set to 1.
KRB	700312	Read the keyboard buffer. The content of the buffer is placed in AC10-17 and the keyboard flag is cleared.
		Teletype Teleprinter
TSF	700401	Skip if the teleprinter flag is set.
TCF	700402	Clear the teleprinter flag.
TLS	700406	Load teleprinter buffer. The content of AC10-17 is placed in the buffer and printed. The flag is cleared before transmission takes place and is set when the character has been printed.
		Automatic Priority Interrupt
CAC	705501	Clear all channels. Turn off all channels.
ASC	705502	Enable selected channel(s). AC2-17 are used to select the channel(s).
DSC	705604	Disable selected channel(s). AC2-17 are used to select the channel(s).
EPI	700044	Enable automatic priority interrupt system.
DPI	700004	Disable automatic priority interrupt system.
ISC	705504	Initiate break on selected channel (for maintenance purposes). AC2-17 are used to select the channel.
DBR	705601	Debreak. Return highest priority channel to receptive state.

INPUT/OUTPUT TRANSFER INSTRUCTIONS (continued)

Mnemonic Symbol	Octal Code	Event Time	Operation Executed
			Memory Extension Control
SEM	707701		Skip if in extend mode.
EEM	707702		Enter extend mode.
LEM	707704		Leave extend mode.
EMIR	707742		Extend mode interrupt restore.

OPERATE INSTRUCTIONS

Mnemonic Symbol	Octal Code	Event Time	Operation Executed
OPR or NOP	740000	---	Operate group or no operation. Causes a 1-cycle program delay.
CMA	740001	3	Complement accumulator. Each bit of the AC is complemented.
CML	740002	3	Complement link.
OAS	740004	3	Inclusive OR ACCUMULATOR switches. The word set into the ACCUMULATOR switches is OR combined with the content of the AC, the result remains in the AC.
RAL	740010	3	Rotate accumulator left. The content of the AC and L are rotated one position to the left.
RLR	740020	2	Rotate accumulator right. The content of the AC and L are rotated one position to the right.
HLT	740040	---	Halt. The program is stopped at the conclusion of the cycle.
SMA	740100	1	Skip on minus accumulator. If the content of the AC is negative (2's complement) number the next instruction is skipped.

OPERATE INSTRUCTIONS (continued)

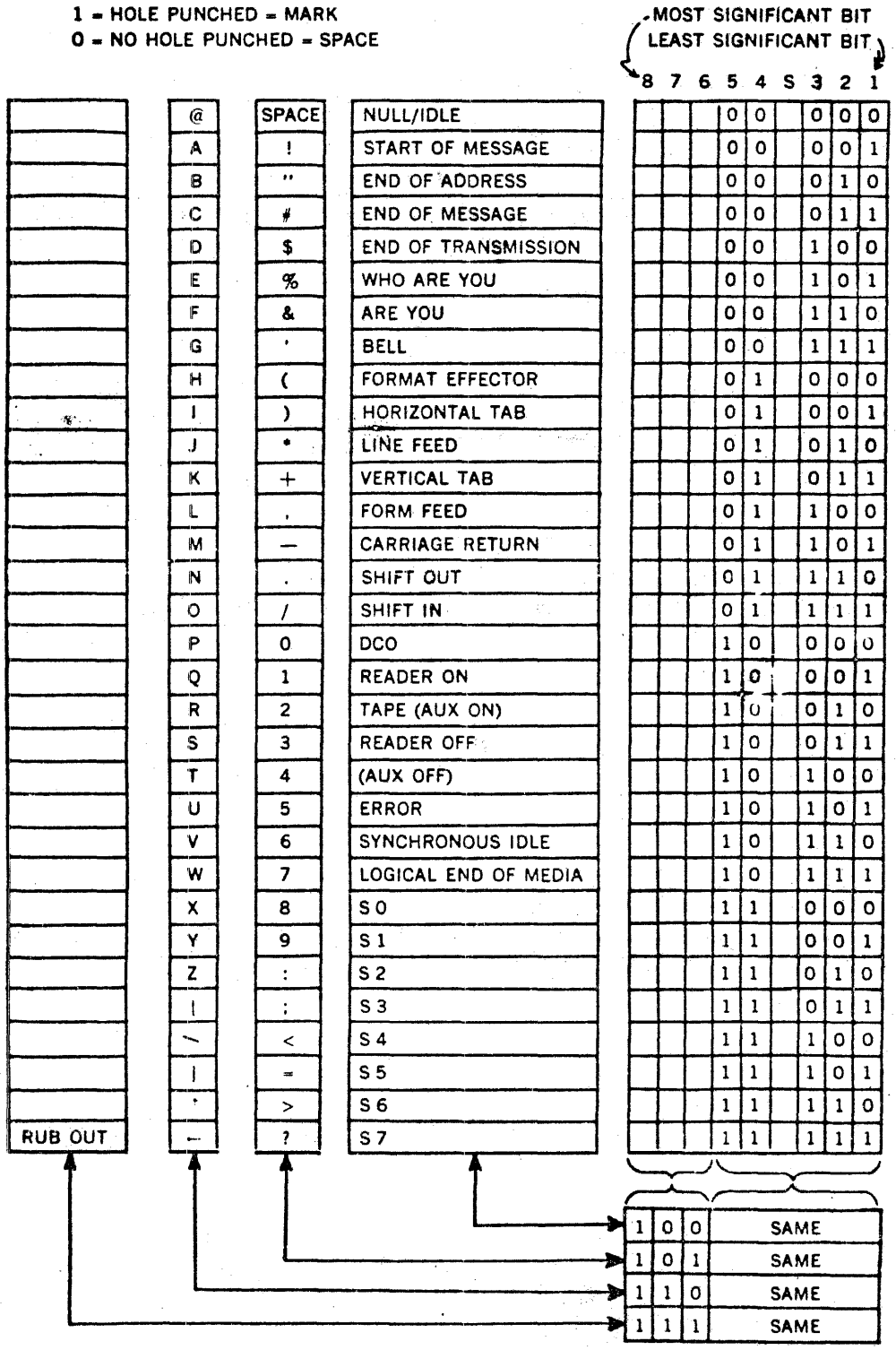
Mnemonic Symbol	Octal Code	Event Time	Operation Executed
SZA	740200	1	Skip on zero accumulator. If the content of the AC equals zero (2's complement), the next instruction is skipped.
SNL	740400	1	Skip on non-zero link. If the L contains a 1, the next instruction is skipped.
SKP	741000	1	Skip. The next instruction is unconditionally skipped.
SPA	741100	1	Skip on positive accumulator. If the content of the AC is zero (2's complement) or a positive number, the next instruction is skipped.
SNA	741200	1	Skip on non-zero accumulator. If the content of the AC is not zero (2's complement), the next instruction is skipped.
SZL	741400	1	Skip on zero link. If the L contains a 0, the next instruction is skipped.
RTL	742010	2,3	Rotate two left. The content of the AC and the L are rotated two positions to the left.
RTR	742020	2,3	Rotate two right. The content of the AC and the L are rotated two positions to the right.
CLL	744000	2	Clear link. The L is cleared.
STL	744002	2,3	Set link. The L is set to 1.
RCL	744010	2,3	Clear link, then rotate left. The L is cleared, then the L and AC are rotated one position left.
RCR	744020	2,3	Clear link, then rotate right. The L is cleared, then the L and AC are rotated one position right.
CLA	750000	2	Clear accumulator. Each bit of the AC is cleared.

OPERATE INSTRUCTIONS (continued)

Mnemonic Symbol	Octal Code	Event Time	Operation Executes
CLC	750001	2,3	Clear and complement accumulator. Each bit of the AC is set to contain a 1.
LAS	750004	2,3	Load accumulator from switches. The word set into the ACCUMULATOR switches is loaded into the AC.
GLK	750010	2,3	Get link. The content of L is set into AC17.
LAW N	76XXXX	---	Load the AC with LAW N.

APPENDIX 2

MODEL 33ASR/KSR TELETYPE CODE (ASCII) IN BINARY FORM



APPENDIX 3

SIGNAL GLOSSARY

The following is a list of the signals used on the engineering drawings for the PDP-7. Each signal is listed in alphanumerical order and the number of the drawing in which it originates is listed in the adjacent column to the right.

Signal	Engineering Drawing Number
AC≠0	BS-D-7-0-26
AC=0	BS-D-7-0-26
AC0(0) through AC8(0)	BS-D-7-0-31, sheet 1
AC0(1) through AC8 (1)	BS-D-7-0-31, sheet 1
AC9(0) through AC17(0)	BS-D-7-0-31, sheet 2
AC9(1) through AC17(1)	BS-D-7-0-31, sheet 2
AC1→ MB	BS-D-7-0-25
ACB0(1) through ACB17 (1)	BS-D-7-0-34
AC0 E2U and AC17 E19U	BS-D-7-0-32
ACS1→ AC	BS-D-7-0-26
AC CRY ADD OV	BS-D-7-0-26
ALPHA and ALPHA-N	BD-D-444B-0-2
ASC 5502	BS-D-172-0-2
ASI→ PC	BS-D-7-0-25
B	BS-D-7-0-24
B SET	BS-D-7-0-24
$\overline{\text{B SET}}$	BS-D-7-0-24
BGN	BS-D-7-0-22
BGN (B)	BS-D-7-0-20
BINARY and $\overline{\text{BINARY}}$	BD-D-444B-0-2
BK RQ Pos	BS-D-7-0-32
BK RQ Neg	BS-D-7-0-32
$\overline{\text{BK RQ}}$ Pos	BS-D-7-0-32
$\overline{\text{BK RQ}}$ Neg	BS-D-7-0-32
C AC	BS-D-7-0-26
CAL and $\overline{\text{CAL}}$	BS-D-7-0-25
CHAN RQ 00 through CHAN RQ 07	BS-D-172-0-3, sheet 1
CHAN RQ 08 through CHAN RQ 17	BS-D-172-0-3, sheet 2
CH17 FLG	BS-D-172-0-2

Signal	Engineering Drawing Number
CLK COUNT RQ (0) CLK COUNT RQ (1) CLK ENABLE (0) CLK ENABLE (1) CLK (0) CLK (1) CLK SYNC (0) CLK SYNC (1) CLOCK 7→ MA	BS-D-7-0-32
CLR FLGS	BS-D-75D-0-2
CLR FLG 0 through CL FLG 7	BS-D-172-0-3, sheet 1
CLR FLG 8 through CLR FLG 17	BS-D-7-0-3, sheet 2
COMMON DEBREAK	BS-D-172-0-2
$\overline{\text{CONT}}$	BS-D-7-0-20
D D SET $\overline{\text{D SET}}$	BS-D-7-0-24
DATA ADDR→MA	BS-D-7-0-32
DATA·B	BS-D-173-0-2
DATA·B Pos and DATA·B Neg	BS-D-7-0-32
DATA IN	BS-D-173-0-2
DATA INFO→MB	BS-D-7-0-32
DATA RQ	BS-D-173-0-2
DATA SYNC (0) and DATA SYNC (1)	BS-D-7-0-32
DSC 5604	BS-D-172-0-2
DBK	BS-D-172-0-2
DP+DN	BS-D-7-0-20

Signal	Engineering Drawing Number
E E·JMP+PROG B E SET $\overline{\text{E SET}}$ E·XCT	BS-D-7-0-24
E·AND E·SAD E·ADD E·TAD E·LAC E·IA1	BS-D-7-0-26
E·ISZ·$\overline{\text{INT REC}}$ (PC+1)	BS-D-172-0-2
ENB NEXT	BS-D-172-0-3, sheet 1
END CRY	BS-D-7-0-26
EX+EN and EX+EN+DP+DPN	BS-D-7-0-20
EXD SW and EXD(1)	WD-D-7-0-37
F F SET $\overline{\text{F SET}}$	BS-D-7-0-24
FLAG FOR (CHANNEL 16)	BS-D-172-0-24
FLG IND	BS-D-444B-0-2
IA0 through IA3 $\overline{\text{IA3}}$ IB0 through IB3	BS-D-7-0-24

Signal	Engineering Drawing Number
IC10(1) through IC17(1)	BS-D-649-0-2
ILL HLT and ILL XCT	BS-D-7-0-23
INH and INH(B)	BS-D-7-0-27
INSURE DEBREAK	BS-D-172-0-2
INT RQ	BS-D-172-0-2
IOP 1 IOP 2 IOP 4	BS-D-7-0-22
I/O SKP	BS-D-7-0-32
IOT and IOT CLA	BS-D-7-0-23
IOT XX01 IOT XX02 IOT XX04	BS-D-7-0-36
Note: XX may be 00 through 76	
I/O TRAP (1) and I/O TRAP (1)B	BS-D-7-0-23
ISC 5504	BS-D-172-0-2
HLT	BS-D-7-0-23
HOLE 7	BD-D-444B-0-2
HOLE 8P	BD-D-444B-0-2
INT RECOGNIZED (0) and INT RECOGNIZED (1)	BS-D-172-0-2
IOT (DBR) and IOT 5601	BS-D-172-0-2

Signal	Engineering Drawing Number
JMP	BS-D-7-0-24
KEY MANUAL	BS-D-7-0-20
KSR 33 DRIVER	BS-D-649-0-2
LINK (1) and LINK (0)	BS-D-7-0-26
LUI ACTIVE LUI CLOCK LUI FLAG LUO ACTIVE LUO CLOCK LUO FLAG	BS-D-649-0-2
MA1→PC	BS-D-7-0-25
MA3(0) through MA17(0) and MA3(1) through MA17(1)	BS-D-7-0-29
MA12 IA and MA14 IA through MA17 IA	BS-D-172-0-2
MB0(1) through MB17(1)	BS-D-7-0-30
MB0→AC	BS-D-7-0-26
MB1→MA and MB1→PC	BS-D-7-0-25
MB INFO→OUT	BS-D-7-0-32
MBB0(0) through MBB17(0) and MBB0(1) through MBB17(1)	BS-D-7-0-28

Signal	Engineering Drawing Number
MB STB INH	BS-D-7-0-25
MOTOR START (SCR)	BS-D-75D-0-2
MPX B SEL 0 through MPX B SEL 3 and MPX 0 through MPX 3	BS-D-173-0-2
OP 1 and OP 2	BS-D-7-0-26
OP LAW OPR OP SKP $\overline{\text{OP SKP}}$ OP SKP EN $\overline{\text{OP SKP EN}}$	BS-D-7-0-26
OVERFLOW FLAG (0) and OVERFLOW FLAG (1)	BS-D-172-0-2
PB10 (0) through PB17 (0) and PB10 (1) through PB17 (1)	BS-D-75D-0-2
PC1→ MA and PC1→ MB	BS-D-7-0-23
PC3(0) through PC17(0) and PC3(1) through PC17(1)	BS-D-7-0-29
PIE(0) and PIE(1)	BS-D-7-0-32
POV(1)	BS-D-7-0-26
PROG·B PROG RQ PROG SYNC (0) PROG SYNC (1)	BS-D-7-0-32
PSE	BS-D-172-0-2
PUN ACTIVE (0) PUN ACTIVE (1) PUN DONE PUN FLAG (0) PUN FLAG (1) PUN GO PUN READY PUN RQ PUN SYNC L	BS-D-75D-0-2
PWR CLR PWR CLR Pos PWR CLR Neg	BS-D-7-0-20
PWR CLR+CAC	BS-D-172-0-2
PWR CLR (P) and PWR CLR (N)	BS-D-75D-0-2
PIB1→ MA	BS-D-177-0-2
RAR and RAL	BS-D-7-0-26
RB0(1) through RB17(1) RD1 (0) RD1 (1) RD2 (0) RD2 (1) RD FLAG (0) RD FLAG (1)	BD-D-444B-0-2

Signal	Engineering Drawing Number
RD MODE (0) RD MODE (1) RD RUN (0) RD RUN (1) RD SHIFT 1 RD SHIFT 2 RD STRB	BD-D-444B-0-2
READ 1 (1) READ (2) READ (2)B	BS-D-7-0-27
READ IN	BS-D-7-0-20
REPEAT	BS-D-7-0-20
REQUEST SLOW CYCLE	(from any slow I/O device)
RPT (1) RPT (0) RPT (1)B	BS-D-7-0-23
RUN (B) TO IND	BS-D-444B-0-2
RUN (1) and RUN (1)B	BS-D-7-0-23
RUN STOP	BS-D-7-0-20
SA0 through SA17	BS-D-149-0-45
SEL-RRB IMIIMI and SEL-RSB IMIIMI	BS-D-7-0-25
SEL 0 SEL 1 SEL 0 READ (1)B SEL 0 WRITE (1)B SEL 1∧READ (1)B SEL 1∧WRITE (1)B SEL 2∧READ (1)B SEL 2∧WRITE (1)B SEL 3∧READ (1)B SEL 3∧WRITE (1)B	BS-D-7-0-27
SELECT 0 and SELECT 1	BS-D-149-0-45
SLOW CYC Pos SLOW CYC Neg SLOW CYC Pos SLOW CYC Neg	BS-D-7-0-23
SP0 through SP4	BS-D-7-0-22
START and START K	BD-D-444B-0-2
START+CONT and START·EX+DP	BS-D-7-0-20
STROBE RETURN	BS-D-149-0-45
STB RETURN	BS-0-7-0-20
SYNC	BS-D-177-0-2
T1 through T7	BS-D-7-0-22
T5-D	BS-D-7-0-32
TAD CRY	BS-D-7-0-26
TAPE FEED	BS-D-750-0-2
TP1 through TP7 and TP7 INVTD	BS-D-7-0-22
TP2 SEL 0, 1 and TP2 SEL 2, 3.	BS-D-7-0-27
TRAP and TRAP (1)	WD-D-7-0-37

Signal	Engineering Drawing Number	Signal	Engineering Drawing Number
WRITE (2) and WRITE (2)B	BS-D-7-0-27	20→MA	BS-D-7-25
XOR→AC	BS-D-7-0-26	3301, 3302, 3304	BS-D-7-0-36
0→AC	BS-D-7-0-26	7001, 7002, 7004 through 7701, 7702, 7704	BS-D-7-0-36
0→MA, 0→MB, 0→PC, +1→MB	BS-D-7-0-25		
+1→PC	BS-D-7-0-23, BS-D-7-0-25		
0101, 0102, 0104 through 0401, 0402, 0404	BS-D-7-0-36		