PDP-15
VT15 GRAPHIC PROCESSOR
MAINTENANCE MANUAL

DIGITAL   EQUIPMENT   CORPORATION   •   MAYNARD,   MASSACHUSETTS

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FOREWORD

The VT15 Graphic Display Processor Maintenance Manual is part of a two volume set. Volume 1 is a basic description of the VT15 Graphic Processor system and related logic circuits; Volume 2 is a complete engineering drawing set for the VT15 Graphic Processor.

This publication consists of six chapters that cover the following general topics:

Chapter 1 consists of a general description, functional and physical characteristics, options, terminology, etc.

Chapter 2 consists of a variety of installation procedures, for example: unpacking, initial setup, power-up, diagnostic programs, etc.

Chapter 3 contains a detailed description of the operation of the VT15 Graphic Processor to the functional group level.

Chapter 4 is a discussion of instruction flow analyses.

Chapter 5 contains a detailed description of the special modules contained in the VT15 Graphic Processor system.

Chapter 6 consists of maintenance procedures for the VT15 Graphic Processor. A variety of topics are discussed including diagnostic programming, preventive maintenance, mechanical and electrical checks, and troubleshooting.

Additional reference documents and programs supplied with the Graphic-15 Display System or previously with the PDP-15 computer are as follows:

Reference Documents

Document No.	Title	Source
042 00370 AKO	Logic Handbook	DEC
142 00970 APH	Control Handbook	DEC
DEC-15-GWSB-D	Graphic-15 Reference Manual	DEC
DEC-15-H2DA-D	PDP-15 Users Handbook	DEC
DEC-15-H2AB-D	PDP-15 Installation Manual	DEC
DEC-15-BRZA-D	PDP-15 Reference Manual	DEC
DEC-15-HOAB-D	PDP-15 Interface Manual	DEC
DEC-15-H2EA-D	PDP-15 Module Manual	DEC
DEC-15-H2GB-D	VT04/VT07 Graphic Display Console Maintenance Manual	DEC

Maintenance Programs

Document No.	Description
MainDEC-15-DAVTB	Display Instruction Test (VT15 IT) Part 1
MainDEC-15-DAVTA	Display Instruction Test (VT15 IT) Part 2 (Manual Intervention Test)
MainDEC-15-D6DD	Display Visual Test (VT15 VT)
MainDEC-15-D6EC	Little Pictures Test (VT15 LP)

CHAPTER 1
VT15 BASIC DESCRIPTION

This manual is one of two documents related to the VT15 Graphic Display Processor (see Figure 1-1).
The VT15 Graphic Processor and a Graphic Display Console comprise the Graphic-15 Display System.
This manual provides a basic understanding of VT15 Graphic Processor operation and capabilities and
assumes that the user is familiar with the technology of the PDP-15 Computer and similar systems. For
a complete list of maintenance program documents for the PDP-15 Programmed Data Processor and the
Graphic-15 Display System, the user should refer to the list provided in the Foreword of this manual.
In-depth operation and programming information for the Graphic-15 Display System is contained in
the Graphic-15 Reference Manual.

1.1 PURPOSE AND SCOPE

Installation, operation, maintenance, and troubleshooting information for the VT15 Graphic Processor
is provided in Volumes 1 and 2 of this manual. Volume 1 describes the basic VT15 Graphic Processor
system and discusses the logic circuits in terms of the program instruction repertoire at the functional
group level; modules that are unique to the VT15 are described and discussed in greater detail.
Volume 2 contains a complete set of engineering drawings for the VT15 Graphic Processor.

1.2 FUNCTIONAL DESCRIPTION

The VT15 Graphic Processor is an 18-bit, general-purpose, graphic processor, which, combined with
the PDP-15 Programmed Data Processor and a display console, comprises the total, basic Graphic-15
Display System (see Figure 1-2).

The VT15 provides the digital-to-analog interface between the PDP-15 Computer and the display con-
sole; this interface accelerates the exchange of instructions and data between the user, the PDP-15
Computer, and the display console. The VT15 interacts with the PDP-15 through the system hardware
to display immediate solutions to a broad range of complex electrical, physical, and mechanical
design and analysis problems.
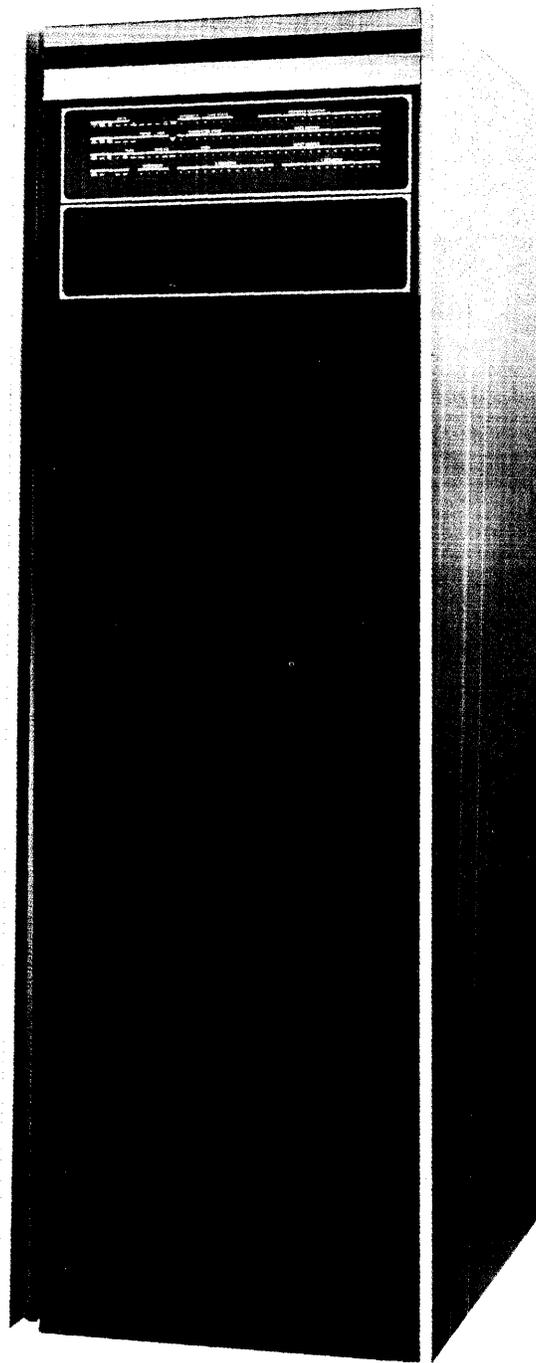
Figure 1-1   VT15 Graphic Processor

*Keyboard in display console
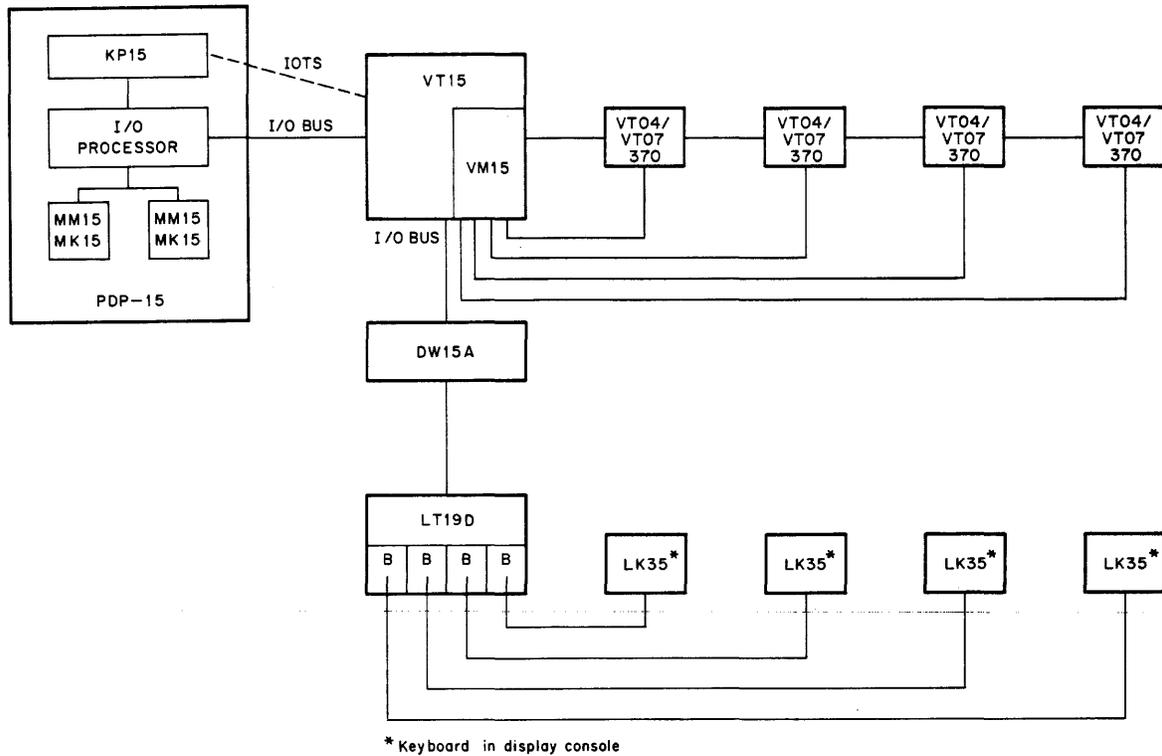
15-0252

Figure 1-2   Graphic-15 Display System Interconnect Diagram

Because the VT15 and PDP-15 Computer share the same (PDP-15) core memory, their programs must interact through the system hardware. For example, the VT15 interacts through the PDP-15 I/O processor (see Figure 1-3) to obtain its operating instructions.

The VT15 program, called the Graphic-15 Display File, is sequentially stored in the PDP-15 core memory. The contents of the display file, in the form of digital instructions and data, are read from the computer core memory, decoded, and then operated on. Digital data to be displayed is converted to analog voltages by the VT15 and transmitted to the display console to drive the X- and Y-deflection circuits of the display CRT. A set of eight basic instructions gives the VT15 system exceptional versatility in the display of points, basic vectors, graph plots, figures, and ASCII characters. Access to the display file is gained by issuing an initial Input/Output Transfer (IOT) command; this instruction starts the transfer of display file instructions through the I/O processor single-cycle data break facility. Thus, the PDP-15 I/O processor controls communication between the VT15 and the PDP-15 core memory and/or central processor; although the VT15 uses the PDP-15 program-controlled IOT facilities for initializing instruction transfers, for computer skip testing, and for read status functions, the basic mode of data and instruction transfers is the single-cycle data break facility of the PDP-15 Computer. In this system, a request originates from the VT15. When the request for data is honored by the

1-3
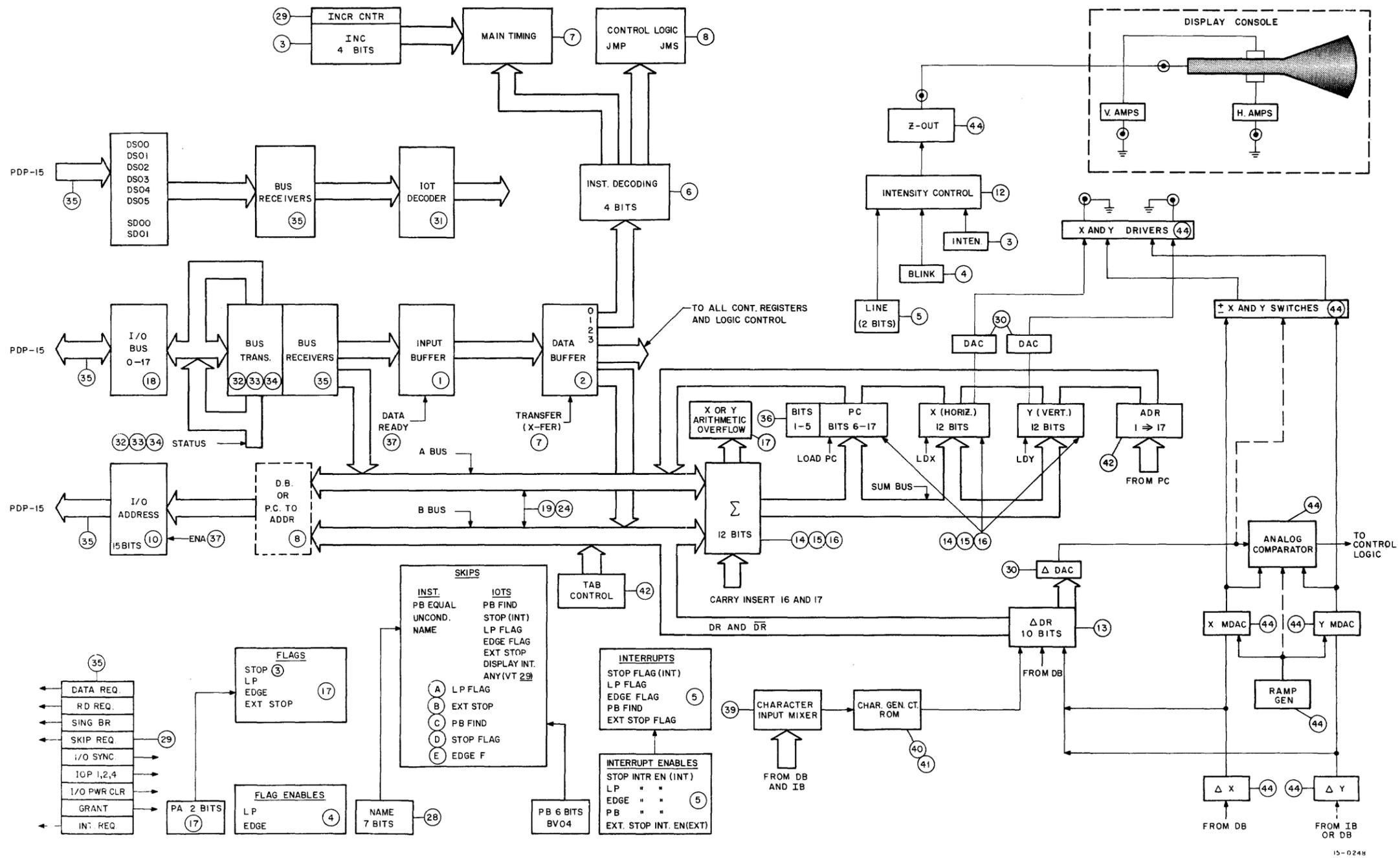
Figure 1-3   VT15 Functional Block Diagram

PDP-15 I/O Processor, the desired instruction, located at the core memory address specified by the VT15 program counter (PC), is read into the VT15 input buffer register. The instruction is then processed by the VT15, and the VT15 program counter is incremented. At the conclusion of the operating cycle, another request is forwarded from the VT15. When the next request is honored, the cycle is repeated. The cycle continues to be repeated until all desired instructions in the display file have been processed.

Thus, on initialization of the pre-programmed display file through a program-controlled IOT command, control is transferred to the VT15, which operates autonomously with respect to the PDP-15, freeing the PDP-15 for computing and I/O operations.

Although the PDP-15 and VT15 share the same memory and the VT15 is asynchronously controlled, the VT15 interacts with the PDP-15 Computer through the IOT instructions and the data channel single-cycle data break facilities.

The VT15 consists of six major functional groups (see Figure 1-3): input/output (I/O) control, data collectors, timing and control, main registers, digital-to-analog converters, and an analog function generator.

The I/O control, data collectors, control and timing, main registers, and digital-to-analog converters (DACs) deal with digital inputs supplied from the PDP-15 Computer. The digital-to-analog converters and the analog function generator (AFG) and related circuitry interact to convert the PDP-15 derived digital data to analog voltage outputs, which are output to the display console to generate the desired image on the display console CRT.

Thus, the basic VT15 consists of the I/O control, coordinate and parameter registers, control and timing circuitry, digital-to-analog converters, an ASCII character generator, an analog function generator, and associated system power supplies. Table 6-2 lists the dc power supplies and corresponding operating voltages required for VT15 operation. Power supply schematics are provided in Volume 2.

1.3 PHYSICAL DESCRIPTION

The VT15 Graphic Processor is self-contained in a single, standard DEC Type H950 cabinet; four casters permit cabinet moveability. Overall cabinet dimensions are: height 71.44 in., width 21.69 in., and depth (front to rear) 30.00 in. Drawing VT15-A-0 in Volume 2 shows the front and side dimensional views of the VT15.

The top, front panel as shown in Drawing VT15-A-0 (frontview) is a 7006331-2 Peripheral Indicator Panel. The second panel is a blank panel. The next four successive panels are Type H911 module mounting panels. The logic modules are mounted in the four mounting racks immediately behind the four front panels.

1.4 SYSTEM OPTIONS

The VT15 is prewired to accept the VV15 Arbitrary Vector Generator and the VM15 Display Console Multiplexer options. The VV15 Arbitrary Vector Generator option provides the capability of drawing a vector of any arbitrary angle on the display console CRT.

The VM15 Display Console Multiplexer option provides the capability to interface up to four VT04/VT07 Display Consoles and four VL04 Light Pens with one VT15 Graphic Processor.

1.5 SYSTEM SPECIFICATIONS

Operating Requirements

Operating Temperature Range	+40° to +95°F
Operating Humidity Range (without condensation)	20% to 55% (relative)
Power Requirements	120V ±15%, 60 cps ±2%, single-phase, 17-30A or 230V ±15%, 50 cps ±2%, single-phase, 17-30A
Power Consumption	2 KW

Dimensions

Cabinet Height	71.44 in.
Cabinet Width	21.69 in.
Cabinet Depth	30.00 in.
Shelf Width	19.00 in.
Cabinet Weight	300 lb (approximate)

1.6 REFERENCING CONVENTIONS

The following paragraphs briefly describe the referencing conventions used in this manual.

a. Numerical Notation – Unless otherwise specified, all number representations are in octal notation.

b. Circuit References – All references to logic signals include the module-type designation, module location code, and output pin designation; e.g., D-Type Flip-Flop M206-F30-E1 indicates that Module M206 is located in rack F, slot 30, and the output signal is taken from pin E1. All racks are designated alphabetically from top to bottom as viewed from the module mounting side. All module mounting slots are numbered 01 through 32 from right to left beginning with the top rack. Slots 1 through 4 of the top or first H911 mounting rack contain the analog output cables. Modules are mounted vertically in the slots. Dual width modules carry dual location designations; e.g., M761-CD13-CK2 where CK2 indicates pin K2 in the C slot of dual location CD, DK2 would indicate pin K2 in the D slot of dual location CD; e.g., M761-CD13-DK2.

c. Signal Mnemonics – Uncommon mnemonics are explained parenthetically the first time they are mentioned in the discussion; e.g., LSD (load and start display). A glossary of all signal mnemonics, their octal code and operation executed is listed in Appendix A of the Graphic-15 Reference Manual.

d. Illustrations – References to in-text illustrations include the chapter prefix number; e.g., Figure 3-5 is the fifth illustration in Chapter 3. References to engineering drawings contained in Volume 2 will be designated by the drawing number; e.g., (VT15-0-1), indicating drawing number 1 of the VT15 Graphic Processor engineering drawing package.

1.7 TERMINOLOGY

Terms used frequently throughout the text are defined below. Other terms are defined within the various discussions.

a. Alternate Mode – Alternate mode (ALT MODE) is ASCII character 175_8. When the character string instruction has been initiated, it remains active until terminated by the generation of an "escape." One method of terminating a character string is through the generation of ALT MODE.

b. Carriage Return – Carriage return (CR) is ASCII character 215. The carriage return key causes the CRT beam to return to the left edge of the paper area. Carriage return can also be used to generate an "escape."

c. Delta Move Time – Delta Δ move time is the time that elapses from the beginning of beam movement to the completion of movement of the beam. Therefore, because CRT beam movement time is constantly varying according to the instruction specified, the term Δ move time is used.

d. Direct Address – The effective address in a memory reference instruction word of a location in core memory that contains an operand.

e. Display File – The VT15 relies on the PDP-15 core memory for storage of the VT15 display file (program), which contains the data and instructions on which the VT15 operates. The single-cycle data break facility enables the digital inputs required by the VT15 to be entered into its input buffer directly from the programmed, sequentially stored, display file (program) in the PDP-15 core memory. The display file is initially entered via an initializing program-controlled input/output transfer. When the display file has been initialized, the VT15 functions autonomously with respect to the PDP-15.

f.   Effective Address – The address of an operand in core memory. It can be an actual address in core memory or an address in core memory that is designated by an indirect address in a memory reference instruction (MRI) word.

g.   Escape (ESC) Mode – The escape mode is used in conjunction with the character string instruction. With ALT MODE or CR enabled, ESC is generated, terminating character string.

h.   Indirect Address – The addressing in a memory reference instruction word of a location in computer core memory that contains an effective address.

i.   Input/Output Pulse (IOP) Code – The last three bits (15, 16, and 17) of the VT15 IOT commands are the IOP codes; IOP4 (bit 15), IOP2 (bit 16), and IOP1 (bit 17). IOP4 is used to effect the transfer of data from the PDP-15 to the VT15 (or peripheral). IOP2 is used to effect the transfer of data from the device, in this case the VT15 to the PDP-15. IOP1 is used to effect I/O skip instructions to test for a device flag or other control function.

j.   Main Registers – The main registers consist of four data holding registers, the X-position and Y-position registers for the X- and Y-axes, the magnitude of change (Δ) register and the VT15 program counter (PC). Outputs from the position and Δ registers (Δ Word, X Word, and Y Word) are applied to the digital-to-analog converters.

k.   Name Register – This register is a 7-bit holding register that permits the identification of up to 128 graphic constructions in the display file. Thus, 128 different 7-bit "names" can be used to name and tag 128 different display files or subroutines.

l.   Program Interrupt – An interruption in the computer program caused by a device service flag. The interrupt is granted on completion of the current instruction.

m.   TAB – The ASCII code TAB is used to specify tabular columns of characters. Tabs begin nine character positions to the right of the normal first character position.

1.8   ENGINEERING DRAWINGS AND CIRCUIT SCHEMATICS

A complete set of VT15 engineering drawings, and power supply and special module schematics are provided in Volume 2 of this manual. Only schematics for special modules that are unique to the VT15 are provided. Remaining module schematics are shown in the Module Manual. A listing of the engineering drawings is provided in Table 6-3. Drawings are listed numerically by drawing code; e.g., VT15-0-01, where VT15 indicates the VT15 Graphic Processor, and 01 indicates the drawing number for the VT15 input buffer. Logic symbols used on the drawings are defined in the Logic Handbook, Document No. 042D 00370 AKO and in the PDP-15 Module Manual, DEC-15-H2EA-D.

CHAPTER 2
INSTALLATION

This chapter provides planning, site preparation, preinstallation, and installation information and recommendations to ensure a successful VT15 Graphic Processor installation.

Digital Equipment Corporation (DEC) provides customer assistance in all phases of site planning. A final layout plan should be approved jointly by the customer and DEC regardless of whether the VT15 Graphic Processor, the PDP-15 Computer, and the display console are installed concurrently, or the VT15 and/or display console are integrated into a previously installed PDP-15 Computer layout plan that may necessitate remodeling of the selected installation site. Site preparation is keyed to the customer's applicable requirements and can range from providing the required source power to construction or remodeling of the selected installation site.

The customer should prepare a list of the actual equipment to be used in the installation. The list should include such items as storage cabinets, work tables, desks, etc., as well as any other items pertinent to the customer's computer application. From this list, the customer can accurately determine his space requirements. Integration of the work area with the storage area can be considered in relation to the work flow requirements between areas.

Additional considerations of importance are: the provision for and availability of adequate power, fire and personnel safety precautions, and proper environmental conditions. Personnel and equipment safety precautions, environmental considerations, and system installation restraints are covered in greater detail in Paragraphs 1.4, 1.5, and 1.6 of the PDP-15 Systems Installation Manual. Functional, physical, and environmental characteristics, and system specifications for the VT15 are provided in Chapter 1 of this manual.

2.1 UNPACKING

CAUTION

Do not attempt to install the system until DEC has been notified, and a Field Service Representative is present. Carefully inspect the VT15 for damage. Any damage should be reported immediately.

Unpack the system according to the following procedures:

Step	Procedure
1	Remove the outer shipping container.

> **NOTE**
>
> The container may be either heavy corrugated card-board or plywood. In either case, first remove all metal straps, then remove any fasteners and cleats securing the container to the skid. When applicable, remove wood framing and supports from around the cabinet perimeter.

Step	Procedure
2	Remove the polyethylene cover from the cabinet.
3	Remove tape and/or plastic shipping pins as applicable from the cabinet rear access door.
4	The cabinet is secured to a type 7605469-1 skid with retaining bolts. Access to these bolts can be obtained by opening the cabinet rear access door and locating the bolts on the lower supporting siderails. Remove the retaining bolts.
5	Ensure that the cabinet leveling feet are raised above the level of the roller-casters.
6	Using wooden blocks and planks, form a ramp from the shipping skid to the floor and carefully roll the cabinet off the skid onto the floor.
7	Roll the system to the proper location for installation.
8	When the cabinet is in the desired position, lower the leveling feet so that the cabinet weight rests on the leveling feet and not on the roller-casters.
9	Use a spirit level to level the cabinet; make certain that all leveling feet are seated firmly on the floor.

2.2 PRIMARY AC POWER CABLES

The primary ac power cable is a three-wire cable that interconnects the site power source to the VT15 Graphic Processor power supplies. The cable is connected at the factory to the VT15 841C Power Controller for either 110V or 220V operation.

> **CAUTION**
>
> Before proceeding, ensure that the VT15 power transformer primary windings are correctly connected (for 110V or 220V operation) to correspond to the installation site source power voltage (Table 2-1). System wiring diagrams (Drawings VT15-A-0 and VT15-A-2) are provided in Volume 2.

Table 2-1
Wiring Jumper Table

Power Supply or Control	Input	From	To
H721	220V	TB1-2 TB1-4	TB1-3 TB1-5
	110V	TB1-1 TB1-2 TB1-3	TB1-3 TB1-4 TB1-5
841C	220V	(2) Orange 110 Vac INPUT jumpers removed	
	110V	(2) Orange jumpers in place	

A jumper connection chart is also provided on the top cover of the H721 main power supply. Each wire in the power cable is color coded as shown in Table 2-2.

Table 2-2
Power Cable Line Identification

Pigtail Information		Terminal Strip Nomenclatures
Line	Wire Color	
Frame Ground	Green	Frame Ground
Neutral/Line 2	White	Neutral or Line 2
Line 1	Black	Line 1

WARNING

The green wire is the cabinet frame ground and does not carry load current but must be connected for personnel safety. It must be securely connected between the VT15 cabinet and the primary power source grounding point.

The white (or light gray) wire is the neutral, common, ac return, or cold load and should never be used for VT15 cabinet grounding purposes.

The VT15 is normally supplied with a 30A Hubbel connector. The ac service outlet to be used must be capable of at least 20A ac, 110V, 60 Hz single phase or 10A ac, 220V, 50 Hz single phase.

2.3 INITIAL SETUP

2.3.1 VT15 Power Connections

Use the following procedure for the initial power check of the VT15:

Step	Procedure
1	Switch the power control circuit breaker to OFF. Set the power control LOCAL-REMOTE switch to LOCAL.
2	Refer to Figure 3-4 of the PDP-15 Installation Manual. Meter the wall receptacle to ensure that the hot, neutral, and ground connections conform to the description given in Figure 3-4.
3	Connect the power cord to the wall receptacle and ensure that the orange indicator lamp on the 841C Power Control Lights.
4	Locate and remove the 4 fuses from the logic panel located on the front of the logic rack.
5	Set the power control circuit breaker to ON.
6	With a multimeter or voltmeter, check the following pins for the specified output voltages:

From	To	Voltage Reading
Pin A20D2	Pin A20F2	+15.0V
Pin A20E2	Pin A20F2	-15.0V
Any pin A2 on Logic Rack	Ground	0V

Step	Procedure
7	Set the power control circuit breaker to OFF.
8	Replace top fuse.
9	Set the power control circuit breaker to ON.
10	Measure +5V ± .1V from pin A20A2 to ground.
11	Set the power control circuit breaker to OFF.
12	Replace the lower 3 fuses.

2.3.2 Cable Installation

The VT15 is normally the last device on the PDP-15 Computer I/O bus. Figure 2-1 shows the various cable lengths and corresponding cable delay settings. To connect the VT15 to the positive I/O bus, reference drawing D-IC-VT15-A-2 and perform the following procedure:

Step	Procedure
1	Determine the last positive I/O device connected to the positive I/O bus in the present configuration.
2	Remove the four M909 I/O Bus Terminator Modules (68 ohm) from the I/O bus output slots of the last positive I/O device. This applies for "add-on" installations only.

Step	Procedure
3	Insert one end of the I/O bus cable into the slots from which the M909 Modules were removed.
4	Insert the opposite end of the I/O bus cable into slots H-J-29 and H-J-30 of the VT15 I/O receptacle.
5	Insert the four M909 Terminator Modules into slots H31, H32, J31 and J32 of the VT15.
6	The X, Y and Z analog cables must be terminated with 100 ohms (part no. 1300229) at the end of each cable run.
7	Connect the VT15 remote power cord from the VT15 (841C) power control to the nearest PDP-15 system power control.
8	Connect the data and control cable to slot H-J-3 of the VT15. Connect the opposite end of the cable to slot AB06 in the VT04/VT07.
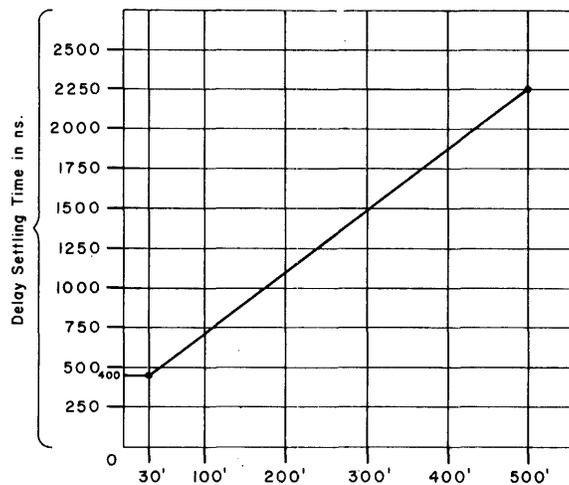
NOTES
1. Allow 4ns foot delay for cable lengths over 500 feet.

15-0411

Figure 2-1   Delay Setting vs Cable Lengths

2.3.3   System Power-Up

After all power checks and cabling have been completed, perform the following power-up procedure:

Step	Procedure
1	Set the VT15 LOCAL-REMOTE switch and display console power controls to REMOTE.
2	Locate the intensity control on the back of the display console and turn the control fully counterclockwise to the minimum position. Set gain fully counterclockwise to minimum and the centering controls to midrange.
3	Set the PDP-15 POWER switch to ON.

Step	Procedure
4	Load and run MainDEC-15-D6EC-D, Little Pictures Test, beginning with Routine 0.

CAUTION

Exercise extreme care when adjusting intensity
controls to avoid burning the CRT screen. If
adjustments are such that the screen cannot be
seen, another person should be present to ob-
serve the CRT during intensity adjustments.

5	Increase the intensity control slowly until a pattern is seen. If a bright spot should appear, immediately decrease the intensity. Adjust the CRT X- and Y-gain and centering to correctly position the images on the screen.
6	Select Routine 5 and run the Intensity Level Test. Adjust the intensity level until level 1 can barely be seen. Intensity level 0 should not be visible (under ambient lighting conditions).

2.4 CUSTOMER ACCEPTANCE

Customer acceptance of the VT15 consists of system operation by running all diagnostic programs pro-
vided, an operating test of the system software, inspection of the shipping list, inspection of the soft-
ware kit, and a physical inspection of the system. No physical damage should be observed, and the
shipping list and software kit should be complete.

2.4.1 Checklist

A checklist is provided with each system to ensure that the following have been accomplished and/or
included. Refer to the Foreword for document reference numbers.

    a. QC Check

    b. Manuals

        Graphic-15 System Reference Manual
        VT15 Graphic Processor Maintenance Manual, Volumes 1 and 2

    c. Other Documents

        Key Sheet
        ECO Sheet

d. Cables

      (1 ea) BC09B, BS01A
      (2) ac Remote Turn-on power cords

e. Diagnostic Software

      The diagnostic software is described in Paragraph 2.4.2.

2.4.2 Diagnostic Programs

Following are the diagnostic programs provided with the VT15 Graphic Processor. Detailed program and test descriptions are provided with each diagnostic program.

a. MAINDEC-15-DAVTB

      Display Instruction Test, Part 1   15 minutes error free.

b. MAINDEC-15-DAVTA

      Display Instruction Test, Part 2   No time limit, manual intervention required.

c. MAINDEC-15-D6DD

      Display Visual Test   15 minutes error free.

d. MAINDEC-15-D6EC

      Little Pictures Test   No time limit, each individual routine is checked against test photographs supplied.

2.5 SYSTEM CHECKS AND ADJUSTMENTS

If a malfunction occurs during system checkout, the fault or problem must be isolated. Fault isolation and troubleshooting procedures are provided in Paragraph 6.5. A listing of system checks and adjustments is provided in Table 2-3.

Table 2-3
System Checks and Adjustments

Checks and Adjustments	Paragraph Number	Purpose
H721 Logic Power Supply Adjustment	6.4.1	Allows adjustment of the logic power supply voltages.
System Clock Adjustment	6.4.2	Checks the M401 basic clock timing.
I/O Loading Delay	6.4.3	Allows adjustment of the time delay between VT15 data requests.

Table 2-3 (Cont)
System Checks and Adjustments

Checks and Adjustments	Paragraph Number	Purpose
Display Console Bus Delay	6.4.4	Allows adjustment of the time delay used to adjust the duration of MS02 and MS03 to compensate for signal latency in the VT15 to display console data and control cable.
Move Settle Delay	6.4.5	Allows adjustment of settling delay time for vectors of 17 units or longer in sector zero. This adjustment is also used for CR and TAB.
Blink Delay	6.4.6	Allows adjustment of the blink rate (blink timing).
Long Point Settle Delay	6.4.7	Allows adjustment of the settling time (of approximately 20 μs) which is used during point moves greater than 200_8 and for sector reentry, CR, and TAB.
Short Point Settle Delay	6.4.8	Allows adjustment of the settling time (approximately 8 μs) used during point moves less than 177_8.
Analog Voltage Adjustments	6.5.1	Checks the voltages used in the analog section.
Analog Adjustments	6.5.2	Provides initial setup and final adjustment of the analog section.

2.6 VM15 DISPLAY MULTIPLEX OPTION INSTALLATION PROCEDURE

The VM15 option allows up to four VT04/VT07s to be connected to a single VT15 Graphic Processor. A common bus, comprised of three coaxial cables, is used to output the X, Y, and Z (unblanking) signals, in parallel, to each of the VT04/VT07 displays. An additional cable, designated the "D" and "C" cable, is used to input and output the INT SEL (Intensity Select), PB SEL (Pushbutton Select), and LP PULSE (Light Pen Pulse) signals between the VT15 and the VT04/VT07(s) (see Figure 2-2).
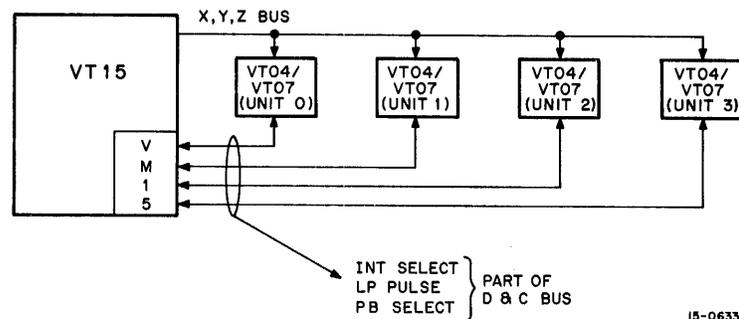
Figure 2-2   VM15 Interconnect Diagram

The standard bus cable length between the VT15 and the first VT04/VT07 (unit 0) is 30 ft. Cables connected between additional VT04/VT07s (units 1, 2, and 3) also have a standard length of 30 ft. Thus, total bus length is 120 ft, with four VT04/VT07s connected to the VT15. A skip 1 latency delay adjustment is required when bus lengths greater than 120 ft are used.

Installation and initial setup procedures for the VT04/VT07 unit 0 are provided in the VT04/VT07 Graphic Display Console Maintenance Manual. The following procedures are provided for installation and checkout of the VM15 Display Multiplexer option:

Step	Procedure
1	Remove the 100Ω terminator plugs from the X and Y "T" connectors on the rear of unit 0 and connect the X and Y coaxial cables to the corresponding X and Y "T" connectors.
2	Connect the opposite ends of the X and Y cables to the X and Y "T" connectors on the rear of unit 1. If only the two VT04/VT07s are connected to the VT15, the 100Ω terminator plugs should be installed in the unit 1 X and Y "T" connector outputs.
3	Remove the 100Ω terminator from the BNC connector designated Z OUT located on the BV04 logic rack of unit 0 and connect the Z coaxial cable. Connect the opposite end of the Z coaxial cable to the BNC connector designated Z IN on the BV04 logic rack of unit 1. If only two units are to be connected to the VT15, install a 100Ω terminator plug in the BNC connector designated Z OUT on unit 1.

Step	Procedure

NOTE
Regardless of the number of VT04/VT07s connected
to the VT15, 100Ω terminators must be installed in
the X, Y, and Z outputs of the last unit.

4   Connect the data and control (D and C) cable from slot AB08 in unit 0
to slot AB06 in unit 1. If only two units (0 and 1) are to be connected,
insert the two M909 Terminator Modules, removed from unit 0, into
slots A08 and B08 of unit 1.

5   If more than two VT04/VT07s are to be connected to the VT15, unit 2 is
connected to unit 1 in the same manner that unit 1 was connected to
unit 0, etc. All terminators will be installed in the last VT04/VT07
that is electrically connected.

There are two W719 Unit Select Modules in each VT04/VT07. The W719 Module located in slot B18
is used to select the light pen and intensity enable for each unit. The W719 Module, located in slot
A10, is used to select the console pushbuttons (see drawing BV04-0-2 in Volume 2 of the VT04/VT07
Graphic Display Console Maintenance Manual). The W719 Unit Select Module is shown in Figure 2-3.

15-0635
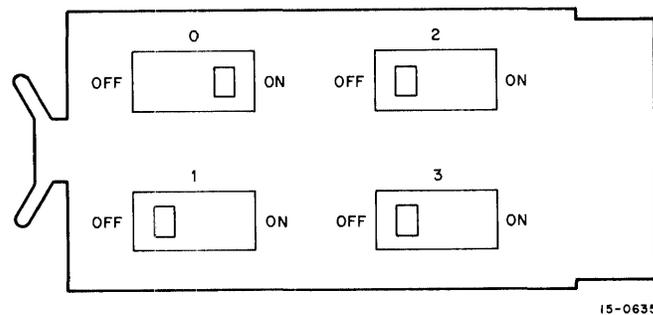
Figure 2-3   W719 Unit Select Module

When running the VM15 Multiplexer Test under normal conditions, the unit select switches should be
set so that each display console has a different logical unit select number (address); i.e., 00, 01, etc.
However, during alignment the intensity select switches should all be set to unit 0 to allow the test
patterns produced by the VT15 Little Pictures diagnostic to be displayed simultaneously on all display
CRTs.

CHAPTER 3
SYSTEM OPERATION

3.1 SYSTEM ORGANIZATION

The primary function of the VT15 Graphic Processor is to convert digital instruction inputs from the PDP-15 Computer into analog signals to drive the X- and Y-deflection circuits of the display console CRT. The inputs are basically two types: program input/output transfer (IOT) instructions and display file instructions. IOTs are program-controlled whereas the display file instructions are obtained via the single-cycle data break facility. The VT15 Graphic Processor consists of six major functional groups: I/O control, data collectors, timing and control, main registers, digital-to-analog converters, and analog function generator.

These six major functional groups (see Figures 3-1 and 3-2) combine to control the interactive functions of the VT15 Graphic Processor, the PDP-15 Computer, and the graphic display console(s). The VT15 has an indicator panel that can be referenced during operation and maintenance to indicate the operational status of the VT15 Graphic Processor.
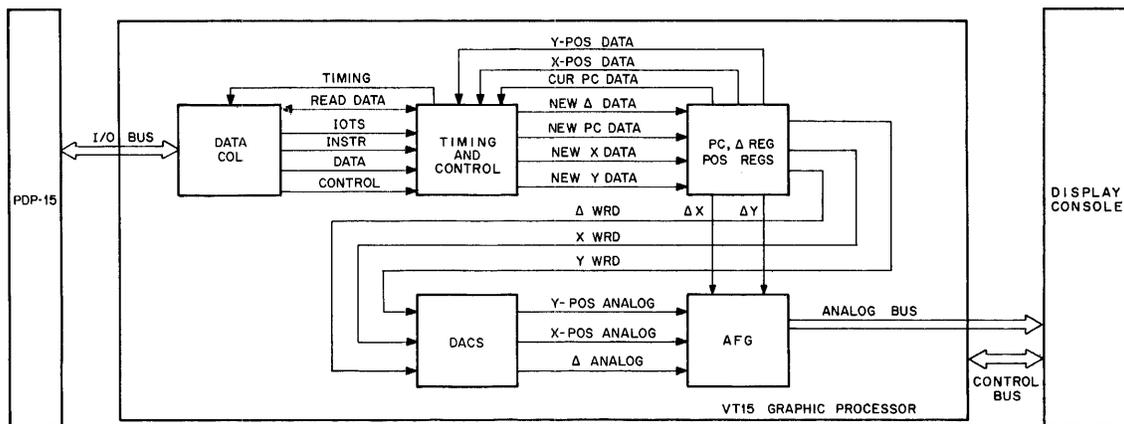
15-0592

Figure 3-1   Major Functional Groups, Interconnect Diagram

3-1

VT15 GRAPHIC PROCESSOR

TIMING AND CONTROL

DATA FROM DATA BUFFER REG

IOTS FROM DATA BUFFER REG

IOT DECODE

LSD

MAIN TIMING

TIMING

CHAN CONT

DATA CHAN MULTIPL

SKIPS

CONTROL TO PDP-15 COMP

NEW Δ DATA TO ADDER GATING

TIMING TO ADDER GATING

DATA
TIMING
PARAM
INSTR

DIRECTION AND ROTATE

TSY
TSX
ADD Δ
SUB Δ

ADDER GATING

PARAM AND SKIP REGS

PARAMS

DATA
TIMING
SET PC
POINT
SUB RUT
GRAPH

GRAPHIC CONTROL

SET REGS

TIMING   DATA

INSTR

INSTR

CHAR GEN

CHAR DATA

INCR AND COUNT

VT15 GRAPHIC PROCESSOR

DATA COLLECTORS

TIMING FROM MAIN TIMING

DATA BUFFER REG 18 BITS

TIMING FROM I/O BUS INTERFACE

INPUT BUFFER REG 18 BITS

READ DATA FROM IOT DECODE

BUS RCVRS

PDP-15 COMP

CONTROL FROM PARAM AND SKIP REGS

DATA

DATA

DATA

INSTR DATA FROM DATA BUFFER REG

15-0268

Figure 3-2   VT15 Major Functional Groups,
Functional Block Diagram (Sheet 1 of 2)

Figure 3-2 VT15 Major Functional Groups,
Functional Block Diagram (Sheet 2 of 2)

15-0269

3.1.1 I/O Control

3.1.1.1 Data Channel (DCH) Control and Automatic Priority Interrupt (API) Multiplexer - The DCH control consists of an M104 Data Channel Multiplexer Module, associated gating, and pulse amplifiers. A VT15 data request and I/O SYNC initiate a single-cycle break (SING BR) request. If a higher priority device has not requested use of the I/O bus, the VT15 will receive a GRANT from the computer. With GRANT and REQ coincident, enable A (ENA) will be set indicating the VT15 has use of the I/O address (ADR) lines. ENA gates the address off the VT15 address lines and onto the I/O address lines of the I/O bus, clears the data request and REQ flip-flops, and gates the read or write request lines. DCH control is depicted in greater detail in Figure 4-12 of the PDP-15 Systems Interface Manual.

3.1.1.2 Read Cycle - If the VT15 requests a read cycle as a result of a jump-to-subroutine (DJMS) or SAVE instruction, data is gated on the bus at the time ENA occurs. A pulse called DATA ACCEPT is produced on the (1) to (0) transition of GRANT, indicating to the VT15 that the computer has accepted its data, and the VT15 may proceed with its timing.

3.1.1.3 Write Cycle - If the VT15 requests a write cycle, a pulse called DATA READY will be produced by the (1) to (0) transition of IOP4 in coincidence with ENA. The DATA READY pulse indicates that the computer has placed the requested data onto the I/O bus, and it may be accepted by the VT15. The DATA READY pulse is primarily used to strobe input data into the input buffer and, under certain circumstances, to continue main timing.

3.1.2 Data Collectors

3.1.2.1 Bus Receivers - The VT15 Graphic Processor receives inputs from the computer and supplies outputs from the graphic processor to the computer via a bus receiver interface consisting of M510 Bus Receivers. The M510 has an input threshold of approximately 1.5V and supplies both the true and complemented TTL levels for a given input signal. All data and control signals received on the I/O bus are processed via these receivers. For more detailed information concerning the M510 Bus Receiver, refer to Paragraph 2.3.4 of the PDP-15 Systems Interface Manual.

3.1.2.2 Bus Drivers - Data is gated onto the computer I/O bus by a series of two-input gating structures and is enabled by either issuing the proper IOT or by a DJMS or SAVE instruction. Noninverting M622 Bus Drivers are used.

3.1.2.3 Input Buffer Register – The VT15 is a double-buffered system that maintains two levels of data registers: an active register and a holding register. The input buffer serves as a holding register and, as previously mentioned, the DATA READY pulse strobes the incoming data from the I/O bus into the input buffer. Nevertheless, the input buffer plays no active part in operation of the VT15 except during the character string instruction, in which case, the second 18-bit word is taken directly from the input buffer.

3.1.2.4 Data Buffer Register – The second level of input buffering occurs in the data buffer. The data buffer always acquires its data from the input buffer and is considered an active register. The instruction decoder operates directly from the data buffer, decoding the first three or four high-order bits of the incoming data.

3.1.3 Timing and Control

The timing and control functional group processes the data acquired by the data collectors; more specifically, the data acquired by, and contained in, the data buffer register.

3.1.3.1 Main Timing – The data processing functions are controlled by main timing circuits that are operated by a basic clock, which generates pulses at a 250-ns repetition rate. Each 250-ns interval is considered one time state. In general, at least three time states, designated MS01, MS02, and MS03, are required to process instruction-word functions. Examples of main timing are shown in Figures 3-3 and 3-4. As shown in Figure 3-3, various instruction-word functions and signals are generated as follows, with respect to the various time states:

a.	Time state 1 (MS01)	Is used to increment the program counter and to load the various registers located in the control logic.
b.	Time state 2 (MS02)	Is used for modification of the X-position register.
c.	Time state 3 (MS03)	Is used for modification of the Y-position register.

The fourth time state (MS00) indicates that the particular cycle is complete. Various signals or functions such as digital-to-analog functions, save/restore, beam movements, incrementing the increment count register, enabling intensity, and repeats (REPT) usually occur during the fourth time state or time state 0 (MS00). Another term used in conjunction with beam movement time is Delta (Δ) Move Time (see Paragraph 1.7, c).

The main timing circuitry of the VT15, designated the main time state generator (VT15-0-07), consists of a 4-bit shift register and a 250-ns basic clock. The main time state generator can be gated on by an XFER or a RESTART-REGO condition. All display instructions, except character string, use OP DONE in conjunction with DATA AVAIL to generate an XFER (transferring the contents of the input buffer to the data buffer) and restart the timing generator.

Character string generates an OP DONE only on the completion of an entire string of ASCII characters through the detection of an escape (ESC) code (ALT MODE or CR). Another level, designated IOPS ENA is used to generate an XFER to transfer new character information from the input buffer to the data buffer and to restart the main timing generator. RESTART-REGO permits re-execution of a graphic instruction and is normally used in conjunction with the increment register.

3.1.3.2 Control and Graphic Timing – In addition to the main timing, the VT15 contains control timing and graphic timing circuitry. The control timing chain controls the display file memory reference and graphic instructions: jump, jump indirect, jump-to-subroutine, jump-to-subroutine indirect, save/restore, character input, and character string.

Basically, the JMP, JMS, or any of the indirect memory reference instructions are executed by temporarily switching the PC off the address lines, putting the address portion of the instruction, contained in the data buffer, onto the address lines and generating another request.

The graphic timing chain is primarily concerned with loading the "magnitude of delta" into the X and Y registers, receiving the "move in progress" (MIP) signal from the analog-function generator (AFG) and processing the proper OP DONE or RESTART-REGO signal(s) when the vector is completed.

3.1.4 Instruction Register and Logic

3.1.4.1 Parameter and Skip Registers – The parameter instruction is further divided into three sub-instructions as described in Paragraph 4.5.1. The instruction operating code is decoded in coincidence with a timing pulse (START CYCLE), which is derived from the main timing generator. Certain parameter registers can also be set through the display file RESTORE instruction or from certain IOTs.

The skip instruction is divided into two subinstructions as described in Paragraph 4.5.1. The instruction operating code, in coincidence with a START CYCLE pulse derived from the main timing generator, tests the specified skip conditions. With a skip condition, a display skip (DSPLY SKP) will be generated, and the VT15 program counter will be incremented.
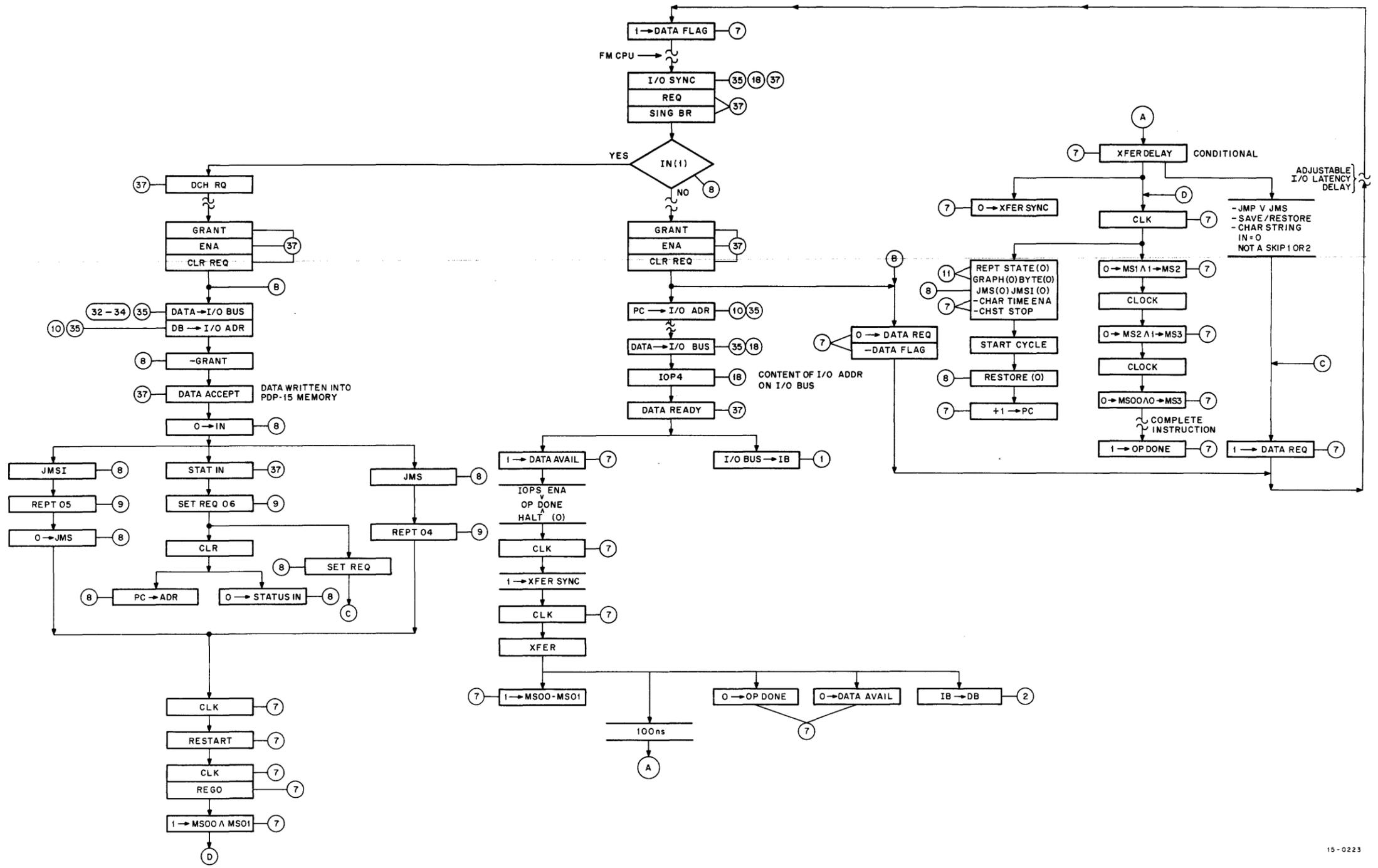
Figure 3-3 VT15 Main Timing Flow Diagram

15-0223
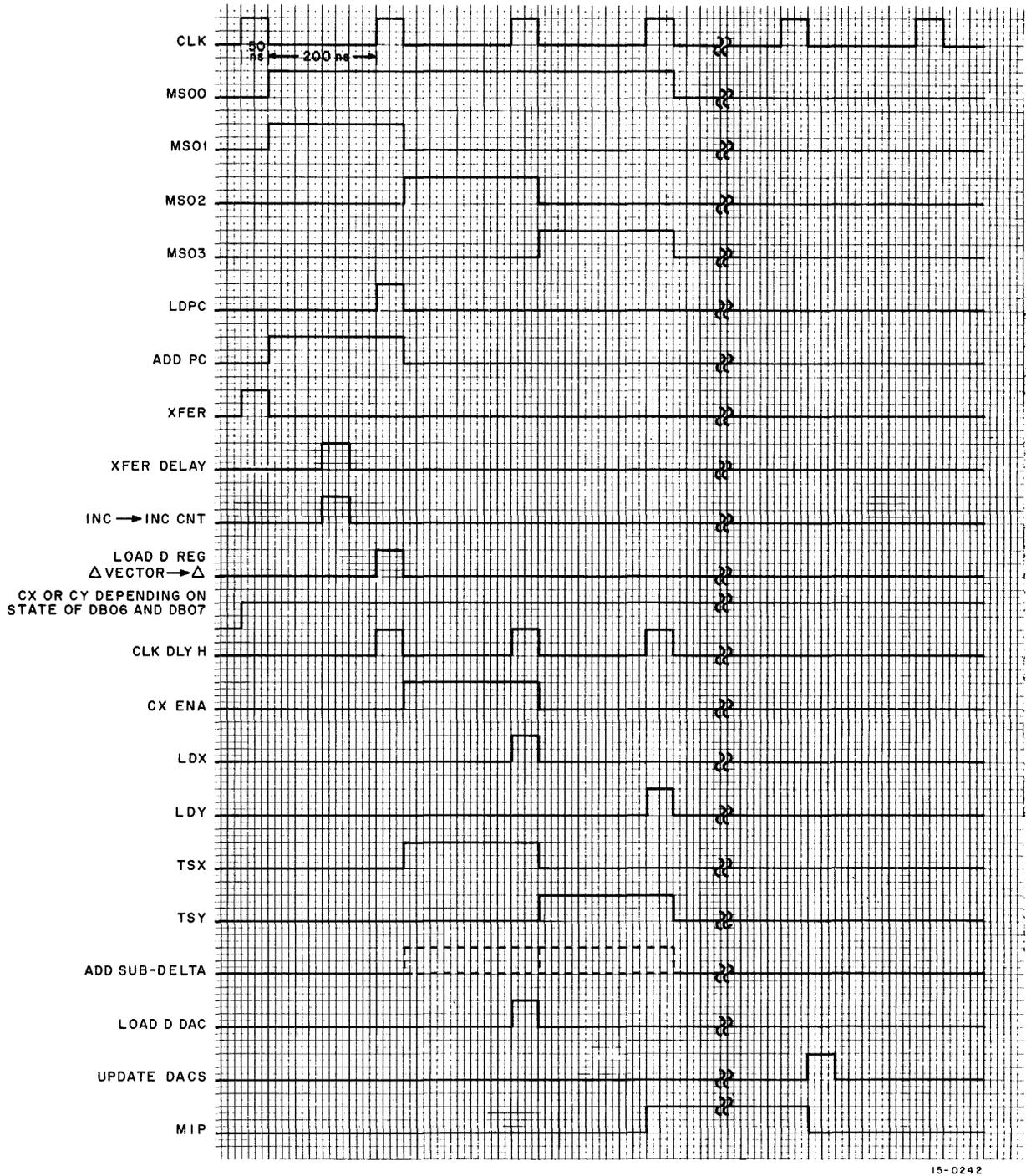
Figure 3-4 VT15 Main Timing Diagram (Sheet 1 of 2)
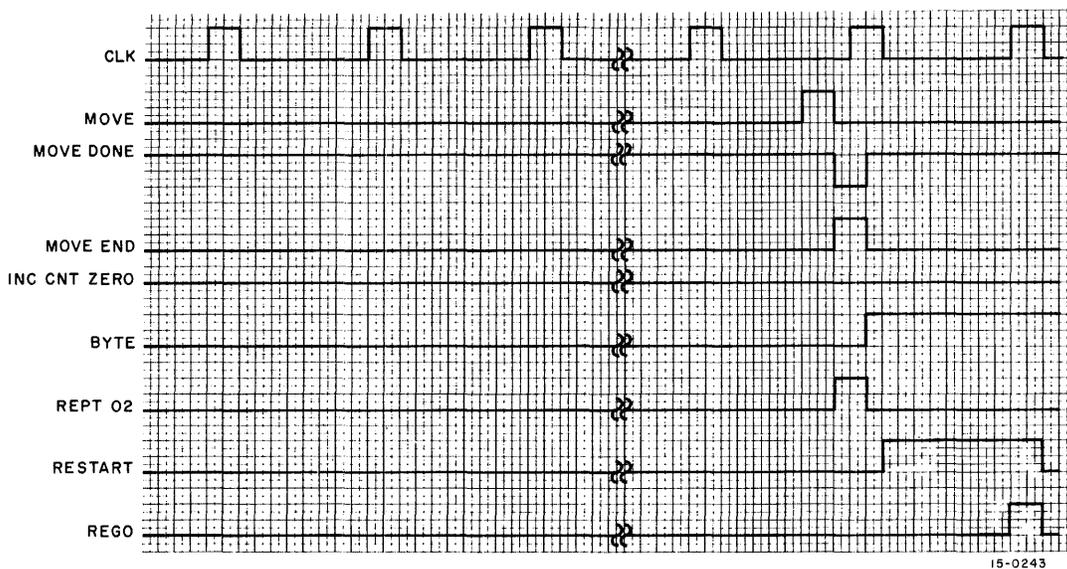
Figure 3-4   VT15 Main Timing Diagram (Sheet 2 of 2)

3.1.4.2   Direction and Rotate Logic – The direction parameter may be specified by bits 5 through 7 of the basic vector instruction, and bits 5 through 7 and 12 through 14 of the basic short vector instruction. The vector, graph plot, and character instructions enable a section of the direction and rotate logic (drawings VT15-0-25 and -26) that is used for decoding beam direction data for subsequent movement. In addition to the decoding bits, the logic also processes an interchange of direction data and adder gated enable time states to allow 90° counterclockwise rotation of basic vectors and characters, when specified. This feature is enabled through bits 12 and 13 of the parameter 2 instruction (Figure 4-22).

3.1.4.3   Increment Register – The increment register or counter is a four-bit register that is loaded from bits 14 through 17 of the parameter 1 instruction (see Figure 4-20) and is used for scaling. The increment register is used in conjunction with the graph plot instruction (see Figure 4-32) to specify beam displacement for the unspecified axis, described in Paragraph 4.5.4.2, d.

3.1.4.4   Intensity – Eight levels of intensity, INT0 through INT7, can be specified by bits 8 through 10 of the parameter 1 instruction (see Figure 4-20) and refer to Paragraph 4.5.1.1. Bit 4 is used as the intensity enabling (INT ENA) bit in all of the above-mentioned instructions. With the desired 3-bit intensity word (level) specified through the parameter 1 instruction, the 3-bit intensity register is loaded with the 3-bit field, setting the intensity level for all intensified points, vectors, and characters generated thereafter. If a different intensity level is desired to emphasize a particular point, vector, or character, the new intensity level must be specified through the parameter 1 instruction.

3-10

3.1.4.5 Status – Six read IOTs are used to check the contents and/or condition of various flags, parameter registers, program counter (PC), and X- and Y-axis position registers.

Various parameters can also be collected by issuing a display file save/restore instruction (see Figure 4-37). When the various parameters have been assembled into the save/restore status format and stored in the computer core memory, the content can be examined easily by issuing a load accumulator (LAC) instruction that examines the status word.

3.1.4.6 Adder Gating – The adders to the main registers are gated by AND/OR gate circuits (VT15-0-19 through -24). The gating provides an addition or subtraction capability, through 2's complement, of up to a 10-bit word (number) that is gated into the X- and/or Y-registers. A given 12-bit number can be transferred into the PC, X- or Y-registers directly from the data buffer. The program counter can be set by an IOT. Provision is also made to increment the program by 1 (+1→PC). A gate is provided to give a "carry insert" into the least significant adder for both incrementing the PC and for the 2's complement subtract operation.

3.1.5 Main Registers

The major registers contained in the VT15 Graphic Processor are the program counter, the X-axis position register, the Y-axis position register, and the Δ register.

3.1.5.1 PC, X- and Y-Registers – Three M215 Modules, each module containing a 4-bit section of the PC, X- and Y-registers, combine to form the 12-bit X- and Y-registers. The 10 least significant bits from the position registers are applied to the position (X- and Y-) DACs. The three M215 Modules also handle the 12 low-order bits (bits 6 through 17) of the PC. A separate five-bit register is used to handle the remaining PC high-order bits.

3.1.5.2 Magnitude of Change (Δ) Register – This 10-bit register holds the binary equivalent of the relative displacement of the writing beam. The data contained in the Δ register defines the magnitude of the relative displacement between a new position and the previous position from which the beam has been moved. This magnitude of relative replacement is the new Δ word (value) that is always summed with the current position data held in the X- and Y-position registers. The content of the Δ register is then added or subtracted from the content of the X- or Y-register, or both registers, depending on the direction and magnitude of beam movement. The output of the Δ register is applied to the Δ DAC.

3-11

3.1.6   Digital-to-Analog Converters

Three digital-to-analog converters (DACs) are used in the VT15 Graphic Processor: the X-position DAC, Y-position DAC, and Δ DAC. These three DACs are used to convert the binary data contained in the X-position, Y-position, and Δ registers to an analog voltage whose magnitude is equivalent to the digital data word, or value. The analog voltages produced by the X- and Y-DACs are used to produce the CRT X- and Y-deflection voltages. The analog voltage produced by the Δ DAC is applied to a comparator circuit in the analog function generator. The magnitude of the Δ DAC analog voltage is compared with the instantaneous magnitude of the ramp voltage to determine if the two voltages are equal. Thus, the beam will be deflected to a point on the CRT equivalent to the magnitude of the analog voltage derived from the Δ register, via the Δ DAC.

3.1.7   Analog Function Group

In the VT15, two types of vectors may be generated; basic and arbitrary. Basic vectors can be generated in only eight directions, as shown in Figure 4-27. Arbitrary vectors can be drawn in any direction. Generation of the analog ramps that produce basic and arbitrary vectors is performed by the Analog Function Group (Figure 3-5).

Vectors are generated by applying a ramp voltage to the X and Y summing amplifiers. The ramp voltage is summed with the X and Y analog holding voltages derived from the Position DACs (Drawing VT15-0-30). The MIP flip-flop, consisting of two NAND gates (Drawing DCS-A3180-0-1) controls ramp generation, and enables vector intensification. The flip-flop, initially cleared by a system power clear, is set by a START GEN pulse from the VT15 logic. (See timing diagrams 3-6 and 3-7.) With the MIP flip-flop set, the ramp generator is enabled; capacitor C is allowed to charge linearly. The ramp voltage developed on this integrator is fed to the multiplying DACs (M-DACs) on the A3170 module, where it is multiplied by a value determined by the digital inputs to the M-DACs.

When basic vectors are generated, the digital inputs to the M-DACs are all high; this yields a multiplying factor (gain) of approximately unity across the M-DACs and their associated amplifiers. The amplified ramp outputs of the M-DACs, ABR RAMP X and ABR RAMP Y, are fed to the A140 Dual Analog Switches. ABR RAMP Y is also applied as an input to the comparator on A3180. Each A140 switches its ramp input to either the non-inverting or inverting input (or neither, if vectoring only in the opposite axis) of its summing amplifier on the A238 module, depending on whether the basic vector is being drawn in a positive or negative direction. In the summing amplifiers, the ramps are summed with the outputs of the X- and Y-Position DACs. Upon completion of a vector, the Position DACs are updated to represent the new beam position.

When an arbitrary vector is being generated, the ramp developed by the integrator is fed to the M-DACs and fractionally multiplied by the normalized binary values of the X and Y vector components. These normalized values are the largest possible 10-bit binary numbers that still retain the magnitude ratio of the X and Y components of the vector.

Normalization is performed to minimize variations in drawing rate (cm/second) from vector to vector, thereby minimizing variations in vector intensity. With normalization, all arbitrary vectors are drawn within a 2:1 error band rate. An extra analog compensation network (explained later) minimizes drawing rate variations even further. Normalization is achieved by shifting the binary bits representing the X and Y vector components, held in the ΔX and ΔY storage registers (Drawing DCS-M7010-0-1 and Paragraph 5.1.10), until the most significant bit in either X or Y or both registers is a 1. The resulting multiplication in the M-DACs and their associated amplifiers is by a factor of from 0 to 1. The slopes of the M-DAC outputs will not be equal (as in basic vector generation), but will reflect the differences in X and Y component values of the arbitrary vector; the ratio of the slopes will equal the ratio of the vector components. The amplified ramp outputs of the M-DACs (ABR RAMP X and ABR RAMP Y) are then switched by the A140s to either the non-inverting or inverting inputs of the summing amplifiers. One of these ramps is also applied as an input to the comparator on A3180. If the Y component of the vector being drawn is greater than or equal to the X component, ABR RAMP Y is switched to the comparator; ABR RAMP X is switched otherwise.

The comparator on the A3180 senses when a vector has been completed, and terminates the vector. It compares the D ANALOG reference voltage from the D-DAC, to the instantaneous value of the ramp (ABR RAMP X or ABR RAMP Y) generating the vector component of greater magnitude. When the two comparator inputs are equal, the magnitude of the vector generated is equal to the value specified by the VT15 instruction; the comparator output goes low, resetting the MIP flip-flop. The MIP flip-flop shuts down integration by shorting out capacitor C, discharging it, and disables vector intensification.

The D/A converter on the A3180, along with its associated circuitry, is a compensation network. It operates to minimize variations in drawing rate caused by changes in multiplying factor at the M-DACs. Operation of the circuit is discussed in detail in Paragraph 5.1.9.
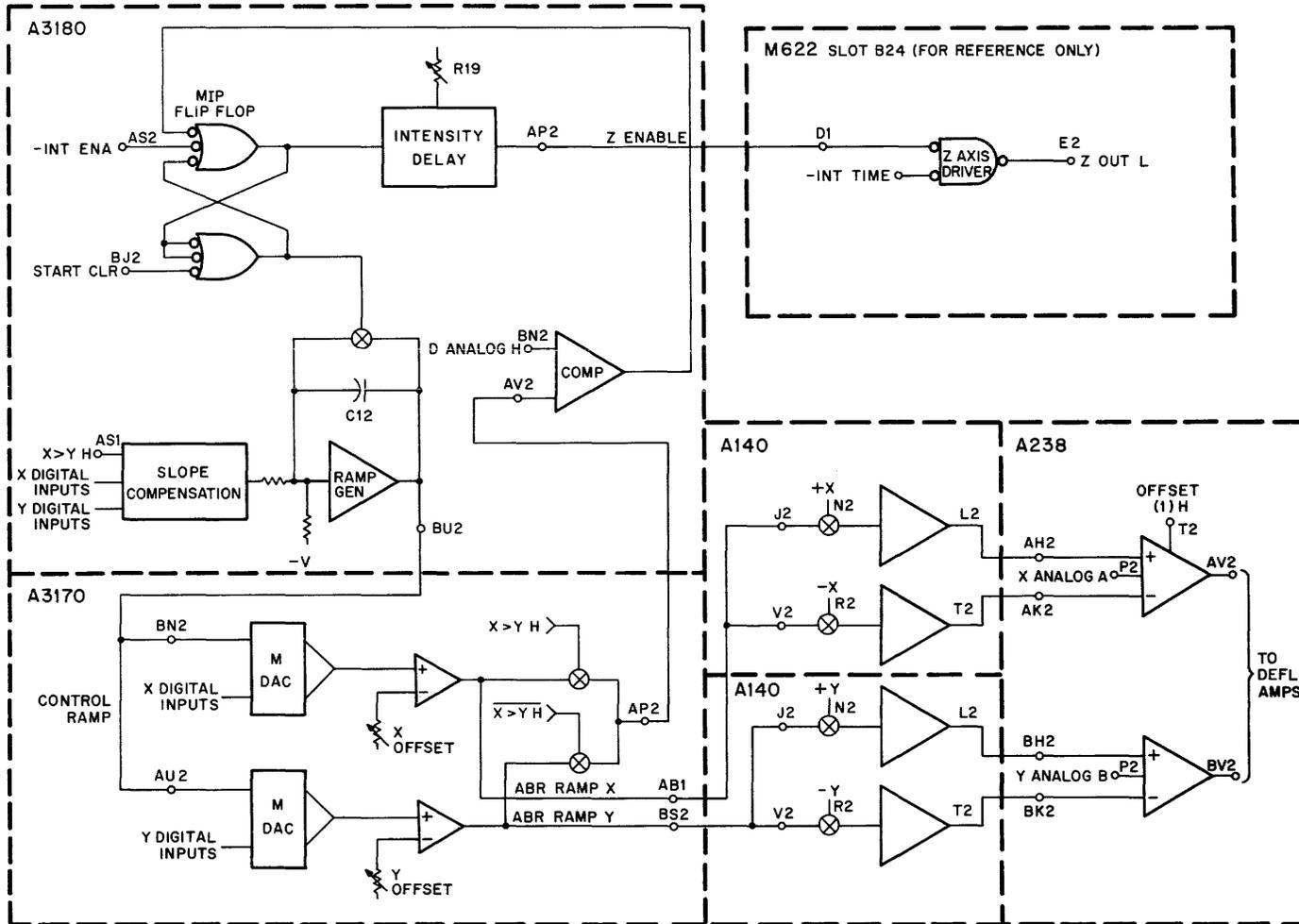
Figure 3-5 Analog Function Group

15-0632

Figure 3-6   Analog Function Timing Diagram (Basic Vector)

3-15
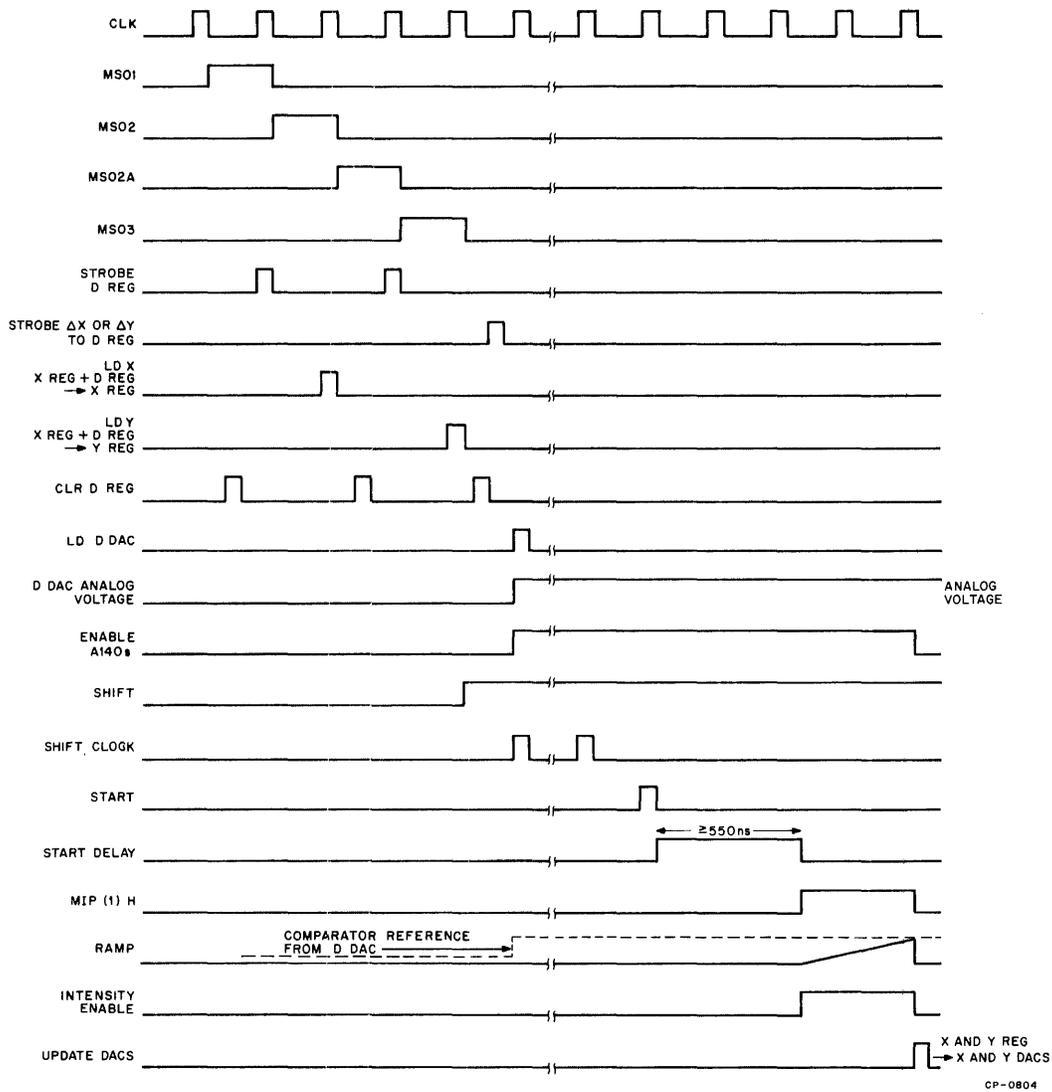
Figure 3-7   Analog Function Timing Diagram (Arbitrary Vector)

CP-0804

3-16

3.1.8 Arbitrary Vector Timing and Control

The VV15 Arbitrary Vector option consists of two modules: the M7010 Timing and Control Module and the A3170 Arbitrary Vector Generator Module. The A3170 module was discussed as part of the Analog Function Group. The M7010 Module provides the timing and control required to process arbitrary vector digital data received from the data and input buffers. It consists of five input data multiplexers, two 10-bit (ΔX and ΔY) holding registers, control and timing logic, a digital magnitude comparator, and X- and Y-data output gating.

3.1.9 Character Generator

The VT15 Graphic Processor character generator consists of address and character generator control logic, a character generator input mixer, and a character generator read-only memory (ROM).

3.1.9.1 Control Logic

3.1.9.1 Control Logic – The character generator control logic consists of various registers and complex logic that provides the timing and control functions necessary for initializing, processing, generating, and terminating ASCII characters through the character input (see Figure 4-38) and character string (see Figure 4-41) instructions.

3.1.9.2 Input Mixer and Read-Only Memory

3.1.9.2 Input Mixer and Read-Only Memory – The input mixer and read-only memory consists of one M163 dual binary-to-decimal decoder, eight G618 ROM diode matrices, two M762 ROM diode matrix receivers, and one M761 32-to-8-bit multiplexer.

For more detailed information concerning VT15 special modules, refer to Chapter 5, Paragraphs 5.1.4 through 5.1.13. For more detailed information concerning IOPS ASCII character generation, refer to Paragraph 4.5.8.1 and 4.5.8.2.

3.1.10 Display Console Multiplexer Option

The VM15 Display Console Multiplexer option allows up to four VT04 or VT07 Graphic Display Consoles to be connected to and controlled by the VT15 Graphic Processor. Two additional modules required with this option are: one M216 General-Purpose Flip-Flop and one M622 Eight-Bit Positive Input/Output Bus Driver. These two modules are used in conjunction with two W719 Unit Select Switch Modules and other light pen and pushbutton related logic contained in the VT15.

There are two VT15 instructions and two IOTs that are used with the VM15 option; they are: the slave (op code 34), Skip 1 (op code 23), and IOT Set Initial Conditions (IOT SIC), used in conjunction with IOT Read Status 2 (IOT RS2).

Display console unit address information is stored in a 2-bit register contained in the VT15. The register is loaded through bits 14 and 15 of the AC using the SIC IOT command. The particular console pushbutton bank is selected on the basis of the unit address specified by the last IOT SIC command. The information is read through issuing IOT RS2. The bit 14 and 15 configurations and corresponding unit addresses are as follows:

Bit 14	Bit 15	Display Console Unit Address
0	0	0
0	1	1
1	0	2
1	1	3

Due to the asynchronous operation of the VT15 and the PDP-15, the VT15 should be stopped prior to issuing IOT RS2 to read the pushbutton status, or erroneous data could be supplied to the CPU.

The Slave instruction is used to selectively blank or unblank any one of the (up to four) VT04/VT07 display consoles. The intensity (INT) and light pen enable (LP ENA) functions control any combination of the (up to four) consoles by setting the appropriate bits within the Slave instruction.

The Skip 1 instruction is used in exactly the same manner with the VM15 option as without the option except that two of the instruction bits (16 and 17) are used as unit select bits. The signals required to set, clear and/or skip test the various display console pushbutton bank(s) and LPSI flip-flops are controlled by setting the proper unit select bits of the Skip 1 instruction.

CHAPTER 4
INSTRUCTION FLOW ANALYSES

The basic VT15 display file transfers occur through the single-cycle data break facility. Of the eight basic display file instructions, three are memory reference instructions (MRIs): character string (CHARST), save/restore, and jump/jump-to-subroutine (DJMP/DJMS). The parameter/skip instructions establish characteristics of points, vectors, graph plots, and characters, as well as establishing program interrupts and skips. The parameter and skip instructions are characterized by a 4-bit operate field, with an additional 2-bit subinstruction field for the parameter instructions and a 3-bit subinstruction field for the skip instructions.

The four remaining basic display file instructions, point/graph plot, basic vector, basic short vector and character input, are considered graphic instructions.

Instruction flow diagrams are provided for each of the VT15 display file instructions and IOT commands. Each diagram contains the particular instruction or command format and a detailed instruction flow. Each event within the respective flow diagrams is keyed to the related VT15 drawing, located in Volume 2 of this manual. For example: ⑥ would equate to VT15-0-06, with VT15 indicating the VT15 drawing package, and -06 indicating drawing number 6, in this case the "instruction decoder" of the VT15 Graphic Processor (drawing package). In some instances more than one reference number is encountered for a single event, i.e., ①, ⑥ , ⑪ , indicating that the particular signal (function) occurs or appears in the order indicated, from left to right. Thus, the order in this example indicates that the particular function or event occurs initially on drawing VT15-0-1, then VT15-0-6, and concludes on VT15-0-11. Off page references, such as from one instruction to another are denoted by encircled letters, i.e., Ⓐ , Ⓑ , etc. These flow diagrams are especially useful for system and instruction flow analyses, as well as for troubleshooting and maintenance purposes.

A full numerical listing of VT15 drawings is provided in Table 6-3. Cross referencing instructions and utilization of the VT15 flow diagrams for maintenance and troubleshooting purposes are covered in greater detail in Chapter 6. A complete listing of VT15 IOT command and display file instruction mnemonics, octal codes, and definitions are provided in Appendix B of the Graphic-15 Reference Manual.

4.1 INPUT/OUTPUT TRANSFER COMMANDS

The VT15 Graphic Processor utilizes 18 input/output transfer commands (see Figure 4-1). Four are operate commands, seven are computer skip commands, six are read commands, and one is a peripheral clear command.
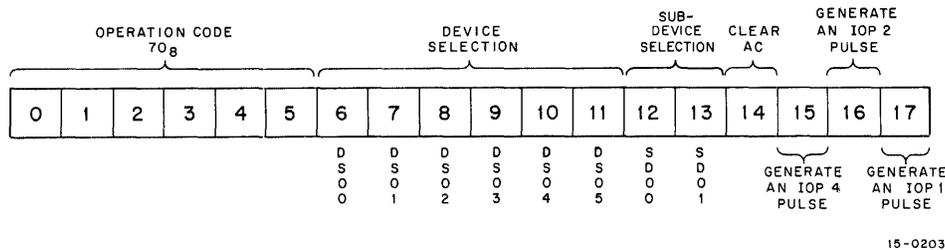
Figure 4-1   Basic IOT Command Format

The basic IOT command is a standard 18-bit word, consisting of four multibit parts. Bits 0 through 5 combine to make up the computer operation code, hereafter referred to as the op code. The op code for all VT15 IOTs is 70_8. Bits 6 through 11 specify the device selected, or the device selection code. These 6 bits permit the allocation of up to 64 peripheral addresses. Device selection codes for the VT15 Graphic Processor are 30_8, and 31_8. Bits 12 and 13 serve as the subdevice selection code. With the subdevice selection code used in conjunction with the device selection code, the number of available peripheral addresses can be increased from 64 to 256. The subdevice selection code can also be used to increase the number of possible VT15 IOT operations. Setting bit 14 clears the PDP-15 accumulator; bit 14 should always be set when any of the read status IOT commands (RS1, RS2, RS3, etc.) are used. Bits 15 through 17 are used for the input/output pulse (IOP) codes, consisting of IOP 1 (bit 17), IOP 2 (bit 16), and IOP 4 (bit 15). IOP 2 is used to effect the transfer of data from the VT15 Graphic Processor to the PDP-15 Computer. IOP 1 is used to generate input/output skip instructions to test a flag or other control function. IOP 4 is used to effect the transfer of data from the PDP-15 to the VT15 Graphic Processor.

All VT15 IOT commands that are considered IOT operate commands (SIC, LSD, etc.) utilize the IOP 4 input/output program code. All VT15 IOT commands that are considered read commands utilize the IOP 2 input/output program code; all VT15 IOT commands that are considered skip commands utilize the IOP 1 input/output program code.

The three IOP codes (bits 15, 16, and 17) control a timing generator in the PDP-15 Computer. This timing generator provides serial output pulses, via the input/output bus, to the VT15 Graphic Processor

4-2

to be used in performing its operations. Thus, setting any one of bits 15, 16, and 17 separately, or in combination, will obtain a desired response from the VT15 Graphic Processor. A separate response is obtained from the VT15 for each of the IOP pulses, even in cases where more than one IOP code is present within a given IOT instruction.

4.2 IOT OPERATE COMMANDS

The IOT operate commands are used to initiate the display file, set initial conditions, clear flags, enable program interrupts, establish paper size, stop the display, and to resume the display file after an interrupt or a display stop. There are four VT15 IOT operate commands: set initial conditions (SIC), load and start display (LSD), external stop display (STPD), and resume display after flag (RES). Clear flags (CLR FLAGS) will also be covered under the IOT operate commands although, by definition, it is not considered as such.

4.2.1 Set Initial Conditions

The IOT command (see Figure 4-2), set initial conditions (SIC), is an initializing command. It is used to establish initial conditions for computer program interrupts, clear flags, and establish paper size.

4.2.1.1 Program Interrupt Enables - Bits 0 through 4 of the SIC IOT command are used to enable program interrupts such as stop interrupt enable, light pen interrupt enable, etc., prior to program initialization.

4.2.1.2 Clear Flags - Bits 5 through 9 are used to clear certain flags and conditions such as stop flag, PB find, etc.

4.2.1.3 Paper Area Change Enable - Bit 10 is used as the paper change enable (PA CHAN EN) bit; bits 11 and 12 contain the paper size information. When the desired paper area size is specified, the SIC instruction loads the VT15 paper-area register.

4.2.1.4 Paper Area - Table 4-1 gives the effective drawing area for each of the four possible bit combinations of this two-bit register. Four different paper area sizes are possible.

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
SET STOP INTR EN	SET LP INTR EN	SET EDGE INTR EN	SET PB INTR EN	EXT STOP EN	CLR STOP FLAG	CLR LP FLAG	CLR EDGE FLAG EN*	CLR PB FIND	CLR EXT STOP	PA CHAN ENA	PA 00	PA 01	CLR LP INTR EN	SLAVE PB00	SLAVE PB01	SET LP FLAG EN	CLR LP FLAG EN
1	1	1	0	0	0	0	1	1	0	0	0	0	1	0	1	0	0

"70"

*ALSO CLEARS:

EDGE FLAG ——(17)
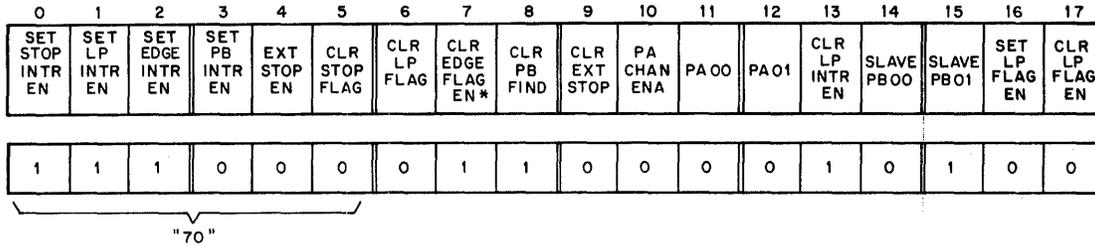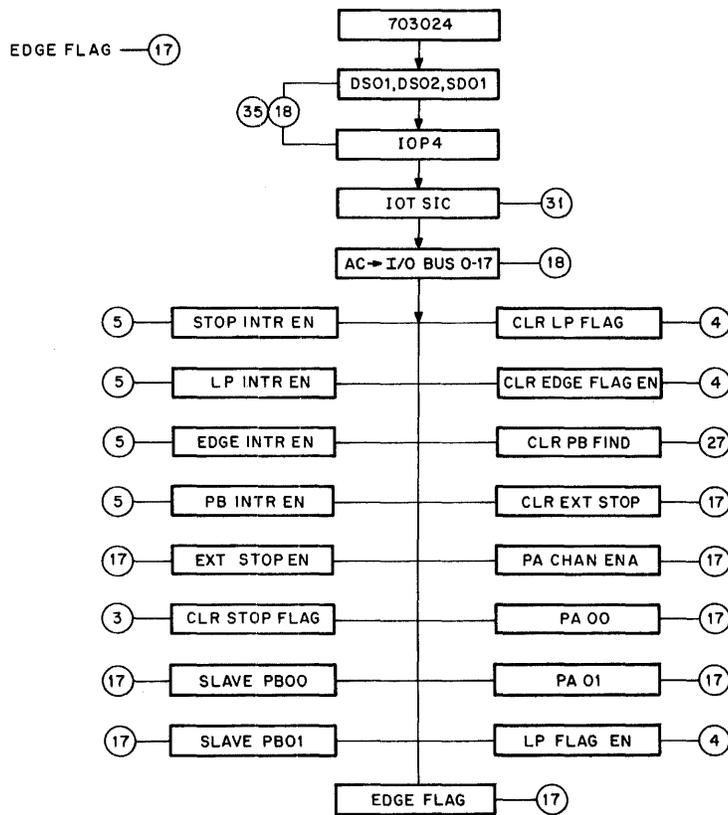
Figure 4-2   Set Initial Conditions (SIC) Flow Diagram

15-0205

4-4

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
	BLOCK 32K		BANK 8K							13 BITS OF ADDRESS							
1	1	1	0	0	0	0	1	1	0	0	0	0	0	0	1	0	0

"70"

703004

DSO1 DSO2 (35)(18)

IOP4

(31) IOT LSD

I/O BUS → PC (18)(19-24)(36)(14-16)

175 NS
(37) PC INIT
(7) LD PC

START CLR — (17) — CLR FLAGS

(40) CHAR END CLR IOPS RESET
(7) 0 → DATA AVAIL

175 NS
CLR (9)
PC → ADR (8)

250 NS
INIT LOAD (37)
SET REQ (8)
1 → OP DONE 1 → DATA REQ (7)
DATA FLAG (7)
I/O SYNC
REQ
SING CY BR (37)

I/O PROC

GRANT* (18)
ENA (37)
PC → ADDR LINE (8)(10)
(A)

*FROM I/O PROCESSOR

(A)
1 → DATA REQ (7)
1 → SING CY BR (37)
IOP4 * (37)
DATA READY (37)
I/O BUS 0-17 → IB (1)
1 → DATA AVAIL (7)
CLK (7)
1 → XFER SYNC (7)
CLK (7)
XFER (7)
IB → DB (2)
0 → OP DONE START MAIN TIMING (7)

START CLR
(4) 0 → LP FLAG EN
0 → EDGE FLAG EN
(7) 0 → CLR TIME STATE
0 → RESTART
(8) 0 → IN
0 → JMSI
(9) 0 → IOPS ASC11
0 → BYTE
(11) 0 → GRAPH
(12) 1 → SECTOR UNBLANK
0 → REF STORAGE
0 → INT ENA 0-3
(43) 0 → LP ENA 1-3
0 → LP ENA 0
(9) 0 → CLR **

CLR FLAGS
0 → EDGE FLAG
0 → SET HALT (17)
0 → HALT
0 → LP FLAG
0 → LPSI (12)
0 → STOP FLAG (3)
0 → CLR PB FIND (27)

(9)
CLR **
0 → JMS
PC → ADR
0 → JMPI
(8) 0 → RESTORE
0 → CHARST I
0 → STATUS IN
0 → PC IN
(9) 0 → JMSI CY2

(17)

100ns
XFER DELAY (7)
0 → XFER SYNC
-60
-24
-04
IN (0)
JMPI (0)
JMSI (0)
-SKIP 1 V SKIP 2
1 → DATA REQ (7)

Figure 4-3 Load and Start Display (LSD) Flow Diagram

Table 4-1
VT15 Paper Area Sizes

PA00 (Bit 11)	PA01 (Bit 12)	Size (in inches)	
		VT04	VT07
0	0	X1 (9-1/4 x 9-1/4)	X1 (12 x 12)
0	1	X2 (18-1/2 x 18-1/2)	X2 (24 x 24)
1	0	X4 (37 x 37)	X4 (48 x 48)
1	1	X4 (37 x 37)	X4 (48 x 48)

4.2.2 Load and Start Display

The load and start display (LSD) IOT command (see Figure 4-3) is used for program initialization and must always be used when a display file is initiated. It is used to initialize a data-break transfer by the PDP-15 Computer to the VT15 Graphic Processor to allow the VT15 to enter the display file. The data-break transfer is initialized by an 17-bit address word that is loaded into the accumulator of the PDP-15 Computer. This 17-bit word denotes the location of the first instruction in the display file. The address word is loaded into the VT15 when IOT command LSD is issued.

Bit 0 of the instruction is not used; bits 1 and 2 specify the particular block (32K) in which the desired address is located. Bits 3 and 4 denote the particular bank (8K), within the designated block, and bits 5 through 17 specify the desired address within the selected bank.

Thus, the LSD instruction transfers the starting address from the AC to the PC, clears all flags, and initiates a DCH break.

4.2.3 External Stop Display

The external stop display (STPD) IOT command (see Figure 4-4) causes an external stop of the display. This stop originates from the PDP-15 Computer program on the issuance of the STPD IOT command. On receipt of this IOT by the VT15 Graphic Processor, the external stop flag is raised when the VT15 stops. If the external stop enable flip-flop is set, an interrupt request will be generated.

With the issuance of a skip on external stop flag (SPES) IOT command (see Figure 4-13), a skip request is generated causing the computer program to skip on the external stop flag.

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
1	1	1	0	0	0	0	1	1	0	0	0	1	0	0	1	0	0

"70"

703044

DSO1
DSO2
SDOO

(35)(18)

IOP4

(31) — IOP STPD

1→ SET HALT

(17)

1 → HALT

NO ← OP DONE =FINISH

(7)

YES

(17) — EXT STOP

NO ← EXT STOP ENA — (5)

NO INTR

YES

DISPLY INTR — (5)(37)

API REQ (1) — (37)

INTR REQ — (5)
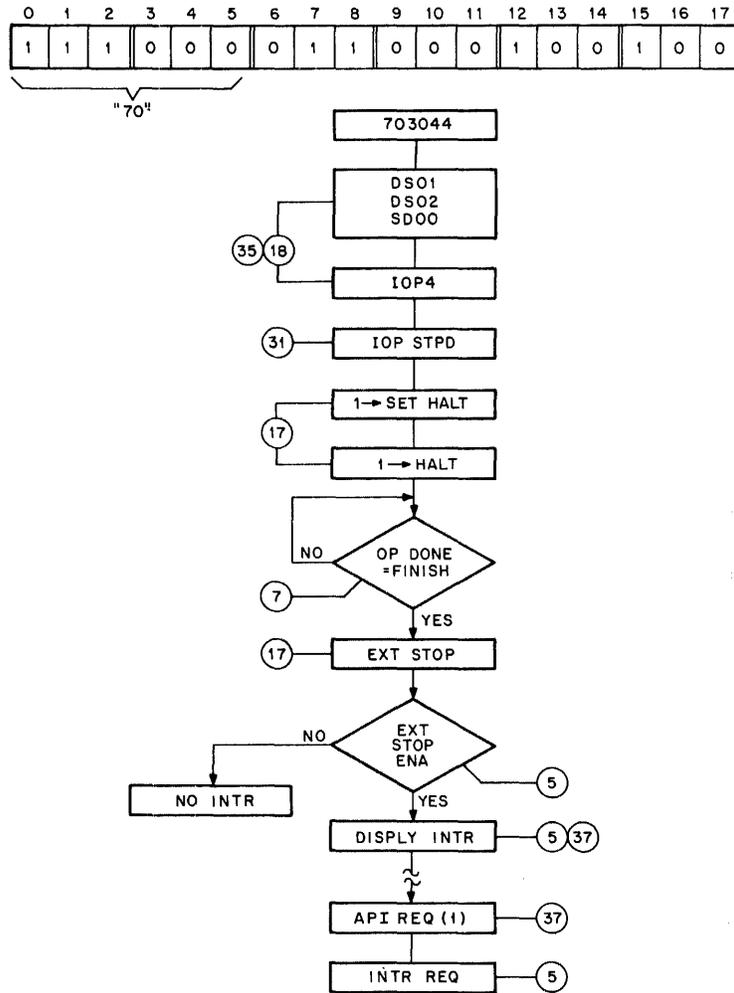
15-0207

Figure 4-4   External Stop Display (STPD) Flow Diagram

4.2.4   Resume Display After Flag

The resume display after flag (RES) IOT command (see Figure 4-5) permits the display to resume after a flag has been raised. When this IOT command is issued, clear flags is enabled to clear stop flag, light pen flag, edge flag, external stop flag, and PB bit.

4.2.5   Clear Flags

The clear flags IOT command (see Figure 4-6) is used to clear flags generated within the VT15 Graphic Processor.
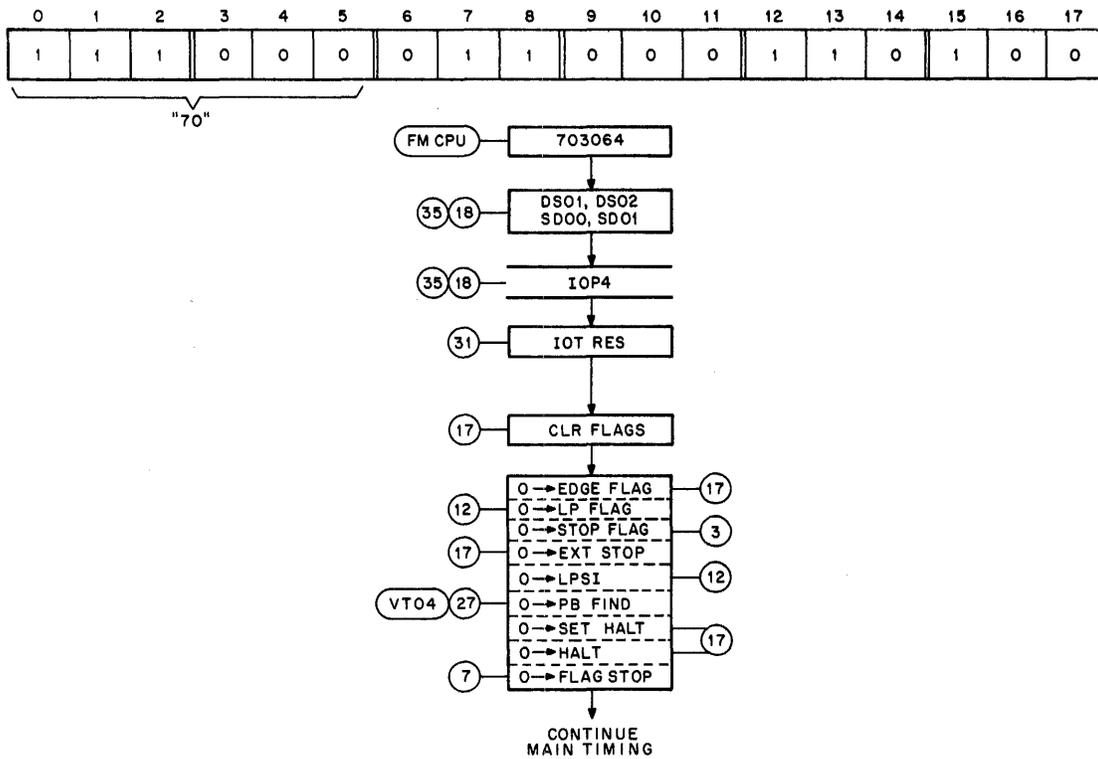
Figure 4-5   Resume Display After Flag (RES) Flow Diagram
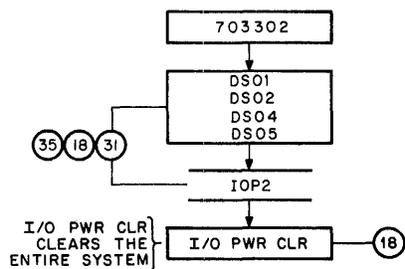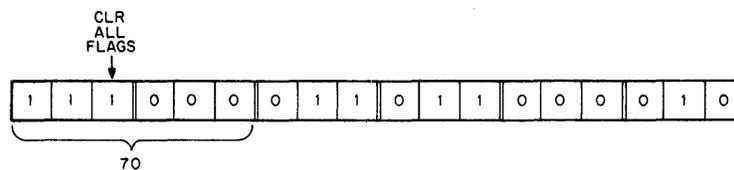
Figure 4-6   Clear Flags (CAF) Flow Diagram

Once the clear flags command is initiated, the following program-ordered flags will be cleared.

      a.   Stop flag

      b.   Light Pen flag

      c.   Pushbutton Find

      d.   Edge flag

      e.   External Stop flag

The clear flags command is normally used during initialization; however, it can also be used when a program interrupt occurs. This is especially useful when the programmer does not wish to identify the particular flag within the VT15 causing the interrupt and desires to continue with minimum time delay.

4.3   IOT SKIP COMMANDS

PDP-15 program skips are generated when any one of seven skip IOT commands are issued. The skips enabled by these IOT commands are produced by a display file stop, a VT15 external stop, when the paper area size has been exceeded, by any one of six manually-operated display console pushbuttons, by LP flag, or any interrupting flag.

4.3.1   Skip On Stop Flag

When the stop flag flip-flop is set in parameter 1 (see Figure 4-7), a stop flag is raised. The skip on stop flag (SPSF) IOT command permits the computer program to skip when the stop flag is raised.

4.3.2   Skip On Light Pen Flag

With the light pen flag flip-flop set (see Figure 4-8), a light pen flag is raised. The skip on light pen flag (SPLP) IOT command permits the computer program to skip when the light pen flag is raised.

4.3.3   Skip On Pushbutton Flag

The six pushbuttons located on the display console are controlled by the display file skip 1 instruction (see Figure 4-9) through the software. The skip on pushbutton flag (SPPB) IOT command permits the computer program to skip, through the generation of a skip request (SKIP RQ), when any of the six display console pushbuttons are depressed.

4.3.4   Skip On Edge Flag

With the parameter 2 edge flag enable flip-flop set, any violation of the paper size vertical or horizontal edge(s) will cause an edge flag to be raised. The skip on edge flag (SPEF) IOT command permits the computer program to skip when the edge flag is raised (see Figure 4-10).

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
1	1	1	0	0	0	0	1	1	0	0	0	0	0	0	0	0	1

"70"

```
                        ┌──────────────┐
                        │    703001    │
                        └──────┬───────┘
                               ▼
                        ┌──────────────┐
                        │  DSO1, DSO2  │
                        └──────┬───────┘
      (35)(18)(31)─────────────┤
                               ▼
                        ┌──────────────┐
                        │    IOP1      │
                        └──────┬───────┘
            (31)───────────────┤
                               ▼
                        ┌──────────────┐
                        │   IOT SPSF   │
                        └──────┬───────┘
                               ▼
                          ╱─────────╲
              NO        ╱    STOP     ╲        YES
         ┌───────────  ╱   FLAG SET    ╲  ───────────┐
         │             ╲      ?        ╱             │
         │              ╲─────────────╱              │
         │                    (3)                    │
         │                   (29)                    │
         ▼                                           ▼
  ┌──────────────┐                          ┌──────────────┐
(29)│  -SKIP REQ  │                          │   SKIP REQ   │(29)(35)
  └──────┬───────┘                          └──────┬───────┘
         │                                         │
         └────────────────┬────────────────────────┘
                          ▼
                     TO I/O BUS
```
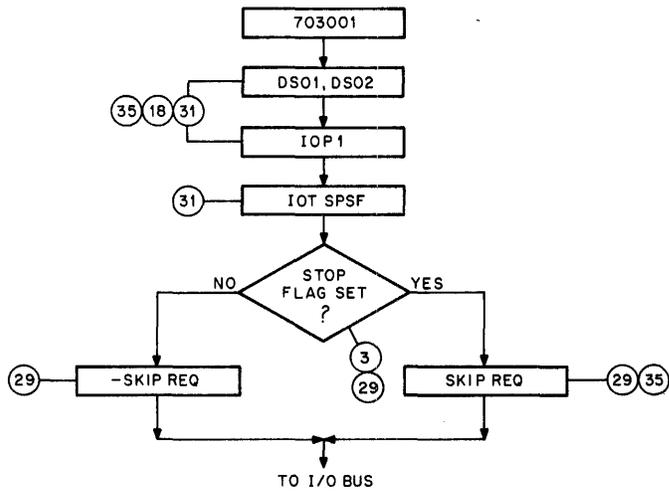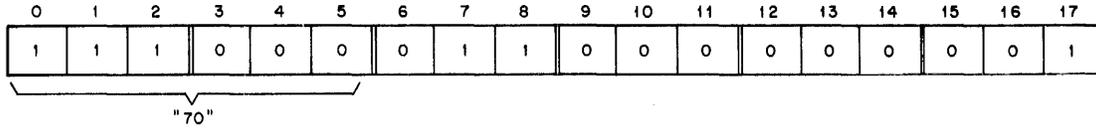
15-0209

Figure 4-7   Skip On Stop Flag (SPSF) Flow Diagram

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
1	1	1	0	0	0	0	1	1	0	0	0	0	1	0	0	0	1

"70"

```
              ┌──────────────┐
              │   703021     │
              └──────┬───────┘
                     │
              ┌──────┴───────┐
         ┌────│ DS01,DS02,SD01│
         │    └──────┬───────┘
  (35)(18)(31)       │
         │    ┌──────┴───────┐
         └────│    IOP1      │
              └──────┬───────┘
                     │
(31)─────────┌──────┴───────┐
             │   IOT SPLP   │
             └──────┬───────┘
                     │
                  ╱─────╲
                 ╱  LP   ╲
          NO    ╱ FLAG SET╲    YES
        ┌──────│     ?     │──────┐
        │       ╲         ╱       │
        │        ╲───────╱        │
        │           (12)          │
        │                         │
 ┌──────┴───────┐         ┌──────┴───────┐
(29)─│  - SKIP REQ │         │   SKIP REQ   │─(29)(35)
 └──────┬───────┘         └──────┬───────┘
        │                         │
        └────────────┬────────────┘
                     │
                TO I/O BUS
```
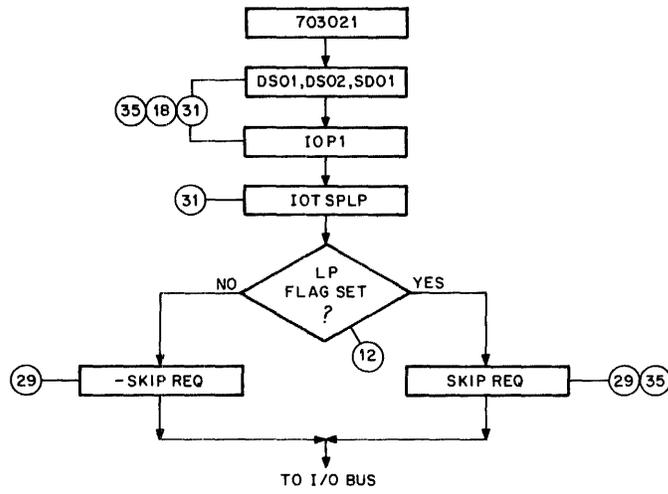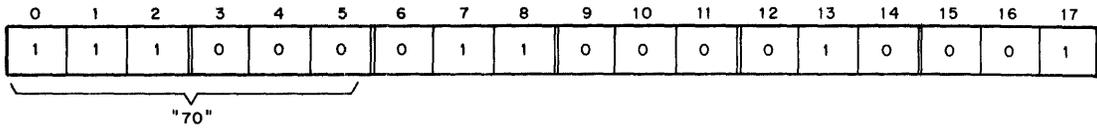
15-0210

Figure 4-8   Skip On Light Pen Flag (SPLP) Flow Diagram

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
1	1	1	0	0	0	0	1	1	0	0	0	1	0	0	0	0	1

70

703C41

DS01
DS02
SD00

㉟ ⑱ ㉛

IOP1

㉛ — IOT SPPB

PB
FIND SET

NO   YES

⑳ — -SKIP REQ   ㉘   SKIP REQ — ㉙㉟

TO I/O BUS
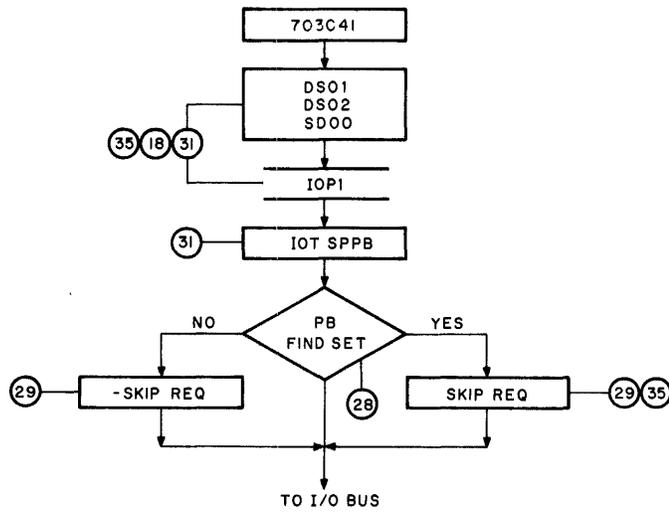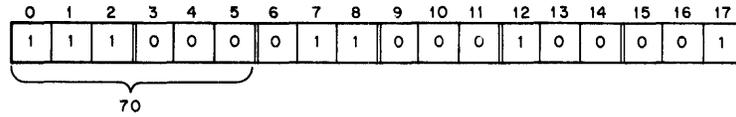
15-0211

Figure 4-9   Skip On Pushbutton Flag (SPPB) Flow Diagram

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
1	1	1	0	0	0	0	1	1	0	0	0	1	1	0	0	0	1

"70"

```
                      ┌─────────┐
                      │ 703061  │
                      └────┬────┘
                           ↓
                      ┌─────────┐
                      │  DSO1   │
                      │  DSO2   │
                      │  SDOO   │
              ┌───────│  SDO1   │
  ③⑤⑱③①      │       └────┬────┘
              │            │
              └───────  IOP1
                           ↓
              ③①──── ┌─────────┐
                      │ IOT SPEF│
                      └────┬────┘
                           ↓
                       ╱ EDGE ╲
            NO        ╱FLAG SET ╲      YES
         ┌───────────          ───────────┐
         │           ╲        ╱ ①⑦        │
         │            ╲      ╱              │
         ↓                                  ↓
  ㉙── ┌─────────┐              ┌─────────┐ ──㉙③⑤
       │-SKIP REQ│              │ SKIP REQ│
       └────┬────┘              └────┬────┘
            │                        │
            └──────────┬─────────────┘
                       ↓
                      TO
                    I/O BUS
```
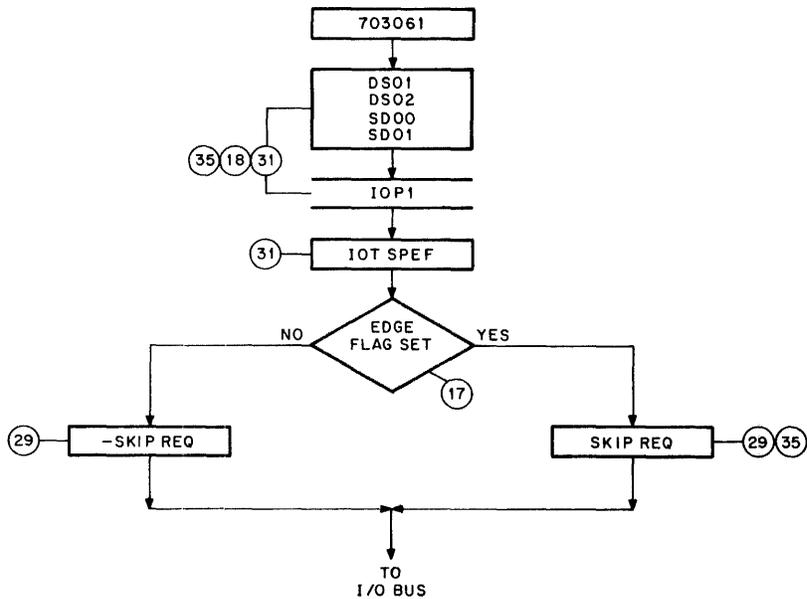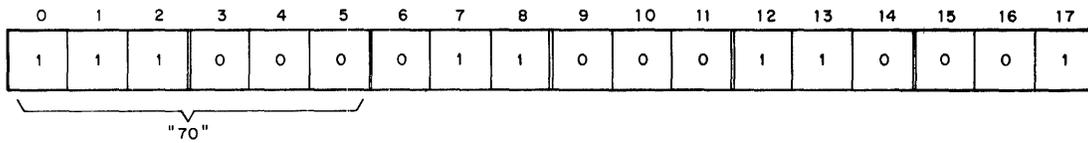
15-0212

Figure 4-10   Skip On Edge Flag (SPEF) Flow Diagram

4.3.5   Skip On Any Flag

The skip on any flag (SPDF) IOT command (see Figure 4-11) permits the computer to skip when any flag generated within the VT15 Graphic Processor is raised.

4.3.6   Skip On Any Interrupt Flag

If the parameter 3 interrupt (see Figure 4-12) is enabled, a program interrupt request will be generated if any of the following flip-flops are set, causing the associated flag to be raised:

    a.   Stop flag

    b.   Light flag

    c.   Edge flag

    d.   Pushbutton find

    e.   External stop

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
1	1	1	0	0	0	0	1	1	0	0	1	0	0	0	0	0	1

"70"
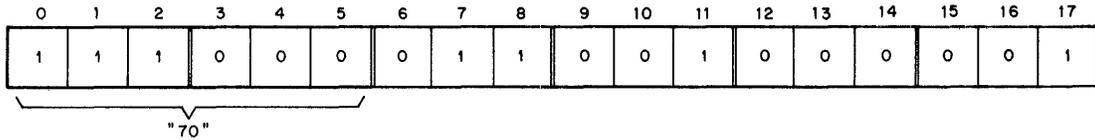
NOTE:
This instruction applies to the
following flags only;

LP FLAG (12)
EXT STOP (17)
PB FIND (28)
STOP FLAG (3)
EDGE FLAG (17)

703101

DSO1
DSO2
DSO5

(35)(18)(31)

IOP1

(31) — IOT SPDF

ANY
FLAG SET (29)

NO   YES

(29) — -SKIP REQ   SKIP REQ — (29)(35)

TO
I/O BUS
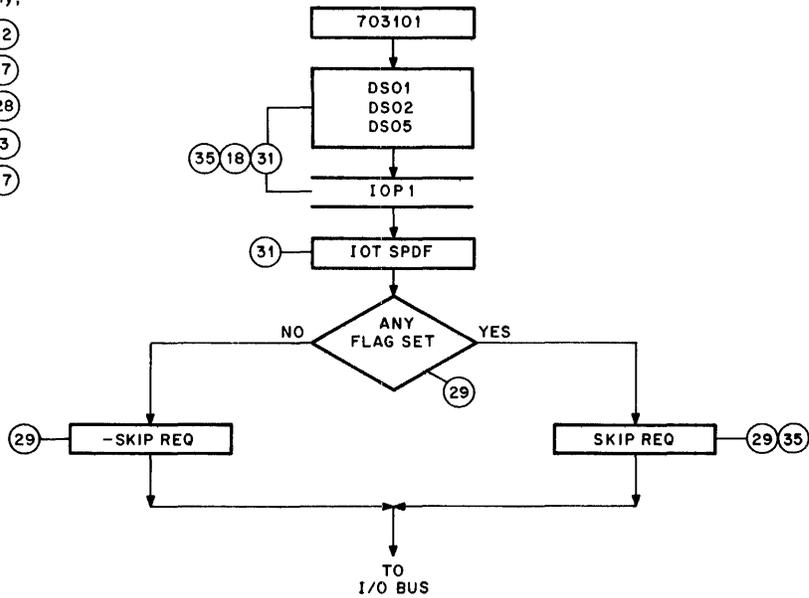
15-0213

Figure 4-11   Skip On Any Flag (SPDF) Flow Diagram

4-15

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
1	1	1	0	0	0	0	1	1	0	0	1	0	1	0	0	0	1

"70"

```
                    703121

                    DS01
                    DS02
                    DS05
                    SD01
      35 18 31
                    IOP1

      31            IOT SPDI

              NO    DSPLAY    YES
                    INTR SET
                              5

29   -SKIP REQ                    SKIP REQ    29 35

                      TO
                    I/O BUS
```
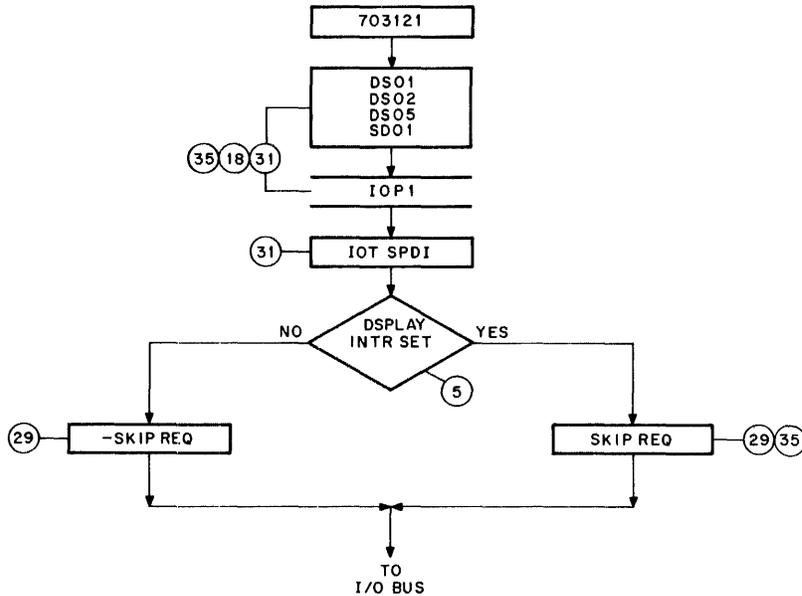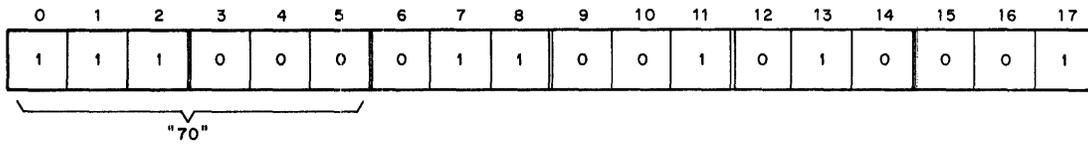
15-0214

Figure 4-12 Skip On Any Interrupt Flag (SPDI) Flow Diagram

Thus, with any one of the five flags raised and its associated parameter 3 interrupt enabled, the computer program will be interrupted, and the skip on any interrupt flag (SPDI) command will cause a computer program skip.

4.3.7 Skip On External Stop

This stop is generated by the STPD IOT command (see Figure 4-13) which originates from the PDP-15 computer. The skip on external stop (SPES) IOT instruction permits the PDP-15 Computer program to skip when the external stop flag is raised.

4.4 IOT READ COMMANDS

The VT15 read IOT commands enable the programmer to gain access to the status of various flags and the content of certain registers. This information is read into the accumulator of the PDP-15 Computer.

4-16

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
1	1	1	0	0	0	0	1	1	0	0	1	1	1	0	0	0	1

"70"
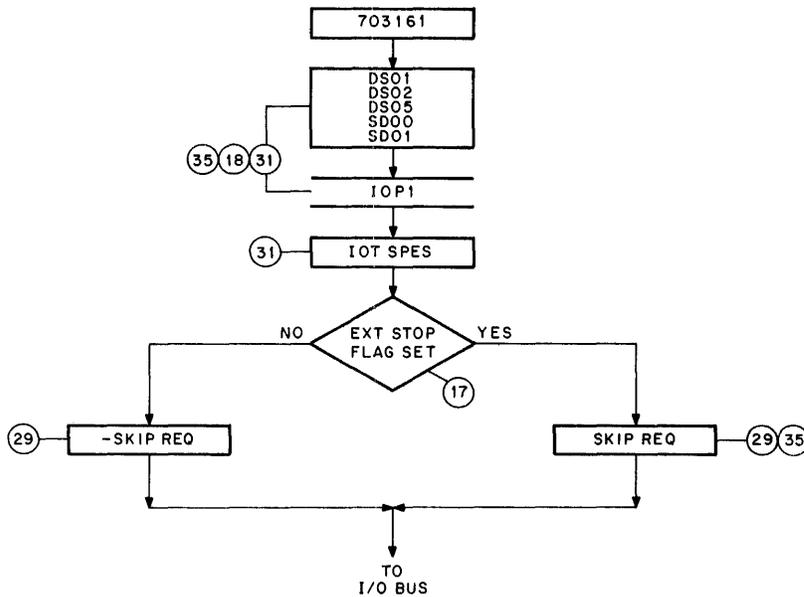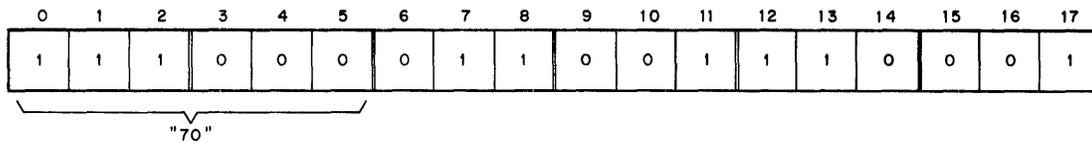
Figure 4-13   Skip On External Stop (SPES) Flow Diagram

There are six read IOT commands. Three of the read IOTs, defined as read status IOTs, examine the status of flags and parameter registers. The remaining three IOTs are used to examine the contents of three data registers: the program counter, the X-axis position register, and the Y-axis position register.

NOTE

When using the read IOT commands, clear accumulator
(CLR AC) bit 14 should be set or a logical OR of the data
in the AC will result.

4.4.1   Read Status 1

The read status 1 (RS1) command (see Figure 4-14) is used to read the status of the various parameter 1, 2, and 3 flags and registers back into the accumulator of the computer. Some of the parameters examined by RS1 are: offset, rotate, blink, paper area (size), increment, various interrupt enables, and the line register.

4-17

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
O	O	OFFSET	ROTATE	BLINK	PAOO	PAOI	INC 00	INC 01	INC 02	INC 03	STOP INTR EN	LP INTR EN	EDGE INTR EN	PB INTR EN	LP FLAG EN	LINE 00	LINE 01

1	1	1	0	0	0	0	1	1	0	0	0	0	0	0	0	1	0

"70"
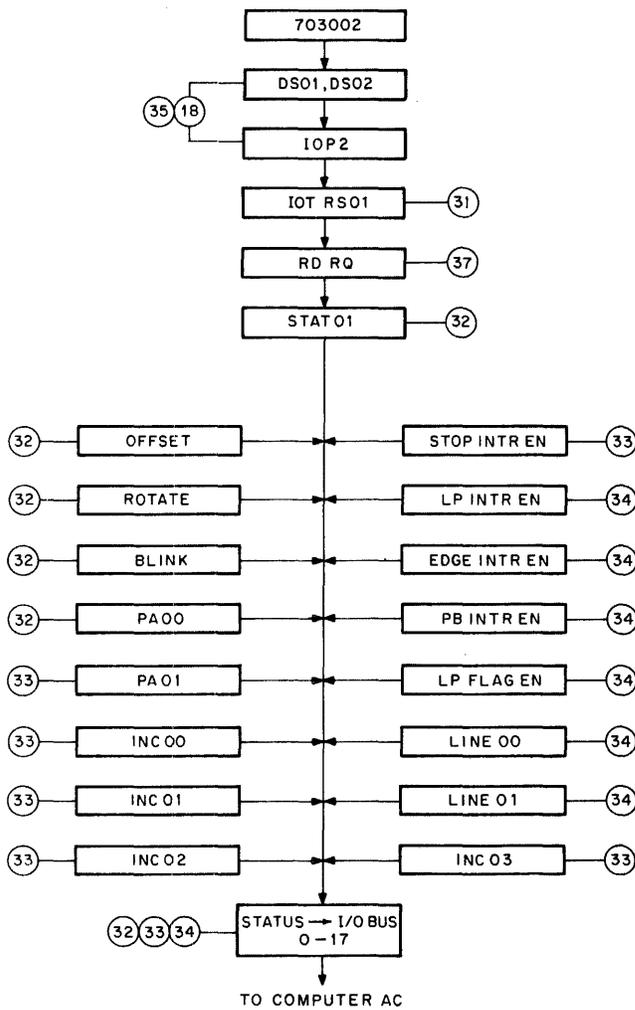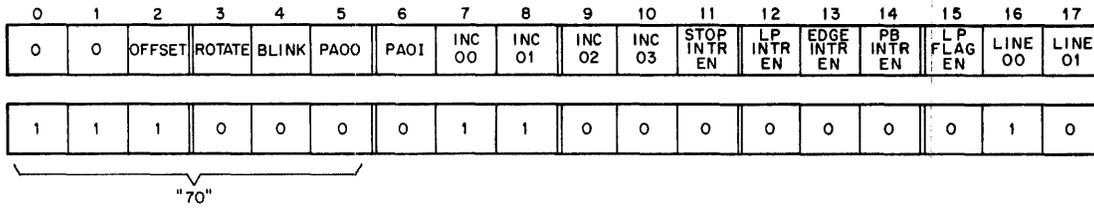
Figure 4-14   Read Status 1 (RS1) Flow Diagram

15-0217

4.4.2 Read Status 2

The read status 2 (RS2) command (see Figure 4-15) is also used to read the status of parameter 1, 2, and 3 flags and registers into the computer accumulator. Some of the parameters examined by RS2 are: pushbuttons PB00 through PB05, move, edge flag enable, the intensity register, and the name register.
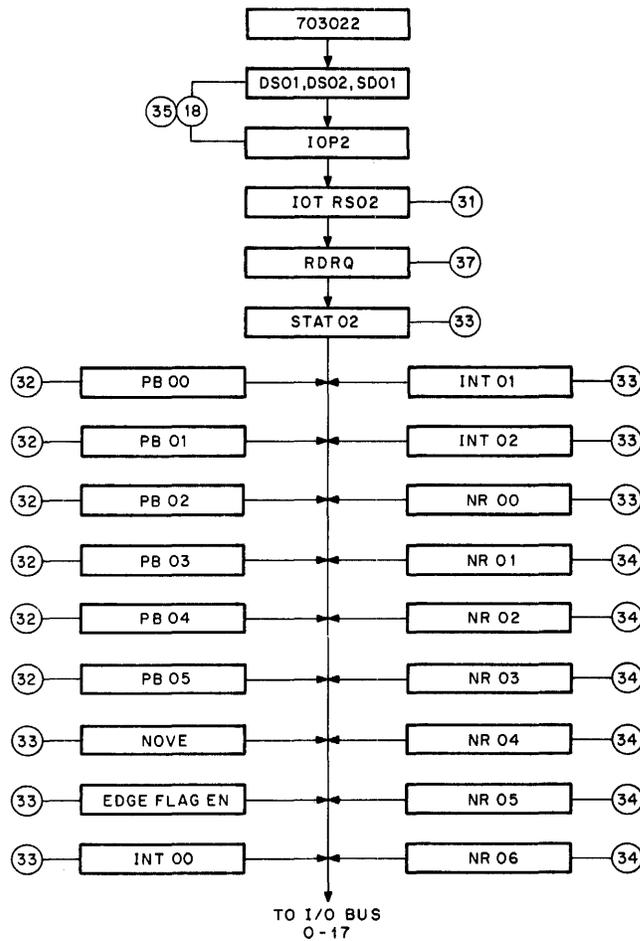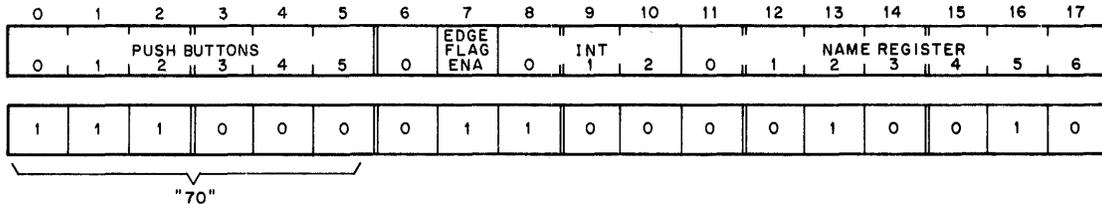
15-0218

Figure 4-15 Read Status 2 (RS2) Flow Diagram

4-19

4.4.3   Read Status 3

The read status 3 (RS3) IOT command (see Figure 4-16) is used to read the status of the following parameter 1 flags and registers back into the PDP-15 accumulator: stop flag, PB find, light pen flag, edge flag, and external stop flag.

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
STOP FLAG	PB FIND	LP FLAG	EDGE FLAG	EXT STOP	ARB VEC												

1	1	1	0	0	0	0	1	1	0	0	1	1	0	0	0	1	0

"70"
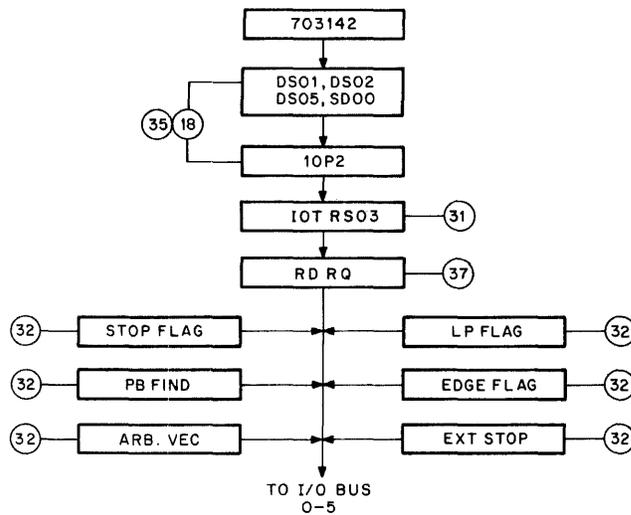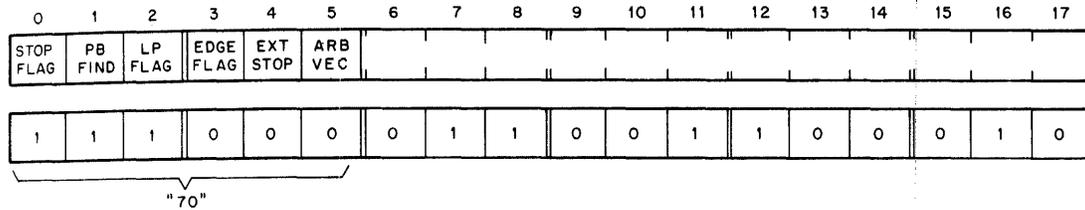
Figure 4-16   Read Status 3 (RS3) Flow Diagram

15-0219

4.4.4   Read Program Counter (RPC) Register

The read program counter (RPC) IOT command format is as shown in Figure 4-17. Bit 0 is not used. This instruction is used to read the content of the VT15 program counter register into the accumulator of the computer to allow examination of the program counter contents.

4-20

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
	PC1	PC2	PC3	PC4	PC5	PC6	PC7	PC8	PC9	PC10	PC11	PC12	PC13	PC14	PC15	PC16	PC17

| 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 |

"70"

703062

DSO1
DSO2
SDOO
SDO1

(35)(18)

IOP2

(31) — IOT RPC

(37)(35) — RD RQ

(32) — RDPC

(32)(33)(34) — PC →
I/O BUS 1-17

TO I/O BUS
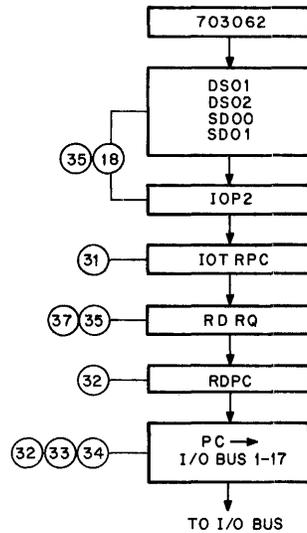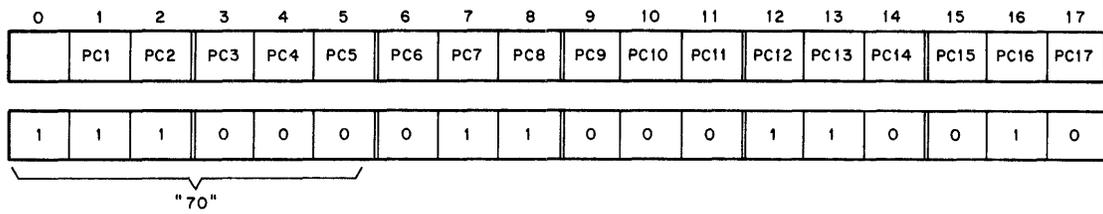
15-0220

Figure 4-17   Read Program Counter (RPC) Register Flow Diagram

4.4.5   Read X-Position Register

The read X-position (RXP) IOT command (see Figure 4-18) is used to read the status of the content of the VT15 X-position register back into the PDP-15 accumulator. Bits 0 through 4 of the instruction are unused; bit 5 is the X-position register overflow bit and is used to inform the programmer when the X-position register capacity (full paper size) has been exceeded. The remaining bits (bits 5 through 17) are read into bits 5 through 17 of the PDP-15 accumulator.

4.4.6   Read Y-Position Register

The read Y-position register (RYP) IOT command (see Figure 4-19) is used to read the status of the VT15 Y-position register back into the accumulator of the computer. Bits 0 through 17 have the same significance for the Y-axis as delineated for the RXP command in Paragraph 4.4.5.

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
					X OVER FLOW	X6	X7	X8	X9	X10	X11	X12	X13	X14	X15	X16	X17

1	1	1	0	0	0	0	1	1	0	0	1	0	0	0	0	1	0

"70"
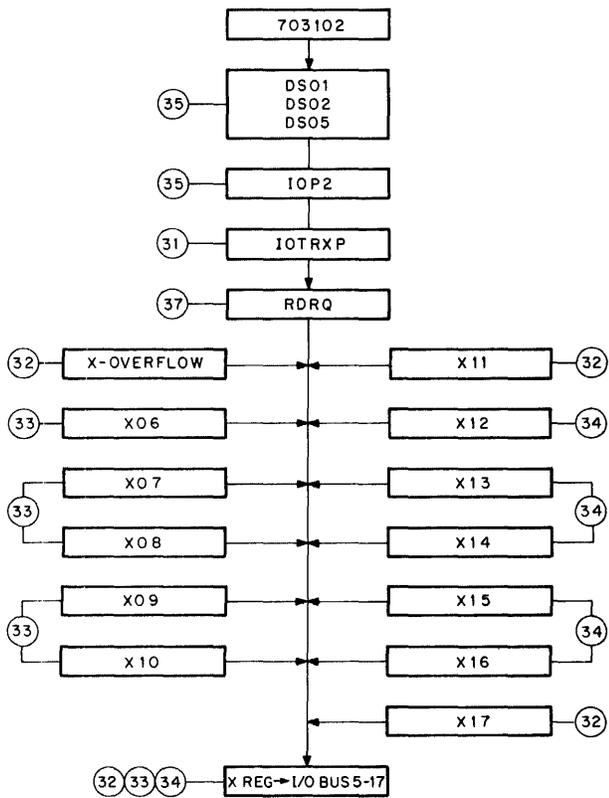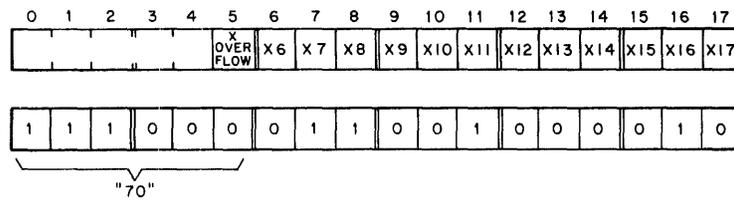
Figure 4-18   Read X-Position Register (RXP) Flow Diagram

15-0221

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
					Y OVER FLOW	Y6	Y7	Y8	Y9	Y10	Y11	Y12	Y13	Y14	Y15	Y16	Y17

1	1	1	0	0	0	0	1	1	0	0	0	1	0	0	0	1	0

"70"

703 042

DSO1
DSO2
SDO0

(35)(18)

IOP2

(31)— IOTRYP

(36)— RDRQ

(32)— Y-OVERFLOW   Y11 —(33)

(33)— YO6   Y12 —(34)

YO7   Y13
(33)
YO8   Y14   (34)

YO9   Y15
(33)
Y10   Y16   (34)

Y17 —(32)

(32)(33)(34)— Y REG→I/O BUS 5-17
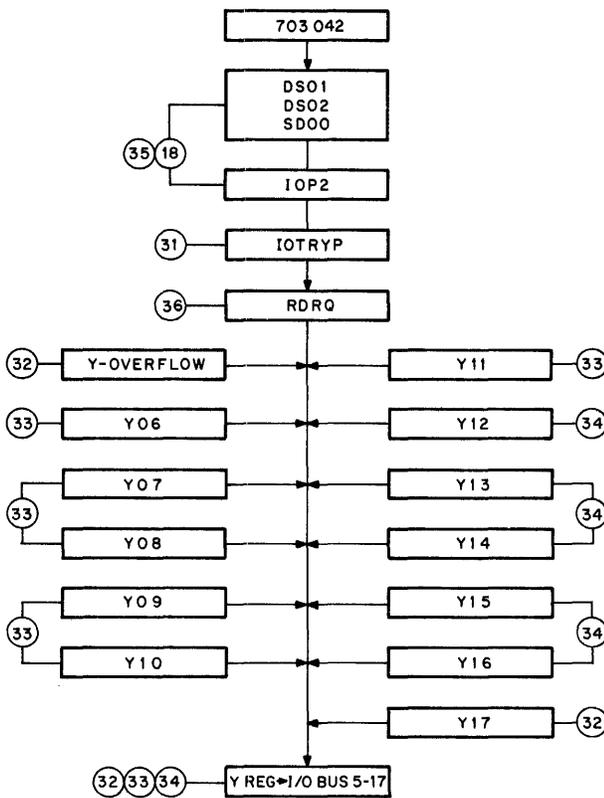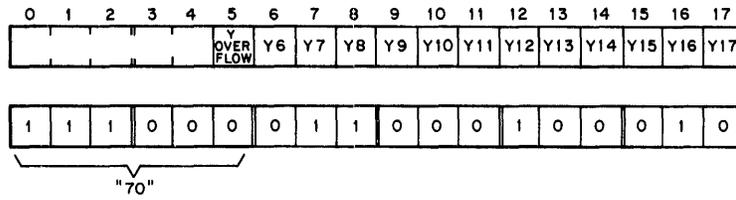
15-0222

Figure 4-19   Read Y-Position Register (RYP) Flow Diagram

4-23

4.5 VT15 GRAPHIC PROCESSOR INSTRUCTIONS

Although the VT15 Graphic Processor uses PDP-15 program-controlled transfer facilities for initialization of VT15 Graphic Processor instruction transfers, for computer skip testing, and for read status functions, the basic mode of data transfers is the single-cycle data break facility of the PDP-15 Computer. The VT15 program (called the display file) is stored in the PDP-15 Computer memory and is initially entered through program-controlled IOT commands, i.e., set initial conditions (SIC) and load and start display (LSD). The set initial conditions IOT (see Figure 4-2) is used only when its bits are of significance to display file operations. For example, before initialization and entry into the display file, the VT15 Graphic Processor registers are randomly set. These registers should be cleared initially so that when the display file is compiled, the actual content of all registers will be known.

The load and start display (LSD) IOT command (see Figure 4-3) is used as the major initializing command and effects the transfer of the contents of the computer accumulator (AC) into the VT15 Graphic Processor program counter (PC), as well as initilizes the VT15 Graphic Processor timing and data channel (DCH) word transfers from PDP-15 core memory into the VT15 data registers. Thus, the load and start display IOT must always be used for display file initialization.

When operation of the VT15 Graphic Processor has been initialized, the VT15 operates autonomously with respect to the computer through the single-cycle data break channel. Thus, with the exception of the 18 program-controlled IOT commands, all VT15 Graphic Processor instructions occur over the single-cycle data break facilities.

There are eight 18-bit instructions in the basic VT15 Graphic Processor instruction repertoire. These eight instructions are further broken down into three basic types of instructions: parameter/skip, graphic, and memory reference instructions.

    a. Parameter/Skip Instruction - This instruction is further augmented into three parameter instructions through a 3-bit register field (bits 3, 4, and 5) and into two skip instructions through a 1-bit subregister field (bit 6). The parameter/skip instructions generally establish the initial parameters of points, graph plots, vectors and characters, and PDP-15 program interrupts when flags are raised within the VT15 Graphic Processor or when pushbuttons on the display console are depressed. They also allow the display file to skip on the various programmable flags and display console pushbuttons.

    b. Graphic Instructions - The graphic instructions provide the data required to effect the actual generation of points, vectors, characters, images, etc. Once they are processed, the VT15 operates directly on these instructions so that the point plot, graph plot, vector, or character named in the data field(s) of the particular instruction is displayed directly from the display file.

    c. Memory Reference Instructions - The memory reference instructions, consisting of jump/jump-to-subroutine, save/restore, and character string are characterized by their 13-bit address fields. These 13-bit addresses are especially useful for communication with and modification of the display file.

4.5.1 Parameter/Skip Instructions

The parameter and skip instructions have 6-bit operating codes that are used to indicate any one of three parameter instructions or two skip instructions. The two skip instructions are further augmented into two subinstructions.

With one exception, the stop-flag bit, each of the individual parameters contained in the three parameter instructions has an enabling bit. When a specific parameter within an instruction is desired, its enabling bit must also be specified (set). Thus, the presence of the enabling bit ensures that only bits (parameters) that are enabled will be processed.

4.5.1.1 Parameter 1

Parameter 1 – The parameter 1 instruction (see Figures 4-20 and 4-21) uses the six-bit operating code 20_8 and is used to specify three parameters: stop flag, intensity (or brightness), and increment.

    a.   Stop Flag – With bit 6 of parameter 1 set, a stop flag is raised causing a display file halt. If STOP INTR ENA is set, a program interrupt will occur.

           The stop flag can be tested by issuing a read status 3 (RS3) IOT command (see Figure 4-17), or by the skip on stop flag IOT command.

    b.   Intensity – Modification of the intensity register is enabled only if bit 7 (INT ENA) is set. Bits 8, 9, and 10 determine the brightness or intensity of the display. Intensity is controlled in eight incremental steps between minimum and maximum intensity by specifying any octal code between 0_8 and 7_8, respectively. Normally, the intensity remains unchanged, however; in certain circumstances the intensity of a point, vector, or character may require a different intensity setting from all those previously generated.

           In such cases, a new parameter 1 instruction must be generated with bit 7 set and bits 8, 9, and 10 coded for the new value. On completion of this instruction, the parameter 1 instruction, with bits 8, 9, and 10 coded to their former values, must be restored in the display file if subsequent points, vectors, or characters are to have the originally selected intensity level.

           Bits 8, 9, and 10 can be tested by using the read status 2 (RS2) IOT command (see Figure 4-15).

    c.   Increment – The 4-bit increment parameter, comprised of bits 14, 15, 16, and 17, is enabled by bit 13 (INC ENA) and permits any vector to be repeated up to fifteen times. Vector repeatability permits graphic enlargement up to sixteen times their original size. This feature allows zooming of the displayed picture. It also permits any graph plot coordinate-point increment between 1 and 15 to be specified for beam deflection in the unnamed axis when the graph-plot method of the point/graph-plot instruction is used. Thus, when a vector or character instruction is processed by the VT15, the increment register is examined for repeatability. When a graph plot instruction is processed, the increment register is examined for the amount of beam displacement in the unspecified axis.

           The increment register can be tested by issuing a read status (RS1) IOT command (see Figure 4-14).

PARAMETER 01

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
O	1	O	O	O	O	STOP FLAG	INT ENA		INTENS				INC ENA		INCREMENT		

"20"
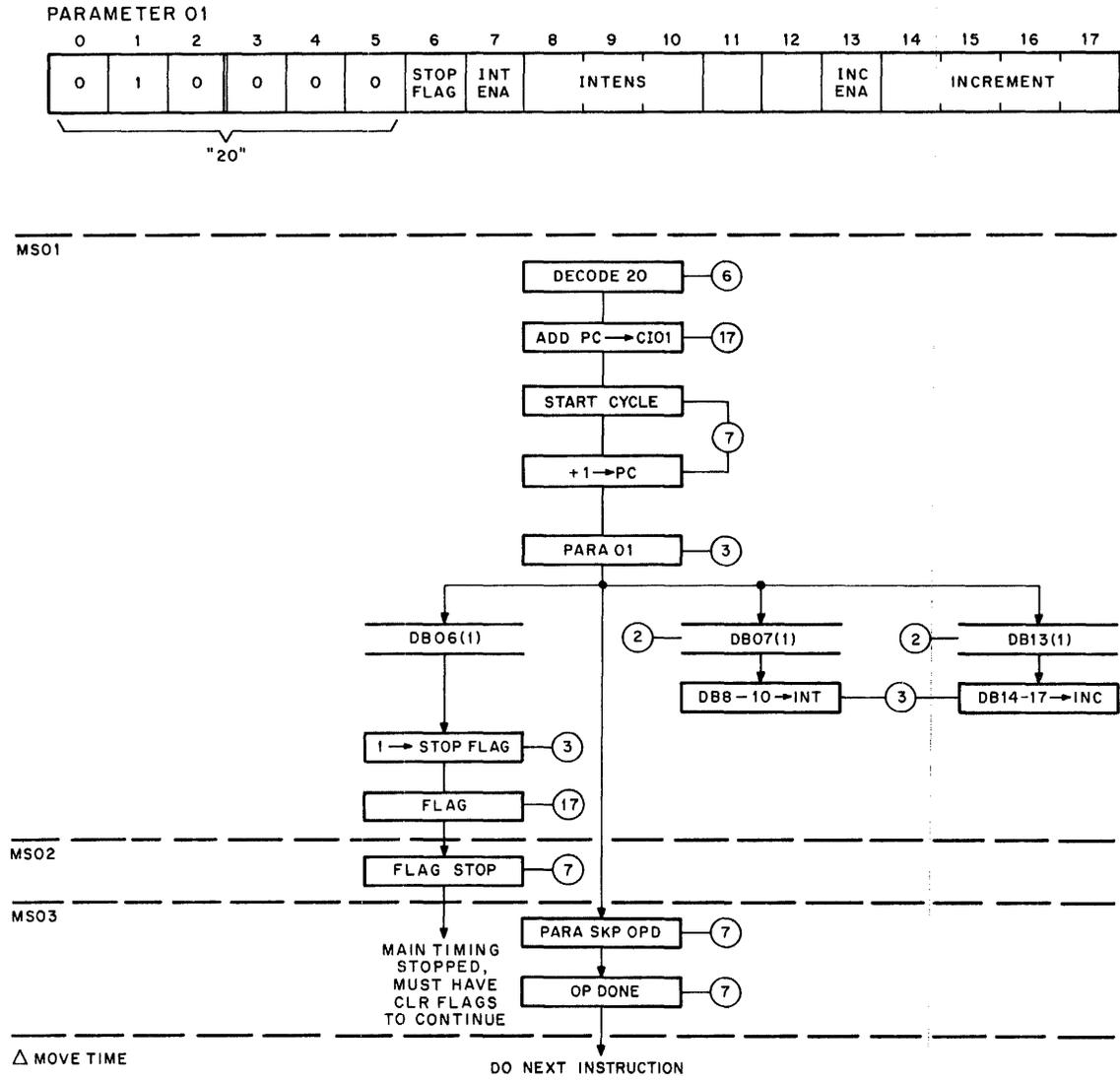
Figure 4-20   Parameter 1 Instruction Flow Diagram

15-0253

4-26

CLK

XFER SYNC

TS CLK H(XFER)

MS00

MS01

MS02

MS03

ADD PC

START CYCLE
(LDPC)

CIO1

PARAMETER 1
(LOAD:STOP FLAG,
INC.REG&INT REG)

PARA SKIP OPD

-FLAG H

OP DONE

XFER DELAY L

XFER DELAY H

SET DATA REQ H

XFER L

ADJ DELAY *
(M302 C16)

DATA FLAG H

*ADJUSTABLE ACCORDING TO SYSTEM I/O LOADING REQUIREMENTS.

15-0333
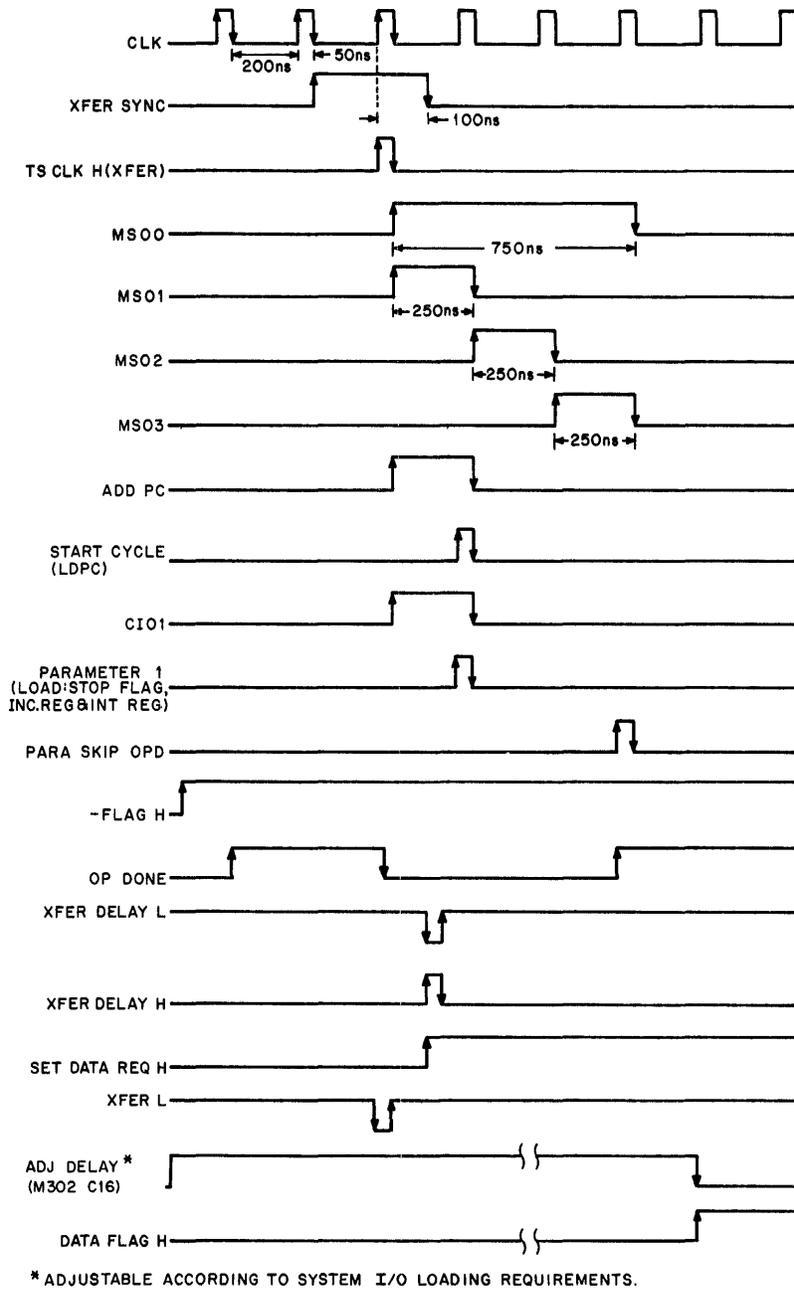
Figure 4-21   Instruction Basic Timing Diagram

The intensity parameter (bits 8, 9, and 10) and increment parameter (bits 14, 15, 16, and 17) can also be tested through the save/restore instruction (see Figure 4-37). When this instruction is used, the respective parameters, including intensity and increment parameters, can be collected from their respective registers and examined. When bit 4 of the save/restore instruction is set, the parameters are restored into the display file. When bit 4 is not set, the parameters are saved. Parameters that normally are unchanged are saved into some location in the PDP-15 core memory and are restored after the desired display file functions or changes have been programmed.

4.5.1.2 Parameter 2 – The parameter 2 instruction (see Figure 4-22) utilizes the 6-bit operating code 21_8 and is used to specify six parameters: escape mode, blink, edge, rotate, light pen, and offset.

    a. Escape – Escape (ESC) mode is used in conjunction with the character string instruction (see Figure 4-41). With bit 6 of the parameter 2 instruction set, the parameter 2 escape mode is enabled, and bit 7 is read. If bit 7 is set, an ALT MODE or CR from VT15 address and character generator control will terminate the character string instruction. If bit 7 is not set, then only ALT MODE will enable the escape mode.

    b. Blink – Blink is normally used to emphasize certain single characters, or vectors. When the character, or vector is written, it blinks at a rate of approximately four times per second. When blink enable bit 8 is set, blink, bit 9 is loaded into the blink register. All characters or vectors generated thereafter, blink until the register is reset, again using the parameter 1 instruction to reset the blink control flip-flop.

       The status of the blink bit can be tested by issuing the Read Status 1 (RS1) command (see Figure 4-14). The status of the blink bit can also be examined through the Save/Restore instruction (see Figure 4-37).

    c. Edge – The paper area (PA) or size is initially chosen through the SIC IOT command, bits 10 and 11. Edge is used to inform the operator that the chosen paper area has been exceeded. Bit 10 of the parameter 2 instruction is used as the EDGE FLAG ENA bit, and ON/OFF bit 11 is used as the edge control bit.

       With edge flag enable bit 10 of the parameter 2 instruction enabled (set), edge control bit 11 sets the edge flag enable flip-flop. When an edge violation occurs, an output will be generated to the edge flag logic, causing an edge flag to be raised and a display halt to occur.

       With edge flag interrupt enable (of parameter 3) set in conjunction with edge flag, a program interrupt occurs causing a display halt. The edge flag can also be used to produce a computer skip by issuing the skip on edge flag (SPEF) IOT command (see Figure 4-10).

       The status of the edge flag bit can be tested through the read status 2 (RS2) IOT command (see Figure 4-15).

    d. Rotate – Rotate is used by the operator to rotate basic vectors or characters 90° counterclockwise. If the rotate bit (bit 13) of the parameter 2 instruction is set, rotate bit 13 and rotate enable bit 12 will be loaded into the rotate register whose output is then applied to the rotate 1 and 2 logic. All vectors and characters generated thereafter will be rotated 90° counterclockwise. Refer to Paragraph 4.5.11 and Figure 4-46.

4-28

Figure 4-22 Parameter 2 Instruction Flow Diagram

e. Light Pen - Light pen is used to detect any intensified part of the display. In cases where the basic vector, basic short vector, point/graph plot, character input, and arbitrary vector instructions are used, each of these instructions has special light pen enable bits that are used to sense the named vector, coordinate point, or character.

With light pen enable bit 14 of the parameter 2 instruction set, the light pen bit will be loaded into the light pen enable flip-flop. If light pen flag bit 15 is set, a light pen flag will be generated at any time a light pen hit occurs.

If a skip on light pen (SPLP) IOT instruction (see Figure 4-8) is generated in conjunction with light pen flag, a program skip will be generated. A program interrupt will occur if the light pen flag is raised and bits 10 and 12 of parameter 3 (see Figure 4-23) are set. Light pen flag can be tested by issuing a read status 1 (RS1) IOT command (see Figure 4-14).

f. Offset - If the minor image area is to be used, parameter 2 offset bits 16 and 17 must be enabled. When offset enable bit 16 is set, offset control bit 17 will be loaded into the offset register, and subsequent graphics can be drawn in the minor image area.

4.5.1.3 Parameter 3 - The parameter 3 instruction (Figure 4-23) uses the 6-bit operating code 22_8 and is used to enable program interrupts for various skip conditions. There are four flags that can cause a program interrupt if their corresponding interrupt enable bits in the parameter 3 instruction are set: stop flag, light pen hit flag, edge flag, and pushbutton flag. The stop flag, light pen hit flag, and edge flag will also cause a display file halt. Thus, a program interrupt will occur when any one (or all) of the flags is raised. The pushbutton flag will be enabled (or raised) when any one of the six pushbuttons on the display console are used to perform functions. Thus, there are a total of nine sources of program interrupts in the Graphic 15 system and two types of interrupts in the PDP-15 Computer: ordinary (program) interrupts and automatic priority interrupts (API).

In the ordinary interrupt system, the program interrupt facility is enabled by programming an ION instruction, causing an interrupt enabling flag to be raised. If one of the display flags is set and the corresponding interrupt enabling flag is raised, an interrupt request will be generated. However, before any of the interrupt registers can be changed, bit 10 of the parameter 3 instruction must be set, or the set-initial-conditions (SIC) IOT command (see Figure 4-2) must be issued with the proper bits set in the SIC word. With one of the above conditions satisfied and the interrupt enabling flag raised, the PDP-15 Computer program will trap to location 0 at the conclusion of the current instruction being executed. The program count is stored at location 0 and the subsequent instruction, location 1, names a subroutine specified by the programmer to identify the source of the interrupt. When the interrupt source is identified, its corresponding flag must also be identified. In the Graphic 15 this can easily be done by issuing a read status 1 (RS1) IOT command. Parameter 3 individual parameters are as follows:

a. Stop Flag Interrupt Enable - With bit 11 of parameter 3 set in conjunction with bit 6 of the parameter 1 instruction, a program interrupt will occur causing a display file halt.

PARAMETER 03

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
0	1	0	0	1	0		NOT USED			INTR ENA	STOP INTR ENA	LP INTR ENA	EDGE INTR ENA	PB INTR ENA	LINE ENA	2-BITS LINE	

"22"

MSO1

DECODE 20 —(6)

START CYCLE —(7)

+1→PC —(7)

PARA 03 —(5)

DB10(1)

DB15(1)

DB16 & BDB17→ LINE 00 & 01 —(5)

TO LINE LOGIC —(12)

DB11(1) DB11(0) DB12(1) DB12(0) DB13(1) DB13(0) DB14(1) DB14(0)

1→STOP INTR EN 0→STOP INTR EN 1→LP INTR EN 0→LP INTR EN 1→EDGE INTR EN 0→EDGE INTR EN 1→PB INTR EN 0→PB INTR EN

(5) (5) (5) (5)

TO INTR LOGIC —(5)

MSO2
MSO3

PARA V SKP OPD —(7)

OP DONE —(7)

△ TIME

TO I/O BUS —(35)

15-0244

DO NEXT INSTRUCTION

Figure 4-23   Parameter 3 Instruction Flow Diagram

4-33

b. Light Pen Flag Interrupt Enable - With the light pen flag of parameter 2 raised and LP INTR ENA bit 12 of the parameter 3 instruction set, a program interrupt will occur causing a display file halt.

c. Edge Flag Interrupt Enable - With the edge flag raised and EDGE INTR ENA bit 13 of parameter 3 set, a program interrupt will occur causing a display file halt.

d. Pushbutton Interrupt Enable - PB INTR ENA bit 14 of the parameter 3 instruction is used in conjunction with the six pushbuttons (PB$_0$ through PB$_5$) located on the display console and bits 9 through 13 of the skip 2 instruction. Parameter 3 bit 14 serves as the enabling bit for the PB INTR EN flip-flop. If bit 14 of parameter 3 is set and PB FIND is received from the display console, a program interrupt will occur. Thus, of the nine possible sources of interrupts in the Graphic 15, six are derived from the six display console pushbuttons.

e. Line - Bit 15 of the parameter 3 instruction is used as the enabling bit for parameter 3 line selection bits 16 and 17. These two bits permit four alternate dashed-vector combinations as shown in Table 4-2. Timing for the line function is shown in Figure 4-24.
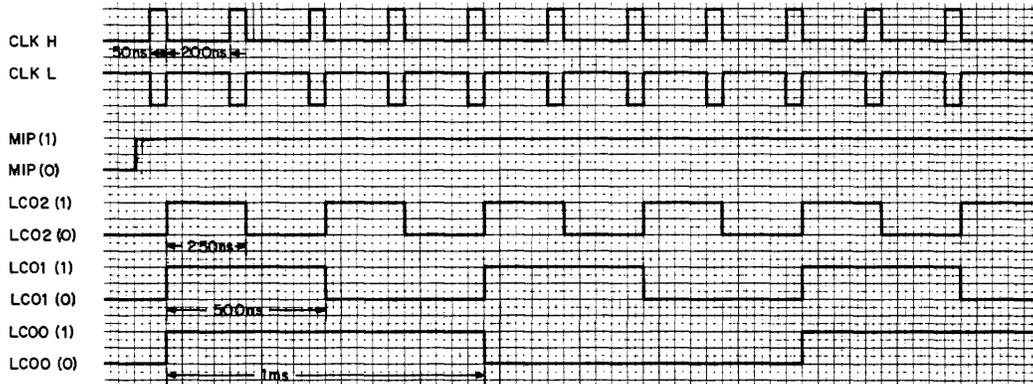
Figure 4-24   Line Function Timing

Table 4-2
Line Pattern Codes

Line Pattern	Line Code		Display Ratio (On to Off)
	Bit 16	Bit 17	
	0	0	Always on
	0	1	6 lines on; 2 lines off
	1	0	3 lines on; 1 line off
	1	1	1 line on; 1 line off
Note: One line length is equal to 0.06 in.			

4.5.1.4 Skip 1 – The skip instructions use the 6-bit operating code 23_8 and are further divided into subinstructions with the operating subcodes: 230_8 for skip 1 and 234_8 for skip 2. The skip 1 and skip 2 instructions differ from the IOT skips in that they do not deal exclusively with skips, but are used to specify other parameters.

The skip 1 instruction (see Figure 4-25) is used to specify five parameters: skip on light pen sense indicator, clear after test, skip on pushbutton, pushbutton enable, and unit select.

    a. Skip on Light Pen Sense Indicator (LPSI) – With bit 7 of the skip 1 instruction set, the LPSI flip-flop will be sensed. If a light pen hit has occurred, the LPSI flip-flop will be set and a display file skip will occur. At the conclusion of this instruction the LPSI flip-flop will be cleared.

    b. Clear After Test – When any of the display console pushbuttons are operated (PB_0 through PB_5), the corresponding pushbutton logic for the particular pushbutton will be enabled and its indicator will light. When bit 8 of the skip 1 instruction is set at the beginning of time state 3 (MS03), the pushbutton logic is disabled, clearing the selected pushbutton(s) and turning the pushbutton indicator lamp(s) off. PB BUS ENA is also generated at this time (MS03).

       If the pushbutton logic is to be cleared immediately after a skip is performed, bit 9 of the skip 1 instruction should also be set. Thus, when the particular pushbutton is depressed, the pushbutton logic is only momentarily set (enabled) if a display file skip occurs. At the beginning of MS03, the pushbutton logic is disabled. Though the corresponding pushbutton indicator is made during this sequence, the sequence occurs so rapidly that no visible indication will be observed.

    c. Skip on Pushbutton – With bit 8 of the skip 1 instruction reset and bit 9 set, and with one of the pushbutton enable bits (bits 10 through 15) set, a display file skip will occur if the pushbutton corresponding to the enabled bit is depressed. If bit 9 is not set, and one of the pushbutton enable bits (bits 10 through 15) is active (set), the associated display light corresponding to the enabled bit will light providing a visual indication to the operator.

       The status of the pushbutton logic can be tested through the read status 2 (RS2) IOT command.

    d. Pushbutton Enable – Bits 10 through 15 of the skip 1 instruction refer to the pushbutton enable logic for PB_0 through PB_5, respectively, and are used in conjunction with bits 8 and 9 as described in the paragraph above.

    e. Unit Select – When the Type VM15 Display Console Multiplexer option is used with the VT15 Graphic Processor, more than one display console can be interfaced with the VT15. Bits 16 and 17 are used in various combinations to allow the selection of one specific pushbutton bank or display console. The pushbutton bank address codes are as shown in Table 4-3.

4.5.1.5 Skip 2 – As previously indicated, the VT15 skip instructions use the 6-bit operating code 23_8 with both the skip 1 and skip 2 instructions further divided into subinstructions (subcodes). The skip 2 instruction (see Figure 4-26) uses subcode 4_8 (or 234_8).
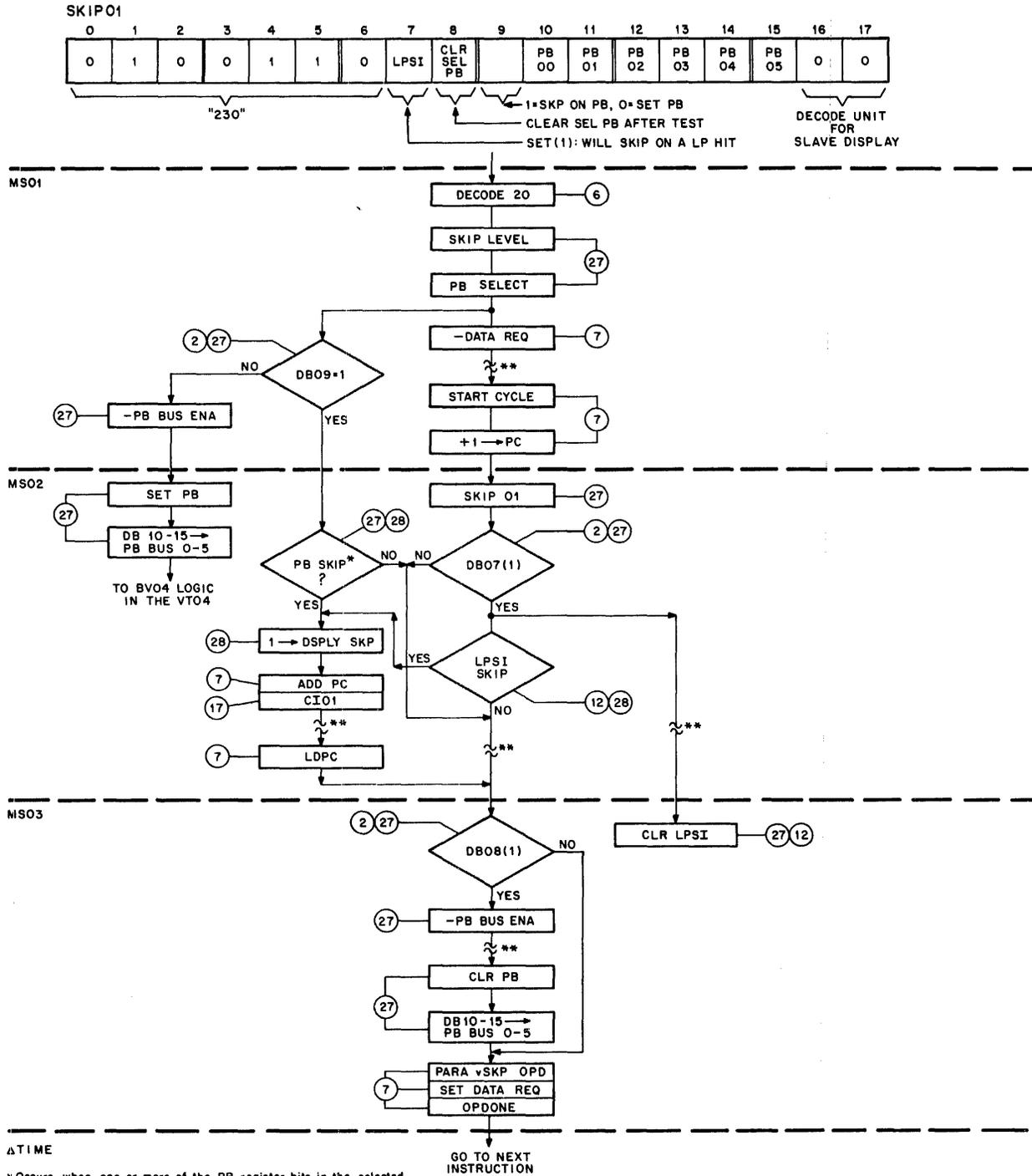
Figure 4-25 Skip 1 Instruction Flow Diagram

15-0255

4-36

Table 4-3
Pushbutton Bank Address Codes

Instruction Bit		Pushbutton Bank
16	17	
0	0	Used for only one bank
0	1	Optional Bank 1
1	0	Optional Bank 2
1	1	Optional Bank 3

The skip 2 instruction, like the skip 1 instruction, does not deal with skips exclusively, but is used to specify other parameters. The parameters specified in the skip 2 instruction are: halt and resume in sync, skip unconditionally, load name register, skip on name word, and name word enable.

a. Halt and Sync to Line Frequency - Bit 7 of the skip 2 instruction is used as the enabling bit to synchronize VT15 operation with the incoming 60-Hz line frequency. With bit 7 set, the display file will halt. When the incoming sample line frequency passes a pre-set threshold, a trigger pulse is produced enabling SYNC RESUME. The display resumes, now synchronized with the line frequency.

b. Skip Unconditionally - With bit 8 of the skip 2 instruction set, an unconditional skip will occur in the display file.

c. Load Name Register - The name register is a 7-bit register capable of storing up to 128 binary codes. These codes can be used to tag subroutines for future identification, as well as with light pen hits and skips, and the read status 1 (RS1) IOT command to provide a wide range of programming alternatives.

When bit 9 of the skip 2 instruction is set, a 7-bit word consisting of bits 11 through 17 of the instruction will be loaded into the hardware name register.

d. Skip On Name Word - With bit 10 of the skip 2 instruction set, the name register (bits 11 through 17) can be examined through a skip test. When bit 10 is set, the name register will be examined. If the content of the current skip code and the name register are different the desired name register code will set into bits 11 through 17 of the skip 2 instruction. If the content of the current skip code and the name register are the same, a display file skip will occur.

e. Name-Word Bits NW_0 through NW_6 - Bits 11 through 17 are used in two ways: with bit 9 of the skip 2 instruction set, bits 11 through 17 will be set. With bit 10 set, a skip test will occur to test the content currently stored in the name register.

4.5.2 Basic Vector

The basic vector instruction (see Figure 4-28) has a literal 3-bit operating code 40_8 that is decoded by the VT15 instruction decoder as a 40_8, though only bits 0, 1, and 2 are used. This instruction provides the parameter and data fields required to draw a 9-1/2 in. (full length) vector in any one of eight directions as shown in Figure 4-27.
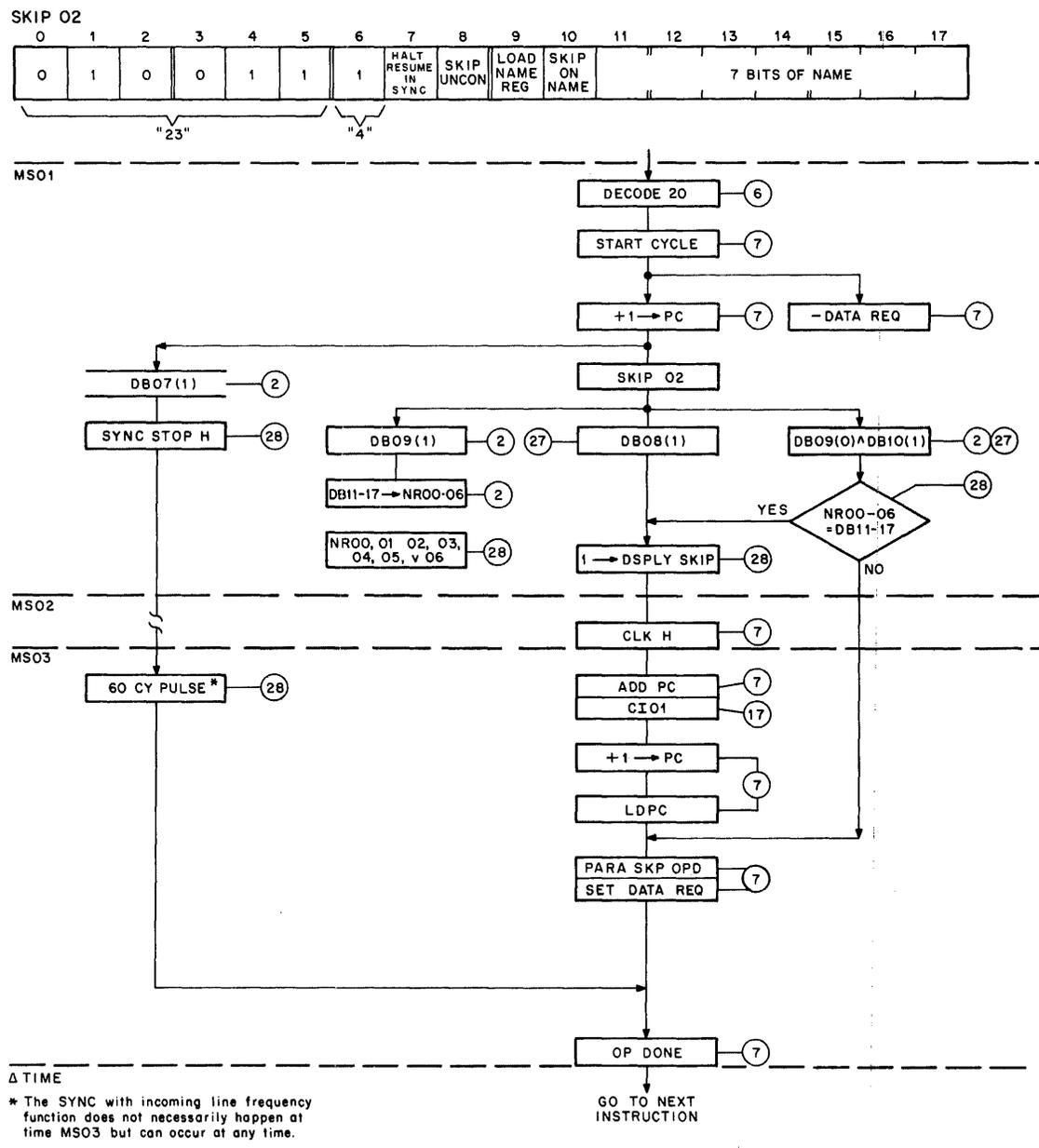
Figure 4-26   Skip 2 Instruction Flow Diagram

15-0256

4-38

```
                    2
          3         ↑         1
            ↖       |       ↗
               ↖    |    ↗
    4 ←──────────── + ────────────→ 0
               ↙    |    ↘
            ↙       |       ↘
          5         ↓         7
                    6
```

15-0228
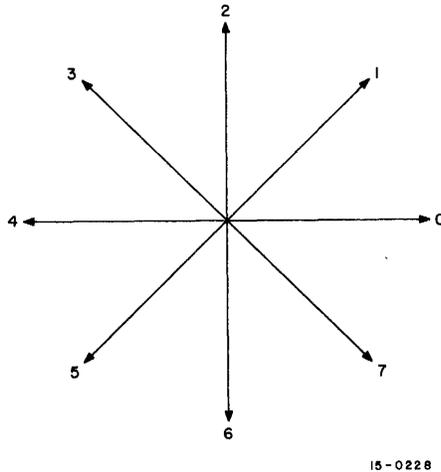
Figure 4-27   Eight Basic Vector Directions

The basic vector instruction is used to specify four parameters: light pen enable, intensity, direction and delta (or magnitude).

    a.   Light Pen Enable - When set (enabled), light pen bit 3 allows a light pen hit, but only on the vector specified by the direction and delta fields of the current basic vector instruction.

    b.   Intensity - Intensity enabling bit 4 permits the vector to be intensified as it is being drawn if bit 4 is set. If bit 4 is not set, the vector will not be intensified and will not be visible.

    c.   Direction - Bits 5, 6, and 7 comprise the basic vector instruction direction field. This three-bit field provides the eight binary codes necessary to specify the eight directions utilized in this instruction as shown in Table 4-4, and Figure 4-27.

    d.   Delta (Magnitude) - Bits 8 through 17 enable any logical length between 0.0 and 9.5 in. to be specified.

        The basic vector instruction can be modified further through the use of the parameter instructions: parameter 1, 2, and 3 (Figures 4-21, 4-22, and 4-23). Some of the parameters contained in the three parameter instructions that are used to modify the basic vector instruction are: brightness or intensity, rotation, repeatability, blink and dash.

4.5.3   Basic Short Vector

The basic short vector instruction (see Figure 4-29) uses the literal 3-bit computer operating code 5_8 which, when decoded by the VT15 instruction decoder, equates to 50_8 when compared with other VT15 operating codes. The basic short vector instruction uses two 3-bit direction fields and two 3-bit delta (magnitude) fields to permit two short vectors to be specified, as opposed to only one vector in the basic vector instruction described in Paragraph 4.5.2. Maximum individual short vector length is approximately 0.063 in. (see Figure 4-30).
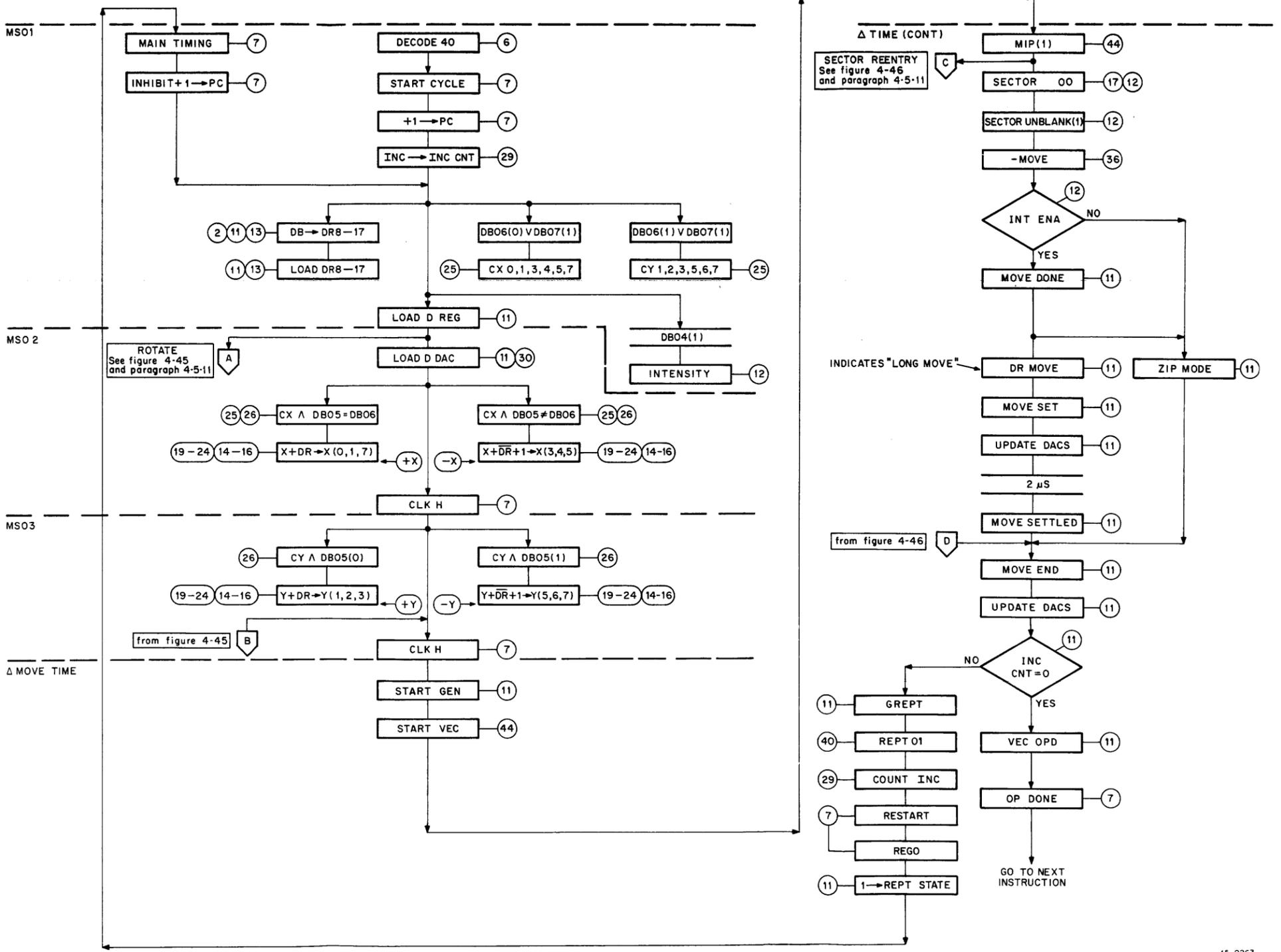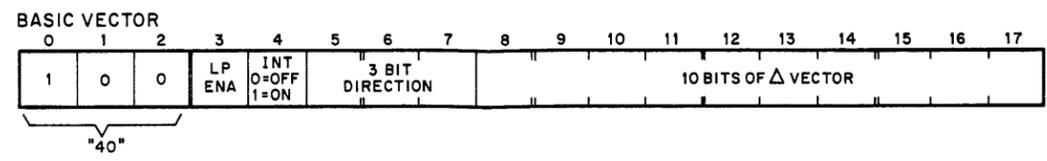
Figure 4-28 Basic Vector Instruction Flow Diagram

15-0263

Table 4-4
Basic Vector Directions

Direction Code Bits 5, 6, and 7	Vector Number	Axis
000	0	+X, 0
001	1	+X, +Y
010	2	0, +Y
011	3	-X, +Y
100	4	-X, 0
101	5	-X, -Y
110	6	0, -Y
111	7	+X, -Y
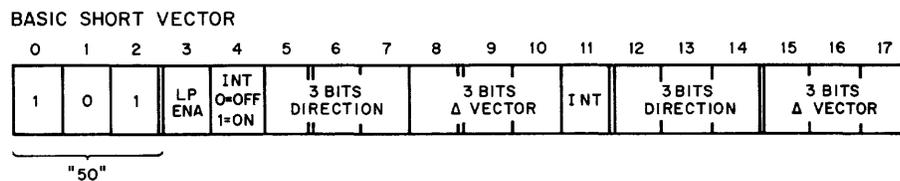
BASIC SHORT VECTOR

Figure 4-29 Basic Short Vector Instruction Format

The basic short vector instruction is used to specify four parameters: light pen enable, intensity, direction, and delta (magnitude). The light pen enable bit is used with the first and second short vector parameters of the instruction. The intensity, direction, and delta (magnitude) parameters are specified as separate values for each of the two short vector parameters.

a. Light Pen Enable - Bit 3 is used as the light pen enable bit as previously described in the basic vector instruction, Paragraph 4.5.2 and Figure 4-28.

b. Intensity - In the basic short vector instruction, two intensity enabling bits are specified, bits 4 and 11, for the first and second short vectors, respectively. With the bit(s) set, the vector(s) will be intensified; if the bit(s) are not set, the vector(s) will not be visible.

c. Direction - Bits 5, 6, and 7 define any one of eight directions for the first short vector in the instruction; bits 12, 13, and 14 provide the same function for the second short vector of the instruction.
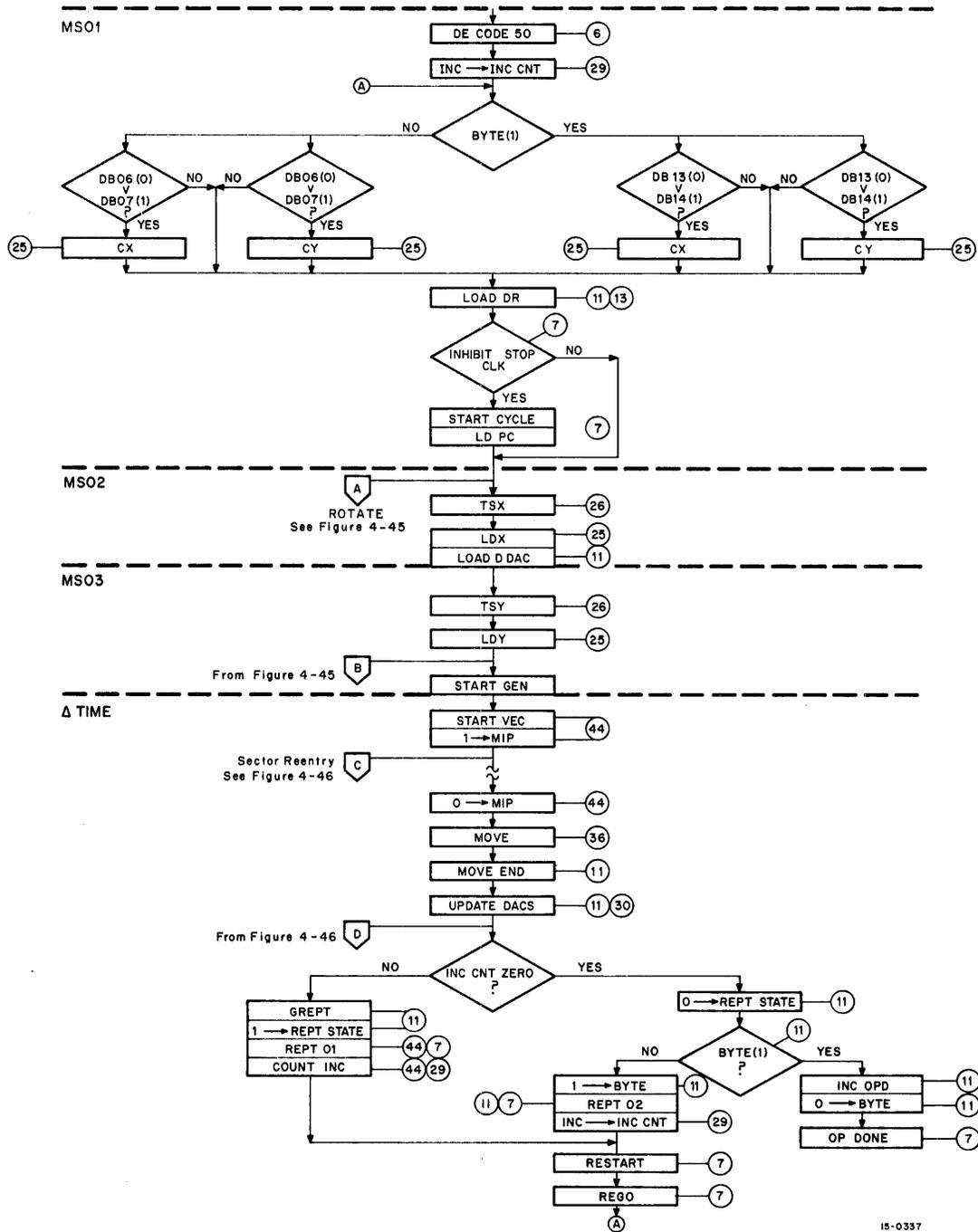
Figure 4-30   Basic Short Vector Instruction Flow Diagram

d. Delta (Magnitude) – The basic short vector instruction utilizes two 3-bit delta data words (or fields) in conjunction with the two previously described direction fields. The two delta words determine the length or magnitude of each of the two short vectors. Bits 8, 9, and 10 define the magnitude of the first short vector; bits 15, 16, and 17 define the magnitude of the second short vector of the instruction.

<div align="center">NOTE</div>

When using the basic short vector instruction with the direction and delta data field of both short vectors used, two cycles are required to complete the instruction as shown in Figure 4-28. Basic short vectors can be modified through use of the same five parameters as described in Paragraph 4.5.2 for the basic vector instruction.

4.5.4   Point/Graph Plot

The point/graph plot instructions use the 4-bit operating code, 14_8, consisting of bits 0 through 3. This instruction is further augmented into two separate instructions: point plot and graph plot, depending on the set (1) or unset (0) condition of bit 7 of the point/graph plot instruction.

4.5.4.1   Point Plot – If bit 7 of the point/graph plot instruction is not set to 0, a point plot will be specified (see Figure 4-31). Bit 6 is used to denote the axis in which the CRT beam is to be moved. If bit 6 is set, the beam will be moved along the X-axis, and with bit 6 in the reset condition, the beam will be moved in the Y-axis. This condition is true if the beam is to be moved along only one of the axes (X or Y). If the beam is to be moved in relation to both axes, then the point plot instruction must be used twice (utilizing two operating cycles), once to move the beam in the X-axis, and once to move the beam in the Y-axis.

A 10-bit data field (bits 8 through 10) is used to define the absolute point location with respect to the previous origin.

The point plot instruction can be used to specify four parameters or characteristics:

a. Intensity Enable – Bit 4 of the point/graph plot instruction is used as the intensity enabling bit. With bit 4 set, the point will be intensified; with bit 4 reset, the point will be unintensified. The condition of bit 4 (set or unset) affects the point specified in the 10-bit coordinate data field (bits 8 through 17) of the current point plot instruction only. The intensity or brightness of the point is determined by the 3-bit intensity field (bits 8 through 10) of the parameter 1 instruction (see Figure 4-20).

b. Axis of Beam Deflection – When moving a point, the axis of beam deflection is determined by bit 6. With bit 6 set, the X-axis is chosen; with bit 6 unset, the Y-axis is chosen.

<div align="center">4-44</div>
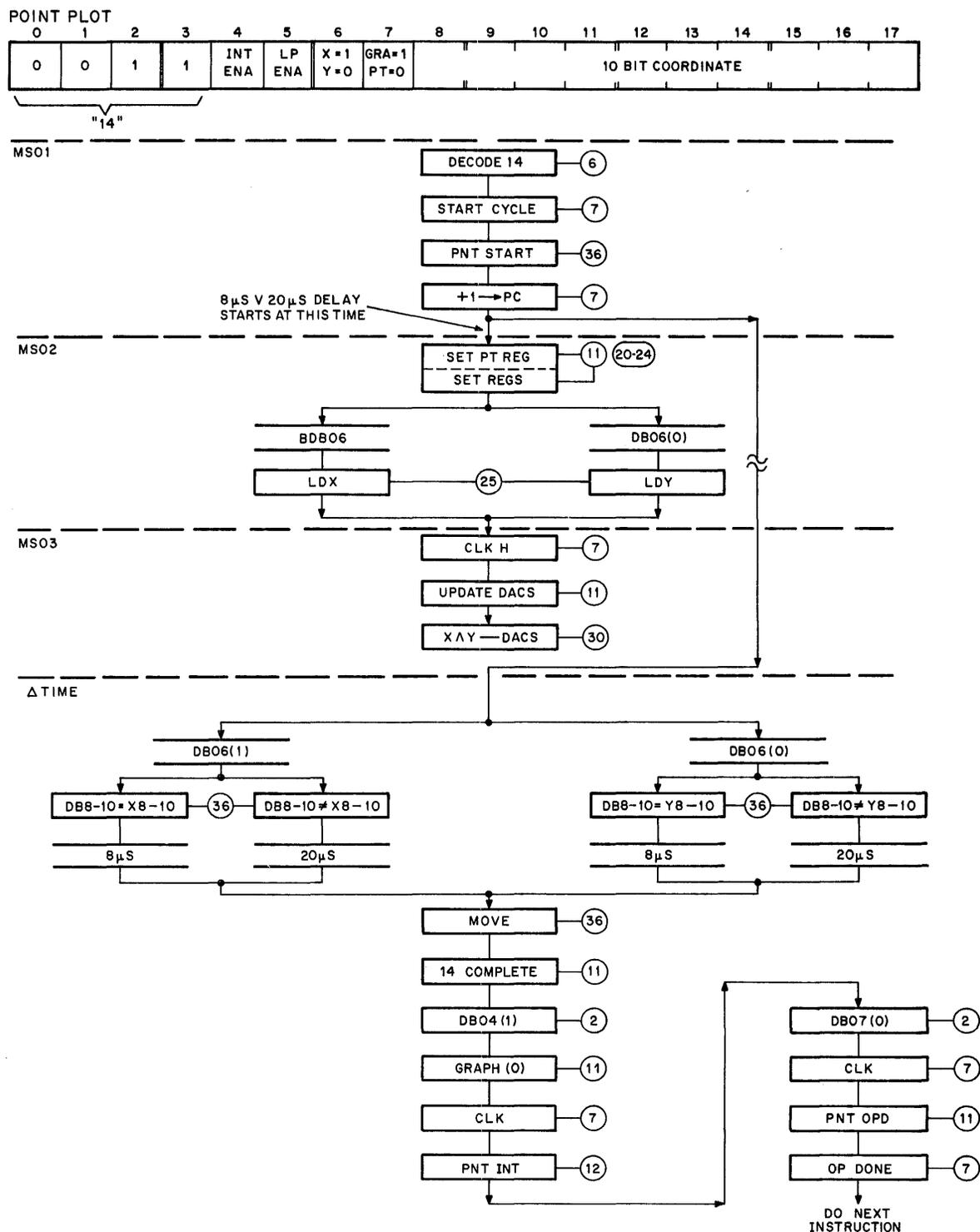
Figure 4-31   Point Plot Instruction Flow Diagram

15-0261

4-45

c. Absolute Displacement from Origin - Bits 8 through 17 combine to make up the coordinate data field. All coordinates between 0 and 1023 within the visible image area (1023 X 1023) can be expressed using various bit combinations within this 10-bit data field. All beam movements should be referenced to the origin in each axis.

d. Light Pen Enable - If bit 5 of the point/graph plot instruction is set, a light pen flag will be raised if a light pen hit occurs. This condition is true for the point named in the coordinate data field of the current point plot instruction only. With a parameter 3 light pen interrupt specified, an interrupt request will be generated to the PDP-15 Computer.

4.5.4.2 Graph Plot - With bit 7 of the point/graph plot instruction set, a graph plot (Figure 4-32) is specified as opposed to a point plot. When a graph plot instruction is specified, only one axis (X or Y) need be specified. The beam will be moved a predetermined distance automatically along the unspecified axis. This predetermined distance is initially defined by the 4-bit increment register (bits 14 through 17) of the parameter 1 instruction (see Figure 4-20). The graph-plot instruction can be used to specify four parameters or characteristics for a graph plot.

a. Intensity Enable - Bit 4 is used as the intensity enabling bit. With bit 4 set, the graph plot is intensified. The intensity or brightness is determined by bits 8 through 10 of the parameter 1 instruction as described in Paragraph 4.5.4,a. Only the point(s) in the named axis will be intensified with bit 4 set; the point(s) in the unnamed axis will remain unintensified.

b. Axis of Beam Deflection - When a graph-plot instruction is specified, only one axis need be defined. With bit 6 set (1), the X-axis is chosen; with bit 6 unset (0), the Y-axis is chosen.

c. Absolute Displacement of Data Points - When graph plotting, beam movement in the specified axis must be referenced absolutely with respect to the origin. Data points can be incremented through use of the parameter 1 increment register. For instance, for a continuous graph (with increments of 1), 1024 samples would be taken between 0 and 1023 with one decimal increment equal to 0.01 in. Data increments may be specified as large as 15, or approximately 0.150 between graph points.

d. Light Pen Enable - With bit 5 set, the light pen will be enabled. Setting this bit raises a light pen flag on when a light pen hit occurs. With light pen interrupt enable (bit 12 of parameter 3) specified (set), an interrupt request will be generated to the PDP-15 Computer.

4.5.5 Jump/Jump-to-Subroutine

The 18-bit jump/jump-to-subroutine instruction format has a 3-bit operating code of 6_8, which when decoded in relation to other display file instruction codes equates to 60_8 in the instruction decoder. This basic instruction can be further divided into four subinstructions, according to the conditions of bits 3 and 4. With bit 3 set, the instruction is a jump-to-subroutine; if bit 3 is not set, the instruction is a jump. Bit 4 is used as the indirect addressing bit and determines whether the jump and jump-to-subroutine instructions use direct or indirect addressing. When indirect addressing bit 4 is set, the address named in the 13-bit address word does not give the actual starting location, but does specify
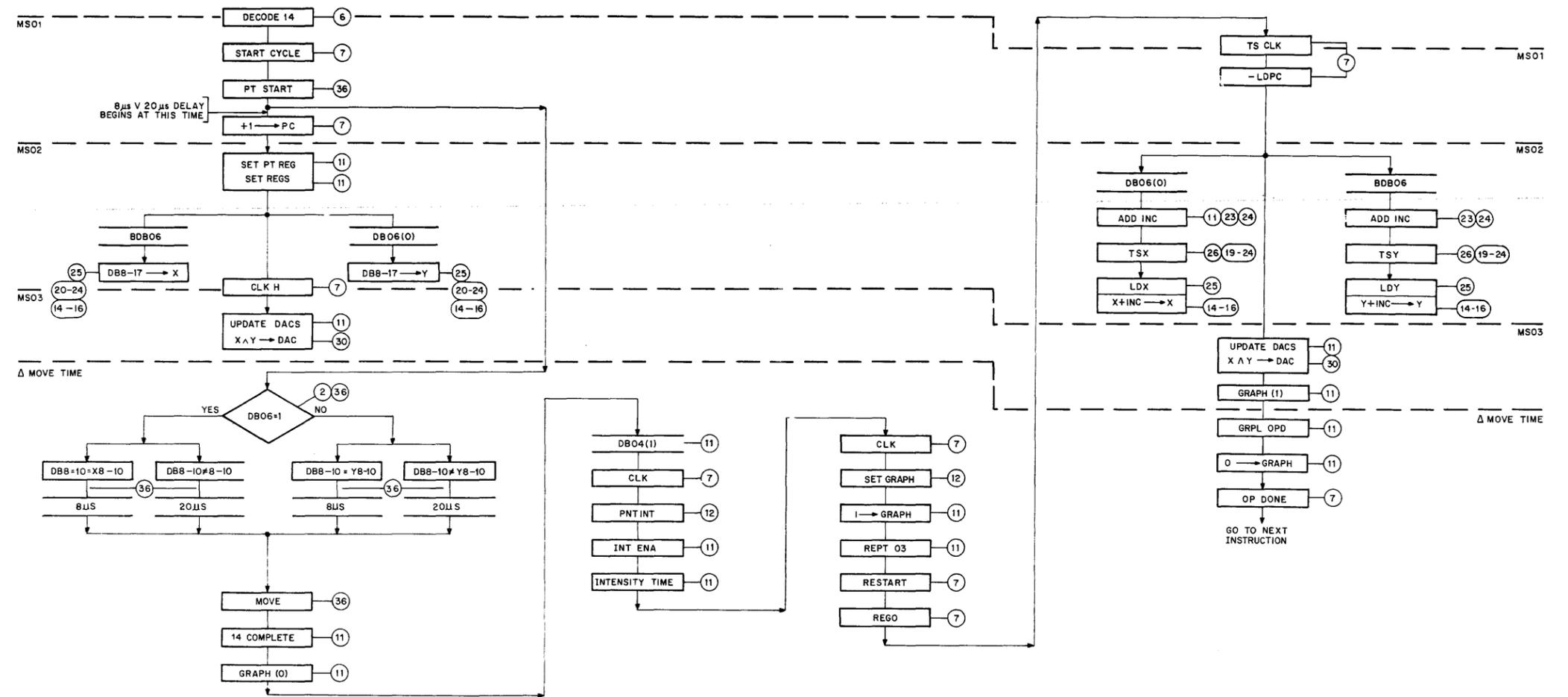
Figure 4-32   Graph Plot Instruction Flow Diagram

the address of the starting location. Indirect addressing permits the actual address word to be expanded to 17 bits, providing a means of branching to any one of 131K core locations. Thus, the 13-bit address (bits 5 through 17) does not give the pointer word's location; however, it does give the location of the pointer word address. Also, with indirect addressing bit 4 set, the jump instruction uses two operating cycles, as opposed to one operating cycle when bit 4 is not set. With bit 4 set in the jump-to-subroutine instruction, three operating cycles are used, as opposed to two operating cycles when bit 4 is in the reset condition.

4.5.5.1   Jump – The jump or DJMP instruction (see Figure 4-33) permits the program to repeat instructions already performed or to jump over display file instructions in the normal programmed sequence. This instruction is only used within one 8K memory bank. The hardware loads the effective (13-bit) address contained in the jump instruction into the VT15 Graphic Processor program counter, to alter the normal programming sequence, because the VT15 program counter always contains the location of the next instruction.

4.5.5.2   Jump Indirect – With bit 4 of the jump instruction set, jump or DJMP becomes jump indirect (JMPI) (see Figure 4-34), and the 13-bit address word provides the location of the starting address or pointer word address (17 bits). This instruction is especially useful when used in conjunction with the character string instruction (see Figure 4-40 and 4-41). If the address specified for the character string address field does not occur within the same memory bank as the instruction, then bit 4 will be set specifying an address in an alternate memory storage bank.

4.5.5.3   Jump-to-Subroutine – The jump-to-subroutine or DJMS instruction (see Figure 4-35) stores a pointer address (bits 5 through 17) in the first location of a subroutine and transfers program control to the second location of the subroutine. On completion of the subroutine, the pointer address identifies the next instruction to be performed. This instruction provides a method for branching from the main program of the basic display file to perform a subroutine, and a means of returning to the correct location in the display file on completion of the subroutine.

4.5.5.4   Jump-to-Subroutine Indirect – With indirect addressing bit 4 set, the jump-to-subroutine instruction is enabled for indirect addressing, yielding jump-to-subroutine indirect (see Figure 4-36) permitting the address word to be expanded to 17 bits and allowing any one of 128K core memory locations to be referenced as previously described in Paragraph 4.5.5.
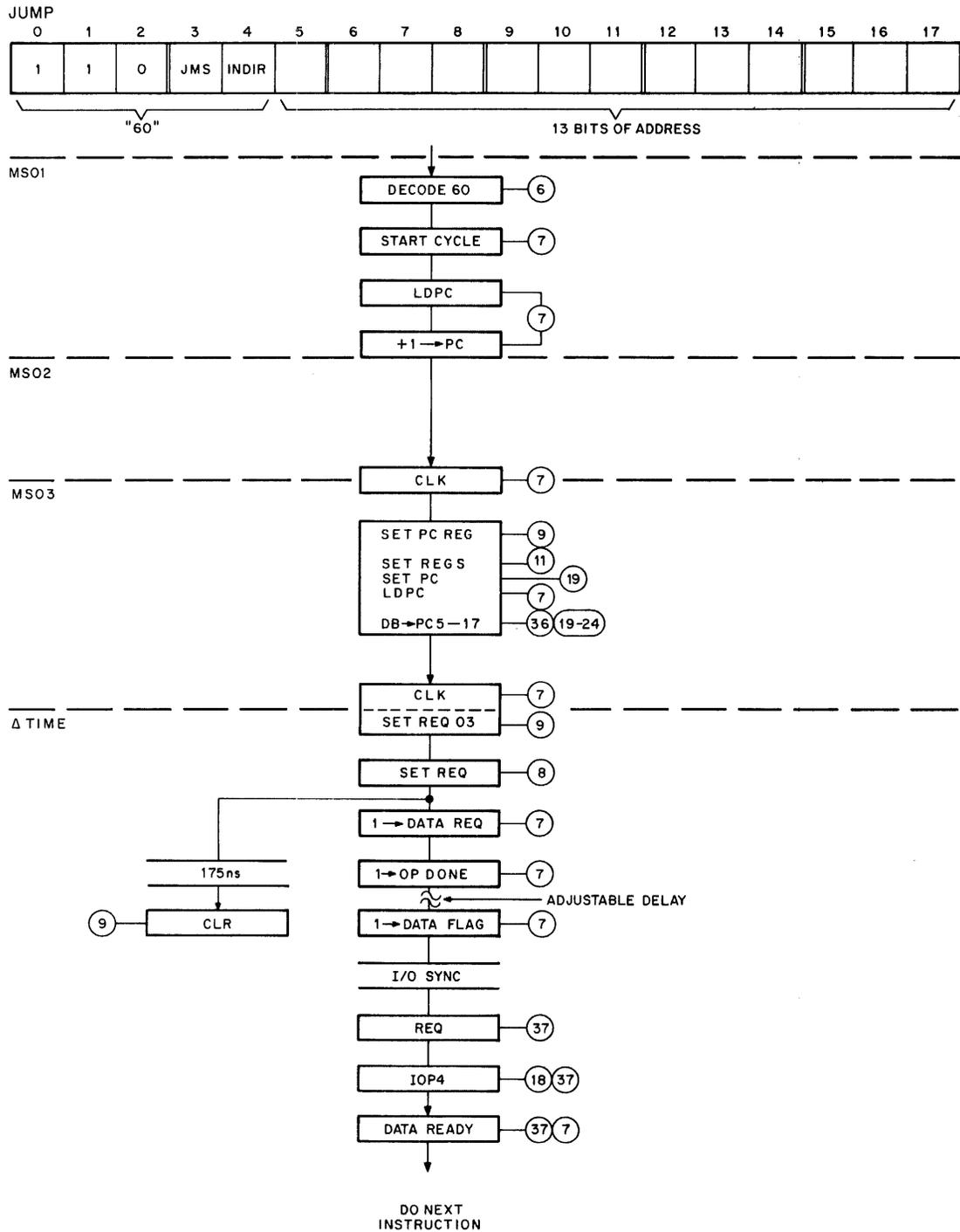
Figure 4-33   Jump Instruction Flow Diagram
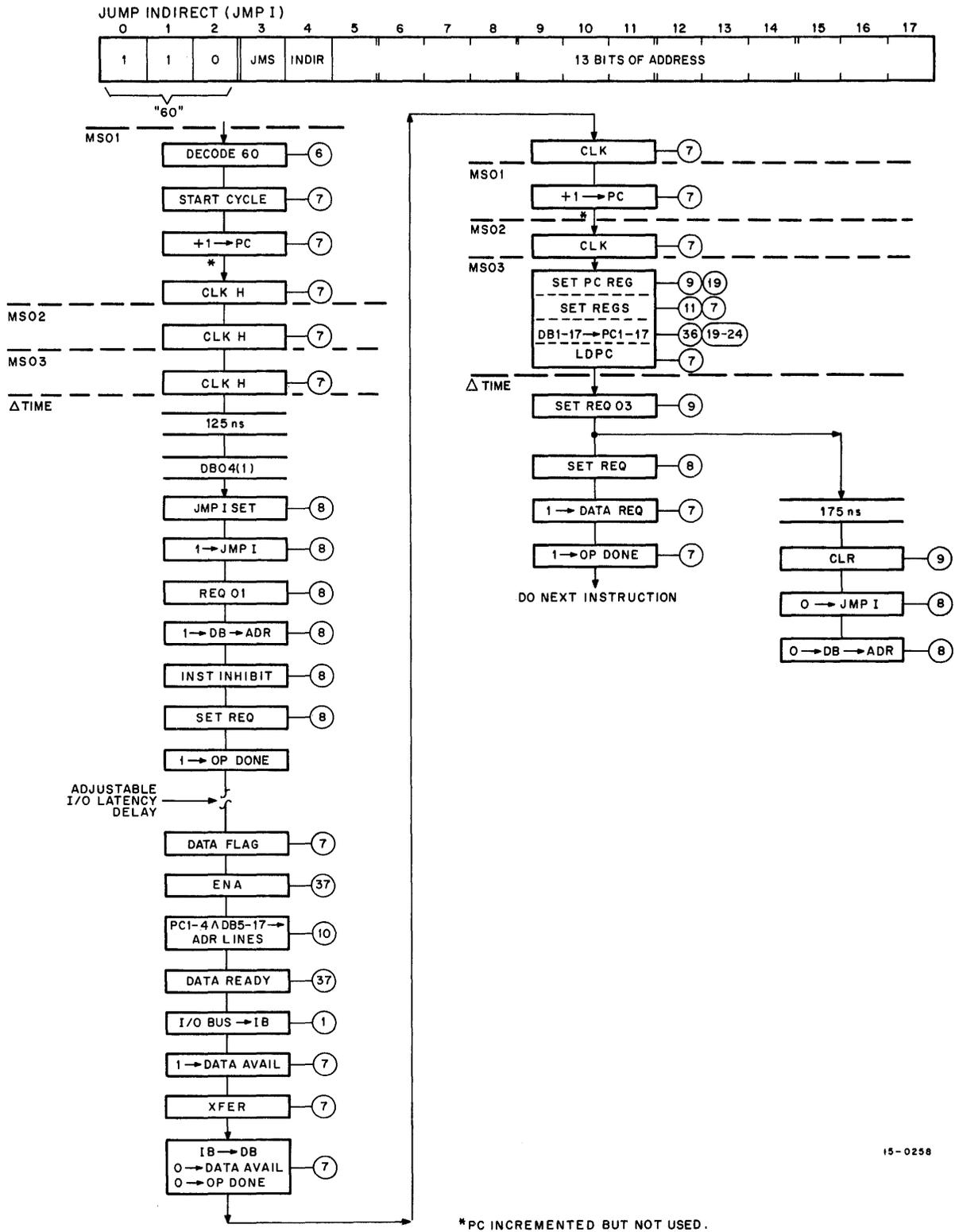
15-0257

Figure 4-34   Jump Indirect Instruction Flow Diagram

15-0258

*PC INCREMENTED BUT NOT USED.

MSO1

DECODE 60 — 6

ADD PC — 7
CIO4 — 17

CLK DLY — 25
START CYCLE
LD PC — 7

MSO2

CLK — 7

MSO3

CLK — 7

ΔTIME

125ns

JMS V JMS I
JMS SET — 8
1 → JMS
SUB RUT — 9
1 → IN
1 → PC IN
SET REQ 01
DB → ADR — 8
INST INHIBIT
SET REQ
1 → OP DONE — 7
1 → DATA REG

ADJUSTABLE LATENCY
DELAY

1 → DATA FLAG — 7 37

I/O SYNC

REQ
SING CY BR — 37
DCH REQ

GRANT — 37
ENA
PC1-4∧DB5-17 → ADR — 10
PC IN CY — 8
RD PC — 32
PC → I/O BUS — 32-34

- GRANT — 37
DATA ACCEPT
0 → IN — 8
REPT 04 — 9

CLK — 7
1 → RESTART

CLK — 7
REGO

MSO1

ADD PC — 7
CIO1 — 17

CLK — 7
- LD PC

MSO2

SET SUBRUT — 11
SET REG — 11
SET PC — 19

CLK — 7
LD PC

MSO3

ADD PC — 7
CIO1 — 17

CLK — 7
END TIME — 8
SET REQ 04 — 9
LD PC — 7
SET REQ — 8

1 → DATA REQ — 7
1 → OP DONE

ΔTIME

175ns

CLR — 9

0 → JMS
0 → PC IN — 8
0 → DB → ADR

DO NEXT INSTRUCTION

15-0259

Figure 4-35   DJMS Instruction Flow Diagram

4-52
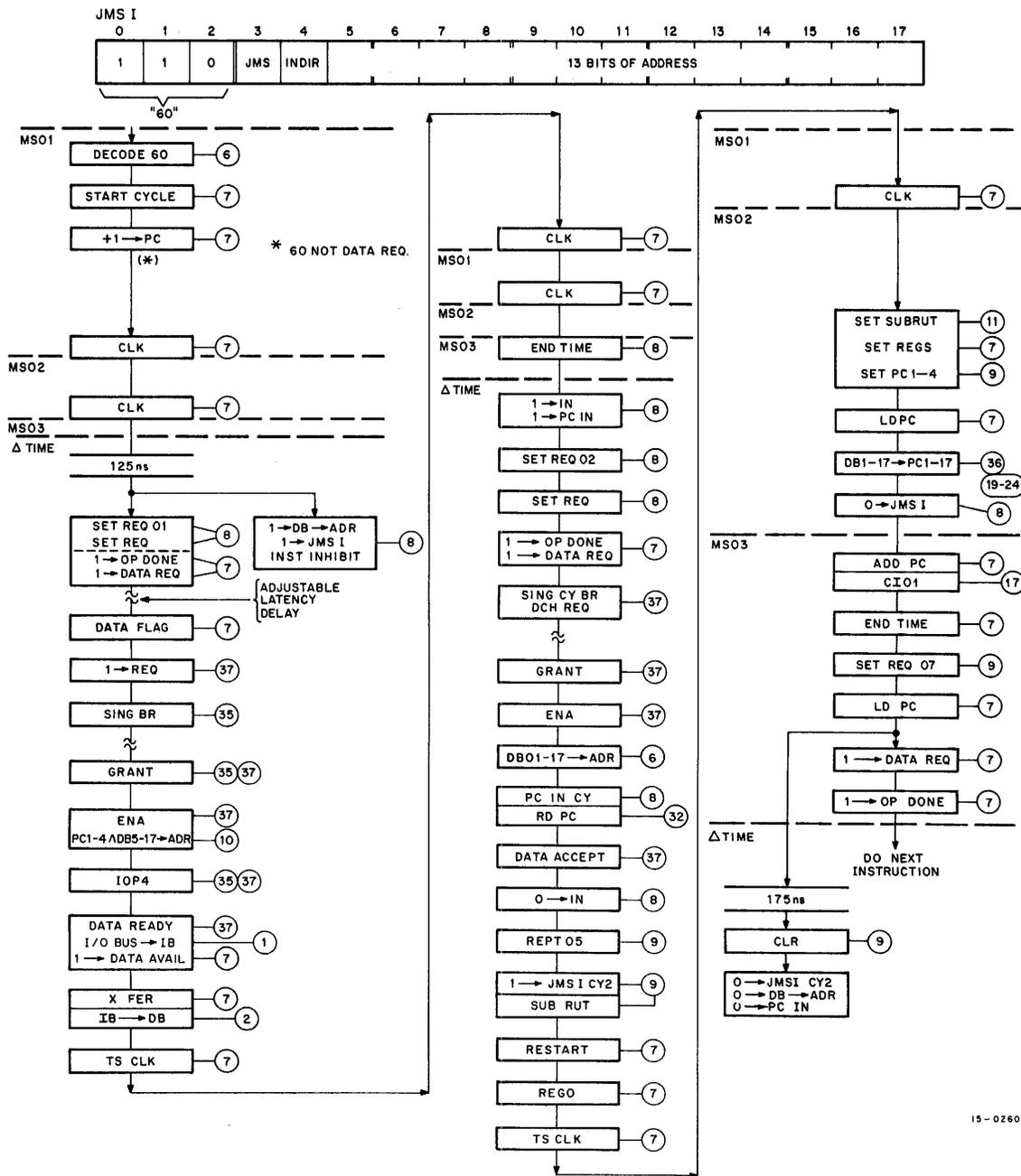
Figure 4-36   JMS Indirect Instruction Flow Diagram

4.5.6   Save/Restore Instruction

The save/restore instruction has the four-bit operating code 24_8, which occupies bits 0 through 3. The save/restore decision bit, bit 4, determines whether the parameters listed in Table 4-5, and shown in Figure 4-37, should be saved or restored. With bit 4 set, the parameter will be restored into the display file. If bit 4 is not set, the parameters will be saved to some location in the PDP-15 core memory. Bits 5 through 17 form a 13-bit address field which is used to specify the location in the PDP-15 core memory where the parameters listed in Table 4-5 are to be saved, or the location from which they are to be restored into the display file. This 13-bit address field provides the capability of naming up to 8,192 locations in the PDP-15 core memory.

Table 4-5
Save/Restore Parameters

Bit No.	Parameter Checked	Display File Instruction
0	INCR 0	Parameter 1
1	INCR 1	Parameter 1
2	INCR 2	Parameter 1
3	INCR 3	Parameter 1
4	BLNK	Parameter 2
5	ROT	Parameter 2
6	OFFSET	Parameter 2
7	EDGE FLAG EN	Parameter 2
8	INT 0	Parameter 1
9	INT 1	Parameter 1
10	INT 2	Parameter 1
11	STOP INTR EN	Parameter 3
12	LP INTR EN	Parameter 3
13	EDGE INTR EN	Parameter 3
14	PB INTR EN	Parameter 3
15	LP FLAG EN	Parameter 2
16	LINE 0	Parameter 3
17	LINE 1	Parameter 3

When the save restore instruction is specified, the parameters listed in Table 4-5 and shown in the save/restore status format (see Figure 4-37) are collected from their respective registers (Figures 4-20, 4-22, and 4-23), and are compiled into an instruction status word or format.
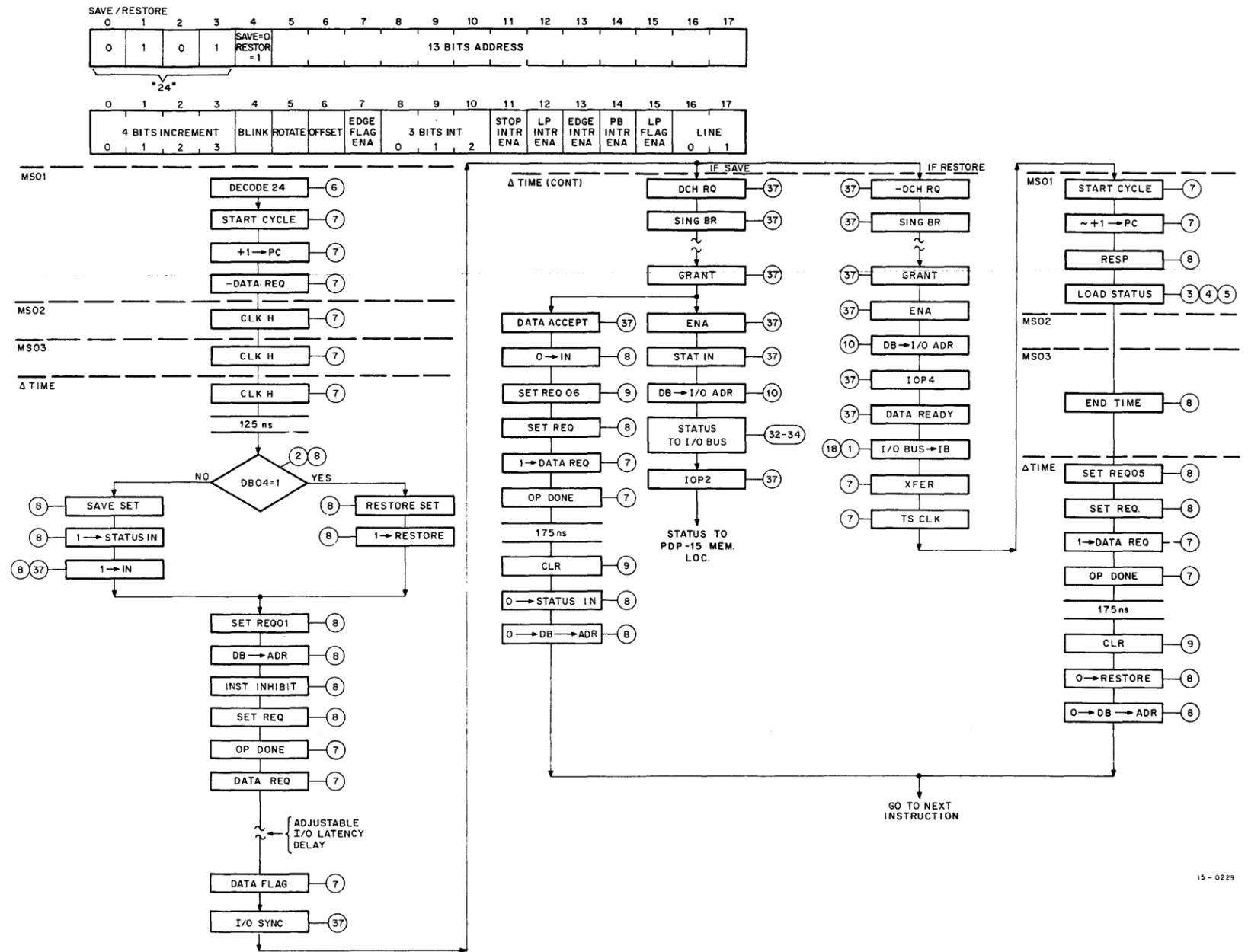
Figure 4-37 Save/Restore Instruction Flow Diagram

The content of the addressed save/restore location(s) can be examined by issuing a LAC instruction that names the status word location. The save/restore instruction is especially useful when the operator wishes to change only one or two of the basic parameters in one small part of the display file. Parameters that normally remain unchanged are saved in some location in PDP-15 core memory and are restored after the desired display file functions or changes have been programmed. The save/restore instruction is also useful for saving the status of previously programmed parameters when jumping to subroutines.

4.5.7 Character Input

The character input instruction (see Figure 4-38) uses the 4-bit operating code 00_8. This instruction provides a convenient means of displaying any one of the individual characters listed in Table 2-3 of the Graphic-15 Reference Manual. The VT15 Graphic Processor operates directly on the specified instruction, and the particular character named in the 7- or 8-bit ASCII field is displayed directly from the display file. Because both the 7- and 8-bit ASCII characters are compatible, the 7-bit ASCII code listed in Table 2-3 of the Graphic-15 Reference Manual, or the standard 8-bit ASCII code generated by a standard Teletype, can be used. This compatibility eliminates the necessity for stripping and packing incoming ASCII characters.

Bit 4 of the instruction is unused, and bit 5 serves as the light pen flag enabling (LP FLAG EN) bit. With bit 5 set, the light pen logic is enabled allowing a light pen hit to occur during generation of the current character. Enabling bit 5 is especially useful when using the light pen to identify a character specified in the ASCII field of the current instruction. Bits 6 through 9 are unused; bits 10 through 17 are used in combination to express any one of 68 ASCII characters in the 7-bit or 8-bit ASCII codes.

Seven parameters or characteristics can be established for characters generated through the character input instruction. Most of these parameters are specified through use of the other display file instructions, such as the parameter 1, 2, and 3 instructions, prior to executing the character input instruction, though all the parameters may or may not be specified:

    a.   Intensity - The intensity of any character is established through bit 7 (INT ENA) and the 3-bit intensity parameter field consisting of bits 8 through 10 of the parameter 2 instruction.

    b.   Size - The size of any of the 65 printing ASCII characters (including linefeed) can be expanded up to 15 times greater than its basic, 3/32 in. by 1/8 in. dimensions, through use of the 4-bit increment field (bits 14 through 17) of the parameter 1 instruction. The content in the VT15 Graphic Processor increment register is processed (read) for each individual vector of the character input instruction to examine the data for repeatability. Each vector is then repeated the number of times specified by value of the particular data word contained in the increment register.
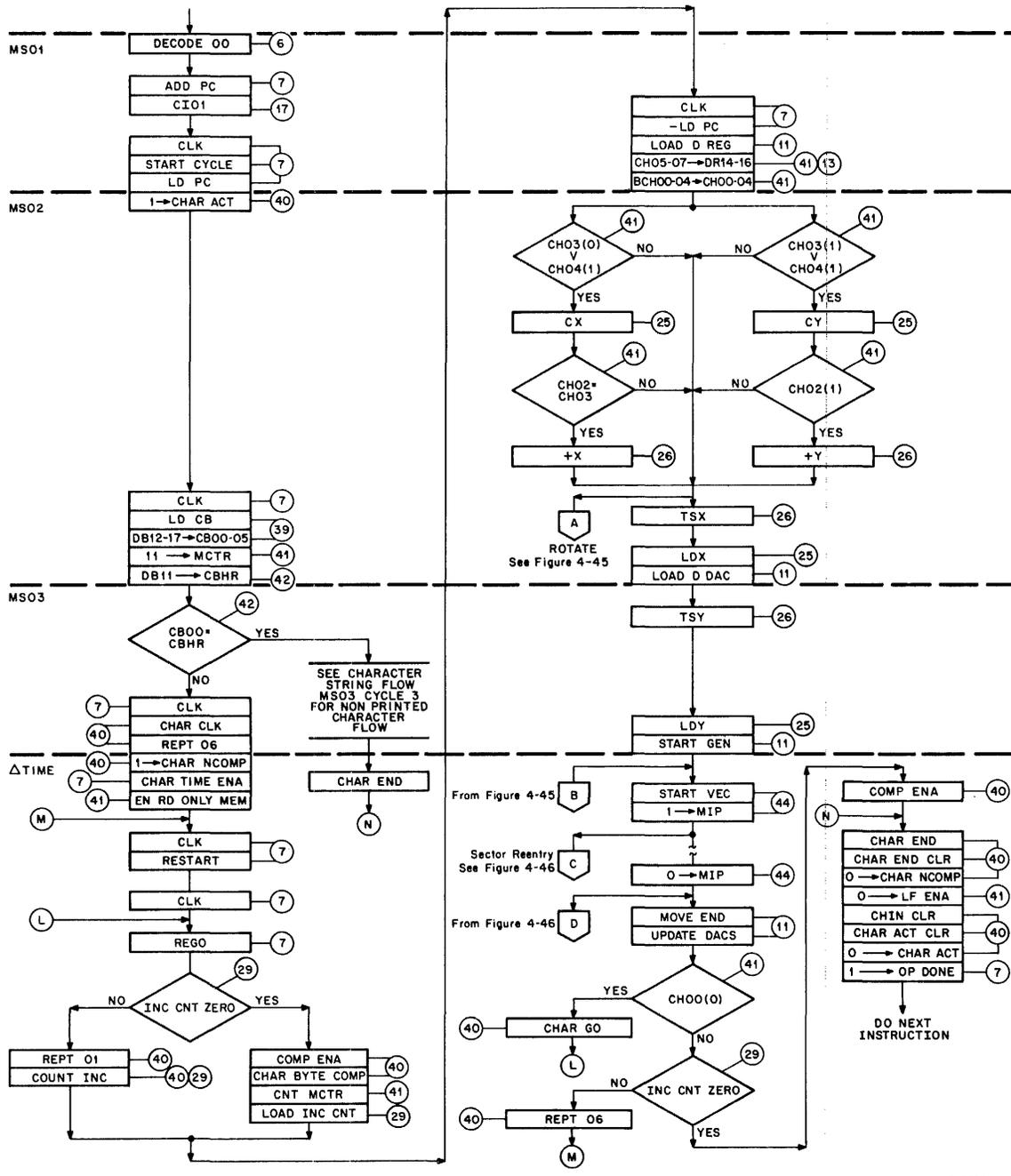
Figure 4-38   Character Input Instruction Flow Diagram

15-0230

4-58

c.   Rotation – All characters can be rotated 90° counterclockwise, allowing characters to be written in both the horizontal and vertical planes. Rotation is specified through the parameter 2 instruction by setting rotate enabling (ROTATE ENA) bit 12 and the vertical/horizontal bit 13. With bit 12 set (enabled) and bit 13 unset, characters will continue being generated in the normal (horizontal) plane. Rotation has no effect on character magnification as described under "increment," above. For a functional description of rotate, refer to Paragraph 4.5.11 and Figure 4-46.

d.   Light Pen Hit – If a light pen hit is desired, bit 5 of the character input instruction must be set for that particular character. Setting bit 5 causes a light pen flag to be raised, but only on the character named in the data field of the character input instruction in which bit 5 was set.

e.   Blink – Individual characters can be blinked by previously setting blink enabling (BLINK ENA) bit 8 and blink ON/OFF bit 9 of the parameter 2 instruction.

f.   Starting Place – Characters can be started anywhere on the specified paper size. All characters are automatically generated by the VT15 Graphic Processor character generator any time the character input instruction is specified and executed. The initial starting point can be determined by using the point plot instruction (Figure 4-31), the basic vector instruction (Figure 4-28), or the arbitrary vector instruction; the arbitrary vector method can only be used if the arbitrary vector option is included within the VT15 Graphic Processor. An example of ASCII character generation as it appears on the display console CRT is shown in Figure 4-39, using the 5 x 7 coordinate-point matrix.

15-0356
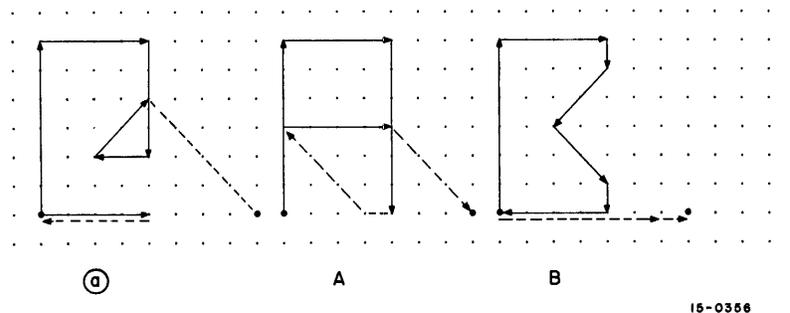
Figure 4-39   ASCII Character Generation

4.5.8   Character String

The 18-bit character string instruction (see Figures 4-40, 4-41, and 4-42) uses the 4-bit operating code 04_8, which occupies bits 0 through 3. Bit 4 of the instruction serves as the indirect addressing bit; bits 5 through 17 combine to makeup a 13-bit absolute address field capable of naming up to

8,192 memory locations. This absolute address, located at the beginning of the ASCII files, specifies the starting location of the IOPS ASCII character format, except where indirect addressing bit 4 is set. With bit 4 set, the 13-bit field or word does not give the starting location but the address of the starting location.

CHARACTER STRING INSTRUCTION

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
O	O	O	1	INDIR ADR						13 BITS OF ADDRESS							
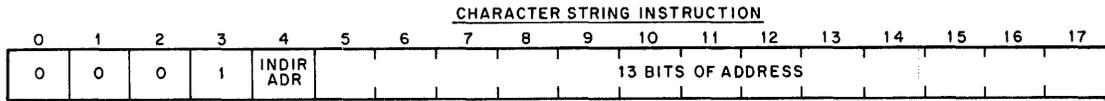
15-0231

Figure 4-40   Character String Instruction Format

Seven parameters or characteristics can be defined for an ASCII string of characters. These seven parameters will be defined through use of other display file instructions such as the parameter 1, 2, and 3 instructions (see Figures 4-20, 4-22, and 4-23). The seven parameters and the related instructions through which they are specified are defined in Table 4-6.

Table 4-6
Character String Parameters

Characteristic	Display File Instruction	Bits
Intensity	Parameter 1	7 through 10
Character Size	Parameter 1	14 through 17
Blink	Parameter 2	8 and 9
Rotate	Parameter 2	12 and 13
Termination	Parameter 2[†]	6 and 7
Tabs	Character String[†]	
Starting Place	Point/Graph plot	7 through 17
	Basic Vector	5 through 17
	Arbitrary Vector[††]	

[†]These characteristics are defined in greater detail in Paragraph 4.5.8.2.

[††]This instruction can be used only if the Arbitrary Vector Generator option is included.

4-60
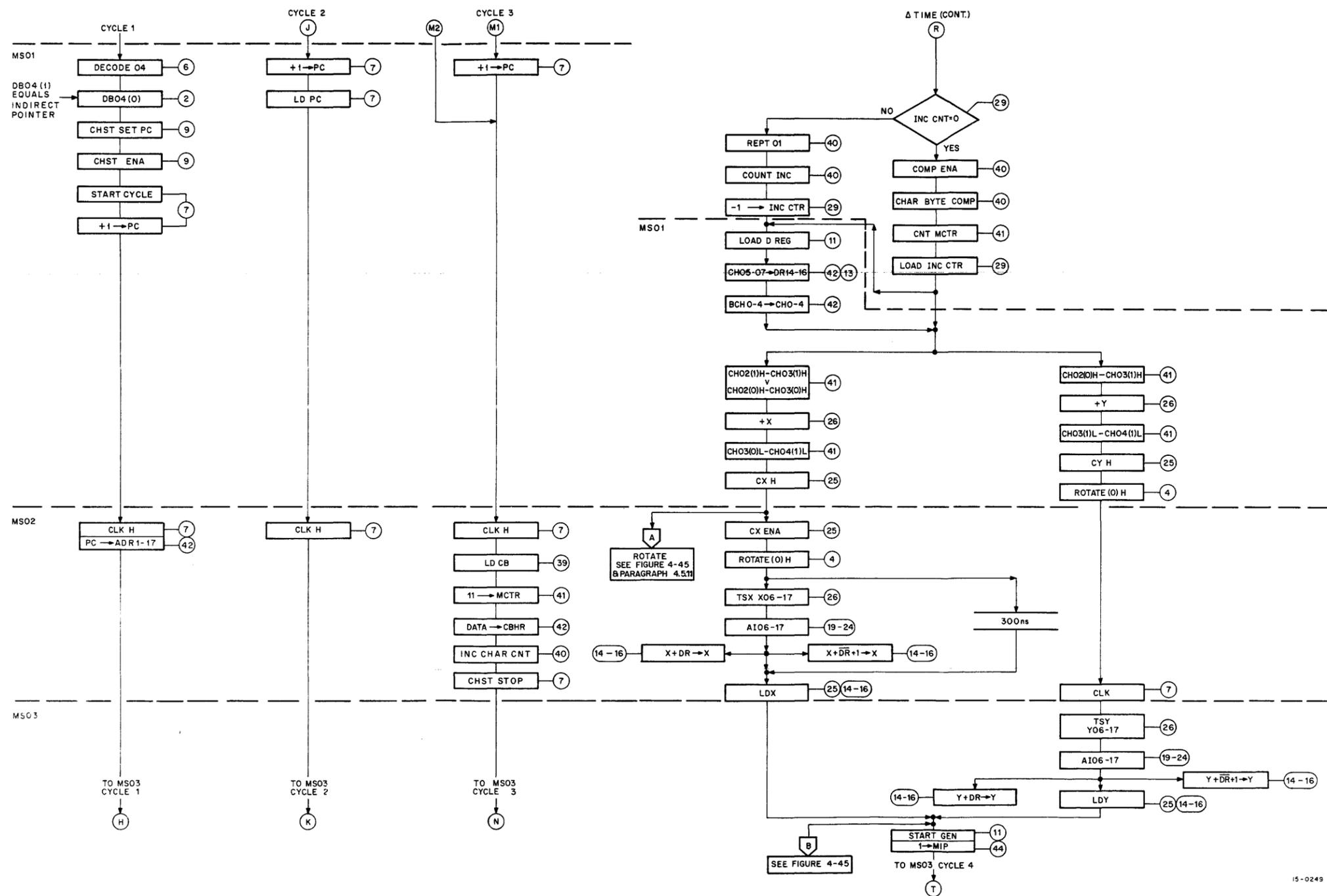
Figure 4-41 Character String Instruction
Flow Diagram (Sheet 1 of 3)

4-61/4-62
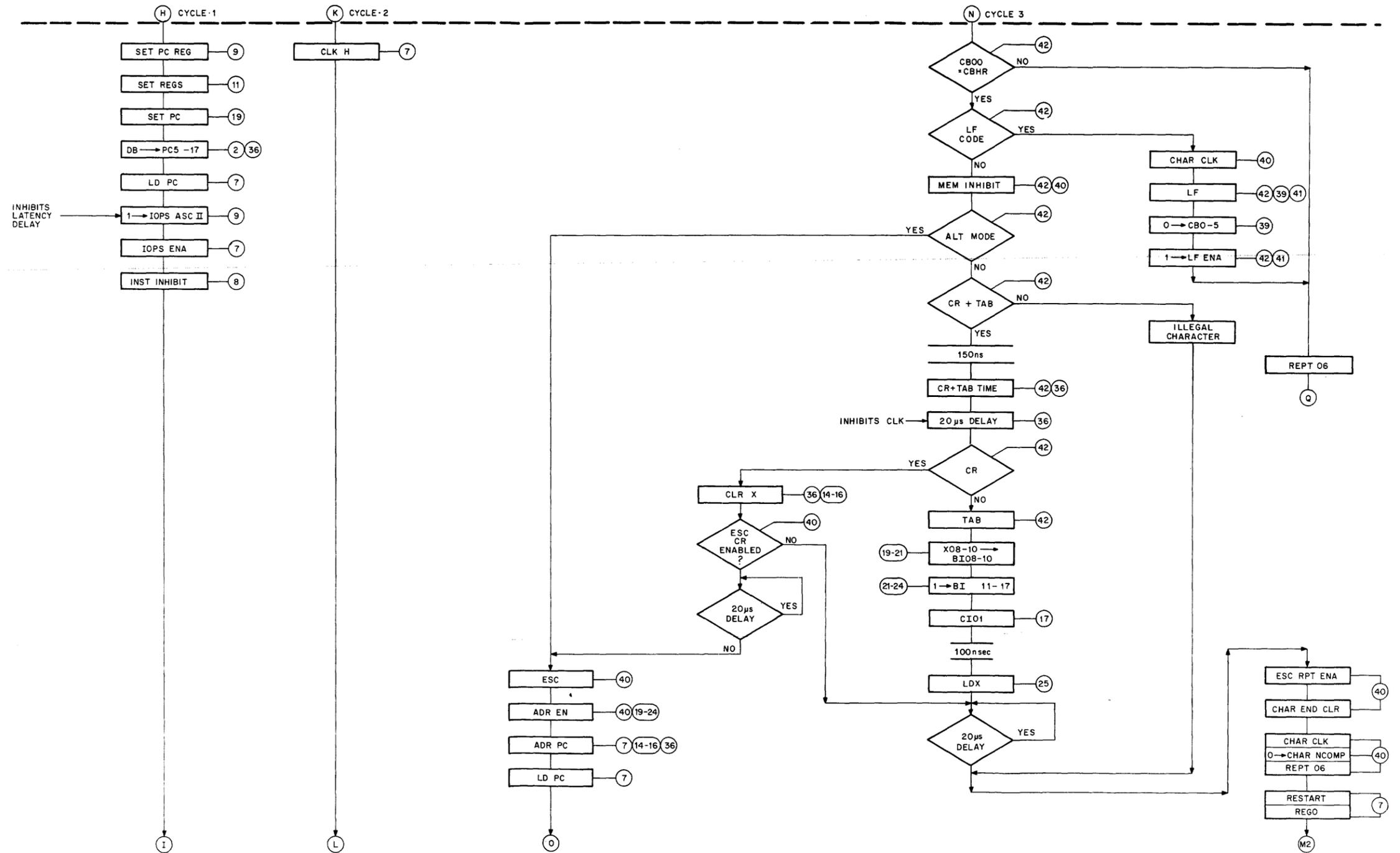
Figure 4-41 Character String Instruction
Flow Diagram (Sheet 2 of 3)

15-0250

4-63/4-64
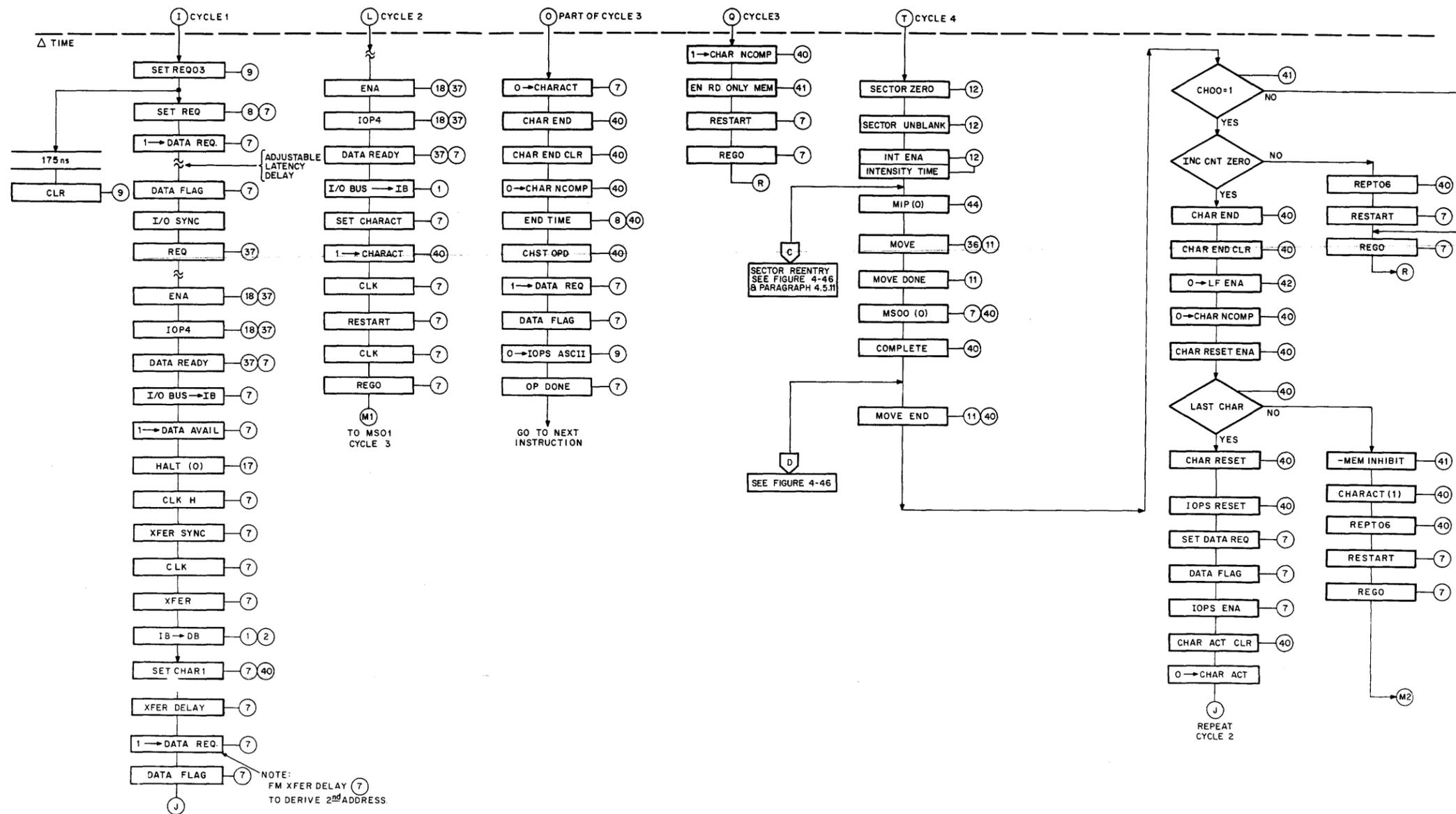
Figure 4-41 Character String Instruction
Flow Diagram (Sheet 3 of 3)

4.5.8.1 IOPS ASCII - The character string instruction directs the VT15 program counter to the starting address of a string of ASCII characters in the computer core memory. The characters within this character string are packed in the input/output programming system (IOPS) format as shown in Figure 4-42.

IOPS CHARACTER FORMAT

	FIRST 18-BIT WORD			SECOND 18-BIT WORD		
BIT POSITION	0　　　　6	7　　　　13	14　　　17	0　2　3　　　9	10　　　16	17
CHARACTER POSITION	1　CHARACTER	2　CHARACTER	3　CHARACTER	4　CHARACTER	5　CHARACTER	0

15-0415
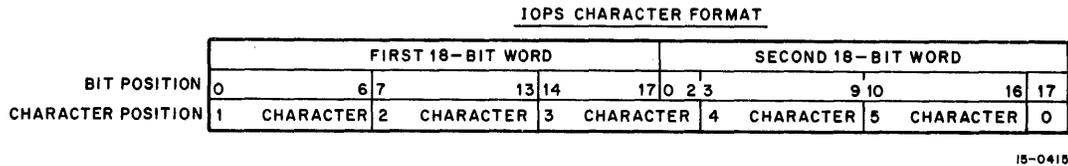
Figure 4-42　IOPS Character Format

When ASCII characters are packed in IOPS format, two 18-bit core memory locations are utilized to give five ASCII character codes with the last bit (bit 17) of the second 18-bit word unused. Thus, characters packed in IOPS format will be contained in a minimum of two consecutive core memory locations. A complete listing of the 7-bit ASCII codes used in VT15 Graphic Processor character generation is contained in Table 2-3 of the Graphic-15 Reference Manual. When indirect addressing bit 4 is set, the character string address word can be expanded to 17 bits allowing any one of 128K core memory locations to be referenced.

The VT15 Graphic Processor can generate up to 68 basic ASCII characters (64 printing and linefeed) using a hardware character generator. The hardware character generator produces the vectors necessary for character generation. Desired characters are produced by writing a succession of short vector strokes according to specified 7-bit ASCII codes. All characters are constructed through vectors drawn in a basic 5-point by 7-point font as described in Paragraph 4.5.7. Thus, all alphanumeric data utilized with the character string instruction is converted and stored as "5/7 ASCII". "5/7 ASCII" refers to the internal packing and storage scheme. As shown in Figure 4-41, five 7-bit ASCII characters are packed in two contiguous locations and are stored as binary data in the PDP-15 core memory.

4.5.8.2 Implied JMS - In the JMS instruction, the contents of the program counter are saved in a core memory location. The location is specified by the Y-field or the JMS instruction.

When character string is specified the current address, contained in the program counter, is loaded into the 17-bit address (ADR) register (PC →ADR), a hardware holding register.

When the character string instruction or operation is complete, the address stored in the ADR register is returned to the program counter to specify the address of the next instruction to be executed. The program counter is incremented (+1 PC) when the "saved" address is transferred back into the program counter from the ADR register (ADR PC).

Thus, this operation, used with the character string instruction, is considered an "implied JMS" and not a normal or true JMS.

4.5.8.3 Termination Functions and Tab - The character string instruction can be terminated by either one of two ASCII codes: the carriage return (CR) ASCII code and the alternate mode (ALT MODE) ASCII code. When the character generator operation is initiated, it continues until either of the ASCII codes has been sensed. Termination of a character string with either of these two ASCII codes is called an "escape."

If the operator desires to write more than one line of characters, he must specify the ALT MODE ASCII code. With carriage return specified, the character generator will escape when the ALT MODE or carriage return character code appears in the character string instruction. The enabling bit for an escape (ESC) during character string is "escape enable" bit 6 of the parameter 2 instruction (see Figure 4-22). Bit 7 of the parameter 2 instruction serves as a decision bit. With bit 7 not set, the character generator will escape only if an ALT MODE occurs. With bit 7 set, the character generator will escape when a carriage return or an ALT MODE occurs. On termination of the character string instruction, the VT15 program counter is restored to the instruction immediately following the completed character string instruction.

Tabular column characters can be specified by the TAB ASCII code. Tabs are moved toward the right, nine character positions from the previous point on the image area. Whereas the ALT MODE and carriage return ASCII codes are considered line terminators, the TAB ASCII code is used as as optional form control character.

Another ASCII code or character that is used as a form control character is line feed (LF). Line feed moves the beam nine positions down the Y-axis. These form control and line terminator characters are decoded by the VT15 Graphic Processor address and character generator control (VT15-0-42) presented in Table 4-7.

Table 4-7
ASCII Character Control Codes

Form Control Characters	CBHR	CB00	CB01	CB02	CB03	CB04	CB05	Char. Act
ALT MODE	1	1	1	1	1	0	1	1
LF CODE	0	0	0	1	0	1	0	1
CR	0	0	0	1	1	0	1	1
TAB	0	0	1	0	0	0	1	1
LEGAL CHAR.	1	0	-	-	-	-	-	1
LEGAL CHAR.	0	1	-	-	-	-	-	1

All characters must be specified in IOPS format, as shown in Table 2-3 of the Graphic-15 Reference Manual.

4.5.9 Arbitrary Vector and Arbitrary Short Vector

The VT15 can normally draw vectors in eight basic directions (Figure 4-27). The arbitrary vector option allows both long and short vectors to be drawn in any arbitrary direction. The arbitrary (long) vector instruction requires two words (fetches) from the PDP-15. The first word defines ΔX and the second word defines ΔY. An arbitrary short vector instruction is similar to an arbitrary vector instruction except the arbitrary short vector instruction only requires a single word and both the ΔX and ΔY components are defined in the same word. A functional flow diagram of the arbitrary vector analog functions appears on page 4-70.

4.5.9.1 Arbitrary Vector

Arbitrary Vector – The arbitrary vector instruction (see Figure 4-43) uses the 4-bit operating code 10_8, that occupies bits 0 through 3. This instruction is used for long vectors (intensified) or moves (unintensified) in any arbitrary direction, although vector lengths can vary from 0001_8 to 1777_8.

<div align="center">

NOTE

The 0000_8 vector length is illegal and should not be used.
Under the condition $\Delta X = \Delta Y = 0$, the VT15 will hang in
a continual "normalization" loop.

</div>

Bit 5 of the arbitrary vector instruction serves as the light pen enabling (LP ENA) bit. When bit 4 is set the light pen flag is enabled. Bit 5 serves as the intensity (INT) bit. When bit 4 is set the vector is intensified. The intensity level is established through the 3-bit parameter field that consists of bits 8 through 10 of the parameter 2 instruction. Bit 6 serves as the direction bit. Setting bit 6 indicates the vector will be drawn in the negative (ΔX or ΔY) direction; with bit 6 cleared, the vector will be drawn in the positive direction. For example, if bit 6 of the first word (ΔX) of the instruction is cleared and bit 6 of the second word (ΔY) is set, the vector will be drawn in the positive X direction and the negative Y direction, or quadrant IV, as shown on page 4-71.

Bit 7 of the instruction is unused and bits 8 through 17 are used to define the ΔX and ΔY components. In the first word of the instruction, bits 8 through 17 define the ΔX component; in the second word they define the ΔY component. Bits 0 through 5 of the second word are unused.

The other parameters that can be established by using other display file instructions, such as the parameter 1, 2, and 3 instructions, prior to executing of the arbitrary vector instruction, are as follows on page 4-73.
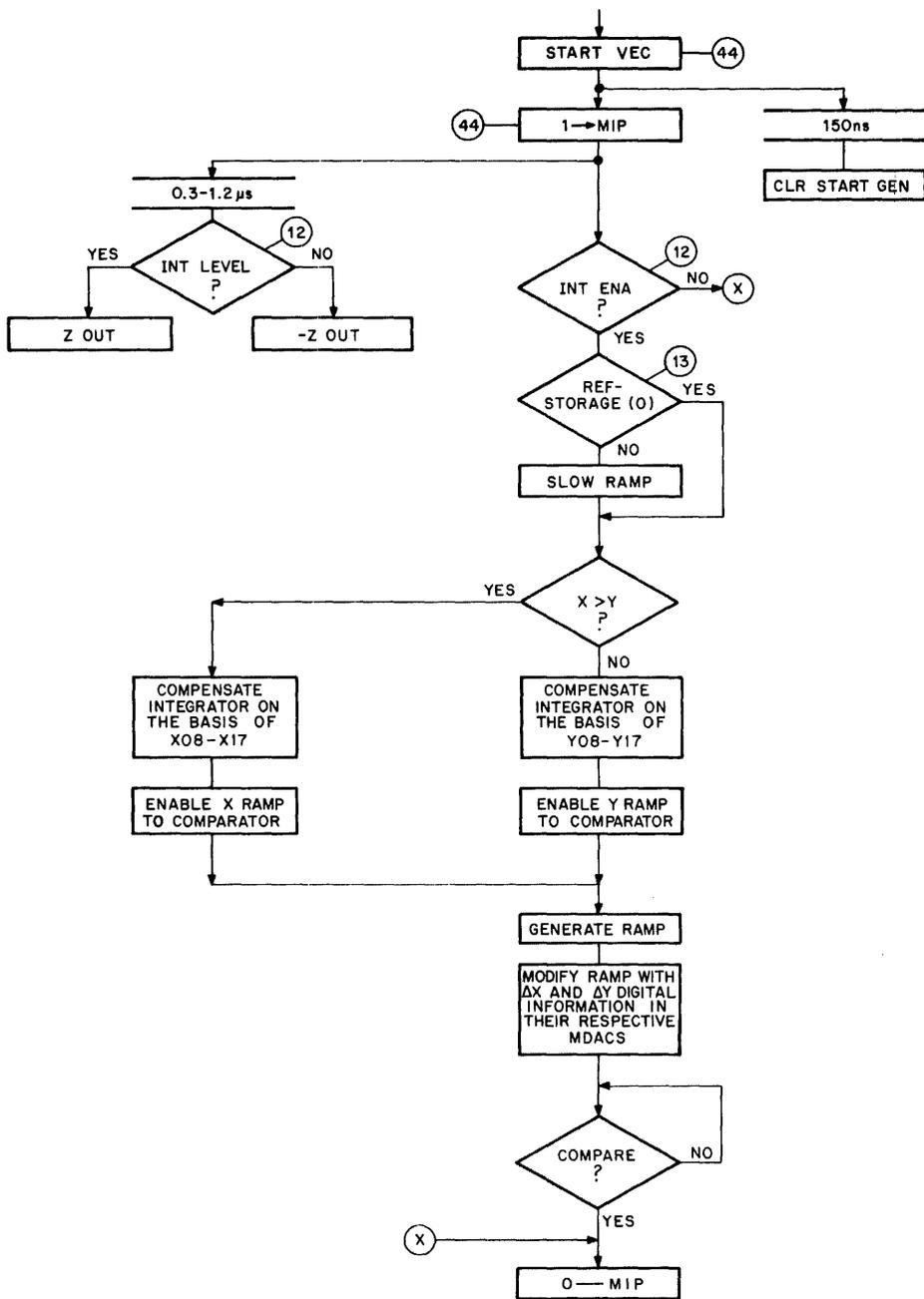
Figure 4-43a Arbitrary Vector Functional Flow Diagram

15-0628

ARBITRARY VECTOR

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
0	0	1	0	LP ENA	INT DOFF 1=ON	(+)=0 (-)=1	NOT USED	1	0	BITS	OF		Δ X				
NOT		USED				(+)=0 (-)=1	NOT USED	1	0	BITS	OF		Δ X				
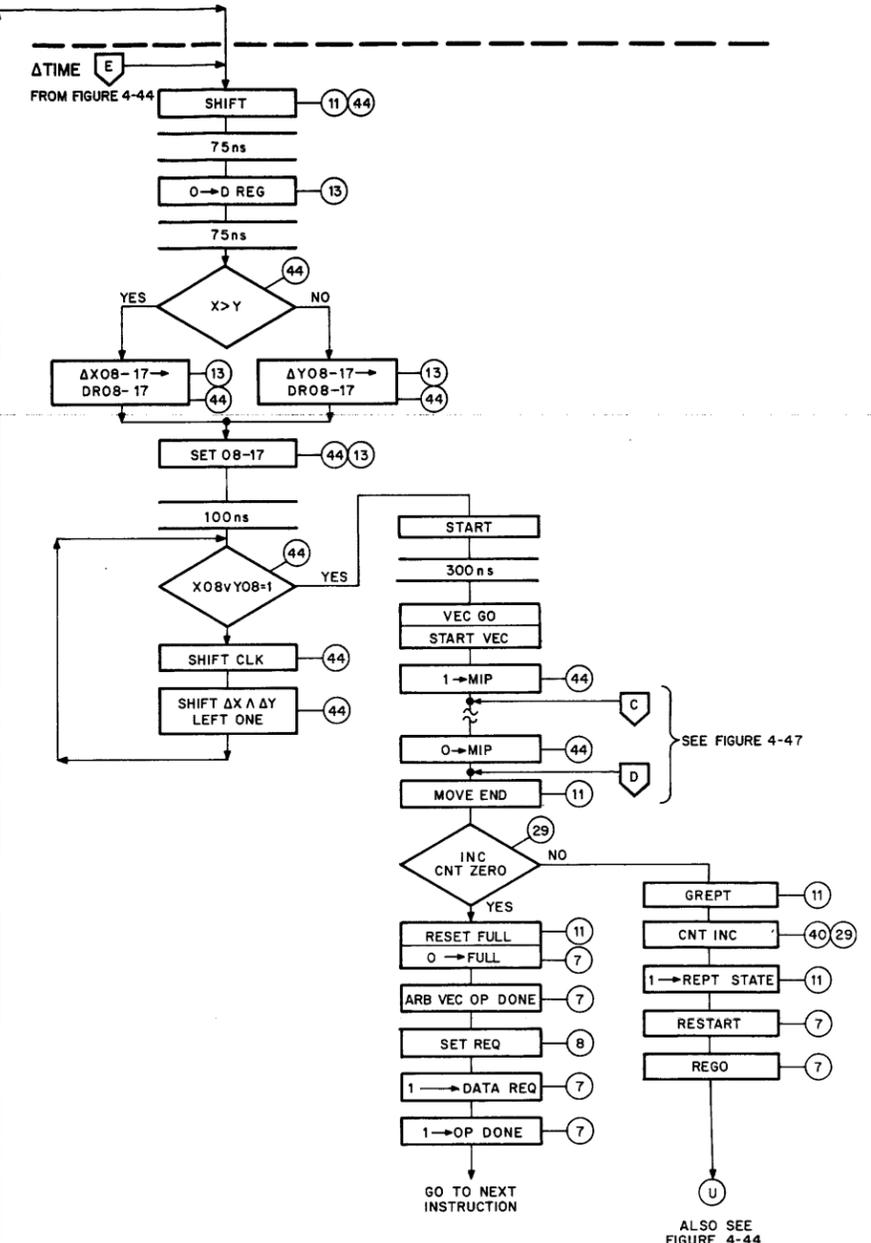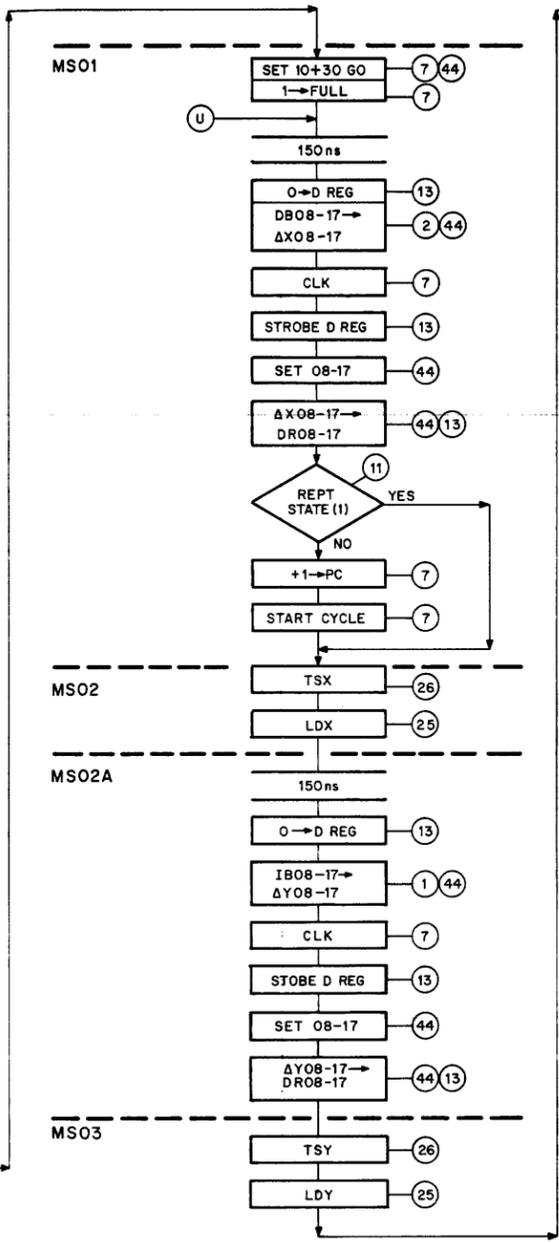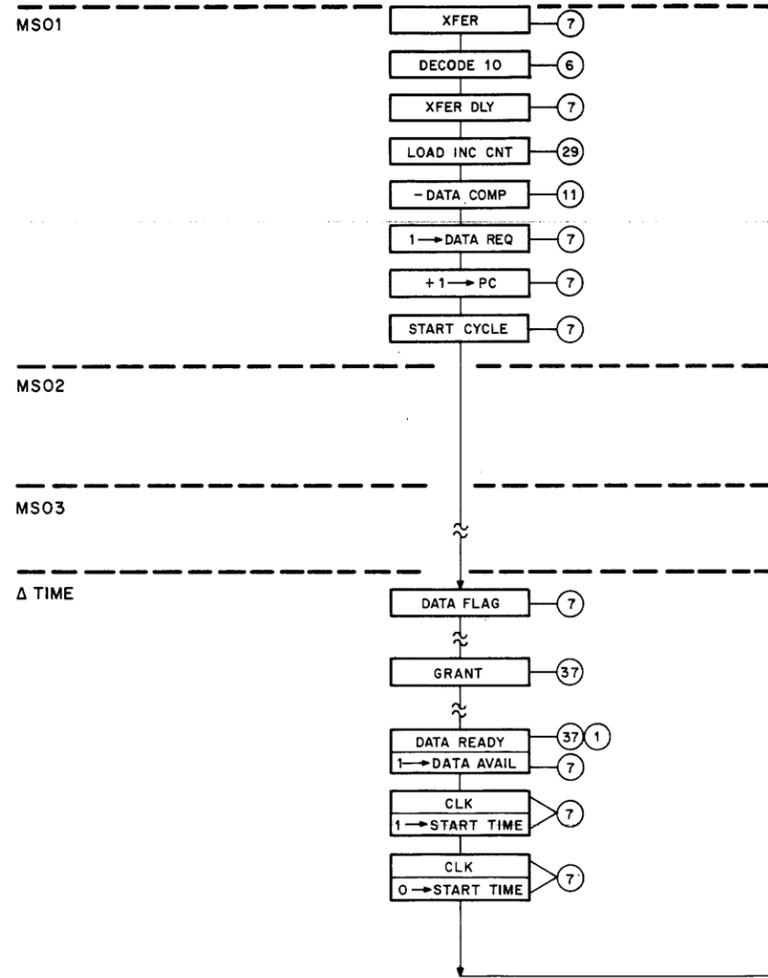
Figure 4-43b Arbitrary Vector Flow Diagram

MSO1

XFER — 7
DECODE 1O — 6
XFER DLY — 7
LOAD INC CNT — 29
– DATA COMP — 11
1 → DATA REQ — 7
+1 → PC — 7
START CYCLE — 7

MSO2

MSO3

Δ TIME

DATA FLAG — 7
GRANT — 37
DATA READY / 1 → DATA AVAIL — 37 1 / 7
CLK / 1 → START TIME — 7
CLK / O → START TIME — 7

MSO1

SET 1O+30 GO — 7 44
1 → FULL — 7
U
150 ns
O → D REG — 13
DB08-17 → ΔX08-17 — 2 44
CLK — 7
STROBE D REG — 13
SET O8-17 — 44
ΔX08-17 → DR08-17 — 44 13
REPT STATE (1) — 11   YES
NO
+1 → PC — 7
START CYCLE — 7

MSO2

TSX — 26
LDX — 25

MSO2A

150 ns
O → D REG — 13
IB08-17 → ΔY08-17 — 1 44
CLK — 7
STOBE D REG — 13
SET O8-17 — 44
ΔY08-17 → DR08-17 — 44 13

MSO3

TSY — 26
LDY — 25

ΔTIME E
FROM FIGURE 4-44

SHIFT — 11 44
75 ns
O → D REG — 13
75 ns
X > Y — 44   YES / NO
ΔX08-17 → DR08-17 — 13 44 (YES side)
ΔY08-17 → DR08-17 — 13 44 (NO side)
SET O8-17 — 44 13
100 ns
X08vY08=1 — 44   YES
SHIFT CLK — 44
SHIFT ΔX ∧ ΔY LEFT ONE — 44

START
300 ns
VEC GO START VEC
1 → MIP — 44   C
0 → MIP — 44   D
MOVE END — 11
INC CNT ZERO — 29   NO
YES
RESET FULL — 11
O → FULL — 7
ARB VEC OP DONE — 7
SET REQ — 8
1 → DATA REQ — 7
1 → OP DONE — 7

GO TO NEXT INSTRUCTION

SEE FIGURE 4-47

GREPT — 11
CNT INC — 40 29
1 → REPT STATE — 11
RESTART — 7
REGO — 7

U

ALSO SEE FIGURE 4-44

15-0626

```
(-X, +Y)              (0, +Y)              (+X, +Y)



           II                      I



-(-X, 0)— — — — — —  • — — — — — —(+X, 0)-



           III                     IV



(-X, -Y)              (0, -Y)              (+X, -Y)
```

15-0634

a. Size – Vector length can be expanded through the use of the 4-bit increment field (bits 14 through 17) of the parameter 1 instruction. The content of the increment register is processed (read) for each individual vector to examine the data for repeatability. Each vector is repeated the number of times specified by the value of the data word contained in the increment register.

b. Rotation – Arbitrary vectors cannot be rotated, as in the case of basic vectors and characters using the parameter 2 instruction.

c. Blink – Individual vectors can be blinked by previously setting BLINK ENA bit 8 and BLINK ON/OFF bit 9 of the parameter 2 instruction.

d. Dash – Various combinations of line selection bits 16 and 17 of the parameter 3 instruction allow the selection of various dashed line combinations depending on the content of the line selection register.

4.5.9.2 Arbitrary Short Vector – The arbitrary short vector instruction (see Figure 4-44) uses the 4-bit operating code 30_8 that occupies bits 0 through 3. This instruction is used for short vectors (intensified) or moves (unintensified) in any arbitrary direction. One major difference between arbitrary vector and short arbitrary vector is that the arbitrary short vector is comprised of a single word that contains the data required to define both the ΔX and ΔY components; two words are required for arbitrary vector. Since the arbitrary short vector instruction uses only a single word, the double-buffering method used with other VT15 instructions can be used; this method cannot be used with the arbitrary long vector instruction due to the two-word formatting structure that is used. Bits 4 and 5 of the arbitrary short vector instruction are used in the same manner as described for the arbitrary vector instruction. The basic format of the instruction is similar to that of the arbitrary vector instruction except two vector direction bits (bits 6 and 12) are used and both ΔX (bits 7 through 11) and ΔY (bits 13 through 17) are defined in the single word. Bit 6 defines the vector direction for ΔX and bit 12 defines the vector direction for ΔY.

Other parameters that can be established using other display file instructions are the same as described for arbitrary vector in Paragraph 4.5.9.1.

ARBITRARY SHORT VECTOR

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
0	1	1	0	INT 0=OFF 1=ON	LP FLAG ENA	(+)= 0 (−)= 1		5 BITS ΔX				(+)=0 (−)= 1		5 BITS ΔY			

MSO1

XFER —⑦

DECODE 30 —⑥

XFER DLY —⑦
LOAD INC CNT —㉙
SET 10+30 GO —⑦
1 → FULL —⑦

See figure 4-43 Ⓤ
Arbitrary Vector

CX —㉕

DB06=0

NO ~ + X —㉖

YES ㉖— + X

0 → D REG —⑬
DB07-11→ΔX13-17 —②㊹

CY —㉕

DB12=0

NO ~ + Y —㉖

YES ㉖— + Y

CLK —⑦
STROBE D REG —⑬
SET 13-17 —㊹
ΔX08-17→DR08-17 —㊹⑬

RE PT STATE ? —⑪

YES

NO

+1 → PC —⑦
START CYCLE

MSO2

TSX —㉖

LDX —㉕

MSO2A

150ns

0 → D REG —⑬
DB13-17→ΔY 13-17 —②㊹

CLK —⑦
STROBE D REG —⑬
SET 13-17 —㊹
ΔY08-17→DR08-17 —㊹⑬

MSO3

TSY —㉖

LDY —㉕

ΔTIME

Ⓔ See figure 4-43 Arbitrary Vector

15-0629

Figure 4-44   Arbitrary Short Vector Flow Diagram

4-74

4.5.10 Slave

The 18-bit slave instruction (see Figure 4-45) is used when the VM15 Display Console Multiplexer option is included as part of the system and more than one VT04/VT07 is connected to and controlled by the VT15. The instruction uses the 4-bit operating code 34_8 that occupies bits 0 through 3. Bits 4 through 9 are not used. This instruction allows up to four VT04/VT07 display consoles to be selectively blanked or unblanked. In addition it is used to control the light pen enable (LP ENA) function of each display. Bits 11, 13, 15, and 17 are used to selectively blank or unblank any one of the four display consoles (units 00 through 03). For example, with only intensity enable (INT ENA) bit 13 set, only the CRT of unit 01 will be enabled. Bits 10, 12, 14, and 16 are the light pen enable (LP ENA) bits that are used to enable or disable the light pens. Two additional functions that evolve from LP ENA are light pen sense indicator (LPSI) and light pen flag (LP FLAG). LP FLAG causes the display to halt, whereas LPSI does not. Light pen, intensity, and pushbutton control through the parameter 1, 2, and 3 instructions and the various IOT commands is the same with the VM15 option installed
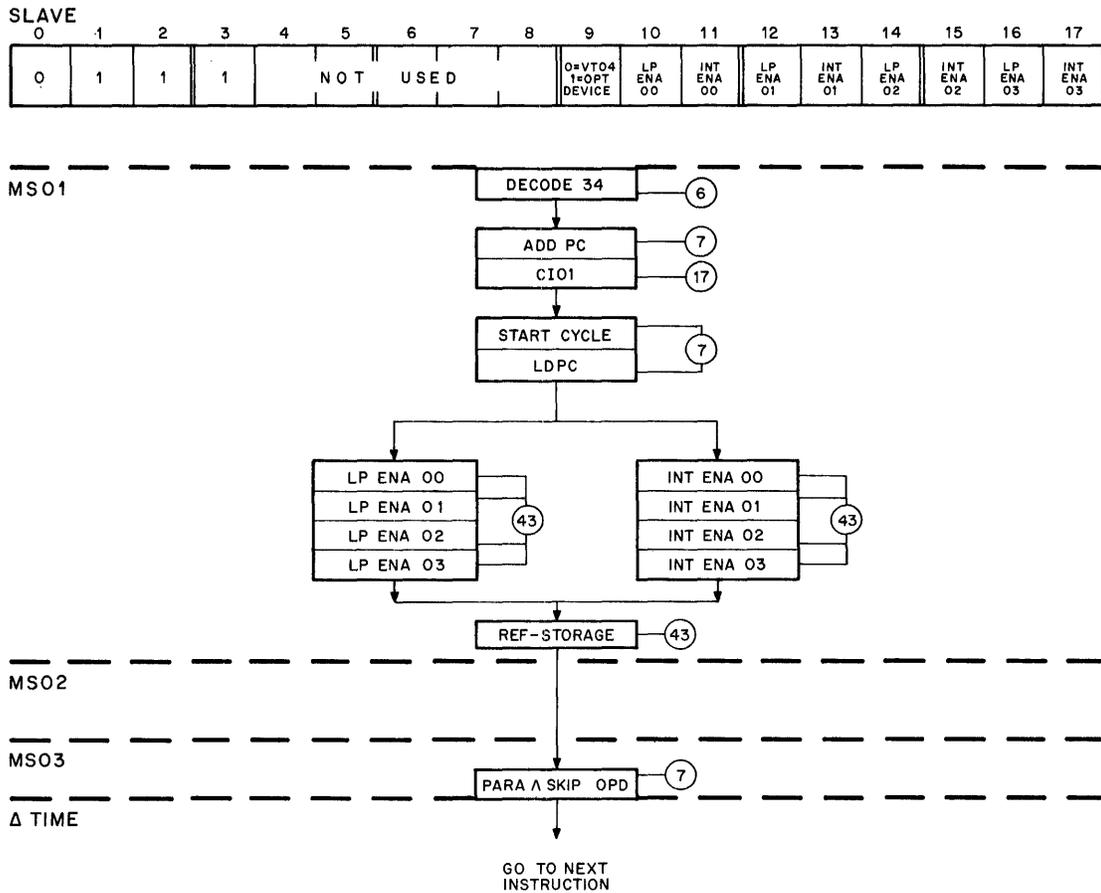
Figure 4-45   Slave Instruction Flow Diagram

as without, except that control of the displays may be selectively exercised through the unit select bits of the slave and skip 1 instructions. With the VM15 option installed, the skip 1 instruction is used in the same manner as without the option, except bits 16 and 17 of the instruction are used as the unit select (or console address) bits.

4.5.11   Rotate

Rotate is used by the operator to rotate basic vectors or characters 90° counterclockwise. The rotate function may be used with the basic vector, basic short vector, character input, and character string instructions. Rotate is accomplished through bits 12 and 13 of the parameter 2 instruction, described in Paragraph 4.5.1.2. Bit 12 is used as the ROTATE ENA bit and bit 13 is used as the rotate bit. A functional flow diagram of the rotate function is provided in Figure 4-46.

4.5.12   Sector Re-entry

The sector re-entry function is used when operating outside the VT04/VT07 screen area (sector 0). When returning to sector 0, the CRT monitor requires settling time, thus a 20-µs delay is introduced to allow sufficient settling time. The sector re-entry function is used in conjunction with character and vector instructions. A functional flow diagram of the sector re-entry function is provided in Figure 4-47.
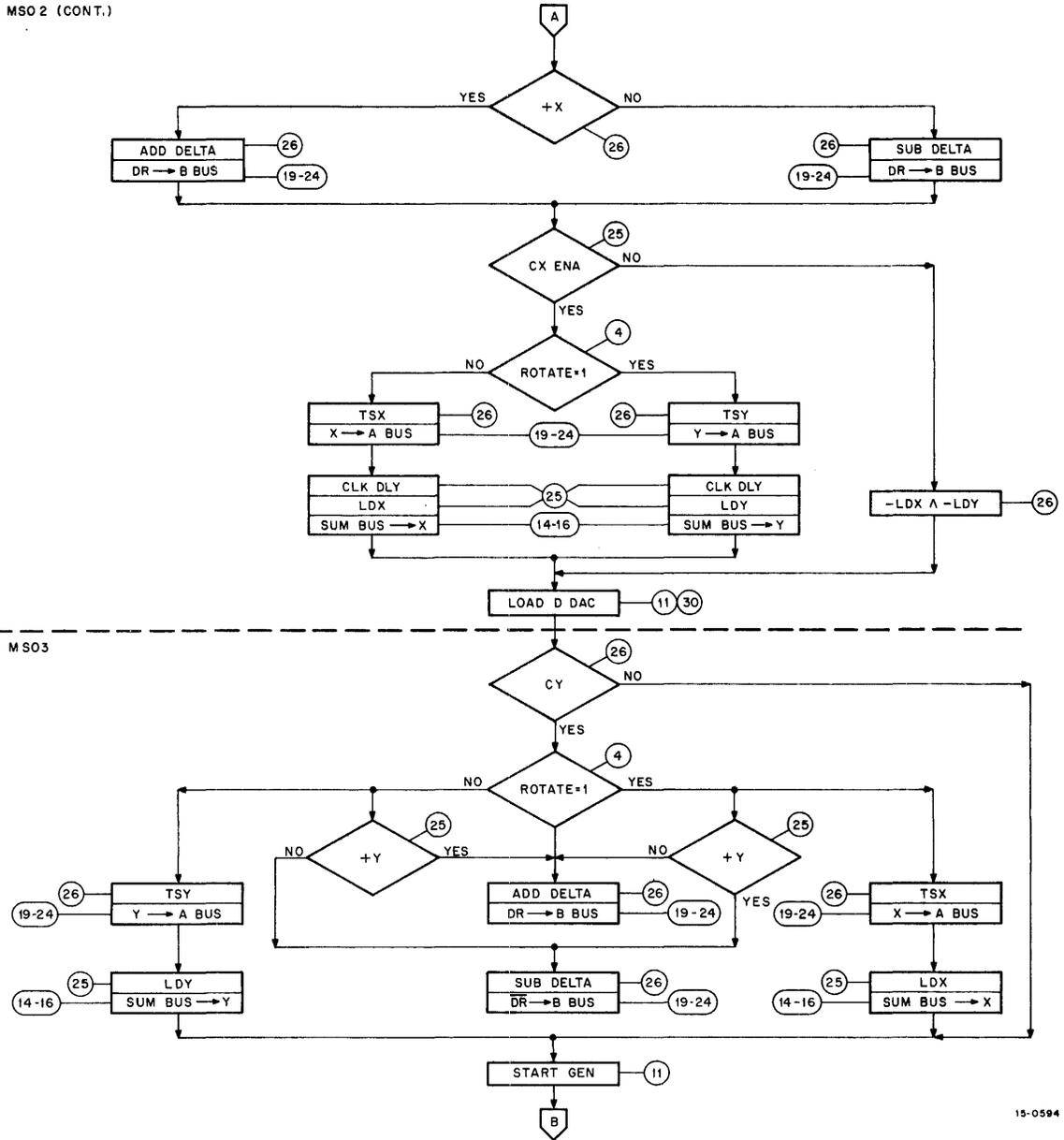
Figure 4-46   Rotate Flow Diagram
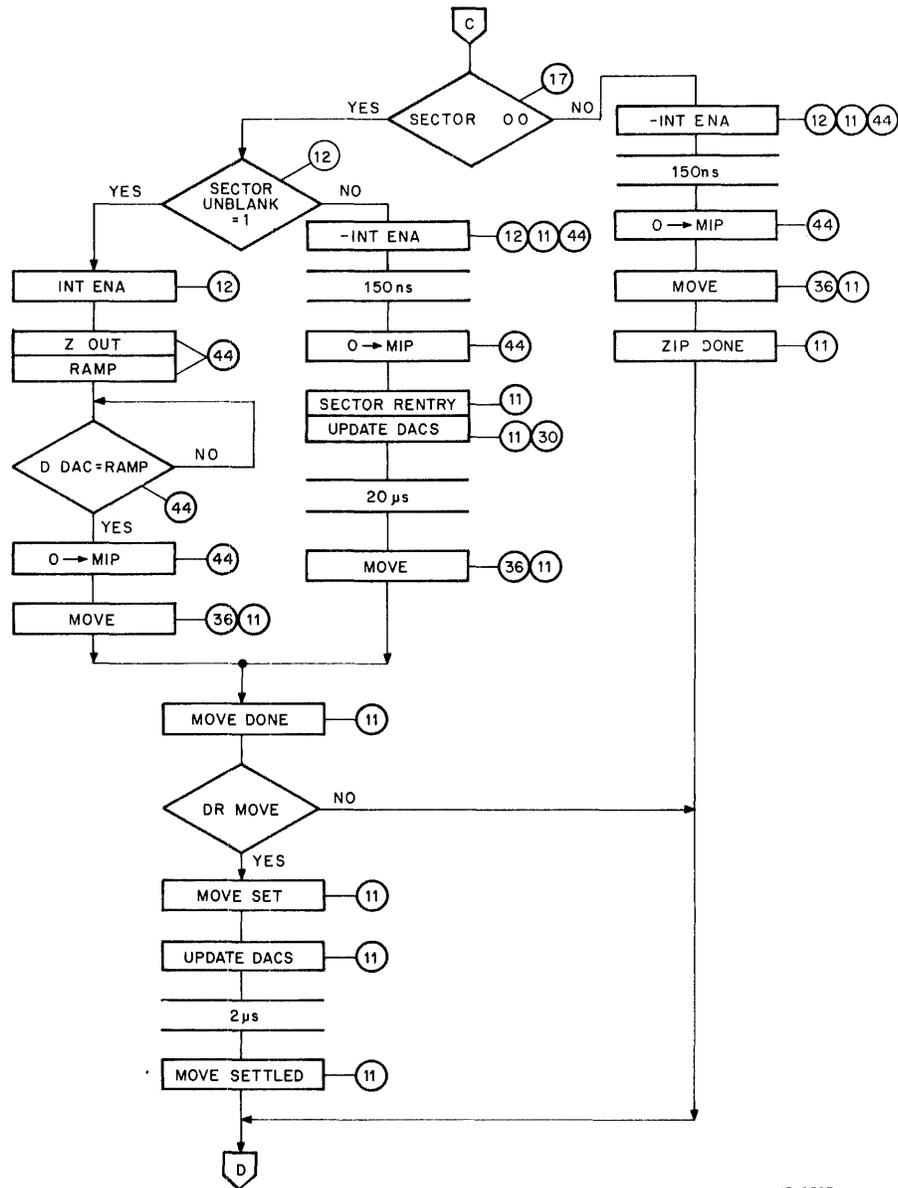
15-0594

Figure 4-47   Sector Re-Entry Flow Diagram

15-0593

CHAPTER 5
SPECIAL MODULES

5.1 GENERAL

The VT15 Graphic Processor contains seven modules that are unique to the VT15. This chapter provides detailed descriptions of these modules. Schematic diagrams for each of the modules are provided in Volume 2. Respective module titles and their individual Volume 2 drawing reference numbers are provided in Table 5-1.

Table 5-1
Special Module Drawing Reference Numbers

Module Title	Volume 2 Drawing Reference No.
Digital-to-Analog Converter A618YA	D-CS-A618YA-0-1
ROM Diode Matrix and Decoder G618	D-CS-G618-0-1
ROM Diode Matrix Receiver M762	D-CS-M762-0-1
32 - to - 8-Bit Multiplexer M761	D-CS-M761-0-1
Vector Generator A3180	D-CS-A3180-0-1
Dual Analog Switch A140	C-CS-A140-0-1
Dual Analog Summer Driver A238	D-CS-A238-0-1
Digital-to-Analog Converter A622	D-CS-A622-0-1
Arbitrary Vector Generator A3170	D-CS-A3170-0-1
Arbitrary Vector Timing and Control M7010	E-CS-M7010-0-1

5.1.1 M Series Measurement Definitions

Timing is measured with the input driven by a gate or pulse amplifier of the series under test. The output is loaded with gates of the same series unless otherwise specified. Percentages are assigned with 0 percent indicating the initial steady-state level and 100 percent indicating the final steady-state level, regardless of the direction of change.

Input/output delay is the time difference between input change and output change, measured from 50 percent input change to 50 percent output change. Rise and fall delays for the same module are usually specified separately.

Rise time and fall time are measured from 10 percent to 90 percent of waveform change, either rising or falling.

5.1.2 Loading

Input loading and output driving are specified in "units", with one unit equivalent to 1.6 mA. The inputs to low-speed gates usually draw 1 unit of load; high-speed gates draw 1.25 units, or 2 mA.

5.1.3 Parts Location

A parts location diagram is provided as an example of modules containing numerous discrete components and integrated circuits. The location of parts on integrated circuit modules can be determined by visual inspection and circuit schematic reference.

"E" designators are assigned to integrated circuits according to the following convention: viewing the component side of the module, "E" numbers are assigned from right-to-left within each horizontal row, beginning with the top row. See the example given in Figure 5-1. This figure illustrates this convention with typical symbols used in parts location diagrams.

NOTES
1. ▭ Indicates diode polarity ─▷├─
2. E9 is an integrated circuit operational amplifier.
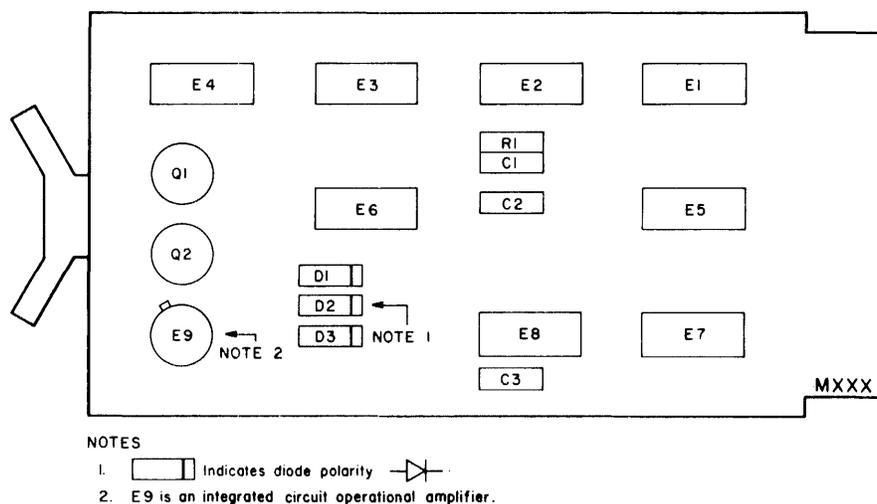
15-0173

Figure 5-1 Parts Location - Example Diagram

5-2

5.1.4 Digital-to-Analog Converter A618YA

The A618YA Module contains a 10-bit D/A converter consisting of a 10-bit buffer, a binary weighting network, and a current summing amplifier. The reference voltage used in the binary weighting network is supplied externally. Data on register input lines must be settled 20 ns before the leading edge (positive-going voltage of the CLOCK pulse) passes the threshold voltage and should remain stable for 5 ns afterward. Duration of the CLOCK pulse should be at least 50 ns. Data present at the input of the register is transferred to the output when the leading edge of the CLOCK pulse passes the threshold. The analog output voltage is unipolar and varies from 0.0V to 5.115V (in 5 mV increments) in accordance with the value(s) of the binary input data. One 20-ohm potentiometer (R62) is located on the module and is used for trim adjustment of the operational amplifier feedback loop, to allow minimal adjustment of the operational amplifier gain.

Any A618YA Modules that are found to be defective should be replaced. Defective modules should be returned to the factory for repair.

5.1.5 Digital-to-Analog Converter A622

The A622 Modules contain a 10-bit input buffer and a 10-bit D/A converter containing a binary weighting network and a current summing amplifier. The reference voltage used in the D/A converter is supplied internally. Data-on register input lines must be settled 20 ns before the leading edge (negative-going transition of the CLOCK pulse) passes the threshold voltage and should remain stable for 5 ns afterward. Duration of the CLOCK pulse should be at least 30 ns. Data present at the input of the register is transferred to the output when the leading edge of the CLOCK pulse passes the threshold. The analog output voltage is unipolar and varies from 0.0V to 5.115V (in 5 mV increments) in accordance with the value(s) of the binary input data.

Any A622 Modules that are found to be defective should be replaced. Defective modules should be returned to the factory for repair.

5.1.6 Read-Only Memory Matrix and Decode G618

The read-only memory (ROM) G618 Module contains 512 diodes connected to form a 32 x 16 diode matrix. Desired characters are generated by the removal of selected diodes within a chosen byte and word. One byte contains 8 bits; one word contains 32 bits. Up to 2 words (8 bytes) or 64 bits can be utilized per each character. Not all characters use the full 8-byte complement.

Eight G618 Modules are utilized within the VT15 Character Generator Read-Only Memory as shown in Drawing VT15-0-41 of Volume 2. Inputs to the eight G618 Modules are derived from the following modules:

a. M163 Dual Binary-to-Decimal Decoder
b. M627 NAND Power Amplifier
c. M117 and M113 Word Selection Flip-Flop

Characters that are derived from individual G618 Modules and module designator numbers are listed in Table 5-2. Refer to Table 2-3 of the Graphic-15 Reference Manual for a more detailed listing of ASCII characters and ASCII character codes.

Table 5-2
ASCII Character Decoding

G618 Module Designator No.	Characters Derived	ASCII Octal Code
YA	@ through G	100 through 107
YB	H through O	110 through 117
YC	P through W	120 through 127
YD	X through "underline"	130 through 137
YE	"Space" through ","	040 through 047
YF	"(" through "/"	050 through 057
YG	0 through 7	060 through 067
YH	8 through "ampersand"	070 through 077

Four other functions listed in Table 2-3 of the Graphic-15 Reference Manual are hardware-derived characters; these characters and their octal codes are listed in Table 5-3.

Table 5-3
Hardware Generated Characters

Character or Function	ASCII Octal Code
TAB	011
LF	012
CR	015
ALT MODE	175

Hardware-derived characters can be described as functions, because they are nondisplayed, non-printed characters.

The ROM control inputs consist of CB00 through CB05. An additional input, other than CB00 through CB05, is also used. This additional input is complemented upon completion of the first word to allow selection of the next (second) word. The CB00 through CB02 inputs that are applied to the M163

Decoder determine which individual module of the eight G618 Modules (YA through YH) is selected. Control characters CB03, CB04, and CB05 permit decoding and character selection within the individual modules.

At the beginning of each ASCII character, the six least-significant bits of the ASCII code, contained in the data buffer, are loaded into CB00 through CB05. The most significant digit is loaded into the CBHR flip-flop and CBHR and CB00 are compared. If they are equal, further decoding tests for the control functions (TAB, CR, LF, and ALT MODE) are inhibited and illegal characters will be ignored. The control characters and the modules selected are listed in Table 5-4.

Table 5-4
ROM Memory G618 Module Selection

Control Character			Module Selected
CB00	CB01	CB02	
0	0	0	YA
0	0	1	YB
0	1	0	YC
0	1	1	YD
1	0	0	YE
1	0	1	YF
1	1	0	YG·
1	1	1	YH

An example of the decoding necessary to generate the character "A" is provided in Figure 5-2 and Table 5-5.

CBHR	CB00	CB01	CB02	CB03	CB04	CB05
1	0	0	0	0	0	1

SELECTS BOARD "YA"   SELECTS DESIRED CHARACTER

15-0271
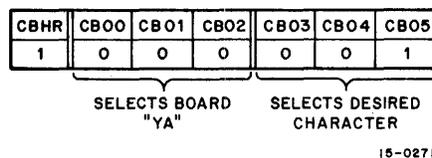
Figure 5-2   Character "YA" Board and Character Selection

Table 5-5 illustrates the method through which the respective bytes and bits are decoded to generate the character "A" (illustrated in Figure 5-2).

Six to eight movements of the beam are normally required to generate one character; some special characters require fewer moves. Individual moves or vectors are represented by 3-digit octal codes.

Table 5-5
Character "A" Byte and Bit Decoding

Byte No.	ESC	Intensity	Direction			Δ Factor			Octal
1	0	1	0	1	0	1	1	0	126
2	0	1	0	0	0	1	0	0	104
3	0	1	1	1	0	0	0	0	166
4	0	0	1	0	0	0	0	1	041
5	0	0	0	1	1	0	1	1	033
6	0	1	0	0	0	1	0	0	104
7	1	0	1	1	1	0	1	1	273
8	Not used								

NOTE: The escape (ESC) bit in byte 7 is set, and byte 8 is not used.

For example, when generating the first (100) character "@" on the YA board (see Appendix A), the 3-digit octal code representing the first move or vector is 01 010 110 or 126_8. The initial digit (two bits) indicates whether the vector is intensified (1) or unintensified (0 or 2). The second digit (three bits) determines the vector direction and is any octal number between 0 and 7. The third digit (three bits) indicates the vector length of magnitude and can also be any number between 0 and 7. Thus, the octal code 126_8 (8 bits) representing the first move of the character "@", indicates that the first move will be intensified $(01=1_8)$, that the vector will be drawn in direction 2 $(010=2_8)$, and that vector length or magnitude will be 6 units $(110=6_8)$. For information concerning the eight vector directions refer to Figure 4-27.

Figure 5-3 further illustrates character byte and bit decoding as well as how to read the three-bit octal codes directly from the G618 diode matrix. This is especially useful for isolating defective diodes during troubleshooting and maintenance procedures.

The characters used as examples in Figure 5-3 are the character "@" and the character "G". The character "@" is the first character on the YA board, and the character "G" is the last character.

Row 1 and row 2, containing two subrows each, are used to generate the character "@". Each row is read from left to right, beginning with row 1. The remaining rows, 3 through 14, are used to generate the characters "A" through "G".

Rows 3 through 14 are read from left to right in the same manner as described for rows 1 and 2, to generate the character "@".
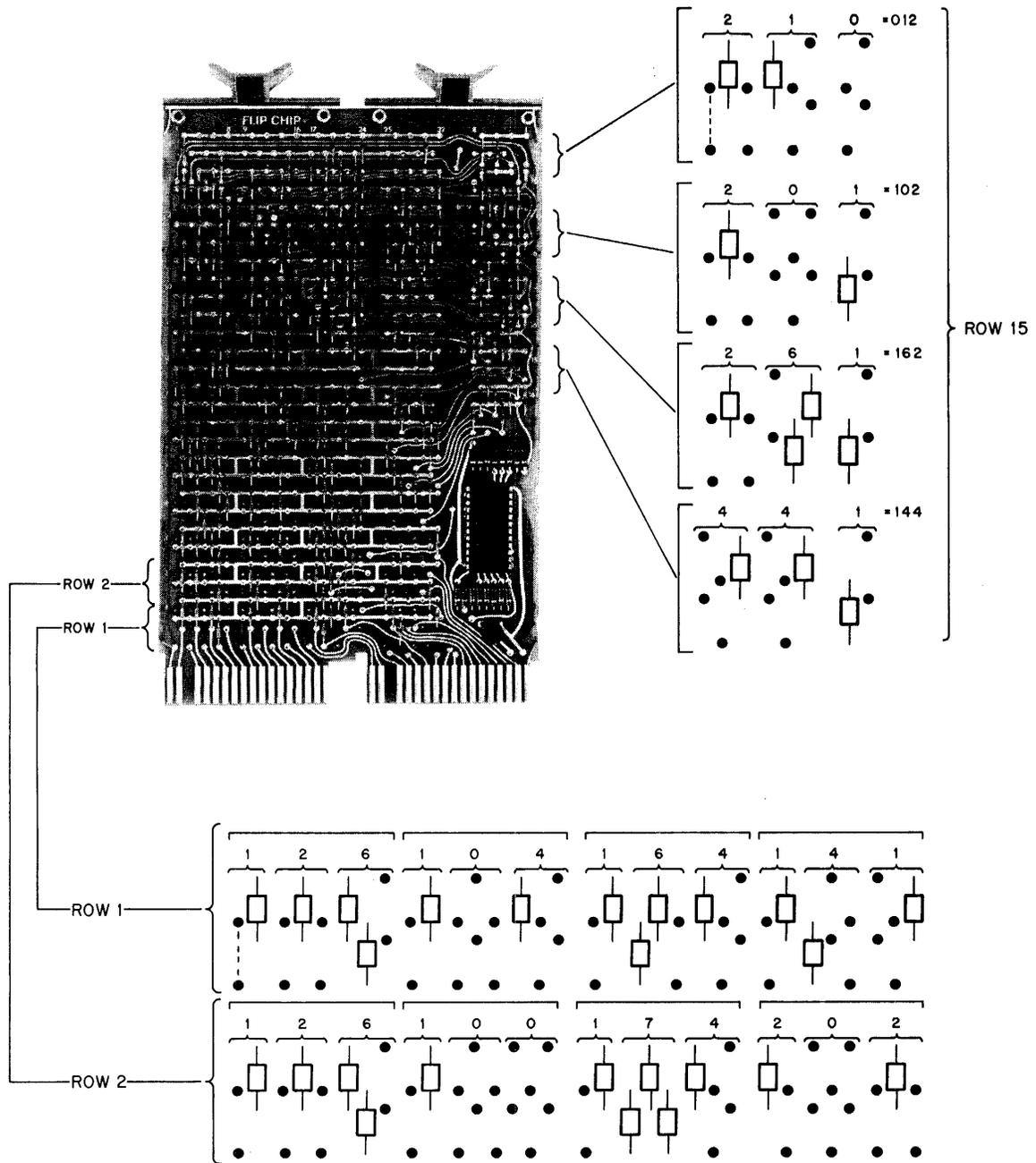
Figure 5-3   G618 Diode Matrix

Rows	Character Generated
3-4	A
5-6	B
7-8	C
9-10	D
11-12	E
13-14	F
15-16	G

Rows 15 and 16 must be read differently than rows 1 through 14. Referring to Figure 5-3, and rows 15 and 16, note that rows 15 and 16 occur alternately, reading from top to bottom. Individual bits are read from right to left.

For example, the first move or vector in the character "G" is contained in row 15, bits 1 through 8. Reading from right to left, the first eight bits would equate to 00 001 010 or 012_8, indicating that the first move or vector will be unintensified (0), that the beam will be moved in direction 1, and that the beam will be moved 2 units.

Skipping the next row, which is the first 8 bits of row 16, the next 8 bits of row 15 are read from right to left yielding 01 000 010=102_8, indicating that the second move or vector for the character "G" will be intensified (1), that the vector direction is 2, and that vector length or magnitude will be 2 units.

The three-digit octal codes for example characters "@" and "G" are as follows:

"@"	"G"
126	012
104	102
164	162
141	144
122	126
142	104
174	063
203	273

All eight moves for the character "@" are shown in Figure 5-3; however, only the first four moves of the character "G" are provided. The remaining four moves (row 16) for character "G" are read or decoded in the same manner as the four moves described for row 15.

5.1.7 ROM Diode Matrix Receiver M762

Two M762 Modules are used in the VT15 Character Generator Read-Only Memory. The selected data word consisting of 32 bits is applied to the two M762 Modules, 16 bits per module. Essentially, the M762 Modules are utilized as active pullup switches (referenced to the +5V source) that actively sink the stored charge of the diode junctions within the ROM diode matrix, effectively decreasing cycle time.

5.1.8 Thirty-Two to Eight Bit Multiplexer M761

The VT15 Character Generator Read-Only Memory utilizes one M761 Module. Inputs are derived from the two M762 Modules described in Paragraph 5.1.6. Thirty-two bits are received by the M761 Module; these bits are decoded into four unique bytes from which escape, intensity, direction, and Δ factor are derived. These unique bytes are enabled according to the condition of a byte counter consisting of two JK flip-flops (E5 and E8). The two flip-flops are initially set to a (1) at pin 2 (the LDCB pulse from the Character Generator logic) to initiate the first move of the desired character. The byte counter sequence is as shown in Table 5-6.

Table 5-6
M761 Byte Counter

Counter State		Byte Derived
E8	E5	
0	0	Byte 1
0	1	Byte 2
1	0	Byte 3
1	1	Byte 4

Table 5-7 is provided to translate the bit numbers on Drawing M761-0-1 to the output signal designations on the M761 Module located on Drawing VT15-0-41.

Table 5-8 defines the M762 Module outputs and their respective parameters. These outputs are applied to the memory decoder "CH" and "D" register (M216, pin D14), which is also part of the Character Generator Read-Only Memory.

5-9

Table 5-7
Module Output Designations

Drawing M761-0-1	Drawing VT15-0-41
Bit 1	BCH00
Bit 2	BCH01
Bit 3	BCH02
Bit 4	BCH03
Bit 5	BCH04
Bit 6	CH05
Bit 7	CH06
Bit 8	CH07

Table 5-8
M761 Module Output Designations and Parameters

M761 Outputs	Parameters	Memory Decoder Outputs
BCH00	1 = ESC	CH00
BCH01	Intensity 1 = ON	CH01
	0 = OFF	
BCH02	Direction	CH02
BCH03	Direction	CH03
BCH04	Direction	CH04
CH05	Δ (Magnitude)	DR14
CH06	Δ (Magnitude)	DR15
CH07	Δ (Magnitude)	DR16

5.1.9   Vector Generator A3180

The vector generator is shown on Drawing A3180-0-1 and Drawing VT15-0-44.

The MIP flip-flop, consisting of two NAND gates (E15) controls the operation of the A3180 integrator circuit. The flip-flop is initially cleared (reset) by a START CLR L at input AS2. The START VEC L signal sets RS flip-flop F14 (see Drawing VT15-0-44), which in turn sets the MIP flip-flop to begin integration. E15 Pin 6 goes high, is inverted by E14, and a low signal is applied to MOSFET Q1's gate. This low voltage is just sufficient to turn Q1 off. With Q1 off, C12 is placed into the integrator circuit consisting of E10 and E11. E10 is an operational amplifier; E11 is a voltage follower. C12 charges linearly as current is fed into E10 pin 2 through R3. The voltage at the junction of R1, R2 and R3 is established by voltage division and equals ≈ -5 V. The integrator ramp output, taken from pin BU2 is fed to the multiplying DACs (M-DACs) on A3170.

5-10

Another source of current to E10 pin 2 is E12. This current will increase the slope of the ramp output of the integrator, and thereby compensate for the multiplication factor of the M-DACs. To provide a constant drawing rate for all vectors, the slope of the M-DAC output which corresponds to the greater component of the vector being drawn, must not vary from vector to vector. The amount of current supplied by E12 depends on the voltage output of A1, a digital to analog converter. The digital input to A1 (Pins 11-20) is the inverted normalized value of the greater component (major axis) of the vector being generated.

X08 through X17 and Y08 through Y17 are the normalized values of the X component and Y component of the vector being generated. They are inverted and fed to a multiplexer (E4, E2 and E8). If the Y component of the vector is greater than or equal to the X component (X > Y H at pin AS1 a low), the Y values are selected as inputs to D/A converter A1. The X values are selected otherwise. The voltage output of the D/A converter and thus the current output of driver E12 vary inversely with the normalized magnitude of the greater component (X or Y) of the vector.

As an example, assume a vector is to be drawn with $X = 0000_8$, $Y = 1777_8$. After normalization $X = 0000_8$, $Y = 1777_8$. Since $Y > X$, the input to D/A converter A1 is Y inverted, or 0000_8. The output of A1 will be 0 V, and E12 will not supply current to E10; the ramp generated by E10 is un-compensated. In the Y-axis M-DAC, and associated amplifiers (E1 and E4), this ramp is multiplied by a factor of 1 as determined by Y normalized = 1777_8. If we now halved the value of the Y com-ponent of the vector, $Y = 1000_8$, Y normalized = 1000_8. The input to the D/A converter would be 0777_8, yielding an output of .5 V. E2 with its gain of -10 would have an output of -5 V, and would supply the same amount of current through R7 as normally flows through R3. The current into E10 pin 2 would be double what it was with Y normalized = 1777_8. The slope of the ramp input to the Y-axis M-DAC would also be double what it was. However, the M-DAC output does NOT change, because now the Y-axis M-DAC and associated amplifiers are multiplying by .5 (as determined by $Y = 1000_8$).

The MIP flip-flop also enables vector intensification. When set, a low is provided to E9 pin 9 through inverters E14. C11 and current source diode D3 delay this function to allow sufficient time for E5, the scope intensification delay one-shot, to trigger. This prevents spurious intensification. R9, R20, and D2 prevent E14 pin 4 from going more positive than 3.5 V; this allows D3 to remain in an on state. When E14 pin 4 goes low, it shorts out C11 and generates a quick turn-off of intensity.

Integration and intensification terminates when comparator E13 resets the MIP flip-flop. With the MIP flip-flop reset; Q1 turns on, discharging C12; E9 is disabled with a high at pin 9. The compara-tor output goes low, when it senses the completion of the vector, as determined by equality of its two inputs. The input at pin BN2 is D ANALOG; the value specified for the greater component of the vector. Pin AV2 is the CONTROL RAMP; the ramp, selected on A3170, that generates the greater

component of the vector. R18 allows for vector length adjustments by offsetting the D ANALOG voltage. D4 and D5 prevent variations in the ± 15 V from affecting the vector length adjustment.

5.1.10 VV15 Timing and Control M7010

The M7010 Module (see Drawings VT15-0-44 and M7010-0-1) consists of an input data multiplexer (comprised of five 12-bit multiplexers), two 10-bit (ΔX and ΔY) holding registers, arbitrary vector control and timing logic, a digital magnitude comparator, and ΔX and ΔY output gating.

The M7010 Module provides the timing and control to process arbitrary vector digital data received from the data buffer (DB) and input buffer (IB). The X and Y digital inputs to the M7010 Module are received via the input multiplexer (E3, E7, E12, E20, and E21), and the multiplexer outputs are connected to the ΔX (E8) and ΔY (E13) storage registers.

The received ΔX and ΔY data is unpacked in format; the format is dependent upon the instruction used. The two instructions that can be used are the "10" instruction, arbitrary vector, and the "30" instruction, short arbitrary vector. If arbitrary vector is used, two 18-bit words are required. The 10 L input at pin AM1 multiplexes DB08 through DB17 to the ΔX storage register, and IB 08 through IB 17 to the ΔY storage register. The 30 L input at pin AL 1 multiplexes DB08 through DB12 to the low order bits of the ΔX storage register, and DB13 through DB17 to the low order bits of the ΔY storage register. When basic vectors are generated, 10 L and 30 L are high, causing E19 pin 4 to go high and strobe the multiplexer outputs X08 through X17 and Y08 through Y17, to all ones.

When SET 10 + 30 GO is received at pin AK1, it sets flip-flop E2, and initiates arbitrary vector timing; E14 pins 3 and 5 receive enabling inputs. At time state MS01, the ΔX data is loaded into the ΔX storage register from the multiplexer. The ΔX data is then strobed by STROBE D REG H at pin BF1 to the D register (Drawing VT15-0-13 and Figure 3-7), from which it is later used to update the X Position Register. At time state MS02A, the ΔY data is loaded into the ΔY storage register, and is then strobed by STROBE D REG H to the D register, this time to update the Y Position Register. The output gating to the D Register consists of E5, E9, E11, E15 and E18.

The ΔX and ΔY storage register outputs are input to a digital comparator (E6, E10, E16) where the values of ΔX and ΔY are compared to determine which is the greater. The comparator output X > Y H determines which data (ΔX or ΔY) will now be strobed to the D Register. If X > Y H is asserted ΔX is strobed; ΔY is strobed otherwise. When MS03 · CLK DLY L (pin BS1) is asserted the D Register is strobed with ΔX or ΔY data, depending on which is greater. This time the D Register is used to update the D-DAC, which will determine the length of the arbitrary vector being drawn. SHIFT L (pin AN1) is asserted at the end of MS03 and enables the multiplexer and storage registers for

shift left operation. MS03 · CLK DLY L initiates the shift left clocking. Shift timing consists of a 250-ns delay line that is part of a timing loop. The MS03 CLK DLY pulse is input to the delay line and the timing sequence occurs as the pulse travels down the delay line. If a logical 1 is not sensed in the MSB of either storage register, the pulse is reshaped and recycled. The shift-left operation continues until a logical 1 is sensed at E1 pins 5 or 6. A low at E1 pin 4 disables the SHIFT CLOCK pulses and generates START H at pin BB1; normalization is complete and vector generation in the A3180 module now begins.

5.1.11 Arbitrary Vector Generator A3170

The Arbitrary Vector Generator (Drawings DCS A3170-0-1 and DBS VT15-0-44) consists of M-DACs A1 and A2, with their associated amplifiers, and a control ramp select switch.

The POS RAMP output of the A3180 is input to pins BN2 and AV2 of the A3170 Arbitrary Vector Generator. The ramp at pin BN2 develops the X component of the vector. The Y component is developed from the input at pin AV2. The two inputs are processed similarly; POS RAMP at BN2 (AV2) is buffered by voltage follower E5 (E4) and is then fed to M-DAC A2 (A1). The multiplying factor in the M-DAC is determined by, and varies linearly with, X08 through X17 (Y08 through Y17), the normalized X (Y) component of the vector. The output of the M-DAC is a current source, which is converted to a voltage by R9 (R8). The voltage developed across R9 (R8) is then amplified by OP AMP E2 (E1). The gain of E2 (E1) is determined by the output impedance of the M-DACs and the ratio of [R11 + R6]/R15 (R10/R12), and nominally equals 4.3. R6 adjusts the gain of E2, and therefore controls relative gain. The over-all gain of E5, A2 and E2 (E4, A1 and E1) may vary from zero to one, depending on the values of X08 through X17 (Y08 through Y17). R4 (R2) controls the offset voltage to E2 (E1). R17 (R19) is an X (Y) ramp phase adjustment. It offsets the M-DAC input with respect to a response threshold voltage. With R17 and R19 properly set, the ramps output to the CRT deflection amplifiers start synchronously.

The outputs of E2 and E1 (ABR RAMP X and ABR RAMP Y) are fed to the A140 Dual Analog Switches. One of these output signals is also switched to the comparator on the A3180, where it is used as the CONTROL RAMP. The switching circuitry consists of MOSFETS Q1 and Q2, and E3. VT44 X > Y H is input to pin AF1, and is inverted and double inverted to drive the gates of Q1 and Q2. If the X component of the vector is greater than the Y component, X > Y H is high; this places 0 V at Q1s gate, (causing it to shut off), and +15 V at the gate of Q2. The +15 V causes Q2 to conduct, switching ABR RAMP X to pin AP2. With X > Y H a low, ABR RAMP Y is switched to pin AP2.

5.1.12 Dual Analog Switch A140

The VT15 contains two A140 modules (Drawings CCS-A140-0-1 and DBS-VT15-0-44) one switches ABR RAMP X, the other ABR RAMP Y. The ABR RAMP is switched to either the inverting, noninverting or neither input of the summer in the A238 module, depending on the direction in which the vector is being drawn. The ABR RAMP is input to pins J2 and V2. ENA X (Y) POS L, input to P2 will switch the ABR RAMP to voltage follower E1. Since pin N2 is at a TTL high (+3 V), a low at P2 will make E2 pin 3 high, causing Q1 to cut off. With Q1 off, D7 clamps the junction of R3 and R4 to ground, causing Q3 to cut off. With Q3 cut off, current source diode D1 changes capacitor C3 linearly from 0 V to a voltage of +10 V. The +10 V limit is determined by clamping diode D3 and zener D5. The voltage on C3 is applied as a switching input to the gates of Q5 and Q7. Q5, an enhancement mode FET, will conduct with its gate at 10 V; Q7 a depletion mode FET will be cut off. ABR RAMP is therefore switched through Q5 to E1, whose output is connected to the non-inverting summer input on A238.

With pin P2 high, Q1 and Q3 turn on. Q3 switches 0 V from pin F2 to the gates of Q5 and Q7. This pinches Q5 off, and turns Q7 on, applying ground from pin F2 to the input of E1. D6 and D7 prevent Q1 and Q3 from going into deep cut-off, and along with C15 and C16 speed the switching time of the transistors.

The circuitry comprised of Q2, Q4, Q6, Q8, and E3 operates identically. When ABR RAMP is switched to E3, it is fed to the inverting input of the summer, causing the vector to be drawn in a negative direction.

ENA X (Y) POS L and ENA X (Y) NEG L are never both active. When arbitrary vectors are generated, one or the other is asserted. When basic vectors are generated, one or the other or neither are asserted. Neither is asserted if the X (Y) component of the basic vector equals zero.

5.1.13 Dual Analog Summer Driver A238

The A238 (Drawings DCS-A238-0-1 and DBS-VT15-0-44) consists of two summer drivers; one for X deflection and one for Y. Summing is implemented by operational amplifiers (Type LM318), with weighted input resistance networks producing a gain of 1/2. E1 is the X-axis summing amplifier. Its inputs are the X ANALOG holding voltage at pin AP2, an offset voltage through R19, and an X-vector ramp at pin AK2 or AH2. If the X vector ramp is applied to pin AK2 (by the X axis A140) it will be inverted and summed, causing the vector to be drawn in the minus X direction. An X-vector ramp to the non-inverting input (pin AH2) causes the vector to be drawn in the positive X direction.

When the input at pin AT2 (-VT04 OFFSET (1) H) is high, E4 pin 6 is high. This causes the voltage at E2 pin 5 to be determined by voltage division of the -10 V established by zener D13. E2 pin 5 will be at -10 V X R29/[R29 + R23] = -2.5 V. Since the voltage gain of E2 equals one, -2.5 V becomes the normal offset voltage. This voltage compensates for an offset in the X ANALOG holding voltage, and establishes the (0,0) coordinates of the screen at its lower left corner. Pin AT2 a low adds -5 V to the output of E2, and offsets the beam to the other side of the screen, allowing the right hand margin column to be utilized.

The Y axis summer operates similarly. It's offset input however, is a constant -2.5 V, which keeps the (0,0) coordinates at the lower left corner of the screen.

E3 and E7 convert the summer output voltages, to a current capable of driving the display monitor. Diodes D1, D2, D4 through D6 and D7 through D12 are clamping circuits that prevent overdriving of the deflection amplifiers in the VT04/VT07. Diodes D4 through D6 and D10 through D12 prevent the A238 outputs from going more negative than -2.4 V. D7, D8, and D9 prevent the Y output (pin BV2) from exceeding +2.4 V. D1 and zener D2 prevent the X output (pin AV2) from exceeding +3 V under the more dynamic conditions encountered in the X-axis.

CHAPTER 6
MAINTENANCE

VT15 maintenance theory is directed to the module replacement level. The maintenance effort is divided into two basic categories: preventive maintenance and corrective maintenance.

Preventive maintenance consists of routine, periodic checks such as visual inspections, standard maintenance procedures which involve cleaning and lubricating, and diagnostic tests to expose possible weakening conditions to allow corrective action to be taken to eliminate possible failures before they occur.

Corrective maintenance is effected when a malfunction occurs, to isolate the fault or problem and to make necessary adjustments and/or replacements. This involves the use of diagnostic routines prepared on paper tape and designed to test the functional units of the system. The procedures and techniques or periodic checking aid in fault isolation. Power requirements can be checked through the checkout procedures for power requirements contained in Paragraphs 2.4 and 6.3.2.

6.1 EQUIPMENT REQUIRED

Maintenance procedures for the VT15 Graphic Processor require the standard equipment (or equivalent), standard hand tools, cleaning materials, test cables, and test probes listed in Table 6-1. Recommended special equipment and materials are also listed.

6.2 DIAGNOSTIC PROGRAMMING

The diagnostic routines are used to test the various system functional units and are supplied as paper tapes. A complete description, with instructions, is provided with each tape. A complete list of required VT15 diagnostic routines appears in the Foreword of this manual. Other test routines are available for optional equipment. The VT15 diagnostic routines are described below, in recommended execution sequence.

Table 6-1
Equipment Required

Equipment	Manufacturer	Designation
Multimeter†	Triplett or Simpson	Model 630-NA or 620
Oscilloscope†	Tektronix	Type 453
Digital Voltmeter	Fluke	8300A
X10 Probe†	Tektronix	P6008
Recessed tip, 0.065 in. for wire-wrap terminals†	Tektronix	206-052
Current Probe Amplifier	Tektronix	Type 131
Hand Unwrapping Tool	Gardner-Denver	500130
Hand-operated Wire-Wrap Tool with 26263 bit for 24 AWG Wire and 18840 sleeve	Gardner-Denver	14H1C
Module Extender†	DEC	Type W982
Diagnostic Self-Test Routines††	DEC	Instruction Test (Part I)
		Instruction Test (Part II)
		Visual Test
		Little Pictures Test

† Indicates standard equipment.
†† For further information on Diagnostics, refer to Paragraph 6.2.

1. Display Instruction Test (MainDEC-15-DAVTB) Part I - Tests the parameter 1, parameter 2, and parameter 3 display file instructions, the JMP and JMS display file instructions, all operate IOT commands, all read IOT commands except RXP and RYP, and all skip IOT commands except SPPB and SSLP. This program also includes API facility and extended memory tests.

2. Display Instruction Test (MainDEC-15-DAVTA) Part II - Tests those functions that require manual intervention by the operator. Functions requiring manual intervention are the pushbuttons (PB00 through PB05), the light pen, and the keyboard.

3. Display Visual Test (MainDEC-15-D6DD) - Tests the point plot, graph plot, basic vector, and basic short vector display file instructions. It also tests read IOT commands, RXP and RYP.

4. Little Pictures Test (MainDEC-15-D6EC) - This program or test contains a series of test patterns that are primarily used as aids for alignment and/or adjustment of the VT15 Graphic Processor.

6.3 PREVENTIVE MAINTENANCE

Preventive maintenance consists of tasks performed periodically; its major purpose is to prevent failures caused by minor damage or progressive deterioration due to aging. A preventive maintenance log book should be established and necessary entries made according to a regular schedule. This data, compiled over an extended period of time, can be very useful in anticipating possible component failures resulting in module replacement on a projected module or component reliability basis.

Preventive maintenance tasks consist of mechanical and electrical checks. All maintenance schedules should be established according to conditions at the particular installation site that are dependent on environmental conditions, etc. Mechanical checks should be performed as often as required to allow the fans and air filters to function efficiently. All other preventive maintenance tasks should be performed on a regular schedule determined by reliability requirements. A recommended schedule is every 600 operating hours or every four months, whichever occurs first.

6.3.1 Mechanical Checks

Step	Procedure
1	Clean the exterior and interior of equipment cabinets with a vacuum cleaner or clean cloth moistened in nonflammable, noncorrosive solvent.
2	Remove and clean the air filters in each added section. The rack fans are equipped with a 1/4 in. mesh which should be vacuumed. The floor fans should be removed and the aluminum mesh filters washed in mild detergent.
3	Lubricate door hinges and casters with a light machine oil. Wipe off excess oil.
4	Inspect all wiring and cables for cuts, breaks, fraying, deterioration, kinks, strain, and mechanical security. Tape, solder, or replace any defective wiring or cable covering.
5	Inspect the following for mechanical security: lamp assemblies, jacks, connectors, power supplies, fans, capacitors, etc. Tighten or replace as required.
6	Inspect all module mounting panels to ensure that each module is securely seated in its connector.
7	Inspect power supply capacitors for leaks, bulges, or discoloration, and replace as required.

6.3.2 Electrical Checks

Perform the power supply checks listed in Table 6-2. Using a multimeter, check the output voltage values under normal load conditions. Using an oscilloscope, measure the peak-to-peak ripple content

on all dc outputs. The Type 716 power supply (6.5 Vdc) is not adjustable; therefore, if the output voltage is not within specifications, the power supply is considered defective and should be replaced.

Table 6-2
Power Supply Output Checks

Measurement Terminals at Power Supply Output	Nominal Output (Vdc)	Acceptable Output Range (V)	Maximum Output Current (A)	Maximum Peak-to-Peak Output Ripple (V)
Type 716 (Indicator Supply) White (+) to Black (-)	+6.5			
Type H707B (Precision Analog Supply) Red (+) to Black (-)	+15.0	+14.9 to +15.1	1.5	1 mV RMS Max.
Blue (-) to Black (+)	-15.0	-14.9 to -15.1	1.5	1 mV RMS Max.
Type H721 (Logic Supply) Green (+) to Black (-)	+5.1	5.0 to 5.2	20.0	20 mV RMS Max.

6.4 SYSTEM LOGIC CHECKS AND ADJUSTMENTS

The following system checks and adjustment procedures are provided for reference during system check-out, maintenance, and troubleshooting. Each procedure contains the reference drawing number of the drawing on which the particular module, test point, and adjustment are located, and defines the adjustment nominal setting.

6.4.1 H721 Logic Power Supply Adjustment

The H721 +5V Power Supply is located in the bottom of the VT15 and provides the required power for the logic modules.

Drawing Number:	H721-0-0
Equipment Required:	DVM
Test Points:	A05A2, C02A2, E02A2, H03A2
Adjustment Location:	Top, left-hand side of H721 Power Supply
Nominal Setting:	+5.1 ± 0.1V
Procedure:	Using the DVM, adjust the power supply for a 5.1 ± 0.1V reading

6.4.2 M401 System Basic Clock Adjustment

The M401 Basic Clock provides the basic timing for the VT15 Graphic Processor. All system timing is derived from the basic clock.

Drawing Number:	VT15-0-7
Equipment Required:	Wideband oscilloscope
Test Point:	M207 D15 D2
Adjustment Location:	On the back of M401 Module in slot D15.
Nominal Setting:	250 ns between pulses.
Procedure:	With the VT15 and computer stopped, sync on oscilloscope channel 1 and adjust for 250 ns between pulses.

6.4.3 Data Flag Delay

Loading delay characteristics are shown in Figure 6-1.
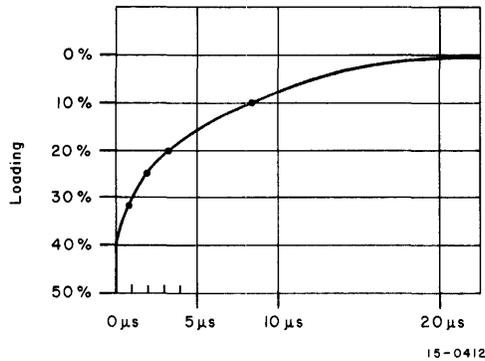
Figure 6-1   I/O Loading Delay Characteristics

Drawing Number:	VT15-0-07
Equipment Required:	Wideband oscilloscope
Test Point:	M302 C16 T2
Adjustment Location:	Bottom potentiometer in slot C16 on the back of the M302 Module.
Nominal Setting:	400 ns

Procedure: Run the first section of VT15 Instruction Test, Part 2 (Blink Square) and adjust for 400 ns (minimum) setting.

Sync (+) on channel 1 and adjust the duration between the positive leading edge and the trailing edge as required.

NOTE

Earlier versions of the VT15 Instruction Test, Part 1 will not run with the specified delay set below 3.5 μs. To run earlier versions of the test, change memory location 003211 to 140000.

6.4.4 Display Console Bus Delay

This procedure allows adjustment of the time delay (used to adjust the duration of MS02 and MS03) to compensate for signal latency in the VT15 to display console data and control cable.

Drawing Number:	VT15-0-07 and -12
Equipment Required:	Wideband oscilloscope
Test Point:	M302 F13 F2
Adjustment Location:	The upper potentiometer in slot F13 on the M302 Module.
Nominal Setting:	750 ns per 30 ft of data and control cable.
Procedure:	While running Routine 11_8 of Little Pictures, sync (+) on channel 1 and adjust the pulse duration, referencing between the positive leading edge and the trailing edge of the pulse.

6.4.5 Move Settle Delay

This procedure allows adjustment of settling delay time for vectors of 17 units or greater in sector zero. This adjustment procedure is also used to adjust CR and TAB.

Drawing Number:	VT15-0-11
Equipment Required:	Wideband oscilloscope
Test Point:	M302 C16 F2
Adjustment Location:	The upper potentiometer in slot C16 of the M302 Module.
Nominal Setting:	2 μs (Basic System) 3.5 μs (With VV15 Option installed)
Procedure:	Run the first section of VT15 Instruction Test, Part 2. Sync (+) on channel 1 and adjust pulse duration between the positive leading edge and the trailing edge to 3.5 μs.

6.4.6 Blink Delay

This procedure allows adjustment of the blink rate (blink timing).

Drawing Number:	VT15-0-12
Equipment Required:	Wideband oscilloscope
Test Point:	M302 F13 T2
Adjustment Location:	The lower potentiometer in slot F13 of the M302 Module.
Nominal Setting:	100 ms
Procedure:	With the PDP-15 and VT15 stopped, sync (+) on channel 1 and adjust the positive output duration time as required.

6.4.7 Long Point Settle Delay

This procedure allows adjustment of the settling time (of approximately 20 µs) used during point moves greater than 200_8, for sector reentry, and for CR and TAB.

Drawing Number:	VT15-0-36
Equipment Required:	Wideband oscilloscope
Test Point:	M302 J12 T2
Adjustment Location:	Lower potentiometer on Module M302 in slot J12.
Nominal Setting:	20 µs
Procedure:	Run the first section of Instruction Test, Part 2 (Blink Square), sync (+) on channel 1 and adjust the duration between the positive leading edge and the trailing edge of the pulse for a 20 µs setting.

6.4.8 Short Point Settle Delay

This procedure allows adjustment of the settling time (of approximately 8 µs) used during point moves of less than 177_8.

Drawing Number:	VT15-0-36
Equipment Required:	Wideband oscilloscope
Test Point:	M302 J12 F2
Adjustment Location:	The upper potentiometer in slot J12 of the M302 Module.

Nominal Setting:	8 μs
Procedure:	While running the first section of VT15 Instruction Test, Part 2, sync (+) on channel 1 and adjust the duration between the positive leading edge and the trailing edge of the pulse for an 8 μs setting.

6.5 ANALOG ADJUSTMENTS

These procedures may be used in part or in total, according to whether only a single module, or the overall analog functional group is to be checked. The adjustments are normally used for initial setup only, and require the use of a calibrated oscilloscope.

NOTE

The precision voltages required in the analog section are preset at the factory. Adjustment of these voltages should not be necessary, except on replacement of the power supply. The VT15 should normally operate even with these voltages out of tolerance. Any adjustment of the power supply will require complete readjustment of the system.

6.5.1 Analog Voltage Adjustments

The following procedures are provided to allow checking of the operating voltages used in the functional analog section.

6.5.1.1 H707 Precision Analog Power Supply Adjustment – Normally, this adjustment is preset at the factory and is not required; however, it should be checked during system installation and periodically during preventive maintenance checks.

Drawing Number:	C-UA-H707-0-0
Equipment Required:	Wideband oscilloscope
Test Point:	B32V2
Adjustment:	Left-hand potentiometer on the H707B power supply
Nominal Setting:	+15 V ±2.5 mV
Procedure:	Using the oscilloscope check for the required reading. Adjust as required.
Test Point:	B32U2
Adjustment:	Right-hand potentiometer on the H707B power supply
Nominal Setting:	–15 V ±2.5 mV
Procedure:	Using the oscilloscope check for the required reading. Adjust as required.

6.5.1.2 D DAC Reference Voltage Adjustment – This procedure allows adjustment of the reference voltage required for the VT15 D DAC.

Drawing Number:	A618YA-0-1
Equipment Required:	Wideband oscilloscope
Test Point:	A704 A32V2
Adjustment Location:	Potentiometer on the back of the A704 Module located in slot AB32.
Nominal Setting:	-10 V ± 2.5 mV
Procedure:	Using the oscilloscope check for the required reading. Adjust for -10 V.

6.5.2 Analog Adjustments

Adjustment procedures for the VT15 Analog Function Group are described in Drawing A-SP-VT15-0-51 of the Engineering Drawings, in Volume 2.

6.6 CORRECTIVE MAINTENANCE

If a malfunction occurs, the condition must be analyzed, isolated, and corrected as delineated in the following procedures. No test equipment or special tools are required for corrective maintenance other than a broadband oscilloscope and a standard multimeter. However, a clip-on current probe such as the Tektronix Type P6008 with a Type 206-052 recessed tip and a Fluke Type 8300A digital voltmeter, or equivalent, are very helpful for monitoring purposes. The best corrective maintenance tool is a thorough understanding of the physical and electrical characteristics of the equipment. Persons responsible for maintenance should be thoroughly familiar with the system concept, IOT command and instruction flow diagrams, engineering logic drawings, operation of the special module circuits, and the location of mechanical and electrical components. A thorough knowledge of cross-referencing techniques will enable maintenance personnel to readily interpret diagnostic routine printouts to facilitate the isolation of malfunctions.

Diagnosis and remedial action for a fault condition usually proceed in the following sequence:

Step	Procedure
1	Preliminary investigation: gather all information to determine the physical and electrical security of the computer.
2	System troubleshooting: define the errors by locating the fault to within a module, through use of diagnostic routines, control panel troubleshooting or signal tracing, and flow diagrams.
3	Replace the defective module or modules to return the system to full operation.
4	Log entry to record pertinent data.

When the system is again in operation, defective parts within a module can be located and repaired or replaced. Repaired modules should be verified by a validation test after repair.

Before commencing troubleshooting procedures record all unusual functions and all observable symptoms of the machine that occurred prior to the fault. In addition, note the program in progress, the condition of operator console indicators, etc. This information should be referenced to the maintenance log to determine whether this type of fault has occurred before or if there is any history of this fault to ascertain how the condition was previously corrected.

If the entire machine fails, first perform a visual inspection to determine the physical and electrical security of all power sources, cables, connectors, etc. Ensure that all power supplies are working properly and that there are no short circuits by performing the power supply checks as described under Paragraph 6.3, of preventive maintenance. Also, check the condition of the fans and air filters in the fan housing. If the fans cease to function or the air filters become clogged, the temperature within the cabinet could attain a level that would cause marginal semiconductors to become defective.

When performing the troubleshooting procedures, the recommended procedure is as follows:

Step	Procedure
1	Run the appropriate diagnostic program test for the specific fault utilizing control panel troubleshooting and/or signal tracing techniques.
2	When troubleshooting, whether through the use of diagnostic routines, control panel troubleshooting or signal tracing, the system flow diagrams (Chapter 4) are especially useful for referencing between diagnostic programs, indicator panel indications, and the engineering logic drawings.

6.6.1 Module Handling

CAUTION

Turn off all power before extracting or inserting modules.
Use a straight, even pull when extracting modules to prevent twisting of the printed-wiring board.

To gain access to adjustment controls or testing points on the module, remove the module and insert a Type W980 Module Extender into the vacated module connector in the mounting panel. Insert the module into the module extender. When access to double-width modules is desired, a W982 Module Extender is used.

6.6.2 System Troubleshooting

Begin troubleshooting procedures by repeating the operation in which the malfunction was initially observed, using the same program. Thoroughly check the program for proper control settings. While referencing the appropriate flow diagram(s), located in Chapter 4, analyze the portion of the program being performed and the general condition of the indicators. By performing these basic troubleshooting steps, the fault can normally be readily isolated.

If at this point the instructions do not seem to be functioning properly, perform the Display Instruction Test, Part I, MAINDEC-15-DAVTB and the Display Visual Test, MAINDEC-15-D6DD. A brief description of the IOT commands, display file instructions, and functions and parameters tested by the various diagnostic programs is provided in Paragraph 6.2. If the program interrupt (PI) and/or automatic program interrupt facilities do not appear to be functioning properly, the Display Instruction Test, Part I should be performed.

6.6.3 Functional Group Troubleshooting

When the fault is definitely isolated to the VT15 Graphic Processor but cannot be immediately localized to a specific logic function, an effort should be made to further isolate the fault to one of the five major functional groups through functional group level analysis using the system drawings provided in Figures 1-2, 1-3, and 3-1 and the functional group descriptions contained in Chapter 3.

When the fault has been isolated to a functional group, continue troubleshooting to locate the defective module or component by means of signal tracing, using the flow diagrams provided in Chapter 4 and the appropriate engineering logic drawings provided in Volume 2.

6.6.4 Module Troubleshooting

Once the fault has been isolated to a specific module, turn computer power off and carefully remove the suspected module. Inspect the receptacle for wear or damaged contacts. When the operability of the module is verified, replace the faulty module with a module known to be good and rerun the last diagnostic program. If the system performs properly, return the system to an operating status and log an entry to record all pertinent data concerning the fault or malfunction. When the individual defective part(s) within a module is located and repaired or replaced, the module should be verified by a validation test.

6.6.5 VT15 Graphic Processor Engineering Drawings

Volume 2 of the VT15 Graphic Processor Maintenance Manual contains the engineering drawings and special module circuit schematics that are referenced in Volume 1.

DRAWING CODES

Digital Equipment Corporation engineering drawings are coded to designate drawing type, major assembly, and series. A drawing number such as D-BS-RF15-0-01 contains the following information:

D	Size (original)
BS	Type (block schematic)
RF15	Equipment designation
0	Manufacturing variation
01	The first drawing of a series

The drawing type codes are defined as follows:

AD	Assembly drawing
BS	Block schematic
CS	Circuit schematic
DD	Drawing directory
IA	Inseparable Assembly
IC	Interconnection cabling
ML	Master Drawing List
MU	Module utilization drawing
PL	Parts list
UA	Unit assembly

DRAWING NUMBER INDEX

Table 6-3 is an index to the engineering drawings contained in Volume 2.

Table 6-3
Drawing Number Index

Size (Original)	Type	Number	Title
B	DD	VT15-0	VT15 Graphic Display
D	UA	VT15-A-0	VT15 Unit Assembly
A	PL	VT15-A-0	VT15 Unit Assembly (PL)
D	IC	VT15-A-2	Cable Configuration
D	UA	VT15-B-0	VT15-B Graphic Display
A	PL	VT15-B-0	VT15-B Graphic Display (PL)
D	AD	7006551-0-0	Wired Assembly VT15
A	PL	7006551-0-0	Wired Assembly VT15 (PL)
D	IA	706691-0-0	±15V Power Cable
E	IA	706692-0-0	DC Power Cable
E	IA	7007120-0-0	DC Power Cable
B	CS	841-B-1	Power Control 841
D	BS	VT15-0-01	Input Buffer
D	BS	VT15-0-02	Data Buffer
D	BS	VT15-0-03	Parameter 1
D	BS	VT15-0-04	Parameter 2
D	BS	VT15-0-05	Parameter 3
D	BS	VT15-0-06	Instruction Decoder
D	BS	VT15-0-07	Main Timing
D	BS	VT15-0-08	Control Timing 1
D	BS	VT15-0-09	Control Timing 2
D	BS	VT15-0-10	Address Lines
D	BS	VT15-0-11	Graphplot Pt Vector Increment
D	BS	VT15-0-12	Intensity and Light Pen
D	BS	VT15-0-13	D Register
D	BS	VT15-0-14	PC, X and Y Register 1
D	BS	VT15-0-15	PC, X and Y Register 2
D	BS	VT15-0-16	PC, X and Y Register 3
D	BS	VT15-0-17	Misc Control
D	BS	VT15-0-18	Bus Receivers
D	BS	VT15-0-19	Adder Gating 6 + 7
D	BS	VT15-0-20	Adder Gating 8 + 9
D	BS	VT15-0-21	Adder Gating 10 + 11

Table 6-3 (Cont)
Drawing Number Index

Size (Original)	Type	Number	Title
D	BS	VT15-0-23	Adder Gating 14 + 15
D	BS	VT15-0-24	Adder Gating 16 + 17
D	BS	VT15-0-25	Direction + Rotate 1
D	BS	VT15-0-26	Direction + Rotate 2
D	BS	VT15-0-27	Skip 1 and Data and Control Bus
D	BS	VT15-0-28	Skip 2
D	BS	VT15-0-29	Skip Request and Increment Count Reg
D	BS	VT15-0-30	DAC
D	BS	VT15-0-31	IOT Decoder
D	BS	VT15-0-32	I/O Bus 0-5
D	BS	VT15-0-33	I/O Bus 6-11
D	BS	VT15-0-34	I/O Bus 12-17
D	IC	VT15-0-35	Cables
D	BS	VT15-0-36	PC1, 2, 3, 4, 5 and Point
D	BS	VT15-0-37	Data Channel and API Multiplex
D	IC	VT15-0-38	Light Cables
D	BS	VT15-0-39	Character Generator Input Mixer
D	BS	VT15-0-40	Character Generator Control
D	BS	VT15-0-41	Character Generator Read-Only-Memory
D	BS	VT15-0-42	Adr and Char Gen Control
D	BS	VT15-0-43	Int and Status
D	BS	VT15-0-44	Basic Vector Generator
D	MU	VT15-0-45	Module Utilization
A	PL	VT15-0-45	Module Utilization (PL)
A	SP	VT15-0-51	Adjustment Procedure
D	CS	H721-0-1	H721 Power Supply
C	CS	716-0-1	Indicator Power Supply
D	CS	A618YA	D/A Converter
B	CS	A622-0-1	10 Bit Single Buffered DAC 0-5 Volt
C	CS	M761-0-1	32 to 8 Bit Multiplexer
C	CS	M762-0-1	ROM Diode Matrix Receivers
C	CS	G618-0-1	ROM Diode Matrix Decoder
C	CS	A140-0-1	Dual Analog Switch

Table 6-3 (Cont)
Drawing Number Index

Size (Original)	Type	Number	Title
B	DD	VV15-0	Arbitrary Vectoring
A	PL	VV15-0-0	Arbitrary Vectoring
A	SP	VV15-0-1	Engineering Specifications
A	AL	VV15-0-2	Accessory List
D	CS	A238-0-1	Analog Summer Driver
D	CS	A3180-0-1	Basic Vector Generator
B	CS	M622-0-1	Bus Driver
D	CS	A3170-0-1	Abr. Vec. Gen.
E	CS	M7010-0-1	VV15 Control
D	AD	7009597-0-0	Push Button Assy
D	CS	5410685-0-1	Push Button Board

APPENDIX A
ASCII CHARACTER GENERATION AND DECODING

The following example is a pictorial listing depicting the method(s) used to generate the IOPS ASCII Characters on the display console CRT. Three-digit octal codes are also provided for each character with the initial character determining whether the particular vector is intensified (1), or unintensified (0) or (2). The second digit determines vector direction and can be any octal number between 0 and 7. The third or right-hand digit indicates vector length or magnitude and can also be any number between 0 and 7. For an example of the eight vector directions refer to Figure 4-6.

100	101	102
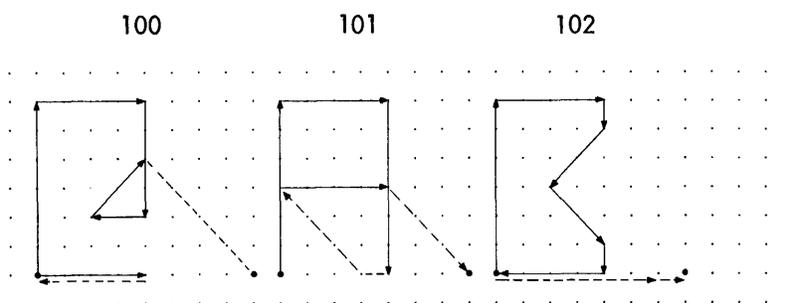
15-0356

@	A	B
104	126	126
044	104	104
126	166	161
104	041	152
164	033	172
142	104	161
112	273	144
274		207

103	104	105
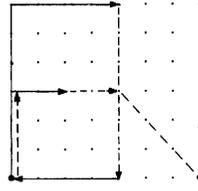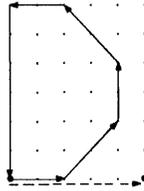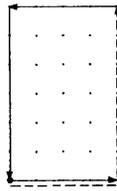
15-0354

<u>C</u>	<u>D</u>	<u>E</u>
104	102	126
026	112	104
144	122	066
166	132	144
207	142	023
	166	102
	207	002
		273

106	107	110

15-0355

<u>F</u>	<u>G</u>	<u>H</u>
126	012	126
104	102	004
053	162	166
041	144	033
102	126	041
002	104	104
273	063	273
	273	
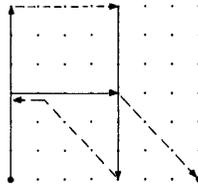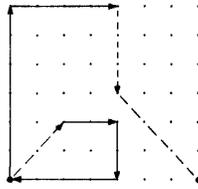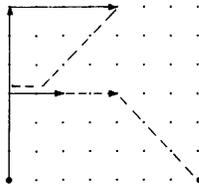
111   112   113
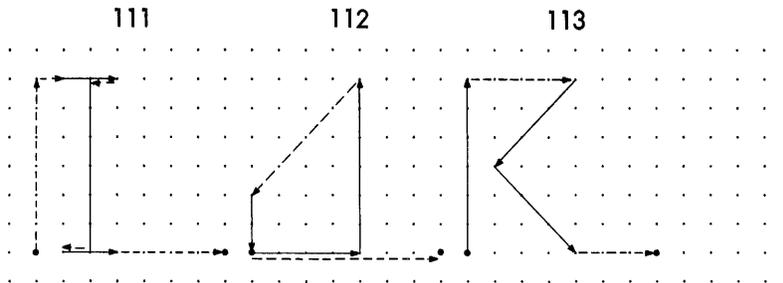
15-0341

I	J	K
026	104	126
001	126	004
102	054	153
041	162	173
166	207	203
041		
102		
204		

114   115   116
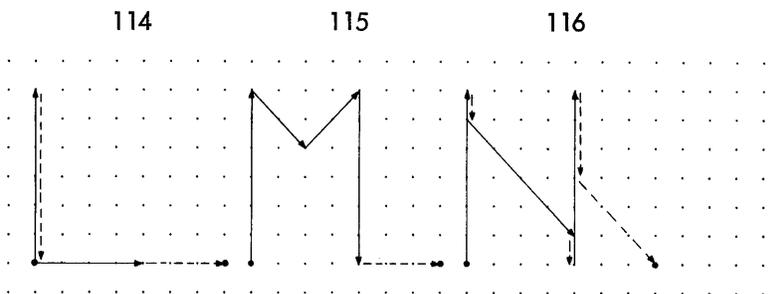
15-0342

L	M	N
126	126	126
066	172	061
104	112	174
203	166	061
	203	126
		063
		273

117 120 121
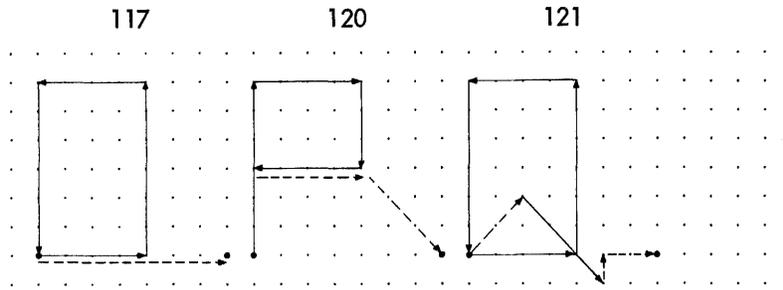
15-0357

O	P	Q
104	126	104
126	104	126
144	163	144
166	144	166
207	004	012
	273	173
		021
		202

122 123 124
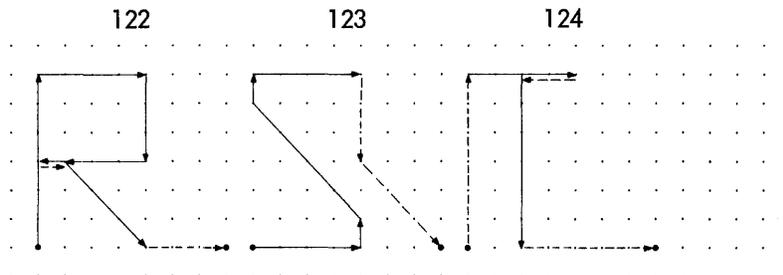
15-0358

R	S	T
126	104	026
104	121	104
163	134	042
144	121	166
001	104	205
173	063	
203	273	

125	126	127
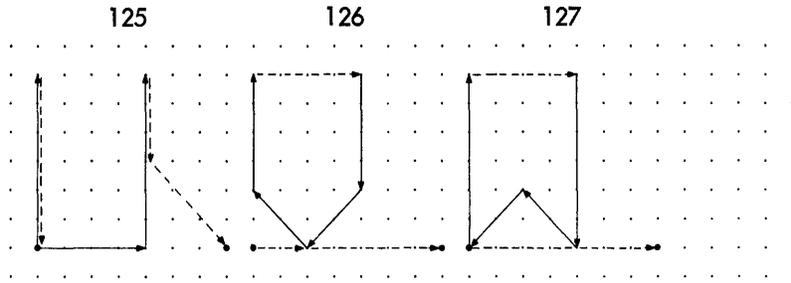
U	V	W
126	002	126
066	132	004
104	124	166
126	004	132
063	164	152
273	152	207
	205	

130	131	132
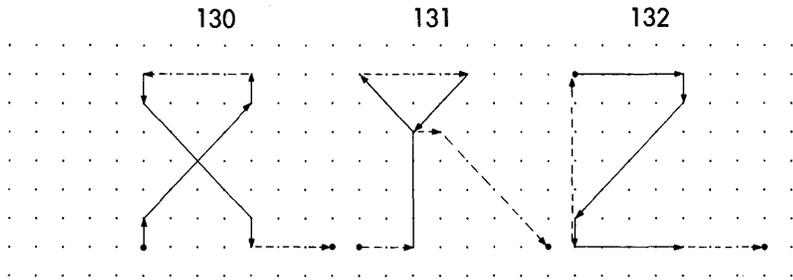
X	Y	Z
121	002	026
114	124	104
121	132	161
044	004	154
161	152	161
174	001	104
161	274	203
203		
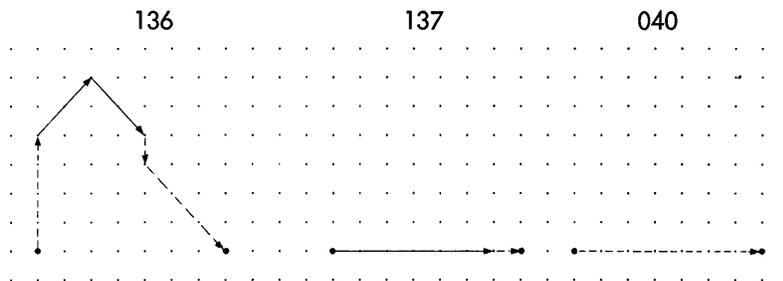
133 134 135

[
002
142
126
102
041
276

\
025
174
071
202

]
002
102
126
142
041
276

15-0345

136 137 040

Λ
024
112
172
061
273

UNDERSCORE
106
201

SPACE
207

15-0346

A-6

041	042	043

!	"	#
002	021	022
120	012	104
023	123	022
123	001	144
041	163	012
276	001	166
	273	205

044	045	046

$	%	&
104	021	121
123	114	113
144	043	132
122	141	151
103	074	175
031	141	145
166	061	207
205	204	

	047	050	051
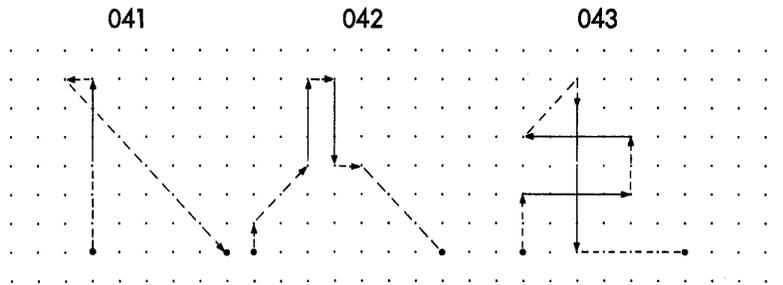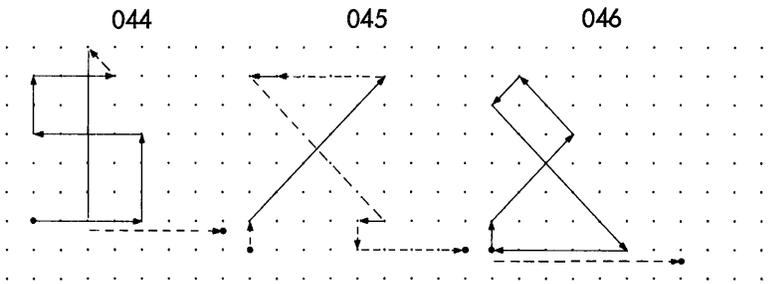
15-0349

	'	(	)
	021	002	002
	012	132	112
	111	122	122
	122	112	132
	001	041	041
	063	276	276
	273		

	052	053	054
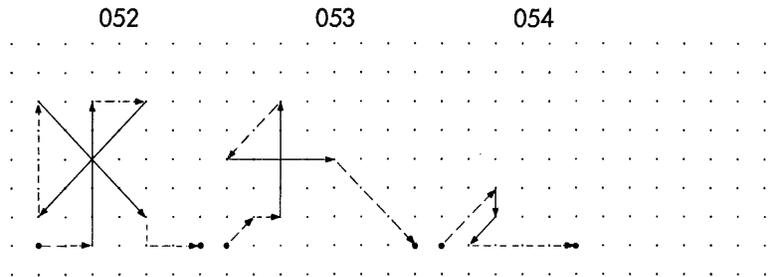
15-0350

	*	+	'
	002	011	012
	125	001	161
	002	124	151
	154	052	206
	024	104	
	174	273	
	061		
	203		
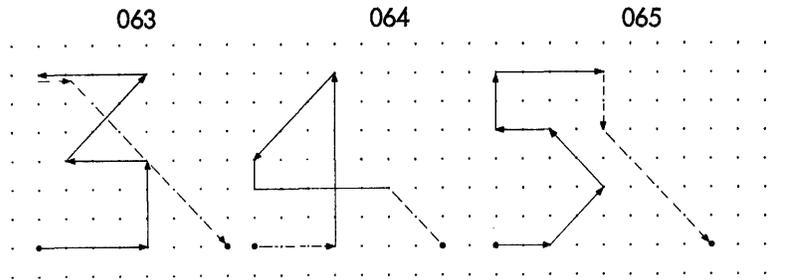
A-8

055

056

057

$-$	$\cdot$	$/$
023	004	021
104	100	114
273	203	062
		273

060

061

062

0	1	2
126	001	025
104	102	111
166	041	102
144	126	171
021	151	154
114	075	161
062	201	104
273		203

063 064 065

15-0347

3	4	5
104	003	102
123	126	112
143	153	132
113	161	142
144	105	122
001	272	104
276		063
		273

066 067 070
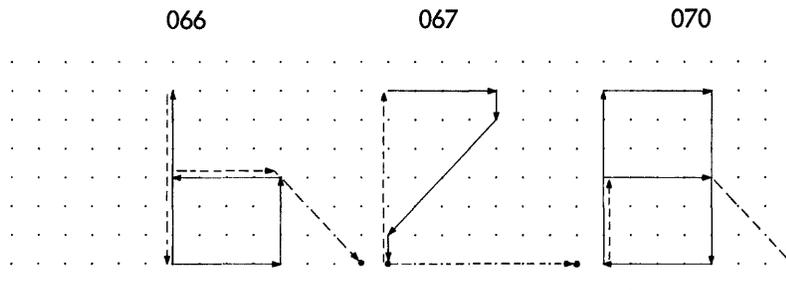
15-0348

6	7	8
126	026	126
066	104	104
104	161	163
123	154	144
144	161	063
004	207	104
273		123
		273

071	072	073

9	:	;
004	022	023
123	012	012
144	160	160
123	063	063
104	160	161
163	061	151
273	205	206

074	075	076

| <	=	>
021	022	021
003	104	001
132	022	112
112	144	132
001	003	003
062	274	062
273		273

077

15-0353

?
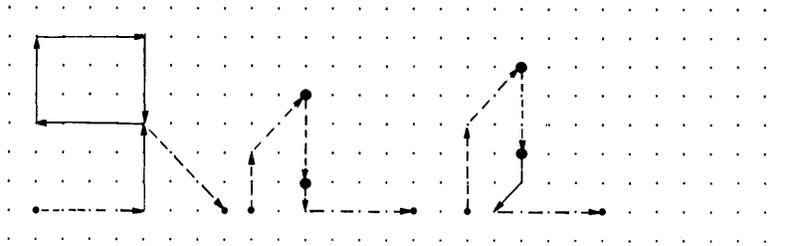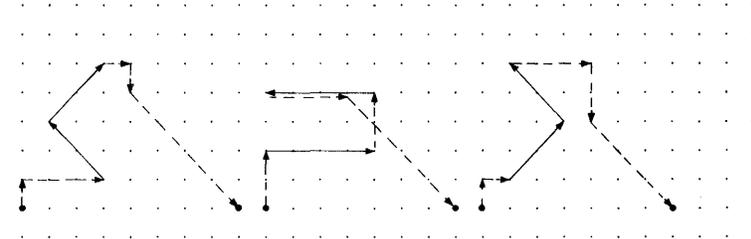
025
111
102
171
152
163
205

Reader's Comments

VT15 GRAPHIC PROCESSOR
MAINTENANCE MANUAL
EK-0VT15-MN-002

Your comments and suggestions will help us in our continuous effort to improve the quality and usefulness of our publications.

What is your general reaction to this manual? In your judgment is it complete, accurate, well organized, well written, etc.? Is it easy to use? _____

_____

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What features are most useful? _____

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What faults do you find with the manual? _____

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Does this manual satisfy the need you think it was intended to satisfy? _____

Does it satisfy *your* needs? _____ Why? _____

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