

MASTER

digital

PDP 12  
DETAILED FLOW  
DIAGRAMS



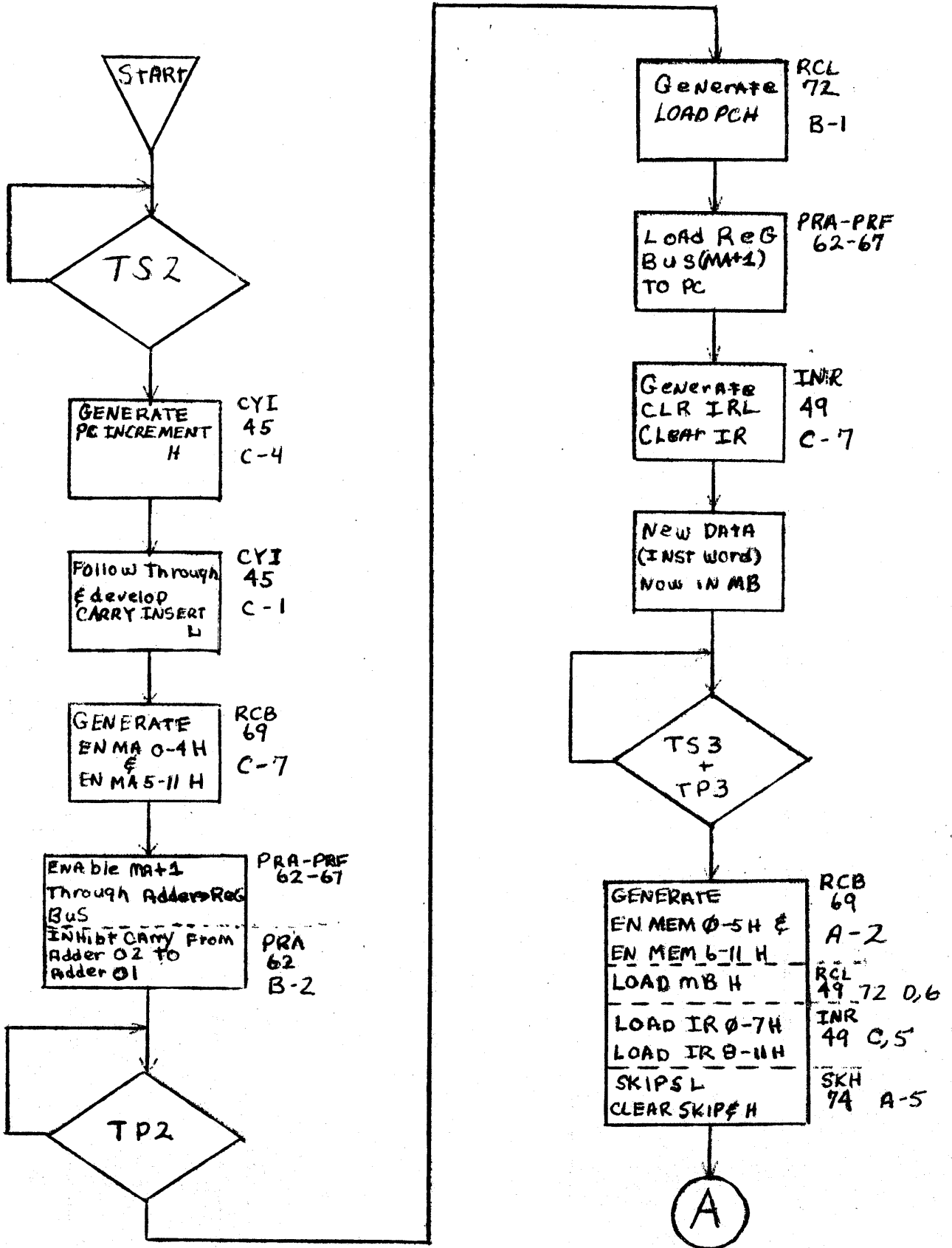
PDP 12  
DETAILED FLOW  
DIAGRAMS

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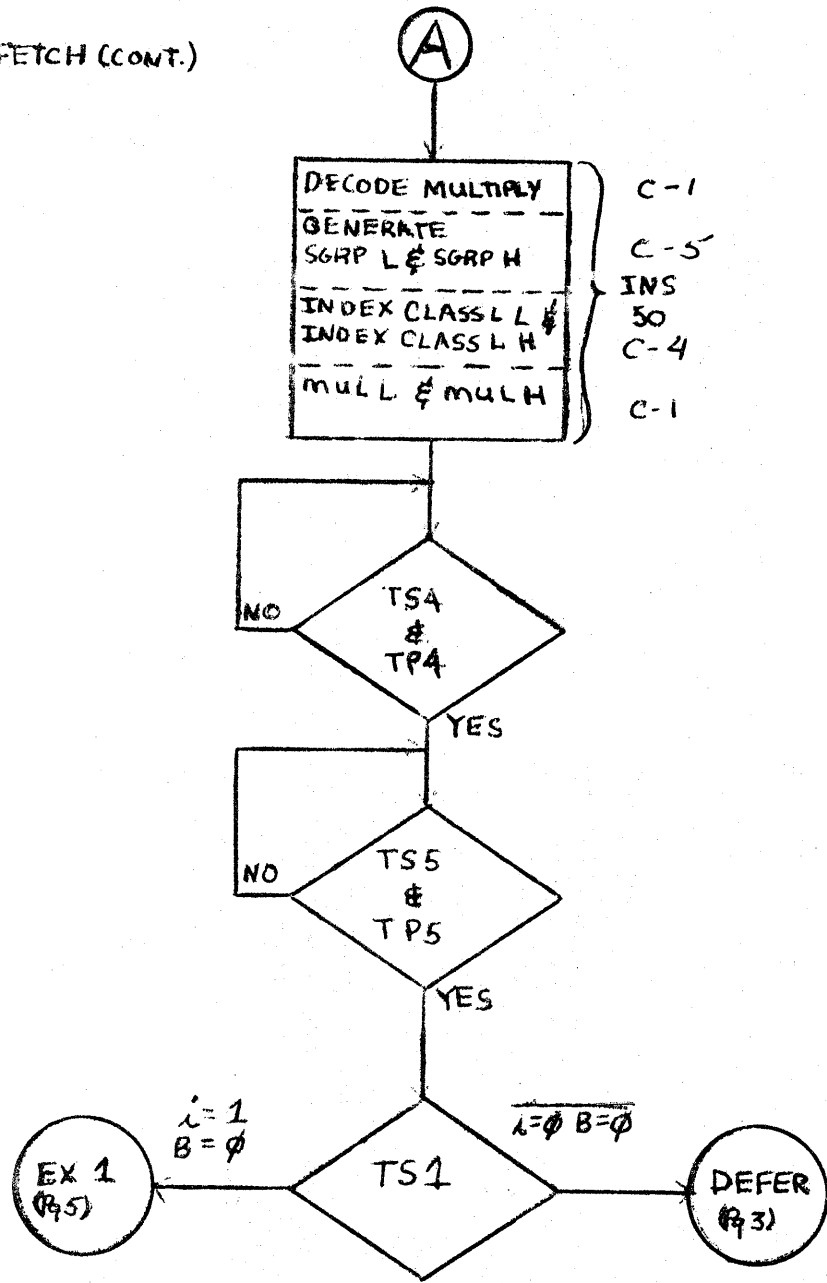
MULTIPLY (1240)  
DETAILED FLOW DIAGRAM

FETCH



# POP-12 MULTIPLY

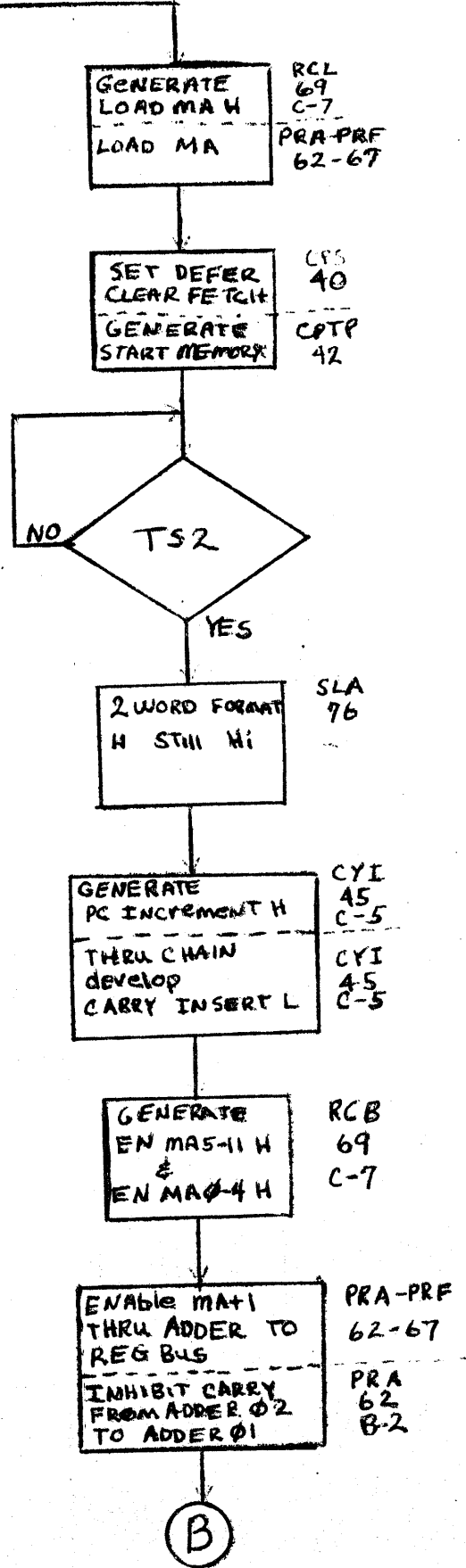
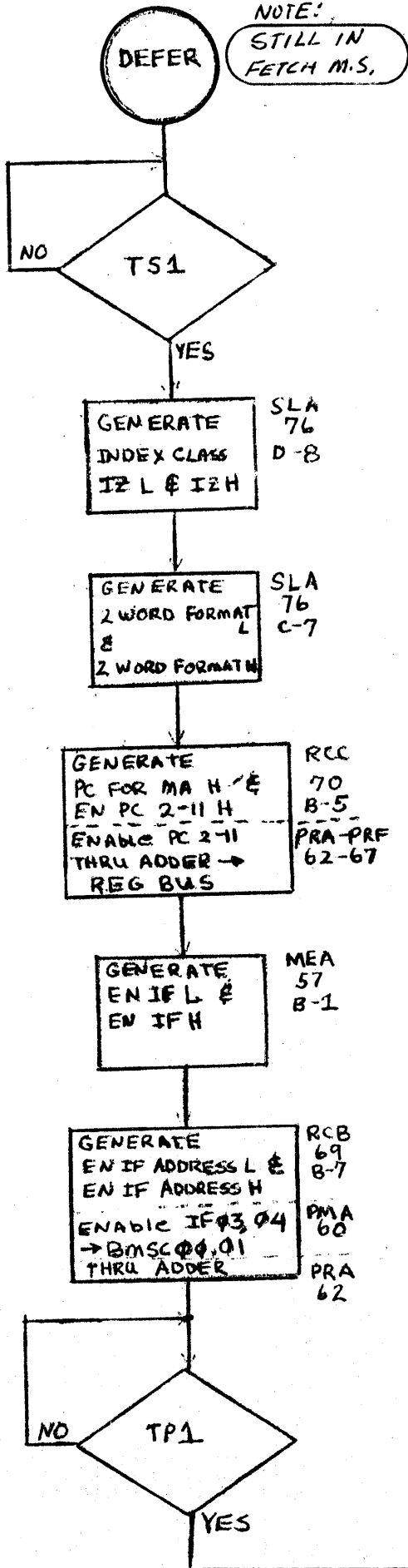
FETCH (CONT.)

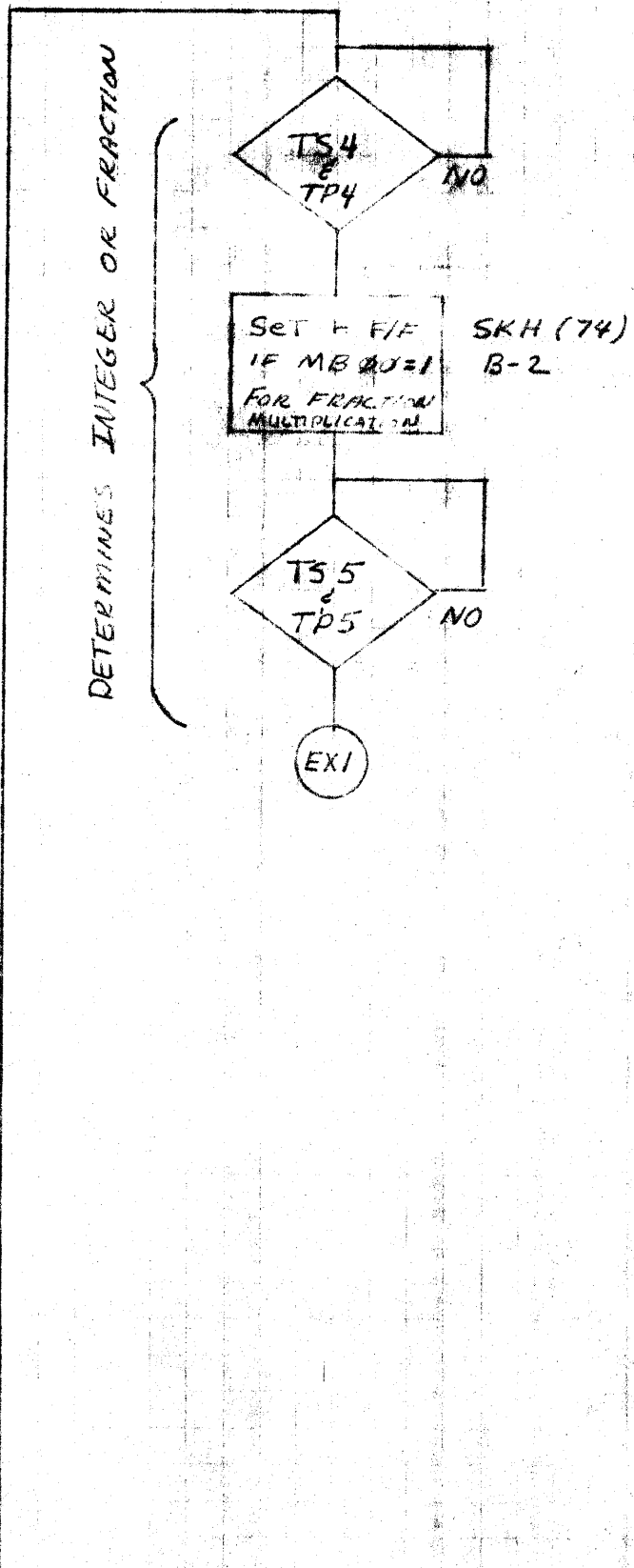
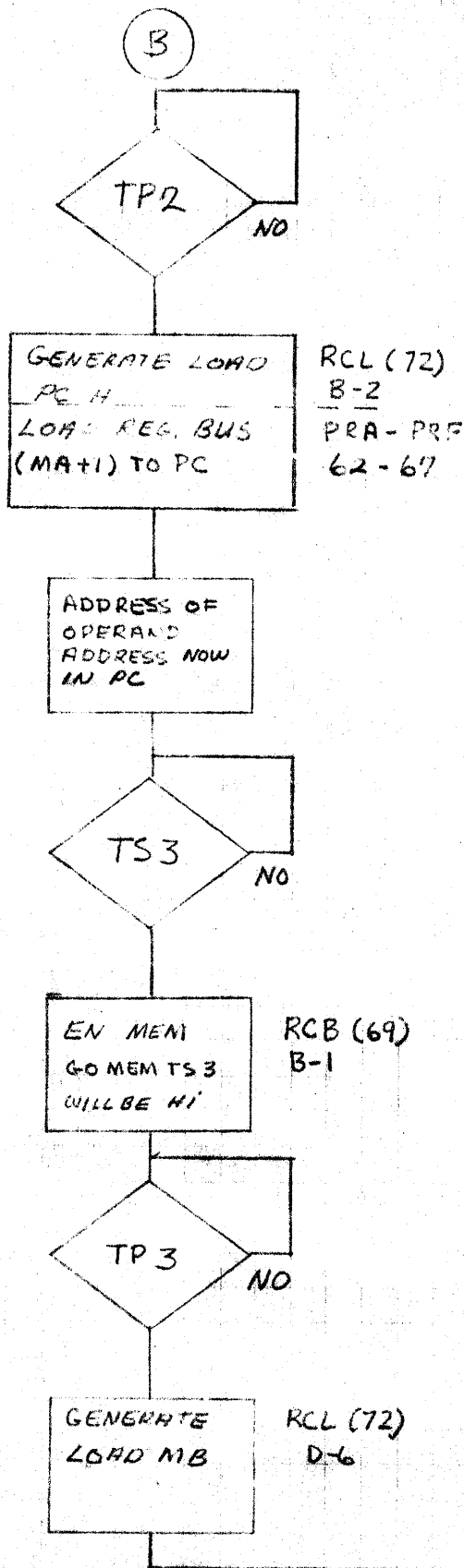


# PDP-12 MULTIPLY

L=φ B=φ

NOTE:  
STILL IN  
FETCH M.S.

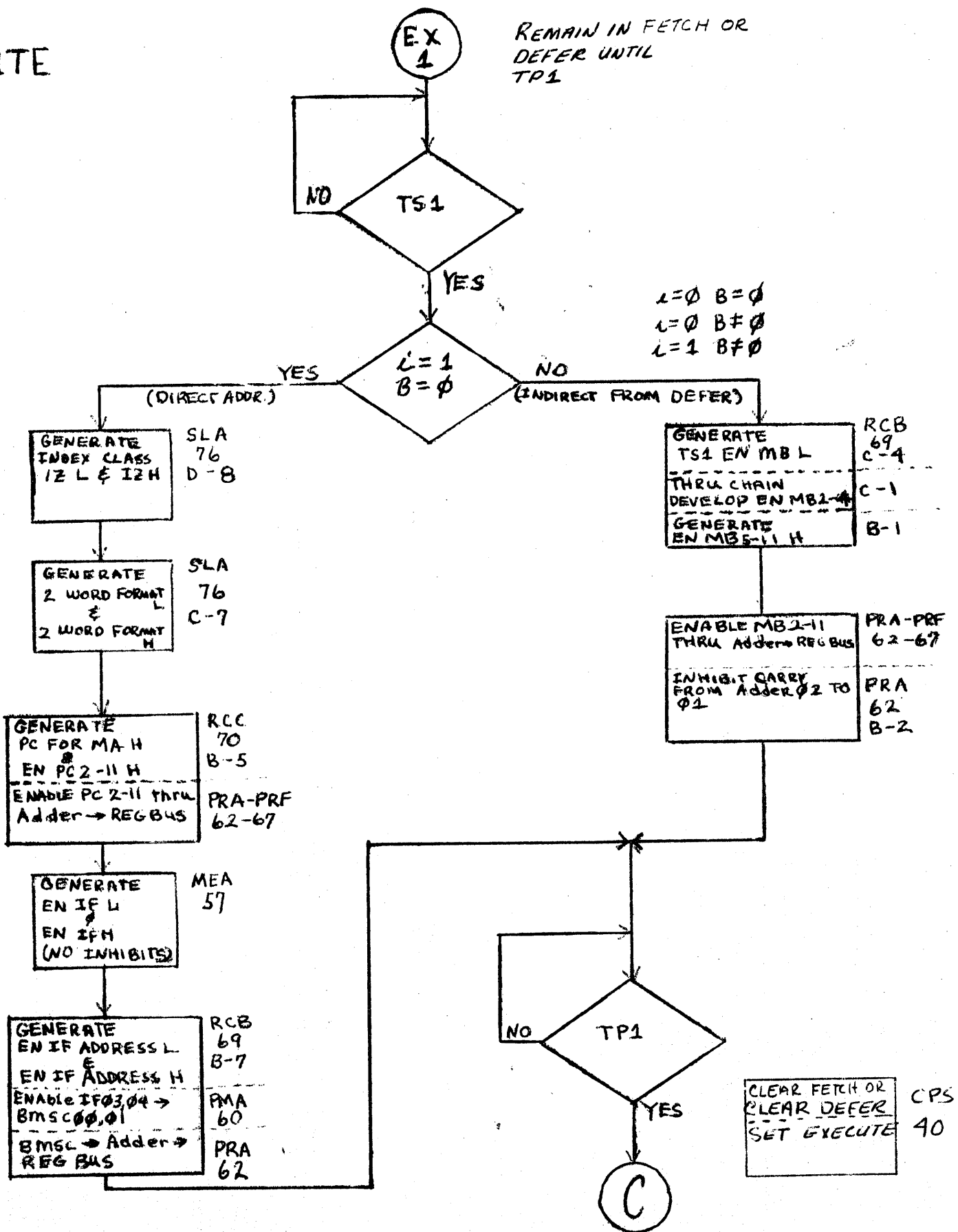




# PDP-12 MULTIPLY

EXECUTE

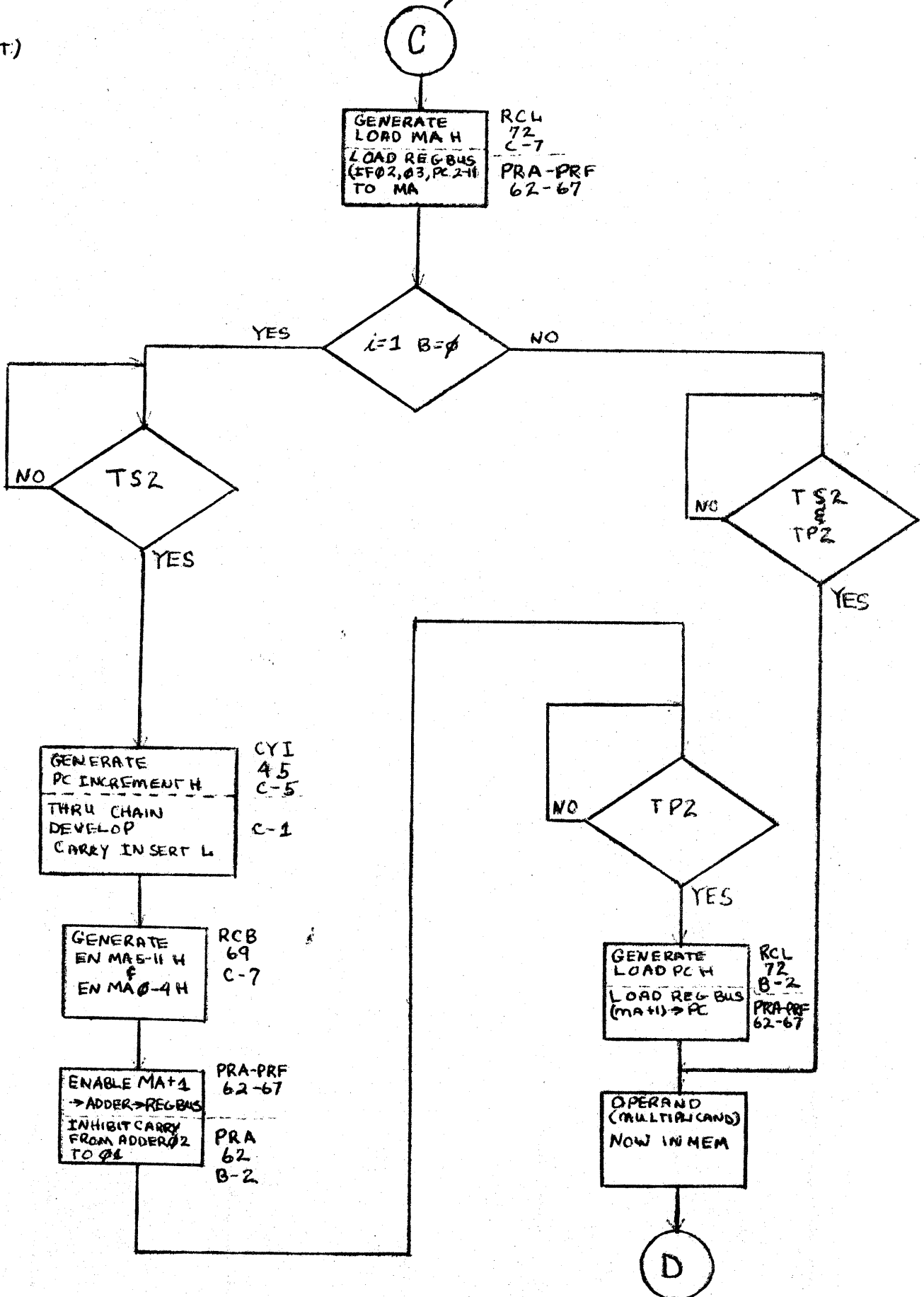
REMAIN IN FETCH OR  
DEFER UNTIL  
TP1



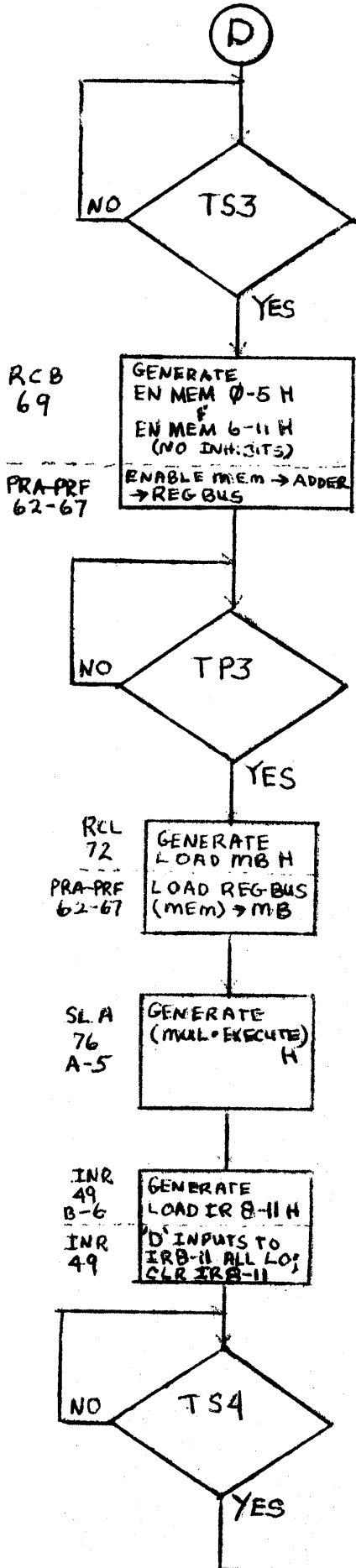


PDP-12  
MULTIPLY

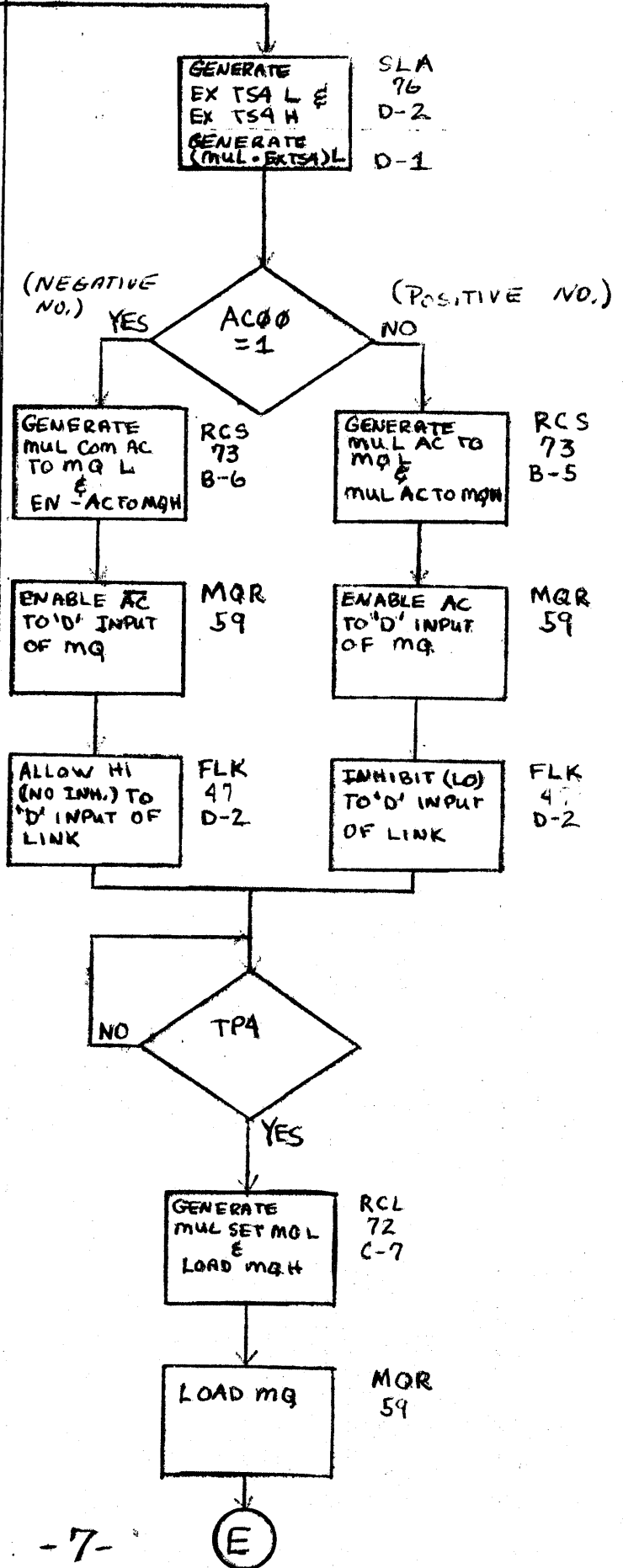
EXECUTE (CONT.)



LOAD MULTIPLICAND TO MB



IF NEGATIVE, COMPLEMENT OF AC -> MQ  
LOAD MULTIPLIER FROM AC -> MQ

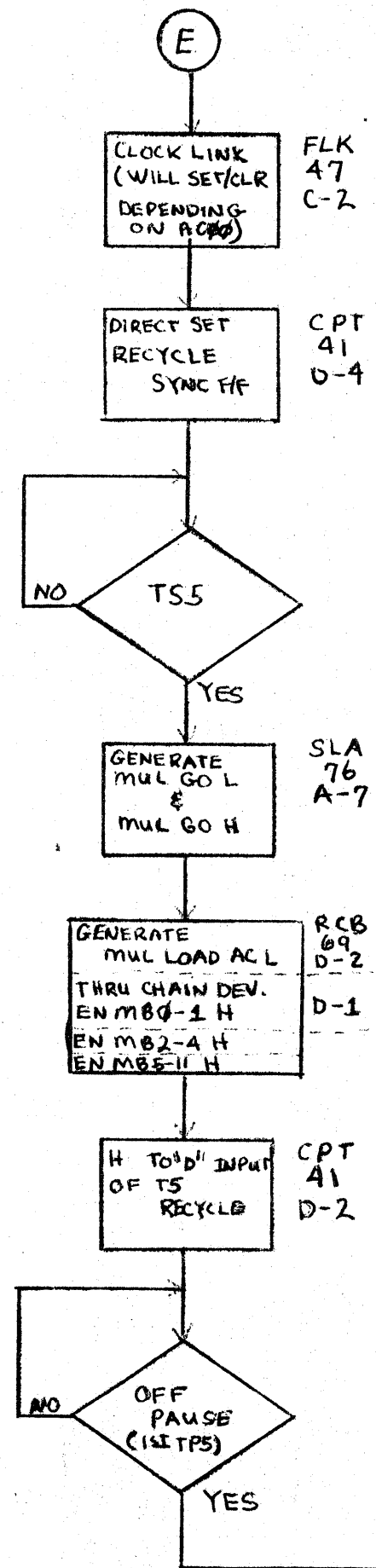


EXECUTE  
(CONT.)

# PDP-12 MULTIPLY

LOAD MULTIPLIER FROM AC → MQ (CONT.)

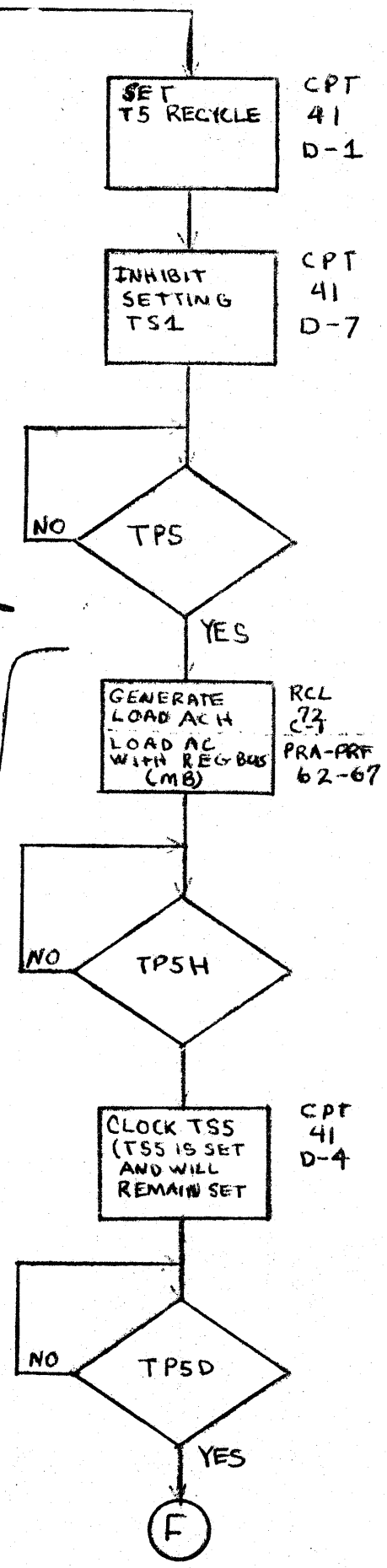
SET UP TIMING TO RECYCLE IN TPS CHAIN



SET UP T5 RECYCLE (CONT.)

LOAD MULTIPLICAND FROM MB TO AC TO CHECK SIGN

T5 1ST TIME



EXECUTE  
(CONT.)

PDP-12  
MULTIPLY

(F)

(TS 1ST TIME (CONT.))

GENERATE LOAD IR8-11 H	INR 49 B-7
LOAD 17(B) → IR8-11 (RESULT OF GATING ON 'D' INPUTS OF IR8-11) INR COUNT ENAB H	INR 49 B-7

RECYCLE TPSD THRU TPS CHAIN	CPTP 42 A-7
-----------------------------------	-------------------

GENERATE N EQ 17L	INS 50 D-1
----------------------	------------------

(NEGATIVE) YES

(POSITIVE) NO

AC 00 = 1

GENERATE TS COMP AC L & EN ACH ----- ENABLE AC → ADDER TO REG BUS	RCC 70 C-7  PRA-PRF 62-67
---	--

GENERATE COMPL H ----- THRU CHAIN WILL PLACE COMP OF LINK ON 'D' INPUT OF LINK FIF	FLK 47 D-7 B-5
--	-------------------------

GENERATE EN AC 0-SH & EN AC 6-11 H	RCA 68 C-2
---	------------------

ENABLE AC THRU ADDER TO REG BUS	PRA-PRF 62-67
---------------------------------------	------------------

GENERATE -LINK EN L=HI (NO INHIBITS) ----- ENABLE LINK → LINK	FLK 47 A-5 D-5
--	-------------------------

(TS 2ND TIME (CONT.))

NO

TP5

YES

GENERATE LOAD MBH & LOAD ACH ----- LOAD REG BUS TO AC & MB	RCL 72 D-7  PRA-PRF 62-67
--	--

CLOCK LINK (WITH LOAD ACH) ----- EITHER LINK → LINK OR LINK → LINK DEPENDING ON AC 00	FLK 47 C-3
---	------------------

SET UP N=16 THRU LOGIC ON 'D' INPUT OF IR8-11	INR 49
--	-----------

NO

TP5D

YES

GENERATE LOAD IR8-11 ----- CLOCK IR8-11 (LOAD N=16)	INR 49
---	-----------

RECYCLE TPSD THRU TPS CHAIN ----- INHIBIT SETTING TS 1 & KEEP TS5 SET	CPTP 42 A-8 CPT 41 D-7
--	---------------------------------------

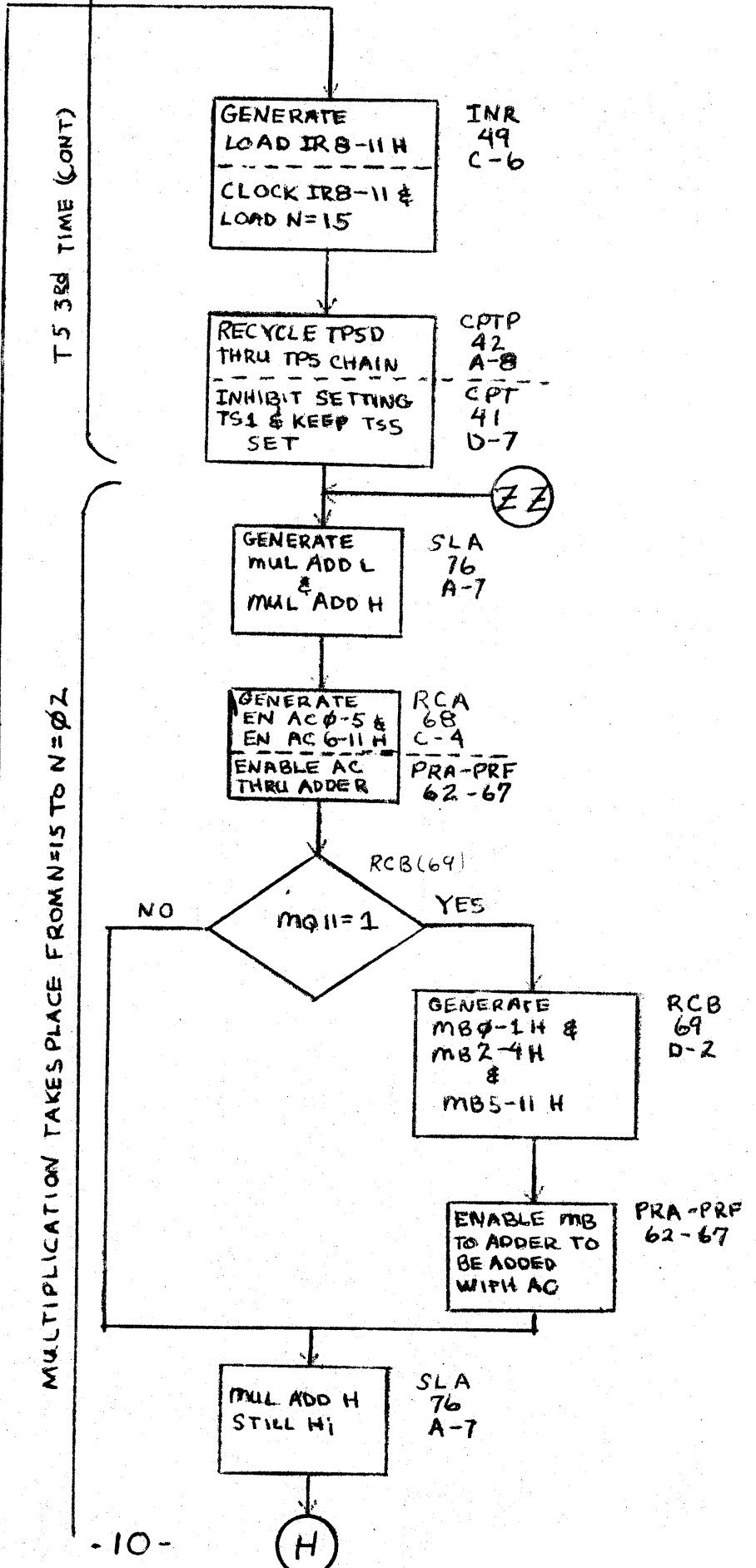
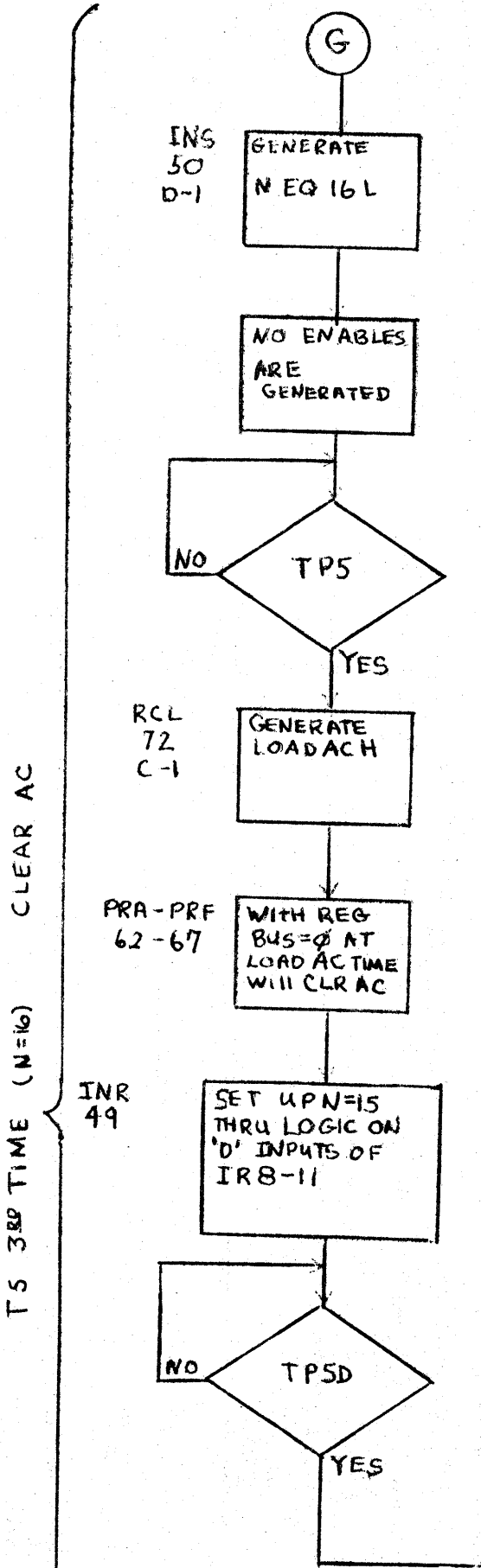
(G)

CHECK SIGN OF  
MULTIPLICAND AND LOAD TO MB

TS 2ND TIME (N=17)

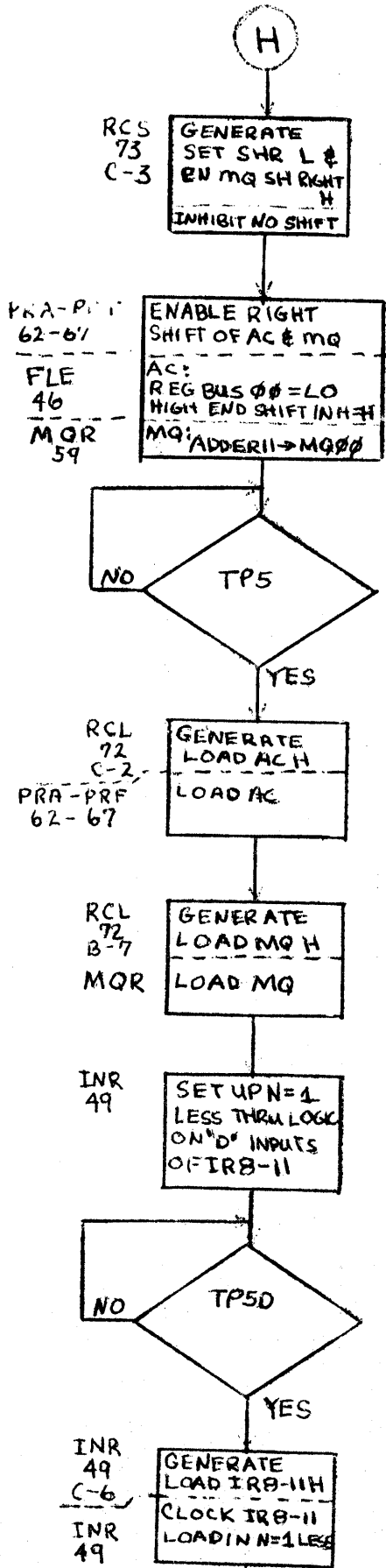
EXECUTE  
(CONT)

PDP-12  
MULTIPLY

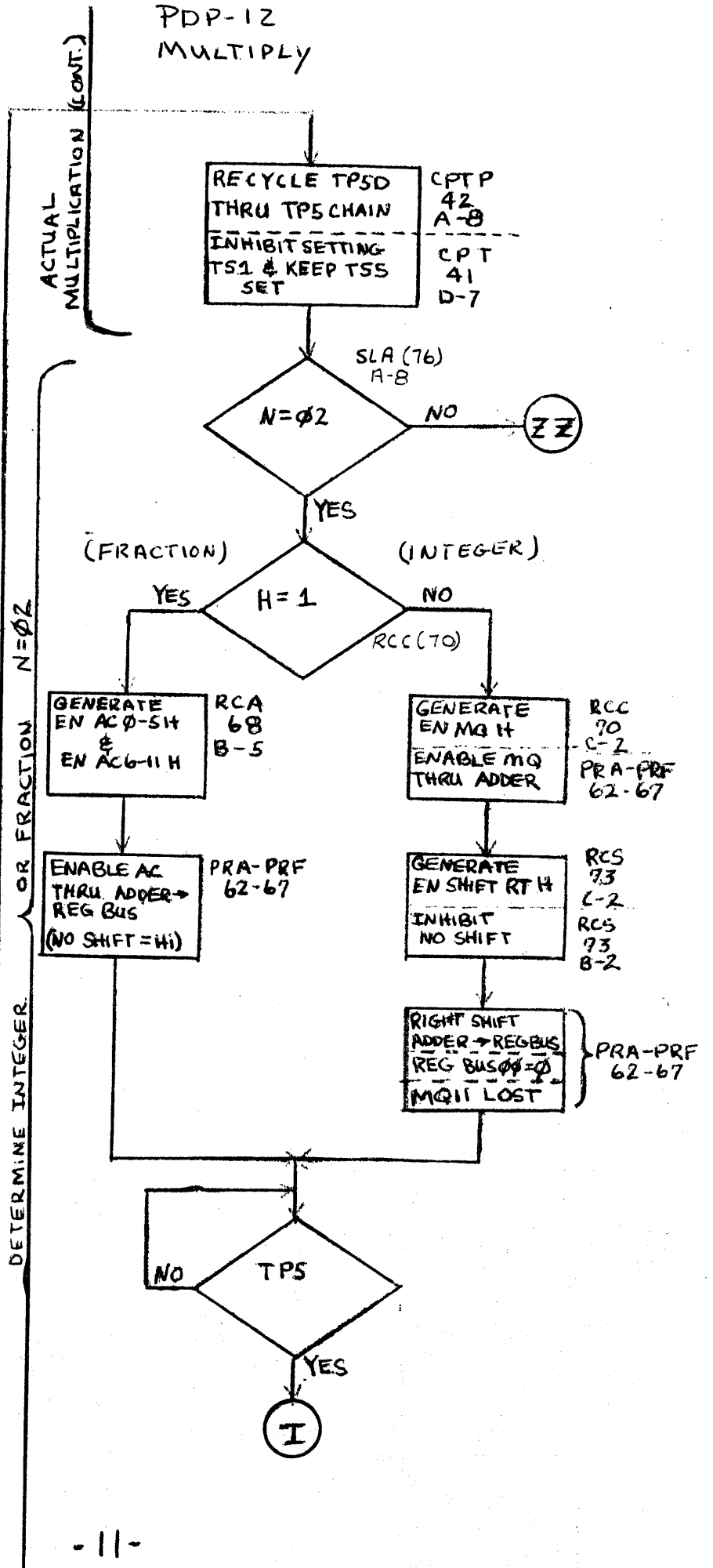


EXECUTE  
(CONT.)

ACTUAL MULTIPLICATION (CONT.)



PDP-12  
MULTIPLY



EXECUTE  
(CONT.)

# PDP-12 MULTIPLY

I

DETERMINE INTEGER / FRACTION (CONT.)

GENERATE LOAD AC H  
LOAD AC  
RCL 72 C-2  
PRA-PRF 62-67

SET UP N=01  
THRU LOGIC ON 'D' INPUTS  
OF IRB-11  
INR 49

NO  
TP5D

GENERATE LOAD IRB-11 H  
LOAD N=01  
INR 49 C-6  
INR 49

RECYCLE TP5D  
THRU TPS CHAIN  
INHIBIT SETTING  
TSL & KEEP TSS SET  
CPTP 42 A-8  
CPT 41 D-7

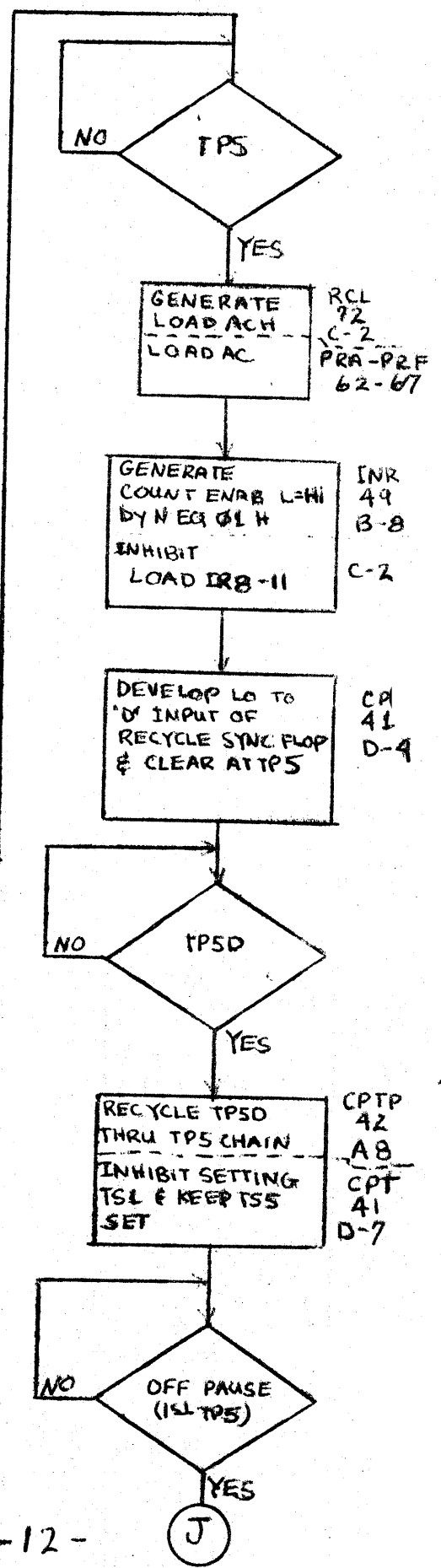
NO  
LINK = 1  
YES

GENERATE EN AC 0-5 H &  
EN AC 6-11 H  
ENABLE AC → ADDER → REG BUS  
RCA 68 B-4  
PRA-PRF 62-67

GENERATE TS COMP AC L  
GENERATE EN -AC H  
INHIBIT EN AC H  
RCC 70 D-7  
C-7  
RCA 68 C-2

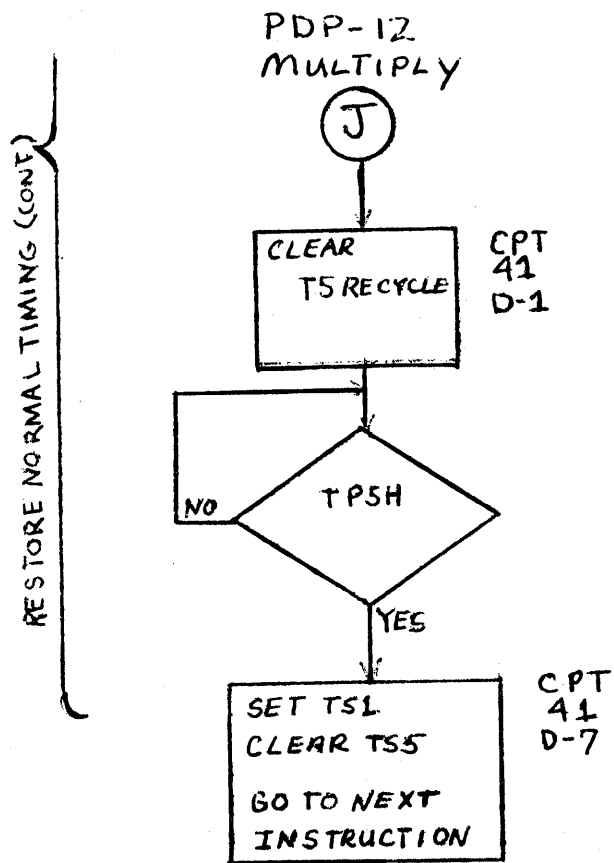
ENABLE AC THRU ADDER  
TO REG BUS  
PRA-PRF 62-67

RESTORE NORMAL TIMING  
COMPLEMENT AC IF NEGATIVE (CONT.)



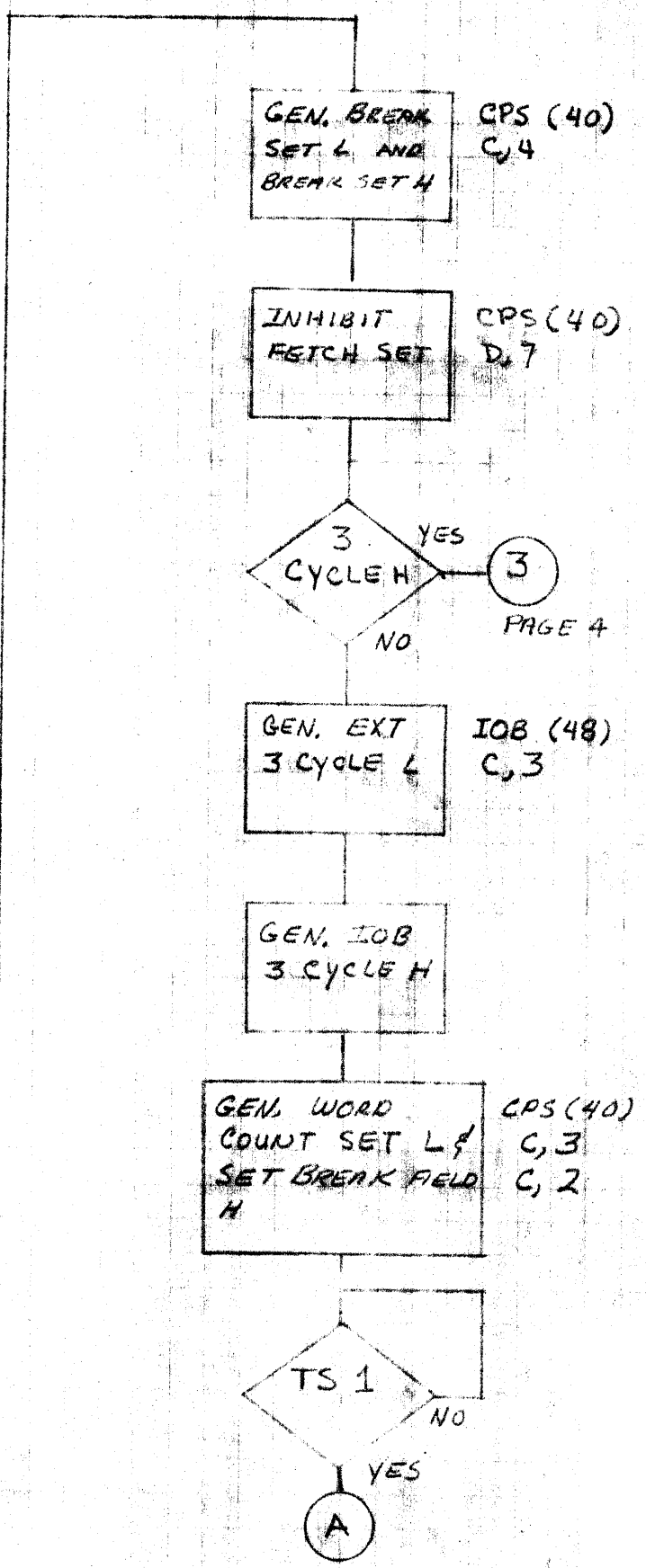
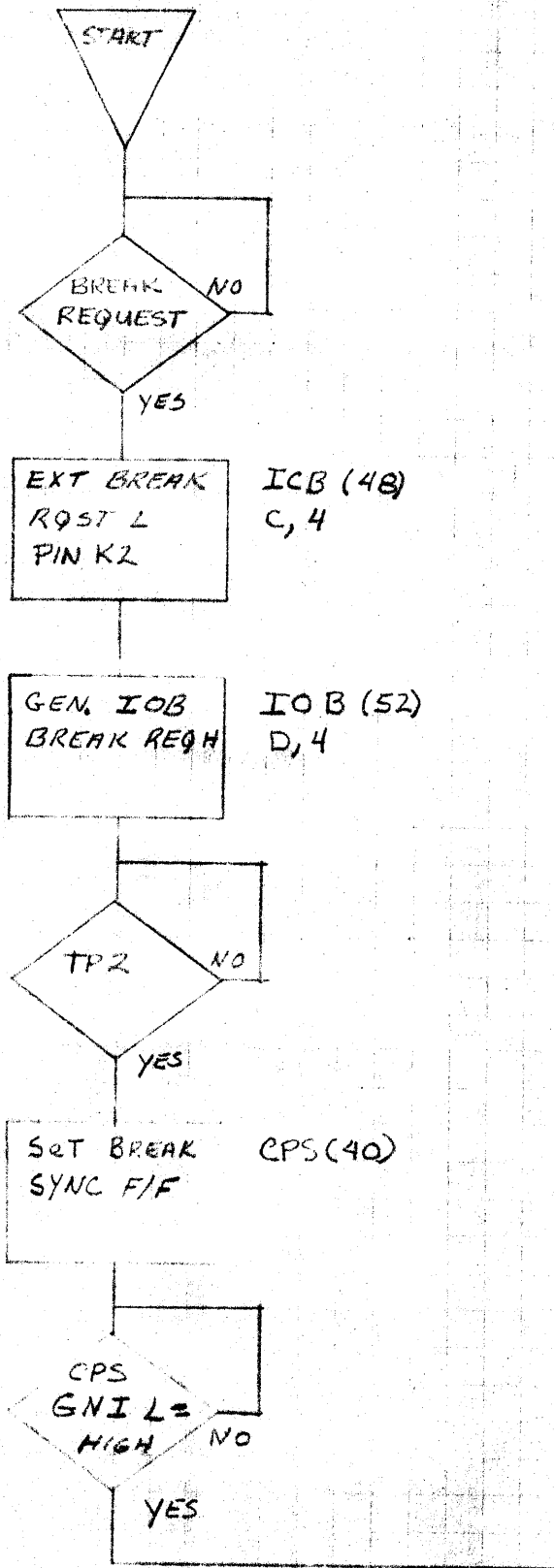
COMPLEMENT AC IF SIGN IS NEGATIVE N=01  
\*NOTE: 'N' WILL NOT be decremented AGAIN

EXECUTE  
(CONT.)

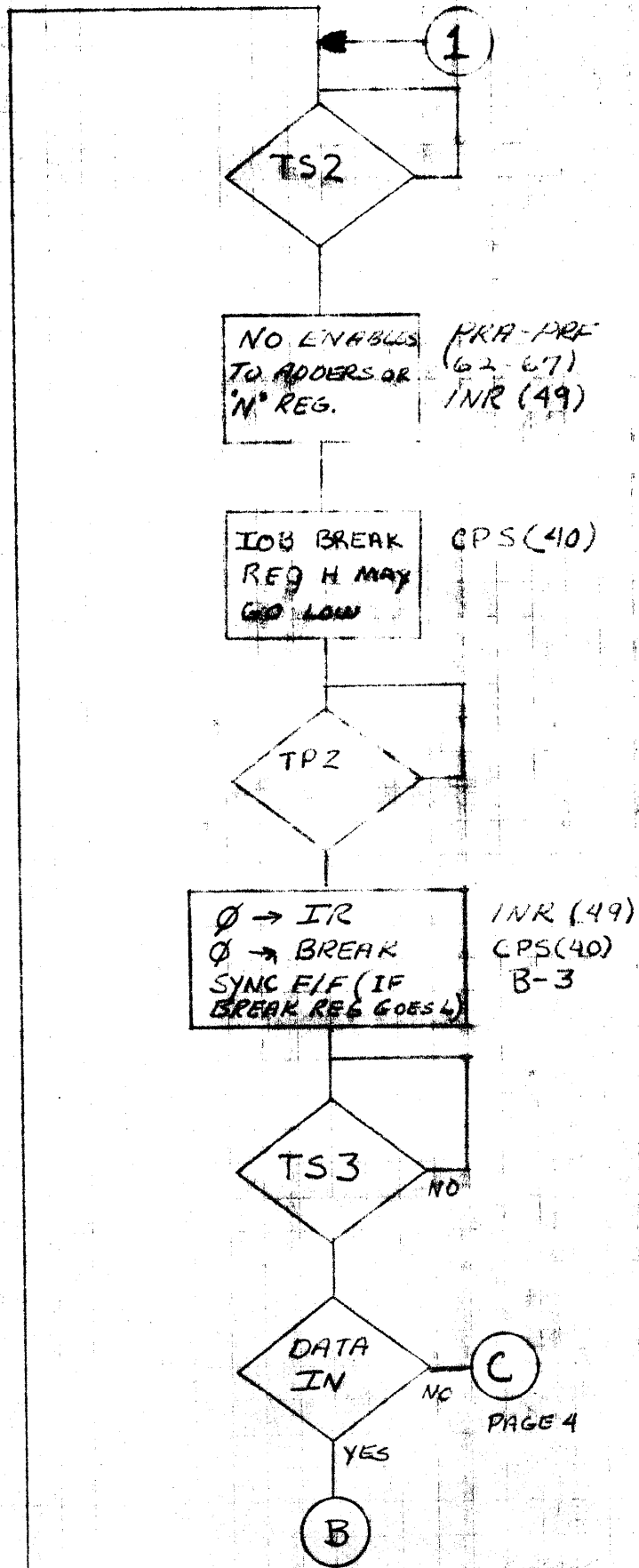
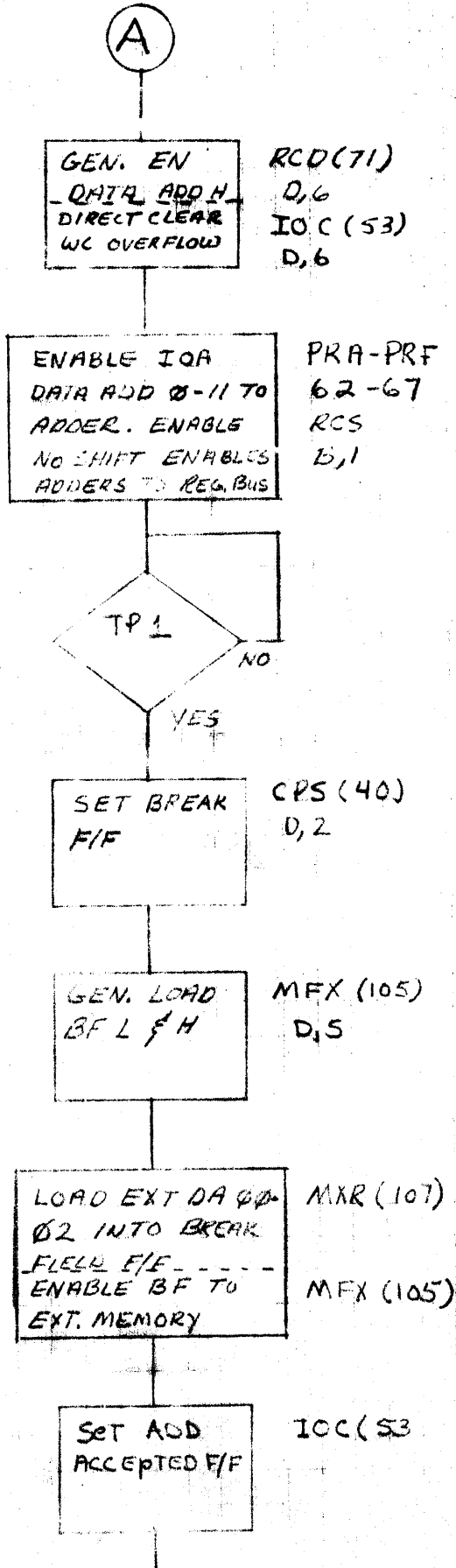




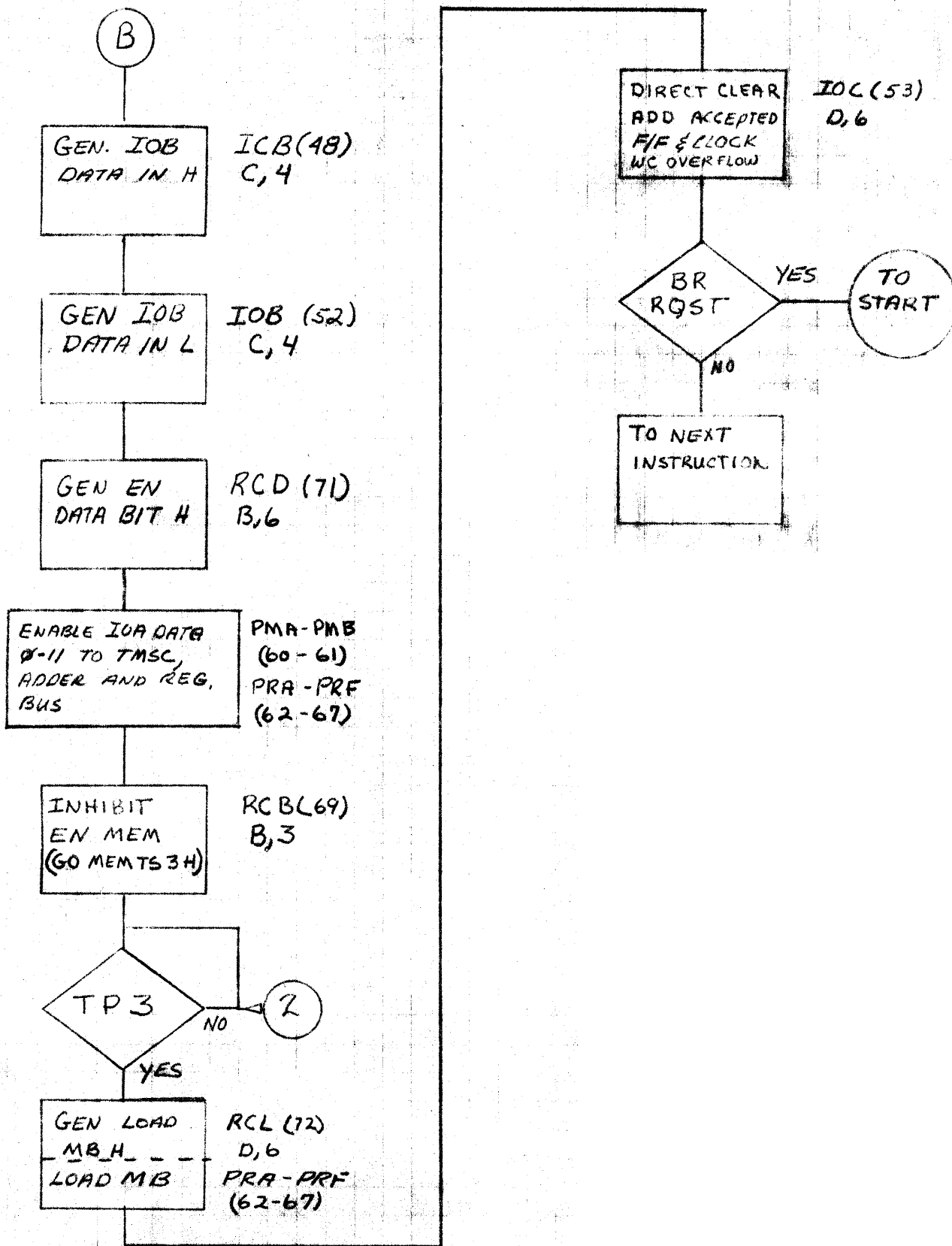
# DATA BREAK POP-12



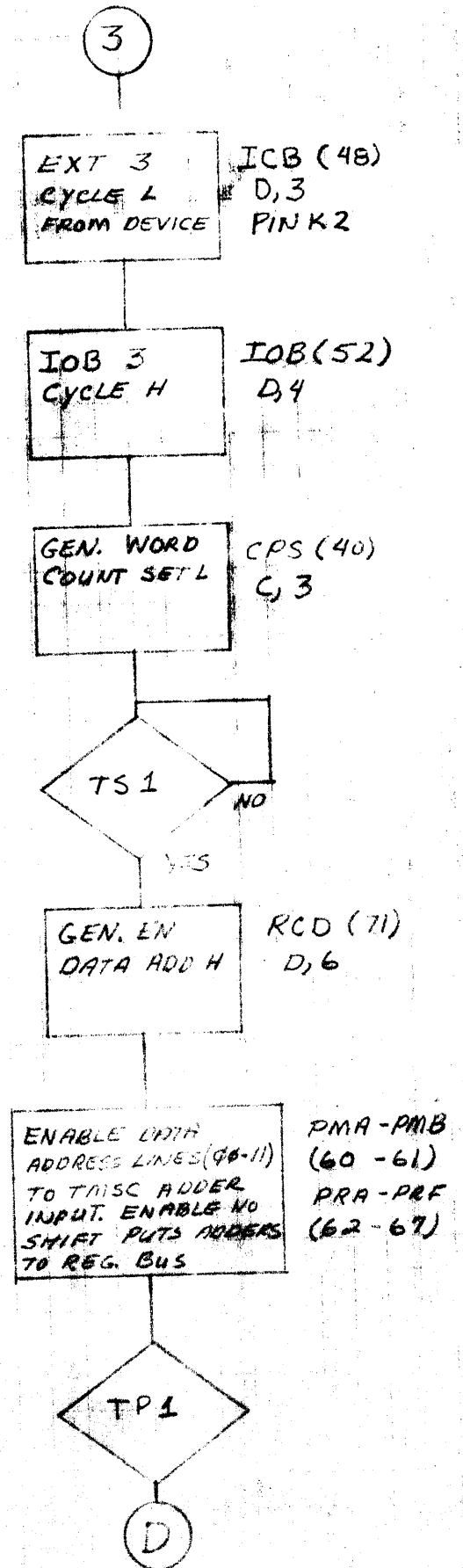
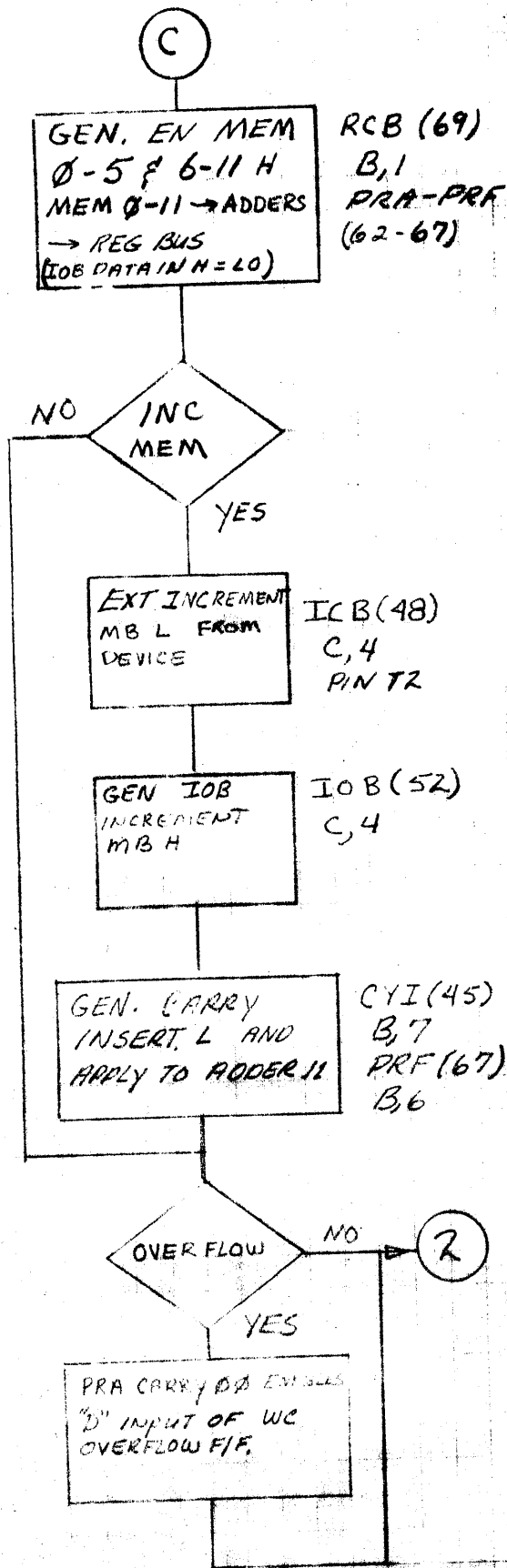
# DATA BREAK PDP-12



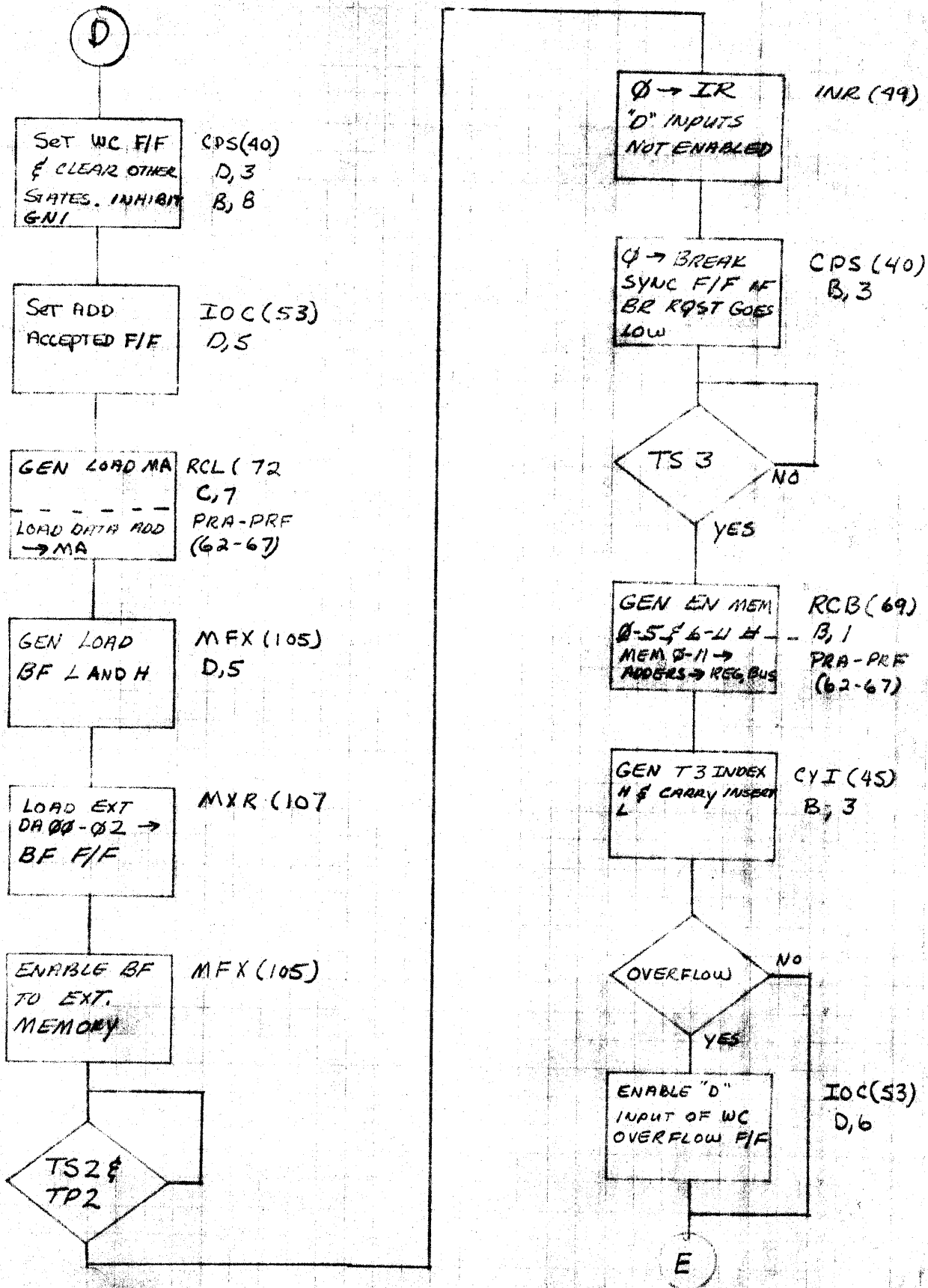
DATA BREAK PDP-12



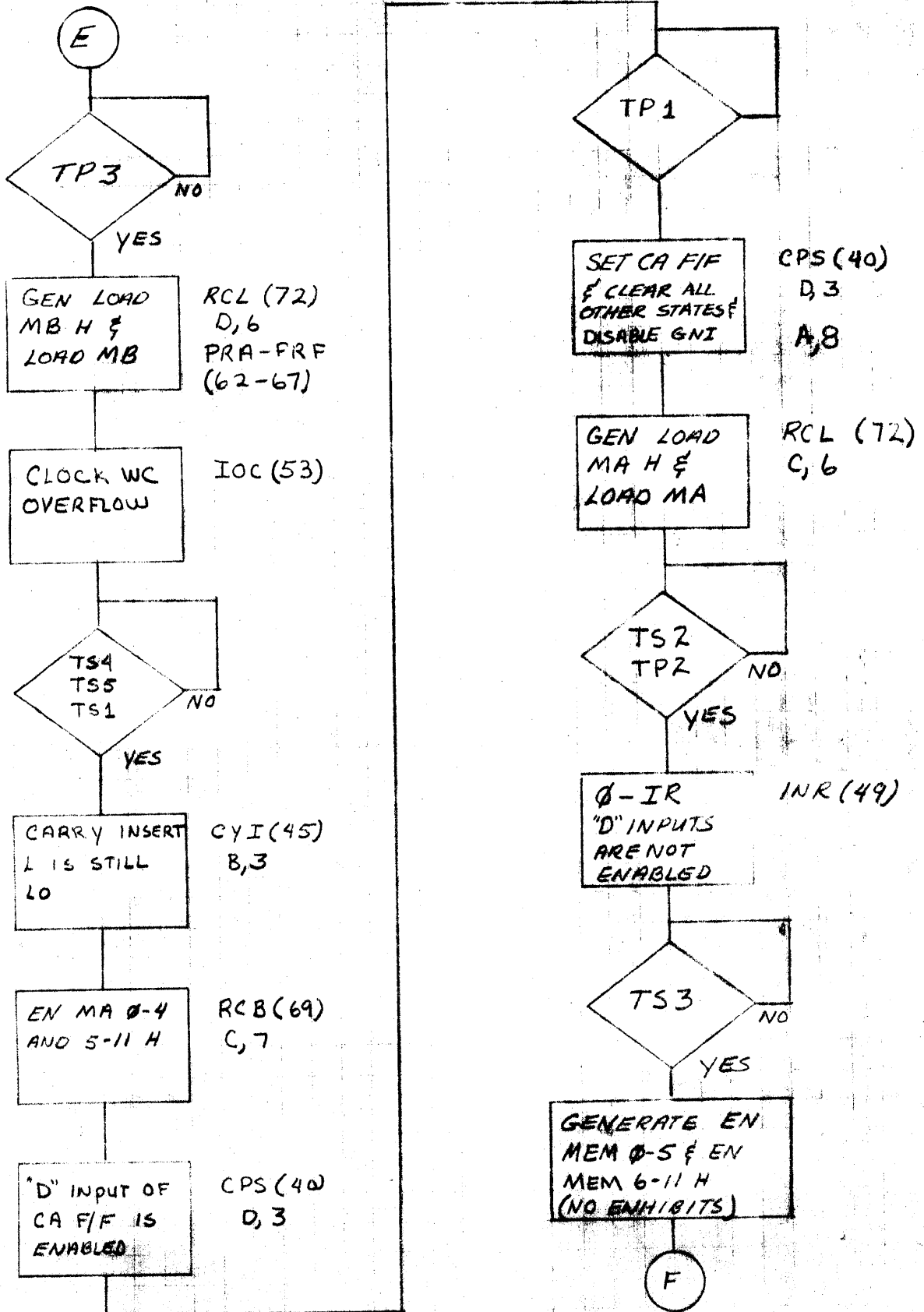
# DATA BREAK PDP-12



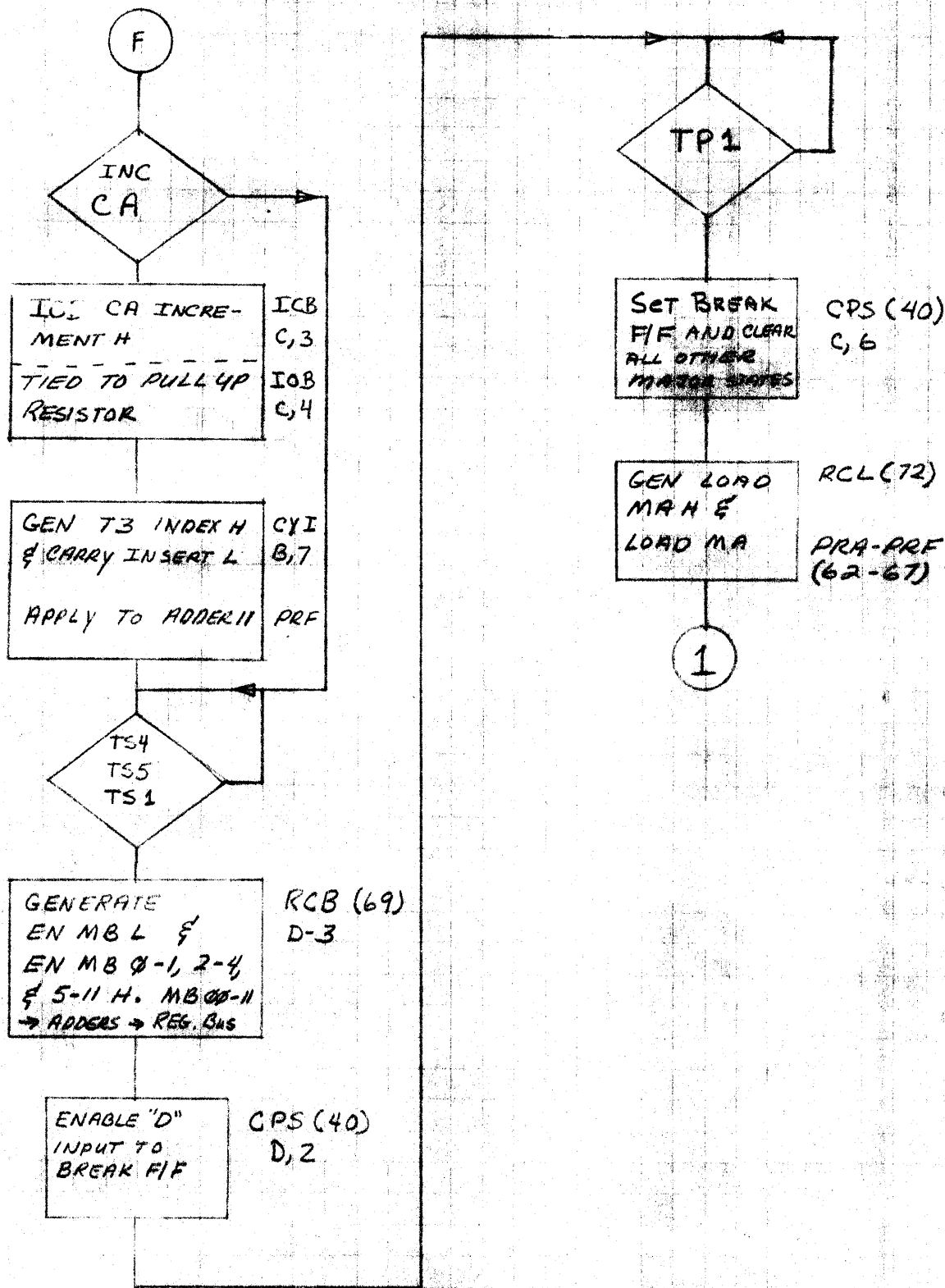
DATA BREAK PDP-12



# DATA BREAK PDP-12



# DATA BREAK FDP-12



# LINC SHIFT AND ROTATES

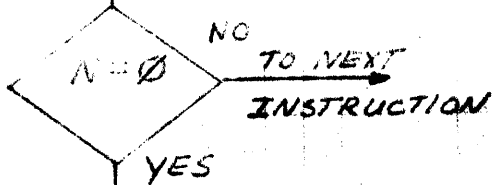
PDP-12

(N COUNTER LOADED AT TP3 OF FETCH)

FECH + TS4

ROR  $\emptyset 3 \emptyset N$   
 SCR  $\emptyset 3 4 N$   
 ROL  $\emptyset 2 4 N$

$$\emptyset \leq N \leq 17$$

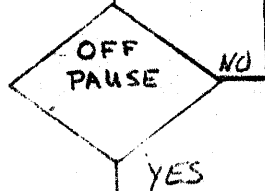
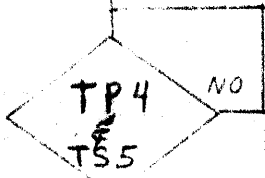


ROTATES L  
 COUNT ENAB H

SLA (76) B-6  
 INR (49) B-7

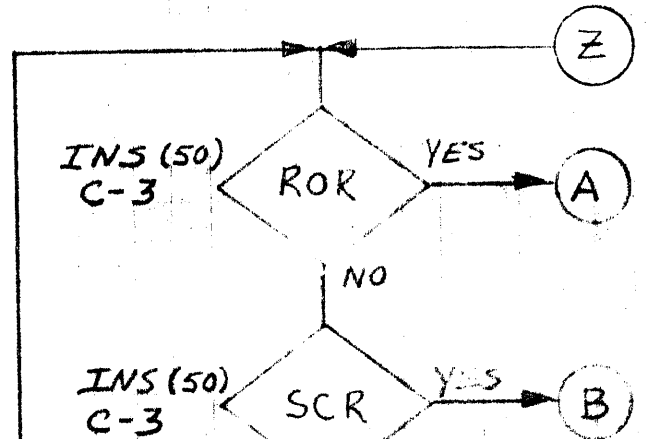
DIRECT SET RECYCLE SYNC F/F

CPT (41) D-3



SET RECYCLE SYNC F/F

CPT (41) D-2



ROL DECODED

INS(50) C-3

EN SHIFT LEFT H  
 ENABLE NO SHIFT DISABLED

RCS (73) C-4

LOW END SHIFT IN

IF  $IR1 = \emptyset$  RC  $\emptyset \rightarrow$  AC11  
 IF  $IR1 = 1$  AC  $\emptyset \rightarrow$  L AND L  $\rightarrow$  RC11

FLE (46) B-4

ADDERS TO REG BUSS

LINK ENABLED (D' AND CLOCK)

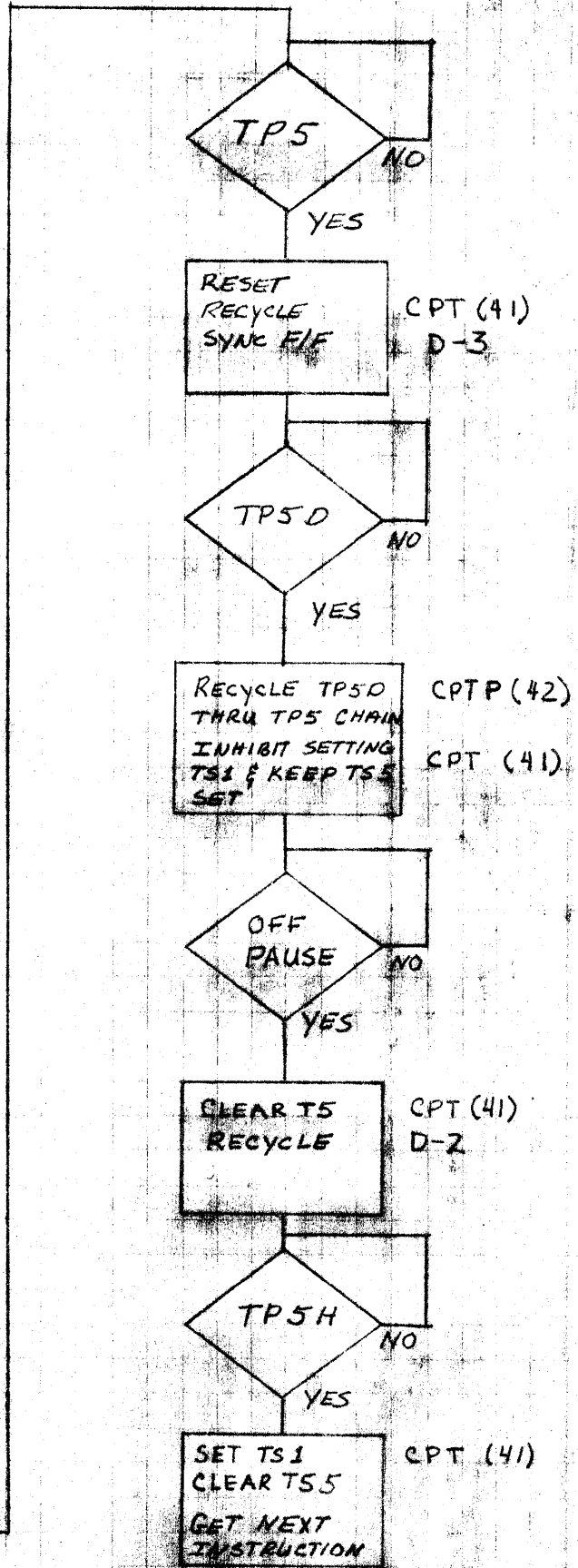
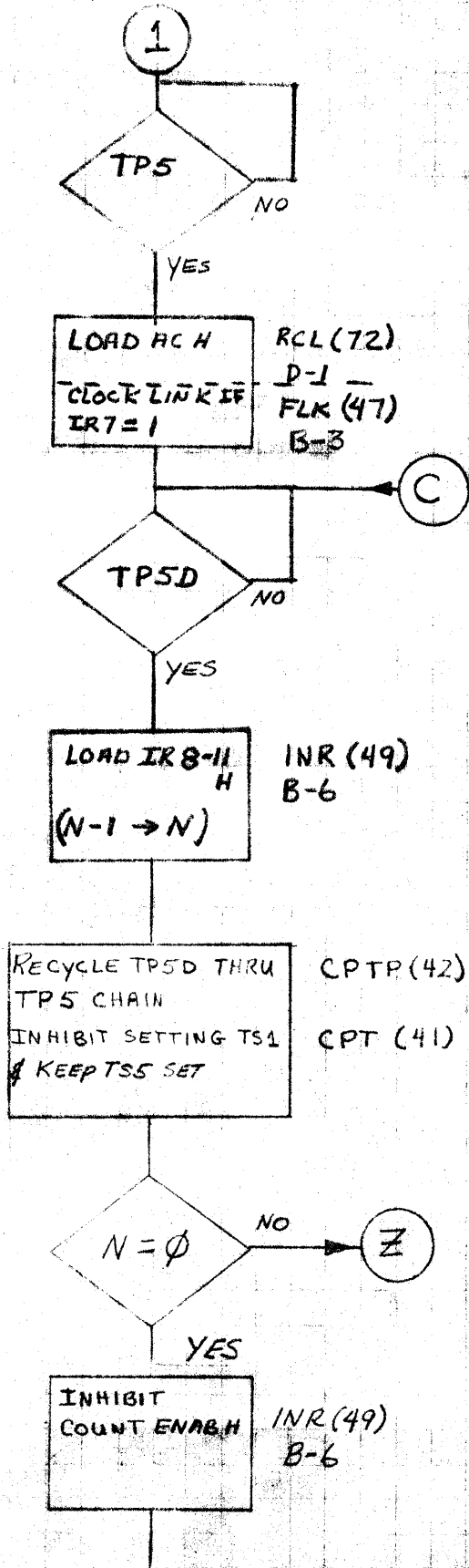
PRA-PRF (62-67) FLK (47) D-2

1



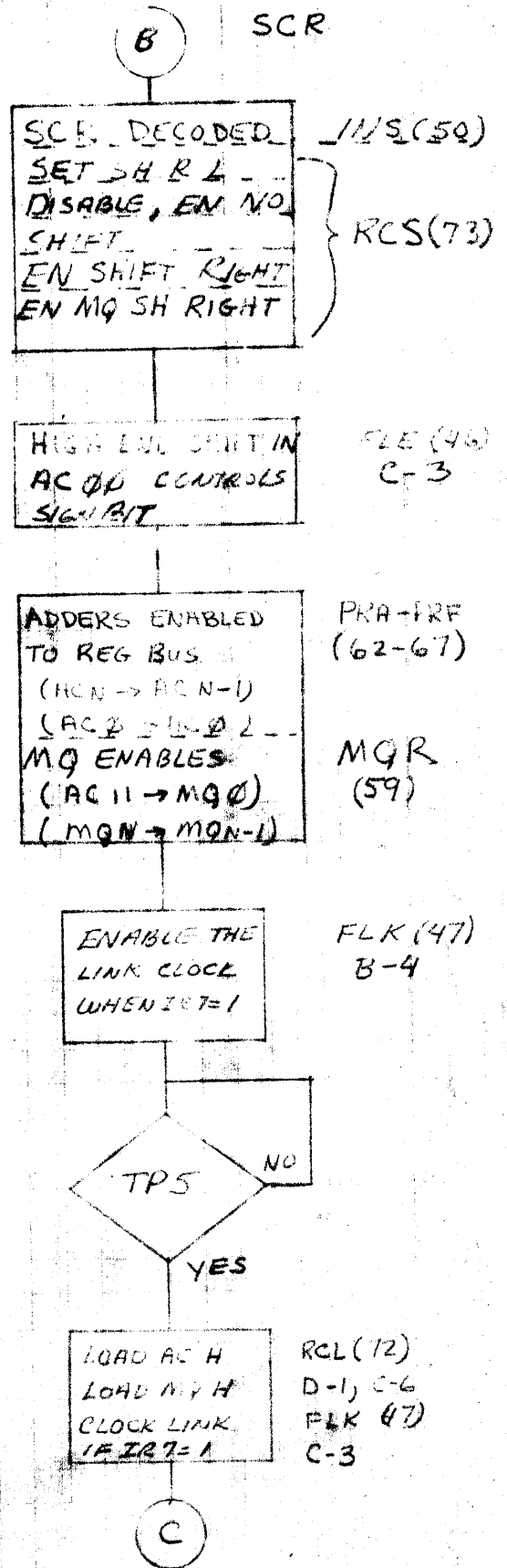
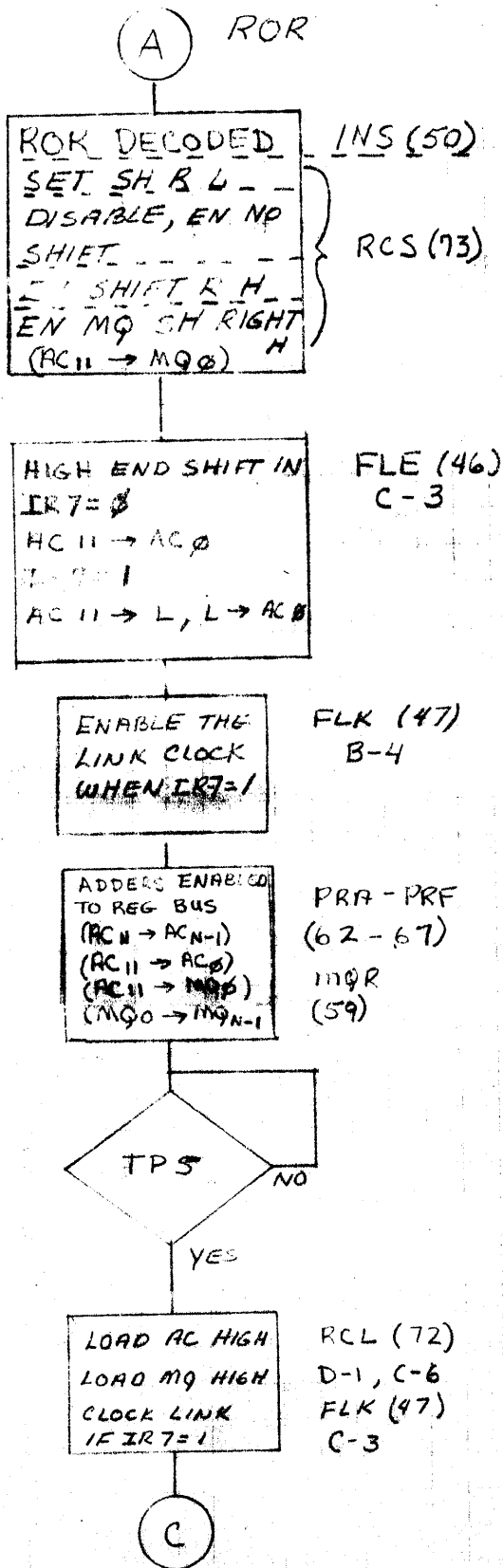
# LINC SHIFTS AND ROTATES

PDP-12

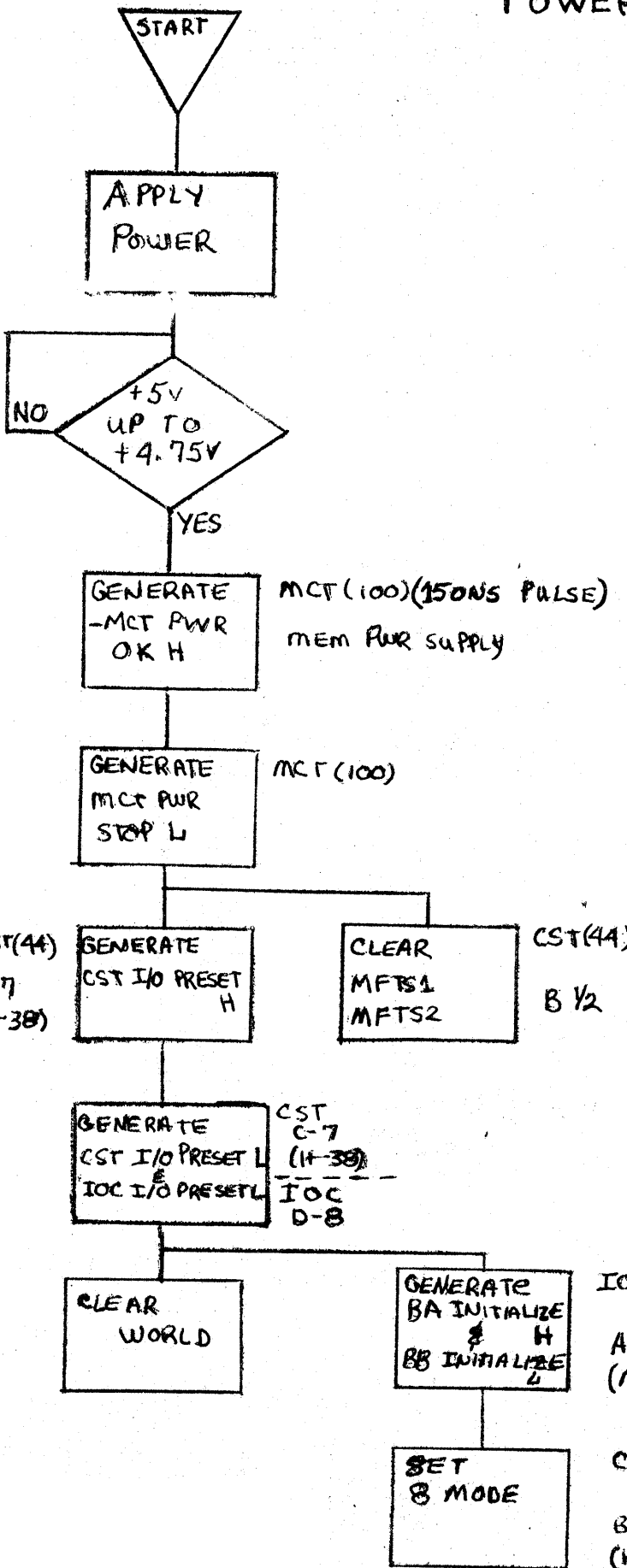


# LINC SHIFTS AND ROTATES

# PDP-12



# PDP-12 POWER UP

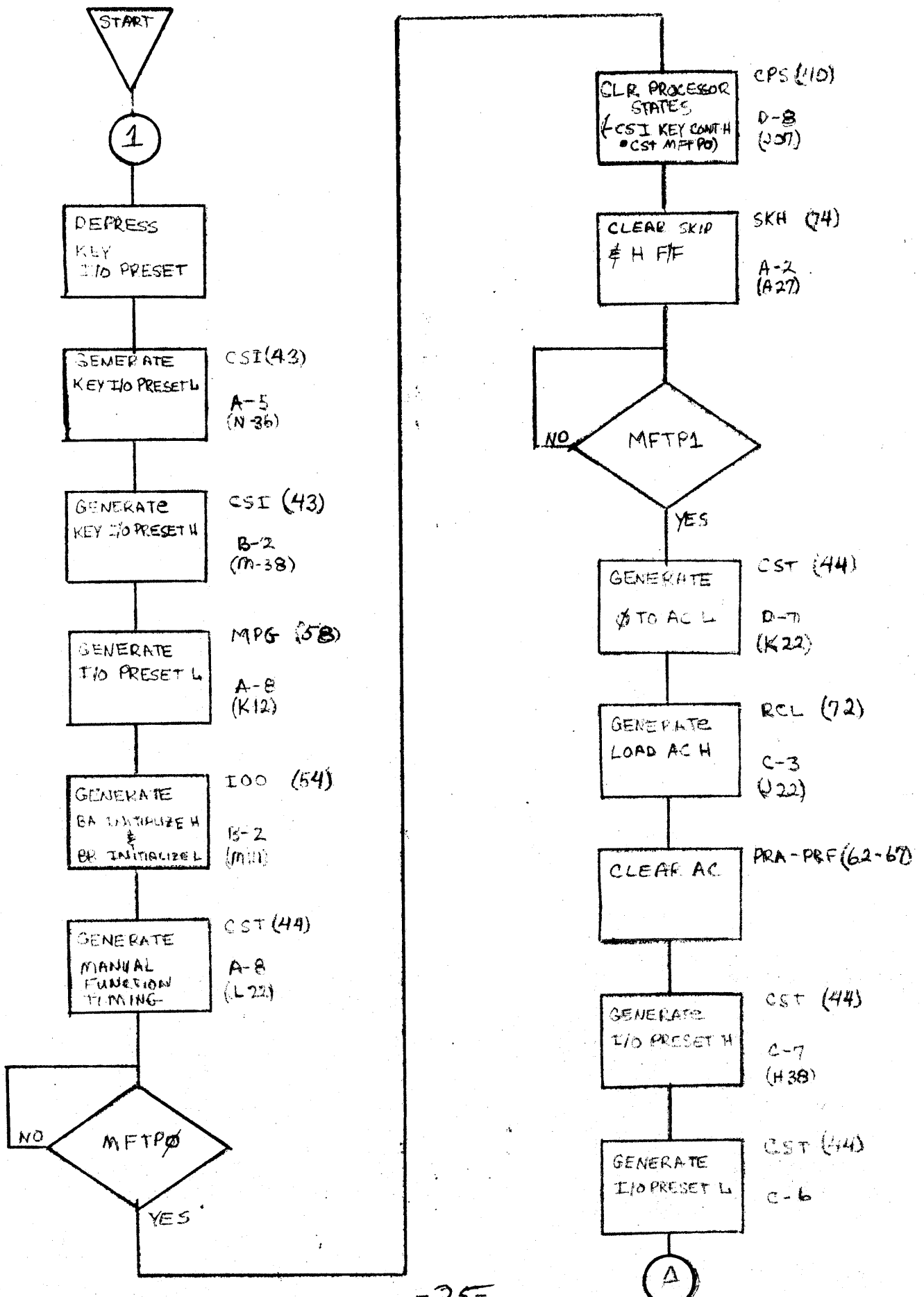


I/O PRESET

<u>CLEAR</u>	<u>SET</u>
DO	EN MEM
FILL STEP	TS1
STEP EXAM	MEM IDLE
AUTO	
TS2	
TS3	
TS4	
TS5	
RUN	
RECYCLE SYNC	
RECYCLE	
INT PAUSE	
IOT PAUSE	

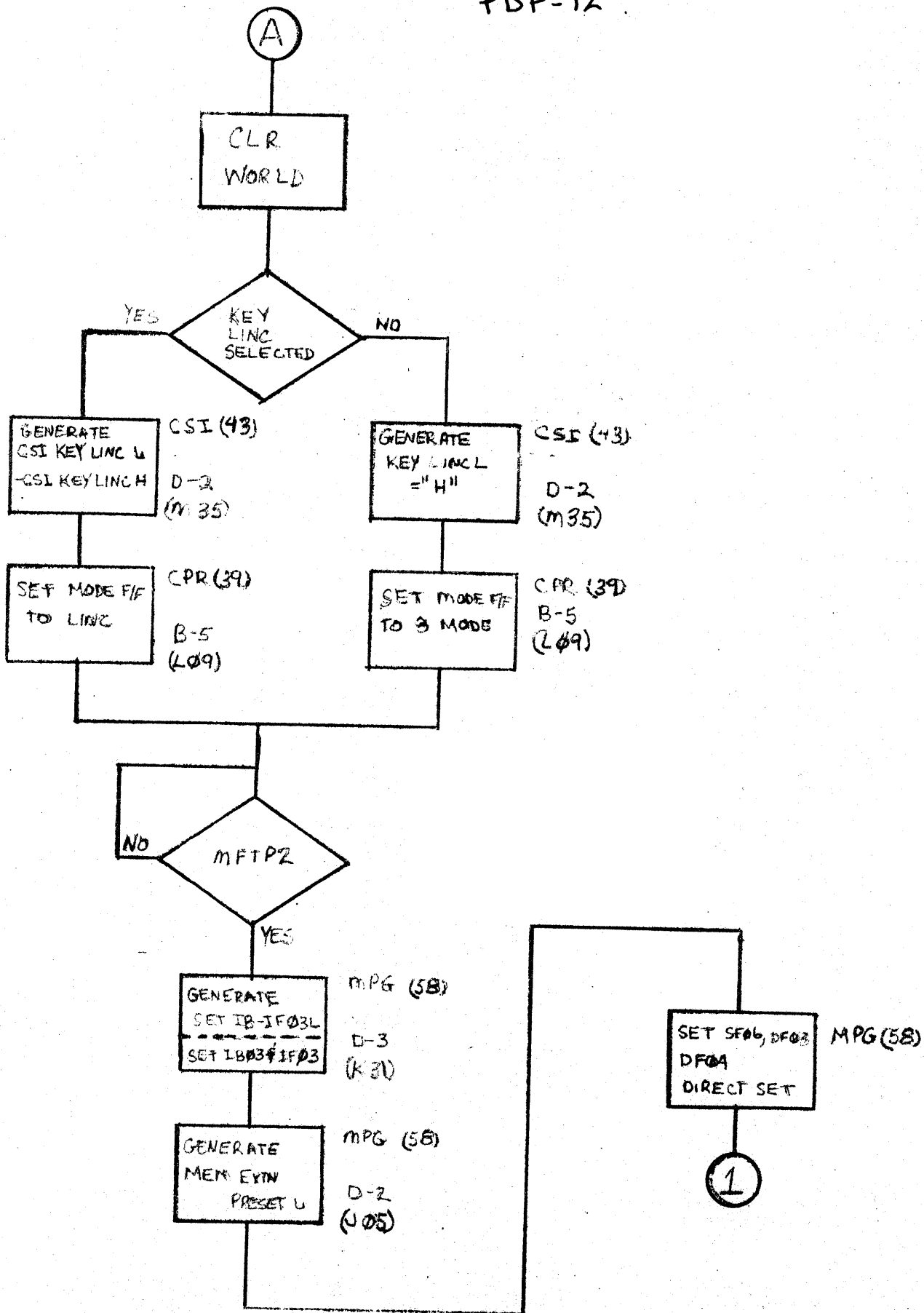
# KEY I/O PRESET

PDP-12



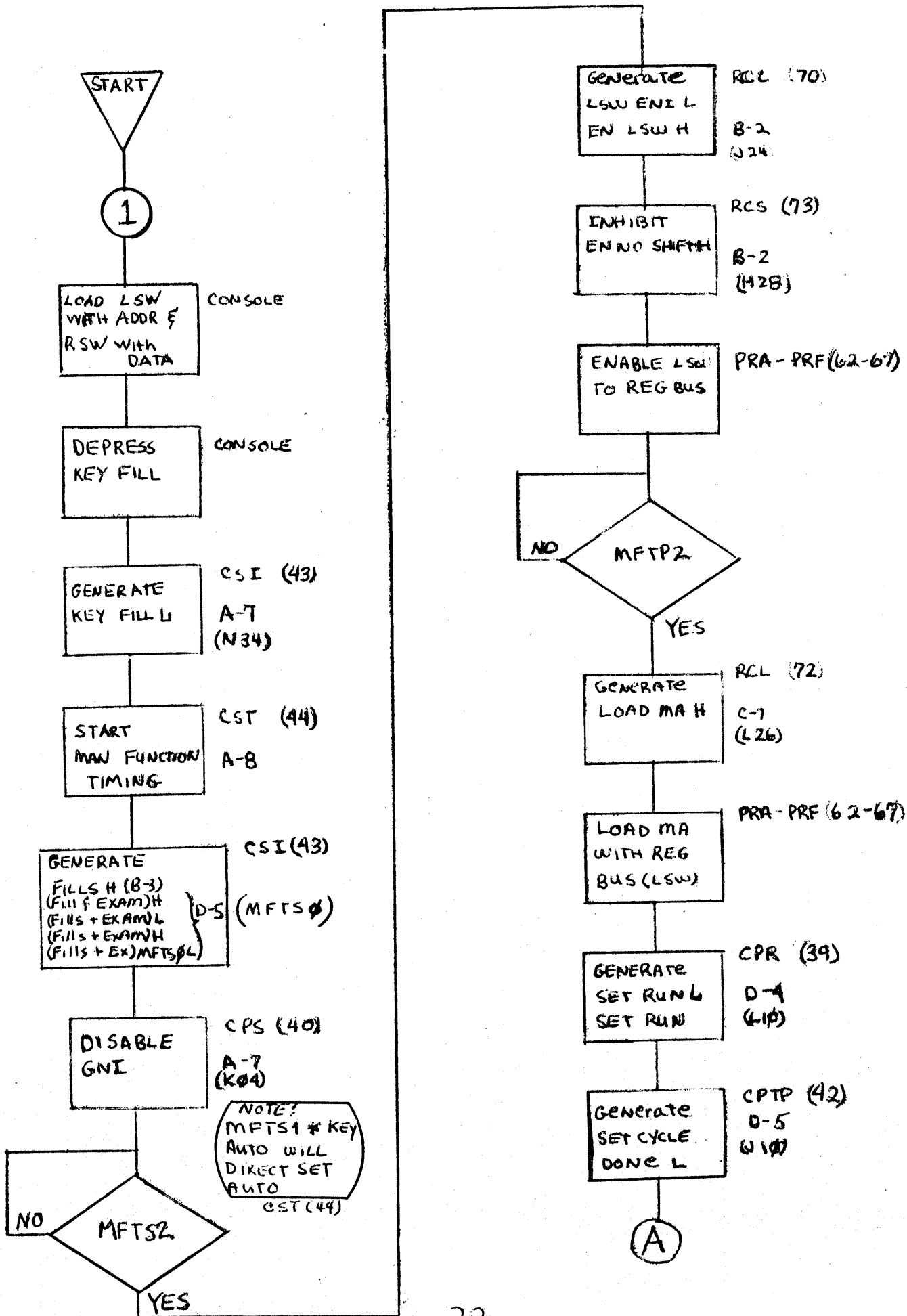
# KEY I/O PRESET (CONT)

PDP-12

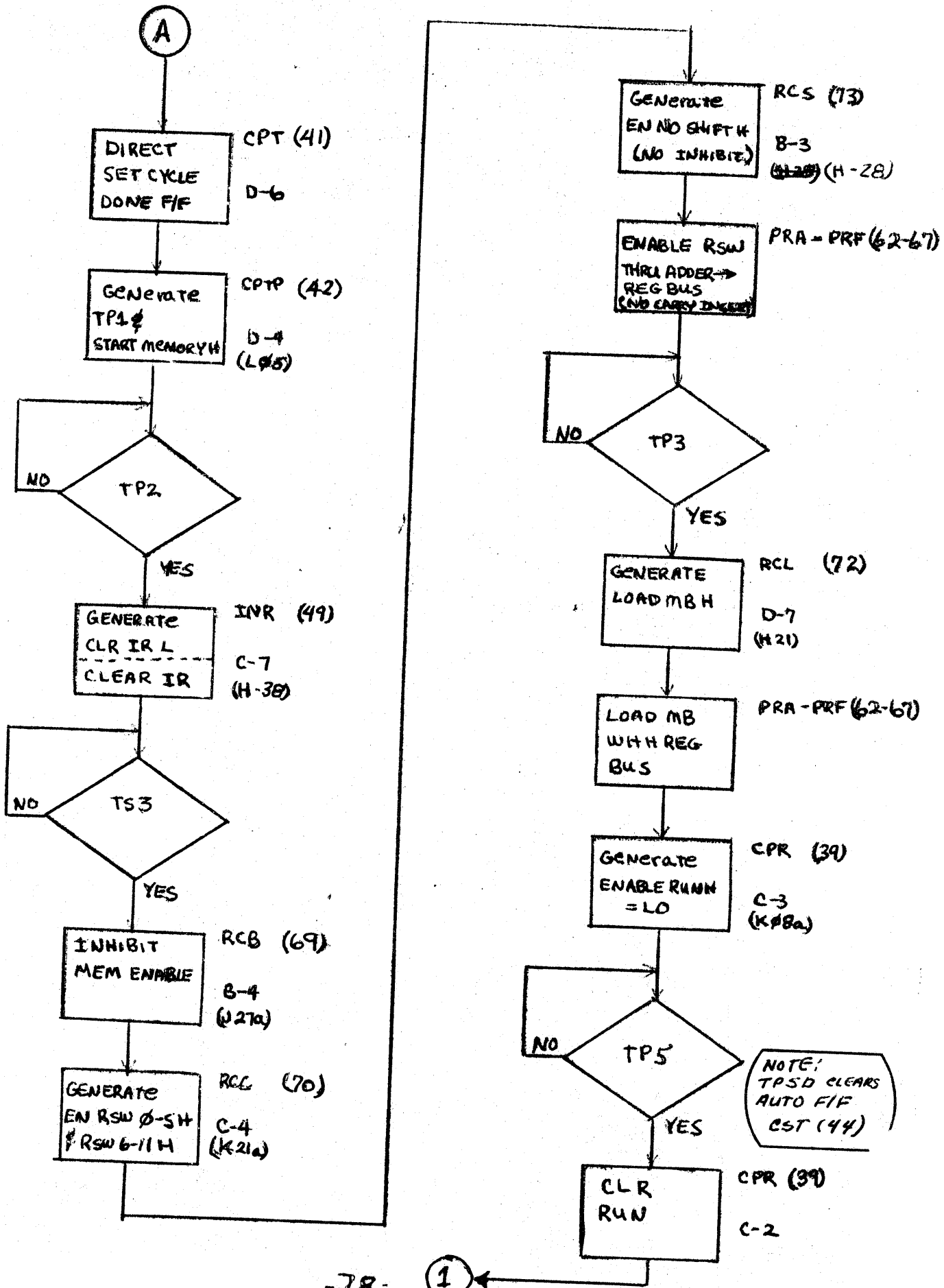


# KEY FILL

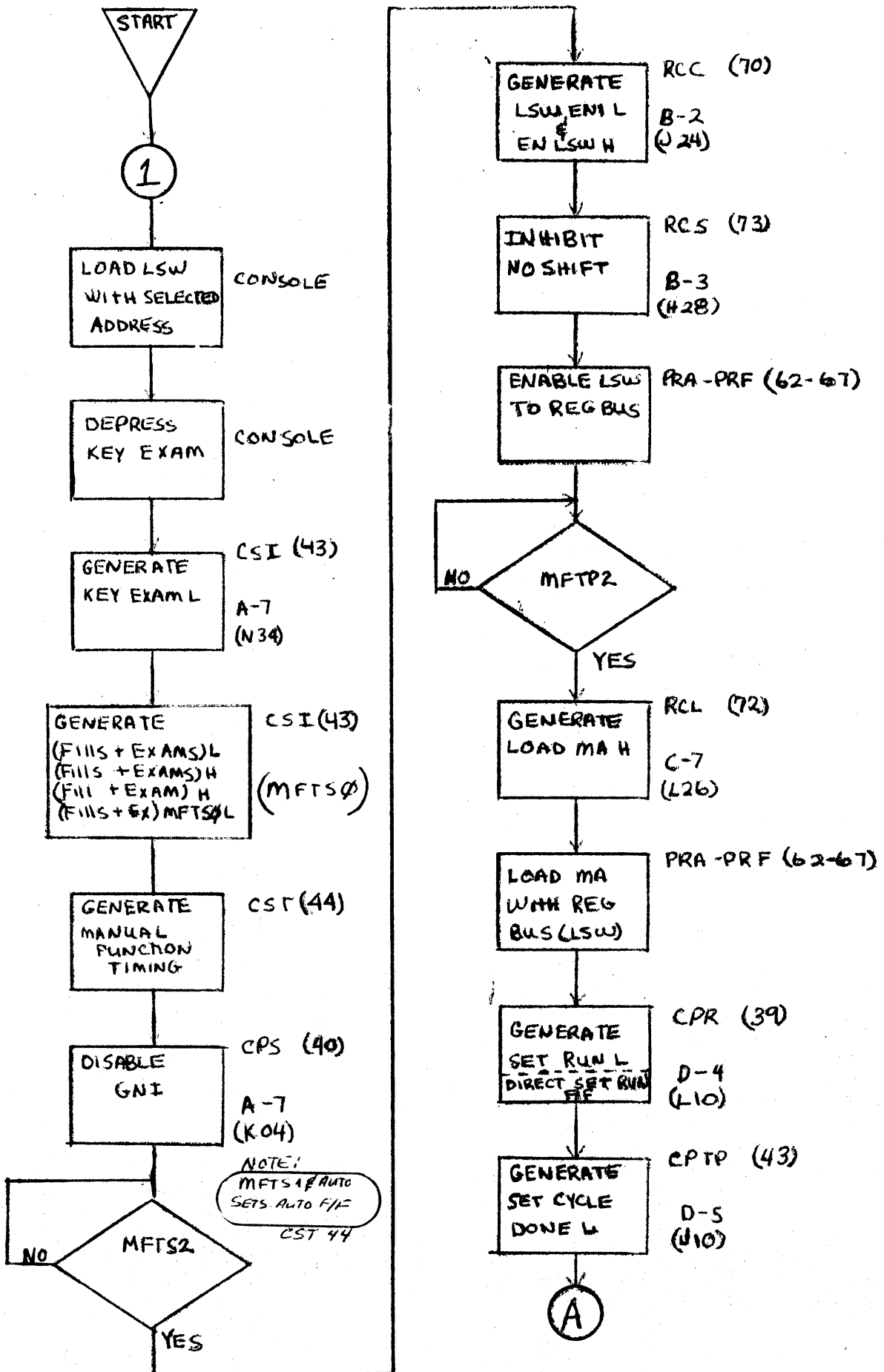
PDP-12



KEY FILE (CONT)  
PDP-12

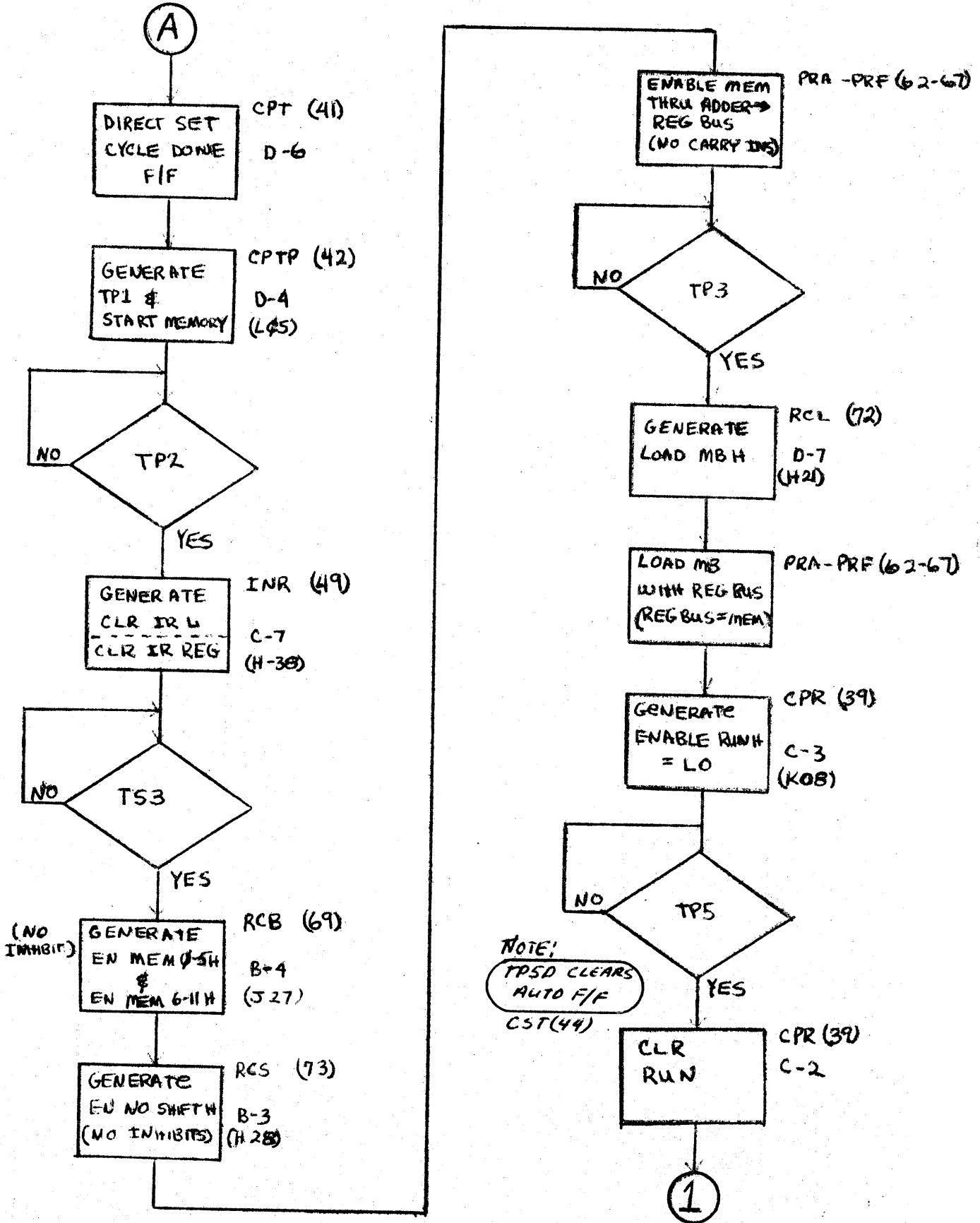


KEY EXAM  
PDP-12



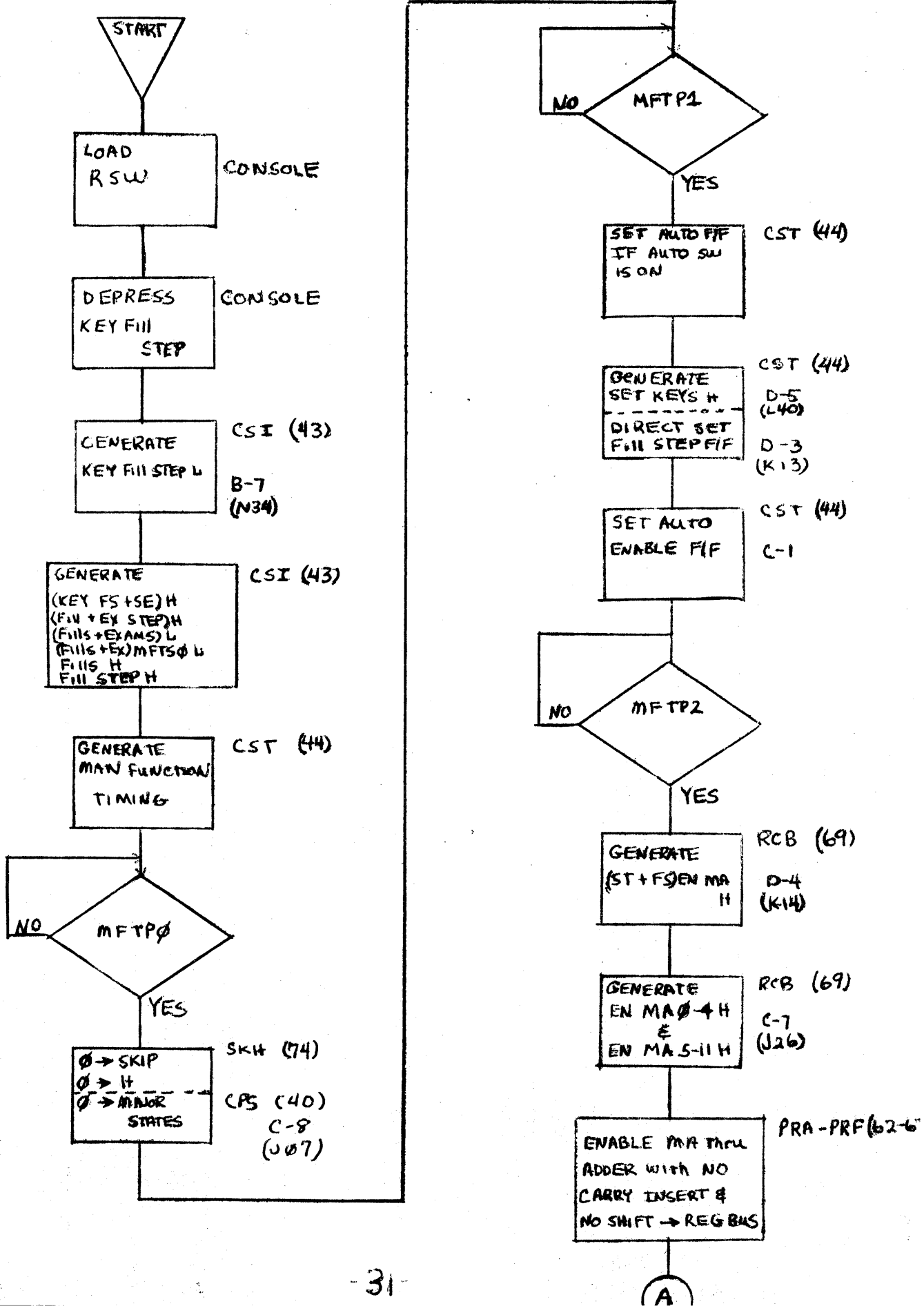


KEY EXAM (CONT.)  
PDP-12



# KEY FILL STEP

PDP-12



# KEY FILL STEP (CONT)

PPD-12

