

16.7.76

IDENTIFICATION

PRODUCT CODE: MAINDEC-11-DZKWA-A
(SUPERSEDES MAINDEC-11-D2DA)
PRODUCT NAME: LINE FREQUENCY CLOCK TEST
DATE REVISED: MAY 10, 1972
MAINTAINER: DIAGNOSTIC GROUP
AUTHOR: JOHN RODENHISER/JIM LACEY

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1. ABSTRACT

THIS PROGRAM TESTS THE KW11L LINE FREQUENCY CLOCK, IT VALIDATES PROPER OPERATION UNDER BOTH INTERRUPT AND NON-INTERRUPT MODES, IT REQUIRES THE OPERATOR TO MONITOR ITS OPERATION WITH A CLOCK CAPABLE OF MEASURING TIME IN SECONDS.

2. REQUIREMENTS

2.1 EQUIPMENT

PDP-11/20 WITH KW11L

2.2 STORAGE

2.2.1 PROGRAM STORAGE - THIS PROGRAM OCCUPIES MEMORY FROM 0 THRU 2170

3. LOADING PROCEDURE

3.1 METHOD

PROCEDURE FOR NORMAL BINARY TAPES SHOULD BE FOLLOWED

1. ABSOLUTE LOADER MUST BE IN MEMORY
2. PLACE BINARY TAPE IN READER
3. LOAD ADDRESS 17500
4. PRESS "START" (PROGRAM WILL LOAD)

4. STARTING PROCEDURE

4.1 CONTROL SWITCH SETTINGS

NOT APPLICABLE

4.2 STARTING ADDRESS

- 200 = 60 HZ, LINE FREQUENCY
- 202 = 50 HZ, LINE FREQUENCY

4.3 PROGRAM AND/OR OPERATOR ACTION

- LOAD PROGRAM INTO MEMORY
- LOAD STARTING ADDRESS
- PRESS "START"

THE PROGRAM WILL BEGIN RUNNING

5, OPERATING PROCEDURE

5,1 OPERATIONAL SWITCH SETTINGS

NOT APPLICABLE

5,2 SUBROUTINES

5,2,1 TIME

THIS SUBROUTINE OPERATES THE CLOCK IN INTERRUPT MODE, THE PROGRAM ENTERS WITH THE NUMBER OF CLOCK PULSES DESIRED IN REGISTER 0 AND EXITS WHEN THAT NUMBER IS REACHED,

6, ERRORS

6,1 ERROR PRINTOUT

NONE

6,2 ERROR RECOVERY

THE PROGRAM WILL HALT ON AN ERROR, TO REPEAT THE SEQUENCE THAT CAUSED THE FAILURE PRESS "CONTINUE" OR RESTART AT 200, IF IT IS DESIRED TO REPEAT THE ERROR SEQUENCE ON A CONTINUOUS BASIS THE OPERATOR CAN REPLACE THE HALT INSTRUCTION WITH A NOP (240).

7, RESTRICTIONS

7,1 STARTING RESTRICTIONS

NONE

7,2 OPERATIONAL RESTRICTIONS

NONE

8, MISCELLANEOUS

NOT APPLICABLE

PROGRAM DESCRIPTION

THE PROGRAM CONSISTS OF A SERIES OF SMALL TESTS THAT CHECK EACH OF THE INDIVIDUAL FUNCTIONS AND CHARACTERISTICS OF THE LINE FREQUENCY CLOCK.

TEST NAME	DESCRIPTION
LKTEST	TEST THAT THE LINE CLOCK INTERRUPT ENABLE (BIT 6) IS CLEARED BY THE START SEQUENCE;
LK1	TEST THAT START SEQUENCE SETS THE CLOCK FLAG (BIT 7);
LK2	TEST THAT THE CLOCK FLAG WILL SET, CLOCK FLAG IS CLEARED AND THEN PROGRAM WAITS A SUFFICIENT AMOUNT OF TIME (20 MILLISECONDS MINIMUM) FOR THE CLOCK FLAG TO REAPPEAR
LK3	TEST THAT INTERRUPT ENABLE (BIT 6) CAN BE SET; PROCESSOR PRIORITY IS RAISED TO LEVEL 7 TO DISALLOW INTERRUPTS AT THIS TIME,
LK4	TEST THAT THE INTERRUPT ENABLE BIT CAN BE CLEARED AFTER IT IS SET;
LK5	TEST THAT THE CLOCK INTERRUPTS TO THE PROPER VECTOR ADDRESS (100), PROCESSOR PRIORITY IS SET TO LEVEL 4 WHICH SHOULD ALLOW A CLOCK INTERRUPT AT LEVEL 6;
LK6	TEST THAT THE CLOCK AT PRIORITY LEVEL 6 WILL INTERRUPT THE PROCESSOR AT PRIORITY LEVEL 5,
LK7	TEST THAT THE CLOCK AT PRIORITY LEVEL 6 WILL NOT INTERRUPT THE PROCESSOR AT PRIORITY LEVEL 6
LK8	TEST THAT THE CLOCK AT PRIORITY LEVEL 6 WILL NOT INTERRUPT THE PROCESSOR AT PRIORITY LEVEL 7

LK9

TEST THAT THE PROCESSOR PUSHES THE STATUS AND PROGRAM COUNTER ONTO THE STACK WHEN INTERRUPTED BY THE CLOCK.

LK10

TEST THAT "RESET" WILL SET THE CLOCK FLAG (BIT 7).

LK11

TEST LINE CLOCK REPEATABILITY BY CHECKING THAT THE CLOCK PUTS OUT THE SAME NUMBER OF PULSES OVER TWO EQUAL PERIODS OF TIME USING BOTH INTERRUPT AND NON INTERRUPT MODES OF OPERATION.

LK12

TEST LINE CLOCK ACCURACY. THIS TEST RINGS THE TELETYPE BELL AT THE COMPLETION OF SEVERAL DIFFERENT TIME INTERVALS OVER A PERIOD OF ONE MINUTE. FROM THE TIME THIS TEST BEGINS THE BELL WILL RING AT THE END OF 1, 2, 3, 4, 5, 10, 20, 30, 40, 50, AND 60 SECONDS. IT WILL THEN REPEAT THIS SEQUENCE AS LONG AS DESIRED. THE 10 SECOND INTERVALS ARE TIMED BY USING THE CLOCK ALTERNATELY IN AN INTERRUPT AND NON-INTERRUPT MODE.

.NLIST SEQ

.TITLE MAINDEC-11-DEKWA-A LINE FREQUENCY CLOCK TEST
;COPYRIGHT 1970, 1972 DIGITAL EQUIPMENT CORP., MAYNARD, MASS
;JOHN RODENHISER/JIM LAGEY
.ENABL ABS
.=0

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.TRAP CATCHER 0-176

000024 000024
000024 001746
000026 000340
000200 000200
000200 000422
000202 000407
000204 177546
000206 000100
000210 177564
000212 177566
000214 177704
000216 177324
000220 176650
177776
000240

.S24
PWR1
340
.S200
BR CYC60
BR CYC50
LKS1 177546
LKV1 100
TCR1 177564
TOBR1 177566
SEC11 =60,
SEC51 =300,
SEC101 =600,
CC=177776
NOP=240

.STARTING ADDRESS FOR 60 HZ,
.STARTING ADDRESS FOR 50 HZ,

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000222 012767 177716 177764 CYC501 MOV #-50,,SEC1 ISET UP 50 HZ CONSTANTS
000230 012767 177406 177760 MOV #-250,,SEC5
000236 012767 177014 177754 MOV #-500,,SEC10
000244 000411 BR START
000246 012767 177704 177740 CYC601 MOV #-60,,SEC1 ISET UP 60 HZ CONSTANTS
000254 012767 177324 177734 MOV #-300,,SEC5
000262 012767 176650 177730 MOV #-600,,SEC10
000270 012706 002124 START1 MOV #BUFF,X6
000274 012737 001746 000024 MOV #PWR1,#24
000302 012737 000340 000026 MOV #340,#26
000310 005737 000042 TST #N42 ILOADED BY A MONITOR
000314 001401 BEQ LKTEST IOR IF NO
000316 000005 RESET IYES--GENERATE AN INIT

000320 032777 000100 177656 ITEST THAT START CLEARS LINE CLOCK INTERRUPT ENABLE BIT
LKTEST1 BIT #100,@LKS
000326 001402 BEQ LK1
000330 000000 HALT IERROR, CLOCK INTERRUPT ENABLE NOT CLEARED BY START
000332 000772 BR LKTEST

000334 105777 177644 ITEST THAT START SETS CLOCK FLAG
LK11 TSTB @LKS
000340 100402 BMI LK2
000342 000000 HALT IERROR, CLOCK FLAG NOT SET BY START
000344 000773 BR LK1

000346 005077 177632 ITEST THAT CLOCK FLAG WILL SET AFTER SUFFICIENT PERIOD OF TIME (20 MS MIN)
LK21 CLR @LKS
000352 005000 CLR X0
000354 105777 177624 LK2A1 TSTB @LKS IIS CLOCK FLAG SET
000360 100404 BMI LK3
000362 005200 INC X0 INO, INCREMENT COUNT
000364 001373 BNE LK2A IWAIT SUFFICIENT AMOUNT OF TIME FOR CLOCK
000366 000000 HALT IERROR, CLOCK FLAG FAILED TO SET
000370 000766 BR LK2

000372 005077 177606 ITEST THAT INTERRUPT ENABLE BIT MAY BE SET
LK31 CLR @LKS
000376 105777 177602 TSTB @LKS
000402 100375 BPL I=-4 ISYNC CLOCK
000404 012767 000340 177364 MOV #340,CC ISET PRIORITY 7
000412 012777 000100 177564 MOV #100,@LKS ICLEAR CLOCK FLAG AND SET INTERRUPT ENABLE
000420 032777 000100 177556 BIT #100,@LKS IIS INTERRUPT ENABLE SET?
000426 001002 BNE LK4
000430 000000 HALT IERROR INTERRUPT ENABLE NOT SET
000432 000757 BR LK3

000434 005077 177544 ITEST THAT INTERRUPT ENABLE BIT MAY BE CLEARED
LK41 CLR @LKS
000440 105777 177540 TSTB @LKS
000444 100375 BPL I=-4 ISYNC CLOCK
000446 012767 000340 177322 MOV #340,CC ISET PRIORITY 7
000454 012777 000100 177522 MOV #100,@LKS ICLEAR CLOCK FLAG AND SET INTERRUPT ENABLE
000462 005077 177516 CLR @LKS ICLEAR INTERRUPT ENABLE

000466 032777 000100 177510 BIT #100,@LKS
000474 001402 BEQ LK5 IIS INTERRUPT ENABLE CLEARED
000476 000000 HALT IERROR, ERROR INTERRUPT BIT CAN NOT BE CLEARED

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MAINDEC-11-DZKWA-A
DZKWA,PI1

LINE FREQUENCY CLOCK TEST

MACY11,616 10-MAY-72 10109 PAGE 3

000500 000755

BR

LK4


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)TEST THAT CLOCK INTERRUPTS TO CORRECT VECTOR ADDRESS
000502 012706 002124 LK5I MOV #BUFF,X6
000506 012767 000200 177262 MOV #200,CC )SET PROCESSOR PRIORITY 4
000514 012777 000554 177464 MOV #LK5B,@LKV )SET UP VECTOR RETURN POINTER
000522 005077 177456 CLR @LKS
000526 105777 177452 TSTB @LKS
000532 100375 BPL ,=4 )SYNC CLOCK
000534 012777 000100 177442 MOV #100,@LKS )ENABLE INTERRUPT
000542 005000 CLR X0
000544 005200 LK5AI INC X0
000546 001376 BNE LK5A )WAIT FOR INTERRUPT
000550 000000 HALT )ERROR, INTERRUPT FAILED TO OCCUR
000552 000753 BR LK5
000554 105777 177424 LK5B: TSTB @LKS )ENTER HERE IF INTERRUPTED
000560 100402 BMI LK6
000562 000000 HALT )ERROR, INTERRUPT NOT CAUSED BY CLOCK
000564 000746 BR LK5

)TEST THAT CLOCK WILL INTERRUPT WITH PROCESSOR AT PRIORITY 5
000566 005077 177412 LK6I CLR @LKS
000572 105777 177406 TSTB @LKS
000576 100375 BPL ,=4 )SYNC CLOCK
000600 012706 002124 MOV #BUFF,X6
000604 012767 000240 177164 MOV #240,CC )SET PRIORITY 5
000612 012777 000640 177366 MOV #LK6B,@LKV )SET UP VECTOR RETURN POINTER
000620 012777 000100 177356 MOV #100,@LKS )ENABLE INTERRUPT
000626 005000 CLR X0
000630 005200 LK6AI INC X0
000632 001376 BNE LK6A )WAIT FOR INTERRUPT
000634 000000 HALT )ERROR, INTERRUPT FAILED TO OCCUR
000636 000753 BR LK6
000640 105777 177340 LK6B: TSTB @LKS )ENTER HERE IF INTERRUPTED
000644 100402 BMI LK7
000646 000000 HALT )ERROR, INTERRUPT NOT CAUSED BY CLOCK
000650 000746 BR LK6

)TEST THAT CLOCK WILL NOT INTERRUPT WITH PROCESSOR PRIORITY 6
000652 005077 177326 LK7I CLR @LKS
000656 105777 177322 TSTB @LKS
000662 100375 BPL ,=4 )SYNC CLOCK
000664 012706 002124 MOV #BUFF,X6
000670 012767 000300 177100 MOV #300,CC )SET PRIORITY 6
000676 012777 000726 177302 MOV #LK7B,@LKV )SET UP VECTOR RETURN
000704 012777 000100 177272 MOV #100,@LKS )ENABLE INTERRUPT
000712 105777 177266 LK7AI TSTB @LKS
000716 100375 BPL LK7A )WAIT FOR NEXT CLOCK FLAG
000720 000240 NOP
000722 000240 NOP )GIVE CLOCK EXTRA TIME TO INTERRUPT
000724 000402 BR LK8
000726 000000 HALT )ERROR, CLOCK INTERRUPTED WITHOUT HAVING PRIORITY
000730 000750 BR LK7

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)TEST THAT CLOCK WILL NOT INTERRUPT WITH PROCESSR AT PRIORITY 7
000732 005077 177246 LK8I CLR @LKS
000736 105777 177242 TSTB @LKS
000742 100375 BPL ,=4 ;SYNC CLOCK

000744 012706 002124 MOV #BUFF,X6
000750 012767 000340 177020 MOV #340,CC ;SET PRIORITY 7
000756 012777 001006 177222 MOV #LK8B,@LKV ;SET UP VECTOR RETURN
000764 012777 000100 177212 MOV #100,@LKS ;ENABLE INTERRUPT
000772 105777 177206 LK8AI TSTB @LKS
000776 100375 BPL LK8A ;WAIT FOR NEXT CLOCK FLAG
001000 000240 NOP
001002 000240 NOP ;GIVE CLOCK EXTRA TIME TO INTERRUPT
001004 000402 BR LK9
001006 000000 LK8BI HALT ;ERROR, CLOCK INTERRUPTED WITHOUT HAVING PRIORITY
001010 000750 BR LK8

)TEST THAT CLOCK INTERRUPT PUSHES CONDITION CODES AND PROGRAM COUNTER ONTO STACK
001012 005077 177166 LK9I CLR @LKS
001016 105777 177162 TSTB @LKS
001022 100375 BPL ,=4 ;SYNC CLOCK
001024 012706 002124 MOV #BUFF,X6
001030 005067 001066 CLR BUF1
001034 005067 001060 CLR BUF2
001040 012777 001066 177140 MOV #LK9A,@LKV ;SET UP VECTOR RETURN
001046 012777 000100 177130 MOV #100,@LKS ;ENABLE INTERRUPT
001054 012767 000200 176714 MOV #200,CC ;SET PRIORITY 4
001062 000277 +SEC;SEV;SEZ;ISEN ;SET ALL CONDITION CODES
001064 000001 WAIT ;WAIT FOR INTERRUPT
001066 022767 000217 001026 LK9AI CMP #217,BUF1
001074 001402 BEQ LK9B
001076 000000 HALT ;ERROR DID NOT PUSH CORRECT CC ONTO STACK
001100 000744 BR LK9
001102 022767 001066 001010 LK9BI CMP #LK9A,BUF2
001110 001402 BEQ LK10
001112 000000 HALT ;ERROR, DID NOT PUSH CORRECT PC ONTO STACK
001114 000736 BR LK9

)TEST THAT RESET SETS CLOCK FLAG
001116 005077 177062 LK10I CLR @LKS ;CLEAR CLOCK FLAG
001122 105777 177056 TSTB @LKS
001126 100375 BPL ,=4 ;WAIT FOR CLOCK FLAG
001130 005077 177050 CLR @LKS
001134 000005 RESET ;SHOULD CLEAR CLOCK FLAG
001136 105777 177042 TSTB @LKS
001142 100402 BMI LK11
001144 000000 HALT ;ERROR, RESET DIDN'T CLEAR CLOCK FLAG
001146 000763 BR LK10

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)TEST LINE CLOCK REPEATABILITY
)MAKE SURE THAT OVER TWO EQUAL PERIODS OF TIME
)THE CLOCK PUTS OUT THE SAME NUMBER OF PULSES
001150 005000 LK111 CLR X0 )CLEAR 1ST TIME COUNT
001152 005001 CLR X1 )CLEAR 1ST CLOCK COUNT
001154 012767 000340 176614 MOV #340,CC )SET PRIORITY 7
001162 005077 177016 CLR @LKS
001166 105777 177012 TSTB @LKS
001172 100375 BPL ,=4
001174 005077 177004 CLR @LKS
001200 105777 177000 TSTB @LKS
001204 100375 BPL ,=4 )SYNC CLOCK 2ND TIME TO MAKE SURE
001206 005077 176772 CLR @LKS
001212 105777 176766 LK11A1 TSTB @LKS )IS CLOCK FLAG SET
001216 100003 BPL LK11B )NO
001220 005201 INC X1 )+I TO CLOCK COUNT
001222 005077 176756 CLR @LKS )CLEAR CLOCK IF SET
001226 005200 LK11B1 INC X0 )+I TO TIME COUNT
001230 001370 BNE LK11A )REPEAT UNTIL X0=0
001232 005000 CLR X0 )CLEAR 2ND TIME COUNT
001234 005002 CLR X2 )CLEAR 2ND CLOCK COUNT
001236 005077 176742 CLR @LKS
001242 105777 176736 TSTB @LKS
001246 100375 BPL ,=4
001250 005077 176730 CLR @LKS
001254 105777 176724 TSTB @LKS
001260 100375 BPL ,=4 )SYNC CLOCK 2ND TIME TO MAKE SURE
001262 005077 176716 CLR @LKS
001266 105777 176712 LK11C1 TSTB @LKS )IS CLOCK FLAG SET
001272 100003 BPL LK11D )NO
001274 005202 INC X2 )+I TO CLOCK COUNT
001276 005077 176702 CLR @LKS )CLEAR CLOCK IF SET
001302 005200 LK11D1 INC X0 )+I TO TIME COUNT
001304 001370 BNE LK11C )REPEAT UNTIL X0=0
001306 020102 CMP X1,X2 )IS 1ST CLOCK COUNT EQUAL TO 2ND CLOCK COUNT?
001310 001402 BEQ LK11E )YES
001312 000000 HALT )ERROR, CLOCK FLAG OCCURRED DIFFERENT
001314 000715 BR LK11 )NUMBER OF TIMES IN EQUAL PERIODS

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TEST LINE CLOCK REPEATABILITY WITH INTERRUPT
001316 012767 000200 176452 LK11E1 MOV #200,CC ISET PRIORITY 4
001324 005000 CLR X0 ICLEAR 1ST TIME COUNT
001326 005001 CLR X1 ICLEAR 1ST CLOCK COUNT
001330 012777 001404 176650 MOV #LK11F,@LKV
001336 012767 000300 176536 MOV #300,102
001344 005077 176634 CLR @LKS
001350 105777 176630 TSTB @LKS
001354 100375 BPL ,=4 ISYNC CLOCK
001356 005077 176622 CLR @LKS
001362 105777 176616 TSTB @LKS
001366 100375 BPL ,=4 ISYNC CLOCK 2ND TIME TO MAKE SURE
001370 012777 000100 176606 MOV #100,@LKS IENABLE INTERRUPT
001376 005200 INC X0
001400 001376 BNE ,=2 IWAIT FOR CLOCK INTERRUPTS
001402 000402 BR LK11G
001404 005201 LK11F1 INC X1
001406 000002 RTI
001410 005000 LK11G1 CLR X0 ICLEAR 2ND TIME COUNT
001412 005002 CLR X2 ICLEAR 2ND CLOCK COUNT
001414 012777 001470 176564 MOV #LK11H,@LKV
001422 012767 000300 176452 MOV #300,102
001430 005077 176550 CLR @LKS
001434 105777 176544 TSTB @LKS
001440 100375 BPL ,=4 ISYNC CLOCK
001442 005077 176536 CLR @LKS
001446 105777 176532 TSTB @LKS
001452 100375 BPL ,=4 ISYNC CLOCK SECOND TIME TO MAKE SURE
001454 012777 000100 176522 MOV #100,@LKS IENABLE INTERRUPT
001462 005200 INC X0
001464 001376 BNE ,=2 IWAIT FOR CLOCK INTERRUPTS
001466 000402 BR LK11J
001470 005202 LK11H1 INC X2
001472 000002 RTI
001474 020102 LK11J1 CMP X1,X2 IIS 1ST CLOCK COUNT EQUAL TO 2ND CLOCK COUNT
001476 001402 BEQ LK12 IYES
001500 000000 HALT IERROR, CLOCK INTERRUPT OCCURRED DIFFERENT
001502 000705 BR LK11E INUMBER OF TIMES IN EQUAL PERIODS
  
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ITEST CLOCK ACCURACY
IRING BELL AFTER EACH OF FIRST(5) 1 SECOND INTERVALS
IRING BELL AFTER 10 SECOND INTERVAL
001504 012706 002124 LK12I MOV #BUFF,X6
001510 016700 176500 MOV SEC1,X0
001514 004767 000152 JSR X7,TIME IBELL AFTER 1 SECOND
001520 016700 176470 MOV SEC1,X0
001524 004767 000142 JSR X7,TIME IBELL AFTER 2 SEC.
001530 016700 176460 MOV SEC1,X0
001534 004767 000132 JSR X7,TIME IBELL AFTER 3 SEC.
001540 016700 176450 MOV SEC1,X0
001544 004767 000122 JSR X7,TIME IBELL AFTER 4 SEC.
001550 016700 176440 MOV SEC1,X0
001554 004767 000112 JSR X7,TIME IBELL AFTER 5 SEC
001560 016700 176432 MOV SEC5,X0
001564 004767 000102 JSR X7,TIME IBELL AFTER 10 SEC
IRING BELL AT 10 SECOND INTERVALS ALTERNATING BETWEEN INTERRUPT AND NON INTERRUPT MODES
001570 012703 177775 MOV #=3,X3
001574 016700 176420 LK12AI MOV SEC10,X0
001600 004767 000066 JSR X7,TIME
001604 005203 INC X3
001606 001011 BNE LK12B
001610 013702 000042 MOV #42,X2
001614 001405 BEQ GOAGN
001616 000005 RESET
001620 004712 LOGICI JSR X7,(2)
001622 000240 NOP
001624 000240 NOP
001626 000240 NOP
001630 000725 GOAGNI BR LK12
IRING BELL AFTER 10 SECONDS USING CLOCK FLAG (NON INTERRUPT)
001632 016700 176362 LK12BI MOV SEC10,X0
001636 005077 176342 LK12CI CLR @LKS ICLEAR CLOCK FLAG
001642 105777 176336 TSTB @LKS IWAIT FOR CLOCK FLAG
001646 100375 BPL ,=4
001650 005200 INC X0 IFINISHED 10 SECONDS?
001652 001371 BNE LK12C INO
001654 105777 176330 TSTB @TCSR IYES, RING BELL
001660 100375 BPL ,=4
001662 012777 000207 176322 MOV #207,@TOBR
001670 000741 BR LK12A IRING BELL EVERY 10 SECONDS

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ITHIS ROUTINE RINGS BELL AT INTERVAL DETERMINED BY REGISTER 0
001672 012777 001720 176306 TIME1 MOV #TIME2,0LKV ;SET UP VECTOR RETURN
001700 012767 000200 176070 MOV #200,CC ;SET PROCESSOR PRIORITY 4
001706 012777 000100 176270 TIME11 MOV #100,0LKS ;ENABLE INTERRUPT
001714 000001 WAIT ;WAIT FOR INTERRUPT
001716 000773 BR TIME1 ;AFTER SERVICING INTERRUPT RETURN HERE
001720 005200 TIME21 INC X0 ;TEST FOR COUNT DONE
001722 001401 BEQ ,+4 ;YES
001724 000002 RTI ;NO, WAIT FOR NEXT INTERRUPT
001726 105777 176256 TSTB @TCSR
001732 100375 BPL ,=4
001734 012777 000207 176250 MOV #207,@DDBR ;RING BELL
001742 022626 CMP (6)+,(6)+
001744 000207 RTS X7
001746 012737 001756 000024 PWR11 MOV #PWRUP,0#24
001754 000000 HALT
001756 012706 002124 PWRUP1 MOV #BUFF,X6
001762 012737 001746 000024 MOV #PWR1,0#24
001770 012702 002126 MOV #MSG1,X2
001774 105777 176210 TYPE1 TSTB @TCSR
002000 100375 BPL TYPE
002002 112277 176204 MOVB (2)+,@DDBR
002006 105712 TSTB (2)
002010 001371 BNE TYPE
002012 000005 RESET
002014 000167 176300 JMP LKTEST
002020 000000 TERMNL1 0
002120 000000 ,TERMNL+100
002122 000000 BUF21 0
002124 000000 BUF11 0
002126 005015 042522 052123 BUF11 0
002134 051101 044524 043516 BUF11 0
002142 040440 052106 051105 MSG11 0
002150 040440 050040 053517 ,ASCIZ <15><12>/RESTARTING AFTER A POWER FAILURE/<15><12>
002156 051105 043040 044501
002164 052514 042522 005015
002172 000000
000001 ,END

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BUFF	002124	BUF1	002128	BUF2	002120	CC	177770
CYC50	000222	CYC60	000240	GOAGN	001030	LKS	000204
LKTEST	000320	LKV	000200	LK1	000334	LK10	001116
LK11	001150	LK11A	001212	LK11B	001226	LK11C	001260
LK11D	001302	LK11E	001316	LK11F	001404	LK11G	001410
LK11H	001470	LK11J	001474	LK12	001504	LK12A	001574
LK12B	001032	LK12C	001630	LK2	000346	LK2A	000394
LK3	000372	LK4	000434	LK5	000502	LK5A	000544
LK5B	000554	LK6	000560	LK6A	000630	LK6B	000640
LK7	000652	LK7A	000712	LK7B	000726	LK8	000732
LK8A	000772	LK8B	001000	LK9	001012	LK9A	001060
LK9B	001102	LOGIC	001620	MSG1	002120	NOF	000240
PWRUP	001750	PWR1	001740	SEC1	000214	SEC10	000220
SEC5	000210	START	000270	TCSR	000210	TDBR	000210
TERMNL	002020	TIME	001672	TIME1	001700	TIME2	001720
TYPE	001774		002173				

ERRORS DETECTED: 0

MAJDEC-11-DEKWA-A LINE FREQUENCY CLOCK TEST MACY11,616 10-MAY-72 10109 PAGE 11
DEKWA, P11

*DEKWA, DEKWA, DEKWA/SOL
RUN-TIME 1 3 0 SECONDS
CORE USED 1 3K