IDENTIFICATION

PRODUCT CODE:	MAINDEC-11-DCKBH-A1-D
PRODUCT NAME:	11/45 REGISTERS TEST
DATE CREATED:	15 MAR 1972
MAINTAINER:	DIAGNOSTIC GROUP
AUTHOR:	JOHN ADAMS

COPYRIGHT(c) 1972
DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASS

1,0 ABSTRACT

THIS IS A TEST OF ALL THE 11/45 HARDWARE REGISTERS (R10-15, SUPERVISOR STACK POINTER(R16), USER STACK POINTER(R17), AND THE MICRO BREAK REGISTER, THIS TEST INSURES THAT ALL BITS IN EACH OF THE REGISTERS CAN BE SET AND CLEARED PROPERLY,

2,0 REQUIREMENTS

2,1 EQUIPMENT
BASIC 11/45 SYSTEM

2,2 STORAGE
THIS PROGRAM USES 0 THRU 17500

2,3 PRELIMINARY PROGRAMS
00AA THRU 00MA

3,0 LOADING PROCEDURE
LOAD PROGRAM USING ABS LOADER

4,0 STARTING PROCEDURE
LOAD ADDRESS 200, PRESS START, THE PROGRAM WILL LOOP AND RING BELL ON PASS COMPLETION,

5,0 OPERATING PROCEDURE

5,1 SWITCH SETTINGS
NONE

5,2 SUBROUTINE ABSTRACTS

5,2,1 SCOPE
SCOPE IS A MOVE PC,R1 AND STORES THE PC+2 IN R1,

5,2,2 HLT
HLT IS A HALT INSTRUCTION,

6,0 ERRORS
ALL ERRORS WILL CAUSE A HALT
TRAP AND INTERRUPT ERRORS WILL CAUSE A HALT AT VECTOR+2,

6,1 ERROR RECOVERY
PRESS CONTINUE TO PROCEDE TO NEXT TEST

6,2 ERROR LOOPING
TO LOOP ON AN ERROR, PLACE A BRANCH TO THE PREVIOUS SCOPE INSTRUCTION IN PLACE OF THE HALT INSTRUCTION,
NOTE THAT IF THE ERROR IS INTERMITTANT THAT THE TEST WILL DROP THRU THE HALT AND PROCEED TO THE NEXT TEST,
THEREFORE, TO LOOP THE TEST CONTINUOSLY REPLACE THE RED '+' INSTRUCTION IMMEDIATLY PRECEEDING THE HALT WITH A BRANCH BACK TO THE PREVIOUS SCOPE,

TO LOOP ON TRAP FAILURES, PATCH IN THE FOLLOWING ROUTINE AT THE ADDRESS OF THE TRAP VECTOR,

```
TRAPVEC:        TRAPVEC+4
TRAPVEC+2:      0
TRAPVEC+4:      012716  ;MOVE SCOPE ADDRESS TO STACK
TRAPVEC+6:      ADDRESS ;ADDRESS OF PREVIOUS SCOPE
```

```
        TRAPVEC+10;     000006  ;RETURN TO TEST AT SCOPE

        RESTORE ALL LOCATIONS BEFORE PROCEEDING TO NEXT TEST.

7,0     RESTRICTIONS
        NONE

8,0     MISCELLANEOUS
        ON TRAP ERRORS THE STACK POINTER(R6) WILL CONTAIN THE
        ADDRESS WHERE THE TRAP OCCURED.

8,1     EXECUTION TIME
        THIS PROGRAM TAKES ABOUT 1 MINUTE.

8,2     STACK POINTER
        THIS PROGRAM INITIALY SETS THE STACK POINTER AT 500.
```

```
                                ;TITLE  MAINDEC-11-DCKBH-A ALL PDP11/45 REGISTERS
                                ;NLIST  MC,MD,SEQ
                                ;LIST   ME
                                ;ABS
                        ;TEST DCKBHA- THIS DIAGNOSTIC TESTS THAT ALL BITS IN THE NEW 11/45 REGISTERS
                        ;R10-R15, SUPERVISOR & USER STACK POINTER (SSP & USP), AND MICRO BREAK REGISTER
                        ;CAN BE SET AND CLEARED, AND ARE SELECTED PROPERLY.
                        ;NOTE! ALL PREREQUISITE INSTRUCTION TESTS SHOULD BE SUCCESSFULLY RUN
                        ;BEFORE THIS PROGRAM.
                        ;NOTE!  R0-R7 REFERS TO CONVENTIONAL (11/22) REGISTERS AND R10-R17 REFERS TO
                        ;ADDITIONAL 11/45 REGISTERS, KSP,SSP,AND USP REFER TO THE KERNEL,SUPERVISOR,
                        ;AND USER STACK POINTERS.
                        ;STARTING PROCEEDURE
                        ;       LOAD ADDRESS=200
                        ;       PRESS START
                        ;       KERNEL STACK POINTER IS AT 500
                        ;       SUPERVISOR STACK POINTER IS AT 600
                        ;       USER STACK POINTER IS AT 700
                        ;       BELL WILL RING WHEN TEST IS COMPLETE

                        ;REGISTER IDENTIFIERS THESE BITS IDENTIFY EACH REGISTER
000001                  BIT0=1                          ;REGISTER 0 IDENT
000002                  BIT1=2                          ;   "     1   "
000004                  BIT2=4                          ;   "     2   "
000010                  BIT3=10                         ;   "     3   "
000020                  BIT4=20                         ;   "     4   "
000040                  BIT5=40                         ;   "     5   "
000100                  BIT6=100                        ;   "     6   "
000200                  BIT7=200                        ;   "     7   "

                        ;UPPER SET
000400                  BIT8=400                        ;REGISTER 10 IDENT
001000                  BIT9=1000                       ;   "     11   "
002000                  BIT10=2000                      ;   "     12   "
004000                  BIT11=4000                      ;   "     13   "
010000                  BIT12=10000                     ;   "     14   "
020000                  BIT13=20000                     ;   "     15   "
040000                  BIT14=40000                     ;   "     16   "
100000                  BIT15=100000                    ;   "     17   "

000000                  R0=%0
000001                  R1=%1
000002                  R2=%2
000003                  R3=%3
000004                  R4=%4
000005                  R5=%5
000006                  R6=%6
000007                  R7=%7
000006                  SP=%6
000006                  KSP=%6                          ;KERNEL'S STACK POINTER
000006                  SSP=%6                          ;SUPERVISOR'S STACK POINTER
000006                  USP=%6                          ;USER'S STACK POINTER
000007                  PC=%7
```



```
000020                  R10=%0
000001                  R11=%1
000002                  R12=%2
000003                  R13=%3
000004                  R14=%4
000005                  R15=%5
000006                  R16=%6
000007                  R17=%7

000500                          KPTR=500                ;KERNEL'S INITIAL STACK POINTER
000600                          SPTR=600                ;SUPERVISOR'S INITIAL STACK POINTER
000700                          UPTR=700                ;USER'S INITIAL STACK POINTER
                        ;REGISTER ADDRESSES
177570                          DISPLAY=177570          ;ADDRESS OF CONSOLE DISPLAY  REGISTER
177776                          PSW=177776              ;ADDRESS OF PROCESSER STATUS WORD
177770                          UBREAK=177770           ;ADDRESS OF MICRO BREAK REGISTER
177564                          TPCSR=177564
177566                          TPBUF=177566
177570                          SWR=177570              ;ADDRESS OF CONSOLE SWITCH REGISTER
022626                          POP2=22626              ;CMP (6)+,(6)+ POPS 2 WORDS OFF STACK
010701                          SCOPE=010701            ;MOV  PC,R1 (R11)
000000                          HLT=0
                        ;VECTOR ADDRESSES
000004                          ERRVEC=4                ;ADDRESS OF ERROR TRAP VECTOR
000014                          TBITVEC=14              ;ADDRESS OF 'T' BIT TRAP VECTOR
000030                          EMTVEC=30               ;ADDRESS OF EMT TRAP VECTOR
000034                          TRAPVEC=34              ;ADDRESS OF TRAP TRAP VECTOR
                        ;BIT ASSIGNMENTS IN PSW
000000                          KM=0                    ;KERNEL MODE
040000                          SM=40000                ;SUPERVISORY MODE
140000                          UM=140000               ;USER MODE


000000                          .=0
000000  000002                  .+2
000002  000000                  HALT
000004  000006                  .+2
000006  000000                  HALT
000010  000012                  .+2
000012  000000                  HALT
000014  000016                  .+2
000016  000000                  HALT
000020  000022                  .+2
000022  000000                  HALT
000024  000026                  .+2
000026  000000                  HALT
000030  000032                  .+2
000032  000000                  HALT
000034  000036                  .+2
000036  000000                  HALT
000040  000042                  .+2
000042  000000                  HALT
000044  000046                  .+2
```

```
000046  000000          HALT
000050  000052          ,+2
000052  000000          HALT
000054  000056          ,+2
000056  000000          HALT
000060  000062          ,+2
000062  000000          HALT
000064  000066          ,+2
000066  000000          HALT
000070  000072          ,+2
000072  000000          HALT
000074  000076          ,+2
000076  000000          HALT
000100  000102          ,+2
000102  000000          HALT
000104  000106          ,+2
000106  000000          HALT
000110  000112          ,+2
000112  000000          HALT
000114  000116          ,+2
000116  000000          HALT
000120  000122          ,+2
000122  000000          HALT
000124  000126          ,+2
000126  000000          HALT
000130  000132          ,+2
000132  000000          HALT
000134  000136          ,+2
000136  000000          HALT
000140  000142          ,+2
000142  000000          HALT
000144  000146          ,+2
000146  000000          HALT
000150  000152          ,+2
000152  000000          HALT
000154  000156          ,+2
000156  000000          HALT
000160  000162          ,+2
000162  000000          HALT
000164  000166          ,+2
000166  000000          HALT
000170  000172          ,+2
000172  000000          HALT
000174  000176          ,+2
000176  000000          HALT
000200  000202          ,+2
000202  000000          HALT
000204  000206          ,+2
000206  000000          HALT
000210  000212          ,+2
000212  000000          HALT
000214  000216          ,+2
000216  000000          HALT
000220  000222          ,+2
```



```
000222  000000          HALT
000224  000226          ,+2
000226  000000          HALT
000230  000232          ,+2
000232  000000          HALT
000234  000236          ,+2
000236  000000          HALT
000240  000242          ,+2
000242  000000          HALT
000244  000246          ,+2
000246  000000          HALT
000250  000252          ,+2
000252  000000          HALT
000254  000256          ,+2
000256  000000          HALT
000260  000262          ,+2
000262  000000          HALT
000264  000266          ,+2
000266  000000          HALT
000270  000272          ,+2
000272  000000          HALT
000274  000276          ,+2
000276  000000          HALT
000300  000302          ,+2
000302  000000          HALT
000304  000306          ,+2
000306  000000          HALT
000310  000312          ,+2
000312  000000          HALT
000314  000316          ,+2
000316  000000          HALT
000320  000322          ,+2
000322  000000          HALT
000324  000326          ,+2
000326  000000          HALT
000330  000332          ,+2
000332  000000          HALT
000334  000336          ,+2
000336  000000          HALT
000340  000342          ,+2
000342  000000          HALT
000344  000346          ,+2
000346  000000          HALT
000350  000352          ,+2
000352  000000          HALT
000354  000356          ,+2
000356  000000          HALT
000360  000362          ,+2
000362  000000          HALT
000364  000366          ,+2
000366  000000          HALT
000370  000372          ,+2
000372  000000          HALT
000374  000376          ,+2
```

```
000376  000000                  HALT


        000200
000200  000167  000624          JMP     START

        001000
001000  000000          ICNT10  .WORD   0                       ;PASS COUNT
001002  000000          TEMP10  .WORD   0
        001010                  .=.+4
001010  005067  177764  START1  CLR     ICNT
001014  716737  177760  177570  BEGIN1  MOV     ICNT,@#DISPLAY  ;DISPLAY PASS COUNT
001022  012706  000500          MOV     #KPTR,KSP       ;INITIALIZE THE STACK POINTER
001026  032737  000400  177570  BIT     #400,@#SWR      ;LOAD MICRO BREAK REGISTER?
001034  001403                  BEQ     .+10
001036  113737  177570  177770  MOVB    @#SWR,@#UBREAK  ;LOAD MICRO BREAK REG WITH SP0-7
001044  005067  176726          CLR     PSW
                        ;LOAD EACH REGISTER WITH ITS IDENTIFIER

001050  012700  000001  T01     MOV     #BIT0,R0
001054  012701  000002          MOV     #BIT1,R1
001060  012702  000004          MOV     #BIT2,R2
001064  012703  000010          MOV     #BIT3,R3
001070  012704  000020          MOV     #BIT4,R4
001074  012705  000040          MOV     #BIT5,R5
001100  012767  004000  176670  MOV     #BIT11,PSW      ;SET REGISTER SET BIT
001106  012700  000400          MOV     #BIT8,R10
001112  012701  001000          MOV     #BIT9,R11
001116  012702  002000          MOV     #BIT10,R12
001122  012703  004000          MOV     #BIT11,R13
001126  012704  010000          MOV     #BIT12,R14
001132  012705  020000          MOV     #BIT13,R15

001136  005067  176634          CLR     PSW             ;SWITCH TO CONVENTIONAL REGISTERS
                                ..
```



```
                        ;TEST THAT ALL REGISTERS WERE PROPERLY LOADED
001142  022700  000001          CMP     #BIT0,R0
001146  001401                  BEQ     .+4
001150  000000                  HLT
001152  022701  000002          CMP     #BIT1,R1
001156  001401                  BEQ     .+4
001160  000000                  HLT
001162  022702  000004          CMP     #BIT2,R2
001166  001401                  BEQ     .+4
001170  000000                  HLT
001172  022703  000010          CMP     #BIT3,R3
001176  001401                  BEQ     .+4
001200  000000                  HLT
001202  022704  000020          CMP     #BIT4,R4
001206  001401                  BEQ     .+4
001210  000000                  HLT
001212  022705  000040          CMP     #BIT5,R5
001216  001401                  BEQ     .+4
001220  000000                  HLT
001222  022706  000500          CMP     #KPTR,KSP
001226  001401                  BEQ     .+4
001230  000000                  HLT
                        ;SWTICH TO UPPER REGISTERS
001232  012767  004000  176536  MOV     #BIT11,PSW
001240  022700  000400          CMP     #BIT8,R10
001244  001401                  BEQ     .+4
001246  000000                  HLT
001250  022701  001000          CMP     #BIT9,R11
001254  001401                  BEQ     .+4
001256  000000                  HLT
001260  022702  002000          CMP     #BIT10,R12
001264  001401                  BEQ     .+4
001266  000000                  HLT
001270  022703  004000          CMP     #BIT11,R13
001274  001401                  BEQ     .+4
001276  000000                  HLT
001300  022704  010000          CMP     #BIT12,R14
001304  001401                  BEQ     .+4
001306  000000                  HLT
001310  022705  020000          CMP     #BIT13,R15
001314  001401                  BEQ     .+4
001316  000000                  HLT
                        ;R7 CHECK
001320  012727  001330          MOV     #T0X,R17
001324  000000                  HLT
001326  000000                  HLT
```

```
001330  005067  176442          T2X:    CLR     PSW
001334  012721                          SCOPE

                                ;CHECK THAT ALL BITS IN R10 CAN BE SET/CLEARED,
001336  012767  004000  176432  A2:     MOV     #BIT11,PSW
001344  012767  000020  177432          MOV     #20,TEMP+2
001352  012720  000001                  MOV     #1,R10
001356  010067  177420                  MOV     R10,TEMP
001362  006367  177414          A0A:    ASL     TEMP
001366  006320                          ASL     R10
001370  020067  177406                  CMP     R10,TEMP
001374  001401                          BEQ     .+4
001376  000000                          HLT
001400  005367  177400                  DEC     TEMP+2
001404  001366                          BNE     A0A
001406  010701                          SCOPE

                                ;CHECK THAT ALL BITS IN R11 CAN BE SET/CLEARED,
001410  012767  004000  176360  A1:     MOV     #BIT11,PSW
001416  012767  000020  177360          MOV     #20,TEMP+2
001424  012701  000001                  MOV     #1,R11
001430  010167  177346                  MOV     R11,TEMP
001434  006367  177342          A1A:    ASL     TEMP
001440  006321                          ASL     R11
001442  020167  177334                  CMP     R11,TEMP
001446  001401                          BEQ     .+4
001450  000000                          HLT
001452  005367  177326                  DEC     TEMP+2
001456  001366                          BNE     A1A
001460  010701                          SCOPE

                                ;CHECK THAT ALL BITS IN R12 CAN BE SET/CLEARED,
001462  012767  004000  176306  A2:     MOV     #BIT11,PSW
001470  012767  000020  177306          MOV     #20,TEMP+2
001476  012702  000001                  MOV     #1,R12
001502  010267  177274                  MOV     R12,TEMP
001506  006367  177270          A2A:    ASL     TEMP
001512  006322                          ASL     R12
001514  020267  177262                  CMP     R12,TEMP
001520  001401                          BEQ     .+4
001522  000000                          HLT
001524  005367  177254                  DEC     TEMP+2
001530  001366                          BNE     A2A
001532  010701                          SCOPE

                                ;CHECK THAT ALL BITS IN R13 CAN BE SET/CLEARED,
001534  012767  004000  176234  A3:     MOV     #BIT11,PSW
001542  012767  000020  177234          MOV     #20,TEMP+2
001550  012703  000001                  MOV     #1,R13
001554  010367  177222                  MOV     R13,TEMP
001560  006367  177216          A3A:    ASL     TEMP
001564  006323                          ASL     R13
001566  020367  177210                  CMP     R13,TEMP
```



```
001572  001401                          BEQ     .+4
001574  000000                          HLT
001576  005367  177202                  DEC     TEMP+2
001602  001366                          BNE     A3A
001604  010701                          SCOPE

                                ;CHECK THAT ALL BITS IN R14 CAN BE SET/CLEARED,
001606  012767  004000  176162  A4:     MOV     #BIT11,PSW
001614  012767  000020  177162          MOV     #20,TEMP+2
001622  012704  000001                  MOV     #1,R14
001626  010467  177150                  MOV     R14,TEMP
001632  006367  177144          A4A:    ASL     TEMP
001636  006324                          ASL     R14
001640  020467  177136                  CMP     R14,TEMP
001644  001401                          BEQ     .+4
001646  000000                          HLT
001650  005367  177130                  DEC     TEMP+2
001654  001366                          BNE     A4A
001656  010701                          SCOPE

                                ;CHECK THAT ALL BITS IN R15 CAN BE SET/CLEARED,
001660  012767  004000  176110  A5:     MOV     #BIT11,PSW
001666  012767  000020  177110          MOV     #20,TEMP+2
001674  012705  000001                  MOV     #1,R15
001700  010567  177076                  MOV     R15,TEMP
001704  006367  177072          A5A:    ASL     TEMP
001710  006325                          ASL     R15
001712  020567  177064                  CMP     R15,TEMP
001716  001401                          BEQ     .+4
001720  000000                          HLT
001722  005367  177056                  DEC     TEMP+2
001726  001366                          BNE     A5A
001730  010701                          SCOPE


001732  012767  004000  176036          MOV     #BIT11,PSW
001740  012720  000400                  MOV     #BIT8,R10
001744  012721  001000                  MOV     #BIT9,R11
001750  012722  002000                  MOV     #BIT10,R12
001754  012723  004000                  MOV     #BIT11,R13
001760  012724  010000                  MOV     #BIT12,R14
001764  012725  020000                  MOV     #BIT13,R15
001770  005067  176002                  CLR     PSW
001774  010701                          SCOPE

001776  012767  004000  175772  T1:     MOV     #BIT11,PSW      ;GO UPPER SET
002004  010067  175766          T1A:    MOV     R0,PSW          ;MOVE BIT8 TO PSW (SWITCHES
002010  016767  175762  176764          MOV     PSW,TEMP        ;TO 11/20 REGS,)
002016  032767  000001  175756          BIT     #BIT7,TEMP      ;WAS CORRECT %0 LOADED IN PSW
002024  001401                          BEQ     .+4             ;IF BIT 7 WAS SET 11/20 REG *
002026  000000                          HLT                     ;WAS INCORRECTLY SELECTED
002030  005767  176746                  TST     TEMP            ;IF TRULY R1? PSW WILL BE
002034  001401                          BEQ     .+4             ;CLEAR
002036  000000                          HLT                     ;ERROR! DID INST AT T1A CLR PSW?
```

```
002040  012701                          SCOPE

002042  012767  004000  175726  T2:     MOV     #BIT11,PSW
002050  012067  175722                  MOV     R10,PSW         ;SEL 11/22 REGS.
002054  012067  175716                  MOV     R0,PSW          ;MOVE BIT0 TO PSW (SETS C)
002060  103401                          BCS     .+4             ;IS CARRY SET?
002062  000000                          HLT                     ;R0 NOT SELECTED
002064  010701                          SCOPE

002066  012767  004000  175702  T3:     MOV     #BIT11,PSW
002074  040367  175676                  BIC     R13,PSW         ;CLEAR BIT11 IN PSW
002100  010267  175672                  MOV     R2,PSW          ;MOVE BIT1 TO PSW
002104  016767  175666  176670          MOV     PSW,TEMP
002112  022767  000004  176662          CMP     #BIT2,TEMP
002120  001401                          BEQ     .+4
002122  000000                          HLT
002124  010701                          SCOPE

002126  012767  004000  175642  T4:     MOV     #BIT11,PSW
002134  160367  175636                  SUB     R13,PSW
002140  074267  175632                  XOR     R2,PSW
002144  016767  175626  176630          MOV     PSW,TEMP
002152  022767  000004  176622          CMP     #BIT2,TEMP
002160  001401                          BEQ     .+4
002162  000000                          HLT
002164  010701                          SCOPE
002166  012767  004000  175602  T5:     MOV     #BIT11,PSW
002174  074367  175576                  XOR     R13,PSW
002200  074367  175572                  XOR     R3,PSW
002204  016767  175566  176570          MOV     PSW,TEMP
002212  022767  000010  176562          CMP     #BIT3,TEMP
002220  001401                          BEQ     .+4
002222  000000                          HLT
002224  010701                          SCOPE

002226  012767  004000  175542  T6:     MOV     #BIT11,PSW
002234  012767  002276  175552          MOV     #T6A,TBITVEC
002242  005067  175550                  CLR     TBITVEC+2
002246  052767  000020  175522          BIS     #BIT4,PSW       ;ATTEMPT TO SET 'T' BIT
002254  016767  175516  176520          MOV     PSW,TEMP
002262  022767  004004  176512          CMP     #BIT11+BIT2,TEMP;'T' BIT SHOULD NOT HAVE SET
002270  001404                          BEQ     T6X             ;'Z' WAS SET BY CLR TBITVEC+2 INST.
002272  000000                          HLT                     ;ERROR! ONLY BIT11 & Z SHOULD BE SET
002274  000402                          BR      T6X
002276  000000                  T6A:    HLT                     ;ERROR! 'T' BIT CAUSED A TRAP
002300  022626                          POP2
002302  010701                  T6X:    SCOPE

002304  012767  002344  175502  T7:     MOV     #T7A,TBITVEC
002312  012767  004000  175456          MOV     #BIT11,PSW
002320  012705  004020                  MOV     #BIT11+BIT4,R15
002324  074567  175446                  XOR     R15,PSW
002330  016767  175442  176444          MOV     PSW,TEMP
002336  001404                          BEQ     T7X
```



```
002340  000000                          HLT
002342  000402                          BR      T7X
002344  000000                  T7A:    HLT
002346  022626                          POP2
002350  012767  000016  175436  T7X:    MOV     #16,14
002356  010701                          SCOPE

002360  012767  004000  175410  T10:    MOV     #BIT11,PSW
002366  012705  004000                  MOV     #BIT11,R15
002372  074567  175400                  XOR     R15,PSW
002376  074567  175374                  XOR     R5,PSW
002402  016767  175370  176372          MOV     PSW,TEMP
002410  022767  000040  176364          CMP     #BIT5,TEMP
002416  001401                          BEQ     .+4
002420  000000                          HLT
002422  010701                          SCOPE

002424  012767  004000  175344  T11:    MOV     #BIT11,PSW
002432  005000                          CLR     R10
002434  010067  176342                  MOV     R10,TEMP
002440  001401                          BEQ     .+4
002442  000000                          HLT
002444  010701                          SCOPE

002446  012767  004000  175322  T12:    MOV     #BIT11,PSW
002454  005000                          CLR     R10
002456  012767  000200  176316          MOV     #BIT7,TEMP
002464  116700  176312                  MOVB    TEMP,R10                ;MOVB TO A REG, EXTENDS SIGN
002470  020027  177600                  CMP     R10,#177600     ;DID SIGN EXTEND
002474  001401                          BEQ     .+4
002476  000000                          HLT
002500  012700  000400                  MOV     #BIT8,R10
002504  010701                          SCOPE

002506  012767  004000  175262  T13:    MOV     #BIT11,PSW
002514  012701  177777                  MOV     #-1,R11
002520  010167  176256                  MOV     R11,TEMP
002524  026727  176252  177777          CMP     TEMP,#-1
002532  001401                          BEQ     .+4
002534  000000                          HLT
002536  010701                          SCOPE

                                ;TEST THAT MOVB TO A REGISTER EXTENDS THE SIGN (SIGN = 0)
002542  012767  004000  175230  T14:    MOV     #BIT11,PSW
002546  012701  177777                  MOV     #-1,R11
002552  012767  017777  176222          MOV     #17777,TEMP
002560  116701  176217                  MOVB    TEMP+1,R11
002564  022701  000037                  CMP     #37,R11
002570  001401                          BEQ     .+4
002572  000000                          HLT
002574  012701  001000                  MOV     #BIT9,R11
002600  010701                          SCOPE

                                ;TEST THAT XOR %9,%R OPERATES PROPERLY
```

```
022672  012767  024000  175166  T15:    MOV     #BIT11,PSW
022610  074273                          XOR     R12,R13
022612  013767  176164                  MOV     R13,TEMP
022616  024727  176162  020000          CMP     TEMP,#BIT15+BIT11
022624  001401                          BEQ     .+4
022626  000000                          HLT
022630  012703  024000                  MOV     #BIT11,R13
022634  010701                          SCOPE

                                ;TEST SOR WITH UPPER REGISTER SET
022636  012767  024000  175132  T16:    MOV     #BIT11,PSW
022644  012704  000001                  MOV     #1,R14
022650  000422                          BR      T16B
022652  000000                  T16A:   HLT
022654  000401                          BR      T16X
022656  077403                  T16B:   SOR     R14,T16A
022660  012704  012000          T16X:   MOV     #BIT12,R14
022664  010701                          SCOPE

                                ;TEST ADD %R,%R USING UPPER REGISTER SET
022666  060302                  T17:    ADD     R13,R12
022670  010267  176106                  MOV     R12,TEMP
022674  022767  020000  176100          CMP     #BIT10+BIT11,TEMP
022702  001401                          BEQ     .+4
022704  000000                          HLT
022706  012702  002000                  MOV     #BIT10,R12
022712  010701                          SCOPE

                                ;TEST UPPER REGISTER SET (R13) IN AUTO INCREMENT MODE.
022714  005067  176064          T22:    CLR     TEMP+2          ;PRE SET MEMORY ADDRESS
022720  012767  177777  176054          MOV     #-1,TEMP
022726  012767  024000  175042          MOV     #BIT11,PSW      ;SWITCH TO UPPER REG. SET
022734  012703  001002                  MOV     #TEMP,R13       ;LOAD REGISTER
022740  012367  176040                  MOV     (R13)+,TEMP+2   ;MOVE TEMP TO TEMP+2
022744  022767  177777  176032          CMP     #-1,TEMP+2      ;WAS TEMP MOVED
022752  001401                          BEQ     .+4
022754  000000                          HLT                     ;ERROR!
022756  022703  001004                  CMP     #TEMP+2,R13     ;DID R13 INCREMENT
022762  001401                          BEQ     .+4
022764  000000                          HLT                     ;ERROR! R13 DID NOT AUTO-INCREMENT
022766  010701                          SCOPE

                                ;TEST UPPER REG, SET (R14) IN AUTO-DECREMENT MODE
022770  012767  001002  176006  T20A:   MOV     #TEMP,TEMP+2
022776  005067  176000                  CLR     TEMP
023002  012767  024000  174766          MOV     #BIT11,PSW
023010  012704  001006                  MOV     #TEMP+4,R14
023014  014467  175762                  MOV     -(R14),TEMP
023020  022767  001002  175754          CMP     #TEMP,TEMP
023026  001401                          BEQ     .+4
023030  000000                          HLT
023032  022704  001004                  CMP     #TEMP+2,R14     ;DID REGISTER AUTO-DECREMENT
023036  001401                          BEQ     .+4
023040  000000                          HLT
```



```
023042  010701                          SCOPE

                                ;TESTS 21 AND 22 HAVE BEEN DELETED.

                                ;TEST UPPER REGISTER SET REGISTERS AS INDEX REGISTERS
023044  000240                  T23:    NOP                     ;THIS LOCATION MAY BE USED TO CLEAR
                                                                ;REGISTER SET BIT.
023046  012767  001002  175730          MOV     #TEMP,TEMP+2
023054  012767  177777  175720          MOV     #-1,TEMP
023062  012702  177776                  MOV     #-2,R12         ;LOAD INDEX
023066  010225                          MOV     R12,R15         ;REGISTERS
023070  067275  001006  001006          ADD     @TEMP+4(2),@TEMP+4(5)   ;ADD TEMP [(TEMP+4(5)] TO ITSELF
023076  103401                          BCS     .+4             ;-1,+-1 RESULTS IN CARRY
023100  000000                          HLT
023102  022767  177776  175672          CMP     #177776,TEMP    ;RESULT CORRECT
023110  001401                          BEQ     .+4
023112  000000                          HLT
023114  010701                          SCOPE

                                ;TEST THAT ALL THREE STACK POINTERS (KSP,SSP,AND USP CAN BE SELECTED.
023116  012767  000000  174652  T24:    MOV     #KM,PSW         ;KERNEL MODE!!!
023124  012706  000500                  MOV     #KPTR,KSP       ;LOAD KERNEL STACK POINTER
023130  052767  040000  174640          BIS     #SM,PSW         ;SUPERVISORY MODE!!!
023136  012706  000600                  MOV     #SPTR,SSP       ;LOAD SUPERVISOR STACK POINTER
023142  052767  140000  174626          BIS     #UM,PSW         ;USER MODE!!!
023150  012706  000700                  MOV     #UPTR,USP       ;LOAD USER STACK POINTER
023154  010667  175692                  MOV     USP,TEMP        ;GET USER STACK POINTER
023160  042767  100000  174610          BIC     #BIT15,PSW      ;SUPERVISORY MODE!!!
023166  010667  175612                  MOV     SSP,TEMP+2      ;GET SUPERVISOR STACK POINTER
023172  005067  174600                  CLR     PSW             ;KERNEL MODE
023176  022706  000500                  CMP     #KPTR,KSP       ;CHECK KERNEL STACK POINTER
023202  001401                          BEQ     .+4
023204  000000                          HLT                     ;ERROR! KERNEL STACK POINTER NOT LOADED

023206  022767  000600  175570          CMP     #SPTR,TEMP+2    ;CHECK SUPERVISOR STACK POINTER
023214  001401                          BEQ     .+4
023216  000000                          HLT                     ;ERROR! SUPERVISOR STACK NOT LOADED

023220  022767  000700  175554          CMP     #UPTR,TEMP      ;CHECK USER STACK POINTER
023226  001401                          BEQ     .+4
023230  000000                          HLT                     ;ERROR! USER STACK POINTER NOT LOADED
023232  010701                          SCOPE

                                ;TEST THAT JSR INST, OPERATES PROPERLY WITH REG, SET BIT SET
023234  012706  000500          T25:    MOV     #KPTR,KSP       ;INITIALIZE THE STACK POINTER
023240  012700  000001                  MOV     #BIT0,R0        ;PRE SET R0
023244  012767  024000  174594          MOV     #BIT11,PSW      ;SET REG. SET BIT
023252  012700  024000                  MOV     #BIT8,R10       ;PRE SET R10
023256  004467  000002                  JSR     R10,T25B        ;GO TO T25B & SAVE R10 ON THE STACK
023262  000000                  T25A:   HLT                     ;JSR DID NOT GO
023264  022706  000476          T25B:   CMP     #KPTR+2,KSP
023270  001401                          BEQ     .+4             ;STACK POINTER DID NOT DECREMENT
023272  000000                          HLT
023274  022767  000410  175546          CMP     #BIT8,KPTR+2    ;WAS OLD CONTENTS OF R10 SAVED?
```

```
003372  001401                          BEQ     .+4
003374  000000                          HLT                     ;ERROR: R10 NOT SAVED ON THE STACK
003376  022720  003262                  CMP     #T25A,R10       ;IS RETURN ADDRESS IN R10
003402  001401                          BEQ     .+4
003404  000000                          HLT                     ;ERROR: RETURN ADRS. NOT SAVED IN R10
003406  005067  174454                  CLR     PSW
003412  022720  000001                  CMP     #BIT0,R0        ;R0 LEFT UNCHANGED?
003416  001401                          BEQ     .+4
003420  000000                          HLT                     ;R0 GOT CHANGED
003422  012701                          SCOPE

                                ;TEST JSR INSTRUCTION USING UPPER REG SET IN DEST, CALCULATION
003424  012706  000500          T26:    MOV     #KPTR,KSP
003430  012705  000040                  MOV     #BIT5,R5        ;PRE SET R5
003434  012767  004000  174424          MOV     #BIT11,PSW      ;SWITH TO UPPER REG, SET
003442  005005                          CLR     R15             ;PRE SET R15
003444  004565  003362                  JSR     R15,T26B(5)     ;GO TO T26B
003450  000000          T26A:   HLT                             ;ERROR: JSR FAILED
003452  005767  175110          T26B:   TST     KPTR-2          ;OLD CONTENTS OF R15 SAVED?
003456  001401                          BEQ     .+4
003460  000000                          HLT                     ;ERROR: OLD CONTENTS OF R15 NOT SAVED
003462  022705  003360                  CMP     #T26A,R15       ;RETURN ADDRESS IN R15?
003466  001401                          BEQ     .+4
003470  000000                          HLT                     ;ERROR: R15 DID NOT GET RETURN ADDRESS
003472  005067  174370                  CLR     PSW             ;SWITCH TO LOWER REGISTERS
003476  022705  000040                  CMP     #BIT5,R5        ;DID R5 CHANGE?
003502  001401                          BEQ     .+4
003504  000000                          HLT                     ;ERROR: R5 GOT CHANGED
003506  012701                          SCOPE

                                ;TEST RTS WITH UPPER REGISTERS
003510  012706  000500          T27:    MOV     #KPTR,KSP
003514  012716  001000                  MOV     #BIT9,(KSP)
003520  012702  000004                  MOV     #BIT2,R2        ;PRE SET R2
003524  012767  004000  174334          MOV     #BIT11,PSW      ;SWITCH TO UPPER REG, SET
003532  012702  003452                  MOV     #T27A,R12       ;LOAD REG, WITH RETURN ADDRESS
003536  000202                          RTS     R12             ;RETURN TO T27A [(R12)]
003540  000000                          HLT                     ;ERROR: RTS FAILED
003542  022706  000502          T27A:   CMP     #KPTR+2,KSP     ;WAS STACK POINTER INCREMENTED
003546  001401                          BEQ     .+4
003550  000000                          HLT                     ;ERROR: STACK POINTER WAS NOT INCREMENTED
003552  022702  001000                  CMP     #BIT9,R12       ;WAS R12 RESTORED?
003556  001401                          BEQ     .+4
003560  000000                          HLT                     ;ERROR: RTS DID NOT RESTORE R12
003562  005067  174300                  CLR     PSW             ;SWITCH TO LOWER REG, SET
003566  022702  000004                  CMP     #BIT2,R2        ;DID R2 CHANGE?
003572  001401                          BEQ     .+4
003574  000000                          HLT                     ;ERROR: R2 CHANGED
003576  012701                          SCOPE

                                ;CHECK THAT ALL BITS IN KSP CAN BE SET/CLEARED;
003600  012700  000001                  MOV     #1,R0           ;GET '1' BIT
003604  012767  000000  174254  T30:    MOV     #KM,PSW
003612  010006                          MOV     R0,KSP  ;LOAD KSP
```



```
003616  010602                          MOV     KSP,R2  ;GET RESULT
003620  005067  174244                  CLR     PSW             ;KERNEL MODE!!!

003624  020200                          CMP     R2,R0           ;WAS KSP LOADED CORRECTLY?
003626  001401                          BEQ     .+4
003630  000000                          HLT
003632  006300                          ASL     R0              ;SHIFT '1' BIT THRU KSP
003634  103364                          BCC     T30             ;UNTIL ALL BITS ARE TESTED
003636  012701                          SCOPE

                                ;CHECK THAT ALL BITS IN SSP CAN BE SET/CLEARED;
003640  012700  000001                  MOV     #1,R0           ;GET '1' BIT
003644  012767  040000  174216  T31:    MOV     #SM,PSW
003652  010006                          MOV     R0,SSP  ;LOAD SSP
003654  010602                          MOV     SSP,R2  ;GET RESULT
003656  005067  174206                  CLR     PSW             ;KERNEL MODE!!!

003662  020200                          CMP     R2,R0           ;WAS SSP LOADED CORRECTLY?
003664  001401                          BEQ     .+4
003666  000000                          HLT
003670  006300                          ASL     R0              ;SHIFT '1' BIT THRU SSP
003672  103364                          BCC     T31             ;UNTIL ALL BITS ARE TESTED
003674  012701                          SCOPE

                                ;CHECK THAT ALL BITS IN USP CAN BE SET/CLEARED;
003676  012700  000001                  MOV     #1,R0           ;GET '1' BIT
003702  012767  140000  174160  T32:    MOV     #UM,PSW
003710  010006                          MOV     R0,USP  ;LOAD USP
003712  010602                          MOV     USP,R2  ;GET RESULT
003714  005067  174150                  CLR     PSW             ;KERNEL MODE!!!

003720  020200                          CMP     R2,R0           ;WAS USP LOADED CORRECTLY?
003722  001401                          BEQ     .+4
003724  000000                          HLT
003726  006300                          ASL     R0              ;SHIFT '1' BIT THRU USP
003730  103364                          BCC     T32             ;UNTIL ALL BITS ARE TESTED
003732  012701                          SCOPE
```

```
                                        ;CHECK THAT ALL BITS IN THE MICRO BREAK REGISTER (177772) CAN BE SET
                                        ;AND CLEARED
003642  012772  000001          T33:    MOV     #1,R0
003646  012772  177772                  MOV     #UBREAK,R2      ;GET ADDRESS OF MICRO BREAK REGISTER
003652  010012                 T33A:   MOV     R0,(R2)         ;LOAD TEST BIT INTO REGISTER
003654  011203                         MOV     (R2),R3         ;GET RESULT
003656  020003                         CMP     R0,R3           ;COMPARE RESULT & TEST BIT
003660  001401                         BEQ     .+4
003662  000000                         HLT                     ;ERROR! TEST BIT (R2) DID NOT SET INTO
                                                                ;REGISTER
003664  040012                         BIC     R0,(R2)         ;CLEAR TEST BIT IN REGISTER
003666  011203                         MOV     (R2),R3         ;GET RESULT
003670  001401                         BEQ     .+4
003672  000000                         HLT                     ;ERROR! TEST BIT DID NOT GET CLEARED
003674  106300                         ASLB    R0              ;SHIFT TEST BIT UNTIL DONE
003676  103365                         BCC     T33A
003700  010701                         SCOPE

                                        ;CHECK THAT RESET DOES NOT CLEAR MICRO BREAK REGISTER
003702  012737  177777  177770 T34:    MOV     #-1,@#UBREAK    ;SET ALL 1'S INTO REGISTER
003710  122737  177777  177770         CMPB    #-1,@#UBREAK    ;CHECK RESULT
003716  001401                         BEQ     .+4
003720  000000                         HLT                     ;ERROR!
003722  000005                         RESET                   ;RESET DOES NOT CLEAR REGISTER
003724  122737  177777  177770         CMPB    #-1,@#UBREAK    ;CHECK THAT RESET DID NOT CLEAR ANY BITS
003732  001401                         BEQ     .+4
003734  000000                         HLT                     ;ERROR!
003736  010701                         SCOPE

003740  005267  175034          END:    INC     ICNT            ;INCREMENT PASS COUNT
003744  026727  175030  001000         CMP     ICNT,#1000      ;1000 PASSES?
003752  001402                         BEQ     DONE
003754  000167  175034                 JMP     BEGIN
003760  012767  000007  173600 DONE:   MOV     #7,TPSUF        ;RING THE BELL
003766  105767  173572                 TSTB    TPCSR           ;WAIT FOR THE BELL
003772  100375                         BPL     .-4             ;TO RING
003774  013702  000042                 MOV     @#42,%2         ;GET DECTAPE MONITOR RETURN ADDRESS
004000  001404                         BEQ     DONE1           ;DO NOT RETURN IF (42)=0
004002  004712                         JSR     7,(2)           ;RETURN TO DECTAPE MONITOR
004004  000240                         NOP                     ;ACT11
004006  000240                         NOP                     ;OVERLAY
004010  000240                         NOP                     ;AREA
004012  000167  174772         DONE1:  JMP     START           ;RESTART TEST

        000001                          .END
```



```
A0      001336  A0A     001362  A1      001410  A1A     001434
A2      001462  A2A     001506  A3      001534  A3A     001560
A4      001606  A4A     001632  A5      001660  A5A     001704
BEGIN   001714  BIT0    = 000001  BIT1    = 000002  BIT10   = 002000
BIT11   = 004000  BIT12   = 010000  BIT13   = 020000  BIT14   = 040000
BIT15   = 100000  BIT2    = 000004  BIT3    = 000010  BIT4    = 000020
BIT5    = 000040  BIT6    = 000100  BIT7    = 000200  BIT8    = 000400
BIT9    = 001000  DISPLA  = 177570  DONE    003760  DONE1   004012
EMTVEC  = 000030  END     003740  ERRVEC  = 000004  HLT     = 000000
ICNT    001000  KM      = 000000  KPTR    = 000500  KSP     =%000006
PC      =%000007  POP2    = 022626  PSW     = 177776  R0      =%000000
R1      =%000001  R10     =%000000  R11     =%000001  R12     =%000002
R13     =%000003  R14     =%000004  R15     =%000005  R16     =%000006
R17     =%000007  R2      =%000002  R3      =%000003  R4      =%000004
R5      =%000005  R6      =%000006  R7      =%000007  SCOPE   = 010701
SM      = 040000  SP      =%000006  SPTR    = 000600  SSP     =%000006
START   001010  SWR     = 177570  TBITVE  = 000014  TEMP    001002
TPBUF   = 177566  TPCSR   = 177564  TRAPVE  = 000034  T0      001052
T0X     001330  T1      001776  T1A     002004  T10     002360
T11     002424  T12     002446  T13     002506  T14     002540
T15     002602  T16     002636  T16A    002652  T16B    002656
T16X    002660  T17     002666  T2      002042  T20     002714
T20A    002770  T23     003044  T24     003116  T25     003234
T25A    003262  T25B    003264  T26     003334  T26A    003360
T26B    003362  T27     003420  T27A    003452  T3      002066
T30     003514  T31     003552  T32     003610  T33     003642
T33A    003652  T34     003702  T4      002126  T5      002166
T6      002224  T6A     002276  T6X     002302  T7      002324
T7A     002344  T7X     002350  UBREAK  = 177770  UM      = 140000
UPTR    = 000700  USP     =%000006  .       = 004016
```

ERRORS DETECTED: 0