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IDENTIFICATION

PRODUCT CODE: MAINDEC-11-DFKTA-A-D
PRODUCT NAME: 11/34 MEMORY MANAGEMENT BASIC LOGIC TEST
DATE: DECEMBER 21,1975
MAINTAINER: DIAGNOSTIC GROUP
AUTHOR: GLENN JOHNSON

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1.0 ABSTRACT

THIS PROGRAM INCREMENTALLY TESTS THE BASIC LOGIC
FUNCTIONS OF THE MEMORY MANAGEMENT FOR THE PDP-11/34.
THEY FULLY TEST RELOCATION, DIRECT AND INDIRECT ADDRESSING OF THE
MEMORY MANAGEMENT REGISTERS, AND CORRECT OPERATION OF ALL
THE BITS IN THE REGISTERS. THE VARIOUS ABORTS ARE TESTED, AS
IS PROPER "LOCKING" AND "UNLOCKING" OF THE ERROR TRACKING LOGIC.

2.0 REQUIREMENTS

2.1 EQUIPMENT

PDP-11/34

2.2 STORAGE

THE PROGRAM REQUIRES 4K OF MEMORY.

3.0 LOADING PROCEDURE

LOAD PROGRAM INTO MEMORY USING ABS LOADER.

4.0 STARTING PROCEDURE

LOAD SWITCH REGISTER WITH DESIRED SETTING.
(SOFTWARE SWITCH REG. LOC. = 176)

START AT 200.
THE PROGRAM WILL RING THE BELL ON COMPLETION
OF A PASS.

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5.0 OPERATING PROCEDURE

5.1 OPERATIONAL SWITCH SETTINGS

NOTE: IF NO HARDWARE SWITCH REGISTER IS AVAILABLE THE PROGRAM WILL AUTOMATICALLY USE THE CONTENTS OF LOC. 176 AS THE SOFTWARE SWITCH REGISTER. THE USER SHOULD SET THIS LOCATION BEFORE STARTING THE PROGRAM.

BIT 15=1 -- HALT ON ERROR
BIT 14=1 -- SCOPE LOOP
BIT 13=1 -- INHIBIT PRINTOUT
— BIT 12=1 -- INHIBIT BELL AT END OF PASS, TYPE ASTERICK
BIT 12=0 -- RING BELL AT END OF EACH PASS
BIT 11=1 -- INHIBIT ITERATIONS
BIT 10=1 -- HALT AT END OF CURRENT TEST WITH NEXT TEST NUMBER IN R0.

5.2 SUBROUTINE ABSTRACTS

5.2.1 SCOPE

THIS SUBROUTINE CALL IS PLACED BETWEEN EACH SUBTEST. IT RECORDS THE STARTING ADDRESS OF EACH SUBTEST AS IT IS BEING ENTERED. IF A SCOPE LOOP IS REQUESTED, IT WILL JUMP TO THE START OF THE SUBTEST THAT THE SCOPE LOOP IS REQUESTED FOR. IF SCOPE LOOP IS NOT REQUESTED, THERE WILL BE 1024 ITERATIONS ON THAT SUBTEST BEFORE THE NEXT SUBTEST IS ENTERED. SWITCH 11 ON A 1 INHIBITS ITERATION OF SUBTESTS.

5.2.2 HLT

THIS EMT CALLS THE SUBROUTINE PRINT, WHICH PRINTS OUT THE LOCATION COUNTER AT THE TIME OF FAILURE AND THE CONTENTS OF THE PROCESSOR STATUS REGISTER. NOTE THAT THE LOCATION COUNTER WILL BE THE ADDRESS OF THE HLT PLUS TWO.

5.2.3 TRAPCATCHER

THIS IS A SERIES OF INSTRUCTIONS STARTING AT LOCATION 0 DESIGNED TO DETECT AND ISOLATE UNEXPECTED TRAPS AND INTERRUPTS TO THE TRAP AND INTERRUPT VECTOR AREA OF MEMORY.

EACH VECTOR ENTRANCE ADDRESS IS LOADED WITH THE ADDRESS OF THE NEXT LOCATION. THE NEXT LOCATION IS LOADED WITH A HALT (000000). THUS AN ILLEGAL TRAP OR INTERRUPT WILL CAUSE A HALT AT THE TRAP LOCATION PLUS TWO.

IF A HALT OCCURS IN THE TRAP OR INTERRUPT AREA EXAMINE REGISTER

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SIX. IT WILL CONTAIN THE CURRENT STACK ADDRESS. THE CONTENTS
OF THE CURRENT STACK ADDRESS IS THE VALUE OF THE LOCATION
COUNTER WHEN THE TRAP OR INTERRUPT OCCURRED.

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5.2.4 EMTSRV (EMT DECODER)

THIS ROUTINE DECODES ALL EMT CALLS, INCLUDING PATCHES AND THE
HLT CALL WHICH PASSES CONTROL TO THE PRINT ROUTINE.

5.2.5 CLRALL

THIS ROUTINE CLEARS ALL THE PAR'S AND PDR'S.
AS WELL AS SR0.

5.2.6 RWALL

THIS ROUTINE MAPS ALL PAGES TO BANK 0 BY CLEARING ALL THE PAR'S.
ALL PAGES ARE MADE 4K READ-WRITE BY LOADING ALL THE PDR'S WITH
THE VALUE 77406.

5.3 PROGRAM AND/OR OPERATOR ACTION

THE PROGRAM FIRST CHECKS THOSE PROPERTIES OF MEMORY MANAGEMENT
WHICH CAN BE TESTED WITH MEMORY MANAGEMENT TURNED OFF.
THEN, DESTINATION ONLY RELOCATION IS USED TO SHOW THAT BASIC
RELOCATION IS WORKING CORRECTLY. FINALLY, FULL RELOCATION IS
ENABLED AND MISCELLANEOUS ASPECTS OF THE MEMORY MANAGEMENT OPERATION
ARE CHECKED.

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180 6.0 ERRORS
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182 6.1 ERROR PRINTOUT
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184 PRINTOUTS ARE IN A STANDARD TWO-WORD FORMAT. THE FIRST WORD IS
185 THE OCTAL VALUE OF THE PC+2 OF THE DETECTED ERROR. THE SECOND IS
186 THE CONTENTS OF THE PROCESSOR STATUS REGISTER WHEN THE ERROR WAS
187 DETECTED.
188
189 6.2 ERROR RECOVERY
190
191 IN GENERAL, TEST FAILURES WILL PRINTOUT AN ERROR MESSAGE AND
192 CONTINUE. IF THE "HALT ON ERROR" SWITCH IS SET, HITTING CONTINUE
193 WILL RECOVER. IF THE PROGRAM HANGS UP IN A LOOP, THE ERROR IS
194 LIKELY TO BE A SIGNAL WHICH WAS NEVER RECEIVED. IF A HALT
195 OCCURS IN THE TRAP AND VECTOR AREA THE PROGRAM MUST BE RESTARTED,
196 IF THE PROGRAM HALTS IN THE MAIN FLOW, CONSULT THE LISTING IF NO
197 MESSAGE IS TYPED OUT.
198
199 6.3 BRANCH SELF
200
201 A BRANCH TO SELF IS USED IN THIS DIAGNOSTIC TO INDICATED A FAILURE
202 WHEN A HALT OR A HLT WORD TRAP CALL COULD LEAD TO PROBLEM.
203
204 7.0 RESTRICTIONS
205
206 PROGRAM MUST BE LOADED INTO LOWER 4K OF MEMORY.
207
208 8.0 MISCELLANEOUS
209
210 8.1 EXECUTION TIME
211
212 EACH PASS TAKES APPROXIMATELY 1 MINUTE WITH CORE MEMORY.
213
214 8.2 STACK POINTERS
215
216 THE KERNEL STACK POINTER IS USUALLY INITIALIZED TO 1000,
217 HOWEVER, IN CERTAIN TESTS IT MAY BE INITIALIZED TO A LOWER
218 ADDRESS (VIRTUAL) TO MAKE UP FOR RELOCATION OF THE BANK,
219
220 THE USER STACK POINTER IS INITIALIZED TO 400.
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8.4 EXECUTION ORDER CHECKING

SINCE THE MEMORY MANAGEMENT MAY CAUSE AN INCORRECT FETCH IF IT IS NOT WORKING CORRECTLY, THE ORDER OF EXECUTION OF ALL SUBTESTS IS CHECKED. THE SCOPE ROUTINE, WHEN IT CHANGES FROM ONE SUBTEST TO THE NEXT, INCREMENTS A COUNTER CALLED TESTCT. AT THE START OF EACH SUBTEST, THIS COUNTER IS CHECKED FOR THE CORRECT VALUE FOR THAT SUBTEST. IF TESTS ARE NOT EXECUTED IN THE CORRECT ORDER, TESTCT WILL NOT CONTAIN THE EXPECTED VALUE, AND AN ERROR PRINTOUT WILL OCCUR.

9.0 PROGRAM DESCRIPTION

THE PROGRAM INITIALLY TESTS THOSE FEATURES OF MEMORY MANAGEMENT WHICH CAN BE TESTED WITHOUT TURNING ON MEMORY MANAGEMENT. IT THEN USES THE MAINTENANCE MODE (DESTINATION ONLY RELOCATION) TO TEST TURNING MEMORY MANAGEMENT ON AND OFF AND TO FULLY CHECK OUT RELOCATION. ONCE RELOCATION HAS BEEN FULLY TESTED, FULL PAGING IS USED TO TEST THE REMAINING OPERATIONS OF THE OPTION.

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;BASIC LOGIC TEST OF THE 11/34 MEMORY MANAGEMENT
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;THIS PROGRAM IS A MODIFIED 11/40 DIAGNOSTIC, DBKTA. THIS VERSION
;HAS THE SOFTWARE SWITCH REGISTER CAPABILITIES AND HAS BEEN MODIFIED
;TO ACCOUNT FOR ANY 11/40 * 11/34 DIFFERENCES. THIS PROGRAM IS
;INTENDED TO BE RUN ONLY ON 11/34 PROCESSORS.

;OPERATING INSTRUCTIONS
/
/ 1. LOAD TEST USING THE ABSOLUTE LOADER
/ 2. LOAD DESIRED SWITCH SETTING (LOC, 176 IS SOFTWARE SWR IF NEEDED)
/ 3. START AT 200.

;BIT15=1 CAUSES HALT ON ERROR
;BIT14=1 CAUSES SCOPE LOOPING
;BIT13=1 INHIBITS ERROR PRINTOUT
;BIT11=1 INHIBITS ITERATIONS
;BIT10=1 HALT AT END OF CURRENT TEST WITH TEST NUMBER OF NEXT TEST IN R0.
/ TEST. PRESS CONTINUE TO ADVANCE TO NEXT TEST. (WITH BIT11=1)

;DEFINITIONS
SCOPE=TRAP
NOP=240
R0=X0
R1=X1
R2=X2
R3=X3
R4=X4
R5=X5
R6=X6
R7=X7
SP=X6
PC=X7
PS=17776
STATUS=PS
HLT=104006
BIT0=1
BIT1=2
BIT2=4
BIT3=10
BIT4=20
BIT5=40
BIT6=100
BIT7=200
BIT8=400
BIT9=1000
BIT10=2000
BIT11=4000
BIT12=10000
BIT13=20000
BIT14=40000
BIT15=100000

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;LOAD TRAP CATCHER INTO 0 THRU 777
;LOAD EACH VECTOR ADDRESS WITH THE ADDRESS OF THE NEXT
;LOCATION, AND LOAD EACH LOCATION IMMEDIATELY FOLLOWING
;A VECTOR ADDRESS WITH A HALT INSTRUCTION

;LOAD VECTOR AREA
    .=30
    EMTSRV
    340
    .=34
    SCOPEC
    0
    .=46
    LOGIC

;SOFTWARE SWITCH REGISTER
    .=174
DISPREG: 0
SWREG: 0
;SOFTWARE DISPLAY REGISTER
;SOFTWARE SWITCH REGISTER

;LOAD STARTING AREA
    .=200
    JMP START
    .=210
    JMP TESTX

;LOAD DATA AREA
    .=400
USTACK: 0
    .=-376
KSTACK: 0
    .WORD 0,0,0

K123: 123456
K134: 134567
TCSR: 177564
TOBR: 177566
TEMP: 0

/
SR0: 177572
SR0H: 177573
SR1: 177574
SR2: 177576
;MEMORY MANAG. STATUS REGISTER ADDRESSES

/
ADRTAB:
UPDR0: 177600
UPDR1: 177602
UPDR2: 177604
UPDR3: 177606
UPDR4: 177610
UPDR5: 177612
UPDR6: 177614
UPDR7: 177616
/
UPAR0: 177640
;USER PAGE ADDRESS REGISTERS

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357 001056 177642      UPAR1: 177642
358 001060 177644      UPAR2: 177644
359 001062 177646      UPAR3: 177646
360 001064 177650      UPAR4: 177650
361 001066 177652      UPAR5: 177652
362 001070 177654      UPAR6: 177654
363 001072 177656      UPAR7: 177656
364                                J
365 001074 172300      KPDR0: 172300      ;KERNEL PAGE DESCRIPTOR REGISTERS
366 001076 172302      KPDR1: 172302
367 001100 172304      KPDR2: 172304
368 001102 172306      KPDR3: 172306
369 001104 172310      KPDR4: 172310
370 001106 172312      KPDR5: 172312
371 001110 172314      KPDR6: 172314
372 001112 172316      KPDR7: 172316
373                                J
374 001114 172340      KPARD: 172340      ;KERNEL PAGE ADDRESS REGISTERS
375 001116 172342      KPARI: 172342
376 001120 172344      KPARD: 172344
377 001122 172346      KPARI: 172346
378 001124 172350      KPARD: 172350
379 001126 172352      KPARI: 172352
380 001130 172354      KPARD: 172354
381 001132 172356      KPARI: 172356
382                                ADREND= ,-2
383                                J
384 001134 177600      PDRTAB: 177600      ;STARTING ADDRESSES OF PDR'S FOR EACH MODE
385 001136 172300      PDREND: 172300
386 001140 177640      PARTAB: 177640      ;STARTING ADDRESSES OF PAR'S FOR EACH MODE
387 001142 172340
388
389 001144 001074      STATAB: KPDR0      ;ADDRESS OF KERNEL TABLE OF PDR'S AND PAR'S
390 001146 000000      0
391 001150 001034      UPDR0      ;ADDRESS OF USER TABLE OF PDR'S AND PAR'S
392 001152 140000      STAEND: 140000
393
394
395 001154 000000      STAPNT: 0
396 001156 000000      PAGES: 0
397 001160 000000      SAVEA: 0
398 001162 000000      SAVEB: 0
399 001164 000250      KTYEC: 250
400 001166 000252      KTSTA: 252
401 001170 100361      PDRM2: 100361
402 001172 000000      FTITLE: 0
403 001174 000000      TESTCT: 0
404 001176 000000      BLDCKS: 0
405 001200 177570      SRI 177570      ;SWITCH REGISTER POINTER
406 001202 000000      DISPLAY: 0      ;DISPLAY REGISTER POINTER
407
408
409
410 001204 005037 177776      ;SET UP FOR START OF BASIC LOGIC TESTS
                                START: CLR      ##PS      ;INITIALIZE STATUS

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411 001210 012706 001000      MOV      #KSTACK,SP      ;SETUP KERNEL STACK
412
413 001214 013746 000004      MOV      ##,-(SP)      ;SAVE ERROR VECTOR
414 001220 013746 000006      MOV      ##,-(SP)
415 001224 012767 001240 176552      MOV      #15,4      ;SET UP TIME OUT VECTOR
416 001232 005777 177742      TST     28      ;TRY TO REFERENCE HARDWARE SWR
417 001236 000407      BR      28      ;BRANCH IF NO TIMEOUT TRAP OCCURS
418 001240 012767 000176 177732 15:      MOV      #SWREG,SR      ;POINT TO SOFTWARE SWR
419 001246 012767 000174 177726      MOV      #DISPREG,DISPLAY ;POINT TO SOFTWARE DISPLAY REG
420 001254 022626      CMP      (SP)+,(SP)+      ;RESTORE STACK
421 001256 012637 000006      MOV      (SP)+,##4      ;RESTORE ERROR VECTOR
422 001262 012637 000004      MOV      #200,ICOUNT      ;INITIALIZE ITERATION COUNT
423 001266 012767 002000 014362      MOV      #TEST1+C,RETRN      ;SETUP SCOPE AND ITERATION LOOP RETURN
424 001274 012767 001334 014360      MOV      #1,TESTCT      ;INITIALIZE TEST COUNT
425 001302 012767 000001 177664      TST     FTITLE      ;DID TITLE PRINT
426 001310 005767 177656      BNE     TEST1+2      ;YES, START TEST
427 001314 001007      JSR     PC,TYPE      ;NO, PRINT TITLE
428 001316 004767 014460      JSR     PC,TYPE
429 001322 015250      MVI     PC,TYPE
430 001324 005267 177642      INC     FTITLE
431 001330 000401      BR      .+4      ;SKP SCOPE INSTRUCTION
432
433
434 001332 104400      JSR0 AND SRI SHOULD BE INITIALIZED TO 0
435 001334 012706 001000      TEST1:  SCOPE
436 001340 004767 015040      MOV      #KSTACK,SP      ;INITIALIZE KERNEL STACK POINTER
437 001344 000001      JSR     PC,ORDER      ;CHECK TEST SEQUENCE + INIT SR0
438 001346 104006      1      ;TEST NUMBER
439 001350 000005      1      ;TEST EXECUTED OUT OF SEQUENCE
440 001352 005777 177446      RESET   #SR0      ;ISSUE INIT
441 001356 001401      TST     #+5      ;CHECK SR0
442 001360 104006      BEQ     .+4      ;SR0 WAS NOT INITIALIZED TO ZERO
443 001362 005777 177442      TST     #SRI      ;CHECK SRI
444 001366 001401      BEQ     .+4
445 001370 104006      TST     #10,ICOUNT      ;SRI WAS NOT INITIALIZED TO ZERO
446 001372 012767 000010 014256      MOV      #10,ICOUNT      ;DROP ITERATION COUNT SINCE RESET IS USED
447
448
449
450 001400 104400      ;CHECK READ/WRITE PROPERTIES OF ALL BITS IN SR0 EXCEPT 0 AND 8
451 001402 012706 001000      ;BY ROTATING A ONE THRU THE BIT POSITIONS BEING CHECKED
452 001406 004767 014772      TEST2:  SCOPE
453 001412 000002      MOV      #KSTACK,SP      ;INITIALIZE KERNEL STACK POINTER
454 001414 104006      JSR     PC,ORDER      ;CHECK TEST SEQUENCE + INIT SR0
455 001416 005777 177402      2      ;TEST NUMBER
456 001422 001402      1      ;TEST EXECUTED OUT OF SEQUENCE
457 001424 104006      TST     #SR0      ;CHECK SR0 INITIALLY
458 001426 000422      BEQ     .+5      ;SR0 NOT ZERO AT START OF TEST
459 001430 012700 000001      BR      EXIT2
460 001434 010001      MOV      #1,R0      ;R0 CONTAINS BIT INDICATING POSITION BEING TESTE
461 001436 010102      MOV      R0,R1
462 001440 042701 000401      BIC     #401,R1      ;DON'T SET THE BIT IN SR0 IF IT'S BIT 0 OR BIT 8
463 001444 042702 017777      BIC     #17777,R2      ;CLEAR THE BIT IN R2 IF IT SHOULDN'T SET IN SR0
464 001450 010177      MOV      R1,#SR0

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465 001454 020277 177344      CMP      R2,#SR0      ;CHECK SR0
466 001460 001401              BEQ      ,*4          ;SR0 INCORRECT WHEN VALUE IN R1
467 001462 104006              HLT                      ;WAS LOADED INTO IT
468
469 001464 006300              ASL      R0
470 001466 103362              BCC     LOOP2
471 001470 005077 177330              CLR      #SR0
472 001474
473
474
475 ;BITS 0-11 OF ALL PAR'S SHOULD BE READ/WRITE
476 ;TEST BY ROTATING A BIT THRU EACH PAR
477 ;ALSO SHOWS THAT OUTPUT PATHS FROM PAR'S ARE OK
478 ;AND THAT EVERY PAR ADDRESS IS RESPONDED TO
479 TEST3: SCOPE
480       MOV      #KSTACK,SP      ;INITIALIZE KERNEL STACK POINTER
481       JSR      PC,ORDER        ;CHECK TEST SEQUENCE + INIT SR0
482       HLT                      ;TEST NUMBER
483       MOV      #2000,ICOUNT     ;TEST EXECUTED OUT OF SEQUENCE
484       JSR      X7,CLRALL       ;RESTORE ICOUNT
485       MOV      #PARTAB,R3     ;INITIALIZE MEMORY MANAG. REGISTERS
486       MOV      #2,R0          ;R3 POINTS TO TABLE OF PAR ADDRESSES
487       MOV      (R3)+,R1       ;R0 IS COUNTER OF STATES LEFT TO TEST
488       MOV      #10,R2        ;PUT ADDRESS OF 1ST PAR IN SET IN R1
489       MOV      #1,R4         ;R2 IS COUNTER OF PAR'S LEFT TO TEST IN SET
490       MOV      R4,#R1        ;R4 IS BIT OF PAR BEING TESTED
491       CMP      R4,#R1        ;SET BIT IN PAR
492       BEQ      ,*4          ;CHECK PAR
493       HLT                      ;BRANCH IF OK
494
495
496 001556 006304              ASL      R4
497 001560 020427 010000      CMP      R4,#10000
498 001564 001370              BNE     LOOP3B
499 001566 005011              CLR      #R1
500 001570 005721              TST     (R1)+          ;MOVE POINTER
501 001572 077215              SOB     R2,LOOP3A     ;TEST ALL PAR'S IN SET
502 001574 077021              SOB     R0,LOOP3     ;TEST ALL 3 REGISTER SETS
503
504 ;BITS 1-3, 8-14 OF ALL PDR'S SHOULD BE READ/WRITE
505 ;BITS 0,4,5,7 AND 15 SHOULD ALWAYS BE ZERO
506 ;BIT 6 SHOULD BE ZERO IF PDR IS WRITTEN
507 ;ACTUAL CLEARING AND SETTING OF 6 TESTED LATER
508 ;ALSO SHOWS THAT OUTPUT PATHS FROM PDR'S ARE OK
509 ;AND THAT EVERY PDR ADDRESS IS RESPONDED TO
510 TEST4: SCOPE
511       MOV      #KSTACK,SP      ;INITIALIZE KERNEL STACK POINTER
512       JSR      PC,ORDER        ;CHECK TEST SEQUENCE + INIT SR0
513       HLT                      ;TEST NUMBER
514       MOV      #4              ;TEST EXECUTED OUT OF SEQUENCE
515       JSR      X7,CLRALL       ;INITIALIZE MEMORY MANAG. REGISTERS
516       MOV      #PDRTAB,R3     ;R3 POINTS TO TABLE OF PDR ADDRESSES
517       MOV      (R3)+,R1       ;LOAD ADDRESS OF 1ST PDR IN STATE
518       MOV      #10,R2        ;USE R2 AS A COUNTER OF PDR'S

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519
520 001632 012700 000001      LOOP4A: MOV      #1,R0          ;LEFT TO TEST
521 001636 010005              LOOP4B: MOV      R0,R5          ;SETUP R0 TO ROTATE A BIT THRU
522 001640 046705 177324      BIC     PDRM2,R5         ;R5 CONTAINS EXPECTED RESULTING CONTENTS OF PDR
523 001644 010011              MOV      R0,#R1          ;LOAD PDR
524 001646 021105              CMP      #R1,R5          ;CHECK RESULTING CONTENTS OF PDR
525 001650 001401              BEQ      ,*4
526 001652 104006              HLT                      ;PDR WHOSE ADDRESS IS IN R1
527
528
529 001654 006300              ASL      R0
530 001656 103367              BCC     LOOP4B
531 001660 005011              CLR      #R1
532 001662 005721              TST     (R1)+
533 001664 077216              SOB     R2,LOOP4A
534 001666 020327 001136      CMP      R3,#PDREND
535 001672 003754              BLE     LOOP4
536
537 ;NO DUAL ADDRESSING TEST FOR PAR'S AND PDR'S
538 TEST5: SCOPE
539       MOV      #KSTACK,SP      ;INITIALIZE KERNEL STACK POINTER
540       JSR      PC,ORDER        ;CHECK TEST SEQUENCE + INIT SR0
541       HLT                      ;TEST NUMBER
542       MOV      #5              ;TEST EXECUTED OUT OF SEQUENCE
543       JSR      X7,CLRALL       ;CLEAR ALL PAR'S AND PDR'S
544       MOV      #ADRTAB,R1     ;R1 POINTS TO ADDRESS OF LOCATION
545
546 001722 012700 001034      LOPSAA: MOV      #ADRTAB,R2    ;LOADED WITH 1 BIT SET IN EACH 4 BITS
547
548
549 001726 012703 000040      MOV      #32,R3          ;R2 USED AS A POINTER TO CYCLE THRU
550 001732 012771 010421 000000  MOV      #10421,(R1)      ;ALL OTHER ADDRESSES OF PAR/PDR PAIR'S TO
551
552
553 001740 020201              LOP5B:  CMP      R2,R1          ;CHECK FOR DUAL ADDRESSING
554 001742 001406              BEQ      CONT5           ;R3 USED AS A COUNTER
555 001744 005772 000000      BEQ      CONT5           ;LOAD A PAR OR PDR = SET ONE BIT
556
557 001750 001403              BEQ      CONT5           ;IN EACH CHIP (4 BITS PER CHIP) IF R/W
558 001752 104006              HLT                      ;SKIP CHECKING THIS ADDRESS TO SEE IF
559
560
561
562 001754 005072 000000      LOP5B:  CMP      R2,R1          ;IT'S A DUAL, SINCE IT WAS THE ONE LOADED
563 001760 005722              BEQ      CONT5           ;OTHERWISE, CHECK TO SEE IF THIS
564 001762 077312              SOB     R3,LOP5B        ;REGISTER RESPONDED TO THE ADDRESS
565
566
567 001764 022701 001132      CMP      #ADREND,R1      ;OF THE ONE LOADED AS A DUAL
568
569
570 001770 001402              BEQ      DONESA
571 001772 005031              CLR      #R1)+
572 001774 000752              BR      LOPSAA
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573
574 001776 012767 000100 013652 DONESA1 MOV #100,ICOUNT ITO BY R1
575 IDROP ITERATION COUNT
576
577 002004 104000 JSHOW THAT BYTE ADDRESSING OF PAR'S WORKS FOR HIGH AND LOW BYTES
578 002006 012706 001000 TEST6: SCOPE
579 002012 004767 014366 MOV #KSTACK,SP IINITIALIZE KERNEL STACK POINTER
580 002016 000006 JSR PC,ORDER ICHECK TEST SEQUENCE + INIT SR0
581 002020 104006 HLT ITEST NUMBER
582 002022 012767 002000 013626 MOV #2000,ICOUNT ITEST EXECUTED OUT OF SEQUENCE
583 002030 004767 013334 JSR #X7,CLRALL IRESTORE ITERATION COUNT
584 002034 012703 001140 MOV #PARTAB,R3 IINITIALIZE MEMORY MANAG. REGISTERS
585 002040 012700 000002 MOV #2,R0 IR3 POINTS TO TABLE OF PAR ADDRESSES
586 002044 012301 LOOP6: MOV (R3)+,R1 IR0 IS COUNTER OF STATES LEFT TO TEST
587 002046 012702 000010 MOV #10,R2 IPUT ADDRESS OF 1ST PAR IN SET IN R1
588 002052 012711 177777 LOOP6A: MOV #-1,R1 IR2 IS COUNTER OF PAR'S LEFT TO TEST IN SET
589 002056 105011 CLR R0 ISET UP PAR BEING TESTED
590 002060 022711 007400 CLR R1 ICLEAR LOW BYTE OF PAR
591 002064 001401 CMP #7400,R1 ICHECK PAR
592 002066 104006 HLT IBRANCH IF OK
593
594 002070 012711 177777 MOV #-1,R1 ISET UP PAR TO TEST HIGH BYTE
595 002074 105061 000001 CLR R1 ICLEAR HIGH BYTE
596 002100 022711 000377 CMP #377,R1 ICHECK PAR
597 002104 001401 BEQ #+4
598 002106 104006 HLT IDATOR TO PAR WHOSE ADDRESS IS IN
599 IR1 FAILED
600 002110 005721 TST (R1)+ ISET UP PAR TO TEST HIGH BYTE
601 002112 077221 SOB R2,LOOP6A ICLEAR HIGH BYTE
602 002114 077025 SOB R0,LOOP6 ITEST ALL PAR'S IN SET
603 ITEST ALL 2 REGISTER SETS
604
605 002116 104400 JSHOW THAT BYTE ADDRESSING OF PDR'S WORKS FOR HIGH AND LOW BYTES
606 002120 012706 001000 TEST7: SCOPE
607 002124 004767 014254 MOV #KSTACK,SP IINITIALIZE KERNEL STACK POINTER
608 002130 000007 JSR PC,ORDER ICHECK TEST SEQUENCE + INIT SR0
609 002132 104006 HLT ITEST NUMBER
610 002134 004767 013230 JSR #X7,CLRALL ITEST EXECUTED OUT OF SEQUENCE
611 002140 012703 001134 MOV #PARTAB,R3 IINITIALIZE MEMORY MANAG. REGISTERS
612 002144 012700 000002 MOV #2,R0 IR3 POINTS TO TABLE OF PDR ADDRESSES
613 002150 012301 LOOP7: MOV (R3)+,R1 IR0 IS COUNTER OF STATES LEFT TO TEST
614 002152 012702 000010 MOV #10,R2 IPUT ADDRESS OF 1ST PDR IN SET INTO R1
615 002156 012711 177777 LOOP7A: MOV #-1,R1 IR2 IS COUNTER OF PDR'S LEFT TO TEST IN SET
616 002162 105011 CLR R0 ISET UP PDR BEING TESTED
617 002164 022711 077400 CLR R1 ICLEAR LOW BYTE OF PDR
618 002170 001401 CMP #77400,R1 ICHECK PDR
619 002172 104006 HLT IBRANCH IF OK
620
621 002174 012711 177777 MOV #-1,R1 ISET UP PDR TO TEST HIGH BYTE
622 002200 105061 000001 CLR R1 ICLEAR HIGH BYTE
623 002204 022711 000016 CMP #16,R1 ICHECK PDR
624 002210 001401 BEQ #+4
625 002212 104006 HLT IDATOR TO HIGH BYTE OF PDR WHOSE
626 IADDRESS IS IN R1 FAILED

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627 002214 005721 TST (R1)+ IMOVE POINTER
628 002216 077221 SOB R2,LOOP7A ITEST ALL PDR'S IN SET
629 002220 077025 SOB R0,LOOP7 ITEST ALL 2 REGISTER SETS
630
631
632 002222 104400 IINIT SHOULD HAVE NO EFFECT ON PAR'S
633 002224 012706 001000 TEST10: SCOPE
634 002230 004767 014150 MOV #KSTACK,SP IINITIALIZE KERNEL STACK POINTER
635 002234 000010 JSR PC,ORDER ICHECK TEST SEQUENCE + INIT SR0
636 002236 104006 HLT ITEST NUMBER
637 002240 012767 000010 013410 MOV #10,ICOUNT ITEST EXECUTED OUT OF SEQUENCE
638 002246 005067 000104 CLR TST10F IDROP ITERATION COUNT
639 002252 012704 005252 MOV #5252,R4
640 002256 012703 001140 TST10: MOV #PARTAB,R3
641 002262 012700 000002 MOV #2,R0
642 002266 012301 LOOP10: MOV (R3)+,R1
643 002270 012702 000010 MOV #10,R2 ICOUNTER TO LOAD PAR'S
644 002274 104021 LOP10A: MOV R4,(R1)+ FLOAD PAR WITH PATTERN
645 002276 077202 SOB R2,LOP10A FLOAD ALL 16 IN THIS SET
646 002300 077006 SOB R0,LOOP10 IINITIALIZE ALL 2 SETS
647 002302 000005 RESET IISSUE INIT
648 002304 012703 001140 MOV #PARTAB,R3
649 002310 012700 000002 MOV #2,R0
650 002314 012301 LOP10B: MOV (R3)+,R1
651 002316 012702 000010 MOV #10,R2 ICOUNTER TO CHECK PAR'S
652 002322 020411 LOP10C: CMP R4,R1 ICHECK DATA
653 002324 001401 BEQ #+4
654 002326 104006 HLT IPAR WHOSE ADDRESS IS IN R1
655 IAS INCORRECT AFTER INIT
656 002330 005721 TST (R1)+ IMOVE POINTER
657 002332 077205 SOB R2,LOP10C ITEST ALL 8 PAR'S IN THIS SET
658 002334 077011 SOB R0,LOP10B ITEST ALL 2 REGISTER SETS
659 002336 005767 000014 TST TST10F ICHECK FOR BOTH PATTERNS USED
660 002342 001006 BNE EXIT10 IF DONE, GO TO NEXT TEST
661 002344 005267 000006 INC TST10F IF NOT, SET FLAG
662 002350 012704 002525 MOV #2525,R4 FLOAD OTHER PATTERN
663 002354 000740 BR TST10 FREPEAT TEST WITH 2ND PATTERN
664 002356 000000 TST10F: 0
665 002360 EXIT10:
666
667
668 002360 104400 IINIT SHOULD'N'T CLEAR OR SET ANY OF THE R/W BITS IN THE PDR'S
669 002362 012706 001000 TEST11: SCOPE
670 002366 004767 014012 MOV #KSTACK,SP IINITIALIZE KERNEL STACK POINTER
671 002372 000011 JSR PC,ORDER ICHECK TEST SEQUENCE + INIT SR0
672 002374 104006 HLT ITEST NUMBER
673 002376 005067 000104 CLR TST11F ITEST EXECUTED OUT OF SEQUENCE
674 002402 012704 025012 MOV #25012,R4 FLOAD PATTERN IN R4
675 002406 012703 001134 TST11: MOV #PARTAB,R3
676 002412 012700 000002 MOV #2,R0
677 002416 012301 LOOP11: MOV (R3)+,R1
678 002420 012702 000010 MOV #10,R2 ICOUNTER TO LOAD PDR'S
679 002424 104021 LOP11A: MOV R4,(R1)+ FLOAD PDR WITH PATTERN
680 002426 077202 SOB R2,LOP11A FLOAD ALL 8 IN THIS SET

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661 002430 077006 SOB R0,LOOP11 ;INITIALIZE ALL 2 SETS
662 002432 000005 RESET ;ISSUE INIT
663 002434 012703 001134 MOV #PDKTAB,R3
664 002440 012700 000002 MOV #2,R0
665 002444 012301 LOP11B: MOV (R3)+,R1
666 002446 012702 000010 MOV #10,R2 ;COUNTER TO CHECK PDR'S
667 002452 020411 LOP11C: CMP R4,#R1 ;CHECK DATA
668 002454 001401 BEQ .+4
669 002456 104006 HLT ;PDR WHOSE ADDRESS IS IN R1
690 ;WAS INCORRECT AFTER INIT
691 002460 005721 TST (R1)+ ;MOVE POINTER
692 002462 077205 SOB R2,LOP11C ;TEST ALL 8 PDR'S IN THIS SET
693 002464 077011 SOB R0,LOP11B ;TEST ALL 2 REGISTER SETS
694 002466 005767 000014 TST TST11F ;CHECK FOR BOTH PATTERNS USED
695 002472 001006 BNE EXIT11 ;IF DONE, GO TO NEXT TEST
696 002474 005267 000006 INC TST11F ;IF NOT, SET FLAG
697 002500 012704 052400 MOV #52400,R4 ;LOAD 2ND PATTERN
698 002504 000740 BR TST11
699 002506 000000 TST11F: 0
700 002510 000240 EXIT11: NOP
701
702 ;SHOW THAT SR1 IS ONLY = 0 AND CANNOT BE LOADED
703 002512 104400 TEST12: SCOPE
704 002514 012706 001200 MOV #KSTACK,SP ;INITIALIZE KERNEL STACK POINTER
705 002520 004767 013660 JSR PC,ORDER ;CHECK TEST SEQUENCE + INIT SR0
706 002524 000012 L2 ;TEST NUMBER
707 002526 104006 HLT ;TEST EXECUTED OUT OF SEQUENCE
708 002530 012767 002000 013120 MOV #2000,ICOUNT ;RESTORE ITERATION COUNT
709 002536 012777 177777 176264 MOV #-1,#SR1 ;TRY TO LOAD SR1
710 002544 005777 176260 TST #SR1
711 002550 001401 BEQ .+4
712 002552 104006 HLT ;SR1 INCORRECT - SHOULD HAVE TRACKED
713 ;SR2 SHOULD CONTAIN ADDRESS OF LAST FETCH WITH MEMORY MANAG. TURNED OFF
714 ;CHECK THAT ABORT FREEZES SR2
715 002554 104400 TEST13: SCOPE
716 002556 012706 001200 MOV #KSTACK,SP ;INITIALIZE KERNEL STACK POINTER
717 002562 004767 013616 JSR PC,ORDER ;CHECK TEST SEQUENCE + INIT SR0
718 002566 000013 L3 ;TEST NUMBER
719 002570 104006 HLT ;TEST EXECUTED OUT OF SEQUENCE
720 002572 017701 176234 AD13: MOV #SR2,R1 ;PICK UP SR2 - SHOULD CONTAIN ADDRESS
721 002576 022701 002572 CMP #AD13,R1 ;OF THIS INSTRUCTION
722 002602 001401 BEQ .+4
723 002604 104006 HLT ;SR2 DID NOT CONTAIN FETCH ADDRESS
724 002606 052777 100000 176210 AD13A: BIS #BIT15,#SR0 ;SET NR ABORT
725 002614 000240 NOP
726 002616 022777 002606 176206 CMP #AD13A,#SR2 ;CHECK IF SR2 FROZE
727 002624 001401 BEQ .+4
728 002626 104006 HLT ;SR2 NOT BEING DISABLED BY NR ABORT
729 002630 042777 100000 176166 BIC #BIT15,#SR0 ;CLEAR NR ABORT
730 002636 052777 040000 176160 AD13B: BIS #BIT14,#SR0 ;SET PL ABORT
731 002644 000240 NOP
732 002646 022777 002636 176156 CMP #AD13B,#SR2 ;DID SR2 FREEZE
733 002654 001401 BEQ .+4
734 002656 104006 HLT ;SR2 NOT BEING DISABLED BY PL ABORT

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735 002660 042777 040000 176136 BIC #BIT14,#SR0 ;CLEAR PL ABORT
736 002666 052777 020000 176130 AD13C: BIS #BIT13,#SR0 ;SET RO ABORT
737 002674 000240 NOP
738 002676 022777 002666 176126 CMP #AD13C,#SR2 ;DID SR2 FREEZE
739 002704 001401 BEQ .+4
740 002706 104006 HLT ;SR2 NOT BEING DISABLED BY RO ABORT
741
742 ;SHOW THAT DESTINATION ONLY RELOCATION DOESN'T RELOCATE AN INSTRUCTION
743 ;FETCH (ONE CASE), AND THAT RESET CLEARS SR0<8>
744 ;AND TURNS OFF DESTINATION ONLY RELOCATION
745 ;IF THAT MUCH WORKS, YOU'LL GET THRU TO THE NEXT TEST
746 002710 104400 TEST14: SCOPE
747 002712 012706 001000 MOV #KSTACK,SP ;INITIALIZE KERNEL STACK POINTER
748 002716 004767 013462 JSR PC,ORDER ;CHECK TEST SEQUENCE + INIT SR0
749 002722 000014 L4 ;TEST NUMBER
750 002724 104006 HLT ;TEST EXECUTED OUT OF SEQUENCE
751 002726 004767 012436 JSR X7,CLRALL ;THIS TEST SHOULDN'T GO THRU ANY PAR/PDR PAIR'S
752 ;SO MAKE THEM ALL GIVE NON-RESIDENT
753 ;AND PAGE LENGTH ERRORS IF ACCESSED
754 002732 012777 001006 176134 MOV #1006,#KPDR0 ;3 BLOCKS OF KERNEL PDR0 MUST BE MAPPED
755 ;TO ALLOW TRAPS AND ABORTS
756 002740 012767 000010 012710 MOV #10,ICOUNT ;DROP THE ITERATION COUNT
757 002746 012777 000400 176050 MOV #400,#SR0 ;TURN ON DESTINATION ONLY RELOCATION
758 002754 000005 RESET ;SHOULD CLEAR DEST ONLY BIT, AND A
759 ;SOLID PLACE TO START
760 ;IF THE FETCH IS RELOCATED
761 ;THIS WILL GIVE A PL ABORT
762 002756 032777 000400 176040 BIT #400,#SR0 ;IF MEMORY MANAG. STILL ON, THIS SHOULD CAUSE
763 002764 001401 BEQ .+4 ;PL AND NR ERRORS
764 002766 000000 HLT ;IF MEMORY MANAG. IS OFF, BIT 0 OF SR0 READS
765 ;AS STILL SET OR ANOTHER BIT IS INCORRECT
766 ;IF MEMORY MANAG. IS ON, NO NR OR SL ABORT
767 ;OCCURRED AND RESET FAILED TO TURN MEMORY MANAG.
768 002770 005077 176030 CLR #SR0
769
770 ;SHOW THAT DESTINATION ONLY RELOCATION DOESN'T RELOCATE THE SOURCE
771 ;ADDRESS AND DOES RELOCATE THE DESTINATION
772 002774 104400 TEST15: SCOPE
773 002776 012706 001000 MOV #KSTACK,SP ;INITIALIZE KERNEL STACK POINTER
774 003002 004767 013376 JSR PC,ORDER ;CHECK TEST SEQUENCE + INIT SR0
775 003006 000015 L5 ;TEST NUMBER
776 003010 104006 HLT ;TEST EXECUTED OUT OF SEQUENCE
777 003012 012767 000010 012636 MOV #10,ICOUNT ;KEEP THE NUMBER OF LOOP3 DOWN
778 003020 004767 012344 X7,CLRALL
779 003024 012777 000001 176062 MOV #1,#KPARD
780 003032 012777 077406 176034 MOV #77406,#KPDR0 ;OFFSET KERNEL PAR/PDR PAIR 0 ONE BLOCK FROM BAN
781 003040 012701 003112 MOV #DATA16,R1 ;LOAD A BANK 0 ADDRESS
782 003044 012777 000400 175752 MOV #400,#SR0 ;TURN ON DESTINATION ONLY RELOCATION
783 003052 021111 CMP #R1,#R1 ;THIS TEST WILL FAIL IF BOTH ARE
784 003054 001001 BNE .+4 ;RELOCATED OR BOTH ARE NOT RELOCATED
785 003056 000000 HALT ;SOURCE AND DESTINATION BOTH ADDRESSED SAME LOCA
786 003060 000005 RESET ;TURN OFF DESTINATION-ONLY RELOCATION
787 003062 012701 003012 MOV #DATA16-100,R1 ;LOAD DESTINATION ADDRESS MINUS RELOCATION FACTO
788 003066 012702 003112 MOV #DATA16,R2 ;LOAD SOURCE ADDRESS

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789 003072 012777 000400 175724 MOV #400,#SR0 ;TURN ON DESTINATION-ONLY RELOCATION
790 003100 021211 CMP #R2,#R1 ;USE SAME INSTRUCTION AND ADDRESS
791 003102 001401 BEQ .+4 ;MODES AS BEFORE
792 003104 000000 HALT ;DESTINATION NOT RELOCATED OR INCORRECTLY
793 ;RELOCATED OR SOURCE RELOCATED
794 003106 000005 RESET ;TURN OFF RELOCATION
795 003110 000401 BR .+4
796 003112 132465 DATA16: 132465
797 ;SHOW THAT A DATO OF 0 TO BIT 8, SR0 THRU KERNEL PAGE 7 WILL
798 ;CLEAR THE DESTINATION ONLY RELOCATION BIT AND TURN OFF DESTINATION ONLY RELOCATION
799 ;TEST16: SCOPE
800 003114 104400 MOV #KSTACK,SP ;INITIALIZE KERNEL STACK POINTER
801 003116 012706 001000 JSR PC,ORDER ;CHECK TEST SEQUENCE + INIT SR0
802 003122 004767 013256 16 ;TEST NUMBER
803 003126 000016 HLT ;TEST EXECUTED OUT OF SEQUENCE
804 003130 104006 JSR #7,CLRALL ;INITIALIZE
805 003132 004767 012232 JSR #1,#KPAR0 ;MAP KERNEL PAR/PDR PAIR 0
806 003136 012777 000001 175750 ;TO BANK 0 OFFSET BY 1 PAGE
807 003144 012777 077406 175722 MOV #77406,#KPDRO ;USED TO PROVE MEMORY MANAG. IS
808 ;TURNED OFF AFTER CLEARING BIT 8, SR0
809 003152 012701 003112 MOV #DATA16,R1 ;SETUP R1 TO REFERENCE KERNEL PAR/PDR PAIR 0
810 003156 004767 013306 JSR PC,KERN7 ;MAP KERNEL PAR/PDR 7 TO EXT BANK
811 003162 016702 175636 SR0,R2 ;SETUP R2 TO ADDRESS SR0
812 003166 012777 000400 175630 MOV #400,#SR0 ;TURN ON DESTINATION ONLY RELOCATION
813 003174 005012 CLR #R2 ;CLEAR SR0 THRU KERNEL PAR/PDR PAIR7
814 003176 021111 CMP #R1,#R1 ;SHOW THAT MEMORY MANAG. IS OFF
815 003200 001401 BEQ .+4
816 003202 000000 HALT ;MEMORY MANAG. STILL ON
817 003204 032777 000400 175612 BIT #400,#SR0 ;SHOW THAT BIT 8, SR0 IS NOW ZERO
818 003212 001402 BEQ .+6
819 003214 104006 HLT ;DESTINATION ONLY RELOCATION BIT IS STILL ON
820 003216 000005 RESET ;MAKE SURE THAT MEMORY MANAG. IS OFF
821 ;SHOW THAT A DATO OF 0 TO BIT 8, SR0 THRU USER PAGE 7
822 ;WILL TURN OFF DESTINATION - ONLY PAGING
823 003220 004767 012144 JSR #7,CLRALL ;INITIALLY CLEAR ALL PAR/PDR PAIRS
824 003224 012777 000001 175622 MOV #1,#UPAR0 ;MAP USER 0 TO
825 003232 012777 077406 175574 MOV #77406,#UPDRO ;BANK 0 OFFSET BY 1 PAGE, RW
826 003240 012701 003112 MOV #DATA16,R1 ;SETUP R1 TO REFERENCE USER 0
827 003244 012777 007600 175620 MOV #7600,#UPAR7 ;MAP USER 7 TO THE
828 003252 012777 077406 175572 MOV #77406,#UPDR7 ;EXTERNAL BANK
829 003260 016702 175540 SR0,R2 ;SETUP R2 TO ADDRESS SR0
830 003264 012737 140000 177776 MOV #140000,#PS ;SET MODE TO USER
831 003272 012777 000400 175524 MOV #400,#SR0 ;TURN ON DESTINATION - ONLY PAGING
832 003300 005012 CLR #R2 ;CLEAR SR0 THRU USER ASR7
833 003302 021111 CMP #R1,#R1 ;SHOW THAT MEMORY MANAG. IS OFF
834 003304 001401 BEQ .+4
835 003306 000777 BR . ;RELOCATION STILL ON
836
837 ;SHOW THAT ALL PAGE BOUNDARY REFERENCES REFERENCE THE CORRECT PAR
838 ;AND RELOCATE CORRECTLY
839 ;USE DESTINATION - ONLY PAGING
840 ;MAP ALL PAR/PDR PAIR'S RESIDENT READ WRITE
841 ;
842 ; R0 - POINTS TO THE ADDRESS OF THE CURRENT PAR IN THE ADDRESS TABLE

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843 ; R1 - CONTAINS VIRTUAL ADDRESS BEING USED TO REFERENCE START OF PAGE
844 ; R2 - CONTAINS VIRTUAL ADDRESS BEING USED TO REFERENCE END OF PAGE
845 ; R3
846 ; R4
847 ; R5 - USED TO REFERENCE SR0 TO TURN OFF DESTINATION ONLY PAGING
848 003310 104400 TEST17: SCOPE
849 003312 012706 001000 MOV #KSTACK,SP ;INITIALIZE KERNEL STACK POINTER
850 003316 004767 013062 JSR PC,ORDER ;CHECK TEST SEQUENCE + INIT SR0
851 003322 000017 17 ;TEST NUMBER
852 003324 104006 HLT ;TEST EXECUTED OUT OF SEQUENCE
853 003326 004767 012036 JSR #7,CLRALL ;INITIALIZE
854 003332 004767 012056 JSR #7,RWALL ;MAKE ALL PAR/PDR PAIR'S RW, BANK 0,4K
855 003336 015767 017700 175614 MOV #017700,SAVEA ;SAVE CONTENTS OF LOCATIONS TO BE USED
856 003344 013767 017776 175610 MOV #017776,SAVEB
857 003352 012737 123456 017700 MOV #123456,#017700 ;SET UP LOCATIONS TO BE REFERENCED
858 003360 012737 134567 017776 MOV #134567,#017776
859 003366 012703 001012 MOV #K123,R3
860 003372 012704 001014 MOV #K134,R4
861 003376 012767 000100 012252 MOV #100,ICOUNT ;CHANGE ITERATION COUNT
862 003404 012737 140000 177776 MOV #140000,#PS ;CHANGE TO USER
863 003412 012706 000400 MOV #USTACK,SP ;SET UP USER STACK POINTER
864 003416 005037 177776 CLR #PS ;RETURN TO KERNEL
865 003422 012767 001144 175524 MOV #STATAB,STAPNT ;SET UP TO REFERENCE STATE TABLE
866 003430 017700 175520 STAT20: MOV #STAPNT,R0 ;PICK UP ADDRESS OF START OF
867 003434 062700 000020 ADD #20,R0 ;ADDRESS TABLE FOR NEW STATE
868 003440 062767 000002 175506 ADD #2,STAPNT
869 003446 017737 175502 177776 MOV #STAPNT,#PS ;SET UP NEW STATE
870 003454 062767 000002 175472 ADD #2,STAPNT
871 003462 012767 000010 175466 MOV #0,#PAGES ;SET UP COUNTER OF ASR'S LEFT TO TEST
872 003470 012770 007600 000016 MOV #7600,#16(R0) ;SET UP SEGMENTED REFERENCE TO SR0,
873 003476 016705 175322 MOV SR0,R5 ;USED TO TURN DESTINATION - ONLY PAGING OFF
874 003502 005001 CLR R1
875 003504 012702 000076 MOV #76,R2
876 003510 012767 000200 175460 PAG20: MOV #120,#BLOCKS ;SET UP BLOCK COUNT
877 003516 012770 000177 000000 MOV #177,#(R0) ;SET UP PAR
878 003524 022767 000001 175424 CMP #1,PAGES ;IS THIS PAGE ?? (WAS USED
879 ;FOR REFERENCE TO SR0)
880 003532 001005 BNE BLK20 ;IF NOT, BRANCH
881 003534 012770 007600 177776 MOV #7600,#-2(R0) ;YES, SET UP PAGE 6 FOR REFERENCES TO SR0
882 003542 042705 020000 BIC #20000,R5 ;CHANGE R5 TO POINT TO SR0 THRU PAR/PDR PAIR6
883 003546 012777 000400 175250 BLK20: MOV #400,#SR0 ;TURN ON DESTINATION ONLY PAGING
884 003554 021311 CMP #R3,#R1 ;ICK BOTTOM PAGE BOUNDARY
885 003556 001401 BEQ .+4
886 003560 000000 HALT ;RELOCATION FAILED
887 003562 021412 CMP #R4,#R2 ;ICK UPPER PAGE BOUNDARY
888 003564 001401 BEQ .+4
889 003566 000000 HALT ;RELOCATION FAILED
890 003570 005015 MOV #R0 ;TURN OFF MEMORY MANAG.
891 003572 005370 000000 DEC #(R0) ;MAP PAR 1 PAGE LOWER
892 003576 062701 000100 ADD #100,R1 ;SET UP R1 AND R2 TO REFERENCE
893 003602 062702 000100 ADD #100,R2 ;NEXT VIRTUAL PAGE
894 003606 005367 175364 DEC BLOCKS ;INCREMENT COUNT OF PAGES LEFT
895 003612 001355 BNE BLK20 ;BRANCH IF NOT DONE WITH THIS PAR/PDR PAIR
896 003614 005070 000000 CLR #(R0)

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1005          JCHECK VIRTUAL ADDRESS OF -1 ADDED TO PAR OF 0 (VALUES FOR BIT
1006          IPOSITIONS RELEVANT TO THE ADDRS ONLY), RESULT SHOULD BE PA 17712
1007 004276 005077 174614 CNT2201 CLR 0KPAR1 ISET PAR TO 0
1008 004302 012737 125252 017712 MOV #125252,##DESTAD ILOAD PHYSICAL LOCATION TO BE REFERENCED
1009          IADDRESS 17712
1010 004310 012777 000400 174506 MOV #400,0SR0 ITURN ON DESTINATION - ONLY PAGING
1011 004316 022737 125252 037712 CMP #125252,##37712 IRELOCATE THRU KERNEL PAR/PDR PAIR1
1012 004324 001011 BNE ERR22B IBRANCH ON FAILURE
1013 004326 005037 037712 CLR 037712 ICLEAR THRU KERNEL PAR/PDR PAIR1
1014 004332 005077 174466 CLR 0SR0 ITURN OFF MEMORY MANAG.
1015 004336 005737 017712 TST 017712 ICHECK TO SEE IF CORRECT LOCATION
1016 004342 001401 BEQ .+4 IWAS CLEARED
1017 004344 104006 HLT IRELOCATION FAILED
1018 004346 000403 BR CNT22C IGO TO NEXT CHECK
1019 004350 005077 174450 ERR22B CLR 0SR0 ITURN OFF MEMORY MANAG.
1020 004354 104006 HLT IRELOCATION FAILED IN THE COMPARE
1021          IAT LOCATION ADR22B
1022
1023          JCHECK VIRTUAL ADDRESS OF 1 (BIT 6) ADDED TO PAR OF -1
1024          IRESULTING PHYSICAL ADDRESS SHOULD BE ZERO
1025          INOTE THAT THIS IS A CHECK OF ADDRESS WRAP AROUND
1026 004356 012777 007777 174532 CNT22C1 MOV #7777,0KPAR1 ISET UP PAR TO -1
1027 004364 012737 034343 000000 MOV #34343,0#0 ISET UP A VALUE IN LOCATION TO
1028          IBE REFERENCED (0)
1029 004372 012777 000400 174424 MOV #400,0SR0 ITURN ON DESTINATION-ONLY PAGING
1030 004400 022737 034343 020100 CMP #34343,0#20100 IEFFECTIVELY ADDS 1 TO PAR ADDRESS
1031          ITO GET PHYSICAL ADDRESS OF 0
1032 004406 001013 BNE ERR22C IBRANCH ON FAILURE
1033 004410 012737 000002 020100 MOV #2,##20100 IWRITE SAME LOCATION
1034 004416 005077 174402 CLR 0SR0 ITURN OFF MEMORY MANAG.
1035 004422 022737 000002 000000 CMP #2,0#0 ICHECK LOCATION WHICH SHOULD HAVE
1036 004430 001401 BEQ .+4 IBEEN REFERENCED
1037 004432 104006 HLT IRELOCATION FAILED WHEN WRITING PA 0
1038 004434 000406 BR CNT22D IGO TO NEXT CHECK
1039 004436 005077 174362 ERR22C CLR 0SR0 ITURN OFF MEMORY MANAG.
1040 004442 104006 HLT IRELOCATION FAILED IN THE COMPARE
1041 004444 012737 000002 000000 MOV #2,0#0 IAT LOCATION ADR22C
1042
1043          JCHECK VIRTUAL ADDRESS OF -1 (BITS 6-12) ADDED TO PAR OF 1
1044          I(PLUS HIGH BITS SET, BUT THEY DON'T ALTER CARRY CONDITION TESTED FOR)
1045          IRESULTING PHYSICAL ADDRESS SHOULD BE ZERO
1046 004452 012777 007601 174436 CNT22D1 MOV #7601,0KPAR1 ISET UP PAR TO 1, WITH HIGH BITS SET
1047 004460 012737 043434 000000 MOV #43434,0#0 ISET UP A VALUE IN LOCATION TO
1048          IBE REFERENCED (0)
1049 004466 012777 000400 174330 MOV #400,0SR0 ITURN ON DESTINATION-ONLY PAGING
1050 004474 022737 043434 037700 CMP #43434,0#37700 IALL HIGH BITS OF VA ARE 1, ADDED TO
1051          IA ONE IN LOWEST BIT OF PAR TO PROPAGATE
1052          ICARRY - RESULTING PHYSICAL ADDRESS 0
1053 004502 001013 BNE ERR22D IBRANCH ON FAILURE
1054 004504 012737 000002 037700 MOV #2,##37700 IWRITE SAME LOCATION
1055 004512 005077 174306 CLR 0SR0 ITURN OFF MEMORY MANAG.
1056 004516 022737 000002 000000 CMP #2,0#0 ICHECK LOCATION WHICH SHOULD HAVE
1057          IBEEN REFERENCED
1058 004524 001401 BEQ .+4

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1059          IRELOCATION FAILED WHEN WRITING PA 0
1060 004530 000406 BR CNT22E IGO TO NEXT CHECK
1061 004532 005077 174266 ERR22D1 CLR 0SR0 ITURN OFF MEMORY MANAG.
1062 004536 104006 HLT IRELOCATION FAILED IN THE COMPARE
1063          IAT LOCATION ADR22D
1064 004540 012737 000002 000000 MOV #2,0#0 IRESTORE LOCATION REFERENCED
1065
1066          JCHECK VIRTUAL ADDRESS -1 ADDED TO PAR OF -1
1067          I(SHOULD GIVE RESULTING PA 17677)
1068          INOTE THAT THIS IS A CASE OF ADDRESS WRAP AROUND
1069 004546 012777 007777 174342 CNT22E1 MOV #7777,0KPAR1 ISET UP PAR TO -1
1070 004554 013746 017676 MOV #17676,-(SP) ISAVE CONTENTS OF LOCATION TO BE
1071          IREFERENCED
1072 004560 012737 076767 017676 MOV #76767,##17676 ILOAD LOCATION TO BE REFERENCED
1073 004566 012777 000400 174230 MOV #400,0SR0 ITURN ON DESTINATION-ONLY PAGING
1074 004574 122737 000175 037777 CMPB #175,##37777 IREAD LOCATION (VA==1, PAR=-1)
1075          ISHOULD GIVE PA 17677 (THRU KERNEL PAR1)
1076 004602 001012 BNE ERR22E IBRANCH ON FAILURE
1077 004604 105037 037777 CLR #37777 IWRITE SAME LOCATION
1078 004610 005077 174210 CLR 0SR0 ITURN OFF MEMORY MANAG.
1079 004614 022737 000367 017676 CMP #367,##17676 ICHECK TO SEE IF CORRECT LOCATION
1080 004622 001401 BEQ .+4 IWAS CLEARED (HIGH BYTE)
1081 004624 104006 HLT IRELOCATION FAILED WHEN CLEARING
1082          I(PHYSICAL ADDRESS 17667 (THRU
1083          IKERNEL PAR1)
1084 004626 000403 BR END22E ITURN OFF MEMORY MANAG.
1085 004630 005077 174170 ERR22E1 CLR 0SR0 IRELOCATION FAILED IN THE COMPARE AT
1086          ILOCATION ADR22E
1087 004636 012637 017676 END22E1 MOV (SP)+,##17676 IRESTORE LOCATION REFERENCED
1088
1089          I(SHOW THAT SETTING SR0<0> TURNS ON FULL RELOCATION
1090          I(SHOW THAT ALL ADDRESS CALCULATIONS ARE RELOCATED
1091          I(SHOW THAT INIT CLEARS SR0<0> AND TURNS OFF RELOCATION
1092 TEST221 SCOPE
1093 004642 104400 MOV #KSTACK,SP IINITIALIZE KERNEL STACK POINTER
1094 004644 012706 JSR 011530 ICHECK TEST SEQUENCE + INIT SR0
1095 004646 000022 ZI ITEST NUMBER
1096 004648 104006 HLT ITEST EXECUTED OUT OF SEQUENCE
1097 004650 012767 000010 010770 MOV #10,ICOUNT IDROP ITERATION COUNT
1098 004652 004767 010475 JSR 010475 INITIALLY CLEAR ALL MEMORY MANAG. REGISTERS
1099 004654 012777 000001 174214 MOV #1,0KPAR0 IMAP KERNEL PAGE 0 TO
1100 004656 012777 077406 174166 MOV #77406,0KPDRO IBANK 0 OFFSET BY 1 BLOCK
1101 004658 004767 011556 JSR PC,KERN7 IMAP KERNEL PAR/PDR 7 TO EXT BANK
1102 004712 012767 052525 012772 MOV #52525,DESTAD IINITIALIZE LOCATION TO BE REFERENCED
1103 004720 012777 000001 174076 MOV #1,0SR0 ITURN ON RELOCATION
1104 004726 000000 ADD231 HALT IWITH RELOCATION ON, SHOULD FETCH
1105 004730 000000 HALT IPROM 1 BLOCK ABOVE THIS
1106 004732 000000 HALT I(ADD23A)
1107 004734 000000 HALT
1108 004736 000000 HALT
1109 004740 000000 HALT
1110 004742 000001 174054 BIT #1,0SR0 IWHEN MEMORY MANAG. IS TURNED OFF, NEXT
1111          IFETCH SHOULD BE FROM HERE -
1112 004750 001401 BEQ .+4 ICHECK BIT 0, SR0

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1113 004752 104006 HLT IMEMORY MANAG, OFF BUT SR0<0> STILL SET
1114 IAFTER AN INIT
1115 004754 005077 174944 CLR #SR0
1116 004760 000432 BR EXIT23
1117 005026 .#ADD23+100
1118 005026 022737 052525 017612 CMP #52525,##DESTAD-100 WHEN MEMORY MANAG. IS TURNED ON, NEXT
1119 INSTRUCTION EXECUTED SHOULD
1120 BE HERE - CK RELOCATION OF SOURCE
1121 AND DESTINATION CALCULATIONS
1122 005034 001401 BEQ .+4 RELOCATION FAILED IN A SOURCE OR
1123 005036 000000 HALT DESTINATION ADDRESS CALCULATION
1124 WITH FULL RELOCATION ON (SR0<0>SET)
1125 005040 000005 RESET ISSUE INIT TO TURN OFF MEMORY MANAG.
1126 005042 000000 HALT INIT DIDN'T TURN OFF MEMORY MANAG.
1127 005044 000777 BR
1128 005046 000240 EXIT23: NOP
1129
1130 ISHOW THAT A DATO OF 0 TO SR0<0> WILL CLEAR SR0<0> AND
1131 ITURN OFF RELOCATION
1132 005050 104400 TEST23: SCOPE
1133 005052 012706 001000 MOV #KSTACK,SP IINITIALIZE KERNEL STACK POINTER
1134 005056 004767 011322 JSR PC,ORDER ICHECK TEST SEQUENCE + INIT SR0
1135 005062 000023 23 ITEST NUMBER
1136 005064 104006 HLT ITEST EXECUTED OUT OF SEQUENCE
1137 005066 012767 002900 010562 MOV #2000,ICOUNT IRESTORE ITERATION COUNT
1138 005074 004767 010270 JSR X7,CLRALL IINITIALLY CLEAR ALL MEMORY MANAG, REGISTERS
1139 005100 012777 000901 174006 MOV #1,#KPAR0 IMAP KERNEL PAGE 0 TO
1140 005106 012777 077406 173760 MOV #77406,#KPDRO IBANK 0 OFFSET BY 1 BLOCK
1141 005114 004767 011350 JSR PC,KERN7 IMAP KERNEL PAR/PDR 7 TO EXT BANK
1142 005120 012777 000901 173676 MOV #1,#SR0 ITURN ON MEMORY MANAG.
1143 005126 000000 ADD24: HALT WHEN MEMORY MANAG. IS TURNED ON, SHOULD
1144 005130 000000 HALT IFETCH FROM THIS ADDRESS PLUS
1145 005132 000000 HALT IONE BLOCK (ADD24)
1146 005134 000240 NOP
1147 005136 000240 NOP
1148 005140 032777 000001 173656 BIT #1,#SR0 IAFTER MEMORY MANAG. IS TURNED OFF, CHECK
1149 005146 001401 BEQ .+4 ISR0<0>
1150 005150 104006 HLT IMEMORY MANAG, OFF BUT SR0<0> STILL
1151 ISET AFTER A BIC #1,#SR0
1152 005152 000433 BR EXIT24
1153
1154 .#ADD24+100
1155 005226 042777 000001 173570 BIC #1,#SR0 WHEN MEMORY MANAG. IS TURNED ON, SHOULD
1156 IRELOCATE FETCH TO HERE = TURN
1157 IOFF MEMORY MANAG, VIA BIC OF SR0<0>
1158 005234 000000 HALT IMEMORY MANAG, STILL RELOCATING AFTER
1159 005236 000005 RESET IBIC OF SR0<0>
1160 005240 000777 BR
1161 005242 000240 EXIT24: NOP
1162
1163 ISHOW THAT A REFERENCE TO A NON-RESIDENT PAGE
1164 IWill ABORT TO THE MEMORY MANAG, ABORT VECTOR ADDRESS (250)
1165 IWITH BIT 15 OF SR0 SET. SR0 AND SR2 ARE CHECKED FOR
1166 ITHE CORRECT VALUES, AS ARE KPDR0 AND KPDR1

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1167 ISHOW THAT BIT 15 OF SR0 CAN BE CLEARED
1168 ISHOW THAT SR2 IS READ ONLY
1169
1170 005244 104400 TEST24: SCOPE
1171 005246 012706 001000 MOV #KSTACK,SP IINITIALIZE KERNEL STACK POINTER
1172 005252 004767 011126 JSR PC,ORDER ICHECK TEST SEQUENCE + INIT SR0
1173 005256 000024 24 ITEST NUMBER
1174 005260 104006 HLT ITEST EXECUTED OUT OF SEQUENCE
1175 005262 004767 010102 JSR X7,CLRALL ICLEAR ALL MEMORY MANAG, REGISTERS
1176 005266 012777 077406 173600 MOV #77406,#KPDRO IMAP KERNEL 0 TO BANK 0, RW, AK
1177 005274 004767 011170 JSR PC,KERN7 IMAP KERNEL PAR/PDR 7 TO EXT BANK
1178 005300 012777 005334 173656 MOV #INT25,#KTVEC ISETUP RETURN VECTOR
1179 005306 005077 173654 CLR #KSTSA
1180 005312 012704 020000 MOV #20000,R4 IUSE R4 TO REFERENCE NR KERNEL 1
1181 005316 005277 173502 INC #SR0 ITURN ON MEMORY MANAG.
1182 005322 005724 ADR25: TST IREFERENCE NR KERNEL 1
1183 005324 000000 ADR25A: HALT I SHOULD HAVE ABORTED ALREADY
1184 005326 005077 173472 CLR #SR0 ITURN OFF MEMORY MANAG.
1185 005332 000442 BR DON25
1186 005334 017701 173464 INT25: MOV #SR0,R1 ISAVE CONTENTS OF SR0
1187 005340 005377 173460 DEC #SR0 ITURN OFF MEMORY MANAG.
1188 005344 022701 100003 CMP #100003,R1 ICHECK SAVED CONTENTS OF SR0
1189 005350 001401 BEQ .+4
1190 005352 104006 HLT ISR0 INCORRECT AFTER NR ABORT
1191 I(SEE SAVED CONTENTS IN R1)
1192 005354 022777 005322 173450 CMP #ADR25,#SR2 ICK SR2
1193 005362 001401 BEQ .+4
1194 005364 104006 HLT ISR2 INCORRECT-SHOULD CONTAIN ADDRESS
1195 IOF LAST FETCH BEFORE THE ABORT
1196 005366 005077 173440 CLR #SR2 ITRY TO WRITE INTO SR2
1197 005372 022777 005322 173432 CMP #ADR25,#SR2 ISR2 SHOULD BE READ ONLY
1198 005400 001401 BEQ .+4
1199 005402 104006 HLT ISR2 NOT READ ONLY
1200 005404 022777 077506 173462 CMP #77506,#KPDRO
1201 005412 001401 BEQ .+4
1202 005414 104006 HLT IKERNEL PDR 0 INCORRECT
1203 I# BIT SHOULD HAVE BEEN SET BY THE STACK WRITE
1204 005416 005777 173454 TST #KPDR1
1205 005422 001401 BEQ .+4
1206 005424 104006 HLT IKERNEL PDR 1 INCORRECT
1207 005426 021627 005324 CMP (R6),#ADR25A ICHECK VALUE PUSHED ON STACK
1208 005432 001401 BEQ .+4
1209 005434 104006 HLT
1210 005436 022626 CMP (R6)+,(R6)+ INCORRECT VALUE ON STACK
1211 005440 005077 173522 DON25: CLR #KSTSA IRESTORE STACK
1212 005444 016777 173516 MOV #KTSTA,#KTVEC ICHANGE TRAP VECTOR TO CAUSE A
1213 IHALT ON A FALSE TRAP
1214 ISHOW THAT WRITING A PAGE WILL SET THE W BIT IN THE CORRESPONDING
1215 IPDR, AND THAT NO OTHER W BITS SET AT THE SAME TIME
1216 ISHOW THAT WRITING THE PDR (VIA A DATO) WILL CLEAR THE W BIT
1217 ISINCE THIS IS DONE FOR ALL PDR'S, THIS IS ALSO
1218 IA TEST OF INDIRECT ADDRESSING (VIA A VIRTUAL ADDRESS) OF THE PDR'S
1219 005452 104400 TEST25: SCOPE
1220 005454 012706 001000 MOV #KSTACK,SP IINITIALIZE KERNEL STACK POINTER
1221 005460 004767 010720 JSR PC,ORDER ICHECK TEST SEQUENCE + INIT SR0

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1321 006162 005277 172636      INC      #SR0      RETURN ON MEMORY MANAG.
1322 006166 000004      IOT      #SR0      /SHOULD USE STACK IN KERNEL ADDRESS SPACE
1323 006170 000240      NOP
1324 006172 005011      KRET34: CLR    #R1      RETURN OFF MEMORY MANAG.
1325 006174 012737 006226 000020      MOV    #URET34,#20    /SETUP FOR IOT TO USER
1326 006202 012737 140000 000022      MOV    #140000,#22
1327 006210 012737 140000 177776      MOV    #140000,#PS
1328 006216 005277 172602      INC      #SR0      RETURN ON MEMORY MANAG.
1329 006222 000004      IOT      #SR0      /SHOULD USE STACK IN USER SPACE
1330 006224 000240      NOP
1331 006226 005011      URET34: CLR    #R1      RETURN OFF MEMORY MANAG.
1332 006230 022737 006170 000474      CMP    #KRET34=2,#474
1333 006236 001401      BEQ    .+4
1334 006240 104006      HLT
1335 006242 022737 000000 000476      CMP    #0,#476      /KERNEL STACK CONTENTS WRONG. PC NOT WHERE IT
                        /SHOULD HAVE BEEN PUSHED OR

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1336 006250 001401      BEQ    .+4      /VALUE WRONG
1337 006252 104006      HLT      /KERNEL STACK WRONG-TRAP STATUS NOT
1338 006254 022737 006224 000074      CMP    #URET34=2,#74    /NOT WHERE IT SHOULD HAVE BEEN PUSHED
1339 006262 001401      BEQ    .+4      /OR VALUE WRONG
1340 006264 104006      HLT      /USER STACK WRONG-PC NOT WHERE
1341 006266 022737 140000 000076      CMP    #140000,#76    /IT SHOULD HAVE BEEN PUSHED
1342 006274 001401      BEQ    .+4      /OR VALUE WRONG
1343 006276 104006      HLT      /USER STACK WRONG-TRAP STATUS
1344      /NOT WHERE IT SHOULD HAVE BEEN
1345      /PUSHED OR VALUE WRONG
1346 006300 012737 000076 000074      MOV    #76,#74      /REINITIALIZE LOCATIONS CHECKED
1347 006306 005037 000076      CLR    #76
1348 006312 012737 000476 000474      MOV    #476,#474
1349 006320 005037 000476      CLR    #476
1350 006324 012706 001000      MOV    #KSTACK,SP
1351
1352      /SHOW THAT TRAP,EMT, AND INTERRUPTS TAKE VECTORS FROM KERNEL
1353      /IRREGARDLESS OF THE MODE AT THE TIME OF THE TRAP SEQUENCE
1354      /ALSO SHOW THAT ODD-ADDRESS TRAP (AN "INTERNAL"
1355      /TRAP) TAKES ITS VECTOR FROM KERNEL
1356      /NOTE THAT IF DUAL ADDRESSING OCCURS, THE ERROR
1357      /ADDRESS WILL BE USED (THE 0 OVERRIDES THE 1)
1358 006330 104400      TEST30: SCOPE
1359 006332 012706 001000      MOV    #KSTACK,SP      /INITIALIZE KERNEL STACK POINTER
1360 006336 004767 010042      JSR    PC,ORDER      /CHECK TEST SEQUENCE + INIT SR0
1361 006342 000030      30      /TEST NUMBER
1362 006344 104006      HLT      /TEST EXECUTED OUT OF SEQUENCE
1363 006346 005077 172452      CLR    #SR0
1364 006352 004767 007036      JSR    X7,RWALL      /MAP ALL PAR/PDR PAIR'S RW, 4K, BANK 0
1365 006356 012777 000001 172470      MOV    #1,#UPAR0      /OFFSET USER 0 1 PAGE
1366 006364 004767 010100      JSR    PC,KERN7      /MAP KERNEL PAR/PDR 7 TO EXT BANK
1367 006370 012777 007600 172474      MOV    #7600,#UPART7 /MAP USER 7 TO THE EXTERNAL BANK
1368 006376 016701 172422      MOV    SR0,R1      /SETUP R1 TO REFERENCE SR0
1369 006402 012737 140000 177776      MOV    #140000,#PS    /SETUP USER STACK
1370 006410 012706 000400      MOV    #USTACK,SP
1371 006414 005037 177776      CLR    #PS
1372 006420 012706 001000      MOV    #KSTACK,SP    /SETUP THE KERNEL STACK POINTER
1373 006424 012737 006564 000136      MOV    #NG35B,#130    /SETUP FAILURE RETURN
1374 006432 012737 006602 000030      MOV    #OK35B,#30     /SETUP SUCCESS RETURN
1375 006440 005037 000132      CLR    #132
1376 006444 005037 000032      CLR    #32
1377 006450 012737 140000 177776      MOV    #140000,#PS    /SET MODE TO USER
1378 006456 005277 172342      INC    #SR0      /TURN ON MEMORY MANAG.
1379 006462 000000      0
1380 006464 000000      0
1381 006466 000000      0
1382 006470 000000      0
1383 006472 000000      0
1384 006474 000000      0
1385 006476 000000      0
1386 006500 000000      0
1387 006502 000000      0
1388 006504 000000      0
1389 006506 000000      0

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1498 007142 000000      0
1499 007144 000000      0
1500 007146 000000      0
1501 007150 000000      0
1502 007152 000000      0
1503 007154 000000      0
1504 007156 000000      0
1505 007160 000000      0
1506 007162 000000      0
1507 007164 000000      0
1508 007166 000000      0
1509 007170 000000      0
1510 007172 012737 000100 177564      MOV      #100,#177564      /JSET TTY INTERRUPT ENABLE=SHOULD
1511 007200 000240      NOP      /INTERRUPT IMMEDIATELY
1512 007202 000240      NOP
1513 007204 005011      CLR      #R1      /TURN OFF MEMORY MANAG.
1514 007206 005077 171604      CLR      #TCSR      /CLEAR TTY IE
1515 007212 104006      HLT      /TTY FAILED TO INTERRUPT
1516 007214 000412      BR      ODDAD
1517 007216 022626      NG35D: CMP      (SP)+,(SP)+      /RESTORE STACK POINTER
1518 007220 005011      CLR      #R1      /TURN OFF MEMORY MANAG.
1519 007222 005077 171570      CLR      #TCSR      /CLEAR TTY IE
1520 007226 104006      HLT      /TTY INTERRUPT DIDN'T GO THRU KERNEL
1521 007230 000404      BR      ODDAD
1522 007232 022626      OK35D: CMP      (SP)+,(SP)+      /RESTORE STACK POINTER
1523 007234 005011      CLR      #R1      /TURN OFF MEMORY MANAG.
1524 007236 005077 171554      CLR      #TCSR
1525 007242 012737 000066 000064 ODDAD: MOV      #66,#64      /RESTORE TTY VECTOR RETURN TO CAUSE
1526 007250 005037 000066      CLR      #66      /A HALT ON A FALSE INTERRUPT
1527 007254 012737 000162 000160      MOV      #162,#160
1528 007262 005037 000162      CLR      #162
1529 007266 005037 177776      CLR      #PS
1530 007272 012737 007436 000104      MOV      #NG35E,#104      /SETUP INTERNAL TRAP FAILURE RETURN
1531 007300 012737 000340 000106      MOV      #340,#106
1532 007306 012737 007446 000004      MOV      #OK35E,#4      /SETUP INTERNAL TRAP SUCCESS RETURN
1533 007314 005037 000006      CLR      #6
1534 007320 012737 140000 177776      MOV      #140000,#PS      /SET MODE TO USER
1535 007326 005277 171472      INC      #SR0      /TURN ON MEMORY MANAG.
1536 007332 000000      0
1537 007334 000000      0
1538 007336 000000      0
1539 007340 000000      0
1540 007342 000000      0
1541 007344 000000      0
1542 007346 000000      0
1543 007350 000000      0
1544 007352 000000      0
1545 007354 000000      0
1546 007356 000000      0
1547 007360 000000      0
1548 007362 000000      0
1549 007364 000000      0
1550 007366 000000      0
1551 007370 000000      0

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1552 007372 000000      0
1553 007374 000000      0
1554 007376 000000      0
1555 007400 000000      0
1556 007402 000000      0
1557 007404 000000      0
1558 007406 000000      0
1559 007410 000000      0
1560 007412 000000      0
1561 007414 000000      0
1562 007416 000000      0
1563 007420 000000      0
1564 007422 000000      0
1565 007424 000000      0
1566 007426 000000      0
1567 007430 000000      0
1568 007432 005737 000001      TST      #1      /ODD ADDRESS REFERENCE - AN "INTERNAL
1569                                /TRAP" SHOULD OCCUR
1570 007436 022626      NG35E: CMP      (SP)+,(SP)+      /RESTORE STACK POINTER
1571 007440 005011      CLR      #R1      /TURN OFF MEMORY MANAG.
1572 007442 104006      HLT      /ODD ADDRESS TRAP DIDN'T TAKE
1573                                /VECTOR FROM KERNEL
1574 007444 000407      BR      END35
1575 007446 022626      OK35E: CMP      (SP)+,(SP)+      /RESTORE STACK POINTER
1576 007450 005011      CLR      #R1      /TURN OFF MEMORY MANAG.
1577 007452 032737 000340 177776      BIT      #340,#PS      /WAS CORRECT STATUS PICKED UP?
1578 007460 001401      BEQ     .44      /YES= BRANCH
1579 007462 104006      HLT      /PICKED UP NEW STATUS WORD FROM USER SPACE
1580 007464 012737 000006 000004 END35: MOV      #6,#4      /RESTORE TRAP CATCHER
1581 007472 012737 000106 000104      MOV      #106,#104
1582
1583
1584 /SHOW THAT THE ABORT LOGIC "LOCKS" SR0, AND SR2 AFTER A NR
1585 /ABORT UNTIL THE CORRESPONDING ABORT BIT IS CLEARED IN SR0, WHEN
1586 /THEY RESUME TRACKING. A NR ERROR SHOULD STILL ABORT TO 250 EVEN
1587 /WHEN BIT 15 (SR0) IS ALREADY SET
1588 TEST31: SCOPE
1589 007500 104400      MOV      #KSTACK,SP      /INITIALIZE KERNEL STACK POINTER
1590 007502 012706 001000      JSR     PC,ORDER      /CHECK TEST SEQUENCE + INIT SR0
1591 007506 004767 006672      31      /TEST NUMBER
1592 007512 000031      HLT     /TEST EXECUTED OUT OF SEQUENCE
1593 007514 104006      JSR     /CLEAR ALL MEMORY MANAG. REGISTERS
1594 007516 004767 005646      JSR     /MAP KERNEL PAR/PDR 7 TO EXT BANK
1595 007522 004767 006742      JSR     /MAP KERNEL 0 RW,RK,BANK0
1596 007526 012777 077406 171340      MOV      #77406,#KPDR0
1597 007534 012777 077400 171334      MOV      #77400,#KPDRC1
1598 007542 012777 007576 171414      MOV      #INT36,#KTVEC1
1599 007550 005077 171412      CLR      #KTSTA
1600 007554 005277 171244      #SR0      /TURN ON MEMORY MANAG.
1601 007560 013737 037776 037776 ADR36: MOV      #037776,#037776      /REFERENCE KERNEL 1 = 1ST ABORT
1602 007566 005077 171232      CLR      #SR0      /TURN OFF MEMORY MANAG.
1603 007572 104006      HLT     /REFERENCE TO KERNEL 1
1604 007574 000510      BR      /DIDN'T ABORT
1605 007576 042777 000001 171220 INT36: BIC     #1,#SR0      /TURN OFF MEMORY MANAG.
1606 007604 022777 100002 171212      CMP     #100002,#SR0      /CHECK SR0

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1606 007612 001401 BEQ .+4
1607 007614 104006 HLT
1608 007616 012777 007652 171340 MOV #INT36A,#KTVEC JSR0 INCORRECT AFTER NR ABORT
1609 007624 022626 CMP (R6)+,(R6)+ ISETUP NEW RETURN VECTOR
1610 007626 012702 037776 MOV #37776,R2 IRESTORE STACK POINTER
1611 007632 052777 000001 171164 BLS #1,#SR0 ISETUP R2 TO REFERENCE KERNEL 1
1612 007640 012242 MOV (R2)+,-(R2) IRETURN ON MEMORY MANAG.
1613 007642 005077 171156 ADR36A1 CLR #SR0 IREFERENCE KERNEL 1 =2ND ABORT
1614 007646 104006 HLT IRETURN OFF MEMORY MANAG.
1615 007650 000462 BR DONE36 I2ND REFERENCE TO KERNEL 1
1616 007652 042777 000001 171144 INT36A1 BIC #1,#SR0 IRETURN OFF MEMORY MANAG.
1617 007660 022777 100002 171136 CMP #100002,#SR0 ICHECK SR0
1618 007666 001401 BEQ .+4
1619 007670 104006 HLT JSR0 INCORRECT AFTER 2ND NR ABORT
1620 007672 022777 007560 171132 CMP #ADR36,#SR2 ICHECK SR2
1621 007700 001401 BEQ .+4
1622 007702 104006 HLT JSR2 DOESN'T CONTAIN VALUE FROM 1ST ABORT
1623 007704 021627 007642 CMP (R6),#ADR36A ICHECK ADDRESS PUSHED ON STACK
1624 007710 001401 BEQ .+4
1625 007712 104006 HLT IINCORRECT ADDRESS ON STACK
1626 007714 022626 CMP (R6)+,(R6)+ IRESTORE STACK POINTER
1627 007716 012777 007752 171240 MOV #INT36B,#KTVEC ICHANGE RETURN ADDRESS
1628 007724 005077 171074 CLR #SR0 ICLEAR NR ERROR BIT=SHOULD
I"UNLOCK" ERROR TRACKING
1630 007730 012702 037776 MOV #37776,R2 ISETUP R2 TO REFERENCE KERNEL 1
1631 007734 005277 171064 INC #SR0 IRETURN ON MEMORY MANAG.
1632 007740 012242 ADR36B1 MOV (R2)+,-(R2) I3RD NR REFERENCE, ERROR BIT WAS CLEARED
1633 007742 005077 171056 ADR36C1 CLR #SR0 IRETURN OFF MEMORY MANAG.
1634 007746 104006 HLT I3RD REFERENCE TO KERNEL 1
1635 007750 000422 BR DONE36 IDIDN'T ABORT
1636 007752 042777 000001 171044 INT36B1 BIC #1,#SR0 IRETURN OFF MEMORY MANAG.
1637 007760 022777 100002 171036 CMP #100002,#SR0 ICHECK SR0
1638 007766 001401 BEQ .+4
1639 007770 104006 HLT JSR0 INCORRECT
1640 007772 022777 007740 171032 CMP #ADR36B,#SR2 ICHECK SR2
1641 010000 001401 BEQ .+4
1642 010002 104006 HLT JSR2 INCORRECT - SHOULD CONTAIN
ILAST FETCH ADDRESS BEFORE ABORT
1643 ICHECK STACK
1644 010004 022716 007742 CMP #ADR36C,(SP)
1645 010010 001401 BEQ .+4
1646 010012 104006 HLT IPC ON STACK INCORRECT
1647 010014 022626 CMP (R6)+,(R6)+ IRESTORE STACK POINTER
1648 010016 005077 171002 DONE361 #SR0 ICLEAR ERROR BIT
1649 010022 005077 171140 CLR #KTSTA ICHANGE TRAP RETURN TO CAUSE A HALT
1650 010026 016777 171134 171130 MOV #KTSTA,#KTVEC ION A FALSE INTERRUPT
1651
1652 ISHOW THAT THE ABORT LOGIC "LOCKS" SR0, AND SR2 AFTER A PL
1653 IABORT UNTIL THE CORRESPONDING ABORT BIT IS CLEARED IN SR0, WHEN
1654 ITHEY RESUME TRACKING, A PL ERROR SHOULD STILL ABORT TO 250 EVEN
1655 IWHEN BIT 14 (SR0) IS ALREADY SET
1656 010034 104400 TEST32: SCOPE
1657 010036 012706 001000 MOV #KSTACK,SP IINITIALIZE KERNEL STACK POINTER
1658 010042 004767 006336 JSR PC,ORDER ICHECK TEST SEQUENCE + INIT SR0
1659 010046 000032 32 ITEST NUMBER

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1660 010050 104006 HLT
1661 010052 004767 005312 JSR X7,CLRALL ICLEAR ALL MEMORY MANAG, REGISTERS
1662 010056 004767 006406 JSR PC,KERN7 IMAP KERNEL PAR/PDR 7 TO EXT BANK
1663 010062 012777 007406 171004 PC,KERN7 #77406,#KPPDR IMAP KERNEL 0 RW,RK,BANK0
1664 010070 012777 017406 171000 MOV #17406,#KPPDR IMAP KERNEL 1 PL,1 K,BANK0
1665 010076 012777 010132 171060 MOV #INT37,#KTVEC ISETUP RETURN VECTOR
1666 010104 005077 171056 CLR #KTSTA
1667 010110 005277 170710 INC #SR0 IRETURN ON MEMORY MANAG.
1668 010114 013737 037776 ADR371 MOV #37776,#37776 IREFERENCE KERNEL 1 = 1ST ABORT
1669 010122 005077 170676 CLR #SR0 IRETURN OFF MEMORY MANAG.
1670 010126 104006 HLT IREFERENCE TO KERNEL 1
1671 010130 000510 BR DONE37 IDIDN'T ABORT
1672 010132 042777 000001 170664 INT371 BIC #1,#SR0 IRETURN OFF MEMORY MANAG.
1673 010140 022777 040002 170656 CMP #40002,#SR0 ICHECK SR0
1674 010146 001401 BEQ .+4
1675 010150 104006 HLT
1676 010152 012777 010206 171004 MOV #INT37A,#KTVEC JSR0 INCORRECT AFTER PL ABORT
1677 010160 022626 CMP (R6)+,(R6)+ ISETUP NEW RETURN VECTOR
1678 010162 012702 037776 MOV #37776,R2 IRESTORE STACK POINTER
1679 010166 052777 000001 170630 BLS #1,#SR0 ISETUP R2 TO REFERENCE KERNEL 1
1680 010174 012242 MOV (R2)+,-(R2) IRETURN ON MEMORY MANAG.
1681 010176 005077 170622 ADR37A1 CLR #SR0 IREFERENCE KERNEL 1 =2ND ABORT
1682 010202 104006 HLT IRETURN OFF MEMORY MANAG.
1683 010204 000462 BR DONE37 I2ND REFERENCE TO KERNEL 1
1684 010206 042777 000001 170610 INT37A1 BIC #1,#SR0 IDIDN'T ABORT
1685 010214 022777 040002 170602 CMP #40002,#SR0 IRETURN OFF MEMORY MANAG.
1686 010222 001401 BEQ .+4 ICHECK SR0
1687 010224 104006 HLT
1688 010226 022777 010114 170576 CMP #ADR37,#SR2 JSR0 INCORRECT AFTER 2ND PL ABORT
1689 010234 001401 BEQ .+4 ICHECK SR2
1690 010236 104006 HLT
1691 010240 021627 010176 CMP (R6),#ADR37A JSR2 DOESN'T CONTAIN VALUE FROM 1ST ABORT
1692 010244 001401 BEQ .+4 ICHECK ADDRESS PUSHED ON STACK
1693 010246 104006 HLT
1694 010250 022626 CMP (R6)+,(R6)+ IINCORRECT ADDRESS ON STACK
1695 010252 012777 010306 170704 MOV #INT37B,#KTVEC IRESTORE STACK POINTER
1696 010260 005077 170540 CLR #SR0 ICHANGE RETURN ADDRESS
I"UNLOCK" ERROR TRACKING
1698 010264 012702 037776 MOV #37776,R2 ISETUP R2 TO REFERENCE KERNEL 1
1699 010270 005277 170530 INC #SR0 IRETURN ON MEMORY MANAG.
1700 010274 012242 ADR37B1 MOV (R2)+,-(R2) I3RD PL REFERENCE, ERROR BIT WAS CLEARED
1701 010276 005077 170522 ADR37C1 CLR #SR0 IRETURN OFF MEMORY MANAG.
1702 010302 104006 HLT I3RD REFERENCE TO KERNEL 1
1703 010304 000422 BR DONE37 IDIDN'T ABORT
1704 010306 042777 000001 170510 INT37B1 BIC #1,#SR0 IRETURN OFF MEMORY MANAG.
1705 010314 022777 040002 170502 CMP #40002,#SR0 ICHECK SR0
1706 010322 001401 BEQ .+4
1707 010324 104006 HLT JSR0 INCORRECT
1708 010326 022777 010274 170476 CMP #ADR37B,#SR2 ICHECK SR2
1709 010334 001401 BEQ .+4
1710 010336 104006 HLT JSR2 INCORRECT - SHOULD CONTAIN
ILAST FETCH ADDRESS BEFORE ABORT
1711 ICHECK STACK
1712 010340 022716 010276 CMP #ADR37C,(SP)
1713 010344 001401 BEQ .+4

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1714 010346 104006      HLT
1715 010350 022626      CMP      (R6)+,(R6)+      ;IPC ON STACK INCORRECT
1716 010352 005077 170446      DONE37: CLR      #SR0      ;RESTORE STACK POINTER
1717 010356 005077 170604      CLR      #KTSTA      ;CLEAR ERROR BIT
1718 010362 016777 170600 170574      MOV      KTSTA,#KTVEC    ;CHANGE TRAP RETURN TO CAUSE A HALT
                                ;ON A FALSE INTERRUPT
1719
1720
1721      ;SHOW THAT THE ABORT LOGIC "LOCKS" SR0, AND SR2 AFTER A ACC
1722      ;ABORT UNTIL THE CORRESPONDING ABORT BIT IS CLEARED IN SR0, WHEN
1723      ;THEY RESUME TRACKING, A ACC ERROR SHOULD STILL ABORT TO 250 EVEN
1724      ;WHEN BIT 13 (SR0) IS ALREADY SET
1724 010370 104400      TEST33: SCOPE
1725 010372 012706 001000      MOV      #KSTACK,SP      ;INITIALIZE KERNEL STACK POINTER
1726 010376 004767 006002      JSR      PC,ORDER        ;CHECK TEST SEQUENCE + INIT SR0
1727 010402 000033      HLT
1728 010404 104006      HLT
1729 010406 004767 004756      JSR      X7,CLRALL       ;TEST NUMBER
1730 010412 004767 006052      JSR      PC,KERN7        ;TEST EXECUTED OUT OF SEQUENCE
1731 010416 012777 077406 170450      MOV      #77400,#KPDR0   ;CLEAR ALL MEMORY MANAG. REGISTERS
1732 010424 012777 077402 170444      MOV      #77402,#KPDRI   ;MAP KERNEL PAR/PDR 7 TO EXT BANK
1733 010432 012777 010466 170524      MOV      #INT40,#KTVEC   ;MAP KERNEL 0 RW,RK,BANK0
1734 010440 005077 170522      CLR      #KTSTA          ;SETUP KERNEL 1 ACC,0 K,BANK0
1735 010444 005277 170354      INC      #SR0            ;RETURN RETURN VECTOR
1736 010450 013737 037776 037776      ADR40: MOV      #37776,#37776 ;TURN ON MEMORY MANAG.
1737 010456 005077 170342      CLR      #SR0            ;REFERENCE KERNEL 1 - 1ST ABORT
1738 010462 104006      HLT
1739 010464 000510      BR       DONE40          ;TURN OFF MEMORY MANAG.
1740 010466 042777 000001 170330      INT40: BIC      #1,#SR0   ;REFERENCE TO KERNEL 1
1741 010474 022777 020002 170322      CMP      #20002,#SR0    ;DIDN'T ABORT
1742 010502 001401      BEQ     .+4              ;TURN OFF MEMORY MANAG.
1743 010504 104006      HLT
1744 010506 012777 010542 170450      MOV      #INT40A,#KTVEC  ;CHECK SR0
1745 010514 022626      CMP      (R6)+,(R6)+
1746 010516 012702 037776      MOV      #37776,R2
1747 010522 052777 000001 170274      BIS      #1,#SR0
1748 010530 012242      MOV      (R2)+,(R2)
1749 010532 005077 170266      ADR40A: CLR     #SR0     ;REFERENCE KERNEL 1 - 2ND ABORT
1750 010536 104006      HLT
1751 010542 000462      BR       .+4
1752 010544 042777 000001 170254      INT40A: BIC     #1,#SR0   ;TURN OFF MEMORY MANAG.
1753 010550 022777 020002 170246      CMP      #20002,#SR0
1754 010556 001401      BEQ     .+4
1755 010560 104006      HLT
1756 010562 022777 010450 170242      CMP      #ADR40,#SR2    ;SR0 INCORRECT AFTER 2ND ACC ABORT
1757 010570 001401      BEQ     .+4              ;CHECK SR2
1758 010572 104006      HLT
1759 010574 022626 010532      CMP      (R6),#ADR40A   ;SR2 DOESN'T CONTAIN VALUE FROM 1ST ABORT
1760 010600 001401      BEQ     .+4              ;CHECK ADDRESS PUSHED ON STACK
1761 010604 022626      HLT
1762 010606 012777 010642 170350      CMP      (R6)+,(R6)+
1763 010614 005077 170204      MOV      #INT40B,#KTVEC ;INCORRECT ADDRESS ON STACK
1764 010616 005077 170204      CLR      #SR0            ;RESTORE STACK POINTER
1765
1766 010620 012702 037776      MOV      #37776,R2
1767 010624 005277 170174      INC      #SR0            ;CHANGE RETURN ADDRESS
                                ;CLEAR ACC ERROR BIT-SHOULD
                                ;"UNLOCK" ERROR TRACKING
                                ;SETUP R2 TO REFERENCE KERNEL 1
                                ;TURN ON MEMORY MANAG.

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1768 010630 012242      ADR40B: MOV      (R2)+,(R2) ;3RD ACC REFERENCE, ERROR BIT WAS CLEARED
1769 010632 005077 170166      ADR40C: CLR      #SR0     ;TURN OFF MEMORY MANAG.
1770 010636 104006      HLT
1771 010640 000422      BR       DONE40          ;3RD REFERENCE TO KERNEL 1
1772 010642 042777 000001 170154      INT40B: BIC     #1,#SR0   ;DIDN'T ABORT
1773 010650 022777 020002 170146      CMP      #20002,#SR0    ;TURN OFF MEMORY MANAG.
1774 010656 001401      BEQ     .+4              ;CHECK SR0
1775 010660 104006      HLT
1776 010662 022777 010630 170142      CMP      #ADR40B,#SR2   ;SR0 INCORRECT
1777 010670 001401      BEQ     .+4              ;CHECK SR2
1778 010672 104006      HLT
1779
1780 010674 022716 010632      CMP      #ADR40C,(SP)   ;SR2 INCORRECT - SHOULD CONTAIN
1781 010700 001401      BEQ     .+4              ;LAST FETCH ADDRESS BEFORE ABORT
1782 010702 104006      HLT
1783 010704 022626      CMP      (R6)+,(R6)+
1784 010706 005077 170112      DONE40: CLR      #SR0     ;IPC ON STACK INCORRECT
1785 010712 005077 170250      CLR      #KTSTA        ;RESTORE STACK POINTER
1786 010716 016777 170244 170240      MOV      KTSTA,#KTVEC    ;CHANGE RETURN ADDRESS
                                ;CLEAR ACC ERROR BIT-SHOULD
                                ;"UNLOCK" ERROR TRACKING
                                ;SETUP R2 TO REFERENCE KERNEL 1
                                ;TURN ON MEMORY MANAG.
1787
1788
1789      ;SHOW THAT INIT CLEARS SR0<13-15>
1789 010724 104400      TEST34: SCOPE
1790 010726 012706 001000      MOV      #KSTACK,SP      ;INITIALIZE KERNEL STACK POINTER
1791 010732 004767 005446      JSR      PC,ORDER        ;CHECK TEST SEQUENCE + INIT SR0
1792 010736 000034      HLT
1793 010740 104006      HLT
1794 010742 112777 000340 170056      MOV     #340,#SR0H      ;SET SR0 BITS 13-15
1795 010750 122777 000340 170050      CMP     #340,#SR0H      ;MAKE SURE THEY SET CORRECTLY
1796 010756 001401      BEQ     .+4
1797 010760 104006      HLT
1798 010762 000005      RESET
1799 010764 122777 000000 170034      CMP     #0,#SR0H        ;SR0 INCORRECT (HIGH BYTE)
1800 010772 001401      BEQ     .+4              ;ISSUE INIT
1801 010774 104006      HLT
1802 010776 012767 000010 004652      MOV     #10,ICOUNT      ;CHECK SR0 HIGH BYTE
1803
1804
1805      ;SHOW THAT INIT CLEARS SR0 AFTER ABORT
1805 011004 104400      TEST35: SCOPE
1806 011006 012706 001000      MOV      #KSTACK,SP      ;INITIALIZE KERNEL STACK POINTER
1807 011012 004767 005366      JSR      PC,ORDER        ;CHECK TEST SEQUENCE + INIT SR0
1808 011016 000035      HLT
1809 011020 104006      HLT
1810 011022 004767 004366      JSR      X7,RWALL       ;TEST NUMBER
1811 011026 012777 000416 170040      MOV      #416,#KPDR0    ;MAP ALL PAR/PDR PAIR'S 4K,RW,BANK 0
1812
1813      JSR      PC,KERN7        ;MAP KERNEL PAR/PDR 7 TO EXT BANK
1814 011040 012777 077400 170030      MOV      #77400,#KPDRI  ;MAP KERNEL PAGE 1 NR
1815 011046 012777 011102 170110      MOV      #RET2,#KTVEC   ;SETUP ABORT RETURN
1816 011054 005077 170106      CLR      #KTSTA
1817 011060 012746 000020      MOV      #20,=(SP)
1818 011064 012746 011076      MOV      #ADR2,=(BP)
1819 011070 005277 167730      INC      #SR0
1820 011074 000002      RTI
1821
1821      ;SET T BIT IN STATUS ON STACK
1821      ;SETUP ADDRESS ON STACK
1821      ;TURN ON MEMORY MANAG.
1821      ;SHOULD TRACE TRAP IMMEDIATELY SINCE T-BIT
1821      ;IS SET - SINCE T-BIT VECTOR IS OUTSIDE ALLOWED

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1822                                     ;PAGE LENGTH, SHOULD DO A MEMORY
1823                                     ;MANAGEMENT ABORT
1824 011076 000000          ADR2:  HALT          DONE2
1825 011100 000412          BR              #40001,0SR0    ;CHECK SR0
1826 011102 022777 040001 167714 RET2:  CMP
1827 011110 001401          BEQ              .+4
1828 011112 104006          HLT
1829                                     ;SR0 INCORRECT = SHOULD SHOW
1830                                     ;REFERENCE TO KERNEL 0
1831 011114 000005          RESET
1832 011116 005777 167702          TST          #SR0
1833 011122 001401          BEQ              .+4
1834 011124 104006          HLT
1835 011126 005077 167672          CLR          #SR0
1836 011132 016777 170030 170024 DONE2:  MOV          KTSTA,KTVEC
1837 011140 012737 000016 000014          MOV          #16,#14    ;RESTORE T-BIT TRAP CATCHER
1838
1839                                     ;SHOW THAT INIT CLEARS SR0<0-3,5-6>
1840                                     ;REFERENCE NR USER PAGE 7 TO SET ALL BITS(0-6)
1841                                     ;THEN ISSUE INIT
1842 011146 104400          TEST36: SCOPE
1843 011150 012706 001000          MOV          #KSTACK,SP    ;INITIALIZE KERNEL STACK POINTER
1844 011154 004767 005224          JSR          PC,ORDER      ;CHECK TEST SEQUENCE + INIT SR0
1845 011160 000036          J3              ;TEST NUMBER
1846 011162 104006          HLT
1847 011164 004767 004224          JSR          X7,RWALL      ;MAP ALL PAR/PDR PAIR'S INITIALLY RW,4K,
1848                                     ;BANK 0
1849 011170 012777 077400 167654          MOV          #77400,0UPDR7 ;MAKE USER 7 NR
1850 011176 004767 005266          JSR          PC,KERN7      ;MAP KERNEL PAR/PDR 7 TO EXT BANK
1851 011202 012777 011240 167754          MOV          #RET3,KTVEC   ;SETUP ABORT RETURN
1852 011210 005077 167752          CLR          #KTSTA
1853 011214 012737 140000 177776          MOV          #140000,0#PS  ;SET MODE TO USER
1854 011222 012706 000400          MOV          #USTACK,R6    ;SETUP USER STACK IN CASE NEEDED
1855 011226 005277 167572          INC          #SR0
1856 011232 005737 160000          TST          #160000
1857 011236 000777          BR              .
1858 011240 022777 100157 167556 RET3:  CMP          #100157,0SR0
1859 011246 001401          BEQ              .+4
1860 011250 104006          HLT
1861                                     ;SR0 INCORRECT - SHOULD HAVE TRACKED
1862 011252 000005          RESET
1863 011254 005777 167544          TST          #SR0
1864 011260 001401          BEQ              .+4
1865 011262 104006          HLT
1866 011264 005077 167534          CLR          #SR0
1867 011270 012767 000010 004360          MOV          #10,ICOUNT    ;DROP ITERATION COUNT
1868 011276 016777 167664 167660          MOV          KTSTA,KTVEC
1869
1870                                     ;SHOW THAT BYTE ADDRESSING OF SR0 WORKS
1871 011304 104400          TEST37: SCOPE
1872 011306 012706 001000          MOV          #KSTACK,SP    ;INITIALIZE KERNEL STACK POINTER
1873 011312 004767 005066          JSR          PC,ORDER      ;CHECK TEST SEQUENCE + INIT SR0
1874 011316 000037          J3              ;TEST NUMBER
1875 011320 104006          HLT
1876                                     ;TEST EXECUTED OUT OF SEQUENCE

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1876 011322 004767 004066          JSR          X7,RWALL      ;MAP ALL PAR/PDR PAIRS RW,4K,BANK 0
1877 011326 004767 005136          JSR          PC,KERN7      ;MAP KERNEL PAR/PDR 7 TO EXT BANK
1878 011332 012777 160001 167464          MOV          #160001,0SR0  ;TURN ON MEMORY MANAG. AND SET ERROR FLAGS
1879 011340 105077 167460          CLR          #SR0
1880 011344 032777 160000 167452          BIT          #160000,0SR0 ;CHECK SR0
1881 011352 001001          BNE          .+4
1882 011354 104006          HLT
1883 011356 012777 160001 167440          MOV          #160001,0SR0 ;SR0 INCORRECT AFTER DATOB
1884 011364 105077 167436          CLR          #SR0
1885 011370 022777 000017 167426          CMP          #17,0SR0
1886 011376 001401          BEQ              .+4
1887 011400 104006          HLT
1888 011402 005077 167416          CLR          #SR0
1889
1890                                     ;SR0 INCORRECT AFTER DATOB
1891
1892                                     ;SHOW THAT SR0 <1-3> TRACK PAGE REFERENCED IF
1893                                     ;MEMORY MANAG. IS ON AND REFERENCE IS NOT TO A MEMORY MANAG. REGISTER
1894                                     ;SHOW THAT EACH VALUE IS CORRECTLY "LOCKED" IN SR0 AFTER AN ABORT
1895 011406 104400          TEST40: SCOPE
1896 011410 012706 001000          MOV          #KSTACK,SP    ;INITIALIZE KERNEL STACK POINTER
1897 011414 004767 004764          JSR          PC,ORDER      ;CHECK TEST SEQUENCE + INIT SR0
1898 011420 000040          J0              ;TEST NUMBER
1899 011422 104006          HLT
1900 011424 004767 003764          JSR          X7,RWALL      ;MAP KERNEL PAR/PDR 7 TO EXT BANK
1901 011430 004767 005034          JSR          PC,KERN7
1902 011434 012777 011512 167522          MOV          #RET5,KTVEC   ;SETUP ABORT RETURN
1903 011442 005077 167520          CLR          #KTSTA
1904 011446 016701 167362          MOV          UPDR0,R1
1905 011452 005002          CLR          R2
1906 011454 012703 100141          MOV          #100141,R3
1907 011460 012704 000010          MOV          #10,R4
1908 011464 012711 077400          MOV          #77400,0R1    ;MAKE USER NR
1909 011470 012737 140000 177776          MOV          #140000,0#PS  ;ENTER USER MODE
1910 011476 005277 167322          INC          #SR0
1911 011502 005712          TST          #R2
1912 011504 000777          BR              .
1913 011506 000005          RESET
1914 011510 000423          BR              DONE5
1915 011512 017705 167306          MOV          #SR0,R5
1916 011516 005077 167302          CLR          #SR0
1917 011522 020503          CMP          R5,R3
1918 011524 001401          BEQ              .+4
1919 011526 104006          HLT
1920 011530 020167 167300          CMP          R1,UPDR0
1921 011534 001002          BNE          LOP5A
1922 011536 012711 077406          MOV          #77406,0R1
1923 011542 022626          CMP          (R6)+,(R6)+
1924 011544 005721          TST          (R1)+
1925 011546 062703 000002          ADD          #2,R3
1926 011552 062702 020000          ADD          #20000,R2
1927 011556 077436          SOB          R4,LOOPS
1928 011560 016777 167402 167376 DONE5: MOV          KTSTA,KTVEC
1929 011566 005077 167374          CLR          #KTSTA
1930
1931                                     ;SHOW THAT SR0 <5-6> TRACK PAGE REFERENCED (MODE) IF

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1930
1931
1932 011572 104400
1933 011574 012706 001000
1934 011600 004767 004600
1935 011604 000041
1936 011606 104006
1937 011610 004767 003600
1938 011614 004767 004650
1939 011620 012777 077400 167250
1940 011626 012777 077400 167202
1941 011634 012777 011662 167322
1942 011642 005277 167156
1943 011646 005737 020000
1944 011652 005077 167146
1945 011656 104006
1946 011660 000436
1947 011662 017701 167136
1948 011666 005077 167132
1949 011672 022701 100003
1950 011676 001401
1951 011700 104006
1952 011702 012777 011736 167254
1953 011710 012737 140000 177776
1954 011716 005277 167102
1955 011722 005737 020000
1956 011726 005077 167072
1957 011732 104006
1958 011734 000410
1959 011736 017701 167062
1960 011742 005077 167056
1961 011746 022701 100143
1962 011752 001401
1963 011754 104006
1964
1965 011756 016777 167204 167200
1966
1967
1968
1969 011764 104400
1970 011766 012706 001000
1971 011772 004767 004406
1972 011776 000042
1973 012000 104006
1974 012002 004767 003406
1975 012006 012777 007600 167056
1976 012014 012737 140000 177776
1977 012022 005277 166776
1978 012026 042777 000001 166770
1979 012034 005037 177776
1980 012040 022777 000156 166756
1981 012046 001401
1982 012050 104006
1983

;MEMORY MANAG. IS ON AND THE REFERENCE IS NOT TO A MEMORY MANAG. REGISTER
;SHOW THAT EACH VALUE IS CORRECTLY "LOCKED" IN SR0 AFTER AN ABORT
TEST41: SCOPE
MOV #KSTACK,SP ;INITIALIZE KERNEL STACK POINTER
JSR PC,ORDER ;CHECK TEST SEQUENCE + INIT SR0
41 ;TEST NUMBER
HLT ;TEST EXECUTED OUT OF SEQUENCE
JSR X7,RWALL ;MAP ALL PAGES RW,4K, BANK 0
JSR PC,KERN7 ;MAP KERNEL PAR/PDR 7 TO EXT BANK
MOV #77400,#KPDR1 ;SETUP PAGE 1 IN EACH MODE TO BE NR
MOV #77400,#UPDR1
MOV #RET7A,#KTVEC ;SETUP ABORT RETURN
INC #SR0 ;TURN ON MEMORY MANAG.
TST #20000 ;REFERENCE PAGE 1 (NR)
CLR #SR0 ;TURN OFF MEMORY MANAG.
HLT ;NR REFERENCE DIDN'T ABORT
BR DONE7
RET7A: MOV #SR0,R1 ;SAVE SR0 CONTENTS IN R1
CLR #SR0 ;TURN OFF MEMORY MANAG.
CMP #100003,R1 ;CHECK SAVED CONTENTS OF SR0
BEQ .+4
HLT ;SR0 INCORRECT SHOULD SHOW NR ERR, KERNEL PAGE 1
MOV #RET7C,#KTVEC ;SETUP NEXT ABORT RETURN
MOV #140000,#SPS ;CHANGE MODE TO USER
INC #SR0 ;TURN ON MEMORY MANAG.
TST #20000 ;REFERENCE USER PAGE 1 (NR)
CLR #SR0 ;TURN OFF MEMORY MANAG.
HLT ;NR REFERENCE DIDN'T ABORT
BR DONE7
RET7C: MOV #SR0,R1 ;SAVE CONTENTS OF SR0
CLR #SR0 ;TURN OFF MEMORY MANAG.
CMP #100143,R1 ;CHECK SAVED CONTENTS OF SR0
BEQ .+4
HLT ;SR0 INCORRECT - SHOULD SHOW NR
;ERROR, USER PAGE 1
;RESTORE TRAP CATCHER
DONE7: MOV KTSTA,#KTVEC

;SHOW THAT SR0 <1-3,5-6> DOESN'T TRACK IF MEMORY MANAG. IS OFF BUT DOES IF REFERENCE IS
;AN INTERNAL (MEMORY MANAG.) REGISTER
TEST42: SCOPE
MOV #KSTACK,SP ;INITIALIZE KERNEL STACK POINTER
JSR PC,ORDER ;CHECK TEST SEQUENCE + INIT SR0
42 ;TEST NUMBER
HLT ;TEST EXECUTED OUT OF SEQUENCE
JSR X7,RWALL ;SET ALL PAR/PDR PAIRS RW, 4K, BANK 0
MOV #7600,#UPAR7 ;MAP USER 7 TO THE EXT. BANK
MOV #140000,#SPS ;SET MODE TO USER
INC #SR0 ;TURN ON MEMORY MANAG.
BIC #1,#SR0 ;TURN OFF MEMORY MANAG.
CLR #SPS ;CHANGE TO KERNEL MODE
CMP #156,#SR0 ;CHECK SR0
BEQ .+4
HLT ;SR0 INCORRECT - SHOULD SHOW REFERENCE
;TO USER 7

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1984
1985
1986
1987
1988 012052 005077 166746 CLR #SR0
1989
1990
1991
1992
1993
1994
1995
1996 012056 104400
1997 012060 012706 001000
1998 012064 004767 004314
1999 012070 000043
2000 012072 104006
2001 012074 004767 003314
2002 012100 012777 000416 166766
2003
2004 012106 004767 004356
2005 012112 012777 012150 167044
2006 012120 005077 167042
2007 012124 012746 000020
2008 012130 012746 012136
2009 012134 000006
2010 012136 012777 000001 166660
2011
2012
2013
2014 012144 000000
2015 012146 000415
2016 012150 042777 000001 166646
2017 012156 022777 040000 166640
2018 012164 001401
2019 012166 104006
2020 012170 022777 012136 166634
2021 012176 001401
2022 012200 104006
2023
2024 012202 005077 166616
2025 012206 016777 166754 166750
2026
2027
2028
2029 012214 104400
2030 012216 012706 001000
2031 012222 004767 004156
2032 012226 000044
2033 012230 104006
2034 012232 004767 003156
2035 012236 012777 077402 166634
2036 012244 004767 004220
2037 012250 012777 012312 166706

;IF IT SHOWS USER 0
;IT DID NOT TRACK THE INTERNAL REFERENCE
;IF IT SHOWS KERNEL 0, IT IS
;TRACKING WITH MEMORY MANAG. OFF

;SHOW THAT IF AN INSTRUCTION IS COMPLETED BEFORE A MEMORY MANAGEMENT FAULT
;OCCURS, SR2 WILL CONTAIN THE ADDRESS OF LAST FETCH BEFORE ABORT
;TO TEST THIS, TRACE TRAP IS USED. THE VECTOR IS MADE NON-RESIDENT BY MAKING
;KERNEL PAGE 0 MAPPED DOWN FROM 17776 TO 100, THUS THE MEMORY MANAGEMENT
;VECTOR IS RESIDENT WHILE THE TRACE TRAP VECTOR IS OUTSIDE THE ALLOWED
;PAGE LENGTH.
TEST43: SCOPE
MOV #KSTACK,SP ;INITIALIZE KERNEL STACK POINTER
JSR PC,ORDER ;CHECK TEST SEQUENCE + INIT SR0
43 ;TEST NUMBER
HLT ;TEST EXECUTED OUT OF SEQUENCE
JSR X7,RWALL ;INITIALIZE ALL PAGES RW,4K,BANK 0
MOV #416,#KPDR0 ;MAP KERNEL TO EXCLUDE
;LOCATIONS 0 TO 77
JSR PC,KERN7 ;MAP KERNEL PAR/PDR 7 TO EXT BANK
MOV #RET11,#KTVEC ;SETUP MEMORY MANAGEMENT ABORT RETURN
CLR #KTSTA
MOV #20,-(SP) ;PREPARE STACK TO TURN ON T-BIT
MOV #,+b,-(SP)
RTT ;SET T-BIT VIA RTT
ADR11: MOV #1,#SR0 ;TURN ON MEMORY MANAG. - SHOULD
;ATTEMPT TO TRACE TRAP AT END OF
;INSTRUCTION - SHOULD GET A PAGE
;LENGTH ERROR ON THAT ATTEMPT
;NO PAGE LENGTH ERROR ON TRACE TRAP
BR CONT11
RET11: BIC #1,#SR0 ;TURN OFF MEMORY MANAG.
CMP #40000,#SR0 ;CHECK SR0
BEQ .+4
HLT ;SR0 INCORRECT - PL FAULT,KERNEL 0 REFERENCE COMPLETED
CMP #ADR11,#SR2 ;CHECK SR2
BEQ .+4
HLT ;SR2 INCORRECT - SHOULD CONTAIN
;ADDRESS OF LAST FETCH BEFORE ABORT
CONT11: CLR #SR0 ;REINITIALIZE SR0
MOV KTSTA,#KTVEC ;RESTORE TRAP CATCHER

;SHOW THAT HAVING THE ABORT ERROR
;BITS SET WILL NOT PREVENT A MEMORY MANAGEMENT TRAP
TEST44: SCOPE
MOV #KSTACK,SP ;INITIALIZE KERNEL STACK POINTER
JSR PC,ORDER ;CHECK TEST SEQUENCE + INIT SR0
44 ;TEST NUMBER
HLT ;TEST EXECUTED OUT OF SEQUENCE
JSR X7,RWALL ;INITIALIZE ALL PAR/PDR PAIRS TO RW,4K, BANK 0
MOV #77402,#KPDR2 ;SET KERNEL PAR/PDR PAIR 2 RRO,4K
JSR PC,KERN7 ;MAP KERNEL PAR/PDR 7 TO EXT BANK
MOV #RET13A,#KTVEC ;SETUP MEMORY MANAGEMENT ABORT RETURN

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2038 012256 005077 166704 CLR #KTSTA
2039 012262 005277 166536 INC #SR0 ;RETURN ON MEMORY MANAG.
2040 012266 012777 160001 166530 MOV #160001,#SR0 ;SET ABORT ERROR BITS
2041 012274 013737 007000 047000 MOV #07000,#047000 ;WRITE KERNEL PAR/PDR PAIR 2 (RRO)-SHOULD TRAP
2042 012302 005077 166516 CLR #SR0
2043 012306 104006 HLT ;NO TRAP OCCURRED
2044 012310 000416 BR DONE13
2045 012312 022626 RET13A: CMP (SP)+,(SP)+ ;RESTORE THE STACK POINTER
2046 012314 017701 166504 MOV #SR0,R1 ;SAVE CONTENTS OF SR0
2047 012320 005077 166500 CLR #SR0 ;TURN OFF MEMORY MANAG.
2048 012324 022701 160017 CMP #160017,R1
2049 012330 001401 BEQ .+4
2050 012332 104006 HLT ;SAVED CONTENTS OF SR0 INCORRECT
2051 012334 022777 077402 166536 CMP #77402,#KPD2 ;CHECK THE PDR CORRESPONDING TO THE TRAP REFERENCE
2052 012342 001401 BEQ .+4
2053 012344 104006 HLT ;THE PDR CORRESPONDING TO THE TRAP REFERENCE IS INCORRECT
2054 012346 016777 166614 166610 DONE13: MOV #KTSTA,#KTVEC ;RESTORE MEMORY MANAGEMENT TRAP RETURN
2055 CLR #SR0 ;TO CAUSE A HALT ON A FALSE TRAP OR ABORT
2056 012354 005077 166444 CLR #SR0 ;REINITIALIZE SR0
2057
2058 ;SHOW THAT MEMORY MANAGEMENT WILL NOT TRAP ON AN INTERNAL REFERENCE
2059 012360 104400 TEST45: SCOPE
2060 012362 012706 MOV #KSTACK,SP ;INITIALIZE KERNEL STACK POINTER
2061 012366 004767 004012 JSR PC,ORDER ;CHECK TEST SEQUENCE + INIT SR0
2062 012372 000045 45 ;TEST NUMBER
2063 012374 104006 HLT ;TEST EXECUTED OUT OF SEQUENCE
2064 012376 004767 003012 JSR X7,RWALL ;MAP ALL PAR/PDR PAIRS 4K, RW, BANK 0
2065 012402 004767 004062 JSR PC,KERN7 ;MAP KERNEL PAR/PDR 7 TO EXT BANK
2066 012406 012777 012450 166550 MOV #RET16,#KTVEC ;SETUP TRAP RETURN IN CASE
2067 012414 005077 166506 CLR #KTSTA
2068 012420 005277 166400 INC #SR0 ;TURN ON MEMORY MANAG.
2069 012424 005777 166374 TST #SR0 ;TRAP REFERENCE TO A MEMORY MANAG. REGISTER
2070 012430 005077 166370 CLR #SR0
2071 012434 022777 077406 166450 CMP #77406,#KPD2
2072 012442 001401 BEQ .+4
2073 012444 104006 HLT
2074 012446 000404 BR DONE16
2075 012450 042777 000001 166346 RET16: BIC #1,#SR0
2076 012456 104006 HLT
2077 012460 005077 166340 DONE16: CLR #SR0
2078 012464 016777 166476 166472 MOV #KTSTA,#KTVEC
2079
2080 ;TEST PAGE LENGTH ERROR CHECKING (EXPAND DOWN NOT SET)
2081 ;KERNEL PAR/PDR PAIR1 IS USED WITH ALL PAGE LENGTH VALUES
2082 ;SHOW THAT REFERENCES TO BOTH BOUNDARIES OF THE ALLOWED AREA DON'T TRAP OR ABORT
2083 ;SHOW THAT A REFERENCE TO THE FIRST WORD BEYOND THE ALLOWABLE AREA DOES TRAP
2084 012472 104400 TEST46: SCOPE
2085 012474 012706 MOV #KSTACK,SP ;INITIALIZE KERNEL STACK POINTER
2086 012500 004767 003700 JSR PC,ORDER ;CHECK TEST SEQUENCE + INIT SR0
2087 012504 000046 46 ;TEST NUMBER
2088 012506 104006 HLT ;TEST EXECUTED OUT OF SEQUENCE
2089 012510 004767 002700 JSR X7,RWALL ;INITIALIZE ALL PAR/PDR PAIRS TO RW,AK, BANK 0
2090 012514 004767 003750 JSR PC,KERN7 ;MAP KERNEL PAR/PDR 7 TO EXT BANK
2091 012520 012702 000006 MOV #6,R2 ;R2 CONTAINS VALUE TO BE LOADED IN THE

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2092
2093 012524 012701 000076 MOV #20076,R1 ;PDR BEING CHECKED (INCLUDING PLF)
2094 ;R1 IS USED TO REFERENCE THE TOP ADDRESS
2095 012530 012777 012610 166426 MOV #RET23A,#KTVEC ;WITHIN THE ALLOWED AREA
2096 012536 005077 166424 CLR #KTSTA ;SETUP ABORT RETURN IN CASE REFERENCE
2097 012542 005277 166256 LOOP23: INC #SR0 ;WITHIN ALLOWED AREA ABORTS
2098 012546 010277 166324 MOV #R2,#KPD1 ;TURN ON MEMORY MANAG.
2099 012552 005727 000000 TST #20000 ;SET KERNEL PAR/PDR PAIR 1 TO NEW PAGE LENGTH
2100 012556 005711 TST #R1 ;READ LOWER BOUNDARY-SHOULDN'T ABORT
2101 ;READ UPPER ALLOWED BOUNDARY-SHOULDN'T
2102 ;ABORT
2103 012560 012777 012630 166376 MOV #RET23B,#KTVEC ;SETUP ABORT RETURN
2104 012566 020127 037776 CMP R1,#37776 ;CHECK FOR DONE (TO AVOID REFERENCING
2105 ;NEXT PAR/PDR PAIR)
2106 012572 103041 BHS DONE23 ;EXIT LOOP IF DONE
2107 012574 005761 000002 TST 2(R1) ;REFERENCE OUTSIDE ALLOWED AREA -
2108 ;SHOULD ABORT
2109 012600 005077 166220 CLR #SR0 ;TURN MEMORY MANAG. OFF
2110 012604 104006 HLT ;NO ABORT OCCURRED ON A REFERENCE
2111 012606 000426 BR CONT23 ;OUTSIDE THE ALLOWED PAGE LENGTH
2112 012610 022777 000001 166206 RET23A: BIC #1,#SR0 ;TURN OFF MEMORY MANAG.
2113 012616 022626 CMP (SP)+,(SP)+ ;RESTORE STACK POINTER
2114 012622 005077 166176 HLT ;REFERENCE WITHIN ALLOWED AREA
2115 012624 000416 BR #SR0 ;CLEAR ERROR BITS
2116 012630 022626 RET23B: CMP (SP)+,(SP)+ ;CAUSED A TRAP OR ABORT
2117 012632 017703 166166 MOV #SR0,R3 ;RESTORE STACK POINTER
2118 012636 005077 166162 CLR #SR0 ;SAVE CURRENT SR0
2119 012642 022703 000003 CMP #40003,R3 ;TURN OFF MEMORY MANAG.
2120 012646 001401 BEQ .+4 ;CK SAVED SR0
2121 012650 104006 HLT
2122 ;CONTENTS OF SR0 INCORRECT AFTER
2123 012652 022777 000002 166144 CMP #2,#SR0 ;PAGE LENGTH ERROR ABORT
2124 012660 001401 BEQ .+4 ;CHECK SR0 TO BE SURE PL BIT CLEARED
2125 012662 104006 HLT
2126 ;SR0 INCORRECT AFTER CLEARING IT
2127 012664 062701 000100 CONT23: ADD #100,R1 ;ONLY KERNEL PAGE 1 SHOULD STILL BE SET
2128 ;SETUP R1 TO REFERENCE BOUNDARY OF
2129 012670 062702 000400 ADD #400,R2 ;NEXT PAGE
2130 ;ADD 1 TO VALUE TO BE LOADED IN
2131 012674 000722 BR LOOP23 ;PAGE LENGTH FIELD
2132 012676 005077 166122 CLR #SR0 ;CHECK NEXT PAGE LENGTH VALUE
2133 012702 016777 166260 166254 DONE23: MOV #KTSTA,#KTVEC ;TURN OFF MEMORY MANAG.
2134 012710 005077 166252 CLR #KTSTA ;RESTORE MEMORY MANAGEMENT ABORT RETURN
2135 ;TO CAUSE HALT ON A FALSE TRAP
2136 ;OR ABORT
2137
2138 ;TEST PAGE LENGTH ERROR CHECKING (EXPAND DOWN SET)
2139 ;KERNEL PAR/PDR PAIR1 IS TESTED WITH ALL VALUES OF PAGE LENGTH FIELD
2140 ;SHOW THAT REFERENCES TO BOTH BOUNDARIES OF THE ALLOWED AREA DON'T TRAP OR ABORT
2141 ;SHOW THAT A REFERENCE TO THE WORD IMMEDIATELY BELOW THE ALLOWED AREA DOES TRAP
2141 012714 104400 TEST47: SCOPE
2142 012716 012706 MOV #KSTACK,SP ;INITIALIZE KERNEL STACK POINTER
2143 012722 004767 003456 JSR PC,ORDER ;CHECK TEST SEQUENCE + INIT SR0
2144 012726 000047 47 ;TEST NUMBER
2145 012730 104006 HLT ;TEST EXECUTED OUT OF SEQUENCE

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2146 012732 004767 002456 JSR X7,RWALL ;INITIALIZE ALL PAR/PDR PAIRS TO RW,AK, BANK 0
2147 012736 004767 003526 JSR PC,KERN7 ;MAP KERNEL PAR/PDR 7 TO EXT BANK
2148 012742 012702 077416 MOV #77416,R2 ;R2 CONTAINS VALUE TO BE LOADED IN THE
2149 ;PDR BEING CHECKING (INCLUDING PLF)
2150 012746 012701 037700 MOV #37700,R1 ;R1 IS USED TO REFERENCE THE LOWEST
2151 ;ALLOWED ADDRESS IN THE PAGE
2152 012752 012777 013032 166204 MOV #RET24A,#KTVEC ;SETUP ABORT RETURN IN CASE REFERENCE
2153 012760 005077 166202 CLR #KTSTA ;WITHIN ALLOWED AREA ABORTS
2154 012764 005277 166034 LOOP24: INC #SR0 ;TURN ON MEMORY MANAG.
2155 012770 010277 166102 MOV R2,#KPDR1 ;SET KERNEL PAR/PDR PAIR 1 TO NEW PAGE LENGTH
2156 012774 005727 037776 TST #37776 ;REFERENCE UPPER ALLOWED BOUNDARY
2157 013000 005711 TST #R1 ;REFERENCE LOWER ALLOWED BOUNDARY
2158 ;I= NEITHER REFERENCE SHOULD ABORT
2159 013002 012777 013044 166154 MOV #RET24B,#KTVEC ;SETUP ABORT RETURN
2160 013010 020127 020000 CMP R1,#20000 ;CHECK FOR DONE
2161 013014 001436 BEQ DONE24 ;EXIT LOOP IF DONE
2162 013016 005761 177776 TST =2(R1) ;REFERENCE BELOW ALLOWED AREA =
2163 ;SHOULD ABORT
2164 013022 005077 165776 CLR #SR0 ;TURN MEMORY MANAG. OFF
2165 013026 104006 HLT ;NO ABORT OCCURRED ON A REFERENCE
2166 013030 000423 BR CONT24 ;OUTSIDE THE ALLOWED PAGE LENGTH
2167 013032 005077 165766 RET24A: CLR #SR0 ;TURN OFF MEMORY MANAG. AND CLEAR
2168 ;ERROR BITS
2169 013036 022626 CMP (SP)+,(SP)+ ;RESTORE STACK POINTER
2170 013040 104006 HLT ;REFERENCE WITHIN ALLOWED AREA CAUSED
2171 013042 000416 BR CONT24 ;A TRAP OR ABORT
2172 013044 022626 RET24B: CMP (SP)+,(SP)+ ;RESTORE STACK POINTER
2173 013046 017703 165752 MOV #SR0,R3 ;SAVE CURRENT SR0
2174 013052 005077 165746 CLR #SR0 ;TURN OFF MEMORY MANAG.
2175 013056 022703 040003 CMP #40003,R3 ;CHECK SAVED SR0
2176 013062 001401 BEQ .+4
2177 013064 104006 HLT ;CONTENTS OF SR0 INCORRECT AFTER
2178 ;PAGE LENGTH ERROR ABORT
2179 013066 022777 000002 165730 CMP #2,#SR0 ;CHECK SR0 TO BE SURE PL BIT CLEARED
2180 013074 001401 BEQ .+4
2181 013076 104006 HLT ;SR0 INCORRECT AFTER CLEARING IT
2182 013100 162701 000100 CONT24: SUB #100,R1 ;SETUP R1 TO REFERENCE BOUNDARY
2183 ;OF NEXT PAGE DOWN
2184 013104 162702 000400 SUB #400,R2 ;INCREASE ALLOWED PAGE LENGTH
2185 ;(DOWN) BY 1 PAGE
2186 013110 000725 BR LOOP24 ;CHECK NEXT PAGE LENGTH VALUE
2187 013112 005077 165706 DONE24: CLR #SR0 ;TURN OFF MEMORY MANAG.
2188 013116 016777 166040 MOV KTSTA,#KTVEC ;RESTORE MEMORY MANAGEMENT ABORT RETURN
2189 013124 005077 166036 CLR #KTSTA ;TO CAUSE A HALT ON A FALSE TRAP
2190 ;FOR ABORT
2191 ;
2192 ;TEST ALL COMBINATIONS OF VALUES FOR THE PAGE LENGTH COMPARATORS-
2193 ;USE KERNEL PAGE PAGE 1
2194 013130 104400 TEST50: SCOPE
2195 013132 012706 001000 MOV #KSTACK,SP ;INITIALIZE KERNEL STACK POINTER
2196 013136 004767 003242 JSR PC,ORDER ;CHECK TEST SEQUENCE + INIT SR0
2197 013142 000050 S0 ;TEST NUMBER
2198 013144 104006 HLT ;TEST EXECUTED OUT OF SEQUENCE
2199 013146 012767 000020 002502 MOV #20,ICOUNT ;DROP ITERATION COUNT

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2200 013154 004767 002234 JSR X7,RWALL ;INITIALIZE ALL PAGES RW, BANK 0
2201 013160 004767 003304 JSR PC,KERN7 ;MAP KERNEL PAR/PDR 7 TO EXT BANK
2202 013164 012777 013276 165772 MOV #RET25,#KTVEC ;SETUP ABORT RETURN
2203 013172 005077 165770 CLR #KTSTA
2204 013176 012701 000006 MOV #6,R1 ;R1 CONTAINS THE VALUE TO BE
2205 ;LOADED INTO THE PDR
2206 013202 012777 000001 165614 MOV #1,#SR0 ;TURN ON MEMORY MANAG.
2207 013210 012703 020000 L25A: MOV #20000,R3 ;R3 CONTAINS VA USED
2208 013214 010177 165656 MOV R1,#KPDR1 ;LOAD NEW PAGE LENGTH FIELD
2209 013220 010102 L25B: MOV R1,R2 ;R2 IS A COPY OF R1
2210 013222 010304 MOV R3,R4 ;R4 IS A COPY OF R3
2211 013224 042704 160000 BIC #160000,R4
2212 013230 005713 TST (R3) ;USE VA IN R3 TO REFERENCE PAGE 1
2213 013232 000302 SWAB R2 ;NO TRAP-CHECK TO MAKE SURE
2214 013234 042702 177400 BIC #177400,R2
2215 013240 006304 ASL R4 ;VIRTUAL ADDRESS WAS WITHIN
2216 013242 006304 ASL R4
2217 013244 000304 SWAB R4
2218 013246 020402 CMP R4,R2 ;ALLOWED PAGE LENGTH
2219 013250 003401 BLE .+4
2220 013252 104006 HLT ;REFERENCE OUTSIDE ALLOWED PAGE LENGTH
2221 ;DIDN'T ABORT
2222 013254 062703 000100 C25: ADD #100,R3
2223 013260 020327 037776 CMP R3,#37776
2224 013264 003755 BLE L25B
2225 013266 062701 000400 ADD #400,R1
2226 013272 100346 BPL L25A
2227 013274 000413 BR DONE25
2228 013276 022626 RET25: CMP (SP)+,(SP)+ ;RESTORE STACK POINTER
2229 013300 000302 SWAB R2 ;CHECK TO MAKE SURE VIRTUAL
2230 013302 042702 177400 BIC #177400,R2
2231 013306 006304 ASL R4 ;ADDRESS WAS OUTSIDE ALLOWED
2232 013310 006304 ASL R4
2233 013312 000304 SWAB R4
2234 013314 020402 CMP R4,R2 ;PAGE LENGTH
2235 013316 000301 BGT .+4
2236 013320 104006 HLT ;REFERENCE WITHIN ALLOWED
2237 013322 000754 BR C25 ;PAGE LENGTH ABORTED=R3 CONTAINS
2238 ;VA USED, R1 CONTAINS VALUE
2239 ;LOADED INTO THE PDR
2240 013324 016777 165636 165632 DONE25: MOV KTSTA,#KTVEC
2241 013332 005077 165466 CLR #SR0
2242 ;
2243 ;SHOW THAT THE W BIT DOESN'T SET IF THE MEMORY MANAG. IS OFF
2244 013336 104400 TEST51: SCOPE
2245 013340 012706 001000 MOV #KSTACK,SP ;INITIALIZE KERNEL STACK POINTER
2246 013344 004767 003034 JSR PC,ORDER ;CHECK TEST SEQUENCE + INIT SR0
2247 013350 000051 S1 ;TEST NUMBER
2248 013352 104006 HLT ;TEST EXECUTED OUT OF SEQUENCE
2249 013354 012767 002000 002274 MOV #2000,ICOUNT ;RESTORE ITERATION COUNT
2250 013362 004767 002002 JSR X7,CLRALL ;CLEAR ALL MEMORY MANAG. REGISTERS
2251 013366 013737 010000 010000 MOV #010000,#10000 ;WRITE BANK 0
2252 013374 005777 165474 TST #KPDR0
2253 013400 001401 BEQ .+4

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2254 013402 104006          HLT                               JN BIT SET OR ANOTHER BIT INCORRECT
2255                                     JIN KERNEL 0 PDR
2256
2257                                     ;SHOW THAT THE W BIT IS CLEARED BY WRITING (VIA DATO) THE CORRESPONDING PAR
2258 ;CHECK EACH PDR
2259 013404 104400          TEST52: SCOPE
2260 013406 012706 001000    MOV      #KSTACK,SP          ;INITIALIZE KERNEL STACK POINTER
2261 013412 004767 002766    JSR      PC,ORDER           ;CHECK TEST SEQUENCE + INIT SR0
2262 013416 000052          S2                          ;TEST NUMBER
2263 013420 104006          HLT                          ;TEST EXECUTED OUT OF SEQUENCE
2264 013422 004767 001766    JSR      X7,RWALL           ;MAP KERNEL PAR/PDR 7 TO EXT BANK
2265 013426 004767 003036    JSR      PC,KERN7          ;MAP USER 7 TO EXTERNAL BANK
2266 013432 012777 007600 165432  MOV      #7600,#UPAR7      ;SET MODE TO USER
2267 013440 012737 140000 177776  MOV      #140000,#0PS      ;SETUP USER STACK
2268 013446 012706 000400    MOV      #USTACK,R6        ;SET UP KT REG TABLE POINTER
2269 013452 012700 001144    MOV      #STATAB,R0       ;R1 CONTAINS ADDRESS OF
2270 013456 012001          LOP27: MOV      (R0)+,R1        ;ADDRESS OF CURRENT PDR
2271
2272 013460 012702 017776    MOV      #17776,R2        ;R2 CONTAINS VIRTUAL ADDRESS TO
2273                                     ;REFERENCE DESIRED PAGE
2274 013464 012037 177776    MOV      (R0)+,#0PS       ;SETUP STATUS FOR CURRENT MODE
2275 013470 005277 165330    LOP27A: INC      #SR0       ;TURN ON MEMORY MANAG.
2276 013474 011212          MOV      (R2),(R2)        ;WRITE
2277 013476 005077 165322    CLR      #SR0             ;TURN OFF MEMORY MANAG.
2278 013502 004767 000016    JSR      X7,CKWBIT        ;TEST W BIT
2279 013506 062702 020000    ADD      #20000,R2        ;CHANGE VA TO REFERENCE NEXT PAGE
2280 013512 103366          BCC     LOP27A           ;LOOP UNTIL ALL PDR'S HAVE BEEN
2281                                     ;CHECKED IN THE CURRENT MODE
2282 013514 020027 001152    CMP      R0,#STAENO       ;
2283 013520 002756          BLT     LOP27           ;
2284 013522 000416          BR      EXT27            ;
2285 013524 032771 000100 000000  CKWRIT: BIT     #100,(R1)   ;CHECK W BIT
2286 013532 001001          BNE     ,+4             ;
2287 013534 104006          HLT
2288
2289 013536 005071 000020    CLR      #20(R1)         ;
2290                                     ;CLEAR W BIT BY WRITING CORRESPONDING
2291 013542 032771 000100 000000    BIT     #100,(R1)       ;PAR VIA DATO
2292 013550 001401          BEQ     ,+4             ;CHECK W BIT
2293 013552 104006          HLT
2294 013554 005721          TST     (R1)+           ;W BIT DIDN'T CLEAR IN PDR WHOSE
2295 013556 000207          RTS      X7              ;ADDRESS IS POINTED TO BY R1
2296 013560
2297
2298                                     ;SHOW THAT THE W BIT IS CLEARED BY A DATOB TO THE PDR
2299 ;CHECK BOTH HIGH AND LOW DATOB'S, ON KERNEL 0
2300 013560 104400          TEST53: SCOPE
2301 013562 012706 001000    MOV      #KSTACK,SP          ;INITIALIZE KERNEL STACK POINTER
2302 013566 004767 002612    JSR      PC,ORDER           ;CHECK TEST SEQUENCE + INIT SR0
2303 013572 000053          S3                          ;TEST NUMBER
2304 013574 104006          HLT                          ;TEST EXECUTED OUT OF SEQUENCE
2305 013576 004767 001612    JSR      X7,RWALL           ;MAP ALL PAR/PDR PAIRS 4K, RW, BANK 0
2306 013602 004767 002662    JSR      PC,KERN7          ;MAP KERNEL PAR/PDR 7 TO EXT BANK
2307 013606 005277 165212    INC      #SR0             ;TURN ON MEMORY MANAG.

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2308 013612 013737 000000 000000    MOV      #00,#00          ;WRITE INTO PAGE 0
2309 013620 005077 165200    CLR      #SR0             ;TURN OFF MEMORY MANAG.
2310 013624 032777 000100 165242    BIT     #100,#KPDR0       ;CHECK W BIT
2311 013632 001001          BNE     ,+4             ;
2312 013634 104006          HLT                          ;W BIT NOT SET AFTER WRITING PAGE
2313 013636 112777 000106 165230  MOVB    #106,#KPDR0       ;DATOB SHOULD CLEAR W BIT
2314 013644 032777 000100 165222    BIT     #100,#KPDR0       ;
2315 013652 001401          BEQ     ,+4             ;
2316 013654 104006          HLT
2317
2318 013656 005277 165142    INC      #SR0             ;TURN ON MEMORY MANAG.
2319 013662 013737 017776 017776    MOV      #017776,#017776 ;WRITE INTO PAGE 0 AGAIN
2320 013670 005077 165130    CLR      #SR0             ;TURN OFF MEMORY MANAG.
2321 013674 032777 000100 165172    BIT     #100,#KPDR0       ;CHECK W BIT
2322 013702 001001          BNE     ,+4             ;
2323 013704 104006          HLT                          ;W BIT NOT SET AFTER WRITING PAGE
2324 013706 016701 165162    MOV      KPAR0,R1         ;SETUP R1 TO REFERENCE HIGH BYTE
2325 013712 005201          INC      R1               ;OF KPAR0
2326 013714 112711 000177 165146  MOVB    #177,#R1          ;DATOB TO HIGH BYTE OF KPAR0
2327 013720 032777 000100 165146    BIT     #100,#KPDR0       ;CHECK W BIT
2328 013726 001401          BEQ     ,+4             ;
2329 013730 104006          HLT                          ;W BIT DIDN'T CLEAR VIA DATOB
2330                                     ;TO HIGH BYTE OF PDR
2331
2332                                     ;SHOW THAT THE W BIT IS CLEARED BY A DATOB TO THE PAR
2333 ;CHECK BOTH HIGH AND LOW DATOB'S, ON KERNEL 0
2334 013732 104400          TEST54: SCOPE
2335 013734 012706 001000    MOV      #KSTACK,SP          ;INITIALIZE KERNEL STACK POINTER
2336 013740 004767 002440    JSR      PC,ORDER           ;CHECK TEST SEQUENCE + INIT SR0
2337 013744 000054          S4                          ;TEST NUMBER
2338 013746 104006          HLT                          ;TEST EXECUTED OUT OF SEQUENCE
2339 013750 004767 001440    JSR      X7,RWALL           ;MAP ALL PAR/PDR PAIRS 4K, RW, BANK 0
2340 013754 004767 002510    JSR      PC,KERN7          ;MAP KERNEL PAR/PDR 7 TO EXT BANK
2341
2342 013760 005277 165040    INC      #SR0             ;EXTERNAL BANK
2343 013764 013737 000000 000000    MOV      #00,#00          ;TURN ON MEMORY MANAG.
2344 013772 005077 165026    CLR      #SR0             ;WRITE INTO PAGE 0
2345 013776 032777 000100 165070    BIT     #100,#KPDR0       ;TURN OFF MEMORY MANAG.
2346 014004 001001          BNE     ,+4             ;CHECK W BIT
2347 014006 104006          HLT                          ;
2348 014010 112777 000000 165076  MOVB    #0,#KPAR0        ;W BIT NOT SET AFTER WRITING PAGE
2349 014016 032777 000100 165050    BIT     #100,#KPDR0       ;DATOB TO THE PAR
2350 014024 001401          BEQ     ,+4             ;CHECK W BIT
2351 014026 104006          HLT                          ;
2352                                     ;W BIT DIDN'T CLEAR VIA DATOB
2353 014030 005277 164770    INC      #SR0             ;TO (LOW) TO THE PAR
2354 014034 013737 017776 017776    MOV      #017776,#017776 ;TURN ON MEMORY MANAG.
2355 014042 005077 164756    CLR      #SR0             ;WRITE INTO PAGE 0 AGAIN
2356 014046 032777 000100 165020    BIT     #100,#KPDR0       ;TURN OFF MEMORY MANAG.
2357 014054 001001          BNE     ,+4             ;CHECK W BIT
2358 014056 104006          HLT                          ;
2359 014060 016701 165030    MOV      KPAR0,R1         ;W BIT NOT SET AFTER WRITING PAGE
2360 014064 005201          INC      R1               ;SETUP R1 TO REFERENCE HIGH BYTE
2361 014066 112711 000000 164774  MOVB    #0,#R1           ;OF KPAR0
2362 014072 032777 000100 164774    BIT     #100,#KPDR0       ;DATOB TO HIGH BYTE OF KPAR0
2363                                     ;CHECK W BIT

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2362 014100 001401      BEQ      .+4
2363 014102 104006      HLT
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2368 014104 104400      ;SHOW THAT THE W BIT IS NOT CLEARED BY INIT
;INITIALLY SET ALL THE W BITS, THEN DO A RESET AND CHECK THE W BITS
TEST55: SCOPE
2369 014106 012706 001000      MOV      #KSTACK,SP      ;INITIALIZE KERNEL STACK POINTER
2370 014112 004767 002266      JSR      PC,ORDER        ;CHECK TEST SEQUENCE + INIT SR0
2371 014116 000055      S5
2372 014120 104006      HLT
2373 014122 012767 000020 001526      MOV      #20,ICOUNT      ;TEST NUMBER
2374 014130 004767 001260      JSR      X7,RWALL        ;TEST EXECUTED OUT OF SEQUENCE
2375 014134 004767 002330      JSR      PC,KERN7        ;INITIALIZE ALL PAGES RW,4K,BANK 0
2376 014140 012777 007600 164724      MOV      #7600,#KPDR7   ;MAP KERNEL PAR/PDR 7 TO EXT BANK
2377 014146 012737 140000 177776      MOV      #140000,#SPS    ;MAP USER 7 TO THE EXTERNAL BANK
2378 014154 012706 000400      MOV      #USTACK,R6      ;SET MODE TO USER
2379 014160 012700 001144      MOV      #STATAB,R0      ;SETUP USER STACK
2380
2381 014164 005720      MOV      (R0)+           ;R0 POINTS TO INFORMATION FOR
2382 014166 012037 177776      MOV      (R0)+,#SPS     ;CURRENT MODE
2383 014172 012702 017776      MOV      #17776,R2      ;MOVE POINTER
2384 014176 005277 164622      INC
2385 014202 011212      MOV      (R2),(R2)      ;SETUP MODE TO REFERENCE NEXT SET OF REGS
2386 014204 062702 020000      ADD      #20000,R2      ;SETUP R2 TO REFERENCE DESIRED PAGE
2387 014210 103374      SCC      LOP32C         ;WRITE IN
2388 014212 005077 164606      CLR      #SR0           ;CHANGE VA TO REFERENCE NEXT PAGE
2389 014216 020027 001152      CMP      R0,#STAEND     ;SET ALL W-BITS IN CURRENT MODE
2390 014222 002760      BLT      LOOP32        ;TURN OFF MEMORY MANAG.
2391 014224 012701 001034      MOV      #ADRTAB,R1     ;CHECK FOR DONE SETTING THE W BITS
2392 014230 012702 000010      MOV      #10,R2        ;IF NOT, LOOP TO DO NEXT MODE
2393
2394 014234 032771 000100 000000      LOP32D: MOV      #10,R2      ;SETUP R1 TO REFERENCE ADDRESSES OF PDR'S OF PDR'S
2395 014242 001001      BNE
2396 014244 104006      HLT
2397
2398
2399
2400 014246 005721      TST      (R1)+         ;AT END OF EACH SET OF REGISTERS
2401 014250 077207      SOB
2402 014252 062701 000020      ADD
2403
2404 014256 020127 001132      CMP      R1,#ADREND     ;CHECK W BIT
2405 014262 002762      BLT      LOP32E        ;CHECK ALL PDR'S IN THIS SET
2406 014264 005037 177776      CLR      #SPS           ;CHANGE R1 TO REFERENCE NEXT
2407 014270 005277 164530      INC
2408 014274 000035      RESET
2409 014276 000005      RESET
2410 014300 012721 001034      MOV      #ADRTAB,R1     ;SET OF PDR ADDRESSES
2411 014304 012702 000010      MOV      #10,R2        ;CHECK FOR DONE
2412
2413 014310 032771 000100 000000      LOP32F: MOV      #10,R2      ;IF NOT, CHECK NEXT SET OF PDR'S
2414 014316 001001      BNE
2415 014320 104006      HLT
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2421 014332 020127 001132      CMP      R1,#ADREND     ;CHECK FOR DONE
2422 014336 002762      BLT      LOP32F        ;IF NOT, CHECK NEXT SET OF PDR'S
2423 014340 005077 164460      CLR      #SR0           ;SET MODE TO KERNEL
2424
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2433 014344 104400      ;SHOW THAT A DATO TO A PDR WILL CLEAR THE W BIT
2434 014346 012706 001000      ;EVEN WHEN THE INSTRUCTION ALSO CAUSES A TRAP REFERENCE TO
2435 014352 004767 002026      ;THE CORRESPONDING PAGE
2436 014356 000056      ;MAP KERNEL PAGE 1 RRW AND MAKE A WRITE ACCESS TO PAGE 1
2437 014360 104006      ;TO SET THE W BIT
2438 014362 012767 002000 001266      ;THEN LOAD THE PDR, MAKING A TRAP REFERENCE TO PAGE 1 IN THE SOURCE
2439 014370 004767 001020      ;FETCH OF THE SAME INSTRUCTION-THE W BIT SHOULD BE CLEARED DUE
2440 014374 004767 002070      ;TO THE DATO TO THE PDR
2441 014400 012777 077406 164470      TEST56: SCOPE
2442 014406 012777 000001 164410      MOV      #KSTACK,SP      ;INITIALIZE KERNEL STACK POINTER
2443 014414 013737 020000 020000      JSR      PC,ORDER        ;CHECK TEST SEQUENCE + INIT SR0
2444 014422 022777 077506 164446      S5
2445 014430 001401      HLT
2446 014432 104006      ;TEST NUMBER
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2448
2449 014434 012767 077506 164360      MOV      #2000,ICOUNT    ;TEST EXECUTED OUT OF SEQUENCE
2450 014442 016777 004354 164426      JSR      X7,RWALL        ;INITIALIZE ALL PAGES RW, BANK 0
2451
2452 014450 022777 077406 164420      JSR      PC,KERN7        ;MAP KERNEL PAR/PDR 7 TO EXT BANK
2453 014456 001401      MOV      #77406,#KPDR1  ;MAKE KERNEL PAGE 1 RRW
2454 014460 104006      MOV      #1,#SR0        ;TURN ON MEMORY MANAG.
2455 014462 005077 164336      CMP      #20000,#20000  ;READ AND WRITE PAGE 1
2456
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2458
2459 014466 104400      CMP      #77506,#KPDR1  ;CHECK PDR OF PAGE 1
2460 014470 012706 001000      BEQ      .+4
2461 014474 004767 001704      HLT
2462 014500 000057      ;KERNEL PAGE 1 PDR
2463 014502 104006      INCORRECT - W BIT SHOULD
2464 014504 012767 000010 001144      MOV      #77506,TEMP     ;BE SET DUE TO PREVIOUS MOVE INSTRUCTION
2465 014512 004767 000676      MOV      TEMP+20000,#KPDR1 ;LOAD TEMP WITH VALUE TO BE MOVED TO KPDR1
2466 014516 004767 001746      MOV      #77406,#KPDR1  ;PAGE 1 REFERENCE SHOULD SET
2467 014522 012777 077406 164346      CMP      #77406,#KPDR1  ;BUT DATO TO THE PDR CLEARS W BIT
2468 014530 012777 000001 164266      BEQ      .+4
2469 014536 013737 020000 020000      CLR      #SR0           ;CHECK PAGE 1 PDR
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2417 014322 005721      TST      (R1)+         ;ADDRESS IS POINTED TO BY R1
2418 014324 077207      SOB
2419 014326 062701 000020      ADD
2420
2421 014332 020127 001132      CMP      R1,#ADREND     ;MOVE POINTER
2422 014336 002762      BLT      LOP32G        ;CHECK ALL PDR'S IN THIS SET
2423 014340 005077 164460      CLR      #SR0           ;CHANGE R1 TO REFERENCE NEXT
2424
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2433 014344 104400      ;SHOW THAT A DATO TO A PDR WILL CLEAR THE W BIT
2434 014346 012706 001000      ;EVEN WHEN THE INSTRUCTION ALSO CAUSES A TRAP REFERENCE TO
2435 014352 004767 002026      ;THE CORRESPONDING PAGE
2436 014356 000056      ;MAP KERNEL PAGE 1 RRW AND MAKE A WRITE ACCESS TO PAGE 1
2437 014360 104006      ;TO SET THE W BIT
2438 014362 012767 002000 001266      ;THEN LOAD THE PDR, MAKING A TRAP REFERENCE TO PAGE 1 IN THE SOURCE
2439 014370 004767 001020      ;FETCH OF THE SAME INSTRUCTION-THE W BIT SHOULD BE CLEARED DUE
2440 014374 004767 002070      ;TO THE DATO TO THE PDR
2441 014400 012777 077406 164470      TEST56: SCOPE
2442 014406 012777 000001 164410      MOV      #KSTACK,SP      ;INITIALIZE KERNEL STACK POINTER
2443 014414 013737 020000 020000      JSR      PC,ORDER        ;CHECK TEST SEQUENCE + INIT SR0
2444 014422 022777 077506 164446      S5
2445 014430 001401      HLT
2446 014432 104006      ;TEST NUMBER
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2449 014434 012767 077506 164360      MOV      #2000,ICOUNT    ;TEST EXECUTED OUT OF SEQUENCE
2450 014442 016777 004354 164426      JSR      X7,RWALL        ;INITIALIZE ALL PAGES RW, BANK 0
2451
2452 014450 022777 077406 164420      JSR      PC,KERN7        ;MAP KERNEL PAR/PDR 7 TO EXT BANK
2453 014456 001401      MOV      #77406,#KPDR1  ;MAKE KERNEL PAGE 1 RRW
2454 014460 104006      MOV      #1,#SR0        ;TURN ON MEMORY MANAG.
2455 014462 005077 164336      CMP      #20000,#20000  ;READ AND WRITE PAGE 1
2456
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2458
2459 014466 104400      CMP      #77506,#KPDR1  ;CHECK PDR OF PAGE 1
2460 014470 012706 001000      BEQ      .+4
2461 014474 004767 001704      HLT
2462 014500 000057      ;KERNEL PAGE 1 PDR
2463 014502 104006      INCORRECT - W BIT SHOULD
2464 014504 012767 000010 001144      MOV      #77506,TEMP     ;BE SET DUE TO PREVIOUS MOVE INSTRUCTION
2465 014512 004767 000676      MOV      TEMP+20000,#KPDR1 ;LOAD TEMP WITH VALUE TO BE MOVED TO KPDR1
2466 014516 004767 001746      MOV      #77406,#KPDR1  ;PAGE 1 REFERENCE SHOULD SET
2467 014522 012777 077406 164346      CMP      #77406,#KPDR1  ;BUT DATO TO THE PDR CLEARS W BIT
2468 014530 012777 000001 164266      BEQ      .+4
2469 014536 013737 020000 020000      CLR      #SR0           ;CHECK PAGE 1 PDR
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2578 015222 100373
2579 015224 013701 000042 LOGIC: MOV BPL 38 ;BRANCH UNTIL IT DOES
2580 015230 001405 BEQ #42,R1 ;MONITOR HOOK
2581 015232 000005 RESET
2582 015234 004711 LOGIC: JSR PC,R1
2583 015236 000240 NOP
2584 015240 000240 NOP
2585 015242 000240 NOP
2586 015244 000167 163734 END: JMP START
2587
2588
2589 ;
2590 015250 005015 030461 031457 ;MESSAGE AREA
2591 015256 020064 042515 047515 MTIT: .ASCII '<15><12>'11/34 MEMORY MANAGEMENT LOGIC TEST MAINDEC-11=DFKTA-A'<15><12>'
2592 015264 054522 046400 047101
2593 015272 0-3501 046505 047105
2594 015300 020124 047514 044507
2595 015306 020103 042524 052123
2596 015314 046440 044501 042116
2597 015322 041505 030455 026461
2598 015330 043104 052113 026501
2599 015336 006501 040012
2600 015342 005815 041520 020075 MPC: .ASCII '<15><12>'PC= #'
2601 015350 120
2602 015351 040 050040 036523 MPS: .ASCII ' PS= #'
2603 015356 040040
2604 015360 177637 000377 BELL: .ASCIZ '<207><377><377>'
2605 015364 177452 000377 ASTER: .ASCIZ '/#/<377><377>'
2606
2607
2608
2609 ;SUBROUTINE TO CLEAR ALL MEMORY MANAG. REGISTERS (EXCEPT SR1,SR2)
2610 015370 005077 163430 CLRALL: CLR #SR0
2611 015374 005000 CLR R0
2612 015376 012701 000040 MOV #32,R1 ;COUNT OF REGISTERS TO BE CLEARED
2613 015402 005070 001034 CLR R0 ;CLEAR REGISTERS THRU ADDRESS TABLE
2614 015406 005720 CLR #ADRTAB(R0) ;MOVE POINTER
2615 015410 077104 TST (R0) ;LOOP TILL DONE
2616 015412 000207 SOB R1,CLRRLP
2617
2618 ;SUBROUTINE TO MAKE ALL PAGES RW, BANK 0, 4K, UP
2619 015414 005077 163404 RWALL: CLR #SR0
2620 015420 012701 001034 MOV #ADRTAB,R1 ;R1 POINTS TO ADDRESS TABLE
2621 015424 012700 000010 RWL1: MOV #10,R0 ;R0 IS COUNTER
2622 015430 005071 000020 RWL2: CLR #20(R1) ;CLEAR PAR
2623 015434 012731 077406 MOV #77406,#(R1)+ ;SET PDR RW, 4K
2624 015440 077005 SOB R0,RWL2
2625 015442 062701 000020 ADD #20,R1
2626 015446 020127 001132 CMP R1,#ADREND ;POINTER TO NEXT GROUP
2627 015452 002764 BLT RWL1
2628 015454 000207 RTS X7
2629
2630 ;ROUTINE TO LOOP THRU A SINGLE INSTRUCTION TEST
2631 ;LOAD THE STARTING ADDRESS OF THE TEST

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2632 ;YOU WISH TO RUN (THE ADDRESS OF THE TESTX
2633 ;TAG) IN LOCATION "RETRNX" BELOW
2634 ;NOTE THAT SW11 MUST BE DOWN TO RUN THIS TEST.
2635 015456 005037 177776 TESTX: CLR #PS
2636 015462 012706 001000 MOV #KSTACK,SP
2637 015466 012737 140000 MOV #140000,#PS ;SETUP USER TRAP
2638 015474 012706 000400 MOV #USTACK,SP
2639 015500 005037 177776 CLR #PS
2640 015504 062767 000030 ADD #2,RETRNX ;ADD 2 TO POINT TO INSTRUCTION AFTER
2641 015512 000000 HALT ;SET SR OPTIONS
2642 015514 005067 000140 CLR SCOPEF ;KEEP COUNT AT ZERO
2643 015520 012767 000134 MOV #XLOOP,RETURN ;LOAD SCOPE LOOP RETURN POINTER
2644 015526 000177 000010 JMP #RETRNX ;JUMP TO TEST
2645 015532 005067 000122 XLOOP: CLR SCOPEF ;KEEP COUNT AT ZERO
2646 015536 000177 000000 JMP #RETRNX ;JUMP TO TEST
2647 015542 000000 RETRNX: 0
2648 ;SCOPE AND/OR ITERATION LOOP FOR EACH TEST 4000 TIMES
2649 015544 032777 040000 163426 SCOPEC: BIT #BIT14,#SR ;TEST SR FOR SCOPE
2650 015552 001015 BNE SCOPEB ;YES,SCOPE
2651 015554 032777 004000 163416 BIT #BIT11,#SR ;NO-TEST FOR ITERATION
2652 015562 001020 BNE SCOPEF ;INHIBIT ITERATION
2653 015564 026767 000070 000064 CMP SCOPEF, ICOUNT ;COMPARE CURRENT COUNT TO MAX NUMBER
2654 015572 100014 BPL SCOPEF ;EXIT-DONE
2655 015574 005267 000060 INC SCOPEF ;INCREMENT COUNT
2656 015600 012737 000340 177776 MOV #340,#PS ;PREVENT TRAPPING WHILE MOVING STACK
2657 015606 022626 SCOPEB: CMP (6)+,(6)+ ;REPOSITION STACK
2658 015610 005037 177776 CLR #PS
2659 015614 005077 163204 CLR #SR0
2660 015620 000177 000036 JMP #RETURN ;REPEAT TEST
2661 015624 005067 000030 SCOPEF: CLR SCOPEF ;CLEAR COUNT
2662 015630 005267 163340 INC TESTCT ;STEP TEST COUNTER TO ALLOW CHECKING
2663 ;ORDER OF EXECUTION.
2664 015634 011667 000022 MOV #0,RETURN ;SAVE SCOPE RETURN POINTER
2665 015640 022626 CMP (6)+,(6)+ ;RETURN INLINE=NEXT TEST
2666 015642 005037 177776 CLR #PS
2667 015646 005077 163152 CLR #SR0
2668 015652 000177 000004 JMP #RETURN
2669 ICOUNT:4000 ;ITERATION COUNT
2670 SCOPEF: 0 ;COUNT LOCATION FOR ITERATION LOOP
2671 015662 000000 RETRNX: 0 ;ADDRESS OF LAST TEST
2672
2673 ;ENTERED WITH SYSTEM TRAP CALL (HLT)
2674 ;PRINT OUT THE ERROR PC+2 AND STATUS REGISTER
2675 015664 012767 000340 162104 PRINT: MOV #340,PS ;SET PRIORITY TO 7
2676 015672 032777 020000 163300 BIT #BIT13,#SR ;TEST FOR INHIBIT PRINT OUT
2677 015700 001401 BEQ .+4 ;BRANCH TO PRINT
2678 015702 000430 BR CK ;INHIBIT, CHECK FOR HALT
2679 015704 012667 000066 MOV (6)+,SAVPC ;PC OF FAILING ROUTINE
2680 015710 012667 000064 MOV (6)+,SAVPSR ;PSR OF ERROR CONDITION
2681 015714 024646 CMP -(6),-(6) ;RESTORE STACK
2682 015716 012767 000200 162052 MOV #200,PS
2683 015724 016767 000046 000374 MOV SAVPC,PTEMP1 ;LOAD WITH FAILING PC+2

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2684 015732 004767 000044 JSR PC,TYPE
2685 015736 015342 MPC
2686 015740 004767 000116 JSR PC,PRSHRT ;PRINT FAILING PC+2
2687 015744 004767 000032 JSR PC,TYPE
2688 015750 015351 MFS
2689 015752 016767 000022 000346 MOV SAVPSR,PTEMP1 ;LOAD PROCESSOR STATUS
2690 015760 004767 000130 JSR PC,PROCT ;PRINT PROCESSOR STATUS
2691 015764 005777 163210 CKI TST ;CHECK SR FOR HALT SWITCH
2692 015770 100001 BPL ;BRANCH IF NOT SET
2693 015772 000000 HALT ;HALT ON ERROR UP
2694 015774 000002 RTI ;RETURN TO MAIN LINE
2695 015776 000000 SAVPC: 0
2696 016000 000000 SAVPSR: 0
2697
2698
2699 016002 010067 000052 ;SUBROUTINE TO OUTPUT ASCII MESSAGE ON TELETYPE
2700 016006 011600 TYPE: MOV ;(6),X0
2701 016010 062716 000002 ADD #2,#X6 ;GET ADDRESS THAT CONTAINS MESSAGE ADDRESS
2702 016014 011000 MOV ;SET UP EXIT
2703 016016 112067 000034 TYPA: MOVB ;(0)+,TYPDAT ;GET CHARACTER
2704 016022 122767 000100 000026 CMVB #100,TYPDAT ;CHECK FOR "*" CHARACTER
2705 016030 001003 BNE TYPB ;BRANCH IF NOT "*"
2706 016032 016730 000022 MOV SAVR0,#X0 ;RESTORE R0
2707 016036 000207 RTS PC ;TERMINATOR CHAR, EXIT
2708 016040 116777 000012 162752 TYPR: MOVSB TYPDAT,#TOBR ;OUTPUT CHAR TO PRINTER
2709 016046 105777 162744 TSTB ;WAIT FOR TTY READY
2710 016052 100375 BPL ;=4
2711 016054 000760 BR TYPA
2712 016056 000000 TYPDAT: 0
2713 016060 000000 SAVR0: 0
2714
2715
2716 ;SUBROUTINE TO PRINT OUT OCTAL NUMBER
2717 ;PRSHRT DELETES LEADING ZEROS
2718 ;PROCT PRINTS OUT 6 OCTAL DIGITS
2719 016062 012767 000001 000232 PRSHRT: MOV #1,PRFLG ;SET FLAG TO INDICATE SHORT PRINTOUT
2720 016070 005767 000232 TST PTEMP1 ;CHECK FOR ZERO
2721 016074 001011 BNE PROCT+4 ;BRANCH IF NOT ZERO
2722 016076 012777 000260 162714 MOV #260,#TOBR ;OUTPUT A SINGLE ZERO
2723 016104 105777 162706 TSTB ;WAIT FOR TTY READY
2724 016110 100375 BPL ;=4
2725 016112 000207 RTS ;RETURN
2726 016114 005067 000202 PROCT: CLR PRSFLG ;CLEAR FLAG TO INDICATE FULL PRINTOUT
2727 016120 005067 000206 CLR PTEMP3 ;CLEAR R4 FOR COUNTING CHARACTERS OUTPUT
2728 016124 005067 000174 CLR PRFLG ;INITIALIZE CARRY FLAG FOR ROTATES
2729 016130 012767 000260 000172 MOV #260,PTEMP2 ;SETUP R3
2730 016136 005767 000164 TST PTEMP1 ;CHECK BIT 15 OF NUMBER
2731 016142 100002 BPL ;=4
2732 016144 005267 000160 INC PTEMP2 ;INCREMENT R3 IF ONE
2733 016150 006167 000152 ROL PTEMP1 ;ROTATE LEFT MOST OCTAL TO RIGHT END
2734 016154 006167 000146 ROL PTEMP1
2735 016160 005567 000140 ADC PRFLG ;STORE CARRY
2736 016170 001404 P.CK: TST PRSFLG ;CHECK FOR SHORT PRINTOUT
2737 016172 026727 000132 000260 BEQ ;WAIT
CMP PTEMP2,#260 ;CHECK FOR ZERO IF SET

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2738 016200 001410 BEQ P.CONT ;IF SET, GO TO NEXT CHARACTER
2739 016202 016777 000122 162610 P.WAIT: MOV PTEMP2,#TOBR ;OUTPUT NEXT CHARACTER
2740 016210 105777 162602 TSTB ;WAIT FOR TTY READY
2741 016214 100375 BPL ;=4
2742 016216 005067 000100 CLR PRSFLG ;PRINT REST OF NUMBER AFTER A NON-ZERO DIGIT
2743 016222 005267 000104 P.CONT: INC ;COUNT
2744 016226 026727 000100 000006 CMP PTEMP3,#6 ;CHECK FOR DONE
2745 016234 001001 BNE P.CNT1 ;BRANCH IF NOT DONE
2746 016236 000207 RTS
2747 016240 000241 P.CNT1: CLC ;CLEAR CARRY
2748 016242 005767 000056 TST PRFLG ;CHECK FOR PREVIOUS CARRY
2749 016246 001403 BEQ ;=10 ;BRANCH IF PREVIOUSLY ZERO
2750 016250 005067 000050 CLR PRFLG ;INITIALIZE FLAG
2751 016254 000261 SEC ;SET CARRY
2752 016256 006167 000044 ROL PTEMP1 ;ROTATE NEXT CHARACTER INTO RIGHT END OF REGISTE
2753 016262 006167 000040 ROL PTEMP1
2754 016266 006167 000034 ROL PTEMP1
2755 016272 005567 000026 ADC PRFLG ;STORE CARRY
2756 016276 016767 000024 000024 MOV PTEMP1,PTEMP2 ;LOAD DATA INTO R3
2757 016304 042767 177770 000016 BIC #17770,PTEMP2 ;CLEAR ALL BUT LOWEST OCTAL DIGIT
2758 016312 052767 000260 000010 BIS #260,PTEMP2 ;SET TO ASCII EQUIVALENT
2759 016320 000721 BR ;LOOP
2760 016322 000000 PRSFLG: 0
2761 016324 000000 PRFLG: 0
2762 016326 000000 PTEMP1: 0
2763 016330 000000 PTEMP2: 0
2764 016332 000000 PTEMP3: 0
2765
2766
2767 ;EMT HANDLER
2768 016334 011667 000032 ;FIRST 3 CALLS LEFT OPEN IN TABLE FOR EASY PATCHES
EMTSRV: MOV ;GET CALL
2769 016340 162767 000002 000024 SUB #2,EPC
2770 016346 017767 000020 000016 MOV ;EPC,EPC
2771 016354 105067 000013 CLR ;EPC+1
2772 016360 062767 016374 000004 ADD ;EMTAB,EPC ;SAVE OFFSET ONLY
2773 016366 017707 000000 MOV ;EPC,PC ;POINT TO TABLE OF ADDRESSES
2774 016372 000000 EPC: 0 ;JUMP TO DESIRED ROUTINE
2775 104000 PATCH1=EMT+0
2776 104002 PATCH2=EMT+2
2777 104004 PATCH3=EMT+4
2778 016374 104000 ENTAB: PATCH1
2779 016376 104002 PATCH2
2780 016400 104004 PATCH3
2781 016402 015664 PRINT
2782
2783 ;SUBROUTINE TO CHECK TEST SEQUENCE
2784 016404 005037 177776 ORDER: CLR ;CLEAR PROCESSOR STATUS
2785 016410 011667 000052 MOV ;(SP),TEMPN ;GET TEST NUMBER ADDRESS
2786 016414 017767 000046 000044 MOV ;TEMPN,TEMPN ;GET TEST NUMBER
2787 016422 032777 002000 162550 BIT ;BIT10,;SR
2788 016430 001404 BEQ ORDERB
2789 016432 016700 000030 MOV ;TEMPN,R0
2790 016436 000005 RESET
2791 016440 000000 HALT

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2792	016442	026767	162526	000016	ORDERB1	CMP	TESTCT,TEMPN		
2793	016450	001403				BEQ	ORDERA		
2794	016452	062716	000002			ADD	#2,(SP)		JIS TEST SEQUENCE CORRECT
2795	016456	000207				RTS	PC		IUPDATE FOR ERROR RETURN
2796	016460	062716	000004		ORDERA1	ADD	#4,(SP)		JUPDATE FOR GOOD RETURN
2797	016464	000207				RTS	PC		
2798	016466	000000				TEMPN:	0		
2799						JMAP	KERNEL PAR/PDR 7 TO EXTERNAL BANK		
2800	016470	012777	007600	162438	KERN7:	MOV	#7600,#KPAR7		
2801	016476	012777	077406	162406		MOV	#77406,#KPDRT		
2802	016504	000207				RTS	PC		
2803		017712					.*17712		
2804									
2805	017712	125252			DESTAD:		125252		
2806		000001					.END		

ADD23	004726	ADD24	005126	ADD42	014664	ADREND	001132
ADRTAB	001034	ADR11	012136	ADR2	011076	ADR25	005322
ADR25A	005324	ADR36	007560	ADR36A	007642	ADR36B	007740
ADR36C	007742	ADR37	010114	ADR37A	010176	ADR37B	010274
ADR37C	010276	ADR40	010450	ADR40A	010532	ADR40B	010630
ADR40C	010632	AD13	002572	AD13A	002606	AD13B	002636
AD13C	002666	AD21A	004020	AD21B	004032	AD21C	004142
ASTER	015364	BELL	015360	BIT0	000001	BIT1	000002
BIT10	002000	BIT11	004000	BIT12	010000	BIT13	020000
BIT14	040000	BIT15	100000	BIT2	000004	BIT3	000010
BIT4	000020	BIT5	000040	BIT6	000100	BIT7	000200
BIT8	000400	BIT9	001000	BLK20	003546	BLOCKS	001176
CK	015764	CKWBIT	013524	CLRALL	015370	CLRLP	015402
CNT22B	004276	CNT22C	004356	CNT22D	004452	CNT22E	004546
CNT31A	005570	CNT31B	005660	CNT11	012202	CNT23	012664
CONT24	013100	CONT42	014744	CNT5	001760	C25	013254
DAT116	003112	DESTAD	017712	DISPLA	001202	DISPRE	000174
DONE13	012346	DONE16	012460	DONE2	011126	DONE23	012676
DONE24	013112	DONE25	013324	DONE36	010016	DONE37	010352
DONE40	010706	DONES	011560	DONE5A	001776	DONE7	011756
DONE5	005440	DST21A	004134	DST21B	004136	DST21C	004140
ENTAB	016374	ENTSRV	016334	END	015244	END20	003632
END22E	004636	END35	007464	EDP	015162	EPC	016372
ERR22A	004264	ERR22B	004350	ERR22C	004436	ERR22D	004532
ERR22E	004630	EXIT10	002360	EXIT11	002510	EXIT2	001474
EXIT21	004144	EXIT23	005046	EXIT24	005242	EXT27	013560
FTITLE	001172	HLT	104006	ICOUNT	015656	INT25	005334
INT35	007010	INT36	007576	INT36A	007652	INT36B	007752
INT37	010132	INT37A	010206	INT37B	010306	INT40	010466
INT40A	010542	INT40B	010642	IDT35	006606	KERN7	016470
KPAR0	001114	KPAR1	001116	KPAR2	001120	KPAR3	001122
KPAR4	001124	KPAR5	001126	KPAR6	001130	KPAR7	001132
KPDR0	001074	KPDR1	001076	KPDR2	001100	KPDR3	001102
KPDR4	001104	KPDR5	001106	KPDR6	001110	KPDR7	001112
KRET34	006172	KSTACK	001000	KTSTA	001166	KTVEC	001164
K123	001012	K134	001014	LOGIC	015234	LOGICT	015224
LOOP10	002266	LOOP11	002416	LOOP2	001434	LOOP23	012542
LOOP24	012764	LOOP3	001534	LOOP3A	001542	LOOP3B	001546
LOOP32	014164	LOOP4	001624	LOOP4A	001632	LOOP4B	001636
LOOP5	011464	LOOP6	002044	LOOP6A	002052	LOOP7	002150
LOOP7A	002156	LOOP10A	002274	LOOP10B	002314	LOOP10C	002322
LOOP11A	002424	LOOP11B	002444	LOOP11C	002452	LOP27	013456
LOP27A	013470	LOP31A	005536	LOP31B	005542	LOP31C	005574
LOP31D	005606	LOP31E	005636	LOP31F	005642	LOP32C	014202
LOP32D	014230	LOP32E	014234	LOP32F	014304	LOP32G	014310
LOP5A	011542	LOP5AA	001722	LOP5B	001740	L25A	013210
L25B	013220	L40	014566	MPC	015342	MPS	015351
MTIT	015250	NG35B	006564	NG35C	006774	NG35D	007216
NG35E	007436	NOP	000240	ODDAD	007242	OK35B	006602
OK35C	007004	OK35D	007232	OK35E	007446	ORDER	016404
ORDERA	016460	ORDERB	016442	PAGES	001156	PAG20	003510
PARTAB	001140	PATCH1	104002	PATCH2	104002	PATCH3	104004
PC	000007	PDREND	001136	PDRM2	001170	PDRTAB	001134
PRFLG	016324	PRINT	015664	PROCT	016114	PR3FLG	016322

PRSHRT	016062	PS	177776	PTEMP1	016326	PTEMP2	016330
PTEMP3	016332	P,CK	016164	P,CNT1	016240	P,CONT	016222
P,WA17	016202	RETRN	015542	RETURN	015062	RET11	012150
RET13A	012312	RET16	012450	RET2	011102	RET23A	012610
RET23B	012630	RET24A	013032	RET24B	013046	RET25	013276
RET3	011240	RET33	006020	RET42	014712	RET5	011512
RET7A	011662	RET7C	011736	RWALL	015414	RWL1	015424
RWL2	015430	R0	X000000	R1	X000001	R2	X000002
R3	X000003	R4	X000004	R5	X000005	R6	X000006
R7	X000007	SAVEA	001160	SAVEB	001162	SAVPC	015776
SAVPSR	016000	SAVR0	016060	SCOPE	100400	SCOPEB	015606
SCOPEC	015544	SCOPEF	015660	SCOPEG	015626	SP	X000006
SR	001200	SR0	001024	SR0H	001026	SR1	001030
SR2	001032	STAEND	001152	STAPNT	001154	START	001204
STATAB	001144	STATUS	177776	STAT20	003430	SWREG	000176
TCSR	001016	TOBR	001020	TEHP	001022	TEMPN	016466
TESTCT	001174	TESTN	000062	TESTX	015456	TEST1	001332
TEST10	002222	TEST11	002360	TEST12	002512	TEST13	002554
TEST14	002710	TEST15	002774	TEST16	003114	TEST17	003310
TEST2	001400	TEST20	003700	TEST21	004146	TEST22	004642
TEST23	005050	TEST24	005244	TEST25	005452	TEST26	005740
TEST27	006044	TEST3	001474	TEST30	006330	TEST31	007500
TEST32	010034	TEST33	010370	TEST34	010724	TEST35	011004
TEST36	011146	TEST37	011304	TEST4	001576	TEST40	011406
TEST41	011572	TEST42	011764	TEST43	012056	TEST44	012214
TEST45	012360	TEST46	012472	TEST47	012714	TEST5	001674
TEST50	013130	TEST51	013336	TEST52	013404	TEST53	013560
TEST54	013732	TEST55	014104	TEST56	014344	TEST57	014466
TEST6	002004	TEST60	014610	TEST61	014756	TEST7	002116
TST10	002256	TST10F	002356	TST11	002406	TST11F	002506
TYPA	016016	TYPB	016040	TYPDAT	016056	TYPE	016002
UPAR0	001054	UPAR1	001056	UPAR2	001060	UPAR3	001062
UPAR4	001064	UPAR5	001066	UPAR6	001070	UPAR7	001072
UPDR0	001034	UPDR1	001036	UPDR2	001040	UPDR3	001042
UPDR4	001044	UPDR5	001046	UPDR6	001050	UPDR7	001052
URET34	006226	USTACK	000400	XLOOP	015532	.	017714

ERRORS DETECTED: 0

*DFKTA,DFKTA,DFKTA, SRC/SOL
 RUN-TIME: 10 21 0 SECONDS
 CORE USED: 6K