```
+---+---+---+---+---+---+---+---+
| d | i | g | i | t | a | l |
+---+---+---+---+---+---+---+---+
```
INTEROFFICE MEMO

To: T-11 Spec. Distribution

Date: 24 MAR 82
From: David Forsythe D.D.F.
Dept: Low Cost LSI
Ext: 225-5283
Decnet: SNICKR::FORSYTHE
Loc/Mail Stop: HL1-1/Q08

SUBJECT: T-11 UPDATE

The T-11 is now a proven microprocessor which is being
manufactured in production quantities (over 3500 to date) and has
been successfully incorporated into many system designs and
applications. The T-11 has achieved Limited Release status at
Hudson as well as at Synertek, our second source. T-11's are now
available to the outside world through Chip Sales as u/T-11. The
T-11 HOT LINE number is (DTN) 225-5061; the HOT LINE is available
to internal users for answering T-11 applications questions.

As we look ahead, the price of T-11's will be coming down as
production costs decrease with improved yields, better testing,
etc. The predicted transfer cost for FY83 is $25 and the cost
for FY84 is not to exceed $18 per chip. Reduced pricing should
open up new areas for T-11 applications.

Revision E of the T-11 Engineering Specification includes all
specification updates as of 1 MAR 82. All changes were approved
at Chip Change Control (CCC) Meetings. These meetings give T-11
users a chance to review proposed changes so the changes that are
approved will not be user sensitive. Most of the changes between
Revisions D and E of the Spec. fall into the category of
documentation clarification. For specific details of the
changes, please refer to "Documentation of T-11 Engineering
Specification History".

This will be the last automatic update you will receive.
Subsequent updates will be processed through the normal ECO
procedure. See HL Document Control in the future.

THE T-11 SPECIFICATION IS COMPANY CONFIDENTIAL, SO,
_____

PLEASE HAVE YOUR OLD SPECIFICATIONS SHREDDED.
_____

Thank you for your interest in the T-11 Microprocessor.

```
+---+---+---+---+---+---+---+
| d | i | g | i | t | a | l |      I N T E R O F F I C E      M E M O
+---+---+---+---+---+---+---+
```

To: T-11 ENGINEERING   Date: 1 MAR 82
    SPECIFICATION DIST.   From: David Forsythe
                                     Dept: Low Cost LSI
                                     Ext: 225-5283
                                     Decnet: SNICKR::FORSYTHE
                                     Loc/Mail Stop: HL1-1/Q08

SUBJECT: DOCUMENTATION OF T-11 ENGINEERING SPECIFICATION HISTORY

In order to better document the history of the T-11 Engineering
Specification, the following lists of the differences between
Rev's. C and D and Rev's. D and E of the T-11 Engineering
Specification have been compiled. I would also like to draw your
attention to two conventions which were adopted in order to help
document the changes between revisions of the T-11 Engineering
Spec. Each page has a revision letter on it corresponding to the
last revision in which any changes were made on that page. For
instance, a page with "Rev B" on it was changed between Revisions
A and B, but has had no changes since. Also, the lines that were
changed between the current and former revisions of each page are
denoted by a "|" in the right hand margin.

The following differences exist between Rev. C and Rev. D of the
T-11 Engineering Specification.

1. Page 8, Section 2.2.7 Signal Utilization for Each Bus Mode:
    A column in the table was added with the heading "Dynamic All
    Modes" and entries were made in the AI rows. Notes were
    added in 8 Bit Dynamic mode and 16 Bit Dynamic mode, "In
    dynamic mode at refresh time the AI are the output of an 8
    bit counter"; in 16 Bit Dynamic 64K mode, "Caution because
    DAL0 maps to AI<6> word and byte operation are mapped to
    different memory locations unless external AI logic is
    used."; for AI<0> in 16 Bit Dynamic 4K/16K mode, "Fetch cycle
    if not doing a refresh cycle."

2. Page 14, Sections 2.3.16 DAL<15:8> (Input/Output TRI-STATE)
    Data and Address Lines and 2.3.17 Dal<7:0> (Input/Output)
    Data and Address Lines: In explanation of when the DALs
    output indeterminate data, "byte not addressed during byte
    operation" was changed to "byte not addressed during
    Write/byte operation with ready slips".

3. Page 15, Section 2.3.18 AI<7:0> (Input/Output TRISTATE)
    Address and Interrupt: the paragraph;

        During refresh, the refresh address is provided on
        the AI Lines. The refresh counter is decremented
        after each refresh.

    was changed to;

        During refresh in all dynamic modes, the refresh
        address 8 bit counter is provided on the AI Lines.
        The refresh counter is decremented after each
        refresh.

    Also, Refresh Counter Bit 7 was designated "MSB" and Refresh
    Counter Bit 0 was designated "LSB".

4. Page 17, Section 2.3.18: Under the FETCH description, the
    note, "CAUTION: During Refresh, the AI lines have the refresh
    counter address on them." was added.

5. Page 18, Section 2.3.19 Sample Signal Equivalency for
    Specific Manufacturer's Chip Families: For the Mostek
    MK4027-3/4, the Equivalent T-11 Signals for Manufact. Family
    Signals A<5:0> were changed from "AI<5:0>" to "AI<6:1>"; for
    the Mostek MK4116-2/3, the Manufact. Family Signals for the
    Equivalent T-11 Signals, AI<7:1>, were changed from "A<7:1>"
    to "A<6:0>".

6. Page 23, Section 3.1 Absolute Maximum Ratings: The
    statement, "Currents sourced by the DC310 are indicated by a
    negative prefix to the value listed." was added. Section 3.2
    Static Characteristics: "TJ = 0 to 100 C" was changed to "TA
    = 0 to 70 C"; the IIL limit was changed from +/-20 uA to
    +/-50 uA; the IFL limit was changed from +/-20 uA to +/-50
    uA. The parameter IILP was deleted. The current direction
    on the IIH parameters was corrected to correspond with the
    current direction convention; IIH (MIN) was changed from 0.1
    mA to -0.1 mA, and IIH (MAX) was changed from 1 uA to -1 mA
    (the uA to mA change was a documentation error correction).

    The following new parameters were added in the Rev. D. Spec.:
    IXLIH (Input High Current on XTL1) has a maximum limit of
    +700 uA with 2.4<VIN<VCC and XTL0 grounded, IXLIL (Input Low
    Current on XTL1 has a maximum limit of -6.4 mA with
    -0.5<VIN<+0.8V and XTL0 grounded, and VOHB (Output High
    Voltage for -BCLR has a minimum limit of 2.2V with IOH = -700
    uA and the -BCLR line terminated with a 1K resistor to VSS.

7. Page 24, Section 4.1 Bus Timing Annotated for Maximum XTL1,
    XTL0 Operating Frequency: Limit on TASF changed from
    "(T - 48) = 85 ns min" to "(T - 83) = 50 ns min"; TASR
    changed from "(T - 68) = 65 ns min" to "(T - 83) = 50 ns
    min".

8. Page 26, Section 4.1: Documentation error corrected; for
    TMRC, "(2T + 10) = 177 ns min" changed to "(2T + 10) = 277 ns
    min".

9. Page 27, Section 4.1: TNHC limit changed from "(T - 10) =
    123 ns min" to "(T - 32) = 101 ns min"; TNHR limit changed
    from "(T - 118) = 15 ns min" to "(T - 108) = 25 ns min";
    TNHP limit changed from "(T - 21) = 112 ns min" to "(T - 43)
    = 90 ns min"; TNMP limit changed from "(6T - 30) = 770 ns
    min" to "(6T - 66) = 734 ns min".

10. Page 28, Section 4.1: TPIP limit changed from "(2T - 37) =
    230 ns min" to "(2T - 47) = 220 ns min"; TPSN limit changed
    from "(3T - 58) = 342 ns min" to "(3T - 90) = 310 ns min";
    TPSR limit changed from "(2T + 24) = 291 ns min" to
    "(2T + 14) = 281 ns min".

11. Page 29, Section 4.1: TRWD limit changed from "(T + 112) =
    245 ns max" to "(2T + 4) = 270 ns max"; TSS limit changed
    from "20 ns min" to "0 ns min".

12. Page 30, Section 4.1: TWSP limit changed from "(3T - 85) =
    315 ns min" to "(3T - 110) = 290 ns min".

13. Page 31, Section 4.1, Notes: Note 11 was deleted; it said
    "When user aserts these signals, he is responsible for
    preventing TRI-STATE conflicts and for meeting any precharge
    times otherwise required by his own external circuits.

14. Page C-3, Comparison of T-11 to other processors in the
    PDP-11 Family: Activity 11A was added for the T-11 only.

      11A. When operating with the T-bit set (e.g. single
           stepping) no interrupt requests will be serviced.
           At the end of instruction execution, the T-bit
           has higher priority than interrupt requests.
           Once in the T-bit service routine, other interrupts
           are blocked to insure no unexpected occurances.
           When the RTT instruction is executed to leave
           the service routine, interrupts will not be
           serviced if the T-bit is set in the new PS
           popped off the stack. The user will, therefore,
           not see any interrupt requests he is expecting.

The following differences exist between Rev. D and Rev. E of the
T-11 Engineering Specification:

Item Number	Description of Change

1. Change TUPP limit to 100,000 ns min. Reference Bug Report 84. (Approved CCC Meeting of 1 April, 1981).

2. * Delete TASF from A.C. Characteristics. Change TASF to TASR on Refresh Timing Diagram. Reference Bug Report 125.

3. * Change limit on TSHF to 10 ns min. Reference Bug Report 134.

4. * Delete TAHF from A.C. Characteristics. Change TAHF to TAHR on Refresh Timing Diagram. Reference Bug Report 135.

5. Change "BUS, NOP" to "BUS NOP" on page 14.

6. Show TORT on READY Timing Diagram.

7. Delete the word TRI-STATE where it applies to the AI lines; rewrite text appropriately. Reference Bug Report 148.

8. Delete IFL from D.C. Characteristics list. Bug Report 150.

9. Change "TSDE" to "TDSE" on IACK diagram. Reference Bug Report 151.

10. Add TSSF to A.C. Characteristics list. Reference Bug Report 152.

11. Revise Power-Up Timing Diagram to include RESET timing. Reference Bug Reports 153, 163.

12. Change "TSFR" on Read/Write Timing Diagram to "TFFR". Change TFFR definition to "Refresh or Fetch on SEL0 (L.E.) Set Up Time to -RAS (L.E.)". Reference Bug Report 156.

13. Add list of pins to each D.C. Characteristic. Reference Bug Report 157.

14.   Redefine TKHR as TWHR and change definition of TWHR
            to "SAL<15:8>, Write Data, or IACK Information Hold
            Time from -RAS (T.E.)". Reference Bug Report 158.

15.   Change "READY (T.E.)" to "READY (L.E.)" in
            definitions for TYSC and TYSR. Reference
            Bug Report 159.

16.   Add TMHB to A.C. Characteristics List. Reference
            Bug Report 160.

17.   Change "TCMP" to "TCSP" on DMA Timing Diagram.
            Reference Bug Report 161.

18.   Add TDFB to A.C. Characteristics List. Change Note
            10 on page 31 (Rev. D page number) to "-BCLR may be
            used to gate mode input during RESET. TDFB may be
            violated on DAL<15:8,1:0> only. Violation of TDFB
            on DAL<7:2> may corrupt the processor." Reference
            Bug Report 162.

19.   Use new convention for showing active pullups on
            all timing diagrams where applicable. Reference
            Bug Report 164.

20.   Change VIHPUP limit to 2.2V min. Reference
            Bug Report 143.

21.   Change VILPUP limits to -0.5V to +0.6V.
            Bug Report 145.

22.   Change ICC limit to "190 mA, STATIC, TA = 0 C".
            Reference Bug Report 144.

23.   Change Absolute Maximum Power Rating to "1.1 Watt".
            Reference Bug Report 149.

24.   Change IIL limit to "-50 uA, VIN = 0.4V; +10 uA,
            VIN = VCCMAX". Reference Bug Report 130.

*   These changes approved at the CCC meeting of 12 NOV 81.
    Rev E. changes with no special notes were approved at the
    26 FEB 82 CCC Meeting.

T-11 ENGINEERING SPECIFICATION

Revision as of March 1, 1982

Rev E

TABLE OF CONTENTS

Rev B

1.0 T-11

1.1 SCOPE

This document specifies the functionality of MOS/LSI chip which is a one chip PDP-11. The descriptions herein assume readers are familiar with the PDP-11 instruction set and software architecture. For further information, the applicable documents should be consulted.

THIS SPECIFICATION IS SUBJECT TO CHANGE BECAUSE OF LOGIC AND LAYOUT CONSIDERATIONS.

ALL CONTENTS OF THIS DOCUMENT ARE COMPANY CONFIDENTIAL, AND DUE CAUTION SHOULD BE EXERCISED TO CONTROL EVEN INTERNAL DISSEMINATION.

1.2 Applicable Documents

For DEC documents, they are assumed to be applicable in general, but this document has precedence.

For other vendors documents, all attempts have been made for this document to be correct, but other vendors' specs must dominate.

    DEC's Microcomputer Processors 1978-1979 (Section 3, Chapters 9,
       10, & 12)
    DCT11-AA User's Guide
    MOSTEK's MK4027-2/3/4 Functional Specification
    MOSTEK's MK4116-2/3 Functional Specification
    INTEL's Component Data Catalog
    MOTOROLA's M6800 Microcomputer System Design Data Handbook
    MOTOROLA's 1.5 and 2.0 MHz Components for the M6800 Microcomputer
       System Data Sheet

1.3 T-11 Chip Description

The T-11 is a one chip PDP-11 intended to be internally competitive (cost and chip count) with the 8085 in bounded system applications. Its major features are the LSI-11 instruction set, an efficient 16-bit internal architecture and a bus which is compatible with TTL, memory chips, 8085 and 6800 peripheral chips, etc. A user-loadable mode register customizes T-11 to a variety of environments: for example, a mode is available which operates the 16-bit T-11 on an 8-bit data bus. Other special features of the T-11, many not found on other microprocessors, are listed in Section 1.4.

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The T-11 is a 16-bit microprocessor which connects easily to many LSI memory and 8-bit I/O chips. The 40 pins of T-11 do multiple duty. They are designed to require few support chips for simple systems, and to need only a few more chips for complex systems. The system designer may save cost when he needs to or may achieve high functionality at still modest costs. To accomplish this range of I/O adaptability, the T-11 accesses during power up an external MODE REGISTER and modifies its pin functions based on the state of the mode register bits.

For example, the simplest T-11 system might have limited memory and I/O. For this system, T-11 in STATIC, 8-BIT, DELAYED STROBE mode has: an address and data-transfer bus identical to the 8085; an internal oscillator amplifier needing only a crystal and two capacitors to clock the CPU; an input PUP, needing only a single capacitor to send the processor to the chosen startup address; an oscillator output, COUT, to drive a baud rate chip; and direct interrupt inputs, AI<7:6,4:1> which are internally prioritized, masked and vectored.

Addition of large ROMs to this system requires an MSI octal latch to demultiplex the low address bits <7:0>; -RAS may clock this latch.

Addition of more interrupting devices requires an MSI priority encoder to send a code, instead of bits, to AI<4:1>.

Addition of 6800-type devices to this system requires a different mode, NORMAL STROBE, for 6800-type Read/Write. An MSI or SSI chip then is needed to make the 8085-type signals -RD, -WT, using the T-11 -CAS signal.

Addition of large amounts of Read/Write memory implies low-cost-per-bit dynamic RAM chips. T-11 in DYNAMIC MODE accomplishes all of the address multiplexing and refreshing these memories need. The only additional support this mode requires is an MSI TRI-STATE buffer enabled by PI (to bring interrupt signals to AI<7:0> only when T-11 has freed those pins from their address multiplexing function).

Finally, the T-11 in 16-BIT MODE executes programs 60% faster than in 8-BIT MODE. It requires two MSI support chips, one to latch address bits <15:8> which are now multiplexed with data, and one to decode -RD, -WT strobes from the R/-WHB & R/-WLB pins.

In all cases, the T-11 runs PDP-11 software, if the system designer or programmer has provided new drivers or compatibility hardware for all 11-incompatible I/O devices.

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1.4 Special Features

Special features are:

- LSI-11 Instruction Set, less MARK
- Internal Clock Oscillator
- Automatic Power-on Initialization
- +5V only operation
- TTL level signals, designed for minimum support chip count
- Specially multiplexed addresses for direct connection to 16-pin dynamic RAM chips, with buried refresh
- Optional features set at power-up by information on data lines (MODE REGISTER).
    - 8 or 16 bit data bus
    - Start/Restart address
    - Static or 4K/16K/64K RAM chip address multiplexing
    - Bus-synchronous or constant frequency output clock
    - Normal or lenghthened bus cycle
- Internally generated interrupt vectors, with extra conditions possible by external expansion

Special PDP-11 differences are:

- Halt is an unmaskable interrupt (at restart address)
- Automatic Start sets stack pointer to 376, PSW to 340
- Internal interrupt vectors are dedicated to specific priorities
- No bus timeout
- Not I/O program compatible with standard DEC operating systems

Approximate speed benchmarks:

All times given in microseconds, unless otherwise noted.

	T-11/16	T-11/8	LSI-11/Q	11/34(MOS)
MOV R0,R1	1.6	2.4	4.3	1.96
ADD MEM1,MEM2	6.00	10.8	14.4	7.27
BEQ (taken)	1.6	2.4	4.3	2.31
AVERAGE BYTES per microsecond	1.5-1.7	1.0-1.1	0.7	

NOTE: T-11 benchmarks are calculated using Revision 5.18 microcode and static modes and are subject to change.

Rev B

2.0 FEATURES

2.1 Interrupt Structure

The T-11 inputs interrupt requests on the AI lines during the assertion of PI.

If -VEC is passive and any of the -CP<3:0> lines are active, and the implied priority of that set of asserted -CP<3:0> lines is not masked by the PSW, an interrupt will be taken using the vector address indicated below.

If -VEC is active and any set of -CP<3:0> lines are active and the implied priority of that set is not masked by the PSW, an interrupt will be taken using a vector address read in from DAL<7:2>.

-CP3	-CP2	-CP1	-CP0	Other	Implied Priority	Implied Vector Address	Other Action
X	X	X	X	-DMR	8	-	DAL<15:0> <-TRI-STATE> AI<7:0> <-LOW-CURRENT PULLUPS
X	X	X	X	-HLT	8	-	-(SP) <- PS -(SP) <- PC PS <- 340 PC <-START ADDRESS + 4
X	X	X	X	-PF	7	24	
L	L	L	L		7	140*	
L	L	L	H		7	144*	
L	L	H	L		7	150*	
L	L	H	H		7	154*	
L	H	L	L		6	100*	
L	H	L	H		6	104*	
L	H	H	L		6	110*	
L	H	H	H		6	114*	
H	L	L	L		5	120*	
H	L	L	H		5	124*	
H	L	H	L		5	130*	
H	L	H	H		5	134*	
H	H	L	L		4	60*	
H	H	L	H		4	64*	
H	H	H	L		4	70*	
H	H	H	H	NO ACTION			

*NOTE: if interrupt was accompanied by -VEC, Vector Address <7:2> is determined by DAL <7:2>.

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2.2 System Modes

The system is configured into specific operating modes at power-up and during a RESET instruction. This is accomplished by the T-11 automatically reading in specific bits of the DAL while it is asserting -BCLR. This -BCLR signal can be used to enable TRI-STATE drivers external to the T-11 that in turn will assert specific bits of the DAL to set the operating mode desired. (NOTE: Since low current pull-ups internal to the T-11 (DAL<15:8>,<2:0>) are enabled on the DAL inputs during -BCLR, only those bits that must be driven low need to be asserted.) The different modes are defined below. MR refers to the mode register that exists internally in the T-11. There is a one-to-one bit mapping of the MR bits and the DAL (i.e., DAL08=MR08, DAL09=MR09, etc.).

2.2.1 Mode Register Bit Designation

Summary:

```
 15  14  13  12  11  10   9   8   7   6   5   4   3   2   1   0
----------------------------------------------------------------
|   |   |   |   |   |   |   |   |   |      <-- RESERVED -->   |   |   |   |
----------------------------------------------------------------

  \                 /  |   |   |   |   |                              |   |
   Restart          |  |   |   |   | \ NORM                           | \ PMC
   Addresses        |  |   |   |   |                                  |
                    |  |   |   | \ DYNAMIC                          \ LMC
                    |  |   | \ MD64K
                    |  | \ MD16
                    | 
                     \ TESTER
```
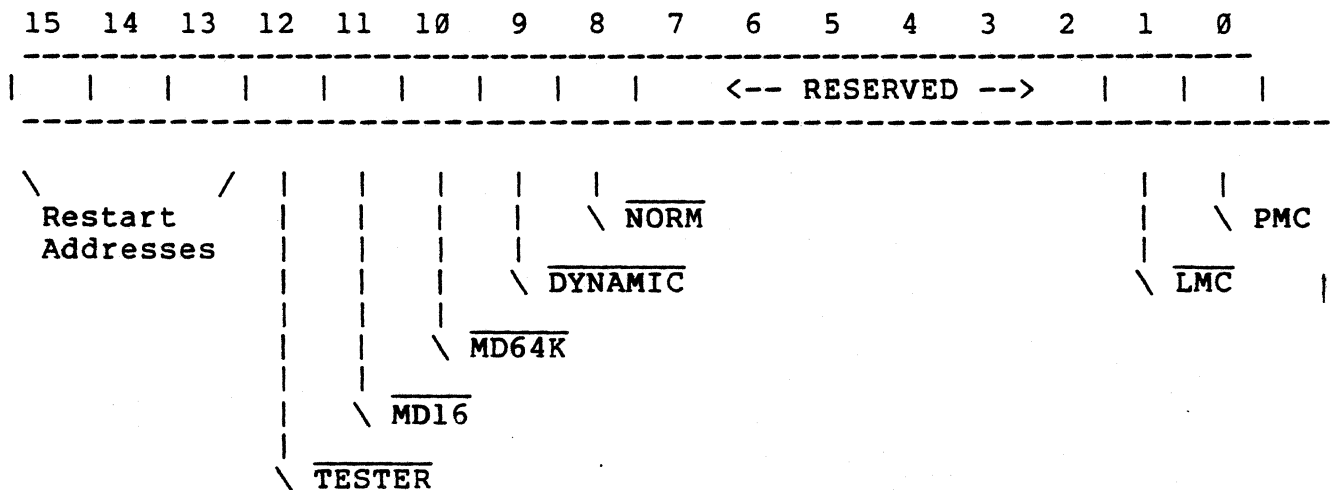
Mode register details will be described in detail in the following sections.

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2.2.2 Bus Modes

	MR11	MR10	MR9	MR8	Address Mode	Data Bus	
Static							
	H	H	H	H	STATIC	8 BITS	NOTE 1
	H	H	H	L	STATIC	8 BITS	NOTE 2
	L	H	H	H	STATIC	16 BITS	NOTE 3
	L	H	H	L	STATIC	16 BITS	NOTE 4
Dynamic							
	H	H	L	H	4/16K DYNAMIC	8 BITS	NOTE 1
	H	H	L	L	4/16K DYNAMIC	8 BITS	NOTE 2
	L	H	L	H	4/16K DYNAMIC	16 BITS	NOTE 3
	L	H	L	L	4/16K DYNAMIC	16 BITS	NOTE 4
	H	L	L	H	64K DYNAMIC	8 BITS	NOTE 1
	H	L	L	L	64K DYNAMIC	8 BITS	NOTE 2
	L	L	L	H	64K DYNAMIC	16 BITS	NOTE 3
	L	L	L	L	64K DYNAMIC	16 BITS	NOTE 4

NOTE 1:   Delayed -RD and -WT control signals. These signals
            become valid after the assertion of -RAS. This mode
            makes the T-11 bus a proper subset of the 8085 bus.

NOTE 2:   -RD and -WT control signals are stable before the leading
            edge of -RAS.

NOTE 3:   Delayed R/-WLB and R/-WHB control signals. These signals
            become valid after the assertion of -RAS.

NOTE 4:   R/-WLB and R/-WHB control signals are stable before the
            leading edge of -RAS.

MR11	=	$\overline{MD16}$
	H	8 bit data bus
	L	16 bit data bus

MR10	=	$\overline{MD64K}$
	H	4/16K dynamic memory support
	L	64K dynamic memory support

MR9	=	$\overline{DYNAMIC}$
	H	Static addressing
	L	Dynamic addressing

MR8	=	$\overline{NORM}$
	H	Delayed Read/Write control signals
	L	Normal Read/Write control signals

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2.2.3   Tester Mode

MR12 = $\overline{\text{TESTER}}$ (reserved for DEC testing use-not a user
                   feature)

H   Normal
L   A special cycle preceeds every instruction fetch.
        The cycle appears as a WRITE bus cycle. The address
        of the WRITE will be 0, PS<7:0>. In 8 bit modes the
        address of the write will be 0, PS<7:0>, for the low
        byte and 0, PS<7:0> with the low bit forced to a 1
        for the high byte. The Data of the WRITE will be the
        contents of the PDP-11 destination register of the
        last instruction.

2.2.4   Bus Length Mode

MR1 = $\overline{\text{LMC}}$ (Long Micro Cycle)

H   Normal Micro cycle
L   Long Micro cycle - Every microcycle is increased by one
                   phase (@7.5MHz = 133 ns). This can
                   provide synchronization of COUT to
                   the I/O cycles (if PMC mode = H).

2.2.5   Restart Modes

        The START Address is used at power-up.   The RESTART
Address is used for the hardware HALT interrupt and during the
execution of a PDP-11 HALT instruction.

MR15	MR14	MR13	RESTART Address	START Address
H	H	H	172004	172000
H	H	L	173004	173000
H	L	H	000004	000000
H	L	L	010004	010000
L	H	H	020004	020000
L	H	L	040004	040000
L	L	H	100004	100000
L	L	L	140004	140000

2.2.6   Clock Modes

MR0 = PMC (Processor Mode Clock)

H   Clock asserted once every microinstruction (3 or 4
        oscillator periods)
L   Clock out constant frequency (two oscillator periods)
                                                    Rev B

2.2.7 Signal Utilization for Each Bus Mode

Chip Pin Out Name	8 BIT Static	Dynamic* 4K/16K	64K	16 BIT Static	Dynamic* 4K/16K	64K	Dynamic All Modes
VCC	VCC	VCC	VCC	VCC	VCC	VCC	
GND	GND	GND	GND	GND	GND	GND	
BGND	BGND	BGND	BGND	BGND	BGND	BGND	
PUP	PUP	PUP	PUP	PUP	PUP	PUP	
XTL1	XTL1	XTL1	XTL1	XTL1	XTL1	XTL1	
XTL0	XTL0	XTL0	XTL0	XTL0	XTL0	XTL0	
COUT	COUT	COUT	COUT	COUT	COUT	COUT	
-BCLR	-BCLR	-BCLR	-BCLR	-BCLR	-BCLR	-BCLR	
-RAS	-RAS	-RAS	-RAS	-RAS	-RAS	-RAS	
-CAS	-CAS	-CAS	-CAS	-CAS	-CAS	-CAS	
PI	PI	PI	PI	PI	PI	PI	
R/-WHB	-RD	-RD	-RD	R/-WHB	R/-WHB	R/-WHB	
R/-WLB	-WT	-WT	-WT	R/-WLB	R/-WLB	R/-WLB	
SEL0	FET+DMG	REF+DMG	FET+DMG	FET+DMG	REF+DMG	FET+DMG	
SEL1	IAK+DMG	IAK+DMG	IAK+DMG	IAK+DMG	IAK+DMG	IAK+DMG	
READY	READY	READY	READY	READY	READY	READY	
DAL<15:13>	SAL<15:13> (0)	SAL<15:13> (0)	SAL<15:13> (0)	DAL<15:13> (0)	DAL<15:13> (0)	DAL<15:13> (0)	
DAL<12>	SAL<12> (-VEC)	SAL<12> (-VEC)	SAL<12> (-VEC)	DAL<12> (-VEC)	DAL<12> (-VEC)	DAL<12> (-VEC)	
DAL<11>	SAL<11> (-CP<0>)	SAL<11> (-CP<0>)	SAL<11> (-CP<0>)	DAL<11> (-CP<0>)	DAL<11> (-CP<0>)	DAL<11> (-CP<0>)	
DAL<10>	SAL<10> (-CP<1>)	SAL<10> (-CP<1>)	SAL<10> (-CP<1>)	DAL<10> (-CP<1>)	DAL<10> (-CP<1>)	DAL<10> (-CP<1>)	
DAL<9>	SAL<9> (-CP<2>)	SAL<9> (-CP<2>)	SAL<9> (-CP<2>)	DAL<9> (-CP<2>)	DAL<9> (-CP<2>)	DAL<9> (-CP<2>)	
DAL<8>	SAL<8> (-CP<3>)	SAL<8> (-CP<3>)	SAL<8> (-CP<3>)	DAL<8> (-CP<3>)	DAL<8> (-CP<3>)	DAL<8> (-CP<3>)	
DAL<7:2>	SAL<7:2> (VECTOR INPUT)	SAL<7:2> (VECTOR INPUT)	SAL<7:2> (VECTOR INPUT)	DAL<7:2> (VECTOR INPUT)	DAL<7:2> (VECTOR INPUT)	DAL<7:2> (VECTOR INPUT)	
AL<1:0>	SAL<1:0>	SAL<1:0>	SAL<1:0>	DAL<1:0>	DAL<1:0>	DAL<1:0>	
AI<0>	-DMR	FET:A14-DMR	A15:A14-DMR	-DMR	+FET:A14-DMR	A15:A14-DMR	-7 MSB
AI<1>	-CP3	A1:A2-CP3	A1:A2-CP3	-CP3	A1:A2-CP3	A1:A2-CP3	-0 LSB
AI<2>	-CP2	A3:A4-CP2	A3:A4-CP2	-CP2	A3:A4-CP2	A3:A4-CP2	-1
AI<3>	-CP1	A5:A6-CP1	A5:A6-CP1	-CP1	A5:A6-CP1	A5:A6-CP1	-2
AI<4>	-CP0	A7:A8-CP0	A7:A8-CP0	-CP0	A7:A8-CP0	A7:A8-CP0	-3
AI<5>	-VEC	A9:A10-VEC	A9:A10-VEC	-VEC	A9:A10-VEC	A9:A10-VEC	-4
AI<6>	-PF	A11:A0-PF	A11:A0-PF	-PF	A11:A12-PF	A11:A12-PF	-5
AI<7>	-HLT	A13:A12-HLT	A13:A12-HLT	-HLT	A13:A14-HLT	A13:A14-HLT	-6

NOTES

- means asserted low

A1:A2-CP0 means: Address bit 1 at -RAS leading edge,
Address bit 2 at -CAS leading edge,
-CP0 input during PI.

Names in ( ) are valid during IACK cycle

*In dynamic mode at refresh time the AI are the output of an 8 bit counter

+Fetch cycle if not doing a refresh cycle.

Rev E

2.3   External Signals

2.3.1 VCC

+5 volt supply (+/- 5%).

2.3.2 GND

Reference ground for most of chip

2.3.3 BGND

Second ground pin. It is recommended that BGND be connected to ground by a separate ground run from the GND pin.

2.3.4 PUP (Input)
Power Up

This schmitt-triggered input has a low-current internal pull-down that is always enabled. When PUP is high, the T-11 internal cycles are forced to an initial condition with undefined register states, with -BCLR asserted, and with low-current pullups on AI<7:0> and those DAL lines used for Mode Register inputs. When T-11 detects a low voltage on PUP, a power-up sequence begins, which:

        starts the internal clock
        loads the Mode Register for several microcycles from DAL;
        negates -BCLR (returns to high);
        performs (if Dynamic Mode) several refresh cycles;
        loads PC with Mode-selected Start Address;
        loads PSW with 340;
        loads SP with 376;
        checks DMR and HALT inputs (others masked by PSW) with an ASPI*
        begins normal operation.

Connecting a capacitor between PUP and VCC can give a simple powerup detector circuit.

*See note on ASPI under 2.3.14.

2.3.5 XTL1 (Input)
Crystal In/External Oscillator In

Crystal connection to the internal clock oscillator. With a crystal/ capacitor network connected to XTL1 and XTL0, T-11 implements a crystal oscillator to generate the operating clock. Alternatively, the user may ground XTL0, and apply an external operating clock (at TTL levels) to XTL1.

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2.3.6 XTL∅ (Output/Input)
Crystal Out

Crystal connection to the internal clock oscillator. This pin must be grounded if an external clock is to drive XTLI. See XTL1.

2.3.7 COUT (Output)
Clock Out

This pin outputs a TTL level clock that is a function of the operating clock and Mode Register bit ∅ (MR∅). If MR∅=1, then a clock is | asserted every 3 or 4 oscillator periods. If MR∅=∅, then a clock is asserted that is half the frequency of the operating clock frequency. A high level on PUP initializes MR∅=1.

2.3.8 -BCLR (Output)
Bus Clear

This signal is asserted low by the T-11 during power-up (see PUP) and also in execution of a PDP-11 RESET instruction. (Note: this pin must be connected to GND through a 1K ohm ± 1% metal film resistor at all times, to ensure correct T-11 operation.) An internal pull down in the T-11 will sink ∅.3 to 1.6 mA (see IILP section 3.2), thus -BCLR is a strobe which should enable user Mode pulldowns on DAL<15:8,2:∅>. The normal high output level will be lower on this pin than on any other pin. However, it will always be at least 3V. Mode bit input begins several microcycles after -BCLR is asserted and PUP is low, and continues until microcode returns -BCLR to a high.

2.3.9 -RAS (Output)
Row Address Strobe

The row address strobe used by dynamic memories. It can be used to latch the address on the DAL bus for ROMs, static RAMs and 8∅85 type peripheral chips. It can also be used to latch refresh information when the refresh output flag is selected.

This signal remains active (i.e., emulates I/O bus timing every two | machine cycles) when DMG (SEL<1:∅>=3) is asserted.

2.3.1∅ -CAS (Output)
Column Address Strobe

The column address strobe used by dynamic RAMs. -CAS can also be used as a critical signal for peripheral chips that need long address set-up times relative to the leading edge of the control signal (e.g., M68XX type parts), or long address and data hold times relative to the trailing edge of the control signal (e.g., 265∅ type parts). The leading edge can also be used to clock interrupt lines to insure theyare stable during PI.

Rev C

This signal remains active (i.e., emulates I/O bus timing every two machine cycles) when DMG (SEL<1:0>=3) is asserted.

2.3.11 PI (Output)
Priority In Strobe

This signal is asserted when the T-11 is executing an I/O cycle, has given up the bus for a DMA cycle, or is monitoring for interrupts. During a Write operation, the data on the DAL lines are stable when PI is asserted. Since the AI internal drivers are off whenever PI is asserted, PI can be used to gate -HALT, -PF, -VEC, -DMR and the -CP<3:0> signals onto the AI lines.

A -CAS signal always accompanies PI, thereby providing an early indication of the interrupt/DMA input operation.

2.3.12 R/-WHB (Output)

NOTE: Since the R/-WHB and -RD signals use the same pin, the signal enabled depends on whether 16-bit or 8-bit mode has been selected.

R/-WHB (16 bit mode)
Read/Write High Byte

In 16-bit modes this signal indicates whether the current I/O cycle is a read from or a write to the high byte of the location addressed. In normal control mode, R/-WHB is stable before the leading edge of -RAS. In delayed control mode, R/-WHB is issued by the T-11 after the assertion of -RAS.

-RD (8 bit mode)
Read

In 8-bit modes this signal indicates that the current I/O cycle is an eight bit read from the location addressed. In normal control mode, -RD is stable before the leading edge of -RAS. In delayed control mode, -RD is issued by the T-11 after the assertion of -RAS (this corresponds to the 8085 timing relationship between ALE and -RD). R/-WHB pin has an internal low-current pullup during DMG.

2.3.13 R/-WLB (Output)

NOTE: Since R/-WLB and -WT signals use the same pin, the signal enabled depends on whether 16-bit or 8-bit mode has been selected.

<div align="right">Rev C</div>

R/-WLB (16 bit mode)
Read/Write Low Byte

In 16-bit modes this signal indicates whether the current I/O cycle
is a read from or a write to the low byte of the location addressed.
In normal control mode, R/-WLB is stable before the leading edge of
-RAS.   In delayed control mode, R/-WLB is issued by the T-11 after
the assertion of -RAS.

  -WT (8 bit mode)
  Write

In 8-bit modes this signal indicates that the current I/O cycle is
an eight bit write to the location addressed.   In normal control
mode, -WT is stable before the leading edge of -RAS.   In delayed
control mode, -WT is issued by the T-11 after the assertion of -RAS
(this corresponds to the 8085 timing relationship between ALE and
-WT).   The R/-WLB pin has an internal low-current pullup during DMG. |

```
         ********************************************************
         *NOTE:   A DATA OUT Cycle to a location is*
         *preceeded by a DATA IN to the same location*
         *(except for stack operations).  A DMG can not be*
         *issued in the interval between DATA IN and DATA*
         *OUT.                                           *
         ********************************************************
```

2.3.14 SEL<1:0> (Output)
Select Output Flags

This signal pair is used to select special output functions.   The
functions are defined as follows:

SEL<1>	SEL<0>	FUNCTION
L	L	Read/Write or Bus NOP or ASPI
L	H	REFRESH**/FETCH*
H	L	IACK - Interrupt acknowledge***
H	H	DMG - Direct Memory Grant****

*See discussion of FETCH in AI section.
**Refresh in dynamic modes (except 64K), Fetch for static modes (plus
64K).
***See discussion of IACK under INTERRUPT in the AI section.
****See discussion of DMG under -DMR in the AI section.

The SEL<1:0> are stable before the leading edge of -RAS.   (NOTE: If
DMA is not implemented in the external hardware, SEL<1:0> may be used
as direct strobes.)

It is sufficient for a DMG decode to monitor for a SEL<1:0> = 3 decode
without using the leading edge of -RAS.
                                                            Rev C

REFRESH

In 8-bit dynamic mode, a refresh occurs after each instruction fetch and once with each source or destination mode 5, 6 or 7 operand fetch. Two additional refreshes occur during any trap sequence.

In 16-bit dynamic mode, refreshes happen at half the frequency of the 8-bit mode refreshes (i.e. every other opportunity, opportunities defined in 8 bit mode). This buried refresh scheme gives a worst case specification of 128 refreshes in 1.33 ms. @7.5MHz operating frequency. This allows 0.66 ms out of every 2 ms for DMA cycles and I/O transaction extensions (READY slips or LMC; long micro cycle mode). See APPENDIX D.

ASPI

An ASPI occurs to check for DMR and HALT inputs before the first instruction fetch and to check for interrupts as well as DMR and HALT during the WAIT instruction. During an ASPI only -CAS and PI are asserted (-RAS remains unasserted).

BUS NOP

A bus NOP occurs whenever the processor requires an internal operation and no other activity can occur on the bus (i.e. no READ/WRITE, REFRESH, ASPI, IACK, or DMG).

2.3.15 READY (Input)

This signal places the T-11 into an idle state waiting for the device that issued the READY to finish the I/O transaction. This signal allows memory or I/O devices of any speed to be synchronized to the T-11. READY slips can occur while -RAS is active except during Refresh cycles (i.e. DATA IN, DATA OUT, IACK, and during DMG). A single assertion of READY causes a single machine cycle slip.

READY must be pulsed in order to cause additional cycle slips. As a special case, an extra machine cycle (400ns min) of idle time can be guaranteed by simply gating -RAS with the external device's Chip Select signal onto the READY line. If the READY line is connected to GND, this single cycle slip will occur during every I/O or IACK cycle. READY is always internally connected to a low current pullup.

Rev E

2.3.16 DAL<15:8> (Input/Output TRI-STATE)
        Data and Address Lines
   SAL<15:8> (Input/Output TRI-STATE)
   Static Address Lines during 8 Bit Mode

Time multiplexed data and address bus. Addresses are stable before
the leading edge of -RAS. Input data should be available before the
trailing edge of -CAS. In 8-bit mode, the high byte of the address is
static throughout the I/O cycle.

During power-up or the execution of a RESET instruction the MODE
register bits are read in from these lines. Low current internal
pull-ups on DAL <15:8> are enabled when -BCLR is asserted.

During an interrupt cycle, the priority level of the interrupt is
output on DAL<12:8>. (DAL<12> = -VEC, DAL<11> = -CP<0>, DAL<10> =
-CP<1>, DAL<9> = -CP <2>, DAL <8> = -CP <3>.)

At all other times (i.e. ASPI, BUS NOP, REFRESH, byte not addressed
during Write/byte operation with ready slips) indeterminate data is|
output on DALs.

TRI-STATED when DMG (SEL<1:0>=3) is asserted.

2.3.17 DAL<7:0> (Input/Output)
        Data and Address Lines

Time multiplexed data and address bus. Addresses are stable before
the leading edge of -RAS. Input data should be available before the
trailing edge of -CAS.

During external vector IACK cycles (SEL<1:0>=2 and assertion of
-VEC), DAL<7:0> are tristated to read a vector address from DAL<7:2>
(NOTE: Data on DAL<1:0> is ignored). DAL<7:0> are tristated also
during internal vector IACK cycles.

During power-up or the execution of a RESET instruction the MODE
register bits are read in from these lines. Low current internal
pull-ups are enabled on DAL <2:0> when -BCLR is asserted.

At all other times (i.e. ASPI, BUS NOP, REFRESH, byte not addressed
during Write/byte operation with Ready Slips) indeterminate data is|
output on DALs.

TRI-STATED when DMG (SEL<1:0>=3) is asserted.

Rev E

2.3.18 AI<7:0> (Input/Output)
        Address and Interrupt

-ADDRESS (Output)
         (Dynamic Mode)

Dynamic RAM address bus and interrupt information bus.
In dynamic modes, row addresses are stable before the
leading edge of -RAS, column addresses before the
leading edge of -CAS and interrupt information is read
in during PI time. The addresses available at -RAS and
-CAS times duplicate the address on the DAL, and are in
a format controlled by the mode bits in the MODE
register. 4K, 16K and 64K dynamic RAMs can be
accommodated as well as the different address bit
mappings required for 8 or 16 bit data busses. In
static modes, these lines are always connected as
inputs.

During refresh in all dynamic modes, the refresh
address 8 bit counter is provided on the AI Lines. The
refresh counter is decremented after each refresh.

AI BIT	Refresh Counter Bit
0	7 MSB
1	0 LSB
2	1
3	2
4	3
5	4
6	5
7	6

In all modes, these pins provide internal low current
pullup when DMG (SEL<1:0>=3) is asserted.

INTERRUPT (Input)

-CP<3:0> (Input)
Coded Priority

During the assertion of PI (except during DATA OUT
transactions), T-11 reads these signals from AI<4:1>.
Logic internal to the T-11 decodes this input as
interrupt requests on 15 levels, maskable at 4 levels
(using PSW<7:5>; the highest requesting level, if not
masked, will be recognized and a PDP-11 trap sequence
executed. For CP interrupts only (both internal and
external), recognition of an interrupt is acknowledged
on the bus with an IACK cycle (where SEL<1:0>=2 and the
recognized input (-VEC, -CP<0:3> is asserted by T-11 on
DAL <12:8>).

                                                  Rev E

-VEC (Input)
Vector

During the assertion of PI (except during DATA OUT
transactions), T-11 reads this signal from AI<5>, but
it has meaning only if a CP request is also present on
AI.   -VEC can be used to increase the number of T-11
interrupts, because it signals the processor to ignore
the vector indicated by CP<3:0> and use instead the
vector to be provided by the user. During the IACK
cycle, in this case, the user-provided vector address
data is read by T-11 from DAL<7:2>.   -VEC is
acknowledged by T-11 asserting DAL <12> low during the
IACK cycle.

-PF (Input)
Power Fail Interrupt Request

During the assertion of PI (except during DATA OUT
transactions), T-11 reads this signal from AI<6>. -PF
is the highest priority interrupt on Level 7.   The
input circuit requires no data setup time because
internal logic samples -PF, then pauses for a time (up
to one instruction) before recognizing a request.
Also, a request must be read as negated once, before
another assertion will be recognized.   This set of
logic makes -PF appropriate for a power-fail interrupt,
especially since -PF results in an interrupt with the
PDP-11 powerfail vector (24_8).

Note: AN IACK cycle is <u>not</u> issued.

-HALT (Input)
Halt Interrupt Request

During the assertion of PI (except during DATA OUT
transactions), T-11 reads this signal from AI<7>. The
-Halt input circuit is pseudo-edge-sensitive, since the
signal must be read as a negation before an assertion
reading will have any effect.   -Halt is an unmaskable
interrupt.   It causes an immediate transfer (after
stacking PC, PSW), with PSW=340, to the RESTART address
(see Restart Modes).

Note: An IACK cycle is <u>not</u> issued

Rev B

-DMR (Input)
DMA Request

During the assertion of any PI, T-11 reads this signal from AI<0>. If the T-11 reads -DMR asserted, it will (upon termination of the current bus cycle except the DATA IN preceeding a DATA OUT) free the bus for DMA, signifying this state with SEL<1:0>=3. The T-11 TRI-STATES DAL<15:0> and places low-current pullups on AI<7:0> and the R/-WHB and R/-WLB pins. The T-11 remains somewhat in control of bus timing: -RAS, -CAS, and PI pulse; signalling of AI address changeover time is by the trailing edge of COUT (if COUT is in Pulse Mode);

- DMG remains asserted as long as the device keeps AI<0> asserted during PI.

FETCH (Output)

This signal is issued by the T-11 on AI<0> when in dynamic mode (except 64K), and by SEL<1:0>=1 in static mode or 64K mode. It signifies that the current I/O operation is an instruction fetch*. FETCH on AI<0> is valid before the leading edge of -RAS and stops driving before the leading edge of PI. When SEL<0> signifies fetch, it is asserted only during the read cycle (In 8 bit mode only during the low byte read cycle).

*CAUTION: During Refresh, the AI lines have the refresh counter address on them.

Rev E

2.3.19 Sample Signal Equivalency for Specific Manufacturer's Chip Families

Manuf.	Family	Applicable T-11 Modes (See Note 1)	Manufact. Family Signals	Equivalent T-11 Signals	Notes
MOSTEK	MK4027-3/4	4K DYNAMIC 8 or 16 BIT REFRESH ON	A<5:0>	AI<6:1>	
			-CS	AI<6>	2
			-RAS	-RAS	
			-CAS	-CAS	
			-WRITE	R/-W AND PI	3
				-WT AND PI	4
			DIN	DAL<n>	
			DOUT	DAL<n>	5
	MK4116-2/3	16K DYNAMIC 8 or 16 BIT REFRESH ON	A<6:0>	AI<7:1>	
			-RAS	-RAS	
			-CAS	-CAS	
			-WRITE	-R/W NAND PI	3
				-RD NAND PI	4
			DIN	DAL<n>	
			DOUT	DAL<n>	
INTEL	8085 (e.g., 8155, 8355, 8755)	STATIC DELAYED CONTROL 8-BIT	A<15:8>	SAL<15:8>	
			AD<7:0>	DAL<7:0>	
			ALE	-RAS	
			-RD	-RD	
			-WT	-WT	
			RESET	-BCLR	6
			IO/M		
			READY	-READY	7
	8080 (e.g., 8251, 8253, 8255, 8279)	STATIC DELAYED CONTROL 8-BIT	A<15:8>	SAL<15:8>	
			A<7:0>	DAL<7:0>	8
			D<7:0>	DAL<7:0>	
			-RD	-RD	9
			-WT	-WT	9
			RESET	-BCLR	6
			WAIT	READY	7,10
MOTOROLA	68X00 (e.g., 68X21, 68X50)	STATIC NORMAL CONTROL 8-BIT	A<15:8>	SAL<15:8>	
			A<7:0>	DAL<7:0>	8
			D<7:0>	DAL<7:0>	
			ENABLE	-CAS	9
			R/W	-WT	
			-RESET	-BCLR	

Rev D

NOTES:

1. The applicable mode listed for each particular family is only meant to be a guideline for minimum hardware systems. It does not mean to imply that chips from a particular family can only be used in the mode listed for it. For example, 8080, 8085 or 68X00 peripheral chips can be used in any of the dynamic modes with an overhead of only a few extra gates.

2. AI<6> can be used as Chip Select only if there are less than 2 banks of 4K RAM in the system. In systems with more than 2 banks, the user will have to use decoding logic to generate the Chip Select signals. Also AI<6> must be gated with the REFRESH signal to properly refresh the MK4027s.

3. To synthesize the -WRITE signal in 16-bit mode, the user must logically NAND the two T-11 signals: PI and an inverted R/-WLB (and/or R/-WHB depending on which byte(s) are being written).

4. To synthesize the -WRITE signal in 8-bit mode, the user must logically NAND the two T-11 signals: PI and -RD.

5. Since the MK4027-3/4 has latched outputs, the user must use TRI-STATE buffers in interfacing these RAM outputs to the T-11 Data Bus.

6. An inverter must be used on the T-11 output to make these signals logically equivalent.

7. The 808X signal is level sensitive and causes the 808X to slip clock cycles. The T-11 signal is edge sensitive and causes the T-11 to slip machine cycles.

8. An address low byte that is stable throughout the I/O cycle is generated by using a transparent octal latch which is clocked by the assertion of -RAS.

9. To insure timing compatibility for some of the chips in this family, the length of time this T-11 signal is asserted must be increased by either asserting the -READY line or by operating the T-11 at a slower frequency.

10. When asserted, this signal must be inverted to be an active input into the T-11.

2.4   Pinout

```
              DAL15 <--->|  1              40  |<---- VCC
              DAL14 <--->|  2              39  |<---> AI7
              DAL13 <--->|  3              38  |<---> AI6
              DAL12 <--->|  4              37  |<---> AI5
              DAL11 <--->|  5              36  |<---> AI4
              DAL10 <--->|  6              35  |<---> AI3
               DAL9 <--->|  7              34  |<---> AI2
               BGND ---->|  8              33  |<---> AI1
               DAL8 <--->|  9              32  |<---> AI0
               DAL7 <--->| 10    T-11      31  |----> PI
               DAL6 <--->| 11    CHIP      30  |----> -CAS
               DAL5 <--->| 12              29  |----> -RAS
               DAL4 <--->| 13              28  |----> R/-WLB
               DAL3 <--->| 14              27  |----> R/-WHB
               DAL2 <--->| 15              26  |<---- READY
               DAL1 <--->| 16              25  |----> SEL0
               DAL0 <--->| 17              24  |----> SEL1
              -BCLR <----| 18              23  |<---> XTL0
                PUP ---->| 19              22  |<---- XTL1
                GND ---->| 20              21  |----> COUT
```

Rev B

2.5 T-11 Block Diagram

INSERT DIAGRAM

T-11 BLOCK DIAGRAM
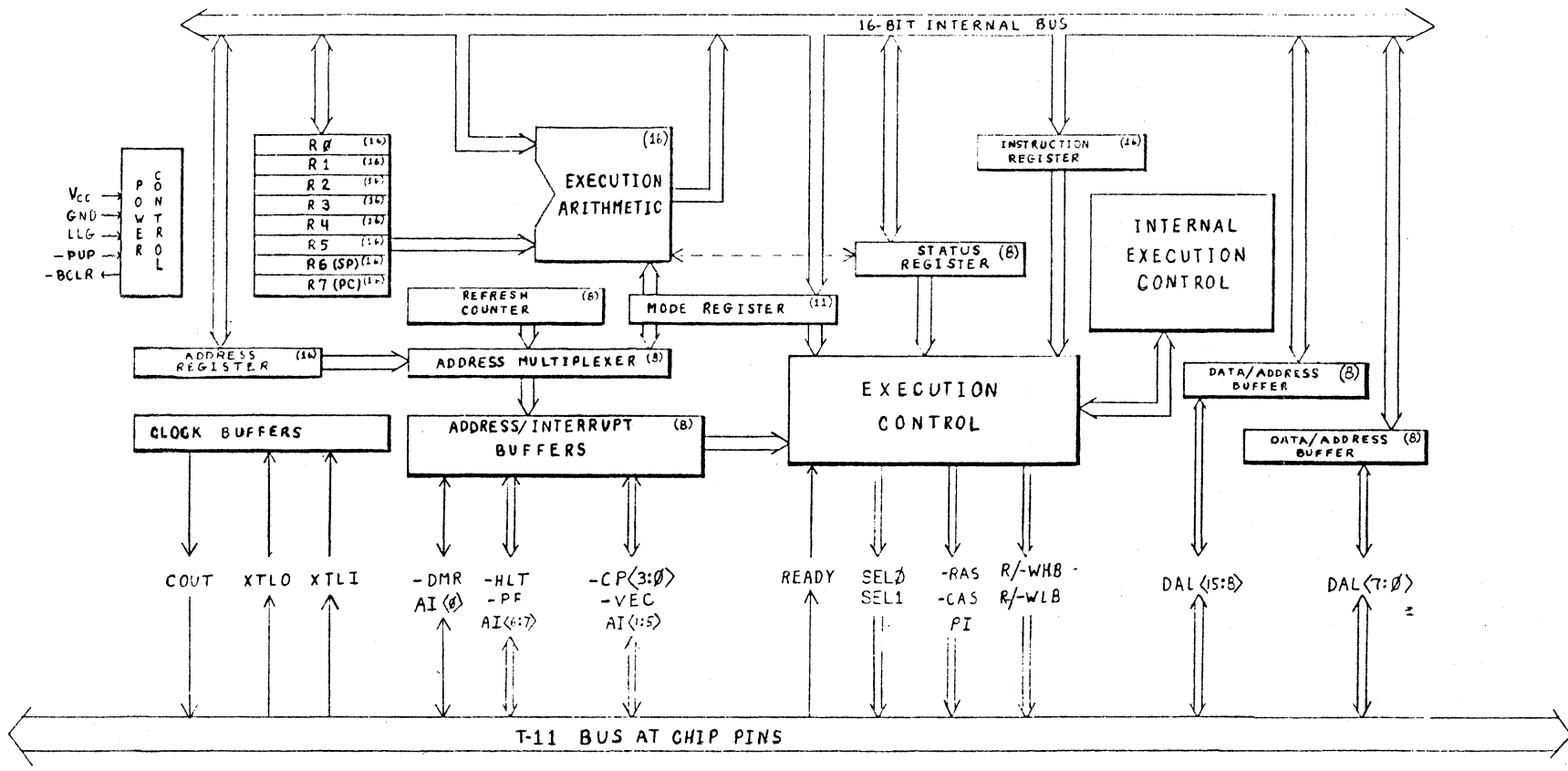
5-AUG-80

digital

2.6   Instruction Set

SOP		DOP	PC MOD		MISC
CLR(B)	ROR(B)	MOV(B)	B(XX)	EMT	S(CC)
COM(B)	ROL(B)	CMP(B)	SOB	TRAP	C(CC)
INC(B)	ASR(B)	BIT(B)	JMP	BPT	HALT
DEC(B)	ASL(B)	BIC(B)	JSR	IOT	WAIT
NEG(B)	SWAB	BIS(B)	RTS		RESET
ADC(B)	SXT	ADD	RTI		NOP
SBC(B)	MTPS	SUB	RTT		MFPT*
TST(B)	MFPS	XOR			

Addressing Modes

Mode	Name
0	REGISTER
1	REGISTER DEFERRED
2	AUTO-INCREMENT
3	AUTO-INCREMENT DEFERRED
4	AUTO-DECREMENT
5	AUTO-DECREMENT DEFERRED
6	INDEX
7	INDEX DEFERRED

*Note: T-11 processor code is 4.

Rev A

3.0   D.C. CHARACTERISTICS

3.1   Absolute Maximum Ratings

Pin voltages	-0.5 to +7V
Operating Junction Temperature Range	0 to 100 degrees C
Storage Temperature Range	-55 to +125 degrees C
Power Dissipation	1.1 watt
Chip Ambient Temperature Operating Range	0 to 70 degrees C

Notes: Stress greater than those listed may cause permanent damage to the device. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability. Currents sourced by the DC310 are indicated by a negative prefix to the value listed.

3.2   Static Characteristics

(TA = 0 C to 70 C, VCC = 5.0V +/- 5%, VSS = 0V)

Symbol	Parameter/Pins	Min	Max	Units	Comments & Conditions
IIL	(Low Input) Tri-State Leakage Current on DAL<0:15>		-50	uA	VIN = 0.4V
IIL	(High Input) Tri-State Leakage Current on DAL<0:15>		+10	uA	VIN = VCCMAX
IIH	(MIN) Input Current for Internal Pullups on AI<0:7>, DAL<0:2,7:15>, READY	-0.1		mA	VIN = 0.4V
IIH	(MAX) Input Current for Internal Pullups on AI<0:7>,DAL<0.2,7:15> READY		-0.1	mA	VIN = 0.4V
IXLIH	Input High Current on XTAL1		+700	uA	2.4<VIN<VCC, X T A L 0 Grounded
IXLIL	Input Low Current on ITAL1		-6.4	mA	-0.5V<VIN<+0.6\ XTAL0 Grounded

Rev E

Symbol	Parameter/Pins	Min	Max	Units	Conditions
ICC	Power Supply Current on VCC		190	mA	Static, TA = 0 C
VIH	Input High Voltage on READY, DAL,0:15>, AI<0:7>	2.0	VCC	V	
VIHPUP	Input High Voltage on PUP	2.2	VCC	V	
VIL	Input Low Voltage on READY, DAL<0:15>, AI<0.7>	-0.5	+0.8	V	
VILPUP	Input Low Voltage on PUP	-0.5*	+0.6	V	
VOH	Output High Voltage for DAL<0:15>, COUT, PI, SEL1, SEL0	2.4		V	IOH = -700 uA
VOHA	Output High Voltage for AI<0:7>	2.6		V	IOH = -700 uA
VOHB	Output High Voltage for BCLR	2.2		V	IOH = -700 uA, Terminated to VSS (Ground) with 1 K percision Resistor of 1% accuracy.
VOHC	Output High Voltage for -RAS,_CAS,R/-WLB, R/-WHB	2.8		V	IOH = -700 uA
VOL	Output Low Voltage for DAL<0:15>, AI<0:7>, COUT, PI, SEL1, SEL0 BCLR, RAS, CAS, R/-WHB, R/-WLB	0.0	0.4	V	IOL = 3.2 mA
CIN	Input Capacitance for READY, DAL<0:15>, AI<0:7>		10	pF	
COUT	Output Capacitance for Tri-State Load Calculation on DAL<0:15>, AI<0:7>,COUT,PI,SEL1,SEL0, BCLR,RAS,CAS,,R/-WHB,R/-WLB		20	pF	

* -0.5V on input pins allows for ringing on unterminated lines

Rev E

4.0 A. C. CHARACTERISTICS

4.1 Bus Timing Annotated for Maximum XTL1, XTL0 Operating Frequency

$(TJ = 0$ to $100^{\circ}C$, VCC = 5.0V +/-5% VSS = 0.0V)

Symbol	Parameter	Function of tCYC	Comments & Conditions
fOP	XTL1, XTL0 Operating Frequency	7.5 MHz 0.1 MHz	max min (11)
tAFP	Column Address on AI<7:0> Float to PI (L.E.)	0 ns	min
tAFS	AI<7:0> Float to DMA Select on SEL<0>	0 ns	min
tAHC	Column Address on AI<7:0> Hold Time from -CAS (L.E.)	T - 43 = 90 ns	min
tAHR	Row Address on AI<7:0> Hold Time from -RAS (L.E.)	T - 60 = 73 ns	min
tASC	Column Address on AI<7:0> Set Up Time to -CAS (L.E.)	20 ns	min
tASR	Row Address on AI<7:0> Set Up Time to -RAS (L.E.)	T - 83 = 50 ns	min
tBCR	T-11 -BCLR Pulse Width on a Reset instruction	(84T) ns	min
tBMR	-BCLR Set Up Time to Mode Bits on DAL<15.0> Valid Following a RESET Instruction	(74T) ns	max
tCAS	-CAS Pulse Width	(3T - 90) = 310 ns	min (4)
tCDE	-CAS (T.E.) or Delayed Mode R/$\overline{W}$ (T.E.) to next DAL <15:0> Address Enable	T - 18 = 115 ns	min
tCPR	-CAS Precharge Time	(3T - 5) = 395 ns	min
tCRD	-CAS (L.E.) or Delayed Mode R/$\overline{W}$ (L.E.) to Read Data Valid	(3T - 180) = 220 ns	max (4) Rev E

tCSP	-CAS (L.E.) or Delayed Mode R/$\overline{W}$ (L.E.) Set Up Time to PI (L.E.)	(T - 28) = 105 ns	min
tCSR	-CAS (L.E.) Set Up Time to -RAS (T.E.)	(3T - 40) = 360 ns	min (4)
tCWD	-CAS (L.E.) or Delayed Mode R/$\overline{W}$ (L.E.) to Write Data Valid	80 ns	max
tCYC	XTL1, XTL0 Operating Period	T = 133 ns	min
tDFB	DAL<15:0>Float from -BCLR (L.E.)	150 ns	max (10)
tDFC	DAL<15:0> Address Float to -CAS (L.E.) or Delayed Mode R/$\overline{W}$ (L.E.)	0 ns	min
tDFS	DAL<15:0> Float to DMA Select on SEL<0> (L.E.)	0 ns	min
tDHN	DAL<15:0> Address Hold Time from Normal Mode Control Strobe (L.E.)	(2T - 20) = 247 ns	min
tDHR	DAL<15:0> Address Hold Time from -RAS (L.E.)	(T - 12) = 121 ns	min
tDRD	DAL<15:0> Address Set Up Time to Read Data Valid	(5T - 157) = 510 ns	max (4)
tDSC	DAL<15:0> Address Set Up Time to -CAS (L.E.) or Delayed Mode R/$\overline{W}$ (L.E.)	(2T - 22) = 245 ns	min
tDSE	DAL<15:0> Enable from DMA Select on SEL<1> (T.E.)	(T - 27) = 106 ns	min
tDSP	DAL<15:0> Address Set Up Time to PI (L.E.)	(3T - 20) = 380 ns	min
tDSR	DAL<15:0> Address or DAL<15:8> IACK information Set Up Time to -RAS (L.E.)	(T - 48) = 85 ns	
tFFR	Refresh or Fetch on SEL0(L.E.), Set Up Time to -RAS(L.E.)	(T - 23) = 110 ns	min
tFRP	Refresh -RAS Pulse Width	(2T + 35) = 302 ns	min
tFSP	Refresh Select on SEL<0> Pulse Width	(4T - 20) = 513 ns	min

Rev E

tIHP	Interrupt or DMA Input on AI<7:0> Hold Time from PI (T.E.)		0 ns	min
tISP	PI (L.E.) to Interrupt or DMA Input on AI<7:0> Valid	$(2T - 167) = 100$ ns		max (4)
tKDS	Vector Data on DAL<7:2> Hold Time from IACK Select on SEL<1> (T.E.)		0 ns	min
tKHS	IACK Information on DAL<15:8> Hold Time from IACK Select on SEL<1> (T.E.)	$(T - 50) = 83$ ns		min
tKKR	IACK on SEL1 (L.E.) Set Up Time to -RAS (L.E.)	$(T - 63) = 70$ ns		min
tKRD	IACK -RAS (L.E.) to Vector Data on DAL<7:0> Valid	$(2T - 148) = 119$ ns		max (4)
tKRP	IACK -RAS Pulse Width	$(2T + 35) = 302$ ns		min (4)
tKSD	IACK Select on SEL<1> (L.E.) to Vector Data on DAL<7:2> Valid	$(3T - 155) = 245$ ns		max (4)
tKSP	IACK Select on SEL<1> Pulse Width	$(3T - 66) = 334$ ns		min (4)
tLPO	DMA or Long Micro Cycle PI (L.E.) Set up time to Constant Mode COUT (T.E.)	$(T - 84) = 49$ ns		min
tMHB	Mode Input on DAL<15:0> Hold Time From -BCLR (T.E.)		0 ns	min
tMOC	ASPI or DMA Pulse Mode COUT (T.E.) Set up Time to -CAS (L.E.)	$(T + 10) = 143$ ns		min
tMOR	Read/Write or DMA Pulse Mode COUT (L.E.) Set Up Time to -RAS (L.E.)		0 ns	min
tMPO	DMA or Long Micro Cycle PI (L.E.) Set Up Time to Pulse Mode COUT (L.E.)	$(2T - 84) = 183$ ns		min
tMRC	DMA Select -RAS (L.E.) Set Up Time to -CAS (L.E.)	$(2T + 10) = 277$ ns		min
tMRO	Read/Write or DMA Pulse Mode COUT (T.E.) Hold Time from -RAS (L.E.)	$(T - 51) = 82$ ns		min

Rev E

tMRP	DMA Select -RAS Pulse Width	$(5T + 35) = 702$ ns	min (8)
tMSF	DMA Select on SEL<0> Pulse Width	$(8T - 38) = 1029$ ns	min(8)(9)
tMSK	DMA Select on SEL<1> Pulse Width	$(7T - 68) = 865$ ns	min(8)(9)
tNHC	Normal Mode R/$\overline{W}$ Hold Time from -CAS (T.E.)	$(T - 32) = 101$ ns	min
tNHP	Normal Mode R/$\overline{W}$ Hold Time from PI (T.E.)	$(T - 43) = 90$ ns	min
tNHR	Normal Mode R/$\overline{W}$ Hold Time from -RAS (T.E.)	$(T - 108) = 25$ ns	min
tNMP	Normal Mode R/$\overline{W}$ Pulse Width	$(6T - 66) = 734$ ns	min (4)
tNMR	Normal Mode R/$\overline{W}$ Recovery Time	0 ns	min
tNRD	Normal Mode -RD Strobe Set Up Time to Read Data Valid	$(5T - 148) = 519$ ns	max (4)
tNSC	Normal Mode R/$\overline{W}$ Set Up Time to -CAS (L.E.)	$(2T - 37) = 230$ ns	min
tNSP	Normal Mode R/$\overline{W}$ Set Up Time to PI (L.E.)	$(3T - 45) = 355$ ns	min
tNSR	Normal Mode R/$\overline{W}$ Set Up Time to -RAS (L.E.)	$(T - 78) = 55$ ns	min
tOPW	Pulse Mode COUT Pulse Width	$(T - 33) = 100$ ns	min
tORD	Pulse Mode COUT Recovery Time when 0D Present	$(3T - 37) = 367$ ns	min
tORT	Pulse Mode COUT Recovery Time	$(2T - 37) = 230$ ns	min
tOSC	Pulse Mode COUT (T.E.) Set Up Time to -CAS (L.E.)	10 ns	min
tPAE	PI (T.E.) to next AI<7:0> Address Enable	$(T - 40) = 93$ ns	min
tPBC	T-11 Power Up to -BCLR (L.E.) Set Up Time	100 ns	max
tPBU	Power Up (T.E.) to -BCLR (T.E.)	$99T = 13200$ ns	min
		$100T = 13333$ ns	max

Rev E

tPCO	Power Up (T.E.) to COUT (L.E.)	T + 60 ns = 193 ns	max
tPFF	Power Up (T.E.) to Beginning of First Instruction Fetch	295T = 39333 ns 315T = 42000 ns	min max
tPHC	PI Hold Time from -CAS (T.E.) or Delayed Mode R/$\overline{W}$ (T.E.)	10 ns	min
tPIP	PI Pulse Width	(2T - 47) = 220 ns	min (4)	
tPMU	Power Up (T.E.) to Mode bits on DAL<15:0> valid	74T	max
tPPR	PI Precharge Time	(4T - 33) = 500 ns	min
tPRD	PI (L.E.) to Read Data Valid	(2T - 176) = 91 ns	max (4)
tPSC	PI (L.E.) Set Up Time to -CAS (T.E.) or Delayed Mode R/$\overline{W}$ (T.E.)	(2T - 75) = 192 ns	min (4)
tPSN	PI (L.E.) Set Up Time to Normal Mode Control Strobe (T.E.)	(3T - 90) = 310 ns	min (4)	
tPSR	PI (L.E.) Set Up Time to -RAS (T.E.)	(2T + 14) = 281 ns	min (4)	
tPUT	Power Up (L.E.) to Output Pins Preset	250 ns	max
tRAS	-RAS Pulse Width	(4T + 35) = 568 ns	min (4)
tRDC	Read Data Hold Time from -CAS (T.E.) or Delayed Mode R/$\overline{W}$ (T.E.)	0 ns	min
tRDE	-RAS (T.E.) to next DAL<15:0> Address Enable	(T - 118) = 15 ns	min
tRHC	-RAS (T.E.) Hold Time from -CAS (T.E.) or Delayed Mode R/$\overline{W}$ (T.E.)	50 ns	min
tRHP	-RAS (T.E.) Hold Time from PI (T.E.)	10 ns	min
tRHS	-RAS (T.E.) Hold Time from IACK or DMA Select on SEL<1> (T.E.)	45 ns	min
tRPR	-RAS Precharge Time	(2T - 120) = 147 ns	min

Rev E

tRRD	-RAS (L.E.) to Read Data Valid	(4T - 128) = 405 ns	max	(4)
tRSC	-RAS (L.E.) Set Up Time to -CAS (L.E.) or Delayed Mode R/$\overline{W}$ (L.E.)	(T + 10) = 143 ns	min	
tRSD	R/$\overline{W}$ Drivers disabled and Passive Pull Up Enabled Set Up Time to DMA Select on SEL<0> (L.E.)	0 ns	min	
tRSE	R/$\overline{W}$ Driver Enabled from DMA Select on SEL<1> (T.E.)	(T - 27) = 106 ns	min	
tRSP	-RAS (L.E.) Set Up Time to PI (L.E.)	(2T + 10) = 277 ns	min	
tRWD	-RAS (L.E.) to Write Data Valid	(2T + 4) = 270 ns	max	|
tSFR	DMA on SEL<0> (L.E.) Set Up Time to -RAS (L.E.)*	(2T - 23) = 243 ns	min	
tSHF	Refresh or DMA Select on SEL<0> (T.E.) Hold Time from -RAS (T.E.)	(T -123) = 10 ns	min	
tSKR	DMA Select on SEL<1> (L.E.) Set Up Time to -RAS (L.E.)	(2T - 63) = 203 ns	min	
tSPR	IACK or DMA Select on SEL<1> Recovery Time	(T) = 133 ns	min	
tSSF	Pulse Width on SEL<0> During Fetch	(3T - 38) = 362 ns	min	| |
tSSS	SEL<0> (L.E.) Set Up Time to SEL<1> (L.E.)	0 ns	min	|
tUPP	T-11 Power Up Time	100,000 ns	min	|
tWDP	Write Data Set Up Time to PI (L.E.)	(T - 83) = 50 ns	min	
tWHC	Write Data or SAL<15:8> Hold Time from -CAS (T.E.) or Delayed Mode R/$\overline{W}$ (T.E.)	(T - 28) = 105 ns	min	
tWHP	Write Data Hold Time from PI (T.E.)	(T - 88) = 45 ns	min	
tWHR	SAL<15:8>, Write Data, or IACK Information Hold Time from -RAS (T.E.)	(T - 118) = 15 ns	min	|

*On R/W SEL0 set up time to RAS is T-23

Rev E

tWSC	Write Data Set Up Time to -CAS (T.E.)	(3T - 150) = 250 ns	min	(4)
tWSP	Write Data Set Up Time to PI (T.E.)	(3T - 110) = 290 ns	min	(4)
tWSR	Write Data Set Up Time to -RAS (T.E.)	(3T - 55) = 345 ns	min	(4)
tYHC	READY (L.E.) Hold Time from COUT (T.E.)	0 ns	min	(6)
tYPW	READY Pulse Width	60 ns	min	(5)
tYRT	READY Recovery Time	60 ns	min	(6)
tYSC	READY (L.E.) Delay from -CAS (L.E.)	(2T - 135) = 132 ns	max	(5)
tYSO	READY (L.E.) Delay from Pulsed Mode COUT (T.E.)	(2T - 127) = 140 ns	max	(5)
tYSR	READY (L.E.) Delay from -RAS (L.E.)	(3T - 100) = 300 ns	max	(5)

NOTES:

1. Timings are measured at the following output voltages:
    -RAS, -CAS, R/-WLB
    & R/-WHB   VOL = 0.8V   VOH = 2.4V
    AI<7:0>   VOL = 0.8V   VOH = 2.2V
    All others   VOL = 0.8V   VOH = 2.0V
    Noise Hazard Timing:
    $$t(0.8V - 0.4V) = 12 \text{ ns max}$$
    $$t(2.0V - 2.4V) = 10 \text{ ns max}$$
    $$t(2.2V - 2.6V) = 11 \text{ ns max}$$
    $$t(2.4V - 2.8V) = 12 \text{ ns max}$$

2. Output timings are measured using a purely capacative load of 80 pf. For loadings other than 80 pf use the following correction factors:
    80pf < CL < 200 pf   +0.3 ns/pf
    25pf < CL < 80 pf   -0.3 ns/pf

3. T = 1/fop
    L.E. => Leading Edge
    T.E. => Trailing Edge

4. Add T ns if in long bus cycle mode, then if RDY slips are initiated, add H*T ns, where:
    T = 1/fop, H = number of RDY pulses times 3 if mode = normal, times 4 if mode = long bus cycle.

Rev E

5. READY is an edge-triggered input that is usually activated by asserting a low on its pin. However, READY is internally activated by the leading edge of -RAS if its pin has been asserted low before these edges.

6. These timing parameters apply only to cases where multiple READY pulses are required, i.e. multiple microcycle slips.

7. Asserting PUP high will leave all registers, including the PDP-11 General Purpose Registers (R0 thru R7) in an indeterminate state except for Mode Reg <1> force to normal | micro cycle.

8. Add 4T for each Ready pulse.

9. Add 8T if multiple DMA cycles are granted.

10. -BCLR may be used to gate mode input during RESET. TDFB may be violated on DAL<15:8,1:0> only.

11. If external TTL clock is used, t_{CYC} min is 0Hz (i.e. DC) since the T-11 is a static part.

Rev E

4.2 Crystal Specification

Symbol	Parameter	Min	Max	Units	Conditions
FREQ	Frequency	0.1	7.5	MHz	+/-0.01%
					0 to 70°C
	Mode				Fundamental
	Spurious Mode				To Be Determined
Rs	Series Resistance				To Be Determined
Cp	Parallel Capacitance				To Be Determined

Rev E

4.3   <u>Timing Diagrams</u>

INSERT TIMING DIAGRAMS

PAGE TITLE	REVISION
T-11 BLOCK DIAGRAM	2
T-11 REFRESH, IACK TIMING	6
T-11 ASPI CYCLE (ASSERT PRIORITY IN)	1
T-11 BUS NOP (NO TRANSACTION ON BUS)	1
T-11 DMA TIMING	4
T-11 READY TIMING	3
T-11 POWER-UP/ RESET TIMING	1
T-11 LONG MICRO CYCLE MODE	2
T-11 READ/WRITE TIMING	6

NOTE: THE FOLLOWING CONVENTION DENOTES INTERNAL PULLUPS ON.
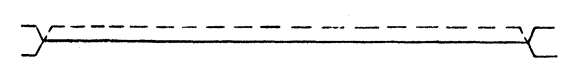
1-MAR-82

DRN.	FIRST USED ON
CHK'D	
ENG.	TITLE: T-11 TIMING DIAGRAMS
PROJ. ENG.	INDEX AND REVISIONS
PROD.	
NEXT HIGHER ASSY.	
SCALE	SIZE D CODE NUMBER REV. 2
SHEET 1 OF 1	DIST.

digital

T-11 REFRESH CYCLE

* WHEN IN 64K DYNAMIC MODE-SEL $\emptyset$ NOT ASSERTED DURING REFRESH CYCLE.

NOTE: AI'S CHANGE BEFORE -RAS TRAILING EDGE.   NOTE1: 64K REFRESH 16 BIT.
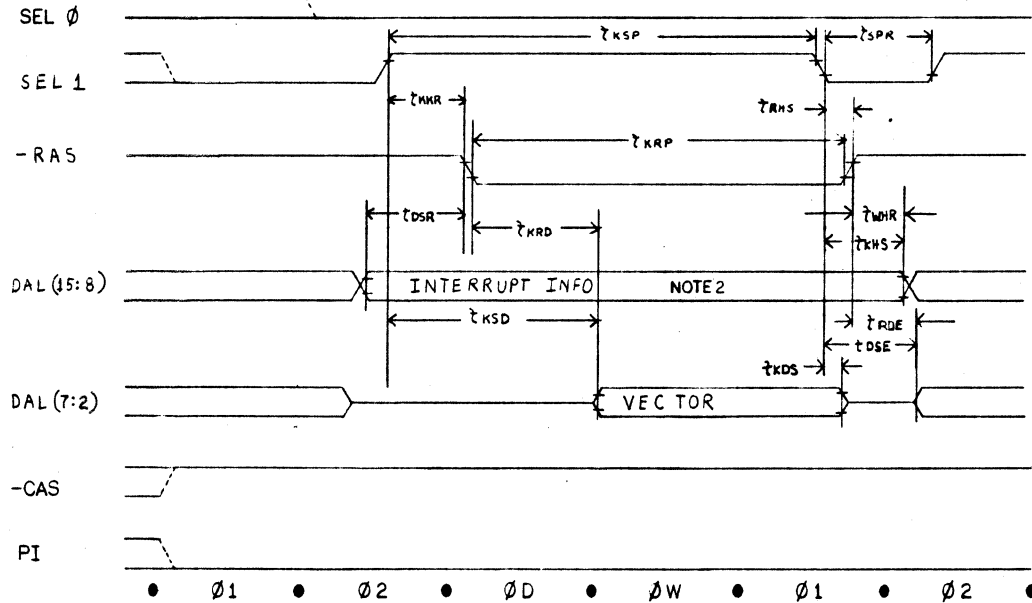
T-11 IACK CYCLE

NOTE: DAL(12:8) REFLECT -VEC,-CP(3:$\emptyset$) BEING ACKNOWLEDGED.

1 MAR 82

DRN. P. J F
CHK'D
ENG.
PROJ. ENG. REO
PROD.
NEXT HIGHER ASSY.

FIRST USED ON

digital

TITLE   T-11
REFRESH, IACK
TIMING

SIZE **D** CODE   NUMBER   REV. **6**

SCALE
SHEET 2 OF 1   DIST.

NOTE: ASPI CYCLES OCCUR BEFORE FIRST FETCH, DURING WAIT INSTRUCTIONS, AND AFTER RESET INSTRUCTIONS.

NOTE1: PULSE MODE CLOCK.

NOTE2: ASSERTED IN 8 BIT MODE, TRISTATED IN 16 BIT MODE.

NOTE3: UNDEFINED.

5-AUG-80

TITLE T-11 ASPI CYCLE
(ASSERT PRIORITY IN)

Ø1   •   Ø2   •   ØW   •   Ø1   •   Ø2   •   ØW   •

DAL(15:Ø) — INDETERMINATE

AI(7:Ø) — NOTE 1

−RAS

−CAS

PI

R/$\overline{WHB}$
R/$\overline{WLB}$

SELØ

SEL1

COUT — NOTE 2

NOTE 1: ASSERTED ONLY IN DYNAMIC MODES, DRIVING INDETERMINATE DATA.
NOTE 2: PULSE MODE CLOCK.

5-AUG-80

digital

DRN.	FIRST USED ON
CHK'D	
ENG.	TITLE T-11 BUS NOP
PROJ. ENG.	(NO TRANSACTION ON BUS)
PROD.	
NEXT HIGHER ASSY.	

SIZE D   CODE   NUMBER   REV. 1

SCALE

SHEET 1   OF 1   DIST.
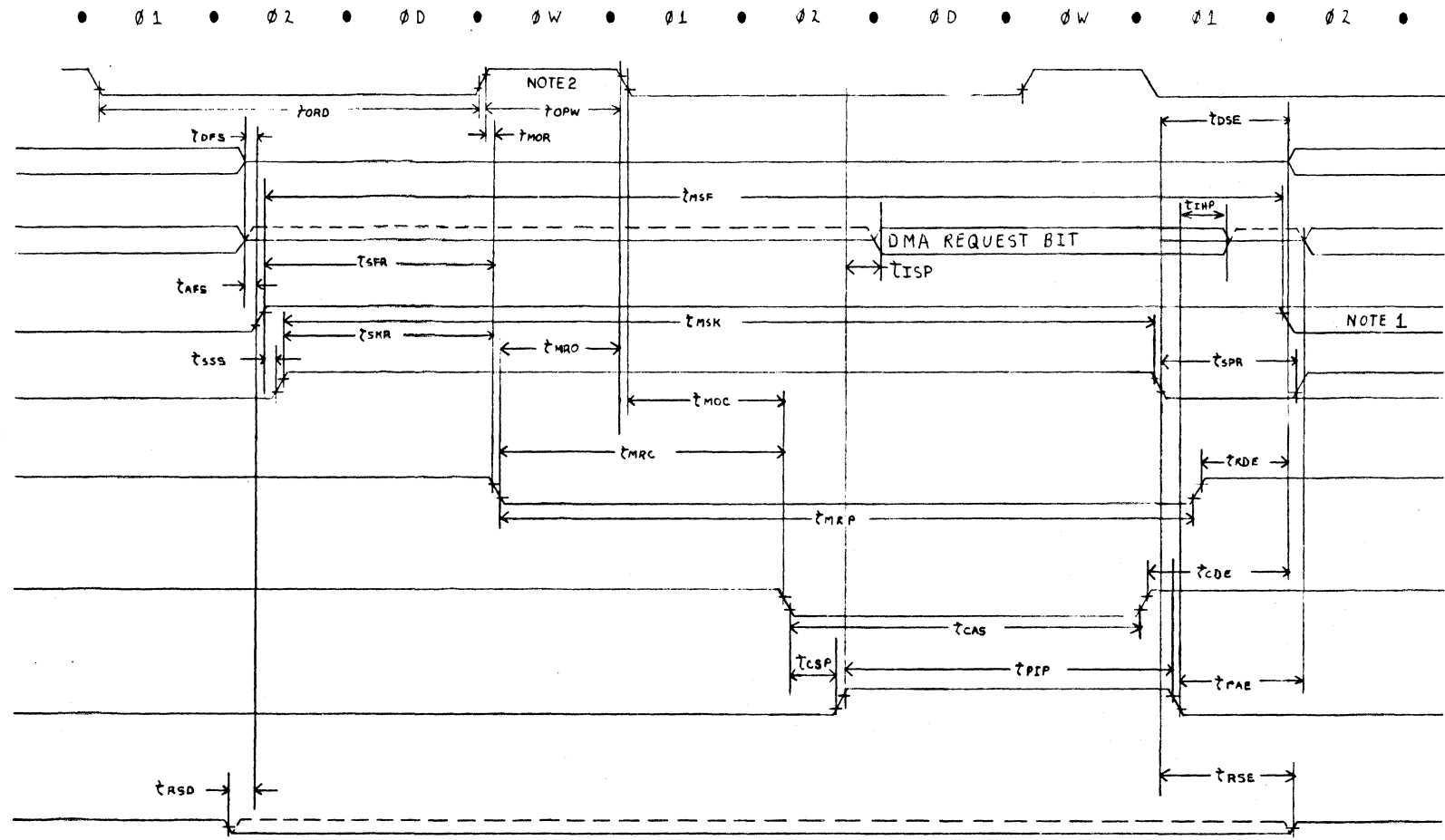
NOTE 1: IF THE NEXT MICRO CYCLE IS REFRESH, SEL∅ WILL REMAIN SET.
NOTE 2: PULSE MODE CLOCK.

NOTE 1: READY SIGNAL ASSERTED LOW TO CAUSE 1 MICRO CYCLE SLIP.
NOTE 2: READY SIGNAL ASSERTED TWICE TO CAUSE 2 MICRO CYCLE SLIP.
NOTE 3: READY SIGNAL TOGGLED DURING ØW (GATED WITH COUT) TO CAUSE MULTIPLE MICRO CYCLE SLIPS.
NOTE 4: PULSE MODE CLOCK.

1-MAR-82

DRN. B.. F
CHK'D
ENG.
PROJ ENG
PROD.
NEXT HIGHER ASSY.

FIRST USED ON

digital

TITLE
T-11
READY TIMING

SIZE D CODE NUMBER REV. 3

SCALE
SHEET OF DIST.

POWER UP TIMING   (NOTE 4)

RESET TIMING
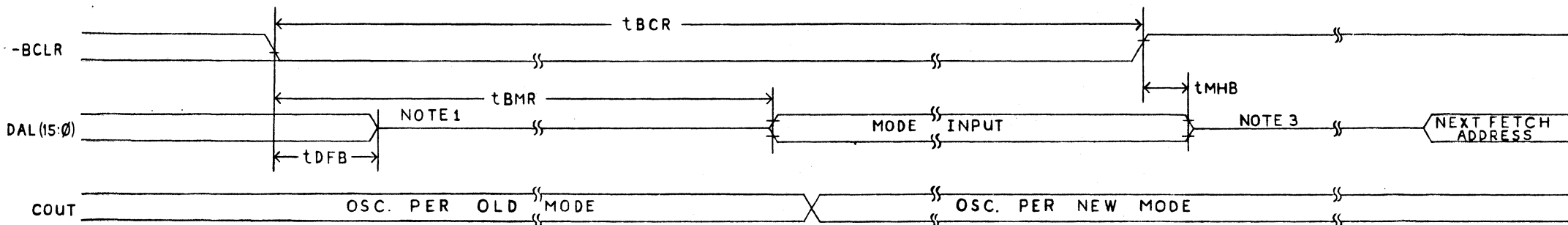
NOTE 1: LOW CURRENT PULLUPS ON DAL (15:8,2:0)
UNTIL -BCLR NEGATED

NOTE 2: REFRESH OR BUSNOP PER MODE SELECTION,
LOAD (SP, PC, PSW), AND ASPI TRANSACTION.
SEE POWER UP DESCRIPTION SECTION 2.3.4

NOTE 3: ASPI TRANSACTION

NOTE 4: -RAS, -CAS, PI, SEL0, SEL1, R/-WHB, R/-WLB
UNDEFINED DURING -BCLR TIME IF MODE
REGISTER INPUT VIOLATES DAL TRISTATE
TIME; OTHERWISE, -RAS, -CAS, PI, SEL0,
SEL1, R/-WHB, R/-WLB UNASSERTED AND LOW
CURRENT PULLUPS ON AI(7:0).

1-MAR-82

* CONSTANT MODE CLOCK (MRØ=Ø).   PHASE OUT COUT CAN CHANGE DEPENDING ON MODE AND INSTRUCTION
** PROCESSOR MODE CLOCK (MRØ=1).
NOTE: ASSERTED FOR READ (DELAYED MODE SHOWN).

5-AUG-80

DRN. M.R. Blake	8-5-80
CHK'D	
ENG.	
PROJ. ENG.	
PROD.	

FIRST USED ON

digital

TITLE T-11 LONG MICRO-
CYCLE MODE

NEXT HIGHER ASSY.

| SIZE | CODE | NUMBER | REV. |
| D | | | |

SCALE

SHEET 1 OF 1   DIST.

NOTE 1: DAL(15:8) IN 8 BIT MODE, WILL CONTAIN THE HIGH BYTE ADDRESS WORD FOR THE ENTIRE BUS CYCLE. IN 16 BIT MODE BYTE OPERATIONS, DAL BYTE NOT BEING ADDRESSED WILL DRIVE INDETERMINATE DATA.
NOTE 2: −RD SIGNAL IN 8 BIT MODE (NORMAL)
NOTE 3: −RD SIGNAL IN 8 BIT MODE (DELAYED)
NOTE 4: R/$\overline{W}$ (DELAYED MODE) HAS SAME TIMING AS −CAS
NOTE 5: ONLY DURING FETCH, IN ALL MODES EXCEPT 4K/16K DYNAMIC
NOTE 6: DURING A WRITE CYCLE, ONLY THE DMR IS ACCEPTED BY THE CHIP. INTERRUPTS ARE NOT ACCEPTED.
NOTE 7: EXCEPT DURING STACK OPERATIONS, ALL WRITE TRANSACTIONS ARE PRECEEDED BY READS.
NOTE 8: IN 8 BIT MODE WORD OPERATIONS, TWO BYTE TRANSACTIONS ARE DONE, THE FIRST TO THE LOW BYTE (ADDRESS ON DAL⟨0⟩=0) THE SECOND TO THE HIGH BYTE (ADDRESS ON DAL⟨0⟩=1).
NOTE 9: PULSE MODE CLOCK.

1-MAR-82
digital
TITLE
T-11
READ/WRITE TIMING
SIZE CODE: D   REV 6
SHEET 1 OF 1

APPENDIX A

T-11 INSTRUCTION EXECUTION TIMES AT MAXIMUM OPERATING FREQUENCY

The following pages contain charts that give execution times for all instructions executable by the T-11. The charts are organized to help those individuals who want to calculate program execution times. To do such a calculation, first choose your system configuration and then outline that column in the charts. Use only those execution times listed in the outlined column. The possible system configurations are:

1. 16 bit mode--REFRESH on;
2. 16 bit mode--REFRESH off;
3. 8 bit mode--REFRESH on;
4. 8 bit mode--REFRESH off.

Since a REFRESH cycle adds a small increment of time to the machine cycle, and since in 8 bit mode REFRESH is done every| instruction cycle and addressing mode 5, 6, or 7 I/O and trap (2 | occurances) it is possible for an instruction to have varying| execution times when REFRESH is on. This is why you will find MIN and MAX execution times for all (in 16 bit mode REFRESH is done| every other) "REFRESH on" configurations. You can calculate| program execution times for "REFRESH on" configurations by summing the average of the MIN and Max execution times. |

The following notes apply to all instruction execution charts:

1. All times are in microseconds.
2. Add 0.4 us for every -READY pulse during an I/O transaction.
3. Operating frequency is 7.5 MHz. To calculate instruction execution times (IET) at different operating frequencies use the following formula:

   $$IET(fOP) = (7.5\ MHz/fOP) * IET(7.5)$$

   Where:

   IET(fOP) = Instruction Execution Time for the new frequency, fOP.

   fOP = The operating frequency at which the instruction execution times are needed.

   IET(7.5) = Instruction Execution Times with an operating frequency of 7.5 MHz. These times are listed in the following charts.
4. NA => Not Applicable

NOTE: Times calculated using Revision 5.18 Microcode |

<div align="right">Rev B</div>

INSTRUCTIONS	DEST MODE	16 BIT MODE REFRESH ON MIN	16 BIT MODE REFRESH ON MAX	16 BIT MODE REFR OFF	8 BIT MODE REFRESH ON WORD INSTR	8 BIT MODE REFRESH ON BYTE INSTR	8 BIT MODE REFRESH OFF WORD INSTR	8 BIT MODE REFRESH OFF BYTE INSTR
===	===	===	===	===	===	===	===	===
CLR(B),COM(B),	0	1.6	1.73	1.6	2.53	2.53	2.4	2.4
INC(B),DEC(B),	1	2.8	2.93	2.8	5.33	3.73	5.2	3.6
NEG(B),ROR(B),	2	2.8	2.93	2.8	5.33	3.73	5.2	3.6
ROL(B),ASR(B),	3	3.6	3.73	3.6	6.93	5.33	6.8	5.2
ASL(B),SWAB,	4	3.2	3.33	3.2	5.73	4.13	5.6	4.0
ADC(B),SBC(B),	5	4.13	4.26	4.0	7.46	5.86	7.2	5.6
SXT,MFPS,	6	4.13	4.26	4.0	7.46	5.86	7.2	5.6
XOR	7	4.93	5.06	4.8	9.06	7.46	8.8	7.2
===	===	===	===	===	===	===	===	===
	0	1.6	1.73	1.6	2.53	2.53	2.4	2.4
	1	2.4	2.53	2.4	4.13	3.33	4.0	3.2
	2	2.4	2.53	2.4	4.13	3.33	4.0	3.2
TST(B)	3	3.2	3.33	3.2	5.73	4.93	5.6	4.8
	4	2.8	2.93	2.8	5.33	3.73	5.2	3.6
	5	3.73	3.86	3.6	6.26	5.46	6.0	5.2
	6	3.73	3.86	3.6	6.26	5.46	6.0	5.2
	7	4.53	4.66	4.4	7.86	7.06	7.6	6.8
===	===	===	===	===	===	===	===	===
	0	3.2	3.33	3.2	4.13	4.13	4.0	4.0
	1	4.0	4.13	4.0	4.93	4.93	4.8	4.8
	2	4.0	4.13	4.0	4.93	4.93	4.8	4.8
MTPS	3	4.8	4.93	4.8	6.53	6.53	6.4	6.4
	4	4.4	4.53	4.4	5.33	5.33	5.2	5.2
	5	5.33	5.46	5.2	7.06	7.06	6.8	6.8
	6	5.33	5.46	5.2	7.06	7.06	6.8	6.8
	7	6.13	6.26	6.0	8.66	8.66	8.4	8.4
===	===	===	===	===	===	===	===	===

NOTES: 1. XOR and Single Operand Instruction execution times include
instruction fetch, instruction decode, operand fetch, instruction
operation and result output (except in Mode 0 and the TST(B)
instruction where there is no output).

Rev B

DOUBLE OPERAND INSTRUCTIONS
==============================

```
****************************************************************************
*                                                                          *
* (DOUBLE OPERAND EXECUTION TIME) = (SOURCE MODE TIME) + (DESTINATION MODE *
*                                                           TIME)          *
*                                                                          *
****************************************************************************
```

SOURCE MODE TIME

INSTRUCTIONS	SRC MODE	16 BIT MODE					8 BIT MODE			
		REFRESH ON				REFR OFF	REFRESH ON		REFRESH OFF	
		DST MODE 0-4		DST MODE 5-7			WORD INSTR	BYTE INSTR	WORD INSTR	BYTE INSTR
		MIN	MAX	MIN	MAX					
	0	1.2	1.33	1.33	1.33	1.2	2.13	2.13	2.0	2.0
	1	2.0	2.13	2.13	2.13	2.0	3.73	2.93	3.6	2.8
MOV(B),CMP(B),	2	2.0	2.13	2.13	2.13	2.0	3.73	2.93	3.6	2.8
ADD,SUB	3	2.8	2.93	2.93	2.93	2.8	5.33	4.53	5.2	4.4
BIT(B),BIC(B),	4	2.4	2.53	2.53	2.53	2.4	4.13	3.33	4.0	3.2
BIS(B)	5	3.33	3.33	3.33	3.46	3.2	5.86	5.06	5.6	4.8
	6	3.33	3.33	3.33	3.46	3.2	5.86	5.06	5.6	4.8
	7	4.13	4.13	4.13	4.26	4.0	7.46	6.66	7.2	6.4

NOTES: 1. Source Mode times include instruction fetch, instruction decode
          and source operand fetch.

Rev B

DESTINATION MODE TIME

INSTRUCTIONS	DEST MODE	16 BIT MODE			8 BIT MODE			
		REFRESH ON		REFR OFF	REFRESH ON		REFRESH OFF	
		MIN	MAX		WORD INSTR	BYTE INSTR	WORD INSTR	BYTE INSTR
	0	0.4	0.4	0.4	0.4	0.4	0.4	0.4
	1	1.6	1.6	1.6	2.4	1.6	2.4	1.6
MOV(B),ADD,	2	1.6	1.6	1.6	2.4	1.6	2.4	1.6
SUB,BIC(B)	3	2.4	2.4	2.4	4.0	3.2	4.0	3.2
BIS(B)	4	2.0	2.0	2.0	2.8	2.0	2.8	2.0
	5	2.8	2.8	2.8	4.53	3.73	4.4	3.6
	6	2.8	2.8	2.8	4.53	3.73	4.4	3.6
	7	3.6	3.6	3.6	6.13	5.33	6.0	5.2
	0	0.4	0.4	0.4	0.4	0.4	0.4	0.4
	1	1.2	1.2	1.2	2.0	1.2	2.0	1.2
	2	1.2	1.2	1.2	2.0	1.2	2.0	1.2
⁻MP(B),BIT(B)	3	2.0	2.0	2.0	3.6	2.8	3.6	2.8
	4	1.6	1.6	1.6	2.4	1.6	2.4	1.6
	5	2.4	2.4	2.4	4.13	3.33	4.0	3.2
	6	2.4	2.4	2.4	4.13	3.33	4.0	3.2
	7	3.2	3.2	3.2	5.73	4.93	5.6	4.8

NOTES: 1. Destination Mode times include destination operand fetch, instruction operation and result output (except in Destination Mode 0 and the CMP(B) and BIT(B) instructions where there is no output).

Rev B

Rev B

INSTRUCTIONS	DEST MODE	16 BIT MODE			8 BIT MODE			
		REFRESH ON		REFR OFF	REFRESH ON		REFRESH OFF	
		MIN	MAX		WORD INSTR	BYTE INSTR	WORD INSTR	BYTE INSTR
===	===	===	===	===	===	===	===	===
JMP	1	2.0	2.13	2.0	2.93	NA	2.8	NA
	2	2.4	2.53	2.4	3.33	NA	3.2	NA
	3	2.4	2.53	2.4	4.13	NA	4.0	NA
	4	2.4	2.53	2.4	3.33	NA	3.2	NA
	5	2.93	2.93	2.8	4.53	NA	4.4	NA
	6	2.93	2.93	2.8	4.53	NA	4.4	NA
	7	3.73	3.73	3.6	6.13	NA	6.0	NA
JSR	1	3.6	3.73	3.6	5.33	NA	5.2	NA
	2	4.0	4.13	4.0	5.73	NA	5.6	NA
	3	4.0	4.13	4.0	6.53	NA	6.4	NA
	4	4.0	4.13	4.0	5.73	NA	5.6	NA
	5	4.53	4.53	4.4	6.93	NA	6.8	NA
	6	4.53	4.53	4.4	6.93	NA	6.8	NA
	7	5.33	5.33	5.2	8.53	NA	8.4	NA
RTS	NA	2.8	2.93	2.8	4.53	NA	4.4	NA
SOB	NA	2.4	2.53	2.4	3.33	NA	3.2	NA

NOTES: 1. JMP/JSR Destination Mode 0 is an illegal instruction that traps to vector location 10.

2. JMP execution times include instruction fetch, instruction decode, operand fetch and loading of the PC.

3. JSR execution times include instruction fetch, instruction decode, operand fetch, pushing the linkage register onto the stack and loading the PC.

4. RTS execution times include instruction fetch, instruction decode, loading the PC and popping the stack and loading the linkage register.

5. SOB execution times include instruction fetch, instruction decode, decrementing the count register, testing for zero and branching if necessary (NOTE: whether or not a branch is taken does not affect the execution time).

Rev B

BRANCH, TRAP & INTERRUPT INSTRUCTIONS
===================================

INSTRUCTIONS	DEST MODE	16 BIT MODE			8 BIT MODE			
		REFRESH ON		REFR OFF	REFRESH ON		REFRESH OFF	
		MIN	MAX		WORD INSTR	BYTE INSTR	WORD INSTR	BYTE INSTR
===	===	===	===	===	===	===	===	===
BR,BNE,BEQ, BPL,BMI,BVC, BVS,BCC,BCS, BGE,BLT,BGT, BLE,BHI,BLOS, BHIS,BLO	NA	1.6	1.73	1.6	2.53	NA	2.4	NA
EMT,TRAP, BPT,IOT	NA	6.53	6.66	6.4	9.73	NA	9.6	NA
₹TI	NA	3.2	3.33	3.2	4.93	NA	4.8	NA
RTT	NA	4.4	4.53	4.4	7.13	NA	7.0	NA

NOTES: 1. Branch instructions execution times include instruction fetch, instruction decoding, doubling the offset, testing the conditions and adding the offset to the PC if the conditions are met (NOTE: Whether or not a branch is taken does not affect the execution times).

2. Trap instructions execution times include instruction fetch, instruction decode, pushing the PS and PC onto the stack, loading the PC with the contents of the vector location and loading the PS with the contents of the vector location plus two.

3. Return from interrupt instructions execution times include instruction fetch, instruction decode and popping the PC and PS from the stack.

Rev B

INSTRUCTIONS	DEST MODE	16 BIT MODE REFRESH ON		REFR OFF	8 BIT MODE REFRESH ON WORD INSTR	BYTE INSTR	REFRESH OFF WORD INSTR	BYTE INSTR
		MIN	MAX					
HALT	NA	5.73	5.86	5.6	8.4	NA	8.0	NA
WAIT	NA	1.6	1.73	1.6	2.43	NA	2.4	NA
RESET	NA	14.6	14.73	14.6	16.53	NA	16.4	NA
NOP	NA	2.4	2.53	2.4	3.33	NA	3.2	NA
CLC,CLV,CLZ, CLN,CCC,SEC, SEV,SEZ,SEN, SCC	NA	2.4	2.53	2.4	3.33	NA	3.2	NA
LFPT	NA	2.0	2.13	2.0	2.93	NA	2.8	NA

NOTES: 1. HALT execution times include instruction fetch, instruction decode, writing the PC & PS into stack then loading the PS with 340 and loading the PC with the RESTART address.

2. WAIT execution times include instruction fetch, instruction decode, pulsing PI to sample the interrupt lines and doing a REFRESH cycle if REFRESH is on. (NOTE: If no interrupt lines were sensed by the T-11 to be asserted during the PI pulse, the WAIT instruction will cycle in a 1.2 us loop (if REFRESH is on the loop will be 1.33 us max) pulsing PI. The looping will continue until an interrupt line is sensed by the T-11 to be asserted.)

3. RESET execution times include instruction fetch, instruction decode, the assertion of -BCLR and the writing of DAL<15:0> into the MODE register.

4. NOP execution times include instruction fetch, instruction decode and idle time.

5. Condition Code instructions execution times include instruction fetch, instruction decode and the setting or resetting of the appropriate status flags in the PS.

MAXIMUM LATENCIES
==================

ACTIVE INPUTS	DEST MODE	16 BIT MODE		8 BIT MODE	
		DYNAMIC	STATIC	DYNAMIC	STATIC
==============================	==========	========	========	========	========
-CP<3:0>,-PF (INTERNAL VECTOR) 4)	NA	15.47	15.20	22.13	21.60
-VEC,-CP<3:0> (EXTERNAL VECTOR) 4)	NA	15.87	15.60	22.53	22.00
DMR 5)	NA	3.66	3.52	4.46	4.32
WAIT INSTR					
INTERNAL VECTOR	NA	7.87	7.73	10.53	10.13
EXTERNAL VECTOR	NA	8.27	8.13	10.93	10.53
DMR	NA	1.66	1.66	1.79	1.66

NOTES: 0. These timings are given in microseconds and assume clock frequency of 7.5 MHz.

1. Interrupt latency is measured from the time the INTERRUPT REQUEST is asserted either on the AI lines (in static modes), or the input of the AI line driver (in dynamic modes), until the time the T-11 is ready to fetch the first instruction in the interrupts' service routine. In this time T-11 takes 3 actions, as shown in figure A.1:

    a)   Keeps going until a PI latches the request. This could happen in the instruction following the request.
    b)   Finishes the instruction that latched the request.
    c)   Executes the IACK microcode, which involves priority arbitration, issuing IACK, generating the interrupt vector (or in the case of -VEC being asserted, reading in the external vector), pushing PSW and PC onto the stack and loading PC and PSW from vector and vector +2.

Rev A

Figure A.1.   Interrupt Latency

Note that the time to synchronize the IRQ and to perform any external priority arbitration is not included in the interrupt latency.

2. DMG latency is calculated from the time DMR is valid on the input of the AI line driver until the T-11 has asserted DMG.

3. WAIT instruction latencies are the maximum encountered in the instruction's execution state.   These times do not include the instruction fetch or the instruction decode.

4. These times refer to IRQ occurring during a JSR (Mode 2 or 4), EMT sequence, which is worst case.

5. These times refer to DMR occurring during a MTPS (Mode 0) instruction, which is worst case.

6. These timings assume T-11 is not in long bus cycle (mode register bit 1) and there are no ready slips either.

<div align="right">Rev B</div>

T-11 INSTRUCTION EXECUTION TIMES IN MICROCYCLES

XOR & SINGLE OPERAND INSTRUCTIONS
=====================================

INSTRUCTIONS	DEST MODE	16 BIT MODE	8 BIT MODE WORD INSTRUCTION	BYTE INSTRUCTION
CLR(B),COM(B),	0	4	6	6
INC(B),DEC(B),	1	7	13	9
NEG(B),ROR(B),	2	7	13	9
ROL(B),ASR(B),	3	9	17	13
ASL(B),SWAB,	4	8	14	10
ADC(B),SBC(B),	5	10	18	14
SXT,MFPS,	6	10	18	14
XOR	7	12	22	18
	0	4	6	6
	1	6	10	8
	2	6	10	8
TST(B)	3	8	14	12
	4	7	11	9
	5	9	15	13
	6	9	15	13
	7	11	19	17
	0	8	10	10
	1	10	12	12
	2	10	12	12
MTPS	3	12	16	16
	4	11	13	13
	5	13	17	17
	6	13	17	17
	7	15	21	21

NOTES: 1. XOR and Single Operand Instruction execution times include
           instruction fetch, instruction decode, operand fetch,
           instruction operation and resultant output (except in Mode
           0 and the TST(B) instruction where there is no output).

Rev B

DOUBLE OPERAND INSTRUCTIONS
============================

```
*****************************************************************
*                                                               *
*      (DOUBLE OPERAND EXECUTION TIME) = (SOURCE MODE TIME) +    *
*                    (DESTINATION MODE TIME)                     *
*                                                               *
*****************************************************************
```

SOURCE MODE TIME

INSTRUCTIONS	SRC MODE	16 BIT MODE	8 BIT MODE	
			WORD INSTRUCTION	BYTE INSTRUCTION
===	===	===	===	===
	0	3	5	5
	1	5	9	7
MOV(B),CMP(B),	2	5	9	7
ADD,SUB,	3	7	13	11
BIT(B),BIC(B),	4	6	10	8
BIS(B)	5	8	14	12
	6	8	14	12
	7	10	18	16

NOTES: 1. Source Mode times include instruction fetch, instruction
           decode and source operand fetch.

Rev B

DESTINATION MODE TIME

INSTRUCTIONS	DEST MODE	MICRO CYCLES REQUIRED		
		16 BIT MODE	8 BIT MODE	
			WORD INSTRUCTION	BYTE INSTRUCTION
==================	========	==============	==============	==============
	0	1	1	1
	1	4	8	4
MOV(B),ADD,	2	4	8	4
SUB,BIC(B),	3	6	12	8
BIS(B)	4	5	9	5
	5	7	13	9
	6	7	13	9
	7	9	17	13
==================	========	==============	==============	==============
	0	1	1	1
	1	3	5	3
	2	3	5	3
CMP(B),BIT(B)	3	5	9	7
	4	4	6	4
	5	6	10	8
	6	6	10	8
	7	8	14	12
==================	========	==============	==============	==============

NOTES: 1. Destination Mode times include destination operand fetch,
         instruction operation and resultant output (except in
         Destination Mode 0 and the CMP(B) and BIT(B) instructions
         where there is no output).

                                                              Rev B

JUMP & SUBROUTINE INSTRUCTIONS
===============================

INSTRUCTIONS	DEST MODE	MICRO CYCLES REQUIRED	
		16 BIT MODE	8 BIT MODE
JMP	1	5	7
	2	6	8
	3	6	10
	4	6	8
	5	7	11
	6	7	11
	7	9	15
JSR	1	9	13
	2	10	14
	3	10	16
	4	10	14
	5	11	17
	6	11	17
	7	13	21
RTS	NA	7	11
SOB	NA	6	8

NOTES: 1. JMP/JSR Destination Mode Ø is an illegal instruction that traps to vector location 1Ø.

2. JMP execution times include instruction fetch, instruction decode, operand fetch and loading of the PC.

3. JSR execution times include instruction fetch, instruction decode, operand fetch, pushing the linkage register onto the stack and loading the PC.

4. RTS execution times include instruction fetch, instruction decode, loading the PC and popping the stack and loading the linkage register.

5. SOB execution times include instruction fetch, instruction decode, decrementing the count register, testing for zero and branching if necessary
(NOTE: Whether or not a branch is taken does not affect the execution time).

Rev B

BRANCH, TRAP & INTERRUPT INSTRUCTIONS
=======================================

INSTRUCTIONS	DEST MODE	MICRO CYCLES REQUIRED	
		16 BIT MODE	8 BIT MODE
BR,BNE,BEQ, BPL,BMI,BVC BVS,BCC,BCS, BGE,BLT,BGT, BLE,BHI,BLOS, BHIS,BLO	NA	4	6
EMT,TRAP, BPT,IOT	NA	16	24
RTI	NA	8	12
RTT	NA	8	12

NOTES: 1. Branch instructions execution times include instruction fetch, instruction decoding, doubling the offset, testing the conditions and adding the offset to the PC if the conditions are met (NOTE: Whether or not a branch is taken does not affect the execution times).

2. Trap instructions execution times include instruction fetch, instruction decode, pushing the PS and PC onto the stack, loading the PC with the contents of the vector location and loading the PS with the contents of the vector location plus two.

3. Return from interrupt instructions execution times include instruction fetch, instruction decode and popping the PC and PS from the stack.

Rev B

INSTRUCTIONS	DEST MODE	CYCLES REQUIRED	
		16 BIT MODE	8 BIT MODE
==================	===========	================	=============
HALT	NA	14	21
WAIT	NA	4 then loop	6 then loop
RESET	NA	39	41
NOP	NA	6	8
CLC,CLV,CLZ, CLN,CCC,SEC, SEV,SEZ,SEN, SCC	NA	6	8
MFPT	NA	5	7

NOTES: 1. HALT execution times include instruction fetch, instruction decode, writing the PC and PS into the stack, then loading the PS with 340 and loading the PC with the RESTART address.

2. WAIT execution times include instruction fetch, instruction decode, pulsing PI to sample the interrupt lines and doing a REFRESH cycle if REFRESH is on. (NOTE: If no interrupt lines were sensed by the T-11 to be asserted during the PI pulse, the WAIT instruc- tion will cycle in a 2 micro-instruction loop (if REFRESH is on the loop will be 2 1/3 micro-instructions max) pulsing PI. The looping will continue until an interrupt line is sensed by the T-11 to be asserted.)

3. RESET execution times include instruction fetch, instruction decode, the assertion of -BCLR and the writing of DAL<15:0> into the MODE register.

4. NOP execution times include instruction fetch, instruction decode and idle time.

5. Condition Code instructions execution times include instruction fetch, instruction decode and the setting or resetting of the appropriate status flags in the PS.

Rev B

MAXIMUM LATENCIES

ACTIVE INPUTS	DEST MODE	MICRO CYCLES REQUIRED											
		STATIC 16 BIT MODE			DYNAMIC 16 BIT MODE			STATIC 8 BIT MODE			DYNAMIC 8 BIT MODE		
		CY	Ø	uS	CY	Ø	uS	CY	Ø	uS	CY	Ø	uS
-CP<3:0>,-PF 4) (INTERNAL VECTOR)	NA	38			38	2		54			54	4	
-VEC,-CP<3:0> 4) (EXTERNAL VECTOR)	NA	39			39	2		55			55	4	
DMR 5)	NA	8	1	.19	8	2	.19	10	1	.19	10	2	.19
WAIT INSTR													
INTERNAL VECTOR	NA	19	1		19	2		25	1		25	4	
EXTERNAL VECTOR	NA	20	1		20	2		26	1		26	4	
DMR	NA	3	2	.19	3	2	.19	3	2	.19	3	3	.19

NOTES: 0. These timings are given in microcycles (assuming 3 phases/cycle) + extra phases + microseconds.

1. Interrupt latency is measured from the time the INTERRUPT REQUEST is asserted either on the AI lines (in static modes), or the input of the AI line driver (in dynamic modes), until the time the T-11 is ready to fetch the first instruction in the interrupts' service routine. In this time T-11 takes 3 actions, as shown in figure A.1:

    a)   Keeps going until a PI latches the request. This could happen in the instruction following the request.

    b)   Finishes the instruction that latched the request.

    c)   Executes the IACK microcode, which involves priority arbitration, issuing IACK, generating the interrupt vector (or in the case of -VEC being asserted, reading in the external vector), pushing PSW and PC onto the stack and loading PC and PSW from vector and vector +2.

Rev B

```
|  _____  |
| |                            |IACK       |FIRST INSTRUCTION |      |
| |                  LAST       |MICROCODE  |OF SERVICE        |      |
| |              INSTRUCTION    |           |ROUTINE           |      |
| |              _____    |           |_____|      |
| |                             |           |                         |
| |      ____ <--a-->|<---b--->|<----c----->|                         |
| |     |    |       |         |            |                         |
| | IRQ |    |_____|_____  |            |                         |
| |     |            |       | |            |                         |
| |     |            |       | |            |                         |
| |                  |  ___  | |            |                         |
| |                  | |   | | |            |                         |
| | PI  _____| |   |_|_|            |                         |
| |                  |_|     | |            |                         |
| |                          | |   ___      |                         |
| |                          | |  |   |     |                         |
| | IACK _____| |__|   |_____|_____       |
| |                          | |      |     |                         |
| |                                                                   |
| |           Figure A.1.   Interrupt Latency                         |
|  _____  |
```

Note that the time to synchronize the IRQ and to perform any
external priority arbitration is not included in the interrupt
latency.

2. DMG latency is calculated from the time DMR is valid on the input
   of the AI line driver until the T-11 has asserted DMG.

3. WAIT instruction latencies are the maximum encountered in the
   instruction's execution state. These times do not include the
   instruction fetch or the instruction decode.

4. These times refer to IRQ occurring during a JSR (Mode 2 or 4),
   EMT sequence, which is worst case.

5. These times refer to DMR occurring during a MTPS (Mode 0)
    instruction, which is worst case.

6. These timings assume T-11 is not in long bus cycle (mode register
   bit 1) and there are no ready slips either.

                                                            Rev A

PDP11 DIFFERENCES LIST

ACTIVITY	PDP-11 FAMILY MACHINES								
	T11	F11	04	34	LSI 11	05 10	15 20	35 40	45
1. OPR %R,(R)+ or OPR %R,-(R) using the same register as both source and destination: contents of R are incremented (decremented) by 2 before being used as the source operand.	X	X					X	X	
OPR %R,(R)+ or OPR %R,-(R) using the same register as both register and destination: initial contents of R are used as the source operand.			X	X	X	X			X
2. OPR %R,@(R)+ or OPR %R,@-(R) using the same register as both source and destination: contents of R are incremented (decremented) by 2 before being used as the source operand.	X	X					X	X	
OPR %R,@(R)+ or OPR %R,@-(R) using the same register as both source and destination: initial contents of R are used as the source operand.			X	X	X	X			X
3. OPR PC,X(R); OPR PC,@X(R); OPR PC,@A; OPR PC,A: Location A will contain the PC of OPR +4.	X	X					X	X	
OPR PC,X(R); OPR PC,@X(R); OPR PC,A; OPR PC,@A: Location A will contain the PC of OPR +2.			X	X	X	X			X
4. JMP (R)+ or JSR reg,(R)+: Contents of R are incremented by 2, then used as the new PC address.						X	X		
JMP (R)+ or JSR reg,(R)+: Initial contents of R are used as the new PC.	X	X	X	X	X			X	X
5. JMP %R or JSR reg,%R traps to 4 (illegal instruction.	X	X	X	X	X	X	X	X	
JMP %R or JSR reg,%R traps to 10 (illegal instruction).									X
6. SWAB does not change V.							X		
SWAB clears V.	X	X	X	X	X	X		X	X

| | PDP-11 FAMILY MACHINES | | | | | | | | |
ACTIVITY	T11	F11	04	34	LSI 11	05 10	15 20	35 40	45
7. Register addresses (177700 - 177717) are valid program addresses when used by the CPU.						X			
Register addressed (177700 - 177717) time out when used as a program address by the CPU. Can be addressed under console operation. Note: Addresses cannot be addressed under console for LSI-11 or F-11.		X			X		X	X	X
Register addresses (177700 - 177717) are handled as regular memory addresses (in the BSIO page). No internal registers are addressable from either the bus or the console.	X								
8. BASIC INSTRUCTIONS noted in PDP-11 processor handbook.	X	X	X	X	X	X	X	X	X
MFPT (move from processor type)	X								
SOB, RTT, SXT instructions.	X	X	X	X	X			X	X
MARK instruction.		X	X	X	X			X	X
ASH, ASHC, DIV, MUL instructions.		X		X	X			X	X
XOR instruction.	X	X	·	X	X			X	X
The external option KE11-A provides MUL, DIV and SHIFT operations in the same data format.						X	X		
The KE11-E (Expansion Instruction Set) provides the instructions MUL, DIV, ASH, and ASHC. These new instructions are 11/45 compatible.		·						X	
The KE11-F adds unique stack ordered floating point instructions: FADD, FSUB, FMUL, FDIV.								X	
The KEV-11 adds ETS/FIS instructions.					X				
SPL instruction.									X

ACTIVITY	T11	F11	04	34	LSI 11	05 10	15 20	35 40	45
Power fail during RESET instruction is not recognized until after the instruction is finished (70 milliseconds). RESET instruction consists of 70 millisecond pause with INIT occurring during first 20 milliseconds.							X	X	
Power fail immediately ends the RESET instruction and traps if an INIT is in progress. A minimum INIT of 1 microsecond occurs if instructions aborted.									X
Power fail acts the same as 11/45 (22 milliseconds with about 300 nanoseconds minimum). Power fail during RESET fetch is fatal with no power down sequence.			X	X	X				
RESET instruction consists of 10 microseconds of INIT followed by a 90 microsecond pause. Power fail not recognized until the instruction is complete.		X			X				
RESET instruction consists of a minimum 8.4 microseconds followed by a minimum 150 nanosecond pause. Power fail is not recognized until the instruction is complete.	X								
. No RTT instruction.						X	X		
If RTT sets the T bit, the T bit trap occurs after the instruction following RTT.	X	X	X	X	X			X	X
. If RTI sets the T bit, the T bit trap is acknowledged after the instruction following RTI.						X	X		
If RTI sets the T bit, the T bit trap is acknowledged immediately following RTI.	X	X	X	X	X			X	X
A. When operating with the T-bit set (e.g. single stepping) no interrupt requests will be serviced. At the end of instruction execution, the T-bit has higher priority than interrupt requests. Once in the T-bit service routine, other interrupts are blocked to insure no unexpected occurances. When the RTT instruction is executed to leave the service routine, interrupts will not be serviced if the T-bit is set in the new PS popped off the stack. The user will, therefore, not see any interrupt requests he is expecting.	X								

ACTIVITY	T11	F11	04	34	LSI 11	05 10	15 20	35 40	45
12. If an interrupt occurs during an instruction that has the T bit set, the T bit trap is acknowledged before the interrupt.	X	X	X	X	X	X	X	X	
If an interrupt occurs during an instruction and the T bit is set, the interrupt is acknowledged before the T bit trap.									X
13. T bit trap will sequence out of WAIT instruction.	X	X	X	X		X	X	X	
T bit trap will not sequence out of WAIT instruction. Waits until an interrupt.					X				X
14. Explicit reference (direct access) to PS can load the T bit. Console can also load the T bit.				X		X	X		
Only implicit references (RTI, RTT, traps and interrupts) can load the T bit. Console cannot load the T bit.	X	X		X	X			X	X
15. Odd address/non-existent references using the SP cause a HALT. This is a case of double bus error with the second error occurring in the trap servicing the first error. Odd address trap not in LSI-11 or F-11.		X	X	X	X	X	X		
Odd address/non-existent references using the SP cause a fatal trap. On bus error in trap service, new stack created at 0/2.								X	X
Odd address/non-existent references using the SP do not trap.	X								
16. The first instruction in an interrupt routine will not be executed if another interrupt occurs at a higher priority level than assumed by the first interrupt.	X	X	X	X	X	X		X	X
The first instruction in an interrupt service is guaranteed to be executed.							X		
17. 8 General purpose registers.	X	X	X	X	X	X	X	X	
16 General purpose registers.									X
18. PSW address, 177776, not implemented. Must use new instructions, MTPS (Move to PS) and MFPS (Move from PS).	X				X				
PSW address implemented. MTPS and MFPS not implemented.			X			X	X	X	X
PSW address and MTPS and MFPS implemented.		X		X					
19. Only one interrupt level (BR4) exists.					X				

	1	2	3	4	5	6	7	8
Four interrupt levels exist.		X	X	X		X	X	X	X
Four interrupt levels exist encoded in four lines.	X								
20. Stack overflow not implemented.	X				X				
Some sort of stack overflow implemented.		X	X	X		X	X	X	X
21. Odd address trap not implemented.	X	X			X				
Odd address trap implemented.			X	X		X	X	X	X
22. FMUL and FDIV instructions implicitly use R6 (one push and pop); hence R6 must be set up correctly.					X				
FMUL and FDIV instructions do not implicitly use R6.								X	
23. Due to their execution time, EIS instructions can abort because of a device interrupt.					X				
EIS instructions do not abort because of a device interrupt.		X						X	X
24. Due to their execution time, FIS instructions can abort because of a device interrupt.					X	X			
25. EIS instructions do a DATIP and DATO bus sequence when fetching source operand.					X				
EIS instructions do a DATI bus sequence when fetching source operand.		X						X	X
26. MOV instruction does just a DATO bus sequence for the last memory cycle.		X	X	X	X		X	X	
MOV instruction does a DATIP and DATO bus sequence for the last memory cycle.			X			X	X		
MOV instruction does a READ (DATI) and a WRITE (DATO) bus sequence for the last memory cycle.	X								
27. If PC contains non-existent memory address and a bus error occurs, PC will have been incremented.		X	X	X	X	X	X		
If PC contains non-existent memory address and a bus error occurs, PC will be unchanged.								X	
Does not support bus errors.	X								
28. If register contains non-existent memory address in mode 2 and a bus error occurs, register will be incremented.		X			X	X	X	X	X
If register contains non-existent memory address in mode 2 and a bus error occurs, register will be unchanged.			X	X					
Does not support bus errors.	X								
29. If register contains an odd value in mode 2 and a		X			X		X	X	

Description									
bus e( ) occurs, register will be incremented.									
If register contains an odd value in mode 2 and a bus error occurs, register will be unchanged.			X	X			X	X		
Does not support bus errors.	X								
30. Condition codes restored to original values after FIS interrupt abort (EIS doesn't abort on 35/40).								X	
Condition codes that are restored after EIS/FIS interrupt abort are indeterminate.						X			
31. Op codes 075040 thru 075377 unconditionally trap to 10 as reserved Op codes.	X	X	X	X			X	X	X
If KEV-11 option is present, Op codes 075040 thru 075377 perform a memory read using the register specified by the low order 3 bits as a pointer. If the register contents is a non-existent address, a trap to 4 occurs. If the register contents is an existent address, a trap to 10 occurs if user microcode is not present. If no KEV-11 option is present, a trap to 10 occurs.						X			
32. Op codes 210 thru 217 trap to 10 as reserved Op codes.	X	X	X	X			X	X	X
Op codes 210 thru 217 are used as a maintenance instruction.						X			
33. Op codes 75040 thru 75777 trap to 10 as reserved Op codes.	X	X	X	X			X	X	X
Only if Kev-11 option is present, op codes 75040 thru 75377 can be used as escapes to user microcode. Op codes 75400 thru 75777 can also be used as escapes to user microcode and KEV-11 option need not be present. If no user microcode exists, a trap to 10 occurs.						X			
34. Op codes 170000 thru 177777 trap to 10 as reserved instructions.	X		X				X	X	X
Op codes 170000 thru 177777 are implemented as floating point instructions.		X		X					X
Op codes 170000 thru 177777 can be used as escapes to user microcode. If no user microcode exists, a trap to 10 occurs.						X			
35. CLR and SXT do just a DATO sequence for the last bus cycle.		X							
CLR and SXT do DATIP-DATO sequence for the last bus cycle.			X	X	X	X	X	X	X
CLR and SXT do a READ (DATI) and a WRITE (DATO) sequence for the last bus cycle.	X								
36. MEM. MGT. maintenance mode SR0 bit 8 is implemented.				X				X	X

Description	1	2	3	4	5	6	7	8
MEM. MGT. maintenance mode SR0 bit 8 is not implemented.		X						
37. PS<15:12>, user mode, user stack pointer, and MTPX and MFPX instructions exist even when MEM. MGT. is not configured.		X						X
PS<15:12>, user mode, user stack pointer, and MTPX and MFPX instructions exist only when MEM. MGT. is configured.							X	
38. Current mode PS bits <15:14> set to 01 or 10 will cause a MEM. MGT. trap upon any memory reference.				X			X	X
Current mode PS bits <15:14> set to 01 or 10 will be treated as kernel mode (00) and not cause a MEM. MGT. trap.		X						
39. MTPS in user mode will cause a MEM. MGT. trap if PS address 177776 is not mapped. If mapped PS<7:5> and <3:0> are affected.		X						
MTPS in user mode will only affect PS<3:0> regardless of whether PS address 177776 is mapped.				X				
40. MFPS in user mode will cause MEM. MGT. trap if PS address 177776 not mapped. If mapped, PS<7:0> are accessed.				X				
MFPS in user mode will acces PS<7:0> regardless of whether PS address 177776 is mapped.		X						
41. A HALT instruction in user mode traps to 4							X	
A HALT instruction in user mode traps to 10.		X		X			X	
42. A HALT instruction pushes PC & PSW to stack, load the PS with 340, and load the PC with power up address + 4 (restart address).	X							
43. Resident ODT microcode.		X		X				
44. All data outs (DATO) are precedeed by a data in (DATI)	X							
45. Instruction execution runs to completion regardless of bus erros.	X							
46. Vector address range limited to 4 to 374.	X							

HARDWARE DIFFERENCES - TRAPS
(TRANSPARENT TO SOFTWARE)

T11	F11	11/04	11/34
Priority of internal processor traps, external interrupts, HALT and WAIT:	Priority of internal processor traps, external interrupts, HALT and WAIT:	Priority of internal processor traps, external interrupts, HALT and WAIT:	Priority of internal processor traps, external interrupts, HALT and WAIT:

TRAP Instructions
HALT INTERRUPT
TRACE TRAP
External Vector
   Interrupt
Internal Vector
  Interrupt
  Power Fail Trap
WAIT Loop
TEST Mode Request
	Memory Parity Errors
	Memory Management
	   Fault
	Bus Error Traps
	TRAP Instructions
	TRACE Trap
	OVFL Trap
	Power Fail Trap
	Console Bus Request
	Q-BUS Bus Request
	WAIT Loop
		Bus Error Trap
		TRAP Instructions
		TRACE Trap
		OVFL Trap
		Power Fail Trap
		UNIBUS Bus Request
		Console HALT
		WAIT Loop
			Memory Parity Errors
			Memory Management
			   Fault
			Bus Error Traps
			TRAP Instructions
			TRACE Trap
			OVFL Trap
			Power Fail Trap
			Console Bus Request
			UNIBUS Bus Request
			WAIT Loop

HARDWARE DIFFERENCES - TRAPS
(TRANSPARENT TO SOFTWARE)

LSI11	PDP11/05,10	PDP11/15,20	PDP11/35,40
Priority of internal processor traps, external interrupts, HALT and WAIT;	Priority of internal processor traps, external interrupts, HALT and WAIT;	Priority of internal processor traps, external interrupts, HALT and WAIT;	Priority of internal processor traps, external interrupts, HALT and WAIT;
Bus Error Trap	Bus Error Trap	Bus Error Trap	Memory Parity Errors

WORST CASE REFRESH RATE CALCULATIONS

Graph axes:
- Y-axis: MINIMUM FREQUENCY (in MHz) TO MEET 128 REFRESHES IN 2 M SECONDS
- X-axis: AVERAGE CYCLES PER INSTRUCTION

Vertical lines labeled (left to right):
- 4 Cycles SOP DM0 16 Bit
- 6.4 Cycles Average 16 Bit
- 11 Cycles Average 8 Bit
- 19 Cycles DOP SDM7 16 Bit
- 33 Cycles DOP SDM7 8 Bit

Legend:

```
───────────        .5 Refreshes/instruction
──·──·──            1 Refresh/instruction
─·─·─·─             2 Refreshes/instruction
···─···─            3 Refreshes/instruction
```

No DMA, No Ready Slips, No IACK's, No LBC

A – Worst Case (all DOP's Source and Destination Mode 3), 16-bit mode
    = 5.0 MHz
B – Worst Case, 8-bit mode = 4.5 MHz
C – Average time in 16-bit mode = 2.5 MHz
D – Average time in 8-bit mode = 2.2 MHz
E – All DOP SDM7, 16-bit mode = 2.5 MHz
F – All DOP SDM7, 8-bid mode = 2.2 MHz

AVERAGE REFRESHES PER INSTRUCTION

INSTRUCTIONS	REFRESHES PER INSTRUCTION		
	DEST Mode	16-Bit Mode	8-Bit Mode
XOR & SOP's JMP & JSR	0 - 4	0.5	1
	5 - 7	1.0	2
		16-Bit Mode	8-Bit Mode
	SRC Mode	DEST Mode	DEST MODE
		0-4 | 5.7	0-4 | 5-7
DOP's	0 - 4	0.5 | 1.0	1 | 2
	5 - 7	1.0 | 1.5	2 | 3
CMT, TRAP	0 - 4	1.5	3
BPT, IOT	5 - 7	0.5	1

f = Minimum Operating Frequency (in MHz) to meet N refreshes in X sec.

A = Average # of cycles/instruction
R = Average # of refreshes/instruction

$$f = \frac{N}{X} \; \frac{3 \cdot A}{R} + 1$$

(one cycle = 3 operating frequency periods)

Example: all DOP's source and destination mode 7, 128 refreshes every 2 ms., 16 - bit mode

$$f = \frac{128 \text{ refreshes}}{2 \text{ m sec.}} \; \frac{3 \text{ periods/cycle} \cdot 19 \text{ cycles/instruction}}{1.5 \text{ refreshes/instruction}} + \frac{1 \text{ period}}{\text{refresh}}$$

= 2.5 MHz

T-11 INSTRUCTION EXECUTION TIMES IN I/O CYCLES

XOR & SINGLE OPERAND INSTRUCTIONS
==================================

INSTRUCTIONS	DEST MODE	CYCLES REQUIRED		
		16 BIT MODE	8 BIT MODE	
			WORD INSTRUCTION	BYTE INSTRUCTION
CLR(B),COM(B),	0	1	2	2
INC(B),DEC(B),	1	3	6	4
NEG(B),ROR(B),	2	3	6	4
ROL(B),ASR(B),	3	4	8	6
ASL(B),SWAB,	4	3	6	4
ADC(B),SBC(B),	5	4	8	6
SXT,MFPS,	6	4	8	6
XOR	7	5	10	8
	0	1	2	2
	1	2	4	3
	2	2	4	3
TST(B)	3	3	6	5
	4	2	4	3
	5	3	6	5
	6	3	6	5
	7	4	8	7
	0	1	2	2
	1	2	3	3
	2	2	3	3
MTPS	3	3	5	5
	4	2	3	3
	5	3	5	5
	6	3	5	5
	7	4	7	7

NOTES: 1. XOR and Single Operand Instruction execution times include
instruction fetch, instruction decode, operand fetch,
instruction operation and resultant output (except in Mode
0 and the TST(B) instruction where there is no output).

DOUBLE OPERAND INSTRUCTIONS
==============================

```
****************************************************************
*                                                              *
*      (DOUBLE OPERAND I/O CYCLES) = (SOURCE MODE CYCLES        *
*         INCLUDING INSTRUCTION FETCH) + (DESTINATION MODE TIME) *
*                                                              *
****************************************************************
```

SOURCE MODE TIME

INSTRUCTIONS	SRC MODE	16 BIT MODE	8 BIT MODE	
			WORD INSTRUCTION	BYTE INSTRUCTION
	0	1	2	2
	1	2	4	3
MOV(B),CMP(B),	2	2	4	3
ADD,SUB,	3	3	6	5
BIT(B),BIC(B),	4	2	4	3
BIS(B)	5	3	6	5
	6	3	6	5
	7	4	8	7

(Header above "16 BIT MODE" and "8 BIT MODE" columns: CYCLES REQUIRED)

NOTES: 1. Source Mode times include instruction fetch, instruction
        decode and source operand fetch.

INSTRUCTIONS	DEST MODE	16 BIT MODE	8 BIT MODE	
			WORD INSTRUCTION	BYTE INSTRUCTION
	0	0	0	0
	1	2	4	2
MOV(B),ADD,	2	2	4	2
SUB,BIC(B),	3	3	6	4
BIS(B)	4	2	4	2
	5	3	6	4
	6	3	6	4
	7	4	8	6
	0	0	0	0
	1	1	2	1
	2	1	2	1
CMP(B),BIT(B)	3	2	4	3
	4	1	2	1
	5	2	4	3
	6	2	4	3
	7	3	6	5

The "I/O CYCLES REQUIRED" header spans the 16 BIT MODE, WORD INSTRUCTION, and BYTE INSTRUCTION columns. The "8 BIT MODE" header spans WORD INSTRUCTION and BYTE INSTRUCTION.

NOTES: 1. Destination Mode times include destination operand fetch, instruction operation and resultant output (except in Destination Mode 0 and the CMP(B) and BIT(B) instructions where there is no output).

INSTRUCTIONS	DEST MODE	CYCLES REQUIRED	
		16 BIT MODE	8 BIT MODE
===	===	===	===
JMP	1	1	2
	2	1	2
	3	2	4
	4	1	2
	5	2	4
	6	2	4
	7	3	6
JSR	1	2	4
	2	2	4
	3	3	6
	4	2	4
	5	3	6
	6	3	6
	7	4	8
RTS	NA	2	4
SOB	NA	1	2

NOTES: 1. JMP/JSR Destination Mode Ø is an illegal instruction that
           traps to vector location 1Ø.

        2. JMP execution times include instruction fetch, instruc-
           tion decode, operand fetch and loading of the PC.

        3. JSR execution times include instruction fetch, instruc-
           tion decode, operand fetch, pushing the linkage register
           onto the stack and loading the PC.

        4. RTS execution times include instruction fetch, instruc-
           tion decode, loading the PC and popping the stack and
           loading the linkage register.

        5. SOB execution times include instruction fetch, instruction
           decode, decrementing the count register, testing for zero
           and branching if necessary
           (NOTE: Whether or not a branch is taken does not affect
           the execution time).

BRANCH, TRAP & INTERRUPT INSTRUCTIONS
===

| INSTRUCTIONS | DEST MODE | CYCLES REQUIRED | |
		16 BIT MODE	8 BIT MODE
BR,BNE,BEQ, BPL,BMI,BVC BVS,BCC,BCS, BGE,BLT,BGT, BLE,BHI,BLOS, BHIS,BLO	NA	1	2
EMT,TRAP, BPT,IOT	NA	7	9
RTI	NA	3	5
RTT	NA	3	5

NOTES: 1. Branch instructions execution times include instruction fetch, instruction decoding, doubling the offset, testing the conditions and adding the offset to the PC if the conditions are met (NOTE: Whether or not a branch is taken does not affect the execution times).

2. Trap instructions execution times include instruction fetch, instruction decode, pushing the PS and PC onto the stack, loading the PC with the contents of the vector location and loading the PS with the contents of the vector location plus two.

3. Return from interrupt instructions execution times include instruction fetch, instruction decode and popping the PC and PS from the stack.

MISCELLANEOUS & CONDITION CODE INSTRUCTIONS
==

INSTRUCTIONS	DEST MODE	CYCLES REQUIRED	
		16 BIT MODE	8 BIT MODE
===	===	===	===
HALT	NA	5	6
WAIT	NA	1 then loop	2 then loop
RESET	NA	1	2
NOP	NA	1	2
CLC,CLV,CLZ, CLN,CCC,SEC, SEV,SEZ,SEN, SCC	NA	1	2
MFPT	NA	1	2

NOTES: 1. HALT execution times include instruction fetch, instruction decode, writing the PC into location 4, writing the PS into location 6, loading the PS with 340 and loading the PC with the RESTART address.

2. WAIT execution times include instruction fetch, instruction decode, pulsing PI to sample the interrupt lines and doing a REFRESH cycle if REFRESH is on. (NOTE: If no interrupt lines were sensed by the T-11 to be asserted during the PI pulse, the WAIT instruction will cycle in a 2 micro-instruction loop (if REFRESH is on the loop will be 2 1/3 micro-instructions max) pulsing PI. The looping will continue until an interrupt line is sensed by the T-11 to be asserted.)

3. RESET execution times include instruction fetch, instruction decode, the assertion of -BCLR and the writing of DAL<15:0> into the MODE register.

4. NOP execution times include instruction fetch, instruction decode and idle time.

5. Condition Code instructions execution times include instruction fetch, instruction decode and the setting or resetting of the appropriate status flags in the PS.