TITLE: CHOICE OF LOGIC

PDP-11/40 Tech Memo #19

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ABSTRACT

The purpose of this memo is to aid us in our decision on the technology to be used in the 11/40 hardware implementation. With a goal of 200 ns maximum cycle time, for register-to-register instruction, the need for circuits faster than the 74 hundred and 74H hundred TTL integrated circuits (used in our present machine) becomes imperative.

We presently have two choices. The first one is the Schottky 74S hundred TTL which is a fast version of the 74H hundred series. The second is the emitter coupled logic family (ECL) which is a non-saturated logic. Although the ECL family offers an advantage in speed, the 74S hundred logic has been chosen in this memo for the 11/40 hardware due to technical, cost, and product availability reasons. Those reasons are discussed with some detail in the following sections of this memo.

TABLE OF CONTENTS

1.0 INTRODUCTION

Choosing a technology today for the 11/40 project is not a straight forward task, especially if the exact organization and goals are not set for that machine. However, based on the information I have been gathering for the last few weeks, I have tried in this report to draw some facts and conclusions about the technology today and what I think is the way to go for the 11/40 hardware implementation.

2.0 WHICH ECL FAMILY TO CONSIDER?

Motorola is the only company today producing a fully developed line of Emitter Coupled Logic. Thus, it is logical to choose Motorola's MECL for consideration in the 11/40 project. There are four different lines of MECL which we are considering now, MECL II, II½, III, and 10K series. Table 1 shows the comparison between these lines and the three TTL family lines with respect to gate speed, cost and power dissipation. Since speed is the primary reason why ECL logic is considered for the 11/40 project, then MECL II should not be considered for the 11/40 implementation, especially in its fast sections.

For cost reasons, I think we should drop MECL III from the picture since it requires multilayer boards. According to a survey made by Dave Nevala, of our Mechanical Engineering Department, multilayer boards can cost roughly 3 times that of our standard double sided boards. This does not include the initial capital equipment to set up a manufacturing facility or the associated problems. Thus, with MECL III chip cost approximately 3 times that of the 74S series logic, or the other MECL families, it is estimated that a system built by MECL III can cost as much as 3 times that built by 74S hundred logic, but with a 3-fold gain in speed.

MECL II½ is available today, and we have only 3 types of nor gates and one type of D flip-flop. By the end of the year, there will be a dual one-bit full adder chip, and a quad two input nor gates, plus 2 other level translator chips. As far as future MSI chips are concerned, they will be made in the 10K series which will be introduced in January, 1971. The 10K series is about 15% slower than MECL II½ and dissipates about half the internal power, thus making it feasible to build MSI chips from. See attached Tables 2 and 3 for chips introduction in 1971.

LOGIC FAMILY	PRICE/QUAD GATE 1971 ($)	1972 ($)	MAX. PROPGN. DELAY @ FAN OUT =0-10 and TA =0°C -75°C	MAX. AVG. DC. POWER DISSIPATION PER CIRCUIT
74 hundred	.20	.19	20 ns	20 mw
74H hundred	.25	.23	10 ns	35 mw
74S hundred	.70	.48	7 ns	32 mw
MECL II (100K quantity)	.57	.44	14 ns	40 mw (1.5K internal termination)
(1 mil quantity)	.50	.38		
MECL II½ (100K quantity)	.68	.52	5 ns (50Ω termination to -2.0 V)	40 mw (no termination)
MECL II½ (1 mil quantity)	.60	.45	7 ns (600Ω termination to -5.2 V)	190 mw (50Ω termination to -2.0 V)
MECL 10K series (100K quantity)	.50	.40	6.0 ns (50Ω termination to -2.0 V)	20 mw (no termination)
MECL 10K series (1 mil quantity)	.45	.35	8.0 ns (600Ω termination to -5.2 V)	160 mw (50Ω termination to -2.0V)
MECL III (100 quantity)	2.00	1.12	2.0 ns (50Ω to -2.0 V)	75 mw (no termination) 215 mw (50Ω termination to -2.0 V)

NOTE: I don't have specs on either the MSI 74S hundred series or 10K series, but I have been told that it is expected that typical propagation delay for a gate in the MSI 74S series and the 10K series is about 2.25 ns and 2.0 ns respectively. A typical gate delay in a 74 hundred series MSI chip is 6.0 ns.

TABLE 1

MECL 10K SERIES INTRODUCTIONS IN JANUARY 1971

	GATES
MC10101	Quad 2 Input with Strobe OR/NOR
MC10102	Quad 2 Input NOR
MC10105	Triple 2 Input OR/NOR
MC10106	3-3-4 Input NOR
MC10107	Triple Ex OR, Ex NOR
MC10109	4-5 Input OR/NOR
MC10119	3-3-3-4 OR AND
	LINE RECEIVERS
MC10115	Quad OR
MC10116	Triple OR/NOR
	COMPLEX FUNCTIONS
MC10181	4 Bit AU
	MEMORY ELEMENTS
MC10130	Dual D Latch
MC10131	Dual D Master-Slave Flip-Flop

TABLE 2

MECL 10K SERIES INTRODUCTIONS BY JUNE 1971

GATES

MC10110	Dual 3 Input 3 Line Driver
MC10118	Dual 2 Wide 2-3, 3-3 Input OA
MC10120	Dual 2 Wide 2 Input AO/AOI
MC10121	3-3-3-2 OA/OAI

COMPLEX FUNCTIONS

MC10160	9 Bit Parity Checker
MC10161	Three Bit Decoder w/Two Enables 1 of 8 Low
MC10162	Three Bit Decoder w/Two Enables 1 of 8 High
MC10163	Twisted Pair to 8 Line De-Multiplexer
MC10164	8 Line Multiplexer
MC10179	Look-Ahead Carry Block

MEMORY ELEMENTS

MC10133	Quad D Latch
MC10134	Dual D Latch
MC10135	Dual J-K Master Slave Flip-Flop
MC10136	4 Bit Universal Counter
MC10139	256 Bit Fusible Link ROM
MC10140	64 Bit RAM
MC10141	4 Bit Universal Shift Register

TABLE 3

3.0 TTL VERSUS ECL

The following six sections discuss, in some detail, the difference between the two logic families and are, in my opinion, listed in the order of importance for the 11/40 project. Conclusions and deductions are based on the information available to me as of this date, such as specs, product introduction, and costs.

3.1 NOISE IMMUNITY AND FIGURES OF MERIT*

Tables 4, 5, and 6 show the guaranteed noise margin and figures of merit for both the logic families under consideration with different supply voltages and temperatures. However, there is a problem with ECL when mixing gates of different supply voltages and temperatures.

According to Motorola specs, the following figures show the trends of output voltages and threshold voltages versus supply voltage and temperature for MECL II logic.

$\frac{\Delta V}{\Delta T}$ = 1.5 MV/°C. where ΔV is the change in output voltage or threshold voltage, and ΔT is the change in temperature

$\frac{\Delta V \text{ out (0)}}{\Delta V \text{ supply}}$ = 1/4 max.

$\frac{\Delta V \text{ threshold}}{\Delta V \text{ supply}}$ = 1/8 max.

Calculations showed that with ΔT of 25°C and 250 MV differences in supply voltages between two MECL II gates reduce the figure of merit to (at best) equal that of the 74S hundred series. Any further variations in the supply voltage or temperature will deteriorate the noise margin.

* Figure of Merit = F = $\frac{\text{worst case noise margin (NM)}}{\text{output voltage swing}}$

As far as the MECL II½ is concerned, the guaranteed noise margin, according to the specifications, is equal to that of MECL II provided that the output termination is no less than 600 ohms at a maximum fan out of eight unit loads. It is also expected that the noise margin will drop further if lower terminations are used.

Finally, the exact noise immunity margins for the 10K series are not specififed yet and from what I gathered, it will be probably 25 mv less than that of MECL II½ and that makes it even less attractive.

GUARANTEED NOISE MARGIN (NM) AND FIGURE OF MERIT (F)

T2L (T_A 0° -75°C and V_{CC} 4.75V-5.25V)

74 hundred NM = 400 mv, F = .133

74H hundred NM = 400 mv, F = .133

74S hundred NM = 300 mv, F = .10

TABLE 4

MECL II WORST LEVELS, NOISE MARGIN (NM), AND FIGURE OF MERIT F

(V_{EE} = -5.2V)

AMBIENT TEMPERATURE	75°C	25°C	0°C
V_{IH} max.	- .615V	- .700V	- .740V
V_{OH} max.	- .615V	- .700V	- .740V
V_{OH} min.	- .775V	- 850V	- .895V
V_{IH} min.	- .950V	-1.025	-1.070V
V_{IL} max.	-1.260V	-1.325V	-1.350V
V_{OL} max.	-1.440V	-1.500V	-1.525V
V_{OL} min.	-1.760V	-1.800V	-1.830V
V_{IL} min.	-5.20V	-5.20V	-5.20V
NM	175 mv	175 mv	175 mv
F	.20	.20	.20

(See Table 1 for definitions)

TABLE 5

MECL II WORST LEVELS, NOISE MARGIN (NM), AND FIGURE OF MERIT F

(V_{EE}= -4.75.)

AMBIENT TEMPERATURE	75°C	25°C	0°C
V_{IH} max.	- .608V	- .693V	- .734V
V_{OH} max.	- .608V	- .693V	- .734V
V_{OH} min.	- .768V	- .843V	- .888V
V_{IH} min.	- .896V	- .971V	-1.016V
V_{IL} max.	-1.206V	-1.271V	-1.296V
V_{OL} max.	-1.328V	-1.388V	-1.413V
V_{OL} min.	-1.648V	-1.688V	-1.718V
V_{IL} min.	-4.75V	-4.75V	-4.75V
NM	122 mv	117mv	117 mv
F	.16	.155	.155

(See Table 7 for definitions)

TABLE 6

DEFINITIONS

$V_{IH\ max.}$ = maximum input high level

$V_{OH\ max.}$ = maximum output "1" or high level

$V_{OH\ min.}$ = minimum output "1" or high level

$V_{IH\ min.}$ = minimum input high level threshold

$V_{IL\ max.}$ = maximum input low level threshold

$V_{OL\ max.}$ = maximum output "0" or low level

$V_{OL\ min.}$ = minimum output "0" or low level

$V_{IL\ min.}$ = minimum input low level

V_I = input voltage

V_O = output voltage

NM = worst case noise margin

$$F = \frac{NM}{\text{output voltage swing}}$$

TABLE 7

3.2 WIRING RULES

Wiring and termination rules, I think, are more of a problem in using MECL II½ or 10K series logic than the 74S series logic. In using big circuit boards, the wiring problem can basically be split into two areas; the first one is wiring internally inside the board, and secondly, back panel wiring.

3.2.1 WIRING INSIDE THE BOARD

This problem can be fairly controllable. By specifying etch separation, having some form of ground plane, careful partitioning and sacrificing some chip density, we can reduce the crosstalk problem inside the board to a minimum for either one of the two logic families. The only problem left to be solved is the reflection problem where, in the case of high speed logic, the interconnection wiring can lead to a considerable time relative to the rise and fall time of the signal.

T. I. did some experiments and theoretical analysis and found that the 74S series logic can drive 3 feet of wire of characteristic impedance, ranging from 50 ohms and up, without a need for any terminations and without having serious reflection problems. However, judging from the results and considering the worst case of everything, such as low supply voltage and high output impedance, I expect some problem in driving low line impedance of 100 ohms or less for wire lengths over 6 inches when the driving output is going high. Nevertheless, we can probably control the line impedance very easily to be above 100 ohms with our double sided boards.

As far as the ECL family is concerned, resistive termination is required on all clock lines longer than 2 or 3 inches. Also, when speed is necessary, other signal lines have to be terminated for the above lengths. This will add to the cost and power dissipation of the system plus further reducing the board density by as

low as 25%, assuming that half of the logic needs to be terminated and that 8 resistors occupy a one chip space.

3.2.2 BACK PANEL WIRING

This is the second major problem we have to deal with. In this case, we will require a more strict wiring rule since there is little, or no control to how the wires are running or stacked on each other, and crosstalk noise will be the primary limitation on wire lengths, and reflection is the second limitation. I would expect to have equal problems in wiring rules in both families considering the rise and fall time are the same for both lines of logic. Termination will be required on both lines; resistive for the ECL family and diodes for the S series logic. On one hand, the resistive termination can give rise to lesser crosstalk noise in the ECL family, but on the other hand, ECL can have smaller figures of merit than the S series logic especially if the lines are terminated with heavy resistive loads.

One advantage ECL has over the S series logic in case of driving long lengths of wires, is that ECL, according to Motorola, is capable of driving up to 20 feet of twisted wires pseudo differentially at the rate of 100 MC with the aid of special line receivers at the end of the lines. While the S series at best, with the aid of a special driver, can drive twisted wires open ended. I expect the need for such long runs to be very small, especially if big boards and MSI chips are used. Wiring rules for the 74S hundred series will be generated in the near future, with the completion of certain experiments in the laboratory.

3.3 COMPATIBILITY PROBLEM

The 74S hundred series is compatible with the 74 hundred and 74H hundred series electrically and pin by pin, including the MSI chips. However, in the MECL family, we have a problem. There is a 125 mv difference between threshold level of the 10K series and that of MECL 11½.

Certain loading and wiring rules have to be followed in mixing both families. Those rules are rules of thumb and as of this date are not guaranteed or written in the specifications. Also, voltage translators are required between the MECL logic and the outside world which is today built in TTL. These incompatibility problems will add to the cost and probably harm the speed and ease of design.

3.4 POWER SUPPLY REQUIREMENTS AND COOLING

The ECL logic requires first of all, a different voltage than the T2L logic and, secondly, the average DC power dissipation of ECL logic runs higher than any of the TTL logic family, especially if terminations are used on the ECL outputs. (See Table 1.)

I predict that the power requirements for the ECL system using MECL II½, will be at least double that of the 74S family. This estimate is based on the assumption that at least half of the MECL II½ gates used require an average termination of 150 ohms while the other half remains unterminated. (Refer to Table 1.) Also, ECL imposes a stricter supply voltage change requirement between chips than the TTL family does if decent noise margins are required to be maintained. It is advisable that no more than 250 mv should be the supply voltage difference between the ECL chips as opposed to 500 mv in the TTL family.

To maintain equal figures of merit in the two family lines, it is recommended, along with the above voltage requirements, to maintain temperature difference between ECL chips to no more than 25°C, which in turn makes the cooling task even harder, especially in such high power requirements and the possibility of different resistive terminations on different gates. It is predicted that roughly 200 mw of power dissipation differential between chips can result in 20°C temperature difference.

As far as the TTL family is concerned, their noise margin is guaranteed over 0° - 75°C temperature range

with voltage regulation of ± 5% on the +5V supply.

Finally, it is essential to have 2 different ground planes if ECL is used as it will be necessary to separate ECL ground from the TTL ground since ECL noise margin is less than ½ that of TTL and will not be able to tolerate the amount of ground noise as TTL can.

3.5 SYSTEM SPEED AND COST

Given a technology for implementation, system cost and performance, I think, are very much dependent on the amount of MSI or LSI chips used in the hardware.

For any given portion implemented by an MSI chip, rather than standard gates of same technology, T.I. predicts 30 to 50% reduction in cost, plus 80% reduction in interconnections. Moreover, power dissipation is halved and speed is increased by at least 25%.

With today's components in TTL, MSI, and S series logic, the system speed, I believe, will be roughly 50% slower than if it was implemented with today's MECL II and MECL II½ components and at cost of 50% to 30% of that of the ECL system

With the new S series MSI chips and gates, some of which will be available by the end of this year, the system speed will become very close to that built by today's MECL II½ logic with less cost. However, ECL technology will have the advantage in speed on the above S series system if the 10K series MSI line is used, but I doubt if it is going to be less expensive. The reason for the speed difference is that it is expected that the propagation delay of gates in an ECL MSI chip is about 25% faster than that of the S series MSI chips. Also, the availability of both sexes at the output of some ECL gates and the feasibility of collector ORing with some strict wiring rules do help in saving some time especially in the control section.

3.6 SECOND SOURCING AND AVAILABILITY PROBLEMS

Second Sourcing has always been an important issue in considering a product. As of this date, none of the MECL product, or the S series product has been second sourced. However I think that the S series has a better chance of being second sourced than the MECL series for the following reasons:

a) Motorola MECL II has been in the market for the last 4 years, and so far it is still single sourced.

b) Big companies showed some serious intention for second sourcing the S series logic, such as National Semiconductor and Sylvania, while smaller companies, which we might not depend on anyway, showed the same interest in MECL II. Those companies I am referring to are Signetics and Stewart Warner.

c) To my knowledge, no company today showed the intention of second sourcing MECL II½ or the 10K series.

d) The S series MSI chips are closer to reality than the 10K series since T.I. started working on it last April and some preliminary specs will be available to DEC in the next two weeks (see Table 8); while Motorola, only a few weeks ago, has started looking into their plans for the 10K MSI series and preliminary specifications will not be available until the end of this year.

4.0 CONCLUSIONS

Based on the above facts, I do recommend choosing the 74S hundred logic over the MECL family to be used in the high speed portions of the 11/40 processor. Also, enhancing the above choice is the fact that DEC already

has the knowledge, experience, and the testing facilities for the TTL family. Double sided quad boards should be aimed at to fulfill our modules need and the possibility of additional wiring connections between adjacent board, other than the back plane wiring, should be considered to further reduce the wiring traffic. My guess is that the CPU of the 11/40 will use approximately 15 of those boards and nearly half of the logic will be 74S hundred including MSl chips if available.

5.0 REMARKS

ECL technology should not be abandoned entirely from the 11/40 project. One application, which I can think of now, and where speed can be of importance, is the memory buffer section. MECL can really pay here to get to memory cycle time of below 100 ns for a small percentage increase in the overall system cost. Also, due to the relative small size of the memory buffer, its environment can be easily controlled, and we will have a good chance of keeping this section under good voltage, temperature, and wiring conditions.

74S DEVICE AVAILABILITY

DEVICE	PINS	FUNCTION	SAMPLES	STOCK
74S00N	14	Quad 2-Input NAND	Complete	Complete
74S20	14	Dual 4-Input NAND	Complete	Complete
74112N	16	Dual J-K Net Flip-Flop	Complete	9/1
74S22N	14	Dual 4-Input NAND (O/C)	Complete	9/20
74S03N	14	Quad 2-Input NAND (O/C)	Complete	9/23
74S04N	14	Hex Inverter	9/3	10/1
74S10N	14	Triple 3-Input NAND	9/22	10/20
74S11N	14	Triple 3-Input AND	9/18	10/16
74S40N	14	Dual 4-Input NAND Buffer	9/7	10/16
74S140N	14	Dual 4-Input NAND Driver	9/14	10/16
74S64N	14	4-Wide 4-2-2-3 AOI	9/21	10/26
74S113N	14	Dual J-K NET Flip-Flop	10/20	11/17
74S114N	14	Dual J-K NET Flip-Flop	10/20	11/17
74S74N	14	Dual D-Type ET Flip-Flop	10/26	11/23
74S157N	16	Quad 2 Multiplexer (true)	11/20	12/18
74S158N	16	Quad 2 Multiplexer (comp)	11/30	12/18
74S168N	24	4-Bit ALU	12/23	1/27
74SXXN	16	4-Bit Shift Register	1/22	-
74S169N	-	Decade Counter	2/11	

TABLE 8