TITLE: PDP-11/40 TECHNICAL MEMO INDEX & ABSTRACTS

PDP-11/40 Tech Memo #1

AUTHOR: Dick Clayton
DATE: September 25, 1970, pages
REVISION: None OBSOLETE: None
INDEX KEY: Index
Abstract

DISTRIBUTION KEY: PDP-11/40 Group
PDP-11/20 Group
PDP-11 Coordinating Committee
PDP-11 Master List

ABSTRACT

This memo consists of the Index, the Abstract, and the Alphabetical Cross-Reference of Index Keys for all PDP-11/40 Technical Memos.

Copies of individual memos are obtainable from the secretary of the PDP-11/40 Engineering Group, Doris Covey, as of the writing of this memo.

PDP-11/40 INDEX

OBSOLETE	PDP-11/40 Tech. Memo #	TITLE	DATE
	1	Index & Abstracts	9-25-70
	2	Guidelines for 11/40 Tech Memos	9-25-70
	3	PDP-K Memo 3; Extension of PDP-11 Address Space	3-12-70
	4	PDP-K Memo 4; Instruction Set for PDP-K	2-20-70
	5	PDP-K Memo 2; Extension of PDP-11 Instruction Set	1-21-70
	6	Non existent	
	7	" "	
	8	" "	
	9	" "	
	10	" "	
	11	Data Format Conventions for PDP-11/40	6-10-70
	12	PDP-11/40 Addressing Modes	6-29-70
	13	A Microprogrammed 11/40 CPU	6-30-70
	14	Register Layout for 11/40 and up	7-14-70
	15	11/60 Instruction Set	6-17-70
	16	Floating Point Format (360)	8-21-70
	17	The Repeat Instruction	9-2-70
	18	The Execute Instruction	9-21-70
	19	Choice of Logic (74S)	9-25-70

CROSS-REFERENCE

ALPHABETICAL LISTING OF INDEX KEYS

CROSS-REFERENCE

ALPHABETICAL LISTING OF INDEX KEYS

(continued)

CROSS-REFERENCE

ALPHABETICAL LISTING OF INDEX KEYS

(continued)

INDEX KEY	MEMO #
Repeat Conditions	17
Repeat Count	17
Resumption	17
Segmentation	3-1
Technical Memoranda	2

TITLE: GUIDELINES FOR PDP-11/40 TECHNICAL MEMORANDA

PDP-11/40 Tech Memo #2

AUTHOR: Dick Clayton
DATE: September 25, 1970, 4 pages
REVISION: None OBSOLETE: None
INDEX KEY: Technical Memoranda
Memoranda Formats
Format

DISTRIBUTION KEY: PDP-11/40 Group
PDP-11/20 Group
PDP-11 Coordinating Committee

ABSTRACT

This memo describes the conventions and purposes of the PDP-11/40 Technical Memoranda Set. Suggested formats and distributions are presented.

TITLE: EXTENSION OF PDP-11 ADDRESS SPACE

PDP-11/40 Tech Memo #3 (PDP-K Tech Memo #3-1)

AUTHOR: Robert Gray
DATE: March 12, 1970, 23 pages
REVISION: 1 OBSOLETE: TECH MEMO #3
INDEX KEY: Memory
Paging
Segmentation

DISTRIBUTION KEYS:

ABSTRACT

This memo discusses the limited address space in the PDP-11 architecture.

The PDP-11 16-bit processor can address a maximum of 32K (indirect or indexed) 16-bit words. A 32-bit version of the PDP-11 could address 16K 32-bit words.

This aspect of the present PDP-11 architecture is examined as a potential problem in larger versions (32-bits) of a proposed PDP-11 family. The 16K limit is compared with medium size computers offered by other manufacturers. It is also compared with the expected user requirements of machines in this performance category. Finally, this memo discusses briefly the limit and advantages of two possible memory expansion techniques: Paging and Segmentation.

It is concluded that the 16K limit in a 32-bit PDP-11 would be a severe competitive handicap. It is further concluded that neither paging nor segmentation offers an efficient way to run procedures that exceed 16K 32-bit words

TITLE: PDP-K INSTRUCTION SET

PDP-11/40 Tech Memo #4

AUTHOR: Ad van de Goor
DATE: February 20, 1970, 32 pages
REVISION: None OBSOLETE: None
INDEX KEY: Instruction Set
OP Code
Data Types

DISTRIBUTION KEYS:

ABSTRACT

An instruction set for an 18-bit computer[1] is proposed. It combines the best features of the PDP-11's architecture and the PDP-10's instruction set.

For several reasons, an 18-bit computer was considered superior; it solves both the OP code and address space problems of a 16-bit computer. In addition, it is a better data base in two important areas. Pulse Height Analysis (PHA) programs have proven the need for 18 bits. Also, the 36-bit floating point representation has much wider acceptance, due to its superiority of 32-bit formats.

[1] i.e., a computer with a word length of 18-bits.

TITLE: Extension of PDP-11 Instruction Set

PDP-11/40 Tech Memo #5 (PDP-K Tech Memo #2)

AUTHOR: Ad van de Goor
DATE: January 21, 1970, 24 pages
REVISION: NONE OBSOLETE: NONE
INDEX KEYS: Instruction Sets
OP Code Space
Modes
Stack Operations

DISTRIBUTION KEYS:

ABSTRACT

This PDP-K Memo (#2) describes 4 methods of expanding the instruction set of the PDP-11. They are:

a) Stack instructions; operands are picked up from and results returned to the stack.

b) Flag word instructions: A single instruction indicates that the instruction space is to extend to the next word. This allows at least 16-bits free for new instruction.

c) Mode; a mode bit controls the decoding of instruction to be from one of two sets.

d) Use of Mul/Divide space; use the remaining two undefined 11/20 OP code spaces for new instructions.

The Mul/Divide solution (d) appears to be preferable.

TITLE: DATA FORMAT CONVENTIONS FOR PDP-11/40

PDP-11/40 Tech Memo #11

AUTHOR: Ad van de Goor
DATE: June 10, 1970, 6 pages
REVISION: None
OBSOLETE: None
INDEX KEYS: Data Formats
Numbering Sequences

DISTRIBUTION KEYS: PDP-11 Coordinating Committee
PDP-11/40 Group
Alan Kotok
Richard DeMorgan

ABSTRACT

This memo is concerned with certain data formats being proposed for the PDP-11/40. It is proposed that multiple word data be stored as most significant data before least significant data. The proposed formats have the property of being compatible with what is considered standard in the computer industry, and people's intuition. It is, however, not compatible with some PDP-11/20 software conventions.

The reasons for the proposed PDP-11/40 formats are given together with guidelines for future decisions. Although issue is taken with the bit and byte numbering schemes used in the PDP-11/20, it is proposed that these remain unchanged because of hardware and documentation reasons.

TITLE: PDP-11/40 ADDRESSING MODES

PDP-11/40 Tech Memo #12

AUTHOR: Ad van de Goor
DATE: June 29, 1970, 7 pages
REVISION: None OBSOLETE: None
INDEX KEYS: Addressing Modes
Indexing
List Addressing

DISTRIBUTION KEYS: PDP-11/40 Group Bruce Delagi
PDP-11 Coordinating Com. Larry McGowan
Dave Knight Jim Bell
Ron Brender Jack Richardson
Jeff Scott

ABSTRACT

The auto decrement deferred mode "@-(R)" as implemented on the PDP-11/20 has been found to be of very little use. In all the PDP-11 programs the author has seen, it has been used only twice.

Three alternative addressing modes are discussed to replace the "@-(R)" mode. It is concluded that the adjusting index mode "(R)A" was the most promising.

The adjusting index mode "(R)A" is very similar to the regular index mode "A(R)" except for the computation of the effective address "EA".

For A(R), the EA is: EA= (R) + A

For (R)A, the EA is: EA= A + L * (R)
where L= length of data in bytes

TITLE: A Microprogrammed 11/40 CPU

PDP-11/40 Technical Memo #13

AUTHOR: Rony Elia-Shaoul
DATE: June 30, 1970, 14 pages
REVISION: None OBSOLETE: None

INDEX KEYS: Hardware

DISTRIBUTION KEYS: Ad van de Goor, Bob Gray, Dennis O'Connor, Dick Lewis, Joe Mangiafico, Jim Murphy, Jim Bell, Bruce Delagi, Don Vonada, Gerry Butler

ABSTRACT

An eight bit microprogram CPU was looked into and was partially designed and analyzed with different existing components. The purpose of the above project was to aid us in arriving at a valid estimate, as far as speed, cost, packaging, and power dissipation for a microprogram 11/40 CPU with using different types of semiconductor components. The flow diagram used for such an implementation is shown in Figure 1. A breakdown of each of the sections drawn in the diagram as far as cost, technology, speed, power dissipation, and packaging, is analyzed in this report. Finally, a similar estimate on a microprogram 11/40 CPU is made using today's components.

It is concluded that present microprogrammed technology would be more expensive until about 1972. A speed penalty of at least 50% would be paid by a microprogrammed system. Microprogramming offers significant advantages in packaging density and design flexibility.

TITLE: REGISTER LAYOUT FOR 11/40 AND UP

PDP-11/40 Tech Memo #14

AUTHOR: Ad van de Goor
DATE: July 14, 1970, 9 pages
REVISION: None OBSOLETE: None
INDEX KEY:S Register Layout
Overlapping
Register-Code Overlay

DISTRIBUTION KEYS: PDP-11/40 Group
PDP-11 Coordinating Committee
Bruce Delagi

ABSTRACT

Because the 11/40 might, and bigger versions of the PDP-11 family will, have 32-bit integer and floating point arithmetic capabilities, the need for more general purpose hardware registers is quite clear.

The competition of the bigger PDP-11's (e.g., PDP-11/60) has typically sixteen 32-bit general purpose registers.

Four methods of adding, in a compatible way, new registers to the PDP-11/20 architecture are discussed. The last method, section 1.4 "The Disjoint Scheme" is preferred because it has most of the advantages and satisfies implementation constraints. This scheme provides six double word format registers (32-bits, DØ-D5) which are independent of the standard single word format registers. Both the single and double registers overlay core to allow program manipulation of their contents.

TITLE: PDP-11/60 INSTRUCTION SET

PDP-11/40 Tech Memo #15

AUTHOR: Ad van de Goor
DATE: June 17, 1970
REVISION: None
OBSOLETE: None
INDEX KEYS: Instructions
Instruction Formats
Data Formats
Addressing Modes
Interrupts
Traps

DISTRIBUTION KEYS: PDP-11 Coordinating Committee
11/40 Group
11/60 Architecture Design Review Committee

ABSTRACT

This memo describes the proposed modification to the 11/20 instruction set to allow the creation of the 11/60 instruction set. It is proposed that BISB, BICB, and BITB be placed in a two word "flagged" form of instruction and that the instruction set be expanded using this and the Mul/Divide space. The memo covers modification of the addressing modes, multiple word arithmetic instruction, multiple shift instruction, floating point instructions, and 11/20 instructions.

Paging and segmentation are not covered and are deferred to a future memo.

TITLE: PDP-11/40 FLOATING POINT FORMAT

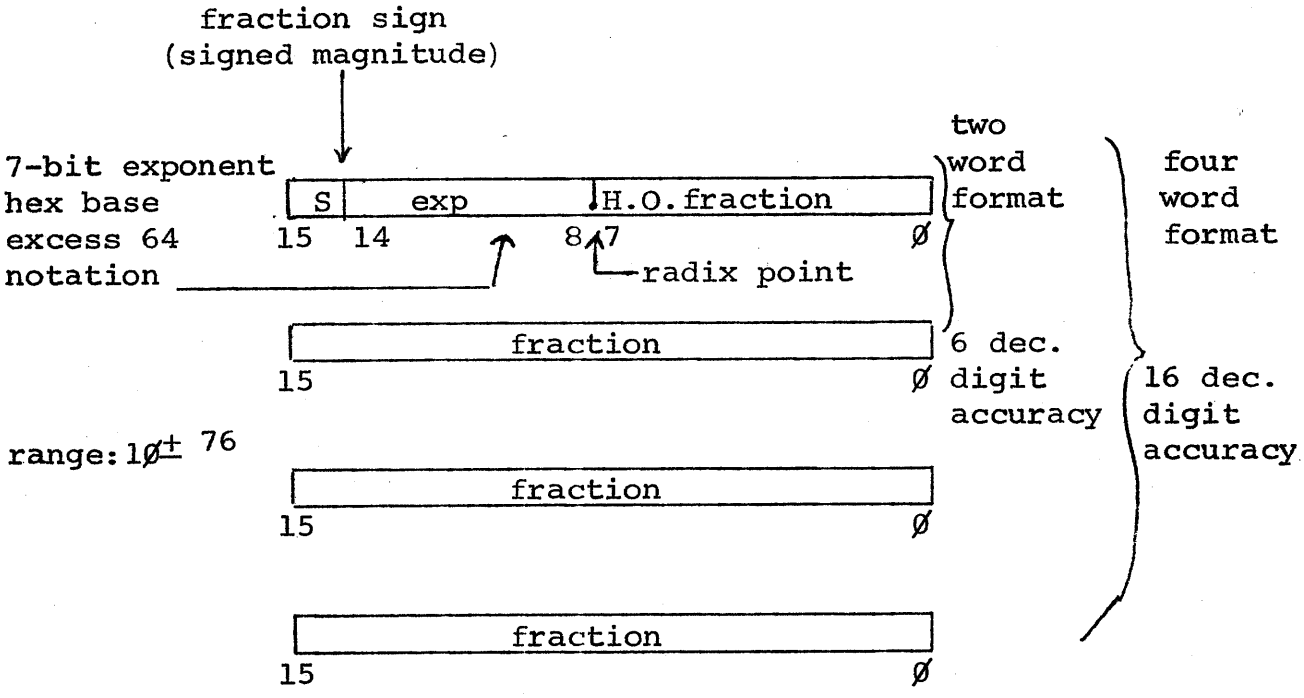
PDP-11/40 Tech Memo #16

AUTHOR(S): Ad van de Goor
Jim Murphy
Hank Spencer
DATE: August 21, 1970, 17 pages
REVISION: None OBSOLETE: None
INDEX KEYS: Floating Point Formats Exponent Base
Radix Point Conversion

DISTRIBUTION KEYS: PDP-11 Coordinating Committee
PDP-11/40 Group

ABSTRACT

It is proposed that the PDP-11 adopt 360 2 and 4 word format. The memo examines the 360, CDC STAR, Byte exponent with quad normalization, and 9-bit exponent formats. A primary assumption is that $\pm 10^{76}$ range is needed in the format.



TITLE: THE REPEAT INSTRUCTION

PDP-11/40 Tech Memo #17

AUTHOR: Ad van de Goor
DATE: September 2, 1970, 11 pages
REVISION: None
OBSOLETE: None
INDEX KEYS: Repeat Count
Repeat Conditions
Resumption
Reentrance
Interruptability

DISTRIBUTION KEYS: PDP-11/40 Group
Bruce Delagi
Jud Leonard
Richard DeMorgan
Jeff Scott
Jack Burness

ABSTRACT

The desirability of a conditional repeat instruction has been demonstrated on several occasions. The repeat instruction provides for the shortest possible program loop (namely a single instruction), besides that it seems to have a big market appeal.

Because this instruction is considered for the 11/25, the possible 11/40 implementations are considered for compatibility reasons.

The problems with this instruction are two-fold:

1) How to implement it, considering implementation cost and required OP code space.

2) Which instructions cannot be repeated, or repeated with restrictions.

It is concluded that a format allowing small counts (0-8) to be specified, within the instruction, is desirable. Using a skip technique to separate end conditions seems reasonable. At this time there does not seem to be a clear concensus as to the way repeat should operate. A revision of this memo, defining the 11/40 final choice, is needed.

TITLE: THE EXECUTE INSTRUCTION

PDP-11/40 Tech Memo #18

AUTHOR: Ad van de Goor
DATE: September 21, 1970, 7 pages
REVISION: None OBSOLETE: None
INDEX KEYS: Execute, Interruptability, Addressing Modes
DISTRIBUTION KEYS: PDP-11/40 Group
PDP-11/60 Architecture Review Committee
Jud Leonard
Jeff Scott
Richard DeMorgan

ABSTRACT

The use of the execute "XCT" instruction is discussed and from that an implementation derived.

Interruptability considerations resulted in a non-interruptable execute sequence. (This was the simplest solution hardware wise.)

Considerations of the addressing modes used by the XCT instructions led to the rule that when the -(R), (R)+ and (R)A modes are used, the instruction to be executed is "thought of" as being one 16-bit word long, independent of the actual length of the instruction to be executed.

In order to have no surprises or side effects in the instructions to be executed, the machine is required to have two program counters:

1) The PC, which is the regular program counter. Upon completion of the XCT sequence, it usually points to the instruction following the XCT instruction.

2) The dummy program counter "DPC", which is only used for the address computation in the instruction to be executed.

The only instructions which cannot be executed are Execute and Repeat.

TITLE: CHOICE OF LOGIC

PDP-11/40 Tech Memo #19

AUTHOR: Rony Elia-Shaoul
DATE: September 29, 1970, 17 pages
REVISION: NONE OBSOLETE: NONE
INDEX KEY: Hardware
DISTRIBUTION KEY: Engineering Committee
11/40 Group
11/40 General List

ABSTRACT

The purpose of this memo is to aid us in our decision on the technology to be used in the 11/40 hardware implementation. With a goal of 200 ns maximum cycle time, for register-to-register instruction, the need for circuits faster than the 74 hundred and 74H hundred TTL integrated circuits (used in our present machine) becomes imperative.

We presently have two choices. The first one is the Schottky 74S hundred TTL which is a fast version of the 74H hundred series. The second is the emitter coupled logic family (ECL) which is a non-saturated logic. Although the ECL family offers an advantage in speed, the 74S hundred logic has been chosen in this memo for the 11/40 hardware due to technical, cost, and product availability reasons. Those reasons are discussed with some detail in the following sections of this memo.

djc

COMPANY CONFIDENTIAL

TITLE: GUIDELINES FOR PDP-11/40 TECHNICAL MEMORANDA

PDP-11/40 Tech Memo # 2

AUTHOR: Dick Clayton
DATE: September 25, 1970, 4 pages
REVISION: None OBSOLETE: None
INDEX KEY: Technical Memoranda
Memoranda Formats
Format

DISTRIBUTION KEY: PDP-11/40 Group
PDP-11/20 Group
PDP-11 Coordinating Committee

ABSTRACT

This memo describes the conventions and purposes of the PDP-11/40 Technical Memoranda Set. Suggested formats and distributions are presented.

I. INTRODUCTION

Documentation of PDP-11/40 will follow the procedures outlined below to permit free flow of information between persons having a legitimate interest in PDP-11/40. Every document should clearly state whether it is a proposal, suggestion, edict, etc.

All technical memoranda will have a Title-Abstract page in a format identical to the format of the first page of this document. All original copies will be submitted to a "coordinator."

II. The coordinator will:

1. Assign a number and date to the memorandum.

2. Distribute copies according to the distribution key.

3. Update 11/40 Technical Memo #1; the Index, Summary of Abstracts, and Cross Reference.

4. File the original.

III. The Title-Abstract page contains the following information:

1. Title - The title should be as informative as possible.

2. Memorandum Number - This is left blank and will be filled in by the coordinator.

3. Author (s)

4. Date - To be filled out by coordinator.

5. Number of pages.

6. Obsolete - This list will indicate all memoranda obsoleted by this document. The index will be updated appropriately.

7. Revision - This list will indicate all memoranda revised by this document. The index will be updated appropriately.

8. Index Keys - Since some memoranda may affect several areas, the index keys are maintained in a cross-reference directory which is a part of PDP-11/40 Technical Memo #1. For example, a memorandum on the design and programming of a disk file might have the following index keys: Disk, I/O, Mass Storage, Programming.

9. Distribution Keys - Since not all of the documents will be of interest to everyone, several distribution lists will be assigned. These presently include:

    11/40 Group (all)
    11/20 Group (Managers & Supervisors)
    PDP-11 Coordinating Committee
    PDP-11 General List

    This list will be modified appropriately in the future. Names may be added to or deleted from any of these lists by contacting the coordinator.

10. Abstract - The abstract is probably the most important part of the document. It should contain, within this first page, if possible, a statement of what problem is investigated, what solutions were examined, and what conclusions were reached. Because of the wide involvement of many PDP-11 groups, total distribution of all Technical Memos is impractical. For this reason, <u>all</u> Title-Abstract pages will be appended to Technical Memo #1 (The Index and Abstracts) for wide distribution.

IV. The organization of the memo will usually be as follows:

1. Title-Abstract page.
2. Contents
3. Introduction
4. Problems
5. Possible solutions, their advantages and disadvantages

(Organization - continued)

6. Conclusions

The format of the body of the Technical Memo is at the discretion of the author who should strive to present the maximum amount of information in a minimum of space (i.e. single space where practical and state things concisely).

The purpose of these memos is to educate the reader and provide a relatively permanent record of the depth of study and rationale behind any technical decisions or problems. For this reason it is important to identify facts; "gut feel" and wild guesses, all have a place, but the author should be careful to distinguish which is which.

djc