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PDP-11

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PDP-11 BUS
TECHNICAL DESCRIPTION

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ABSTRACT

Technical description of PDP-11 Uni-Bus concept, signals, and bus operations. Includes data transfer, priority scheme, and interrupt sequence.

MARCH DATAMATION - SMALL COMPUTERS ARCHITECTURE.

I. INTRODUCTION

The PDP-11 I/O Bus is composed of thirty (3Ø) bi-directional signal lines. It is used for all communications and data transfers between system units. Programmed controlled data transfer, direct memory transfer, interrupt, and priority determination are all done via these thirty signals.

Since the exterior bus is bi-directional and may be used by any device, it may be controlled by any device. Such a controlling device is referred to as master. The device to which the master is communicating is called slave. This relationship could reverse should the slave become controller of the bus, i.e. it would be master.

Direction of data transfers is defined with relation to the master (controlling) device. Thus, a data transfer from processor to memory is data out, and a transfer from memory to processor is data in.

II. BUS SIGNALS

Bus communication is achieved through the following signals:

MSYN - Master synchronization - signal from bus master.

SSYN - Slave synchronization - signal from slave device in response to master.

C <2:Ø> - Control - 3 bus lines which indicate one of eight bus commands.

D <17:Ø> - Data - 18 bus lines which are used for data transfer (word on D <15:Ø> , high-order byte on D <15:8> , low order byte on D <7:Ø>), slave addressing (18 bit bus address on D <17:Ø>), and priority determination.

NPR - Non-processor bus request - signal to request bus control for data-break device use.

BR <3:Ø> - Bus request - bus control request for each of the four major device levels.

BBSY - Bus busy - signals bus use by devices other than processor.

PCLR - Power clear - initialization signal on console start, power up, and power down. PCLR initializes all devices, clearing device flags and processor condition codes and setting the processor's priority level to 1. Before PCLR is asserted on a power down condition, the power fail option must be activated so that machine parameters can be saved.

III. PRIORITY ARRANGEMENT

In normal operation, the processor is bus master fetching instructions and operands from memory. In this state the processor will recognize three types of bus control requests: (1) a request which will be granted during instruction execution, (2) a request which will be granted between instruction execution, and (3) a request from an Automatic Priority Interrupt device (API not implemented in small processor.)

A device making the first type of bus request cannot affect the state of the processor and must restrict its use of the bus to data-type bus transactions. Requests of this type are labeled NPR (Non-Processor Request).

A device making the second type of bus request is not restricted as in a NPR request and can interrupt program execution (using a INT to the processor). This type of request is labeled BR (Bus Request).

An API device would make the third type of request. Such a request would be made internally to the processor and only implemented in larger versions.

The PDP-11 has five device major bus control priority levels, each of which has 8 sublevels. These device major levels are NPR (highest), BR3, BR2, BR1, BRØ (lowest). The processor has eight priority levels as determined by 3 bits in the status register. Four processor levels correspond to the four BR levels, three are reserved for use with the API facility, and the lowest, level Ø, is reserved for time-shared systems. The NPR device priority level exceeds all processor levels and will therefore always be honored. The hierarchy of priorities are shown in the accompanying table.

The API device would be used for background-foreground programming and priority job stacking. An interrupt service routine for a BR3 interrupt for example, would probably make the essential data transfers and set the API facility to interrupt the processor at a lower level to execute the data processing routine.

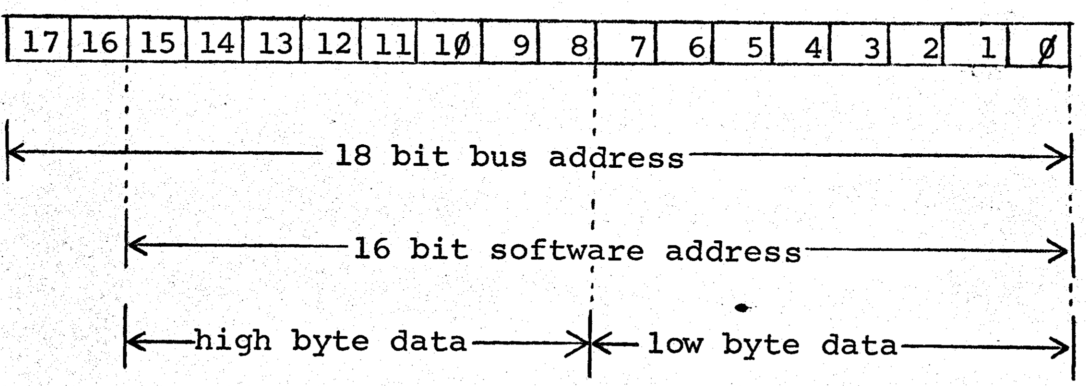
It should be noted that data-break use of the bus is not restricted to the NPR major level. The NPR level allows quickest bus control access, whereas, the BR levels must wait for instruction execution completion and may be locked out by a higher processor priority. Also note that once a device is bus master its control of the bus is uninterruptive and ends when control is returned to the processor (through an INT or by negating BBSY and MSYN).

IV. BUS TRANSACTIONS

C <2:Ø> are controlled by the bus master and define a bus command when MSYN is asserted. The C-lines must be set 15Øns before MSYN is asserted and are not reset until 15Øns after MSYN is negated. The C-lines are coded as follows:

	C2	C1	CØ	
Ø	Ø	Ø	Ø	INT - interrupt
1	Ø	Ø	1	PTR - priority bus transfer
2	Ø	1	Ø	CTR - console bus transfer
3	Ø	1	1	DATI - data in, word
4	1	Ø	Ø	DATO - data out, word
5	1	Ø	1	DATOB - data out, byte
6	1	1	Ø	DATM - data modify, word
7	1	1	1	DATMB - data modify, byte

In the data transactions, the D-lines are used as follows:



The processor converts the software address to a full 18-bit bus address. On word bus commands (DATI, DATO, DATM), the slave ignores DØ; on byte bus commands (DATOB, DATMB), slave receives byte data on D <15:8> if DØ=1 or D <7:Ø> if DØ=Ø.

Bus addresses 7776ØØ through 777777 are reserved for processor address use. External device registers are selected by bus addresses 76ØØØØ through 777577. When the processor sees the software address bits 15, 14 and 13 set to 1, it asserts D17 and D16 to form an 18-bit external device register address.

The following describes each of the bus transactions.

<u>DATM - Data Modify</u> - used in read-modify - restore word operations.

1. Master sets C = 6 and D <17:0> to a bus address.

2. Master asserts MSYN 150ns minimum after step 1.

3. All devices see C = 6 and allow the transition $\overline{\text{MSYN}} \longrightarrow$ MSYN to set their "select" flop if their address is deinfed by D <17:1> . The selected slave initiates response to the data request.

4. The slave asserts SSYN.

5. When the master sees SSYN, it removes address from the D-lines.

6. When slave has word ready, it puts it on D <15:0> and negates SSYN 150ns minimum later. Slave removes data 100ns after dropping SSYN.

7. When master sees SSYN $\longrightarrow \overline{\text{SSYN}}$, it strobes data off the D-lines. After modification master puts the data back on D <15:0> .

8. 150ns minimum after data has been on line, master negates MSYN. Data is removed from the D-lines 100ns after MSYN is negated.

9. Slave strobes data off D-lines at the fall of MSYN and enters a write cycle. Transaction is now complete.

NOTE:
1. SSYN must have a minimum width of 300ns. 150ns assures that master has seen SSYN and has removed address; 150ns is set up time for data on D-lines.

2. Selected slave need not immediately respond with SSYN.

3. Master will not assert MSYN again until 300ns minimum after it negates MSYN.

<u>DATMB - Data modify, byte</u> - used in read-modify-restore byte operations.

The sequence of steps is similar to the DATM transaction with the following changes:

1. Master sets C = 7 and D <17:0> to a bus address.

2. Slave sends to master the data word as defined by D <17:1> .

3. Master modifies the byte under consideration and returns that byte on the same D-lines that it received it on.

4. Slave accepts modified byte from D <15:8> if DØ = 1 or D <7:Ø> if DØ = Ø.

DATO - Data Out - Word transfer out of master

1. Master sets C = 4 and D <17:Ø> to a bus address.

2. Master asserts MSYN 15Øns minimum after Step 1.

3. All devices see C = 4 and allow the transition $\overline{\text{MSYN}} \longrightarrow \text{MSYN}$ to set their "select" flop if their address is defined by D <17:1> .

4. The slave asserts SSYN when it is ready to accept data.

5. When master sees SSYN, it removes address from the D-lines and then puts word on D <15:Ø> .

6. Master negates MSYN 15Øns minimum after setting data on D-lines. Data is removed 1ØØns after MSYN is dropped.

7. When the slave sees $\text{MSYN} \longrightarrow \overline{\text{MSYN}}$, it stobes data off the D-lines and negates SSYN.

NOTE: 1. Since only the leading edge of SSYN is being used, SSYN need only be asserted for 3ØØns minimum.

2. SSYN need not be asserted immediately upon selection.

3. Master will not assert MSYN again until it sees SSYN and 3ØØns minimum after it negates MSYN.

<u>DATOB - Data out, byte</u> - byte transfer out of master.

The sequence of steps is similar to DATO transaction with the following changes:

1. Master sets C = 5 and D <17:Ø> to a bus address.

2. Master sends byte out on D <15:8> if DØ = 1 or on D <7:Ø> if DØ = Ø.

3. Slave accepts byte from D <15:8> or D <7:Ø> depending on DØ.

DATI - Data In - Word transfer into master

1. Master sets C = 3 and D <17:Ø> to a bus address.

2. Master asserts MSYN 15Øns minimum after Step 1.

3. All devices see C = 3 and allow the transition $\overline{\text{MSYN}}$→MSYN to set their "select" flop if their address is defined by D <17:1> The slave initiates response to the data request.

4. The slave asserts SSYN.

5. When master sees SSYN it removes address from the D-lines.

6. When slave has data ready, it puts it on the D-lines and negates SSYN 15Øns minimum later. Slave removes data 1ØØns after dropping SSYN.

7. When master sees SSYN→$\overline{\text{SSYN}}$ it strobes data off the D-lines.

8. Master negates MSYN and transaction is complete.

NOTE: 1. SSYN has a minimum width of 3ØØns.

2. Selected slave need not immediately respond with SSYN.

3. Master will not assert MSYN again until 3ØØns minimum after it negates MSYN.

PTR - Priority bus transfer

The processor enters the following PTR bus sequence if it sees NPR asserted or a BR line asserted that is greater than the current processor's priority.

1. The processor sets C = 1 and sets D <15:11> as follows:

15	14	13	12	11
NPG	BG3	BG2	BG1	BGØ

NPG = NPR grant
BG <3:Ø> = BR grant

The grant line corresponding to the highest request at the time when the processor entered the PTR sequence is asserted.

2. Master asserts MSYN 15Øns minimum after Step 1.

3. All devices see C = 1 and MSYN. Each device that is requesting and has the major priority level indicated by D <15:11> assert one D <7:Ø> line (D7 (highest) to DØ (lowest))corresponding to its minor priority level. Each device must have a distinct priority.

4. After a fixed time delay about equal to one bus round trip (3ØØns minimum), the processor negates MSYN.

5. All participating devices at the fall of MSYN determine whether any device of higher priority than themselves have asserted their respective D <7:Ø> minor priority lines. The device which sees no higher D-line asserted asserts BBSY and becomes the new master device. All other devices negate any signals they have placed on the bus.

6. When the processor sees BBSY, it sets its wait flag and will thereafter become master whenever it sees MSYN and SSYN and BBSY. If no D <7:Ø>line is asserted, processor retains bus control.

NOTE: 1. New master may not assert MSYN until 3ØØns minimum after it asserts BBSY. 15Øns assure all devices and processor have dropped the D-lines; another 15Øns is set up time for new bus command.

2. No device making a bus request may enter the PTR sequence during its execution.

INT - Interrupt

This bus transaction is the means by which a device may interrupt processor's program execution. Note that for a device to execute an INT, it first must have gained bus control through a PTR sequence.

1. Master sets C = Ø and sets D <15:Ø> to the interrupt vector address. D17, D16, are not asserted.

2. Master asserts MSYN 15Øns minimum after Step 1.

3. The processor sees C = Ø and MSYN and strobes the interrupt vector address.

4. The processor asserts SSYN.

5. The master sees SSYN and negates MSYN and BBSY and removes the address from the D-lines.

6. The processor sees $\overline{\text{MSYN}}$ and negates SSYN. It then becomes master.

NOTE: 1. The processor may not assert MSYN until 15Øns minimum after seeing MSYN.

2. The interrupt vector address is the location of a new program counter and status word.

CTR - Console bus transfer

This bus command is used to transfer bus control to the console. It is the processor's response to the halt instruction.

1. Processor sets C = 2.

2. Processor asserts MSYN 15Øns minimum after Step 1.

3. Console sees C = 2 and MSYN and asserts BBSY.

4. When processor sees BBSY, it negates MSYN.

5. When console sees $\overline{\text{MSYN}}$, it is new master.

TABLE OF RELATIVE PRIORITIES

Device		Priority Level				
		Processor Status Bits: 15	14	13	External Device Major	Minor
Data-break device #7					NPR	7
" " " #6					NPR	6
" " " #5					NPR	5
" " " #4					NPR	4
" " " #3					NPR	3
" " " #2					NPR	2
" " " #1					NPR	1
" " " #∅					NPR	∅
Processor		1	1	1		
Device #7	Device group #3				BR3	7
" #6					BR3	6
" #5					BR3	5
" #4					BR3	4
" #3					BR3	3
" #2					BR3	2
" #1					BR3	1
" #∅					BR3	∅
Processor		1	1	∅		
Device #7	Device group #2				BR2	7
"					"	•
"					"	•
Device #∅					BR2	∅
Processor		1	∅	1		
Device #7	Device group #1				BR1	7
"					"	•
"					"	•
Device #∅					BR1	∅
Processor		1	∅	∅		
Device #7	Device group #∅				BR0	7
"					"	•
"					"	•
Device #∅					BR0	∅
Processor		∅	1	1		
API Software Interrupt Level #3						
Processor		∅	1	∅		
API Software Interrupt Level #2						
Processor		∅	∅	1		
API software Interrupt Level #1						
Processor--User Mode		∅	∅	∅		