3-0006-9

Grant Saviers

digital INTEROFFICE MEMORANDUM

DATE: 10 March 1969

SUBJECT: March 7 Meeting Minutes (Third Session)

TO: PDP-11 Design Review Committee FROM: Jerry Butler
CC: Engineering Committee
R. Cady
N. Mazzarese

The third session of the PDP-11 Electrical Design Review was held on Friday March 7, 1969. Present were: R. Pyle, R. Best, G. Saviers, I. Morris, D. Dubay, G. Fligg, R. Cady.

Roger Cady presented a paper of the latest pass at the architecture. In summary, the following changes were made:

1. The x, y, m, and n registers were replaced by x, x_2, x_3 and x_4 registers - all index registers.

2. A series of AC to register and register to AC instructions were added at the expense of the IOR instruction.

3. Auto increment addressing was omitted.

4. External addressing mode was omitted.

5. General register addressing was omitted.

6. Indexed addressing was expanded to include the four index registers.

It was generally agreed that the new hardware arrangement seemed cleaner.

Roger pointed out that his investigation of Alan Kotok's idea of adding a multiply step instruction (a la PDP-1), showed that instruction does not fit neatly into the hardware for the PDP-11.

The subject of indexing was discussed at length. There were two view points raised:

a. The 16-bit index with an 8-bit offset was adequate for most indexed instruction applications.

b. The indexed instructions should have a full 16-bit offset for full versatility.

The committee felt that its combined experience with indexed addressing was limited. A sub-committee of Grant Saviers and Roger Pylse was assigned to consult with PDP-10 programmers and others and report back.

Roger discussed the basic I/O philosophy. Because a paper revising the I/O architecture had just been released, the I/O details were set aside until the next meeting.

Roger Cady asked the committee for a commitment as to when it would complete its task. The committee agreed to meet more often (2 or 3 times a week). The committee will try to finish its recommendation on the architecture by March 14. The specific hardware implementation review will continue beyond that date.

The next meeting will be Monday, March 10. Roger Cady will arrange for a conference room.

Topics to be discussed will include:

I/O Bus Sequences
Indexed Addressing Sub-Committee Report
Console

Future Topics:

Hardware Implementation

a. Circuits
b. Packaging
c. Manufacturing Cost Estimates
d. Power Supply
e. Cooling
f. Field Service Policy

Please notify me if there are any mistakes or ommissions in these minutes.