digital INTEROFFICE MEMORANDUM

DATE: January 29, 1969

SUBJECT: PDP-11 Informantion

TO: Allan Kotok
John Cohen
Don Langbein
Larry Seligman
Rick Merrill
Bill Vaillancourt
Engineering Committee

FROM: R. Cady

The attached are descriptions of instruction set and bus configuration and dialogue on the PDP-11. This information will be of value if you can review it prior to the Engineering Committee meeting on the subject, January 30, 1969 at 8:30.

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DATE: January 29, 1969

SUBJECT: PDP-11 Bus

TO: Lists B, C, D

FROM: Roger Cady

The attached is a final draft of the technical specifications for PDP-11 bus signals and transactions. The definition of electrical characteristics (signal voltages, preferred circuits and loading) will be established in a subsequent memo. This corrects and finalizes the preliminary specifications of January 27, 1969.

I. Introduction

The PDP-11 I/O Bus is composed of thirty (30) bi-directional signals. It is used for all communications and data transfers between systems units. Programmed control, program transfer, direct memory transfer, interrupt, and priority determination are all done via these thirty signals.

Since the bus is bi-directional and may be used by any device, it may be controlled by any device. Such a controlling device is referred to as master. The device to which the master is communicating is called slave. This relationship could reverse should the slave become controller of the bus, i.e. it would be master.

Direction of data transfers is defined with relation to the master (controlling) device. Thus, a data transfer from processor to memory is data out, and a transfer from memory to processor is data in.

II. Signals

MSYN	Master SYNc	1
SSYN	Slave SYNc	1
PCLR	Power CLeaR	1
BYTE	BYTE transfer	1
C<2:0>	Control lines	3
D<15:0>	Data lines	16
BR<3:0>	Bus Request	4
BBSY	Bus BuSY	1
NPR	Non Processor Request	1
	request	1
FLAG	FLAG set	1
		30

MSYN - Master Sycn - Synchronizing signal from the master device (that which has control of the bus).

SSYN - Slave Sync - Signal from the selected slave device in response to MSYN.

PCLR - Power Clear - Clears the system, including all selection and master flags, clears the processor condition codes, and sets the processor to the Fetch state. PCLR must occur on power up, power down, and console start.

BYTE - Byte Transfer - Pulled down by either master or slave if it can only transfer byte data at the time.

C<2:0> - Control Lines - Lines controlled by master which, when MSYN is asserted, define a bus command.

Commands:

	C2	C1	C0		
0	0	0	0	DINI	Data IN, & Increment
1	0	0	1	DINE	Data IN, End transfer
2	0	1	0	DOTI	Data OuT & Increment
3	0	1	1	DOTE	Data OuT, End transfer
4	1	0	0	DIN	Data IN, no increment
5	1	0	1	ADRS	ADdReSs
6	1	1	0	DTR	Direct TRansfer
7	1	1	1	PTR	Priority TRansfer

D<15:0> - Data Bus<15:0> - Transmits data, addresses, priorities, device selections, and commands, etc.

BR<3:0> - Bus Request<3:0> - Priority Transfer request lines for each of the four major priority levels.

BBSY - Bus Busy - All devices on the bus except the processor assert BBSY when they are in control of the bus, and negate BBSY to return control to the processor.

NPR - Non Processor request - The device requesting the bus asserts NPR if it wishes the bus for data transfer or control. Devices wishing to perform an interrupt of the processor do not assert NPR. The processor will yield the bus between memory cycles of an instruction only if NPR is asserted.

FLAG - Flag set - Sets the I/O Flag (F) bit (bit 3) of the condition codes whenever FLAG is asserted at the rise of SSYN. The F bit may be tested by means of the conditional jump instructions JFS (Jump on Flag Set) and JFR (Jump on Flag Reset).

III. Bus Transactions

ADRS - Address

1. Master puts Address (16 bits) of device to be selected on D<15:0>. Sets C<2:0>=5.
2. Master asserts MSYN.
3. All units on bus decode C=5 and allow MSYN to set their "SELECTED" flop if their address is defined by D<15:0>.
4. SELECTED device responds by asserting SSYN.
5. Master sees SSYN, negates MSYN
6. Slave sees $\overline{\text{MSYN}}$, negates SSYN.

DINI, DIN, DINE - Data Input

This group of commands effect data transfer into the master. They may be byte, word, or terminating byte or word.

1. Slave must be selected by a previous ADRS sequence.
2. Master puts C=0, 1, or 4 on C bus.
3. Master asserts MSYN.
4. Slave puts DATA on D<7:0> (BYTE) if BYTE=1 and DATA on D<15:0> (WORD) if BYTE=0 (D<7:0> is low order byte of the word).
5. Slave asserts SSYN
6. Master accepts DATA from D lines and negates MSYN.
7. Slave sees $\overline{\text{MSYN}}$ and negates SSYN. If command was DINI (C<2:0>=0) the slave increments its address register by one if BYTE=1 and by two if BYTE=0. If command was DIN (C<2:0>=4) the address is not incremented. If DINE (C<2:0>=1) then the slave ends the communication by deselecting itself.

DOTI, DOTE - Data Output

This group of commands effect data transfer out of the master.

1. Slave must have been previously selected by an ADRS sequence.
2. Master puts C<2:0>=2 or 3 on C bus.
3. Master puts Data on D<7:0> if byte, on D<15:0> if word (low order byte D<7:0>).
4. Master asserts MSYN
5. Slave sees MSYN and accepts data and asserts SSYN. Data is byte if BYTE=1, word if BYTE=0.
6. Master sees SSYN, negates MSYN, C, D.
7. Slave sees $\overline{\text{MSYN}}$, negates SSYN and deselects itself if C0 was =1 during DATO transaction (DOTE). Otherwise it increments its address register (DOTI).

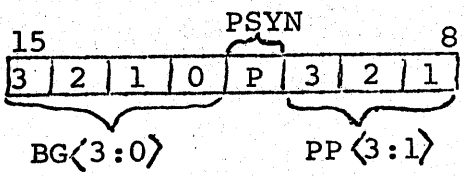
PTR

Each device that requires control of the bus is pre-assigned a major priority level from 0 (lowest) to 3, and a minor priority level from 0 (lowest) to 7. Each device must have a distinct priority level. When such a device requires the bus, it asserts the BR (Bus Request) line corresponding to its major priority level.

When the processor a) has control of the bus, b) does not have a slave device selected, c) has completed the current instruction, (see NPR), and d) sees one or more of the BR lines asserted, it compares the highest BR line asserted with the decoded value of high-order two

bits of the processor priority. If the processor priority is higher than the BR priority, the processor ignores the request(s) and continues; otherwise, the processor proceeds with the PTR sequence as follows.

1. The processor sets C⟨2:0⟩=7, and sets D⟨15:8⟩as follows:



The BG line corresponding to the highest BR line asserted at the beginning of the PTR sequence is asserted. PSYN is asserted. If the processor is operating at the major priority indicated by BG⟨3:0⟩, then the lower two bits of the processor priority (the processor's minor priority) are decoded and PP⟨3:1⟩ are set accordingly.

2. Processor asserts MSYN
3. All units see C⟨2:0⟩=7 and MSYN. Those units that are requesting and have the major priority indicated by D⟨15:12⟩ assert the D⟨7:0⟩ lines corresponding to their minor priorities upon transition of MSYN. Each device must have a distinct priority. The highest priority device in a given major priority level is assigned a minor priority level of 7, and so on down through 0. Devices requesting the bus for processor interrupt (DTR sequence) or other processor operation and who see NPR asserted inhibit putting their minor priorities on the D⟨7:0⟩ lines.
4. After a fixed time delay about equal to one bus round-trip time, the processor negates D11 (PSYN)and MSYN
5. All participating devices, at the transition of PSYN to $\overline{\text{PSYN}}$, determine whether any devices of higher minor priority than themselves have asserted their respective D⟨7:0⟩minor priority lines. PP1 (Processor Priority 1) is taken as a priority being between minor priority 1 and 2, PP2 is taken as being between 3 and 4, and PP3 is taken as being between 5 and 6. The device which sees no other device of higher minor priority(the winning device) asserts BBSY and becomes the new master device. All devices negate any signals they have placed on the bus during the sequence.
6. When the new master sees D⟨7:0⟩=0 it may proceed with an ADRS or DTR.
7. When the Processor sees BBSY, it sets its Wait flag and will thereafter become Master whenever it sees $\overline{\text{MSYN}}$ and $\overline{\text{SSYN}}$ and $\overline{\text{BBSY}}$.

Use of NPR line when making bus request:

If the use of the bus is requested by a device for data transfer or other operation which does not affect the processor (DIN, DOT, or DTR other than to processor) it may gain access to the bus in the middle of an instruction cycle by asserting ASAP along with its BR line. When the processor a) has control of the bus, b) does not have a slave device selected, and c) sees NPR asserted, it enters into a PTR sequence if the BR priority is greater than the processor priority. Note that by means of the NPR line, a device may obtain the bus before completion of the current instruction. The processor may not be interrupted (DTR sequence) at this time. Thus, the NPR signal must inhibit a device from putting its minor priority on D⟨7:0⟩ if it is requesting the bus for processor interrupt.

DTR - Direct Transfer

This is used to unconditionally transfer control of the bus to another device. It is the means by which the processor executes EXC and EXS instructions and by which a device may interrupt the processor.

1. Master sets C=6, sets D⟨15:8⟩ to the Device Selection code (DS) of the device to which it wishes to transfer control, and sets D⟨7:0⟩ to the Function Command (FC) being issued to the selected device, (the significance of the Device Command is specific to the selected device.)
2. Master asserts MSYN and negates BBSY.
3. All devices see C=6 and MSYN, and examine D⟨15:8⟩. The selected device examines D⟨7:0⟩ (FC) and performs accordingly. If the selected device requires the bus, it asserts BBSY.
4. The selected device asserts SSYN.
5. The master sees SSYN and negates MSYN.
6. The selected device sees $\overline{\text{MSYN}}$, negates SSYN. If the selected device has asserted BBSY, it then becomes master; otherwise, the processor sees $\overline{\text{MSYN}}$ and $\overline{\text{SSYN}}$ and $\overline{\text{BBSY}}$ and becomes master.

Note:
The processor responds to DS=0. Processor interprets FC as the address in the first 256 bytes of memory at which an interrupt entry vector is located and performs an interrupt via that address.

The console responds to DS=FF_{16}. The console interprets any command as a Halt, and holds the bus until manual intervention restarts the system. In addition, if the Function Command is in the range of $F0_{16}$ to FF_{16}, the console examines and displays the contents of the processor register with that address in the last 256

bytes, if there is display capability on the console.