PDP-11 Family

student workbook introduction to the pdp11

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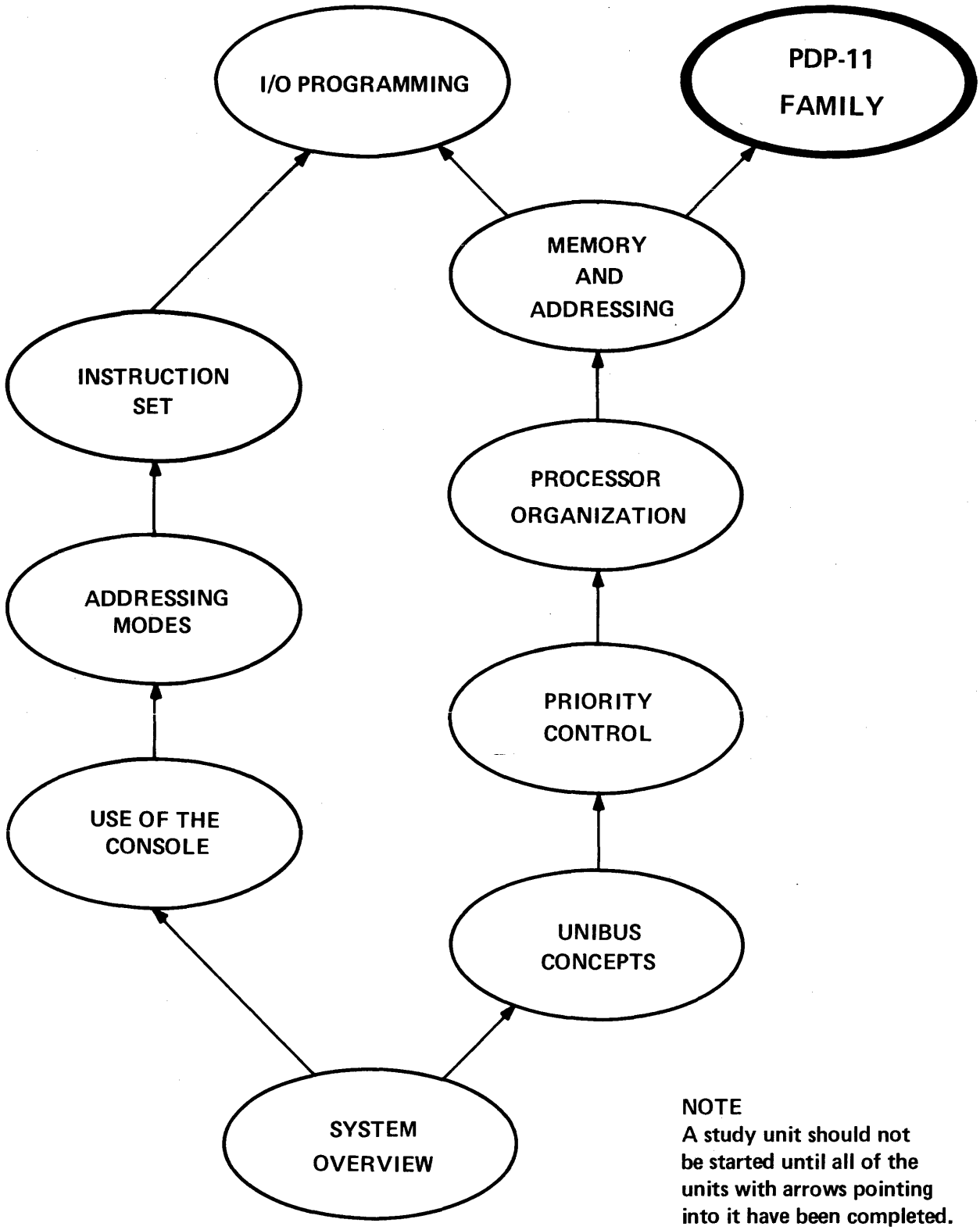
course map



NOTE
A study unit should not be started until all of the units with arrows pointing into it have been completed.

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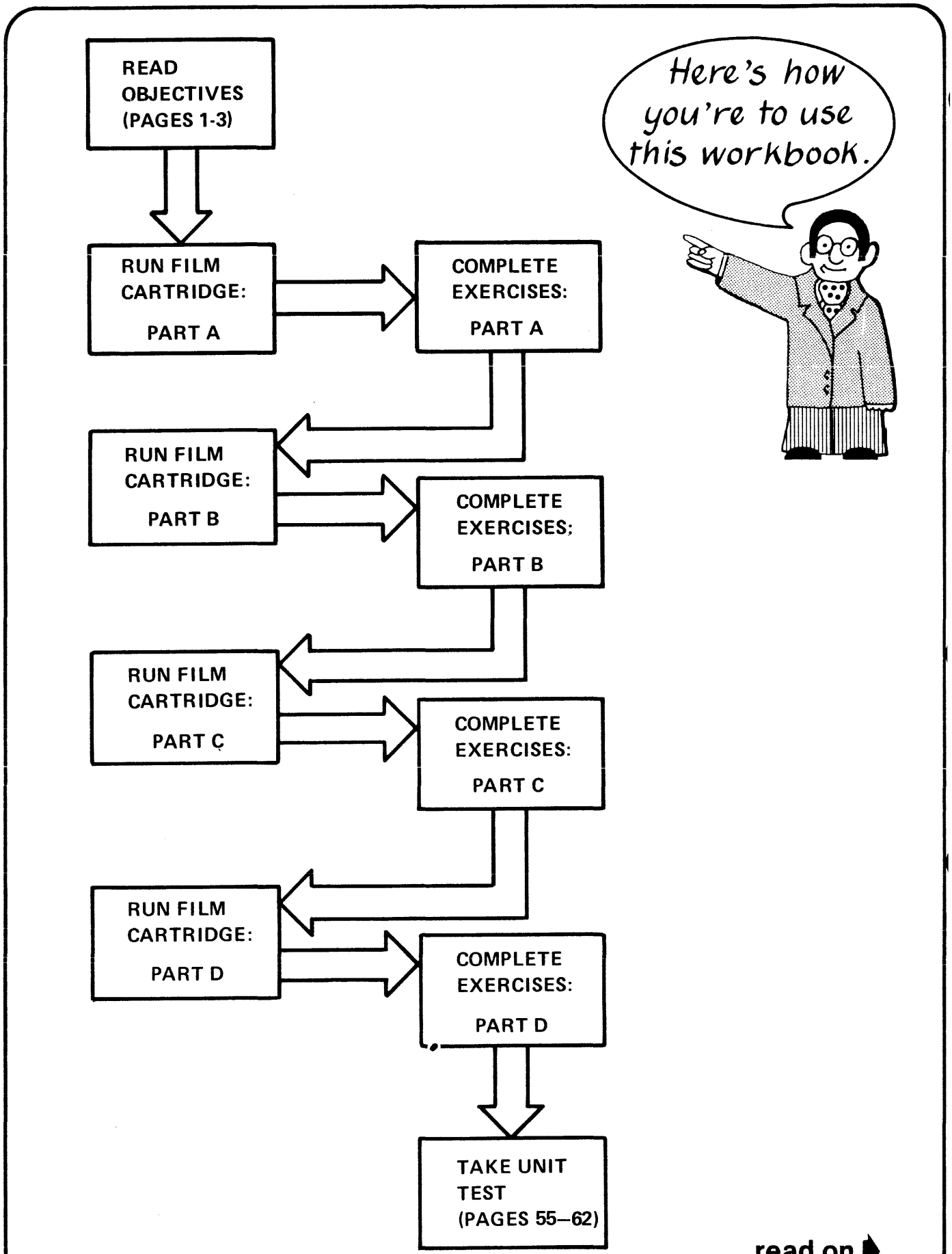

READ OBJECTIVES (PAGES 1-3)
RUN FILM CARTRIDGE: PART A
COMPLETE EXERCISES: PART A
RUN FILM CARTRIDGE: PART B
COMPLETE EXERCISES: PART B
RUN FILM CARTRIDGE: PART C
COMPLETE EXERCISES: PART C
RUN FILM CARTRIDGE: PART D
COMPLETE EXERCISES: PART D
TAKE UNIT TEST (PAGES 55–62)
Here's how you're to use this workbook.

read on

objectives

After completing this study unit you should be able to . . .

★ List the four major categories of computers in the PDP-11 family and identify by model number the PDP-11 computers that fall into each of the four categories.

★ Specify the *principal market area* for each PDP-11 computer (OEM, End-User, or OEM and End-User).

★ Draw a simple block diagram of an LSI-11 computer system that contains the following system components:

- Microcomputer Module
- Core Memory Module
- 1K and 4K MOS Modules
- PROM Module
- Serial Line Interface
- Parallel Line Interface
- LSI-11 Bus

★ Differentiate between the *LSI-11 Bus* and the *PDP-11 Unibus* in terms of:

- Hardware Interrupt Levels
- Data and Address Lines

★ List the three major functions performed by the memory management unit.

★ Differentiate between the PDP-11 Programmer's Console and the Operator's Panel in terms of:

- Implementation of load, examine, deposit, and start functions.
- Customer option or standard hardware on 11/04 and 11/34 computers.

(continued on next page)

read on ➧

objectives

★ Draw a simple block diagram of an 11/45 computer system and label the following system components:

- Central Processor
- Core Memory
- Solid-State MOS Memory
- I/O Device
- Unibus
- Fast Bus

★ Draw a simple block diagram of an 11/70 computer system and label the following system components:

- Central Processor
- DECwriter (I/O Device)
- Disk
- Magnetic Tape Unit
- High-Speed Controllers (two)
- Core Memory
- Cache Memory
- Unibus Map
- Unibus
- DMA Bus
- Memory Bus

read on

objectives

★ List the major characteristics of each computer in the PDP-11 family. These characteristics include:

- Names of Processing Modes
- Number of General-Purpose Registers
- Number of Hardware Interrupt Levels
- Number of Software Interrupt Levels
- Maximum Address Space
- Maximum Memory Size
- Bus Structure
- Types of Memory
- Number of Hardware Stacks
- Memory Management (not available, optional, standard)

read on ➧

Topic	*Key Points*	*Visual Ref.*
PDP-11 Computer Family	★ The PDP-11 Computer family consists of . . . • A series of compatible central processors, and • A variety of peripheral devices, operating systems, and applications software.	1
common characteristics	★ The following characteristics are common to all processors in the PDP-11 family: • 16-bit machines (the processors can work with 16-bit words or 8-bit bytes). • Common set of instructions. • Similar architecture.	2–5
upward compatibility	★ Because of their common characteristics, the processors are upward compatible (PDP-11 users can upgrade their systems without rewriting existing programs).	6
end user versus OEM	★ The PDP-11 computer family includes processors intended primarily for end users and equivalent models for original equipment manufacturers (OEMs). • An *end user* purchases the computer for direct use. • An *OEM* purchases the basic hardware and incorporates it into systems for resale to other customers (end users).	7–10

(continued on next page)

read on ➧

Topic	*Key Points*	*Visual Ref.*
end user versus OEM (Cont)	• Processors designed specifically for the end-user market generally have more standard features and hardware than equivalent OEM models. Also, supporting services (documentation, training, etc.) are supplied with the end-user system. • In OEM computers, many of the supporting services are "unbundled" and offered as *optional* items.	
major categories of PDP-11 processors	★ The family of PDP-11 processors is divided into four major categories: • Microcomputers, • Minicomputers for dedicated applications, • Minicomputers for multi-task applications, • Medium-scale computers for large multi-user, multi-task applications.	11–15
microcomputers	★ The LSI-11 and PDP-11/03 are classified as microcomputers. • They execute the same basic set of instructions as the larger PDP-11 processors. However, their processing speeds are slower.	16, 17

read on ➧

Topic	*Key Points*	*Visual Ref.*
LSI-11	★ The LSI-11 is constructed using large scale integration (LSI) techniques. • Four semiconductor chips make up the processor section of the LSI-11 microcomputer. • Up to 4K of MOS memory is also provided on the microcomputer module. • Memory expansion modules and I/O interfaces are contained on separate printed circuit boards.	18–21
PDP-11/03	★ The PDP-11/03 is a "packaged" version of the LSI-11 that includes . . . • LSI-11 microcomputer • Main memory • Power supply • Serial line interface for a teleprinter or display terminal • Operator's panel • Enclosure	22
principal markets	★ The 11/03 is marketed to both OEMs and high-volume end users; the LSI-11 is sold primarily to OEMs.	23
minicomputers: dedicated applications	★ The 11/04, 11/05, and 11/10 minicomputers are designed for *dedicated* applications such as data acquisition or numerical control.	24–27

read on

Topic	*Key Points*	*Visual Ref.*
11/04	• The 11/04 is marketed to OEMs and end users. It offers customers a choice of non-volatile core memory or solid-state MOS memory.	
11/05	• The 11/05 is only marketed to OEMs. It uses non-volatile core memory.	
11/10	• The 11/10 is electrically identical to the 11/05. However, it is packaged for end users and, therefore, offers more standard features and expansion space.	
minicomputers: multi-task applications	★ Our third category of computers includes the 11/34, 11/35, and 11/40. These minicomputers can handle several problems (tasks) simultaneously such as in timesharing applications where many users are interacting with the computer on a concurrent basis.	28–34
11/35 and 11/40	• The 11/35 and 11/40 use core memory and are electrically similar. However, the 11/35 is directed at the OEM market, while the 11/40 is packaged for end users.	
11/34	• The 11/34 is marketed to OEMs and end users. It offers customers a choice of MOS memory or core memory. Features such as memory management and an extended instruction set are an integral part of the 11/34 processor. These features are optional in the 11/35 and 11/40.	

read on

Topic	*Key Points*	*Visual Ref.*
medium-scale computers	★ The 11/45, 11/50, 11/55, and 11/70 are classified as medium-scale computers. • These computers are generally used for large, multi-user, multi-task applications. • Each of these computers is a complete system that can be marketed to OEMs and end users (separate model designations are not used to distinguish an OEM system from an end-user system).	35, 36
11/45, 11/50, and 11/55	★ The 11/45, 11/50, and 11/55 use the same basic CPU and bus structure. However, different types of memory are supplied in the *basic* system package. • Main storage in the *basic* 11/45 system consists of 32K of core memory. • The basic 11/50 system uses faster MOS memory or a mixture of MOS and core memory. • The basic 11/55 system is supplied with 32K of bipolar memory or a mixture of bipolar and core memory. • Larger 11/45 and 11/50 systems can be expanded using combinations of bipolar, MOS, and core memory.	37–41
floating-point processor (FP11-C)	★ The 11/55 can accommodate a very fast floating-point processor option (the FP11-C). The FP11-C is used in combination with bipolar memory for high-speed "number crunching" applications.	42

read on ➧

Topic	*Key Points*	*Visual Ref.*
11/70	★ The 11/70 CPU is similar to the 11/55 central processor. However, the 11/70 bus structure is redesigned to triple system throughput (the maximum DMA transfer rate is 5.8 megabytes per second).	43, 44
summary	★ Figure 1 summarizes the four major categories of computers in the PDP-11 family. Table 1 lists the principal markets for each computer.	—

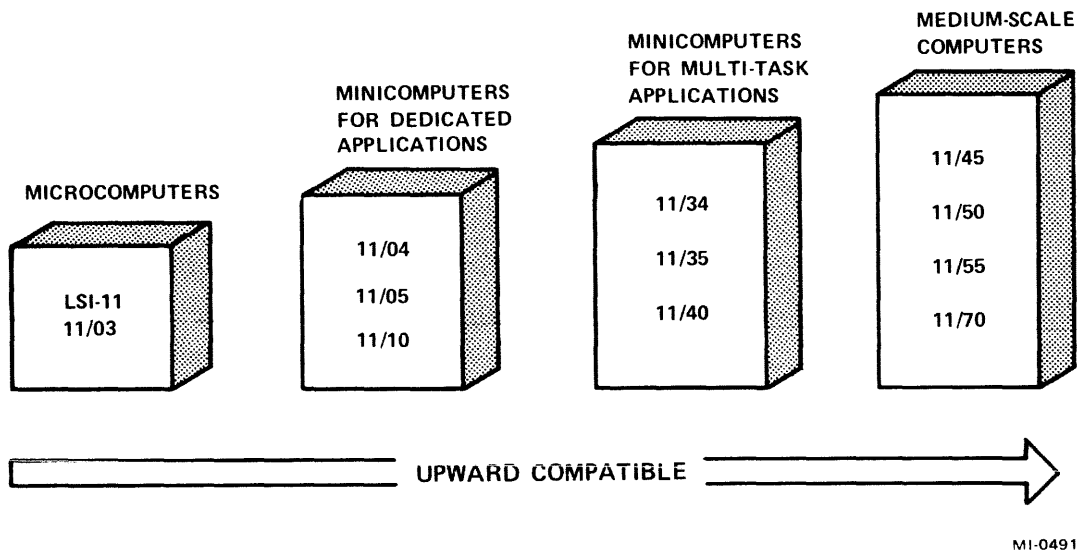


Figure 1 Major Categories of PDP-11 Computers

read on

Table 1 Principal Markets

	OEM	End User
LSI-11	✓	
11/03	✓	✓
11/04	✓	✓
11/05	✓	
11/10		✓
11/34	✓	✓
11/35	✓	
11/40		✓
11/45	✓	✓
11/50	✓	✓
11/55	✓	✓
11/70	✓	✓

read on

1. A customer who purchases a computer system for *direct use* is called an _____ _____.

2. A customer who purchases the *basic* computer hardware and then incorporates it into systems for resale to other customers is called an _____ _____.

3. Complete the following chart by:

   (a) Listing the *four major categories* of PDP-11 computers,

   (b) Specifying the *model numbers* of the PDP-11 computers that fall into each category, and

   (c) Specifying the *principal market* for each PDP-11 computer (OEM, End User, or OEM and End User).

(a) Major Category	(b) Model Number(s)	(c) Principal Market(s)

read on

1. A customer who purchases a computer system for *direct use* is called an End User .

2. A customer who purchases the *basic* computer hardware and then incorporates it into systems for resale to other customers is called an Original Equipment Manufacturer (OEM) .

3. Complete the following chart by:

   (a) Listing the *four major categories* of PDP-11 computers,

   (b) Specifying the *model numbers* of the PDP-11 computers that fall into each category, and

   (c) Specifying the *principal market* for each PDP-11 computer (OEM, End User, or OEM and End User).

(a) Major Category	(b) Model Number(s)	(c) Principal Market(s)
Microcomputers	LSI-11 11/03	OEM OEM & End User
Minicomputers for dedicated applications	11/04 11/05 11/10	OEM & End User OEM End User
Minicomputers for multi-task applications	11/34 11/35 11/40	OEM & End User OEM End User
Medium-scale computers for large multi-user, multi-task applications	11/45 11/50 11/55 11/70	OEM & End User

Mark your place in the workbook and return to the A-V program.

read on

Topic	*Key Points*	*Visual Ref.*
LSI-11	★ The LSI-11 is configured by selecting a specific combination of printed circuit boards (modules). • The modules plug into a backplane assembly. • The backplane assembly distributes power and bus signals to all of the modules.	46–48
microcomputer module	★ The LSI-11 microcomputer module contains three system components: • 16-bit central processor (consists of four semiconductor chips), • I/O bus port, • Up to 4K of MOS memory.	49, 50
extended instruction set	★ An optional, fifth semiconductor chip extends the LSI-11 instruction set to include . . . • *Fixed-point* multiply, divide and multiple shift instructions. • *Floating-point* add, substract, multiply, and divide instructions.	51
general-purpose registers	★ Eight general-purpose registers are provided in the LSI-11: • R6 and R7 are normally used as the stack pointer and program counter. • The other 6 registers (R0–R5) are general registers; they are not dedicated to specific functions.	52

read on ➧

Topic	*Key Points*	*Visual Ref.*
LSI-11 memory and I/O modules	★ The LSI-11 can be expanded using the following modules: • Core memory (expandable in 4K-word increments) • MOS memory (expandable in 1K or 4K-word increments) • Programmable read-only memory or PROM (expandable in 256-word increments to 2K; or 512-word increments to 4K) • Serial line interface (for serial communications devices such as a teleprinter or display terminal) • Parallel line interface (a 16-bit general-purpose interface)	53–56
LSI-11 bus	★ All LSI-11 modules communicate over a single I/O bus. The LSI-11 I/O bus differs from the Unibus in two key areas: • Data and addresses are transmitted over the same set of bus lines (the Unibus has one set of lines for data and another separate set of lines for addresses). • A *single* hardware interrupt level is implemented in the LSI-11 bus (the Unibus has 4 hardware interrupt levels).	57–60
LSI-11 address space	★ The LSI-11 can reference a maximum of 32K words (64K bytes) using the 16-bit address. • The top 4K of the address space is available for referencing I/O registers. • The balance of the address space (28K) is used for main memory.	61–63

read on ➧

Topic	*Key Points*	*Visual Ref.*
PDP-11/03	★ The PDP-11/03 uses the same printed circuit modules as the LSI-11. • These modules are installed in a rack-mountable enclosure. • The enclosure also houses a power supply, cooling fans, and an operator's panel.	64, 65
principal markets	★ The LSI-11 is sold primarily to OEMs; the 11/03 is marketed to OEMs and high-volume end users.	66
11/04, 11/05, and 11/10	★ The 11/04, 11/05, and 11/10 minicomputers are used primarily for *dedicated* applications. The following characteristics are common to these minicomputers: • Eight general-purpose registers. • Same bus structure; the 56-line Unibus with four hardware interrupt levels and one NPR (non-processor request) level for DMA transfers. • Memory management hardware is not used; therefore, the maximum address space is 32K words (4K for I/O register addresses; 28K for main memory).	67–72

read on ➧

Topic	*Key Points*	*Visual Ref.*
major differences: 11/04 versus 11/05, 11/10	★ The 11/04 differs from the 11/05 and 11/10 in the following areas: • *Memory types* – the 11/04 offers customers a choice of MOS memory (725 ns cycle time) or core memory (980 ns); the 11/05 and 11/10 use core memory only. • *Processing speed* – the 11/04 executes instructions faster than the 11/05 or 11/10 (example: ADD R0, R1 takes 2.7 μs in the 11/04 versus 3.7 μs for the 11/05 and 11/10). • *Standard features* – a programmer's console, real-time clock, and serial communication line interface are standard features in the 11/05 and 11/10; these features are optional in the 11/04.	73–80
programmer's console	★ The programmer's console that is used in the 11/05 and 11/10 contains switches and lamps for depositing data in memory and examining previously stored data.	81
operator's panel	★ Most switches and lamps are excluded from the 11/04 operator's panel. • The operator's panel works in combination with a ROM front panel emulator. • Special routines are hardwired into the ROM so that it replaces (emulates) basic console functions (load, examine, deposit, start, etc.) when the appropriate keys are pressed on an ASCII terminal.	82, 83
real-time clock	★ The real-time clock generates an internal timing signal (program interrupt) that allows the CPU to keep track of when events happen.	84, 85

read on ➧

Topic	*Key Points*	*Visual Ref.*
SCL interface	★ The serial communication line (SCL) interface handles all communications between the CPU and a *local terminal* (console teleprinter or keyboard display). • The SCL interface is not connected to the Unibus; it communicates with the CPU over an internal bus.	86, 87
ROM bootstrap loader	★ A ROM bootstrap loader is standard on the 11/04 and is optional on the 11/05 and 11/10. • This hardware feature allows the CPU to automatically load system programs into main memory from standard peripheral devices. • A separate bootstrap loader is preprogrammed into the ROM for each type of peripheral device.	88, 89
initiating the 11/04 bootstrap loader	★ On the 11/04 the bootstrap loader can be initiated three ways: • automatically whenever a "power-up" condition occurs, • manually by pressing the BOOT switch on the operator's panel, or • by typing in a bootstrap command from an ASCII terminal.	90
summary	★ Table 2 summarizes the major characteristics of the LSI-11 and 11/03 microcomputers and the 11/04, 11/05, and 11/10 minicomputers.	—

read on

Table 2 Major Characteristics of the LSI-11, 11/03, 11/04, 11/05, and 11/10

	LSI-11	11/03	11/04	11/05	11/10
PRINCIPAL MARKETS	OEM	OEM & End User	OEM & End User	OEM	End User
NUMBER OF GPRs	8	8	8	8	8
NUMBER OF HARDWARE INTERRUPT LEVELS	1	1	4	4	4
MAXIMUM ADDRESS SPACE (words)	32K	32K	32K	32K	32K
MAXIMUM MEMORY SIZE (words)	28K	28K	28K	28K	28K
BUS STRUCTURE	LSI-11 Bus	LSI-11 Bus	Unibus	Unibus	Unibus
TYPES OF MAIN MEMORY	Core MOS PROM	Core MOS PROM	Core MOS	Core	Core
PROGRAMMER'S CONSOLE (PC) OPERATOR'S PANEL (OP)	none	OP	OP*	PC	PC

* The Programmer's Console is available on the 11/04 as a customer *option*.

read on

1. An LSI-11 can be configured using various combinations of printed circuit modules. Name at least five of these modules.

   a. _____

   b. _____

   c. _____

   d. _____

   e. _____

2. A "packaged" version of the LSI-11 is called the _____

   _____

3. Match each term in the left-hand column with one or more of the descriptions in the right-hand column.

   a. LSI-11 Bus

   b. PDP-11 Unibus

   ( ) Transmits data over one set of lines and addresses over another set of lines.

   ( ) Transmits data and addresses over the *same* set of lines.

   ( ) Contains one hardware interrupt level.

   ( ) Contains four hardware interrupt levels.

   ( ) Used in the 11/04, 11/05 and 11/10 computers.

read on ➧

1. An LSI-11 can be configured using various combinations of printed circuit modules. Name at least five of these modules.

   a. Microcomputer Module
   b. Core Memory Module
   c. MOS Memory Module
   d. PROM Module
   e. Serial Line Interface
   Parallel Line Interface

   any 5 modules

2. A "packaged" version of the LSI-11 is called the 11/03.

3. Match each term in the left-hand column with one or more of the descriptions in the right-hand column.

   a. LSI-11 Bus
   b. PDP-11 Unibus

   (b) Transmits data over one set of lines and addresses over another set of lines.

   (a) Transmits data and addresses over the same set of lines.

   (a) Contains one hardware interrupt level.

   (b) Contains four hardware interrupt levels.

   (b) Used in the 11/04, 11/05 and 11/10 computers.

read on

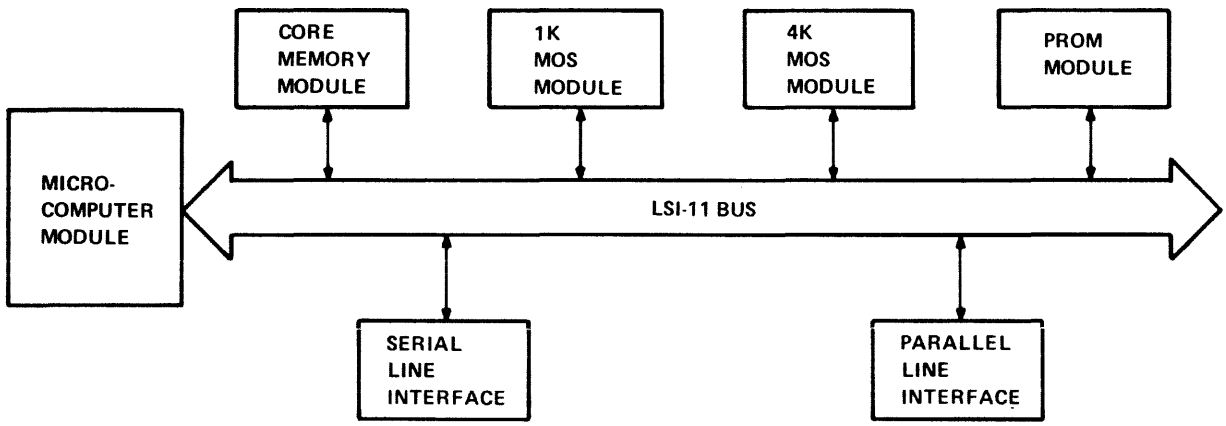
4. Draw a simple block diagram of an LSI-11 computer system and label the following system components:

- Microcomputer Module
- Core Memory Module
- 1K and 4K MOS Modules
- PROM Module
- Serial Line Interface
- Parallel Line Interface
- LSI-11 Bus

read on

4. Draw a simple block diagram of an LSI-11 computer system and label the following system components:

- Microcomputer Module
- Core Memory Module
- 1K and 4K MOS Modules
- PROM Module
- Serial Line Interface
- Parallel Line Interface
- LSI-11 Bus



read on

5. Fill in the missing information in the chart below.

	LSI-11 & 11/03	11/04	11/05 & 11/10
NUMBER OF GPRs			
NUMBER OF HARDWARE INTERRUPT LEVELS			
MAXIMUM ADDRESS SPACE (words)			
MAXIMUM MEMORY SIZE (words)			
BUS STRUCTURE			
TYPES OF MEMORY			

read on

5. Fill in the missing information in the chart below.

	LSI-11 & 11/03	11/04	11/05 & 11/10
NUMBER OF GPRs	8	8	8
NUMBER OF HARDWARE INTERRUPT LEVELS	1	4	4
MAXIMUM ADDRESS SPACE (words)	32K	32K	32K
MAXIMUM MEMORY SIZE (words)	28K	28K	28K
BUS STRUCTURE	LSI-11 Bus	Unibus	Unibus
TYPES OF MEMORY	Core MOS PROM	Core MOS	Core

Mark your place in the workbook and return to the A-V program.

read on

Topic	*Key Points*	*Visual Ref.*
11/34, 11/35, and 11/40	★ The 11/34, 11/35, and 11/40 minicomputers accommodate additional features that are required for multi-task applications such as timesharing. Two of the most important features are: • memory management hardware and • dual processing modes.	99, 100
memory management	★ Memory management is standard on 11/34 systems and is optional on the 11/35 and 11/40.	101
memory management functions	★ Memory management performs three system functions: • Address expansion • Memory protection • Program relocation	102
address expansion	★ When the memory management unit is enabled, it converts 16-bit addresses supplied by the CPU (virtual addresses) into expanded 18-bit addresses that are sent over the Unibus. • The 18-bit address increases the maximum address space to 128K words. • 124K is available for referencing locations in main memory; the other 4K is reserved for I/O and CPU registers.	103, 104

read on

Topic	*Key Points*	*Visual Ref.*
memory protection	★ When several programs are resident in main memory, the memory management unit provides hardware facilities that protect these programs from unauthorized access or modification. • Protection is accomplished by first dividing main storage into smaller segments called "pages." • The starting address of each page is established using page address registers (PARs) in the memory management unit. • Access to individual pages is controlled by special access keys that are stored in page descriptor registers (PDRs).	105–108
access keys	★ Three types of access keys are implemented in the 11/34, 11/35, and 11/40: • *Non-resident key* – protects the corresponding page from both read and write operations (the page is declared inaccessible to user programs). • *Read-only key* – allows information to be read from the page, but aborts any attempts to write into that page (this key protects the contents of the page from willful or accidental modification). • *Read-write key* – allows complete read access and write access to the page.	109–112

read on

Topic	*Key Points*	*Visual Ref.*
program relocation	★ Program relocation involves the page address registers (PARs) that are part of the memory management unit. • When a program is stored in main memory, its starting address is derived from a program relocation constant that is held in one of the PARs. • Later, when the program is executed, its relocation constant is automatically combined with each 16-bit virtual address issued by the CPU. The resulting 18-bit address is then used to access main memory.	113–116
dual processing modes	★ If an 11/34, 11/35, or 11/40 system contains memory management hardware, the CPU may be operated in two processing modes – Kernel mode and User mode. (Remember, the 11/03, 11/04, 11/05, and 11/10 can only operate in Kernel mode.) • *Kernel mode* allows the program currently running in the CPU to have complete control over the system. (The system monitor is executed in Kernel mode because it requires unrestricted use of the computer.) • *User mode* inhibits the CPU from executing certain instructions such as HALT or RESET (user programs are executed in User mode).	117–119
two hardware stacks	★ When there are two processing modes, there are also two hardware stacks. Each stack requires its own stack pointer (SP).	120, 121

read on ➧

Topic	*Key Points*	*Visual Ref.*
nine GPRs	★ 11/34, 11/35, and 11/40 systems equipped with memory management contain nine GPRs. • Two registers function as the Kernel and User stack pointers. • One register serves as the program counter. • The six remaining GPRs are general registers; they are not used for special functions.	122
major differences: 11/34 versus 11/35, 11/40	★ The 11/34 differs from the 11/35 and 11/40 in the following areas: • *Memory types* – the 11/34 offers customers a choice of core memory (1 μs cycle time) or MOS memory (775 ns cycle time); the 11/35 and 11/40 are only available with core memory (980 ns cycle time). • *Standard features* – memory management, a ROM bootstrap loader, and an extended instruction set are built into all 11/34 systems; in the 11/35 and 11/40 these features are available as customer options. • *Console* – the 11/35 and 11/40 use the programmer's console; the 11/34 uses a simplified operator's panel.	127–131

read on

Topic	*Key Points*	*Visual Ref.*
extended instruction set	★ The extended instruction set (EIS) provides hardware facilities for executing multiply, divide, and arithmetic shift instructions (the EIS instructions are directly compatible with instructions used in the larger PDP-11 computers). • In the 11/34, the EIS hardware is an integral part of the CPU. • In the 11/35 and 11/40, the EIS is implemented on a separate printed circuit module (KE11-E) that connects to the Unibus.	132–135
programmer's console	★ The 11/35 and 11/40 programmer's console contains switches and lamps for performing LOAD, EXAMINE, DEPOSIT, and START functions.	136, 137
operator's panel	★ The 11/34 operator's panel has a limited number of switches and lamps. • This operator's panel is used in combination with a ROM console emulator. • The ROM emulator permits console functions, such as LOAD, EXAMINE, DEPOSIT, and START, to be performed simply by typing in the appropriate code on the keyboard of the ASCII terminal.	138–140
11/34 programmer's console	★ A programmer's console is available as optional hardware on 11/34 systems (the ROM console emulator can be used in conjunction with this optional programmer's console).	141
summary	★ Table 3 summarizes the major characteristics of the 11/34, 11/35, and 11/40 minicomputers.	—

read on ➧

Table 3 Major Characteristics of the 11/34, 11/35, and 11/40

	11/34	11/35	11/40
PRINCIPAL MARKETS	OEM & End User	OEM	End User
PROCESSING MODES	Kernel & User	Kernel & User	Kernel & User
NUMBER OF GPRs	*9	*9	*9
NUMBER OF HARDWARE INTERRUPT LEVELS	4	4	4
MAXIMUM ADDRESS SPACE (words)	*128K	*128K	*128K
MAXIMUM MEMORY SIZE (words)	*124K	*124K	*124K
BUS STRUCTURE	Unibus	Unibus	Unibus
TYPES OF MAIN MEMORY	Core MOS	Core	Core
NUMBER OF HARDWARE STACKS	*2	*2	*2
MEMORY MANAGEMENT	Standard	Optional	Optional
ROM BOOTSTRAP LOADER	Standard	Optional	Optional
EXTENDED INSTRUCTION SET	Standard	Optional	Optional
PROGRAMMER'S CONSOLE (PC) OPERATOR'S PANEL (OP)	**OP	PC	PC

*With Memory Management

**The Programmer's Console is available as an option.

read on

1. List the three major functions of the memory management unit.

   a. _____

   b. _____

   c. _____

2. Check the appropriate box or boxes to indicate whether each of the statements below describes the 11/34 *Programmer's Console* or the 11/34 *Operator's Panel*.

PROGRAMMER'S CONSOLE	OPERATOR'S PANEL	
☐	☐	Used in combination with a ROM emulator.
☐	☐	Load, examine, deposit, and start functions must be initiated from an ASCII terminal.
☐	☐	Contains all of the switches and lamps required for performing load, examine, deposit, and start functions.
☐	☐	*Standard* on all 11/34 computers.
☐	☐	Supplied as a customer *option* on the 11/34 computer.

read on

1. List the three major functions of the memory management unit.

   a. Address expansion

   b. Memory protection

   c. Program relocation

2. Check the appropriate box or boxes to indicate whether each of the statements below describes the 11/34 *Programmer's Console* or the 11/34 *Operator's Panel*.

PROGRAMMER'S CONSOLE	OPERATOR'S PANEL	
☐	☑	Used in combination with a ROM emulator.
☐	☑	Load, examine, deposit, and start functions must be initiated from an ASCII terminal.
☑	☐	Contains all of the switches and lamps required for performing load, examine, deposit, and start functions.
☐	☑	*Standard* on all 11/34 computers.
☑	☐	Supplied as a customer *option* on the 11/34 computer.

read on

3. Fill in the missing information in the following chart.

	11/34	11/35 & 11/40
PROCESSING MODES (names)		
NUMBER OF GPRs		
NUMBER OF HARDWARE INTERRUPT LEVELS		
MAXIMUM ADDRESS SPACE (words)		
MAXIMUM MEMORY SIZE (words)		
BUS STRUCTURE		
TYPES OF MEMORY		
NUMBER OF HARDWARE STACKS		
MEMORY MANAGEMENT (standard or optional)		
TYPE OF CONSOLE (Programmer's Console or Operator's Panel)		

read on

3. Fill in the missing information in the following chart.

	11/34	11/35 & 11/40
PROCESSING MODES (names)	Kernel User	Kernel User
NUMBER OF GPRs	9	9
NUMBER OF HARDWARE INTERRUPT LEVELS	4	4
MAXIMUM ADDRESS SPACE (words)	128K	128K
MAXIMUM MEMORY SIZE (words)	124K	124K
BUS STRUCTURE	Unibus	Unibus
TYPES OF MEMORY	Core MOS	Core
NUMBER OF HARDWARE STACKS	2	2
MEMORY MANAGEMENT (standard or optional)	Standard	Optional
TYPE OF CONSOLE (Programmer's Console or Operator's Panel)	Operator's Panel	Programmer's Console

Mark your place in the workbook and return to the A-V program.

read on

Topic	*Key Points*	*Visual Ref.*
11/45, 11/50, 11/55, 11/70	★ The following features are available on the medium-scale 11/45, 11/50, 11/55, and 11/70 computers: • Three processing modes. • Sixteen general-purpose registers. • A larger instruction set. • Seven software interrupt levels.	144–148
three processing modes	★ The three processing modes are Kernel, Supervisor, and User. • Supervisor mode is only implemented in 11/45, 11/50, 11/55, and 11/70 computers. • Supervisory programs operating in supervisor mode can pass control *outward* to user programs. • However, programs operating in supervisor mode cannot pass control *inward* to Kernel mode except by way interrupts or traps.	149–151
three hardware stacks	★ Each processing mode (Kernel, Supervisor, and User) has its own hardware stack. The active stack provides temporary storage for the current program count (PC) and processor status (PS).	152, 153
three sets of memory management registers	★ Each processing mode also has its own set of memory management registers (bits 14 and 15 in the processor status word specify which set of registers is active).	154, 155

read on

Topic	*Key Points*	*Visual Ref.*
16 general-purpose registers	★ The 16 GPRs implemented in these medium-scale PDP-11 computers are functionally organized as follows: • One register serves as the program counter (PC). • Three registers function as stack pointers (SPs); only one SP is active at any one time. • The 12 remaining registers are divided into two sets of six registers each. Each set of registers is available for general use, but only one set can be active at any given time (bit 11 in the PSW specifies which set is active). • Because there are two independent sets of general registers, the CPU can honor interrupt requests without having to copy the contents of its general registers into another storage area. When an interrupt occurs during program execution, the CPU simply switches to the other set of general registers.	156–162
expanded instruction set	★ Eleven new instructions are hardwired into the 11/45, 11/50, 11/55, and 11/70 central processor. Included are fixed-point multiply and divide instructions.	163
floating-point instructions	★ An optional floating-point processor (FPP) is also available. • 46 floating-point instructions are executed by the FPP. • Since the FPP is a separate processor, it can operate independently of the central processor (interaction between the FPP and CPU is automatically taken care of by the hardware).	164–166

read on

Topic	*Key Points*	*Visual Ref.*
interrupt structure	★ Four hardware interrupt levels and seven software interrupt levels are implemented in all 11/45, 11/50, 11/55, and 11/70 systems. • This interrupt structure allows programmers to assign different software priorities to segments within a program. • Less vital program segments (e.g., housekeeping operations) can be given lower priorities so that they will not interfere with more vital system functions (e.g., handling interrupts).	167, 168
major differences: 11/45, 50, 55, versus 11/70	★ The 11/70 differs from 11/45, 11/50, and 11/55 systems in three major areas: • Maximum address space • Memory configuration • Bus structure	170
11/45, 50, 55 address space	★ In the 11/45, 11/50, and 11/55 systems the memory management unit converts 16-bit addresses to 18 bits. • With the 18-bit address, the maximum address space is 128K words. • The top 4K is reserved for I/O interface registers and CPU registers. • The remaining 124K is used for main memory.	171, 172

read on ➧

Topic	*Key Points*	*Visual Ref.*
11/70 address space	★ In the 11/70 system the memory management unit converts 16-bit addresses to 22 bits. • With the 22-bit address, the maximum address space exceeds two million words. • The top 128K words of the address space is used for Unibus addresses. Of these addresses, 4K are reserved for CPU and I/O registers, and 124K are used by the *Unibus Map* to reference main memory (the Unibus Map is the interface to main memory from the Unibus). • The balance of the address space (over 1.9 million words) is available for referencing storage locations in main memory.	173–175
11/45, 50, 55 memory configurations	★ Main storage in an 11/45, 11/50, or 11/55 system can be configured using three different types of memory: • Non-volatile core memory (900 ns cycle time), • Solid-state MOS memory (500 ns cycle time), and • Solid-state bipolar memory (300 ns cycle time). • A system may utilize just one of these memory types or a mixture of all three types.	177–181
11/45, 50, 55 bus structure	★ In 11/45, 11/50, and 11/55 systems core memory attaches directly to the PDP-11 Unibus, while MOS and bipolar memories are connected to an internal fast bus as well as the Unibus (Figure 2).	182–184

(continued on next page)

read on

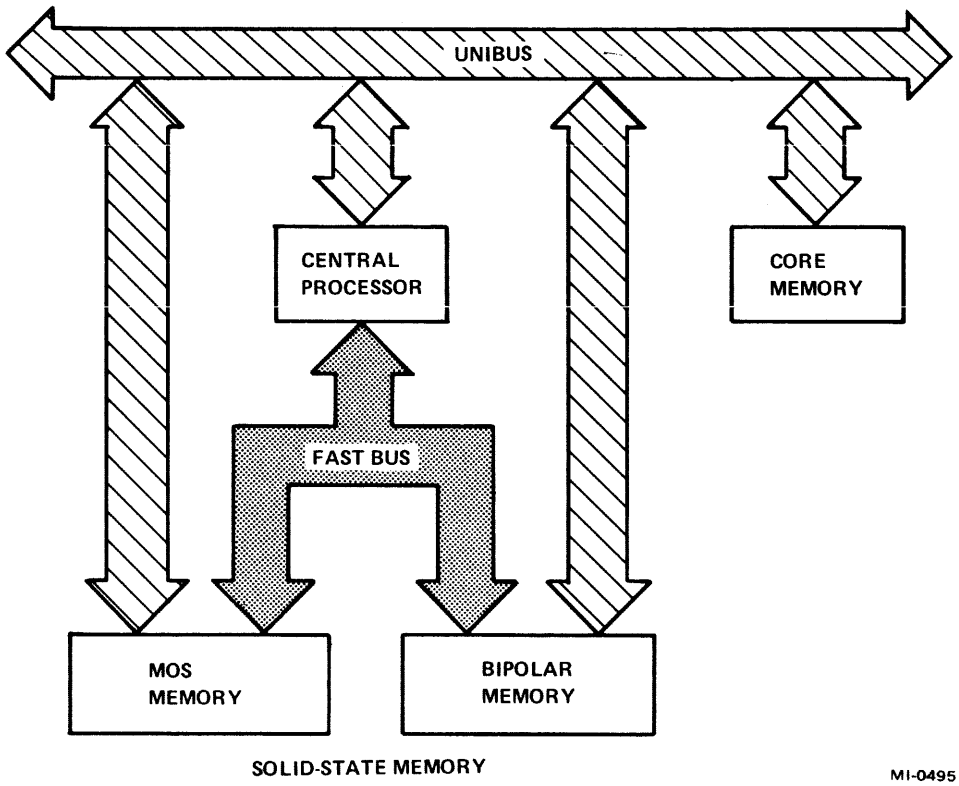


Figure 2 Typical PDP-11/45, 11/50, or 11/55 Computer System

Topic	*Key Points*	*Visual Ref.*
11/45, 50, 55 bus structure (Cont)	• This dual-bus structure increases system throughput. While the CPU is fetching and executing instructions from solid-state memory, a data transfer can occur between core memory and an I/O device.	

read on

Topic	*Key Points*	*Visual Ref.*
11/70 memory configuration	★ In the 11/70 system, main storage is functionally organized into two elements. • *core memory* with a maximum capacity of over 1.9 million words and a cycle time of 950 ns and • bipolar *cache memory* with a storage capacity of 1024 words (2048 bytes) and a cycle time of 240 ns. Cache memory maintains a copy of selected portions of core memory, thus providing faster access to instructions and data.	185–188
interaction: cache and core memory	★ The computer first looks for data in cache memory. • If the data resides in cache memory, it is retrieved, and slower core memory is not accessed. • If the data is not resident in cache memory, the computer must access slower core memory. Four bytes are then copied into cache memory, and the word or byte that was requested is sent to the CPU.	189, 190
Advantage of cache memory	★ Because programs tend to use localized sections of code (e.g., program loops), information is likely to be in cache memory when the CPU needs it. Since it takes less time to retrieve information from cache memory, the 11/70 will execute its programs faster (the effective cycle time is reduced to 400 ns).	191–193

read on

Topic	*Key Points*	*Visual Ref.*
11/70 structure	★ Three buses are used in the 11/70 in order to increase system throughput (Figure 3). • *PDP-11 Unibus* – the primary control path for the system; also handles data transfers involving low-speed devices such as DECwriters and paper tape units. • *DMA Bus* – a 32-bit data path between main memory and mass storage devices (disks and magnetic tape units). • *Memory Bus* – a 32-bit data path connecting cache memory and core memory; allows four bytes to be transferred in parallel between cache memory and core memory.	194–203
11/70 high-speed I/O controllers	★ Data transfers that take place over the DMA bus are managed by high-speed I/O controllers (see Figure 3). • The controllers connect to the 11/70 DMA bus and operate independently of the CPU. • Data is exchanged between the I/O controller and its mass storage device as two 16-bit words. • The I/O controller, in turn, sends and receives data over the DMA bus as one 32-bit word. • The Unibus transmits status and control information to or from the controller and also carries interrupt requests back to the CPU. • Up to four I/O controllers can be implemented in the 11/70 system.	197–202

read on ➧

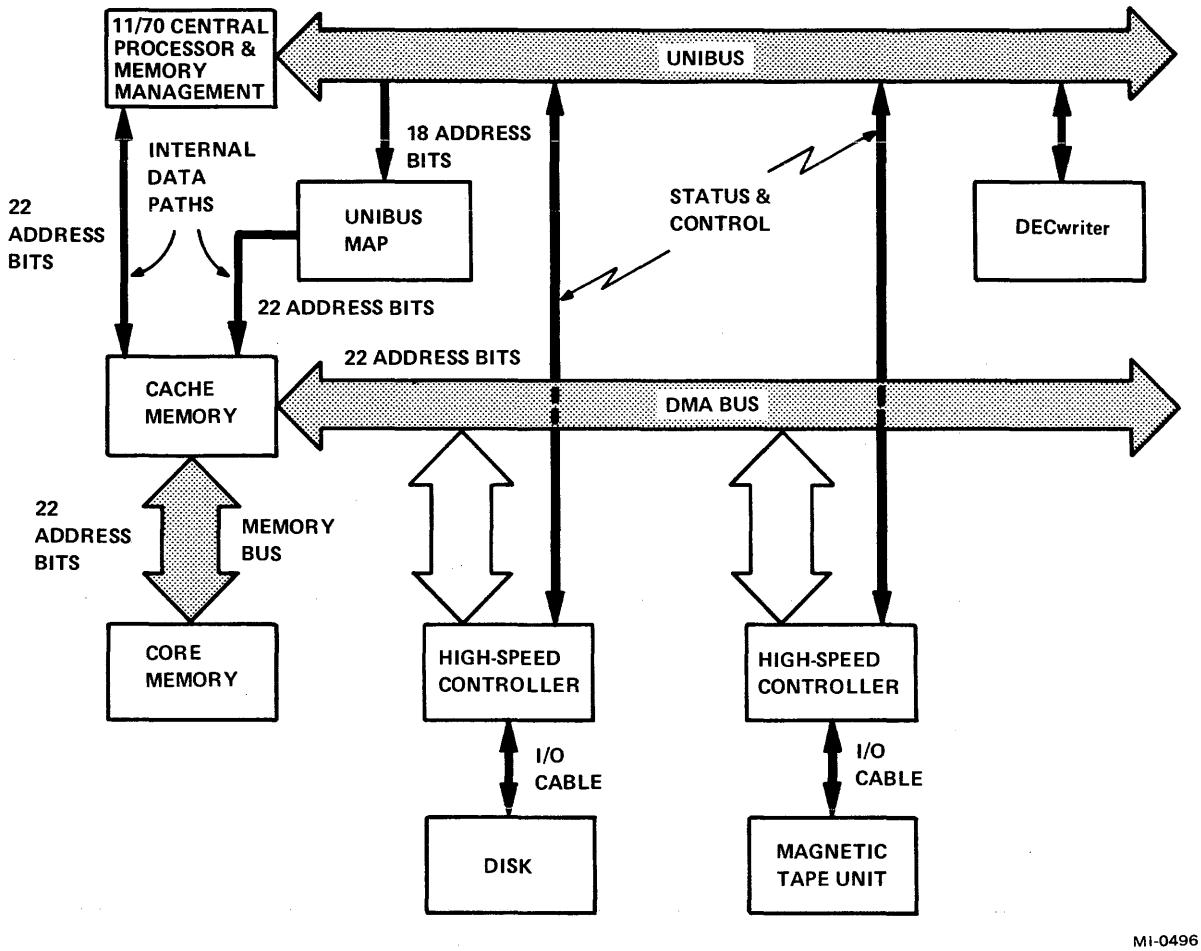


Figure 3 Typical PDP-11/70 Computer System

read on

Topic	*Key Points*	*Visual Ref.*
11/70 **Unibus map**	★ When a device on the Unibus wishes to communicate with main memory, the *Unibus map* converts 18-bit Unibus addresses into their corresponding 22-bit memory addresses. • The Unibus map is enabled or disabled under program control. • When disabled, the Unibus map adds *four leading zeros* to each incoming 18-bit address. **NOTE** Requests for memory access come from three sources: CPU, Unibus Map, and I/O Controllers. When more than one of these units require memory access concurrently, Cache Memory acts as a clearing house by granting memory access according to the following priorities: 1st priority – Unibus Map 2nd priority – High-Speed I/O Controllers 3rd priority – Central Processor	205–207
summary	★ Table 4 summarizes the major characteristics of the 11/45, 11/50, 11/55, and 11/70 computer systems.	--

read on ➧

Table 4 Major Characteristics of the 11/45, 11/50, 11/55, and 11/70

	11/45 11/50 & 11/55	11/70
PRINCIPAL MARKETS	OEM & End User	OEM & End User
PROCESSING MODES	Kernel Supervisor User	Kernel Supervisor User
NUMBER OF GPRs	16	16
NUMBER OF HARDWARE INTERRUPT LEVELS	4	4
NUMBER OF SOFTWARE INTERRUPT LEVELS	7	7
MAXIMUM ADDRESS SPACE (Words)	128K	2 million
MAXIMUM MEMORY SIZE (words)	124K	1.9 million
BUS STRUCTURE	Unibus & Fast Bus	Unibus DMA Bus Memory Bus
TYPES OF MAIN MEMORY	Core MOS Bipolar	Core & Bipolar Cache
NUMBER OF HARDWARE STACKS	3	3
MEMORY MANAGEMENT	Standard	Standard
STANDARD INSTRUCTION SET	Basic PDP-11 instruction set plus 11 new instructions	

read on

1. Name the two buses that are used in the 11/45, 11/50, and 11/55 computer systems.

   a. _____

   b. _____

2. Name the three buses that are used in the 11/70 computer system.

   a. _____

   b. _____

   c. _____

3. Main storage in the 11/70 system is functionally divided into two components.

   a. Name these two components _____

   _____

   b. Which component has the fastest cycle time? _____

   _____

   c. Which component has the largest storage capacity? _____

   _____

   d. What is the "effective cycle time" when these two components operate together? _____

   _____

read on ➧

answer sheet: part d

1. Name the two buses that are used in the 11/45, 11/50, and 11/55 computer systems.

   a. Unibus

   b. Fast Bus

2. Name the three buses that are used in the 11/70 computer system.

   a. Unibus

   b. DMA Bus

   c. Memory Bus

3. Main storage in the 11/70 system is functionally divided into two components.

   a. Name these two components. Cache Memory

   Core Memory

   b. Which component has the fastest cycle time?

   Cache Memory

   c. Which component has the largest storage capacity?

   Core Memory

   d. What is the "effective cycle time" when these two components operate together?

   400 nanoseconds

read on

4. Draw a simple block diagram of an 11/45 computer system. Your diagram should show the bus connections between the following system components:

   - Central Processor
   - Core Memory
   - Solid-State MOS Memory
   - An I/O Device

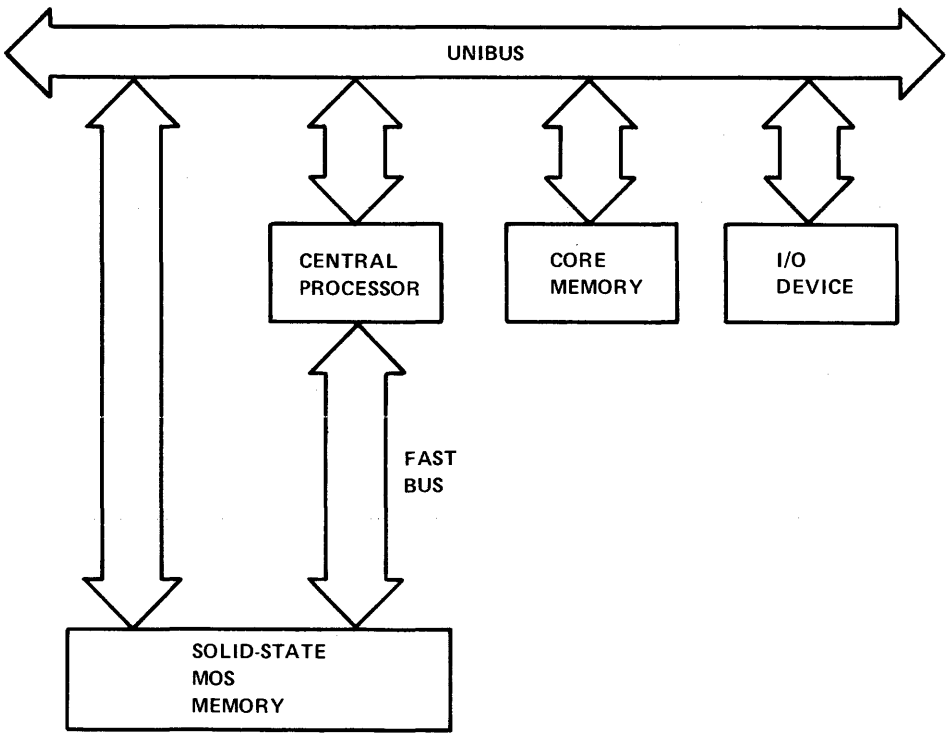
   Label each bus and each system component.

read on

4. Draw a simple block diagram of an 11/45 computer system. Your diagram should show the bus connections between the following system components:

- Central Processor
- Core Memory
- Solid-State MOS Memory
- An I/O Device

Label each bus and each system component.



read on

5. Draw a block diagram of the 11/70 computer system. Your diagram should show the bus connections between the following system components:

- Central Processor
- DECwriter
- Core Memory
- Cache Memory
- High-Speed Controllers (two)
- Disk
- Magnetic Tape Unit
- Unibus Map

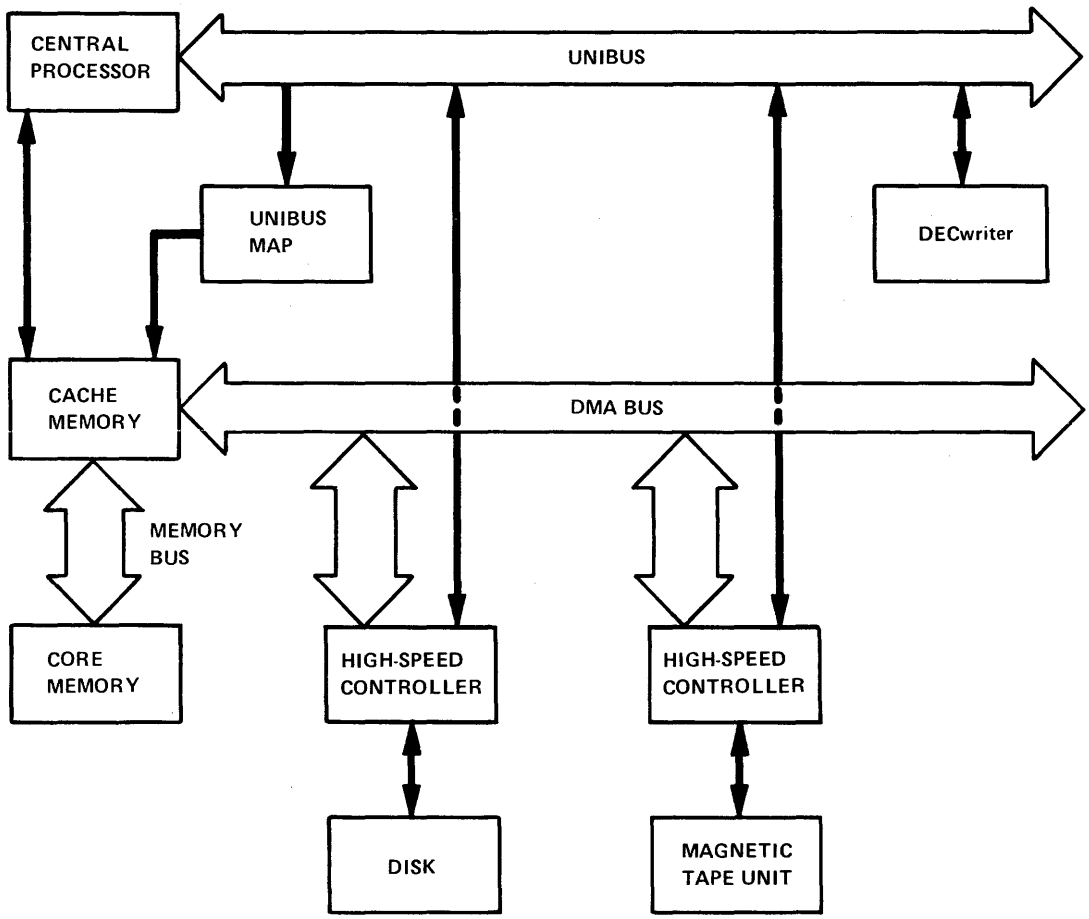
Label each bus and each system component.

read on

5. Draw a block diagram of the 11/70 computer system. Your diagram should show the bus connections between the following system components:

- Central Processor
- DECwriter
- Core Memory
- Cache Memory
- High-Speed Controllers (two)
- Disk
- Magnetic Tape Unit
- Unibus Map

Label each bus and each system component.



read on

6. Fill in the missing information in the chart below.

	11/45 11/50 & 11/55	11/70
PROCESSING MODES (Names)		
NUMBER OF GPRs		
NUMBER OF HARDWARE INTERRUPT LEVELS		
NUMBER OF SOFTWARE INTERRUPT LEVELS		
MAXIMUM ADDRESS SPACE (Words)		
MAXIMUM MEMORY SIZE (Words)		
TYPES OF MEMORY		
NUMBER OF HARDWARE STACKS		
MEMORY MANAGEMENT (Standard or Optional)		
BUS STRUCTURE (Names of Buses)		

read on

6. Fill in the missing information in the chart below.

	11/45 11/50 & 11/55	11/70
PROCESSING MODES (Names)	Kernel Supervisor User	Kernel Supervisor User
NUMBER OF GPRs	16	16
NUMBER OF HARDWARE INTERRUPT LEVELS	4	4
NUMBER OF SOFTWARE INTERRUPT LEVELS	7	7
MAXIMUM ADDRESS SPACE (Words)	128K	2 million
MAXIMUM MEMORY SIZE (Words)	124K	1.9 million
TYPES OF MEMORY	Core MOS Bipolar	Core & Cache
NUMBER OF HARDWARE STACKS	3	3
MEMORY MANAGEMENT (Standard or Optional)	Standard	Standard
BUS STRUCTURE (Names of Buses)	Unibus & Fast Bus	Unibus DMA Bus Memory Bus

read on

When you have completed the study unit, please take this self-scoring test. Then compare your answers against the "answer sheet" which can be obtained from your supervisor.

1. List the *four major categories* of computers in the PDP-11 family and specify the *model numbers* of the PDP-11 computers that fall into each category.

Category	Model Numbers

read on

2. Check the appropriate box or boxes to specify the principal market area for each of the PDP-11 computers listed below.

Computer	OEM	End User
LSI-11	☐	☐
11/03	☐	☐
11/04	☐	☐
11/05	☐	☐
11/10	☐	☐
11/34	☐	☐
11/35	☐	☐
11/40	☐	☐
11/45, 50, 55	☐	☐
11/70	☐	☐

read on

3. Draw a simple block diagram of an LSI-11 computer system that contains the following system components:

   - Microcomputer Module
   - Core Memory Module
   - 1K and 4K MOS Modules
   - PROM Module
   - Serial Line Interface
   - Parallel Line Interface
   - LSI-11 Bus

   Label each system component.

read on

4. Check the appropriate box to indicate whether each of the statements below refers to the *LSI-11 Bus* or the *PDP-11 Unibus.*

LSI-11 Bus	PDP-11 Unibus	
☐	☐	Contains four hardware interrupt levels.
☐	☐	Data and addresses are sent over the *same set* of 16 bus lines.
☐	☐	Data and addresses are sent over *two separate sets* of bus lines.
☐	☐	Contains one hardware interrupt level.

5. List the three major functions performed by the memory management unit:

   a. _____

   b. _____

   c. _____

6. Match each term with its corresponding description or descriptions.

   a. Programmer's Console

   b. Operator's Panel

   ( ) *Standard* on the 11/04 and 11/34 computers.

   ( ) A customer *option* on the 11/04 and 11/34 computers.

   ( ) Contains switches and indicator lamps that are necessary for load, examine, deposit, and start functions.

   ( ) Functions such as load, examine, deposit, and start are initiated from an ASCII terminal.

   ( ) Operates in combination with a ROM console emulator.

read on

7. Draw a simple block diagram of an 11/45 computer system and label the following system components:

- Central Processor
- Core Memory
- MOS Memory
- I/O Device
- Unibus
- Fast Bus

read on

8. Draw a block diagram of an 11/70 computer system and label the following system components:

- Central Processor
- DECwriter
- Core Memory
- Cache Memory
- Unibus Map
- High-Speed Controllers (two)
- Disk
- Magnetic Tape Unit
- Unibus
- DMA Bus
- Memory Bus

read on

9. Fill in the missing information in the following chart.

	LSI-11 & 11/03	11/04	11/05 & 11/10	11/34	11/35 & 11/40	11/45 11/50 11/55	11/70
Processing Modes (Names)							
Number of GPRs							
Number of Hardware Interrupt Levels							
Number of Software Interrupt Levels							
Maximum Address Space (Words)							
Maximum Memory Size (Words)							
Bus Structure (Names of Buses)							
Types of Memory							
Number of Hardware Stacks							
Memory Management (Not available, Optional, or Standard)							

notes

notes