KL10-Based DECSYSTEM-20 Installation Manual

digital equipment corporation • marlboro, massachusetts

EK-0KL20-IN-001

KL10-Based DECSYSTEM-20
Installation Manual

digital equipment corporation • marlboro, massachusetts

1st Edition, August 1978

The drawings and specifications herein are the property of Digital Equipment Corporation and shall not be reproduced or copied or used in whole or in part as the basis for the manufacture or sale of equipment described herein without written permission.

Copyright © 1978 by Digital Equipment Corporation

The material in this manual is for informational purposes and is subject to change without notice. Digital Equipment Corporation assumes no responsibility for any errors which may appear in this manual.

Printed in U.S.A.

This document was set on DIGITAL's DECset-8000 computerized typesetting system.

The following are trademarks of Digital Equipment Corporation, Maynard, Massachusetts:

DIGITAL	DECsystem-10	MASSBUS
DEC	DECSYSTEM-20	OMNIBUS
PDP	DIBOL	OS/8
DECUS	EDUSYSTEM	RSTS
UNIBUS	VAX	RSX
	VMS	IAS

CONTENTS

CONTENTS (Cont)

CONTENTS (Cont)

CONTENTS (Cont)

CONTENTS (Cont)

FIGURES

FIGURES (Cont)

TABLES

CHAPTER 1
INTRODUCTION

The installation procedures contained in this manual provide for system checkout and acceptance of the DECSYSTEM-20. Adherence to these procedures ensures that both the system and the configuration conform to design specifications. Where applicable, flow diagrams complement specific procedures. Table 1-1 is a list of related documents.

Personnel involvement, scheduling, customer data, prerequisites and assumptions, a day-to-day installation plan, and spare parts checkout are contained in Chapter 2.

Unpacking and inspection procedures, Chapter 3, are intended to ensure that the proper system is received at the customer site, and all equipment is in good physical condition.

Chapter 4 contains unit placement information dealing with the transportation of equipment from loading dock to site location, and the procedures for deskidding.

Unit interconnection procedures in Chapter 5 provide installation and interconnection information for the DECSYSTEM-20. Included are system positioning and grounding, cable identification, and sequence of installation and routing. These procedures are designed to eliminate failures due to improper ac wiring, shorted power cables, etc.

The system integration procedure described in Chapter 6 is designed to ensure that all component parts of the DECSYSTEM-20 are connected properly.

Chapter 7 contains power checkout procedures required to verify that the power system is functioning properly.

Total system operation is checked via the standard diagnostic checkout procedures described in Chapter 8. Appendix B contains sample diagnostic printouts.

Standard field service hardware acceptance procedures are contained in Chapter 9 and Appendix C.

Chapter 10 describes system add-on and adjustment procedures, including those for cabling, cache upgrade, model B upgrade, and MB20 installation.

Reporting procedures such as LARS forms, installation reports, and daily logs are explained in Chapter 11.

Table 1-1 Related Documents

Document No.	Title
EK-10/20-HR*†	Hardware Reference Manual
EK-20XX-PD*	DECSYSTEM-20 Physical Description
EK-45/03-MM*	TU45/TM03 Maintenance Manual
EK-BUS-ID*†	DECSYSTEM-20 Bus System Interface Description
EK-CD11-TM*	CD20 Maintenance Manual
EK-DATA-ID*	DECSYSTEM-20 Data Channel Interface Description
EK-DEC20-SD*	DECSYSTEM-20 System Description
EK-DEC20-SP†	DECSYSTEM-20 Site Preparation Guide
EK-DIA20-UD*	DIA20 Unit Description
EK-0DN2X-TM*	DN2X-DNHXX Technical Manual
EK-DTE20-UD*†	DTE20 Unit Description
EK-EBOX-UD*†	EBox Unit Description
EK-FE-ID*	DECSYSTEM-20 Front End Channel Interface Description
EK-KL10-HB†	KL10 Maintenance Handbook
EK-KL10-TD*	Introduction to KL10-Based System Technical Description
EK-KL10C-BD*	KL10-C Field Maintenance Print Set Supplement
EK-KL10C-IP*	KL10-C Illustrated Parts Breakdown
EK-KLINI-UG*†	KLINIK User's Guide
EK-LP20-MM*	LP20 Maintenance Manual
EK-MA020-UD*	MA20 Unit Description
EK-MB020-UD*†	MB20 Unit Description
EK-MBOX-UD*†	EBox Unit Description
EK-METER-UD*	Meter Board Unit Description
EK-PWR20-SD*	DECSYSTEM-20 Power System Description
EK-RH20-UD*†	RH20 Unit Description
EK-TU45A-MM*	TU45A/TM02 Maintenance Manual
EK-DEC20-LK†	DECSYSTEM-20 Layout Kit

*Available on microfiche. For information concerning Microfiche Libraries, contact:

Digital Equipment Corporation
Micropublishing Group
PK3-2/T12
Maynard, Massachusetts 01754

†Available in hard copy. Hard copy reference documents may be ordered from:

Digital Equipment Corporation
444 Whitney Street
Northboro, Massachusetts 01532

Attention: Printing and Circulation Services (NR2/M15)
Customer Service Section

CHAPTER 2
DECSYSTEM-20 INSTALLATION PLAN

2.1 INTRODUCTION

A critical factor in the predelivery phase is to develop an installation plan agreeable to all parties concerned. This chapter outlines personnel involvement, scheduling, customer data, prerequisites and assumptions, and a day-by-day hardware installation plan. An example of an installation planning sheet is shown in Appendix A.

2.2 PERSONNEL

The DIGITAL personnel involved in the complete installation and acceptance plan are listed below and should be consulted before the customer receives the plan.

1. Account sales representative
2. Software representative
3. Field service account supervisor/manager
4. Field service account representative
5. Field service district support representative
6. Field service regional support (support engineer or installation specialist)

2.3 SCHEDULING

The appropriate time to generate the final installation plan is approximately 30 days prior to delivery. This is close enough to installation time that people/resource commitments can be made with little chance of circumstances changing.

2.4 PREREQUISITES AND ASSUMPTIONS

1. Environment: Stable and Clean

   a. Power: 120/208/240/380 V +6%, -13%; 50/60 Hz ±1 Hz

   b. Temperature: 18° to 24° C (65° to 75° F) Rate of change 2° F/hr

   c. Humidity: 40 to 60 percent. Rate of change 2 percent/hr

2. System layout determined

3. Preinstallation site survey completed

4. System cables ordered

5. KLINIK modem installed (NORAM)

6. Installation team (2 hardware installers)

7. Work period (8 hours per day)

8. System Contents

   a. Disk drive (1)
   b. Tape drive (1)
   c. Line printer (1)
   d. Card reader (1)

   Add three (3) hours to total installation period per each additional unit.

2.5 SYSTEM INSTALLATION AND CHECKOUT

1. Day 1: Preliminary

   a. Unpacking
   b. Inventory
   c. Quality control inspection of interior and exterior

2. Day 2: Cabinet assembly

   a. Cabinet positioning
   b. Cabinets bolted together
   c. Preliminary power checks
   d. Cable installation

3. Day 3: Power checkout

   a. Prepower checks
   b. Power-on checks (adjustments if necessary)

4. Day 4: PDP-11 front end checkout

   a. PDP-11 CPU and memory diagnostics
   b. PDP-11 communication diagnostic
   c. Hard copy diagnostics
   d. KLINIK link
   e. SY2040 system exerciser (12 hours or overnight)

5. Day 5: Unit checkout

   a. Memory deskew check
   b. KL10 CPU and memory diagnostics
   c. RH20 deskew
   d. RH20 channel loopback diagnostics
   e. DFKDA (12 hours or overnight)

6. Day 6: Disk and tape drive checkout

   a. Run appropriate diagnostics
   b. Alignment checks
   c. Reliability checks (one each hour)
   d. DFSXA (12 hours or overnight)

7. Day 7:

    a. Monitor from KLAD-20 pack
    b. Acceptance script

8. Day 8: Reliability checks

    a. System reliability via SYSERR
    b. Software installation
    c. Initiate acceptance

2.6 SYSTEM SPARES

For systems which are geographically remote or isolated from repair/replacement facilities, a spare parts checkout program should be considered prior to hardware acceptance. A quick go/no go, dead-on-arrival check extends installation time approximately one day. Following checkout, it is advisable to remove all spare modules from the system and to restore the originals prior to hardware acceptance.

When a spare parts checkout program is to be performed, care should be taken to tag all modules to be tested or removed. The sequence of insertion should be planned prior to starting the test. An appropriate time to cycle spares is after all diagnostic checkout procedures have been completed; i.e., following day 7 of the day-by-day installation plan (Paragraph 2.5).

A suitable sequence of diagnostics should be run after each module/module batch insertion. The particular sequence will depend on which part of the system the spares are being checked in.

CHAPTER 3
UNPACKING AND INSPECTION

3.1 SHIPPING AREA PROCEDURES (Refer to Figure 3-1.)

Because of dock or shipping area procedures and/or ease of performing inventory, the shipment may be moved from the customer's shipping area to the computer area. If so, follow the procedures in Paragraphs 4.1 and 4.2 at this time.

3.2 SEALED CONTAINERS

Ensure that all boxes are sealed and that system cabinets and free-standing peripherals are in unopened shipping containers. If anything is opened, call it to the attention of the customer and document it on the installation report or field service report.

3.3 PACKING LIST

Check the shipment against the packing list to ensure that the correct number of packages has been received. If an incorrect number of packages has been delivered notify the customer and the branch service manager or the branch supervisor. The customer should check with the carrier to locate the missing package(s) and have the missing package(s) delivered to the site. The branch service manager or branch supervisor may have to check with the traffic and shipping departments to locate missing packages if the carrier does not have them.

3.4 SHIPPING DAMAGES

Check all boxes for external damages. Inspect for dents, protrusions, holes, smashed corners and pins, etc. If any boxes are damaged, notify the customer and document it on the installation report or field service report.

3.5 OPENING SHIPPING CONTAINERS

Open each box, one at a time (starting with the READ ME FIRST box) and locate its packing slip. Inventory each box against the packing slip and note any missing items on the installation report or field service report. While performing inventory, inspect each item for damage. Note damaged items on the installation report or field service report and inform the customer immediately. If the damage is extensive, call the branch service manager immediately and report the damages.

3.6 EXTERNAL DAMAGE INSPECTION

Check the system cabinets and free-standing peripherals for external damage to the shipping skid, covers, etc. Inspect the shipping containers for signs of stress or abusive handling. Remove the polyethylene covers and inspect external surfaces for scratches, holes, broken switches, broken panels, dented end panels, broken stabilizer feet, and any other damage or sign of abusive handling during shipment.

3.7 INTERNAL DAMAGE INSPECTION

Inspect each cabinet and free-standing peripheral for internal damage as follows.

1. Remove the tape or plastic shipping pins from the rear access door(s) of the cabinet(s). Open the rear door(s) of the cabinet(s) and ensure that each option is secure in the cabinet. Inspect the cabinet for cable damage (ac and dc cables), loose mounting rails, loose fans or blower motors, loose nuts and bolts, screws, loose module clips and module retaining bars, broken switches, lights, breakers, connectors on the power controllers and power supplies, broken cable connectors, console switches, etc.

UNPACKING AND INSPECTION FLOW

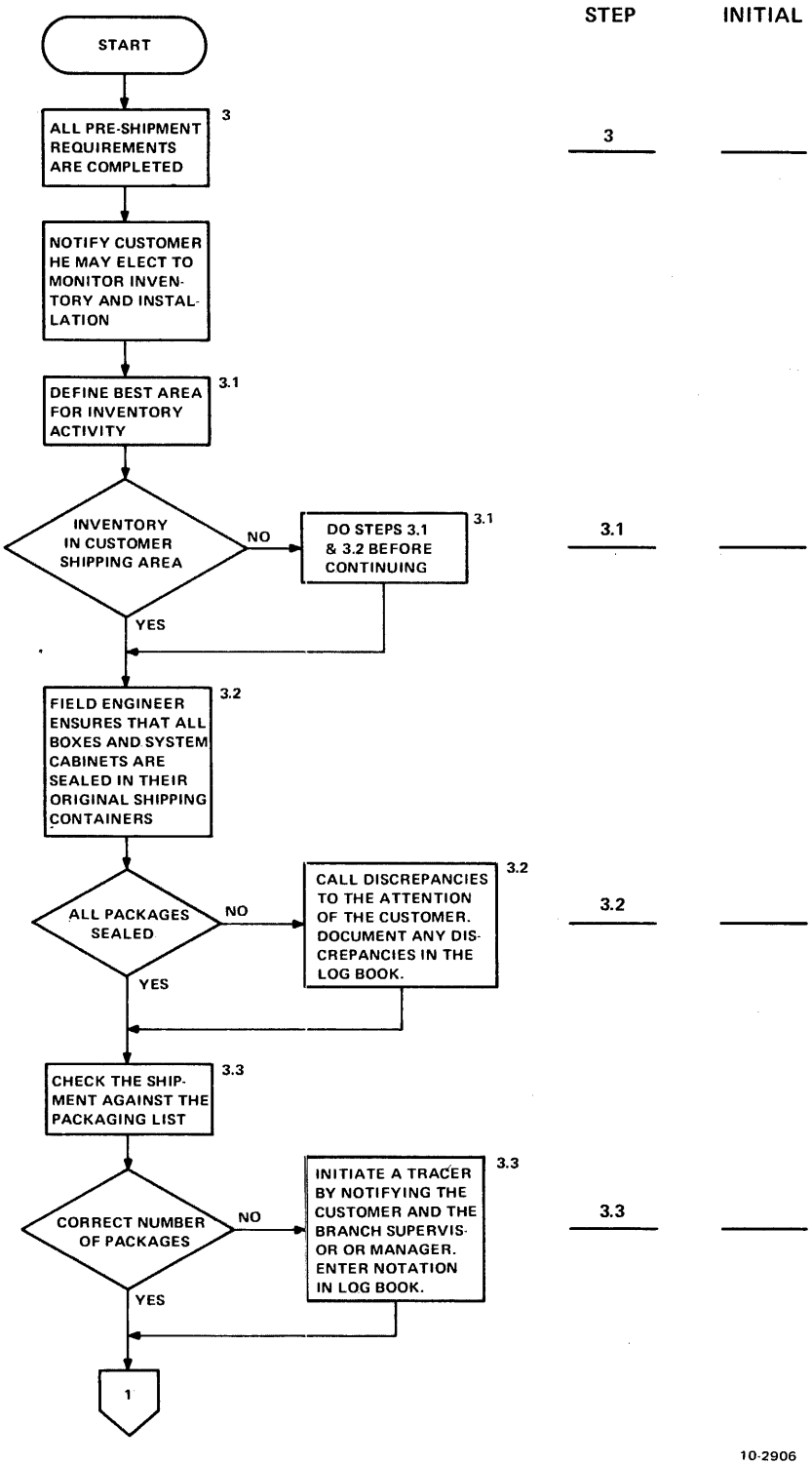


Figure 3-1 Unpacking and Inspection Flowchart (Sheet 1 of 4)

UNPACKING AND INSPECTION FLOW (Cont.)

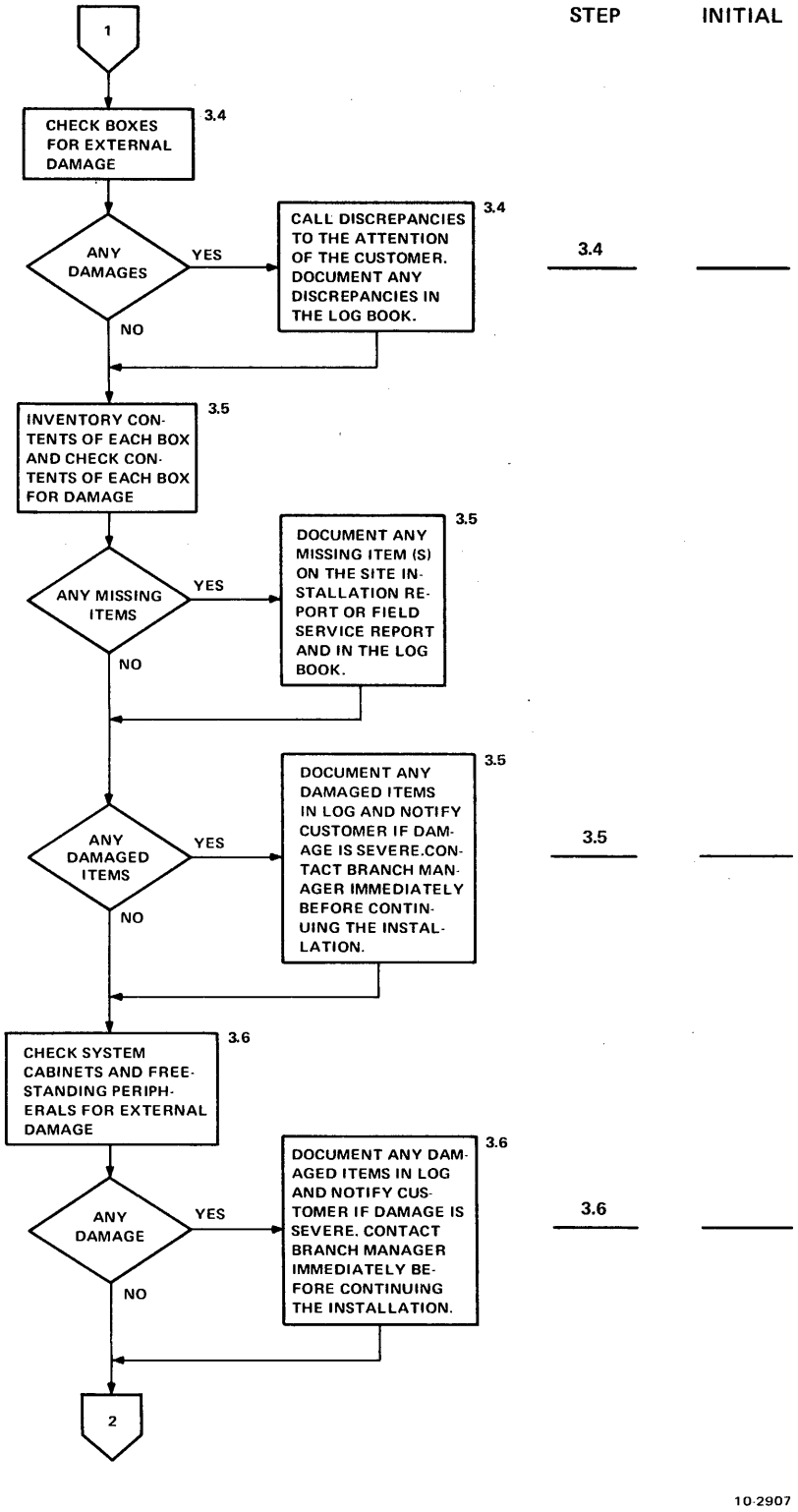


Figure 3-1 Unpacking and Inspection Flowchart (Sheet 2 of 4)

UNPACKING AND INSPECTION FLOW (Cont)

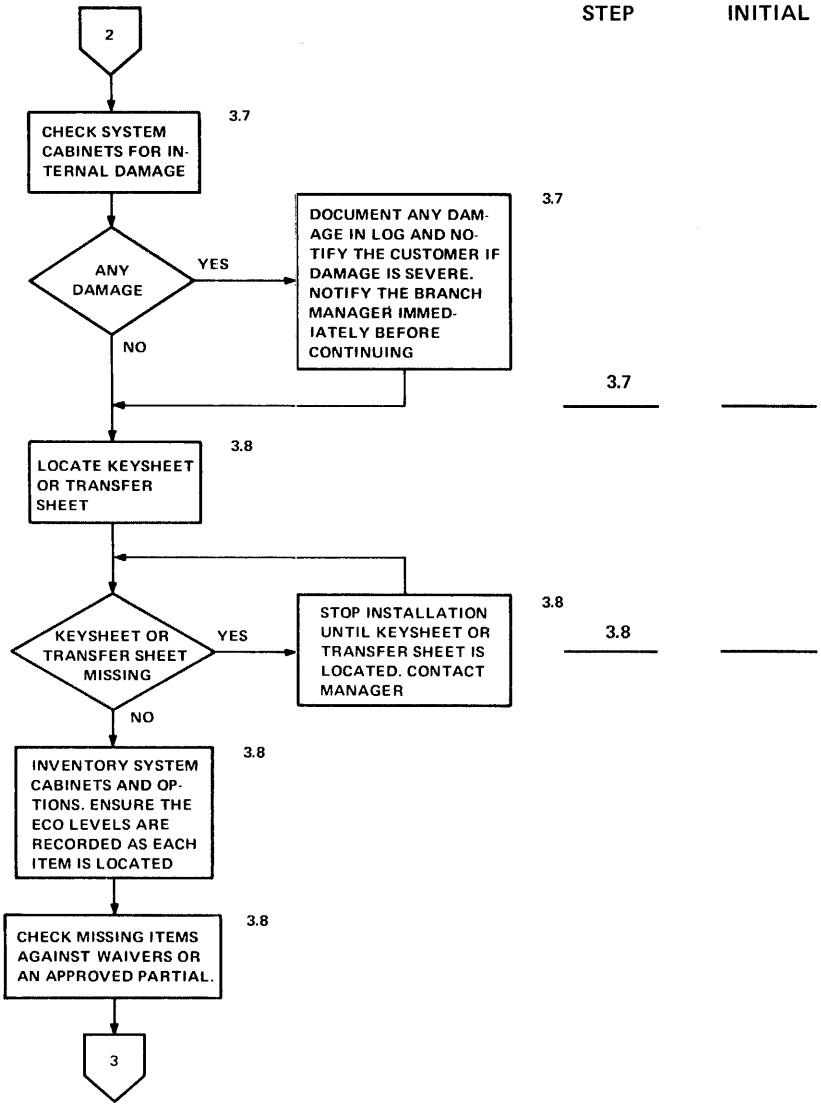


Figure 3-1 Unpacking and Inspection Flowchart (Sheet 3 of 4)

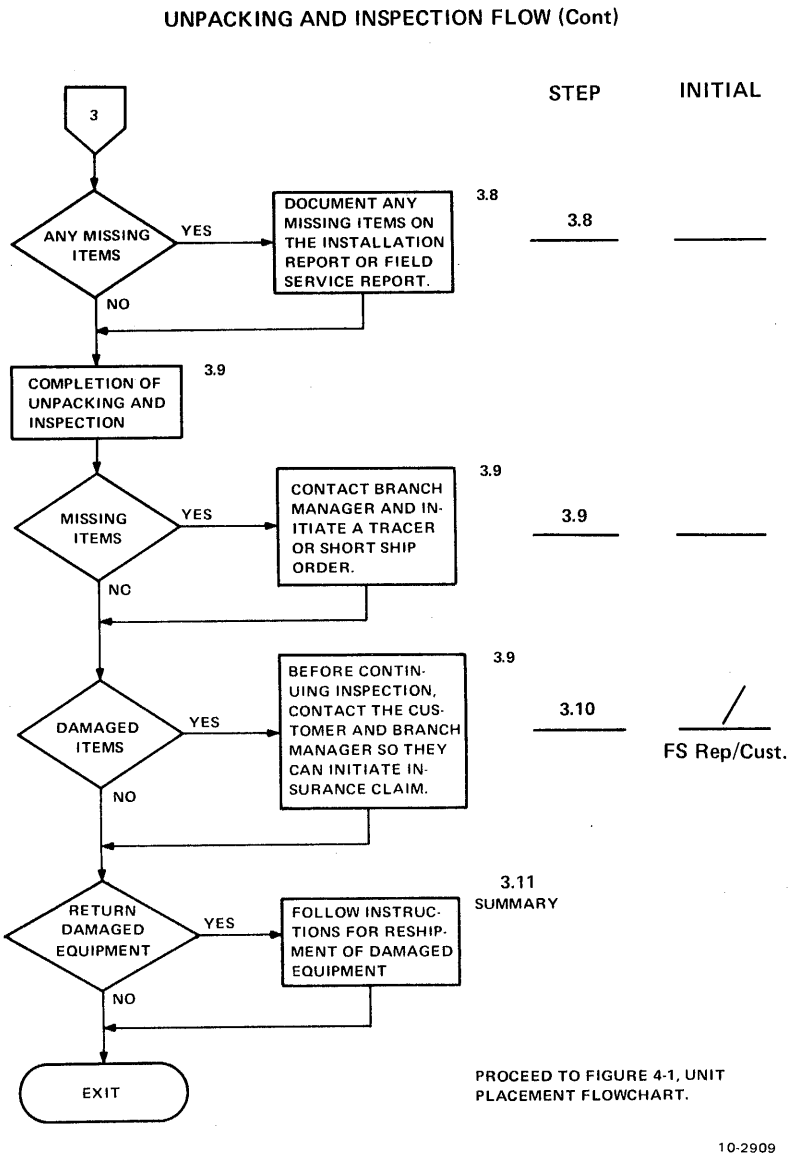


Figure 3-1 Unpacking and Inspection Flowchart (Sheet 4 of 4)

2. Remove the shipping retainer bolts of each expander chassis, or peripheral on slides, and inspect the internals of each box and peripheral for damage such as bent pins, and loose or broken modules, switches, lights, or backplanes, etc.

3. Document any damage and call it to the attention of the customer. If the damage is extensive, report the damage to the branch service manager immediately. DIGITAL is not responsible for shipping damage on systems that are FOB from the manufacturing facility. If reshipping equipment back to DIGITAL is required, follow the instructions in Paragraphs 3.10 and 3.11.

3.8 INVENTORY

Inventory each system cabinet and free-standing peripheral to ensure that it contains the items identified on the keysheet or transfer sheet. Also, check the ECO REV level and serial numbers against the keysheet or ECO status sheets. Document any missing items, wrong serial-numbered item, or incorrect revision level item on the installation report or field service report. Ensure that the missing item is not covered by a waiver or an approved partial ship. Also, update the keysheet if ECO status does not appear on it.

NOTE

If the keysheet is missing, stop the installation and call the branch service manager to locate the keysheet or transfer sheet.

Documentation is provided in the customer envelope to allow the customer and the field service person to answer the following inventory questions.

1. Have all the cartons and boxes been received?

   Using the shipper's waybill, the number of containers should be counted to ensure that none were lost in shipment. If any are missing, the shipper should institute a trace or insurance claim at the customer's request.

2. Are all of the options which the customer ordered present?

   Using the Actual Cost Jobs Closes or Transfers sheet, the system configuration should be inventoried for correct content and quantities of options. This form indicates what was ordered from the manufacturing group.

3. Are all the accessories which should accompany the options and system present?

   Using the accessory shipping lists, count and check as received every item contained in the boxes.

NOTE

Check the customer's envelope for waiver forms which indicate that items have been backordered and will be shipped separately. Do not order waivered or partialed items as short shipped.

If all items and parts have been received, inform the customer and continue with the installation following the installation and acceptance procedures (Paragraph 3.10).

3.9 MISSING PARTS PROCEDURES

This paragraph defines an order short shipment, and the procedures for processing a short shipment P1 request through Field Service Logistics. It also outlines the procedures to follow when a missing item other than a short shipment is encountered, with the responsibilities identified for each organization. An overview of a short shipment is presented in Figure 3-2 and a detailed flowchart in Figure 3-3.

A short shipment is an item or items identified on the shipping document as required to ship with the order, but which inventory shows to be missing from the shipment. Paragraph 3.9.1 describes the procedures to follow in case of short shipment.

If a required item is missing and is not listed on one of the shipping documents as having been shipped or as required to ship, proceed to Paragraph 3.9.2.

NOTE

If the customer is performing the installation and finds material missing, then the customer should directly contact an account salesperson with the list of missing parts.

3.9.1 Short Shipment Procedure

If an item is listed on one of the shipping documents as required to ship but it cannot be found when the installation inventory is performed, it is short shipped. Contact the branch logistics administrator and provide the following information.

DEC No.
Product Line
System Type
System Serial No.
Customer Name
Part No.
Part Description
Quantity

The branch logistics administrator will then assign an SBA number to the request and TWX it to the regional logistics center with the following additional information.

The branch office contact name and location
The SBA No.
Branch DECNET code

NOTE

When the materials requested are low cost and readily available in the branch or regional stockroom, they should be used and the short ship P1 request should be filled in at that point. The materials used should then be charged to the installation activity and product line. The intent is to ensure that the customer will be serviced efficiently.

The regional logistics center should check stock upon receipt of the short ship P1 request as noted above. If parts cannot be released due to cost or availability, retransmit the TWX to the Woburn P1 group immediately.

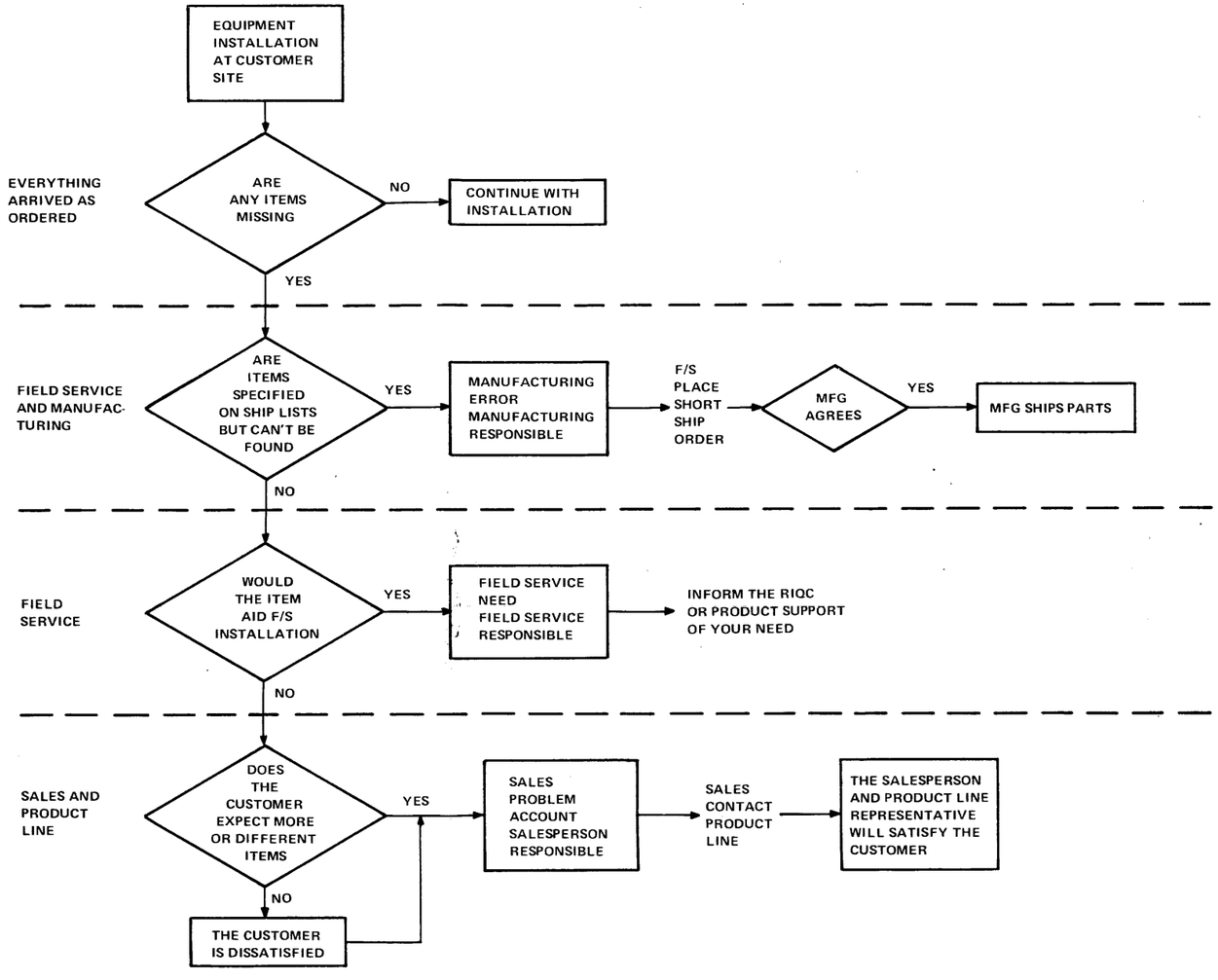


Figure 3-2 Installation Short Shipment Procedures – Overview

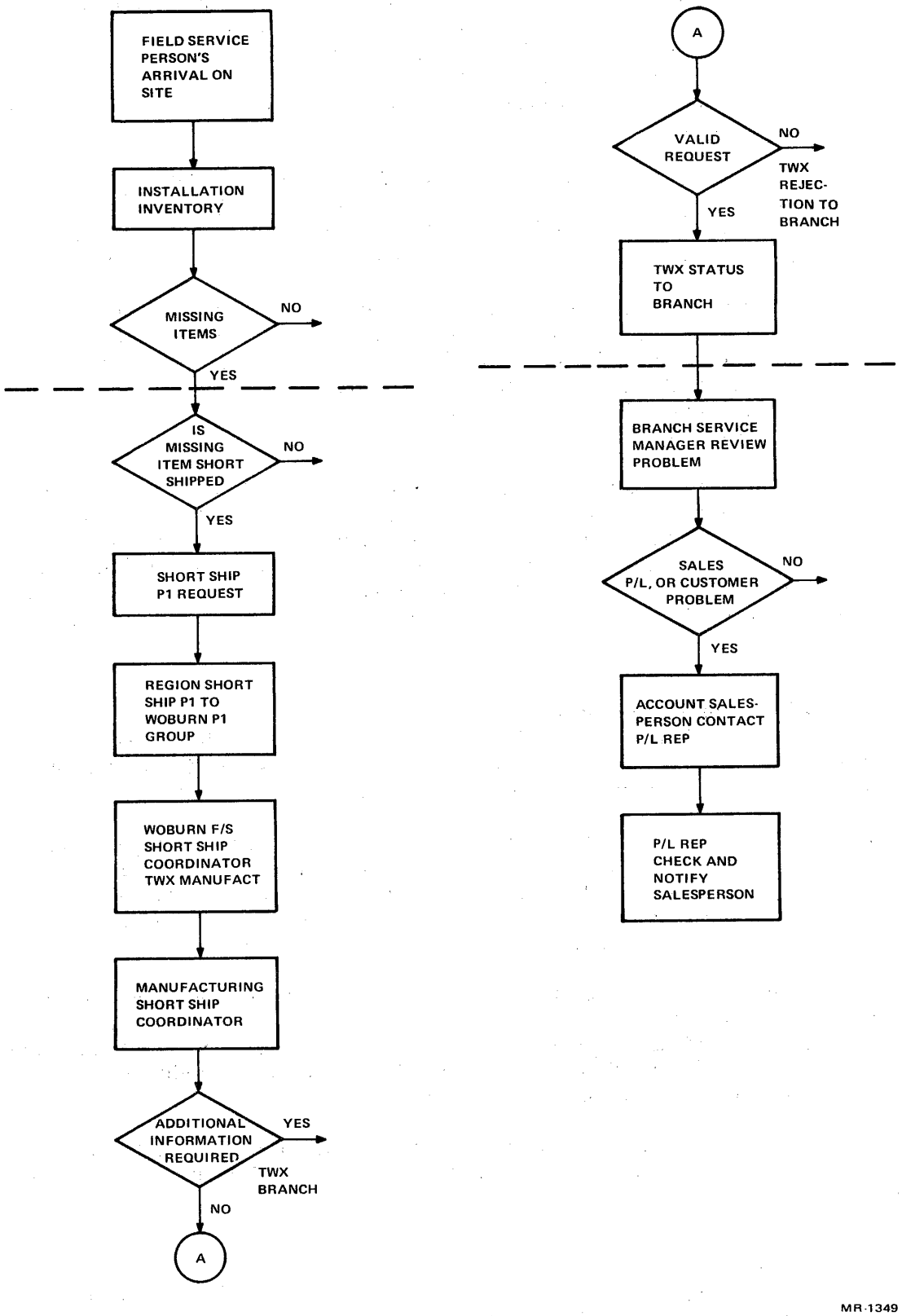


Figure 3-3 Detailed Short Shipment Flowchart

The Woburn P1 group will log the short ship request, and TWX directly to the responsible manufacturing short ship coordinator as listed by manufacturing within two hours of receipt. Each manufacturing group in each plant has a designated short ship coordinator in its facility who will receive the short ship request from Woburn and will verify the request. The responsibilities of the field service short ship coordinator, from this point, will be to monitor and log the status of the request as received from manufacturing until the SBA has been closed.

If the manufacturing short ship coordinator needs additional information, TWX questions should be sent directly to the requesting branch, with a copy going to the field service coordinator in Woburn for logging. A response from the branch should go directly to the individual requesting the information in manufacturing within 24 hours. When the branch responds, the request will resume processing.

The manufacturing short ship coordinator will check the request against the manufacturing records. If it is determined that the request is not valid a TWX will be sent to the branch rejecting the order with the reason why it is being rejected. A copy of the TWX will also be sent to the logistics coordinator who will then close the SBA. Appeals (when deemed necessary by the branch service manager) should go directly to the person sending the rejection TWX if there was miscommunication, or to the account salesperson for product line or customer resolution.

If the request is valid, the manufacturing short ship coordinator will TWX the P1 request status directly to the branch with a copy to the logistics coordinator, giving parts availability and an estimated time of arrival. If the parts will not be readily available within two days, the manufacturing coordinator will make the appropriate contact with the product line to authorize other priority acquisition procedures. In any case, status of the short ship P1 request should be sent by the manufacturing coordinator directly to the branch contact within 24 hours of the time manufacturing received the request.

3.9.2 Non-Short-Shipment Missing Items

The installing field person should provide the branch service manager or branch supervisor with the details of the problem encountered. It should be made clear that this is not a short shipment but that it prevents continuation or completion of the installation or customer acceptance.

Having collected the complete information, the branch service manager should work with the customer's account salesperson to determine whether the item requested is a service aid or customer-required. A service aid is an item or tool that field service could use to improve the installation or checkout process. If the missing item is a service aid, information should be documented and sent to the proper support supervisor or the regional installation quality coordinator.

If the item is required by the customer, the account salesperson for the customer will gather all the relevant details and contact the appropriate product line representative. The product line representative will check the details and respond within 24 hours directly to the salesperson with the findings, the action to be taken and the time it will require. It is the salesperson's responsibility to notify the service manager and the customer of the information received.

The product line representative will arrange directly with manufacturing for all materials to be scheduled and shipped if it is determined to be the obligation of DIGITAL or in the best interest of the customer.

3.10 COMPLETION

This completes the unpacking and inspection phase. Documentation of the entire system should be intact at this time. Notify the branch service manager or branch supervisor of any discrepancies noted during this phase. If no discrepancies exist, the customer should initial the last entry in Figure 3-1 signifying agreement with the inventory and inspection. Then continue to Chapter 4.

If discrepancies such as damage do exist, the branch supervisor may want the customer to initiate an insurance claim. For missing items, the branch service manager or branch supervisor should initiate a short ship request (Paragraph 3.9.1). All other problems should be discussed with the branch service manager or branch supervisor.

Customer claims on damaged equipment may be difficult to obtain if the equipment in question has been removed from the skid. Therefore, if any damage exists, the damaged equipment should not be deskidded or moved until authorized by the branch service manager. The customer is responsible for payment of the replacement or repair of damaged equipment. This arrangement will be discussed between the customer and the branch service manager. If damaged equipment is to be returned to Digital Equipment Corporation, the procedures in Paragraph 3.11 should be followed.

3.11 RETURNING DAMAGED EQUIPMENT

Any piece of equipment to be shipped to Digital Equipment Corporation, as a return authorization from the field, must be transported on a proper skid or in the container in which it was shipped. If the equipment has been removed from a skid and the skid is not available, a replacement must be ordered from the Maynard traffic department or Stockroom 17.

Skids may also be manufactured in the locality of the customer site. All part numbers, specifications, and associated hardware are documented in print set D-PS-1210568-0-0.

Part of the customer's upgrade contract is that the customer is liable for all rigging and transportation charges; therefore, the customer can be billed for the skids and associated hardware.

A sample of various devices is listed below, along with the respective skid part numbers.

Options	Skid Part No.
RP04/06	12-10568-2
LA36	9405651
LP20-A,B	12-10568-5

When a return authorization has been validated by DIGITAL and a skid has been procured, the procedure for loading a piece of equipment for reshipment to DIGITAL is as follows.

1. Remove the end panels and front and rear outer doors.
2. Raise the leveler feet.
3. Carefully place the equipment on skids.
4. Tighten the shipping bolts and lower the leveler feet. Also, lower any stabilizer feet levelers (if applicable).
5. Check to be sure that all shipping brackets for sliding chassis are in place and all module hold-down bars are secured.
6. Replace all end panels and doors, securing the doors with door holders.
7. Crate the cabinet appropriately; i.e., use a polyethylene bag, corrugated wraparound, etc.

CHAPTER 4
UNIT PLACEMENT

4.1 EQUIPMENT MOVEMENT (See Figure 4-1.)

Move all boxes to the computer area. If inventory is complete and Figure 3-1 is initialed by the DIGITAL representative and the customer, properly store the documentation (e.g., prints, manuals, diagnostics, write-ups, etc.) in the storage facility – preferably a cabinet with shelves. (A storage cabinet is usually supplied by the local field service branch.) This facilitates a smoother and more organized installation and eliminates searching for prints, manuals, or diagnostics in the various boxes.

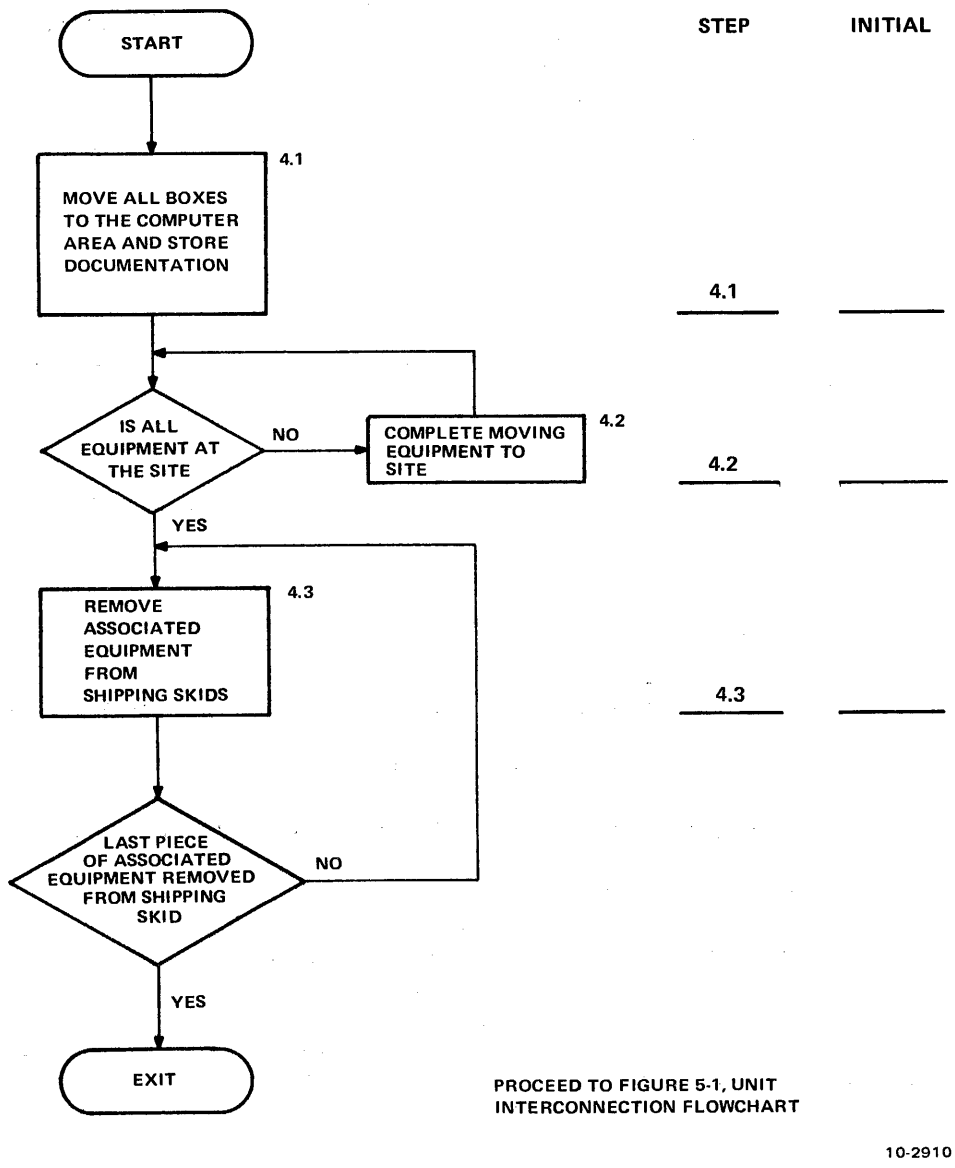


Figure 4-1 Unit Placement Flowchart

4.2 KL10-C (2040) CABINET HANDLING (Figure 4-2)

Obtain the site layout sheet from the customer. Also, obtain the configuration sheet; some part lists include it in the shipping documentation. Move the system cabinets to the computer area.

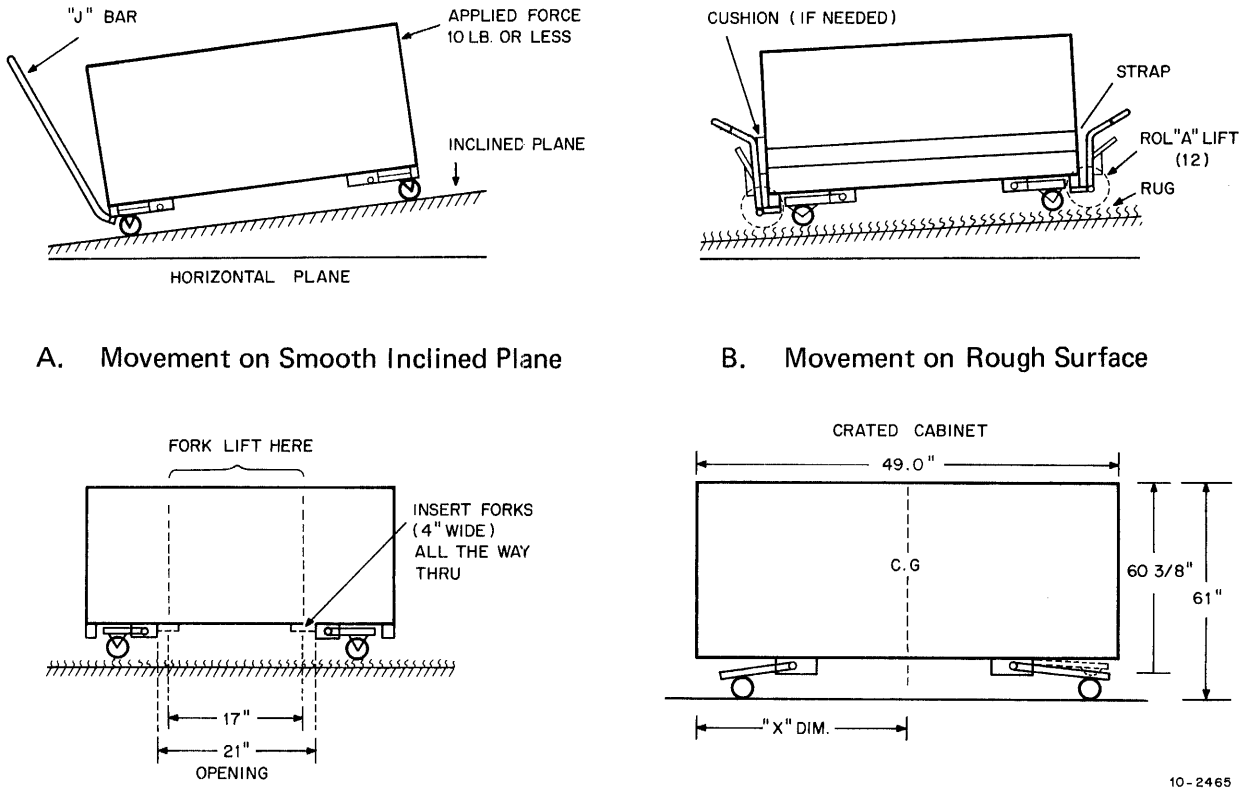


Figure 4-2 Unit Movement

The following procedures should be followed for handling the double-width Hi Boy cabinets.

1. At least two workers are required to handle each cabinet.
2. When cabinets are to be pushed over steps (steel ramps over steps), riggers may be hired.
3. Cabinets are to be handled one at a time.
4. While loading or unloading cabinets on a ramp, a "come-along" (a type of block and tackle) should be used to prevent loss of control over cabinet.
5. A "J" bar or a "come-along" should be used in these situations: when moving cabinets on a smooth inclined plane having a pitch greater than 1 inch per foot (such as in corridors, hallways, etc.); or where a cabinet is at rest on an incline plane of less than 1.4 inch per foot but an applied horizontal force of less than 10 lb could move or slide the cabinet in either direction. See Figure 4-2A.

6. When moving such cabinets over any kind of carpet or rough floor, a "roller lift" is recommended to prevent damage to flooring or equipment. See Figure 4-2B.

7. If the cabinet is to be pulled over steps, or gaps or crevices greater than 1/4 inch between buildings, partitions, etc., a flat steel plate or ramp should be used.

8. Fork-lifting the cabinet can be accomplished if forks are inserted as shown in Figure 4-2C.

4.3 DESKIDDING ASSOCIATED EQUIPMENT

Carefully deskid all equipment associated with the DECSYSTEM-20.

4.4 REQUIRED TOOLS

The tools required to deskid and install a DECSYSTEM-20 computer system are listed below.

1. Basic Tool Kit (7606864)

DEC Part No.	Description
29-13456	Nut driver set
29-13457	Adjustable wrench
29-13460	Diagonal cutting pliers (95ELH-EREM)
29-13462	Miniature needle nose (UTICAB5317)
29-13463	Pliers, 6-1/2 inch
29-12573	Ratchet offset screwdriver
29-13466	Utility knife (Xacto no. 51ST)
29-13467	Wire strippers
29-13468	4 inch × 5/16 inch screwdriver
29-13470	No. 0 Phillips screwdriver
29-13471	Trimpot screwdriver
29-13472	No. 2 Phillips screwdriver
29-13474	6 inch round smooth cut file
29-10779	6 inch half-round smooth cut file
29-13515	Thickness gauge set
29-13451	Solder pullit
29-10780	Penlight
29-13461	Needle-nose pliers
29-12574	Phillips stubby screwdriver
29-13459	Allen wrench set
29-12559	Tweezers, no. 151392
29-12575	Valve spout oiler no. 990034
29-12567	Service case

2. Additional Tools Required

DEC Part No.	Description
29-12529	Screw holder
29-12577	Miniature combination wrench set
29-13452	Soldering iron
29-19333	Soldering iron tip
29-13512	Burnishing blade
29-13513	Unwrapping tool – 24 gauge
29-18387	Unwrapping tool – 30 gauge
29-13450	Handwrap tool – 24 gauge

29-18301	Handwrap tool – 30 gauge
29-10246	IC clips (2)
	Large adjustable wrench
	Hammer
29-13455	Crimping tool for Faston connectors
	Tightening tool for Faston connectors
	1/4 inch drive ratchet and socket set and level

4.5 FINAL CHECKS

When the equipment is situated in the site location, perform the following procedures in the order listed.

1. Check the pins on the backplane, making sure none of the pins is bent or smashed.

2. Check all Faston type connectors, making sure they are all tight.

3. Check all modules and cables, making sure they are properly seated and in their correct slots.

4. Beginning with the topmost circuit breaker on the main power box, check to ensure that each power cable is correctly labeled, both on the cable and at the box.

5. Use a digital voltmeter (DVM) to ensure that all power phases are correct.

6. Ensure that all circuit breakers within the main power box are in the OFF position.

CHAPTER 5
UNIT INTERCONNECTION

5.1 EQUIPMENT POSITIONING (Figure 5-1)

Starting with the KL10-C (2040) central processor and extending outward, position all the associated DECSYSTEM-20 equipment according to the accepted floor layout plan.

5.2 BOLTING FRAMES

Bolt all frames together (where applicable) and/or install end panels.

5.3 KL10-C (2040) CABINET INSTALLATION AND INTERCONNECTION

Paragraphs 5.3.1 through 5.3.5 list the procedures for interconnecting the KL10-C cabinets.See Figures 5-2 through 5-9. The cabinets are identified as follows.

Cabinet 1 - Front end
Cabinet 2 - I/O
Cabinet 3 - CPU

WARNING

Before beginning this set of instructions, ensure that the main power line cord is unplugged from the wall receptacle and no peripheral equipment is connected to the machine.

Table 5-1 lists the parts needed to assemble the three processor cabinets. These parts should be kept in a container and no parts should be discarded unless noted.

5.3.1 Cabinet 2 - Cabinet 3 Assembly (Figures 5-2 - 5-4)

1. Place rear arm stabilizer on all cabinets (Figure 5-5).
2. Place leveling feet under all cabinets and secure with screws (Figure 5-6).
3. Remove doors and air inlets, top covers, filler strips, and ground straps for ease of bolting cabinets together.
4. Place level on top rail of cabinet.
5. Level base of cabinet on x-y axis by adjusting leveling feet (Figure 5-7).
6. Bring CPU cabinet in contact with I/O right side as viewed from the front.
7. Raise CPU cabinet until lower bolting plate holes are in line with I/O cabinets by raising leveling feet (left front and rear as viewed front).
8. Bolt down the two lower bolting plates with lower plates of CPU cabinets.
9. Bolt middle and upper bolting plates.

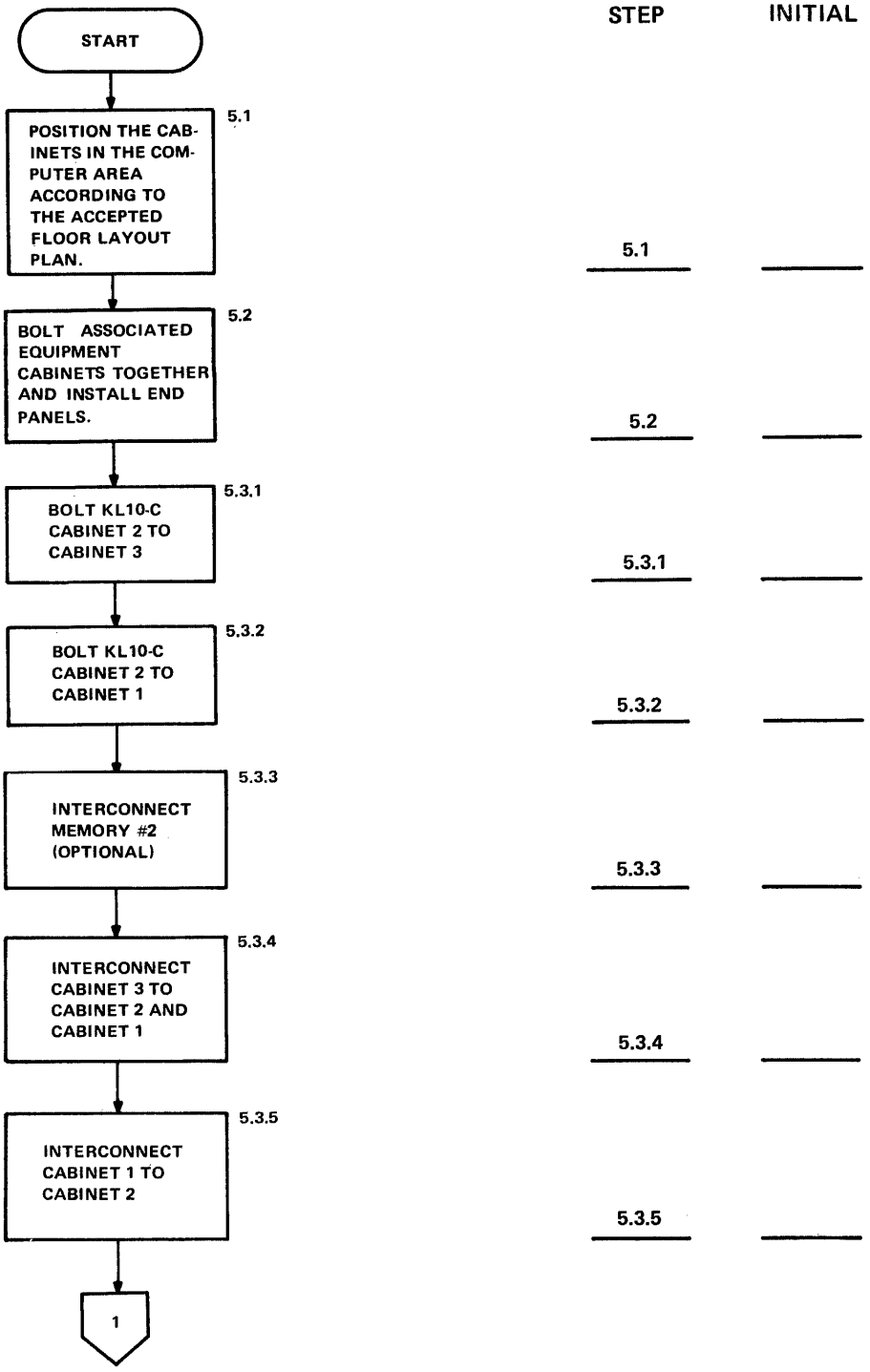


Figure 5-1 Unit Interconnection Flowchart (Sheet 1 of 3)

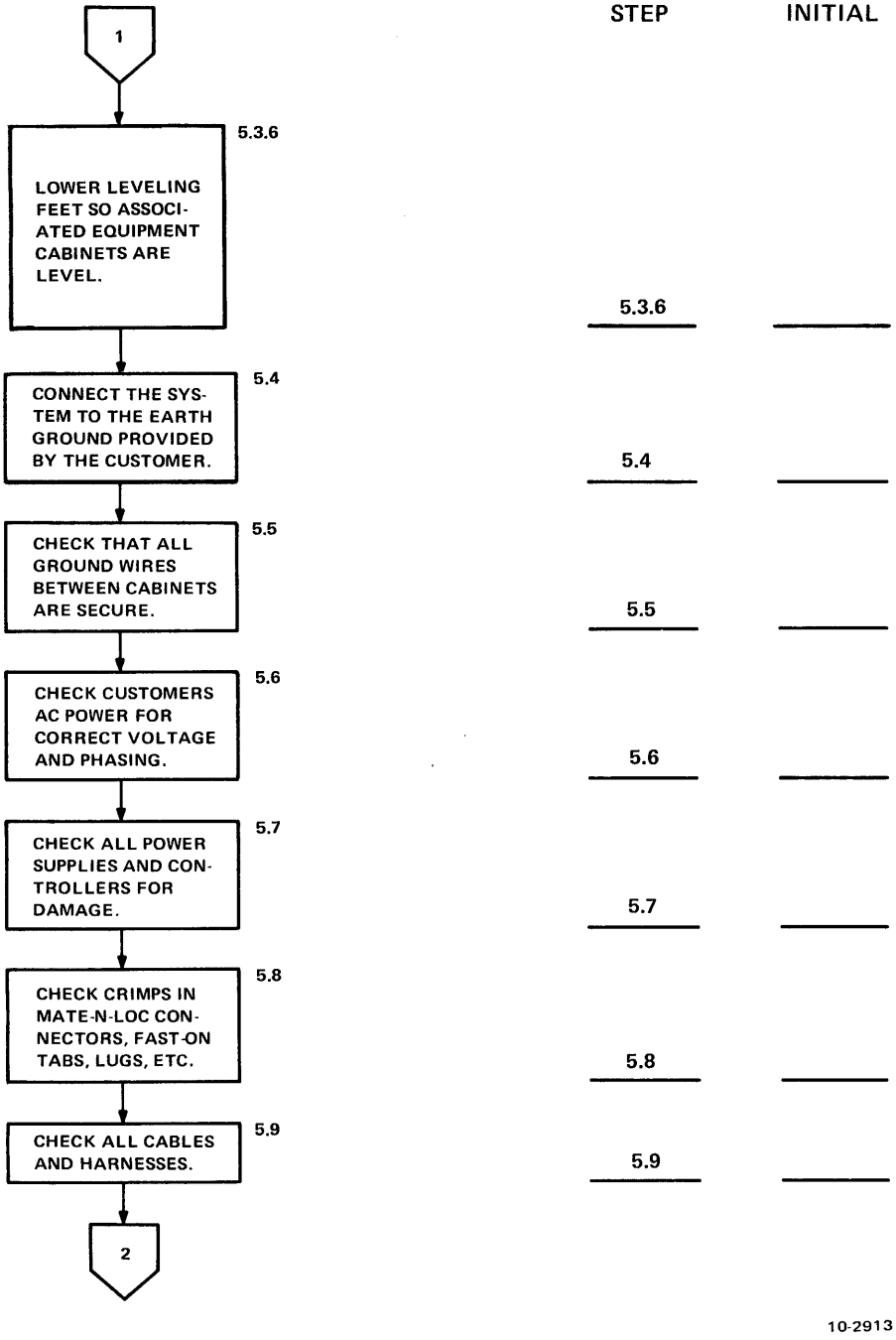


Figure 5-1 Unit Interconnection Flowchart (Sheet 2 of 3)

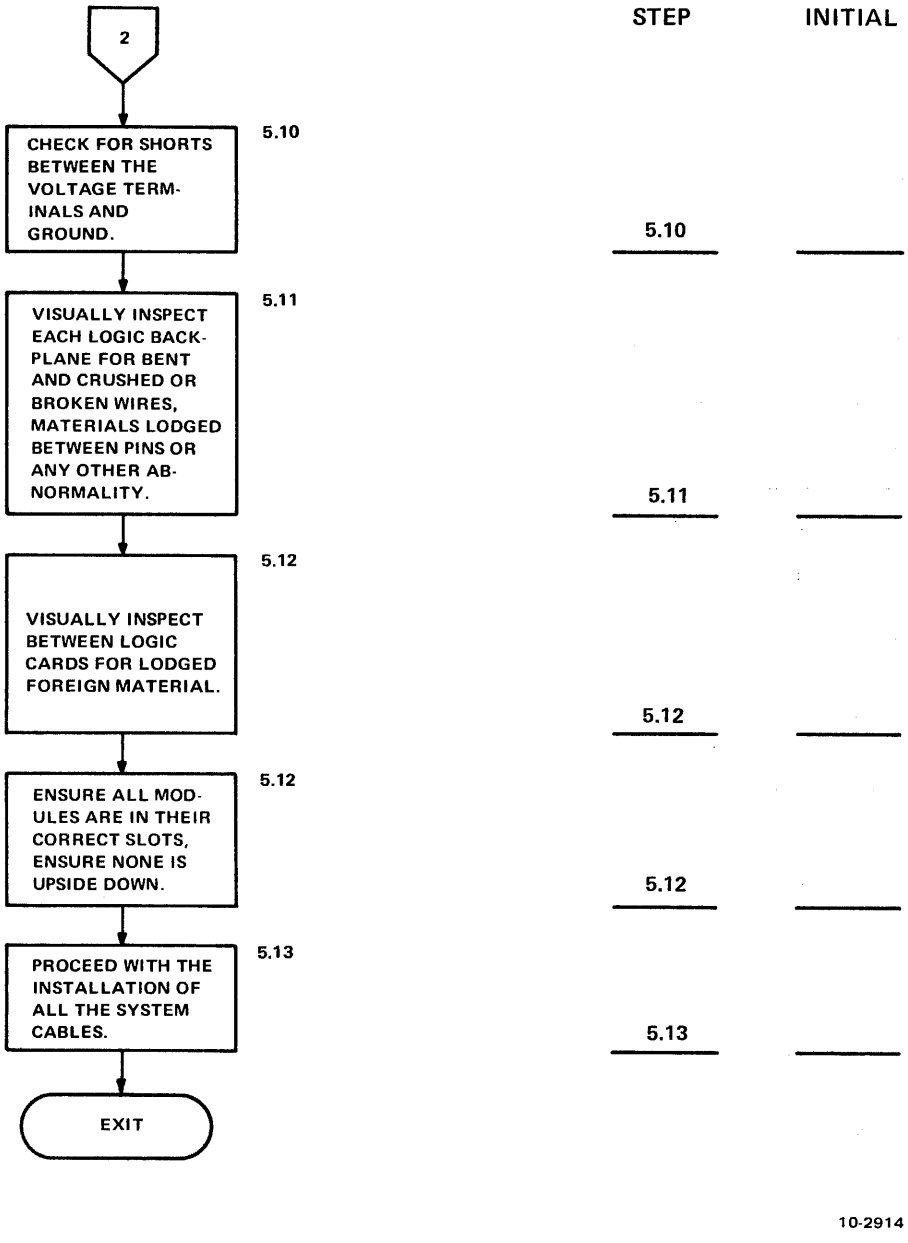


Figure 5-1 Unit Interconnection Flowchart (Sheet 3 of 3)

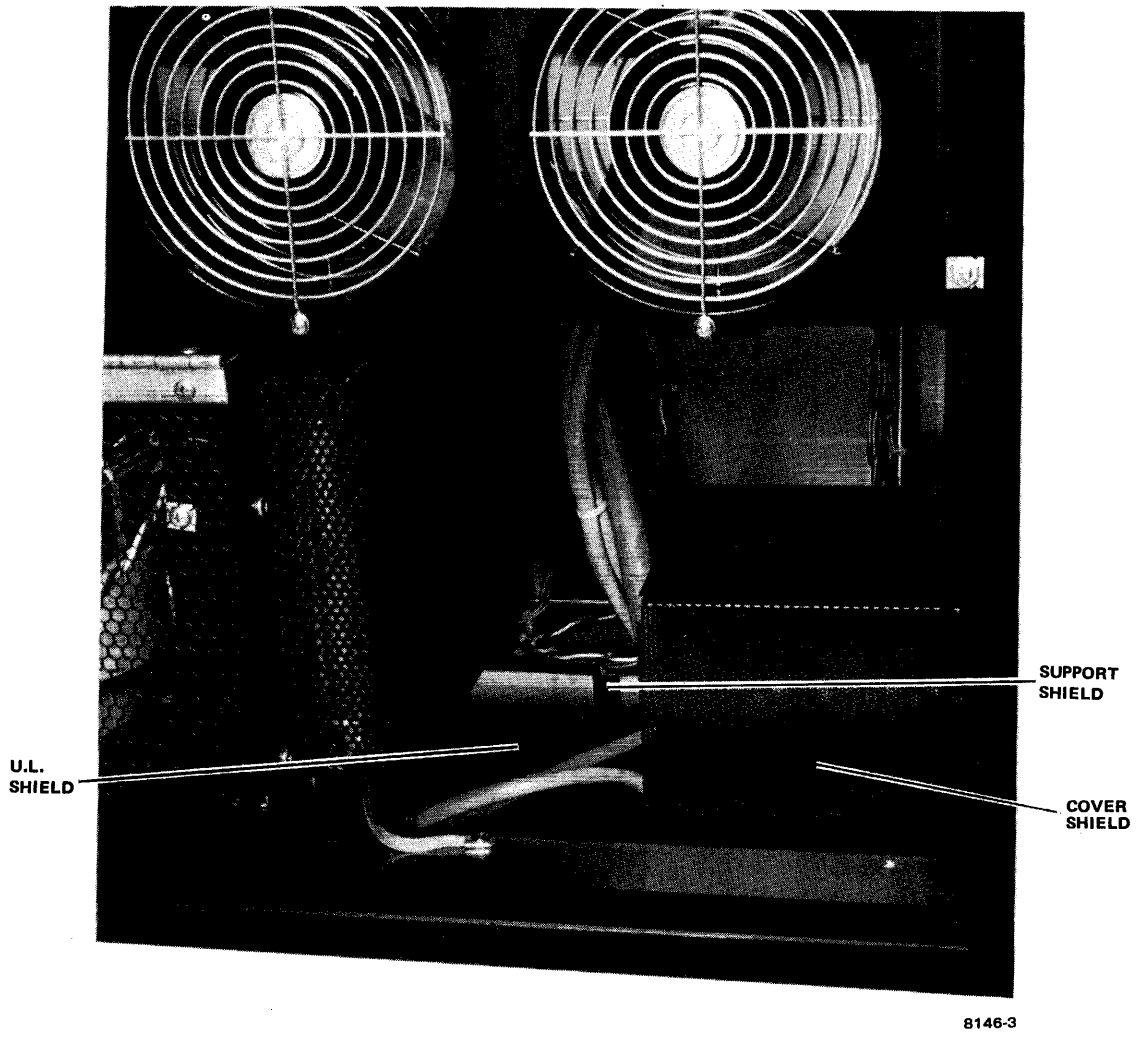
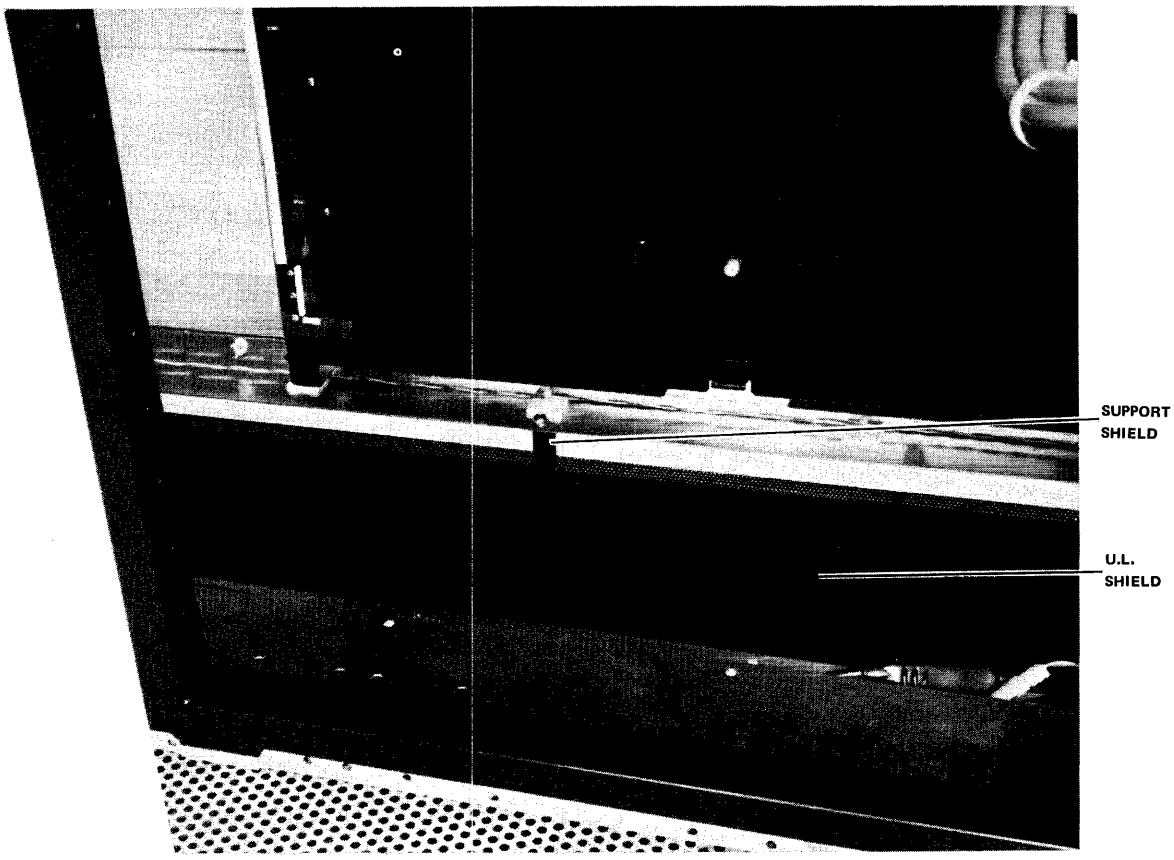


Figure 5-2 I/O Processor Cabinet (Rear View) –
Cover and U.L. Shields Showing Power Cable, Massbus,
and Ground Cables



NOTE:
Support shields are installed with screws and U. L. shield rests on top of them.

8146-2

Figure 5-3 CPU Cabinet (Rear View) – Support Shield and U.L. Shields

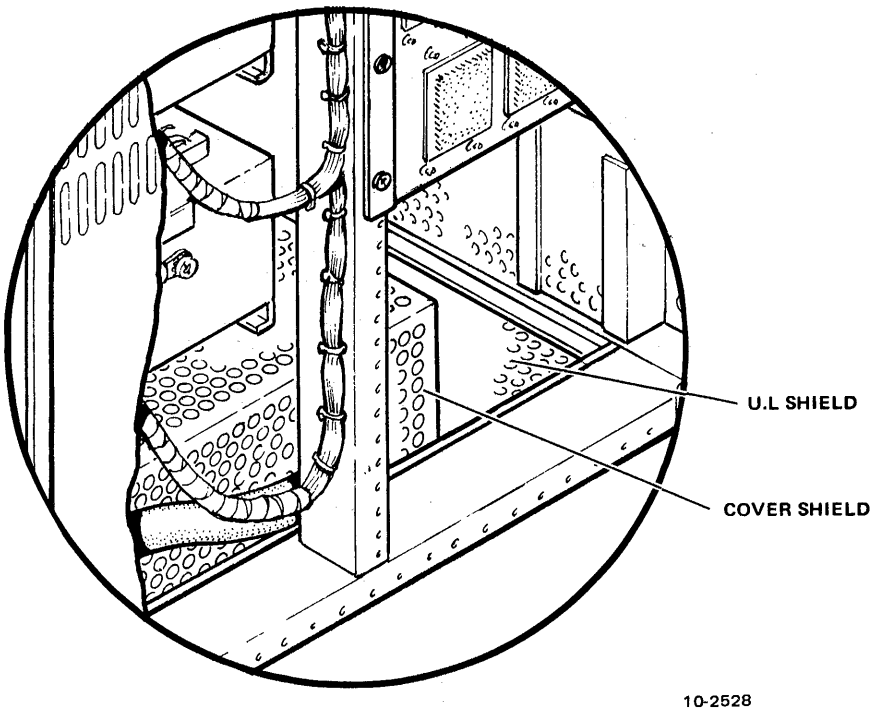


Figure 5-4 I/O Processor Cabinet (Front View) – Cover and U.L. Shields

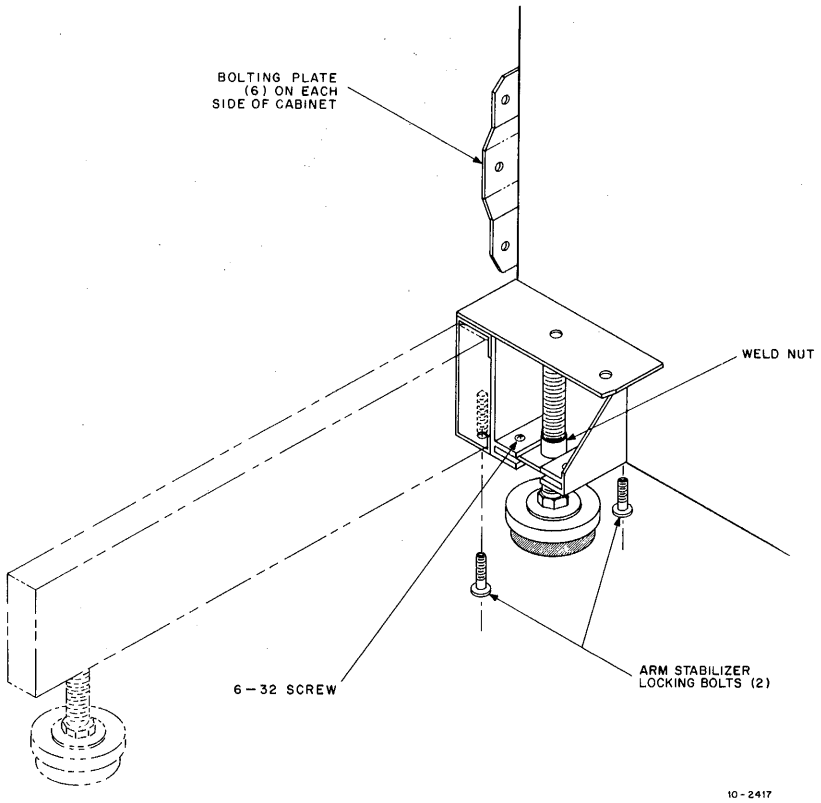


Figure 5-5 Arm Stabilizer Detail

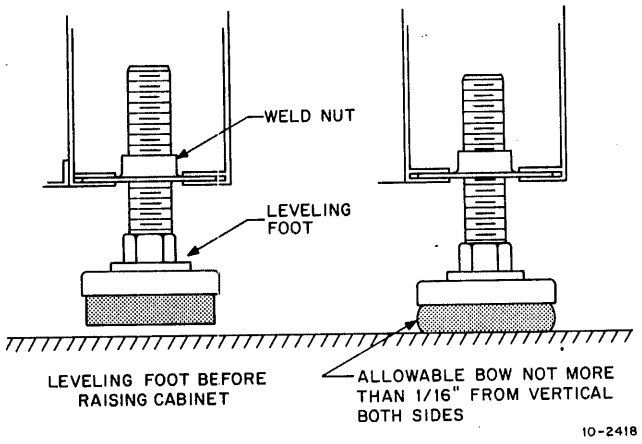


Figure 5-6 Leveling Foot Detail

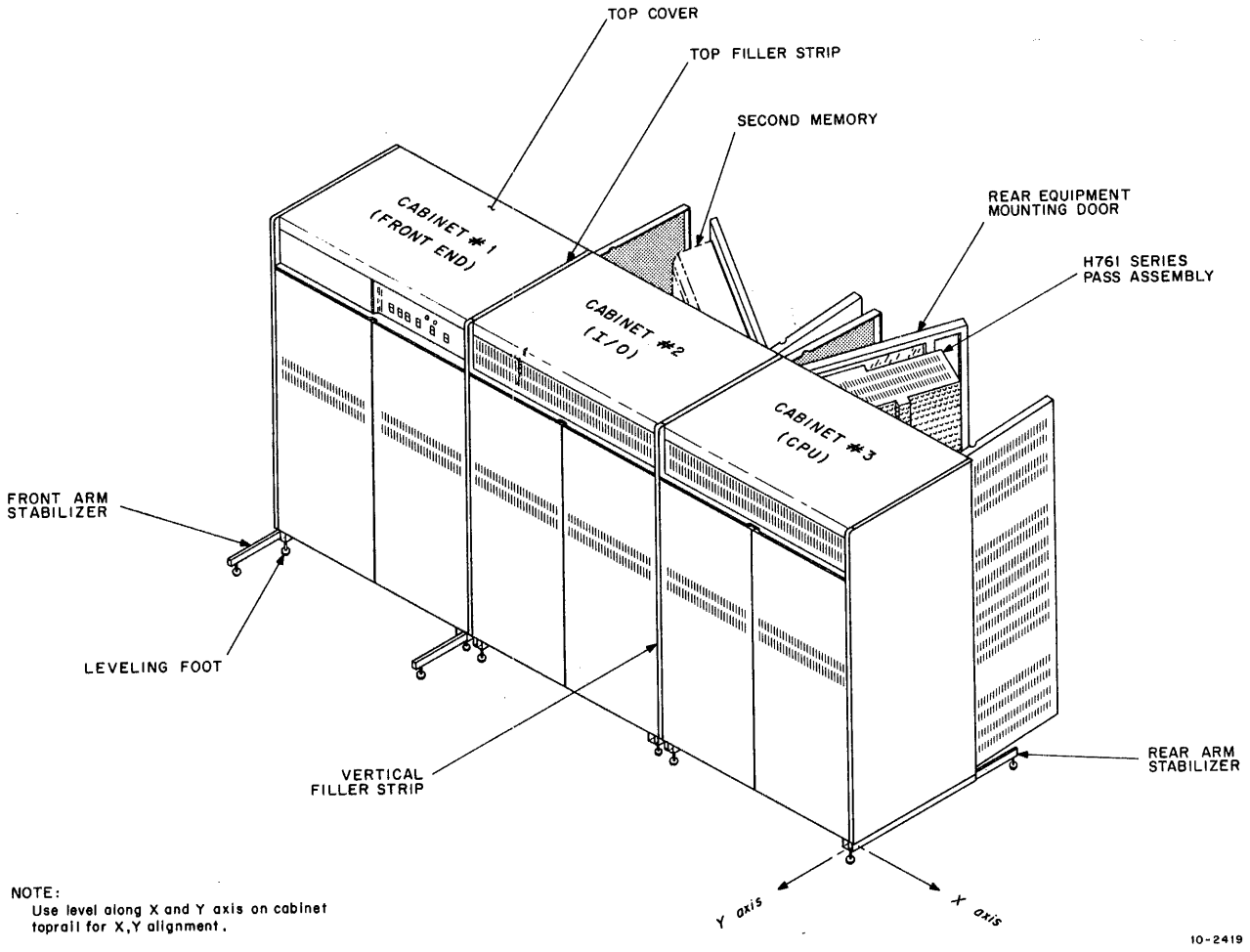


Figure 5-7 Exterior Assembly and Leveling Detail

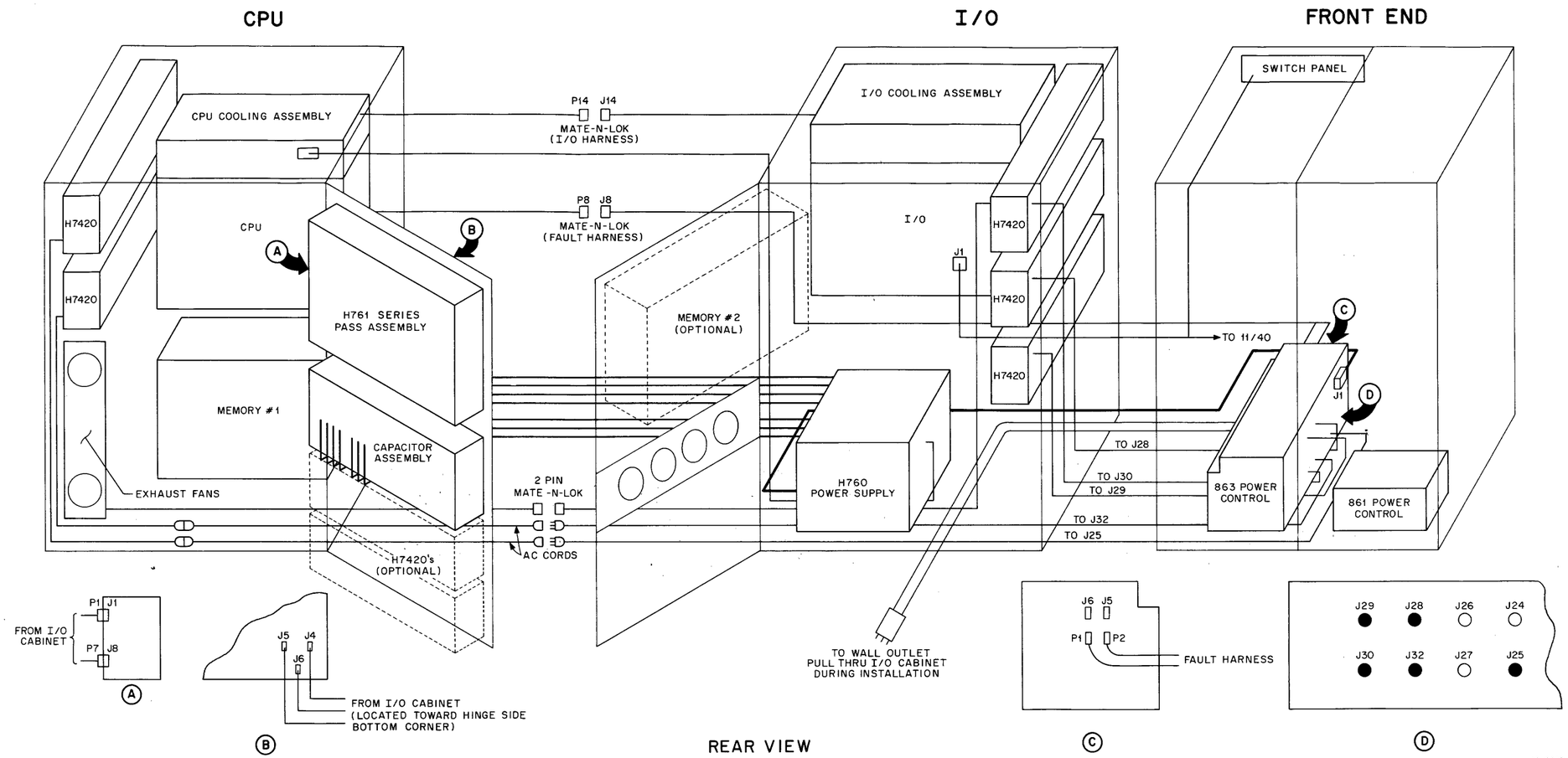


Figure 5-8 Central Processor KL10-C Connections

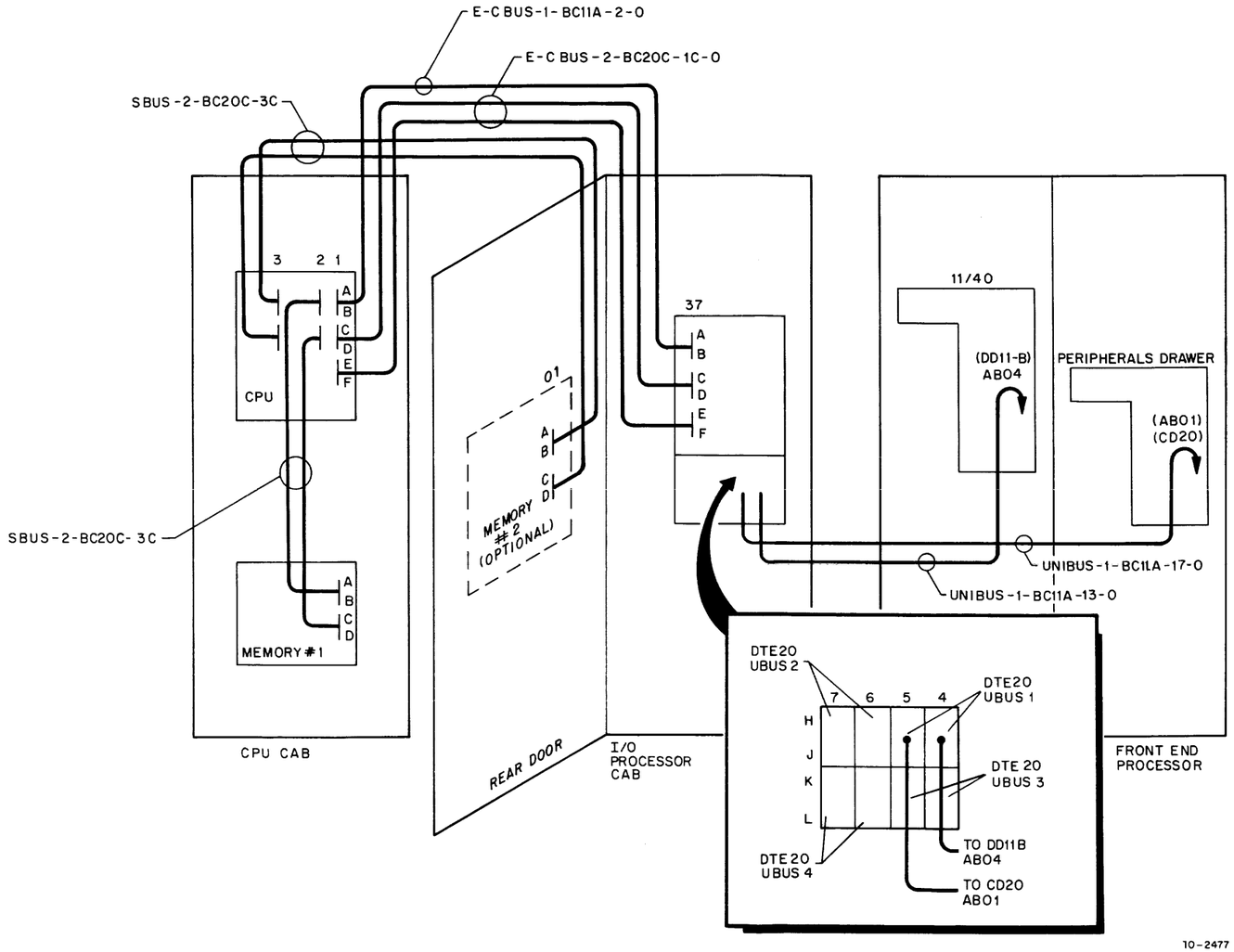


Figure 5-9 Signal Interconnections (KL10-C)

Table 5-1 Parts Required to Assemble CPU Cabinets

No. Needed	Part No.	Description
4	70-11838	Filler bar assembly
2	74-14403	Top filler strip
1	70-12196	Shield weldment
3	74-15268	Support shield (Figures 5-2 – 5-4)
5	74-15394	U.L. shield (Figures 5-2 – 5-4)
1	74-15476	Cover shield (Figures 5-2 – 5-4)
2	Bolting package	For Hi Boy cabinets
	(6) 9006241-9	No. 1/4-20 ±0.5 hex head screw
	(6) 9006724	No. 1/4 external-tooth lock washer
	(6) 9008203	No. 1/4-20 Kep nuts
2	Hardware package	For filler strips
	(20) 9006071-3	No. 10-32 ±0.38 Phillips truss screw
	(20) 9007651	No. 10 external-tooth lock washer
1	Hardware package	For U.L. shields
	(4) 9006563	No. 8-32 Kep nuts
	(6) 9006055-1	No. 1/4-20 ±0.38 Phillips pan head screw
	(6) 9009025	0.281 ID ±0.873 OD flat washer
	(6) 9006724	No. 1/4 external-tooth lock washer
2	Hardware package	Ground straps
	(1) 9008887	10 inch ground strap
	(2) 9006565	No. 10-32 Kep nuts
	(2) 9006071-3	No. 10-32 ±0.62 Phillips truss head
	(4) 9007651	No. 10 external-tooth lock washer
6	Hardware Package	Leveling feet
	(12) 9007600	Leveling feet
	(12) 9008878	Weld nuts
	(24) 9008185	Kep nuts
	(24) 9006024-1	Screws

5.3.2 Cabinet 2 – Cabinet 1 Assembly

1. Repeat step 3 in Paragraph 5.3.1.
2. Place shield weldment in bottom of cabinet 2.
3. Slide main power cable from cabinet 1 through U.L. shield weldment on cabinet 2 (see Figure 5-2); at the same time wheel cabinet 1 close to cabinet 2.
4. Repeat steps 8, 9, 10, and 11 in Paragraph 5.3.1 for front-end cabinet (cabinet 1).

5.3.3 Memory 2 (Option) Cabling Interconnections (Figure 5-8)

1. Connect memory 2 harness to H7420 power supplies (2) on cabinet 3 rear door (Mate-N-Lok).
2. Tie wrap harness.
3. Connect pins 3 (white) and 7 (red) to Mate-N-Lok on both H7420 power supplies.
4. Connect memory 2 ac (H7420) cords on cabinet 2 from 863 power control to front-end cabinet (J24 and J26).
5. Tie wrap cords.

5.3.4 Cabinet 3 to Cabinet 2 and Cabinet 1 Cabling Connections (Figure 5-8)

1. Connect number 2 gauge cap wires at capacitor bank to their corresponding labels (5, 6, 7, 8, 9, 10, and 11). Torque to 132 in-lb.
2. Replace strain relief support plate (two screws only), cable routing bracket, and Dakota clamp cover at cabinet 2 – 3 interface.
3. Replace Lexan cover (cap box).
4. Remove U.L. Lexan shield of H761 on rear door of cabinet 3.
5. Attach Mate-N-Loks at H761 connections labeled P1 to J1 and P7 to J8, respectively.
6. Connect color-coded wires J4, J5, J6 to correspondingly color-coded terminals of H761 (Figure 5-8).
7. Tie wrap wires to cable harness.
8. Replace U.L. Lexan shield on H761.
9. Connect CPU blower ac plug (4-pin Mate-N-Lok at blower).
10. Connect BC20 and BC11 cables from CPU to memory 1, memory 2 (if present), and I/O.
11. Connect Mate-N-Lok P14 to J14.
12. Connect Mate-N-Lok P8 to J8.
13. Connect exhaust fans to 2-pin Mate-N-Lok located in bottom of CPU cabinet.
14. Connect ac cords for memory 1 H7420 power supplies.

5.3.5 Cabinet 1 – Cabinet 2 (Front End – I/O Cabling Interconnections)

1. Roll maintenance panel wires (R and B) and (W and B) from cabinet 2.
2. Connect maintenance panel wires (R and B) and (W and B) to DTE (J1 4-pin Mate-N-Lok).
3. Tie wrap wires to cabinet 2.

4. Roll H760 5-conductor extension cord at 863 power control (J1).

5. Connect to 863-J1.

6. Roll all H7420 power cords from cabinet 2 to 863 cabinet 1.

7. Connect all H7420 power cords to their respective 863 jacks (for phase balance) (Figure 5-8).

8. Tie wrap cords to cabinet 1 frame.

9. Unroll Unibus from cabinet 1 to cabinet 2.

10. Connect Unibus to respective DTE connectors as labeled (Figure 5-9).

11. Roll fault harness from cabinet 2 to cabinet 1.

12. Connect fault harness at cabinet 1, 863 power control Mate-N-Loks labeled P1 to J6 and P2 to J5.

13. Tie wrap harness onto cabinet 1.

5.3.6 Leveling Feet

Lower the leveling feet (see Figure 5-6). Ensure that all leveling feet are planted firmly on the floor and that the equipment is all kept level. Raise the I/O cabinet with the leveling feet until rubber grommets begin to bow out slightly (Figure 5-6).

5.3.7 Final KL10-C (2040) Central Processor Assembly

1. Replace cover shield of cabinet 2 with four 8-32 nuts (Figures 5-2 – 5-4).

2. Replace filler strips (6) for all three cabinets.

3. At this point, since all three cabinets are bolted together, there is no need to have the arm stabilizer extended. If traffic around the machine requires the removal of the arm stabilizer, unbolt rear arm stabilizers and slide them in. Arm stabilizers should never be discarded; they should remain on the site in the event there is a future need to break the machine apart.

4. Install U.L. shields and bracket in CPU cabinet (Figure 5-3).

5. Install U.L. shields and bracket in front end cabinet (Figure 5-3).

6. Remove PDP-11-type shipping brackets from front end cabinet.

7. Replace doors, air inlets, top covers, filler strips, and ground straps.

5.4 SYSTEM GROUNDING

Refer to the system grounding scheme as laid out by the installation planner and connect the grounding accordingly.

NOTE

Planning of this ground should have been discussed with the customer during site preparation planning.

5.5 CHECKING GROUND WIRES

Check all ground wires that are connecting the system frames. Ensure that the ground lugs are making firm contact with the metal on the system cabinet frames (e.g., no paint between wire lugs and frames). All ground connections should have lock washers behind the ground strap lugs.

5.6 CUSTOMER VOLTAGE CHECKS

Check the customer's ac power for proper voltage, proper phasing, correctly wired power receptacles, and to ensure that ac ground is connected to all ground pins in all power receptacles for this computer system. Use a DVM. Reference the DECSYSTEM-20 Site Preparation Guide individual option data sheets for ac requirements.

WARNING

It is very important that safety ground be obtained throughout the system to minimize the possibility of injury to personnel or damage to the equipment.

5.7 COMPONENT CHECKS

Check each power supply and controller for damage, loose components, loose screws, or extra hardware that may be laying on or lodged into a component board. Check the fans for the supplies to ensure that cables and harnesses are clear of the fan blades and that the fans turn freely.

5.8 FASTENER CHECKS

Check all the crimps that are in all Mate-N-Lok connectors, Faston tabs, lugs, etc., for solid connections. This can be accomplished by pulling on the wires. If a lug pulls out, reconnect it to its plug and/or jack. Also, ensure that all connectors are seated properly.

5.9 CABLING CHECKS

Check all the cables and harnesses for crushed wires, cut wires, wires smashed together, etc. (especially under logic cabinet door hinges). If any exist, repair or replace the wire(s) or harness.

5.10 SHORT CIRCUIT CHECKS

Using a multimeter, check for short circuits between the voltage terminals and ground on all the power supplies.

NOTE

Usually resistance reading is low, approximately 5 ohms, depending on the load.

5.11 BACKPLANE CHECKS

Visually inspect each logic backplane for bent pins, crushed or broken wires, foreign material lodged between pins, or any other abnormality.

5.12 VISUAL INSPECTION

Visually inspect between every module for any hardware (nuts, screws, washers, etc.) that may be lodged between them. Inspect the entire system including the free-standing peripheral devices. Ensure that all modules are in their correct slots and none are upside-down.

5.13 SYSTEM CABLES (Also refer to Chapter 7)

Refer to the detailed cabling diagram prepared before system delivery, and install the system cables in the order indicated, observing manufacturing cable tags (refer to Chapter 7).

NOTE

All cables should be run from point to point, keeping the following requirements in mind.

1. **All cables (including ground cables) run under the flooring except RP04/06 cables, which run above floor between drives. Refer to the RP04/06 maintenance manual for further information.**

2. **All cables should be labeled on both ends, stating the device type and the slot numbers where they come from and go to.**

3. **Signal cables should not run parallel with power cables, but should cross them at a 90 degree angle.**

4. **Cables should not be drawn tight around cabinet corners or floor posts.**

5.14 CABLE INSTALLATION

Proceed as follows.

1. Install the power cables to all devices.

CAUTION

Check to ensure that all circuit breakers in the main power box and internal to each device are in the OFF position. Also, ensure that all devices are in LOCAL until the system is fully checked out.

2. Connect all device cables (and terminators, if applicable).

3. Connect all the DIGITAL power control bus cables.

4. Recheck all power and system cabling and grounding before continuing.

5. Recheck to ensure that all shipping restraints have been removed.

CHAPTER 6
SYSTEM INTEGRATION

6.1 INTRODUCTION

At this point all internal cabling within the processor should be completed. The remainder of the installation consists of all peripheral devices and their associated interface and power cables.

All device interface cables will be routed into the CPU via a hole cut in a tile of the false floor, beneath the I/O cabinet. An exception is the modem cables which are routed through a hole in the false floor beneath the front end cabinet.

NOTE

All holes should be sealed following final cable placement.

6.2 RP04/06 DISK DRIVES

1. Refer to the ISS Service Manual and RP04 Disk Drive Installation Manual (EK-RP04-IN-001) for RP04 installation procedure, and to the Memorex 677-01/51 Technical Manual for RP06 drive installation procedure.

2. One 3-phase power source may supply up to two drives. If a third or fourth drive is to be used in the system, a separate supply source will be required. Ensure correct voltage settings in the drive.

3. The first drive (drive 0) is always dual-ported. The port switch on the control panel of the drive should be in the A/B position (except while running diagnostics). Additional drives are selected port A.

4. The Massbus cable from channel 0 should always be connected to port A; however, it can be connected to channel 1 during initial checkout.

5. The BC06S Massbus cable from the front end RH11 should be connected to port B. The plug connection at the front end is located below the 11/40 and to the right of the 863 power controller (as viewed from the front).

6. A Massbus terminator should be connected to the OUT slot for port B. If the system has one drive only, a Massbus terminator must be connected to the OUT slot of Port A. For additional drives continue the Massbus cabling and terminate port A of the last drive in the system. Check that W2 has been removed from the terminator (Enable MASSFAIL).

7. Check the drive number selection switches on the M7775 module in each DCL for correct setting (RP04). Set for 0 in RP06.

8. Remove red carriageway hold-down clip (RP04).

9. Remove the shipping hardware (RP06).

6.3 TU45 MAGNETIC TAPE DRIVES

1. Refer to Pertec service manual for drive installation procedure.

2. Connect BC06S Massbus cable between channel 1 and the Massbus connector in the master TU45 drive (if more than one drive is on the system). This is the drive containing the TM02/3 controller. Connect Massbus terminator to the out slot of the Massbus connector. Check for W2 as in step 6 (Paragraph 6.2).

3. Ensure that the six resistor terminator chips on the M8921 are installed in the last drive on the system. Also check that other drives do not have the terminators installed.

4. With more than one drive the slave bus is connected between the MTAs in each TU45. These connections are as follows.

MTA 1st TU45		MTA 2nd TU45
J6	to	SB1
J8	to	SB2
J10	to	SB3

   These cables have been twisted between output and input; i.e., rough side of the cable outermost from the Js and smooth side outermost into the SBs.

5. Connect single-phase power to each drive. Ensure drives are set for correct input voltage.

6.4 LP20 LINE PRINTER

1. Refer to Data Products Service Manual for unit installation.

2. Connect interface cable from the line printer to the LP20 plate assembly connector located to the left of the 863 power controller (viewed from front).

3. Connect single-phase power. Ensure printer is set for correct voltage.

4. Remove the hammer bank shipping clip (located to the left of the bank) if it is on the LP05.

6.5 CARD READER

1. Refer to the appropriate documentation service manual for installation procedure.

2. Remove the two red painted shipping screws from the base of the reader (M200).

3. Connect interface cable from card reader to slot B02 of the CD20 controller in the peripheral expander box.

4. Connect single-phase power. Ensure reader is set for correct input voltage.

6.6 LA36 CONSOLE DEVICE

1. Connect interface cable to 4-pin connector plug located to the right of the 863 power control.

2. Connect power lead to a single-phase power receptacle.

6.7 DC20 COMMUNICATIONS

NOTE
These cables can be connected after the diagnostic checkout for the DC20.

1. Connect the BC05D or BC03M cables to the H317B patch panel and dress the cables as per KL10C vol. I CPU assembly sheets 4, 11, and 12.

2. In many countries, fused barrier boxes are necessary for modem protection. Cables with this type of protection are normally obtained through CSS.

6.8 GROUNDING

Supplied with each system are several no. 4 gauge black ground cables. These cables are connected from earth lugs on the frames of peripheral devices back to the CPU frame. In general they should run parallel to the interface cables. The short (2.5 ft) no. 4 cables are used to connect adjacent devices such as multiple disk drives or multiple magnetic tape drives.

6.9 DN20 SUBSYSTEM

This is a complex subsystem and requires a separate section to cover its complete installation process. Refer to Chapter 2 of the DN2X Communications Subsystem Technical Manual (EK-0DN2X-TM-001) for system integration.

CHAPTER 7
POWER CHECKOUT

7.1 PREPOWER CHECKOUT PROCEDURES (Figure 7-1)

Perform the prepower-up procedures described in the following paragraphs.

WARNING

The H760 power supply produces lethal current. Extreme caution should be observed whenever working with or near the power supply.

NOTE

Some emergency power systems are connected to fire alarm systems. If this is true, be sure the proper customer authorities are notified that power is being applied for the first time.

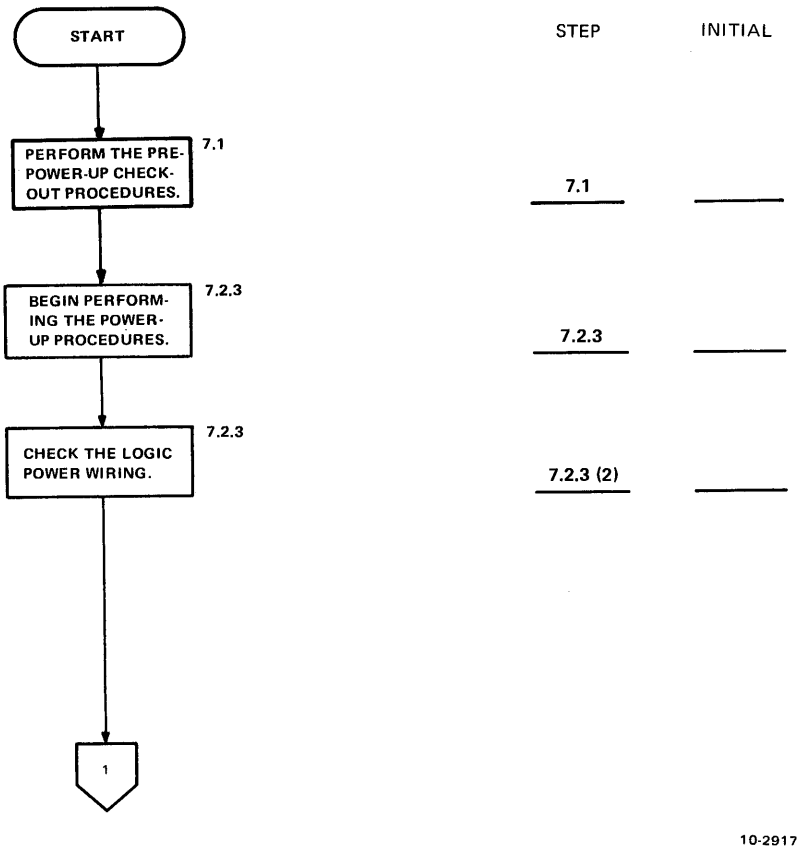


Figure 7-1 System Checkout Flowchart (Sheet 1 of 4)

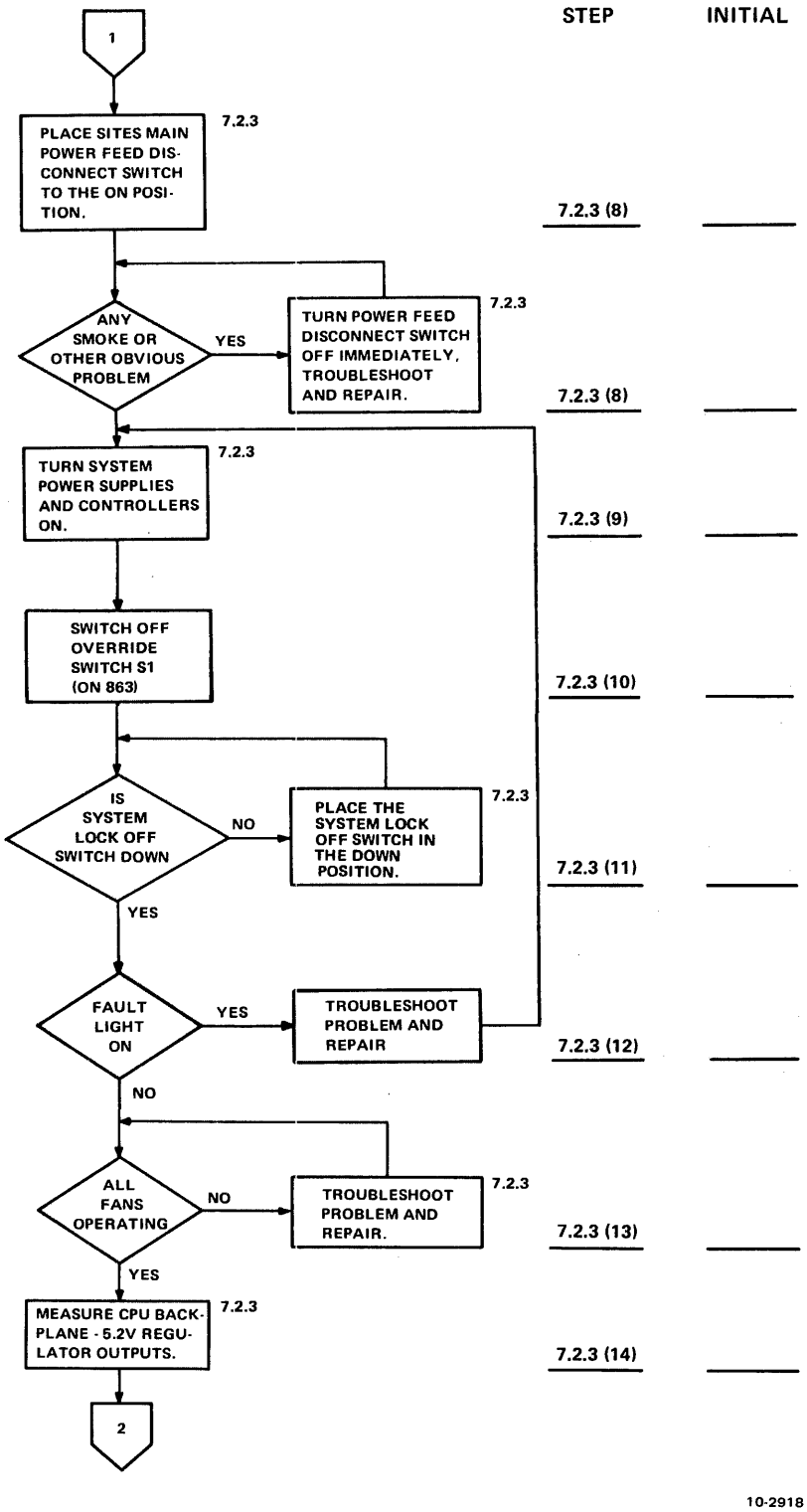


Figure 7-1 System Checkout Flowchart (Sheet 2 of 4)

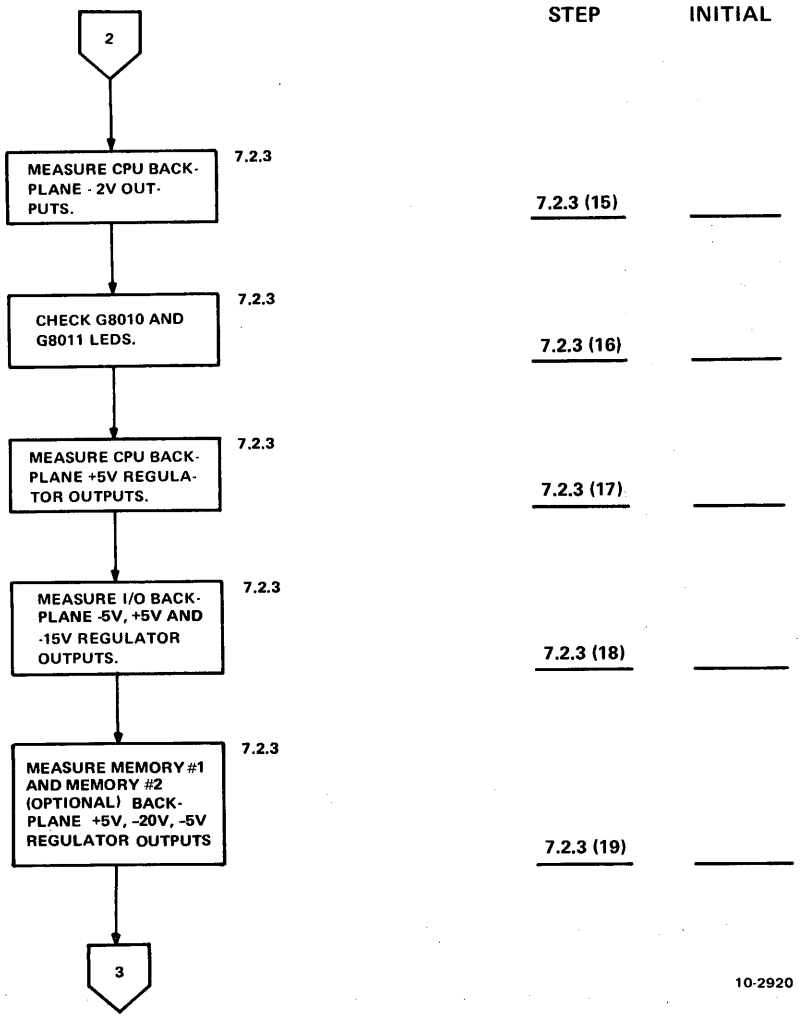


Figure 7-1 System Checkout Flowchart (Sheet 3 of 4)

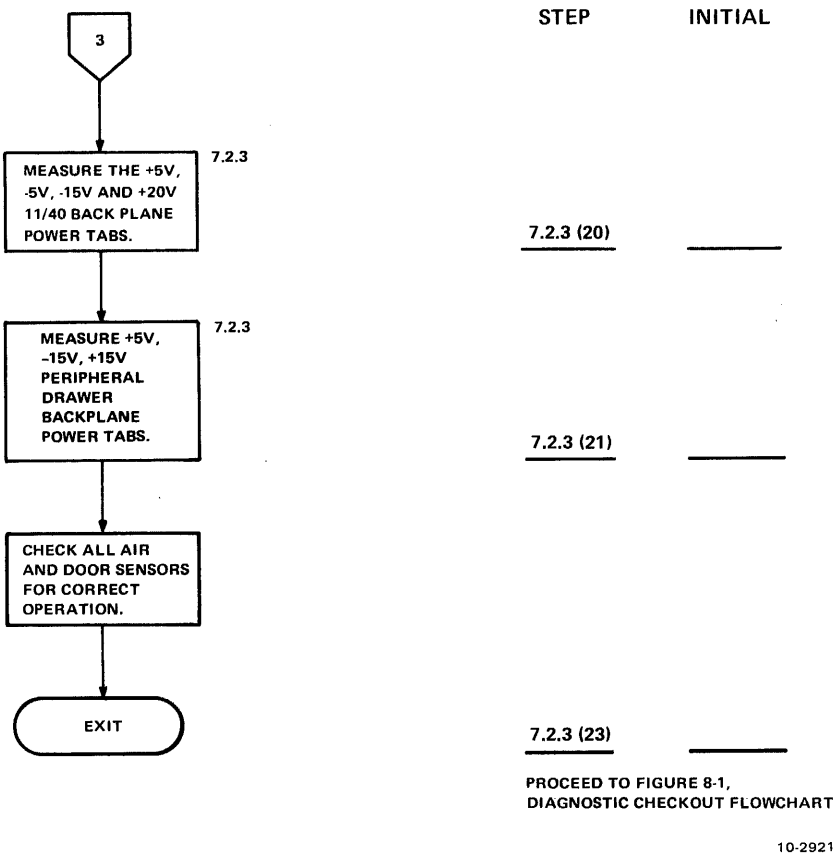


Figure 7-1 System Checkout Flowchart (Sheet 4 of 4)

7.1.1 11/40 CPU - Front End

1. Pull out and fully extend the 11/40 CPU.
2. Check all connections from the H7420 power supply and voltage regulators to the 11/40 power distribution panel.
3. Check to ensure that all harnesses are secured and that all connections are properly made. Refer to the 2040 Console Processor Power Harness Distribution Print Set No. 7011448-0-0 (sheet 6 of 12).
4. Check to ensure that all modules are seated properly.
5. Ensure that the power distribution is correct (refer to the 2040 Console Processor Harness Distribution Print Set).

7.1.2 Peripheral Drawers

1. Pull and fully extend the peripherals drawer.
2. Check all connections from the H7420 power supply and H744 voltage regulators to the peripherals drawer.

3. Check to ensure that all harnesses are secured and that all connections are properly made. (Refer to Arithmetic Processor, D-UA-KL10-C-0, sheet 7 of 12.)

4. Check to ensure that all modules are seated properly.

5. Ensure that the power distribution is correct. (Refer to Arithmetic Processor, D-UA-KL10-C-0, sheet 7 of 12.)

7.1.3 863 Power Control

1. Check the connections of all the J plugs located on the front of the 863 power control.

2. Check the connections of the J2 and J3 plugs located on the rear of the 863 power control.

3. Place the 863 power control LOCAL-REMOTE switch to the LOCAL position.

4. Check to ensure that the OVERRIDE switch is in the OFF (down) position.

7.1.4 861 Power Control

1. Place the 861 power control LOCAL-REMOTE switch to the LOCAL position.

2. Ensure the J3 connection is secure.

7.1.5 H761 Regulated Power Supply

1. Remove screen assembly from H761.

2. Check all Faston tabs and terminal connections in power supply.

3. Ensure proper seating of G8010, G8011, G8013, and G8014.

4. Do not replace screen assembly until voltage checks and adjustments have been completed.

5. Ensure that the J1 and J8 plug connections are secure.

6. Verify that all harnesses and connections are secure and properly made. Refer to the KL10-C print set.

7.1.6 H7420 Power Supplies and Associated Voltage Regulators

1. The H7420 power supplies and associated voltage regulators are located in the CPU and I/O cabinet.

2. Verify that all harnesses and connections are secure and properly made.

7.2 SYSTEMS CHECKOUT

The systems checkout procedures flowchart is shown in Figure 7-1.

7.2.1 Print Set Definitions

The KL10 print set, entitled 2040 Console Processor (7011418-0-0 and D-UA-KL10C-0) contains the following information for each front-end option.

1. The option name, number, and wire list revision (if applicable; e.g., KD11A, 11/40 processor, wire list Rev. F).

2. Each option backplane revision, etch, and number (e.g., 5410904 etched backplane, Etch Rev. C, CS Rev. C, 11/40 CPU).

3. Every module of each option, listed individually with information pertaining to:

   a. The lowest acceptable revision (CS and etch)

   b. The status and use of each jumper (in or out)

   c. Any necessary cable information, e.g., cable type and connection locations

   d. Information relative to any other configurable component (e.g., crystal frequency, speed group, and potentiometer setting for DL11).

7.2.2 PDP-11/40 and Peripheral Drawer Power Harness

The power harness cabling internal to the PDP-11/40 (BA11-F) and peripherals drawer (BA11-F) is normally connected prior to shipment and is, therefore, not reconfigured at the site. However, if either harness becomes disconnected or has to be replaced, refer to Chapter 6 of the PDP-11/40 system manual for complete instructions, and refer to print set no. 7011418-0-0.

7.2.3 Power Checkout Procedures (Figure 7-1)

Begin the systems checkout procedure by performing the various power-up procedures on the computer system sections in the following order.

1. Switch Panel

   a. Ensure that the SYSTEM ON switch is in the OFF position.

   b. Ensure that the SYSTEM OFF LOCK switch is in the down position; this will allow the system to follow the normal POWER ON/OFF switch.

NOTE

In order to reset the SYSTEM OFF LOCK switch, insert nonconductive pin upward through the cutout on the bottom of switch panel. Gently press upward on the lock with pin, while pressing lower half of this switch until it is in the down (OFF) position.

   c. Place the override switch S1 (on front of 863) OFF (down).

2. Logic Power Wiring

   a. Check all the power wiring connections to the memories (memory 2 optional), CPU, and I/O backplanes to ensure that no errors have been made in placement of the wiring harness, e.g., power connected to ground tabs, sense lines on incorrect pins, etc. Refer to the KL10-C-0 and MA20 (D-IC-MA20-PW) ac/dc wiring prints while checking these wiring connections.

   b. Using the X1 ohms scale on a VOM, check for short circuits between the listed power tabs and grounds on the following backplanes. Refer to the 2040 Console Processor (7011418 and KL10-C-0) prints for these connections.

      (1) CPU +5 V, -2 V: A, B, C, D
               -5 V, -2 V: A - K

(2) I/O
+5 V: A, B, C, D, E, F, H, J, K
-5 V: A - K
+15 V: A - K
-15 V: A - K

(3) Memory 1
+5 V: A, E, F, L
-5 V: B, C, D, H, J, K

(4) Memory 2
+5 V: A, E, F, L
-5 V: B, C, D, H, J, K

c. Using the X1 ohms scale on a VOM check for short circuits between the listed power tabs and ground.

(1)	KD11-A	+5 V, +15 V, and -15 V
(2)	MF11-UP, MM11-UP	+5 V, -5 V, and +20 V
(3)	RH11-AB	+5 V, +15 V, and -15 V
(4)	DD11-B	+5 V, +15 V, and -15 V
(5)	CD11	+5 V, +15 V, and -15 V
(6)	DH11 no. 1	+5 V and -15 V
(7)	D11 no. 2	+5 V and -15 V
(8)	LP20 no. 1	+5 V
(9)	LP20 no. 2	+5 V

3. Ensure that the main power feed disconnect switch is OFF.

4. Check again that all console power switches are OFF.

5. Check the module placement with the MU list.

6. Ensure that the main power check is complete.

7. Connect the 2040 main power cable to its power source.

8. Place the site's main power feed disconnect switch in the ON position.

NOTE

This, essentially, is a "smoke test." If problems occur at this time, turn power OFF immediately and proceed to troubleshoot the problem.

9. Check to ensure that the circuit breakers on the power supplies and power controls listed below are all ON.

   a. H7420 power supply 1

   b. 863-D power control

c. 861-D power control

d. H760 power supply

e. H761 power supply

f. H7420 power supply 2

g. H7420 power supply 3

h. H7420 power supply 4

i. H7420 power supply 5

j. H7420 power supply 6 (optional)

k. H7420 power supply 7 (optional)

l. H7420 power supply - peripherals drawer

m. M7420 power supply - 11/40 CPU

10. Set override switch (S1) on 863 to OFF.

11. After checking to be sure that the SYSTEM LOCK OFF switch is still in the down position, place the 2040 SYSTEM ON switch, located on the switch panel, to the ON position.

12. If FAULT light illuminates, troubleshoot problem and repair.

13. Check to ensure that all fans are operating.

14. Connect a DVM between the -5.2 A sense output (sense tab ST17) on the CPU backplane and the corresponding ground (sense tab ST16). Adjust the -5.2 V potentiometer (R14) on the G8013 module (Figure 7-2) so that the sense voltage read is -5.2 V. Then, using the DVM, measure the other sense outputs (-5.2B, C, D, E, F, H, J, and K) and check that the sense voltage is -5.2 V.

    The relative measuring points are listed below.

Sense Output	**Sense Tab**	**Ground**
-5.2B	ST19	ST18
-5.2C	ST1	PT15-U
-5.2D	ST2	PT17-U
-5.2E	ST13	PT27-L
-5.2F	ST17	ST6
-5.2H	ST5	ST4
-5.2J	ST3	ST4
-5.2K	ST10	ST11

15. Connect a DVM between the -2 A sense output (sense tab ST15) on the CPU backplane and the corresponding ground (sense tab ST16). Adjust the -2.0 V potentiometer (R21) on the G8013 module (Figure 7-2) so that the sense voltage read is as close to -2.0 V as possible.

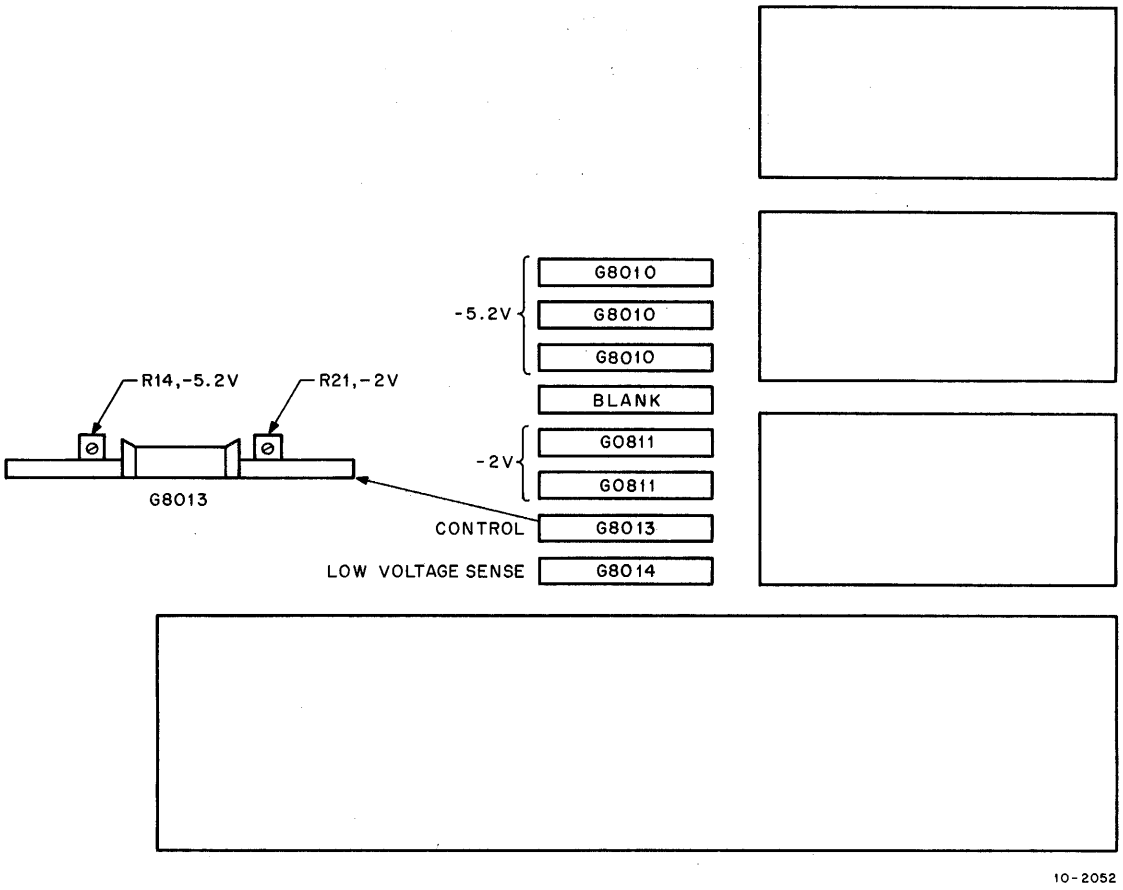


Figure 7-2 Sense Voltage Potentiometer Locations

Then, using the DVM measure the other sense outputs and check that the sense voltages are -2.0 V. The relative measuring points are listed below.

Sense Output	Sense Tab	Ground
-2B	ST14	PT15-L
-2C	ST12	ST11
-2D	ST8	ST9

16. Figure 7-3 shows the G8010 and G8011 modules and their relative positions in the regulator circuitry. Three LEDs are on each module. LEDs that are labeled (Figure 7-2) should be on; those not labeled should be off. Each letter relates to a sense voltage that was checked earlier. Ensure that all LEDs that should be on are illuminated.

17. Using a DVM, measure the +5 V regulator outputs at CPU backplane power tabs PT16-L and PT6-U. All voltages should read +5 V. Adjust the regulators as necessary. Refer to drawing D-UA-KL10-C-0, I/O DC Wiring, to identify the relative +5 V regulators.

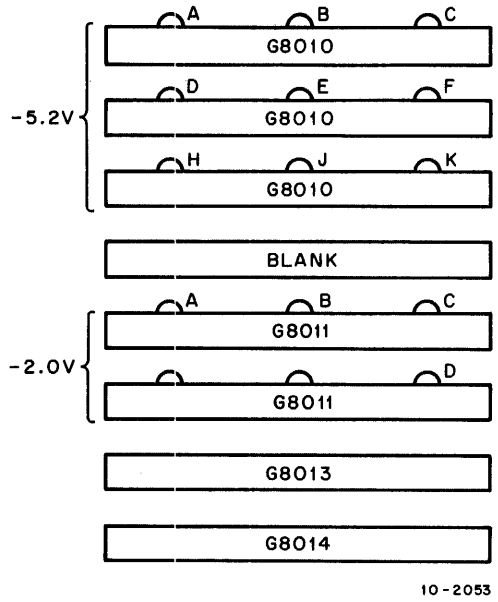


Figure 7-3 Voltage Sense LEDs

18. I/O Backplane Power Wiring

a. Using a DVM, measure the following regulator outputs at I/O backplane power tabs. Voltages should read +5 V and -5 V. Adjust the appropriate regulators as necessary. Refer to drawing D-UA-KL10-C-0, I/O DC Wiring, to identify regulators.

(1) +5 V: PT9-U, PT11-U, PT13-U, PT15-U, PT17-U, PT19-U, PT21-U, PT23-U

(2) -5 V: PT25-U, PT25-L, and DTE

b. If DIA/DMA-20 option is installed, make the following measurements. Adjust appropriate regulators if necessary.

(1) +5 V: PT1-U, PT7-U, PT1-L, and PT7-L

(2) -5 V: PT6-U and PT6-L

(3) -15 V: PT3-U

19. Memory Backplane Power Wiring

a. Using a DVM, measure the following regulator outputs at memory 1 backplane upper and lower power tabs. Adjust appropriate regulators as required. Refer to drawing D-IC-MA20-0-0-PW, MA20 AC/DC Power Wiring, to identify +5 V, -20 V, and -5 V regulators.

(1) +5 V upper: PT0A, PT13A, PT0B, and PT13B
+5 V lower: PT2A, PT15A, PT2B, and PT15B

(2) -20 V upper: PT5A, PT8A, PT11A, PT5B, PT8B, and PT11B
-20 V lower: PT5A, PT8A, PT11A, PT5B, PT8B, and PT11B

(3) -5 V upper: PT4B, PT10A, and PT7A

b. If memory 2 option is installed, use a DVM to measure regulator outputs at backplane upper and lower power tabs. Adjust appropriate regulators as required.

(1) +5 V upper: PT0A, PT13A, PT0B, and PT13B
+5 V lower: PT2A, PT15A, PT2B, and PT15B

(2) -20 V upper: PT5A, PT8A, PT11A, PT5B, PT8B, and PT11B
-20 V lower: PT5A, PT8A, PT11A, PT5B, PT8B, and PT11B

(3) -5 V upper: PT4B, PT10A, and PT7A

20. Using a DVM, measure all the voltages on the PDP-11/40 backplane power tabs. Voltages should be as follows: +5 V, -15 V, and +20 V. Adjust the appropriate regulators as necessary. Refer to 2040 Console Processor drawing (20114-8, sheet 6 of 12) for the various power tab definitions and for the regulator locations.

21. Using a DVM, measure all the voltages on the peripheral drawer backplane power tabs. Voltages should be as follows: +5 V, +15 V, -15 V. Adjust the appropriate regulators as necessary. Refer to the Arithmetic Processor drawing D-UA-KL10-C-0, sheet 7 of 33 for the various power tab definitions and for the regulator locations.

22. Remove power from the system and replace screen on H761.

23. Trip Circuitry Test

a. Using a DVM, measure the voltage on the H770 in the I/O cabinet H7420 no. 3 (bottom one). Adjust for +15 Vdc. Place S1 up (override ON).

b. Place a finger over one of the airflow sensors under the CPU bay. The fault light on the front panel should come ON, and the AIRFLOW CPU LED should light on the 863 power controller.

c. Insert a scope probe on the corresponding yellow wire on plug P2 (on 863) and place a finger on the air sensors one at a time under the CPU. The HI level on scope should go to ground almost immediately as the airflow is blocked. Do this for all CPU sensors.

d. Repeat the last process for all the memory and I/O airflow sensors.

NOTE

These sensors will take approximately 30 seconds to 1 minute to cause a trip, whereas the CPU sensor trips almost immediately.

e. Check that the module bay door microswitches for the CPU, memory, and I/O all cause fault indications. Now check to see if a fault will shut the machine down. First clear all faults, place S1 down (override off) then cause each of the above faults and the machine should power down. The W813 in the 863 controller is at fault if the machine fails to power down.

CHAPTER 8
SYSTEM CHECKOUT

8.1 INTRODUCTION

This section provides the installation engineer with a diagnostic sequence that must be successfully completed before the TOPS-20 monitor can be loaded and run. Any problems or errors that occur should be corrected and any associated diagnostics rerun before continuing with the sequential check-out. The diagnostic run sequence is flowcharted in Figure 8-1. Samples of the diagnostics are shown in Appendix B.

If an option which is listed is not included in the system, skip the associated diagnostic process for that option and proceed to the next step. For NORAM the completion of this section constitutes running standard test procedures and beginning the 90-day warranty period.

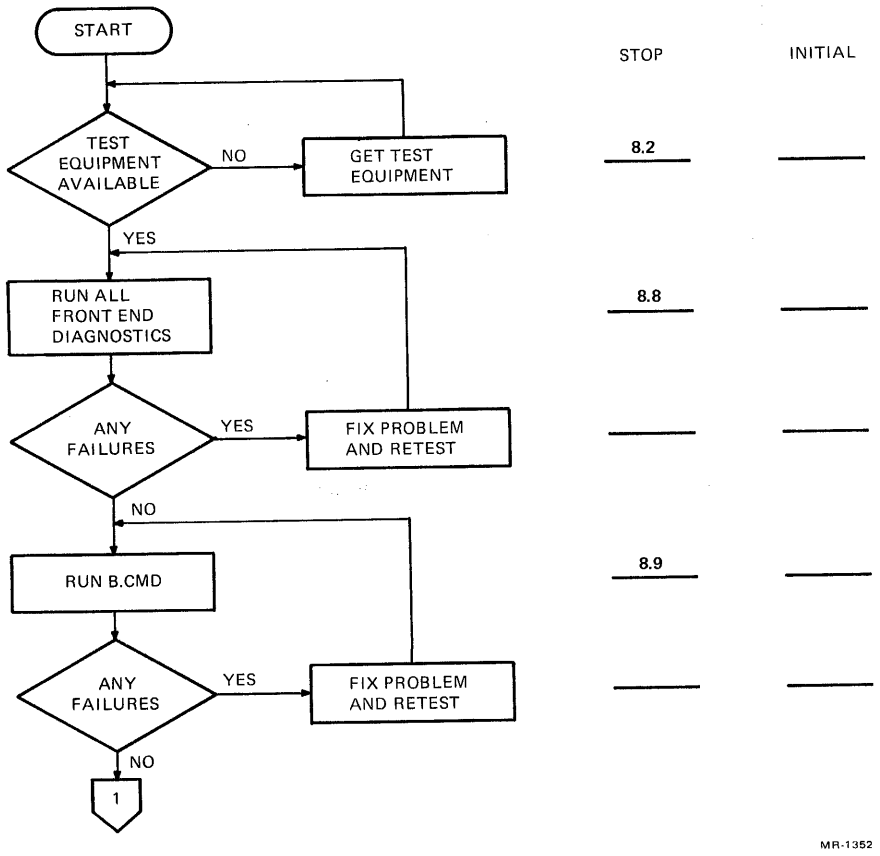


Figure 8-1 Diagnostic Checkout Flowchart (Sheet 1 of 3)

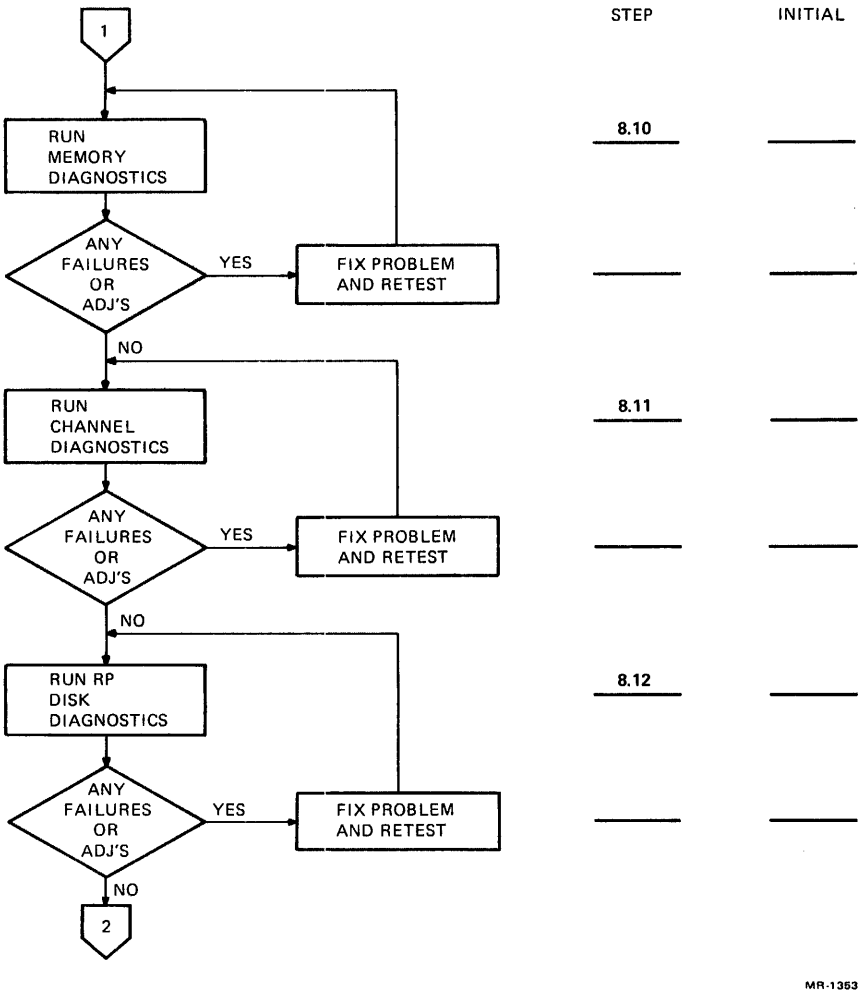


Figure 8-1 Diagnostic Checkout Flowchart (Sheet 2 of 3)

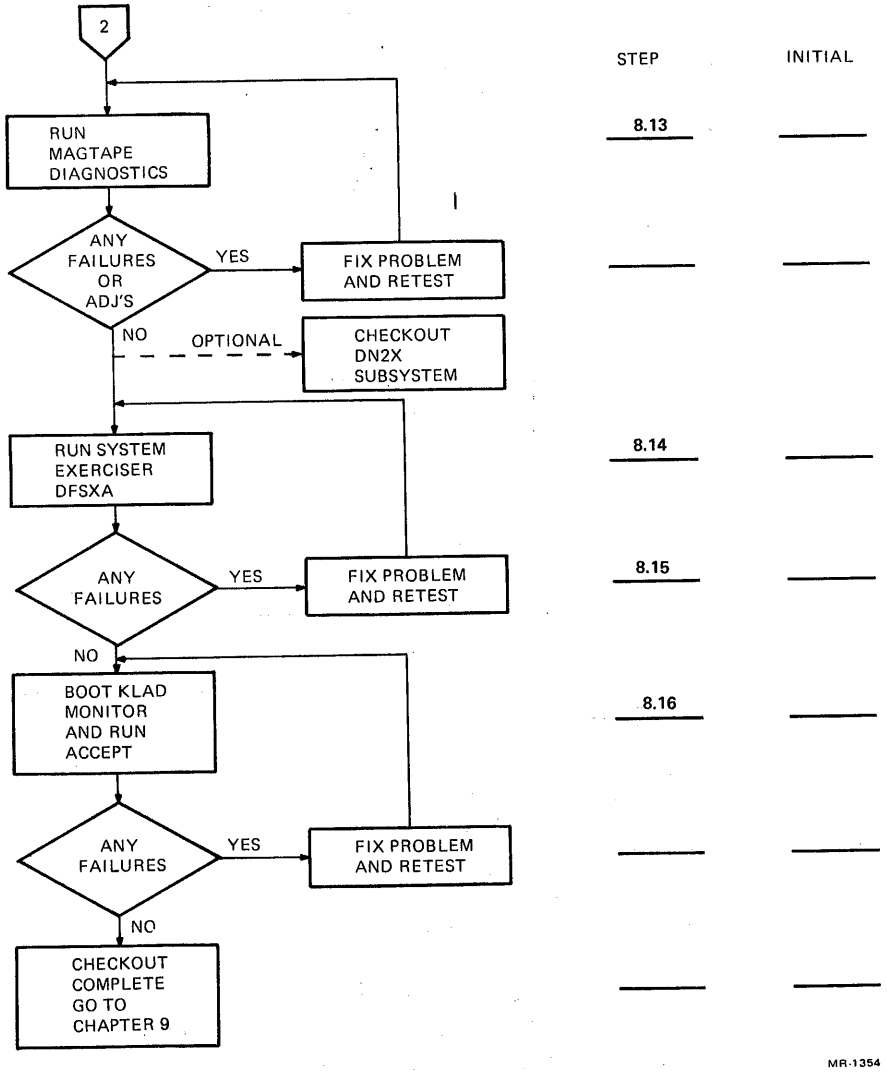


Figure 8-1 Diagnostic Checkout Flowchart (Sheet 3 of 3)

8.2 TEST EQUIPMENT

Table 8-1 shows the test equipment/media or equivalent required for the standard diagnostic checkout procedure.

8.3 TEST SOFTWARE

8.3.1 PDP-11 11/40 Front-End Diagnostics

RXDP	BIN	Floppy Loader
UPD3	BIN	Device Utility Program
COPY	BIN	Copy Program
DBQEA	BIC	11/40 CPU
DZQMC	BIC	Memory Parity
DZBMD	BIN	BM873 ROM
DZCDB	BIN	CD11/CD20 Card Reader

Table 8-1 Equipment for Diagnostic Checkout

Item	Qty.	Description
1	1	Multimeter
2	1	Oscilloscope, Tektronix 475
3	1	Digital voltmeter
4	1	C.O.M. microfiche reader
5	1	Microfiche library
6	1	TU45 Pertec off-line tester
7	1	RP04 DDU or RP06 PERCH tester
8	4	H315 test connector (DC20)
9	1	RP CE pack (RP04/05/06)
10	2	H8611 test connectors (DC20)
11	1 set	Diagnostic floppys
12	1	KLAD-20 pack
13	1	Master skew tape
14	*	Scratch magtapes
15	*	Scratch disks
16	2	Scratch floppys

*Dependent on number of drives on system.

DZDLC	BIC	DL11/E
DZKWA	BIC	KW11-L
DZRXB	BIC	RX11 Floppy Diagnostic
DZRXA	BIC	RX11 Floppy Reliability
DZDHM	BIC	DH11 Diagnostic
DZDHN	BIN	DH11 Reliability
DZDHK	BIC	DM11-BB Modem
DXLPB	BIN	DECsystem-10 LP20 Diagnostic
DZRJA	BIC	RH11/RP04/5/6 Mechanical and Read/Write
DZRJB	BIN	RH11/RP04/5/6 Formatter
DZRJC	BIN	RH11/RP04/5/6 Head Alignment Verification
DZRJD	BIC	RH11/RP04/5/6 Performance Exercise
DZRJG	BIC	RH11/RP04/5/6 Diskless Controller
DZRJH	BIC	RH11/RP04/5/6 Diskless Controller
DZRJI	BIC	RH11/RP04/5/6 Functional Controller
DZRJJ	BIC	RH11/RP04/5/6 Functional Controller
SY2040	BIN	2040 Front End Exerciser
DZQUX	BIN	Configurator/Linker
XQLKGO	LIB	Monitor Library
XQLKAO	LIB	Module Library
DZKAQ	BIN	PDP-11 Power Fail Test

8.3.2 Diagnostic Support Programs

KLDCP	BIN	KL10 Diagnostic Console
KLDCPU	A11	KL10 Console Utility
CDUMP	A11	KL10 Console Core Dump Utility
KLDCP	HLP	Help File
KLRXBT	BIN	KLDCP Floppy Boot
XTECO	BIN	Text Editor
UB	RAM	KL10 Microcode – Model B
BB	CMD	KL10 Diagnostic Run File – Model B

BBT	CMD	KL10 Boot Ten Run File - Model B
CONFG	CCL	Memory Configuration Run File
KLLD	CCL	KL10 "SUBRTN" and "KLDDT" Load
MEMCON	A11	Console Extension and Memory Configuration
TRACON	HLP	Trace Routine
SUBRTN	A10	PDP-10 Subroutine Program
KLDDT	A10	PDP-10 DDT
KLDDT	HLP	PDP-10 Help File
DIAMON	A10	PDP-10 Diagnostic Monitor
MAGMON	A10	PDP-10 Magtape Monitor
KLCPU	CMD	Functional Command Run File
KLPROC	CMD	"DIAMON" Functional Run File
KLUSR	CMD	"DIAMON" User Functional Run File
CM	CCL	Clear Memory
WRMEM	CCL	Cache Memory Test
DGQDE	A11	DLDP - DL11-E Monitor
DGQEA	BIN	DN2X Bootstrap Loader Program
DGQDF	A11	DN2X Front End Loader Utility
DGQDG	A11	DN2X Secondary Front End Monitor
CONFG1	CCL	Internal Memory Confg - 1 Way Interleave
CONFGR	CCL	CCL File to Relocate Internal Memories
LOMARC	CCL	CCL File to Set Low Current Margins
HIMARC	CCL	CCL File to Set High Current Margins
LOMARS	CCL	CCL File to Set Low Strobe Margins
HIMARS	CCL	CCL File to Set High Strobe Margins
LOMART	CCL	CCL File to Set Low Threshold Margins
HIMART	CC	CCL File to Set High Threshold Margins
MGNOFF	C	CCL File to Clear Margins

8.3.3 KL10 Processor Hardware Diagnostics - Model B

DHDIAG	CMD	Diagnostic Command Run File
EBOXB	RAM	EBox Diagnostic Microcode
DHKAA	A11	EBox Part 1
DHKAB	A11	EBox Part 2
DIAGB	RAM	MBox Diagnostic Microcode
DHKBA	A11	MBox Basic
DHKBB	A11	Memory Control and Memory
DHKBC	A11	Paging Logic
DHKBD	A11	MBox Channel Loopback
DHKCA	A11	Meter Board
DHMCA	A11	MBox Cache Option Part 1
DHMCB	A11	MBox Cache Option Part 2
DHQFA	A11	TRACON Model B
SWITCH	HLP	Switch Help File
DIACON	HLP	Diagnostic Execute Help File
TRACON	HLP	TRACON Help File
DGDTE	A11	DTE20 10/11 Interface
DGKBE	A11	MBox Channel Loopback
DGMMA	A11	Memory Reliability

8.3.4 Processor Functional Diagnostics

DFKAA	A10	Basic Instructions No. 1
DFKAB	A10	Basic Instructions No. 2

DGKAC	A10	Basic Instructions No. 3
DGKAD	A10	Basic Instructions No. 4
DFKBA	A10	Basic Instruction Reliability
DGKBB	A10	Basic Instruction Reliability
DGKCA	A10	Advanced Instructions
DFKDA	A10	CPU/PI/Memory Reliability
DFKEA	A10	Paging Hardware
DFKEB	A10	MUUO and User Mode
DFKFB	A10	Instruction Timing
DFDTE	A10	DTE20 10/11 Interface

8.3.5 Memory Diagnostics

DDMMC	A10	Fast AC Diagnostic
DDMMD	A10	Memory
DDMME	A10	BLT/Memory Exerciser
DDMMF	A10	Floating Ones/Zeros
DDMMG	A10	4096K Memory

8.3.6 TM02/TU45 Magtape Diagnostics

DFTUE	A10	Basic Functions
DFTUF	A10	Multidrive Exerciser
DDTUH	A10	Reliability

8.3.7 RH20 Controller Diagnostics

DFRHB	A10	RH20 Device-Less

8.3.8 RP04/RP06/(Massbus) Disk Diagnostics

DFRPH	A10	RH20/RP04 Basic Device
DFRPK	A10	RH20/RP06 Basic Device

8.3.9 Disk Subsystem Reliability

DDRPI	A10	RP04/5/6 Reliability
DDRPB	SAV	User Mode Disk Performance

8.3.10 System Exerciser Tests

DFSXA	A10	KL10 Channel/DTE20 Interaction

8.4 DOCUMENTATION

The following is a list of print sets and manuals needed if the option is on the system. These are shipped in hard copy form with the system. Refer to the ship list for part numbers.

1. Front End:
   11/40 print set (includes KW11-L and DL11)
   A-AD-7011418-0-0
   RH11-AB
   MF11-UP/MM11-UP
   BM783-YD, YF, YH, YG
   RX11
   RX01

LP20
CD11
DN20
DC20

2. CPU and Channels:
   KL10-E print set Vol. 1 and Vol. 2
3. MB20 print set
4. RH20 print set
5. RP04 print set
6. RP06 print set
7. TU45 print set
8. TM02 print set
9. Process sheet RP04-C-0-0 MR0002-TP
10. Line Printer vender manuals
11. Card Reader vender manuals
12. RP04 vender manuals
13. RP06 vender manuals
14. TU45 vender manuals

8.5 STANDARD CONSOLE SWITCHES

Switch	Reset (0)	Set (1)
2	Allow cache use	Inhibit cache
4	Allow paging and traps	Inhibit paging and traps
5	Print full error message	Inhibit comment portion
7	Print only first error	Print all errors
8	No function	Halt on test error
9	Proceed to next test	Scope loop on test error
10	No function	Ring TTY bell on error

8.6 DIAGNOSTIC SOFTWARE REFERENCE

Index MD-10-DDXXA is contained on microfiche and can be located in the microfiche diagnostic listing. It lists all currently available diagnostics and their latest revision.

8.7 DIAGNOSTIC INPUT MEDIA

For the initial checkout of the 11/40 front end the input media will be from an RX01 floppy disk. Once a certain degree of system integrity has been reached, the diagnostic input media can revert to the KLAD pack.

WARNING

Until complete system integrity is guaranteed the RP disk should be write-locked and KLDCP booted from the RX01 floppy disk.

8.8 PHASE A - 11/40 FRONT END AND OPTIONS VERIFICATION

8.8.1 Load Medium: RX01 Floppy Disk

Either KLDCP or RXDP console diagnostic monitor can be used when loading front-end diagnostics.

8.8.2 Applicable Diagnostics

Option	Diagnostic	Estimated Problem-Free Run Time (Minutes)
KD11-A	DBQEA	30
MF11-UP	DZQMC	30
BM873-YF	DZBMD	10
KW11L	DZKWA	10
RZ01/RX11	DZRXA	15
	DZRXB	15
DC20	DZDHM	30
	DZDHN	30
	DZDHK	30
DL11E	DZDLC	10
LP20	DZLPL	30
CD20		30
RH11/RP*	DZRJG	
	DZRJH	
	DZRJI	
	DZRJJ	120
	DZRJB	
	DZRJA	
	DZRJD	
SYSTEM†	SY2040	Overnight

8.8.3 CD20 Checkout

8.8.3.1 Indicator Test - Check all function light indicators by using the lamp test switch on the back of the reader.

8.8.3.2 Alpha and Binary Deck Tests - Run the following tests (no errors allowed). All MAINDEC tests must be the latest revision.

1. Load MAINDEC-11-DZCDB.
2. Load address 200 into the 11/40.
3. Load alpha deck into input hopper.
4. Set all 11/40 switches to zero and press start switch.
5. Run alpha deck through the card reader 10 times.
6. Load address 200 into 11/40.
7. Load binary deck into the input hopper.

*Disk pack is 22-sector format.
†Disk pack is 20-sector format.

8. Set console switch 4, press start.

9. Run binary deck through card reader 10 times.

10. In multiswitch mode, check the DZCDB listing for proper switch settings.

    a. Load two alpha decks into the hopper. Set console switch 5 and check for program halting between decks.

    b. Run 10 passes in image mode using both alpha and binary decks.

    c. Run 10 passes in packing mode using both alpha and binary decks.

8.8.4 DC20 Verification

8.8.4.1 Equipment Required

1 MAINDEC-11-DZDHM, DZDHN, DZDHK (all at latest revision)
1 DC20 installed in a KL10 front end
4 H315 test connectors
2 H8611 test connectors

8.8.4.2 DZDHK Modem Control Check

1. Install the H8611 test connectors into J16, J18, J19, and J21 on the H317B patch panel.

2. Load and run diagnostic DZDHZ test group 0 for one pass.

3. If there are more than 16 lines on the system, move the H8611 connector to the next H317B patch panels and repeat the diagnostic test.

4. Once all DM11 modem controls have been checked, ensure that all cables are replaced.

8.8.4.3 DZDHM/DZDHN Checkout

1. Connect one H315 test connector into one line of each 8-line group at the H317B patch panel.

2. Load and run the DZDHM/DZDHN diagnostics to check out the functionality of data paths.

3. The other seven lines in each 8-line group may be checked out when the KLAD monitor is up and running. By this time the communications cables should be connected to customer terminals thus allowing LOGIN/LOGOUT facility.

8.9 PHASE B - PDP-11-BASED KL10 AND KL10-BASED KL10 DIAGNOSTIC VERIFICATION

8.9.1 Deskew Check

Both RH20 and MB20 Deskew should be checked before proceeding. See Paragraphs 8.18 and 8.19.

8.9.2 Load Medium - RP KLAD Pack

Providing the front end has run successfully, the diagnostics for phase B can be loaded from the KLAD pack. However, KLDCP should be loaded from RX01 floppy disk and the RP disk should be write-locked.

8.9.3 DTE/CPU Checkout

The 11-based 10 diagnostics may be run in a chained format by using the J DHDIAG command, and the 10-based 10 diagnostics may be run using the J KLCPU command. DHDIAG and KLCPU can themselves be chained by using the B command.

The previous sequence of diagnostics should run error-free at clock source zero (CS0) and clock source one (CS1). Clock source 1 is the fast clock. The B command file takes approximately 30 minutes to run.

The last diagnostic in the command file is DFKDA which after 1 pass will enter extended run mode and signify an end pass every 100 passes.

The following sequence of diagnostics is the same as the chained command file format. All diagnostics should run error-free at CS1, CR0 before continuing. DFKDA can be left running as a reliability test for the back end processor and memory.

Option	Diagnostic	
DTE20	DHDTE.A11	
EBox Part 1	DHKAA.A11	
EBox Part 2	DHKAB.A11	
MBox Test 1	DHKBA.A11	
Memory Control	DHKBB.A11	
MBox Cache	DHMCA.A11	
Cache RAM Banger	DHMCB.A11	
Meter Board	DHKCA.A11	
Channel Control	DHKBD.A11	
Channel Loopback	DHKBE.A11	
Basic Instruction 1	DFKAA.A10	
Basic Instruction 2	DFKAB.A10	
Basic Instruction 3	DFKAC.A10	
Basic Instruction 4	DFKAD.A10	
Advance Instruction	DFKCA.A10	
Basic Reliability	DFKBA.A10	
Paging	DFKEA.A10	
Monitor And User UUOs	DFKEB.A10	
DTE20	DFDTE.A10	
Functional Reliability	DFKDA.A10	Overnight Run
Instruction Timing	DFKFB.A10	Note this is not part of the B. CMD.

8.10 PHASE C - MEMORY DIAGNOSTIC VERIFICATION

8.10.1 Introduction

The MB20 memory can initially be checked using the 11-based 10 diagnostic DGMMA. This diagnostic checks basic memory reliability and also has a switch (/MARGINS:X) to enable current, strobe, and threshold margins to be tested. Further memory testing can then be made by using 10-based 10 diagnostics DDMMD, DDMME, DDMMG.

8.10.2 DGMMA.A11

(Set 11SW1 = 1)

1. Run DGMMA at CR0, CS0 with no RH switches set for a basic reliability check.

2. Run DGMMA at CR0, CS0 with RH switches set for ALL MARGINS (see sample diagnostic for setting). Run time is approximately 30 minutes for 256K.

8.10.3 DDMMD/DDMMG Memory Exerciser

1. These are A10 files. The BT command should be loaded first.
2. DDMMD is for systems with less than 256K.
3. DDMMG is for systems with more than 256K.

8.10.4 DDMME BLT Test

This is an A10 file to check the functionality and speed of memory using the BLT instruction.

8.10.5 MB20 Option Diagnostics

Option	Diagnostics	Run Time (Minutes)
MB20	DGMMA	30
	DDMMD	30
	DDMME	5
	DDMMG	

8.11 PHASE D - RH20 CHANNEL DIAGNOSTIC VERIFICATION

This diagnostic is an A10 file and requires that the BT command file be run before being loaded.

1. Run diagnostic at CR0, CS0.
2. Set SW1 = 1 for multiple RH20 operator-select.

Option	Diagnostic	Run Time (Minutes)
RH20	DFRHB	20

8.12 PHASE E - RP DISK DIAGNOSTIC VERIFICATION

8.12.1 Formatting

The scratch disk packs should be formatted and verified in 20-sector formats before use.

8.12.2 Error Rates

1. If a disk pack has five or more hard bad spots it should not be used. No bad spots are allowed on surfaces 0 and 1 of cylinder 0. Thirty soft bad spots are allowed.
2. The allowable error rates for RP04/RP06 are as follows.

   Irrecoverable - 1 error in 10^{12} bits read
   Recoverable - 1 error in 10^{9} bits read
   Seek - 1 error in 10^{6} bits operations

3. Disk pack - attributable errors (bad spots) are any errors (DCK, ECH, OPI, DTE, etc.) which occur on the same cylinder and head (track) more than once, even though they may not occur every time. A record of the pack location of every error should be kept so that pack errors can be identified since they may occur on a certain area as little as one time in ten or less.

   If bad spots are seen on the same surface in many areas then this may be caused by a weak head.

8.12.3 Head Alignment Verification (DFRPH or DFRPK)

(Refer to the appropriate alignment procedures in respective technical manuals.)

1. This should be run for each disk drive.
2. The DDU (RP04) or PERCH (RP06) should be connected and the CE mounted for 20 minutes prior to running the alignment check.
3. If a head is outside ±80 microinches from dead center then adjustment will be necessary.
4. The final results should be retained for future reference when head drift checks are made at preventive maintenance time.

8.12.4 PTIME (DDRPI)

When running PTIME the average seek time should be within 27.6 to 28.6 ms. Adjustment is necessary if the above is out of specification. Refer to the appropriate adjustment procedure in technical manual.

8.12.5 Diagnostics

Option	Diagnostic	Run Time (Minutes)
RP Disk	DFRPH (RP04) DFRPK (RP06)	20
RP Disk Head Alignment	DFRPH (RP04) DFRPK (RP06)	5 per drive after CE pack warmup period (20 min). Retain final results.
RP Disk	DDRPI Run: FORMAT PTIME ACCEPT RONLY for all drives	60 per drive

NOTE

For compatibility, run RONLY on all drives and then rotate packs and run RONLY until all packs have cycled through all drives.

8.13 PHASE F - TU45 MAGNETIC TAPE SYSTEM DIAGNOSTIC VERIFICATION

The acceptance script ACCEPT should be run on all drives present. ACCEPT will run one pass of B1, B2, R1, and R8. If multiple drives are on the system, then a drive compatibility check should be made.

8.13.1 DFTUE

Tests B1 and B2 will test the basic functionality of the drive.

8.13.2 DFTUK

ACCEPT will run R1 (1600 bits/in) and R8 (800 bits/in) reliability.

8.13.3 DFTUF

This is a multiple drive exercise and all drives should be run concurrently for one pass.

Option	Diagnostic	Run Time (Minutes)
TU45	DFTUE (BASIC)	5 per drive
	DFTUK (RELIABILITY)	40
	DFTUF	1 pass

8.13.4 Errors

1. No errors are allowed on test B1.
2. Only write errors due to tape defects are allowed on test B2.
3. Only write errors due to tape defects are allowed on reliability tests.

8.13.5 Adjustment

If any drive is exhibiting unacceptable errors or is not read/write compatible with other drives, adjustment will be necessary. The TU45 off-line tester should be used together with the associated set-up and adjustment procedure. This allows the drive to be fixed while diagnostic checkout continues.

8.13.6 DFTUE Compatibility Test

This is to be used with multiple drive systems. With DFTUK in core, run IW test, set PDP-10 right half switches to 400010. Type the following responses to the console questions.

Density	- CR
Close Skew Window	- CR
Data COMPARE Mask	- CR
SYSERR Recording	- N
Fast Mode Y or N	- Y
Verify Tapes	- N

One write error per pass of tape allowed not due to tape defects.

Next, run IR test until all tapes have been rotated and read on each drive. No read errors allowed. Read errors indicate a drive with skew problems.

Run IW test. This time answer console questions as follows.

Density	- 800
Close Skew Window	- CR
Data Compare Mask	- CR
SYSERR Recording	- N
Fast Mode Y or N	- Y
Verify Tapes	- N

One write error per pass not due to tape defects is allowed.

Next, run IR test until all tapes have been rotated and read on each drive. No read errors allowed. A read error would indicate drive skew problems.

8.14 DN2X COMMUNICATIONS SUBSYSTEM

The DN2X Communications Subsystem Technical Manual (EK-0DN2X-TM-001) contains a detailed installation and checkout procedure (Chapter 2).

The integration of this subsystem with the DECSYSTEM-20 should be made after the standard diagnostic checkout for the basic system has been completed.

8.15 PHASE G - SYSTEM EXERCISER DFSXA

This system exerciser will interactively check all channels, KL memory, channel devices, and the front end. The channels may be exercised in loopback mode or device read/write mode. An overnight run is desirable prior to booting the KLAD monitor or building a TOPS-20 monitor pack.

8.16 PHASE H - KLAD-20 MONITOR CHECK

8.16.1 Introduction

A copy of KLAD-20.MEM has been shipped with the system. It is important to read this document before continuing. If all preceding diagnostics have run correctly, then the monitor check can begin. However, if any intermittent problems exist, they must be corrected before proceeding.

8.16.2 KLDCP Disk Boot Check

1. Write-enable the KLAD pack.
2. The procedure to boot KLDCP from the disk using the SW REG is well documented in KLAD-20.MEM Section B (Usage of KLAD-20).
3. If KLDCP prompts with CMD:> then the front end (FE) boots area on the disk is intact.
4. Write-protect the KLAD pack.
5. Core memory should be cleared before continuing. See KLAD-20.MEM Section B to use MZ command to clear memory.

8.16.3 KLAD Monitor Disk Boot Check

1. KLAD pack is write-permit
2. Read KLAD-20.MEM Section B2

8.16.4 General Rules

1. Zero KL memory
2. Master reset the CPU (MR)
3. Halt front end
4. Clear front end SW REG
5. Write-permit the RP KLAD pack
6. Press ENABLE and DISK switches simultaneously.

Once the TOPS-20 monitor is loaded and response is made to the Date, Time, Why Reload, and Checkd questions, the 72-hour final acceptance and test (FA&T) acceptance package can be set up and run for a final check of system integrity.

NOTE

Read Section B2 and Appendix G of KLAD-20.MEM.

If the LOG files and SYSERR show no unacceptable errors then Chapter 9 of this manual (Hardware Acceptance) may be entered. For NORAM the completion of Chapter 8 constitutes the start of the 90-day warranty.

8.16.5 KLAD-20 Backup

It is important to back up the KLAD monitor on magnetic tape; it might be needed.

8.17 DECX/11 PROCEDURE/MAP LISTINGS
SY2040

1. Map

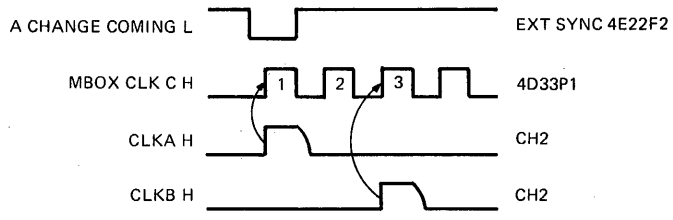
   KWDA0 - Timing analysis
   KWAF0 - Systems clock
   RXAB0 - Floppy
   RPBE0 - RP04 - RH11
   DLBA0 - DL11-E
   DTAA0 - DTE20
   CPCA0 - 11/40 CPU
   BMEA0 - BM873 ROMs
   DMBG0 - DM11-BB
   DHAI0 - DH11 - DC20
   BKAA0 - Worst case memory
   BKBA0 - Monitor check sum
   CDAE0 - CD11 - CD20
   LPFA0 - LP20 line printer

2. Switch settings

   12 - End of pass print
   13 - Inhibit error printout
   14 - Inhibit dropping modules after 20 errors
   15 - Drop modules on first error

   (Refer to listings for further explanation.)

8.18 MA20 - MB20 DESKEW PROCEDURE
Figure 8-2 is a timing diagram for the MA20/MB20.



CH2: PIN: ADJUST:
CLKA – 5D26A1 – 5EF1 (TOP POTENTIOMETER)
CLKA – 5D29A1 – 5EF54 (TOP POTENTIOMETER)

CH2: PIN: ADJUST:

CLKB – 5D26K1 – 5EF1 (BOTTOM POTENTIOMETER)
CLKB – 5D29K1 – 5EF54 (BOTTOM POTENTIOMETER)

MR-1350

Figure 8-2 MA20/MB20 Timing Diagram

1. A Tektronix 7000, 475, or equivalent oscilloscope should be used. The scope time base should be 20 ns for initial deskewing, and 2 ns for final deskewing (sweep magnifier X10).

Final deskewing adjustments will be done at the horizontal centerline. Use equal length probes with grounds.

2. Adjust scope vertical sensitivity to 0.5 Vcm for CH1 and CH2.

3. Adjust CH1 vertical position to 1.3 V above centerline.

4. Adjust CH2 vertical position to 1.5 V below centerline.

5. Read the time base between CH1 and CH2 where the signal edges cross the center graticule line.

6. Proceed as follows.

   a. Load microcode
   b. Set CR0, CS0, FX1
   c. Sync negative

7. External sync on 4E22F2 "A CHANGE COMING L"

8. Channel 1 on 4D33P1 "MTR MBOX CLK C H"

9. Channel 2 on:

   5D26A1 - CLKA HA - Adjust top potentiometer on 1-EF
   5D29A1 - CLKA H - Adjust top potentiometer on 54-EF.

10. Align CH2 with CH1 at the centerline where they cross.

11. Magnify the two signals (10X) and adjust the potentiometer so that CH2 crosses CH1 at centerline. (Do this for both CLKAs.)

12. Channel 2 on:

    5D26K1 - CLKB H - Adjust bottom potentiometer 1-EF
    5D29K1 - CLKB H - Adjust bottom potentiometer 54-EF.

13. Align CH2 with the third "MBOX CLK" on CH1 where they cross at the centerline. Magnify the scope (10X) and adjust the potentiometer so that CH2 crosses CH1 at centerline. (Do this for both CLKBs.)

8.19 RH20 DESKEW PROCEDURE

The following information and equipment are necessary for the deskew procedure (see Figure 8-3).

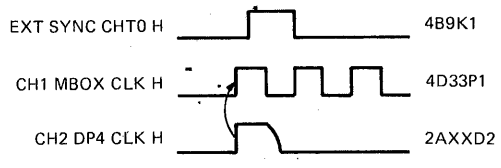
1. Use a Tektronix 475 or a 4-trace oscilloscope.

2. Use equal length probes with grounds.

3. All RH20 clocks are deskewed to the MBOX CLK H that produces CHT0 H in the channel.

4. Recheck skew whenever the CBus cable or M8556 board is replaced.

5. The potentiometers to be adjusted are located on the M8559 board. The top potentiometer is for RH20 no. 0; the second potentiometer is for RH20 no. 1, etc.



RH20 NO	PIN NO
0	2A36D2
1	2A33D2
2	2A30D2
3	2A27D2
4	2A24D2
5	2A21D2
6	2A18D2
7	2A15D2

MR-1351

Figure 8-3 RH20 Deskew Timing Diagram

Perform the following adjustments.

1. Set CS0 - CR0, FX1.
2. Sync positive
3. External sync on 4B9K1 - CHT0 H - (CHC1)
4. Channel 1 on 4D33P1 - MBOX CLK H - (MTR2)
5. Channel 2 on 2AXXD2 - DP4 CLK H - (DP4)
6. Align 50 percent point of AXX02 (CH2) with the 50 percent point of the MBOX CLK (CH1) that occurs approximately 10 ns before the CHT0 clock. Refer to timing diagram.

CHAPTER 9
HARDWARE ACCEPTANCE PROCEDURES

9.1 PURPOSE

This procedure is intended to provide for the standard field service hardware acceptance of the DECSYSTEM-20.

9.2 GENERAL INFORMATION

The DECSYSTEM-20 and its peripherals being installed have previously undergone stringent acceptance procedures during manufacture of the system. These procedures included numerous quality and performance tests on individual components and assemblies. In addition to these checks the system has successfully undergone a 72-hour final acceptance test during which the standard monitor, software and user mode diagnostics were run. The system has also undergone a complete diagnostic checkout during its installation phase. The series of tests listed in this chapter are intended as a default hardware acceptance procedure if no other procedure has been requested by the customer. The intent of this procedure is to ensure that the integrity of the system has not been compromised during shipping or installation.

9.3 REQUIREMENTS

1. The system (or option) should be fully installed in accordance with the DECSYSTEM-20 installation procedures described in this manual. All cables, covers, and doors should be on. All preliminary power and ground checks should have been completed.

2. An authorized customer representative should be present to observe and sign each hardware acceptance sheet.

9.4 TEST VERIFICATION

The hardware acceptance test verification sheets in Appendix C contain lists of the standard tests to be run for the system and the applicable options.

A separate test sheet exists for each subsystem/device available on the DECSYSTEM-20. Only the sheets applicable to the particular system configuration should be used.

The tests should be run in the following sequence, with reference to appropriate sheets for procedures.

Sheet 1	Front end
Sheet 2	11-based isolation
Sheet 3	10-based functional
Sheet 4	Memory
Sheet 5	RH20
Sheet 6a	RP04 disk system
Sheet 6b	RP06 disk system
Sheet 7	Tape system
Sheet 8	Line printer
Sheet 9	DC20
Sheet 10	Card reader
Sheet 11	Communications
Sheet 12	Systems exerciser

9.5 COMPLETION

Upon the successful completion of these standard test procedures, the system will be considered to have met the field service criteria for installation and acceptance of the hardware. A copy of the field service summary sheet should be sent to Field Service Product Support MR1-1/S35 upon completion of installation.

CHAPTER 10
SYSTEM ADD-ON AND ADJUSTMENT PROCEDURES

10.1 MA20/MB20 ADD-ON MEMORY INSTALLATION, CHECKOUT, AND ACCEPTANCE PROCEDURE

10.1.1 Introduction

MA20/MB20 add-on installations should be very simple to perform if care is taken to follow each step outlined in these procedures. However, there are points that require consideration before entering a customer site.

1. All DECSYSTEM-20s being shipped today have mounting holes (for the H7420 power supplies) set in the CPU back door upright (refer to Paragraph 10.1.5, step 10). However, some of the first DECSYSTEM-20s delivered did not have the mounting holes, and others had them but they were not properly spaced. If a machine has this problem, contact Product Support in Marlboro and they will P1 the necessary equipment to correct the problem.

2. A preinstallation (skidded) checkout procedure is part of this document. The purpose of skidded checkout is to determine if there is any reason why the delivered memory unit should not be mounted in the customer's system. At this point, look for "catastrophic" problems, not logic or stack problems.

10.1.2 MA20/MB20 Add-On Parts List

The MA20/MB20 add-on parts are listed in Table 10-1.

Before beginning the installation, read through the entire procedure and become familiar with all diagrams and required parts. Ensure that all required parts have been included.

10.1.2.1 Various MA20 System Components – The various MA20 system components are as follows (module utilization is shown in Figure 10-1). The numbers preceding component parts are quantity designations.

MA20-M (16K × 19-bit core memory section)

1 – G114 sense inhibit module
1 – G235 X-Y driver module
1 – H217-B stack module

MA20-E (2 storage modules, 32K × 37-bit expansion core memory)

4 – MA20-M

MA20-A (Controller pair plus two storage modules)

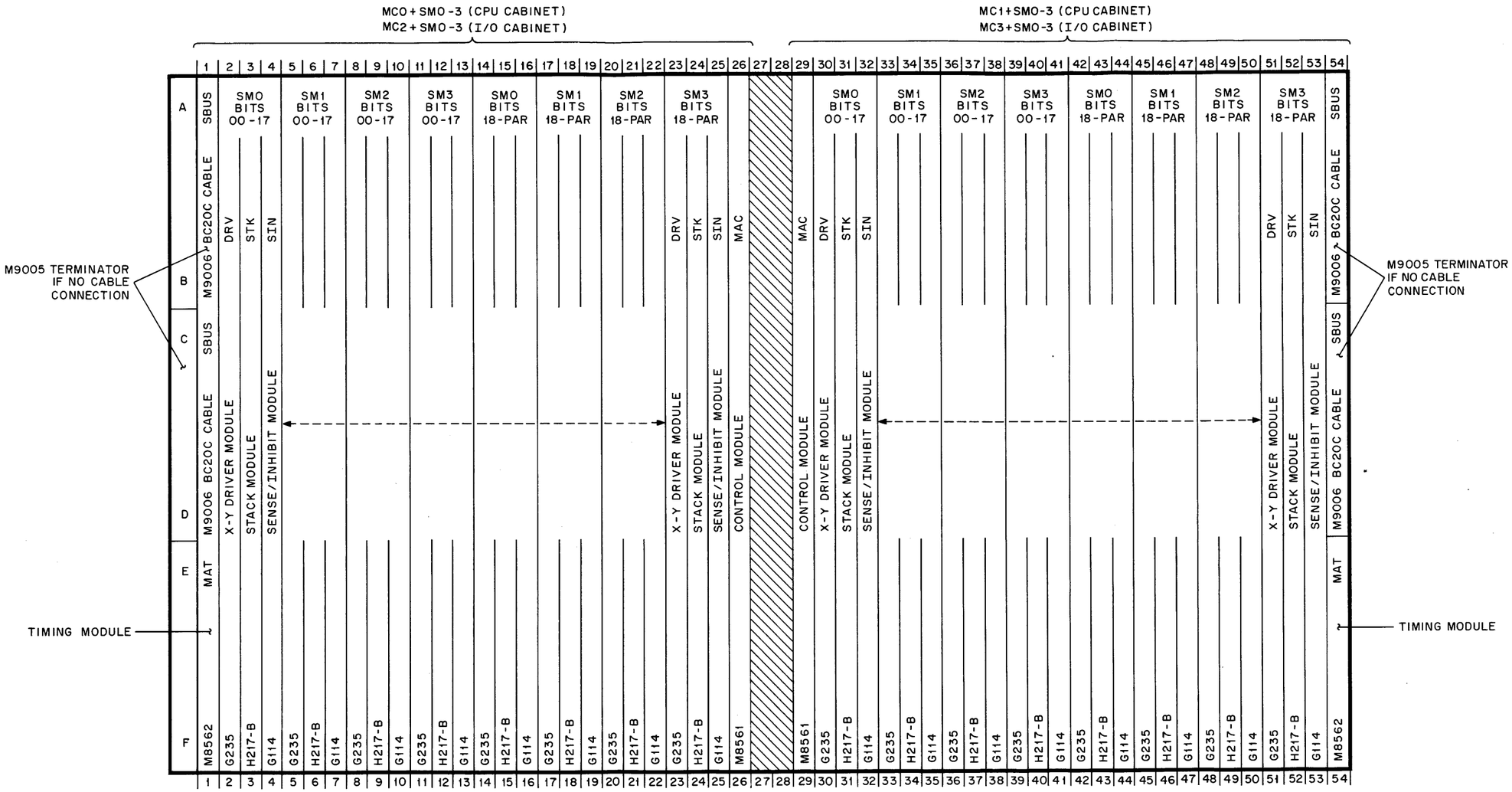
1 – MA20-E
2 – M8561 control module
2 – M8562 timing module

Table 10-1 MA20/MB20 Add-On Parts List

Quantity		Part Number	Description	Item
50 Hz	60 Hz			
1	1	Note 1	MA20/MB20 memory assembly	1
2	2	Note 2	H7420 power supply	2
1	1	Note 2	No. 2 memory harness	3
1	1	Note 3	Duct assembly	4
18	18	9007786	Nut, Tinnerman	5
28	28	9006074-3	Screws, Phl. truss hd. 10-32 × 62	6
30	30	9007651	Washer, ext. tooth no. 10	7
75	75	9007032	Cable tie	8
15	15	9008264	Mount, cable tie, adh. back	9
10 ft	10 ft	9107430-29	Wire, no. 18 AWG str. tw-pr. (red/white)	10
1	1	1209351-03	HSG connector 3-pin	11
4	4	1209378-00	Pin contact	12
3	3	9008887	Ground strap	13
4	4	9006565	Nut, Kep 10-32	14
–	2	9107673-09	Power cord extension	15
2	–	7011432-03	Power cord extension	16
2	2	BC20C-5C	SBus cable	17
6 ft	6 ft	9008274	Foam tape	18
2 ft	2 ft	9007241-9	1/8 in spiral wrap	19

NOTES

1. **MA20/MB20 memory assembly GC/GD less items 7, 8, 24, 27, 28 from A-PL-MB20-0-0.**
2. **MA20 PC or PD (items 7 and 8 from A-PL-MB20-0-0).**
3. **Item 24 from A-PL-MB20-0-0.**
4. **Items 5 through 16 are items 27 and 28 from A-PL-MB20-0-00.**



NOTES:
1. Viewed from wire side
2. MU same for CPU and I/O cabinets

10-2126

Figure 10-1 MA20 Module Utilization

2 – M9005 SBus terminator module
2 – H742 power supply
4 – H744 power supply (+5 V)
6 – H754 power supply (+20 V)
2 – BC20C SBus cable
1 – 7009894 fan assembly
1 – 7009465 logic assembly

MA20-G (Controller pair plus four storage modules)

1 – MA20-A
1 – MA20-E

MA20-H (Controller pair plus eight storage modules)

1 – MA20-A
3 – MA20-E

10.1.2.2 MB20 System Components – The various MB20 system components are as follows (module utilization is shown in Figure 10-2).

MB20-M (32K × 19-bit core memory section)

1 – G116 sense inhibit module
1 – G236 X-Y driver module
1 – H224-B stack module

MB20-E (two storage modules, 64K × 37-bit expansion core memory)

4 – MB20-M

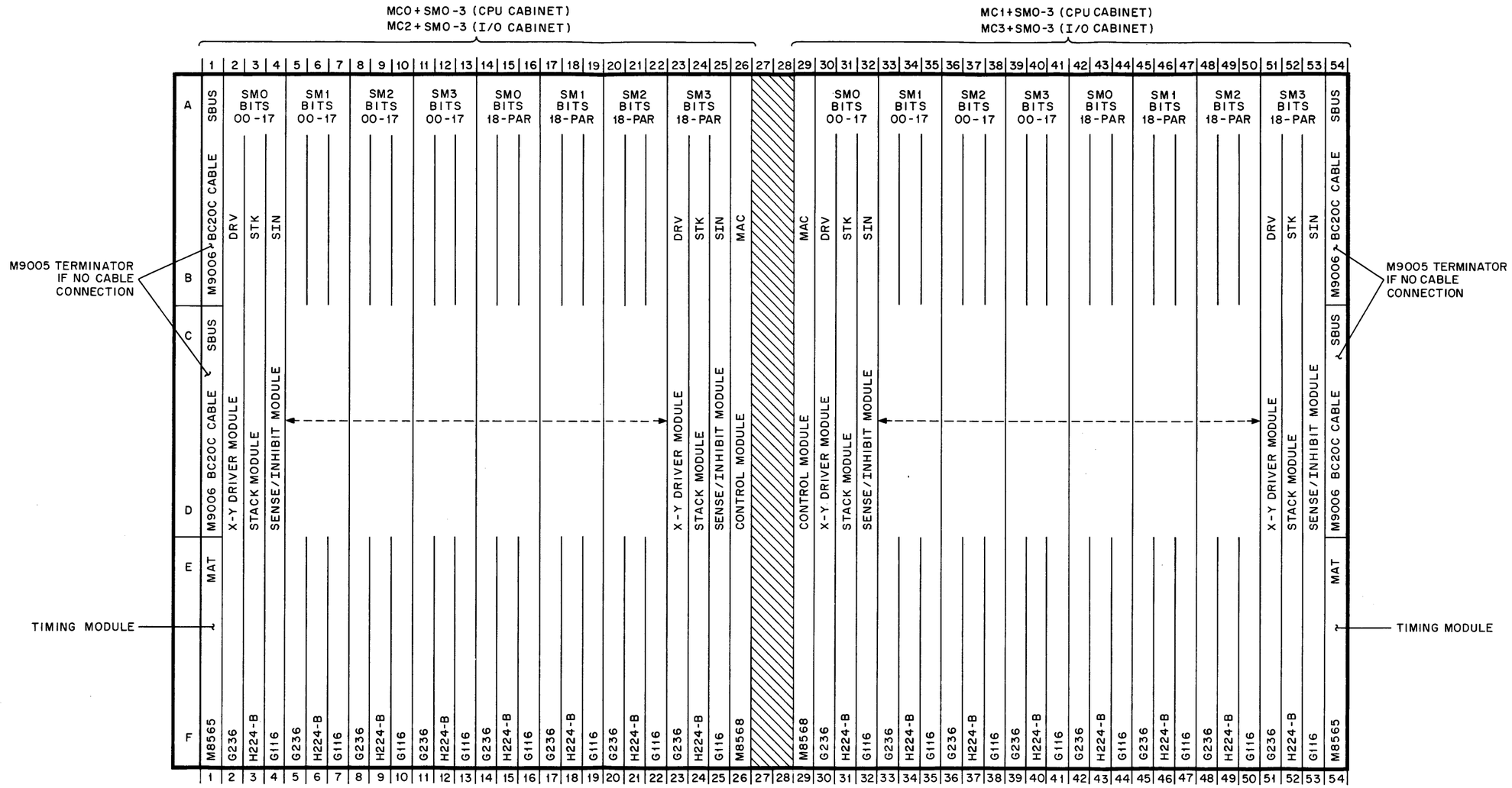
MB20-G (controller pair plus two storage modules)

1 – MB20-E
2 – M8568 control module
2 – M8565 timing module
2 – M9005 SBus terminator module
2 – H7420 power supply
4 – H744 power supply (+5 V)
6 – H754 power supply (+20 V)
2 – BC20C SBus cable
1 – 1213011 blower assembly
1 – 7012773 logic assembly

10.1.3 Applicable Documentation, Diagnostics, and Required Tools

1. Documentation

   a. MA20 Field Maintenance Print Set, MP00010
   b. MB20 Field Maintenance Print Set
   c. MA20 Internal Memory Unit Description, EK-MA020-UD-001
   d. MB20 Internal Memory Unit Description, EK-MB020-UD-001



NOTES:
1. Viewed from wire side
2. MU same for CPU and I/O cabinets

10-2653

Figure 10-2 MB20 Module Utilization

2. Diagnostics

    a. KLDCP
    b. CONEX
    c. DGKBB.A11
    d. DDMMD.A10
    e. DGMMA.A11
    f. DDMMG.A10 (for greater than 256K)
    g. U.RAM
    h. CONFIG.CMD

3. Required Tools

    a. Phillips head screwdriver
    b. Wire strippers
    c. Diagonal pliers
    d. Crimping tool
    e. Flat blade screwdriver
    f. Adjustable wrench
    g. Trimpot adjusting tool
    h. DVM
    i. Oscilloscope

4. Required Manpower: 2 field service people (1 of them trained in DECSYSTEM-20)

5. Time Required

    a. 8 hours to install and check out
    b. Overnight reliability run (approximately 12 hours)

10.1.4 MA20/MB20 Preinstallation (Skidded) Checkout

The item numbers in parentheses in the following paragraphs refer to tools listed in Table 10-1.

To save time and trouble in the case of catastrophic problems (shipping damage, etc.), the MA20/MB20 memory units have been packaged in such a way as to allow initial checkout of the unit while still skidded. Typically, the package as received will have the number 2 memory harness attached to the MA20/MB20 memory assembly and the H7420 power supplies.

For skidded checkout, where the skidded unit will be positioned will be determined by individual site conditions and by SBus cable length restrictions. SBus cables are provided in 5-ft lengths. The most convenient location is behind the CPU cabinet (with CPU cabinet door open), but if there is insufficient space here, an alternative will have to be found.

The only cable connections which will be made at this time are the SBus cables and the two H7420 power supply ac cords (item 15 or 16). The vane switch assembly or blower duct is not assembled at this time. Check to make sure fan ac voltage is connected. The memory unit will not be powered up more than fifteen minutes for this initial checkout period and should not be in danger of overheating. Care should be taken to prevent overheating. (For cable connections, refer to Figures 5-8 and 5-9.)

After the necessary cabling has been completed, perform the operations in Paragraph 10.1.6, steps 1–7 and 9–10. If there are no major problems after this initial testing, power down the machine and continue with the add-on installation. (Major problems are, for example, cracked backplanes. Logic problems, i.e., controllers or stacks, are not major problems and should not halt the installation.)

10.1.5 Mounting Procedures

1. Disconnect the dc harness from the regulators (H744, H754) on the H7420, and the ac harness (7010805-0-0) from the H7420 transformer housing.

2. Remove the two heads for the internal H7420 fans from plug no. 2, pins 7 and 3 on both power supplies.

   The MA20/MB20 memory assembly is to be installed on the mounting door of the I/O cabinet from the outside with the door closed. Refer to Figure 10-3.

3. With the mounting door of the I/O cab closed, install six Tinnerman nuts (item 5) on both the left and right uprights, with nut portion on far side, using holes no. 29, 38, 52, 61, 63, and 69, counting from the bottom of the door. Refer to Figure 10-3.

   CAUTION
   Do not attempt the next step with fewer than two people.

4. Install the MA20/MB20 memory assembly on the door using the four lowest Tinnerman nuts (on each upright) with eight screws and external-tooth lock washers (items 6 and 7). Refer to Figure 10-3.

   CAUTION
   Note that the harness attached to memory assembly is allowed to hang free during step 4.

5. Install foam tape (item 18) along the perimeter of the blower assembly opening which butts up against the duct assembly. Install duct assembly on door using two upper Tinnerman nuts with four screws and external-tooth lock washers. Refer to Figure 10-3.

6. Coil up the harness and insert it under the wire assembly where shown so that it may be routed to adjoining cabinet (Figure 10-3).

7. Move to CPU cabinet and open mounting door to fully open position (Figure 10-4).

   NOTE
   The power supplies are installed on the mounting door of the CPU cabinet from the inside with the door open. Refer to Figure 10-5.

8. To the left upright only, install six Tinnerman nuts with nut portion on far side, in holes 2, 5, 8, 19, 22, and 25. Reference KL10E Vol. 1, Sheet 18 of 34 (Arithmetic Processor).

9. Remove regulators from power supplies.

10. Assemble one H7420 power supply to upper three Tinnerman nuts with three screws and three external-tooth lock washers. To the right (far side) of power supply, assemble with four screws and four external-tooth lock washers into inserts on upright.

11. Repeat for second H7420 with lower Tinnerman nuts.

12. Replace regulators (H744, H754) into H7420 power supplies with P1, P2, P6, and P7 going to H744 and P3, P4, P5, P8, P9, and P10 to H754 regulators. Use one thumb screw for each regulator from underneath supply and two screws and washers in the top of each regulator. Refer to Figure 10-5.

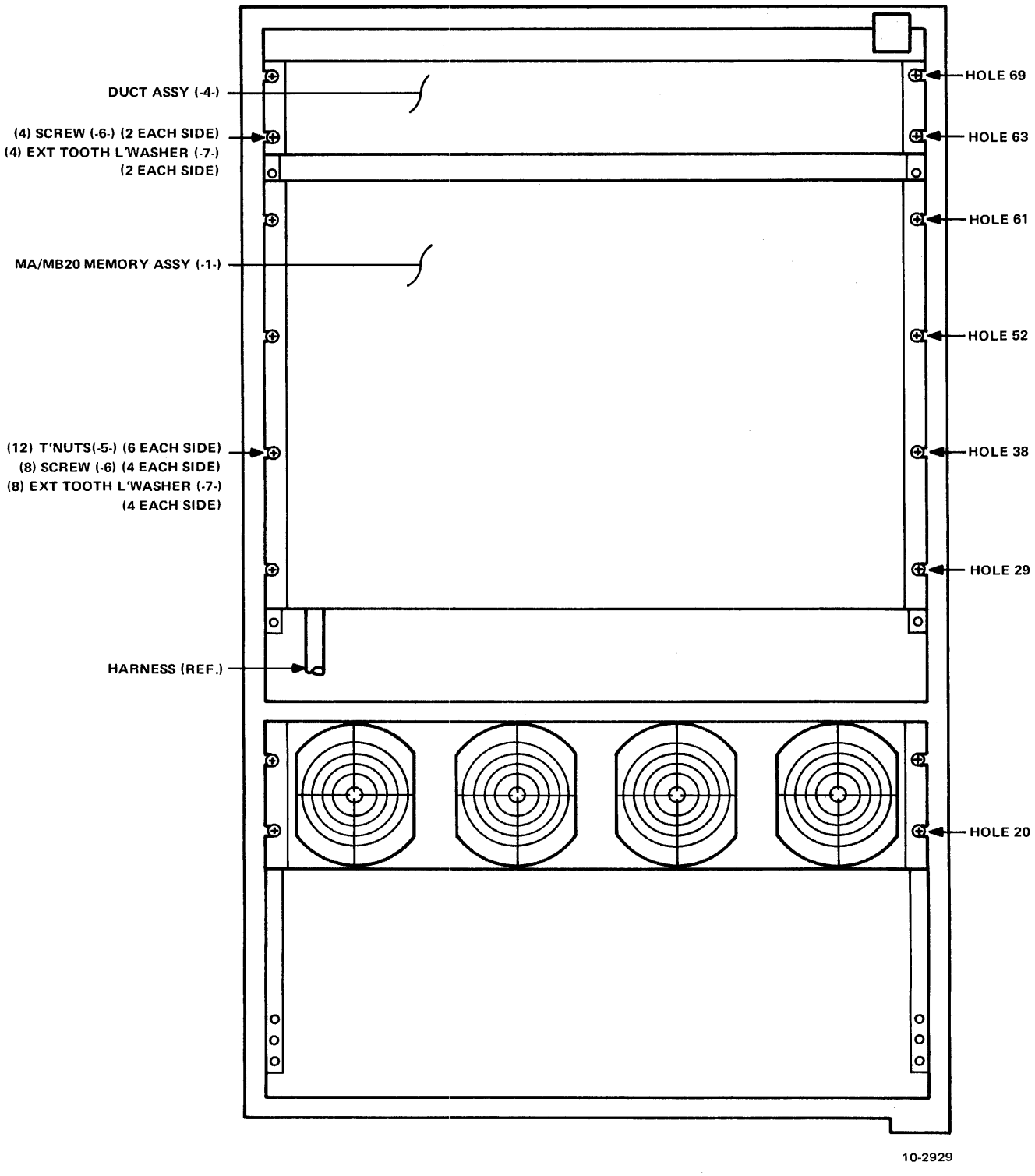


Figure 10-3 I/O Processor Cabinet (Rear View - Doors Removed)

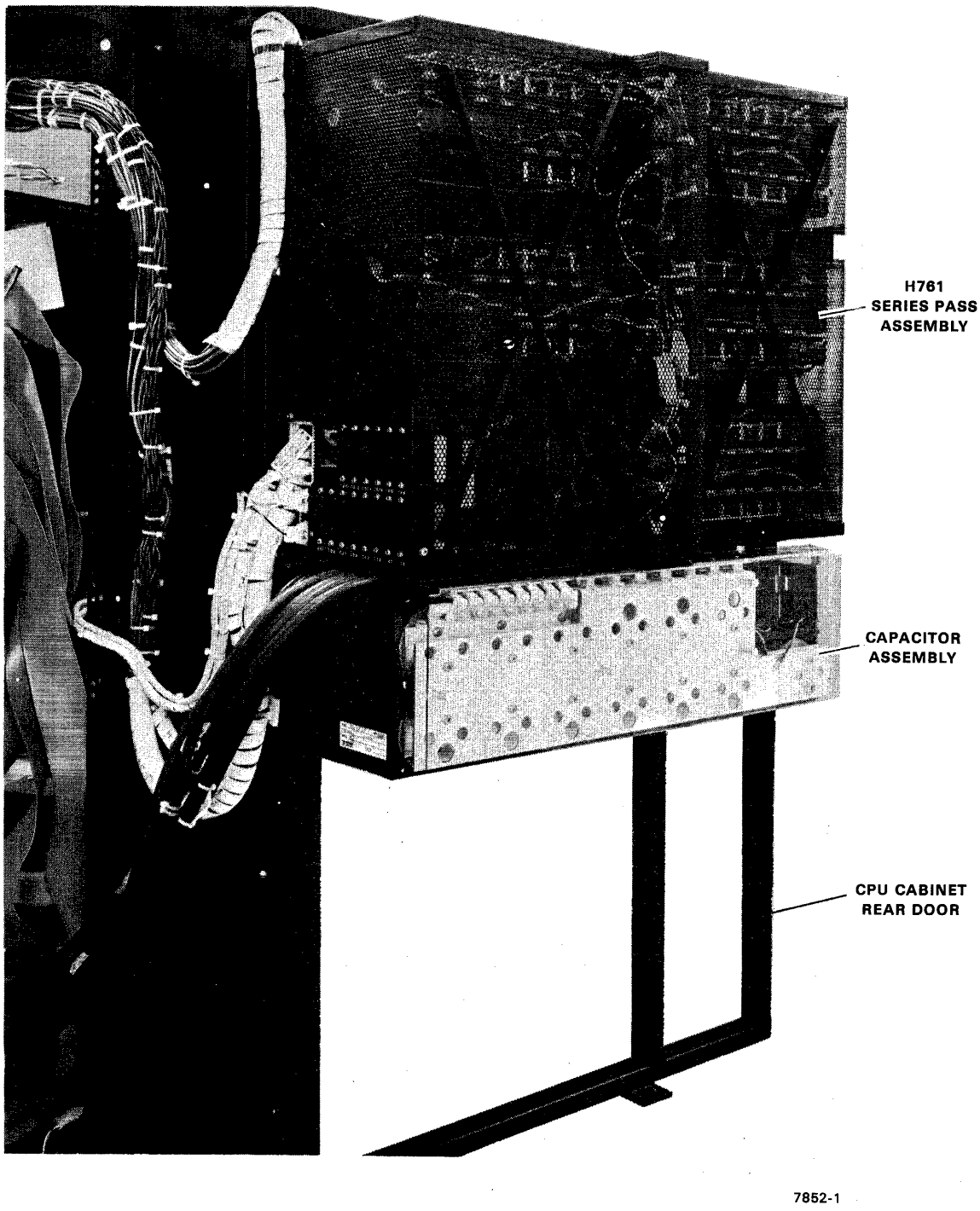


Figure 10-4 CPU Cabinet (Inner Door)

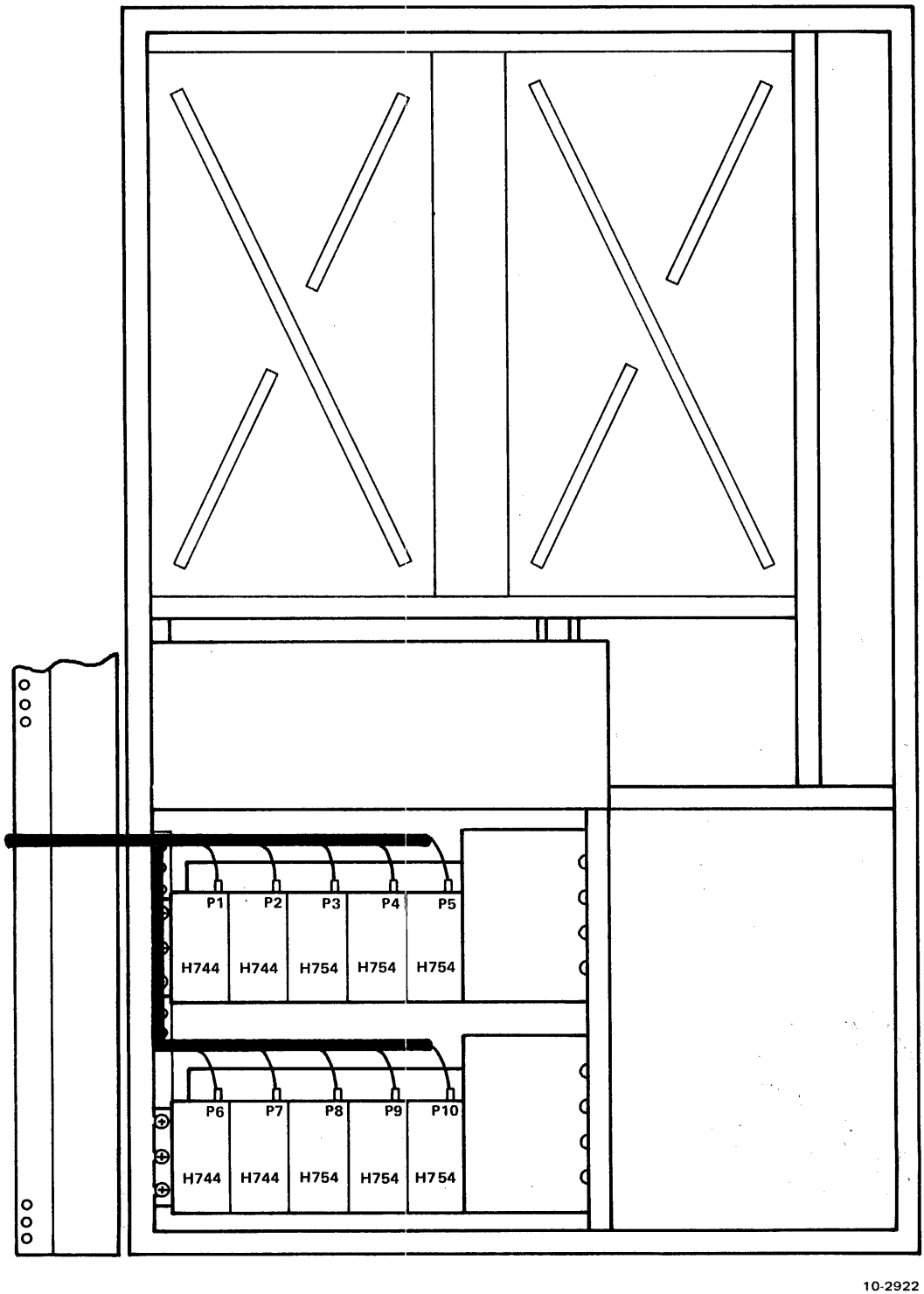


Figure 10-5 DC Power Supplies and Regulators
(I/O Processor Cabinet) (Sheet 1 of 2)

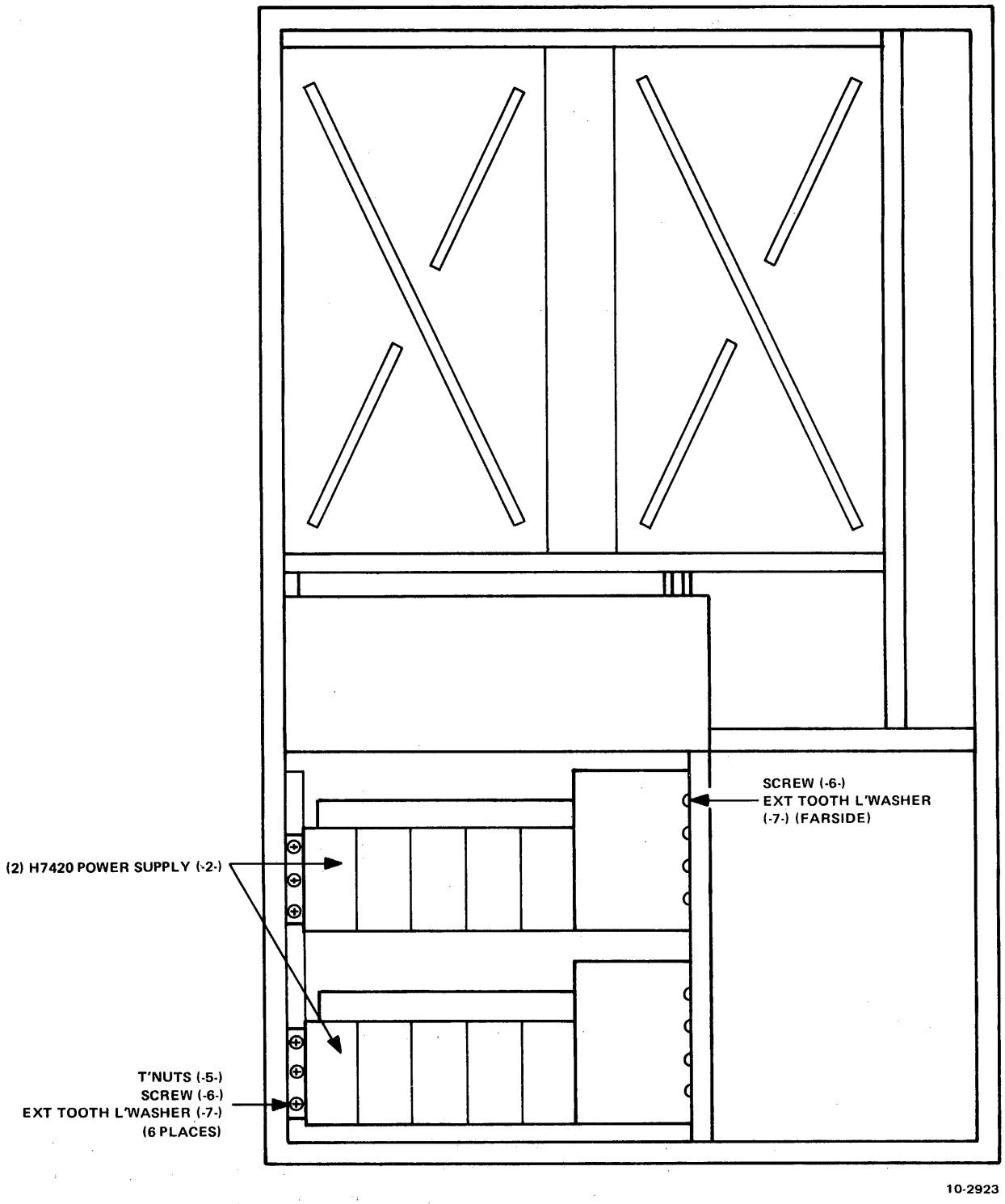


Figure 10-5 DC Power Supplies and Regulators
(I/O Processor Cabinet) (Sheet 2 of 2)

13. Route the harness from the memory assembly in the I/O cabinet to the H7420 power supplies using adhesive backed mounts and cable ties (items 8 and 9) as necessary. Install the Mate-N-Lok connectors to the power supplies as shown in Figure 10-5 and install the red and white leads from the internal H7420 fans in hole 7 for the red lead, and hole 3 for the white lead in P2. P2 mates with J2 and P3 mates with J3 (Figure 10-6).

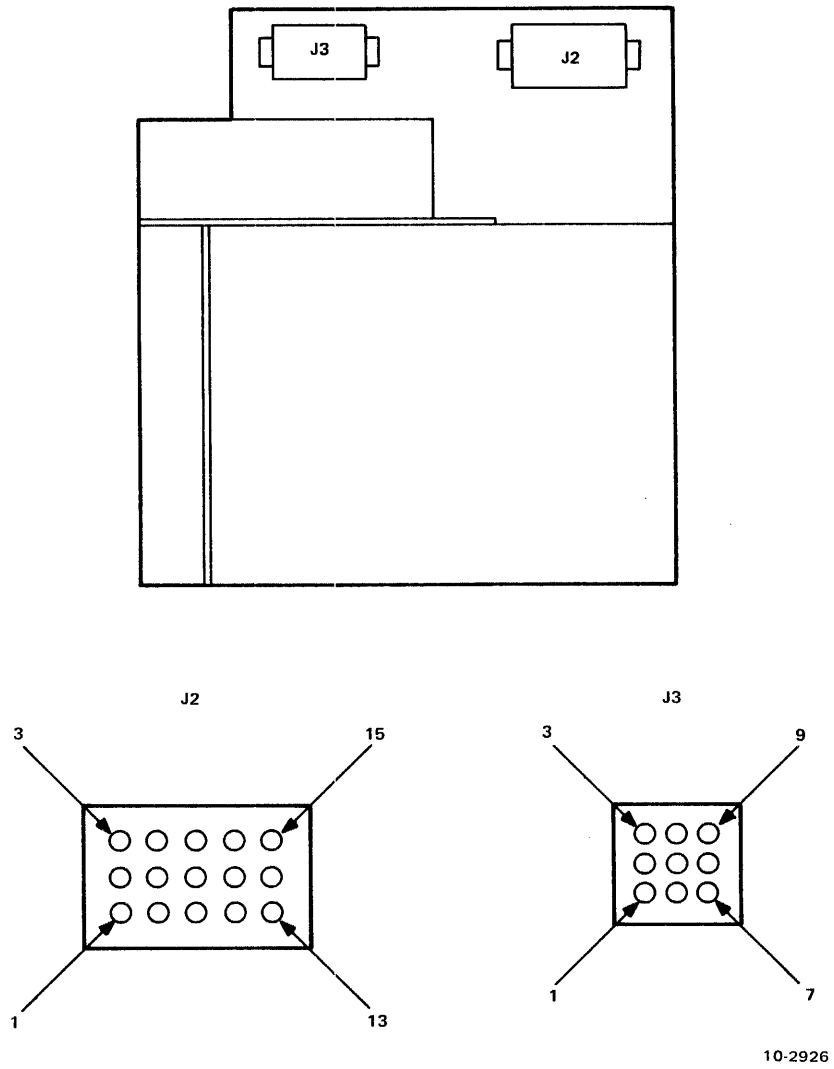


Figure 10--6 Connector J2 and J3, Pin Identification

14. Strip end of red and white twisted pair wire (item 10) at 3/16 inch and crimp on two contact pins (item 12). Plug these into the J2 Mate-N-Lok on the lower H7420 (white lead into P2 pin 5 and red lead into P2 pin 6, Figure 10-6). Route these leads along cabinet channel to the memory blower assembly. When correct length is established, cut, strip, and terminate lead ends as described above. Then get the 3-pin connector housing (item 11), and insert the white lead into hole 1 and the red lead into hole 2. Then attach this connector housing to the Mate-N-Lok on the blower. Use spiral wrap where necessary to prevent cut-throughs.

15. Located inside the I/O cabinet mounting door are two Mate-N-Loks bundled with the fault indicator harness. Untie this section and route the P5 Mate-N-Lok to the memory assembly vane switch assembly and plug into existing Mate-N-Lok.

16. Route the J3 Mate-N-Lok to the memory assembly door switch and connect to existing Mate-N-Lok. Tie wrap wires to the vane switch bracket where necessary to support cable.

17. Route the two power cords from the H7420 power supplies into the CPU cabinet and toward the front end cabinet. Attach these power cords to the power cord extensions for the specific system as follows.

    60 Hz – power cord extensions no. 9107673-09 (item 15)
    50 Hz – power cord extensions no. 7011432-03 (item 16)

    Continue run to front end and plug the power cord extension from the upper H7420 power supply into the 863 power controller at J24, and the power cord extension from the lower H7420 power supply into the 863 and J26. Refer to Figure 5-8. Use cable ties and cable tie mounts to make neat runs of all wires and cords which have been installed.

18. This step is the installation of the SBus cables. First remove the doors from the CPU and MA20/MB20 logic assemblies. Install the two SBus cable assemblies (item 17) as follows (refer to Figure 5-9).

    Slot 1, row A, B of memory to slot 2, row A, B of CPU
    Slot 1, row C, D of memory to slot 2, row C, D of CPU

    Replace the logic assembly doors

    NOTE
    Replacing these doors is easier if the plastic strip along the side of the door is removed first. This strip is to be replaced after the door is refitted.

19. Note that on the inner end of each H7420 power supply there is a ground stud. Place an external-tooth lock washer on each ground stud. Then place an end from each ground strap (item 13) on each ground stud and assemble with two kep nuts (item 14). Route both ground straps to convenient holes on the cabinet upright and assemble as shown in Figure 10-7. Attach ground strap to fan housing.

10.1.6 Checkout and Acceptance Procedure

1. Check for shorts between the voltage terminals and ground on the MA20/MB20 backpanel.

2. Visually inspect the backpanel for bent or crushed pins, broken wires, materials lodged between pins, or any other abnormality.

3. Visually inspect between logic cards for lodged foreign material.

4. Ensure all modules are in their correct slot and are installed properly.

5. Ensure that all connections are secure.

6. Using the chart in Figure 10-8, check to ensure that the appropriate backplane jumpers are installed to select the add-on memory controller as C2 and C3.

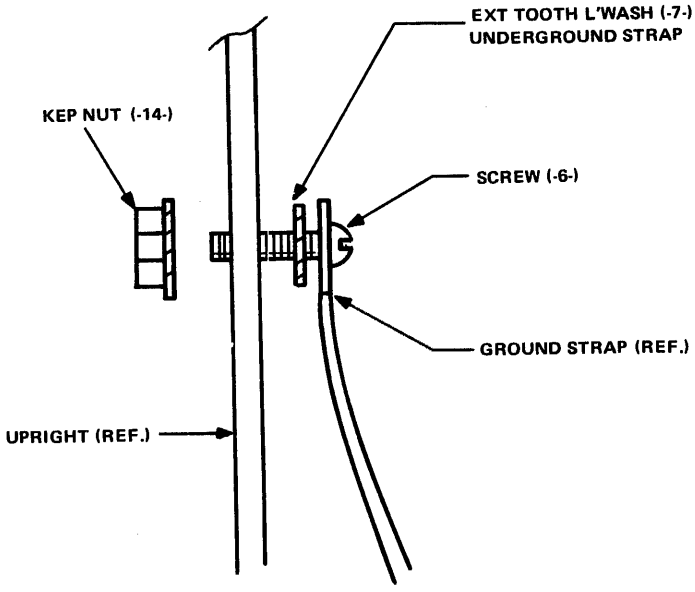


Figure 10-7 Ground Strap Installation

HARDWIRED CONTROLLER SELECTION		
	PIN EF2	PIN EE1
C0	GND	GND
C1	GND	—
C2	—	GND
C3	—	—

M8561/M8568

FIRST CONTROLLER: SLOT 26 (C0, C2)

SECOND CONTROLLER: SLOT 29 (C1, C3)

* SEE MUL CHART

10-2928

Figure 10-8 Memory Controller Jumper Installation

7. Apply power and check for obvious problems (e.g., smoke). Check to ensure that all fans are operating. Using a DVM, check and adjust all voltages (+5, -20, -5) at the backplane tabs. Refer to the MA20 print set drawing MA20 AC/DC Power Wiring, D-IC-MA20-0-0-PW, to relate each power tab to its associated regulator. Note that sheet 1 of this drawing applies to the add-on memory, sheet 2 applies to the first MA20.

8. Check to ensure that blocking air flow over each vane switch or opening the logic assembly door will power down the machine (check LEDs on 863 also). Check H770 regulator which supplies +15 V to vane switches.

9. Check the MA20/MB20 deskew using the procedure described in the MA20/MB20 Memory Print Set or Paragraph 8.18 of this manual.

10. Run DGKBB.A11 as a basic check at CR0, CS0.

11. Run MARGIN.CMD at CR0, CS0 all switches set to 0. MARGIN will run all margins on internal memory. The Instruction/Set-Up sheet (D-BS-MA20-0-INS) in the MA20 print may be helpful in isolating failures.

12. At CR0, CS0, console switch 6 set to a 1 (up: reliability mode). All memory must run DDMMD overnight (12 hours) with no failures. (See Table 10-2.)

10.2 KL10-PV UPGRADE PROCEDURE FOR KL10-C

1. Obtain all resources listed in Paragraph 10.2.1.

2. Obtain permission to remove all customer software media and then remove them. (Disks, floppies, magnetic tapes and DECtapes)

3. Refer to Paragraph 10.2.2 to run the required diagnostic at this time (Model A CPU system diagnostic).

4. a. Turn the power off at the system console.

   b. Turn off the main 3-phase circuit breaker CB1 in the 863 power supply.

   c. Turn off the wall circuit breaker to the system.

5. a. Remove the top cover to the CPU assembly cabinet. Label and disconnect the ground strap.

   b. Remove the side panel of the cabinet. Label and disconnect the ground strap at the bottom of the panel.

   c. Remove the doors. Label and disconnect the ground straps.

   d. Remove the front trim bar and blower filter. Label and disconnect the ground strap.

   e. Remove the air intake shroud.

   f. Remove the UL screens at the bottom of the cabinet.

Table 10-2 DDMMD: Right-Hand Switch Settings

Switch Number	Mnemonic	Functional Description
18	SWCON	Use switches for test control – testing parameters input from RH switches rather than from TTY.
19	EXTDIN	Extended input format – used to specify and run on selected MA bit in fast rate addressing. If in switches mode also allows user to type in selection of specific data patterns for the data patterns test and for the WCP test.
20	WCPIT2	WCP interleave – sets up WCP for interleaved modules.
21	WCPSW3	Module type selection (WCP test)
22	WCPSW2	0 = run all module types
23	WCPSW1	1 = MA10 2 = MB10 64 × 64 3 = MB10 128 × 128 4 = MD10 5 = ME10 6 = alt. 1s and 0s 7 = 1s and 0s checkerboard
24	TSTSW3	Test Selection
25	TSTSW2	0 = data patterns, address, WCP, float I/O
26	TSTSW1	1 = data patterns 2 = address 3 = WCP 4 = float 1s/0s 5 = heating 6 = address and WCP 7 = all tests
27	INHMSK	Inhibit error checking on mask. Do not report errors in bits masked by 1s in location mask (4037).
28	INHCMP	Inhibit data complement (R/C/W) when executing fast rate addressing. Do a read restore instead.
29	INHBLT	Inhibit block transfer cycles.
30	INHFR	Inhibit fast rate addressing.
31	INHRR	Inhibit read restore cycles. WCP – RCW cycles.
32	NOPARP	Inhibit parity error typeout.
33	NOERPT	Inhibit data error typeout.
34	LOCKPG	USER – lock program in core.
35	PNTTLS	Print totals at compleetion of all selected tests.

6. a. Remove the card cage doors on the CPU assembly cabinet.

   b. Remove the diffuser screen.

   c. Unplug the ac power to the blower above the CPU assembly.

   d. Remove the blower straight out from the rear.

7. a. Unplug the vane switch connector P4.

   b. Cut the tie wraps holding the blue/black twin pair for the door switch.

   c. Remove the vane switch assembly.

8. a. Carefully remove and label the end of each cable in CPU assembly slots 1, 2 and/or 3.

   b. Place covers on these cables and place them out of the way (back to I/O bay).

9. Reinstall the card cage rear doors.

10. Disconnect the dc harness using a small plier, grabbing each Faston at the crimp. Make sure each Faston is labeled.

11. a. Cut the four tie wraps holding the dc harness on top of the CPU assembly.

    b. Unscrew the cable clamps holding the dc harness on the bottom.

12. Place the supplied 2 × 4s under the CPU assembly as illustrated in Figure 10-9.

NOTE
The next steps are very important. Read steps 13 through 19 before proceeding.

13. Remove screw no. 2L from the left of the CPU assembly, freeing up the clamp; replace and tighten the screw. (Refer to Figure 10-9.)

14. a. With someone in back of CPU assembly (supporting unit), remove screw no. 1L and no. 1R.

    b. Remove the bottom screws no. 3R, no. 4R, no. 3L and no. 4L.

15. a. Remove the remaining tie wraps that prevent placing the harness out of the way.

    b. Place the complete harness out of the way (on top of the I/O cabinet).

NOTE
In handling the 150 lb CPU assembly, use the outer perimeter to hold it, not the card cage. (See Figure 10-10.) Use three people.

16. With one person in back of CPU assembly at all times, remove screws no. 2R and no. 2L (the box rests on the 2 × 4s).

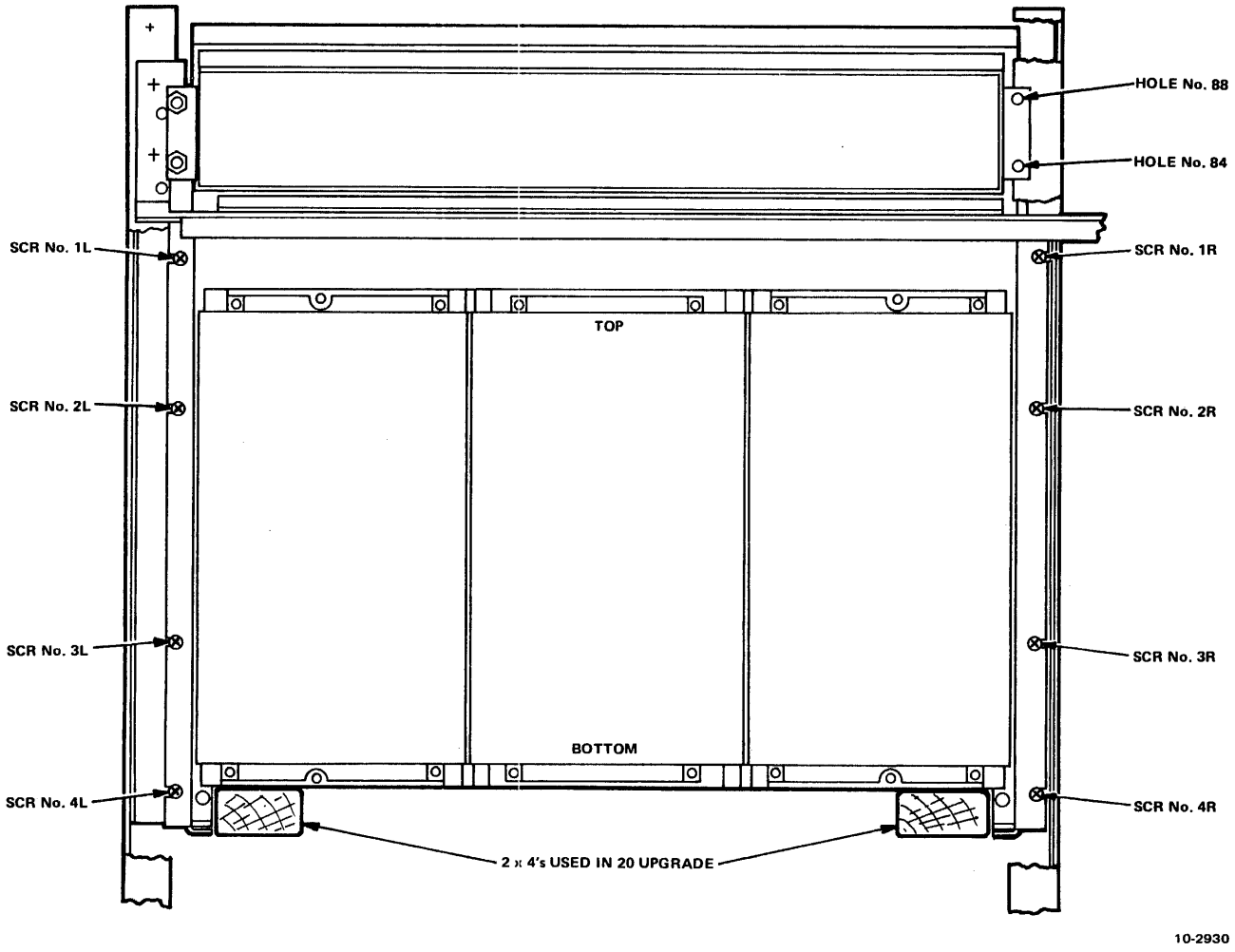


Figure 10-9 KL10-PV Assembly

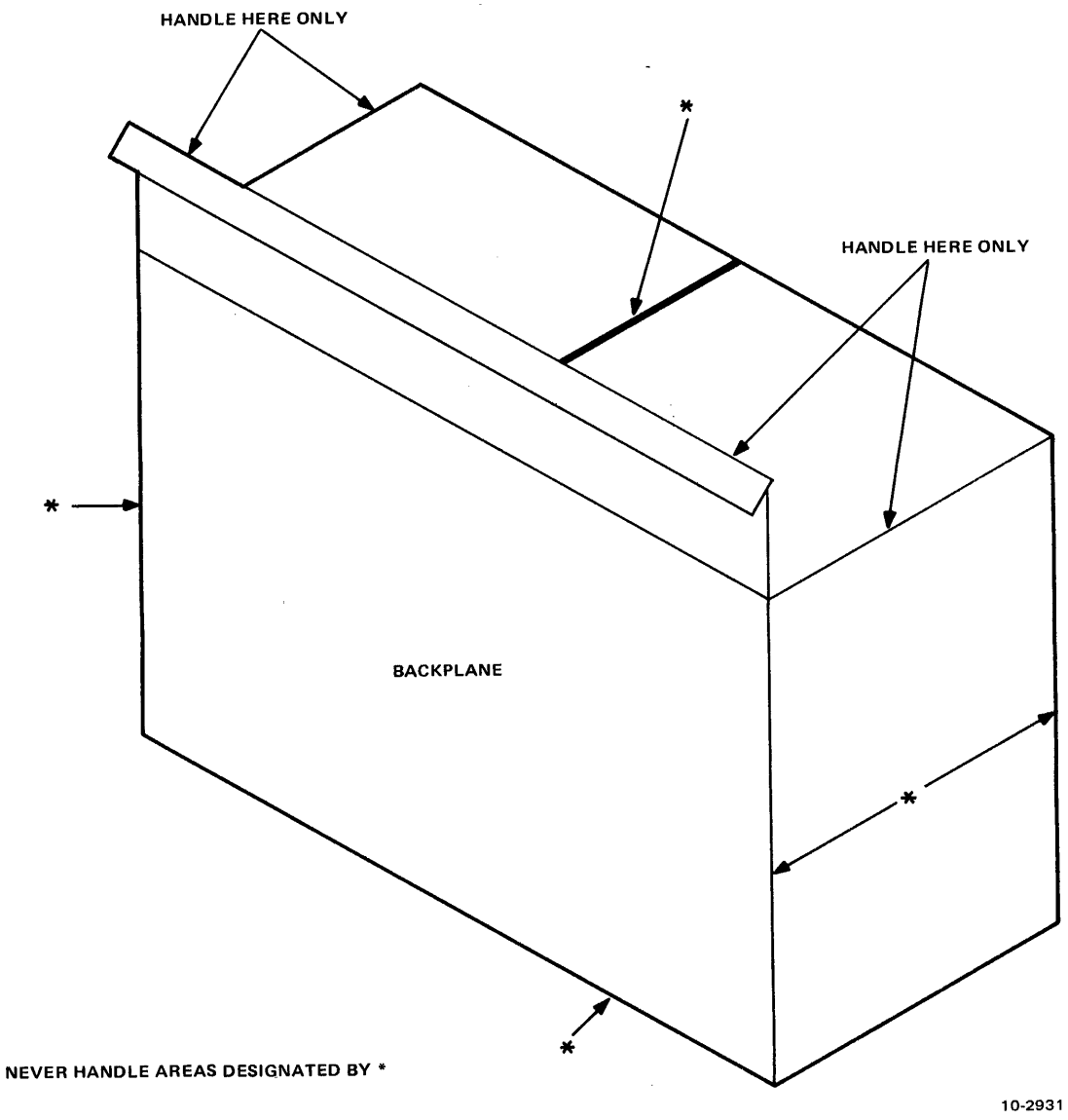


Figure 10-10 Handling of CPU Assembly

17. While the CPU assembly is resting on the 2 × 4s and is being held by someone in front and rear, have a third person remove the bracket that is bolted to the frame (as illustrated in Figure 10-11) using a socket wrench (7/16).

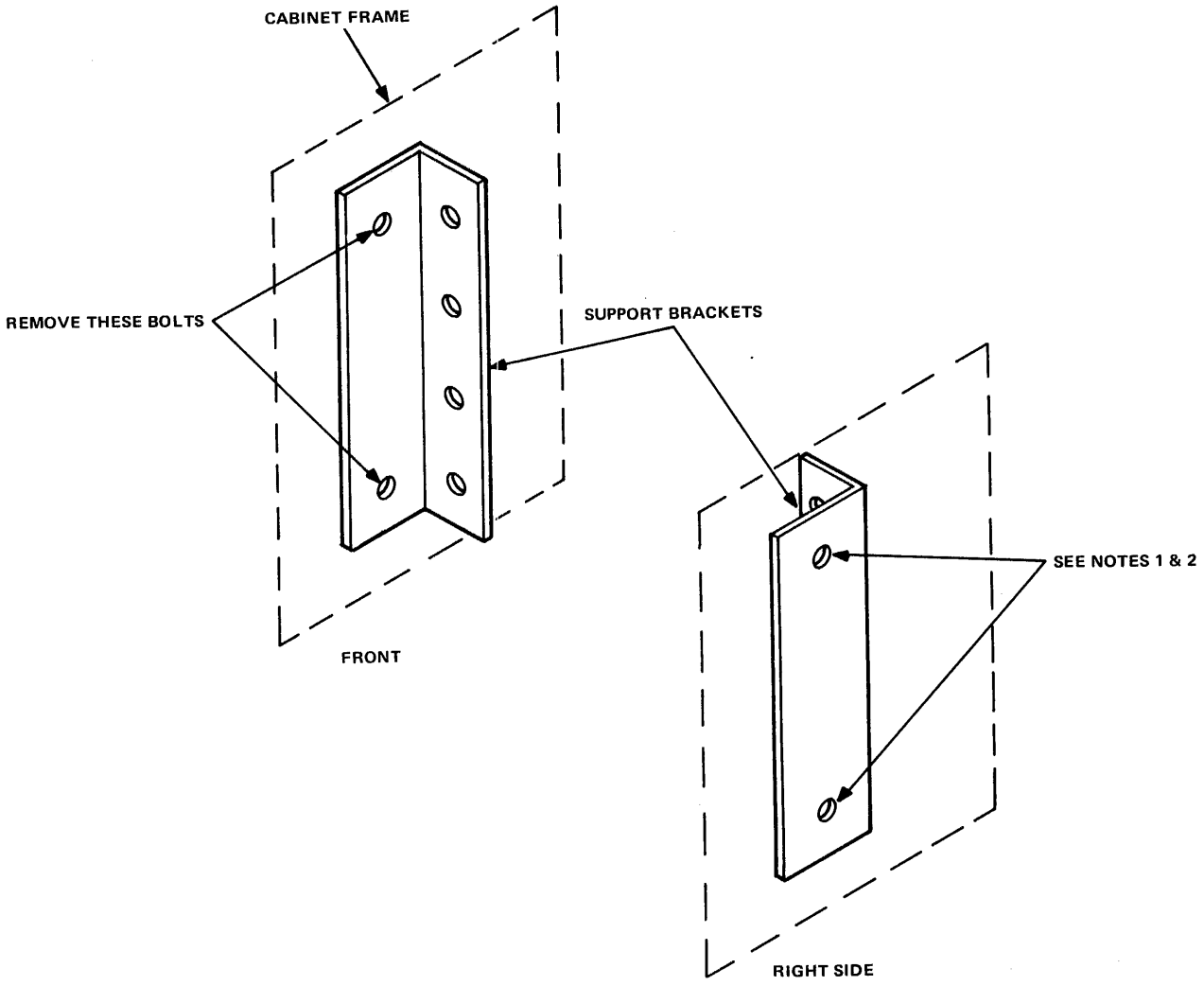


Figure 10-11 Support Bracket Bolts

18. Carefully guide the CPU assembly out from the front of the cabinet and place it on the floor. (Make sure that the left side – slot 1 – exits first.)

19. Remove the KL10-PV from the shipping assembly.

20. a. Place the 2 × 4s on the memory blower assembly.

    b. Insert the new KL10-PV assembly on the 2 × 4s by placing the right end in first (slot 54). Make sure that someone is in back of the assembly.

21. a. Install the support brackets to the frame.

    b. Line up the KL10-PV assembly with the support brackets.

    c. Install the second screws from the top on the left and right of the KL10-PV assembly (see Figure 10-9, screws 2L and 2R).

    d. Install the bottom screws on the right and left (see Figure 10-9, screws 4R and 4L).

22. Reconnect all the Faston connectors for the dc harness to their proper tabs. Refer to notes taken in step 10.

23. a. Replace the harness clamps removed in step 11b.

    b. Install the tie wraps removed in step 11a.

24. a. Replace the wraps removed in step 15a.

    b. Install the cable clamps for screws no. 1 and no. 3 on the right and left of the KL10-PV assembly. Tighten these screws.

    c. Secure the cable clamps for screws no. 2 and no. 4 on the right and left of the KL10-PV assembly. Tighten these screws.

    d. Now the 2 × 4s are free to be removed.

25. a. Reinstall the vane switch assembly. (See step 7.)

    b. Replace the blue/black twin pair for the door switch and tie wrap TAC plug.

    c. Plug the vane switch connector P4.

26. a. Reinstall the blower assembly. (See step 6.)

    b. Plug the ac power to the blower above the CPU assembly.

    c. Reinstall the diffuser screen.

    d. Reinstall the UL screens.

27. a. Remove the card cage doors on the KL10-PV assembly.

    b. Remove the necessary modules to reinstall the removed cables in step 8 properly.

    c. Replace the removed modules after reinstalling the cables.

    d. Double-check the modules in all slots against the module utilization print for proper slots.

    e. Make sure all modules are seated.

28. a. Replace the air intake shroud.

    b. Replace the trim bar.

    c. Replace the blower filter and connect the ground strap.

    d. Replace the side panel and connect the ground strap.

    e. Check for miscellaneous items or tools on top of the cabinet; then replace the top cover and connect the ground strap.

29. a. Inspect the KL10-PV assembly backplane for bent pins or loose items such as washers, etc.

    b. Inspect the memory backplane similarly.

    c. Double-check the Faston connectors of the dc harness for physical integrity and proper connection (i.e., 5 V wire to 5 V tab, etc.).

    d. Reinstall the front doors and connect the ground straps.

30. a. Turn on the wall circuit breaker for the system.

    b. Turn on the 3-phase main circuit breaker CB1 of the 863 power supply.

    c. Resolve faults if indicated by console indicators.

    d. Turn the power on at the system console.

31. a. Check all tabs on KL10-PV backplane with an oscilloscope for the proper levels (i.e., -2, GND, -5.2 ripple).

    b. Check all dc power in the entire system at this point with digital voltmeter (Figure 10-12).

dc (TTL) voltage tolerance (measured at module power pins)	+5.0
	-5.0
	-15.0
	+20.0
dc (ECL) voltage tolerance (measured at sense tabs on CPU backplane)	-5.2
	-2.0

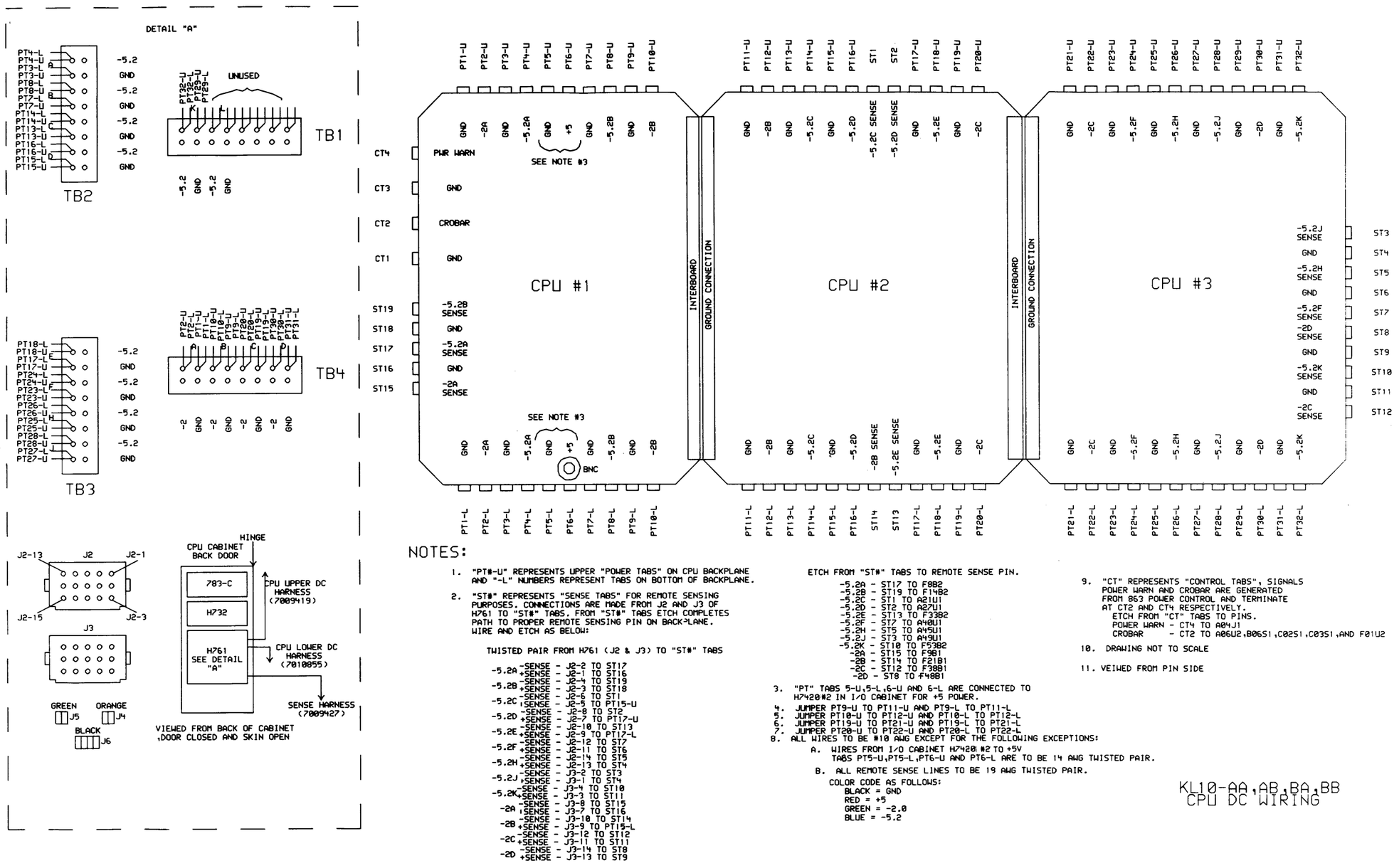
    c. Perform the deskew procedure adjustment in accordance with procedures given in the RH20 and MA20/MB20 print sets or Paragraphs 8.18 and 8.19 in this manual.

32. Run diagnostics according to Paragraph 10.2.2, and resolve all problems.

33. Bring up monitor in accordance with procedures given in the software installation manual.

34. Pack old KL10-C for shipment along with other related materials.

35. Clean up site.



NOTES:

1. "PT#-U" REPRESENTS UPPER "POWER TABS" ON CPU BACKPLANE AND "-L" NUMBERS REPRESENT TABS ON BOTTOM OF BACKPLANE.
2. "ST#" REPRESENTS "SENSE TABS" FOR REMOTE SENSING PURPOSES. CONNECTIONS ARE MADE FROM J2 AND J3 OF H761 TO "ST#" TABS. FROM "ST#" TABS ETCH COMPLETES PATH TO PROPER REMOTE SENSING PIN ON BACKPLANE. WIRE AND ETCH AS BELOW:

   TWISTED PAIR FROM H761 (J2 & J3) TO "ST#" TABS

   -5.2A -SENSE - J2-2 TO ST17
   +SENSE - J2-1 TO ST16
   -5.2B -SENSE - J2-4 TO ST19
   +SENSE - J2-3 TO ST18
   -5.2C -SENSE - J2-6 TO ST1
   +SENSE - J2-5 TO PT15-U
   -5.2D -SENSE - J2-8 TO ST2
   +SENSE - J2-7 TO PT17-U
   -5.2E -SENSE - J2-10 TO ST13
   +SENSE - J2-9 TO PT17-L
   -5.2F -SENSE - J2-12 TO ST7
   +SENSE - J2-11 TO ST6
   -5.2H -SENSE - J2-14 TO ST5
   +SENSE - J2-13 TO ST4
   -5.2J -SENSE - J3-2 TO ST3
   +SENSE - J3-1 TO ST4
   -5.2K -SENSE - J3-4 TO ST10
   +SENSE - J3-3 TO ST11
   -2A -SENSE - J3-8 TO ST15
   +SENSE - J3-7 TO ST16
   -2B -SENSE - J3-10 TO ST14
   +SENSE - J3-9 TO PT15-L
   -2C -SENSE - J3-12 TO ST12
   +SENSE - J3-11 TO ST11
   -2D -SENSE - J3-14 TO ST8
   +SENSE - J3-13 TO ST9

   ETCH FROM "ST#" TABS TO REMOTE SENSE PIN.

   -5.2A - ST17 TO F8B2
   -5.2B - ST19 TO F14B2
   -5.2C - ST1 TO A21U1
   -5.2D - ST2 TO A27U1
   -5.2E - ST13 TO F3B2
   -5.2F - ST7 TO A40U1
   -5.2H - ST5 TO A45U1
   -5.2J - ST3 TO A49U1
   -5.2K - ST10 TO F5B2
   -2A - ST15 TO F9B1
   -2B - ST14 TO F21B1
   -2C - ST12 TO F38B1
   -2D - ST8 TO F48B1

3. "PT" TABS 5-U,5-L,6-U AND 6-L ARE CONNECTED TO H7420#2 IN I/O CABINET FOR +5 POWER.
4. JUMPER PT9-U TO PT11-U AND PT9-L TO PT11-L
5. JUMPER PT10-U TO PT12-U AND PT10-L TO PT12-L
6. JUMPER PT19-U TO PT21-U AND PT19-L TO PT21-L
7. JUMPER PT20-U TO PT22-U AND PT20-L TO PT22-L
8. ALL WIRES TO BE #10 AWG EXCEPT FOR THE FOLLOWING EXCEPTIONS:
   A. WIRES FROM I/O CABINET H7420 #2 TO +5V TABS PT5-U,PT5-L,PT6-U AND PT6-L ARE TO BE 14 AWG TWISTED PAIR.
   B. ALL REMOTE SENSE LINES TO BE 19 AWG TWISTED PAIR.

   COLOR CODE AS FOLLOWS:
   BLACK = GND
   RED = +5
   GREEN = -2.0
   BLUE = -5.2

9. "CT" REPRESENTS "CONTROL TABS", SIGNALS POWER WARN AND CROBAR ARE GENERATED FROM 863 POWER CONTROL AND TERMINATE AT CT2 AND CT4 RESPECTIVELY.
   ETCH FROM "CT" TABS TO PINS.
   POWER WARN - CT4 TO A04J1
   CROBAR - CT2 TO A06U2,B06S1,C02S1,C03S1,AND F01U2
10. DRAWING NOT TO SCALE
11. VEIWED FROM PIN SIDE

KL10-AA,AB,BA,BB
CPU DC WIRING

10-2632

Figure 10-12 KL10-PV CPU dc Wiring (Pin Side View)

10.2.1 PV Upgrade Resources

10.2.1.1 On-Site or Locally Supplied Resources

Time Required

1. Eight hours for upgrade
2. 72 hours for reliability test
3. "X" hours for customer acceptance

Personnel Requirements

1. Three field service people (one of these familiar with "B" diagnostics and hardware)
2. Software specialist (required after hardware installation is complete)

Test Equipment Required

1. Digital voltmeter accuracy ±0.05% or better on dc voltages
2. Oscilloscope (Tektronix type 465, 475, 7000 series, or equivalent accuracy)
3. 3 probes of equal length and ground clips
4. Microfiche reader
5. DEC tool kit
6. Socket set or two 7/16 open wrenches

10.2.1.2 Resources To Be Supplied (Shipped)

1. New prints
2. New microfiche (for uncode, wire lists, test writeups)
3. Floppy disks for diagnostics
4. Miscellaneous

    a. Spare tie wraps (part no. 9007032)
    b. Faston connectors (part no. 9007920, 9007969, 9007970)
    c. Two pieces of wood 2 in × 4 in × 18 in
    d. Spare bolts for support brackets (1/4 – 20 × 5/8) part no. 9006242-09

10.2.2 Diagnostic Test Programs

10.2.2.1 Model A CPU System

CPU Tests

1. DGKAA – EBox Test No. 1
2. DGKAB – EBox Test No. 2
3. DGKBA – MBox Test No. 1
4. DGKBB – Memory Control Test
5. DGKBC – Paging Logic Test
6. DGMCA – Cache Option Test
7. DGMCB – RAM Banger Test
8. DGKBD – Channel Logic Test
9. DGKBE – Channel Loopback Test
10. DGKCA – Meter Board Test
11. DFKBB – Cache Reliability
12. DFKAA – Basic Instruction Test No. 1

13. DFKAB - Basic Instruction Test No. 2
14. DFKAC - Basic Instruction Test No. 3
15. DFKBA - Basic Instruction Reliability
16. DFKCA - Advanced Instructions
17. DFKDA - CPU/PI/Memory Reliability
18. DFKEA - Paging Hardware
19. DFKEB - MUUO and User Mode Test
20. DFKAD - Basic Instruction Test No. 4

DTE20 Tests

1. DGDTE - Basic DTE Test
2. DFDTE - DTE Reliability Test

DMA20/MA20/MB20 Tests

1. DDMMD - Memory Exerciser
2. DDMME - BLT Test
3. DDMMF - Floating Ones and Zeros Test
4. DDMMG - Memory Exerciser (over 256K)
5. DGMMA - Memories Exerciser

LP20 Test

1. DZLPL - LP20 Logic and Printer Test

RH20 Tests

1. DFRHB - Tests RH20s - does not use any Massbus devices
2. DFSXA - System 20 exerciser - tests RH20s with or without Massbus devices

TU45/TM02 Tests

1. DFRHB - RH20 Fault Isolator
2. DFTUE/K - TU45 Device Test
3. DFTUF - TU45 Multidevice Test

RP04/RP06

1. DFRPH - RP04 Device Test
2. DFRPK - RP06 Device Test
3. DDRPI - RP04/RP06 Reliability Test

10.2.2.2 Model B CPU System

CPU Tests

1. DHKAA - EBox Test No. 1
2. DHKAB - EBox Test No. 2
3. DHKBA - MBox Test No. 1
4. DHKBB - Memory Control Test
5. DHKBC - Paging Logic Test
6. DHMCA - Cache Option Test
7. DHMCB - RAM Banger Test

8. DHKBD - Channel Logic Test
9. DGKBE - Channel Loopback Test
10. DHKCA - Meter Board Test
11. DFKBB - Cache Reliability
12. DFKAA - Basic Instruction Test No. 1
13. DFKAB - Basic Instruction Test No. 2
14. DFKAC - Basic Instruction Test No. 3
15. DFKBA - Basic Instruction Reliability
16. DFKCA - Advanced Instructions
17. DFKDA - CPU/PI/Memory Reliability
18. DFKEA - Paging Hardware
19. DFKEB - MUUO and User Mode Test
20. DFKAD - Basic Instruction Test No. 4

DTE20 Tests

1. DGDTE - Basic DTE Test
2. DFDTE - DTE Reliability Test

DMA20/MA20/MB20 Tests

1. DDMMD - Memory Exerciser
2. DDMME - BLT Test
3. DDMMF - Floating Ones and Zeros Test
4. DDMMG - Memory Exerciser (over 256K)
5. DGMMA - Memory Exerciser

LP20 Test

1. DZLPL - LP20 Logic and Printer Set

RH20 Tests

1. DFRHB - Does not use any Massbus devices
2. DFSXA - System 20 exerciser - tests RH20s with or without Massbus devices

TU45/TM02 Tests

1. DFRHB - RH20 Fault Isolator
2. DFTUE/K - TU45 Device Test
3. DFTUF - TU45 Multidevice Test

RP04/RP06

1. DFRPH - RP04 Device Test
2. DFRPK - RP06 Device Test
3. DDRPI - RP04/RP06 Reliability Test

10.2.3 PDP-10 KL10 Instruction Timing Test (DFKFB)

VERSION 0.1, SV=0.11, CPU#G0, MCV=126, MCO=0, HO=30, 60 HZ

SWITCHES = 000000 000000

CLK SOURCE = NORMAL, CLK RATE + FULL, AC BLK 0, CACHE: 0 1 2

1 - BASIC CLOCK IS 40 NS.

2 - INDEXING TAKES 40 NS.

3 - INDIRECT TAKES 280 NS.

4 - INDEXING AND INDIRECT TAKES 320 NS.

5 - MOVEI TAKES 320 NS.

6 - MOVE FROM AC TAKES 440 NS.

7 - MOVE FROM MEMORY TAKES 480 NS.

8 - HRR FROM MEMORY TAKES 520 NS.

9 - STEOM 0 TAKES 560 NS.

10 - JRST TAKES 360 NS.

11 - JSR TAKES 680 NS.

12 - PUSHJ TAKES 840 NS.

13 - ADD FROM MEMORY TAKES 520 NS.

14 - MUL (9 ADD/SUB - 18 SHIFTS) TAKES 2.52 μS.

15 - DIV TAKES 5.58 μS.

16 - FIX A FLOATING POINT ONE TAKES 1.04 μS.

17 - FLTR AN INTERGER ONE TAKES 1.84 μS.

18 - FAD (1 RIGHT SHIFT) TAKES 1.88 μS.

19 - FAD (8 SHIFT RIGHT - 3 LEFT) TAKES 2.16 μS.

20 - FMP (7 ADD/SUB - 14 SHIFTS) TAKES 2.80 μS.

21 - FDV TAKES 5.72 μS.

22 - DMOVE FROM MEMORY TAKES 880 NS.

23 - DFAD (1 RIGHT SHIFT) TAKES 2.44 μS.

24 - DFAD (8 SHIFT RIGHT - 1 LEFT) TAKES 2.44 μS.

25 - DFMP (7 ADD/SUB - 32 SHIFTS) TAKES 4.92 μS.

26 - DFDV TAKES 10.32 μS.

27 - CONO PI TAKES 1.92 μS.

28 - CONI PI TAKES 3.36 μS.

29 - DATAO APR TAKES 1.56 μS.

30 - DATAI APR TAKES 1.76 μS.

31 - MOVE TO MEMORY TAKES 680 NS.

32 - LOGICAL SHIFT (35 PLACES LEFT) TAKES 640 NS.

33 - LOGICAL SHIFT (35 PLACES RIGHT) TAKES 760 NS.

34 - LOGICAL SHIFT COMBINED (71 PLACES LEFT) TAKES 1.12 μS.

35 - LOGICAL SHIFT COMBINED (71 PLACES RIGHT) TAKES 1.16 μS.

36 - INCREMENT BYTE POINTER TAKES 1.00 μS.

37 - INCREMENT AND LOAD BYTE TAKES 1.44 μS.

38 - INCREMENT AND DEPOSIT BYTE TAKES 1.80 μS.

39 - JFCL TAKES 880 NS.

40 - CAI TAKES 480 NS.

41 - JUMP TAKES 480 NS.

42 - CAM TAKES 600 NS.

43 - EQV AC TO AC TAKES 480 NS.

44 - EQV MEMORY TO AC TAKES 520 NS.

45 - SETOB TAKES 680 NS.

46 - AOS TO MEMORY TAKES 840 NS.

47 - EXCHANGE AN AC WITH AN AC TAKES 640 NS.

48 - EXCHANGE AN AC WITH MEMORY TAKES 840 NS.

49 - EXECUTE TAKES 640 NS.

50 - BLT MEMORY TO MEMORY TAKES 1.92 μS.

51 - BLT AC TO MEMORY TAKES 1.88 μS.

52 - DATAI TAKES 10.00 μS.

53 - DATAO TAKES 10.00 μS.

TEST COMPLETED

10.3 CACHE UPGRADE PROCEDURE

10.3.1 Introduction

The following are the procedural steps in upgrading a noncache DECSYSTEM-20 to a cached DECSYSTEM-20. It is necessary to follow these steps in order.

10.3.2 Test Equipment Required

1. Digital voltmeter with accuracy ±0.05 percent, or better, on dc voltage scales.
2. Oscilloscope (Tektronix type 465, 475 series, or equivalent accuracy).
3. Three probes of equal length with ground clips.

10.3.3 Upgrade Procedure

1. Run all system diagnostics at CR0, CS0 (25 MHz) and CR0, CS1 (28 MHz). Refer to Paragraph 10.2.2. If any failures occur in this step, problems must be resolved before continuing the upgrade procedure.

2. Power the system down and remove the following modules. Refer to module utilization (CPU).

M8549YH	Slot 17
M8549YH	Slot 19
M8549YH	Slot 24
M8549YH	Slot 25
M8549YE	Slot 27
M8549YF	Slot 28

3. Install the following modules in place of those removed.

M8521	Slot 17
M8521	Slot 19
M8521	Slot 24
M8521	Slot 25
M8514	Slot 27
M8515	Slot 28

Reference documentation for steps 2 and 3:

KL10-C/Vol. 2
Print KL10-0-CPU
Module Utilization (CPU).

4. Add CPU backpanel wire from pin 4E43A1 to pin 4D44E1 (cache available).

5. Power the system up and check all the dc power in the entire system at this point with digital voltmeter.

dc (TTL) voltage tolerance (measured at power module pins)	+5.0
	-5.0
	-15.0
	+20.0
dc (ECL) voltage tolerance (measured at sense tabs on CPU backplane)	- 5.2
	- 2.0

6. Check timing following the MA20/MB20/RH20 adjustment procedure contained in the respective print sets.

   If any timing is not within ± 1.0 ns of 50 percent points on the waveforms, readjust to within ± 1.0 ns before continuing with upgrade procedure.

7. Rerun all CPU, memory and system diagnostics at CR0, CS0 (25 MH) and CR0, CS1 (28 MHz) as listed in Paragraph 10.2.3.

8. Run DDFKFB (instruction timing test) at CR0, CS0 (25 MHz) and compare the output with the accompanying data in Paragraph 10.2.4.

10.3.4 Power Tab Identification Notes

1. "PT#-U" represents upper "power tabs" on CPU backplane and "-L" numbers represent tabs on bottom of backplane.

2. "ST#" represents "sense tabs" for remote sensing purposes. Connections are made from J2 and J3 of H761 to "ST#" tabs, from "ST#" tabs etch complete path to proper remote sensing pin on backplane.

   Twisted-pair from H761 (J2 and J3) to "ST#" tabs

-5.2A	-SENSE - J2-2 to ST17
	+SENSE - J2-1 to ST16
-5.2B	-SENSE - J2-4 to ST19
	+SENSE - J2-3 to ST18

-5.2C	-SENSE - J2-6 to ST1 +SENSE - J2-5 to PT15-U
-5.2D	-SENSE - J2-8 to ST2 +SENSE - J2-7 to PT17-U
-5.2E	-SENSE - J2-10 to ST13 +SENSE - J2-9 to PT17-L
-5.2F	-SENSE - J2-12 to ST7 +SENSE - J2-11 to ST6
-5.2H	-SENSE - J2-14 to ST5 +SENSE - J2-13 to ST4
-5.2J	-SENSE - J3-2 to ST3 +SENSE - J3-1 to ST4
-5.2K	-SENSE - J3-4 to ST10 +SENSE - J3-3 to ST11
-2A	-SENSE - J3-8 to ST15 +SENSE - J3-7 to ST16
-2B	-SENSE - J3-10 to ST14 +SENSE - J3-9 to PT15-L
-2C	-SENSE - J3-12 to ST12 +SENSE - J3-11 to ST11
-2D	-SENSE - J3-14 to ST8 +SENSE - J3-13 to ST9

Etch from "ST#" tabs to remote sense pin.

-5.2A - ST17 to F8B2
-5.2B - ST19 to F14B2
-5.2C - ST1 to A21U1
-5.2D - ST2 to A27U1
-5.2E - ST13 to F33B2
-5.2F - ST7 to A40U1
-5.2H - ST5 to A45U1
-5.2J - ST3 to A49U1
-5.2K - ST10 to F53B2
-2A - ST15 to F9B1
-2B - ST14 to F21B1
-2C - ST12 to F38B1
-2D - ST8 to F48B1

3. "PT" tabs 5-U, 5-L, 6-U and 6-L are connected to H7420 no. 2 in I/O cabinet for +5 power.

4. Jumper PT9-U to PT11-U A D PT9-L to PT11-L.

5. Jumper PT10-U to PT12-U and PT10 to PT12-L.

6. Jumper PT19-U to PT21-U and PT19-L to PT21-L.

7. Jumper PT20-U to PT22-U and PT20-L to PT220-L.

8. All wires to be no. 10 AWG except for the following.

   a. Wires from I/O cabinet H7420 no. 2 to +5 V tabs PT5-U, PT5-L, PT6-U and PT6-L are to be 14 AWG twisted-pair.

   b. All remote sense lines to be 18 AWG twisted-pair.

      Color Code as follows.

      Black = GND
      Red = +5
      Green = 2.0
      Blue = 5.2

9. "CT" represents "Control Tabs." Signals power warn and crobar are generated from 863 power control and terminate at CT2 and CT4, respectively.

   Etch from "CT" tabs to pins.

   Power Warn - CT4 to A04J1
   Crobar - CT2 to A06U2, B06S1, C0201, C0301, and F01U2

CHAPTER 11
REPORTING PROCEDURES

11.1 INTRODUCTION

The job of installation is not done until the paperwork is complete. The reports generated form an important part of the customer history file, and the feedback to regional and corporate quality control is essential to maintaining a check on the quality of installation and pinpointing problem areas when they arise.

11.2 LARS REPORT FORM

An important tool in the reporting process is the LARS form. This is the primary method of reporting and cannot be substituted by any other form. However, in some instances another installation feedback form may be necessary.

Accuracy is essential when writing LARS forms which are used to gather data for statistics. Therefore, the installer should be familiar with the LARS manual (EK-LARS-FS-00X). This manual has a section specifically on installation and how to apply the various codes not usually used during normal PM or on fault-finding calls. Several examples are included for clarification.

Figure 11-1 is a sample LARS form used on a typical DECSYSTEM-20 installation. To create a valid LARS data base for statistical analysis the following rules should be applied when filling in blanks.

1. Assigned Person – The assigned person should use all necessary installation codes and complete the material and comment section.

   An unassigned person who is plainly assisting on the same device should duplicate the assigned person's coding except for the MATERIALS USED section which should be left blank. "Assisting" should be written in the COMMENTS section. However, an unassigned person working on a separate device is responsibile for reporting this activity.

2. Product Line – There are four LCG product lines and the appropriate designation should be used for a particular system.

   a. PL66 – Commercial System Group
   b. PL67 – Education Systems Group
   c. PL73 – Federal Systems Group (Government/Scientific)
   d. PL74 – Engineering Systems Group

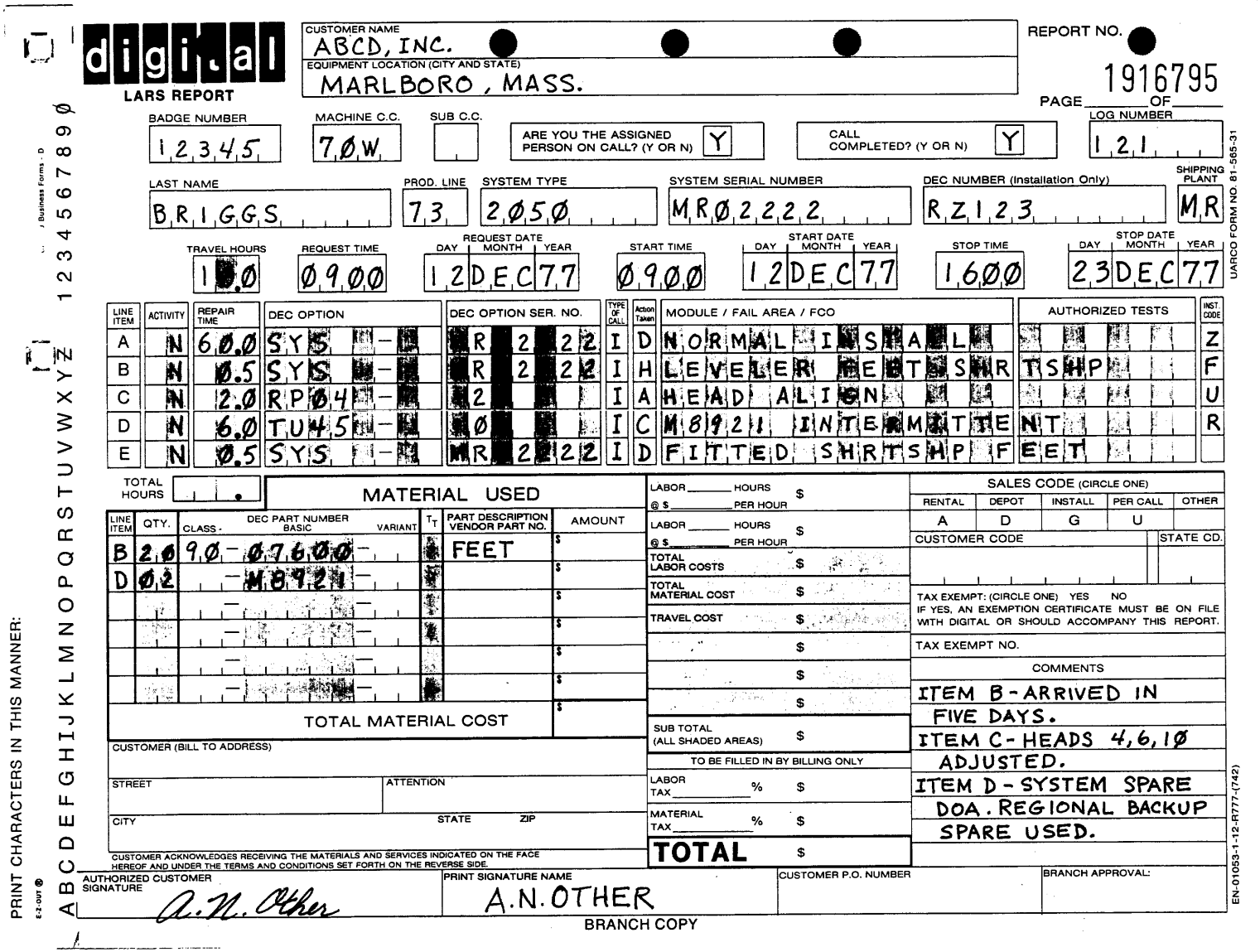
3. System Type

   2040 – KL-based DECSYSTEM-20 without cache
   2050 – KL-based DECSYSTEM-20 with cache

   At this time, there are no other valid entries for system type.

4. System Serial Number – Ensure that the system serial number entered is identical to the CPU serial number.

5. DEC Number – This should always be quoted for installations and can be located on the system keysheet or from the account manager/salesperson.



digital

LARS REPORT

CUSTOMER NAME: ABCD, INC.

EQUIPMENT LOCATION (CITY AND STATE): MARLBORO, MASS.

REPORT NO. 1916795

PAGE ____ OF ____

BADGE NUMBER: 12345 | MACHINE C.C.: 70W | SUB C.C.: | ARE YOU THE ASSIGNED PERSON ON CALL? (Y OR N): Y | CALL COMPLETED? (Y OR N): Y | LOG NUMBER: 121

LAST NAME	PROD. LINE	SYSTEM TYPE	SYSTEM SERIAL NUMBER	DEC NUMBER (Installation Only)	SHIPPING PLANT
BRIGGS	73	2050	MR02222	RZ123	MR

TRAVEL HOURS	REQUEST TIME	REQUEST DATE (DAY / MONTH / YEAR)	START TIME	START DATE (DAY / MONTH / YEAR)	STOP TIME	STOP DATE (DAY / MONTH / YEAR)
1.0	0900	12 DEC 77	0900	12 DEC 77	1600	23 DEC 77

LINE ITEM	ACTIVITY	REPAIR TIME	DEC OPTION	DEC OPTION SER. NO.	TYPE OF CALL	Action Taken	MODULE / FAIL AREA / FCO	AUTHORIZED TESTS	INST CODE
A	N	6.0	SYS	MR222	I	D	NORMAL INSTALL		Z
B	N	0.5	SYS	MR222	I	H	LEVELER REPLACEMENT	TSHP	F
C	N	2.0	RP04	2	I	A	HEAD ALIGN		U
D	N	6.0	TU45	0	I	C	M8921 INTERMITTENT		R
E	N	0.5	SYS	MR222	I	D	FITTED SHRTSHP FEET		

TOTAL HOURS: .

MATERIAL USED

LINE ITEM	QTY.	DEC PART NUMBER CLASS	BASIC	VARIANT	T_T	PART DESCRIPTION VENDOR PART NO.	AMOUNT
B	20	90	07600			FEET	$
D	02		M8921				$
							$
							$
							$
							$
TOTAL MATERIAL COST							$

CUSTOMER (BILL TO ADDRESS)

STREET | ATTENTION

CITY | STATE | ZIP

CUSTOMER ACKNOWLEDGES RECEIVING THE MATERIALS AND SERVICES INDICATED ON THE FACE HEREOF AND UNDER THE TERMS AND CONDITIONS SET FORTH ON THE REVERSE SIDE.

LABOR ____ HOURS @ $ ____ PER HOUR	$
LABOR ____ HOURS @ $ ____ PER HOUR	$
TOTAL LABOR COSTS	$
TOTAL MATERIAL COST	$
TRAVEL COST	$
	$
	$
	$
SUB TOTAL (ALL SHADED AREAS)	$
TO BE FILLED IN BY BILLING ONLY	
LABOR TAX ____ %	$
MATERIAL TAX ____ %	$
TOTAL	$

SALES CODE (CIRCLE ONE)

RENTAL	DEPOT	INSTALL	PER CALL	OTHER
A	D	G	U	

CUSTOMER CODE | STATE CD.

TAX EXEMPT: (CIRCLE ONE) YES NO
IF YES, AN EXEMPTION CERTIFICATE MUST BE ON FILE WITH DIGITAL OR SHOULD ACCOMPANY THIS REPORT.

TAX EXEMPT NO.

COMMENTS

ITEM B - ARRIVED IN FIVE DAYS.
ITEM C - HEADS 4,6,10 ADJUSTED.
ITEM D - SYSTEM SPARE DOA. REGIONAL BACKUP SPARE USED.

AUTHORIZED CUSTOMER SIGNATURE: A.N. Other | PRINT SIGNATURE NAME: A.N. OTHER | CUSTOMER P.O. NUMBER | BRANCH APPROVAL:

BRANCH COPY

UARCO FORM NO. 81-565-31

EN-01053-1-12-R777-(742)

PRINT CHARACTERS IN THIS MANNER: A B C D E F G H I J K L M N O P Q R S T U V W X Y Z 1 2 3 4 5 6 7 8 9 0

Figure 11-1 Sample LARS Report Form

6. Activity Codes

   NORAM – The new system installation code N should be used from the start of installation until completion of all DIGITAL standard diagnostics (i.e., completion of Chapter 8 of this manual). All activity for the next 90 days, including the hardware and software acceptance periods, shall be booked under code W.

   Other Areas – If a day 1 contract after acceptance exists then the new system installation code (N) should be used from delivery of the system until customer acceptance.

   Add-Ons – An add-on should be booked to code W from the start of installation until customer acceptance.

7. DEC Option – Errors are frequently made in the coding of KL10 mainframes and options, and of electro-mechanical peripherals. Correct coding is as follows.

   KL10 Mainframes and Options
   Service activities on all KL-based mainframes should be coded. This may be confusing since each mainframe also contains some "internal" options. The following "internal" options should be coded as separate options.

   MA20/MB20 and any future internal memory
   RH20
   DIA20
   DTE20
   DMA20
   LP20
   CD20
   DC20

   There is no KL20.

   Electro-Mechanical Options
   Use the complete option designation contained on the DEC serial number tag. For example, LP10-FA instead of LP10, CR10-DA instead of CR10.

   Ensure that the MODULE/FAIL AREA/FCO field is filled out for every entry. Include module or subassembly part numbers; "PM" if that is what was done; indicate what adjustment was made; "not found" if that is what happened. There are sixteen spares in this entry.

8. Type of Call – Installation code I should be used for all hardware installation.

9. MODULE/FAIL AREA/FCO – This area should contain pertinent data or comments to complement the action code and installation code. If additional comment is necessary then the COMMENTS section of the LARS form may be used. However, the primary information area should be the MODULE/FAIL AREA/FCO portion.

11.3 DECSYSTEM-20 INSTALLATION REPORT

The quality assurance group within LCG Corporate Support will selectively include this form with some system shipments. Its purpose is to gain complete installation profiles on one summary sheet and to receive written feedback on the appended device sheets. If such a form is received it should be completed and returned, in the preaddressed envelope provided, to LCG Corporate Quality Assurance.

The report is preceded by some instructions on how to fill out the sections which are not self-explanatory.

11.4 DAILY LOG

To assist in the detailed completion of the above forms, a daily installation activity log should be maintained by the installation supervisor/engineer. If several people are involved in the installation, their daily activity should be noted by the responsible installation engineer to ensure that all work is logged.

11.5 LCG INSTALLATION WARRANTY ACTIVITY SUMMARY FORMS

The following descriptions outline the details to be completed in each section of the installation warranty activity form. Refer to Figure 11-2 which is a sample of this form.

1. Section 1

   a. Customer – This is the customer name, which is used to reference the system.

   b. System Serial No. – The serial number of the CPU of the system, for example, MR02105.

   c. Branch – The branch responsible for the system.

   d. Cost Center – This is the cost center of the branch responsible for the system, for example, 7A3.

   e. MLP of System – This is the Maynard list price in dollars of the system being installed. In the case of an add-on the MLP of the add-on should be put in this space.

   f. Product Line (top right-hand corner) – This is the LCG product line which has shipped the system. The four product lines are as follows.

      Commercial Systems Group – Product Line 66
      Education Systems Group – Product Line 67
      Federal Systems Group – Product Line 73 (Government/Scientific)
      Engineering Systems Group – Product Line 74

2. Section 2

   a. Delivery of System – The day, month, and year of the actual physical delivery of the equipment to the site whether the site was ready or not. The DEC standard for writing dates is: 15 Oct 76.

   b. Hardware Acceptance – The day, month, and year of the date the system passed the DEC specified hardware acceptance, i.e., before handing over for software installation or before any other customer, or government hardware/software acceptance tests.

   c. Date of Contract – The first day on which the system or add-on equipment is to be covered by DEC field service maintenance contract.

3. Section 3

   a. Names of Engineers, Badge No., and Cost Center – This information is required on all the engineers who have ever been concerned with the new system or add-on equipment either in pre-sales visits to the customer, time spent with salespersons, site planning, installation, etc., up to the date the system or add-on was delivered.

digital **L.C.G. INSTALLATION WARRANTY COSTS SUMMARY** PRODUCT LINE:-

1 CUSTOMER		SYSTEM SERIAL No.		BRANCH		COST CENTRE		MLP OF SYSTEM	

2	DAY	MONTH	YEAR		DAY	MONTH	YEAR		DAY	MONTH	YEAR
DELIVERY OF SYSTEM				HARDWARE ACCEPTANCE				DATE OF CONTRACT			

3 NAMES OF ENGINEERS	Badge No.	Cost Centre	Pre-Sales Hours	Installation Hours	Software Installation Hours	Unusual Installation Hours	Total Installation Hours
TOTALS	----	----					

GIVE REASONS FOR UNUSUAL HOURS	
4 LIST OPTIONS DELIVERED WITH SERIAL Nos.	
5 MISSING COSMETICS	
MISSING OPTIONS	
MISSING C.S.S. OPTIONS	
MISSING COMMS OPTIONS	
6 PHYSICAL CONDITION OF SYSTEM Brief Summary	
7 SPARES AVAILABILITY SITE / BRANCH	
8 CONDITION OF SITE A) PHYSICAL / B) ELECTRICAL / C) ENVIRONMENTAL	

9 INSTALLATION FAULTS	OPTION	COMPONENT OR MODULE	LOCATION	PART No.

Figure 11-2 LCG Installation Warranty Costs Summary Form
(Sample Only)

b. Pre-Sales Hours – Any time spent concerned with the delivery of the installation of the new equipment before the actual delivery of that equipment.

c. Installation Hours – Time spent by the engineers from the date of delivery until the date of hardware acceptance.

d. Software Installation Hours – Time spent on site by the engineers during the installation of software, i.e., from the date of hardware acceptance until the system is taken over by the customer. This means to the date of contract or until the date of beginning a customer or government prolonged acceptance test with the system being used normally by the customer.

e. Unusual Installation Hours – This is the period after the completion of software installation during which there may be a customer or government acceptance period, or a reluctance on the part of the customer to sign the field service contract for some reason.

When any figures are entered in the Unusual Installation Hours column, a brief note on the reasons why it was necessary to record for unusual hours should be entered; for example, "System subject to CCA acceptance trial."

4. Section 4

List Options Delivered with Serial Nos. – This section provides a record of the equipment on site; it also serves as a check on the LCG equipment data base.

5. Section 5

List any missing items under the appropriate headings. Missing cosmetic items holding up the acceptance of the system are to be noted in this section.

6. Section 6

Physical Condition of System – A very brief note on the physical condition of the system paying particular attention to damage rather than the expected good condition; for example, CPU door bent in transit, or door paint scratched. In the event that there was no damage, state "No damage."

7. Section 7

a. Spares – A brief statement, as appropriate, describing the availability of spares at the time of installation.

b. Site – A rough estimate of the percentage of site spares that were available on the day of installation of the system. Note any major omissions, for example, "80% site spares only available, LP20 and CR20 spares completely missing."

Note that there is a site kit for the DECSYSTEM-20 which consists mainly of fans and filters, etc.

c. Branch – Particularly in the case of DECSYSTEM-20, the branch kit is the major source of spares. Later versions of DECsystem-10 will have branch-based rather than site-based spares. In this case make a short statement of the spares available at branch, for example, "only 90% KL10E modules available, no CD20 spares arrived," etc.

8. Section 8

   Condition of Site – A brief statement outlining the readiness of the three major site parame ters; i.e., physical condition and electrical and environmental status.

9. Section 9

   Installation Faults – Complete this section under the four columns and add extra sheets if necessary. Components or modules which were "dead-on-arrival" should be marked with DOA. This information provides valuable feedback for production and quality control.

APPENDIX A
INSTALLATION PLANNING SHEET

INSTALLATION PLANNING SHEET

Customer: _____

Salesperson: _____

Installation Supervisor: _____

Installation Team: _____

Team Leader: _____

Working Hrs/Day: _____

Customer Contact: _____

Site Phone: _____

Software Specialist: _____

Customer Acceptance Criteria: (standard) (special) _____

_____

_____

_____

_____

Equipment Being Installed: _____

_____

_____

_____

_____

_____

Person Responsible to Unload System and Place in Computer Room: _____

_____

_____

_____

APPENDIX B
SAMPLE DIAGNOSTICS

B.1 11/40 FRONT END DIAGNOSTICS

B.1.1 RXDP

```
DZQUJ-C 21-JUL-76 RXDP - XXDP RX11/RX01 MONITOR 28K
RESTART ADDR:152254
BOOTED VIA UNIT#:  0
TO ABORT THE FOLLOWING HELP MESSAGE TYPE CTRL C (^C)

TYPE:
F<CR> TO SET CONSOLE FILL COUNT
D<CR> FOR DIRECTORY ON CONSOLE, OR
D/F<CR> FOR SHORT DIRECTORY ON CONSOLE, OR
D/L<CR> FOR DIRECTORY ON LINE PRINTER, OR
D/L/F<CR> FOR SHORT DIRECTORY ON LINE PRINTER,
R COPY<CR> TO RUN COPY PROGRAM,
R FILENAME<CR> TO RUN ANY OTHER PROGRAM.
L FILENAME<CR> TO LOAD A PROGRAM ONLY
S<CR> TO START THE PROGRAM JUST LOADED,
S ADDR<CR> TO START THE PROGRAM AT SPECIFIC ADDRESS
C FILENAME<CR> TO RUN A CHAIN,
C FILENAME/QV<CR> TO RUN A CHAIN IN QUICK VERIFY MODE.
REFER TO XXDP USER MANUAL MD-11-DZQXA FOR ADDITIONAL HELP.
.D/F

000001 RXDP   .BIN
000002 UPD2   .BIN
000003 COPY   .BIN
000004 XTECO  .BIN
000005 YPTCBO.BIN
000006 ZQMCCO.BIC
000007 ZDLCAO.BIC
000010 ZKWAEO.BIC
000011 ZTCBCO.BIC
000012 BQEABO.BIC
000013 ZBMDHO.BIC
000014 DFQAAC.BIN
.
```

B.1.2 11/40 CPU

```
 R BQEABO

DBQEA-B   KD11-A DIAGNOSTIC   VERSION 001

PDP11/40 INTERNAL OPTIONS FOUND

KW11-L
!
PASCNT = 000001     ERRCNT = 000000

PASCNT = 000002     ERRCNT = 000000
```

B.1.3 11/40 Memory

```
NOTE: SET SW12=1 DISABLE MEMORY MANAGEMENT

 R ZQMCC0

MAINDEC-11-DZQMC-C

MEMORY MAP:
FROM    000000 TO    157777

PARITY MEMORY MAP:
CORE PARITY REGISTER AT 172100 CONTROLS
FROM    000000 TO    157777

PROGRAM RELOCATED TO 120000
PROGRAM RELOCATED TO 000000

END PASS #      1
```

B.1.4 KW11

```
.R ZKWAE0


MD-11-DZKWA-E LINE FREQUENCY CLOCK TEST

END PASS #      1
END PASS #      2


    note: reload rxdp
```

B.1.5 BM873

```
 R ZBMDHO

MAINDEC-11-DZBMDH
DEVICE VERSION
BM873-Yh

*,A,B,C,D,F,G,H ONLY.
MAINDEC-11-DZBMDH
DEVICE VERSION
BM873-YH

PROGRAM NO. (1,2,3,4)   1

END PASS BM873-YH
```

B.1.6 RX01

```
.R ZRXAE0

MAINDEC-11-DZRXA-E
RXCS = 177170 RXDB = 177172 INT VECTOR = 264
CAUTION - IF YOU DESIRE TO TEST UNIT 0
REPLACE LOAD MEDIUM WITH A SCRATCH DISKETTE
THEN PRESS CONTINUE
DRIVE(S)  UNIT 0        P= 0   T= 0   S= 0

D
```

B.1.7 DC20 Data Line Control

```
.R ZDHNB0

MAINDEC-11-DZDHN-B DH11 DATA RELIABILITY TEST

TYPE NO. OF ADDRESSES (OCTAL) BETWEEN VECTORS (10 OR 20)
20

TYPE SCR ADDRESS FOR FIRST DH11
160020

TYPE VECTOR ADDRESS FOR FIRST DH11
330

TYPE DH11 DEVICE SELECTION PARAMETER
1

TYPE LINE SELECTION PARAMETER
000002

TESTING DH11 #00

TESTING LINE #01

DH #00 STATISTICS:
LINE #   RTOTAL   XTOTAL   DATERR   PARERR   FRMERR   OVRERR

000001     1824     1824        0        0        0        0


END PASS #      1
TESTING DH11 #00

TESTING LINE #01
```

NOTE
This test is for one DH11 only.

B.1.8 DC20 Modem Control

```
.R ZDHKC1

DZDHK-C      ------MODEM CONTROL DIAGNOSTIC------
VECTOR ADDRESS-320
CONTROL REGISTER ADDRESS-770500
LINE SELECT PARAMETER -000001
TEST-00


16 LINE SCANNER TEST

NOTE: TEST SELECTION FOR 1 LINE ONLY
        CONSOLE BEEP = END PASS
        RELOAD RXDP
```

B.1.9 Line Printer

```
NOTE: SW0=0 LP20 ONLY
      SW0=1 LP20 AND PRINTER


MAINDEC-10-DXLPB  REV. C
IF LP05 OR LP07 SET TO 6 LINES PER INCH
LP20 #1 IS AVAILABLE
LP20 #2 IS AVAILABLE
TO SELECT AN LP20 TYPE 1<CR> OR 2<CR> OR <CR>
1
TESTING LP20 #1
FOR THE NEXT QUESTIONS, ANSWER "Y" OR "N"...
LOWER CASE:  N
LP14 PRINTER: Y
LP07 CHAIN PRINTER:  N
END PASS #     1
```

B.1.10 Disk (DRJGAO)

```
R ZRJGAO

RP04/5/6 DISKLESS CONTROLLER TEST - PART I - DZRJG-A
REVISION DATE: 21-MAR-76

ALL DCL'S UNDER TEST MUST BE LOCKED ON CORRECT PORT
IF CHANGES ARE REQUIRED ON PORT SWITCH THEN
A CYCLE UP SEQUENCE IS REQUIRED FOR STROBING
THE PORT SELECT FLOP

ALL DCL'S NOT UNDER TEST MUST BE SWITCHED OFF
OR LOCKED ON THE OTHER PORT


LOOKING AT RHAS - DRIVES ASSUMED PRESENT

****************************************
   THIS MUST BE VERIFIED BY OPERATOR !!
****************************************
     1
TESTING DRIVE NUMBER      1
SERIAL NO. = 003004
DRIVE TYPE = 024020
DRIVE IS AN RP04

IF DRIVE CONNECTED "STAND BY" LAMP SHOULD BE LIT ON DRIVE NO
TOTAL ERRORS ON THIS PASS ON  UNIT NO.       1=       0
END PASS #      1

LOOKING AT RHAS - DRIVES ASSUMED PRESENT

**************************


NOTE: RH11 CONNECTED TO DRIVE 1 IN THIS SAMPLE
```

B.1.11 Disk (ZRJHAO)

```
 R ZRJHAO

RP04/5/6 DISKLESS CONTROLLER TEST - PART II  - DZRJH-A
REVISION DATE: 21-MAR-76

ALL DCL'S UNDER TEST MUST BE LOCKED ON CORRECT PORT
IF CHANGES ARE REQUIRED ON PORT SWITCH, A CYCLE UP
SEQUENCE IS REQUIRED FOR STROBING THE PORT SELECT FLOP

ALL DCL'S NOT UNDER TEST MUST BE SWITCHED OFF

**************************************
IF THIS IS NOT DONE, ERRORS WILL RESULT ON
'NED' TESTS (T21 & T36)
**************************************

LOOKING AT RHAS - DRIVES PRESENT
      1
TESTING DRIVE NUMBER      1
SERIAL NO. = 003004
DRIVE TYPE = 024020
DRIVE IS AN RP04
^
TOTAL ERRORS ON THIS PASS ON  UNIT NO.      1=       0
END PASS #  1


NOTE: RH11 CONNECTED TO DRIVE 1 IN THIS SAMPLE
```

B.1.12 Disk (ZRJJAO)

```
R ZRJJAO

RP04/5/6 FUNCTIONAL CONTROLLER TEST, PART II  - DZRJJ-A
REVISION 21-MAR-76

ALL DCL'S UNDER TEST MUST BE LOCKED ON CORRECT PORT
IF CHANGES ARE REQUIRED ON PORT SWITCH, A CYCLE UP
SEQUENCE IS REQUIRED FOR STROBING THE PORT SELECT FLOP

ALL DCL'S NOT UNDER TEST MUST BE SWITCHED OFF
OR LOCKED ON THE OTHER PO

LOOKING AT RHAS - DRIVES PRESENT
     1
TESTING DRIVE NUMBER      1
SERIAL NO. = 003004
DRIVE TYPE = 024020
DRIVE IS AN RP04

DRIVE IS OFFLINE - MOL IS LOW
HIT START ON DRIVE TO GET IT ON LINE
PROGRAM WILL HANG TESTING MOL TILL MOL IS HIGH
GOOD - MOL IS HIGH, PROGRAM WILL BE EXECUTED
TOTAL ERRORS ON THIS PASS ON  UNIT NO.      1 =      0
END PASS #      1


NOTE: RH11 CONNECTED TO DRIVE 1 IN THIS SAMPLE
```

B.1.13 Disk (ZRJBA1)

```
.R ZRJBA1


MAINDEC-11-DZRJB-A
RP04/5/6 FORMATTER PROGRAM


UNIT STATUS

 0      NOT PRESENT
 1      ONLINE  RP04
 2      NOT PRESENT
 3      NOT PRESENT
 4      NOT PRESENT
 5      NOT PRESENT
 6      NOT PRESENT
 7      NOT PRESENT


PROGRAM MODE (C OR F): F
FORMAT & VERIFY

OPERATE IN 22 SECTOR MODE (Y OR N) ? Y
OPERATION WILL BE IN 22 SECTOR (16 BIT) MODE

DRIVE: 1
ENTER ADDRESS LIMITS:
START CYL       0 /
START TRK       0 /
END CYL     410 /
END TRK      18 /
SELECT DATA PATTERN
 (0) ZERO'S
 (1) ONE'S
 (2) WORST CASE:
WORST CASE

STARTING FORMAT ON DRIVE 1

DATA ERROR DURING WRITE CHECK
DRIVE   ERR PC CYLINDER TRACK   SECTOR
000001  004436     121       18        5
  RPCS1   RPCS2   RPDS1   RPER1   RPER2   RPER3   RPEC1   RPEC2
  144252  040301  150700  100000  000000  000000  003000  002000
RPWC    RPBA    RPDA    RPAS    RPLA    RPDB    RPMR    RPDT
167441  032512  011006  000002  001740  164555  000400  024020
  RPSN    RPOF    RPCA    RPCC
  003004  110000  000171  000171
```

```
DATA ERROR DURING WRITE CHECK
DRIVE    ERR PC CYLINDER TRACK    SECTOR
000001   004436      137       15       13
  RPCS1    RPCS2    RPDS1    RPER1    RPER2    RPER3    RPEC1    RPEC2
  144252   040301   150700   100000   000000   000000   005635   002000
RPWC     RPBA     RPDA     RPAS     RPLA     RPDB     RPMR     RPDT
173633   043076   007416   000002   000160   165455   000400   024020
  RPSN     RPOF     RPCA     RPCC
  003004   110000   000211   000211

DATA ERROR DURING WRITE CHECK
DRIVE    ERR PC CYLINDER TRACK    SECTOR
000001   004436      372       15        9
  RPCS1    RPCS2    RPDS1    RPER1    RPER2    RPER3    RPEC1    RPEC2
  144252   040301   150700   100420   000000   000000   001742   003000
RPWC     RPBA     RPDA     RPAS     RPLA     RPDB     RPMR     RPDT
171315   036242   007412   000002   002340   004564   000400   024020
  RPSN     RPOF     RPCA     RPCC
  003004   110000   000564   000564


FORMAT COMPLETE, TOTAL ERRORS DETECTED:       3

DRIVE:
```

B.1.14 Disk (ZRJAA1)

```
.R ZRJAA1


MAINDEC-11-DZRJA-A
RP04/5/6 MECHANICAL & READ-WRITE TEST



UNIT STATUS:

 0      NOT PRESENT
 1      ONLINE  RP04
 2      NOT PRESENT
 3      NOT PRESENT
 4      NOT PRESENT
 5      NOT PRESENT
 6      NOT PRESENT
 7      NOT PRESENT

DRIVE(S) TO BE TESTED 1
NO KW11-P CLOCK, TIMING TESTS WILL NOT BE PERFORMED

TESTING DRIVE 1  SERIAL NUMBER 0604


END OF PASS ON DRIVE 1    ERRORS DETECTED=000000
END OF TEST

TESTING DRIVE 1  SERIAL NUMBER 0604
```

B.1.15 SY2040

```
 R SY2040

DEC/X11.  DXQAB-K  STANDARD MONITOR
WRITE BUFFER ROTATION ENABLED. RANGE: 074000  157776
SYSTEM SIZE:   28K
NO KT11
PARITY ENABLED

TO EXERCISE LOAD MEDIUM YOU MUST CLEAR LOC 40

.MAP

KWDA0 AT 027406 STAT 041000
KWAF0 AT 030574 STAT 140000
RXAB0 AT 032270 STAT 140000
RPBE0 AT 036260 STAT 150000
DLBA0 AT 046034 STAT 140000
DTAA0 AT 052546 STAT 040020
CPCA0 AT 055630 STAT 040020
LPFA0 AT 057366 STAT 140000
BMEA0 AT 062516 STAT 040020
DMBG0 AT 064040 STAT 140000
DHAI0 AT 065112 STAT 140000
BKAA0 AT 070764 STAT 040020
BKBA0 AT 071236 STAT 040020
CDAE0 AT 071572 STAT 140000
.DES
```

NOTE
This is a sample. Select all modules available for the particular configuration.

```
.SEL KWDA0

.SEL KWAF0

.SEL DLBA0

.SEL BMEA0

.SEL DMBG0

.SEL DHAI0

.SEL BKAA0

.SEL BKBA0

.MAP
```

```
KWDA0 AT 027406 STAT 041000
KWAF0 AT 030574 STAT 140000
RXAB0 AT 032270 STAT 100000
RPBE0 AT 036260 STAT 110000
DLBA0 AT 046034 STAT 140000
DTAA0 AT 052546 STAT 000020
CPCA0 AT 055630 STAT 000020
LPFA0 AT 057366 STAT 100000
BMEA0 AT 062516 STAT 040020
DMBG0 AT 064040 STAT 140000
DHAI0 AT 065112 STAT 140000
BKAA0 AT 070764 STAT 040020
BKBA0 AT 071236 STAT 040020
CDAE0 AT 071572 STAT 100000
.RUN

.

^C

RUN SUMMARY AT RUNTIME-000:33:55

KWDA0 AT 027406 STAT 061000  PASCNT 00001.  ERRCNT 00000.
KWAF0 AT 030574 STAT 140000  PASCNT 00033.  ERRCNT 00000.
DLBA0 AT 046034 STAT 140000  PASCNT 00029.  ERRCNT 00000.
DMBG0 AT 064040 STAT 140000  PASCNT 00022.  ERRCNT 00000.
DHAI0 AT 065112 STAT 140000  PASCNT 00024.  ERRCNT 00000.
BKAA0 AT 070764 STAT 040020  PASCNT 00005.  ERRCNT 00000.
BKBA0 AT 071236 STAT 040020  PASCNT 00004.  ERRCNT 00000.
SYSTEM ERRORS:    0     POWER FAILS:    0
.
```

B.2 FLOPPY BOOT OF KLDCP

```
                    FLOPPY BOOT OF KLDCP


                DECSYSTEM DIAGNOSTIC CONSOLE
                VERSION 0.16
                SWR = 000000    DTE # 0
                CMD:
                >. RPO
                >.
```

B.3 BB. CMD

```
   RI
DECSYSTEM DIAGNOSTIC CONSOLE
VERSION 0.16
SWR = 000207    DTE # 0
CMD:
>. B
;BB.CMD, KL10B PROCESSOR DIAGNOSTIC BOOT, 6-APR-77
;PROCESSOR HARDWARE

;DTE20 INTERFACE
P DGDTE.A11
SED 2

DGDTE   DTE20 DIAGNOSTIC        VER. 1.10

THE FOLLOWING 10/11 INTERFACE(S) EXIST

DTE #0          ADDRESS 174434
TESTED DTE20 IS PRIVELEGED

ENTERING INTERRUPT TEST PASS 1 (INT 1) PC= 016042

EXITING INTERRUPT TEST PASS 1

ENTERING NPR TEST PASS 1 PC= 025336

THE PROGRAM IS ATTEMPTING AN NPR TO A NON-EXISTANT
ADDRESS. IF THE BUS TIMEOUT LOGIC TIMEOUT AND ITS
ASSOCIATED ONE-SHOT FAIL THE PROCESSOR WILL REGRETABLY
HANG. THERE IS NO GOOD WAY TO LOOP. GOOD LUCK!!
```

```
EXIT FROM NPR TESTING PASS 1
TESTING E AND DIAGNOSTIC BUSSES
END PASS 1.
#EBOX PART 1
P DHKAA.A11
SED 1
KL-10 MODEL B CPU EBOX DIAGNOSTIC, PART 1 (DHKAA)
        VERSION: 0.1
STARTING INITIALIZATION TESTS
STARTING CLOCK TESTS
STARTING CRAM TESTS
STARTING DRAM TESTS
STARTING CONTROL LOGIC TESTS
STARTING NEXT ADDRESS TESTS
STARTING MICROCODE SUBROUTINE STACK TESTING
STARTING FM EXTENDED RAM TEST
END PASS 1.
#EBOX PART 2
P DHKAB.A11
SED 1
KL-10 MODEL B CPU EBOX DIAGNOSTIC, PART 2 (DHKAB)
        VERSION: 0.1

EBOX DIAGNOSTIC MICRO-CODE IS LOADING
STARTING DATA PATH TESTS
STARTING VMA TESTS
STARTING CONTROL LOGIC TESTS
STARTING 10-BIT ARITHMETIC TESTS
STARTING PI TESTS
END PASS 1.
#MBOX BASIC
P DHKBA.A11
SED 1
MAINDEC-10-DHKBA
BASIC MBOX DIAGNOSTIC  VER 0.2
CONSOLE SWITCHES = 000000
PROCESSOR SERIAL # 1087.

END PASS 1.
#MEM CONTROL
P DHKBB.A11
SED 1

MAINDEC-10  DHKBB
MEMORY SYSTEM DIAGNOSTIC  VER 1.1  JAB29857
SWITCHES = 000000
UCODE VERSION 156, CLOCK RATE 0, PROCESSOR ID #1087.
```

```
MEMORY REPORTED:
CONTROLLER ADDRESS   TYPE   STORAGE
                            7 6 5 4 3 2 1 0

         0           MB20   0 0 0 0 1 1 1 1
         1           MB20   0 0 0 0 1 1 1 1

***** MEM CONTROLLER 0
***** MEM CONTROLLER 1

LOGICAL MEMORY CONFIGURATION:
                    CONTROLLER
ADDRESS    SIZE    RQ0 RQ1 RQ2 RQ3   CONTYPE INT
000000     256.K   00  01  00  01      MB20   4
01 000000 3840.K NONEXISTENT MEMORY
END PASS 1.
;PAGING LOGIC
P DHKBC.A11
SED 1
PAGING HARDWARE DIAGNOSTIC
DHKBC..VER 0.1
END PASS 1.
;CACHE OPTION
P DHMCA.A11
SED 1

MAINDEC-10-DHMCA
CACHE DIAGNOSTIC VER 1.1
SWITCHES = 000000
PROC # 1087.
END PASS 1.
P DHMCB.A11
SED 1
MAINDEC-10  DHMCB
CACHE RAM BANGER DIAGNOSTIC  VER 1.1  JAB29857
SWITCHES:000000
UCODE VERSION 156, CACHE, CLOCK RATE 0, PROCESSOR ID #1087.
END PASS 1.
;CHANNELS
P DHKBD.A11
SED 1
MAINDEC-10-DHKBD
KL-10 CHANNEL CONTROL DIAGNOSTIC  VER 0.2
CONSOLE SWITCHES = 000000
PROCESSOR SERIAL # 1087.
END PASS 1.
P DGKBE.A11
SED 1
MAINDEC-10-DGKBE
CHANNEL LOOPBACK DIAGNOSTIC  VER 1.10
```

```
CONSOLE SWITCHES = 000000
PROCESSOR SERIAL # 1087.
SLOW-MODE DATA LOOPBACK O.K.
STARTING CHANNEL DATA ADDRESSING TEST
STARTING CHANNEL PARITY ADDRESSING TEST
BASIC ADDRESSING O.K.
STARTING CHANNEL BUFFER INTERACTION TEST
STARTING BUFFER PARITY INTERACTION TEST
CHANNEL BUFFER O.K.
SLOW-MODE REVERSE O.K.
STARTING FAST-MODE LOOPBACK
END PASS 1.
;METER BOARD
P DHKCA.A11
SED 1
MAINDEC-10  DHKCA
METER (M8538) DIAGNOSTIC  VER 0.1  JAB29857
SWITCHES:000000
UCODE VERSION 156, CACHE, CLOCK RATE 0, PROCESSOR ID #1087.
END PASS 1.

;PROCESSOR FUNCTIONALS
P UB.RAM
I CONFG.CCL
MEMORY CONFIGURATOR VER 0.1

LOGICAL MEMORY CONFIGURATION:
                    CONTROLLER
ADDRESS    SIZE    RQ0 RQ1 RQ2 RQ3  CONTYPE INT
000000     256.K   00  01  00  01     MB20  4
01 000000 3840.K NONEXISTENT MEMORY
SM
MZ 0,-1
P DFKAA.A10
STD 102
>. END PASS 1.
END PASS 101.
P SUBRTN.A10
P KLDDT.A10
P DFKAB.A10
STD 102
>.
PDP-10 KL10 BASIC INSTRUCTION DIAGNOSTIC [DFKAB]
SHIFT/ROTATE
VERSION 0.1, SV=0.13, CPU#=1087, MCV=157, MCO=1, HO=34, 60HZ
```

```
SWITCHES = 000000 000000
CLK SOURCE = NORMAL, CLK RATE = FULL, AC BLK 0 , CACHE: 0 1 2 3
END PASS 1.
END PASS 101.
P DFKAC.A10
STD 102
>.
PDP-10 KL10 BASIC INSTRUCTION DIAGNOSTIC [DFKAC]
MULTIPLY & DIVIDE
VERSION 0.1, SV=0.13, CPU#=1087, MCV=157, MCO=1, HO=34, 60HZ

SWITCHES = 000000 000000
CLK SOURCE = NORMAL, CLK RATE = FULL, AC BLK 0 , CACHE: 0 1 2 3
END PASS 1.
END PASS 101.
P DFKAD.A10
STD 102
>.
PDP-10 KL10 BASIC INSTRUCTION DIAGNOSTIC [DFKAD]
BYTE/BLT/JFFO/MISC
VERSION 0.1, SV=0.13, CPU#=1087, MCV=157, MCO=1, HO=34, 60HZ

SWITCHES = 000000 000000
CLK SOURCE = NORMAL, CLK RATE = FULL, AC BLK 0 , CACHE: 0 1 2 3
END PASS 1.
END PASS 101.
P DFKCA.A10
STD 102
>.
PDP-10 KL10 ADVANCED INSTRUCTION DIAGNOSTIC #1 (DFKCA)
VERSION 0.1, SV=0.13, CPU#=1087, MCV=157, MCO=1, HO=34, 60HZ

SWITCHES = 000000 000000
CLK SOURCE = NORMAL, CLK RATE = FULL, AC BLK 0 , CACHE: 0 1 2 3
END PASS 1.
END PASS 101.
P DFKBA.A10
STD 1
>.
PDP-10 KL10 BASIC INSTRUCTION RELIABILITY TEST 1 (DFKBA)
VERSION 0.1, SV=0.13, CPU#=1087, MCV=157, MCO=1, HO=34, 60HZ

SWITCHES = 000000 000000
CLK SOURCE = NORMAL, CLK RATE = FULL, AC BLK 0 , CACHE: 0 1 2 3

MEMORY MAP =
FROM      TO          SIZE/K
00000000 00777777        256
```

```
TESTING 32K
END PASS 1.
P DFKEA.A10
STD 1
>.
PDP-10 KL10 PAGING HARDWARE DIAGNOSTIC (DFKEA)
VERSION 0.1, SV=0.13, CPU#=1087, MCV=157, MCO=1, HO=34, 60HZ

SWITCHES = 000000 000000
CLK SOURCE = NORMAL, CLK RATE = FULL, AC BLK 0
END PASS 1.
P DFKEB.A10
STD 1
>.
PDP-10 KL10 MONITOR UUO DIAGNOSTIC (DFKEB)
VERSION 0.1, SV=0.13, CPU#=1087, MCV=157, MCO=1, HO=34, 60HZ

SWITCHES = 000000 000000
CLK SOURCE = NORMAL, CLK RATE = FULL, AC BLK 0 , CACHE: 0 1 2 3
END PASS 1.
P DFDTE.A10
STD 1
>.
DECSYSTEM10 KL10 DTE20 FUNCTIONAL DIAGNOSTIC (DFDTE)
VERSION 0.10, SV=0.13, CPU#=1087, MCV=157, MCO=1, HO=34, 60HZ

SWITCHES = 000000 000000
CLK SOURCE = NORMAL, CLK RATE = FULL, AC BLK 0 , CACHE: 0 1 2 3

MEMORY MAP =
FROM      TO          SIZE/K
00000000 00777777        256


TESTING DTE20 # 0
END PASS 1.
P DFKDA.A10
STD
>.
PDP-10 KL10 ARITHMETIC/RANDOM/INTERRUPT/MEMORY RELIABILITY TEST (DFKDA)
VERSION 0.2, SV=0.13, CPU#=1087, MCV=157, MCO=1, HO=34, 60HZ

SWITCHES = 000000 000000
CLK SOURCE = NORMAL, CLK RATE = FULL, AC BLK 0 , CACHE: 0 1 2 3

MEMORY MAP =
FROM      TO          SIZE/K
00000000 00777777        256

END PASS 1.
```

B.4 DGMMA

```
>. P DGMMA
DGMMA.A11   VER 2.2   10-NOV-77
>. SED
DIACON
*/H

PROGRAM SWITCHES ARE:

/FREEZE:CX,MY    WHERE X IS CONTROLLER & Y IS INTERNAL MODULE
/FREEZE:NONE     TO CLEAR C OR C & M FREEZE
/MARGINS:X       WHERE X IS DEFINED AS FOLLOWS:
                 NONE (DEFAULT)
                 ALL
                 CURRENT H,L (OR H OR L)
                 STROBE H,L (OR H OR L)
                 THRESHOLD H,L (OR H OR L)
/PATTERN:X       TO USE A SPECIFIC TEST PATTERN
/PATTERN:NONE    TO USE DEFAULT PATTERNS

/BUS:X           TO SET EXTERNAL MEMORY BUS MODE, WHERE X IS
                 NORMAL (DEFAULT) ,0 (OFF), 1, 2 OR 4
/TYPE:X          WHERE X IS ME10,MF10,MG10 OR MH10
/SEGMENT:SA,N    TO TEST 16K SEGMENTS OF EXTERNAL MEMORY, WHERE
                 SA IS THE STARTING ADDRESS & N IS THE NUMBER
                 OF 16K SEGMENTS
/SEGMENT:NONE    TO CLEAR SEGMENT TESTING

SWITCHES REMAIN IN EFFECT UNTIL CLEARED.
A SWITCH STRING ENDING WITH AN ALTMODE WILL CAUSE
THE PROGRAM TO BE STARTED.


PROGRAM SWITCHES: /MARGINS:ALL$
MAINDEC-10-DGMMA
KL-10 CORE MEMORY RELIABILITY TEST  VER 2.2
CONSOLE SWITCHES = 000002
KL10-PV PROCESSOR SERIAL # 1087.

MEMORY REPORTED:
CONTROLLER ADDRESS  TYPE  STORAGE
                          7 6 5 4 3 2 1 0

         0          MB20  0 0 0 0 1 1 1 1
         1          MB20  0 0 0 0 1 1 1 1


INTERNAL MEMORY MARGINS: ALL
END PASS 1.
^C
CMD:
>.
```

B.5 DIAGNOSTIC BOOT

```
>. BT
;BBT.CMD, KL10B DIAGNOSTIC BOOT, 20-SEP-76
P UB.RAM
I CONFG.CCL
MEMORY CONFIGURATOR VER 0.1

LOGICAL MEMORY CONFIGURATION:
                    CONTROLLER
ADDRESS   SIZE    RQ0 RQ1 RQ2 RQ3  CONTYPE INT
000000    256.K   00  01  00  01     MB20  4
01 000000 3840.K NONEXISTENT MEMORY
SM
MZ 0,-1
P SUBRTN.A10
P KLDDT.A10
STD
>.
DECSYSTEM DIAGNOSTIC SUBROUTINE'S
VERSION 0.11, SV=0.13, CPU#=1087, MCV=157, MCO=1, HO=34, 60HZ

SWITCHES = 000010 000000
CLK SOURCE = NORMAL, CLK RATE = FULL, AC BLK 0 , CACHE: 0 1 2 3

MEMORY MAP =
FROM      TO          SIZE/K
00000000 00777777        256

END PASS 1.
;END
CMD:
>.
```

B.6 DDMME

```
>. R DDMME
DDMME.A10   VER 0.1   16-JUN-75
>. STD
>.
PDP-10 BLT/MEMORY EXERCISER TEST (DDMME)
VERSION 0.1, SV=0.13, CPU#=1087, MCV=157, MC0=1, H0=34, 60HZ

SWITCHES = 000010 000000
CLK SOURCE = NORMAL, CLK RATE = FULL, AC BLK 0 , CACHE: 0 1 2 3

MEMORY MAP =
FROM      TO          SIZE/K
00000000 00777777        256

END PASS 1.
SP
>.
```

B.7 DDMMD

```
>. P DDMMD
DDMMD.A10   VER 0.2   03-MAR-77
>. SW 523
>. STD
>.
PDP-10 MEMORY DIAGNOSTIC (DDMMD)
VERSION 0.2, SV=0.13, CPU#=1087, MCV=157, MCO=1, HO=34, 60HZ

SWITCHES = 000010 000523
CLK SOURCE = NORMAL, CLK RATE = FULL, AC BLK 0 , CACHE: 0 1 2 3

MEMORY MAP =
FROM      TO          SIZE/K
00000000 00777777        256


SEGMENT TESTING ? Y OR N <CR> - N

SPECIFY MEMORY SIZE TO BE TESTED IN K, 0=ALL - 0

SPECIFY NUMBER OF MODULES, 0=ALL SAME OR 1 TO 16 - 0

SPECIFY SIZE IN K, MODULE TYPE (0 TO 17) OF EACH
MODULE SIZE, ALL - 32,ALL
MODULE TYPE, ALL - MODULE TYPE, ALL - (CR=DEFAULT)

TEST SELECTION
DATA PATTERNS - 1 TO 7, Y OR N (CR) Y

ADDRESS, Y OR N <CR> - Y
WCP - 1 TO 4, Y OR N (CR) - Y

FLOATING ONES/ZEROS, Y OR N <CR> - Y
CORE HEATING, Y OR N <CR> - N

SELECTION COMPLETED, IS IT OK, Y OR N <CR> - Y

END PASS 1
```

B.8 DFRHD

```
   >.P DFRHB
DFRHB.A10   VER 0.12   16-JAN-78
>. STD
>. MD-10-DFRHB-I RH20 LOGIC TEST
VERSION 0.12, SV=0.13, CPU#=1087, MCV=157, MCO=1, HO=34, 60HZ

SWITCHES = 000010 000000
CLK SOURCE = NORMAL, CLK RATE = FULL, AC BLK 0 , CACHE: 0 1 2 3

MEMORY MAP =
FROM     TO          SIZE/K
00000000 00777777       256


**************************************************
ALL DUAL PORTED DRIVES MUST BE LOCKED ON THE RH20 PORT!
**************************************************


LIST THE PROGRAM SWITCHES? Y OR N <CR> - N

THE FOLLOWING RH20'S ARE DETECTED:
0 (540 ) - 1 (544 )

IS THIS CPU A MODEL "B" OR MODEL "A" REV LEVEL 10 OR HIGHER? Y OR N <CR> -

TYPE RH20'S TO BE TESTED SEPARATED BY COMMAS, <CR> AT END
#0,1

TYPE DRIVE NUMBER OF NONEXISTANT DRIVE ON ALL CONTROLLERS TESTED
#7

END PASS 1.
^C
CMD:
>.
```

B.9 DFRPK

```
   P DFRPK
DFRPK.A10   VER 0.2   31-JAN-77
>. STD
>.
MD-10-DFRPK RP06-RH20 BASIC DRIVE DIAGNOSTIC
VERSION 0.2, SV=0.13, CPU#=1087, MCV=157, MCO=1, HO=34, 60HZ

SWITCHES = 000000 000000
CLK SOURCE = NORMAL, CLK RATE = FULL, AC BLK 0 , CACHE: 0 1 2 3

MEMORY MAP =
FROM      TO          SIZE/K
00000000 00777777        256


**********
CAUTION - - MOUNT SCRATCH PACK(S) BEFORE RUNNING.
THIS DIAG. WRITES THE PACK. IF AN 11-FMT SCRATCH PACK IS USED,
IT WILL HAVE TO BE REFORMATED AFTER RUNNING THIS DIAG.
**********

HEAD ALIGNMENT AND DUAL PORT TESTS DO NOT WRITE THE PACK

LIST PGM SWITCH OPTIONS ?  Y OR N <CR> - N


ALL DRIVES BEING TESTED SHOULD BE LOCKED ON PROPER PORT
WITH DEVICE SELECT PLUG INSTALLED
UNLESS INSTRUCTED OTHERWISE ...


THE FOLLOWING RH'S AND RP06'S  ARE DETECTED

RH'S     DRIVES
540
544      0


SELECT RH'S TO BE TESTED
  (540,544,550,554,560,564,570,574 OR "A" ARE LEGAL)
RH'S = 544


SELECT DRIVES (0-7 OR "A")
 ON RH-544 = 0


END PASS - 1.

THE FOLLOWING DEVICES HAVE BEEN TESTED
 DRIVE-0 RH-544  DRIVE TYPE= DUAL PORTED RP06 DRIVE SER. NO.=0205.
END PASS 1.
```

NOTE
For an RP04 use DFRPH.

B.10 DDRPI (FORMAT BEFORE ACCEPT)

```
CMD:
>. STM
>. DDRPI - RH10/RH20 - RP04/05/06 - RELIABILITY TEST
VERSION 0.5, SV=0.13, CPU#=1087, MCV=157, MC0=1, H0=34, 60HZ

SWITCHES = 000010 000000
CLK SOURCE = NORMAL, CLK RATE = FULL, AC BLK 0 , CACHE: 0 1 2 3

MEMORY MAP =
FROM      TO          SIZE/K
00000000 00777777        256


LIST THE PGM SWITCH OPTIONS? Y OR N <CR> - N

RH20 MASSBUS CONFIGURATION
MBC - DR - STATUS OF UNIT FOUND

544 - 10 - RP06 DRIVE SER. NO.=0205.(ONLINE), WRT ENABLED, DUAL PORT
********** 10 FORMATTED BY DRIVE SER. NO.=0000.

*****
DRIVES'S <TYPE> AVAILABLE = 10<6>
WHAT DRIVE(S) TO BE TESTED (00 TO 77, ALL, H=HELP) ?
#10


WHAT TEST ? - FORMAT


FORMAT A PACK? Y OR N <CR> - Y

THE PACK SPECIFICATION ALLOWS A TOTAL OF 20 ERRORS...
OF WHICH 5 MAY BE "HARD" ERRORS.
CYLINDER 000 SURFACE 00 CAN NOT HAVE ANY "HARD" ERRORS!


16 BIT MODE (11 FORMAT)? Y OR N <CR> - N

VERIFY AFTER FORMATTING? Y OR N <CR> - Y

PROCESS ENTIRE PACK FOR ALL SELECTED DRIVES ? Y OR N <CR> - Y

PROGRAM RUN TIME = 0:0:34        FORMATTING STARTED

PROGRAM RUN TIME = 0:9:15        OPERATION COMPLETED

PROGRAM RUN TIME = 0:9:17        VERIFICATION STARTED
```

```
*-*-*-*-* DONE INTERRUPT          PGM SW = 000010 000000
PROGRAM RUN TIME = 0:11:15
CONI-544:  EXCEP CHN-ER CNR MBCENB ATTN ATN-EN DONE PIA=4

DRAS:   200001

TEST NAME: "FORMAT" AT PC ADDRESS 33163


DRIVE #10
DISK START ADDRESS IS:  CYLINDER #261 SURFACE #11  SECTOR #00
(WHICH EQUALS LOGICAL BLOCK #67440.)  BUFFER START ADDRESS = 112000
AND TRANSFER SIZE =  5050(8) OR 2600.(10)

PGM INTERRUPT PC WAS - 44276

DRIVE EXCEPTION ERROR ON DRIVE 544 - 0<6>
RHPTCR   544:  DRIVE=0  + BLOCK CNT=20. FNCTN+GO=73 (READ)
RHSTCR   544:  DRIVE=0  + BLOCK CNT=20. FNCTN+GO=73 (READ)
DRCR     544-0:  DRAES TRA DVA FNCTN(30-34)=RDH+D GO-BIT=0
DRSR     544-0:  DRAES TRA PARBIT ERR MOL PGM DPR DRY VV
DRER1    544-0:  DRAES TRA PARBIT DCK ECH
DRER2    544: 140600 200000
DRER3    544: 150600 200000
DRDA     544-0:  DRAES TRA SURFACE=11 SECTOR=10
DRDCY    544-0:  DRAES TRA PARBIT DESIRED CYLINDER=261
DRCCY    544-0:  DRAES TRA PARBIT CURRENT CYLINDER=261
DROFST   544-0:  DRAES TRA SGNCHG OFFSET=0.
DRECPS   544-0:  DRAES TRA ECC POSITION=2814.
DRECPT   544-0:  DRAES TRA ECC PATTERN=1341
CHAN-1 LOGOUT DATA
LOC
004     ICW: 200000 103074
005     SW1:  LOGOUT SBUSEN NWCSZ LNG-WC CLP POINTS TO: 103103
006     LAST UPDATED CCW: 440340 113620     +WC=1038.  ADR=113620


CCW'S   CHAN-1
 LOC       +WC        ADR        MISC.
 ---       ---        ---        -----
103102    003636     00112000     OPDATA
103103    001212     00115636     OPDATA LSTXFR
```

```
ECC FAULT: DCK =1, ECI =0, POS =NON-0 & ECH =1
POSITION COUNT INCORRECT FOR ECH =1  COUNT MUST BE GREATER THAN 4639.!!

COMMAND ERROR RECOVERY @ ADDR 77452 IS
READ HEADERS & DATA ISSUED TO DRIVE #10
PATTERN IS "ANY" STARTING @ DISK BLK #67440.
(CYL=261, SUR=11, SECT=0)
TRANSFER SIZE = 5050 AT PGM PC #33745

RECOVERY WAS UN-SUCCESSFUL FOR THIS OPERATION ON DRIVE 544 - 0<6>
==========================================

*-*-*-*-* DONE INTERRUPT          PGM SW = 000010 000000
PROGRAM RUN TIME = 0:13:56
CONI-544:  EXCEP CHN-ER CNR MBCENB ATTN ATN-EN DONE PIA=4

DRAS:   200001

TEST NAME: "FORMAT" AT PC ADDRESS 33163


DRIVE #10
DISK START ADDRESS IS:  CYLINDER #456 SURFACE #04  SECTOR #00
(WHICH EQUALS LOGICAL BLOCK #114840.)  BUFFER START ADDRESS = 112000
AND TRANSFER SIZE =  5050(8) OR 2600.(10)

PGM INTERRUPT PC WAS - 44106

DRIVE EXCEPTION ERROR ON DRIVE 544 - 0<6>
RHPTCR  544:  DRIVE=0  + BLOCK CNT=20. FNCTN+GO=73 (READ)
RHSTCR  544:  DRIVE=0  + BLOCK CNT=20. FNCTN+GO=73 (READ)
DRCR    544-0:  DRAES TRA DVA FNCTN(30-34)=RDH+D GO-BIT=0
DRSR    544-0:  DRAES TRA PARBIT ERR MOL PGM DPR DRY VV
DRER1   544-0:  DRAES TRA DCK
DRER2   544: 140600 200000
DRER3   544: 150600 200000
DRDA    544-0:  DRAES TRA SURFACE=4 SECTOR=12
DRDCY   544-0:  DRAES TRA DESIRED CYLINDER=456
DRCCY   544-0:  DRAES TRA CURRENT CYLINDER=456
DROFST  544-0:  DRAES TRA SGNCHG OFFSET=0.
DRECPS  544-0:  DRAES TRA PARBIT ECC POSITION=1695.
DRECPT  544-0:  DRAES TRA PARBIT ECC PATTERN=2400
CHAN-1 LOGOUT DATA
LOC
004    ICW: 200000 103074
005    SW1:  LOGOUT SBUSEN NWCSZ LNG-WC CLP POINTS TO: 103105
006    LAST UPDATED CCW: 424240 114424    +WC=650.  ADR=114424
```

```
CCW'S   CHAN-1
 LOC      +WC        ADR        MISC.
 ----     ----       ----       -------
103104    003636     00112000    OPDATA
103105    001212     00115636    OPDATA LSTXFR


COMMAND ERROR RECOVERY @ ADDR 77426 IS
READ HEADERS & DATA ISSUED TO DRIVE #10
PATTERN IS "ANY" STARTING @ DISK BLK #114840.
(CYL=456, SUR=4, SECT=0)
TRANSFER SIZE = 5050 AT PGM PC #33745


PROGRAM RUN TIME = 0:15:3
DRIVE 544 - 0<6> CYL# 456 SURF# 04  SECT# 00    LOG BLK# 114840.
RECOVERED FROM A READ HEADERS & DATA ON RETRY #1.
-------------------------


==========================================================


*-*-*-*-* DONE INTERRUPT          PGM SW = 000010 000000
PROGRAM RUN TIME = 0:20:33
CONI-544:  EXCEP CHN-ER CNR MBCENB ATTN ATN-EN DONE PIA=4

DRAS:   200001

TEST NAME: "FORMAT" AT PC ADDRESS 33163


DRIVE #10
DISK START ADDRESS IS:  CYLINDER #1442 SURFACE #11  SECTOR #00
(WHICH EQUALS LOGICAL BLOCK #304940.)  BUFFER START ADDRESS = 112000
AND TRANSFER SIZE =  5050(8) OR 2600.(10)

PGM INTERRUPT PC WAS - 44135
```

```
DRIVE EXCEPTION ERROR ON DRIVE 544 - 0<6>
RHPTCR  544:  DRIVE=0  + BLOCK CNT=20. FNCTN+GO=73 (READ)
RHSTCR  544:  DRIVE=0  + BLOCK CNT=20. FNCTN+GO=73 (READ)
DRCR    544-0:  DRAES TRA DVA FNCTN(30-34)=RDH+D GO-BIT=0
DRSR    544-0:  DRAES TRA PARBIT ERR MOL PGM DPR DRY VV
DRER1   544-0:  DRAES TRA DCK
DRER2   544: 140600 200000
DRER3   544: 150600 200000
DRDA    544-0:  DRAES TRA SURFACE=11 SECTOR=16
DRDCY   544-0:  DRAES TRA PARBIT DESIRED CYLINDER=1442
DRCCY   544-0:  DRAES TRA PARBIT CURRENT CYLINDER=1442
DROFST  544-0:  DRAES TRA SGNCHG OFFSET=0.
DRECPS  544-0:  DRAES TRA ECC POSITION=314.
DRECPT  544-0:  DRAES TRA PARBIT ECC PATTERN=2400
CHAN-1 LOGOUT DATA
LOC
004     ICW: 200000 103074
005     SW1:  LOGOUT SBUSEN NWCSZ LNG-WC CLP POINTS TO: 103075
006     LAST UPDATED CCW: 404040 115434    +WC=130.  ADR=115434


CCW'S   CHAN-1
 LOC       +WC        ADR        MISC.
 ---       ---        ---        -----
103107    000000     00103074   JUMP-WD
103074    003636     00112000    OPDATA
103075    001212     00115636    OPDATA LSTXFR


COMMAND ERROR RECOVERY @ ADDR 77440 IS
READ HEADERS & DATA ISSUED TO DRIVE #10
PATTERN IS "ANY" STARTING @ DISK BLK #304940.
(CYL=1442, SUR=11, SECT=0)
TRANSFER SIZE = 5050 AT PGM PC #33745


PROGRAM RUN TIME = 0:21:41
DRIVE 544 - 0<6> CYL# 1442 SURF# 11  SECT# 00    LOG BLK# 304940.
RECOVERED FROM A READ HEADERS & DATA ON RETRY #1.
--------------------


==========================================


PROGRAM RUN TIME = 0:21:58      OPERATION COMPLETED

WHAT TEST ? -
```

```
                C
CMD:
>. SP
>. STM
>. DDRPI - RH10/RH20 - RP04/05/06 - RELIABILITY TEST
VERSION 0.5, SV=0.13, CPU#=1087, MCV=157, MCO=1, HO=34, 60HZ

SWITCHES = 000010 000000
CLK SOURCE = NORMAL, CLK RATE = FULL, AC BLK 0 , CACHE: 0 1 2 3

MEMORY MAP =
FROM     TO          SIZE/K
00000000 00777777        256


LIST THE PGM SWITCH OPTIONS? Y OR N <CR> - N

RH20 MASSBUS CONFIGURATION
MBC - DR - STATUS OF UNIT FOUND

544 - 10 - RP06 DRIVE SER. NO.=0205.(ONLINE), WRT ENABLED, DUAL PORT
********** 10 FORMATTED BY DRIVE SER. NO.=0205.

*****
DRIVES'S <TYPE> AVAILABLE = 10<6>
WHAT DRIVE(S) TO BE TESTED (00 TO 77, ALL, H=HELP) ?
#10


WHAT TEST ? - ACCEPT


PROGRAM RUN TIME = 0:0:18        STARTING PASS #1. ***


PROGRAM RUN TIME = 0:0:18        SEKTST

* TRACE * @ SEKT1 - RECAL/SEEK MAXCYL
* TRACE * @ SEKT2 - SEEK 000/128.
* TRACE * @ SEKT3 - 1 CYL SEEKS
* TRACE * @ SEKT4 - INCREMENTAL SEEKS
>.
* TRACE * @ SEKT5 - RANDOM SEEKS
* TRACE * @ SEKT6 - SERVO NOISE
* TRACE * @ SEKT7 - CYLINDER DIFFERENCE TEST

PROGRAM RUN TIME = 0:7:46        RONLY
```

```
*-*-*-*-* DONE INTERRUPT          PGM SW = 000010 000000
PROGRAM RUN TIME = 0:9:16
CONI-544:  EXCEP CHN-ER CNR MBCENB ATTN ATN-EN DONE PIA=4

DRAS:   200001

TEST NAME: "ACCEPT" RUNNING "RONLY" AT PC ADDRESS 31206


DRIVE #10
DISK START ADDRESS IS:  CYLINDER #261 SURFACE #10  SECTOR #00
(WHICH EQUALS LOGICAL BLOCK #67420.)  BUFFER START ADDRESS = 104000
AND TRANSFER SIZE =  12000(8) OR 5120.(10)

PGM INTERRUPT PC WAS - 44106

DRIVE EXCEPTION ERROR ON DRIVE 544 - 0<6>
RHPTCR  544:  DRIVE=0  + BLOCK CNT=40. FNCTN+GO=71 (READ)
RHSTCR  544:  DRIVE=0  + BLOCK CNT=40. FNCTN+GO=71 (READ)
DRCR    544-0:  DRAES TRA PARBIT DVA FNCTN(30-34)=READ GO-BIT=0
DRSR    544-0:  DRAES TRA PARBIT ERR MOL PGM DPR DRY VV
DRER1   544-0:  DRAES TRA PARBIT DCK ECH
DRER2   544: 140600 200000
DRER3   544: 150600 200000
DRDA    544-0:  DRAES TRA SURFACE=11 SECTOR=10
DRDCY   544-0:  DRAES TRA PARBIT DESIRED CYLINDER=261
DRCCY   544-0:  DRAES TRA PARBIT CURRENT CYLINDER=261
DROFST  544-0:  DRAES TRA SGNCHG OFFSET=0.
DRECPS  544-0:  DRAES TRA ECC POSITION=4.
DRECPT  544-0:  DRAES TRA ECC PATTERN=1341
CHAN-1 LOGOUT DATA
LOC
004    ICW: 200000 103074
005    SW1:  LOGOUT SBUSEN NWCSZ LNG-WC CLP POINTS TO: 103106
006    LAST UPDATED CCW: 414000 112600    +WC=384.  ADR=112600


CCW'S   CHAN-1
 LOC      +WC       ADR       MISC.
 ---      ---       ---       -----
103104   003600    00104000    OPDATA
103105   003600    00107600    OPDATA
103106   002400    00113400    OPDATA LSTXFR
```

```
ECC FAULT: DCK =1, ECI =0, POS =NON-0 & ECH =1
POSITION COUNT INCORRECT FOR ECH =1  COUNT MUST BE GREATER THAN 4639.!!

COMMAND ERROR RECOVERY @ ADDR 77420 IS
READ ISSUED TO DRIVE #10
PATTERN IS "ANY" STARTING @ DISK BLK #67420.
(CYL=261, SUR=10, SECT=0)
TRANSFER SIZE = 12000 AT PGM PC #31215

ATTEMPTING RECOVERY OF A 40. SECTOR TRANSFER BY INDIVIDUAL SECTORS


PROGRAM RUN TIME = 0:10:36
DRIVE 544 - 0<6> CYL# 261 SURF# 11  SECT# 07    LOG BLK# 67447.
RECOVERED FROM A READ ON RETRY #21. (USED HEADER COMPARE INHIBIT)
OFF-SETTING AT 400. MICRO - INCHES
_____________________


==========================================


*-*-*-*-* DONE INTERRUPT          PGM SW = 000010 000000
PROGRAM RUN TIME = 0:11:51
CONI-544:  EXCEP CHN-ER CNR MBCENB ATTN ATN-EN DONE PIA=4

DRAS:   200001

TEST NAME: "ACCEPT" RUNNING "RONLY" AT PC ADDRESS 31206


DRIVE #10
DISK START ADDRESS IS:  CYLINDER #456 SURFACE #04  SECTOR #00
(WHICH EQUALS LOGICAL BLOCK #114840.)  BUFFER START ADDRESS = 104000
AND TRANSFER SIZE =  12000(8) OR 5120.(10)

PGM INTERRUPT PC WAS - 47054

DRIVE EXCEPTION ERROR ON DRIVE 544 - 0<6>
RHPTCR  544:  DRIVE=0  + BLOCK CNT=40. FNCTN+GO=71 (READ)
RHSTCR  544:  DRIVE=0  + BLOCK CNT=40. FNCTN+GO=71 (READ)
DRCR    544-0:  DRAES TRA PARBIT DVA FNCTN(30-34)=READ GO-BIT=0
DRSR    544-0:  DRAES TRA PARBIT ERR MOL PGM DPR DRY VV
DRER1   544-0:  DRAES TRA DCK
DRER2   544: 140600 200000
DRER3   544: 150600 200000
DRDA    544-0:  DRAES TRA SURFACE=4 SECTOR=12
DRDCY   544-0:  DRAES TRA DESIRED CYLINDER=456
DRCCY   544-0:  DRAES TRA CURRENT CYLINDER=456
DROFST  544-0:  DRAES TRA SGNCHG OFFSET=0.
DRECPS  544-0:  DRAES TRA PARBIT ECC POSITION=1695.
```

```
DRECPT  544-0:  DRAES TRA PARBIT ECC PATTERN=2400
CHAN-1 LOGOUT DATA
LOC
004     ICW: 200000 103074
005     SW1:  LOGOUT SBUSEN NWCSZ LNG-WC CLP POINTS TO: 103105
006     LAST UPDATED CCW: 424000 106400    +WC=640.  ADR=106400


CCW'S   CHAN-1
 LOC       +WC        ADR        MISC.
 ----      ----       ----       -------
103104    003600     00104000     OPDATA
103105    003600     00107600     OPDATA
103106    002400     00113400     OPDATA LSTXFR



COMMAND ERROR RECOVERY @ ADDR 77440 IS
READ ISSUED TO DRIVE #10
PATTERN IS "ANY" STARTING @ DISK BLK #114840.
(CYL=456, SUR=4, SECT=0)
TRANSFER SIZE = 12000 AT PGM PC #31215

ATTEMPTING RECOVERY OF A 40. SECTOR TRANSFER BY INDIVIDUAL SECTORS

## ECC CORRECTION RECOVERY ##
 ECC POSITION=1695.      ECC PATTERN=202400
BUFFER ADDRESS  106257
DATA BEFORE ECC 561333 333333
DATA AFTER ECC  573333 333333
CORRECTION ENTIRELY IN DATA FIELD

PROGRAM RUN TIME = 0:13:11
DRIVE 544 - 0<6> CYL# 456 SURF# 04  SECT# 11     LOG BLK# 114849.
RECOVERED FROM A READ ON RETRY #1.
ECC CORRECTION WAS USED...
--------------------


==========================================


*-*-*-*-* DONE INTERRUPT          PGM SW = 000010 000000
PROGRAM RUN TIME = 0:17:27
CONI-544:  EXCEP CHN-ER CNR MBCENB ATTN ATN-EN DONE PIA=4

DRAS:   200001

TEST NAME: "ACCEPT" RUNNING "RONLY" AT PC ADDRESS 31206
```

```
DRIVE #10
DISK START ADDRESS IS:  CYLINDER #1442 SURFACE #10  SECTOR #00
(WHICH EQUALS LOGICAL BLOCK #304920.)  BUFFER START ADDRESS = 104000
AND TRANSFER SIZE =  12000(8) OR 5120.(10)

PGM INTERRUPT PC WAS - 63145

DRIVE EXCEPTION ERROR ON DRIVE 544 - 0<6>
RHPTCR  544:  DRIVE=0  + BLOCK CNT=40. FNCTN+GO=71 (READ)
RHSTCR  544:  DRIVE=0  + BLOCK CNT=40. FNCTN+GO=71 (READ)
DRCR    544-0:  DRAES TRA PARBIT DVA FNCTN(3Q-34)=READ GO-BIT=0
DRSR    544-0:  DRAES TRA PARBIT ERR MOL PGM DPR DRY VV
DRER1   544-0:  DRAES TRA DCK
DRER2   544: 140600 200000
DRER3   544: 150600 200000
DRDA    544-0:  DRAES TRA SURFACE=11 SECTOR=16
DRDCY   544-0:  DRAES TRA PARBIT DESIRED CYLINDER=1442
DRCCY   544-0:  DRAES TRA PARBIT CURRENT CYLINDER=1442
DROFST  544-0:  DRAES TRA SGNCHG OFFSET=0.
DRECPS  544-0:  DRAES TRA ECC POSITION=314.
DRECPT  544-0:  DRAES TRA PARBIT ECC PATTERN=2400
CHAN-1 LOGOUT DATA
LOC
004     ICW: 200000 103074
005     SW1:  LOGOUT SBUSEN NWCSZ LNG-WC CLP POINTS TO: 103104
006     LAST UPDATED CCW: 630000 114400    +WC=768.  ADR=114400


CCW'S   CHAN-1
 LOC      +WC       ADR       MISC.
 ---      ---       ---       -----
103101   003600    00104000    OPDATA
103102   003600    00107600    OPDATA
103103   002400    00113400    OPDATA LSTXFR


COMMAND ERROR RECOVERY @ ADDR 77444 IS
READ ISSUED TO DRIVE #10
PATTERN IS "ANY" STARTING @ DISK BLK #304920.
(CYL=1442, SUR=10, SECT=0)
TRANSFER SIZE = 12000 AT PGM PC #31215

ATTEMPTING RECOVERY OF A 40. SECTOR TRANSFER BY INDIVIDUAL SECTORS

## ECC CORRECTION RECOVERY ##
 ECC POSITION=314.       ECC PATTERN=202400
BUFFER ADDRESS  114210
DATA BEFORE ECC 555555 055753
DATA AFTER ECC  555555 555753
CORRECTION ENTIRELY IN DATA FIELD
```

```
PROGRAM RUN TIME = 0:18:49
DRIVE 544 - 0<6> CYL# 1442 SURF# 11   SECT# 15     LOG BLK# 304953.
RECOVERED FROM A READ ON RETRY #1.
ECC CORRECTION WAS USED...
-----------------------

==========================================

PROGRAM RUN TIME = 0:19:5          RCTEST

PROGRAM RUN TIME = 0:20:44         FRTEST

PROGRAM RUN TIME = 0:22:0          NEXTST

PROGRAM RUN TIME = 0:23:44         INTTST

PROGRAM RUN TIME = 0:25:52         STEST

* TRACE * @ STST0 - FLT ONES
* TRACE * @ STST1 - FLT ZEROS

#-#-# SUMMARY DATA #-#-#
PROGRAM RUN TIME = 1:0:2


SYSTEM TOTALS (10)
BITS XFRED = 7.733 X 10(9)

         BITS READ =  4.623 X 10(9)
         BITS WRT =  3.109 X 10(9)


SEEKS = 31250.

RECALS = 100.


ERROR TOTALS - SYSTEM

SOFT READ = 3.
HARD READ = 0.

SOFT WRT = 0.
HARD WRT = 0.

SOFT POS = 0.
HARD POS = 0.

DATA COMPARE ERRORS = 0.
```

```
MBC DETECTED ERRORS

DATA BUS PARITY ERRORS = 0.
DRIVE RAE ERRORS = 0.
MBC DRIVE RESPONSE ERRORS = 0.
CHANNEL ERRORS = 0.

==========================================

* TRACE * @ STST2 - ALT BITS DATA

*-*-*-*-* DONE INTERRUPT          PGM SW = 000010 000000
PROGRAM RUN TIME = 1:4:51
CONI-544:  EXCEP CHN-ER CNR MBCENB ATTN ATN-EN DONE PIA=4

DRAS:   200001

TEST NAME: "ACCEPT" RUNNING "STEST" AT PC ADDRESS 31562


DRIVE #10
DISK START ADDRESS IS:  CYLINDER #226 SURFACE #11  SECTOR #00
(WHICH EQUALS LOGICAL BLOCK #57180.)  BUFFER START ADDRESS = 152000
AND TRANSFER SIZE =  2200(8) OR 1152.(10)

PGM INTERRUPT PC WAS - 52400

DRIVE EXCEPTION ERROR ON DRIVE 544 - 0<6>
RHPTCR  544:  DRIVE=0  + BLOCK CNT=9. FNCTN+GO=71 (READ)
RHSTCR  544:  DRIVE=0  + BLOCK CNT=11. FNCTN+GO=71 (READ)
DRCR    544-0:  DRAES TRA PARBIT DVA FNCTN(30-34)=READ GO-BIT=0
DRSR    544-0:  DRAES TRA PARBIT ERR MOL PGM DPR DRY VV
DRER1   544-0:  DRAES TRA DCK
DRER2   544: 140600 200000
DRER3   544: 150600 200000
DRDA    544-0:  DRAES TRA SURFACE=11 SECTOR=10
DRDCY   544-0:  DRAES TRA PARBIT DESIRED CYLINDER=226
DRCCY   544-0:  DRAES TRA PARBIT CURRENT CYLINDER=226
DROFST  544-0:  DRAES TRA SGNCHG OFFSET=0.
DRECPS  544-0:  DRAES TRA ECC POSITION=148.
DRECPT  544-0:  DRAES TRA ECC PATTERN=2000
CHAN-1 LOGOUT DATA
LOC
004    ICW: 200000 103074
005    SW1:  LOGOUT SBUSEN NWCSZ LNG-WC CLP POINTS TO: 103106
006    LAST UPDATED CCW: 604000 154000    +WC=128.  ADR=154000


CCW'S   CHAN-1
 LOC      +WC       ADR       MISC.
 ---      ---       ---       -----
103105   002200    00152000    OPDATA LSTXFR
```

```
COMMAND ERROR RECOVERY @ ADDR 77452 IS
READ ISSUED TO DRIVE #10
PATTERN IS "ALTB" STARTING @ DISK BLK #57180.
(CYL=226, SUR=11, SECT=0)
TRANSFER SIZE = 2200 AT PGM PC #31662

ATTEMPTING RECOVERY OF A 9. SECTOR TRANSFER BY INDIVIDUAL SECTORS


PROGRAM RUN TIME = 1:6:0
DRIVE 544 - 0<6> CYL# 226 SURF# 11  SECT# 07    LOG BLK# 57187.
RECOVERED FROM A READ ON RETRY #1.
--------------------


==================================================


*-*-*-*-* DONE INTERRUPT          PGM SW = 000010 000000
PROGRAM RUN TIME = 1:22:33
CONI-544:  EXCEP CHN-ER CNR MBCENB ATTN ATN-EN DONE PIA=4

DRAS:   200001

TEST NAME: "ACCEPT" RUNNING "STEST" AT PC ADDRESS 31562


DRIVE #10
DISK START ADDRESS IS:  CYLINDER #1442 SURFACE #11  SECTOR #11
(WHICH EQUALS LOGICAL BLOCK #304949.)  BUFFER START ADDRESS = 125000
AND TRANSFER SIZE =  2600(8) OR 1408.(10)

PGM INTERRUPT PC WAS - 44300

DRIVE EXCEPTION ERROR ON DRIVE 544 - 0<6>
RHPTCR  544:  DRIVE=0  + BLOCK CNT=11. FNCTN+GO=71 (READ)
RHSTCR  544:  DRIVE=0  + BLOCK CNT=20. FNCTN+GO=61 (WRITE)
DRCR    544-0:  DRAES TRA PARBIT DVA FNCTN(30-34)=READ GO-BIT=0
DRSR    544-0:  DRAES TRA PARBIT ERR MOL PGM DPR DRY VV
DRER1   544-0:  DRAES TRA DCK
DRER2   544: 140600 200000
DRER3   544: 150600 200000
DRDA    544-0:  DRAES TRA SURFACE=11 SECTOR=16
DRDCY   544-0:  DRAES TRA PARBIT DESIRED CYLINDER=1442
DRCCY   544-0:  DRAES TRA PARBIT CURRENT CYLINDER=1442
DROFST  544-0:  DRAES TRA SGNCHG OFFSET=0.
DRECPS  544-0:  DRAES TRA ECC POSITION=304.
DRECPT  544-0:  DRAES TRA PARBIT ECC PATTERN=2400
CHAN-1 LOGOUT DATA
LOC
004    ICW: 200000 103074
005    SW1:  LOGOUT SBUSEN NWCSZ LNG-WC CLP POINTS TO: 103106
006    LAST UPDATED CCW: 630000 126200    +WC=768.  ADR=126200
```

```
CCW'S   CHAN-1
 LOC      +WC        ADR        MISC.
 ----     ----       ---        -------
103105    002600     00125000    OPDATA LSTXFR


COMMAND ERROR RECOVERY @ ADDR 77426 IS
READ ISSUED TO DRIVE #10
PATTERN IS "ALTB" STARTING @ DISK BLK #304949.
(CYL=1442, SUR=11, SECT=11)
TRANSFER SIZE = 2600 AT PGM PC #31654

ATTEMPTING RECOVERY OF A 11. SECTOR TRANSFER BY INDIVIDUAL SECTORS

## ECC CORRECTION RECOVERY ##
 ECC POSITION=304.      ECC PATTERN=202400
BUFFER ADDRESS  126010
DATA BEFORE ECC 525252 525012
DATA AFTER ECC  525252 525252
CORRECTION ENTIRELY IN DATA FIELD

PROGRAM RUN TIME = 1:23:50
DRIVE 544 - 0<6> CYL# 1442 SURF# 11  SECT# 15    LOG BLK# 304953.
RECOVERED FROM A READ ON RETRY #1.
ECC CORRECTION WAS USED...
--------------------


==========================================


* TRACE * @ STST3 - RANDOM DATA
* TRACE * @ STST3B - BINARY COUNT DATA

*-*-*-*-* DONE INTERRUPT         PGM SW = 000010 000000
PROGRAM RUN TIME = 1:48:8
CONI-544:  EXCEP CHN-ER CNR MBCENB ATTN ATN-EN DONE PIA=4

DRAS:   200001

TEST NAME: "ACCEPT" RUNNING "STEST" AT PC ADDRESS 31562


DRIVE #10
DISK START ADDRESS IS:  CYLINDER #456 SURFACE #04  SECTOR #00
(WHICH EQUALS LOGICAL BLOCK #114840.)  BUFFER START ADDRESS = 154000
AND TRANSFER SIZE =  5000(8) OR 2560.(10)

PGM INTERRUPT PC WAS - 52375
```

```
DRIVE EXCEPTION ERROR ON DRIVE 544 - 0<6>
RHPTCR  544:  DRIVE=0  + BLOCK CNT=20. FNCTN+GO=71 (READ)
RHSTCR  544:  DRIVE=0  + BLOCK CNT=20. FNCTN+GO=61 (WRITE)
DRCR    544-0:  DRAES TRA PARBIT DVA FNCTN(30-34)=READ GO-BIT=0
DRSR    544-0:  DRAES TRA PARBIT ERR MOL PGM DPR DRY VV
DRER1   544-0:  DRAES TRA DCK
DRER2   544: 140600 200000
DRER3   544: 150600 200000
DRDA    544-0:  DRAES TRA SURFACE=4 SECTOR=12
DRDCY   544-0:  DRAES TRA DESIRED CYLINDER=456
DRCCY   544-0:  DRAES TRA CURRENT CYLINDER=456
DROFST  544-0:  DRAES TRA SGNCHG OFFSET=0.
DRECPS  544-0:  DRAES TRA PARBIT ECC POSITION=1683.
DRECPT  544-0:  DRAES TRA ECC PATTERN=2000
CHAN-1 LOGOUT DATA
LOC
004    ICW: 200000 103074
005    SW1:  LOGOUT SBUSEN NWCSZ LNG-WC CLP POINTS TO: 103104
006    LAST UPDATED CCW: 424000 156400    +WC=640.  ADR=156400


CCW'S   CHAN-1
 LOC      +WC       ADR       MISC.
 ---      ---       ---       -----
103103   003600    00154000    OPDATA
103104   001200    00157600    OPDATA LSTXFR



COMMAND ERROR RECOVERY @ ADDR 77450 IS
READ ISSUED TO DRIVE #10
PATTERN IS "COUNT" STARTING @ DISK BLK #114840.
(CYL=456, SUR=4, SECT=0)
TRANSFER SIZE = 5000 AT PGM PC #31714

ATTEMPTING RECOVERY OF A 20. SECTOR TRANSFER BY INDIVIDUAL SECTORS

## ECC CORRECTION RECOVERY ##
 ECC POSITION=1683.     ECC PATTERN=2000
BUFFER ADDRESS  156256          156257
DATA BEFORE ECC 673567 356616   735672 567237
DATA AFTER ECC  673567 356616   735673 567237
CORRECTION ENTIRELY IN DATA FIELD

PROGRAM RUN TIME = 1:49:28
DRIVE 544 - 0<6> CYL# 456 SURF# 04  SECT# 11    LOG BLK# 114849.
RECOVERED FROM A READ ON RETRY #1.
ECC CORRECTION WAS USED...
-------------------------
```

```
#-#-# SUMMARY DATA #-#-#
PROGRAM RUN TIME = 2:0:1


SYSTEM TOTALS (10)
BITS XFRED = 1.615 X 10(10)

         BITS READ =  8.832 X 10(9)
         BITS WRT =  7.318 X 10(9)


SEEKS = 31250.

RECALS = 100.


ERROR TOTALS - SYSTEM

SOFT READ = 6.
HARD READ = 0.

SOFT WRT = 0.
HARD WRT = 0.

SOFT POS = 0.
HARD POS = 0.

DATA COMPARE ERRORS = 0.


MBC DETECTED ERRORS

DATA BUS PARITY ERRORS = 0.
DRIVE RAE ERRORS = 0.
MBC DRIVE RESPONSE ERRORS = 0.
CHANNEL ERRORS = 0.

==========================================================

SP
>.
```

B.11 DFTUE

```
   STM
>. DFTUE VERSION 0.4, SV=0.13, CPU#=2257, MCV=157, MC0=1, H0=34, 60HZ

SWITCHES = 000000 000000
CLK SOURCE = NORMAL, CLK RATE = FULL, AC BLK 0 , CACHE: 0 1 2 3

MEMORY MAP =
FROM      TO          SIZE/K
00000000 00777777        256


TEST RH# OR DEV (CR WILL TEST ALL ON-LINE DRIVES ON FIRST RH):

CONFIGURATION:
RH20#  0  DEVICE CODE= 540
TM02 #0  TU45 #'S:  0

NOTE: ANY TAPES MOUNTED WRITE-ENABLED MAY BE WRITTEN ON.

WHAT TEST (H<CR> FOR HELP):  A

ACCEPTANCE TEST

BASIC TEST PART 1

NOW TESTING TM02/TU45 0/0 **********************
END PASS 1.

BASIC TEST PART 2

NOW TESTING TM02/TU45 0/0  ****************


NOTE: ASSUME ECO M8921-00008 HAS BEEN INSTALLED.
```

NOTE
The following tests will become DFTUK.

```
1600BPI RELIABILITY TEST
TM02/TU45 0/0      SN= 0576.

FINISHED TAPE PASS 1.******
800BPI RELIABILITY TEST
FINISHED TAPE PASS 1.******

CURRENT TEST= 267; CURRENT PASS = 3.;  STATISTICS:
```

```
TM02/TU45 0/0 IN 1600BPI MODE
         RECORDS*          SERS*    HERS*    BS/DERS NR OF WDS*
WRITE:   4385.             0.       0.       0.      8700462.
RD FWD:  4366.             0.       0.       0.      8700462.
RD REV:  4366.             0.       0.       0.      8700462.
NO DEAD TRKS

TM02/TU45 0/0 IN NRZI MODE
         RECORDS*          SERS*    HERS*    BS/DERS NR OF WDS*
WRITE:   2253.             0.       0. .     0.      4604207.
RD FWD:  2246.             0.       0.       0.      4602735.
RD REV:  2246.             0.       0.       0.      4602735.

WAITING FOR ALL DRIVES TO FINISH REWINDING...
```

B.12 DFSXA

```
>. P DFSXA
DFSXA.A10   VER 0.4   04-JAN-78
>. STD
>.
DECSYSTEM KL10 CHANNEL/DTE20 INTERACTION TEST (DFSXA)
VERSION 0.4, SV=0.13, CPU#=1087, MCV=157, MCO=1, HO=34, 60HZ

SWITCHES = 000010 000000
CLK SOURCE = NORMAL, CLK RATE = FULL, AC BLK 0 , CACHE: 0 1 2 3

MEMORY MAP =
FROM     TO          SIZE/K
00000000 00777777        256


PI LEVEL (1-7)?

DATA MASK(0-7777777777777)?

SYSTEM CONFIGURATION:
C0<T0,>
C1<P0,>
FOM:
F3R:


THE AVAILABLE COMMANDS ARE:

        A-      AUTO SELECT & GO
        BL-     BOOT LOAD FRONT END
        BH-     BOOT LOAD & HALT FRONT END
        BT-     BOOT TEST FRONT END
        CP-     PRINT CPU STATUS
        D-      ENTER DDT
        E-      EXAM SPECIFIED REGISTER(S)
        G-      GO START TESTING SELECTED DEVICES
        H-      TYPE THE HELP FILE
        MB-     PRINT MBOX STATUS
        N-      PRINT NAMES OF LEGAL REGISTERS
        PC-     PRINT SYSTEM CONFIGURATION
        PT-     PRINT CURRENTLY SELECTED PARAMETERS
        R-      REMOVE THE SPECIFIED DEVICE(S) FROM TEST SELECTION
        S-      SELECT THE FOLLOWING DEVICE(S)
        TM-     PRINT PROGRAM RUNTIME(ELAPSE TIME SINCE PROGRAM STARTED)
        Z-      ZERO TEST SELECTION TABLE
```

```
*A

CURRENT DEVICE SELECTION:
C0:
C1:
F0:
F3:

LOADING "DFSXAX" INTO FE# 3

TEST SUMMARY-RUNTIME: 0:4:29                (SW13 = 1)
<C0:>
WORDS WRITTEN: 135168.  WRITE RETRIES: 0.       WRITE ERRORS: 0.
WORDS READ: 4224.       READ ERRORS: 0. DATA ERRORS: 0.
CHN ERRORS: 0.
<C1:>
WORDS WRITTEN: 135168.  WRITE RETRIES: 0.       WRITE ERRORS: 0.
WORDS READ: 4224.       READ ERRORS: 0. DATA ERRORS: 0.
CHN ERRORS: 0.
<C10:>
WORDS WRITTEN: 99072.   WRITE RETRIES: 0.       WRITE ERRORS: 0.
WORDS READ: 33024.      READ ERRORS: 0. DATA ERRORS: 0.
CHN ERRORS: 0.
<C13:>
WORDS WRITTEN: 99072.   WRITE RETRIES: 0.       WRITE ERRORS: 0.
WORDS READ: 33024.      READ ERRORS: 0. DATA ERRORS: 0.
CHN ERRORS: 0.

TEST SUMMARY-RUNTIME: 0:4:57
<C0:>
WORDS WRITTEN: 135168.  WRITE RETRIES: 0.       WRITE ERRORS: 0.
WORDS READ: 9856.       READ ERRORS: 0. DATA ERRORS: 0.
CHN ERRORS: 0.
<C1:>
WORDS WRITTEN: 135168.  WRITE RETRIES: 0.       WRITE ERRORS: 0.
WORDS READ: 9856.       READ ERRORS: 0. DATA ERRORS: 0.
CHN ERRORS: 0.
<C10:>
WORDS WRITTEN: 99072.   WRITE RETRIES: 0.       WRITE ERRORS: 0.
WORDS READ: 37152.      READ ERRORS: 0. DATA ERRORS: 0.
CHN ERRORS: 0.
<C13:>
WORDS WRITTEN: 99072.   WRITE RETRIES: 0.       WRITE ERRORS: 0.
WORDS READ: 37152.      READ ERRORS: 0. DATA ERRORS: 0.
CHN ERRORS: 0.
```

```
TEST SUMMARY-RUNTIME: 0:5:24
<C0:>
WORDS WRITTEN: 135168.  WRITE RETRIES: 0.       WRITE ERRORS: 0.
WORDS READ: 15488.      READ ERRORS: 0. DATA ERRORS: 0.
CHN ERRORS: 0.
<C1:>
WORDS WRITTEN: 135168.  WRITE RETRIES: 0.       WRITE ERRORS: 0.
WORDS READ: 15488.      READ ERRORS: 0. DATA ERRORS: 0.
CHN ERRORS: 0.
<C10:>
WORDS WRITTEN: 99072.   WRITE RETRIES: 0.       WRITE ERRORS: 0.
WORDS READ: 41280.      READ ERRORS: 0. DATA ERRORS: 0.
CHN ERRORS: 0.
<C13:>
WORDS WRITTEN: 99072.   WRITE RETRIES: 0.       WRITE ERRORS: 0.
WORDS READ: 41280.      READ ERRORS: 0. DATA ERRORS: 0.
CHN ERRORS: 0.

=> 016                  (SW7 = 1)

=> 017

=> 020

=> 021
END PASS 1.
CMD:
>.
```

B.13 KLDCP BOOT VIA SW REG

```
RSX-20F VB12-12 11:50 19-DEC-77

[SY0: REDIRECTED TO DB0:]
[DB0: MOUNTED]
KLI -- VERSION VB06-07 RUNNING
KLI -- ENTER DIALOG [NO,YES,EXIT,BOOT]?
KLI>EXIT


PAR -- [PARSER] ESE - EBOX STOPPED - EXAMINE
PAR#MCR BOO

BOO>DBOOT
DECSYSTEM DIAGNOSTIC CONSOLE
VERSION 0.16
SWR = 000207    DTE # 0
CMD:
>.
```

B.14 MONITOR LOAD SAMPLE

```
RSX-20F VB12-12 11:50 19-DEC-77

[SY0: REDIRECTED TO DB0:]
[DB0: MOUNTED]
KLI -- VERSION VB06-07 RUNNING
KLI -- MICROCODE VERSION 202 LOADED
KLI -- ALL CACHES ENABLED
LOGICAL MEMORY CONFIGURATION:
                    CONTROLLER
ADDRESS    SIZE   RQ0 RQ1 RQ2 RQ3   CONTYPE INT
00000000   192K   00  01  00  01     MB20     2
KLI -- BOOTSTRAP LOADED AND STARTED


[PS MOUNTED]

? SETSPD: COULD NOT SET MTA 0 SERI
System restarting, wait...AL # 350
? SETSPD: COULD NOT SET MTA 1 SERIAL # 398
? SETSPD: COULD NOT SET MTA 2 SERIAL # 418
ENTER CURRENT DATE AND TIME: 26 JUNE 78 1640

YOU HAVE ENTERED MONDAY, 26-JUNE-1978 4:40PM,
 IS THIS CORRECT (Y,N) Y
WHY RELOAD? TEST SAMPLE
RUN CHECKD? N

RUNNING DDMP


SYSJOB 3(7) STARTED AT 26-JUN-78 1640
RUN SYS:INFO
RUN SYS:MAILER
RUN SYS:QUASAR

JOB 0 /LOG OPERATOR XX OPERATOR
ENA
^ESET LOGINS ANY
^ESEND * WARNING, KLAD-20  SYSTEM IN OPERATION
PTYCON
GET SYSTEM:PTYCON.ATO
/
SJ  0:
SJ  0:  SYS SN# 1234  KLAD V3  (KLAD20-K-3.0-A), TOPS-20 MONITOR 3(1371)
SJ  0: @LOG OPERATOR OPERATOR
SJ  0:  JOB 1 ON TTY106 26-JUN-78 16:40:47
SJ  0: YOU UNDERSTAND HUMAN NATURE AND SYMPATHIZE WITH ITS WEAKNESS.
SJ  0:  END OF LOGIN.CMD.1
```

```
[From OPERATOR: WARNING, KLAD-20  SYSTEM IN OPERATION]
SJ  0: @ENA
SJ  0: $^ESET LOGINS ANY
SJ  0: $^ESEND * WARNING, KLAD-20  SYSTEM IN OPERATION
SJ  0: $PTYCON
SJ  0: PTYCON> GET SYSTEM:PTYCON.ATO
SJ  0: PTYCON> SILENCE
SJ  0: PTYCON.LOG.1
SJ  0: PTYCON> B-START
SJ  0: PTYCON> L-START PLPT0=LPT0
SJ  0: PTYCON>
SJ  0: **** L(0) 16:41:49 ****
SJ  0: START PLPT0=LPT0
SJ  0: %LPTDOL  DEVICE PLPT0 IS OFF-LINE
SJ  0: LPTSPL>[LPTLVF  LOADING VFU 'NORMAL' IN PLPT0]
SJ  0: **** B(1) 16:41:51 ****
SJ  0: START
SJ  0: !
SJ  0: PTYCON> ;LPT1:L1-START PLPT1=LPT1
SJ  0: PTYCON> ;CDR:S-START PCDR0:=CDR0:
SJ  0: PTYCON> WHAT ALL
SJ  0: L(0)       4          OPERATOR   LPTSPL     TI          0:0:0
SJ  0: B(1)       5          OPERATOR   BATCON     TI          0:0:0
SJ  0: P(2)       3          OPERATOR   OPLEAS     RN          0:0:0
SJ  0: ACC(3)     6          F-S        EXEC       TI          0:0:0
SJ  0: O(4)       2          OPERATOR   EXEC       TI          0:0:2
SJ  0: PTYCON> ;*** IF YOU WISH TO ENABLE THE "BACK-UP REGISTERS",   ***
SJ  0: PTYCON> ;*** SUBMIT THE BATCH FILE <OPERATOR>BKUP.CTL FROM     **
*
SJ  0: PTYCON> ;*** ANOTHER JOB LOGGED-IN AS <OPERATOR>               **
*
SJ  0: PTYCON> ;*** WARNING * * * IF REV 3/11 ECO IS NOT INSTALLED,   **
*
SJ  0: PTYCON> ;*** PERMANENT DAMAGE WILL RESULT TO THE FILE SYSTEM   **
*

 SYS SN# 1234  KLAD V3  (KLAD20-K-3.0-A), TOPS-20 Monitor 3(1371)
@
```

APPENDIX C
HARDWARE ACCEPTANCE TESTS

DIGITAL EQUIPMENT CORPORATION
HARDWARE ACCEPTANCE TESTS

Customer: _____

System: _____ Serial No: _____

Device: **Front End** Serial No: _____

Test No	Run Time (Min)	To Demonstrate	Method of Test/ Diagnostic	Notes	Pass Check
1.1	10	11/40 CPU	DBQEA		
1.2	5	BM873-Y*	DZBMD	Run Test 1 *Designates current revision	
1.3	5	DL11-E	DZDLC	Use H315 test connector	
1.4	5	KW11-L	DZKWA		
1.5	15	MF11UP	DZQMC		
1.6	15	RX01/RX11	DZRXA	(D = PASS COUNT)	
1.7	30	F/E System	SY2040 (See Note)	SY2040 = DECX11 Modify KWDAO and KWAFO for 50 Hz. Set SW12 for pass count.	

Signoff Date

DIGITAL Representative _____

Customer Signature _____

DIGITAL EQUIPMENT CORPORATION
HARDWARE ACCEPTANCE TESTS

Customer: _____

System: _____ Serial No: _____

Device: **KL10 CPU** serial No: _____

Test No	Run Time (Min)	To Demonstrate	Method of Test/ Diagnostic	Notes	Pass Check
2.1	5	Instruction times	DFKFB	Load J BT. CMD first. Compare results with sample set.	
2.2	15	DTE from F/E	DHDTE	2.2 – 2.11 and 3.1 – 3.10 may be run automatically by using the B command string.	
2.3		EBox Part 1	DHKAA		
2.4		EBox Part 2	DHKAB		
2.5		MBox	DHKBA		
2.6		Memory Control	DHKBB		
2.7		MBox cache	DHMCA See Note 1	Note 1 Will say "both option bit 19" and "cache bit." Indicate no cache if cache option is not installed. Test will abort.	
2.8		Cache RAM banger	DHMCB		
2.9		Meter board	DHKCA		
2.10		Channel control	DHKBD		
2.11		Channel loop-back	DHKBE		

Signoff Date

DIGITAL Representative _____

Customer Signature _____

DIGITAL EQUIPMENT CORPORATION
HARDWARE ACCEPTANCE TESTS

Customer: _____

System: _____ Serial No: _____

Device: **KL10 CPU** Serial No: _____

Test No	Run Time (Min)	To Demonstrate	Method of Test/ Diagnostic	Notes	Pass Check
3.1	15	Basic instructions	DFKAA	3.1 – 3.10 may be run automatically by using the KLCPU command string.	
3.2		Basic instructions	DFKAB		
3.3		Basic instructions	DFKAC		
3.4		Basic instructions	DFKAD		
3.5		Advance instruction set	DFKCA		
3.6		Basic instruction reliability	DFKBA		
3.7		Paging	DFKEA		
3.8		Monitor UUOs and user UUOs	DFKEB		
3.9		DTE from B/E	DFDTE		
3.10		Processor function reliability	DFKDA		

Signoff Date

DIGITAL Representative _____

Customer Signature _____

DIGITAL EQUIPMENT CORPORATION
HARDWARE ACCEPTANCE TESTS

Customer: _____

System: _____ Serial No: _____

Device: **Memory** Serial No: _____

Test No	Run Time (Min)	To Demonstrate	Method of Test/ Diagnostic	Notes	Pass Check
4.1	40	Memory 1. Data pattern 2. Memory address 3. Worst case pattern 4. Floating 1s and 0s	DDMMD	Run BT command string to load microcode, subroutine, etc.	
4.2	5	Memory functions	DDMME		
4.3	20	Memory margins	DGMMA		

Signoff Date

DIGITAL Representative _____

Customer Signature _____

DIGITAL EQUIPMENT CORPORATION
HARDWARE ACCEPTANCE TESTS

Customer: _____

System: _____ Serial No: _____

Device: **RH20** Serial No: _____

Test No	Run Time (Min)	To Demonstrate	Method of Test/ Diagnostic	Notes	Pass Check
5.1	5	RH20 functions for all channels available	DFRHB	Switch 1 up for operator select.	

Signoff Date

DIGITAL Representative _____

Customer Signature _____

DIGITAL EQUIPMENT CORPORATION
HARDWARE ACCEPTANCE TESTS

Customer: _____

System: _____ Serial No: _____

Device: **RP04** _____ Serial No: _____

Test No	Run Time (Min)	To Demonstrate	Method of Test/ Notes	Check	Pass
6.1	5	Disk format	DDRPI	Test name: FORMAT Demonstrate for 1 drive only unless packs are unformatted. 20-sector format	
6.2	60	Disk functions	DDRPI	Run ACCEPT script on all drives for 1 pass. Allowable errors as per pack format spec.	
6.3	30	Drive compatability	DDRPI	Run RONLY and rotate packs through all drives.	
6.4	10	Access times	DDRPI	Test name: PTIME Average 28 ms Trk to trk 4 ms Max seek 50 ms	
6.5	60	Dual port facility	DZRJA	Mech. read/write test. Pack must be 22-sector format.	

Signoff Date

DIGITAL Representative _____

Customer Signature _____

DIGITAL EQUIPMENT CORPORATION
HARDWARE ACCEPTANCE TESTS

Customer: _____

System: _____ Serial No: _____

Device: **RP06** _____ Serial No: _____

Test No	Run Time (Min)	To Demonstrate	Method of Test/ Diagnostic	Notes	Pass Check
6.1	5	Disk format	DDRPI	Test name: FORMAT Demonstrate for 1 drive only unless packs are unformatted. 20-sector format	
6.2	60	Disk functions	DDRPI	Test name: ACCEPT Run ACCEPT script on all drives for 1 pass. Allowable errors as per pack format spec.	
6.3	30	Drive compatability	DDRPI	Run RONLY and rotate packs through all drives.	
6.4	10	Access times	DDRPI	Test name: PTIME Average 28 ms Trk to trk 7 ms Max seek 54 ms	
6.5	60	Dual port facility	DZRJA	Mech. read/write test. Pack must be 22-sector format.	

Signoff Date

DIGITAL Representative _____

Customer Signature _____

DIGITAL EQUIPMENT CORPORATION
HARDWARE ACCEPTANCE TESTS

Customer: _____

System: _____ Serial No: _____

Device: TU45 Serial No: _____

Test No	Run Time (Min)	To Demonstrate	Method of Test/ Diagnostic	Notes	Pass Check
7.1	60	Basic functions	DFTUK	Run ACCEPT script on all drives.	
7.2	60	Reliability	DFTUF		
7.3	5	Rewind	Stop watch check	Nominal rewind time 115 s	

Signoff Date

DIGITAL Representative _____

Customer Signature _____

DIGITAL EQUIPMENT CORPORATION
HARDWARE ACCEPTANCE TESTS

Customer: _____

System: _____ Serial No: _____

Device: **LP20-AB** Serial No: _____

Test No	Run Time (Min)	To Demonstrate	Method of Test/ Diagnostic	Notes	Pass Check
8.1	15	Function test	DZLPB	Set SW0 = 1	
8.2	5	Switches, lights and indicators	Manual	Check all error functions for correct operation.	
8.3	5	Print quality	Visual		

Signoff Date

DIGITAL Representative _____

Customer Signature _____

DIGITAL EQUIPMENT CORPORATION
HARDWARE ACCEPTANCE TESTS

Customer: _____

System: _____ Serial No: _____

Device: **DC20** Serial No: _____

Test No	Run Time (Min)	To Demonstrate	Method of Test/ Diagnostic	Notes	Pass Check
9.1	75	Diagnostic functions	DZDHM	Use H315 test plugs. Prints end pass.	
9.2	30	Reliability	DZDHN	Set SW7 for quick pass. Prints end pass.	
9.3	15	Modem tests	DZDHK	Use H8611 test connectors. End pass = ring bell	

Signoff Date

DIGITAL Representative _____

Customer Signature _____

DIGITAL EQUIPMENT CORPORATION
HARDWARE ACCEPTANCE TESTS

Customer: _____

System: _____ Serial No: _____

Device: CD20 Serial No: _____

Test No	Run Time (Min)	To Demonstrate	Method of Test/ Diagnostic	Notes	Pass Check
10.1	15	Logic tests Data tests	DZCDB	Two card decks required as follows: 1. Binary deck MAINDEC - 89-D1B2-C 2. Alphanumeric deck MAINDEC - 89-D1B1-C.	

Signoff Date

DIGITAL Representative _____

Customer Signature _____

DIGITAL EQUIPMENT CORPORATION
HARDWARE ACCEPTANCE TESTS

Customer: _____

System: _____ Serial No: _____

Device: **DN20** Serial No: _____

Test No	Run Time (Min)	To Demonstrate	Method of Test/ Diagnostic	Notes	Pass Check
11.1	5	11/34 CPU	FKAAB		
11.2	2	11/34 TRAPS	FKABB		
11.3	5	11/34 EIS	FKACA		
11.4	2	DL11-W	ZDLDA		
11.5	2	DZ11	ZDZAD	Asynch 8-line test	
11.6	4	DUP11	ZDPBB	Transmitter test	
11.7	4	DUP11	ZDPCB	Receiver test	
11.8	4	DUP11	ZDPDB	Data/function test	
11.9	4	DUP11	ZDPEA	Confidence test	
11.10	2	DTE20	DGDTE	2nd F/E DTE test	
11.11	3	11/34 Mem. management	FKTHA		
11.12	15	Memory	DZQMC		
11.13	15	System	DECX11		

Signoff Date

DIGITAL Representative _____

Customer Signature _____

DIGITAL EQUIPMENT CORPORATION
HARDWARE ACCEPTANCE TESTS

Customer: _____

System: _____ Serial No: _____

Device: **System (Start-up)** Serial No: _____

Test No	Run Time (Min)	To Demonstrate	Method of Test/ Diagnostic	Notes	Pass Check
12.1	5	Power switching 1. ON (Note 1) 2. OFF (Note 2)	Manual	Note 1 No failure indication Note 2 To be done using system or main room power emergency OFF. No failure indication on restart.	
12.2	5	Cold restart	Manual	To be performed after overnight switch-off. May be combined with 12.1. No fault indication.	
12.3	30	System exerciser	DFSXA		
12.4	See note	Microprogram and monitor load	Disk Boot	Boot KLAD moniter. Configure command file. Submit FA&T ACCEPT. Run 72 hours.	

Signoff Date

DIGITAL Representative _____

Customer Signature _____

APPENDIX D
DECSYSTEM-20 INSTALLATION REPORT

Accurate, detailed, and timely installation data is necessary to improve the DECSYSTEM-20. With this information it will be possible to detect reoccuring problems. Once a problem is identified it will be corrected. This process will result in future systems that are easier and faster to install.

The installation report on the following page is the vehicle for providing the needed information. It should be completed and returned within five days after the hardware acceptance date. The form should be returned to:

Field Service Product Support
MR1-1/S35
Attention: Installation Department.

The quality of the future DECSYSTEM-20 depends on the quality of the installation report completed today.

DECSYSTEM-20 INSTALLATION REPORT

Customer Name: _____

System Serial No: _____

Field Service Branch: _____

Hardware Installation Period: From _____ To _____

Software Installation Period: From _____ To _____

Hardware Acceptance Date: _____

Contract Type: _____ Hours/Day _____ Days/Week _____

Missing Documentation: _____

_____

Missing Diagnostics: _____

_____

Missing Hardware: _____

_____

General Condition of System Upon Arrival: _____

_____

PROBLEMS DURING INSTALLATION

Device _____ **Comments** _____

KL10-Based DECSYSTEM-20 INSTALLATION MANUAL
EK-0KL20-IN-001

Reader's Comments

Your comments and suggestions will help us in our continuous effort to improve the quality and usefulness of our publications.

What is your general reaction to this manual? In your judgment is it complete, accurate, well organized, well written, etc.? Is it easy to use? _____

_____

_____

_____

What features are most useful? _____

_____

_____

_____

What faults or errors have you found in the manual? _____

_____

_____

_____

Does this manual satisfy the need you think it was intended to satisfy? _____

Does it satisfy *your* needs? _____ Why? _____

_____

_____

_____

☐ Please send me the current copy of the *Technical Documentation Catalog*, which contains information on the remainder of DIGITAL's technical documentation.

Name _____ Street _____
Title _____ City _____
Company _____ State/Country _____
Department _____ Zip _____

Additional copies of this document are available from:

Digital Equipment Corporation
444 Whitney Street
Northboro, Ma 01532
Attention: Communications Services (NR2/M15)
Customer Services Section

Order No. EK-0KL20-IN-001

— — — — — — — — — — — — Fold Here — — — — — — — — — — —

— — — — — — — — — — Do Not Tear - Fold Here and Staple — — — — — — — — —

FIRST CLASS
PERMIT NO. 33
MAYNARD, MASS.

BUSINESS REPLY MAIL
NO POSTAGE STAMP NECESSARY IF MAILED IN THE UNITED STATES

Postage will be paid by:

Digital Equipment Corporation
Technical Documentation Department
200 Forest Street (MR1-2/T17)
Marlboro, Massachusetts 01752