C-100

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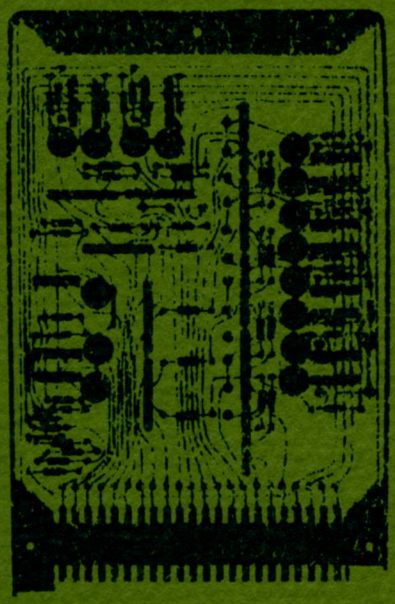
SYSTEM MODULES



DIGITAL EQUIPMENT CORPORATION

digital

MODULES

A complete selection of solid state circuit modules in three compatible speed lines specially packaged for system design, test, and construction applications

DIGITAL EQUIPMENT CORPORATION • MAYNARD, MASSACHUSETTS

CONTENTS

INPUT-OUTPUT MODULES

MODULE ACCESSORIES

PREFACE

Digital Equipment Corporation (DEC) System Modules are packaged electronic circuits for use in the design and construction of digital equipment. Well defined loading rules and wiring instructions and a plentiful supply of application information make designing with these modules as easy for the least experienced as for the most expert. Careful circuit design and built-in safety features permit the experimenter to try different logical arrangements without risking burnt out components.

The basic logical element for DEC modules is the transistor inverter. It offers both emitter and base gating, high gain, and well defined output levels at either ground or —3 volts. The state of a decision element is changed by the coincidence of static levels and a differentiated level change or a trigger pulse. Since all DEC System Modules use levels and pulses of the same amplitude, modules with different speed characteristics can be used together compatibly. Changing the duration of trigger pulses to match speed characteristics is the task of standard pulse amplifiers that link groups of modules.

Saturating transistors, a key design feature, free DEC modules from dependence on close tolerance components or closely regulated power supplies. Logic level stability is preserved within the circuits. Clamped load resistors and silicon diode chains stabilize ONE (—3 volt) outputs; internal resistor paths return transistor bases to ground for ZERO stability when no ONE's are present. Because logic levels are not drawn directly from power supplies, accidental shorting will not disable whole sections of logic. Power wiring which, if shorted, could damage circuit components, is isolated from logic wiring by busses across the top three pins of each module backboard. Remaining pins carry only logic levels which cannot damage circuits.

Module flexibility, an important consideration in implementing system design, is enhanced by circuit simplicity and iterseries compatibility. From the few basic circuits that are the fundamental building blocks of logical design, complex system can be built. Operating speeds indicate from which series basic circuits are to be selected for different portions of such systems.

For the design tasks of input-output communication and intersystem buffering or for specialized jobs such as analog-digital conversion, a variety of special circuits is available. Accessory equipment such as power supplies, mounting panels, and housing cabinets is made to accommodate system modules in various applications.

A review of DEC symbology and common design configurations, detailed descriptions of circuit functions and applications, and complete specifications for the entire line of system modules and module accessories appear on pages of this catalogue. More information on modules and accessories, news of recent additions to the module line, and assistance with module application problems can be obtained by contacting DEC's Application Department in Maynard, Massachusetts, or any of the conveniently located field offices.

DEFINITIONS, LOADING, AND HELPFUL HINTS

STANDARD SIGNALS

Standard Levels are 0 and −3 volts. The tolerance on the more positive level is 0 to −0.3 volts. The tolerance on the more negative level is −3 volts to −4 volts.

Standard Negative Pulses are −2.5 volts in amplitude with a positive overshoot of similar amplitude. These pulses are referenced to ground. The overshoot pulse is necessary to allow the transformer to recover, and also cleans out holes in the transistors, increasing the speed of logical operations.

Standard Positive Pulses are identical to the Negative Pulses except that the polarity is reversed.

The timing characteristics of Standard Pulses depend on the speed line. For the 4000-series, pulses have a duration of 0.4 microseconds. For the 1000-series the pulse duration is 70 nanoseconds. For the 6000-series pulse duration is 40 nanoseconds. A detailed description of the requirements for external input signals which may be used as the equivalent of Standard Pulses is outlined under the pulse amplifier descriptions of each series.

LOGIC LEVELS DEFINITIONS

DEC modules use dual-polarity level logic. Logical voltage levels are −3 volts and ground. Correspondence between the logic state ONE or ZERO and the voltage levels −3 and ground is indicated at each point in the logic drawing by a diamond. This diamond defines the necessary voltage level for the action desired. A solid ◆ diamond denotes a −3 volt assertion level and a hollow ◇ diamond denotes a ground assertion level. When two uses are to be made of the same level a split ◈ diamond is used.

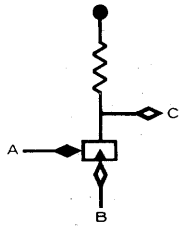
With these symbols the logical designer is able to produce in one step a logical drawing which can be directly implemented with modules. This method also allows a combination of amplification and gating without the added inversions usually required if a single logical state is always associated with a single logical voltage level.

Figures 1 and 2 show how the Digital logical method is used to form an AND gate or an OR gate from a single inverter. The inverter serves as an AND gate when the definitions in Figure 1 are satisfied.

A = 1, if negative (−3V)

B = 1, if ground

C = 1, if ground



AB = C

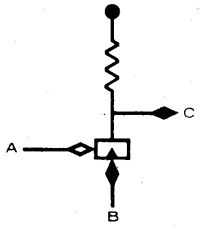
Figure 1

The same inverter serves as an OR gate if the definitions of Figure 2 are satisfied.

A = 1, if ground

B = 1, if negative

C = 1, if negative



A + B = C

Figure 2

LOADING

DEFINITIONS

To facilitate the design of systems, a number of simple loading definitions and rules have been made. These do not cover all possible configurations, but they do serve as a useful guide.

Base Load is the current which must be taken from the base of a d-c inverter to keep it in a saturated state. In this condition the inverter base input terminal is at −3 volts, the transistor base is at ground, and a nominal 1-milliampere current is drawn through the 3000-ohm base resistor to ground. Inverter load resistors, when clamped at −3 volts, have nominally 12 volts across their 1500 ohms; they can accept a nominal current of eight milliamperes. Ideally, this would drive eight units of Base Load, but tolerance considerations limit the number to seven.

Pulse Load is the load presented to a pulse source when driving the base of an inverter. Pulse amplifiers are usually limited to driving 16 pulse bases. This number should be decreased if the bases are widely separated, and it can be increased to 18 if they are close together. The series inductance and shunt capacitance of the connecting wires can make the pulses at the end of a string of bases either large or small. Consequently, when

a number near the maximum is being driven, the pulse amplitude should be carefully checked after installation. A terminating resistor of 100 to 300 ohms will reduce ringing on a heavily loaded pulse line.

Pulse Load is also the load seen by a pulse source when driving one direct set or direct clear input of a flip-flop — approximately the same as when driving a base. One pulse source cannot drive both direct inputs of flip-flops and inverter bases because the direct input pulses are positive from a normal ground level and base input pulses are negative from a normal ground level.

Pulsed Emitter Load is the load seen by the collector of an inverter driving the pulse input to a flip-flop, pulse amplifier, or delay. The pulse current goes through all the inverters in series with the pulse input, and it should be assumed to be the load on each of the series inverters.

DC Emitter Load is the load seen by the collector of an inverter driving a clamped load resistor. This load is also seen by the collector of an inverter which is driving an emitter in a network of inverters which is terminated by a clamped load resistor. The collector of an inverter driving an emitter in a network of transistors must also supply the base current leaving the inverters higher in the chain. This number is normally small, but in complex networks it must be considered.

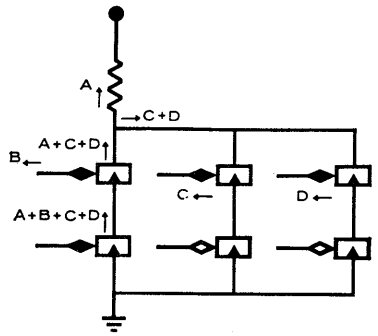


Figure 3

An inverter can drive no more than one clamped load resistor and six bases of on-inverters. Since transistors are almost symmetrical, this on-base current can also flow through the collector of a transistor whose emitter is open, as shown in Figure 3. In this case, the collector of the bottom on-transistor must carry the current A from the load resistor and the base currents from B, C, and D. Nominally, the current required is 10 milliamperes to a negative voltage return; however, this is increased by the base current required. Most inverters can supply a 15-milliampere collector current; 20 milliamperes can be supplied by the inverters in Types 4102, 4105, 4106, 4110, 4111, 4150, 4151, 4201, and 4603.

Capacitor-Diode Gate Level Input does not present any d-c load. A transient load occurs when the input level changes.

LOADING FOR 500 KC AND 5 MC INVERTERS

Transistor inverters serve two functions. When used as level gates, they are placed in series and parallel configurations to perform logic. When used as pulse gates, the inverter will sample the logic performed by the level gates and read the results into a flip-flop or other active element.

When used as a pulse gate, an inverter will drive only one pulsed unit. Inverters serving as level gates are usually considered as simple switches when designing logical networks, but because they are not ideal switches, there are certain limitations which have to be taken into account. The voltage drop across saturated inverters is not zero; it is closer to 0.1 volt. As a result, inverters cannot be stacked indefinitely. Three inverters are the most that can be put in series if the output is to drive another inverter, as in Figure 4.

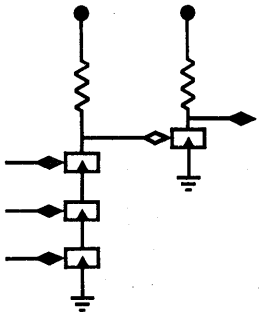


Figure 4

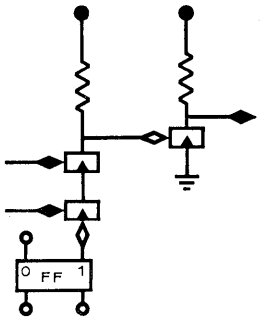


Figure 5

If inverters are in series with the output of a flip-flop, as in Figure 5, the flip-flop buffer inverter is considered to be one of the three series transistors allowed.

When the output of a series of inverters is driving the input of a pulse amplifier or delay unit or the set or clear input of a flip-flop, as in Figure 6, a fourth transistor serving as a pulse gate may be added in series. Only three may be used in series when driving the complement input of a buffered flip-flop when the P-pulse is used.

It is important to note that a clamped load resistor is tied to the emitter of each pulse transistor when it is being driven from an inverter or a network of inverters, as in Figure 6.

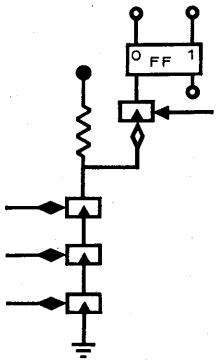
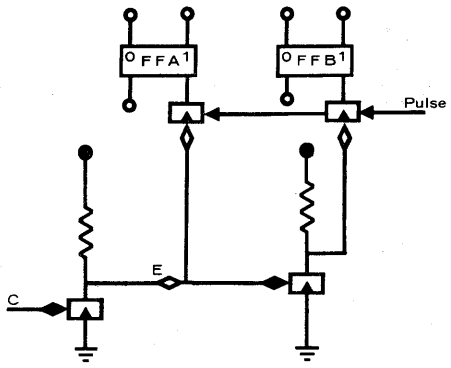


Figure 6*

Because inverters are not really ideal switches, each collector of a series string of d-c inverters supplying a pulse inverter will go somewhat negative during the pulse. This means that if a series of inverters is supplying both pulse current and a d-c signal, care must be taken because a signal will occur in the d-c output during the pulse.

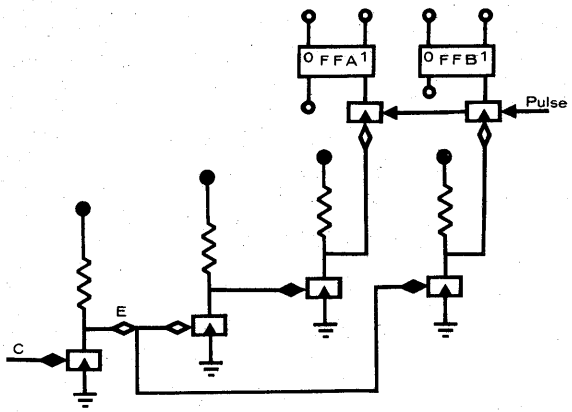


Illegal Inverter Use

Figure 7

In Figure 7, when the input C is negative, flip-flop A should be set by the pulse, but flip-flop B should not be set. However, during the pulse, collector E of the d-c inverter feeding flip-flop A will go slightly negative. It will partly turn on the d-c inverter feeding flip-flop B, and sometimes it will set flip-flop B as well as flip-flop A. This network will work only if the pulses are not simultaneous.

*The clamped load resistor is not needed in 5-megacycle circuits when the pulse inverter is driven from a single series of inverters and the length of wire between inverters is short. In the 500-kilocycle line this clamped load resistor can be replaced by a 1N276 diode from the emitter of the pulse inverter to ground, connected so as to prevent this point from going positive.



Recommended Inverter Use

Figure 8

The network shown in Figure 8 will work whether or not the pulses are simultaneous. Two additional inverters have been added so that collector E will no longer be pulled negative by the pulse, since the pulse current will now come directly from ground instead of collector E. (If both outputs are driving the same flip-flop, the network shown in Figure 7 can be used safely because the output of the A-side will be much greater than that of the B-side.)

LOADING RULES FOR 10-MC INVERTERS

The high speed transistors used in 10-megacycle inverters have a larger saturation voltage drop than the transistors used in the 5-megacycle and 500-kilocycle inverters. Because of this slightly larger d-c drop, a maximum of two inverters may be put in series if the output is to drive another inverter. (See Figure 9.) If a flip-flop output is driving an inverter emitter, this flip-flop must be counted as an inverter. (See Figure 10.)

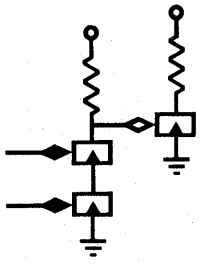


Figure 9

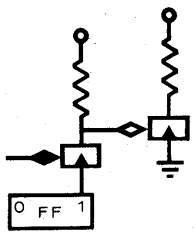


Figure 10

When the output of a series of transistor inverters is driving the input of a flip-flop or pulse amplifier, as in Figure 11, an inverter pulse gate may be added in series with the two level gates. This pulsed inverter must be placed at the bottom of the series string;

that is, the end farthest from the load. The emitter may be driven by a flip-flop unless the sampling pulse is a P-pulse (the carrying pulse in counters); in this case the emitter should be grounded.

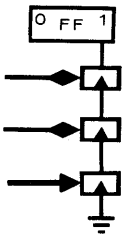


Figure 11

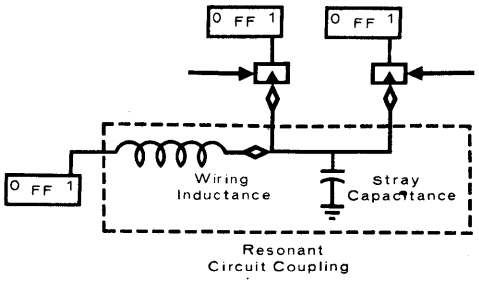


Figure 12

When connecting 10-megacycle inverters, the user should avoid wiring inductance and stray capacitance as much as possible. Figure 12 illustrates how a wire, which is conducting current for two pulsed inverters back to the flip-flop output, may serve as a coupling connection between the two pulsed inverters and produce ringing. This ringing may produce a positive pulse on the emitter of the other inverter, thus turning it on at the wrong time. To avoid this, each emitter must be driven by a separate wire unless the distance is very short.

TIMING

DEFINITIONS

Level Delay Time is the time delay between the point of 10-percent input change and the point of 10-percent output change in a given circuit. The input is assumed to be the output of a flip-flop of the same frequency series as the circuit under discussion, or a level change with similar characteristics. This is also referred to as delay for output fall or delay for output rise.

Pulse Delay Time is the time delay between the point of 10-percent input change and the point of 10-percent output change in a given circuit, when the input is a Standard Pulse of the same frequency line as the circuit under discussion.

Rise Time and Fall Time are the time delay between the 10-percent and 90-percent points of a voltage change.

Total Transition Time is the time delay between the point of 10-percent input change and the point of 90-percent output change in a given circuit. It is the sum of delay time and rise (or fall) time.

Set-up Time is the time required for a capacitor-diode gate to open or close after a change of input level. This time is measured from the point of 10-percent input change.

INTEGRATING MODULES OF DIFFERENT FREQENCIES

No special interconnecting units are necessary for adjusting current and voltage when mixing units from different series. Timing characteristics, however, must accommodate the maximum speed of each series, and timing differences must be taken into account.

In the 10-megacycle lines, pulses are 40 nanoseconds wide and flip-flops have a built in delay of 30 to 75 nanoseconds. In the 5-megacycle lines, pulses are 70 nanoseconds wide and the built in flip-flop delay is 65 to 135 nanoseconds. The 500-kilocycle units use 400-nanosecond pulses; the buffered flip-flops have a delay of 0.5 to 1.3 microsecond.

Whenever it is desired to go from a higher speed unit to a lower speed unit, the pulse must be lengthened using a pulse amplifier with feedback. This method is illustrated in the technical descriptions of the pulse amplifiers.

In going from a lower speed series to a higher speed series, no changes in the pulse shape need to be made unless the long pulse is being used to complement a flip-flop or the pulse is being used to activate a unit which will be activated again while the longer pulse is still present. An example of this last case would be a counter made from 5-megacycle and 500-kilocycle equipment. It would be possible to use a 400-nanosecond pulse to clear all counter flip-flops provided that the first flip-flop would not be expected to count within 500 nanoseconds. When a narrower pulse is to be generated from a wide one, the wide pulse is applied to the input of a pulse amplifier of the higher speed series. The output of this pulse amplifier will be a standard pulse of the correct width.

A high speed flip-flop may not be changed and simultaneously sampled with a low speed pulse.

The unbuffered flip-flop packages and their associated capacitor-diode gate packages use a somewhat different method of timing than the buffered flip-flop packages. In the unbuffered units, the delay is contained in the capacitor-diode gates rather than in the flip-flops. Thus, if an unbuffered flip-flop is to be changed and sampled simultaneously, it must be sampled with a capacitor-diode gate rather than an inverter. Any of the negative capacitor-diode gates may be used to sample a 4000-series unbuffered flip-flop and drive a buffered flip-flop or other pulsed unit such as a pulse amplifier or delay unit. Feedback is recommended when the capacitor-diode-inverter is used to drive a Type 4603 Pulse Amplifier, particularly at high speeds.

No interconnecting units are used when going from a standard buffered flip-flop to an unbuffered flip-flop. However, it is necessary to make sure that all levels are present for the required amount of time before a sampling pulse arrives.

WIRING HINTS

When any type of system is being designed, consideration should be given to wiring techniques The space between connectors on all mounting panels must be kept open to allow air flow. This can be accomplished by running the ground wire from the top lug of the mounting panel to pin D, then to other ground pins on the socket, ending at the bottom ground lug. Any parts such as diodes or capacitors may be tucked into the space between connectors provided they use up no more than half the space.

All horizontal wires are run first, then the vertical wires are run outside the horizontal wires. In general, point-to-point wring should be used. When soldering is done on a mounting panel containing modules, a 6-volt (transformer) soldering iron should be used. A 110-volt soldering iron may damage the modules.

The recommended wire size is 22. Larger or smaller wire may be used depending on the number of connections to be made to each lug. Solid wire and a heat resistant spaghetti such as Teflon are easiest to use but are not mandatory.

Grounding the mounting panels together is extremely important. At least three points should be used as well as the regular power terminals. If more than one cabinet is used, cabinets should be bolted together and grounds interconnected horizontally, by at least one wire per mounting panel pair.

Pulse transmission is optimized by using a twisted pair of wires, one grounded at the first load. All pulse lines should be loaded with a shunt terminating resistor at the receiving end. The transmission line effect will cause the pulse amplitude to increase and a carbon resistor small enough to reduce the amplitude to 2.5 volts should be used. Lightly loaded 4000-series pulses may be successfully transmitted about two feet on a single wire; 1000-series pulses, about one foot; and 6000-series pulses, a few inches only.

Level transmission may be accomplished through a single wire if the wire is less than five feet for the 4000-series gates or buffered flip-flops, three feet for 1000-series modules or 4000-series unbuffered flip-flops, or one foot for 6000-series units. A series termination of about 100 ohms is recommended for longer lines. This successfully isolates the line capacitance but reduces driving capability. This loss in driving capability may usually be overcome by slight logic changes. Level transmission may also be accomplished using multi-conductor strip cable. If the length of the strip cable exceeds the lengths above, or for any length when unbuffered flip-flops are used, every other wire should be grounded to provide isolation. Long level transmission lines must not be bundled together. Unbuffered flip-flops can be set or cleared by the capacitive coupling of fast changes to their output leads.

The total current path from the pulse gate emitter to ground (including the path through level gates) should be as short as possible. The recommended maximum length is the same as unterminated pulse leads. If this path is closed to ground by a mechanical switch, the lead length may be longer. A 0.001 to 0.01 microfarad capacitor should be connected from the emitter to ground to isolate the lead inductance. The switch should be single-pole, double-throw with one side to ground and the other to −3 volts.

When the whole job is completed, loose vertical wires may be tied in bundles to make it all look neat.

MARGINAL CHECKING

Marginal checking is used in a system to find the margin of safety between the operating condition of a system and the point of failure. Marginal checking is normally used in routine maintenance to find deteriorating components before they can cause system failure. In many instances routine marginal checking is not necessary with long-life,

modern transistors, but it is invaluable in debugging a system. Marginal checking discovers those assembly mistakes which, while they do not cause noticeable failure, narrow the margin of satisfactory operation.

In systems made with DEC modules, the +10 volt bias on inverters is varied for marginal checking. In most modules, the +10 inputs are broken into two groups to make possible most critical marginal checking. In large systems, the +10 lines to the modules are broken down into several groups so that small portions of the system can be marginal checked at one time.

If the inverter transistor has marginal gain, it will fail when the +10 supply is increased less than 5 volts because the drive to the base of that transistor is lessened.

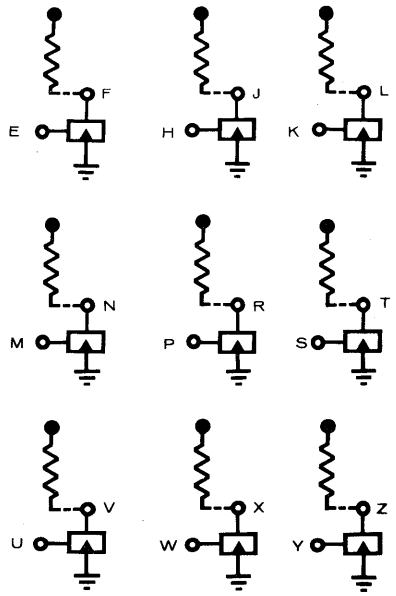
Reducing the positive bias on an inverter will detect noise on the inverter input or a condition where the input does not come sufficiently close to ground. Normal margins on a system are plus and minus 5 volts on the +10 volt supply.

INVERTERS

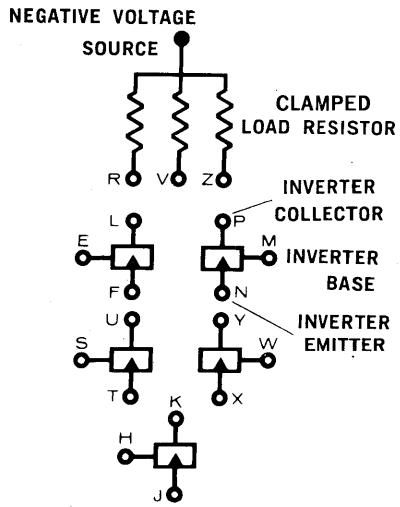
TYPES 4102, 4105, 4106

500 KILOCYCLES

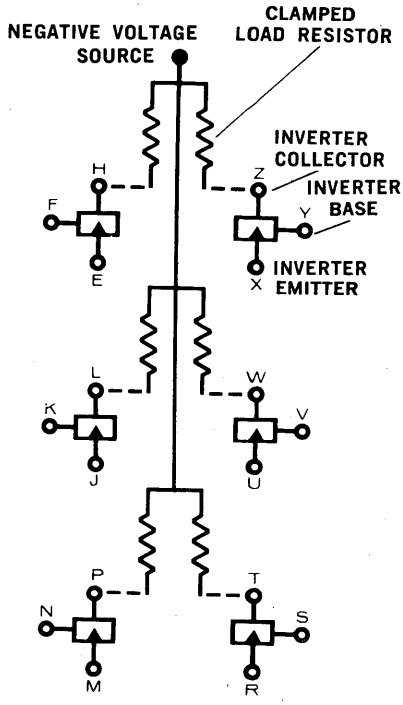
4000 SERIES



4102 INVERTER



4105 INVERTER



4106 INVERTER

The Types 4102, 4105, and 4106 contain transistor inverters for use as pulse or level gates. Each inverter is analogous to a switch. If —3 volts is applied to a base input, a conducting path is established between the emitter and the collector. If the base is brought to ground, the emitter-collector path is open. Delay through each inverter is approximately 0.3 microsecond.

The Type 4102 contains nine inverters with grounded emitters. Each inverter has a clamped load resistor which may be internally jumpered to the collector, if desired. The Type 4105 contains five inverters and three clamped load resistors. The Type 4106 contains six inverters, each with a clamped load resistor which may be internally jumpered to the inverter collector, if desired.

INPUT: Base — Inputs are DEC Standard 0.4 microsecond Negative Pulses when the inverter is used as a pulse gate at any frequency up to 500 kilocycles (1 unit of Pulse Load). Inputs are DEC Standard Levels or equivalent when the inverter is used as a level gate (1 unit of Base Load). **Emitter** — The inputs are DEC Standard Levels or equivalent, including grounding if emitter gating is not desired. If the collector is connected directly or through another inverter to a clamped load resistor, this input represents 1 unit of DC Emitter Load. If an emitter-collector path to a pulse gate exists, this input represents 1 unit of Pulsed Emitter Load.

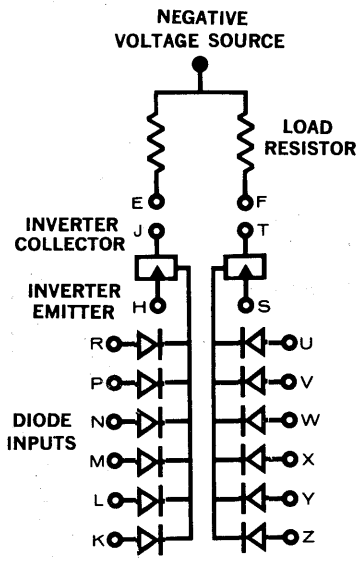
OUTPUT: The collector may be connected directly to a clamped load resistor, to the emitter of another inverter, or to the gated input terminal of the flip-flop or other unit being pulsed. When used as a level gate, a collector connected to a load resistor can simultaneously drive seven units of Base Load, one unit of DC Emitter Load, and any number of Pulsed Emitter Loads, providing not more than one is pulsed at a time (maximum nominal d-c collector current of 20 milliamperes). A collector with no clamped load resistor can be connected to several emitters simultaneously, providing not more than one of the inverters is conducting at a time. No more than three level gates can be connected in series. When a flip-flop drives the emitter of the first gate in the series string, the flip-flop must be counted as one of the inverters. When one of the series-connected gates is used as a pulse gate, four gates may be connected in series.

POWER: Type 4102: —15 volts/112 ma; +10 volts (A)/1.4 ma; +10 volts (B)/0 ma. **Type 4105:** —15 volts/52 ma; +10 volts (A)/0.5 ma; +10 volts (B)/0.3 ma. **Type 4106:** —15 volts/72 ma; +10 volts (A)/0.5 ma; +10 volts (B)/0.5 ma.

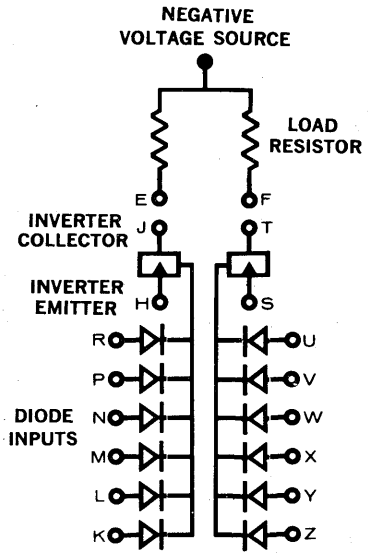
Additional information on 500-kilocycle inverter usage is included in Section 4.

DIODE GATES
TYPES 4110, 4111
500 KILOCYCLES

4000 SERIES



4110 NEGATIVE DIODE NOR



4111 POSITIVE DIODE NOR

Two six-input diode gates are OR circuits for negative level inputs and AND circuits for ground inputs. Each diode gate is connected to the base of a transistor inverter which is similar to those in the DEC Inverter Type 4106. The emitter and collector are available for external connections. Delay of a level through a diode and its inverter is approximately 0.4 microsecond. This unit may also be used for pulse mixing. Since it will widen pulses, it should not be used at the Complement input of a Type 4201 flip-flop.

INPUT: Diodes — The inputs are DEC Standard Levels or equivalent (2 units of Base Load shared among the negative inputs) or DEC 0.4 microsecond 2.5 volt Negative Pulses (1 unit of Pulse Load). **Emitter** — Same as 4106.

OUTPUT: Same as 4106.

POWER: −15 volts/42 ma; +10 volts (A)/0.9 ma; +10 volts (B)/0.9 ma.

The Type 4111, like the Type 4110, contains 2 six-input diode gates, each connected to the base of a transistor inverter; however, this unit is an OR circuit for ground level inputs and an AND circuit for negative level inputs. The diode inputs of this unit may not be used for gating pulses since the turn-on time for the transistor may be too long. The emitter and collector of each inverter are available for external connections. Delay of a level through a diode and its inverter is approximately 0.4 microsecond.

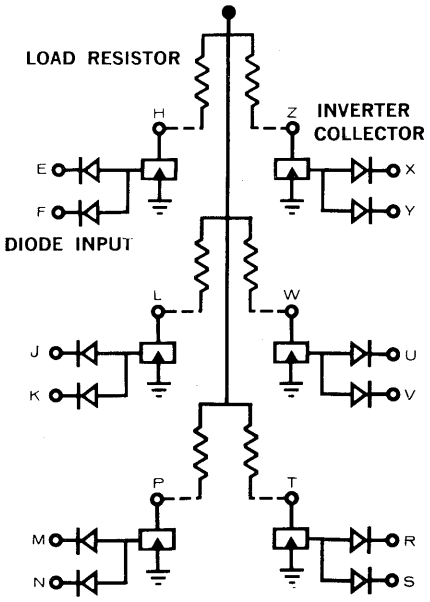
INPUT: Diodes — DEC Standard Levels or equivalent supply the input to the diodes; the load is ⅛ unit of DC Emitter Load, shared by the ground inputs. Emitter — Same as 4106.

OUTPUT: Same as 4106.

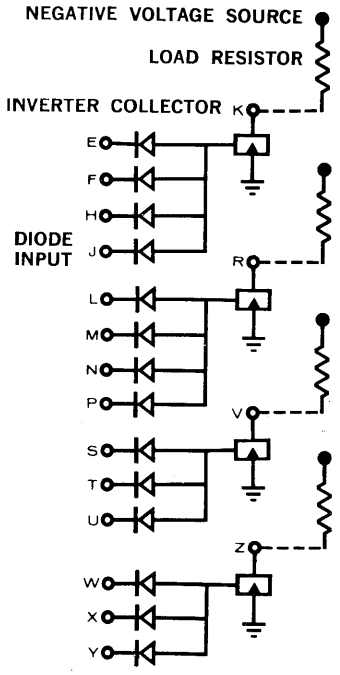
POWER: −15 volts/45 ma; +10 volts (A)/0.2 ma; +10 volts (B)/0.2 ma.

DIODE GATES
TYPES 4112, 4114, 4116, 4118
1 MEGACYCLE

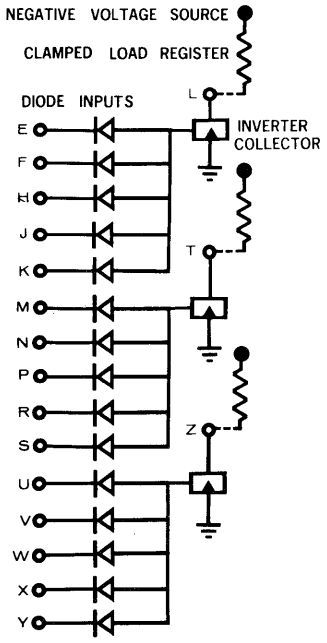
4000 SERIES



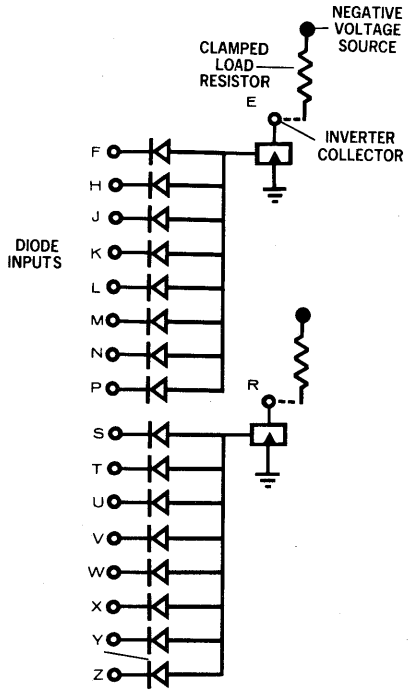
4112 NEGATIVE DIODE NOR



4114 NEGATIVE DIODE NOR



4116 NEGATIVE DIODE NOR



4118 NEGATIVE DIODE NOR

These modules are logically similar to Type 4110 and electrically faster. However, they cannot have as many level gates stacked in series with them. Typical total transition time for output rise is 0.07 microseconds; for output fall, 0.6 microseconds.

INPUT: Inputs may be pulses or levels. The d-c load presented by the input is one unit of Base Load shared among the negative inputs. The transient load presented to a pulse input is one unit of Pulse Load.

OUTPUT: Same as the Type 4105 except that the maximum series configuration is two level gates plus one pulse gate. The maximum d-c collector current is 15 milliamperes, and one-half unit of DC Emitter Load may be driven in addition to a clamped load resistor.

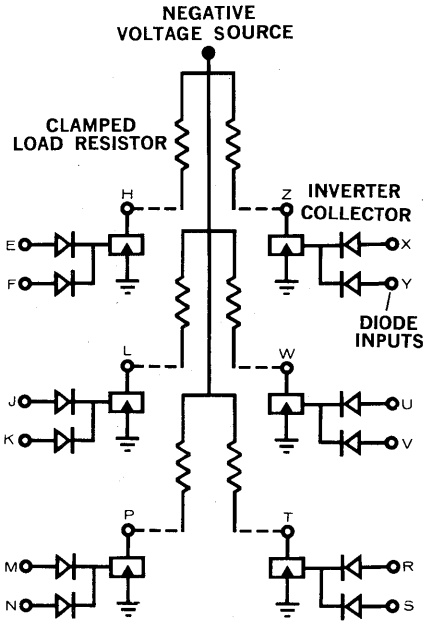
POWER: Type 4112: −15 volts/82 ma; +10 volts (A)/0.5 ma; +10 volts (B)/0.5 ma. **Type 4114:** −15 volts/62 ma; +10 volts (A)/0.35 ma; +10 volts (B)/0.35 ma. **Type 4116:** −15 volts/55 ma; +10 volts (A)/7.5 ma; +10 volts (B)/4.3 ma. **Type 4118:** −15 volts/35 ma; +10 volts (A)/2.5 ma; +10 volts (B)/2.7 ma.

DIODE GATES

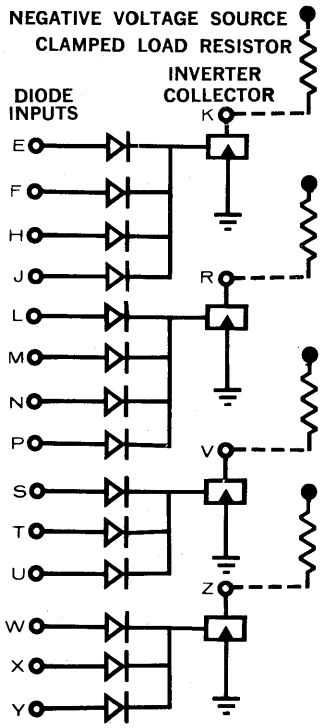
TYPES 4113, 4115, 4117, 4119

1 MEGACYCLE

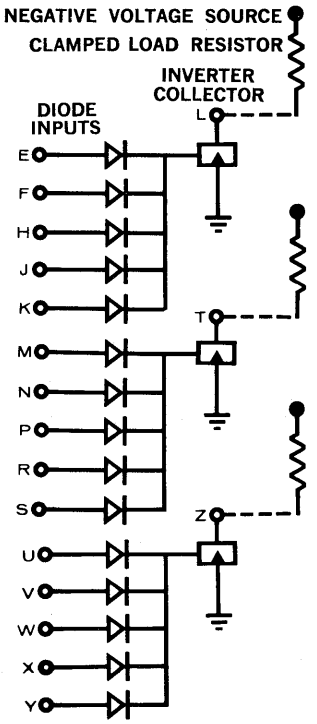
4000 SERIES



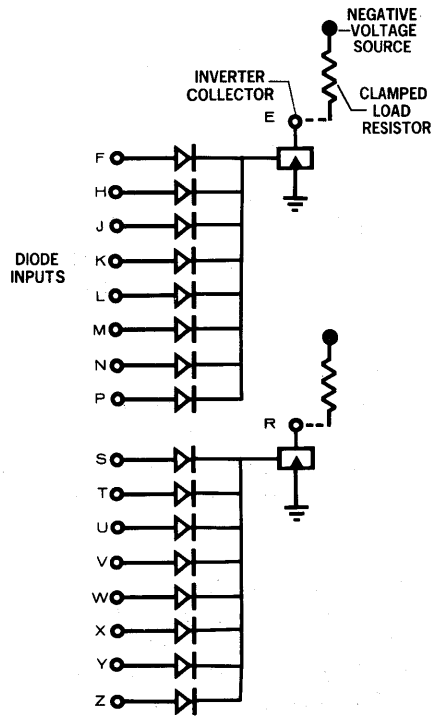
4113 POSITIVE DIODE NOR



4115 POSITIVE DIODE NOR



4117 POSITIVE DIODE NOR



4119 POSITIVE DIODE NOR

These units are logically similar to the Type 4111; however, since they are faster, they may also be used to AND a negative pulse with a group of negative levels. Typical total transition time for output rise is 0.13 microseconds; for output fall, 0.07 microseconds.

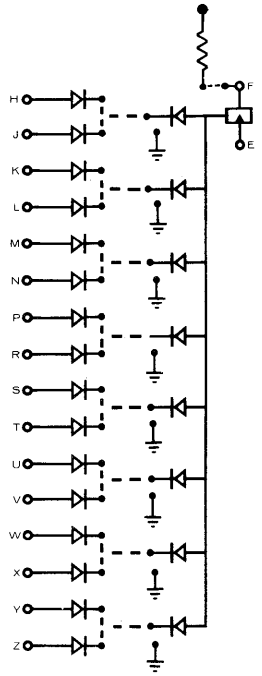
INPUT: DEC Standard Levels or DEC Standard 0.4 microsecond Pulses may be used for the inputs. The d-c load presented by the inputs is ⅛ unit of DC Emitter Load. This load is shared by those inputs which are at ground. The transient load presented to a pulse input is one unit of Pulse Load.

OUTPUT: Same as 4112.

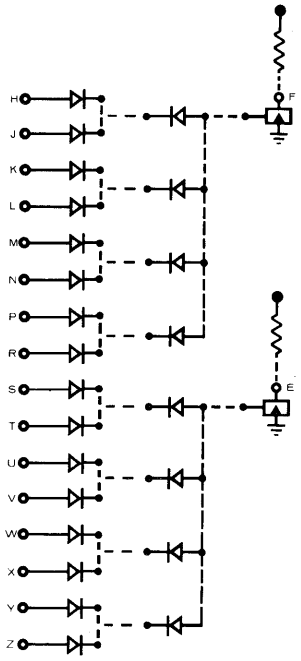
POWER: Type 4113: −15 volts/88 ma; +10 volts (A)/0.45 ma; +10 volts (B)/0.45 ma. **Type 4115:** −15 volts/67 ma; +10 volts (A)/0.3 ma; +10 volts (B)/0.3 ma. **Type 4117:** −15 volts/55 ma; +10 volts (A)/0.3 ma; +10 volts (B)/0.15 ma. **Type 4119:** −15 volts/45 ma; +10 volts (A)/0.2 ma; +10 volts (B)/0.2 ma.

DIODE GATES
TYPES 4141, 4143
500 KILOCYCLES

4000 SERIES



4141 NEGATIVE AND-NOR GATES



4143 NEGATIVE AND-NOR GATES

The Types 4141 and 4143 Gates perform two levels of logic within one circuit. Internal jumpers allow different combinations of logical functions to be implemented. When shipped, the module jumpers are connected as shown by the dotted lines on the logic diagram. For negative input signals, the first level of logic is an AND and the second level of logic is a NOR. For ground input signals the functions are reversed.

A large variety of different uses are possible. For example, the Type 4141, when connected as shown, will compare two 4-bit flip-flop registers for equality. When the Type 4141 is connected as four 3-input AND gates OR'ed together, it determines the parity of three binary bits. If all the input diodes are connected to a single second-stage diode, then the unit will form a 16-input AND gate.

Back-to-back diode circuits are possible because of an internal bias resistor connected to the input of each second-stage diode. This bias holds the input of the second-stage diode at −3 volts unless there is a ground or internal connection from a first-stage diode. Typical total transition time with one active second-stage diode is 0.2 microseconds for output rise, and 0.5 microseconds for output fall. This unit may not be used for gating pulses. When more than one second-stage diode is active, the output fall time becomes longer.

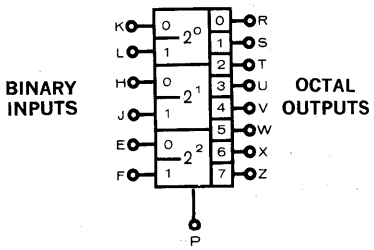
INPUT: DEC Standard Levels or equivalent. The input loading is determined by the bias resistor on the second-stage diode. This load (⅛ unit of DC Emitter Load) is shared by all first-stage inputs connected to this point. All second-stage diodes not in use should be grounded.

OUTPUT: Same as Type 4112.

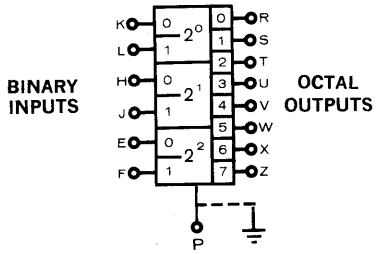
POWER: Type 4139: −15 volts/42 ma; +10 volts (A)/0.3 ma; +10 volts (B)/0 ma. **Type 4141:** −15 volts/42 ma; +10 volts (A)/0.3 ma; +10 volts (B)/0 ma. **Type 4143:** −15 volts 50/ma; +10 volts (A)/0.3 ma; +10 volts (B)/0.3 ma.

DECODERS
TYPES 4150, 4151
500 KILOCYCLES

4000 SERIES



4150 BINARY-TO-OCTAL DECODER



4151 BINARY-TO-OCTAL DECODER

These modules decode binary information from three flip-flops into octal form. For the Type 4150 the selected output line is at —3 volts and the other seven outputs are at ground. For the Type 4151 the selected output line is at ground while the other seven outputs are at —3 volts. If the gate signal is negative, all lines will be inhibited. Decoding is accomplished with eight diode gates arranged so that each gate has a unique set of inputs. For the Type 4150 the gates are similar to those of the Type 4110. For the Type 4151 the diode gates are similar to those in the Type 1111. For both modules total transition time is less than 0.9 microseconds.

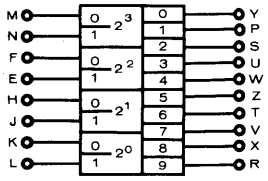
INPUT: Type 4150: Standard Levels or equivalent drive the decoder, which represents five units of Base Load. If inputs L, J, F, and P are at ground, output R is selected and is at —3 volts. The gate input represents five units of Base Load. **Type 4151:** DEC Standard Levels or equivalent drive the decoder, which represents 0.3 units of DC Emitter Load. The gate input is internally jumpered to ground when the unit is shipped. If this jumper is removed, pin P becomes a common gate for all outputs with a —3 volt signal for inhibit. The load of the gate is one unit of DC Emitter Load. If inputs K, H, and E are at —3 volts and pin P is at ground, then output R is selected and is at ground.

OUTPUT: Each output is similar to the collector of a Type 4106 inverter. Clamped load resistors are internally jumpered to all outputs and may be clipped out if desired. Outputs can be connected in series or parallel arrangements as with the Type 4106 Inverters. In the Type 4151 the gate inputs for all the output transistors are emitters; thus if gating is done on this terminal, it must be counted as part of the series string of inverters.

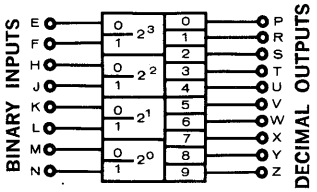
POWER: Type 4150: —15 volts/100 ma; +10 volts (A)/4.4 ma; +10 volts (B)/3 ma. **Type 4151:** —15 volts/103 ma; +10 volts (A)/0.9 ma; +10 volts (B)/0 ma.

DECODERS
TYPE 4161
500 KILOCYCLES

4000 SERIES



4161 AS AN EXCESS 3 DECODER



4161 AS AN 8-4-2-1 DECODER

The Type 4161 Binary-Coded Decimal-to-Decimal Decoder is a diode matrix which decodes four complementary pairs of BCD input signals to produce an output on a selected decimal line. The ground-level output signal is produced from input signals in the 8-4-2-1 or excess 3 codes in which the binary ONE is represented by −3 volts and ZERO is ground potential. Total transition time, to raise a selected output line to ground level and return the 9 other output lines to −3 volts, is 1000 nanoseconds.

Each diode negative AND gate is followed by a transistor inverter. Each of the 10 inverters is provided with a clamped load resistor which can be disconnected by removing a jumper wire. Although designed to decode the 8-4-2-1 or excess 3 BCD code, the Type 4161 can be used with other codes which require the following logic:

P = EHKM	V = JKN
R = EHKN	W = EJLM
S = HLM	X = JLN
T = HLN	Y = FM
U = JKM	Z = FHKN

INPUT: Standard DEC Levels, or equivalent, drive the decoder which represents 0.28 unit of DC Emitter Load per input (2.8 ma at ground, no load at −3 volts).

OUTPUT: Each output is a standard inverter collector similar to the 4106. Clamped load resistors are internally jumpered to all outputs and may be clipped out if desired. Outputs can be connected in series and parallel arrangements as with the 4106.

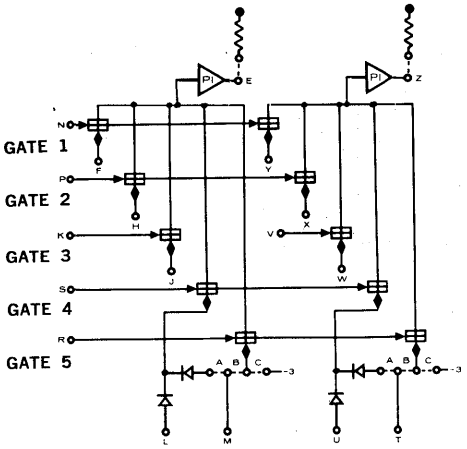
POWER: −15 volts/110 ma; +10 volts (A)/0 ma; +10 volts (B)/2 ma.

CAPACITOR-DIODE GATES

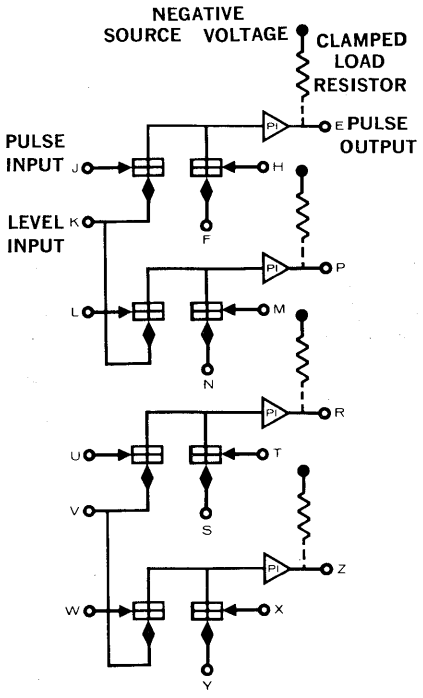
TYPES 4123, 4125, 4127, 4129, 1011

1 MEGACYCLE

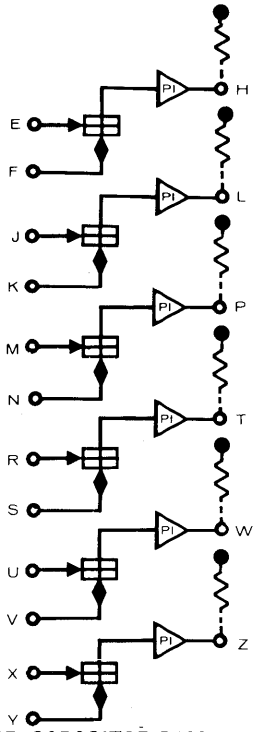
4000 SERIES



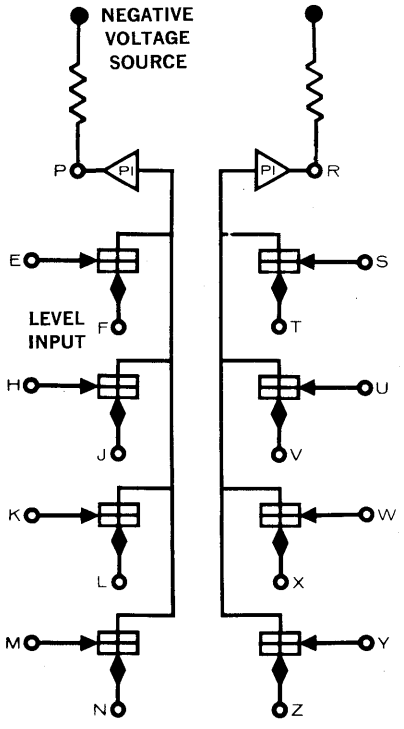
4123 CAPACITOR-DIODE GATE



4125 CAPACITOR-DIODE GATE



4127 CAPACITOR-DIODE GATE



4129 CAPACITOR-DIODE GATE

The negative capacitor-diode gates contained in the Types 4123, 4125, 4127, and 4129 have a capacitor-resistor-diode circuit on the input and a standard DEC Inverter on the output for high driving capability. A clamped load resistor may be internally jumpered to each output.

Capacitor-diode gates will provide a logical delay for sampling a changing level and also differentiate a changing level to produce a pulse. When a changing level is to be differentiated, it is applied to the pulse input. If a level is to be pulse sampled at a time when it may be in the process of changing, it is applied to the conditioning level input. Since the internal capacitor will not discharge as fast as the level input will change, the output will be conditioned by the state of the level before the change occurred. The level set-up time required for negative capacitor-diode gate is one microsecond, hence, the maximum prf is 1 megacycle.

The Type 4123 is frequently used to provide the gating for an accumulator register or to allow read-in to a flip-flop from five sources. Lugs are provided to modify the level inputs on gates 4 and 5 depending on the application used. Jumpers A and C are normally installed when the Type 4123 is used to control the complement input to an accumulator flip-flop. Gate 4 then implements the half-add function while gate 5 is used to complement the accumulator. Jumper B is normally installed when the

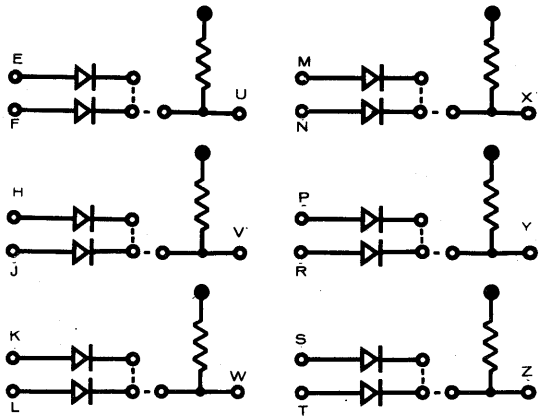
Type 4123 is used to read-in inputs from five sources.

The Type 4125 is frequently used with the Type 4215 or the Type 4217 Quadruple Flip-Flop modules to form four bits of an up-down counter. The Type 4127 is useful in control or other applications where individual gates are required. The Type 4129 is used to read into a flip-flop from four sources.

INPUT: Level: Inputs are DEC Standard Levels of 0 and −3 volts. The gate is enabled by a negative level, present at least one microsecond before the gate is pulsed. There is no d-c load at the level input; the transient load is two units of Base Load or ¼ unit of DC Emitter Load, depending on the direction of the level change. (Note that two gates are driven from pins K and V of Type 4125). **Pulse:** The pulse input (one unit of Pulse Load) may be driven by a DEC Standard 0.4-microsecond Negative Pulse or by a negative-going level change. The level change should be 2.5 to 3.3 volts with a maximum fall time of 0.5 microseconds. When the pulse input is driven from the level output of a 4000-series flip-flop or gate package, the source should be limited to approximately ¼ the normal allowable Base and/or Transient Loads in order to provide the necessary fall time. Fractional Emitter Loads (such as the Type 4113) increase the speed of the driving source hence the full amount of emitter loading may be used.

OUTPUT: The output is similar to that of the Type 4112 diode gate when it is used as a pulse gate. It may drive one unit of Pulse Load. However, because the capacitor-diode gate output pulse is somewhat narrower than the normal 4112 output pulse, it should not be used to drive the complement input of the Type 4201 Flip-Flop, the input of the Type 4410 Pulse Generator, or the input of a non-standardizing pulse amplifier such as the Type 4603 or 4605.

POWER: Type 4123: −15 volts/42 ma; +10 volts (A)/0.5 ma; +10 volts (B)/0.5 ma. **Type 4125:** −15 volts/62 ma; +10 volts (A)/0.3 ma; +10 volts (B)/0.3 ma. **Type 4127:** −15 volts/82 ma; +10 volts (A)/1.2 ma; +10 volts (B)/1.2 ma. **Type 4129:** −15 volts/42 ma; +10 volts (A)/1.2 ma; +10 volts (B)/1.2 ma.



1011 DIODE

The Type 1011 contains diodes which can be used to gate multiple inputs into the level input of a negative capacitor-diode gate. The diodes form an AND circuit for negative inputs and an OR circuit for positive inputs.

The Type 1011 contains 12 input diodes and 6 clamped load resistors. When the module is shipped, these are wired as six 2-input gates but internal lugs permit other arrangements. There is no restriction on the number of diodes which can be connected to a clamped load resistor. Inverters are not included.

INPUT: Diode inputs should be DEC Standard Levels or equivalent. The load is ¼ of a standard DC Emitter Load for each clamped load resistor plus the load of the capacitor-diode level input. This load is shared among the positive inputs.

OUTPUT: The output is 0.5 volts more positive than the most positive input. It may be used to drive the level input of a single negative capacitor-diode gate.

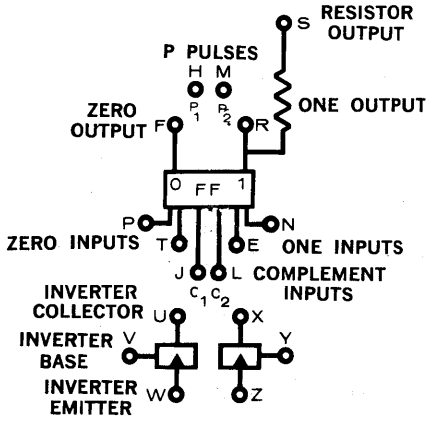
POWER: −15 volts/14 ma; +10 volts (A)/1 ma; +10 volts (B)/0 ma.

BUFFERED FLIP-FLOPS

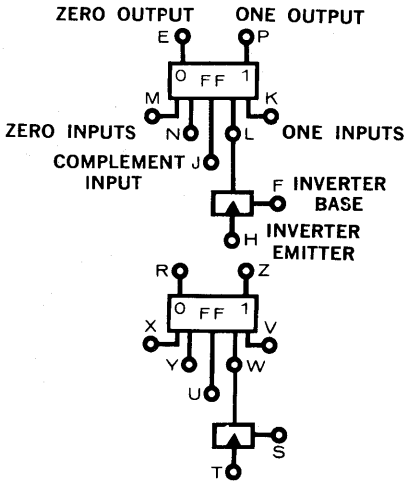
TYPES 4201, 4202, 4209

500 KILOCYCLES

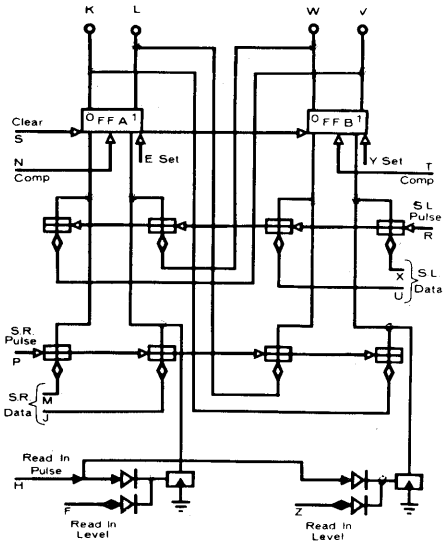
4000 SERIES



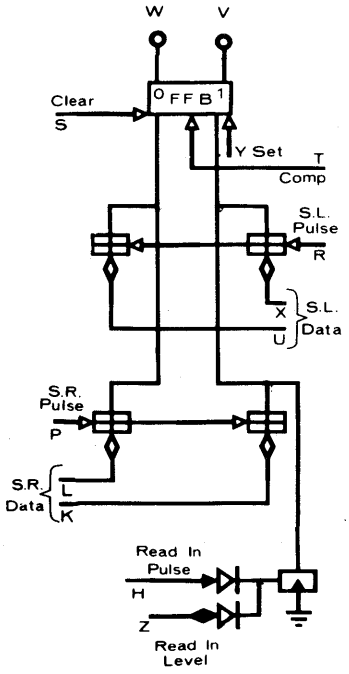
4201 FLIP-FLOP



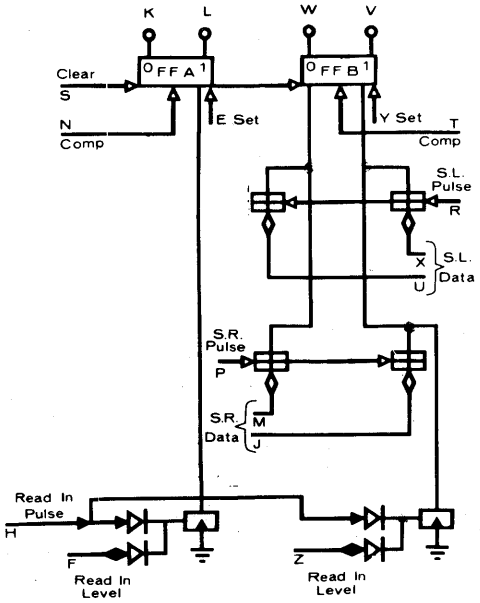
4209 DUAL FLIP-FLOP



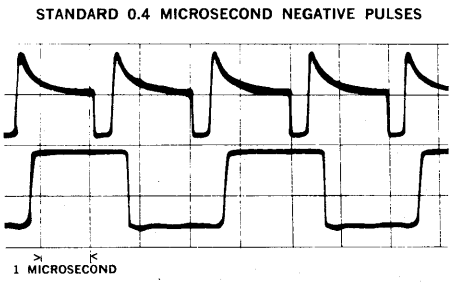
4202 DUAL FLIP-FLOP



4202A



4202B



BUFFERED FLIP-FLOP OUTPUT

The 4000-series buffered flip-flops have high output driving capabilities and are particularly useful in test setups. They may be quickly and easily patched together with a minimum of restrictions on lead lengths or load driving capability.

The Type 4201, the most general purpose flip-flop of this group, may be used in all applications. The two complement input terminals and P-pulse output terminals are useful in counter and adder applications. The module also contains two independent inverters for use as pulse or level gates.

The Type 4202 is a more specialized dual flip-flop module with built-in gates for bi-directional shifting, complementing, and read-in from external sources. This unit is often used in serial arithmetic units, shift registers, and serial-parallel converters. Two variations, the Type 4202A and the Type 4202B, are available for use when special logic is required for the sign bit. The built-in diode gates are similar to the Type 4113.

Type 4209 is a general purpose set-reset flip-flop which can be used in shift register, buffer register, or general purpose control applications. A complement input is also available, but, like the 4202, there are no provisions for carry output signals. The built-in inverters are similar to Type 4106.

INPUT: The ZERO, ONE, complement, and shift inputs may be treated either as gated or as direct inputs. However, a single terminal may not be used for both. When used as a gated input terminal, the input signal must come from the collector of one or more pulse gates. The base of the pulse gate must be driven by a Standard 0.4-microsecond Negative Pulse or equivalent. When an input is treated as a direct input, it must be driven by a Standard 0.4-microsecond Positive Pulse (such as obtained from the output of a pulse amplifier). All inputs are one unit of pulse load except the 4202 Shift Terminals which are two units of Pulse Load each.

The Type 4202 set input (one unit of Pulse Load) and clear input (two units of Pulse Load) are direct positive inputs and may be driven by Standard 0.4-microsecond Positive Pulses only. The read-in levels for the Type 4202 must be Standard Levels or equivalent, with −3 volts for assertion. The load presented by each input is ⅛ of a DC Emitter Load.

Type 4202 shift left and shift right data inputs are 1500-ohm capacitor-diode gate levels similar to the Type 4127 except that zero volts represents the assertion level. Each pair of inputs must receive complementary levels which must be present at least one microsecond before the corresponding shift pulse.

OUTPUT: The flip-flop level outputs have built-in delays which are greater than the input pulse width; thus an output can be sensed reliably by an inverter or diode gate at the same time as the input is being pulsed. The maximum total transition time is 1.4 microseconds. The ZERO and ONE outputs provide Standard Levels, each capable of simultaneously driving 14 units of Base Load, 1.4 units of DC Emitter Load, and any number of Pulse Emitter Loads, providing not more than one is pulsed at a time. The resistor coupled output is suitable for driving one indicator driver input.

Each time the C_1 (or C_2) terminal on the Type 4201 is pulsed, a Standard 0.4-microsecond Negative Pulse will occur at the P_1 (or P_2) terminal. This pulse is capable of driving one unit of Pulse Load. The carry propagate time (through an inverter, complement input, and P-pulse output) is 0.05 microseconds per bit.

POWER: Type 4201: −15 volts/90 ma; +10 volts (A)/0.6 ma; +10 volts (B)/0.6 ma. **Type 4202:** −15 volts/120 ma; +10 volts (A)/1.2 ma; +10 volts (B)/1.2 ma. **Type 4209:** −15 volts/120 ma; +10 volts (A)/1.2 ma; +10 volts (B)/1.2 ma.

GENERAL INFORMATION
UNBUFFERED FLIP-FLOPS

4000 SERIES

The 19 types of unbuffered flip-flop modules available for building economical systems may be grouped roughly in the categories of general purpose, special purpose, and special application.

General purpose modules contain independent flip-flops with both output terminals available. Since these units can be set or cleared through their outputs, gates may be added for performing any logical function. Some of the general purpose flip-flops listed below have built-in complement terminals for counting and adding applications.

4214	Four set-reset flip-flops, no gates.
4215	Four complement flip-flops, gates for special counts.
4217	Four complement flip-flops, gates for read-in.
4218	Four set-reset flip-flops, gates for jam or shift.
4224	Nine set-reset flip-flops, no gates.
4227	Eight set-reset flip-flops, two clear busses, no gates.

Special purpose modules are preconnected for commonly used functions such as counting, shifting, and buffering. Most units have only one output terminal available. This may be selected to be either the ZERO or ONE terminal by means of internal jumpers. If the ZERO terminal is selected, external gates may be connected for additional read-in from other sources. Special purpose modules include the following.

4216	Four-bit shift register with read-in gate, other functions with external gates.
4219	Five-bit jam buffer.
4220	Eight-bit buffer.
4221	Six-bit shift register with read-in gates.
4222	Seven-bit binary counter with read-in gates.
4223	Ten-bit shift register.
4225	Eight-bit binary or BCD counter.
4231	Four-bit bi-directional shift register with read-in gates, other functions with external gates.

Modules designed for a specific application include units for analog-digital conversion, transfer of information between asynchronous devices, relay driving registers, multiple read-in buffers, and serial accumulators.

4204	Two-bit counter with three sets of read-in gates and high output driving ability.*

*The 4204 and 4205 have output amplifiers, but have delays that are short compared to the pulse width, so that the timing restrictions are similar to those of the other 1-megacycle flip-flops described here.

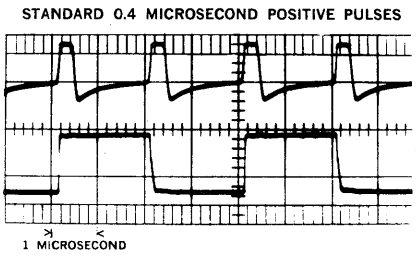
4205	Two-bit counter and bi-directional shift register with high output driving ability.
4226	Four-bit buffer with 4-bit control register for use in successive approximation analog-to-digital converters.
4228	Three-bit shift register with 3-bit buffer for transferring information between asynchronous devices.
4290	Eight-bit buffer with outputs for driving solenoids and/or indicators only.

The 4000-series unbuffered flip-flops described in this section will operate at frequencies up to one megacycle. The total transition time for the flip-flop output is 180 nanoseconds when unloaded. The carry propagate time when connected as a counter is 50 nanoseconds per bit. (These times do not apply to the 4204, 4205, 4228, or 4290.)

INPUT INFORMATION

The read-in and shift inputs are Standard 0.4-microsecond Negative Pulses. Each input represents one unit of Pulse Load. The complement input may be a Standard 0.4-microsecond Positive Pulse, a positive-going pulse from an inverter or capacitor-diode gate or a positive step of three volts with a less than 0.2-microsecond rise time. Flip-flops will not complement on negative steps. The load is one unit of Pulse Load or one unit of 1-megacycle Base Load.

The clear (or preset) input for set-reset flip-flops should be Standard 0.4-microsecond Pulse. If the clear input goes directly to the flip-flops, the pulse should be positive and load is one unit of Pulse Load per flip-flop. If the input goes to a pulse inverter, the clear signal should be a negative pulse and the load is one unit of Pulse Load per inverter.



UNBUFFERED FLIP-FLOP OUTPUT

The clear (or preset) input for complementing flip-flops is normally a 1-microsecond pulse such as produced by the Type 4604 Pulse Amplifier. This long clear signal is used to override carries which would otherwise be generated from one stage to another. (If carries are inhibited or not connected, then complementing flip-flop clear terminals may be treated as set-reset clear terminals.) If the input goes directly to the flip-flop, the pulse should be a 2.5-volt positive pulse and the load is one unit of Pulse Load per flip-flop. If the clear signal goes to a pulse inverter, the input signal should be a 2.5-volt negative pulse and the load is one unit of Pulse Load per pulse inverter.

Capacitor-diode gate level inputs are Standard Levels or equivalent, with ground representing the assertion level. There is no d-c load at these points. If information is being shifted or jammed into the flip-flop (Figure 1), the levels must be present 1 or 1.5* microseconds before the shift or jam operation takes place. When the gate is being used for read-in of one line only (Figure 2), then the level must be present 1 or 1.5* microseconds to enable and 2 or 3* microseconds to disable. Thus, if the level lines are changing, the full disable time must be allowed before pulsing the line. However, if the lines are normally disabled they may be brought to the enable level just 1 or 1.5* microseconds before pulsing. Unused inputs should be inhibited.

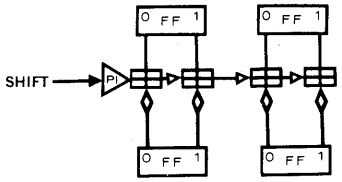


Figure 1 SHIFT OR JAM TRANSFER

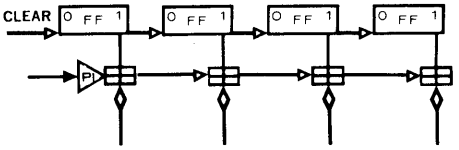


Figure 2 SINGLE LINE READ IN

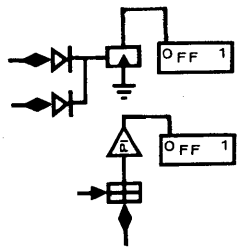


Figure 3 SETTING A FLIP-FLOP BY GROUNDING ITS ZERO OUTPUT

Flip-flops may be set or cleared by connecting a negative diode NAND or a negative capacitor-diode gate to the appropriate output terminal (Figure 3). The gate will then be turned on by the coincidence of two negative levels or a negative level and a Standard 0.4-microsecond Negative Pulse. Negative capacitor-diode gates such as the Type 4127 may be used for this purpose. An inverter may be used only if the emitter is tied directly to ground (not gated). If the flip-flops are directly connected as a counter, this technique can be used for setting only. For clearing or jam transferring a diode gate (such as the Type 4113) or an inverter must be used and the input pulse must be one microsecond to inhibit carries.

OUTPUT INFORMATION

TYPICAL APPLICATIONS

Figure 4 illustrates how pulse sampling of an unbuffered flip-flop is performed with a negative capacitor-diode gate. The unit being sampled is assumed to be a Type 4216 Shift Register and the sampling pulse is the same pulse that is used in shifting the register. The set-up time of the capacitor-diode gates assures that the output signal will not be split by a change in the conditioning level while it is being sampled.

*See individual module descriptions.

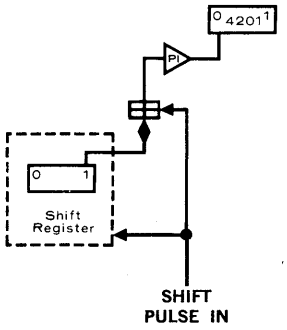


Figure 4

LOADING RULES

At 500 kilocycles a set-reset flip-flop can drive four units of Base Load, a half unit of DC Emitter Load and eight units of Transient Load. At frequencies above 500 kilocycles the total Base Load plus Transient Load cannot exceed nine units.

At 500 kilocycles a flip-flop with a complement input can drive four units of Base Load, a half unit of Emitter Load, and five units Transient Load. At frequencies above 500 kilocycles the total base and transient load must not exceed six units.

Loading of the ZERO and ONE outputs is independent. When an output is used to drive an inverter base, the emitter of that inverter must be grounded. If the flip-flop output has loads connected within the module, these loads must be counted in determining the maximum load driving capability.

The input load is included in the description of each module. Transient loads apply only to unbuffered flip-flops hence are not listed with the module description. The table following shows the equivalent transient load that each type of input represents; this load is in addition to its normal d-c input load.

DC Load	**Additional Transient Load**
Capacitor-diode gate level input	2.2
500-kc base	2.7
1-mc base or flip-flop complement input	1.2
5-mc base	0.7
10-mc base	0.3
Fractional emitter (such as 4113)	0
Indicator driver input	0.3
Inverter collector	0.3
Leads over one foot* (assuming negligible coupling to other signal lines)	0.2/ft.

The following are some examples of how the load driving ability is calculated for different modules:

*For long leads a series 100-ohm resistor should be used at the flip-flop output.

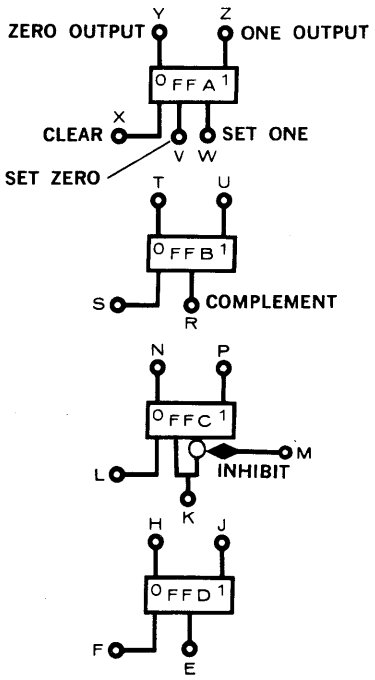
1. A 4216 with an internally connected capacitor diode gate can drive two additional capacitor-diode gate level inputs and two 5-megacycle Base Loads (transient limit) at 500 kilocycles.
2. A 4222 complementing with an internal complement load can also drive three units of 10-megacycle base load and four inputs to 4113 diode gates (d-c limit).
3. A 4222 with an internally connected complement load can drive one 500-kilocycle, one 5-megacycle and one 10-megacycle base at 500 kilocycles (transient limit).
4. A 4214 can drive four 10-megacycle bases (d-c limit) and four inputs to 4113 diode gates, (d-c limit).
5. A 4214 can drive three capacitor-diode gate level inputs and two 5-megacycle base loads (transient limit) at 500 kilocycles.

UNBUFFERED FLIP-FLOPS

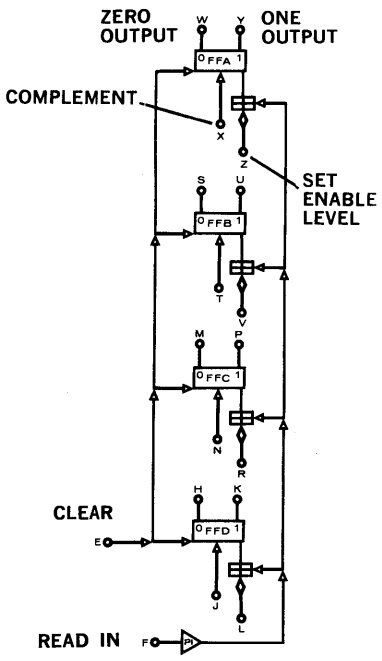
TYPES 4215, 4217

1 MEGACYCLE

4000 SERIES



4215 COMPLEMENTING FLIP-FLOPS



4217 COMPLEMENTING FLIP-FLOPS

The Types 4215 and 4217 Quadruple Flip-Flops can be used in any flip-flop application, but are particularly useful in counters, accumulators, or applications where one of these functions will be combined with other functions.

The Type 4215 contains four independent flip-flops. Special built-in gates allow all counts from 1 to 12 (except 7 and 11) to be implemented without additional logic. Many of the uses of this module are described in Section 3.

The Type 4217 contains four flip-flops which are independent except for the common clear and read-in logic. This module is particularly useful for straight binary counting with external read-in of ONE's and for accumulator registers.

INPUT: Same as described on page 6.13 except for the special gates on the Type 4215. The 4215 set ZERO and set ONE gates to flip-flop A require the same signals as for a complement. The set ZERO will operate only when flip-flop A is in the ONE state and set ONE will operate only when flip-flop A is in the ZERO state. Thus a complement input terminal may be formed by connecting the set ZERO and set ONE terminals together. The load for either or both terminals is the same as a normal complement load.

If the 4215 inhibit terminal is at ground, flip-flop C will complement normally. If the inhibit terminal is negative, flip-flop C will not complement from the ZERO to the ONE state. However, it will complement in the other direction. This input terminal is similar to a capacitor-diode gate and the level must be set up for two microseconds before the complement signal is received. The load presented by this input is two units of DC Base Load and 0.6 of a unit of transient load. (See page 6.15.)

OUTPUT: Same as described for complementing flip-flops on page 6.15, except for pin P of the Type 4215. This terminal, the ONE output of flip-flop C is normally connected internally to part of the inhibit circuit which reduces its d-c load driving capability by two units of Base Load and 0.6 of a unit of transient load. If the inhibit feature is not desired, it may be removed by means of internal jumpers on the board, so that pin P may drive the same load as other flip-flop outputs. The module is shipped with the inhibit feature installed. There are 3 lugs in row on the board. To remove the inhibit feature, cut the jumper between the center lug and the lug nearest the plug and install a jumper between the center lug and the lug farthest from the plug.

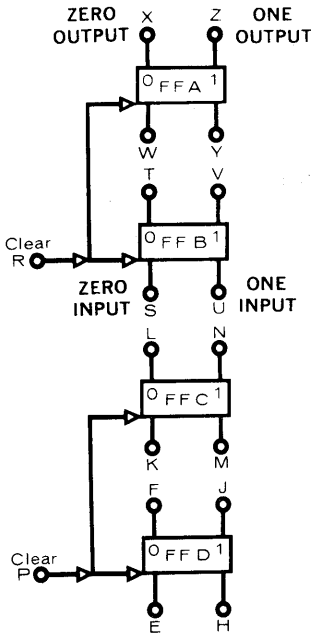
POWER: Type 4215: −15 volts/94 ma; +10 volts (A)/0.6 ma; +10 volts (B)/0.6 ma. **Type 4217:** −15 volts/95 ma; +10 volts (A)/0.6 ma; +10 volts (B)/0.6 ma.

UNBUFFERED FLIP-FLOPS

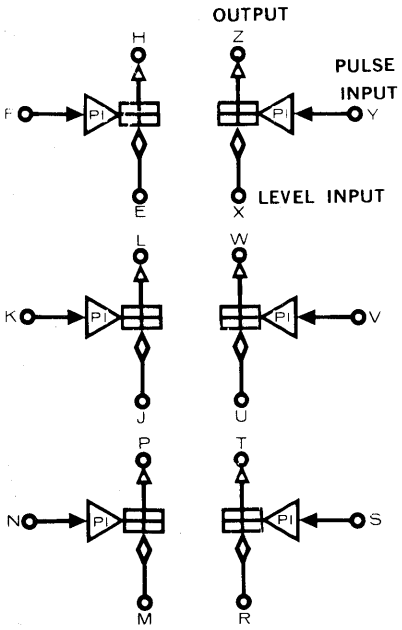
TYPE 4214 WITH TYPES 4126, 4128 GATES

1 MEGACYCLE

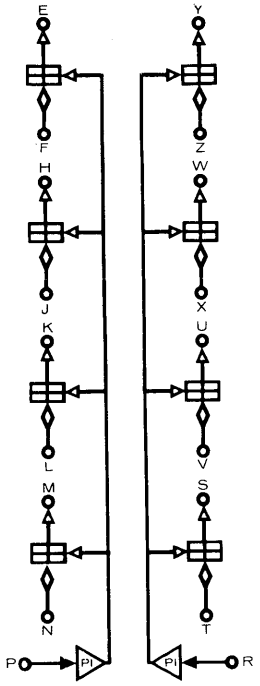
4000 SERIES



4214 SET-RESET FLIP-FLOPS



4126 CAPACITOR-DIODE GATE



4128 CAPACITOR-DIODE GATE

The Type 4214 module contains quadruple, general purpose, set-reset flip-flops. These may be set and reset through the input terminals by means of special gates which are available in two separate module packages, the Type 4126 and the Type 4128. (The maximum prf in this case is 600 kilocycles.) The flip-flop may also be set and reset through the output terminals. (The maximum prf in this case is one megacycle.)

Since the flip-flops in the 4214 are completely independent (except for common clear which connects two flip-flops) they are particularly useful for control applications and/or extending the range of the standard 4- to 10-bit modules.

The capacitor-diode gate modules are logically similar to other capacitor-diode gates except that the output is a 3-volt positive-going signal referenced to ground which should be used only for driving the ONE and ZERO inputs on the 4214.

The Type 4126 Capacitor-Diode Gate provides six completely independent gate circuits for reading into the 4214. The Type 4128 provides economical gates for reading or shifting into flip-flops.

INPUT: The clear inputs on the Type 4214 and the pulse inverter inputs on the Types 4126 and 4128 are as described on page 6.13. The 4214 may also be set or cleared through the output terminals as described on page 6.13. The ZERO and ONE inputs on the 4214 may be driven only from the outputs of Types 4126 and 4128 Capacitor-Diode Gates or Standard 0.4-microsecond Positive Pulses.

The level inputs for the 4126 and 4128 are ground for assertion and normally must be present at least three microseconds before the unit is pulsed. If information is being jammed or shifted into the flip-flop with a pair of complementary levels, it may be present only 1.5 microseconds before the pulse. The load is the same as the level input of the capacitor-diode gate described on page 6.15.

OUTPUT: Type 4214 outputs are the same as those described on page 6.15. The outputs of the capacitor-diode gates are positive-going pulses from ground similar to Standard 0.4-microsecond Positive Pulses but with no overshoot. Each output will drive one input to a Type 4214. Many such gates may be OR'ed together by tying them to the same input.

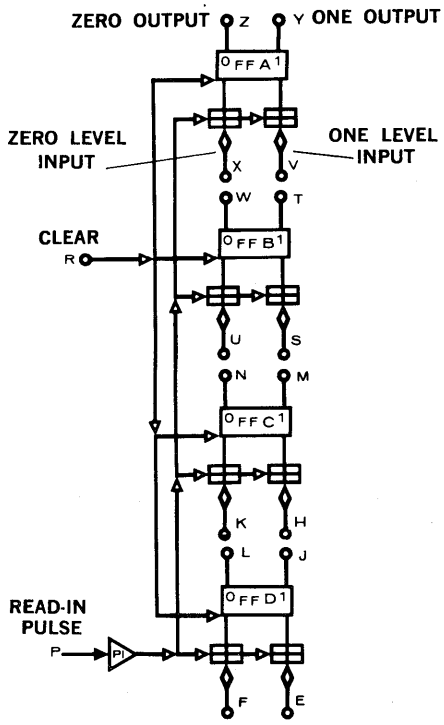
POWER: Type 4126: −15 volts/60 ma; +10 volts (A)/0.45 ma; +10 volts (B)/0.45 ma. **Type 4128:** −15 volts/35 ma; +10 volts (A)/0.3 ma; +10 volts (B)/0 ma. **Type 4214:** −15 volts/93 ma; +10 volts (A)/0.6 ma; +10 volts (B)/0.6 ma.

UNBUFFERED FLIP-FLOPS

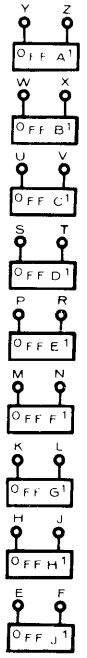
TYPES 4218, 4224, 4227

1 MEGACYCLE

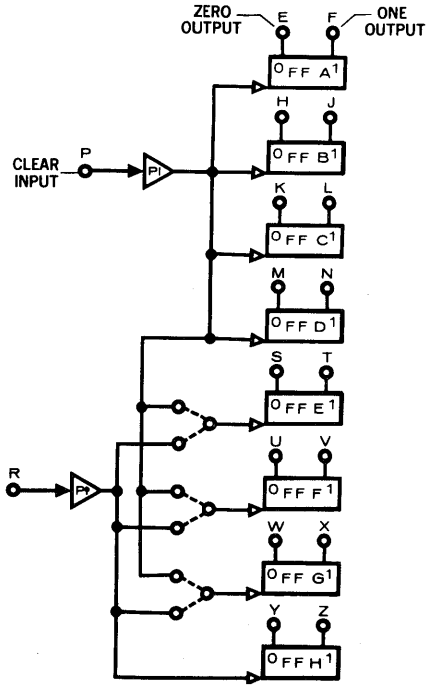
4000 SERIES



4218 SET-RESET FLIP-FLOPS



4224 SET-RESET FLIP-FLOPS



4227 SET-RESET FLIP-FLOPS

The 4218, 4224, and 4227 contain independent flip-flops for use in general set-reset applications. The Type 4218 contains four flip-flops with associated gates for connection as a shift register or jam transfer buffer. The gates are preconnected. The Type 4224 contains nine flip-flops which are set and cleared through the output terminals.

The 4227 contains eight independent flip-flops plus two pulse inverters for clearing. The clear inputs for three of the flip-flops have jumpers so that they may be connected to either pulse inverter. Thus, for example, three flip-flops may be cleared from one inverter and five from the other. All jumpers are in place when the module is shipped and therefore all flip-flops are cleared from either input. Each clear diode is connected to the center of three lugs which are shorted together. To connect the clear input of flip-flop E, F, or G to input R only, cut the jumper nearest the plug for each flip-flop.

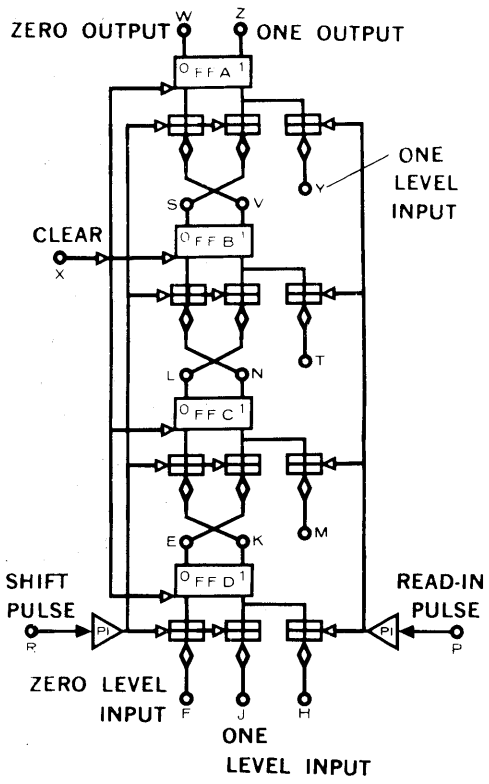
INPUT: Flip-flops may be set and cleared through the outputs described on page 6.13. Inputs are also as described on page 6.13. If a conditional read-in is desired on the Type 42 .8, the level may be brought to just one input gate uch as V). The other input gate (pin X) must be biased off by connection to a clamped load resistor. The level at V must be at −3 volts for at least two microseconds to inhibit the read-in, and must be at ground for at least one microsecond to enable the read-in. Any number of level inputs may be inhibited with one clamped load resistor.

OUTPUT: As described on page 6.15.

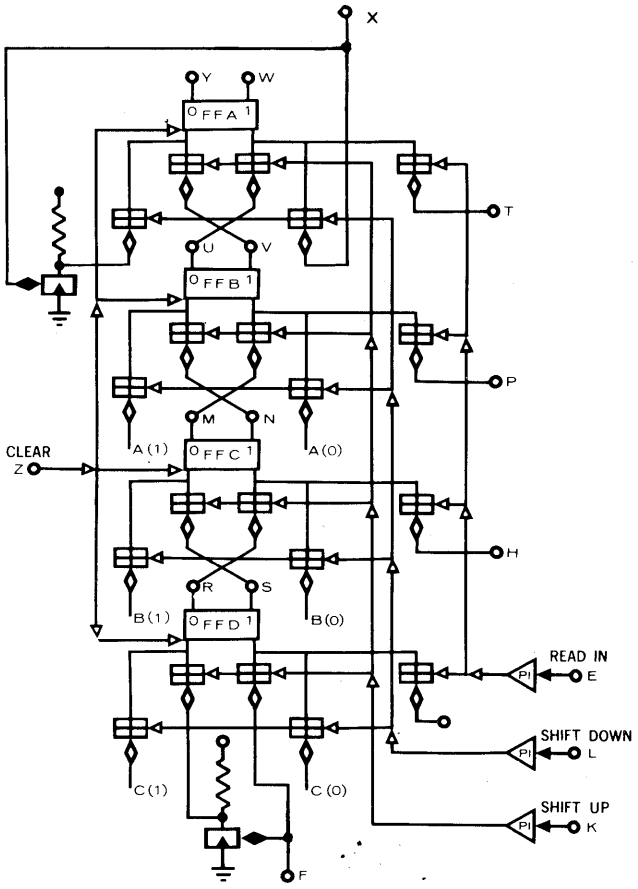
POWER: Type 4218: −15 volts/98 ma; +10 volts (A)/0.5 ma; +10 volts (B)/0.5 ma. **Type 4224:** −15 volts/165 ma; +10 volts (A)/3 ma; +10 volts (B)/0 ma. **Type 4227:** −15 volts/160 ma; +10 volts (A)/2 ma; +10 volts (B)/2 ma.

UNBUFFERED FLIP-FLOPS
TYPES 4216, 4231
1 MEGACYCLE

4000 SERIES



4216 SHIFT REGISTER



4231 SHIFT REGISTER

The Types 4216 and 4231 contain quadruple flip-flops prewired as shift registers with provision for external read-in of ONE's. The Type 4216 has gates for shifting in one direction only while the Type 4231 has provisions for bi-directional shifting.

These modules are particularly useful for parallel-serial or serial-parallel conversion, as a shift registers in a serial arithmetic element, or as a multiplier-quotient register in either serial or parallel arithmetic units.

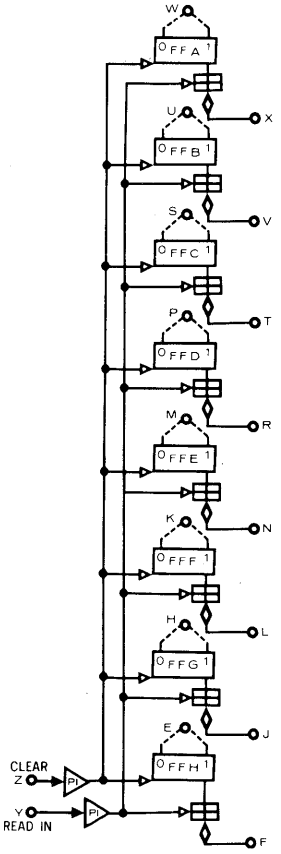
INPUT: As described on page 6.13. The load on the shift data inputs for the Type 4231 is one unit of 1-megacycle Base Load plus one capacitor-diode gate level input. The shift data inputs should be grounded if they are not being used. Additional inputs may be brought in through the flip-flop output terminals.

OUTPUT: As described on page 6.15.

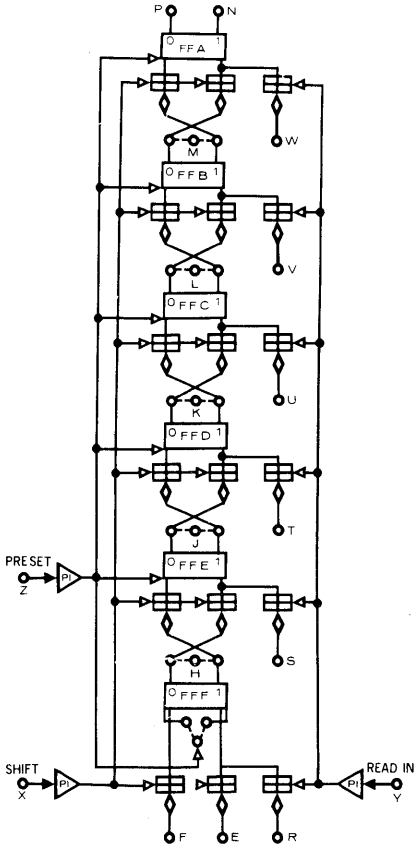
POWER: Type 4216: −15 volts/100 ma; +10 volts (A)/0.65 ma; +10 volts (B)/0.5 ma. **Type 4231:** −15 volts/130 ma; +10 volts (A)/0.9 ma; +10 volts (B)/1.05 ma.

UNBUFFERED FLIP-FLOPS
TYPES 4220, 4221, 4223
1 MEGACYCLE

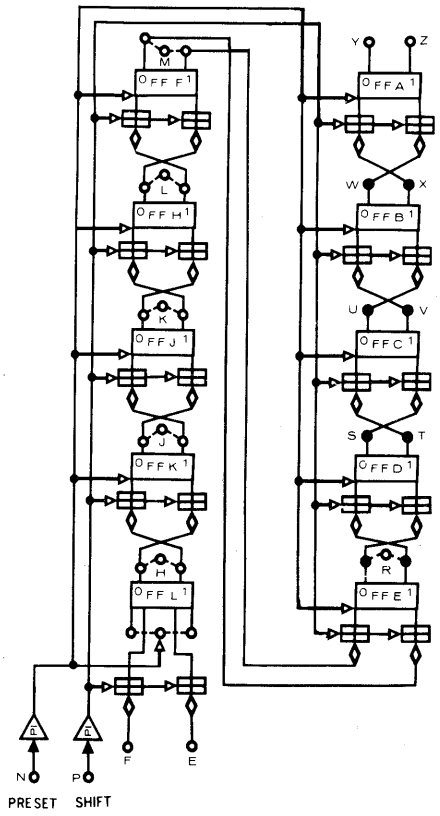
4000 SERIES



4220 BUFFER REGISTER



4221 SHIFT REGISTER



4223 SHIFT REGISTER

Flip-flops in these modules are preconnected for buffering and/or shifting applications. The Type 4220 is an 8-bit buffer register; the Type 4221 is a 6-bit shift register with provisions for parallel read-in of ONE's. (This is similar to the Type 4216.) The Type 4223 is a 10-bit shift register.

Most of the flip-flops in this group have only one output terminal available. This may be selected by internal jumper, to be either the ONE terminal or the ZERO terminal. If the ZERO output terminal is selected, it may be used for gated read-in of ONE's from external sources. If additional functions are required, the flip-flop modules with two output terminals should be used. The modules are shipped with no output jumpers installed. The jumpers are labeled "1" and "0" on the board, and may be traced easily to their output pins.

In addition to the shift and read-in functions, each module has a clear input line. In the Types 4221 and 4222 this line may be jumpered to either set or clear the first flip-flop. This feature is particularly useful in building ring counters, where it is desired to preset the shift register with a single ONE in it. (The modules are shipped with neither jumper installed. The jumpers are labeled "S" and "C" on the board for set and clear.)

INPUT: All input signals are as described on page 6.13.

OUTPUT: As described on page 6.15.

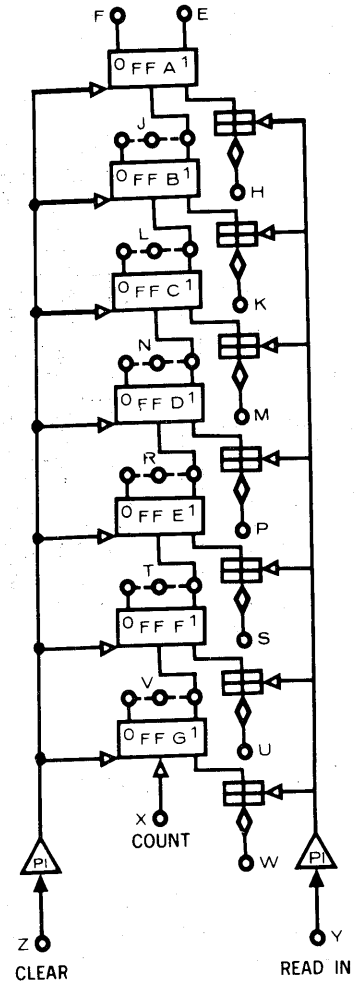
POWER: Type 4220: −15 volts/180 ma; +10 volts (A)/3 ma; +10 volts (B)/0 ma. **Type 4221:** −15 volts/150 ma; +10 volts (A)/2.5 ma; +10 volts (B)/0 ma. **Type 4223:** −15 volts/130 ma; +10 volts (A)/2 ma; +10 volts (B)/0 ma.

UNBUFFERED FLIP-FLOPS

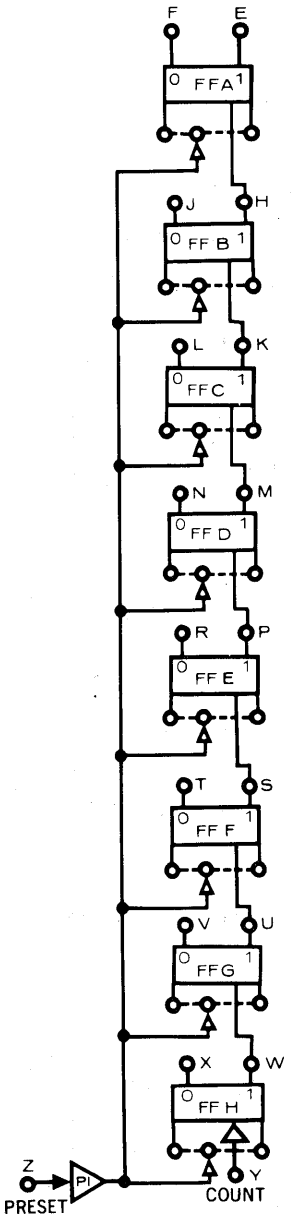
TYPES 4222, 4225

1 MEGACYCLE

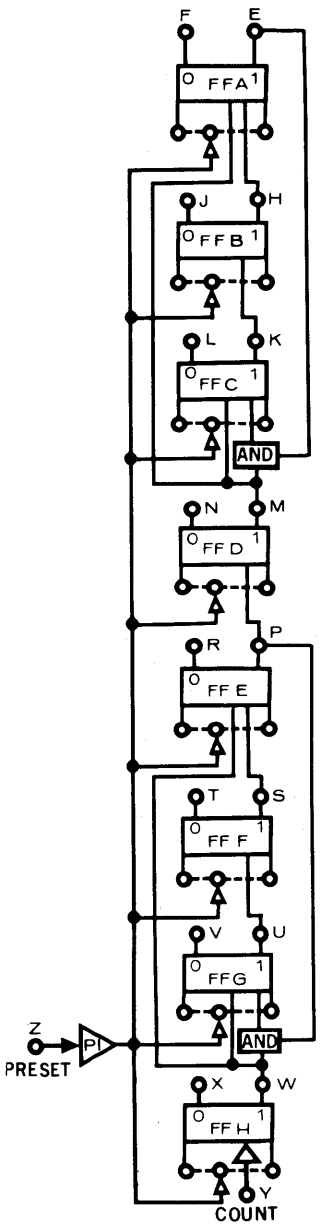
4000 SERIES



4222 COUNTER WITH READ-IN



4225 AS A BINARY COUNTER



4225 AS A BCD COUNTER

The Types 4222 and 4225 are multiple flip-flop modules, preconnected for counter applications. The Type 4222 contains seven stages connected for normal binary counting. Gates are also provided for read-in of ONE's from an external source. Six flip-flops have only one output terminal which may be jumpered to the ONE or ZERO output of each flip-flop. The jumpers are labeled "1" and "0" on the board. The module is shipped with no jumpers installed.

Type 4225 is an 8 flip-flop module with internal jumpers which allow it to be used as either a binary or a BCD counter (8-4-2-1 code). These jumpers are labeled inside the board. Those marked "B" are used for binary counting and those marked "D" are used for decimal counting. The Type 4225 also has provisions for jamming the counter to a preset number. Each flip-flop has a pair of independent jumpers so that it may be cleared or set whenever the preset line is pulsed. These jumpers are labeled "C" and

"S" respectively. The module is shipped with no jumpers installed.

INPUT: All inputs are as described on page 6.13. The clear and preset lines must receive a 1-microsecond pulse. Gated read-in of ONE's from an external source can be done through the ZERO flip-flop output terminal. (In the Type 4222, this assumes that the ZERO output has been selected with the jumpers.) Gated read-in of ZERO's normally generates carries; thus, it may be done only with the Type 4225 and diode gates. The gates must be set up in a jam transfer configuration and a 1-microsecond pulse must be used to strobe the information. If considerable extra logic is required, the general purpose flip-flops, Type 4215 and 4217, are recommended.

OUTPUT: Outputs are as described on page 6.15 for complementing flip-flops. Note the internally connected complement input loads. When the Type 4225 is preconnected as a binary coded decimal counter there are a number of additional internally connected loads which must be taken into account. Pins E, P, K, and U are driving inhibit inputs which reduce the loading by two units of DC Base Load and 0.6 of a unit of transient load. Pins M and W are driving two complement inputs each.

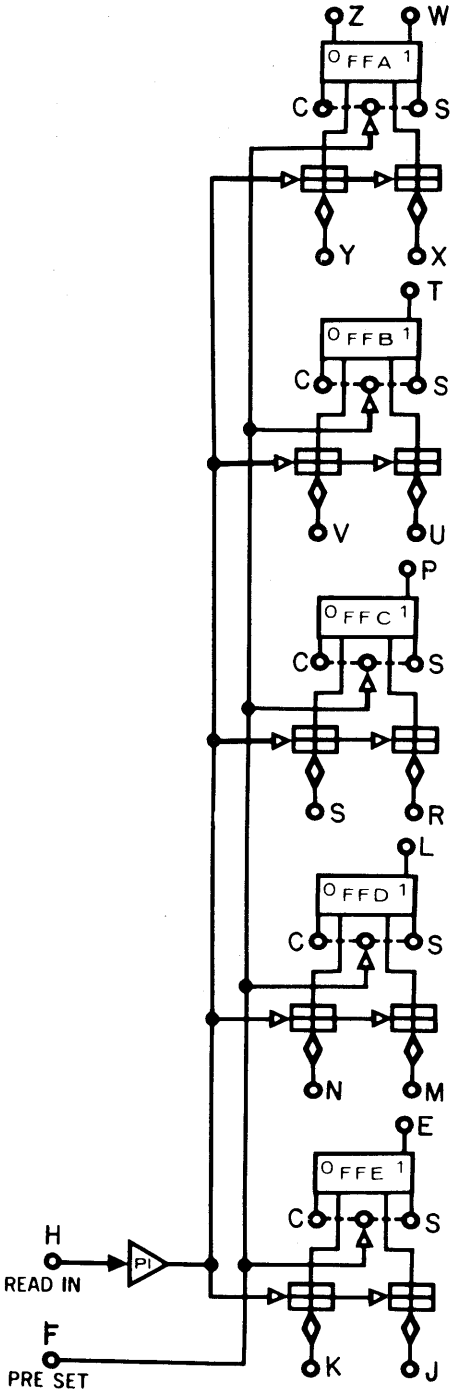
POWER: Type 4222: −15 volts/160 ma; +10 volts (A)/2.5 ma; +10 volts (B)/0 ma. **Type 4225:** −15 volts/150 ma; +10 volts (A)/2.7 ma; +10 volts (B)/0 ma.

UNBUFFERED FLIP-FLOPS

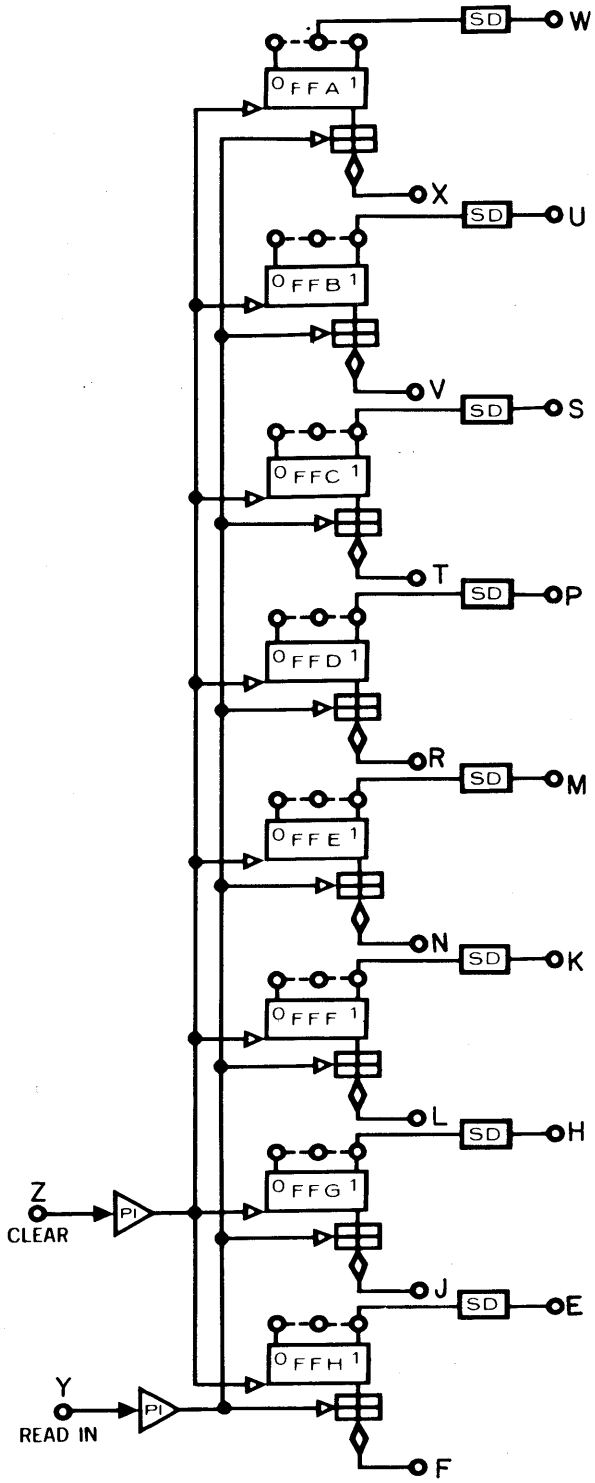
TYPES 4219, 4290

1 MEGACYCLE

4000 SERIES



4219 JAM BUFFER



4290 BUFFER AND SOLENOID DRIVER

Types 4219 and 4290 are multiple flip-flop buffer registers. The Type 4219 contains five flip-flops with provisions for jam transfer input. It is frequently used in digital-to-analog converters where the jam transfer feature is required to prevent spurious pulses from appearing on output lines. Four of the flip-flops have only one output terminal available. The opposite terminal may be obtained by simply reversing the definitions on the flip-flops. For example, to obtain a ZERO output from flip-flop B, pin T would become the ZERO output, pin U would become the ZERO input and pin V would become the ONE input. The preset line can be jumpered to either set or clear each flip-flop. The module is shipped with the clear jumpers installed. For each flip-flop, the jumper nearest pin Z clears, and the jumper nearest pin A sets.

The Type 4290 is an 8-bit buffer register like the 4220 with output amplifiers for driving loads such as incandescent indicators or solenoids. The 10-1/4 inch 4290 (3-1/4 inches longer than the standard 7-inch module) is frequently used in control systems for driving relays. For example, a relay setting may be calculated and read into this buffer register to hold the relays in the desired position while a new setting was being calculated. There is one solenoid driver per flip-flop. Its input may be connected to either the ZERO or the ONE output of the flip-flop with a jumper. The jumpers are labeled "1" and "0", and the module is shipped with the "1" jumper installed. The flip-flops will operate at one megacycle. The solenoid driver delay may be as long as 10 microseconds.

INPUT: As described on page 6.13.

OUTPUT: Type 4219 outputs are the same as those described on page 6.15. Type 4290 outputs are intended for driving indicators and/or solenoids. The more positive output level is −0.3 volts and can drive 100 milliamperes to a more negative voltage. The more negative level is diode-clamped to −15 volts. (The solenoid driver is inverting. With the "1" jumper installed the output will be ground when the flip-flop holds a ONE.)

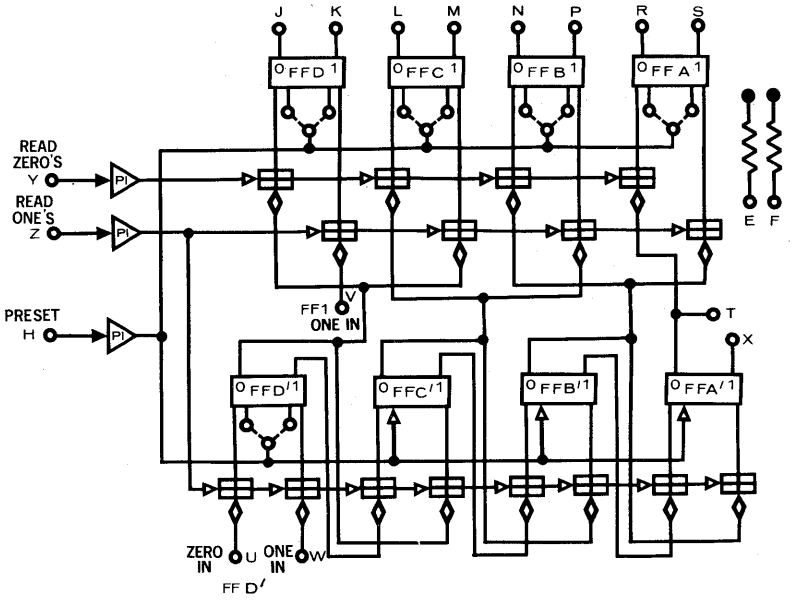
POWER: Type 4219: −15 volts/116 ma; +10 volts (A)/0.65 ma; +10 volts (B)/0.8 ma. **Type 4290:** −15 volts/110 ma; +10 volts (A)/0 ma; +10 volts (B)/5 ma. This module may also require as much as 800 milliamperes from an external negative source when all of the solenoid drivers are conducting and have a maximum load.

UNBUFFERED FLIP-FLOPS

TYPE 4226

1 MEGACYCLE

4000 SERIES



4226 SERIAL-TO-PARALLEL ASSEMBLER

The Type 4226 Serial-to-Parallel Assembler is frequently used in successive approximation analog-to-digital converters. This unit contains a 4-bit buffer and a 4-bit shift register, which controls the operation of the buffer. Maximum prf is one megacycle. Clamped load resistors are available for inhibiting unused inputs.

In normal usage the shift register (FFA′ to FFD′) is connected as a ring counter and the read ONE's and read ZERO's pulse inputs are activated in synchronism, with the read ZERO's line being conditioned by the external information to be read in. Thus, if both registers have been preset to 1000 and the shift register inputs are biased to read in ZERO'S (U ground and W at −3 volts), the first input pulse will set flip-flop C and conditionally reset flip-flop D. The next input pulse will set flip-flop B and conditionally reset flip-flop C, etc. Five flip-flops may be jumpered to be either set or cleared by the preset, as shown. The module is shipped with none of these jumpers installed. There are three lugs near each flip-flop. If the pair of lugs farthest from the plug are jumpered, the corresponding flip-flop will be cleared. The pair of flip-flops closest to the plug are flip-flops D and D′.

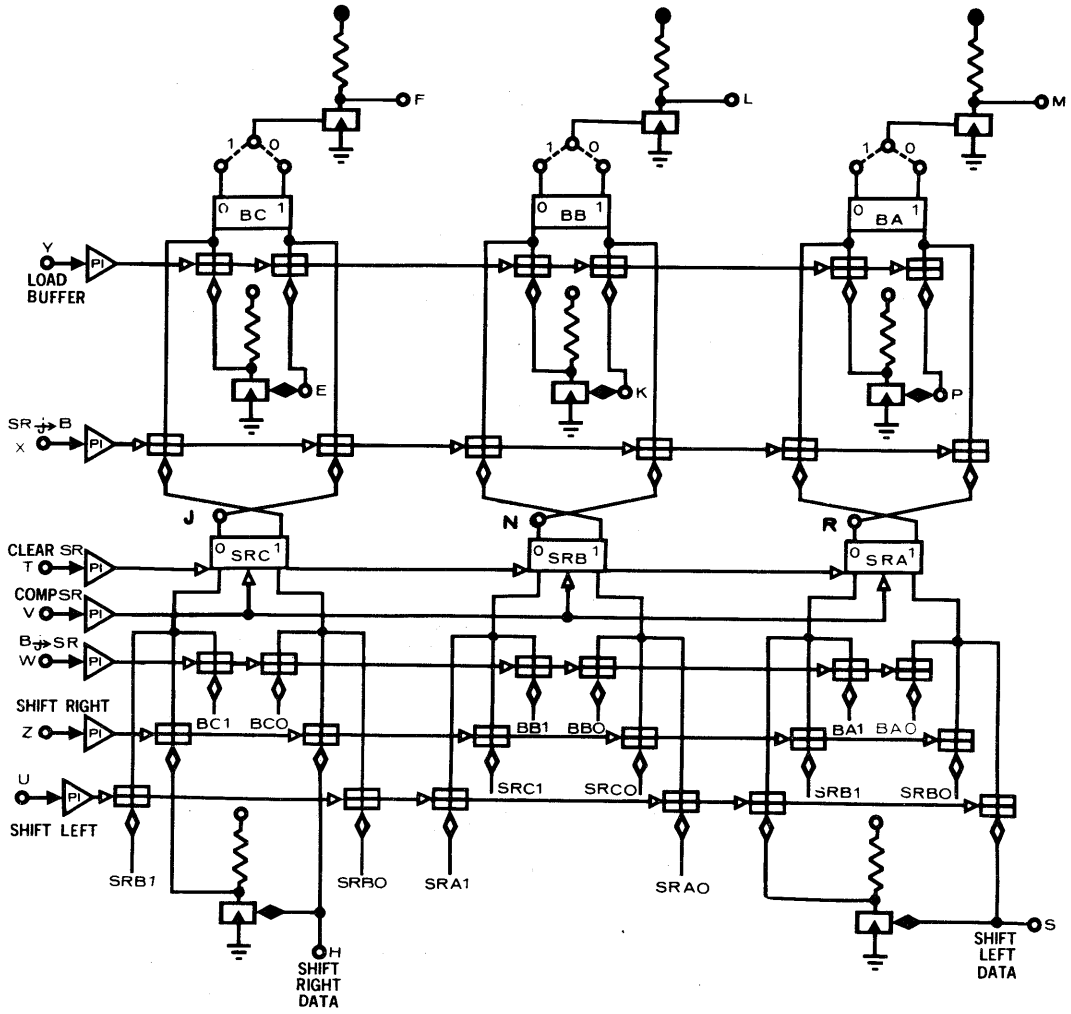
INPUT: Read ONE's, read ZERO's, and preset inputs require Standard 0.4-microsecond Negative Pulses, and each input represents one unit of Pulse Load. One microsecond should be allowed between pre-setting and read-in. The two read lines may be pulsed simultaneously. If not pulsed simultaneously, the read ZERO's line may be pulsed any time before the read ONE's line, but at least one microsecond must be allowed between pulsing the read ONE's line and pulsing the read ZERO's line. Capacitor-diode gate level inputs are as described on page 6.13.

OUTPUT: Outputs are described on page 6.15.

POWER: −15 volts/192 ma; +10 volts (A)/1.7 ma; +10 volts (B)/1.2 ma.

UNBUFFERED FLIP-FLOPS
TYPE 4228,
1 MEGACYCLE

4000 SERIES



4228 ASSEMBLER

The Type 4228 is a 3-bit shift register with a 3-bit buffer register. The 10-1/4 inch 4228 (3-1/4 inches longer than a standard, 7-inch module) may be used for transferring information between two asynchronous devices at rates up to one megacycle.

These units are particularly useful where the word lengths of the two devices are different, or where one of the devices operates in serial and the other in parallel. For example, with six Type 4228 modules, information from a 6-channel magnetic tape can be assembled into 18-bit words for a direct computer input and 18-bit computer words can be separated into 6-bit output words. The magnetic tape information would come into the shift right data input (pin H) and would move from SRC to SRB to SRA. When three pieces of information have come in (three 6-bit words in six such modules) they are transferred to the buffer, which holds the information for the computer while additional information is coming from the magnetic tape. To write data on tape, parallel information comes into the buffer register, is jammed into the shift register, and is shifted out to the right. To read data when tape is moving backward, the shift left is used.

A complement input terminal is also available on the shift register flip-flops. This can be used to reverse the polarity of the required input or output levels. The Type 42281 is a 1-bit version of the 4228 on a similar, extra-long module.

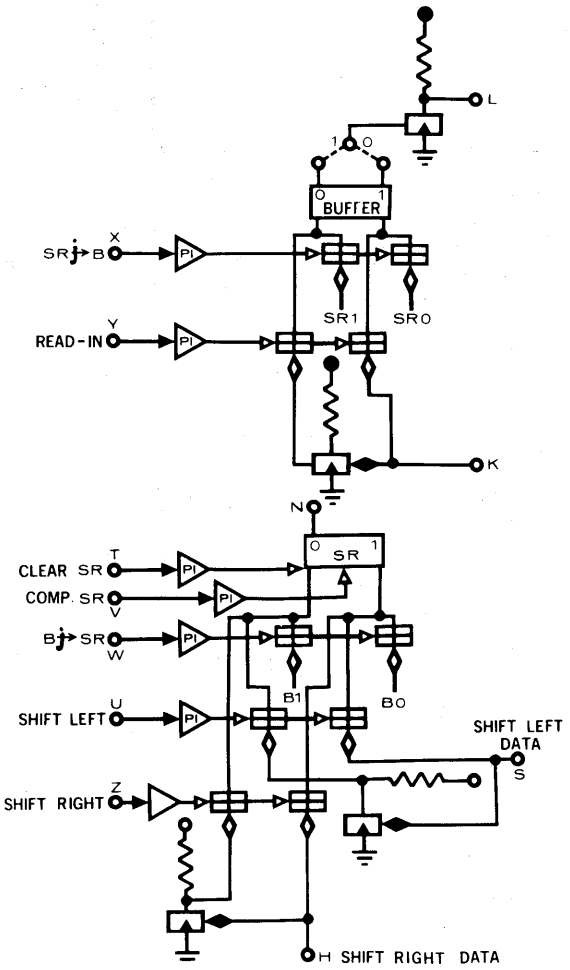
INPUT: All pulse inputs are Standard 0.4-microsecond Negative Pulses. Each represents one unit of load. The level inputs are zero volts for a logical ONE and −3 volts for a logical ZERO. These levels must be enabled one microsecond before the corres-

UNBUFFERED FLIP-FLOPS

TYPE 42281

1 MEGACYCLE

4000 SERIES



42281 ASSEMBLER

ponding pulse occurs. The load is one unit of 1-megacycle Base Load plus one capacitor-diode gate level input.

OUTPUT: The shift register outputs are as described on page 6.15. (Note internally connected gates.) The buffer outputs come from 500-kc inverters which can drive seven units of Base Load and one unit of DC Emitter Load. Total transition time is typically 0.2 microsecond. There is one output amplifier for each buffer flip-flop. There are jumpers which connect one side or the other of each buffer flip-flop to its output amplifier. The jumpers are labeled "1" and "0", and the module is shipped with the 0-jumpers installed. The 0-jumper connects the ONE output of the buffer flip-flop to its output inverting amplifier, so that the module output is at −3 volts when the flip-flop is cleared.

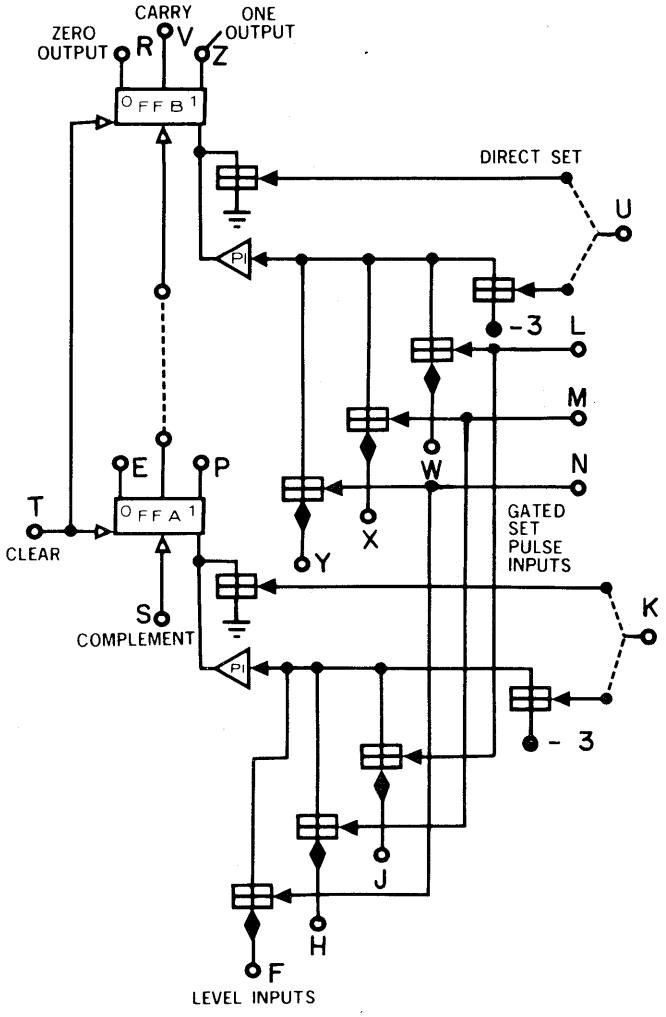
POWER: Type 4228: −15 volts/288 ma; +10 volts (A)/2.5 ma; +10 volts (B)/0 ma. **Type 42281:** −15 volts/160 ma; +10 volts (A)/2.5 ma; +10 volts (B)/0 ma.

BUFFERED FLIP-FLOPS

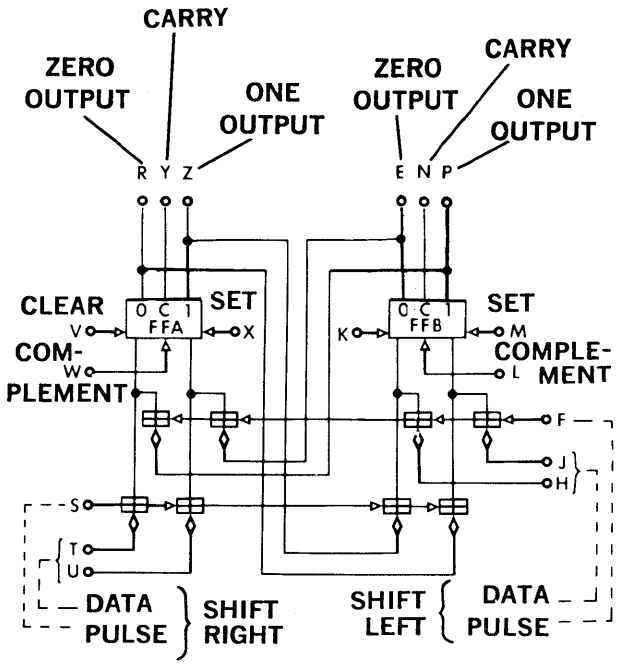
TYPES 4204, 4205

1 MEGACYCLE

4000 SERIES



4204 BUFFER



4205 ACCUMULATOR

The Types 4204 and 4205 are dual flip-flop packages with high output driving capability. The Type 4204 is a counter module with provisions for external read-in from many sources.

The Type 4205 is useful in serial or parallel accumulators. It includes provisions for shift left, shift right, and complement. This module is frequently used in conjunction with the Type 4123 to form a parallel arithmetic element.

Both units can operate at one megacycle. The total transition time for the outputs is approximately 300 nanoseconds. The flip-flops cannot be set or cleared through the output terminals.

INPUT: Same as on page 6.13 with the following exceptions. In the Type 4204 the gated set pulse inputs are the same as the pulse inputs of a negative capacitor-diode gate. The direct clear may be jumpered to a negative terminal (similar to the gated set pulse input) or to a positive terminal (similar to a complement input). It is shipped with the negative clear connection; that is, the clear input lugs are connected to the lugs nearest pin A. The positive clear connection is made by jumpering the input lugs to the lugs nearest pin Z. The carry input to FFB may be jumpered to the carry output of FFA.

The carry propagate time is approximately 70 nano-

seconds per bit with this counting connection. A 1-microsecond clear pulse is required. The module is shipped without a carry jumper.

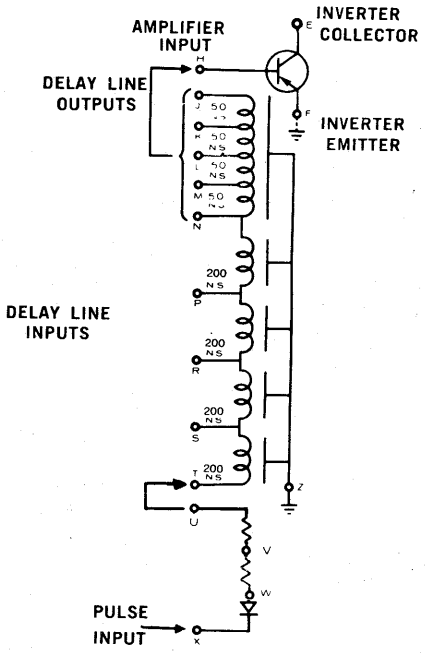
In the Type 4205 the complement input should be driven by capacitor-diode gates or other pulse gates. It should not be driven directly from the carry output of the previous stage because then there would be no provisions for disabling the carry and the carries would attempt to operate when the shift lines were being operated. The carry propagate time is approximately 100 nanoseconds per bit when used with the 4123 capacitor-diode gate module.

OUTPUT: ZERO and ONE outputs provide DEC Standard Levels, each capable of simultaneously driving (a) 14 units of Base Load, (b) 1 unit of DC Emitter Load, and (c) any number of non-synchronously Pulsed Emitter Loads. Output signal delay is less than the DEC Standard 0.4-microsecond Pulse width, so that a capacitor-diode gate must be used to sample them at the same time they are being changed. The carry output may only drive the complement input of a flip-flop or the pulse input of a negative capacitor-diode gate.

POWER: Type 4204: −15 volts/140 ma; +10 volts (A)/1.3 ma; +10 volts (B)/2.0 ma. **Type 4205:** −15 volts/155 ma; +10 volts (A)/1.0 ma; +10 volts (B)/1.0 ma.

DELAYS
GENERAL INFORMATION, TYPE 1310

4000 SERIES



1310 DELAY LINE

GENERAL INFORMATION

In the 4000-series there are four types of delay circuits. One, the Type 1310, is a delay line which may be used to produce delays of 0.8 to 1 microsecond for Standard 0.4-microsecond Pulses. The output is the collector of a pulse gate which can drive one unit of Pulse Load.

A second type, the 4301, is a single-shot which produces negative level for the duration of the delay and a Standard Negative Pulse at the end of the delay. The duration of the delay, 2.5 microseconds or greater, may be controlled externally. Circuit recovery time must be allowed between repetitive pulses.

A third type, the 4303, is an integrating one-shot with a level output. This module, when repeatedly pulsed, will hold its output level for the delay time specified after the final input pulse has been received. It may also be used to form a gated pulse source. Minimum delay available is 0.6 microsecond. This unit may be controlled externally and may be used with the Types 4304 and 4305 to produce programmable delays.

The fourth 4000-series delay, the Type 4306, contains three one-shots similar to the Type 4301 without provision for external control. The delay duration is variable from one microsecond up.

1310 DELAY LINE

The Type 1310 is a 1000-series module but it may be used with 4000-series modules to delay Standard 0.4-microsecond Negative Pulses. The delay range is 0.8 to 1 microsecond, variable in 50-nanosecond steps.

Connections for this module are shown on the logic diagram. The primary input is pin X. Additional inputs may be OR'ed to pin W through external high speed diodes such as a 1N994. Pin U should be jumpered to pin T and one of the delay line outputs should be jumpered to pin H. The delay through the output transistor is approximately 20 nanoseconds.

INPUT: The input should be a Standard 0.4-microsecond Negative Pulse or its equivalent. The load is five units of Pulse Load.

OUTPUT: The emitter of the output inverter must be grounded. The transistor collector should be connected directly to the input of a pulse amplifier or the unit being pulsed. However, if additional logical gating is required, it may be done with up to three transistor inverters placed in series between the collector and the pulse amplifier.

POWER: −15 volts/0 ma; +10 volts (A)/2.1 ma; +10 volts (B)/0 ma.

DELAYS

TYPE 4301

130 KILOCYCLES

4000 SERIES

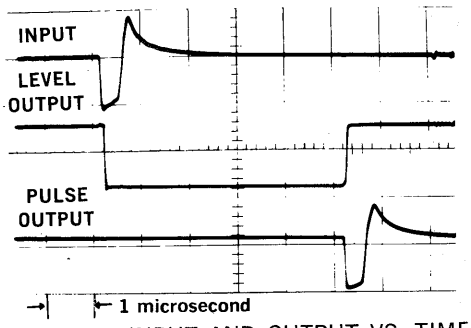
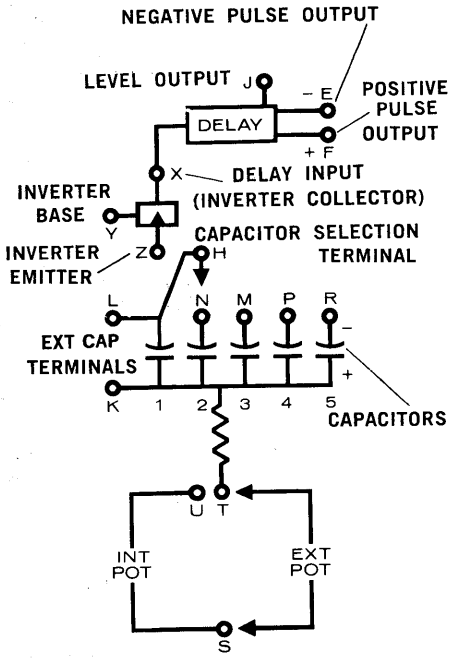


Figure 1 — INPUT AND OUTPUT VS. TIME



4301 DELAY (ONE-SHOT)

The Type 4301 delay unit is a mono-stable multivibrator. When the input terminal is grounded through an inverter the level output terminal will switch from its normal ground level to −3 volts for a predetermined, but adjustable, period of time and then back to ground. A pulse transformer generates a DEC Standard 0.4 microsecond Pulse at the pulse output during the final transition. The pulse transformer has both positive and negative terminals so that either polarity pulse may be obtained. Typical output and input wave forms are shown in Figure 1.

The delay duration is variable from 2.5 microseconds to 0.2 second. The five internal capacitors determine the coarse range. Capacitor 1 is internally connected to provide delays at the range of 2.5 to 25 microseconds. Connecting the capacitor selection terminal to capacitors 2, 3, 4 or 5 increases the delay in approximate factors of 10, with capacitor 5 representing the maximum delay range available with an internal capacitor. By installing an additional external capacitor to the indicated terminals, the delay range may be further extended.

An internal 15,500 ohm potentiometer may be used for fine adjustment if pin U is connected to pin T. An external potentiometer may also be used if desired. Circuit recovery time is equal to 20% of the maximum delay available on the coarse range being used. A 20% change in power supply voltage will change the delay less than 1%. Delay jitter (due to power supply ripple) is less than 0.5%, peak to peak.

The inverter is similar to the Type 4105.

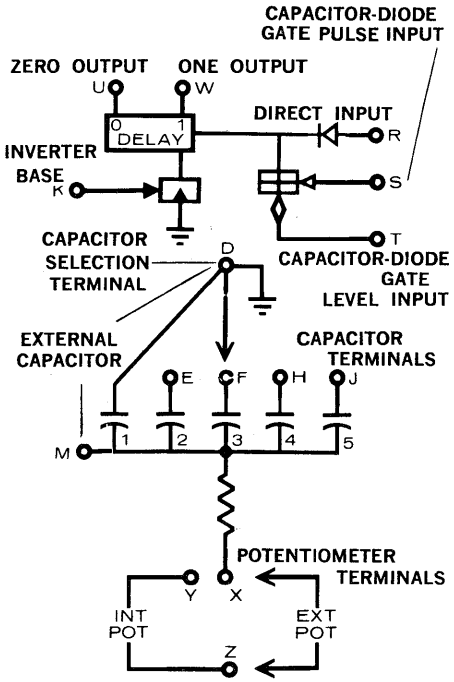
INPUT: Same as a Type 4603 Pulse Amplifier.

OUTPUT: Level: When the input is pulsed, a negative DEC Standard Level occurs for the duration of the delay interval. This level is capable of simultaneously driving: (a) 12 units of Base Load; (b) 1 unit of DC Emitter Load; and (c) any number of Pulsed Emitter Loads, providing not more than one is pulsed at a time. **Pulse:** At the end of the delay interval, a DEC Standard 0.4 microsecond Pulse occurs. The output pulse will be negative if the positive terminal is grounded; it will be positive if the negative terminal is grounded. This signal can drive 8 units of Pulse Load.

POWER: −15 volts/70 ma; +10 volts (A)/1.1 ma; +10 volts (B)/0 ma.

DELAYS
TYPE 4303
1.6 MEGACYCLES

4000 SERIES



4303 INTEGRATING SINGLE SHOT

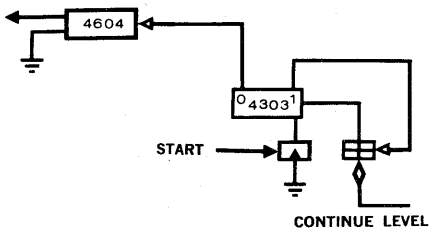


Figure 1 – GATABLE PULSE SOURCE

The Type 4303 Integrating Single Shot contains a stable single shot multivibrator which generates a flip-flop type output during the delay. The delay intervals are variable in four overlapping ranges from 3.4 microseconds to 0.9 second. (Longer delays may be obtained with an external capacitor.) The unit has an internal potentiometer for fine control and provisions for an external potentiometer, if desired. The unit may be repeatedly triggered, and the delay will continue for the specified duration after the final triggering. If a negative level is applied to the base of the input inverter, the delay will begin when the level is applied and remain for the specified duration after the level has been removed. The unit has no recovery time. The delay time will change less than ±2% for a 20% change in supply voltage, and the peak-to-peak jitter is less than 1.4%. Controls: Capacitor 1 is internally connected to the capacitor selection terminal to give the shortest delay range. Delay ranges may be increased by approximate factors of 10 by connecting capacitors 2, 3, 4 or 5 to the capacitor selection terminal. (Capacitor 5 gives the largest delay range, up to 0.9 second.) For longer delays an external capacitor may be connected between the external capacitor terminal and the capacitor selection terminal.

To use the internal potentiometer for fine control, pin X should be jumpered to pin Y. If an external potentiometer is desired, it should be placed between pin X and pin Z.

INPUT: Inverter: The delay may be triggered by a Standard 0.4-microsecond Negative Pulse or a Negative Level applied to the base of the inverter attached to the delay. The d-c load at this point is one unit of 1-megacycle Base Load. The transient load presented to a pulse input is one unit of Pulse Load. **Direct Input:** The direct input (pin R) may be connected to the output of one or more Positive Capacitor-Diode Gates, such as Types 4126 and 4128, or may be driven by a Standard 0.4-microsecond Positive Pulse. Load is 1 unit Pulse Load. **Capacitor-Diode Gate:** Same as Type 4306.

OUTPUT: The ONE output will produce −3 volts during a delay period and ground volts otherwise. The ZERO output will produce ground volts during a delay and −3 volts otherwise. Driving ability is the same as an unbuffered flip-flop.

POWER: −15 volts/70 ma; +10 volts (A)/2.9 ma; +10 volts (B)/3.2 ma.

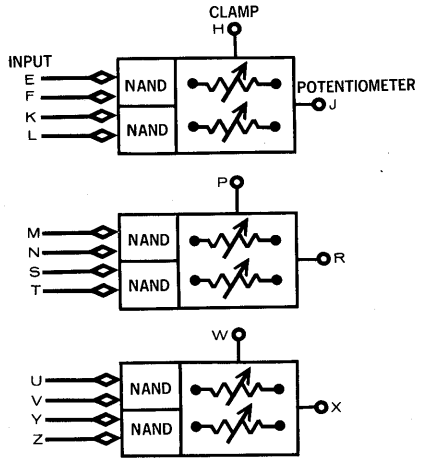
TYPICAL APPLICATIONS

GATABLE PULSE SOURCE

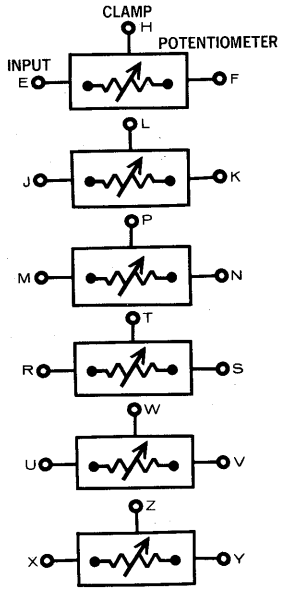
A typical application for the Type 4303 is in making a gatable pulse source such as shown in Figure 1. The delay is turned on by a negative pulse on the inverter base. When the delay is completed, the unit will be retriggered by the feedback loop from the ONE output to the capacitor-diode gate input. This retriggering process will continue as long as the continue level is at ground.

DELAY CONTROLS
TYPES 4304, 4305

4000 SERIES



4304 DELAY CONTROL



4305 DELAY CONTROL

The delay controls are used to program the potentiometer settings externally on the Type 4303 integrating single-shot. These are particularly useful in converting a binary word to a time interval.

To use this feature the range selection is done on the Type 4303 by the capacitor connection. The potentiometer terminals of the delay controls are connected to the external potentiometer terminals on the Type 4303. Up to 20 potentiometers are selected by digital levels to produce the desired delay interval. The variation in delays which may be programmed will depend on the capacitor connection of the Type 4303. However, the total range covered will be about 10.

At least one potentiometer must be enabled at all times; otherwise, the capacitors in the Type 4303 will discharge and the output flip-flop will go to the ONE state. The minimum time between disabling one potentiometer and enabling another is 0.5 microseconds.

INPUT: Type 4304: The input should be Standard Levels or equivalent. The load is one unit of Base Load shared among the negative inputs. The potentiometer is enabled when both inputs are at ground and is disabled if either input is negative. If an unused potentiometer is connected to Type 4303, its input should be held negative. **Type 4305:** The input is driven by the collector of a level gate (or many gates in parallel), without a clamp load resistor. The potentiometer is enabled when the input is open-circuited and is disabled when the level gate looks like a short-circuit. The load is one unit of DC Emitter Load.

OUTPUT: The clamp outputs are connected to pin Z of the Type 4303 and the potentiometer outputs are connected to pin X of the Type 4303.

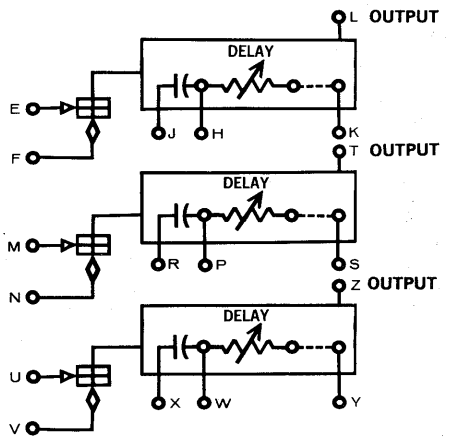
POWER: Type 4304: −15 volts/6 ma; +10 volts (A)/0.5 ma; +10 volts (B)/0.5 ma. **Type 4305:** −15 volts/6 ma; +10 volts (A)/0 ma; +10 volts (B)/0 ma.

DELAYS

TYPE 4306

330 KILOCYCLES

4000 SERIES



4306 DELAY

The Type 4306 has three identical delays. They are all monostable multivibrators. The unit is triggered when a positive pulse and a ground level are applied to the capacitor-diode gate input terminals. The output terminal will switch from its normal ground level to −3 volts for a predetermined, but adjustable, period of time and then back to ground. The delay duration is variable from 1 to 10 microseconds and may be extended by installing an external capacitor. Internal potentiometers are provided, but external potentiometers may be used by removing jumpers on the board. Circuit recovery time is 20 percent of the maximum delay of the range. A 20-percent change in power supply voltage will change the delay less than one percent. Delay jitter is less than one-half percent, peak-to-peak.

INPUT: Level inputs are Standard Levels of 0 and −3 volts. The gate is enabled by a ground level. There is no d-c load at the level input; the transient load is two units of Base Load. The gate must be enabled for at least one microsecond, and disabled two microseconds before the application of the input pulse or level change.

The pulse input may be driven from a Standard 0.4-microsecond +2.5 volt Pulse, or it may be driven from a positive-going level change. The level change should be 2.5 to 3.3 volts, with a maximum rise time of 0.5 microseconds. This input represents one unit of Pulse Load.

OUTPUT: When the input is pulsed, a Standard Negative Level occurs for the duration of the delay interval. This level is capable of driving seven units of Base Load and one unit of DC Emitter Load.

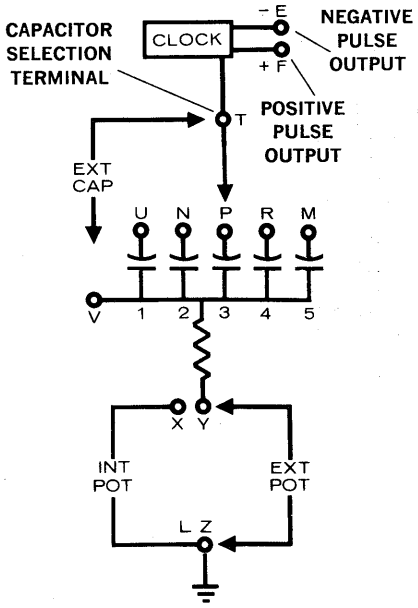
POWER: −15 volts/115 ma; +10 volts (A)/4 ma; +10 volts (B)/0 ma.

CLOCKS

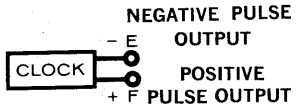
TYPES 4401, 4407

500 KILOCYCLES

4000 SERIES



4401
VARIABLE CLOCK



4407
CRYSTAL CLOCK

The DEC Variable Clock Type 4401 produces standard pulses from a stable, RC-coupled oscillator with a wide range of frequencies available. The variable clock is often used as a primary source of timing for large systems. Where very precise timing is needed, the Type 4407 Crystal Clock, which contains a single-frequency crystal oscillator, may be used.

The frequency of the Type 4401 is variable from 5 cycles/second to 500 kilocycles/second. The capacitor connection determines the frequency range and a 20,000 ohm potentiometer provides fine control. Capacitor 1 gives a range of approximately 50 to 500 KC; capacitor 2, 5 to 50 KC; capacitor 3, 500 to 5000 cycles; capacitor 4, 50 to 500 cycles; and capacitor 5, 5 to 50 cycles. An external capacitor may be used for lower frequencies. If terminals X and Y are connected together, the internal potentiometer will provide the fine control. An external potentiometer can be connected between terminals Y and Z.

The Type 4407 contains a series resonant crystal oscillator circuit and two pulse shaping buffer amplifiers which produce DEC Standard 0.4 microsecond Pulses. The frequency, specified by the customer, may be between 5 and 500 kilocycles. The frequency is stamped on the crystal in the plug-in unit.

For information on synchronizing clocks, see Types 1404, 1406. The same method and pin connections apply to the Types 4401 and 4407.

OUTPUT: The output is a DEC Standard 0.4 microsecond Pulse which occurs at the preselected frequency. The pulse may be made positive by grounding the negative output terminals; it may be made negative by grounding the positive output terminal. The signal can drive 8 units of Pulse Load. **Crystal Clock:** The stability of the crystal clock's output frequency is 0.01% between −20 and +55°C. **Variable Clock:** A 20% change in the power supply voltage on the Type 4401 Clock will change the prf less than 1% and its pulse-to-pulse jitter is less than 0.2%.

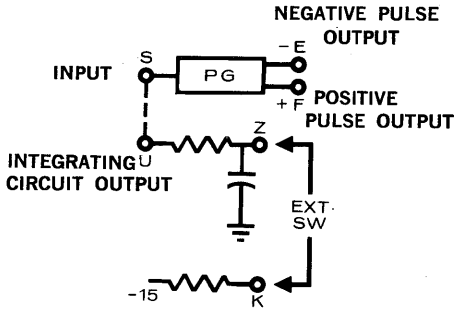
POWER: Type 4401: −15 volts/45 ma; +10 volts (A)/0 ma; +10 volts (B)/0 ma. **Type 4407:** −15 volts/81 ma; +10volts (A)/5 ma; +10 volts (B)/4.5 ma.

PULSE GENERATORS

TYPE 4410

500 KILOCYCLES

4000 SERIES



4410 PULSE GENERATOR

The Type 4410 converts external signals to DEC Standard Pulses. A Schmitt circuit produces a DEC Standard 0.4 microsecond Pulse at the output every time the input voltage goes more negative than −2.5 volts after having been more positive than −1.0 volts. This unit also contains an integrating circuit to filter contact bounce when a switch or relay is used to generate the pulse. The time constant of the integrating circuit is 12 milliseconds.

INPUT: Pulse Generator: The input is a DC connection, thereby eliminating fall time as a characteristic of the incoming signal. Input impedance is 3000 ohms. The input signal should stay between +10 volts and −10 volts. The input can come from an external source or from the output of the integrating circuit. **Integrating Circuit:** The two inputs to this circuit come from switch or relay contacts.

OUTPUT: Pulse Generator: The output is a DEC Standard 0.4 microsecond Pulse. The pulse will be negative if the positive terminal is grounded; it will be positive if the negative terminal is grounded. The maximum prf is 500 KC. This signal can drive 8 units of Pulse Load.

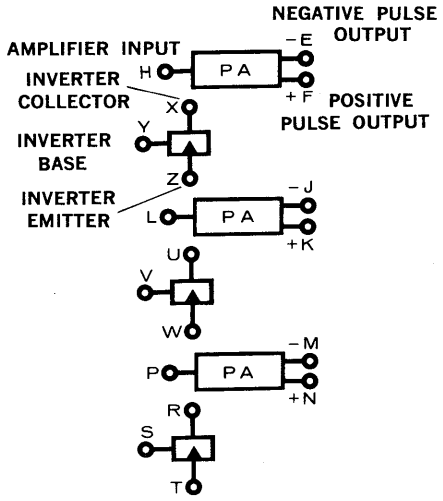
POWER: −15 volts/68 ma; +10 volts (A)/5 ma; +10 volts (B)/5 ma.

PULSE AMPLIFIERS

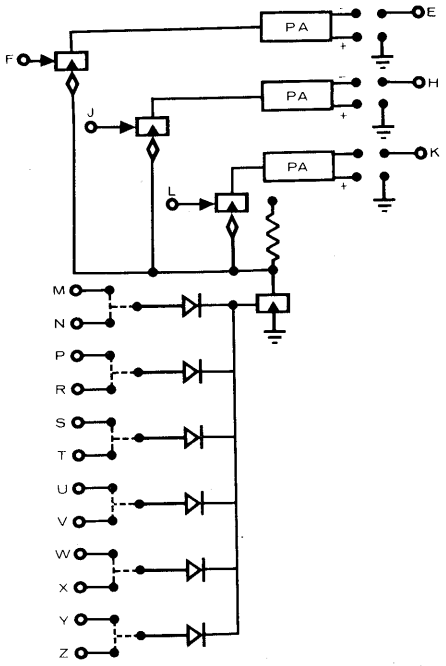
TYPES 4603, 4605

500 KILOCYCLES

4000 SERIES



4603 PULSE AMPLIFIER



4605 PULSE AMPLIFIER

Pulse amplifiers are used for clearing, jamming, and shifting the contents of flip-flop registers, for sending pre-gated information to a variety of loads, and for amplifying and standardizing pulses. The Type 4603 contains three circuits which increase the driving power of the input pulse, standardize the amplitude, and reduce the duration of wide input pulses. With an external feedback connection this module will also increase the duration of 70-nanosecond pulses to 0.4 microseconds.

The Type 4605 contains three pulse amplifiers and inverter gates which share a 6-input diode NAND gate. Each input can be internally jumpered to either of its associated pair of input terminals. The total of twelve such input terminals allows arbitrary decoding of six pair of logic level inputs. Each pulse amplifier has a separate pulse input. Output terminals, connected by jumpers, allow either positive or negative output pulses.

The pulse amplifiers will operate up to 500 kilocycles. Delay through the pulse amplifiers is approximately 0.05 microsecond. Inverters included in the package are similar to the Type 4105; diode gates are similar to Type 4111.

INPUT: The Type 4603 input must come from the collector of one or more pulse gates. The signal on the base of the pulse gate is normally a Standard 0.4-microsecond Negative Pulse. However, any negative pulse having an amplitude between 2.0 and 5.0 volts, leading edge less than 0.2 microsecond and width greater than 0.3 microsecond may be used. Input pulses of less than −0.5 volts will not generate an output pulse. Several remote pulse gate collectors may be connected together to mix pulse sources. A Standard 70-nanosecond Negative Pulse may be used as an input, providing a feedback loop is used (as shown in Figure 2 of the applications section) and high speed pulse gates such as those in Type 1105 are used as the input and feedback pulse gates.

The Type 4605 inverter inputs are similar to the Type 4603. Pulses must be at least 0.3 microsecond since there is no feedback loop. Only one pulse amplifier may be pulsed at a time. Standard Levels or equivalent supply the input to the diode NAND gate; the load is 1/8 unit of DC Emitter Load, shared by the ground inputs.

OUTPUT: The output is a Standard 2.5-volt, 0.4-microsecond Pulse capable of driving 16 units of Pulse Load. The output comes from a pulse transformer. For negative pulses the positive terminal should be grounded. For positive pulses the negative terminal should be grounded. For greater amplitude or driving capability PA outputs may be stacked in series or parallel configurations.

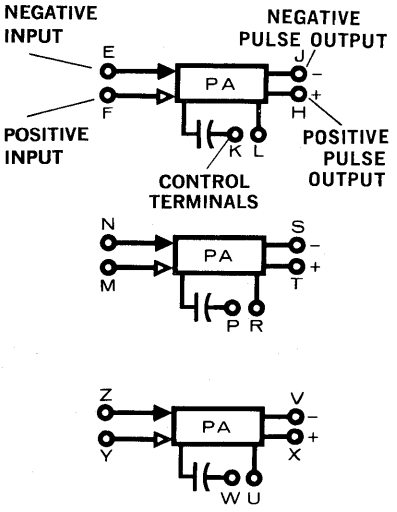
POWER: Type 4603: +10 volts (A)/0.3 ma; +10 volts (B)/0.2 ma; −15 volts/110 ma. **Type 4605:** −15 volts/119 ma; + 10 volts (A)/0.6 ma.

PULSE AMPLIFIERS

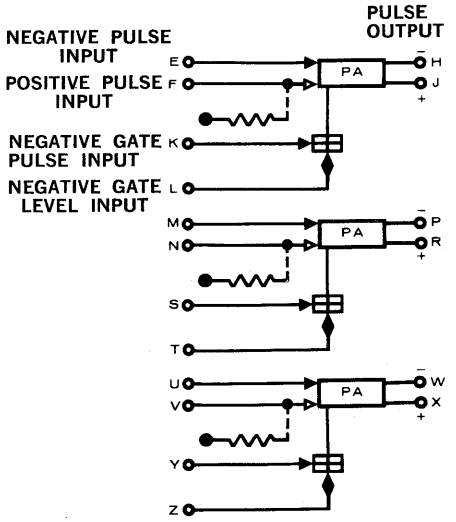
TYPES 4604, 4606

1 MEGACYCLE

4000 SERIES



4604 PULSE AMPLIFIER



4606 PULSE AMPLIFIER

The pulse amplifiers in the Type 4604 perform power amplification and standardize pulses to any width between 0.4 and 1 microsecond. Each pulse amplifier has two control pins for determining the output pulse width. When these control terminals are left open-circuited, the unit will amplify all input signals to Standard 0.4-microsecond Pulses at pulse repetition frequencies up to one megacycle. When the control terminals are shorted together, the unit will standardize inputs to produce 1-microsecond pulses at any rate up to 330 kilocycles. Any pulse width between 0.4 and 1 microsecond can be obtained by connecting an appropriate external capacitor between the two control terminals. The maximum pulse repetition frequency varies with the pulse width from 330 kilocycles to 1 megacycle.

The 4606 contains three identical pulse amplifiers which produce Standard 0.4-microsecond, 2.5-volt Pulses. The pulse amplifier circuits are true pulse standardizers, consisting of a monostable multivibrator followed by an output pulse amplifier. Inputs as narrow as 70 nanoseconds will trigger the circuit. Maximum operating frequency for any one of the pulse amplifiers is one megacycle. A standard 1500-ohm clamped load resistor is internally connected to each positive-going input. Each may be disconnected by removing a jumper wire between lugs on the printed-wiring board.

INPUT: Three types of pulse inputs are provided: a positive pulse, a negative pulse, and a gated negative pulse. All pulse inputs represent one unit of Pulse Load. Standard Pulses of 70 nanoseconds or 400 nanoseconds, or level changes of 2.5 to 4.0 volts with 0.4-microsecond rise or fall time can be used as pulse inputs. When level changes are used, a change in only one direction will produce an output; e.g., a positive-going change at terminal F will produce a pulse, while a negative-going change applied to the same terminal will not.

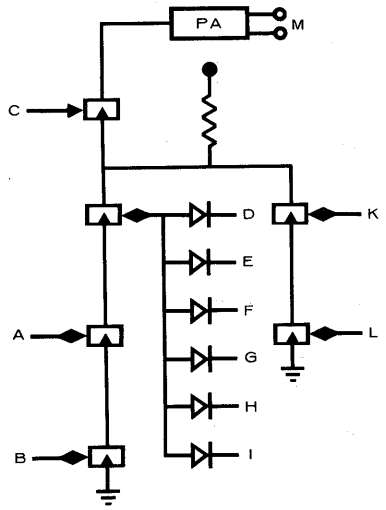
The gated pulse input is enabled by applying a Standard −3 volt Level to the negative gate level input. The transient load is a maximum of two milliamperes; the gate is a 1500-ohm, 330-picofarad negative capacitor-diode gate similar to Types 4127 and 4129. To enable the gate, the gate level must be present for at least one microsecond before the gate pulse is received.

OUTPUT: Same as Type 4603 with longer duration pulses available in Type 4604.

POWER: Type 4604: −15 volts/180 ma; +10 volts (A)/0.6 ma; +10 volts (B)/0.6 ma. **Type 4606:** −15 volts/210 ma; +10 volts (A)/1 ma; +10 volts (B)/1 ma.

TYPICAL APPLICATION

LOGICAL GATING



$$M = C[A \cdot B(D+E+F+G+H+I)+K \cdot L]$$

Figure 1 — PULSE AMPLIFIER GATING

When a large amount of gating must be performed in several places, it is often economical to perform this gating at the input of a pulse amplifier. The output pulse may then go directly to flip-flops and other pulsed units with the same results as if the gating had been performed at each unit being pulsed. Figure 1 illustrates a typical gated pulse amplifier.

For more information on mixed systems, see page 8

PULSE STANDARDIZATION

DEC Pulse Amplifiers are also useful in providing compatibility between the different series of DEC Modules. Since the modules are designed with compatibility in mind, the only differences between frequency lines are in the timing characteristics. In particular, pulses in the 10 megacycle line have a duration of 40 nanoseconds; in the 5 megacycle line, 70 nanoseconds; and in the 500 kilocycle line, 400 nanoseconds (0.4 microseconds).

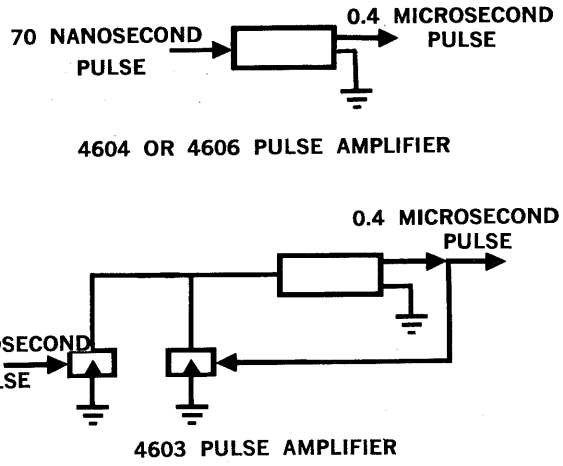


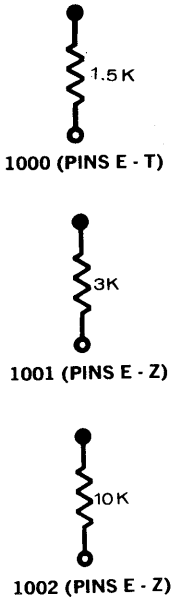
Figure 2 — PULSE STRETCHING

To produce a 0.4-microsecond pulse from a 70-nanosecond pulse, a Type 4603, 4604, or 4606 pulse amplifier may be used. The Types 4604 and 4606 do not require additional gating to perform this function; however, the Type 4603 requires a feedback loop which reduces the output driving ability somewhat.

CLAMPED LOAD RESISTORS
TYPES 1000, 1001, 1002

1000 SERIES

3 VOLT CLAMP LOAD RESISTORS



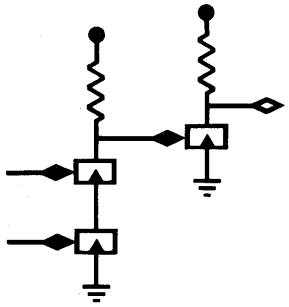


Figure 1 — SERIES INVERTER STRING DRIVING INVERTER BASE

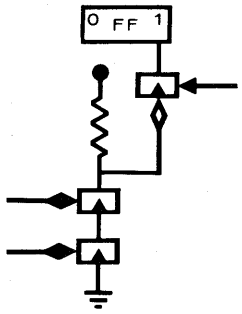


Figure 2 — SERIES INVERTER STRING DRIVING EMITTER OF PULSE GATE

The Types 1000, 1001 and 1002 are for use where extra standard loads, special lighter loads, or −3 volt sources are required.

The Type 1000 contains twelve standard clamped load resistors of 1500 ohms each. These may be used for clamping the voltage at the output of inverter collectors. A standard clamped load resistor presents 1 unit of DC Emitter Load when held at ground by an inverter. When not held at ground, the load resistor can drive 7 units of Base Load. (Output pins are E-T.)

The Type 1001 contains eighteen light clamped load resistors of 3000 ohms each. The load presented by a 3000-ohm resistor is ½ unit of DC Emitter Load. The driving capabilities are 3 units of Base Load. (Output pins are E-Z.)

The Type 1002 contains eighteen light clamped load resistors of 10,000 ohms each. These are particularly useful where a clamp which presents a light load is required, as in exclusive OR circuits. The load presented is 1/6 unit Emitter Load. The driving capability is 1 unit Base Load. A DEC inverter or diode gate can supply two Type 1002 resistors as well as a full unit of DC Emitter Load, providing this is in accordance with the rules for maximum series configurations for the specific gate used.

POWER: Type 1000: −15 volts/142 ma; **Type 1001:** −15 volts/134 ma; **Type 1002:** −15 volts/40 ma.

TYPICAL APPLICATIONS

CLAMPING LOGIC LEVELS

Standard clamped load resistors are used to establish the voltage level whenever a level gate output is required to drive inverter base inputs. They are also used whenever a level gate or a number of level gates are used to condition the emitter of a pulse gate. The 3000-ohm or 10,000-ohm clamped load resistor may be used for this latter purpose with 1000 Series Modules, if desired. A 1500-ohm load must be used with the 4000 Series Modules. Figures 1 and 2 illustrate these uses.

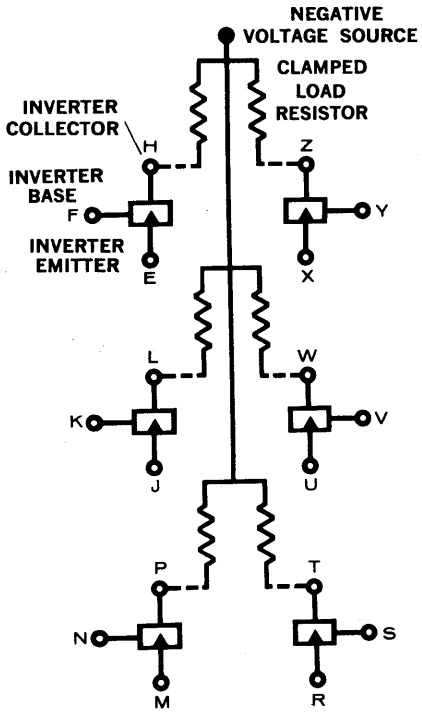
Any of the clamped load resistors may be used to permanently enable the level input to a negative capacitor-diode gate, Types 4125, 4127 and 4129. A 10,000-ohm clamped load resistor is used whenever it is desired to have the output of a level gate drive both an Emitter Load and a Base Load.

INVERTERS

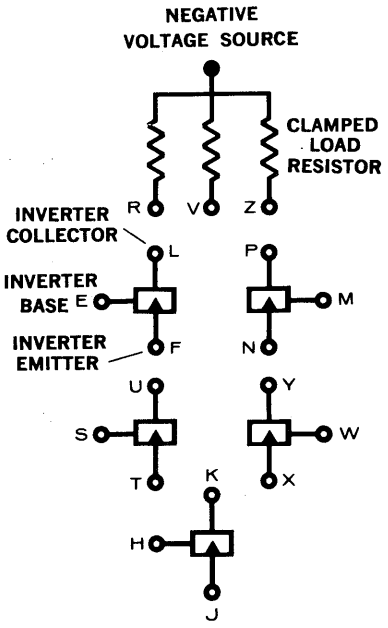
TYPES 1103, 1105

5 MEGACYCLES

1000 SERIES



1103 INVERTER



1105 INVERTER

Types 1103 and 1105 contain transistor inverters for use as pulse gates or level gates. Type 1103 has six inverters; Type 1105 has five. The clamped load resistors are available at output pins of the 1105 (three resistors). The six clamped load resistors in the 1103 are internally jumpered to the inverter collectors and may be clipped out as needed. The load resistors are all clamped to −3 volts. Delay through each inverter is approximately 20 nanoseconds.

INPUT: Base — DEC Standard 70 nanosecond Negative Pulses drive the inverter at any frequency up to 5 megacycles (1 unit of Pulse Load) when it is used as a pulse gate. As a level gate (1 unit of Base Load), the inverter uses DEC Standard Levels or the equivalent. **Emitter** — The inputs are DEC Standard Levels or the equivalent, including ground if emitter gating is not desired. When the collector is connected directly or through another inverter to a clamped load resistor, this input represents 1 unit of DC Emitter Load. If an emitter-collector path to a pulse gate exists, this input represents 1 unit of Pulsed Emitter Load.

OUTPUT: The collector may be connected directly to a clamped load resistor, to the emitter of another inverter, or to the gated input terminal of the flip-flop or other unit being pulsed. When used as a level gate, a collector connected to a load resistor can simultaneously drive (a) four units of Base Load at five megacycles or seven where speed is not a problem, (b) one-half unit of DC Emitter Load, and (c) any number of Pulsed Emitter Loads, providing not more than one is pulsed at a time. A collector with no clamped load resistor can be connected to several emitters, providing there is not more than one simultaneous emitter-collector path to a DC Emitter Load or to the pulse input of a flip-flop or other unit being pulsed. No more than three level gates can be connected in series. When a flip-flop drives the emitter of the first gate in the series string, the flip-flop must be counted as one of the inverters. When one of the series-connected gates is used as a pulse gate, four gates may be connected in series.

POWER: Type 1103: +10 volts (A)/0.9 ma; +10 volts (B)/0 ma; −15 volts/82 ma. **Type 1105:** +10 volts A/0.3 ma; +10 volts (B)/0.5 ma; −15 volts /52 ma.

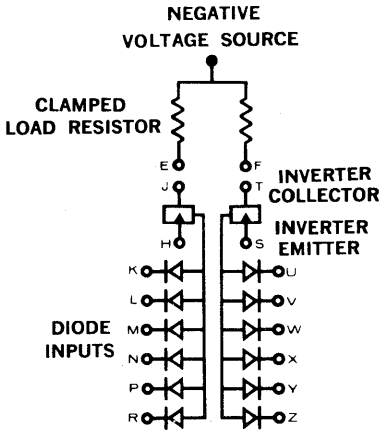
Additional information on inverter usage is included in the definition section.

DIODE GATES

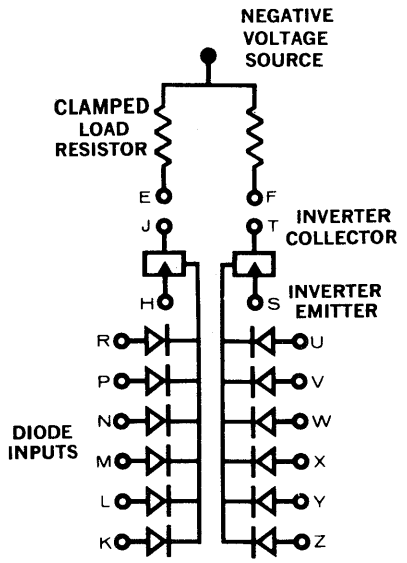
TYPES 1110, 1111

5 MEGACYCLES

1000 SERIES



1110 NEGATIVE DIODE NOR



1111 POSITIVE DIODE NOR

The Type 1110 consists of 2 six-input diode gates, each gate being connected to the base of a transistor inverter similar to a DEC Inverter Type 1105. The gates serve as NOR circuits for negative level inputs and NAND circuits for ground inputs. The gates may also be used to mix pulses. The emitter and collector of each transistor are available for external connections. Delay of a level through a diode and its inverter is approximately 30 nanoseconds; total transition time is typically 60 nanoseconds.

INPUT: Diodes — DEC Standard Levels, DEC Standard 70 nanosecond Negative Pulse or the equivalent, will supply the input. When the diodes are used as a level gate, the load is three units of Base Load shared among those inputs which are at a negative voltage. When the diodes are used for pulse mixing, each input is 1 unit of Pulse Load. **Emitter** — Same as Type 1105.

OUTPUT: Same as Type 1105.

POWER: −15 volts/42 ma; +10 volts (A)/1.3 ma; −10 volts (B)/1.3 ma.

See also 6000-series diode gates.

The Type 1111, like the Type 1110, contains 2 six-input diode gates, each connected to the base of a transistor inverter; however, this unit is a NOR circuit for ground level inputs and a NAND circuit for negative inputs. The emitter and collector of each inverter are available for external connections. Delay of a level through a diode and its inverter is approximately 30 nanoseconds. Typical total transition time for output fall is 50 nanoseconds; for output rise, 90 nanoseconds.

INPUT: Diodes — DEC Standard Levels or equivalent supply the input to the diodes; the load is ⅛ unit of DC Emitter Load shared by the ground inputs. This unit may not be used for gating pulses. **Emitter** — Same as Type 1105.

OUTPUT: Same as Type 1105.

POWER: −15 volts/45 ma; +10 volts (A)/0.2 ma; −10 volts (B)/0.2 ma.

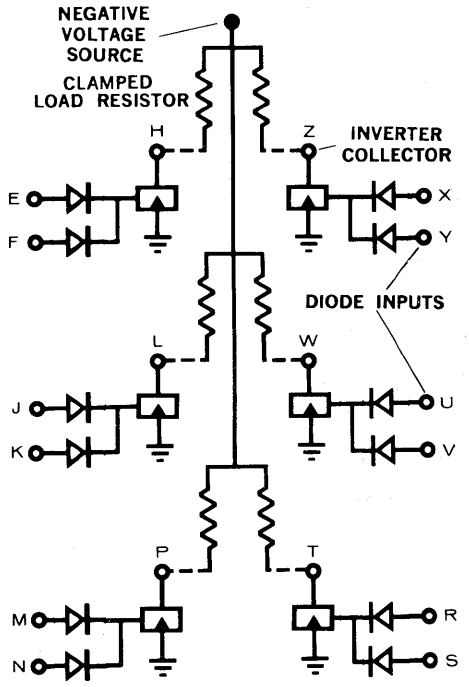
See also 6000-series diode gates.

DIODE GATES

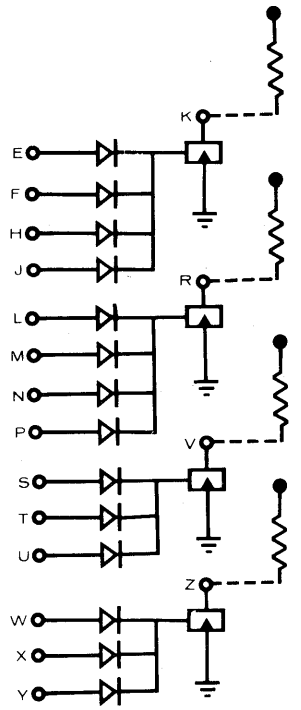
TYPES 1113, 1115, 1117

5 MEGACYCLES

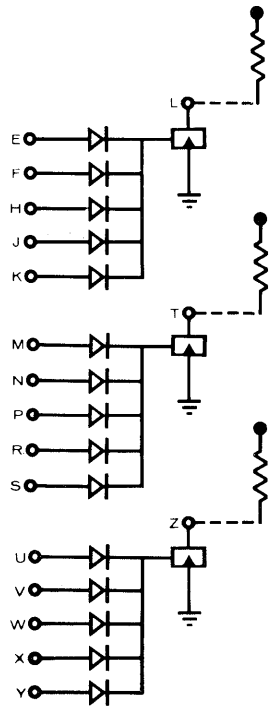
1000 SERIES



1113 POSITIVE DIODE NOR



1115 POSITIVE DIODE NOR



1117 POSITIVE DIODE NOR

Types 1113, 1115, and 1117 are like the Type 1111, except for the logical connection and the number of circuits in the module. The clamped load resistors are connected to the inverter collectors by internal jumpers (indicated by the dotted lines on the logic diagram). The jumpers are on lugs so they may be easily changed as needed.

See the Type 1111 for details on input and output signals.

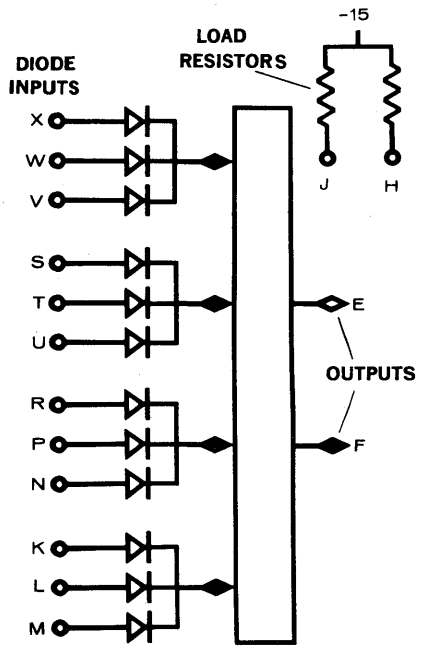
POWER: Type 1113: −15 volts/88 ma; +10 volts (A)/0.45 ma; +10 volts (B)/0.45 ma. **Type 1115** −15 volts/67 ma; +10 volts (A)/0.3 ma; +10 volts (B)/0.3 ma. **Type 1117** −15 volts/55 ma; +10 volts (A)/0.3 ma; +10 volts (B)/0.15 ma.

PARITY DECODER

TYPE 1130

5 MEGACYCLES

1000 SERIES



1130 THREE-BIT PARITY DECODER

Four three-input negative AND gates are OR'ed together to produce a circuit that is principally used for determining the parity of three binary bits. Units may be cascaded in a pyramid arrangement to determine parity of larger number of bits. Both polarity outputs are available. Delay is approximately 25 nanoseconds with light output loading.

INPUT: The inputs used are DEC Standard Levels or equivalent. Each three-input AND gate represents ½ unit of DC Emitter Load shared among those inputs which are at ground. (When this unit is used as a parity circuit with three sets of complementary level inputs, the maximum load presented to any input is ¾ unit of DC Emitter Load.)

OUTPUT: The Complementary DEC Standard Levels are produced at the output. When all inputs to any AND gate are negative, output pin F will be −3 volts and output pin E will be ground. Each output is capable of driving the input to Type 1130 used as a parity circuit, plus 7 units of Base Load, if speed is no problem. For maximum speed, the load should be restricted to one Type 1130 used as a parity circuit and 4 units of Base Load. If no Type 1130's are driven by the output, the two resistors available on the package may be connected to the outputs to increase the base driving ability. Each output is then capable of driving 12 units of Base Load where speed is no problem, or 7 units at high speed operation.

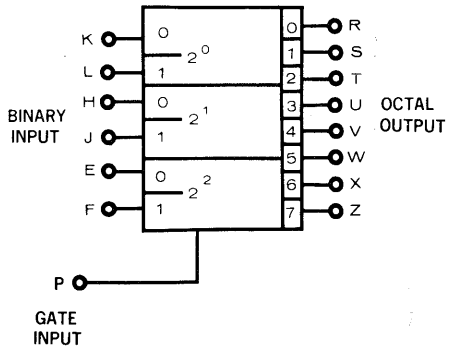
POWER: −15 volts/77 ma; +10 volts (A)/16 ma; +10 volts (B)/30 ma. The +10 volt (B) terminal should be connected to a fixed voltage supply. To avoid extreme power dissipation, the +10 volt (B) terminal voltage should not be increased significantly (as in marginal checking).

BINARY-TO-OCTAL DECODERS

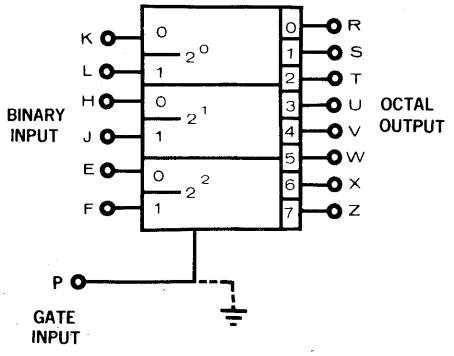
TYPES 1150, 1151

5 MEGACYLES

1000 SERIES



1150 BINARY-TO-OCTAL DECODER



1151 BINARY-TO-OCTAL DECODER

The Types 1150 and 1151 decode binary information from three flip-flops to octal form. For the Type 1150, the selected output line is at −3 volts, and the other seven outputs are at ground. For the Type 1151, the selected output line is at ground, while the other seven outputs are at −3 volts. If the gate signal is negative, all lines will be deselected. Decoding is accomplished by eight diode gates arranged so that each has a unique set of inputs. Type 1150 gates are similar to those of the Type 1110; Type 1151 gates resemble Type 1111's. The total transition time is less than 70 nanoseconds for the Type 1150 and less than 90 nanoseconds for the Type 1151.

INPUT: Type 1150: DEC Standard Levels or equivalent drive the decoder which represents five units of Base Load. If inputs L, J and F are at ground, output R is selected and is at −3 volts. The gate input represents four units of Base Load. Type 1151: DEC Standard Levels or equivalent drive the decoder which represents 0.3 unit of DC Emitter Load. If inputs K, H and E are at −3 volts, output R is selected and is at ground. The gate input is internally jumpered to ground when the unit is shipped. If the jumper is removed, pin P becomes a gate for all outputs. A −3 volt signal inhibits all outputs. Load of the gate input is one unit of DC Emitter Load.

OUTPUT: Each output is a standard inverter collector, connected internally to a clamped load resistor. Each output can simultaneously drive four units of Base Load at five megacycles (seven where speed is not a problem) and any number of Pulsed Emitter Loads, providing not more than one is pulsed at a time. The clamped load resistors are connected by jumpers. If these are removed, each output can drive one unit of DC Emitter Load.

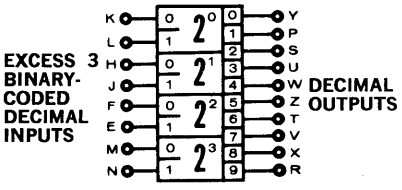
POWER: Type 1150: −15 volts/100 ma; +10 volts (A)/7 ma; +10 volts (B)/5.5 ma. **Type 1151:** −15 volts/88 ma; +10 volts (A)/1.2 ma; +10 volts (B)/0 ma.

BCD-TO-DECIMAL DECODER

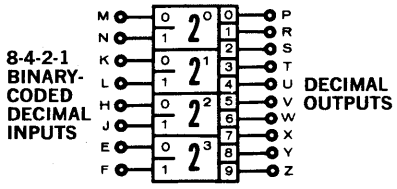
TYPE 1161

5 MEGACYCLES

1000 SERIES



1161 AS AN EXCESS 3 DECODER



1161 AS AN 8-4-2-1 DECODER

The Type 1161 Binary-Coded Decimal-to-Decimal Decoder is a diode matrix which decodes four complementary pairs of BCD input signals to produce an output on a selected decimal line. The ground-level output signal is produced from input signals in the 8-4-2-1 or excess 3 codes in which the binary ONE is represented by −3 volts and ZERO is ground potential. Total transition time, to raise a selected output line to ground level and return the 9 other ouput lines to −3 volts, is 90 nanoseconds.

Each diode negative AND gate is followed by a transistor inverter. Each of the 10 inverters is provided with a clamped load resistor which can be disconnected by removing a jumper wire. Although designed to decode the 8-4-2-1 or excess 3 BCD code, the Type 1161 can be used with other codes which require the following logic:

P = EHKM	V = JKN
R = EHKN	W = EJLM
S = HLM	X = JLN
T = HLN	Y = FM
U = JKM	Z = FHKN

INPUT: Standard DEC Levels, or equivalent, drive the decoder which represents 0.28 unit of DC Emitter Load per input (2.8 ma at ground, no load at −3 volts).

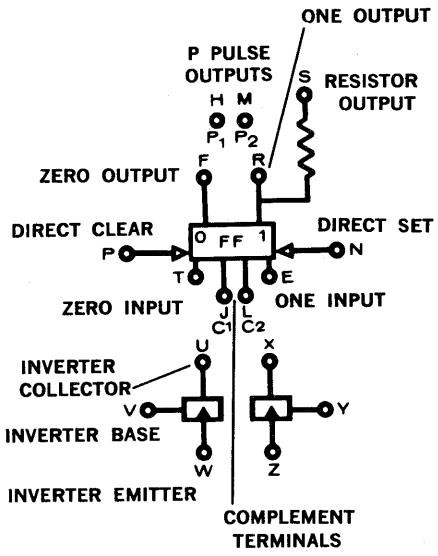
OUTPUT: Each inverter collector is connected to an internal clamped load, which may be disconnected. A collector connected to a load resistor can simultaneously drive: (a) 4 units of Base Load at 5 megacycles (7 where speed is not a problem); and (b) any number of Pulsed Emitter Loads, providing not more than one is pulsed at a time.

A collector with no clamped load can be connected to several emitters simultaneously, providing not more than one of the inverters is conducting at a time. No more than three level gates can be connected in series. When one of the series-connected gates is used as a pulse gate, four gates may be connected in series.

POWER: −15 volts/110 ma; +10 volts (A)/0 ma; +10 volts (B)/1.5 ma.

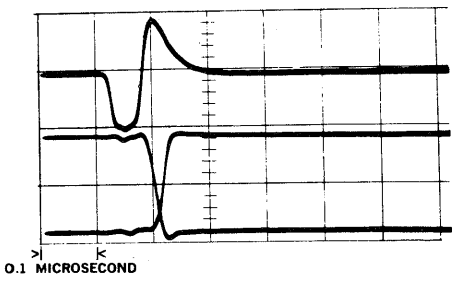
FLIP-FLOP
TYPE 1201
5 MEGACYCLES

1000 SERIES



1201 GENERAL PURPOSE FLIP-FLOP

DEC STANDARD 70 NANOSECOND NEGATIVE PULSE



1201 FLIP-FLOP OUTPUT

The Flip-flop Type 1201 is basically a two-transistor static flip-flop with built-in output amplifiers, Direct Set and Clear inputs, Gated Set and Clear inputs, two sources of counting carry pulses (P Pulse), two Complement inputs, and two inverter gates. It has sufficient built-in gating to be used as one digit of a shift register, or one digit of a binary counter. It can also be used for all general type logical operations. It has a built-in delay so that its output terminals can be sensed at the same instant that an input terminal is being pulsed, which is very useful in counter, shift register, and adder applications. A resistor coupled output suitable for driving a transistor indicator amplifier is available.

INPUT: Direct Clear and Direct Set require DEC Standard 70 nanosecond Positive Pulses (1 unit of Pulse Load). ZERO input, ONE input, and the Complement inputs each must come from the collector of a pulse gate. More than one pulse gate can be connected to the same terminal. The above signals can occur in any sequence, at any frequency, and at any time intervals which have a minimum of 0.2 microsecond between any two signals. (Maximum frequency is 5 megacycles.) The two inverters are similar to those included in the DEC Inverter Type 1105.

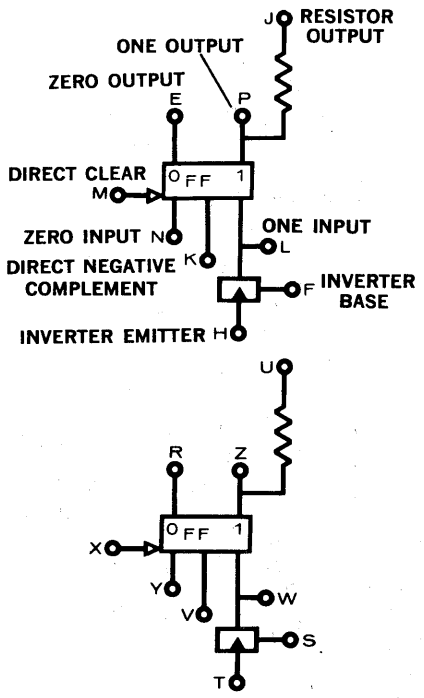
OUTPUT: ZERO output and ONE output provide DEC Standard Levels each capable of simultaneously driving: (a) 10 units of Base Load at 5 megacycles or 14 units where speed is not a problem; (b) 1 unit of DC Emitter Load; and (c) any number of Pulsed Emitter Loads, providing not more than one is pulsed at a time.

Each time the C_1 complement terminal is pulsed, a DEC Standard 70 nanosecond Negative Pulse, capable of driving 1 unit of Pulse Load, will occur on the P_1 terminal. P_2 and C_2 work the same way with respect to each other. Delay from the time the input inverter of either complement terminal is pulsed to the time the corresponding P Pulse occurs is approximately 20 nanoseconds.

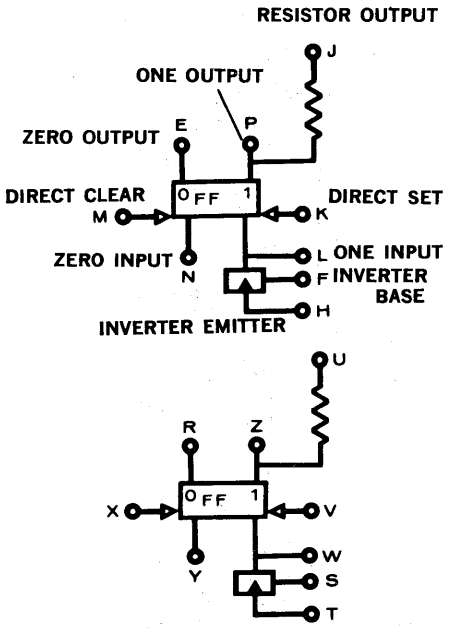
POWER: −15 volts/64 ma; +10 volts (A)/1.3 ma; +10 volts (B)/1.3 ma.

FLIP-FLOPS
TYPES 1204, 1209
5 MEGACYCLES

1000 SERIES



1204 DUAL FLIP-FLOP



1209 DUAL FLIP-FLOP

The 1204 Dual Flip-Flop is used in shift register, buffer register and control applications. The flip-flops are similar to the Type 1201 but do not have pulse outputs, and thus cannot be used in a counter. The inverters are the same as the Type 1105.

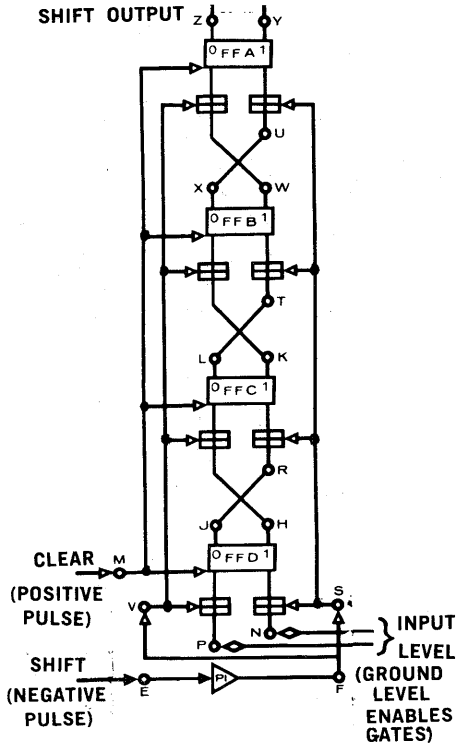
INPUTS: Same as 1201. In addition, the complement input on the 1204 has jumpers which permit it to be modified to accept a DEC Standard 70 nanosecond Negative Pulse. The load is a 2½ unit pulse load. Jumpering instructions are included on the test data sheet shipped with the module.

OUTPUTS: Same as Type 1201.

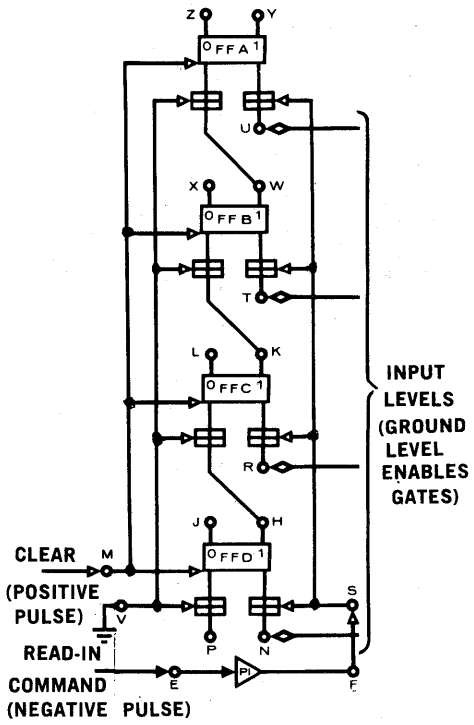
POWER: Type 1204: −15 volts/108 ma; +10 volts (A)/2.4 ma; +10 volts (B)/2.4 ma. **Type 1209:** −15 volts/108 ma; +10 volts (A)/2.4 ma; +10 volts (B) /2.4 ma.

FLIP-FLOPS
TYPE 1213
3 MEGACYCLES

1000 SERIES



1213 AS A SHIFT REGISTER



1213 AS A BUFFER REGISTER

The Type 1213 contains four flip-flops with associated gates for connection as a shift or buffer register. A pulse inverter is included for driving the capacitor-diode gates during either a read-in or a shift operation. The flip-flops can be individually set or cleared by connecting pulse gates (such as DEC Type 1105 inverters) to the proper output terminals. The maximum operating frequency is 3 megacycles.

INPUT: Pulse Inverter Input — A DEC Standard 70 nanosecond Negative Pulse (1 unit of Pulse Load). **Clear Input** — A DEC Standard 70 nanosecond Positive Pulse (1 unit of Pulse Load per flip-flop). Clear pulses may precede read-ins by as little as 0.2 microsecond. **Shift One** and **Shift Zero Inputs** — May be driven only by the output of the included pulse inverter. **Level Inputs** — Are DEC Standard Levels or equivalent (ground for assertion). There is no DC Load at these points. The transient load approximates 1 unit of Base Load. The level must be present at least 0.3 microsecond before a shift operation and 0.5 microsecond before a read-in operation. The flip-flops may be set or cleared by connecting an inverter to the appropriate output terminal. The emitter of the inverter must be permanently grounded. When the inverter is pulsed the flip-flop output to which it is connected is grounded.

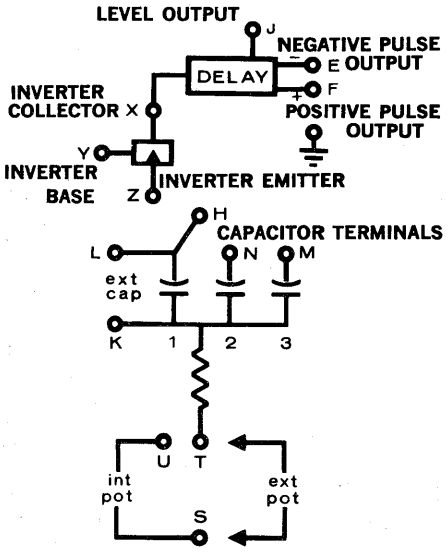
OUTPUT: One Output and **Zero Output** from each flip-flop provide DEC Standard Levels each capable of simultaneously driving: a) 2 units of Base Load and b) 1 capacitor-diode gate level input. The outputs are unbuffered and the delay is; therefore, short compared to the 70 nanosecond pulse width. When the flip-flop output is to be sampled and changed at the same time, provision must be made for a logical delay. This delay may be provided by the use of a capacitor-diode gate or three cascaded inverters.

Pulse Inverter Output — A positive 3 volt pulse from a DC level of −3 volts. This can only drive the Shift 1 and/or the Shift 0 gates included in the plug-in unit.

POWER: −15 volts/98 ma; +10 volts (A)/0.5 ma; +10 volts (B)/0.5 ma.

DELAYS
TYPE 1304
1.5 MEGACYCLES

1000 SERIES



1304 DELAY (ONE SHOT)

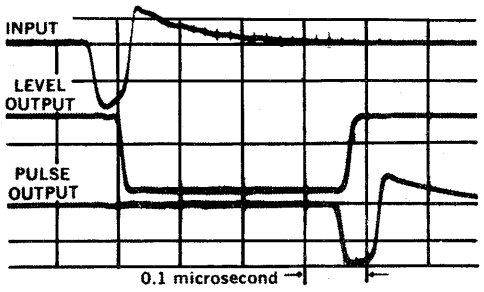


Figure 1 — INPUT AND OUTPUT VS TIME

The Type 1304 delay unit is a mono-stable multivibrator. When the input terminal is grounded, either through the inverter or externally, the level output terminal will switch from its normal ground level to −3 volts for a predetermined, but adjustable, period of time and then back to ground. A pulse transformer generates a DEC Standard 70 nanosecond Pulse at the pulse output during the final transition. The pulse transformer has both positive and negative terminals so that either polarity pulse may be obtained. Typical output and input wave forms are shown in Figure 1. The delay interval is determined primarily by the capacitor connection (3 capacitors are available). An internal 15,500 ohm potentiometer provides for the fine adjustment. The capacitor 1 will permit adjustment from approximately 0.25 microsecond to 2.5 microseconds; 2, from approximately 2.5 microseconds to 35 microseconds; and 3, from approximately 35 microseconds to 500 microseconds. A longer delay may be accomplished by installing an additional capacitor between the external capacitor terminals. Terminals U and T must be jumpered to use the internal potentiometer for fine control. Circuit recovery time is equal to 20% of the maximum delay available on that particular circuit's capacitor connection.

A 20% change in power supply voltage will change the delay less than 1%. Delay jitter (due to power supply ripple) is less than 0.3%.

INPUT: The input to the delay is a DEC Standard 70 nanosecond Negative Pulse on the base of a pulse gate, such as the one included in the delay module. The base of the built-in pulse gate represents 1 unit of Pulse Load. If more logical inputs are desired, they can be provided by connecting pulse gate collectors to the collector of the built-in pulse gate. Mixing of several pulses can also be accomplished by using half of a DEC Diode Type 1110 with DEC Standard 70 nanosecond Negative Pulses applied to the diodes and the collector tied to the collector of the built-in pulse gate.

OUTPUT: Level — When the input is pulsed, a negative DEC Standard Level occurs for the duration of the delay interval. This level is capable of simultaneously driving: (a) 8 units of Base Load if speed is important, otherwise 12 bases; (b) 1 unit of DC Emitter Load; and (c) any number of Pulsed Emitter Loads, providing not more than one is pulsed at a time. **Pulse** — At the end of the delay interval, a DEC Standard 70 nanosecond Pulse occurs. The output pulse will be negative if the positive terminal is grounded; it will be positive if the negative terminal is grounded. This signal can drive 8 units of Pulse Load.

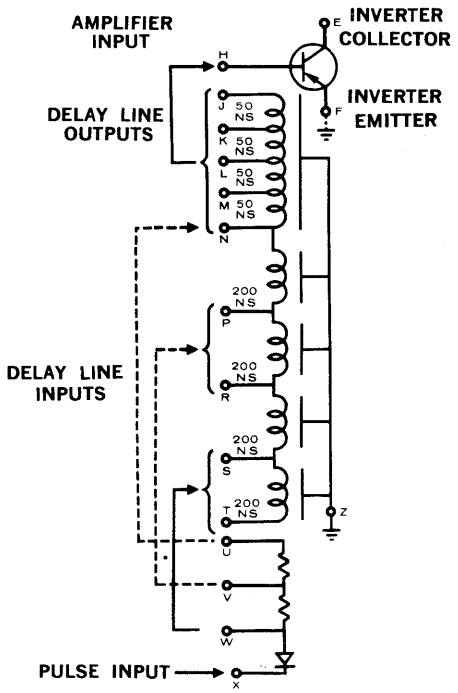
POWER: −15 volts/80 ma; +10 volts (A)/0.6 ma; +10 volts·(B)/0 ma.

DELAYS

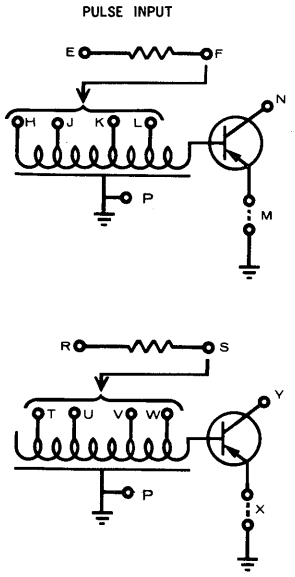
TYPES 1310, 1311, 1316

5 MEGACYCLES

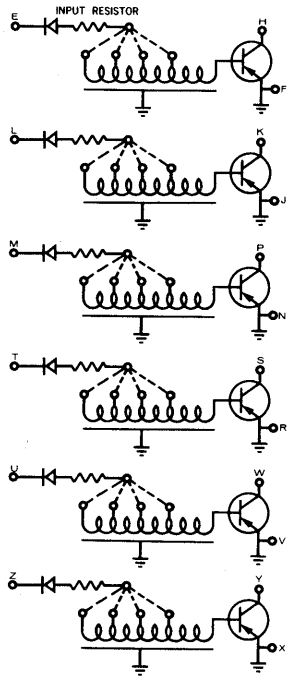
1000 SERIES



1310 DELAY LINE
(UP TO 1 MICROSECOND)



1311 DELAY LINE
(UP TO 200 NANOSECONDS)



1316 DELAY LINE
(UP TO 200 NANOSECONDS)

Types 1310, 1311 and 1316 Delay Lines may be used to delay DEC Standard 70 nanosecond Pulses. Delay increments are adjustable in steps of 50 nanoseconds. In the Types 1311 and 1316 each delay line is 200 nanoseconds long with taps at 50-nanosecond intervals. The input pulse goes through a resistor diode combination into the appropriate tap on the delay line. In the 1311, delay line taps are brought out to the module connector. In Type 1316, the taps are brought to lugs inside the module. The delay through the output transistor is approximately 20 nanoseconds. This should be added to the total through the line. The 1310 will delay pulses for up to one microsecond. The primary input is pin X. Additional inputs may be OR'ed into pin W through external high speed diodes such as the 1N994. Duration of the delay is set by jumpering one of the delay line inputs to pins U, V or W and one of the delay line outputs to pin H. The output transistor is not a standard inverter and must be driven only from the delay line. The output transistor has a delay of approximately 20 nanoseconds which must be added to the total delay. The Type 1310 may also be used to delay 4000 series pulses. In this case, the minimum delay is 800 nanoseconds and pin U must be jumpered to pin T.

INPUT: The input should be a DEC Standard 70 nanosecond Negative Pulse or its equivalent. The Type 1310 represents 5 units of Pulse Load; the Types 1311 and 1316 represent 3 units of Pulse Load each.

OUTPUT: The emitter of the output inverter must be grounded; the transistor's collector should be connected to the input of a DEC Pulse Amplifier Type 1607 or other unit being pulsed. However, if additional logic gating is required, it may be done with up to three transistor inverters placed in series between the collector and the pulse amplifier.

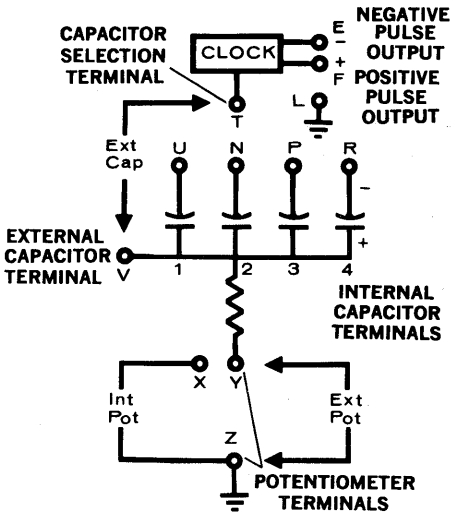
POWER: Type 1310: −15 volts/0 ma; +10 volts (A)/2.1 ma; +10 volts (B)/0 ma. **Type 1311:** −15 volts/0 ma; +10 volts (A)/1.0 ma; +10 volts (B)/1.0 ma. **Type 1316:** −15 volts 10 ma; +10 volts (A)/2 ma; +10 volts (B)/2 ma.

CLOCKS

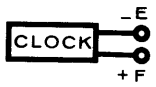
TYPES 1404, 1406

5 MEGACYCLES

1000 SERIES



1404 VARIABLE CLOCK



1406 CRYSTAL CLOCK

The frequency of the Type 1404 Variable Clock can be varied from 500 cycles/second to 5 megacycles/second. Four scales provide coarse frequency control, and a built-in 20,000-ohm potentiometer permits fine adjustment. Terminals for an external potentiometer are available. Lower frequencies may be obtained by adding an external capacitor between pins V and T. A 20% change in the power supply voltage will change the prf less than 1% and its pulse-to-pulse jitter is less than 0.2%.

The Type 1406 employs a series resonant crystal oscillator circuit and pulse shaping buffer amplifiers to provide very precise timing. The amplifiers produce DEC Standard 70 nanosecond Pulses in the 500 kilocycle to 5 megacycle range. The clock frequency, specified by the customer, is stamped on the crystal. The 1404 and 1406 have the same output connection.

OUTPUT: The output is a DEC Standard 70 nanosecond Pulse which occurs at the preselected frequency. The pulse may be made either positive or negative by grounding the appropriate output terminal. The signal can drive 8 units of Pulse Load.

Crystal Clock: The stability of the crystal clock's output frequency is 0.01% over a temperature range of −20 to +55°C.

OUTPUT: Same as Type 1304 pulse output

POWER: Type 1404: −15 volts/66 ma; +10 volts (A)/0 ma; +10 volts (B)/0 ma. **Type 1406:** −15 volts/171 ma; +10 volts (A)/0 ma; +10 volts (B)/0 ma.

TYPICAL APPLICATIONS

SYNCHRONIZATION

A typical application is the synchronization of DEC Variable Clocks to a DEC Crystal Clock to obtain the desirable features of both the crystal and variable clocks. Provide the DEC Crystal Clock Type 1406 with a simple resistive attenuator whose output (capacity coupled) can be used as the standardization signal for the variable clocks used in the system. Synchronization signal amplitudes of from one-tenth to several tenths of a volt peak to peak are most satisfactory. The signal of the crystal clock is applied to the capacitor of the variable clock at pin V. (This signal must be applied through a blocking capacitor with an impedance on the order of 1000 ohms at the operating frequency.)

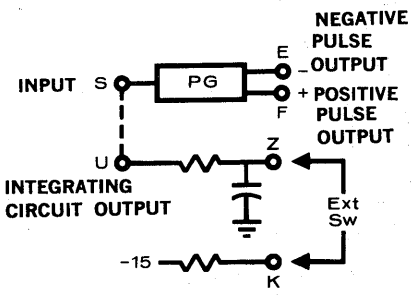
As in all synchronizing schemes, the smaller the synchronization signal, the less reliable is the lock and the more tendency there is over a long period of time for small variations in the natural free running frequency of the multivibrator to cause the locking action to become intermittent or fail. There may be cases, however, in which it is desirable to be able to synchronize the variable clock in a special ratio to the synchronizing frequency for a short period of time (e.g. 2/3, 4/3, 5/7) to perform a single experiment, and in these cases the locking reliability for the weak inputs required will be found to be satisfactory.

PULSE GENERATORS

TYPE 1410

2 MEGACYCLES

1000 SERIES



1410 PULSE GENERATOR

The Type 1410 converts external signals to DEC Standard Pulses. A Schmitt circuit produces a DEC Standard 70 nanosecond Pulse at the output every time the input voltage goes more negative than −2.5 volts after having been more positive than −1.0 volts. This unit also contains an integrating circuit to filter contact bounce when a switch or relay is used to generate the pulse.

INPUT: Pulse Generator — The input is a DC connection, thereby eliminating fall time as a characteristic of the incoming signal. Input impedance is 3000 ohms. The input signal should stay between +10 volts and −10 volts. The input can come from an external source or from the output of the integrating circuit. **Integrating Circuit** — The two inputs to this circuit come from switch or relay outputs.

OUTPUT: Pulse Generator — The output is a DEC Standard 70 nanosecond Pulse. The pulse will be negative if the positive terminal is grounded; it will be positive, if the negative terminal is grounded. The maximum prf is 2 megacycles. This signal can drive 8 units of Pulse Load. **Integrating Circuit:** The time constant of the integrating circuit is 12 milliseconds.

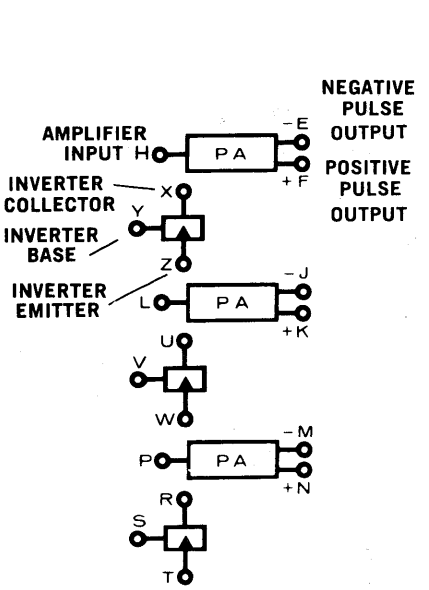
POWER: −15 volts/34 ma; −3 volts/0 ma; +10 volts (A)/5 ma; +10 volts (B)/5 ma.

PULSE AMPLIFIERS

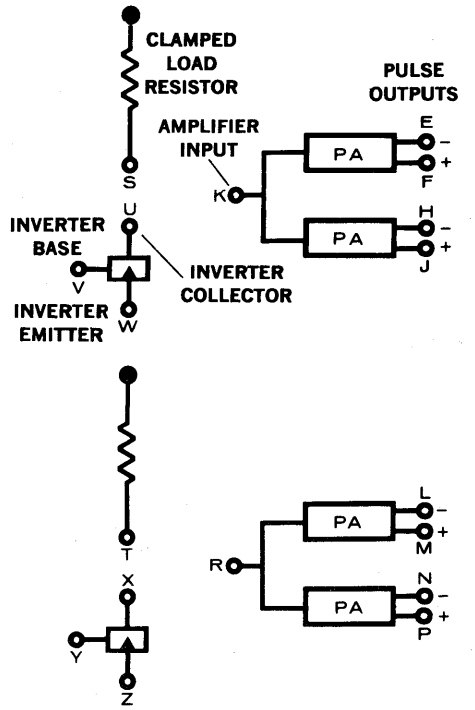
TYPES 1607, 1608, 1609

5 MEGACYCLES 2.5 MEGACYCLES

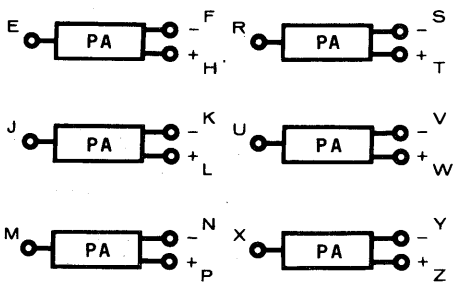
1000 SERIES



1607 PULSE AMPLIFIER



1608 DUAL PULSE AMPLIFIER



1609 PULSE AMPLIFIER

INPUT: Types 1607 and 1608: The input of the pulse amplifier is the collector of a pulse gate — either an inverter or a Type 1110 Diode Gate. To mix pulse sources, many inverters may be tied together. The input to the pulse gate, whose collector drives the pulse amplifier (it may pass through some level gates on the way), is normally a DEC Standard 70 nanosecond Negative Pulse. However, any negative pulse having an amplitude between 2.0 and 5.0 volts, leading edge less than 50 nanoseconds and width (at 2 volts) greater than 50 nanoseconds can be used. A $\pm 4\frac{1}{4}$-volt, 2-megacycle sine wave will meet this requirement. Input pulses of less than -0.5 volts will not generate an output pulse. The Type 1609 is the same as the 1607 and 1608 except that the input pulse width can be as narrow as 25 nanoseconds. Input leads should be kept short.

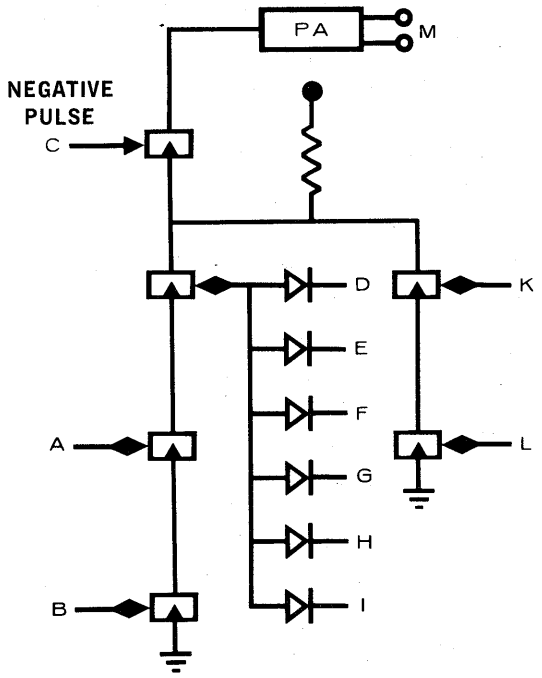
Types 1607, 1608 and 1609 Pulse Amplifiers are used for clearing, jamming and shifting the contents of flip-flop registers, for sending pre-gated information to a variety of loads and for amplifying and standardizing pulses. The Types 1607 and 1608 will increase the driving power of the input pulse, standardize the amplitude and reduce the duration of wide input pulses. With an external feedback connection these units will also increase the duration of the 40 nanosecond pulse to 70 nanoseconds. These units will operate up to five megacycles. The inverters and clamped load resistors are the same as in the Type 1105. The Type 1609 is less powerful than the 1607 and 1608, but it will standardize the duration of both 0.4-microsecond and 40-nanosecond pulses. It will operate up to 2.5 megacycles.

OUTPUT: Type 1607 and 1608: The output is a DEC 2.5 volt, 70 nanosecond Pulse which occurs at the output every time the input signal meets the input requirement. Each pulse amplifier output is an independent transformer winding, which may be used to produce positive or negative pulses by grounding the appropriate terminal. Transformers may be connected in parallel to increase the driving power or in series to increase the pulse amplitude for driving external devices. Each output is capable of driving 16 units of Pulse Load. A terminating resistor of 25 to 100 ohms should be used at the farthest load. **Type 1609:** Similar to 1607 and 1608 but will drive only 10 units pulse load.

POWER: Type 1607: -15 volts/136 ma; $+10$ volts (A)/0.3 ma; $+10$ volts (B)/0.15 ma. **Type 1604:** -15 volts/160 ma; $+10$ volts (A)/0.15 ma; $+10$ volts (B)/0.15 ma. **Type 1609:** -15 volts/200 ma; $+10$ volts (A)/10 ma; $+10$ volts (B)/10 ma.

TYPICAL APPLICATION

LOGICAL GATING



$$M = C[A \cdot B(D+E+F+G+H+I)+K \cdot L]$$

Figure 1 — PULSE AMPLIFIER GATING

When a large amount of gating must be performed in several places, it is often economical to perform this gating before a pulse amplifier. The output pulse may then go directly to flip-flops and other pulsed units with the same results as if the gating had been performed at each unit being pulsed. Figure 1 illustrates a typical gated pulse amplifier.

For more information on mixed systems, see page 8

PULSE STANDARDIZING

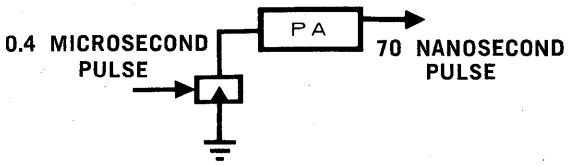


Figure 2 — REDUCING PULSE DURATION

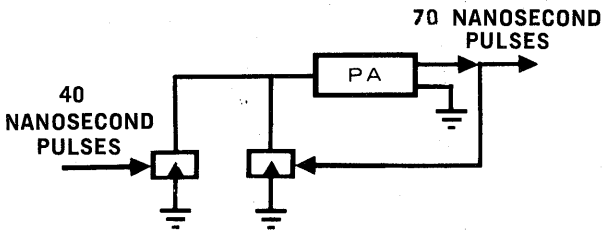


Figure 3 — INCREASING PULSE DURATION

DEC Pulse Amplifiers are also useful in providing compatibility between the different series of DEC Modules. Since the modules are designed with compatibility in mind, the only differences between frequency lines are in the timing characteristics. In particular, pulses in the 10 megacycle line have a duration of 40 nanoseconds in the 5 megacycle line, 70 nanoseconds; and in the 500 kilocycle line, 400 nanoseconds (0.4 microseconds).

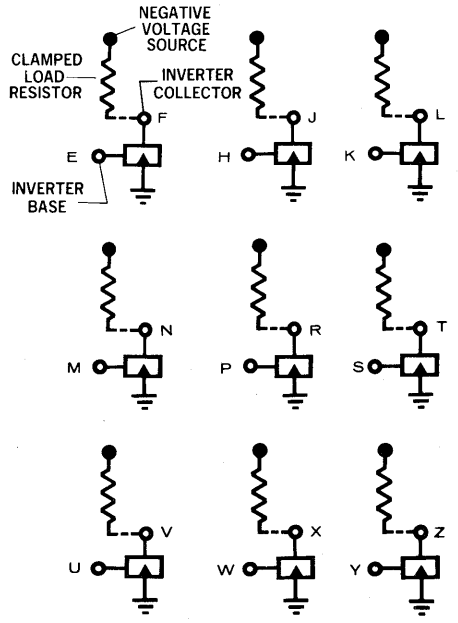
To produce a 70-nanosecond pulse from an 0.4 microsecond pulse, the Types 1607, 1608 or 1609 Pulse Amplifier is used, as shown in Figure 2. To produce a 70-nanosecond pulse from a 40-nanosecond pulse, the Types 1607 or 1608 may be used with a feedback loop. This method, as shown in Figure 3, produces a full duration pulse, but reduces the output driving ability slightly. The Type 1609 will produce a 70-nanosecond pulse from a 40-nanosecond pulse directly.

INVERTERS

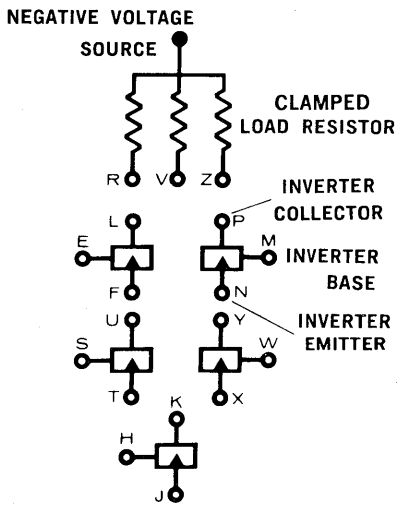
TYPES 6102, 6105, 6106

10 MEGACYCLES

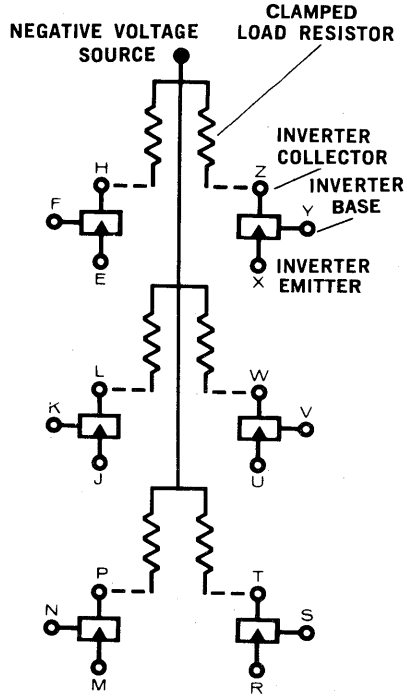
6000 SERIES



6102 INVERTER



6105 INVERTER



6106 INVERTER

The Type 6102, 6105 and 6106 Transistor Inverters are for use as pulse or level gates. Clamped load resistors are available at the output pins of the 6105. In the 6102 and 6106 the clamped loads are internally jumpered to the inverter collectors and may be clipped out as required. Delay through each inverter is approximately 12 nanoseconds.

INPUT: Base: Inputs are DEC Standard 40 nanosecond Negative Pulses when the inverter is used as a pulse gate at any frequency up to 10 megacycles (one unit of Pulse Load). Inputs are DEC Standard Levels or equivalent when the inverter is used as a level gate (one unit of Base Load).

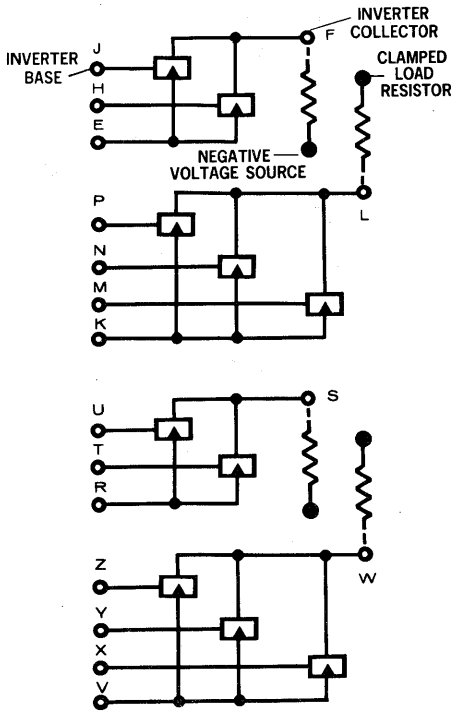
Emitter: The inputs are DEC Standard Levels or equivalent, including grounding if emitter gating is not desired. If the collector is connected directly or through another inverter to a clamped load resistor, this input represents one unit of DC Emitter Load. If an emitter-collector path to a pulse gate exists, this input represents one unit of Pulsed Emitter Load.

OUTPUT: The collector may be connected directly to a clamped load resistor, to the emitter of another inverter, or to the gated input terminal of the flip-flop or other unit being pulsed. When used as a level gate, a collector connected to a load resistor can drive two units of Base Load and 0.5 units of DC Emitter Load at ten megacycles, or seven units of Base Load and 0.5 units of DC Emitter Load at slower speeds. A collector can be connected to several emitters simultaneously, providing not more than one of the inverters is conducting at a time. No more than two level gates can be connected in series. When a flip-flop drives the emitter of the first gate in the series string, the flip-flop must be counted as one of the inverters. When one of the series-connected gates is used as a pulse gate, three gates may be connected in series. The pulse gate must be placed at the beginning of the string (the end furthest from the load).

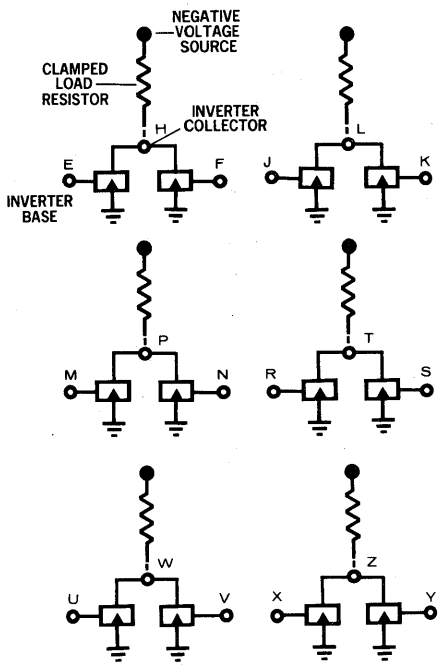
POWER: Type 6102: −15 volts/135 ma; + 10 volts (A)/1.4 ma; +10 volts (B)/0 ma. **Type 6105:** −15 volts/52 ma; +10 volts (A)/0.5 ma; +10 volts (B) /0.3 ma. **Type 6106:** −15 volts/82 ma; +10 volts (A)/0.5 ma; +10 volts (B)/0.5 ma.

INVERTERS
TYPES 6109, 6122, 6123, 6124
10 MEGACYCLES

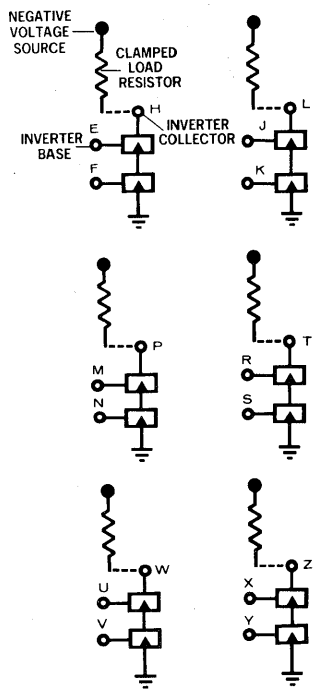
6000 SERIES



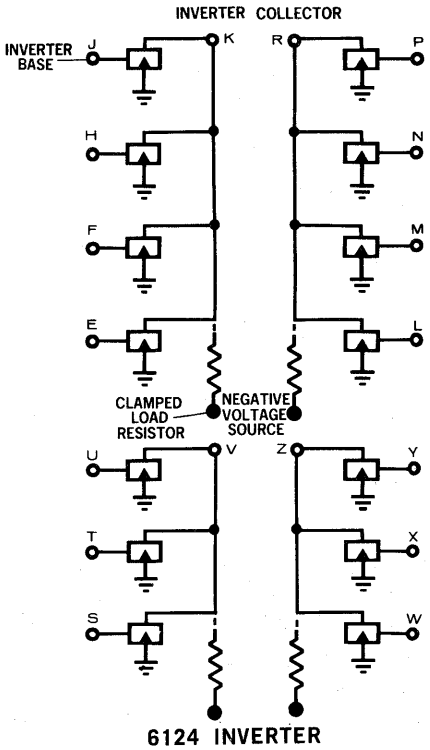
6109 INVERTER



6122 INVERTER



6123 INVERTER



6124 INVERTER

The Types 6109, 6122, 6123 and 6124 contain multiple inverters which are prewired to form different logical functions. The even numbered types are NOR gates for negative signals and NAND gates for positive signals. The odd numbered gates form a NOR circuit for positive inputs and a NAND for negative inputs. The individual inverters and clamped load resistors are identical to those in the Type 6106. The loads are internally jumpered to the collectors of inverter sets and may be removed as required.

POWER: Type 6109: −15 volts/65 ma; +10 volts (A)/1.5 ma; +10 volts (B)/0 ma. **Type 6122:** −15 volts/84 ma; +10 volts (A)/2 ma; +10 volts (B)/0 ma. **Type 6123:** −15 volts/80 ma; +10 volts (A)/2 ma; +10 volts (B)/0 ma. **Type 6124:** −15 volts/70 ma; +10 volts (A)/2.5 ma; +10 volts (B)/0 ma.

INVERTER USAGE

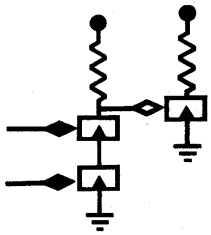


Figure 1

The high speed transistors used in 10 megacycle inverters have a larger saturation voltage drop than the transistors used in the 5 megacycle and 500 kilocycle inverters. Because of this slightly larger DC drop, a maximum of two inverters may be put in series if the output is to drive another inverter. (See Figure 1). If a flip-flop output is driving an inverter emitter, this flip-flop must be counted as an inverter. (See Figure 2)

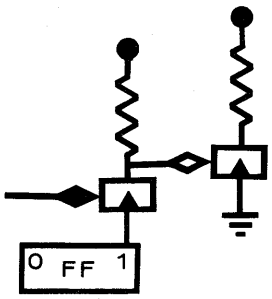


Figure 2

When the output of a series of transistor inverters is driving the input of a flip-flop or pulse amplifier, as in Figure 3, an inverter pulse gate may be added in series with the two level gates. This pulsed inverter must be placed at the bottom of the series string; that is, the end farthest from the load. The emitter may be driven by a flip-flop unless the sampling pulse is a P pulse (the carry pulse in counters); in this case the emitter should be grounded.

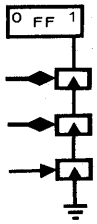


Figure 3

When connecting 10 MC inverters, the user should avoid wiring inductance and stray capacitance as much as possible. Figure 4 illustrates how a wire which is conducting current for two pulsed inverters back to the flip-flop output, may serve as a coupling connection between the two pulsed inverters and produce ringing. This ringing may produce a positive pulse on the emitter of the other inverter, thus turning it on at the wrong time. To avoid this, each emitter must be driven by a separate wire, unless the distance is very short. For maximum noise rejection and widest voltage margins, it is recommended that all unused inverter inputs be grounded.

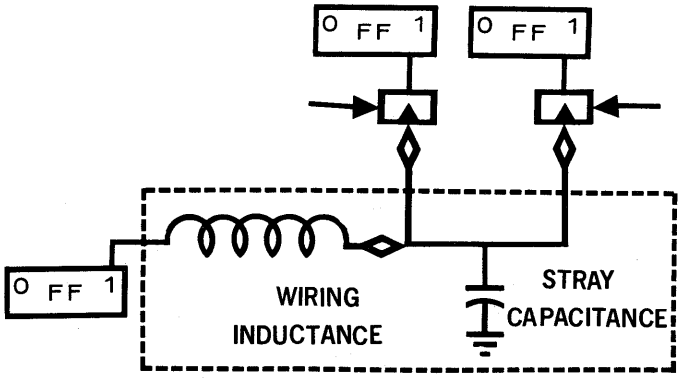


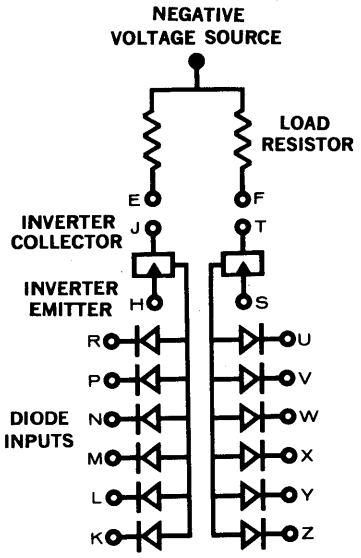
Figure 4

DIODE GATES

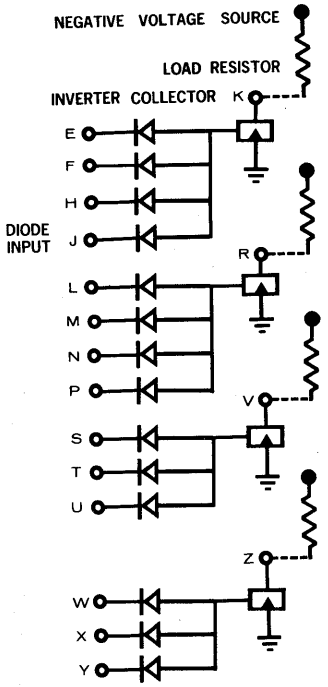
TYPES 6110, 6114, 6116, 6118

10 MEGACYCLES

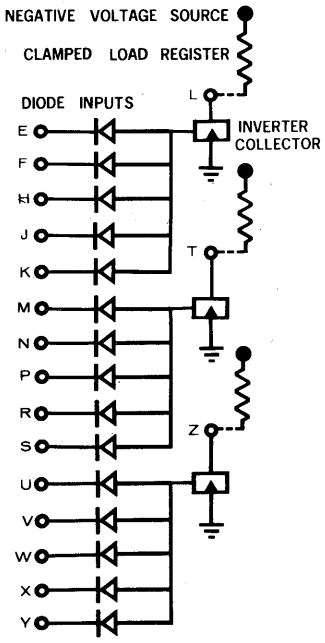
6000 SERIES



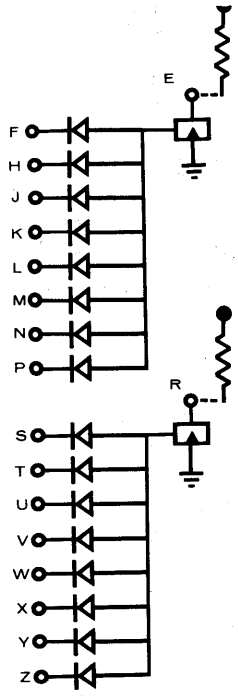
6110 NEGATIVE DIODE NOR



6114 NEGATIVE DIODE NOR



6116 NEGATIVE DIODE NOR



6118 NEGATIVE DIODE NOR

The negative diode NOR's contain multiple input diode gates, each attached to the base of a transistor inverter. The gates form a NOR circuit for negative inputs and a NAND circuit for ground inputs. These units may also be used with the 1000-series for mixing negative pulses but may not be used with 40-nanosecond pulses. Typical response times are a 30-nanosecond delay, 50-nanosecond output total transition rise time and 70-nanosecond total transition fall time.

INPUT: Diodes: DEC Standard Levels and/or DEC Standard 70 (or more) nanosecond Negative Pulses. When used as a level gate the load is three units of Base Load shared among those inputs with −3 volts on them. When used as a pulse gate, each input is one unit of Pulse Load. **Emitter:** (6110 only) Same as 6106.

OUTPUT: Same as 6106.

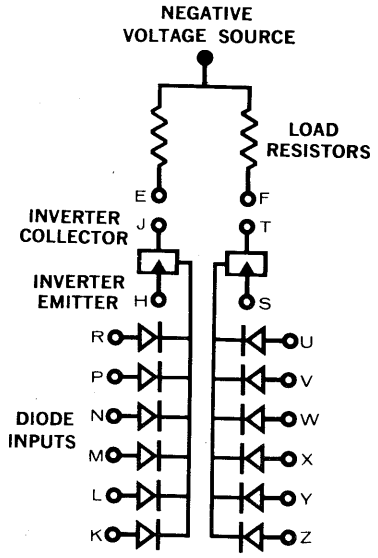
POWER: Type 6110: −15 volts/45 ma; +10 volts (A)/2.5 ma; +10 volts (B)/2.7 ma. **Type 6114:** −15 volts/67 ma; +10 volts (A)/10 ma; +10 volts (B)/11 ma. **Type 6116:** −15 volts/55 ma; +10 volts (A)/7.5 ma; +10 volts (B)/4.3 ma. **Type 6118:** −15 volts/35 ma; +10 volts (A)/2.5 ma; +10 volts (B)/2.7 ma.

DIODE GATES

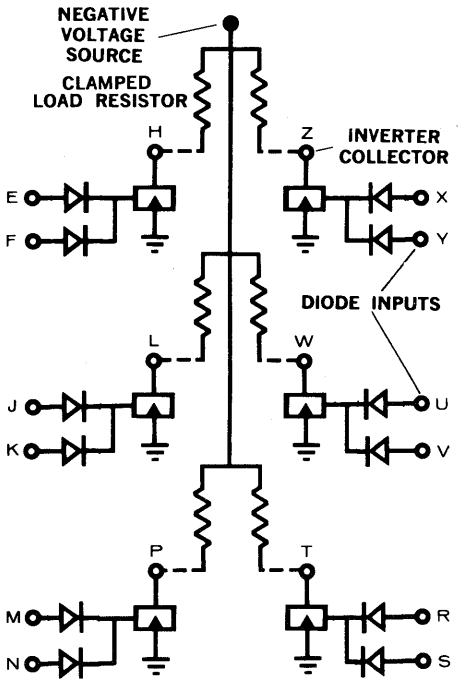
TYPES 6111, 6113, 6115, 6117, 6119

10 MEGACYCLES

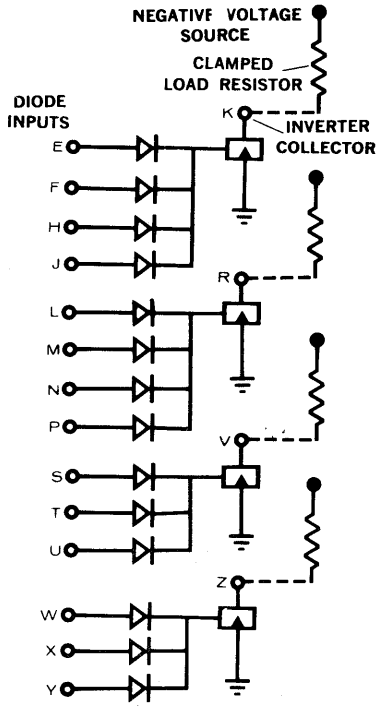
6000 SERIES



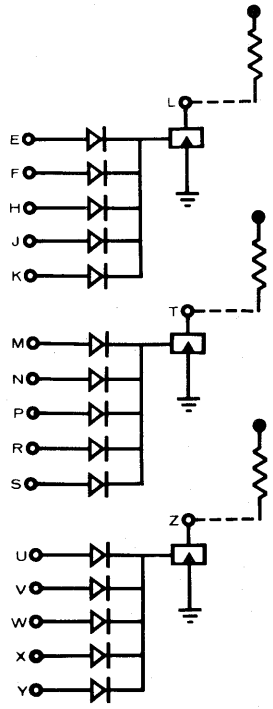
6111 POSITIVE DIODE NOR



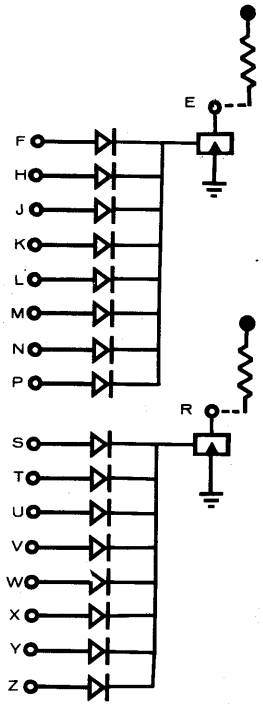
6113 POSITIVE DIODE NOR



6115 POSITIVE DIODE NOR



6117 POSITIVE DIODE NOR



6119 POSITIVE DIODE NOR

The positive diode NOR's are similar to the negative diode NOR's except that they form NOR circuits for ground inputs and NAND circuits for negative inputs. These units may be used with 1000-series modules to AND a 70-nanosecond negative pulse with a group of negative levels, but may not be used with 40 nanosecond pulses. Typical response times are a 20-nanosecond delay, 60-nanosecond total transition rise time, and 50-nanosecond total transition fall time.

INPUT: Diodes: DEC Standard Levels and/or DEC Standard 70 nanosecond or more Negative Pulses. The load is 1/8 unit of DC Emitter Load shared among the grounded inputs. **Emitter:** (6111 only) Same as 6106.

OUTPUTS: Same as 6106.

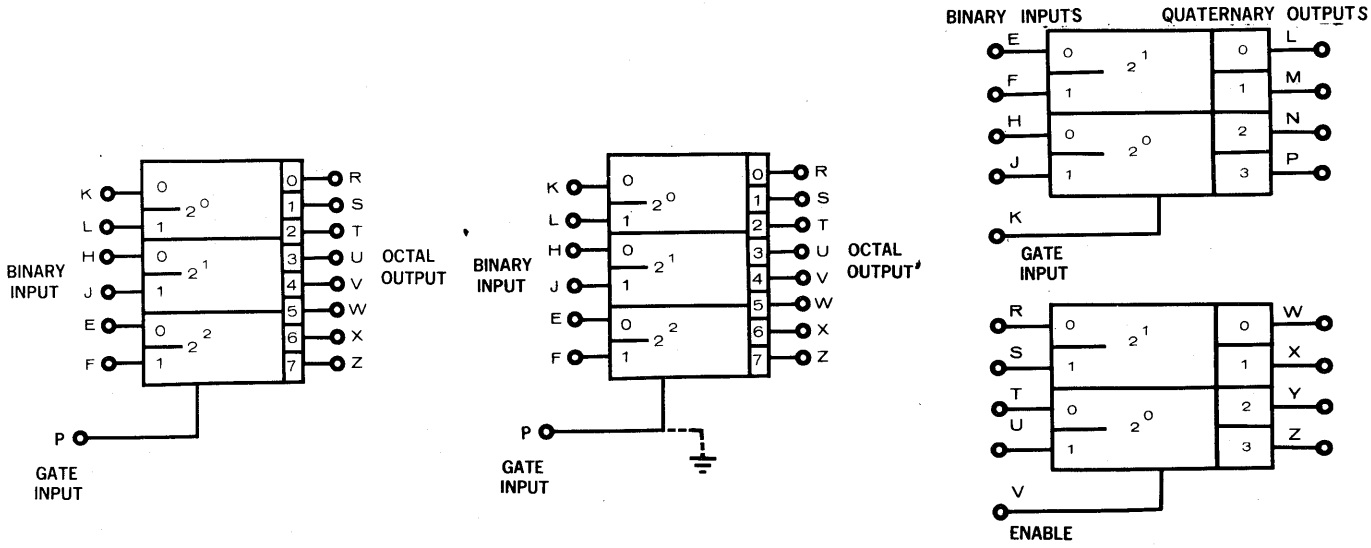
POWER: Type 6111: −15 volts/45 ma; +10 volts (A)/0.2 ma; +10 volts (B)/0.2 ma. **Type 6113:** −15 volts/35 ma; +10 volts (A)/0.15 ma; +10 volts (B)/0.15 ma. **Type 6115:** −15 volts/67 ma; +10 volts (A)/0.3 ma; +10 volts (B)/0.3 ma. **Type 6117:** −15 volts/55 ma; +10 volts (A)/0.30 ma; +10 volts (B)/0.15 ma. **Type 6119:** −15 volts/35 ma; +10 volts (A)/0.15 ma; +10 volts (B)/0.15 ma.

DECODERS

TYPES 6150, 6151, 6155

10 MEGACYCLES

6000 SERIES



6150 BINARY TO OCTAL DECODER **6151 BINARY-TO-OCTAL DECODER** **6155 BINARY-TO-QUATERNARY DECODER**

Types 6150, 6151 and 6155 Decoders change binary information into single line outputs. Each circuit has a gate input which disables all output lines. The delay through the decoder is approximately 30 nanoseconds. The Type 6150 contains eight diode gates similar to those in the Type 6110. These gates are internally connected so that each output comes from a separate set of inputs. The selected output line is at −3 volts while other lines are at ground. Typical total transition times are 50 nanoseconds for output rise and 70 nanoseconds for output fall. In the Types 6151 and 6155 the selected line is at ground and all other lines are at −3 volts. The internal gates are similar to those in the Type 6111. The Types 6151 and 6155 may also be used with 1000-series or 4000-series modules for gating 70-nanosecond or 0.4-microsecond pulses. In these cases, the pulse output would be similar to an inverter pulse output and would drive one unit of pulsed emitter load. Typical total transition times are 75 nanoseconds for output rise and 60 nanoseconds for output fall. The enable input on the 6151 is the common emitter connection of the output inverters, and is ground for enable. The enable input on the 6155 is a common input to the diode gates, and is therefore at −3 volts to enable.

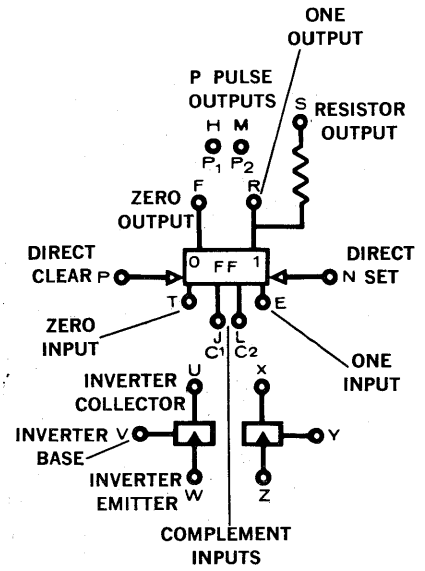
INPUTS: Type 6150: Binary inputs are DEC Standard Levels or equivalent with eight units of Base Load per line when terminal P is grounded and seven units when P is at −3 volts. The gate input is also a DEC Standard Level or equivalent (ground for enable). The load is seven units of Base Load. When P is not used to gating, it should be grounded. **Type 6151:** Binary inputs are DEC Standard Levels or equivalent with 0.3-unit DC Emitter Load. The gate input is a DEC Standard Level (ground for enable) or the output of an inverter, the base of which may be pulsed with a DEC Standard 70-nanosecond or wider Negative Pulse. The load is one unit of DC Emitter Load or one unit of Pulsed Emitter Load. The gate is internally jumpered to ground when the unit is shipped. **Type 6155:** Binary inputs are DEC Standard Levels or equivalent with 0.2-unit DC Emitter Load. The gate input can be DEC Standard Levels or equivalent (−3 volts for enable) or a DEC Standard 70-nanosecond or wider negative pulse. The enable input load is also 0.2-unit DC Emitter Load.

OUTPUT: Each output is similar to the collector of the Type 6106 inverter. Clamped load resistors are internally jumpered to all outputs and may be clipped out if desired. Outputs can be connected in series or parallel arrangements as with Type 6106 Inverters. In the Type 6151 the gate input is actually the emitters of all the output transistors; thus, if gating is done on this terminal, it must be counted as part of the series string of inverters.

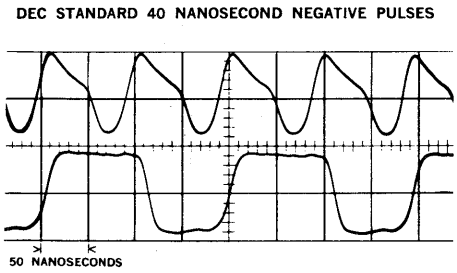
POWER: Type 6150: −15 volts/100 ma; +10 volts (A)/5 ma; +10 volts (B)/4 ma. **Type 6151:** −15 volts/88 ma; +10 volts (A) / 1.2 ma; +10 volts (B)/0 ma. **Type 6155:** −15 volts/110 ma; +10 volts (A)/1 ma; +10 volts (B)/1 ma.

FLIP-FLOPS
TYPE 6202
10 MEGACYCLES

6000 SERIES



6202 FLIP-FLOP



6202 FLIP-FLOP OUTPUT

The Type 6202 contains one flip-flop with built-in output amplifiers, direct and gated inputs to the ZERO and ONE sides and two independent gated complement inputs with carry pulse outputs. The package also contains two transistor inverters for use as pulse or level gates. The output signals have built-in delays so that they can be sensed reliably at the same time that the input is being pulsed. This general purpose flip-flop is useful in up-down counter, shift register, adder or control application.

INPUT: Direct clear and direct set inputs require DEC 40-nanosecond, 2.5-volt Positive Pulses (one unit of Pulse Load). Gated (ZERO, ONE, and compliment) input signals must come from one or more collectors of pulse gates. Signals can occur in any sequence at any frequency and at any time interval between two signals 100 nanoseconds or greater (maximum frequency of ten megacycles). The two inverters are similar to those included in DEC Inverter 6105.

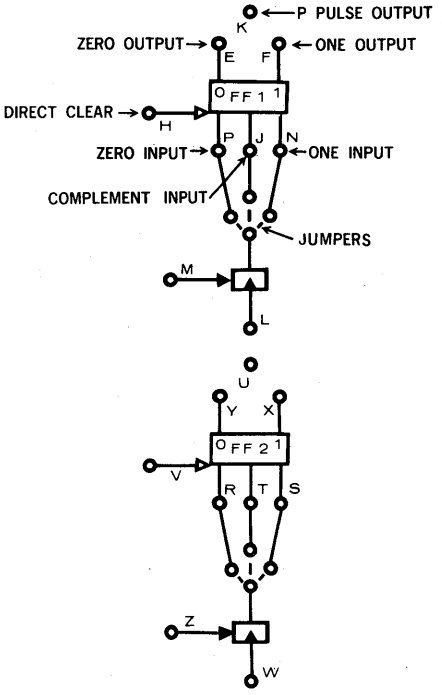
OUTPUT: ZERO output and ONE output provide DEC Standard Levels each capable of simultaneously driving at 10 megacycles, up to 6 loads each of which may be a Base or Emitter Load. There can be only one unit of DC Emitter Load, and only one unit of pulsed emitter load may be pulsed at a time. At lower frequencies each output may simultaneously drive: (a) 14 units of Base Load; (b) 1 unit of DC Emitter Load; (c) any number of Pulsed Emitter Loads providing not more than one is pulsed at a time. A resistor-coupled output suitable for driving a transistor indicator amplifier is available.

PULSE OUTPUT: Each time the Complement terminal is pulsed, a DEC Standard 40 nanosecond Negative Pulse will occur on the P terminal. This pulse is capable of driving one inverter base; however, the inverter emitter must be permanently grounded. The P Pulse will be delayed by approximately 15 nanoseconds with respect to the signal on the base of the input inverter.

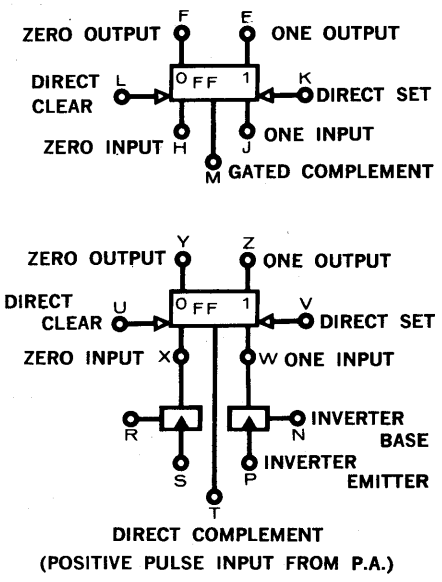
POWER: −15 volts/85 ma; +10 volts (A)/1.4 ma; +10 volts (B)/1.4 ma.

FLIP-FLOPS
TYPES 6207, 6208
10 MEGACYCLES

6000 SERIES



6207 DUAL FLIP-FLOP



6208 DUAL FLIP-FLOP

The Type 6207 and 6208 Flip-flops are for use in shift registers, buffer registers and general control applications. The Type 6207 may also be used for counting since it has complement inputs and P-pulse outputs. Each module contains two flip-flops and two inverters. The circuits are the same as the Type 6202 except that there are no paired gate complement inputs and P-pulse outputs and no resistor output. The inverter collectors are internally connected to flip-flop inputs in the 6208 and jumpered in the 6207.

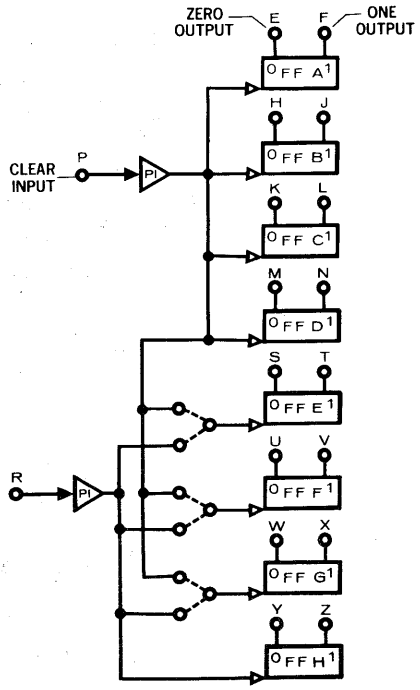
INPUTS: Same as Type 6202. The direct complement on the 6208 is like a direct clear input but represents three units of Pulse Load.

OUTPUTS: Same as Type 6202.

POWER: Type 6207: −15 volts/170 ma; +10 volts (A)/2.8 ma; +10 volts (B)/2.8 ma. **Type 6208:** −15 volts/170 ma; + 10 volts (A)/2.8 ma; + 10 volts (B)/2.8 ma.

FLIP-FLOPS
TYPE 6227
10 MEGACYCLES

6000 SERIES



6227 – UNBUFFERED FLIP-FLOPS

The 6227 contains eight unbuffered flip-flops and two pulse inverters. Each flip-flop is individually set by grounding the 0 output and may be cleared by grounding the 1 output. The two pulse inverters allow any number of flip-flops to be simultaneously cleared by appropriate internal jumpering of three flip-flops. The module is shipped with all jumpers connected, so either pulse inverter will clear all eight flip-flops.

INPUT: Direct: Flip-flops are set or cleared by grounding the 0 or 1 outputs, respectively with the collector of an inverter, such as the 6105. Inverters from diode gates and capacitor-diode gates may also be used. The emitter of such inverters must be tied directly to ground. The collector requires no load resistor as flip-flop outputs are clamped to −3 volts by an internal load resistor. The grounding signal must last at least 20 nanoseconds. Clear: A Standard DEC 40-nanosecond or longer Negative Pulse (one unit of Pulse Load) is required by each pulse inverter.

OUTPUT: Both the zero and one outputs of each flip-flop provide Standard DEC Levels of ground and −3 volts. Each output can drive two units of Base Load at ten megacycles, or four at slower speeds. Each output can also drive 0.5 units of DC Emitter Load. The emitter of any inverter or diode gate being driven must always be grounded. Each output has a clamped load resistor that fixes the off voltage at −3 volts. When the flip-flop has been cleared it is in the ZERO state, and the 0 output is at −3 volts while the 1 output is grounded. When the flip-flop has been set it is in the ONE state, and the outputs are reversed. Total transition time (TTT) is less than 40 nanoseconds or voltage rise, and less than 70 nanoseconds for voltage fall.

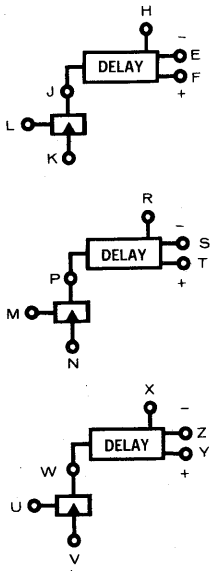
POWER: −15 volts/190 ma; +10 (A)/1.5 ma; +10 (B)/1.5 ma.

DELAYS

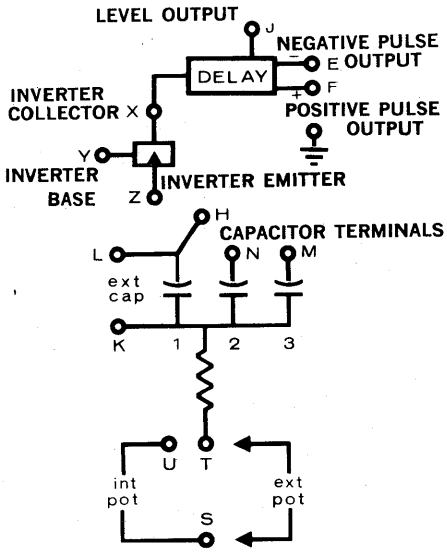
TYPES 6303, 6304

6.5 MEGACYCLES

6000 SERIES



6303 DELAY (ONE SHOT)



6304 DELAY (ONE SHOT)

The Types 6303 and 6304 Delays are one shot, mono-stable multivibrators. When the input terminal is grounded, either through the inverter or externally, the level output will switch from its normal ground level to −3 volts for a predetermined, but adjustable, period of time then back to ground. Simultaneously with the final transition, a DEC Standard 40-nanosecond Pulse is generated at the pulse output. Each delay in the Type 6303 has an individual potentiometer for adjusting the delay duration from 50 nanoseconds to 1 microsecond. Each circuit also has a pair of lugs where an additional capacitor may be inserted if a longer duration is desired. The Type 6304 contains three capacitors for delay range selection and a potentiometer for fine adjustment. Capacitor 1 permits adjustment from 50 nanoseconds to approximately 1 microsecond; Capacitor 2, from approximately 1 to 25 microseconds; and Capacitor 3, from approximately 25 to 250 microseconds. To increase the range further, an external capacitor may be connected between pins L and K. The fine control is adjusted with the internal potentiometer when pins U and T are jumpered together. For external control, a potentiometer of about 10,000 ohms can be connected between pins S and T. For both modules, the circuit recovery time is equal to approximately 10% of the maximum delay available with that capacitor connection. A 20% change in power supply voltage will change the delay less than 1%. Delay jitter (due to power supply ripple) is less than 0.3%.

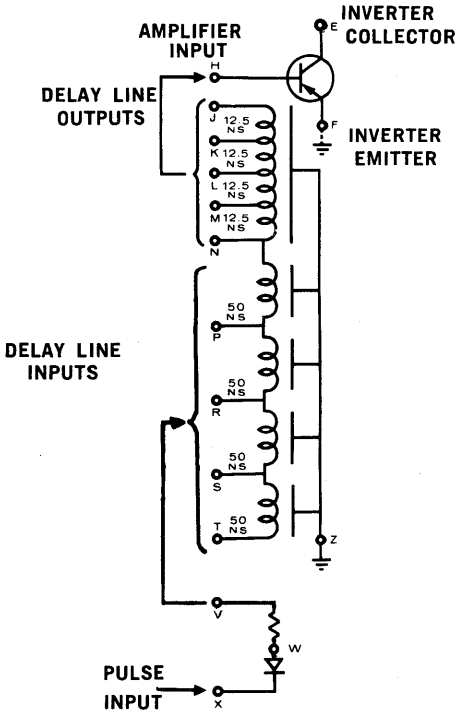
INPUT: The input to the delay is a DEC Standard 40-nanosecond Negative Pulse on the base of a pulse gate, such as the one included in the delay module. The base of the built-in pulse gate represents one unit of Pulse Load. If more logical inputs are desired, they can be provided by connecting pulse gate collectors to the collector of the built-in pulse gate.

OUTPUT: Level: When the input is pulsed, a negative DEC Standard Level occurs for the duration of the delay interval. This level is capable of simultaneously driving (a) six units of Base Load if speed is important, otherwise 14 bases; (b) one unit of DC Emitter Load; and (c) any number of Pulsed Emitter Loads, providing not more than one is pulsed at a time. Pulse: At the end of the delay interval, a DEC Standard 40-nanosecond Pulse occurs. The output pulse will be negative if the positive terminal is grounded; it will be positive if the negative terminal is grounded. This signal can drive eight units of Pulse Load.

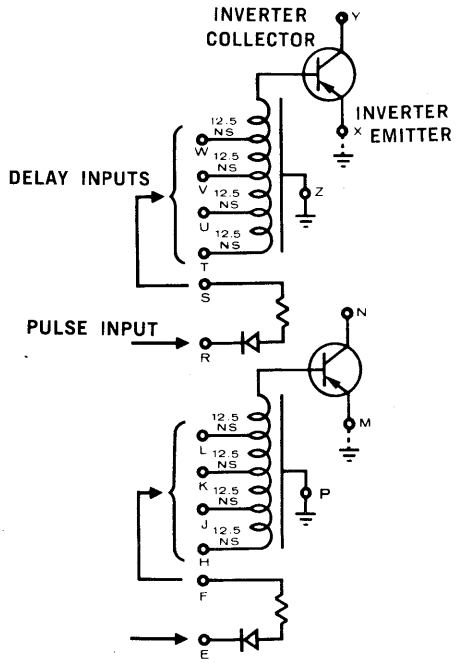
POWER: Type 6303: −15 volts/300 ma; +10 volts (A)/2.4 ma; +10 volts (B)/0 ma. **Type 6304:** −15 volts/100 ma; +10 volts (A)/0.6 ma; +10 volts (B)/0 ma.

DELAYS
TYPES 6310, 6311
10 MEGACYCLES

6000 SERIES



6310 DELAY LINE



6311 DELAY LINE

THE TYPE 6310 produces delays up to 0.25 microsecond in steps of 12.5 nanoseconds. A transistor amplifier is built into the package. Its input, not being a standard inverter, must be driven by the delay line. The 15 nanosecond delay of the inverter must be added to the total delay time. The input pulse is applied to pin X, and the input of the delay line (pins N through T) is connected to pin V, as shown. The output of the delay line (pin J through N) is connected to the base of the output inverter, pin H.

The Type 6311 contains two delay lines. Each line produces a maximum delay of 50 nanoseconds in 12.5-nanosecond steps. The output of each of the delay lines is connected to a transistor inverter. The collector terminal is available for logical gating. The 15-nanosecond delay through the inverter must be added to the delay of the line. The inputs are applied at pin R (or E) and the desired delay is obtained by connecting S (or F) to one of the delay line taps.

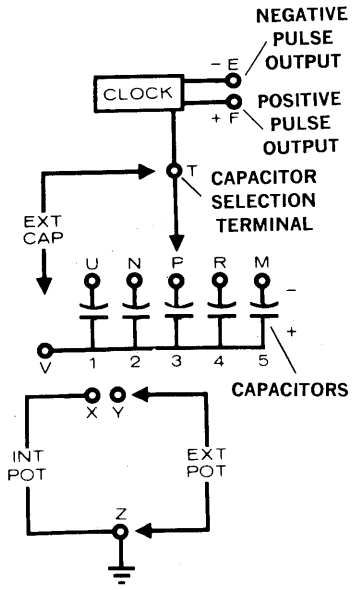
A 2-unit Pulse Load for the 6310 and 1-unit Pulse Load for each 6311 input are the input loads.

OUTPUT: The emitter of the output inverter must be grounded; the transistor's collector should be connected to the input of a Type 6603 Pulse Amplifier or other unit being pulsed. However, if additional logic gating is required, it may be done with up to two transistor inverters placed in series between the collector and the pulse amplifier.

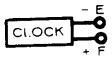
POWER: Type 6310: −15 volts/0 ma; +10 volts (A)/2.1 ma; +10 volts (B)/0 ma. **Type 6311:** −15 volts/0 ma; +10 volts (A)/1.0 ma; +10 volts (B)/1.0 ma.

CLOCKS
TYPES 6401, 6403
10 MEGACYCLES

6000 SERIES



6401 VARIABLE CLOCK



6403 CRYSTAL CLOCK

The Type 6401 Variable Clock produces standard pulses from a stable, RC-coupled oscillator with a wide range of frequencies available. The variable clock is often used as a primary source of timing for large systems. Where very precise timing is needed, the Type 6403 Crystal Clock, which contains a single-frequency crystal oscillator may be used. The frequency of the Type 6401 is variable from 250 cycles/second to 10 megacycles. Five capacitors determine the frequency range and a potentiometer provides fine control. For lower frequencies, an external capacitor may be used. If terminals X and Y are connected together, the internal 20,000 ohm potentiometer will provide the fine control. If desired, an external potentiometer can be connected between terminals Y and Z.

The Type 6403 contains a series resonant crystal oscillator circuit and two pulse shaping buffer amplifiers which produce DEC Standard 40 nanosecond Pulses. The frequency, specified by the customer, may be between 5 and 10 megacycles. The frequency is stamped on the crystal in the plug-in unit. Stability is 0.01% over the temperature range of −20 to +55° C.

OUTPUT: DEC Standard 40 nanosecond Pulses will appear at the output at the preselected frequency. The output pulse will be negative if the positive output terminal is grounded; it will be positive if the negative output terminal is grounded. Each output is capable of driving 8 units of Pulse Load.

POWER: Type 6401: −15 volts/185 ma; +10 volts/0 ma; +10 volts/0 ma. **Type 6403:** −15 volts/60 ma; +10 volts/0 ma; +10 volts/0 ma.

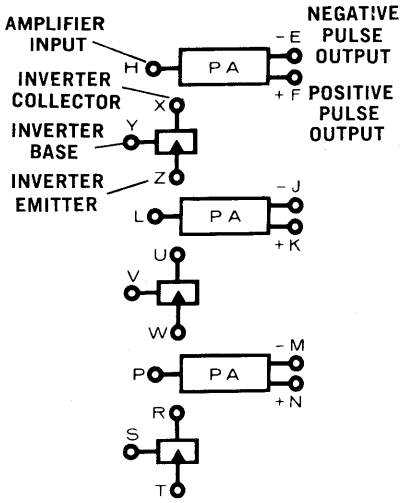
See 1000-series clocks for information on synchronizing clocks of different frequencies.

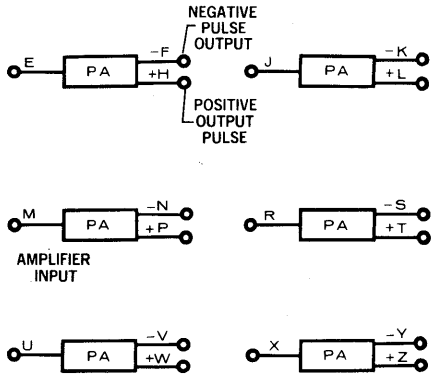
PULSE AMPLIFIERS

TYPES 6603, 6609

10 MEGACYCLES, 5 MEGACYCLES

6000 SERIES





6603 PULSE AMPLIFIERS

The Type 6603 contains three pulse amplifiers which are used for power amplification and for standardizing pulses in amplitude and width. Three inverters are available for gating input levels or for mixing pulses. Delay through the pulse amplifier is approximately 25 nanoseconds. Input pulses may occur at any frequency up to 10 megacycles.

INPUT: The input to the base of the inverter whose collector drives the pulse amplifier is normally a DEC Standard 40-nanosecond Negative Pulse. However, any negative pulse having an amplitude between 2.0 and 5.0 volts, leading edge less than 25 nanoseconds and width (at 2 volts) greater than 25 nanoseconds, can be used. This includes a ±3.6-volt, 5-megacycle sine wave or a DEC Standard 70-nanosecond Negative Pulse. Input pulses of less than −0.5 volts will not generate an output pulse. Many pulse gate collectors can be connected together to mix pulse sources. The pulse gates are inverters like those included in the Type 6105 Inverter.

OUTPUT: The output is a 2.5-volt Standard 40-nanosecond Pulse which occurs at the output every time the input signal meets the input requirement. The output will be negative if the positive output terminal is grounded; it will be positive if the negative terminal is grounded. Each output is capable of driving 12 units of Pulse Load.

POWER: −15 volts/91 ma; +10 volts (A)/0.3 ma; +10 volts (B)/0.2 ma.

6609 PULSE AMPLIFIERS

The 6609 contains six identical pulse amplifiers, each with pulse transformer outputs and input. It is designed to be driven directly by the collector of an external inverter, and each input contains a load resistor clamped to −3 volts. The pulse amplifiers are used for power amplification and pulse standardizing, producing a DEC Standard 40 nanosecond Pulse. Delay through the pulse amplifier is approximately 20 nanoseconds, and the input pulse repetition rate is 5 megacycles or less.

INPUT: Same as 6603

OUTPUT: Same as 6603 except that each output can drive 10 units of Pulse Load.

POWER: −15 volts/200 ma; +10 volts (A)/0 ma; +10 volts (B)/0 ma.

GENERAL INFORMATION
STANDARDIZERS

INPUT-OUTPUT

Standardizers convert switch closures or external logic signals to standard DEC signals. Included in this section are the following units:

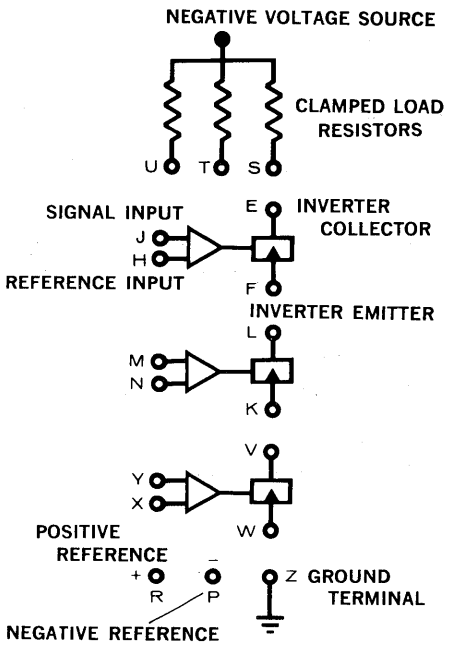
Type	Function
1501	Converts levels in the range of ±10 volts to DEC levels. Threshold is 0.1 volt. One level input must be more positive than −1.5 volts.
1502	Converts levels in the range of +10 to −50 volts to DEC levels. Upper level must be more positive than ground. Lower level must be more negative than −2.5 volts.
1503	Converts switch closures or levels in the range of ±10 volts to DEC levels; hysteresis and threshold variable over the range of 0 to −2 volts.
1703	Filters contact closures for driving DEC inverters.

See the pulse amplifiers and pulse generators of the particular series for converting pulses.
See also DEC <—> IBM for special conversion devices.

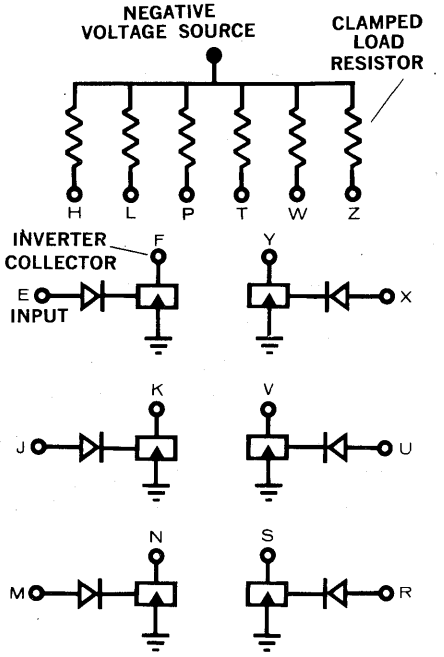
INPUT CONVERTERS

TYPES 1501, 1502

INPUT-OUTPUT



1501 LEVEL STANDARDIZER



1502 LEVEL STANDARDIZER

1501 LEVEL STANDARDIZER

Three difference amplifiers convert signals in the range of ±10 volts to DEC Standard Levels. Reference levels may be between +4 and −1.5 volts. The maximum ZERO offset is 0.1 volt and the minimum dynamic range is 0.1 volt. Three reference voltages are provided in the package: +1.2 (±0.1), −1.5 (±0.1), and ground.

INPUT: Reference: An external reference voltage from +4 to −1.5 volts may be used. The current required is +0.1 milliamperes if the reference is more positive than the input, and −0.2 milliamperes if the reference is more negative than the input. When the reference is more negative than +3.0 volts and also more negative than the input, the load is 1800 ohms to +3.3 volts.

Signal Input: Voltages may be in the ±10-volt range. If the input is more positive than the reference, the load is ±0.1 milliamperes. If the input is more negative than the reference, the load is −0.2 milliamperes. If the input is more negative than −2.7 volts, the load is 800 ohms to −2.5 volts.

OUTPUT: Same as 1105. Negative signal input gives ground output.

POWER: −15 volts/72 milliamperes; +10 volts (A)/0.5 milliamperes; +10 volts (B)/18 milliamperes.

1502 LEVEL STANDARDIZER

Six circuits convert levels in the range of −50 to +10 volts into Standard Levels. The upper input level must be more positive than ground and the lower level more negative than −2.5 volts. The total transition time is 0.6 microseconds or less. A typical application of the Type 1502 is for conversion of Univac 1102 levels into DEC Standard Levels.

INPUT: Voltage levels must be within the range of −50 volts to +10 volts. Maximum input current is 2.5 milliamperes at +10 volts. Less than 0.15 milliampere is required when the input is more negative than −2.5 volts. When the input is more negative than −2.5 volts, the output will be at ground. When the input is more positive than ground, the output will be at −3 volts.

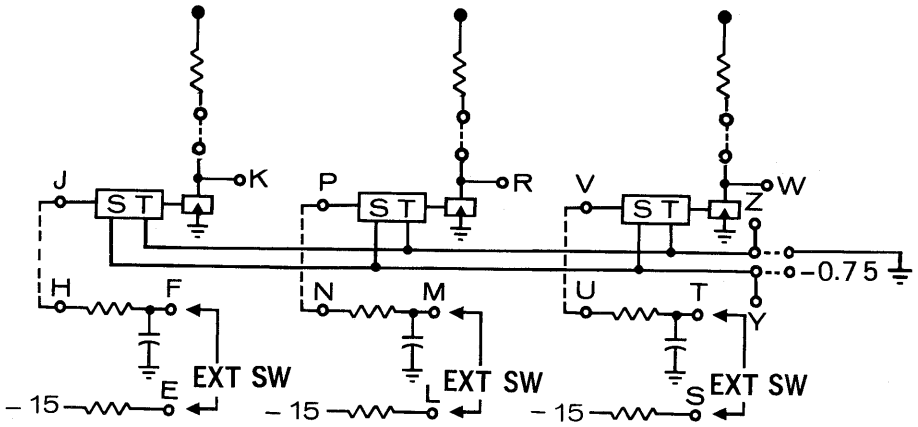
OUTPUT: Same as 1105. Negative input gives ground out.

POWER: −15 volts/94 milliamperes; +10 volts (A)/9 milliamperes; +10 volts (B)/0 milliamperes.

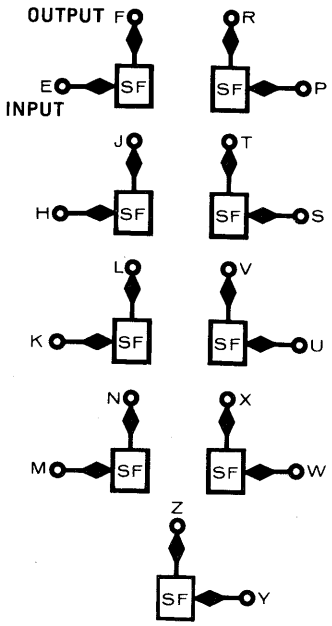
INPUT CONVERTERS

TYPES 1503, 1703

INPUT-OUTPUT



1503 SCHMITT TRIGGER



1703 SWITCH FILTER

1503 SCHMITT TRIGGER

The 1503 contains three separate Schmitt-trigger circuits that produce Standard Levels. A ground input produces a −3 volt level, and a negative input produces a ground level. The Schmitt trigger is internally connected to provide nominal switching thresholds at −2 and −0.75 volts; however, by removing jumpers and applying suitable voltage levels at pins Y and Z, the thresholds may be varied over the 0 to −2.5 volt range. Pin Y determines the lower switching point; pin Z determines the upper. For example, if the pin Y jumper is cut and Y is grounded, the nominal switching points are −0.75 and −1.25 volts.

The module also contains three input integrating circuits to filter contact bounce when a switch or relay is used to generate the levels. The time constant of the integrating circuit is 12 milliseconds.

INPUT: Direct: The input is d-c connected and may be either pulse or level. It should stay within the limits of ±10 volts. Input impedance is 10,000 ohms to +10 volts when output is −3 volts, 500 ohms to +1 volt when output is ground . As internally connected, a ground output is produced if the input voltage goes more negative than −2.0 volts after being more positive than −0.5 volts. **Integrating:** Input from switch or relay contact.

OUTPUT: Same as Type 1105; output is ground for a negative input. The module is shipped with clamped load resistors in place.

OUTPUT: Same as Type 1105; output is ground for a negative input.

1703 SWITCH FILTER

Nine switch filters eliminate contact bounce in converting contact closures to DEC Standard Logic Levels. An open input terminal produces a ground output, and a −15 volt input produces a −3 volt output. Output fall time varies from 2.5 to 5 milliseconds, and the output rise time is approximately twice the fall time.

INPUT: A 10 ma current flows through a contact when it connects an input to the −15 volt supply.

OUTPUT: Each output can drive 3 units of Base Load, ¼ unit of DC Emitter Load, any number of level inputs to capacitor-diode gates, and any number of Pulsed Emitter Loads providing no more than one is pulsed at a time.

POWER: −15 volts/90 ma; +10 volts (A)/27 ma.

GENERAL INFORMATION

DRIVERS

These modules include signal converters and circuits for driving heavy loads. For many units the output voltage is variable, hence they may be used with standard DEC signal or a variety of other signals.

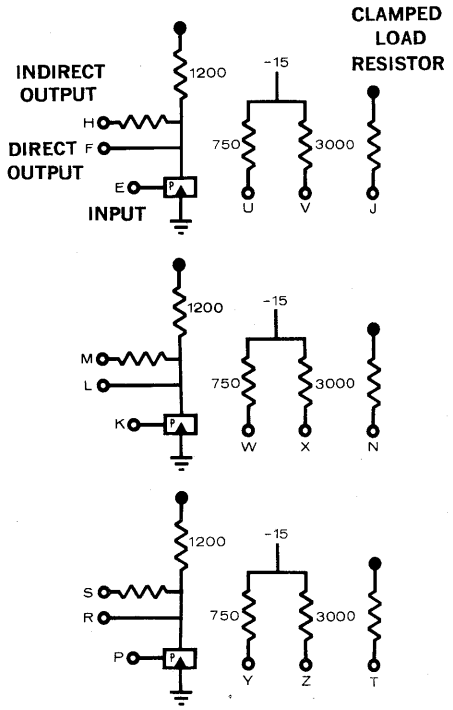
Type	Function
Bus Drivers, DEC Signals	
1678	Three non-inverting circuits supply negative drive only; therefore, many circuits may be OR'ed together.
1681	Three fast, inverting circuits.
1684	Four fast, non-inverting circuits.
1685	Four non-inverting circuits provide 1-microsecond ramp.
1690	Four inverting circuits provide 1-microsecond ramp.
1693	Three fast, non-inverting circuits drive terminated cable.
6684	Four fast non-inverting circuits drive terminated or unterminated cable.
Output Pulse Amplifiers	
1616	Produces a 5-volt, 0.5-microsecond pulse.
4610	Produces a 2- to 34-volt, 2- to 3-microsecond pulse.
Level Amplifiers	
1667	Upper level is ground, lower level is 0 to −15 volts.
1687	Upper level is 0 to +6.5 volts; lower level is 0 to −6.5 volts.
4667	Upper level is ground; lower level is 0 to −15 volts.
4685	Upper level is ground; lower level is 0 to −30 volts.
4686	Upper level is 0 to +20 volts; lower level is ground.
Amplifying Bus Drivers	
1678	Upper level is +0.1 to −0.3 volts; lower level is 0 to −12 volts.
1691	Upper level is ground; lower level is −10 volts; output is 1.5-microsecond ramp.
1692	Upper level is +6 volts; lower level is ground.
1693	Upper level is 0 to +6.5 volts; lower level is 0 to −6.5 volts.
Indicator Drivers (See also accessories section.)	
1669	Accepts up to 30 milliamperes.
1675	Accepts up to 30 milliamperes (input from remote 3,000-ohm resistor).
4689	Accepts up to 100 milliamperes.
BCD Decoders and Light Drivers	
4671	Drives incandescent bulbs.
4673	Drives neon bulbs.
Solenoid Drivers	
4681	Upper level is −3.5 volts; lower level is −3.5 to −70 volts.
4682	Lower level is ground; upper level is 0 to +28 volts.

BUS DRIVERS

TYPE 1681

5 MEGACYCLES

INPUT-OUTPUT



1681 POWER INVERTER

1681 POWER INVERTER

The Type 1681 contains three circuits, each similar to an ordinary inverter, except that the current level is higher. This module is used where a heavy load must be driven by Standard Logic Levels. The total transition time for output rise is less than 35 nanoseconds. For output fall, it is less than 45 nanoseconds.

INPUT: The inputs are DEC Standard Levels. Each input represents 3 units of Base Load.

OUTPUT: Both direct and indirect outputs are available from each power inverter. The indirect outputs (through 100-ohm resistors) may be used to drive coaxial cable so that the source end of the line may be terminated. The direct outputs are used for all other purposes.

The output driving ability of the Type 1681 is determined by the load resistors that are connected to the direct output. A 1200-ohm clamped load resistor is internally connected and the following additional loads are available: A 1500-ohm clamped load resistor, a 3000-ohm unclamped load resistor, and a 750-ohm unclamped load resistor. The following configurations may be used:

No external load resistors: The output driving ability is 3 units DC Emitter Load and 9 units Base Load.

3000-ohm load resistor: The output driving ability is 2½ units DC Emitter Load and 12 units Base Load.

1500-ohm clamped load resistor: The output driving ability is 2 units DC Emitter Load and 16 units Base Load.

3000-ohm load resistor and 1500-ohm clamped load resistor: Output driving ability is 1½ units DC Emitter Load and 19 units Base Load.

1500-ohm clamped load resistor and 750-ohm load resistor: The output driving ability is 30 units Base Load.

A power inverter may drive many units of Pulsed Emitter Load, providing only one is pulsed at a time. The DC Emitter loading should be decreased by one unit.

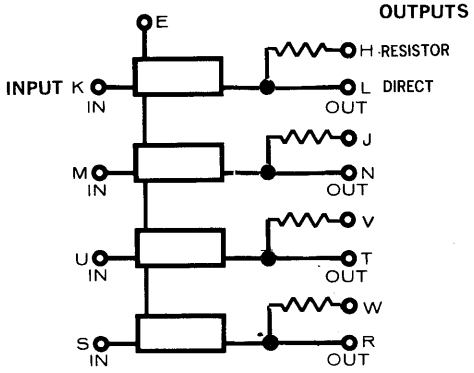
POWER: −15 volts/175 ma; +10 volts (A)/0.11 ma; +10 volts (B)/0.23 ma.

BUS DRIVERS

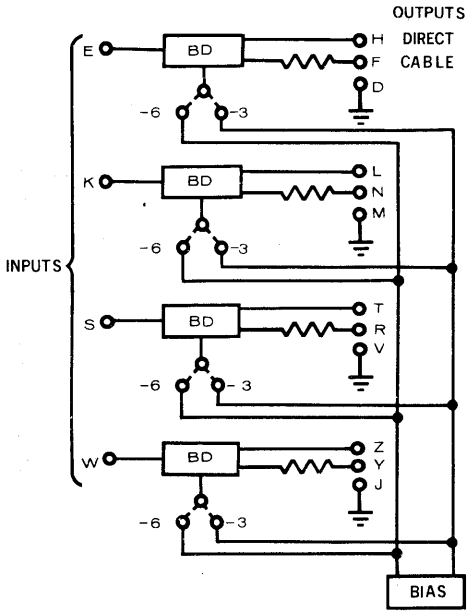
TYPES 1684, 6684

5 MEGACYCLES 10 MEGACYCLES

INPUT-OUTPUT



1684 BUS DRIVER



6684 BUS DRIVER

1684 BUS DRIVER

The Type 1684 is a non-inverting bus driver used to provide levels for heavily loaded logic lines at speeds up to 5 megacycles. There are four identical circuits in the module. The input to each circuit is through a grounded inverter. The unloaded total transition time is $\leq$75 nanoseconds. Increasing the driving capabilities of each output from 5 to 20 units of Base Load is accomplished by connecting pin E through a 120-ohm, 2 watt resistor to −15 volts.

INPUT: Each input represents 1 unit of 5 megacycle Base Load.

OUTPUT: Direct: Each circuit can drive five units of DC Base Load and an infinite amount of capacitance. Output impedance is 22 ohms. With an external, 120-ohm, 2-watt resistor connected between pin E and −15 volts (pin C) each output can drive 20 units of 5-megacycle Base Load at five megacycles, 15 units of 500-kilocycle Base Load at 500 kilocycles, or 20 units of 500-kilocycle Base Load at lower frequencies. **Resistor:** The resistor output is used to drive a light load (two units of Base Load) at the end of an unterminated, 93-ohm cable.

POWER: −15 volts/84 ma; +10 volts (A)/1.6 ma; +10 volts (B)/1.6 ma. Optional 120-ohm, 2-watt resistor to −15 volts from pin E requires an additional 93 ma.

6684 BUS DRIVER

The 6684 contains four dual-purpose, non-inverting bus drivers and associated biasing circuits. Each bus driver provides Standard Levels to a line heavily loaded with base and diode loads or at the end of a terminated 93-ohm cable. All logic terminals are available at the connector. Delay through a bus driver is typically 30 nanoseconds.

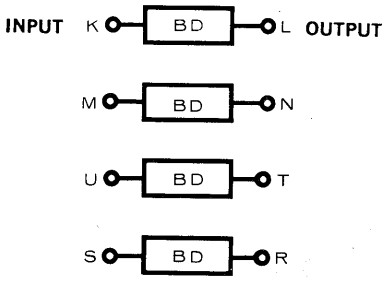
INPUT: DEC Standard Levels or equivalent (1 unit of Base Load).

OUTPUT: Direct: DEC Standard Levels of the same polarity as the input, capable of driving 40 units of Base Load or 4 units of DC Emitter Load at 10 megacycles. Each bus driver must be internally jumpered to the −3 volt bias when driving a bus from the direct output. **Resistor:** Ground and −6 volt levels at the resistor output provide DEC Standard Levels at the end of a 93 ohm cable when it is terminated with a 100 ohm resistor to ground. The terminated cable will drive 10 units of Base Load or 1 unit of DC Emitter Load at 10 megacycles. Each bus driver must be internally jumpered to the −6 volt bias when driving a terminated cable from the resistor output. A separate terminal is available at the connector for grounding the cable shield.

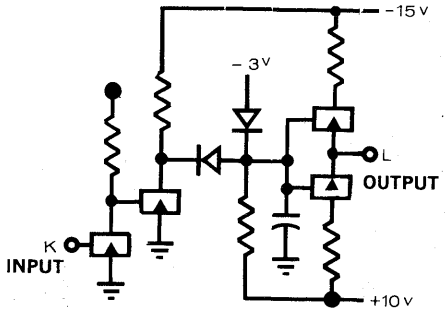
POWER: Outputs at ground, no load: +10 volts (B)/135 ma: −15 volts/133 ma. Outputs at −3 volts, no load: +10 volts (B)/113 ma; −15 volts/248 ma. Outputs at −6 volts, 100-ohm load from resistor outputs: +10 volts (B)/113 ma; −15 volts/431 ma. Load currents at ground output come from +10 volts (B); load currents at lower output level come from −15 volts.

BUS DRIVERS
TYPES 1685, 1690
500 KILOCYCLES

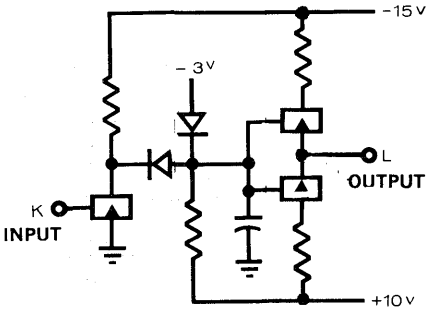
INPUT-OUTPUT



1685 AND 1690 BUS DRIVERS



1685 SCHEMATIC



1690 SCHEMATIC

1685 AND 1690 BUS DRIVERS

The Types 1685 and 1690 contain bus drivers for use in driving heavily loaded output lines where fast rise and fall times would create severe ringing and large induced voltage transients. The rise and fall times of the output signal are approximately one microsecond. There are four identical circuits in the module. For more than 5000 picofarad output load, the maximum rise or fall time in microseconds is equal to the capacitance in picofarads divided by 5000. The Type 1690 inverts the input signal. The Type 1685 does not invert.

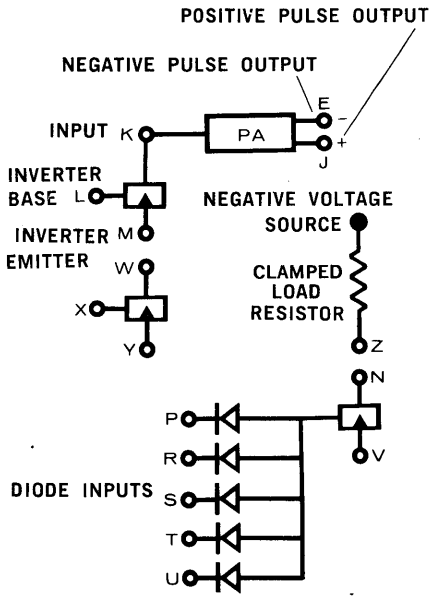
INPUT: Each input represents one-half unit of 5-megacycle Base Load.

OUTPUT: Each output is capable of driving 15 units of 5-megacycle Base Load at 500 kilocycles or 8 units of 500-kilocycle Base Load at 500 kilocycles or 15 units of 500-kilocycle Base Load at lower frequencies. It can supply a maximum current of ±15 milliamperes.

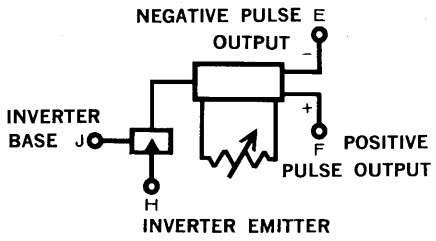
POWER: Type 1685: −15 volts/145 milliamperes; +10 volts (A)/0.8 milliamperes; +10 volts (B)/10.5 milliamperes. **Type 1690:** −15 volts/123 milliamperes; +10 volts (A)0.8 milliamperes; +10 volts (B)/10.5 milliamperes.

OUTPUT DRIVERS
TYPES 1616, 4610
500 KILOCYCLES, 1 KILOCYCLE

INPUT-OUTPUT



1616 OUTPUT PULSE AMPLIFIER



4610 OUTPUT PULSE AMPLIFIER

1616 OUTPUT PULSE AMPLIFIER

The Type 1616 contains one pulse amplifier which produces 5-volt, 0.5-microsecond pulses for driving external devices. Flexible input gating is available through the use of the two inverters and the 5-input diode gate contained in the package. The two inverters are similar to those in the Type 1105. The diode gate is similar to that in the Type 1110 and may be used for mixing negative pulse inputs. Delay through the pulse amplifier is approximately 25 nanoseconds. Input pulses may occur at any frequency up to 500 kilocycles.

INPUT: Same as Type 1607.

OUTPUT: Each time the input requirement is met, the pulse amplifier will produce a 5 volt, 0.5 microsecond pulse into a 100-ohm load. Pulse outputs may be made either positive or negative by grounding the appropriate output terminal.

POWER: −15 volts/60 ma; +10 volts (A)/1.2 ma; +10 volts (B)/0.9 ma.

4610 OUTPUT PULSE AMPLIFIER

This pulse amplifier delivers 2 to 3 microsecond pulses with amplitudes variable from 2 to 34 volts into 100 ohms. The input is through an inverter gate. A 0.4 microsecond input produces a 2 microsecond pulse, and a 1.0 microsecond input produces a 3 microsecond pulse. The maximum prf is 1 kilocycle. Delay is less than 0.5 microsecond, and the rise and fall times are less than .25 microsecond. Controls: a potentiometer varies the output amplitude.

INPUT: The base input requires Standard 0.4-microsecond Negative Pulses or equivalent and represents one unit of Pulse Load. The emitter represents one unit of DC Emitter Load.

OUTPUT: The output will be negative if the positive output terminal is grounded, and it will be positive if the negative output terminal is grounded.

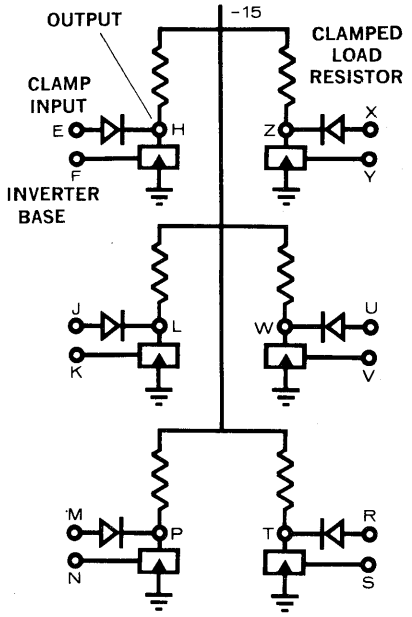
POWER: −15 volts/30 ma; +10 volts (A)/1 ma; +10 volts (B)/0 ma.

LEVEL AMPLIFIERS

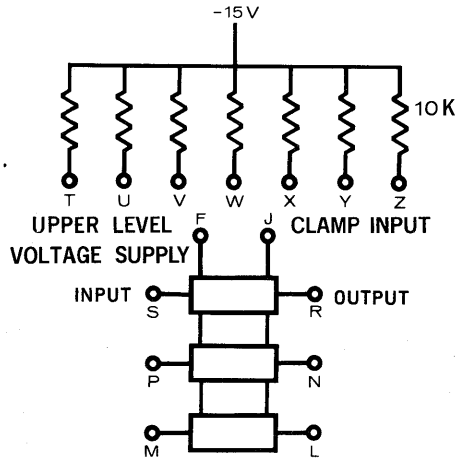
TYPES 1667, 4667, 1687

5 MEGACYCLES, 500 KILOCYCLES 5 MEGACYCLES

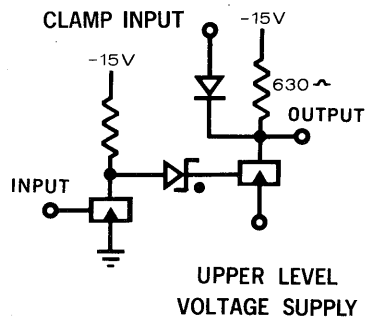
INPUT-OUTPUT



1667 AND 4667 NEGATIVE LEVEL AMPLIFIERS



1687 LEVEL AMPLIFIERS



SIMPLIFIED 1687 SCHEMATIC

1667 AND 4667 NEGATIVE LEVEL AMPLIFIERS

Six grounded emitter inverters amplify DEC Standard Levels. The output signals are ground and a negative voltage that is determined by clamping diodes. These clamping diodes are connected to each inverter collector and brought out to the plug to be returned to an external voltage between ground and −15 volts. Delay is approximately 0.05 microseconds through the 1667 and 0.2 microseconds through the 4667.

INPUT: The base input is DEC Standard Levels or equivalent (1 unit of Base Load). When the base is at ground level, the output is at −15 volts. When the base is at −3 volts, the output is at ground level.

OUTPUT: The upper output level is ground. The lower output level is determined by the external supply attached to the clamp diodes, and must be in the range of ground to −15 volts. When the output signal is at ground, each inverter will supply up to 5 ma to external circuitry. When the output level is negative, the maximum current which can be accepted is determined by a 1500-ohm resistor to −15 volts.

POWER: −15 volts/82 ma; +10 volts (A)/0.45 ma. +10 volts (B)/0.45 ma.

1687 LEVEL AMPLIFIERS

The Type 1687 contains three general-purpose level amplifiers whose upper level is determined by an external supply between 0 and +6.5 volts and whose lower level is determined by an external clamp voltage that may be as negative as −6.5 volts. Total transition time is approximately 70 nanoseconds. Seven 10,000-ohm resistors, returned to −15 volts, are included in the package but are not part of the level circuit. These may be used with inverters to form Exclusive OR circuits, if desired.

INPUT: The inputs should be Standard Levels (one unit of 5-megacycle Base Load).

OUTPUT: The level amplifier can deliver up to 10 milliamperes at its upper level of 0 to +6.5 volts. The current available at the lower level is determined by a 630-ohm internal load to −15 volts. The output is not short-circuit proof.

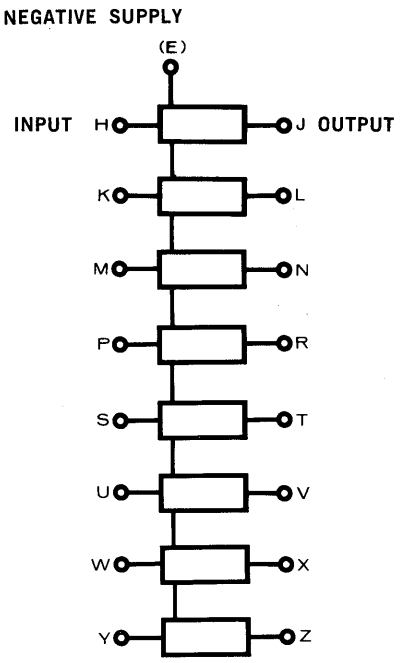
POWER: −15 volts/150 ma; +10 volts (A)/0.4 ma; +10 volts (B)/5.4 ma; pin F at +6.5 volts/140 ma + external load current; pin J at −6.5 volts/40 ma charging current.

LEVEL AMPLIFIERS

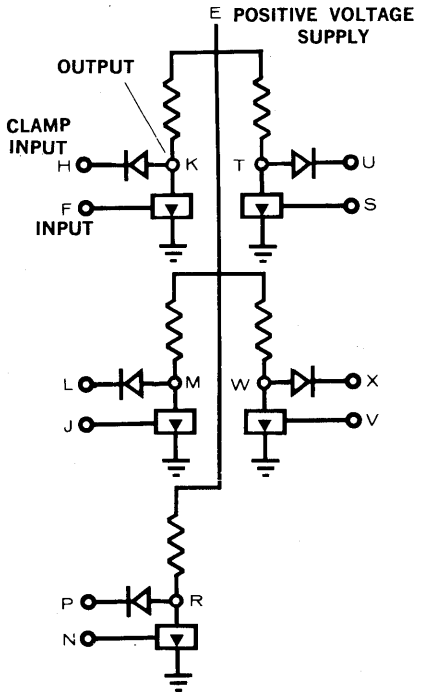
TYPES 4685, 4686

50 KILOCYCLES 500 KILOCYCLES

INPUT-OUTPUT



4685 LEVEL AMPLIFIER



4686 POSITIVE LEVEL AMPLIFIER

4685 LEVEL AMPLIFIER

Eight circuits convert DEC Standard Levels into 0 and −30 volt levels. The maximum operating frequency of this module is 50 kilocycles. Typical total transition times are 20 microseconds for output fall and 2 microseconds for output rise.

INPUT: Inputs are Standard Levels. Each input represents one unit of 500-kilocycle Base Load.

OUTPUT: A −3 volt input produces a ground output which will be no more negative than −0.2 volts while supplying up to 5 ma to an external load. A ground input produces a −30 volt output. The output driving capability in this state is determined by the 3000-ohm internal load resistor to −30 volts.

POWER: An external power supply must be used to supply −30 volts to pin E. This source should be capable of supplying 80 milliamperes.

POWER: −15 volts/0 ma; +10 volts (A)/1.3 ma; +10 volts (B)/0 ma; −30 volts (E)/ 80 ma.

4686 POSITIVE LEVEL AMPLIFIER

The five amplifier circuits contained in the Type 4686 are similar to DEC Inverters using NPN transistors instead of PNP. This unit is used to convert DEC Standard Levels to levels of ground and some positive voltage between 0 and +20 volts. The positive voltage is determined by the clamp voltage. The load resistors are brought out to pin E, and should be connected to +10 volts or to an external source up to +20 volts.

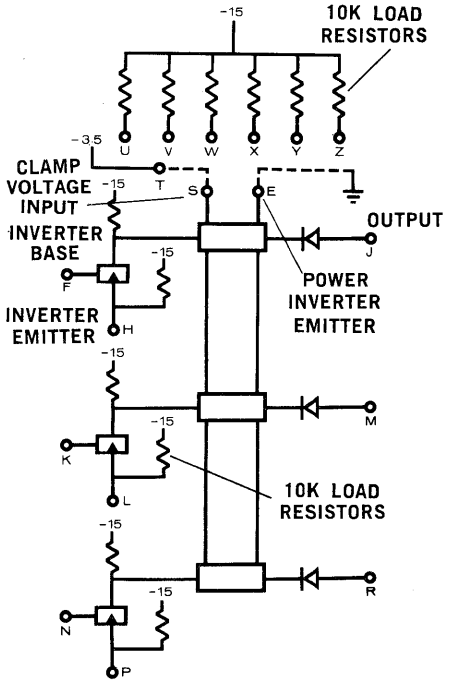
INPUT: Standard Levels (1⅓ units of Base Load, 330 picofarads).

OUTPUT: A ground input signal produces a ground output signal capable of supplying up to 20 ma to the 1000-ohm load resistor and external circuitry. A negative input signal produces a positive voltage (determined by the external clamp).

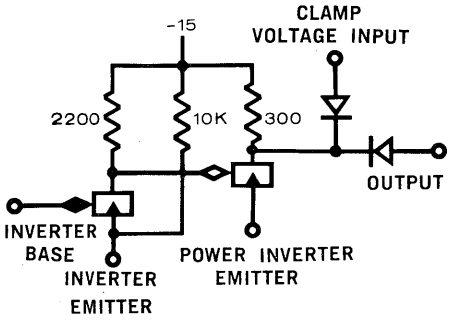
POWER: −15 volts/0 ma; +10 volts (A)/4 ma; +10 volts (B)/0 ma.

AMPLIFYING BUS DRIVERS
TYPE 1678

INPUT-OUTPUT



1678 AMPLIFYING BUS DRIVER



SIMPLIFIED SCHEMATIC

1678 AMPLIFYING BUS DRIVER

The Type 1678 contains three non-inverting bus drivers which provide high negative drive currents to heavy loads. This unit may also be used to amplify DEC Standard Levels, up to −12 volts, for driving external devices. Each circuit consists of a DEC Standard Inverter followed by a special power inverter. Both base and emitter inputs of the standard inverter are brought out to permit gating. The emitter has an attached 10K load, useful when it is part of an exclusive OR network.

The power inverter emitters are connected to a common external voltage which determines the more positive output level. The more negative output level is determined by an external clamp voltage. A fixed supply of −3.5 volts is provided within the module for connection to this point if desired. When the bus driver is operating with ground and −3.5 volt output levels, the total transition time is less than 100 nanoseconds.

Diodes in series with the output terminals prevent the Type 1678 from supplying positive drive; therefore, several circuits may be used in parallel to operate as a logical OR for negative signals. The module contains six 10,000 ohm resistors returned to −15 volts. These resistors are useful in constructing exclusive OR circuits from DEC Standard Inverters.

INPUT: The inputs to the standard inverter are Standard Levels or equivalent. The base represents one unit of 5-megacycle Base Load; the emitter represents one unit of DC Emitter Load.

The power inverter emitters are brought out to a separate pin so that the upper output level may be varied, as a marginal check on the equipment that the bus driver is driving. The allowable voltage range of this input is +0.1 to −0.3 volts. It may be connected to ground if this feature is not desired. The clamp voltage input may be connected to the −3.5 volt terminal provided or to an external clamp voltage between −12 volts and ground. A 6.8 microfarad capacitor is internally connected from the clamp input to ground.

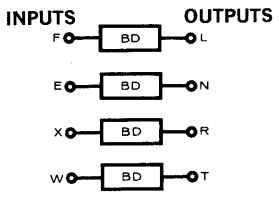
OUTPUT: Since each bus driver has a diode in series with the output, no current will be supplied to a positive return. Thus, several bus drivers may be ORed together to drive the same load.

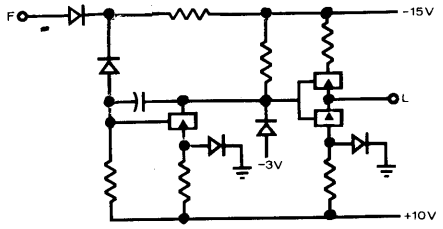
Using the internal clamped load, each driver can generate −3.5 volts into a 100 ohm load. At other clamp voltages, and loads, the lower level is determined by the internal 300 ohm resistor returned to −15 volts, the output load, and the clamp voltage. The clamp voltage should be made no more negative than −12 volts.

POWER: −15 volts/200 ma; +10 volts (A)/0.35 ma; +10 volts (B)/0.5 ma.

AMPLIFYING BUS DRIVERS
TYPE 1691
500 KILOCYCLES

INPUT-OUTPUT





1691 AMPLIFYING BUS DRIVER

SIMPLIFIED SCHEMATIC

1691 AMPLIFYING BUS DRIVER

The four inverting drivers in the Type 1691 drive external equipment with logic levels of 0 and −10 volts. The delay is less than 600 nanoseconds and the rise and fall times are both approximately 1.5 microseconds. For more than 1500 pf output load, the maximum rise or fall time, in microseconds, is equal to the capacitance in pf divided by 1000.

INPUT: DEC Standard Levels or their equivalent are required for input levels. Each input represents ⅛ unit of DC Emitter Load.

OUTPUT: Ground input produces −10 volt output; −3 volt input produces 0 ±0.1 volts. Each output can supply ±10 ma.

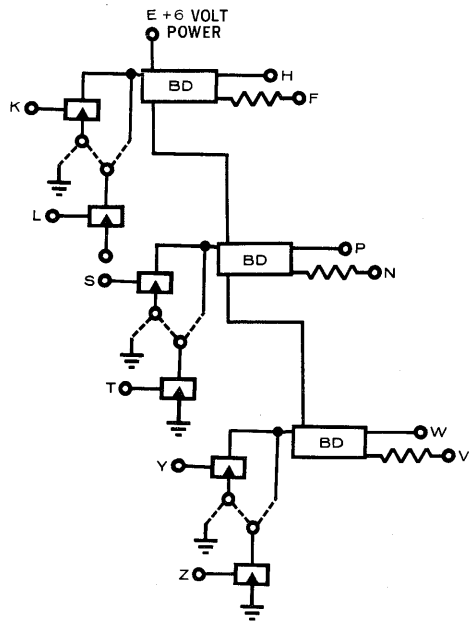
POWER: −15 volts/68 ma; +10 volts (A)/48 ma; +10 volts (B)/48 ma.

AMPLIFYING BUS DRIVERS

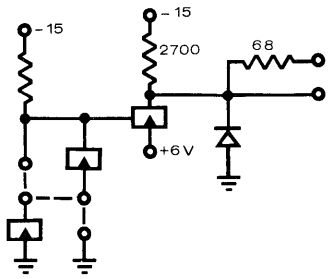
TYPE 1692

5 MEGACYCLES

INPUT-OUTPUT



1692 AMPLIFYING BUS DRIVER



SIMPLIFIED SCHEMATIC

1692 AMPLIFYING BUS DRIVER

Three identical circuits are used as line or bus drivers for signals from 0 to +6 volts. Three sets of internal lugs permit series or parallel connection of input inverters. The module is shipped with the inverters connected in parallel. When connected in this manner, two ground inputs produce a +6 volt output that can drive 75 ohms to ground. One or two negative inputs produce a ground output. Three 68-ohm resistors are included for driving coaxial cable.

When driving a 75-ohm load, the total transition time for output fall is 150 nanoseconds; for output rise, the total transition time is 60 nanoseconds.

INPUT: The inputs are Standard Levels. Each input represents one unit of Base Load. A 0 to +6 volt source should be connected to pin E. This input requires 300 milliamperes maximum; the exact value is dependent upon the maximum load to be driven.

OUTPUT: Output levels are ground and +6 volts. When an output is ground, it can supply a current of three milliamperes. When the output is +6 volts, it can supply 100 milliamperes. The output is not short-circuit proof.

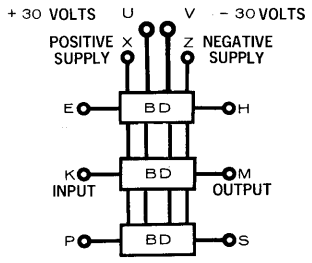
POWER: −15 volts/80 milliamperes; +10 volts (A)/1 milliamperes; +10 volts (B)/14 milliamperes.

AMPLIFYING BUS DRIVER

TYPE 1693

5 MEGACYCLES

INPUT-OUTPUT



1693 AMPLIFYING BUS DRIVER

1693 AMPLIFYING BUS DRIVER

The 1693 contains three non-inverting bus drivers, designed to drive 100-ohm coaxial cable, shunt-terminated with 100 ohms to ground. The output voltages of the bus driver may be varied by changing the d-c voltages applied to pins X and Z. The voltages applied to these pins must be less than ±13 volts with respect to ground and pin X must always be more positive than pin Z. The output circuit is a transistor saturated by one or the other of these two voltages, and a series resistor of 100 ohms. Thus by proper choice of voltages the module may be used to obtain any digital transmission line voltages between ±6.5 volts. Typical total transition time is 60 nanoseconds.

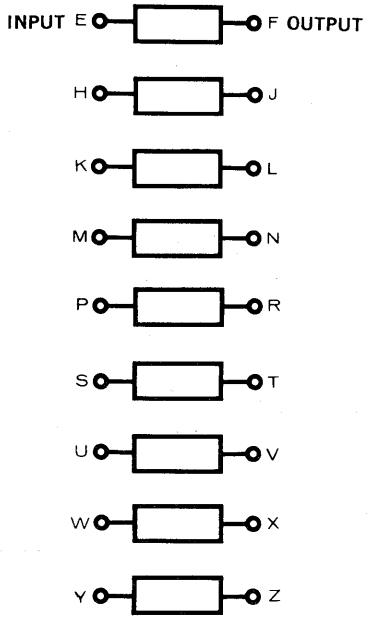
INPUT: The inputs are Standard Levels (one-half unit of Base Load plus one-half unit of DC Emitter Load).

OUTPUT: Each output can drive a shunt-terminated, 100-ohm transmission line. Outputs are short-circuit proof.

POWER: −15 volts/45 milliamperes; +10 volts (A)/45 milliamperes; +10 volts (B)/0 milliamperes. +30 volts (U)/10 milliamperes; −30 volts (V)/10 milliamperes; 0 to +13 volts (X)/0 to 60 milliamperes; 0 to −13 volts (Z)/0 to −60 milliamperes.

INDICATOR DRIVERS
TYPES 1669, 1675, 4689

INPUT-OUTPUT



1669, 1675, 4689 INDICATOR DRIVERS

1669, 1675, 4689 INDICATOR DRIVER

The Types 1669, 1675 and 4689 contain nine transistor amplifiers capable of driving an indicator panel of miniature incandescent bulbs. They are ideal for providing remote indicators from DEC Flip-flops. The indicator lights are on whenever the inputs to their respective amplifiers are −3 volts; if the input is from a flip-flop, the indicator usually indicates a ONE state.

INPUT: Type 1669: DEC Standard Levels or equivalent; represents one unit of Base Load (no capacitance). **Type 1675:** The base of a transistor inverter with no input resistor. It may be driven only by the resistor outputs of the Types 4201, 1201, 1209, or 6202 Flip-flops, or any flip-flop that has a 3000-ohm resistor wired between it and the Type 1675. When an indicator driver is used, the driving ability of the flip-flop ONE output must be decreased by one unit of Base Load. Use of this technique minimizes capacitive loading on the driving flip-flop. **Type 4689:** DEC Standard Levels or equivalent; represents three units of Base Load.

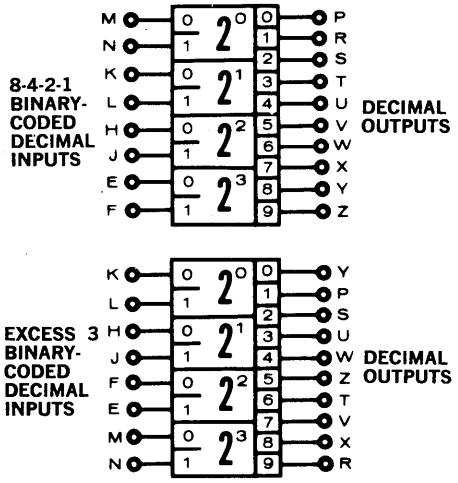
OUTPUT: Each output of the **Types 1669** and **1675** is suitable for driving a Type 327, 28-volt indicator lamp that is returned to −15 volts. Other loads may be driven, providing the required current is no greater than 30 milliamperes and the voltage no more negative than −20 volts. Each output of the **Type 4689** is suitable for driving an indicator lamp that is returned to −15 volts. Other loads may be driven, providing the required current is no greater than 100 milliamperes and the voltage is no more negative than −20 volts.

POWER: Types 1669, 1675: +10 volts (A)/1.3 milliamperes: +10 volts (B)/0 milliamperes; −15 volts/270 milliamperes;* **Type 4689:** +10 volts (A)/4 milliamperes; +10 volts (B)/0 milliamperes; −15 volts/900 milliamperes.*

*This voltage is not supplied to this unit; this is the maximum current drawn by the remote loads from −15 volts when they are all turned on.

DRIVERS
TYPES 4671, 4673

INPUT-OUTPUT



4671 AND 4673 BCD DECODES AND INDICATOR DRIVERS

4671 AND 4673 BCD DECODERS AND INDICATOR DRIVERS

The 4671 and 4673 decode 8-4-2-1 or Excess 3 BCD codes into 10 separate output lines that drive decimal indicators. The 4671 drives GE47 lamps like those in the Industrial Electronic Engineers Model 10000-47 Display Unit. The 4673 drives gas-filled, cold-cathode indicators.

INPUT: Both 4671 and 4673 must be driven by four flip-flops with two inputs coming from each flip-flop as shown above. Output 0 is selected when all flip-flops hold the code for 0. For example, in 8-4-2-1 code when all 0 inputs are at −3 volts and all 1 inputs are at ground, output 0 (P) is selected. **Type 4671:** The input load is ⅛ unit of DC Emitter Load for each ground input (1.25 ma). The circuit consists of 10 negative AND gates. When inputs M, K, H, and E are at −3 volts, output P is selected. **Type 4673:** The input load is 1.4 units of Base Load for each input at −3 volts (1.4 ma). The circuit consists of 10 positive AND gates. When inputs N, L, J, and F are at ground, output P is selected.

OUTPUT: The output amplifiers of the 4671 will switch up to 150 milliamperes returned to a voltage of −20 volts maximum. The selected output is at a d-c level of −1.7 volts. Outputs not selected are open circuits for negative voltages. No positive voltages may be applied. The selected output level of the 4673 is −1.5 volts. Outputs are open-circuited, and may be as positive as +55 volts. The common anode for the indicators must be returned through a series resistor to a positive voltage. The voltage must be positive enough to start the indicator glowing; the resistor must be of such a value to limit the current to the proper value. Maximum current output at −1.5 volts is 4.5 milliamperes. The module is designed to limit current to 6.5 milliamperes maximum.

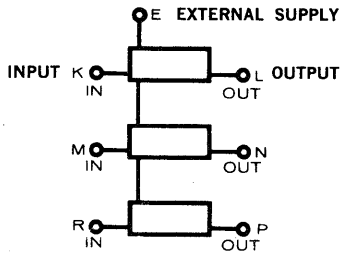
POWER: Type 4671: −15 volts/20 milliamperes; +10 volts (A)/0 milliamperes; +10 volts (B)/10 milliamperes. **Type 4673:** −15 volts/6 milliamperes; +10 volts (A)/5 milliamperes; +10 volts (B)/0 milliamperes.

CAUTION

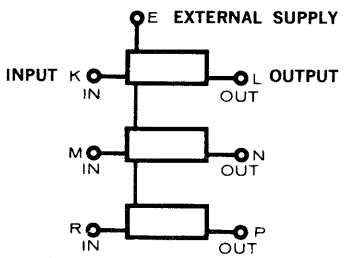
Because the output lines of the 4673 drive neon indicators, they will have large voltage transients. These lines should be routed well away from high impedance circuits to avoid undesired capacitive coupling.

SOLENOID DRIVERS
TYPES 4681, 4682

INPUT-OUTPUT



4681 SOLENOID DRIVER



4682 SOLENOID DRIVER

4681 SOLENOID DRIVER

Each solenoid driver supplies up to 500 milliamperes to solenoids returned to a negative external supply as great as −70 volts. The upper level is −3.5 volts when the output transistor is saturated. The lower level is the external negative supply. It should be connected to both pin E and the solenoid returns so that the internal damping diodes can prevent overvoltage during the turn of the transient.

INPUT: Inputs are DEC Standard Levels or equivalent, which represent four units of Base Load (No capacitance).

OUTPUT: A ground signal at the input produces a −3.5 volt output to turn the solenoid on. A −3 volt input cuts off the output transistor, turning off the solenoid current and allowing the output to return to the external supply. The external supply should be connected to pin E so that the damping diodes can prevent overvoltage when the output current is turned off. The external supply may be no greater than −70 volts. Each driver can supply up to 500 milliamperes to a load connected between its output and the negative supply.

POWER: −15 volts/144 milliamperes; +10 volts (A)/3 milliamperes; +10 volts (B)/0 milliamperes.

4682 SOLENOID DRIVER

Each solenoid driver supplies up to 100 milliamperes to solenoids returned to a positive external supply as great as +28 volts. The lower level is ground when the output transistor is saturated. The upper level is the external positive supply, which should be connected to both pin E and the solenoid returns so that the internal damping diodes can prevent overvoltage during the turn-off transient.

INPUT: The inputs require DEC Standard Levels or equivalent (1⅔ units Base Load).

OUTPUT: A −3 volt input produces a ground output level, turning the solenoid on. A ground input cuts off the output transistor, turning off the solenoid current and allowing the output to return to the external positive supply. The external positive supply should be connected to pin E so that the damping diodes can prevent overvoltage when the output current is turned off. The external supply may be no greater than +28 volts. Each driver can supply up to 100 milliamperes to a load connected between its output and the positive supply.

POWER: −15 volts/0 milliamperes; +10 volts (A)/4.8 milliamperes; +10 volts (B)/33.6 milliamperes.

GENERAL INFORMATION
DEC ↔ IBM

INPUT-OUTPUT

The modules described on the next few pages are for use in connecting DEC equipment to IBM equipment. The modules to be used depend on the type of IBM signal as shown in the table below.

		Logic Level	C Line	Transmission Line	Nominal Voltage
N	IBM-DEC	4506	4507	4507	+.5
	DEC-IBM	4669	4659	4659	−.5
P	IBM-DEC	4505		4505	−5.5
	DEC-IBM	4670		4660	−6.5
LINE CURRENT		0, 6 ma	0, 12 ma	0, 20 ma	

DIRECT DATA CONNECTION VOLTAGE MODE

IBM-DEC	4504 with 4508	0, +8 volts
DEC-IBM	1689	0, 80 ma.

VACUUM TUBE

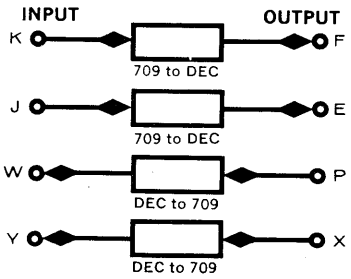
IBM-DEC	1672	+6, −26 volts
DEC-IBM		

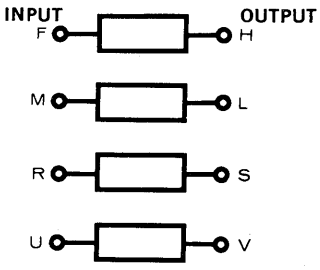
DEC ↔ IBM

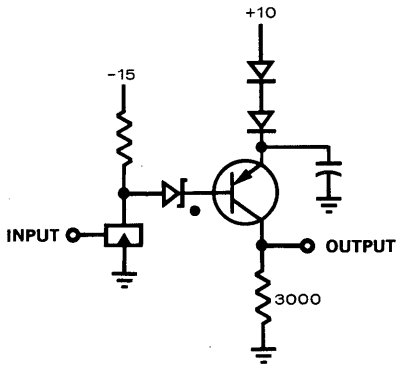
TYPES 1672, 1689

500 KILOCYCLES 5 MEGACYCLES

INPUT-OUTPUT







1672 DEC-709 CONVERTER | 1689 DEC-TO-7090 CONVERTER | SIMPLIFIED SCHEMATIC

1672 DEC-709 CONVERTER

Type 1672 provides signal compatiblity between the IBM 709 Electronic Data Processor and DEC Modules.

INPUT: 709-to-DEC Circuits: The upper level must be more positive than +5 volts, and the lower level more negative than −20 volts. There is no limit on rise and fall times. Input impedance may be approximated by 270,000 ohms and 15 picofarads to ground. **DEC-to-709 Circuits:** Standard Levels, one unit of pulse load with 250 picofarads.

OUTPUT: 709-to-DEC Circuits: The output is 0 volts for +10 volt input, and is −3 volts for −30 volt input. The output can drive four units of Base Load and/or any number of Pulse Emitter Loads provided only one is pulsed at a time. With an input rise or fall time of ½ microsecond the output delay will be less than ½ microsecond and the output rise or fall time less than ¼ microsecond. **DEC-to-709 Circuits:** The upper level will be more positive than +6 volts for a ground level input, and the lower level more negative than −26 volts for a −3 volt level input. The intended load is the 709 bus system. The DEC-to-709 circuit drives this load through a diode, and has no built-in load resistor of its own. The rise delay is less than ¼ microsecond and the rise time less than ½ microsecond. The fall delay is less than ½ microsecond and the fall time is limited by the shunt capacitance of the bus system. The DEC-to-709 circuit cannot drive the bus negatively since it drives the bus through a diode.

POWER: −15 volts/44 milliamperes; +10 volts (A)/0.3 milliamperes; +10 volts (B)/20 milliamperes.

1689 DEC-TO-7090 CONVERTER

The Type 1689 contains four circuits that convert DEC signals to voltage-mode IBM 7090 signals. A ground input signal will give an output of +8 volts and a −3 volt input will give an output of ground. Each circuit is able to drive a 93-ohm load with a total transition time of less than 0.20 microseconds.

INPUT: Standard levels (one unit of base load).

OUTPUT: Each output is able to drive a 93-ohm load. The output total transition time is less than 0.20 microseconds. The upper level is +8 (±2) volts, and the lower level is determined by the internal 3000-ohm load in parallel with the external load.

POWER: +10 volts (A)/180 milliamperes;* +10 volts (B)/180 milliamperes;* −15 volts/60 milliamperes.

---

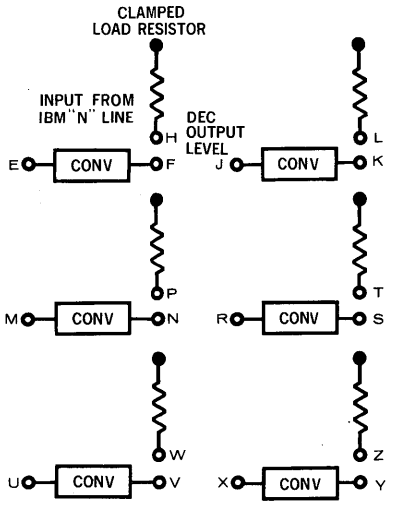
*This is the +10 volt current for 100% duty factor driving 93-ohm loads. When the output voltages are ground these currents are reduced to one milliampere.

DEC ↔ IBM

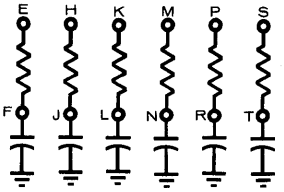
TYPES 4504, 4505, 4506, 4507, 4508

500 KILOCYCLES

INPUT-OUTPUT



4504, 4505, 4506, 4507
7090-TO-DEC CONVERTERS



4508 TERMINATOR

7090-TO-DEC CONVERTERS

These modules convert IBM 7090 signals to DEC voltages. Each module contains six circuits and six standard clamped load resistors. The total transition time is less than 800 nanoseconds for output rise and 200 nanoseconds for output fall.

INPUT: Type 4504 (from IBM direct data connection voltage mode): For input voltages between +4 and +15 the inverter is cutoff, and the input load is equivalent to a 6000-ohm resistor returned to −12 volts. For inputs less than +2 volts, the inverter is saturated and the input load is equivalent to 12,000 ohms returned to −12 volts.

Type 4505 (P-line signals from an N-block): The input terminals require an IBM current source of 0 and +6 milliamperes. The input circuit is similar to the IBM standard N-block load. The output inverter is cut off when the input current level is zero and saturated (ground) when the input current is 6 milliamperes. Input load is equivalent to a 100-ohm resistor returned to −6 volts. Any input current that exceeds this range may be used provided it does not exceed 20 milliamperes.

Type 4506 (N-line from a P-block):Inputs are standard IBM current-mode signal levels of 0 and 6 milliamprese returned to ground. The nominal input voltages are ground potential (±0.4 volts). The module input circuits are designed to terminate a 93-ohm cable and are equivalent to an IBM Alloy N-line Terminator. An input of +N (0 current) gives −3 volts out.

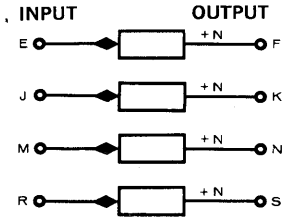
Type 4507 (N-line from a P-block): An IBM-type load used to terminate N-transmission lines (type C lines). When zero current flows on the line, the input is at +2 volts and the output inverter is off. When 13 milliamperes flows, the output transistor is on. The transmission line is terminated in 100 ohms.

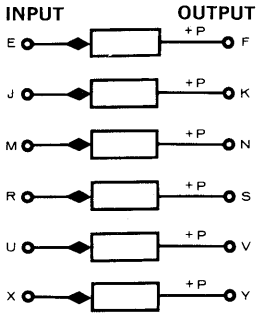
Type 4508: Terminates voltage-mode signals. The center conductor of the coaxial cables should be attached to pin E; the shield attached to F; etc.

POWER: Type 4504: −15 volts/120 milliamperes; +10 volts (A)/1.2 milliamperes; +10 volts (B)/1.2 milliamperes. **Type 4505:** −15 volts/115 milliamperes; +10 volts (A)/9 milliamperes; +10 volts (B)/0 milliamperes. **Type 4506:** −15 volts/85 milliamperes; ±10 volts (A)/9 milliamperes; +10 volts (B)/9 milliamperes. **Type 4507:** −15 volts/95 milliamperes; +10 volts (A)/20 milliamperes; +10 volts (B)/20 milliamperes.

DEC ↔ IBM
TYPES 4659, 4660
500 KILOCYCLES

INPUT-OUTPUT





4659 DEC-TO-7090 (N) TRANSMISSION LINE DRIVER

4659 DEC-TO-7090 (N) TRANSMISSION LINE DRIVER

The type 4659 is used to drive IBM 7090 N-transmission lines which are terminated with the IBM Terminating Shoe (IBM P/N 535098) or the Current Mode Transmission Line Drive Coupling Network (IBM P/N 371240). Lines terminated with this shoe require a minimum current of 20 milliampere to achieve proper switching. The module contains four identical transmission line drivers.

Maximum delay for output fall is less than 0.1 microsecond; for output rise, the maximum delay is less than 0.1 microsecond. Total transition time is less than 0.2 microsecond.

INPUT: Inputs are Standard DEC Levels of 0 and −3 volts. The input load is 1 unit of Base Load.

OUTPUT: Each output is capable of driving a 90-ohm load returned to +1.5 volts (a load equivalent to the IBM 535098 Terminating Shoe) between the limits of −1.0 and +1.5 volts. A 0 volt input produces a −1 volt (−N) output at −25 ma; a −3 volt input produces a +1.5 volt (+N) output at 0 ma.

POWER: −15 volts/100 ma; +10 volts (A)/0.6 ma.

4660 DEC-TO-7090 (P) TRANSMISSION LINE DRIVER

4660 DEC-TO-7090 (P) TRANSMISSION LINE DRIVER

The Type 4660 is used to drive IBM 7090 P-transmission lines which are terminated with the IBM Terminating Shoe (IBM P/N 535098) or the Current Mode Transmission Line Drive Coupling Network (IBM P/N 371240). Lines terminated with this shoe require a minimum current of 20 milliamperes to achieve proper switching. The unit consists of six identical transmission line drivers.

Maximum delay for output fall is less than 0.1 microsecond; for output rise, the maximum delay is less than 0.1 microsecond. Total transition time is less than 0.2 microsecond.

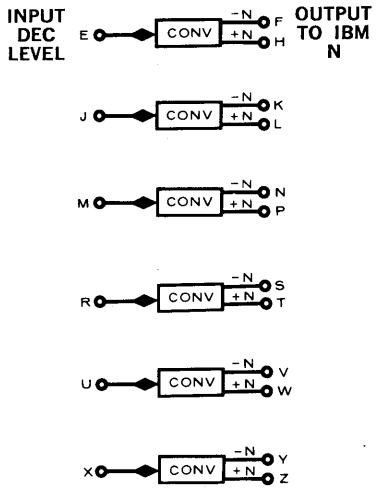
INPUT: Inputs are Standard DEC Levels of 0 and −3 volts. The input load is 1 unit of Base Load.

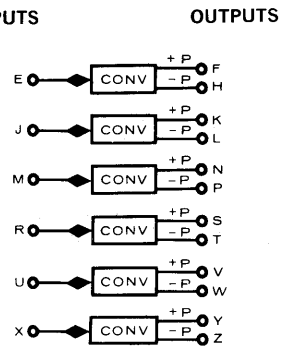
OUTPUT: Each output is capable of driving a 90-ohm load returned to −7.5 volts (the equivalent of the IBM P line termination) between the limits of −5.0 volts and −7.5 volts. A 0 volt input produces a −7.5 volt (−P) output at 0 ma. A −3 volt input produces a −5.0 volt (+P) output at −25 ma.

POWER: +10 volts (A)/160 ma.

DEC ↔ IBM
TYPES 4669, 4670
500 KILOCYCLES

INPUT-OUTPUT





4669 DEC-TO-7090 (N) CONVERTER

4669 DEC-TO-7090 (N) CONVERTER

The Type 4669 contains 6 circuits to convert Standard DEC signal Levels to IBM current mode "N line" signals. Each converter output simulates an IBM P block so that the module can drive an N line. Both the +N and −N outputs are provided so that a −3 volt input signal produces both a 0· and a 6-milliampere output.

Maximum frequency of module operation is 2 megacycles. With a 100-ohm load resistor connected to ground, the signal delay through the module is a maximum of 125 nanoseconds and the total transition time is a maximum of 250 nanoseconds.

INPUT: Input signals are Standard DEC Levels of ground and −3 volts. Each converter input represents 1 unit of Base Load. The capacitance presented by each input is approximately 150 picofarads.

OUTPUT: Signal outputs of 0 and 6 milliamperes ±10% are presented to an IBM Alloy N Line Terminator, producing nominal output voltages of ground potential ±0.4 volts. A −3 volt input at terminal E produces a −N level output at terminal F and a +N level output at terminal H. Similarly, a ground input at terminal E produces a +N level output at terminal F and a −N level output at terminal H. Unused output terminals may be left open circuited.

4670 DEC-TO-7090 (P) CONVERTER

POWER: −15 volts/120 ma; +10 volts (A)/0.5 ma; +10 volts (B)/0.5 ma.

*A 5000 picofarad capacitor to ground is recommended on each line driving the 7090 Direct Data Connection.

4670 DEC-TO-7090 (P) CONVERTER

The Type 4670 contains six circuits which convert DEC Standard Levels to IBM P-type current levels of 0 and +6 ma. Total transition time is 250 nanoseconds, maximum. The output circuits of this module are electrically similar to the unterminated outputs of IBM N-blocks.

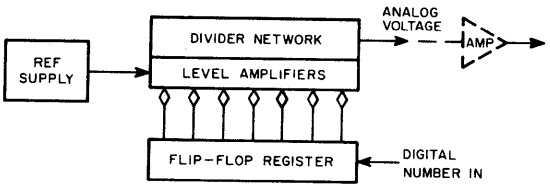
INPUT: Input voltages are Standard Levels of 0 and −3 volts. The load is light: 1/30 unit of DC Emitter Load for each input.

OUTPUT: The output is a current source of 0 or +6 milliamperes. The output is clamped to a maximum voltage of ground; it may drive a load returned to a voltage as negative as −12 volts. When terminal E is at −3 volts, 6 milliamperes comes out of terminal F and none comes out of terminal H. When E is at ground, the current comes out of H instead, reversing the output polarity. No termination is required on the unused outputs.

POWER: −15 volts/45 ma; +10 volts (A)/70 ma; +10 volts (B)/0 ma.

DIGITAL-TO-ANALOG

To convert from a digital number to an analog voltage, a resistive ladder network is connected to the flip-flop register which holds the digital number. The ladder network is weighted so that each digit of the register will contribute to the output voltage in proportion to its value.



Digital-to-Analog Conversion

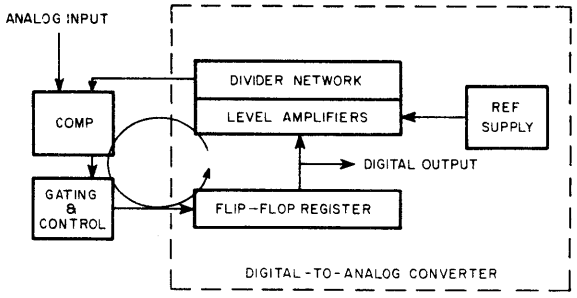
DIGITAL-TO-ANALOG

The digital input signal determines the analog output voltage, since the resistive ladder network is a passive component. Since digital voltage levels are not as precise as is usually required in an analog system, level amplifiers are often placed between the flip-flops and the ladder network. These may be Type 1677, 4678 or 4679 Level Amplifiers. Where less accuracy is required, Types 1667 or 4667 may be used. A reference voltage is supplied to the level amplifiers from a precision reference power supply such as Type 1562 or 1704. In some cases, an operational amplifier such as the Type 1751 is used on the output to lower the output impedance.

ANALOG-TO-DIGITAL

Analog-to-digital conversion is implemented by assuming a digital number, converting this number to an analog signal with a digital-to-analog converter, comparing this voltage with the analog input, and using the results of this comparison to adjust the assumed number. The comparison device used is the Type 1572 Difference Amplifier.

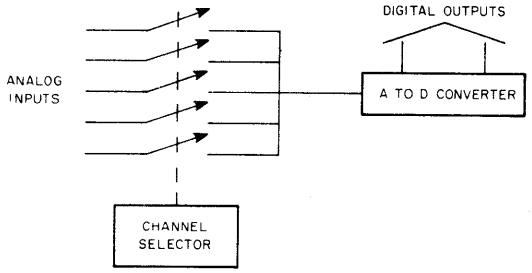
The speed of an analog-to-digital conversion system depends on the method chosen for adjusting the assumed number and on the accuracy required. (The accuracy has a two-fold effect, since it determines the number of steps in the adjustment process and the more accurate components, ladders level amplifiers, and the difference amplifier operate more slowly.)



Analog-to-Digital Converter

MULTIPLEXING

Analog signals can be multiplexed with a relay such as the Type 1807 or with a solid state switch such as Type 15780, 15781, 15782 or 15783.



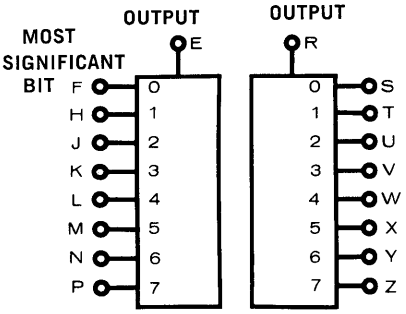
Multiplexed Analog-to-Digital Conversion System

ADDITIONAL INFORMATION

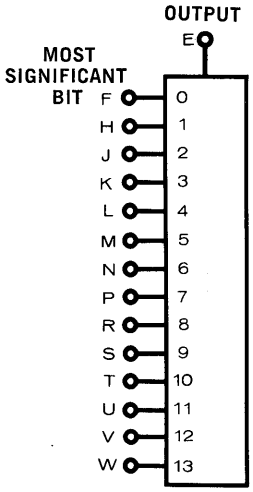
For further information, adjustment and calibration of procedures, and typical applications consult the DEC Analog-Digital Conversion Handbook.

ANALOG-DIGITAL
TYPES 1563, 1564, 1574

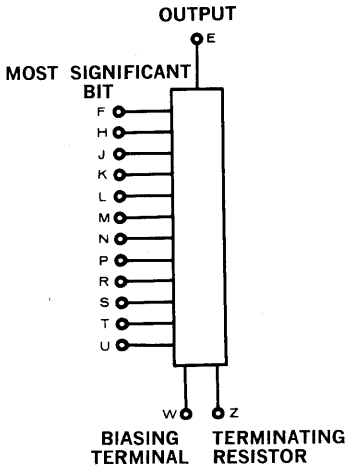
INPUT-OUTPUT



1563 DIVIDER



1564 DIVIDER



1574 DIVIDER

1563, 1564, 1574 DIVIDERS

The Types 1563, 1564, and 1574 are digital-to-analog converters employing binary weighted resistor ladder networks. The Type 1563 contains two converters for up to eight bits each. The Types 1564 and 1574 contain one converter each. The potentiometers are used for adjusting the most significant bits of each ladder. The Type 1954 Module Extender should be used during potentiometer adjustment. The settling time to 90 percent is about one microsecond for wire-wound ladders and 0.3 microseconds for metal film ladders. Settling time to final values is approximately the same in both cases and depends on use and loading.

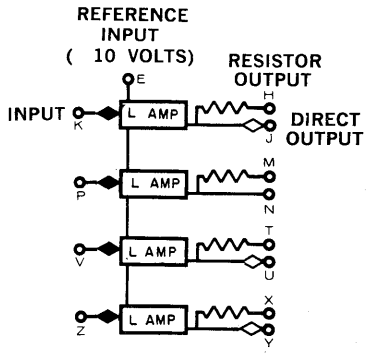
INPUT: The input impedance is 3000 ohms. The inputs are normally driven from precision reference bridges with 0 and −10 volt levels. When accuracy requirements permit, level amplifiers such as the Types 4667 or 1667 may be used with the more negative voltage level in the range of −3 to −10 volts. When accuracy of three bits or less is required, the input may be driven by Standard Levels of 0 and −3 volts. The input current will vary from 0 to ±1 milliampere (±1 unit of Base Load) depending on the state of the ladder. Inputs not in use must be grounded.

OUTPUT: The output impedance is 1000 ohms. The maximum open circuit output voltage is equal to the more negative input level less the value of the least significant bit.

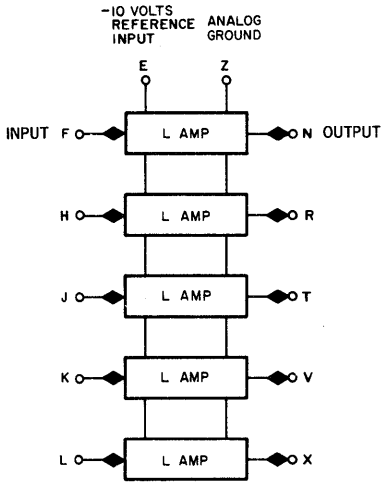
Module Type	T.C. ppm/°C	Resistor Type	Tolerance R out.
1563	20	ww	.1%
1564	20	ww	.1%
1574	14	mf	.35%

ANALOG-DIGITAL
TYPES 1677, 4678, 4679

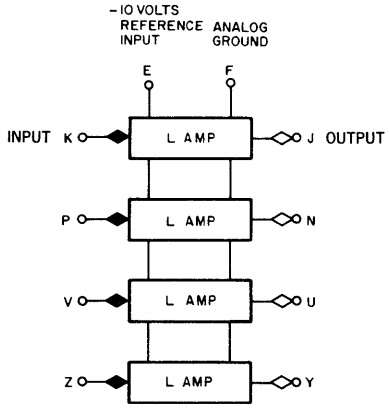
INPUT-OUTPUT



TYPE 1677 LEVEL AMPLIFIER



TYPE 4678 LEVEL AMPLIFIER



TYPE 4679 LEVEL AMPLIFIER

Module Type	Speed to 90% Output (μsec)	Input Load (ma, pf)	Inverting	Output Characteristics: Output Resistance (ohms)	Output Characteristics: Variation in R	Output Characteristics: V_G (mv offset at 0 v)	Output Characteristics: V_N (mv offset at −10 v)
1677	0.045	2, 156	yes	0-16	16	0 to 20	0 to −10
4678	0.8	0.5, 330	no	2	1.2	0 to −1.0	−0.5 to −1.5
4679	0.1	±1.3, 762	yes	4-9	0.5	3.2 to 9.7	−0.3 to −3.2

These precision level amplifiers are designed to drive the inputs of divider networks. They have extremely low output impedance and offset. The Type 1677 has a 100-ohm resistor output which allows it to be used as a bus driver. The Types 4678 and 4679 have analog grounds to allow isolation from noise and ground loops. However, these points must be tied to ground.

INPUT: Standard Level.

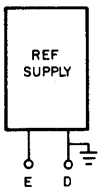
OUTPUT: Ground and −10 volt levels can supply up to three milliamperes with the accuracy shown in the table or up to 10 milliamperes at lower accuracy.

POWER: Type 1677: −15 volts/40 ma; +10 volts (A)/0.6 ma; +10 volts (B)/0.6 ma; −10 volts/−20 ma. **Type 4678:** −15 volts/145 ma; +10 volts (A)/0.4 ma; +10 volts (B)/31 ma; −10 volts/−20 ma. **Type 4679:** −15 volts/45 ma; +10 volts (A)/0.6 ma; +10 volts (B)/0.6 ma; −10 volts/−20 ma.

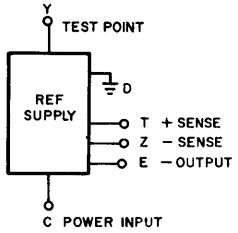
ANALOG-DIGITAL

TYPES 1562, 1704

INPUT-OUTPUT



1562 REFERENCE SUPPLY



1704 PRECISION REFERENCE SUPPLY

Module Type	Output	Current	Stability	Regulation	Ripple Peak to Peak
1562	−10v	±60 ma	2 mv/°C	30 mv, no load to full load	10 mv
1704	−10v	−90 to +40 ma	1 mv/8 hrs 1 mv/15 to 35°C 4 mv/0 to 50° C	0.1 mv, no load to full load	0.1 mv

Module Type	Adjustment Resolution	Input Power	Use	Output Impedance
1562	80 mv	−15 volts/100 ma +10 volts (B)/ 10 ma	Load with 500 mfd at load. May also be pre-loaded if desired	0.5 ohms
1704	0.01 mv	−15±2 volts/ 250 ma	See below for sensing and preloading	.0025 ohms

REMOTE SENSING

The input to the regular circuits of the 1704 is connected at sense terminals T (+) and Z (−). Connection from these points to the load voltage at the most critical location provides maximum regulation at a selected point in a distributed or remote load. When the sense terminals are connected to the load at a relatively distant location, a capacitor of approximately 100 microfarads should be connected across the load at the sensing point.

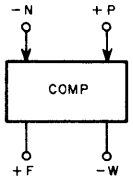
PRELOADING

The supplies may be preloaded to ground or −15 volts to change the amount of current available in either direction.

ANALOG-DIGITAL

TYPE 1572

INPUT-OUTPUT



1572 COMPARATOR

1572 COMPARATOR

The speed of the Type 1572 Comparator depends on the application, principally on the ratio of the voltage difference before passing through the switching point (V_B) to the voltage afterward (V_A). Speed is affected to a lesser degree by the length of time the input difference is at V_B, by the magnitude of V_A, by the source impedance, and by the load. Typical speeds in an analog-to-digital converter system where the source is a ladder network and level amplifiers and the load is one Base Load, are listed below. These speeds include allowance for extra divider settling time at high accuracy.

Two adjustable potentiometers control zero set and common balance.

V_B/V_A	V_A in mv	Time in μsec
−512	10	3.0
−128	40	1.6
−32	160	1.2
−2	20	0.6
−2	80	0.5
−1/512	10	0.15

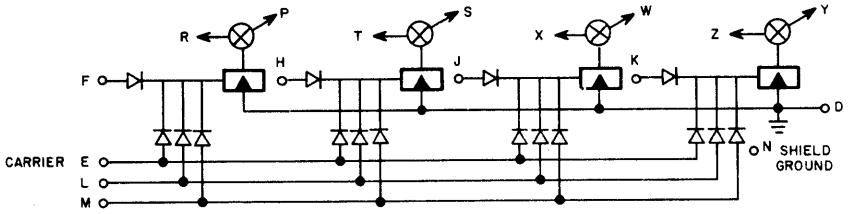
INPUT: 0 to −10 volts. Input impedance is one microampere and 75 picofarads. (The input current depends on the relative polarity of the two inputs. The more positive input may draw up to one microampere and the more negative input may supply up to one microampere. The maximum current difference between states is one microampere.)

OUTPUT: 0 and −3 volt levels. Output loading is seven units of Base Load at dc, one unit at maximum speed. Output resolution is one millivolt at dc. Common mode and temperature specifications are a 5-millivolt maximum equivalent input offset for a 10-volt common mode change and 20°C temperature change.

POWER: −15 volts/55 ma; +10 volts (A)/0; +10 volts (B)/21 ma.

ANALOG-DIGITAL
TYPES 15780, 15781, 15782, AND 15783

INPUT-OUTPUT



15780, 15781, 15782, and 15783
MULTIPLEXER SWITCHES

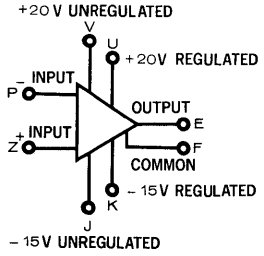
	15780	15781	15782	15783
Control				
Signals	Digital levels and 5-mc square wave			
Enable	−3 v (5-mc square wave pin E)			
Load	1/8 unit Emitter Load shared among grounded inputs			
Signal				
Max. voltage	12 v			30 v
Max. current	1 ma			1 ma
"On" offset (max.)	200 μV	100 μV	300 μV	300 μV
"On" resistance (max.)	50Ω	50Ω	100Ω	50Ω
"Off" leakage capacitance	2 na, 10 pf	2 na, 10 pf	10 na, 10 pf	2 na, 10 pf
Speed				
50% input to tolerance output	Delay + sync + charging time (RC)			
Turn on delay	400 nsec	600 nsec	600 nsec	600 nsec
Turn off delay	200 nsec	400 nsec	400 nsec	400 nsec
Synchronization	100 nsec	100 nsec	100 nsec	100 nsec

The multiplexer modules contain four, single pole, high speed, solid state switches. The switch drive is transformer-coupled so that the switch may be completely isolated from ground.

The switch is turned on when the three control inputs are at −3 volts (or open-circuited) and the carrier is receiving a 5-megacycle square wave. The square wave can be made using a 10-megacycle clock and a 10-megacycle flip-flop. Since the switches are low impedance, care should be taken to avoid shorting both signal terminals, or turning on two switches simultaneously if they are connected to the same point. For low frequency multiplexing, see the Type 1807 Relay module.

ANALOG - DIGITAL
TYPE 1751

INPUT-OUTPUT



1751 OPERATIONAL AMPLIFIER

1751 OPERATIONAL AMPLIFIER

The 1751 is a linear, d-c amplifier with a voltage gain of 10,000 and a current gain of up to 40,000 at low frequencies. It can operate in the presence of common mode signals between ±10 volts. Its maximum output voltage is ±10 volts; it can deliver as well as accept up to 20 milliamperes of output current.

BANDPASS (3 db down): 1.5 kc

GAIN-BANDWIDTH PRODUCT: 15 mc

OFFSET VOLTAGE TEMPERATURE COEFFICIENT: ±10 μV/°C between +55°C and −20°C

OFFSET VOLTAGE/SUPPLY VOLTAGE STABILITY COEFFICIENT: ±5 μV per 1% of supply voltage change

OFFSET VOLTAGE/COMMON MODE STABILITY COEFFICIENT: ±60 μV/V common mode between ±10V

INPUT CURRENT PER SIDE: 500 na

DIFFERENTIAL INPUT CURRENT: ±200 na

INPUT CURRENT TEMPERATURE COEFFICIENT: ±10 na/°C between −20°C and +55°C

DIFFERENTIAL CURRENT TEMPERATURE COEFFICIENT: ±4 na/°C between −20°C and +55°C

OPEN LOOP VOLTAGE GAIN: 10,000

DIFFERENTIAL INPUT IMPEDANCE: 100K Ω

OPEN LOOP OUTPUT IMPEDANCE: 2Ω (typical)

OUTPUT RISE AND FALL TIMES (follower configuration): 2 microseconds to 99%.

OUTPUT: ±10 volts, ±20 milliamperes, maximum. (Amplifier delivers or accepts current.) Output is short-circuit proof.

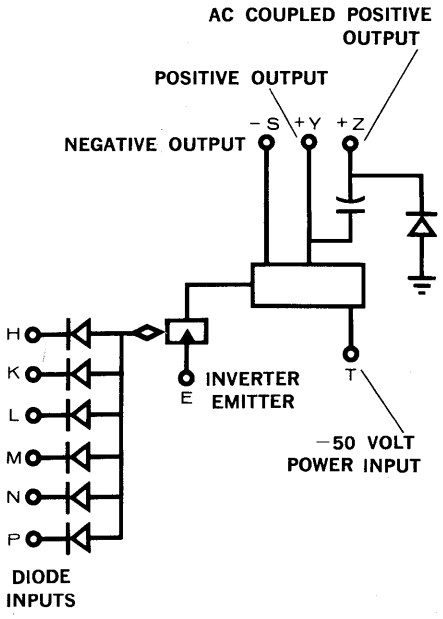
POWER: −15 volts (C)/0 ma; +10 volts (A)/0 ma; +10 volts (B)/0 ma; +20 volts (V)/5 to 45 ma depending on load; +20 volts regulated (U)/15 ma; −15 volts (V)/38 ma; −15 volts regulated (K)/13 ma; common (F).

SCOPE INTENSIFIER

TYPE 4676

100 KILOCYCLES

INPUT-OUTPUT



4676 INTENSITY AMPLIFIER

4676 INTENSITY AMPLIFIER

The Type 4676 Amplifier produces a 50 volt gate which will supply the grid or cathode of a cathode ray display tube. Outputs available include a direct coupled negative gate (0 to −50 volts), a direct coupled positive gate (−50 to 0), and an AC coupled positive gate with respect to ground. The total transition time for the amplifier is less than 8 microseconds.

INPUT: The amplifier will be turned on when all diode inputs are at ground or the emitter of the input inverter is at −3 volts. Input signals are DEC Standard Levels or equivalent. The diode inputs represent 2 units of Base Load shared among those inputs which are negative. The emitter input is 1 unit DC Emitter Load.

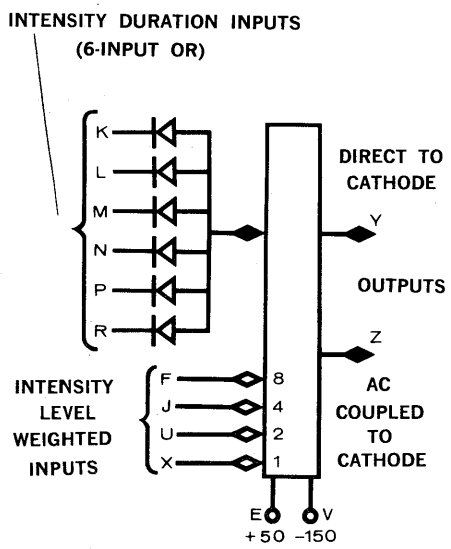
OUTPUT: Pin S will be at −50 volts when the amplifier is turned on and at −1 volt when the amplifier is off. ±5 ma can be supplied at the upper level. Output current at the lower level is determined by 36,000 ohms to −50 volts. Output pin Y will be at −1 volt when the amplifier is turned on and −50 volts when the amplifier is off. Pin Z is coupled to pin Y by a 0.1 microfarad capacitor. The output at this point will go to +50 volts when the amplifier is turned on and will return to ground when the amplifier is turned off. Pins Y and Z together can supply the same amount of current as pin S.

POWER: −50 volts/14 ma*; −15 volts/37 ma; +10 volts (A)/0.8 ma; +10 volts (B)/0.4 ma.

*Must be supplied from an external source.

SCOPE INTENSIFIERS
TYPE 4688

INPUT-OUTPUT



4688 VARIABLE AMPLITUDE NEGATIVE INTENSIFIER

4688 VARIABLE AMPLITUDE NEGATIVE INTENSIFIER

Type 4688 is used to generate the intensity gate in an oscilloscope display system when the intensity level is to be under program control. Selection of one of the sixteen-output gate amplitudes between −1 and −30 volts is accomplished by decoding the 4-bit intensity level input. The duration of the output gate is determined by the duration of the negative level input to any of the 6-input OR gates. The turn-on time varies between 0.1 and 0.3 microsecond, determined by the intensity level selected. The turn-off time is 0.3 microsecond for all intensity levels.

INPUT: Intensity Duration: The intensity gate will be on as long as there is a −3 volt level into any of the 6-input OR gates. The load is one unit of Base Load shared among the negative inputs. **Intensity Level:** These inputs are weighted as shown on the logic diagram. If all inputs are ground the maximum gate level of weight 15 will be generated. If, for example, only J and U are ground, a gate level of weight 6 will be generated. The maximum gate of −30 volts is produced with an input weight of 15, and the minimum gate of −1 volt is produced with an input weight of 0. The input load of F is two units of Base Load; pin J is one unit of Base Load; pin U is one-half unit of Base Load; and pin X is one-quarter unit of Base Load.

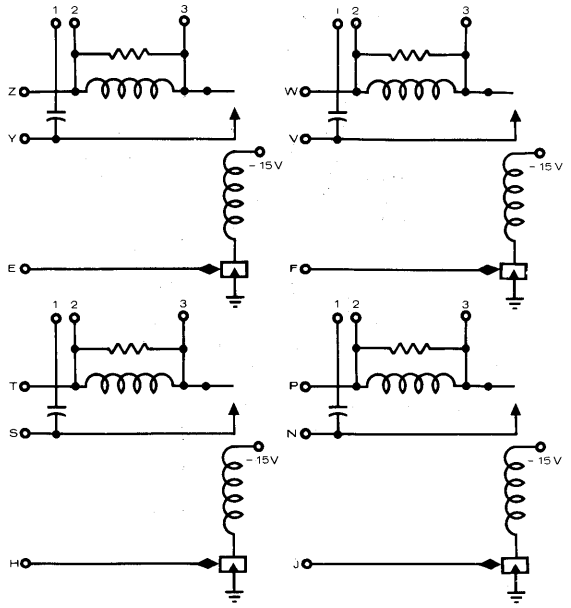
OUTPUT: Direct Output: This output is normally at a d-c level of about −1 volt. The output gate will be a −1 to −30 volt change from this quiescent level, so that the output gate will be at a d-c level of −2 to −31 volts. The turn-on time varies from 0.1 to 0.3 microsecond depending on the intensity level selected, while the turn-off time is 0.3 microsecond for all levels.

AC Coupled Output: This output is the direct output through a 0.01-microfarad capacitor with a diode and 100,000-ohm resistor to ground. The quiescent level is ground and the output gate will be between −1 and −30 volts.

POWER: −15 volts/10 ma; +10 volts (A)/0.6 ma; +10 volts (B)/0 ma; +50 volts/3 ma; −150 volts/14 ma.

RELAYS
TYPE 1803

INPUT-OUTPUT



1803 RELAY (OPTIONAL FILTER)

1803 RELAY (OPTIONAL FILTER)

The Type 1803 consists of four separate Form A Reed Relays, each with an optional protecting circuit. When the protecting circuit feature is desired, lugs 1 and 2 should be connected together. (The module is shipped with lugs 1 and 2 connected; lugs 2 and 3, disconnected.) To use the relay without the protecting circuit, lugs 2 and 3 should be connected together and lugs 1 and 2 should be left open. The protecting circuit consists of a capacitor and a parallel combination of an inductor and a resistor. The protection circuit slows down current and voltage rise time at the time of contact closure or opening in order to minimize undesirable effects on sensitive logic in the vicinity of the relay. The Type 1803 is used to drive heavy loads on computer or logic command. The frequency limit is one kilocycle. Maximum relay operating time is three milliseconds. These modules are twice as thick as standard types. In mounting, a blank space must be left next to each to accommodate the extra width.

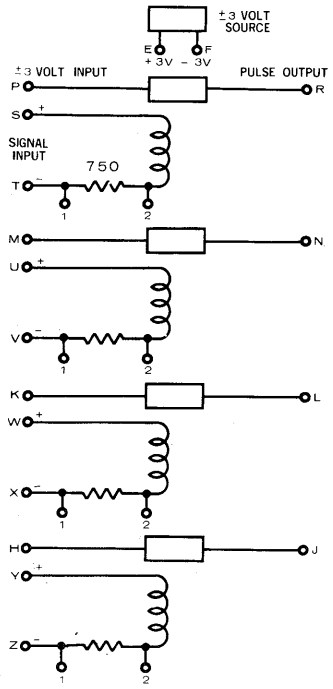
INPUT: A Standard Level of —3 volts at one milliampere operates the relay. The input impedance is one unit of DC Base Load.

OUTPUT: The relay contacts close when the input requirements are met. Maximum contact ratings are 15 watts, 1 ampere, and 250 volts.

POWER: —15 volts/124 ma; +10 volts (A)/0.6 ma.

RELAYS
TYPE 1804

INPUT-OUTPUT



1804 RELAY PULSER

1804 RELAY PULSER

The Type 1804 consists of four separate Form A Reed Relays, each with a pulse forming network incorporated into the relay contact circuit. The pulse forming network filters high frequency signals coupled from the relay driving lines to decouple input and output, converts the input level to a pulse with appropriate rise times, and recharges the circuit when the relay is off to prepare the circuit for the next operation. Because the width of the pulse produced is less than 25 microseconds and has considerable sawtooth ripple due to the relay contact bounce, it cannot be used for flip-flop complementing.

This module is useful in clearing and setting 4000 series flip-flops. At least 25 microseconds should elapse between clearing or setting operations and the logic operation which follows. The module is shipped without jumpers.

INPUT: A 15-volt signal operates the coil when lugs 1 and 2 are shorted together. When operating the coil on 24 volts, lugs 1 and 2 should not be shorted. Input to the relay contact and pulse forming network is from ±3 volt sources provided in the module (terminals E and F). If a positive output pulse is desired from pin R, pin E (+3 volts) is connected to pin P. The nominal coil current is 12 milliamperes.

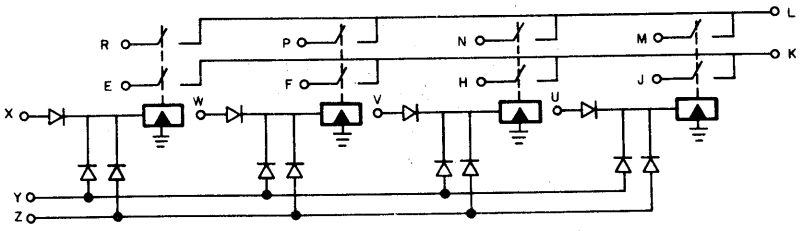
Similarly, a negative output pulse may be obtained by connecting pin F to P. Each circuit may be similarly connected to generate a positive or a negative pulse.

OUTPUT: The output is a ±2.5-volt pulse equal to or less than 25 microseconds in width with a maximum rise time of 150 nanoseconds on relay closure. It will drive five units of load. There is no pulse on relay opening.

POWER: −15 volts/8 ma; +10 volts (A)/7.5 ma; +10 volts (B)/10 ma.

RELAYS
TYPE 1807

INPUT-OUTPUT



1807 RELAY MULTIPLEXER

1807 RELAY MULTIPLEXER

The Type 1807 is a general purpose relay module designed principally for use as a multiplexer. The double pole relays connect lines to a common bus. Three-input, negative-diode decoding is employed with two of the inputs common to all four drivers. The frequency limit is 500 cps. Maximum time from enabling level to end of contact bounce is 1.2 milliseconds. As is typical of relays, this figure may vary widely from device to device.

INPUT: Negative AND diode gates. Each internal inverter, except the enabled one, requires ⅛ unit of DC Emitter Load shared among the grounded inputs. Inputs are Standard Levels of 0 and −3V.

OUTPUT: Relay contacts. Each relay is capable of withstanding 250 volts, dc, across contacts or from contacts to any other portions of the relay. Contacts are rated for 125 milliamperes dc maximum and have a contact resistance of less than 200 milliohms.

POWER: −15 volts/95 ma; +10 volts (A)/0.6 ma; +10 volts (B)/0 ma.

POWER SUPPLIES
TYPES 743, 743A, 778, 778A
DUAL 15 VOLTS

MODULE ACCESSORIES

The Type 743 is a dual channel, floating 15-volt power supply designed to adequately withstand wide, line and load variations for general systems use. The 743A is a 743 power supply with a 50-cycle transformer. For input voltage connections, refer to the Type 728A Power Supply, page 11.8. The Type 778 is a dual channel, floating 15-volt power supply designed to be mounted on the plenum door of a DEC Computer Cabinet. The 778A is a 778 power supply with a 50-cycle transformer. For input voltage connections refer to 728A Power Supply, page 11.8. These packages consist of two identical supplies, each one made up of resonant transformer, full wave silicon rectifier and filter capacitor.

ELECTRICAL CHARACTERISTICS

OUTPUT VOLTAGE: 15 volts DC
OUTPUT CURRENT: 1.5 to 8.5 amperes per channel. At least 1.5 amperes must be drawn to assure proper load regulation.
LINE AND LOAD REGULATION: Output voltage remains between 14.5 and 16.5 volts when load varies from minimum to maximum and line voltage varies from 105 to 125 volts.
P-P RIPPLE: 0.7 volt (20% more ripple on the 50-cycle types).
LINE FREQUENCY REGULATION: ±2% of line frequency.

MECHANICAL CHARACTERISTICS
778-778A

PANEL WIDTH: 16⅝″
PANEL HEIGHT: 12″
DEPTH: 5¼″
FINISH: Chromicoat
POWER INPUT CONNECTION: Cinch Jones No. 141 terminal strip
POWER OUTPUT CONNECTION: Heyman tab terminals to fit with AMP "Faston" Receptacles Series 250, part no. 41774.

MECHANICAL CHARACTERISTICS
743-743A

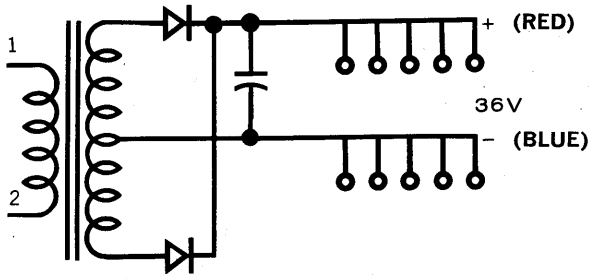
PANEL WIDTH: 19″
PANEL HEIGHT: 5¼″
CHASSIS WIDTH BEHIND PANEL: 17⅛″
CHASSIS DEPTH BEHIND PANEL: 10¼″
CHASSIS HEIGHT BEHIND PANEL: 5″
FINISH: CHASSIS — Chromicoat
PANEL — Brown "tweed"
POWER INPUT CONNECTION: Amphenol 160-5 socket
POWER OUTPUT CONNECTION: DC: 10-32 screw terminals. AC: Amphenol 160-4 Socket. A Power cable with two-prong adapter is also furnished.

POWER SUPPLIES

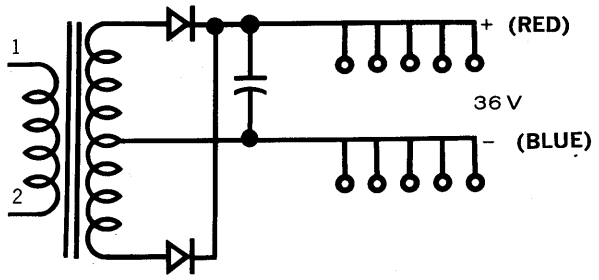
TYPES 772, 772A

DUAL 36 VOLTS

MODULE ACCESSORIES



Supply A



Supply B

The Type 772 is a dual channel floating, 36-volt DC power supply. Each output can supply 1.0 to 5.0 amperes. Each channel contains a resonant transformer, a full wave silicon rectifier, and filter capacitors, resulting in a simple rugged supply able to adequately withstand wide line and load variations for general system use. The unit was designed to be mounted on the plenum door of a DEC Computer Cabinet and may be mounted on standard racks with suitable adapter plates.

The 772A is a 772 power supply with a 50-cycle transformer. For input voltage connections, refer to the 728A power supply.

ELECTRICAL CHARACTERISTICS

OUTPUT VOLTAGE: 36 volts DC, floating

OUTPUT CURRENT: 1.0 to 5.0 per channel. At least 1.0 ampere must be drawn from the supply to assure proper load regulation.

LINE AND LOAD REGULATION: Output voltage will be between 35 and 39 volts when load varies from minimum to maximum and line voltage varies from 105 to 125 volts AC

RIPPLE: $\leq$2 volts (20% more ripple on the 50-cycle type).

LINE FREQUENCY REGULATION: $\pm$2% of line frequency.

MECHANICAL CHARACTERISTICS

PANEL WIDTH: 16⅝″

PANEL HEIGHT 8″

DEPTH BEHIND PANEL: 5″

FINISH: Chromicoat

POWER INPUT CONNECTION: Cinch Jones No. 141 terminal strip

POWER OUTPUT CONNECTION: Heyman Tab terminals to fit with AMP "Faston" Receptacles Series 250, part No. 41774.

POWER SUPPLIES
TYPE 730
DUAL VARIABLE 0 to 20 VOLTS

MODULE ACCESSORIES

The Dual Variable Power Supply Type 730 is a two-channel, floating output unit for general purpose laboratory use. It is designed to offer the maximum in flexible, maintenance-free operation. Some of its features are: resonant transformers to protect against line variations, variable transformers to give continuous control of output voltage, and silicon rectifiers to insure long life. Placement of meters and all controls on the front panel provides complete ease of operation. Incorporation of two channels in the same package results in a more economical, more compact unit. This is the supply normally used for marginal checking of systems made from DEC Modules.

ELECTRICAL CHARACTERISTICS

OUTPUT VOLTAGE: 0 to ±20 volts DC continuously variable (no load)

OUTPUT CURRENT: 2.5 amperes per channel

LOAD REGULATION: Maximum 3.0 volts drop at 20 volts when load varies from minimum to maximum

LINE REGULATION: 2.0% for input variation from 105 to 125 volts AC

P-P RIPPLE: 1.0 volt at maximum load

LINE FREQUENCY REGULATION: 60 cycle ±2%

MECHANICAL CHARACTERISTICS

PANEL WIDTH: 19″

PANEL HEIGHT: 5¼″

CHASSIS WIDTH BEHIND PANEL: 17⅛″

CHASSIS DEPTH BEHIND PANEL: 10¼″

CHASSIS HEIGHT BEHIND PANEL: 5″

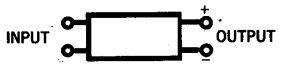
FINISH: CHASSIS — Chromicoat; PANEL — Brown "tweed"

POWER INPUT CONNECTION: Amphenol 160-5 socket

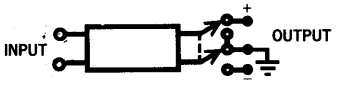
POWER OUTPUT CONNECTION: DC: 10-32 screw terminals. AC: Amphenol 160-4 Socket. A 3-wire power cable with a two-prong adapter is also furnished.

POWER SUPPLIES
TYPES 734, 734A, 734B, 734C
VARIABLE 0 to 20 VOLTS

MODULE ACCESSORIES



734, 734A



734B, 734C

The Types 734, 734A, 734B, 734C floating power supplies are variable from 0 to 20 volts. They are often used for system marginal checking. A variable transformer gives continuous control of output voltage, a resonant transformer protects against line variations; and silicon rectifiers insure long life. The placement of meter and controls on the front panel facilitates operation. Although designed for mounting on the plenum door of a computer cabinet, these 17 by 8 inch units may be mounted on a standard 19-inch rack using suitable adapter plates.

The Types 734A through 734C are 734 power supplies with 50-cycle transformers. For input voltage connections, refer to 728A power supply.

The Types 734B and 734C are 734 power supplies each with a switch and five extra terminals. The switch is wired to provide a plus or minus voltage with respect to ground.

MECHANICAL CHARACTERISTICS

OUTPUT VOLTAGES: 0 to 20 volts DC, continuously variable

MAXIMUM OUTPUT CURRENT: 2.5 amperes

LOAD REGULATION: Maximum 3.0 volts drop at 20 volts when load varies from minimum to maximum

LINE REGULATION: 2% for input variation from 105 to 125 volts AC

P-P RIPPLE: $\leq$1.0 volts. (20% more ripple on the 50-cycle types.)

LINE FREQUENCY REGULATION: $\pm$2% of line frequency.

ELECTRICAL CHARACTERISTICS

PANEL WIDTH: 16 5/8"

PANEL HEIGHT: 8"

DEPTH: 5 3/8"

FINISH: Chromicoat

POWER INPUT CONNECTIONS: Cinch Jones No. 141 Terminal Strip

POWER OUTPUT CONNECTIONS: Heyman Tab Terminals to fit with AMP "Faston" Receptacles Series 250, part no. 41774.

POWER SUPPLIES
TYPES 722, 722A
+10, −3 −15 VOLTS

MODULE ACCESSORIES

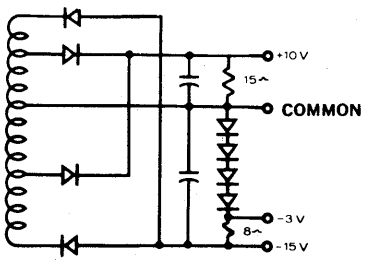


Figure 1

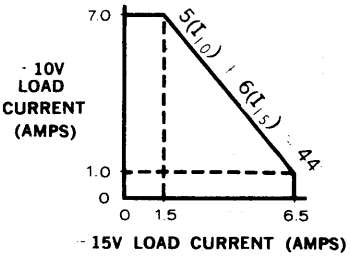


Figure 2

The Types 722 and 722A are simple rugged +10, −3, and −15 volt power supplies designed for mounting in a standard 19-inch rack. These supplies are able to adequately withstand wide line and load variation for general system use. The Type 722A is a 722 with a 50-cycle transformer. For input voltage connections for the 722A, refer to the 728A power supply.

ELECTRICAL CHARACTERISTICS

OUTPUT VOLTAGE: +10 volts; −3 volts; −15 volts DC

OUTPUT CURRENT: +10 volts: 0 to 7.0 amperes*
−3 volts: 0 to ±1.2 amperes
−15 volts: 0 to 6.5 amperes*

COMBINED LINE AND LOAD REGULATION: For all combinations of above loads and line between 105 and 125 volts AC.
−15 volts: −14.5 volts to −16.5 volts
−3 volts: −2.8 volts to −3.4 volts
+10 volts: 9.5 volts to 11.5 volts

P-P RIPPLE: 0.7 volts for +10 and −15 outputs and less than 15 mv for the −3 outputs. **

LINE FREQUENCY REGULATION: ±2% of line frequency.

* The sum of the output currents is limited by the equation in figure 2.

**There is 20% more ripple on the 50 cycle power supply.

MECHANICAL CHARACTERISTICS

PANEL WIDTH: 19″

PANEL HEIGHT: 5¼″

CHASSIS WIDTH BEHIND PANEL: 17⅛″

CHASSIS DEPTH BEHIND PANEL: 9 15/16″

CHASSIS HEIGHT BEHIND PANEL: 5″

FINISH: CHASSIS — Chromicoat; PANEL — Brown "tweed"

POWER INPUT CONNECTION: Amphenol 160-5 socket

POWER OUTPUT CONNECTION: DC: Cinch Jones S-308F.P. socket that fits to DEC 750 Power Cable 110 AC: Amphenol 160-4 Socket. A 3-wire power cable with two-prong adapter is also furnished.

POWER SUPPLIES
TYPES 728, 728A
+10, −15 VOLTS

MODULE ACCESSORIES

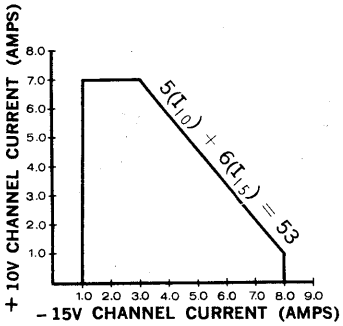


Figure 1 COMBINED LOAD OPERATING REGION

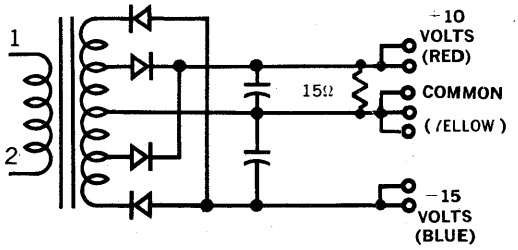


Figure 2 SCHEMATIC

The Types 728 and 728A (+10, −15 volt) Power Supplies are capable of withstanding wide line and load variation for general system use. When used singly the 10-volt channel can supply 0 to 7.5 amperes, or the 15-volt channel can supply 1.0 to 8.5 amperes. The 728A is a 728 with a 50-cycle transformer. For input voltage connections, see Figure 3. These supplies are designed for mounting on the plenum door of a computer cabinet, but can also be mounted on a standard 19-inch rack with suitable adapter plates.

728A Input Connections

Line: 3 and 4
112.5V 2 to 4, 3 to 7
123.5V 1 to 4, 3 to 8
195V 1 to 5
220V 1 to 6
235V 2 to 8

Shipped Connected for 235V.
Pilot light, if used, is permanently connected to 2 and 3.

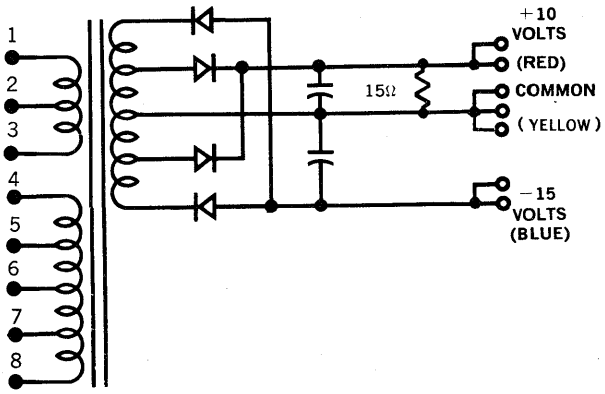


Figure 3 728A SCHEMATIC

ELECTRICAL CHARACTERISTICS

OUTPUT VOLTAGE: +10 volts, −15 volts DC, floating.

OUTPUT CURRENT: 1. When only one output is loaded: +10 volts: 0 to 7.5 amperes −15 volts: 1.0 to 8.5 amperes. 2. When both outputs are loaded: +10 volts: 0 to 7 amperes* −15 volts: 1.0 to 8.0 amperes*. At least 1.0 ampere must be drawn from the −15 volt channel to assure proper load regulation.

LINE AND LOAD REGULATION: The output voltage remains between −14.5 to −16.5 volts for the −15 volt channel and within +9.5 to +11.5 volts for the +10 volt channel, when load varies from minimum to maximum and line voltage varies from 105 to 125 volts AC.

P-P RIPPLE: less than 0.7v for +10v output
less than 0.7v for −15v output
(20% more ripple on the 50-cycle type.)

LINE FREQUENCY REGULATION: ±2% of line frequency.

MECHANICAL CHARACTERISTICS

PANEL WIDTH: 16⅝″

PANEL HEIGHT: 8″

DEPTH: 5¼″

FINISH: Chromicoat

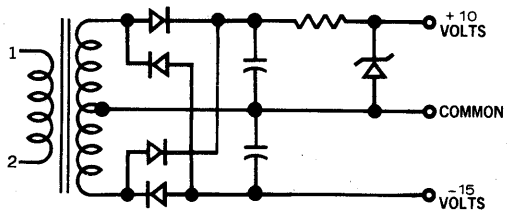
POWER INPUT CONNECTION: Cinch Jones No. 141 terminal strip

POWER OUTPUT CONNECTION: Heyman tab terminals to fit with AMP "Faston" Receptacles Series 250, part no. 41774.

*The sum of the output currents is limited by the following equation: $5(I_{10}) + 6(I_{15}) = 53$. (See Figure 1.)

POWER SUPPLIES
TYPES 782, 782A
+10, −15 VOLTS

MODULE ACCESSORIES



SIMPLIFIED SCHEMATIC TYPE 782

The Type 782 Power Supply is a ruggedly built, low cost power supply which fits a standard 19-inch rack. Providing +10 and −15 volts, it is an ideal unit for powering modules for general system use. The Type 782A is a 782 power supply with a 50-cycle transformer. For input voltage connections, refer to 728A power supply.

ELECTRICAL CHARACTERISTICS

OUTPUT VOLTAGE: +10 volts, −15 volts DC, floating.

OUTPUT CURRENT: −15 volts: 0.5 amp to 3 amps; +10 volts: 0 to 0.4 amps.

LINE AND LOAD REGULATION: The output voltage remains between −14.5 and −16.5 volts for the −15 volt output and within +9.2 and +11.5 volts for the +10 volt output, when load varies from minimum to maximum and line voltage varies from 105 to 125 volts AC.

P-P RIPPLE: Less than 0.4v for +10 volt output; less than 0.6v for −15 volt output. (20% more ripple on the 50-cycle type.)

LINE FREQUENCY REGULATION: ±2% of line frequency.

MECHANICAL CHARACTERISTICS

PANEL WIDTH: 19″

PANEL HEIGHT: 5 3/16″

DEPTH: 5 1/8″

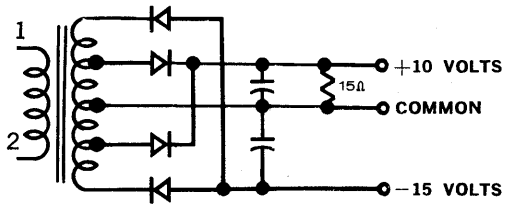
FINISH: Chromicoat

POWER INPUT CONNECTION: Screw terminals provided on transformer.

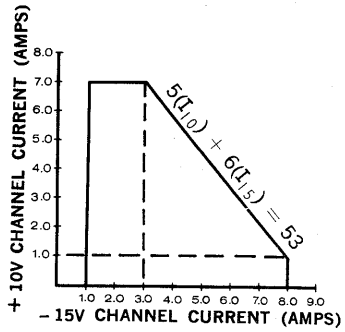
POWER OUTPUT CONNECTION: Four-terminal barrier strip with screw terminals and tabs which fit AMP "Faston" receptacle series 250, part number 41774.

POWER SUPPLIES
TYPES 783, 783A
+10, −15 VOLTS

MODULE ACCESSORIES



SIMPLIFIED SCHEMATIC TYPE 783



COMBINED LOAD OPERATING REGION

The Type 783 Power Supply (+10, −15 volt) is a simple, rugged supply capable of withstanding wide line and load variation for general systems use. The graph above shows the permissible region of operation when both outputs are used. When used singly, the 10-volt output can supply 0 to 7.5 amperes, or the 15-volt output can supply 1.0 to 8.5 amperes. It is designed for mounting in a standard 19-inch rack. The Type 783A is a 783 power supply with a 50-cycle transformer. For input voltage connections, refer to the 728A power supply.

ELECTRICAL CHARACTERISTICS

OUTPUT VOLTAGE: +10 volts, −15 volts DC, floating.

OUTPUT CURRENT: 1) When only one output is loaded: +10 volts: 0 to 7.5 amperes, −15 volts: 1.0 to 8.5 amperes. 2) When both outputs are loaded: +10 volts: 0 to 7.0 amperes*, −15 volts: 1.0 to 8.0 amperes*.

At least 1.0 ampere must be drawn from the −15 volt channel to assure proper load regulation.

LINE AND LOAD REGULATION: The output voltage remains between −14.5 and −16.5 volts for the −15 volt output and within +9.5 and +11.5 volts for the +10 volt output, when load varies from minimum to maximum and line voltage varies from 105 to 125 volts AC.

P-P RIPPLE: Less than 0.7v for +10v output. Less than 0.5v for −15v output. (20% more ripple on the 50-cycle type.)

LINE FREQUENCY REGULATION: ±2% of line frequency.

*The sum of the output currents is limited by the following equation: $5(I_{10}) + 6(I_{15}) = 53$.

MECHANICAL CHARACTERISTICS

PANEL WIDTH: 19″

PANEL HEIGHT: 10½″

DEPTH: 6″

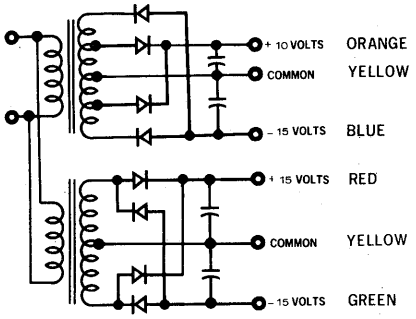
FINISH: Chromicoat

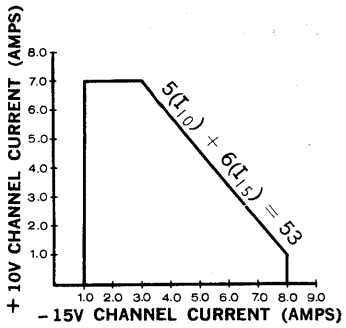
POWER INPUT CONNECTION: Screw terminals on transformer.

POWER OUTPUT CONNECTION: Four-terminal barrier strip with screw terminals and tabs which fit the AMP "Faston" receptacle series 250, part number 41774.

POWER SUPPLIES
TYPES 779, 779A
+10 VOLTS, −15 VOLTS: +15 VOLTS AND −15 VOLTS

MODULE ACCESSORIES





The Type 779 is a combination power supply for driving DEC logic and solenoids. It may be mounted on the plenum door of a DEC cabinet. The logic supply delivers +10 volts and −15 volts. The solenoid supply consists of a lightly filtered 30-volt floating supply. It is center-tapped so that it may also be used to supply +15 and −15 volts. The Type 779A is a 779 power supply with a 50-cycle transformer. For input supply voltage connections, refer to the 728A power supply.

ELECTRICAL CHARACTERISTICS

OUTPUT VOLTAGE: Supply 1: +10 volts, −15 volts floating. Supply 2: Center-tapped 30 volts (+15, −15).

OUTPUT CURRENT: Supply 1: When only one output is loaded, +10 volts: 0 to 7.5 amperes; −15 volts: 1.0 to 8.5 amperes. When both outputs are loaded, +10 volts: 0 to 7.5 amperes*; −15 volts: 1.0 to 8.0 amperes*. Supply 2: When only one output is loaded, +15 volts or −15 volts: 1.5 to 8.5 amperes. When both supplies are loaded, +15 volts or −15 volts: 1.0 to 7.5 amperes**.

COMBINED LINE AND LOAD REGULATION: For all combinations of above loads and line between 105 and 125 volts AC, +10 volts: 9.5 volts to 11.5 volts. All 15-volt supplies: 14.5 volts to 16.5 volts.

P-P RIPPLE: Supply 1: 1.0 volt for +10, 0.6 volts for −15. Supply 2: 1.1 volt on both outputs. There is 20% more ripple on the Type 779A.

LINE FREQUENCY REGULATION: ±2% of line frequency.

MAXIMUM VOLTAGE: between output and chassis is 300 volts DC.

MECHANICAL CHARACTERISTICS

PANEL WIDTH: 16⅝″

PANEL HEIGHT: 12″

CHASSIS DEPTH: 5½″

FINISH: Chromicoat

POWER INPUT CONNECTION: Jones Strip 141.

POWER OUTPUT CONNECTION: Heyman tab terminals to fit with AMP "Faston" Receptacles Series 250, part 41774.

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* The sum of the output currents is limited by the following equation: $5(I_{10}) + 6(I_{15}) \leq 53$. See Figure 1.

** The sum of the output currents is limited by the following equation: $I_{+15} + I_{-15} \leq 8.5$.

POWER CONTROL
TYPE 831

MODULE ACCESSORIES

The Type 831 Power Control Panel features a two-pole circuit breaker which provides convenient one-step control and protection for entire systems, including auxiliary equipment. The panel fits standard 19-inch racks and is finished with a protective aluminum conversion coating. Available in 4-, 10-, 20-, or 30-ampere capacity.

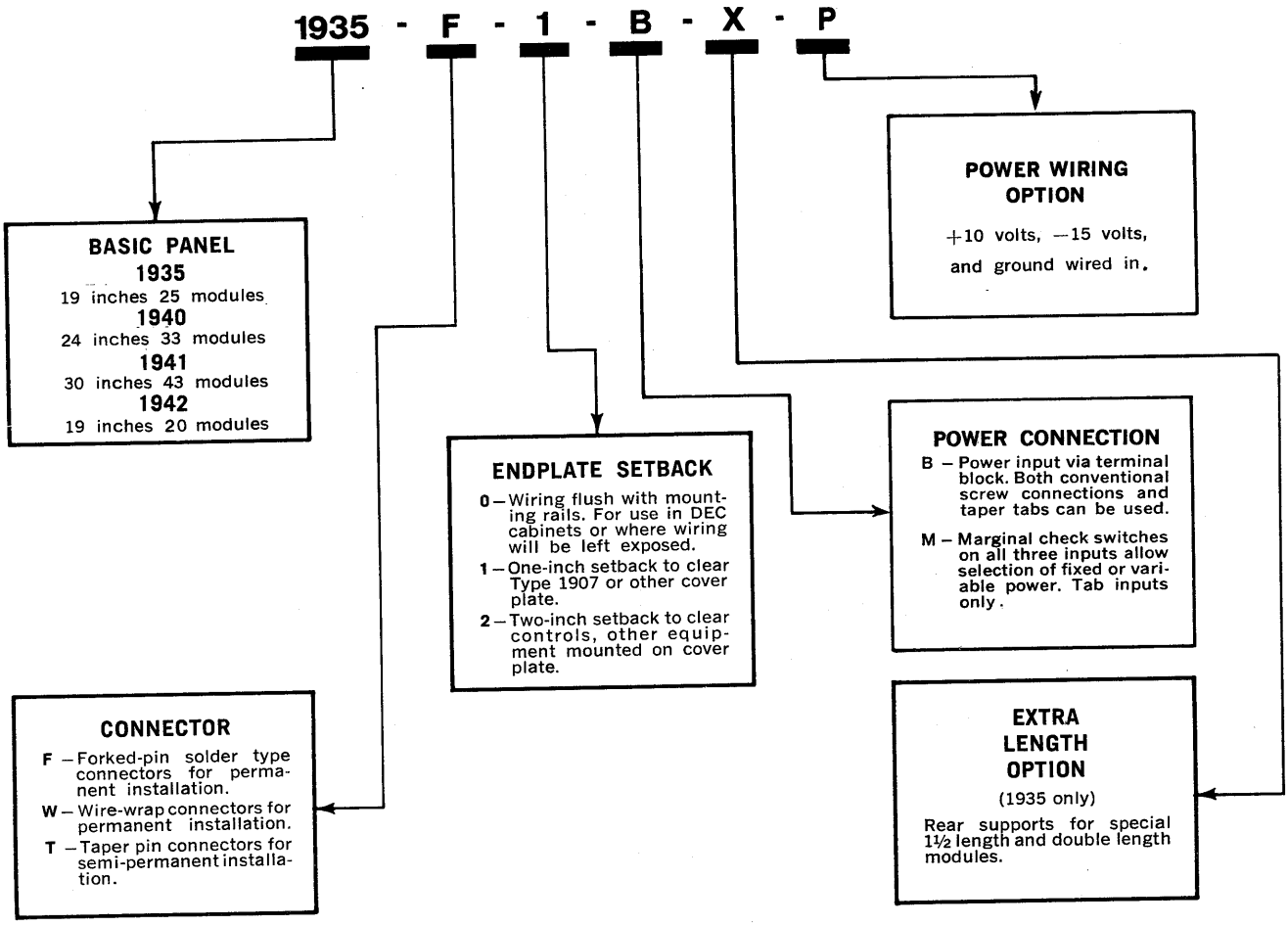
PANEL HEIGHT: 3-7/16″
PANEL WIDTH: 19″

MOUNTING PANELS
TYPE 1935, 1940, 1941, 1942

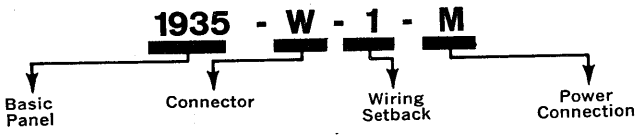
MODULE ACCESSORIES

The Types 1935, 1940, 1941, and 1942 Mounting Panels give maximum operational flexibility and reliability to systems constructed with Digital modules. A total of 72 different versions of the Type 1935 and 36 different versions of the Types 1940, 1941, and 1942 are available to satisfy customer requirements. Combinations include choice of connector, endplate setback, and power connection. Optional rear supports permit use of extra length modules. See page 4.8 for wiring hints. Heavy duty sockets supply high contact pressure for reliable connections. Staggered-pin solder connectors facilitate wiring and checkout. Lettered contacts permit positive identification, prevent wiring errors. Specially constructed top and bottom plate retainers have raised guides to simplify module insertion and removal. Filtered power connections, using tantalum capacitors, suppress local noise. Advanced mechanical design provides improved ventilation. Optional hold-down bar, Type 1936-19, for use with 1935 and 1942 only, reduces vibration and keeps modules securely mounted when panel or system is moved. Type 1936-24 is used with 1940.

ORDERING INFORMATION: Specify connector, endplate setback, and power connections. Use the chart below to select the combination required. An example of complete ordering information, showing all categories involved, follows.



A Type 1935 Mounting Panel with wire wrap connectors, endplate setback of one inch, and marginal check switches on the power connection, would be ordered by



For the same model as above, but with rear supports for extra length modules and power wiring the order becomes 1935-W-1-M-X-P

MECHANICAL DIMENSIONS:

WIDTH: **Type 1935:** 19 inches **Type 1940:** 24 inches **Type 1941:** 30 inches **Type 1942:** 19 inches.

HEIGHT: All types: 5-3/16 inches

DEPTH: Depends on endplate setback: 7⅞", 8⅞", or 9⅞".

Tabs for power connections fit AMP "Faston" receptacles, Series 250, part number 41774.

TYPE 1936 HOLD DOWN BAR: Option which adds ½" to depth of the Type 1935, 1940 or 1942.

MOUNTING PANEL AND POWER SUPPLY
TYPE 1938, 1938A

MODULE ACCESSORIES

The Types 1938 and 1938A are combined power supplies and mounting panels for DEC Modules, designed to fit a standard 19-inch rack and to hold up to 19 modules. A choice of three types of connectors is available. The power supply provides up to 0.4 amperes at +10 volts, and from ½ to 3 amperes at — 15 volts. See page 4.8 for wiring hints. Heavy duty sockets supply high contact pressure for reliable connections. Staggered pin solder connectors facilitate wiring and checkout. Lettered contacts permit positive identification, prevent wiring errors. Specially constructed plate retainers have raised guides to simplify module insertion and removal. Advanced mechanical design provides improved ventilation. The Type 1938A is a 1938 Power supply with a 50-cycle transformer. For input voltage connections, refer to the 728A Power supply.

ELECTRICAL CHARACTERISTICS

OUTPUT VOLTAGE: +10 volts, —15 volts DC.

OUTPUT CURRENT: —15 volts: ½ to 3 amp; +10 volts: 0 to 0.4 amp.

LINE AND LOAD REGULATION: The output voltage remains between —14.5 and —16.5 volts for the —15 output, and within +9.2 and +11.5 volts for the +10 output, when load varies from minimum to maximum and line voltage varies from 105 to 125 volts AC.

P-P RIPPLE: Less than 0.4 volt for +10 output. Less than 0.6 volt for —15 output; 20% more ripple on the 50-cycle type.

LINE FREQUENCY REGULATION: ±2% of line frequency.

MECHANICAL CHARACTERISTICS

PANEL WIDTH: 19″

PANEL HEIGHT: 5 3/16″

DEPTH: 11½″

FINISH: Chromicoat

POWER INPUT CONNECTIONS: Screw terminals provided on transformer.

MODULES ACCOMMODATED: 19

MODULE SOCKETS: New heavy duty socket with deep fork solder contacts for logical wiring. Also available with taper pin sockets and wire wrap lugs.

TYPE 1938 and 1938A ORDERING INSTRUCTIONS:

Use the chart below to select the connector required.

1938-F-P

BASIC PANEL
1938
1938A

POWER WIRING OPTION
+10 volts, —15 volts, and ground wired in.

CONNECTOR
F — Forked-pin solder type connectors for permanent installation.
W — Wire-wrap connectors for permanent installation.
T — Taper pin connectors for semi-permanent installation.

MOUNTING PANELS
TYPE 1906

MODULE ACCESSORIES

DEC Type 1906 Mounting Panel provides patchboard flexibility for up to 20 DEC Modules used as plug-in units for permanent systems. The panel permits System Modules to serve either as a permanent or as experimental logic packages, thus providing additional economy. The panel uses 5¼ inches of vertical space in a standard 19-inch relay rack. The chassis is furnished in brown "tweed". The patchboard is "chocolate brown". The terminals (E through Z) of each module connector are attached to 18 corresponding banana-jack sockets on the front of the mounting panel, making possible speedy interconnections with stacking banana-jack patchcords Type 911. The functions of the various lettered sockets can be readily determined from the logical diagrams of the respective modules, enabling the engineer to make a rapid circuit set up that is easily modified. Wiring hints on page 4.8 should be consulted, especially when the 6000 (10-megacycle) series is being used. The lead length from the jack to the module socket is one inch, so that every patchcord is effectively lengthened by two inches.

MOUNTING PANELS
TYPE 1916

MODULE ACCESSORIES

The Type 1916 is a 17-inch rack mounting panel designed to fit on the plenum doors of a Computer Cabinet. It will accommodate up to twenty-one modules. Logical wiring is solder-connected to the mounting panel. Marginal check switches are provided at the power input terminals. Mounting panel finish is chromicoat. See page 4.8 for wiring hints.

MECHANICAL CHARACTERISTICS

MODULES HOUSED	PANEL LENGTH	CHASSIS LENGTH
21	17″	14 13/16″

MOUNTING PANELS
TYPE 1913

MODULE ACCESSORIES

Type 1913 is a 19-inch mounting panel designed to accommodate a maximum of six current drivers (Types 52, 53, 58, 62, 63, or 68) or four current drivers and one current/voltage calibrator Type 72.

MECHANICAL CHARACTERISTICS

PANEL HEIGHT: 10½" CHASSIS DEPTH: 7"

FINISH: SIDE PANELS — Brown "Tweed" or Blue.
UPPER AND LOWER PANELS — Chromicoat

MOUNTING PANEL COVERS
TYPE 1907, 1925, 1926, 1929

MODULE ACCESSORIES

Blank panels designed to fit 19-inch racks are available for mounting indicator lights and control switches. Panels are finished in brown "tweed" or blue and are available in 3½ inch (Type 1925) or 5¼ inch (Type 1926) heights. The Type 1907 and 1929 Mounting Panel Covers are designed to cover the power and logic wiring for the Type 1935, 1938, or 1942 Mounting Panels. The cover is fastened to the mounting panels with captive screws that fit tapped holes in the mounting panels. The cover is shaped to fit over the wiring terminals and is finished in brown "tweed or blue". Dimensions are 5¼ by 19 inches. The 1907 is a plain cover, while the 1929 is louvered for better air flow.

BLANK SYSTEM MODULES
TYPE 1950, 1951, 1955, 1957, 1958, 1964, 1965

MODULE ACCESSORIES

Blank system modules are available for mounting special circuits. All necessary hardware is provided, including the circuit board, standard 22-pin plug, protective aluminum frame, and a set of eyelets.

Assembled modules are available with a plain glass board or a prepunched vector board. The latter type, includes miniature terminals for easy component insertion. Unassembled blank modules have a copper-clad glass board on which the user can print his own special circuit. The following types are available:

TYPE	CONFIGURATION	AVAILABLE CIRCUIT SPACE
1950	Assembled plain board	4⅛ by 5
1951	Unassembled	4⅛ by 5
1955	Assembled, vector board	4⅛ by 5
1957	Assembled, plain board	4⅛ by 8
1958	Unassembled	4⅛ by 8
1964	Assembled, plain board	4⅛ by 12
1965	Unassembled	4⅛ by 12

MODULE EXTENDER AND PULLER
TYPE 1954, 1960

MODULE ACCESSORIES

1954 SYSTEM MODULE EXTENDER

The Type 1954 System Module Extender allows access to the module circuitry without breaking connections between the unit and the mounting panel wiring. The module extender is particularly useful with the digital-to-analog converters and other modules which contain potentiometers to be adjusted.

1960 SYSTEM MODULE PULLER

The Type 1960 System Module Puller may be used to remove System Modules from the mounting panels. The modules may also be removed by hand, if desired.

PATCHCORDS AND TOOLS
TYPE 911, 912, 1961, 1962, 1963

MODULE ACCESSORIES

911 PATCHCORDS

DEC Type 911 Banana-Jack Patchcords are supplied in color-coded lengths of 2 inches (brown), 4 inches (red), 8 inches (orange), 16 inches (yellow), 32 inches (green), and 64 inches (blue). These easy-to-use patchcords may be stacked to permit multiple connections at any circuit point on the graphic front panels of the DEC line of Digital Laboratory Modules. The cords are supplied in snap-lid plastic boxes of 10 for handy storage.

912 PATCHCORDS

Taper-pin patchcords can be inserted or removed from the mounting panels with needle-nosed pliers or with special inserter and puller tools available as optional accessories. Type 912 Patchcords featuring gold-plated taper pins, are available in color-coded standard lengths of 2, 4, 8, 16, 32, and 64 inches. All cords are shipped in quantities of 100 in handy polystyrene window-type, snap-lid boxes. Gold plated taper-pins are AMP 53 series, part number 41649 (strip form) or 41666 (loose piece).

1961-1962-1963 TAPER PIN TOOLS

Taper pin inserter and extractor tools are available for easy handling of the taper pin connections. A crimper tool is also available for attaching taper pins to special wires.

The spring loaded taper pin inserter tool, Type 1962, permits taper pins to be easily seated in their mating receptacles. The tool is designed to permit dexterity in confined areas. The spring mechanism in the tool assures that the proper amount of force will be exerted for placing the pin firmly in the receptacle. In addition, the inserter tool will firmly support both the pin and wire during the entire operation. This tool may also be purchased from AMP Inc. as AMP Model Number 380306-3.

The Type 1963 Taper Pin Extractor Tool allows the pins to be removed easily from the mating connectors. The two-prong fork may be hooked over the metal portion of the pin so that the connector is removed without strain on the wire. The AMP Model Number is 380305-1.

A hand crimper tool, Type 1961, may be used to crimp taper pins. Use of this tool assures a good electrical connection. The AMP Model Number is 47042.

POWER CABLES
TYPE 922, 1919

MODULE ACCESSORIES

1919 POWER CABLE

The Type 1919 Power Cable is used to connect the Type 722 or 784 Power Supply to a module mounting panel. The Type 1919 has a Jones plug on one end for connection to the power supply and spade lugs on the other end for connection to the system module mounting panels.

922 TEST POWER CABLE

A Type 922 Test Power Cable permits testing and maintenance of individual modules. Power is brought into the module through a cable with a Cinch-Jones male plug which connects to the Type 722, 765, or the Type 784 Power Supply. Logical connections are brought out to eyelets for use with the Type 911 stacking banana-jack patchcords.

INDICATOR LIGHTS
TYPE 4901, 4906, 4908

MODULE ACCESSORIES

4901
INDICATOR LIGHT BRACKET

Bracket containing nine 15 volt indicator bulbs. Mounting feet fit under connector mounting nuts of any general-purpose DEC System Module mounting panel. Designed to be driven from Type 1669 or Type 4689 indicator driver modules. Power required is −15 volts at 270 ma. Overall dimensions are 4½" x ⅞" x 1⅞".

4906
INDICATOR WITH AMPLIFIER

Single indicator lamp with transistor driver. May be panel mounted in ⅜" hole; bulb is replaceable from the front. Power required is −15 volts at 30 ma. Overall dimensions are 2½" x ⅝" x ⅞".

4908
PANEL INDICATOR ASSEMBLY

Consists of lamp, spring clip, and terminal. Facilitates panel mounting of individual indicator lamps. Power required is −15 volts at 30 ma. Requires a 5/16" hole for mounting.

All indicators utilize 28-volt bulbs which are operated at 15 volts. This provides more than adequate illumination and greatly extends the life of the bulbs.

Type 4906: The inputs to the transistor drivers require DEC Standard Levels or equivalent and represent one unit of DC Base Load (no speedup capacitors). Minus 3 volts lights the lamp; zero volts turns it off. **Type 4901, 4908:** These units contain the lamp assembly only and should be driven by indicator drivers such as Types 1669 or 4689.

INDICATORS
TYPE 4902, 4903

MODULE ACCESSORIES

4902
INDICATORS WITH AMPLIFIERS

Same as 4903 except with 7 indicator bulbs and transistor drivers. Power required is −15 volts at 210 ma. Overall dimensions are 4″ x 3¾″ x 15/16″.

4903
INDICATORS WITH AMPLIFIERS

Bracket containing 18 indicator bulbs and transistor drivers. Mounting holes provided. Power required is −15 volts at 540 ma. Amphenol connector provided for input. Overall dimensions are 9½″ x 3¾″ x 15/16″.

All indicators utilize 28-volt bulbs which are operated at 15 volts. This provides more than adequate illumination and greatly extends the life of the bulbs. The Type 4902 and 4903 have indicators on half-in. centers and mate with Amphenol connectors, Types 143-010 and 143-022 respectively. Indicators are 5/16 of an inch in diameter.

INPUT: The input is the base of a transistor inverter with no input resistor. It may be driven by the resistor outputs of the DEC Flip-flops Type 4201, 1201, 1209, or 6202, or from any flip-flop that has a 3000-ohm resistor wired between it and the driver. It represents one unit of DC Base Load (no speedup capacitors). Minus 3 volts lights the lamp; zero volts turns it off.

INDICATOR PANEL AND POWER CABLE
TYPE 750, 960

MODULE ACCESSORIES

750 POWER CABLE

The Type 750 is a 2½-foot power cable equipped with Jones plugs on both ends for connecting the Indicator Panel Type 960 to the Type 784 Power Supply.

960 INDICATOR PANEL

The Type 960 Indicator Panel provides remote indicator lights for use with a 1906 Patchcord Mounting Panel. The panel contains 18 indicator lights and associated drive circuits. The input to each of the 18 indicator circuits is a miniature banana jack. The rear of the panel is protected by a cover which also contains power receptacles for Type 750 Power Cables.

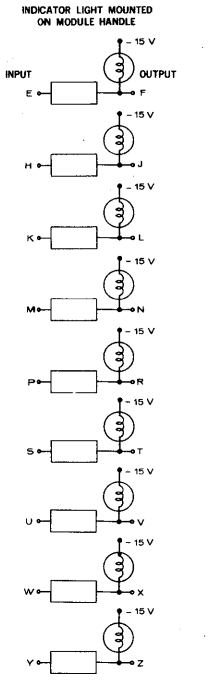
INPUTS: An input signal of −3 volts (DEC Standard Level) lights the corresponding light. The load is one unit of Base Load without speed-up capacitors. If these lights are driven by logic levels more than 6 feet away, a 3000-ohm resistor should be inserted in series with each wire at the sending end. There is an adapter plug within the Type 960 which contains a set of such resistors. This adapter plug should be removed when the resistors are at the sending end of the cable.

MECHANICAL CHARACTERISTICS

19 inches long, 3½ inches high, and 7 inches deep.
POWER: +10V (A)/1.4 ma.; +10 (B)/1.4 ma.; −15V/540 ma.

INDICATOR DRIVERS
TYPE 4691

MODULE ACCESSORIES



The Type 4691 contains nine transistor amplifiers and nine indicator lights mounted on the handle of the module. Each amplifier can drive external loads of up to 30 milliamperes.

INPUTS: Each input requires DEC Standard Levels or equivalent and represents two units of Base Load without speed-up capacitors.

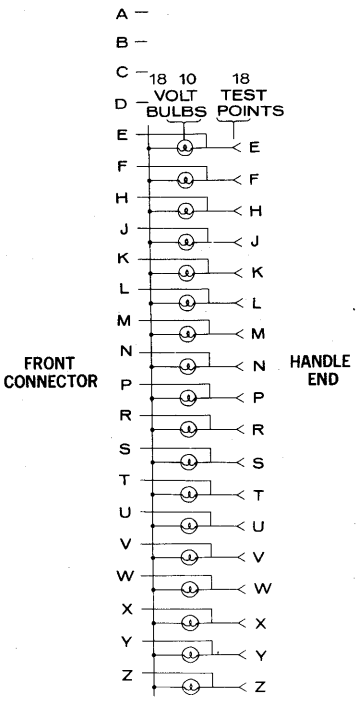
OUTPUTS: Each output is capable of driving resistive loads of up to 30 milliamperes. The load device should be connected to −15 volts.

POWER: −15 volts/270 ma.; +10 volts (A)/2 ma.; +10 volts (B)/0 ma.

OTHER POWER: Up to 270 milliamperes may be supplied from the external −15 volt supply when all remote loads are turned on.

INDICATOR BOARD
TYPE 4909

MODULE ACCESSORIES

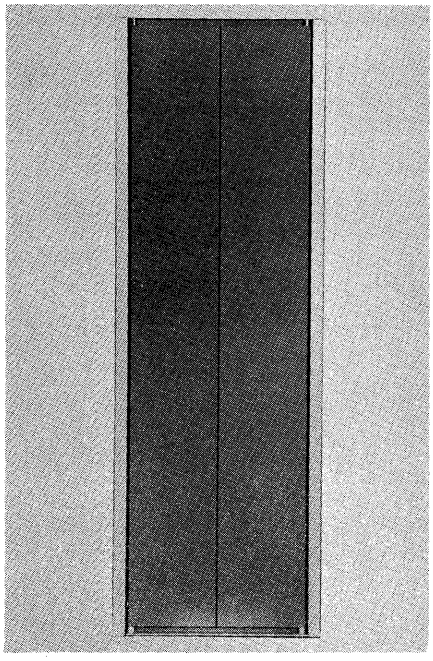


Eighteen light bulbs at the handle end of this module respond to the presence of +10 volts at their respective connector pins. System wiring can be checked out by plugging 4909 modules into all sockets, and observing which lights light up as +10 volts is applied to each successive logic connection. There are 18 test points on the handle to allow a test prod to apply +10 volts to any of the 18 signal pins from the module side of the mounting panel. Each bulb draws about 70 milliamperes with +10 volts applied.

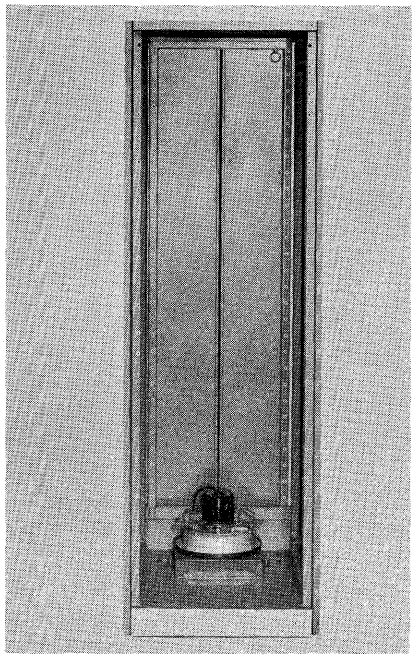
CABINETS

TYPES CAB-1, CAB-2, CAB-3, CAB-6, CAB-8

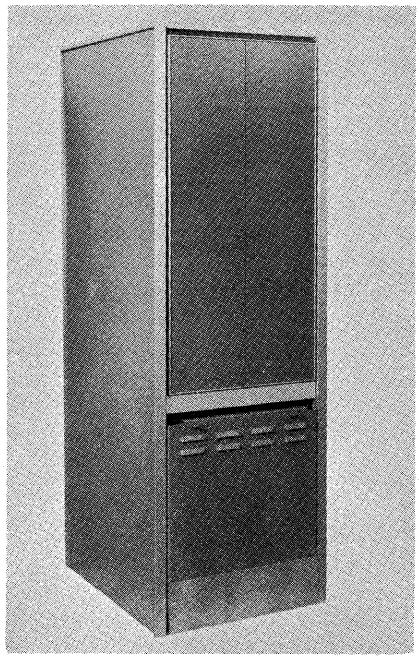
MODULE ACCESSORIES



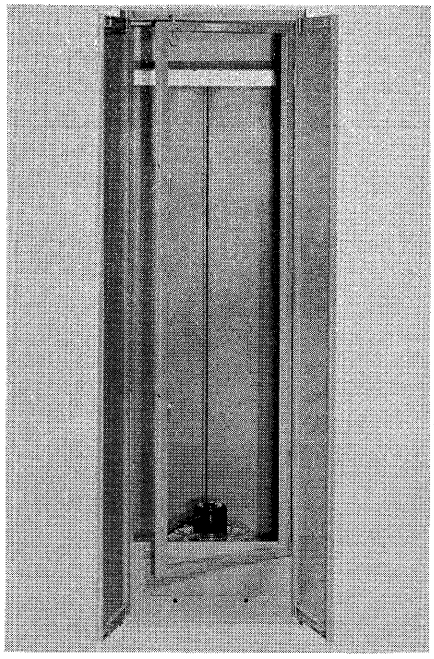
CAB-1



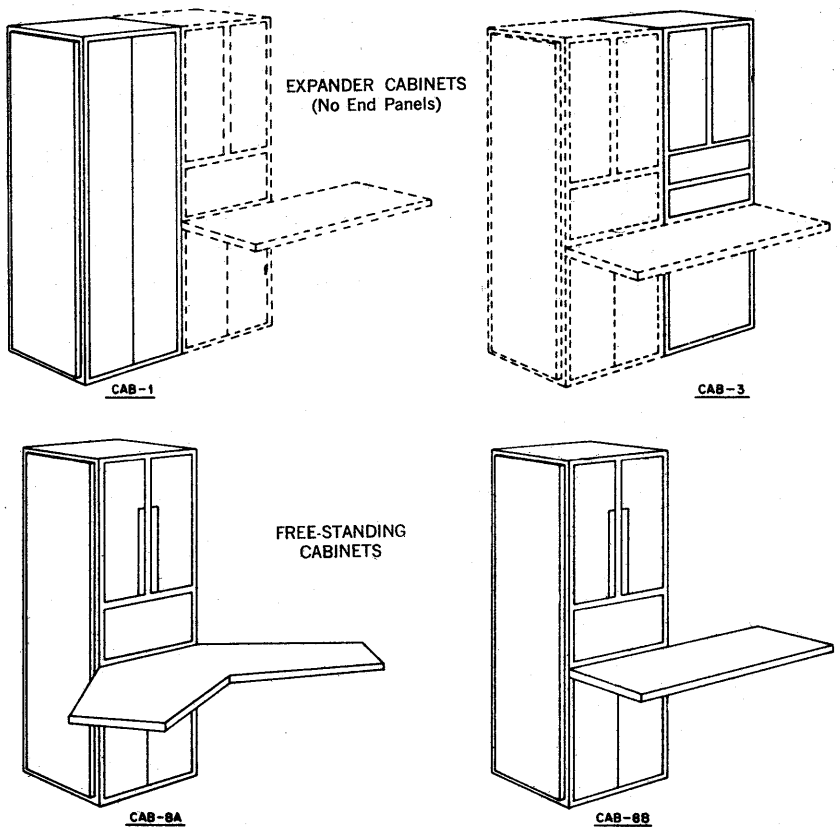
CAB-2



CAB-3



CAB-6 (Inside view)



CABINETS

TYPES CAB-1, CAB-2, CAB-3, CAB-6, CAB-8

MODULE ACCESSORIES

Digital offers a variety of cabinets which can be used to build up special systems.

The Type CAB-1 can be used alone or in multicabinet systems where only one control cabinet or indicator cabinet is desired. The standard cabinet has full length French doors for access to logic wiring.

The Type CAB-2 cabinet is used where many controls and indicators are required. No French doors are provided in front.

The Type CAB-3 is intended as an expander cabinet for the PDP-8. The cabinet has a wood panel in the front above the table top. The wood panel comes down to the table and the bottom of the panel can be removed to add accessories from the table up. In addition to use as an expander cabinet, the CAB-3 provides a means of ready access to the front of the system.

The Type CAB-6 can be used with other cabinets or as a remote indicator cabinet. The French doors give access to logic wiring. The brushed aluminum, clear anodized panel is placed at a convenient height for viewing indicators.

All cabinets are alike with the exception of end panels and the French door configuration. All cabinets come, as shown, with fan, fan housing, and filter. A plenum door for mounting power supplies is provided in the rear behind full length French doors. Casters are provided for mobility. All cables enter through an access cutout in the bottom of the cabinet.

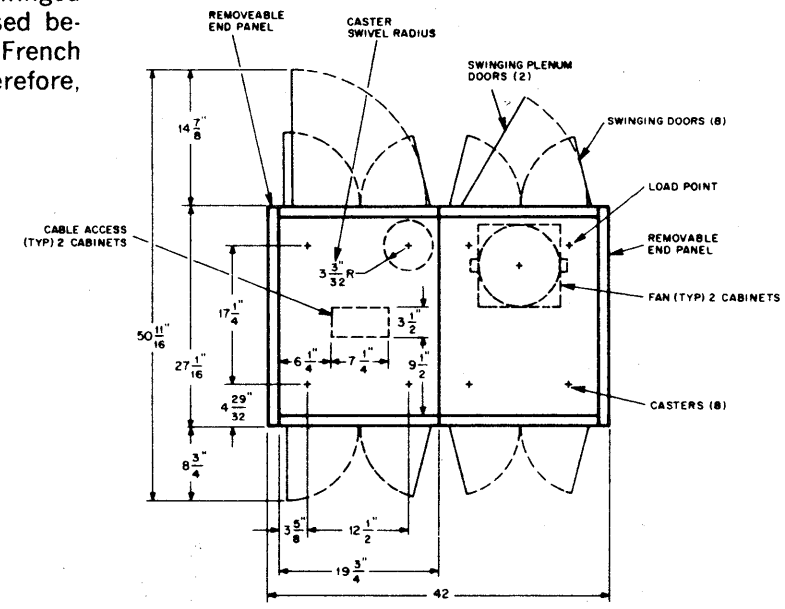
The CAB-8A is a free-standing cabinet, with a winged table with legs. The logic modules are housed beneath this table and enclosed with short French doors. The CAB-8A is not expandable and, therefore, not recommended for systems that have multiple bays bolted together.

The CAB-8B is similar to the CAB-8A with the exception of the table. The table is rectangular and is positioned so that other cabinets may be placed adjacent to the cabinet. The CAB-1 will normally be bolted to the left on the CAB-8B and the CAB-3 will normally be bolted to the right of the CAB-8B.

Cabinets can be factory assembled into multicabinet groups. Cabinet types can be mixed in one group except for the CAB-2, which has different end panel and trim details.

The cooling fan built into the bottom of each cabinet is adequate to ventilate up to 5¼ in. mounting panels of B-series FLIP CHIP modules mounted near the bottom of the cabinet. If the lower dissipation R-series modules of W or A series modules make up a significant portion of the system, more modules can be installed. Four-hundred watts is the maximum total power that should be dissipated in all of the modules mounted in any one cabinet. The top panel of each cabinet must be removed when FLIP CHIP modules are installed, and all side panels and plenum doors should be closed except during system checkout.

The price of the first cabinet includes end panels. The price of each additional cabinet includes the cabinet joining hardware. Cabinets are shipped assembled and on skids with the tables packed separately.



DIMENSIONS

Cabinet

42 in. wide
27-1/16 in. deep
69⅛ in. high

SERVICE CLEARANCE

8¾ in. front
14⅞ in. rear

In addition to the 728 power supply, there are several other items especially designed for plenum door mounting. For example, there are the 1946 mounting panel and the 734B marginal checking supply. Your nearest DEC sales office can supply details.

SUBJECT INDEX

TYPE NUMBER INDEX

digital

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146 Main Street, Maynard, Massachusetts 01754
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