digital

Computer Special Systems

TWU45
MAGTAPE SYSTEM

SYSTEM MANUAL

ADDENDUM REQUIRED

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CHAPTER 1
SYSTEM AND PHYSICAL DESCRIPTION

1.1 GENERAL

This manual describes the TWU45 Magnetic Tape System manufactured by Digital Equipment Corporation. The basic items in the system are:

RH70 Massbus Controller(s)
TM02 Magnetic Tape Controller(s)
TU45 Tape Transport(s) (Figure 1-1)
Magtape Transport Adapter (MTA).

The TWU45 is employed with the PDP-11/70 Central Processor which can accommodate up to four RH70 Massbus Controllers.

1.1.1 Scope

This manual is designed to provide Digital Field Service and customer maintenance personnel with sufficient installation, operation, and servicing information to install and maintain a TWU45 Magtape System.

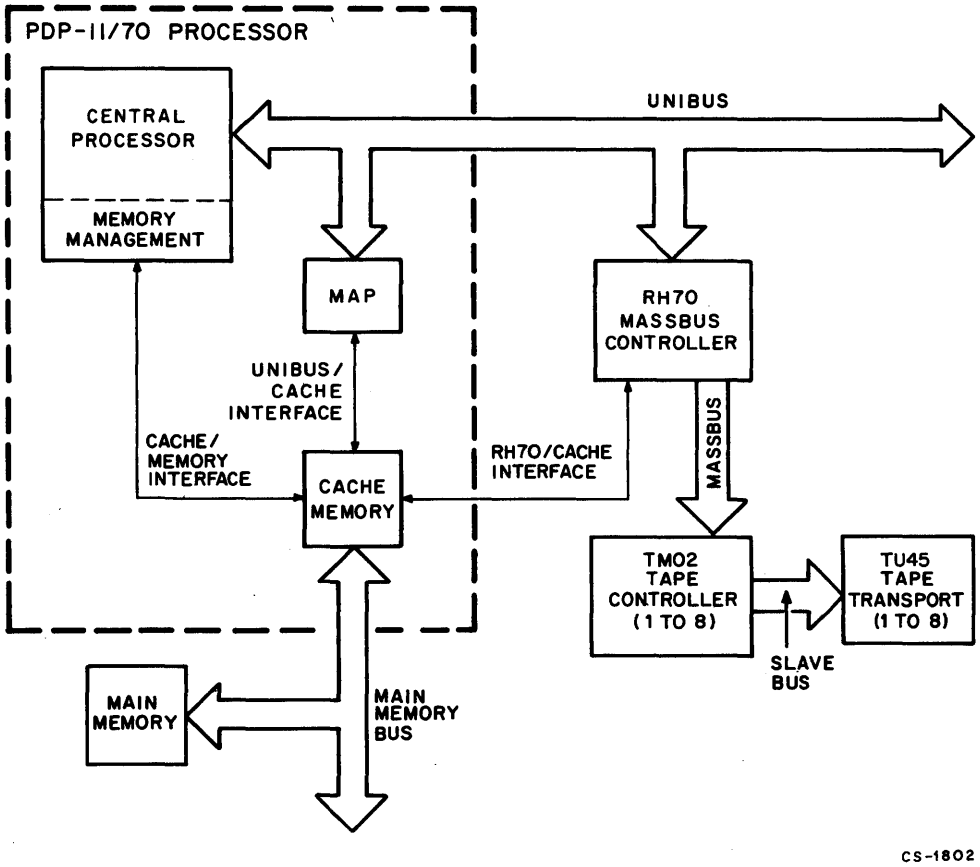


Figure 1-1 TWU45 Simplified System Diagram

1.1.2 Related Documentation

Table 1-1 lists related documentation that supplements the information in this manual.

1.2 BUS INTERFACES

This paragraph briefly describes the following interfaces which are incorporated into the system.

Unibus – provides interface between PDP-11/70 Central Processor and RH70 Massbus Controller.

Massbus – provides interface between RH70 Massbus Controller and TM02 Tape Controller.

Slave Bus – provides interface between TM02 Tape Controller and TU45 Tape Transports.

RH70/Cache Interface – provides interface between RH70 Massbus Controller and Cache memory.

Main Memory Bus – provides interface between cache memory and main memory.

Unibus/Cache Interface – provides interface between Unibus Map and Cache memory.

CPU/Cache Interface – provides interface between PDP-11/70 Central Processor and Cache memory.

1.2.1 Unibus

The Unibus provides the interface between the PDP-11/70 Processor, Cache, the RH70 Massbus Controller and general-purpose peripherals. Unibus devices contain the highest priority for main memory accesses. Since a dedicated separate data path is available for memory and high-speed peripherals, the Unibus is not overloaded, resulting in less contention at the Unibus. Peripheral devices are connected to the Unibus access main memory via the Cache.

1.2.2 Massbus

The Massbus provides a parallel data path between the RH70 and the TM02 Tape Controller; it has a maximum cable length of 120 ft, allowing 15 ft between TM02 Controllers if the "daisy-chain" configuration (with a maximum of 8 controllers) is employed. The Massbus comprises two sections: an asynchronous control bus and a synchronous data bus for high-speed data transmission.

The asynchronous control bus:

1. Transmits commands and information from the controller to the drive to read or write drive registers.
2. Notifies the controller when an unusual (attention) condition exists in one or more drives.
3. Transmits status information from the drive to the controller
4. Provides a master reset to all drives from the controller.

The synchronous data bus transmits blocks of data at high speed between the RH70 Controller and the TM02 Controller and controls the initiation and termination of block transmissions. Because the data and control buses operate independently, the Massbus Controller can monitor drive status on the control bus while a data transfer operation on the data bus is being performed. Additional details on the Massbus can be found in Chapter 2 of the RH70 manual.

Table 1-1
Related Documentation

Title	Document Number
PDP-11 Peripherals Handbook	2002.20175.4526
TU45 Operating and Service Manual	(PERTEC #104597)
TM02-FE/FF Magtape System Manual	CSS-MO-F-5.2-22
PDP-11/70 Processor Handbook	EB-04588/750100
KB11-B Processor System (PDP-11/70 Manual)	19H161
PDP-11/70 Maintenance and Installation Manual	EX-11070-MM
Magtape Transport Adapter	CSS-MO-F-5.2-23
RH70/Special Massbus Controller	CSS-MO-F-5.2-27
861-A,B,C Power Controller Maintenance Manual	DEC-00-H861A-A-D

1.2.3 Slave Bus

All TU45s controlled by a TM02 are "daisy-chained" on the Slave Bus (Figure 1-1). Essentially, this means that the TU45s are configured parallel to each other. The Slave Bus consists of slave select lines, write data lines, read data lines, transport control lines and various TU45 status lines. The various signals on the Slave Bus are tabulated in the TU45/TM02 *Tape Drive System Maintenance Manual.*

1.2.4 RH70 to Cache Interface

The RH70-to-Cache Interface is an integral interface with an open-collector bus to which each RH70 connects. This interface routes 22 bits of address, 36 bits of data (32 data bits, plus 4 parity bits), and three control signals (C0, C1 and CX) to or from Cache. C0 specifies a Data Out Byte (DATOB) or Data In Pause (DATIP); however, the RH70 does not implement these operations and this bit is always unasserted, (see chart below).

C1	C0	CX	
0	0	0	*DATI always double words
0	1	0	DATIP
1	0	0	*DATO single word
1	0	1	*DATO double word
1	1	0	DATOB

C1 specifies a DATI (read from memory) or a DATO (write into memory) transfer; and CX specifies a double-word transfer, if asserted, or a single-word transfer, if negated.

For transfers between the RH70 and memory, the Cache merely serves as an interface and is not updated as in Unibus/memory transfers or CPU/memory transfers. If the memory location being modified during a read (drive to RH70) is also in Cache, the data in Cache is invalidated. As a result, the CPU and Unibus memory cycles must access main memory to obtain correct data.

The RH70 initiates a data transfer by issuing a request to Cache. Cache arbitrates the request along with requests from other RH70 Controllers, the Map box, or the CPU. It then sends back an acknowledge signal to the device of highest priority. If an RH70 is selected for the next memory cycle, the Cache asserts signals which gate that controller's bus address, bus address extension (memory address), and control information (C0, C1, and CX) onto the RH70 to Cache Interface. Additional select signals allow the specified controller to gate data onto the interface (read) or to clock data off the interface (write or write-check).

* RH70 functions – DATIP and DATOB operations are not implemented by the RH70.

1.2.5 Main Memory Bus

The Main Memory Bus is a bus structure which originates at the Cache and daisy-chains through all the control modules of the memory. Physically, it consists of 4 cables containing 22 bits of address, 1 bit of address and control parity, 36 bits of data (32 bits of data, plus 4 parity bits), four byte mask signals, which determine the byte(s) to be written on write cycles, and various handshake signals associated with controlling the interface sequence.

1.2.6 Unibus to Cache Interface

During Unibus memory cycles, the Unibus-to-Cache interface controls the mapping of 18-bit Unibus addresses to the 22-bit address field of the Main Memory Bus. The interface contains 22 address bits, a 16-bit wide data path, a Request signal that requests use of the Cache, a parity error signal, and two control signals (C0, C1) to determine the direction of data transfer. The interface is integral with the 11/70 and contains no external bus structure.

1.2.6.1 CPU to Cache Interface – The CPU to Cache Interface is an integral interface (with no external buses) between the 11/70 processor and Cache memory. It contains a 22-bit wide address, 16-bit wide data path and associated error signals such as parity abort. The CPU/Cache Interface also contains C0 and C1 control signals which specify the type and direction of data transfer between Cache and the 11/70.

The Memory Management and Relocation unit in the processor converts the 16-bit virtual address from the processor into the 22-bit address which specifies a location in main memory.

1.3 PDP-11/70 CENTRAL PROCESSOR SYSTEM

The PDP-11/70 Central Processor System consists of the following components.

PDP-11/70 Central Processor
Cache Memory, Main Memory
Unibus Map
RH70 Massbus Controller
TM02 Tape Controller and TU45 Tape Transport

Each component is briefly described below.

1.3.1 PDP-11 Central Processor

The 11/70 Central Processor is an advanced processor of the PDP-11 family, available with an optional floating point unit. Several additional features are contained in this processor. The large memory capacity allows up to 2 million words of core memory. The entire 2 million words of core memory is made to appear as fast memory to the 11/70. This is accomplished via a fast 1K or 1024-word Cache memory. Core memory cycle time is approximately 1 μs and the Cache memory cycle time is approximately 300 ns. Statistically, it has been determined that 80 to 95 percent of the words referenced by the 11/70 may be in Cache, which creates an effective memory time of less than 450 ns.

1.3.2 Cache Memory, Main Memory

The 11/70 Central Processor contains a 1024-word bipolar memory system, designated Cache Memory. The Cache Memory system simulates a system having a large amount of moderately fast memory by relying on a small amount of very fast bipolar memory, a large amount of slow core memory and the statistical behavior of operating programs. The concept is to have most of the data that the processor needs in the fast Cache Memory, to allow the program to operate quickly, while having to slow down only occasionally for slow core memory cycles. This is accomplished by constantly updating the data in Cache to provide a high probability that the data most likely needed by the processor will be in fast memory.

The primary functions of the Cache Memory are to:

1. Act as a high speed buffer and interface between memory and the requesting device (e.g. CPU, Unibus or Massbus Controls).
2. Process parity and perform error detection to maintain system integrity.
3. Arbitrate cycles to determine which device will have access to memory. The Unibus Map box has the highest priority, followed by the RH70 I/O Controllers (Controller A, B, C and D, in that order) with the CPU having the lowest priority.

When the Cache is interfacing between the CPU and memory or between the Unibus Map and memory, it is continually being updated by the current data with which the CPU or Unibus Map is working. During a CPU-to-memory or Unibus-to-memory transfer, if a word to be written into memory is also in Cache, the word in Cache is updated and at the same time is transferred to main memory. If the word to be written into memory is not in Cache, the CPU-to-memory or Map-to-memory cycle occurs with no Cache update.

During a memory-to-CPU or memory-to-Unibus transfer, if a word to be read from main memory is also in Cache, the word in Cache is directly transferred to the CPU or Unibus Map and no slow memory cycle is performed. If the word to be read from memory is not in Cache, a slow memory cycle is performed and the two words of that block are sent to Cache. The word requested is then sent to the CPU or Unibus Map.

In the case of data transfers from the RH70 to memory or from memory to the RH70, the Cache merely serves as an interface and there is no updating of Cache.

1.3.3 Unibus Map

The Unibus Map is a standard hex board which allows Unibus devices in the 11/70 system to address up to 2 million words of core memory through the use of 31 read/write registers. These registers are each 22 bits long and require two Unibus register addresses. A block of 62 Unibus addresses is consequently reserved for the Unibus Map–31 registers with two addresses per register.

Bits 13 – 17 of the Unibus address dynamically select one of 31 mapping registers during Unibus memory cycles.

NOTE

A 32nd Map register is dynamically selected when Unibus address bits 13 - 17 are all 1s. In the PDP-11 architecture, this address field is defined as I/O register space; therefore, the 32nd register is not used to map address to memory.

When an Initialize is received or when power is first turned on, the system is set for one-to-one mapping, which means that a specific Unibus address specifies the corresponding main memory address with no relocation. In other words, Unibus address 5000 specifies main memory location 5000. This process is valid up to 124K of memory. Beyond that point, memory relocation (mapping) is required. In order to implement this, the programmer loads the Map registers and sets a bit in a Control register, located in the processor Memory Management Unit. When the Unibus address selects a particular mapping register via bits 13 - 17, bits 0 - 21 of the Unibus address are added to bits 1 - 21 of the mapping register. The sum of these bits results in a relocated address in core memory. Consequently, this mapping scheme allows any of core memory to be accessed.

1.3.4 RH70 Massbus Controller

The RH70 Controller, in conjunction with the TM02/TU45, provides an extremely fast and reliable mass storage system that can be employed in timesharing or real-time data storage applications. The following major functions are performed by the RH70:

1. Communicates with the main memory via Cache in order to fetch and store data.

2. Communicates with the central processor via the Unibus in order to receive commands, provide error and status information, and generate interrupts.

3. Interfaces with from one to eight drives via the Massbus.

The RH70 can accommodate up to eight TM02 Tape Controllers. Each TM02 Tape Controller, in turn, can accommodate up to eight TU45 Tape Transports.

1.3.5 TU45/TM02 Tape System

The TU45/TM02 is a Massbus-compatible, versatile tape drive system, consisting of a TM02 Tape Controller and TU45 Tape Transport(s). The TU45/TM02 records and reads digital data in industry-standard PE or NRZI mode at a maximum data transfer rate of 120,000 tape characters per second. Tape density and tape character format are program-selectable. Forward/reverse tape speed is 75 in/sec, while rewind is performed at 250 in/sec. The TU45/TM02 Tape Drive System also has forward and reverse read/space capability.

The TU45/TM02 Tape System performs the following functions:

1. Records and plays back data.

2. Generates tape marks to separate files.

3. Provides clock signals to synchronize data transmission between drive and controllers.

4. Maintains error and status indicators and generates an Attention signal when exceptional conditions occur.

5. Locates data records by the spacing function.

6. Provides mechanisms for convenience and diagnostic testing.

7. Performs error detection on the data and provides error correction in PE (Phase-Encoded) mode only.

The major assemblies of the TU45/TM02 Tape System include the TU45 Tape Transport, the TM02 Tape Controller, the H740DA Power Supply for the TM02, the 861 Power Controller, which controls power in the TU45/TM02 cabinet, the Magtape Transport Adapter Module (M8921), and the H716 Power Supply for the MTA Module.

1.4 RH70 FUNCTIONAL OPERATION

The RH70 is divided into two major functional groups: the register access control path, and the DMA (Direct Memory Access) data path (Figure 1-2). The register access control path allows the program to read from or write into any register contained in the RH70 or in the selected tape drive.

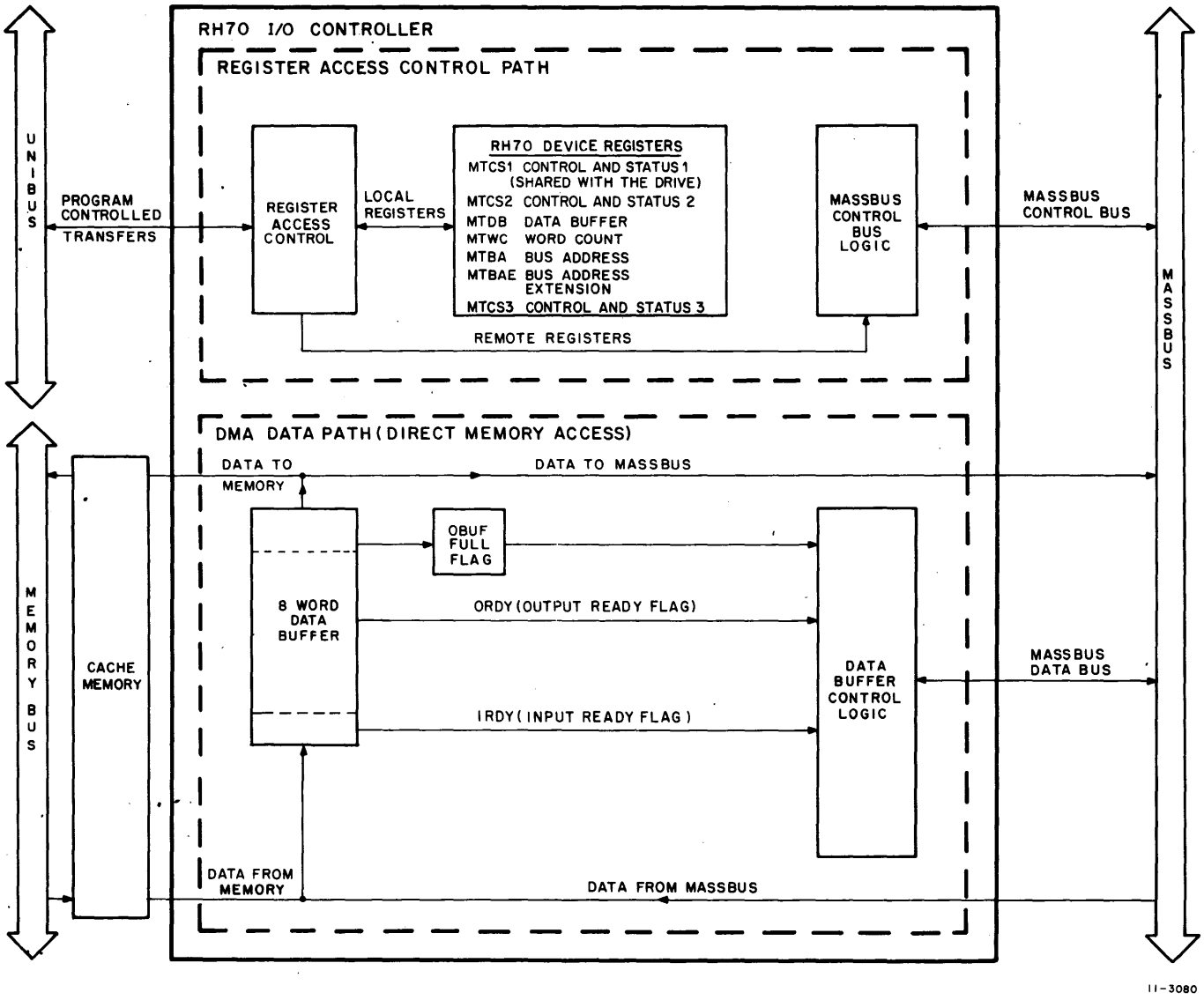


Figure 1-2 RH70 Simplified Data Path Diagram

There are a total of six registers in the RH70, nine registers in each TM02, and one shared register which is contained partially in the RH70 and partially in the selected TM02.

The DMA data path functionally consists of an 8 word × 16 bit first-in, first-out memory and associated control logic. The major function of this memory is to buffer data in order to compensate for fluctuations in cycle arbitration time of the Cache.

1.4.1 Register Access Control Path

When a PDP-11 instruction addresses the RH70 to read or write any device register in the RH70 or in the drive, a Unibus cycle is initiated and this data is routed to or from the RH70. (Refer to Chapter 2 for a detailed description of the registers.) If the register to be addressed is local (contained within the RH70), the register control logic immediately gates the data to or from the appropriate register.

If the register to be accessed is remote (contained in the TM02 Controllers), the register access control logic initiates a Massbus control bus cycle. TM02 registers are loaded in the following manner:

1. The controller places the drive select code of the desired TM02 on the Drive Select lines.
2. The controller places a register select code on the Register Select lines.
3. The controller asserts CTOD (Controller-to-Drive).
4. The controller places data on the Control lines.
5. The controller then asserts DEM.

The selected TM02 responds to DEM and CTOD asserted by loading the selected register with the data on the Control lines; then it asserts TRA. The controller responds by negating DEM, which causes the TM02 to negate TRA; the write operation is thereby terminated.

A TM02 register is read in a similar manner except that CTOD is negated (step 3) and step 4 is eliminated. The selected TM02 responds to DEM asserted and CTOD negated by gating out the contents of the selected register onto the Control lines. The TM02 then asserts TRA to the controller.

When the RH70 receives TRA, it gates the Control lines onto the Unibus. After a deskew delay, the RH70 asserts SSYN to the processor. When the processor receives the control data and SSYN, it clears MSYN, which in turn negates SSYN and DEMAND. The negation of DEMAND negates TRA and completes the operation.

Accesses to a TM02 register via the control bus portion of the Massbus do not interfere with data transfer operations occurring over the data bus portion of the Massbus.

1.4.2 DMA Data Path

The DMA data path is used for the actual transfer of blocks of data and functionally consists of the synchronous (data) portion of the Massbus, a data buffer, and the memory bus. The data buffer compensates for cycle arbitration time of the Cache by buffering data between the RH70 to Cache Interface and the Massbus data bus during data transfers.

1.4.3 Data Transfer Rates

The data transfer rate from the drive is determined by a clock in the drive. The basic data transfer rates for the TWU45 are approximately 16.8 μs/word in PE mode and 33.6 μs/word in NRZI mode. The memory transfer rate depends on cycle arbitration time in the Cache and memory cycle time. Figure 1-3 shows the data transfer sequence for a read operation; Figure 1-4 shows the sequence for a write operation. For lengthy data transfers, the average memory transfer rate is half the average disk data transfer since double words are transferred. Statistical fluctuations in cycle arbitration times are absorbed by the buffering in the data buffer.

1.5 MAGNETIC TAPE FUNDAMENTALS

Referenced Edge – The edge of the tape as defined by Figure 1-5. For tape loaded on a TU16, the reference edge is toward the observer.

BOT (Beginning of Tape) Marker – A reflective strip placed on the non-oxide side of the tape, against the reference edge, 15 ft (±1 ft) from the beginning of the tape.

EOT (End of Tape) Marker – A reflective strip placed on the non-oxide side of the tape, against the non-reference edge, 25 to 30 ft from the trailing edge of the tape.

Nine-Channel Recording – Eight tracks of data plus one track of vertical parity. Figure 1-6 shows the relationship between track and bit weight for a nine-channel transport.

Tape Character – A bit recorded in each of the nine channels.

Record – A series of consecutive tape characters.

File – An undefined number of records (minimum = zero, no maximum).

Interrecord Gap (IRG) – A length of erased tape used to separate records (0.5 in. minimum for nine-track; maximum IRG is 25 ft).

Extended IRG – A length of erased tape (3 in. minimum) optionally used to separate records. It must be used between BOT and the first record.

Tape Speed – The speed at which tape moves past the read/write heads; normally stated in inches per second.

Tape Density – The density of sequential characters on the tape. It is normally specified in bytes per inch (bpi), since 800 bpi means that there are 800 tape characters per inch of tape.

Write Enable Ring – A rubber ring which must be inserted on the supply reel to allow the transport to write on the particular tape. This safety feature helps to prevent accidental destruction of previously-recorded data.

Tape Mark (TM) – A record written on the tape to designate the end of a file; sometimes referred to as a File Mark (FMK). In the TU45/TM02, the TM is always preceded by an extended IRG.

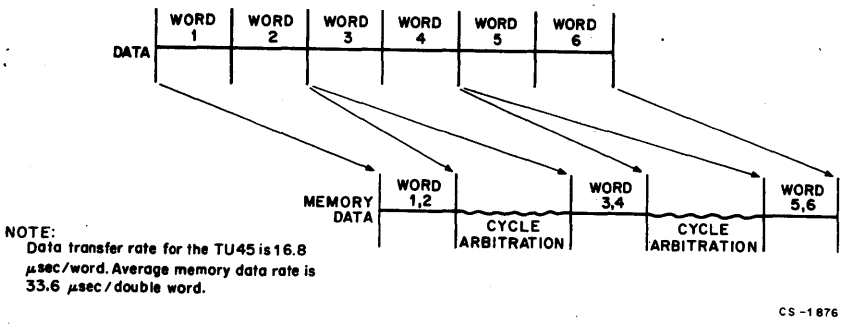


Figure 1-3 Read Data Transfer Sequence

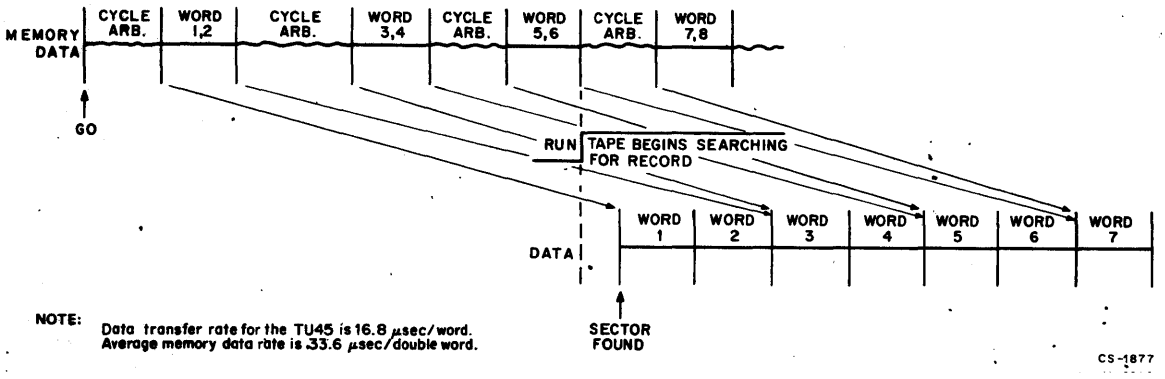


Figure 1-4 Write Data Transfer Sequence

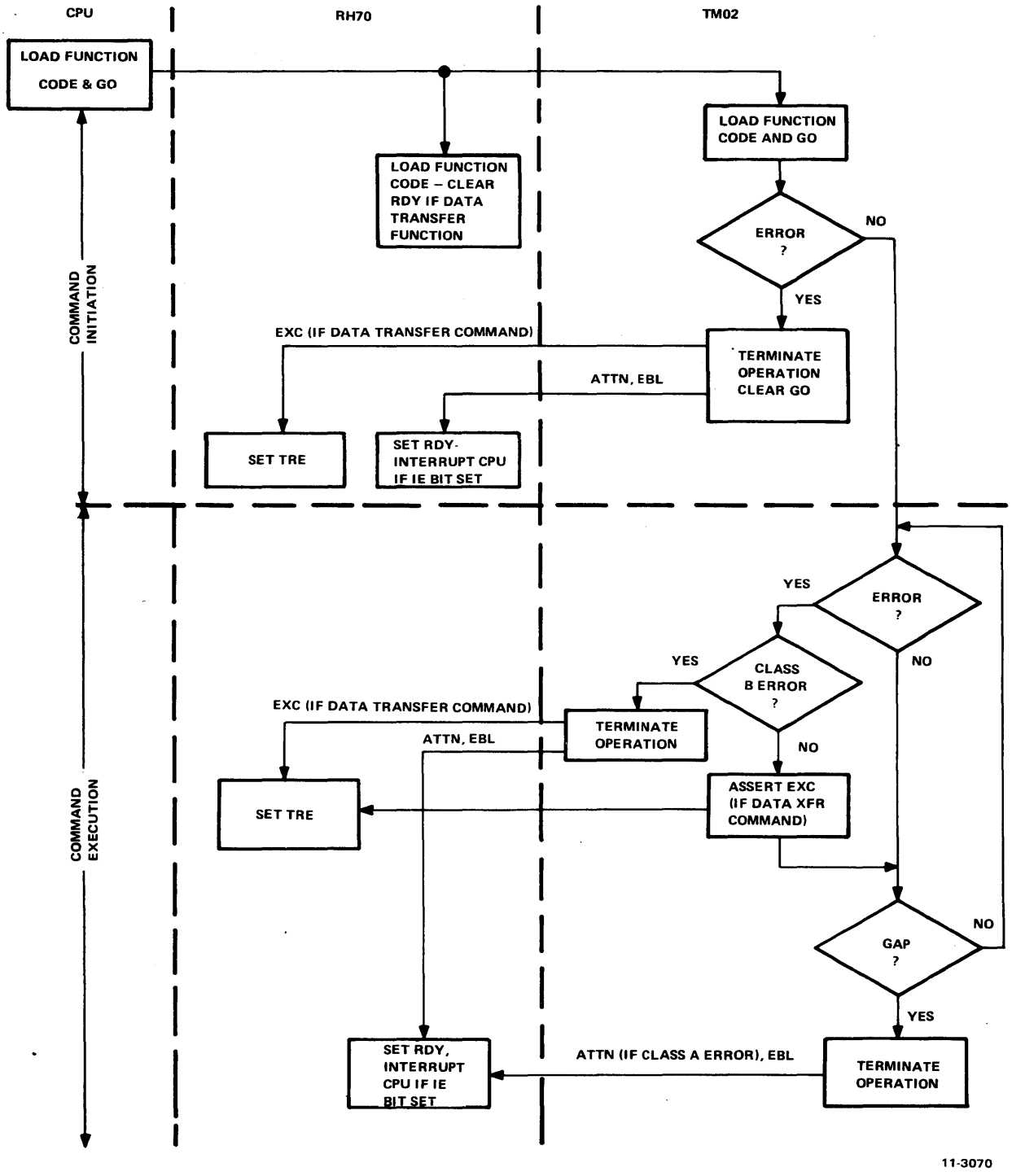


Figure 1-5 RH70 Error Termination

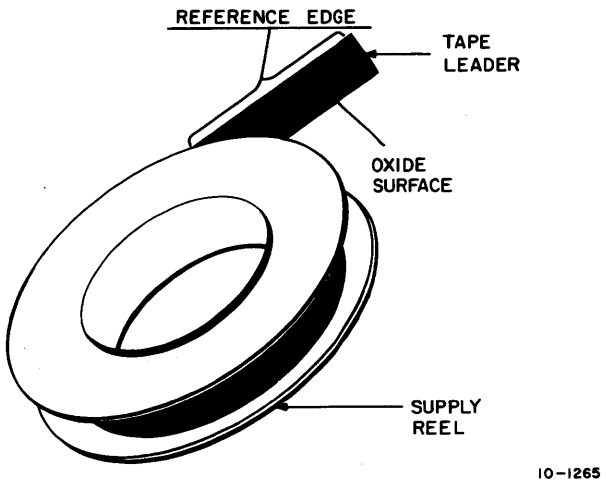


Figure 1-6 Reference Edge of Tape

1.6 TU45/TM02 RECORDING TECHNIQUES

1.6.1 NRZI (Non-Return to Zero - Change on a 1)

1.6.1.1 Definition - NRZI is a recording technique which requires a change of state (flux change) to write a 1, and no change of state (no flux change) to write a 0.

1.6.1.2 Format - A record is a minimum of 12 characters. A CRCC character occurs four character spaces after the record. An LPCC character occurs four character spaces after the CRCC (Figure 1-7).

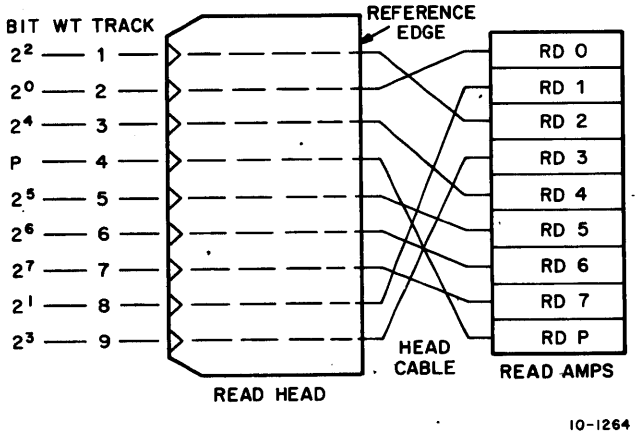


Figure 1-7 Track-Bit Weight Relationship for Nine-Channel Transport

Cyclic Redundancy Check Character (CRCC) - A check character that is written four character spaces after the last character of an NRZI record (nine-channel only). CRCC is derived by a complex mathematical formula applied to the characters written in the record. The result of this manipulation (CRCC) can be used to recover a lost bit in a record read from tape. CRCC error recovery hardware is not available in the TU45/TM02, but CRCC is written for purposes of compatibility.

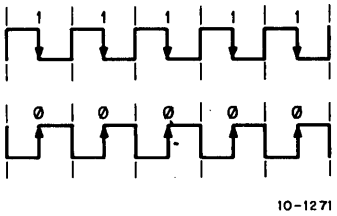
Longitudinal Parity Check Character (LPCC) - A check character written four character spaces after CRCC (nine-channel). LPCC consists of one bit of even parity for each track of data. For example, if track 1 had an odd number of 1s written in a record, then a 1 must be written in the LPCC bit associated with track 1.

Tape Mark – A nine-channel NRZI tape mark consists of one tape character (23_8), followed by seven blank spaces, and then LRCC (23_8). (CRCC is not written.) Figure 1-8 illustrates nine-channel NRZI tape format.

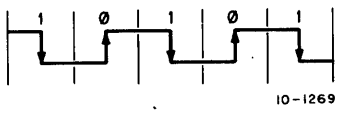
1.6.2 Phase Encoding (PE)

1.6.2.1 Definition - Phase encoding is a recording technique in which a flux reversal occurs for each bit of information written onto the tape. A 1 can be defined as a positive level followed by a negative transition; a 0 can be defined as a negative level, followed by a positive transition.

Sequential flux transitions on the tape are either at the data rate or at twice the data rate. Sequential 1s or sequential 0s will cause flux reversals to occur at twice the data rate:



Alternate 1s and 0s cause flux reversals to occur at the data rate:



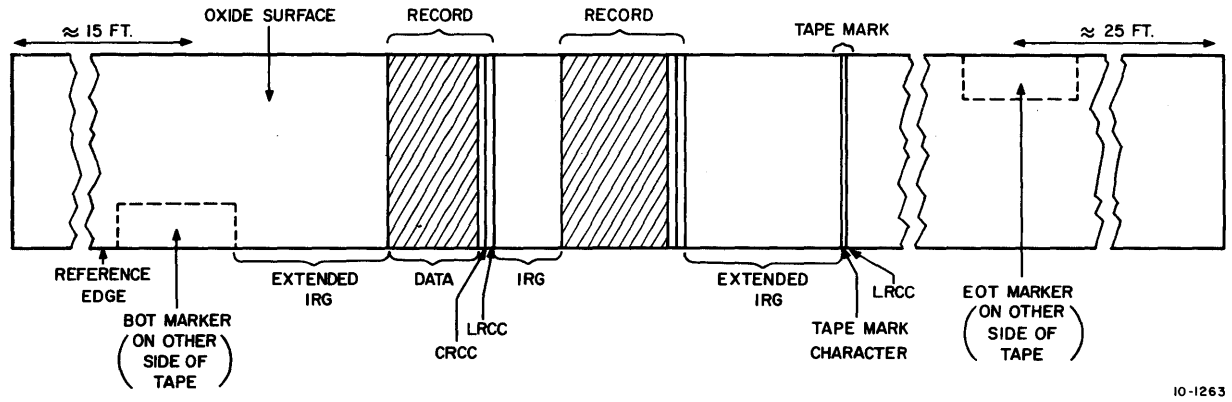


Figure 1-8 NRZI Format (Nine-Channel)

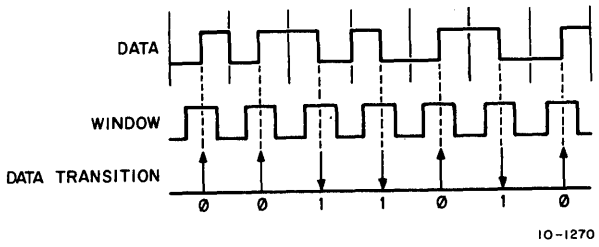
1.6.2.2 Format – To ensure proper extraction of PE data from the serial stream of transitions coming off the tape, PE data must be recorded in a precise format. A PE record consists of preamble, data, and postamble.

Preamble – Forty characters of 0s in all nine tracks, followed by a character of 1s in all nine tracks.

Data – The data consists of flux reversals for each bit of information. Negative flux reversals designate 1s; positive flux reversals designate 0s.

Postamble – One character of 1s in all nine tracks, followed by 40 characters of 0s in all nine tracks.

The PE read electronics uses a data window to isolate data transitions. For example,



Zeros in the preamble are used to set the window in position when reading in a *forward* direction; 0s in the postamble perform this function when reading in the *reverse* direction. The all-1s character in the preamble and postamble is used to mark the beginning of data.

Tape Mark – A PE tape mark consists of forty 0s in tracks 2, 5, and 8 (bit positions 0, 5, and 1) with tracks 3, 6, and 9 (bit positions 4, 6, and 3) erased.

Identification Burst (IDB) – The IDB identifies the tape as a PE tape. It consists of alternating 1s and 0s in the parity track (track 4) with all other tracks erased. The IDB is located at BOT and has a minimum length of 1.7 in. Figure 1-9 illustrates PE tape format.

1.7 TAPE HANDLING

WARRANTY

Removable media involve use, handling, and maintenance which are beyond DEC's direct control. DEC disclaims responsibility for performance of the equipment when operated with media not meeting DEC specifications or with media not maintained in accordance with procedures approved by DEC. DEC shall not be liable for damages to the equipment or to media resulting from such operation.

The operator should observe the following precautions when handling magnetic tape:

1. Always handle a tape reel by the hub hole; squeezing the reel flanges can cause damage to the tape edges when winding or unwinding tape.

2. Never touch the portion of tape between the BOT and EOT markers. Oil from fingers attracts dust and dirt. Do not allow a tape to drag on the floor.

3. Never use a contaminated reel of tape; this spreads dirt to clean tape reels and can affect tape transport operation.

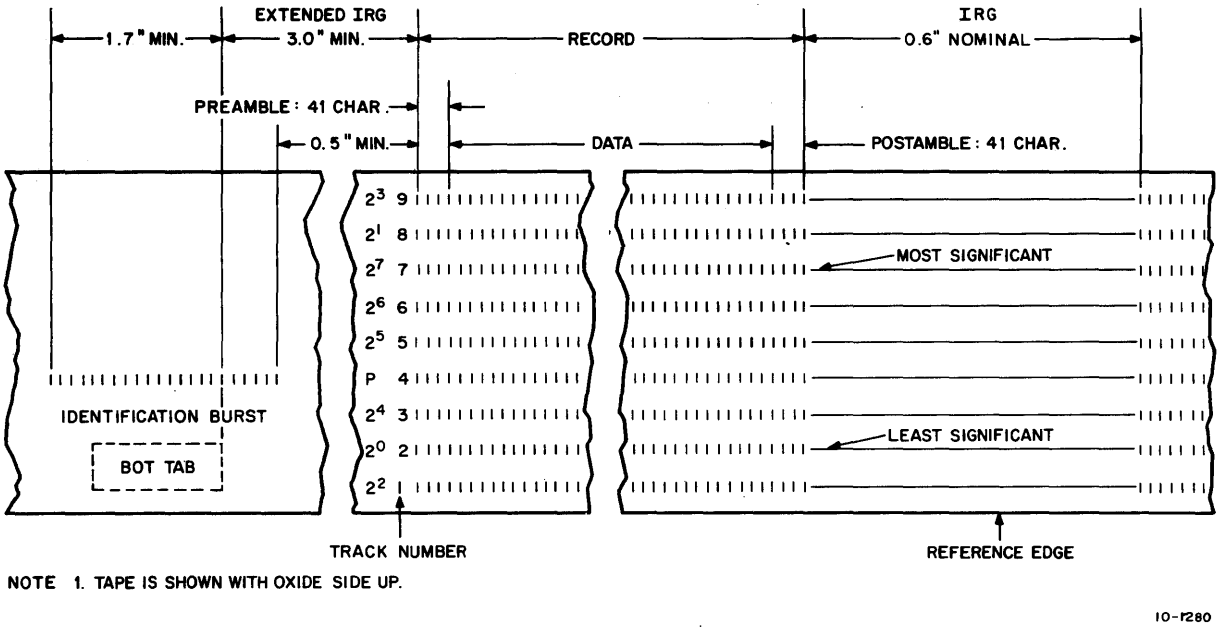


Figure 1-9 PE Recording Format

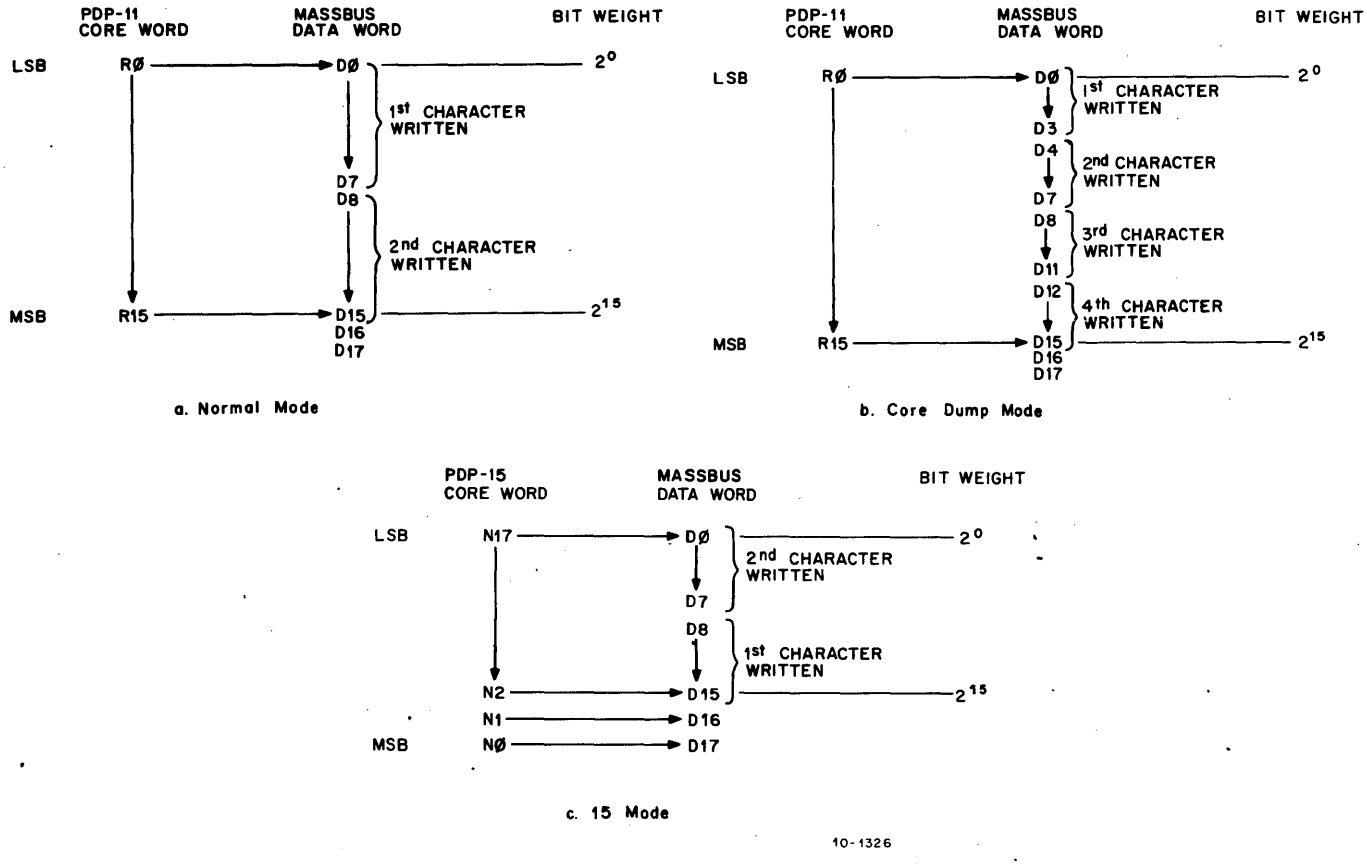


Figure 1-10 Data Formats

4. Always store tape reels inside their respective containers. Keep empty containers closed so dust and dirt cannot get inside.

5. Inspect tapes, reels, and containers for dust and dirt. Replace damaged take-up reels.

6. Do not smoke near the transport or tape storage area. Tobacco smoke and ash are especially damaging to tape.

7. Do not place the TU45 Tape Transport near a line printer or other device that produces paper dust.

8. Clean the tape path (see TU45 Manual).

1.8 TWU45 SPECIFICATIONS

This paragraph defines the parameters in the TWU45 Magnetic Tape Subsystem.

1.8.1 Data Format

Data Format is selected by the format select bits (FMT 0–3) in the tape control register as follows:

FMT (0 – 3)

Bit				Mode
3	2	1	0	
1	1	0	0	Normal Mode
1	1	0	1	Core Dump
1	1	1	0	15 Mode

Figure 1-10 shows the three modes in the TWU45 system: normal mode, core dump mode and 15 mode. In 15 mode, bit 15 in memory corresponds to Massbus data bit D0; bit 0 in memory corresponds to Massbus data bit D17.

1.8.2 TU45/TM02 Specifications

Packing Density
800 and 1600 bpi; program-selectable.

Tape Speed
Forward/Reverse: 75 in/sec

Rewind: 250 in/sec

Maximum Transfer Rate
120,000 characters/sec

Tape Motion Times
Start: Normal operating speed is reached within 5 ms after initiation of forward or reverse command.

Stop: Motion stops in less than 5 ms after removal of forward or reverse command.

Electrical Skew
Write deskew only. Read skew mechanically aligned.

Recording Method
NRZI or PE recording; industry-compatible.

Transport Mechanism
Single capstan; vacuum columns

Read/Write Heads
Dual gap, read after write.

BOT, EOT Detection
Photoelectric sensing of reflective strip

Interrecord Gap
0.5 in. minimum, 0.65 in. nominal

Tape
Width: 0.5 in.
Thickness: 1.5 mil

Take-up Reel
Diameter: 10-1/2 in. (For 1600 bpi mode, the tape should be certified at 3200 flux changes per inch).

Capacity: 2400 ft

Power Control
861 Power Controller

Voltage Requirement
TU45: 115/230 Vac + 10% at 50/60 Hz + 2%

TM02: 90–135 Vac; 180–270 Vac at 47–63 Hz

Power Dissipation
TU45: 900 W max
TM02: 300 W max

TU45 Transport (without cabinet)
Depth: 16 in. (0.41 m)
Width: 19 in. (0.48 m)
Height: 24 in. (0.61 m)
Weight: 155 lb (70.3 kg)

TM02 Tape Controller
Depth: 23 in. (0.58 m)
Width: 19 in. (0.48 m)
Height: 7 in. (0.17 m)
Weight: 45 lb. (21 kg)

TM02 Power Supply (H740D)
Depth: 8 in. (0.18 m)
Width: 19 in. (0.48 m)
Height: 5 in. (0.13 m)
Weight: 24 lb. (11.2 kg)

861 Power Controller
Depth: 8 in. (0.20 m)
Width: 19 in. (0.48 m)
Height: 5 in. (0.13 m)
Weight: 10 lb (4.54 kg)

MTA Power Supply (H716-B or -D)
Depth: 12.00 in. (0.305 m)
Width: 5.25 in. (0.133 m)
Height: 4.13 in. (0.105 m)
Weight: 7 lb (3.18 kg)

Environmental Limits
Temperature*: 60° to 95° F (15° to 35° C)
Relative Humidity: 30% to 80% (no condensation)

1.8.3 RH70 Massbus Controller Specifications

Mechanical

RH70 Logic
3 quad-height modules
1 hex-height module
3 double-height modules
CPU Backplane
4 module slots

Power Requirements (RH70)
+5.0±.25 Vdc at 8.5 A max
-15±1.5 Vdc at 0.5 A max

Logic Voltage
High=3.0 V; Low=0 V

* Magnetic tape operation is more reliable if the temperature is limited to 65° to 75° F (18° to 24° C) and the relative humidity to 40% to 60%.

Environmental

Temperature
32° - 122° F (0° - 50° C) Class C

Relative Humidity
8% to 90%, no condensation

Vibration Shock
1.89 g rms, 10–300 Hz
20 g, half sine, 30 ms duration, any plane

Data Transfers Memory/Controller
Data is normally transferred as double data words (32 data bits, plus 4 parity bits) via the RH70/Cache Interface, and then to or/from memory via the memory bus.

1.9 TU45/TM02 POWER SYSTEM

Power to the TU45/TM02 cabinet is controlled by an 861 Power Controller, which is in turn controlled, via a remote cable, by a power controller in an adjacent cabinet. The power controllers in each cabinet are interconnected by remote cables. A ground (which originates at the processor POWER Key switch), transmitted via the remote cables, activates the interconnected controllers, and causes them to apply ac power to the power controller's switched outlets. Refer to the *861-A, B, C Power Controller Maintenance Manual* (DEC-00-H861A-A-D) for a complete description of the 861 Power Controller.

The TU45 power supply, MTA power supply (type H716), and the TM02 power supply (type H740D) plug into the switched outlets of the 861 Power Controller (Figure 1-11). The TU45 power supply supplies all power required by the TU45 Tape Transport, as well as 115 Vac to operate the cabinet fan. The TM02 power supply (H740DA) provides power (and power fail logic signals AC LO and DC LO) to the TM02 logic assembly. The H740DA is a H740D Power Supply that has been modified slightly to provide 115 Vac to the TM02 logic assembly cooling fan. The H740D ac harness (Figures 1-1 and 1-5 in the *H740D Power Supply Maintenance Manual*) has been tapped, and 115 Vac is brought out through the side of the power supply mounting box. (The H740D Power Supply is discussed in detail in the *H740D Power Supply Maintenance Manual* (DEC-11-H740A-A-D).) The MTA power supply (H716-B or H716-D) supplies all of the power required by the MTA board.

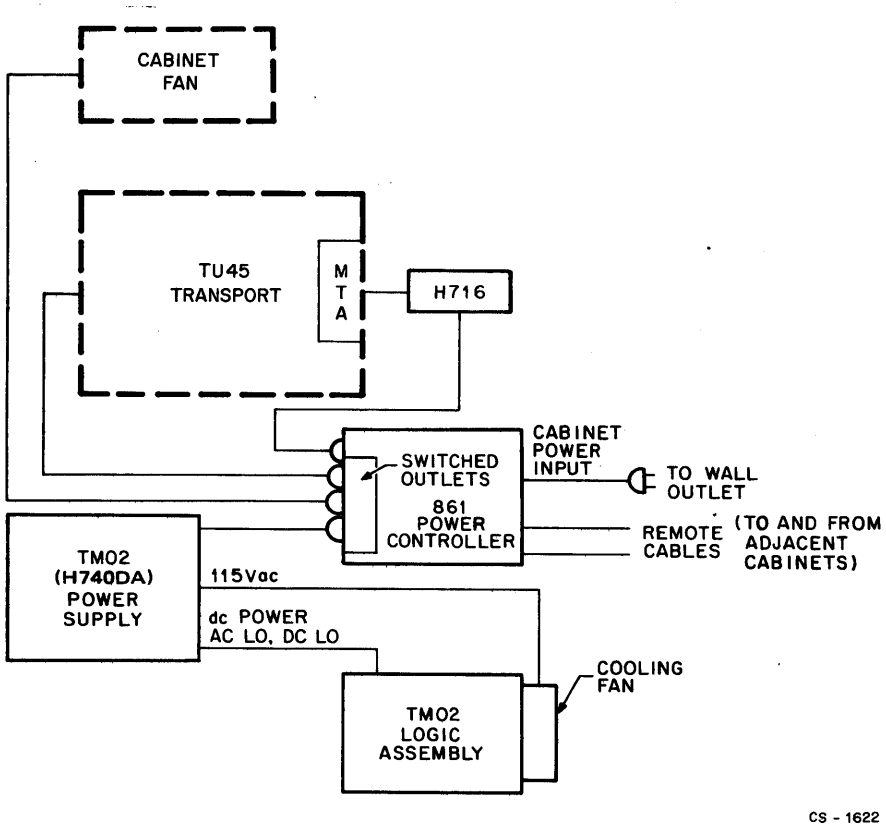


Figure 1-11 TU45/TM02 Power System

CHAPTER 2
INSTALLATION AND MAINTENANCE

2.1 INTRODUCTION

This chapter describes the necessary installation information required to install the RH70. The chapter also describes the preventive and corrective maintenance procedures that apply to the RH70 when connected to TM02/TU45 drive. A major point in the maintenance philosophy of this manual is that the user understand the normal operation of the RH70.

This knowledge, and the maintenance information contained in the *RH70 Massbus Controller Manual,* will assist maintenance personnel in isolating system malfunctions.

2.2 RH70 INSTALLATION

The following paragraphs describe the mechanical and electrical installation, power checks, and visual inspection of the RH70.

2.2.1 Mechanical

The RH70 uses one hex-height module, three quad-height modules and three double-height modules (Massbus connectors). *There is no mechanical unit to mount.* The modules are merely inserted into the appropriate slots in the 11/70 CPU box as shown in the Module Utilization chart in Figure 2-1. The Massbus Cables are plugged into the double-height slots and the jumpers are configured for the proper address and interrupt vector.

2.2.2 Electrical

The 11/70 CPU mounting box contains a wired backplane that runs the full depth of the box. The Unibus signals are prewired on the backplane. Power to the RH70 is provided by the cabinet power supply as follows:

+5 V @ 18.5 A max.
-15 V @ 0.5 A max.

2.2.3 Module Locations

The 11/70 CPU mounting box houses the Floating Point Unit, Central Processor, Memory Management, Unibus Map, Cache, 5 Small Peripheral Controller (SPC) slots, the KW11 clock, and up to four RH70 Controllers. The location of the respective modules is shown in Figure 2-1.

2.2.4 Massbus Cables

Connect the Massbus cables as described in Paragraph 2.4.

2.3 TM02 AND TU45 INSTALLATION

1. Unpack the TM02/TU45 cabinet and bolt it to the system cabinet.
2. Install the cabinet ground strap.
3. Set the 861 circuit breaker to the OFF position.
4. Set the 861 LOCAL/OFF/REMOTE switch to OFF.
5. Check the power receptacle to be used for the 861 for correct hot, neutral, and ground connections. Refer to the *861-A,B,C Power Controller Maintenance Manual,* DEC-00-H861A-A-D, for the plug and receptacle diagrams for the particular 861 being used.
6. Plug the 861 power cord to the power receptacle.
7. Set the 861 circuit breaker to the on position.
8. Set the 861 LOCAL/OFF/REMOTE switch to LOCAL.

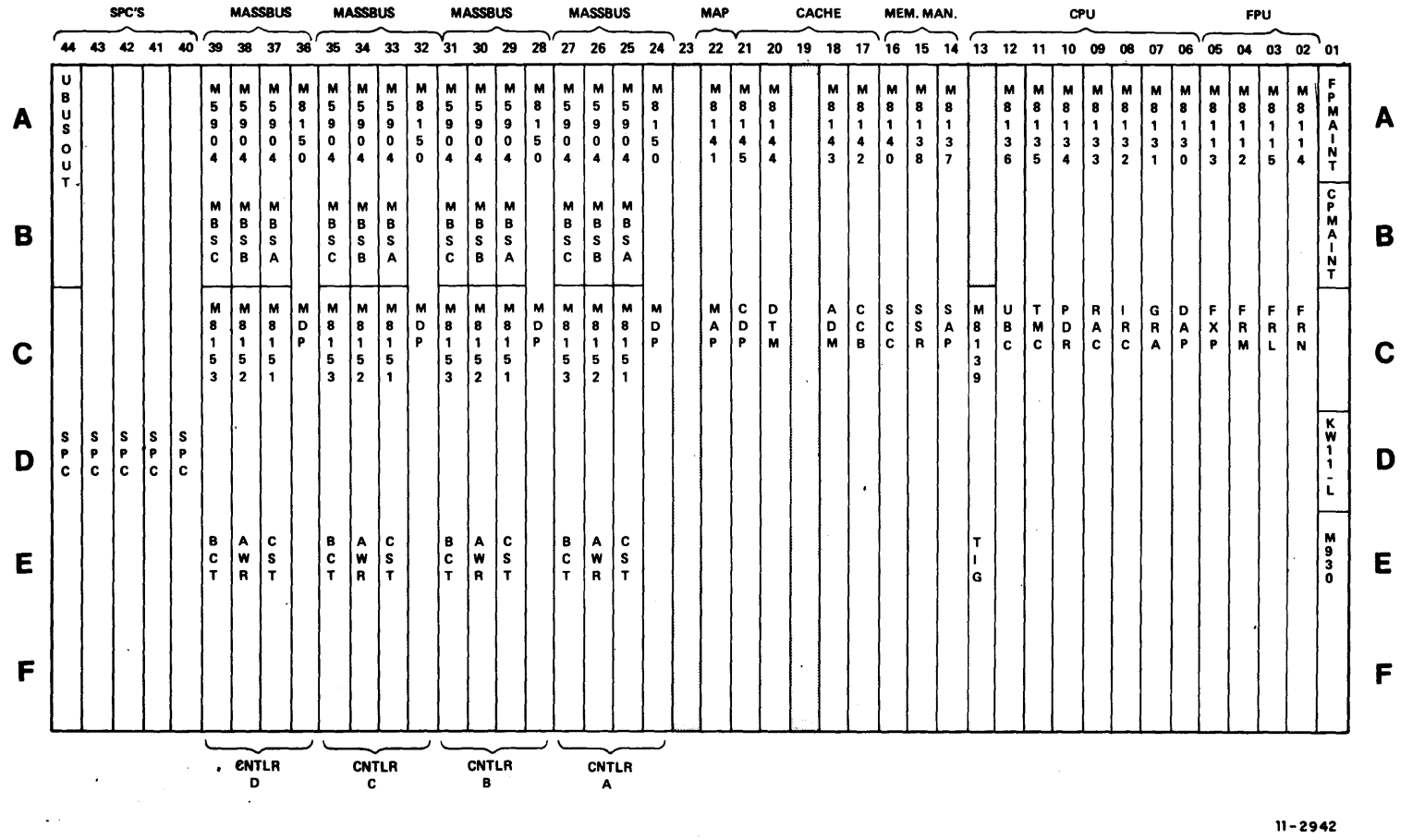


Figure 2-1 Module Utilization Chart

9. Verify the following:

   a. Cabinet fan operating.
   b. TM02 fan operating.
   c. TU45 PWR indicator lit.
   d. TM02 power LED (bottom LED) lit.
   e. MTA power LED (upper LED) lit.

10. Turn off power.

11. Connect the Massbus and slave bus as described in Paragraphs 2.4 and 2.5.

12. Apply system power. Verify that the TM02 power indicators are lit.

13. Attempt to examine locations 772440 through 772472 (standard addresses). If the processor traps, refer to Paragraph 2.7.1 for possible addressing jumper problems.

14. Attempt to deposit and examine all 1s in location 772446. If any bits are missing, check out the Massbus cabling (Paragraphs 2.4 and 2.6).

2.4 MASSBUS CABLES

Massbus connections between the TM02 and RH70 are made via three 40-conductor ribbon cables. These cables plug into three M5904 Transceivers in the RH70 and are designated Massbus Cable A, Massbus Cable B, and Massbus Cable C. The connections are made as shown in Figure 2-2.

The ribbed surface of the Massbus cables must face up at the RH70 output, and the smooth surface of the cables must face up at the input of the TM02. Refer to Paragraph 2.6 for cable identification markings.

CAUTION

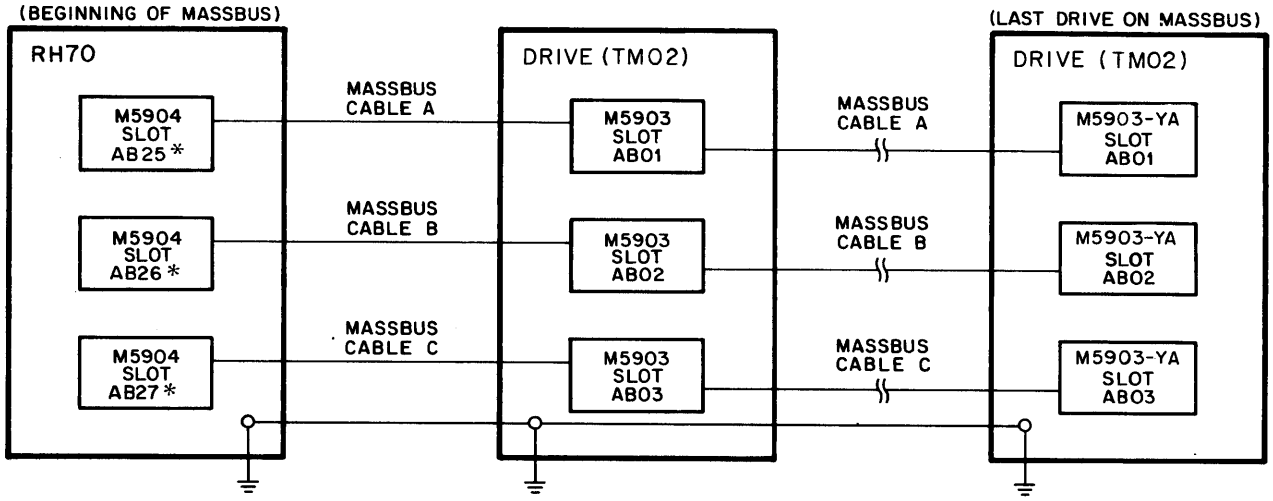
All Massbus cables must be installed with the red line toward the module handle. Otherwise, a signal line will be grounded.

If more than one TM02 is used:

1. All TM02s must have the smooth side of the BC06R Massubs cable up at the input of the TM02, and the ribbed side up at the output.

2. Mid-bus TM02s use M5903 modules.

3. The end-of-bus TM02 (as in the case of a single TM02) uses M5903YA modules.



*	CONTROLLER A	CONTROLLER B	CONTROLLER C	CONTROLLER D
MASSBUS CABLE A	AB 25	AB 29	AB 33	AB 37
MASSBUS CABLE B	AB 26	AB 30	AB 34	AB 38
MASSBUS CABLE C	AB 27	AB 31	AB 35	AB 39

CS-1878

Figure 2-2 Massbus Cable System Configuration

2.5 TM02/TU45 SLAVE BUS CABLE INSTALLATION

Slave Bus cable connections between the TM02 and the TU45 and between daisy-chained TU45s are shown in Figure 2-3. A half-twist in the slave bus cable is not required between the TM02 and the first (or single) TU45, but if multiple TU45s are installed, a half-twist of the slave bus cable must be used between the TU45s. Refer to Paragraph 2.6 for cable identification markings.

CAUTION

All slave bus cables must be installed with the red line toward the left side. Otherwise, the +5 V will be applied to a signal line instead of the shield where it belongs.

NOTE

The last TU45 (M8921) must contain six terminators (ICs DEC part no. 13-11003-01) in locations E16, E17, E38, E39, E62, and E63.

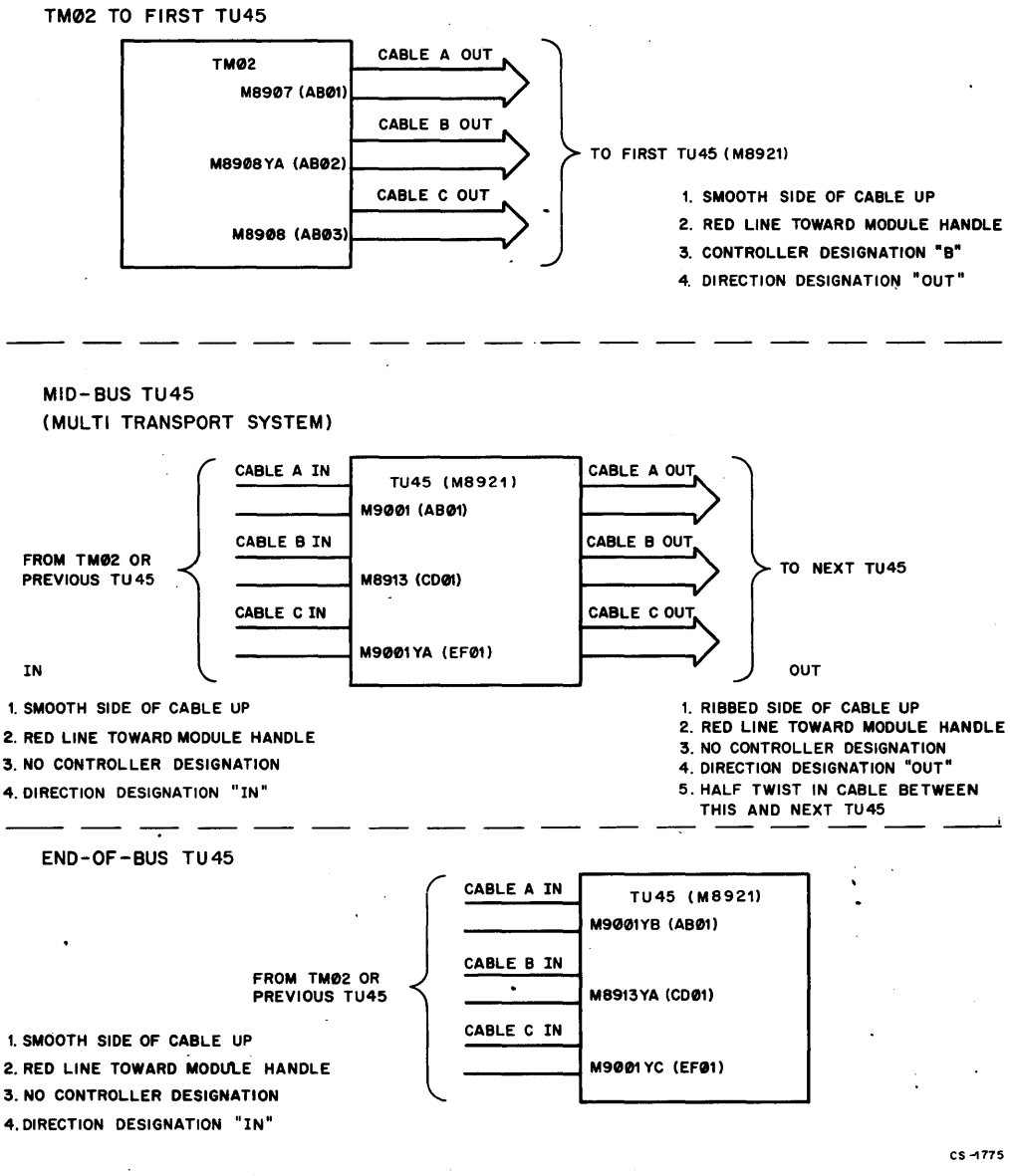


Figure 2-3 TM02/TU45 Slave Bus Cabling Diagram

2.6 MARKUP OF MASSBUS AND SLAVE BUS CABLES

Both surfaces of each end of the Massbus and slave bus cables are stamped as shown in Figure 2-4. The stamps are marked up to indicate cable designations at the time the cables are installed. Mark the BC06R Massbus cables as follows when installing them:

1. Cross out the designation THIS SIDE UP on the under side of the cable.

2. Cross out the CONTROLLER designation that does not apply. Cross out B when plugging into the RH70 and cross out A when plugging into the TM02.

3. Cross out the CONNECTOR MODULE designations that do not match the cable letter being used.

4. Cross out IN for the output cables and cross out OUT for the input cables.

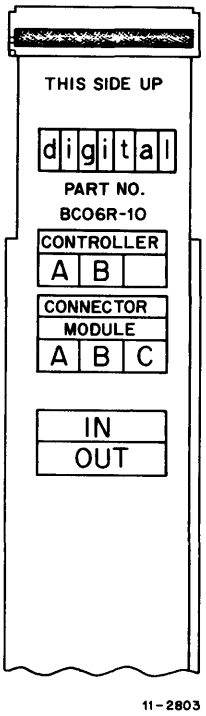


Figure 2-4 Massbus Cable Stamp

Figure 2-5 shows an example of a cable that is marked up to be plugged into the M5903YA module in slot A/B06 of an end-of-bus TM02.

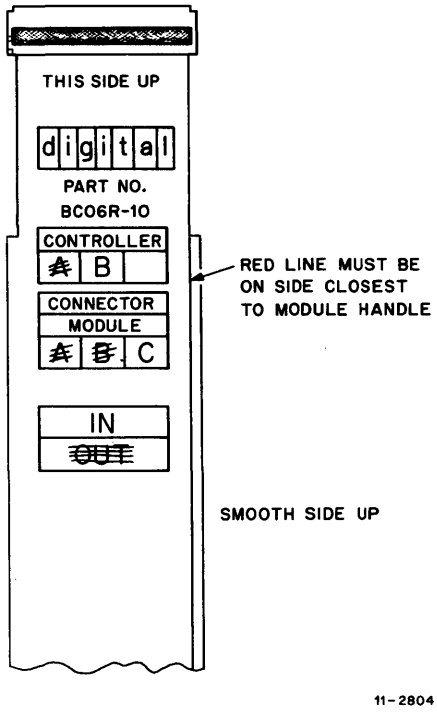


Figure 2-5 Marked-Up Massbus Cable

2.7 JUMPER CONFIGURATIONS

The following paragraphs describe the various jumper configurations on the BCT (M8153) module and on the MDP (M8150) modules.

2.7.1 BCT Module (M8153)

The BCT module contains jumpers for register selection, BR level interrupt and vector address.

Register Selection

The RH70 is capable of responding to 32 possible Unibus addresses. The number of addresses, however, is dependent on the Massbus device. Jumpers W8 – W15 select the block of Unibus addresses to which the TWU45 subsystem responds. The standard addressing block assigned is 772440 – 772476.

For the TWU45 subsystem, the following jumper configuration should be used (see D-CS-M8153-0-1, sheet 2 of 6).

Jumper In = Binary 0

Address Bit	Jumper	Jumper In/Jumper Out
12	W14	OUT
11	W10	IN
10	W9	OUT
9	W8	IN
8	W11	OUT
7	W13	IN
6	W15	IN
5	W12	OUT

ADDR.

BIT	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	1	1	1	1	1	1	0	1	0	1	0	0	1	X	X	X	X	X
	7			7			2			4			4 to 7			0 to 7		

The jumpers in E41 (D-CS-M8153-0-1, sheet 2 of 6) are selected for the appropriate number of registers in the subsystem, minus 2. For example, there are 16 registers in the TWU45 subsystem, so the jumpers are selected for a weighted value of 16 −2 or 14, as shown below. This procedure is described in detail in Paragraph 4.2 of the RH70 Manual.

Jumper In = Binary 0

Slot	Jumper	Jumper In/Jumper Out
E41	1-16	IN
	2-15	IN
	3-14	OUT
	4-13	OUT
	5-12 (2)	OUT
	6-11 (4)	OUT
	7-10 (8)	OUT
	8-9 (16)	IN

BR Level Interrupt

The priority jumper plug for the RH70 is normally set for the BR5 level. This plug is located in E022 (refer to D-CS-M8153-0-1, sheet 4 of 6).

Vector Address Jumpers

The interrupt vector transferred to the processor is jumper-selectable via jumpers W1 – W7, representing vectors bits 2 – 8. The TWU45 subsystem has been assigned a vector address of 000224. The jumper configuration for this vector address is shown below:

Jumper In = Binary 1

Vector Bits	Jumper	Jumper In/Jumper Out
V2	W7	IN
V3	W3	OUT
V4	W6	IN
V5	W2	OUT
V6	W5	OUT
V7	W1	IN
V8	W4	OUT

V8	V7	V6	V5	V4	V3	V2	V1	V0
0	1	0	0	1	0	1	0	0
2			2			4		

2.7.2 MDP Module (M8150)

The MDP module contains jumpers which allow maintenance personnel to disconnect wired-OR connections from the Exclusive-OR network used to detect write-check errors. These jumpers are designated W1 – W4 and are shown on D-CS-M8150-0-1, sheet 6 of 9. The jumpers provide maintenance personnel with a method of isolating a faulty output (stuck low) of the wired-OR bus to one of four integrated circuit (IC) chips which perform the Exclusive-OR function during write-check operations. For example, if the output of the E21 and E23 open-collector line is stuck low when scoping of the inputs indicates that it should be high, the faulty IC (E21 or E23) can be ascertained by removing jumpers W2 and W1. If after removing the jumpers, the outputs of the Exclusive-OR gates in E23 are still low, it indicates that the E23 chip is defective. If E23 outputs are high, the E21 chip is defective (outputs stuck low).

2.8 LIGHT-EMITTING DIODES (LEDs)

The following light-emitting diodes are incorporated in the RH70 Massbus Controller logic on the M8153 BCT module (Figure 2-3).

SSYN (Slave Sync) D-CS-M8153-0-1, Sheet 3 of 6

TRA (Transfer) D-CS-M8153-0-1, Sheet 3 of 6

BG IN (Bus Grant In) D-CS-M8153-0-1, Sheet 4 of 6

SACK (Selection Acknowledge) D-CS-M8153-0-1, Sheet 4 of 6

BBSY (Bus Busy) D-CS-M8153-0-1, Sheet 4 of 6

These LEDs are provided to aid maintenance personnel in isolating system faults as described below:

1. Unibus on PDP-11/70 is in "hung" condition (no operations can be performed on Unibus).

2.9 ACCEPTANCE PROCEDURE

2.9.1 General

Before testing the system the tape unit should be given a good cleaning (heads and other items the tape comes in contact with as described in the *TU45 Tape Transport Manual*). A good quality tape should be used to reduce the probability of errors due to flaws in the tape. The following diagnostic programs are used in the acceptance testing of the TU45 tape system and should be available along with the appropriate listings (printouts).

Basic Function Test	DECSPEC-11-AYVBD
TM02/TU45 Logic Test	DECSPEC-11-AYVCD
TM02/TU45 Drive Function Timer	DECSPEC-11-AYVDD
TU45 Data Reliability Program	DECSPEC-11-AYVAD

2.9.2 Acceptance Tests

The diagnostics should be run on the system in the order presented below. All of the programs start at location 200_8. For a detailed description of the diagnostic programs see the appropriate listings. The number of passes of each routine that are to be made and the number of errors that are acceptable are specified for each diagnostic program.

NOTE

Typical test typeouts are provided in Appendix A.

2.9.2.1 TM02/TU45 Logic Test (DECSPEC-11-AYVCD)

Acceptance Criteria:

a. Four passes per drive; no errors are allowed.

NOTE

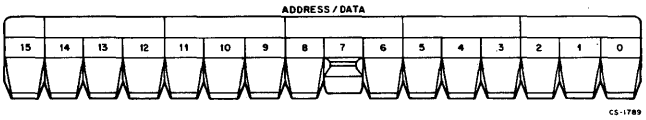
Only one slave may be on-line at any time.

Procedure:

a. Load the program from the appropriate media.

b. Ensure that the TU45 is loaded, at load point (LD PT), and on-line.

c. Set the processor ADDRESS/DATA keys as shown.



d. Press and release the LOAD ADRS key.

e. Press and release the START key.

f. Immediately put all ADDRESS/DATA keys down.

g. The Teletype® will print:

REGISTER START: 172448

h. Type a CR (carriage return).

i. The Teletype will print:

VECTOR ADDRESS: 224

j. Type a CR.

k. The Teletype will print:

NRZ ONLY: TYPE 0
STATIC TESTS ONLY: TYPE 0
FOR DRIVE ADDRESS TEST; ENTER EXPT DRIVE NUMBER, ALL OTHERS SHOULD BE NON-EXISTENT.
DRIVE NUMBER

l. The Teletype will again print:

ENTER DRIVE NUMBER

m. Type a CR.

n. The Teletype will print:

FOR SLAVE ADDRESS TEST; ENTER EXPT SLAVE NUMBER, ALL OTHERS SHOULD BE NON-EXISTENT.
SLAVE NUMBER SN:0001

o. Observe the unit select number of the TU45 and type in that number.

p. The Teletype will again print:

SLAVE NUMBER

q. If no other TU45's are being tested, type a CR.

r. The test will start. When it is completed, the Teletype will print:

END OF PASS 0

s. If the test failed, press and release the processor CONT KEY to run the test again.

t. If the second pass fails, consult the acceptance technician.

2.9.2.2 Basic Function Test (DECSPEC-11-AYVBD)

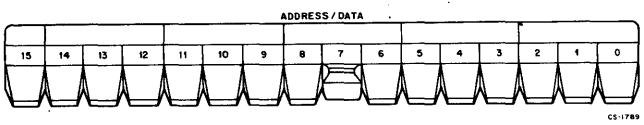
Acceptance Criteria:
Two passes per drive; no errors are allowed.

Procedure:

a. Load program from the appropriate media.

b. Ensure that the TU45 is loaded, at load point (LD PT), and on-line.

c. Set the processor ADDRESS/DATA keys as shown:



® Teletype is a registered trademark of Teletype Corporation.

d. Press and release the LOAD ADRS key.

e. Press and release the START key.

f. Immediately put all ADDRESS/DATA keys down.

g. The Teletype will print:

TM02-TU45 BASIC FUNCTION TEST
ENTER CONDITIONS IN OCTAL
REGISTER START: 172440

h. Type in 172440 followed by a CR.

i. The Teletype will print:

VECTOR: 224

j. Type a CR.

k. The Teletype will print:

DRIVE NUMBER:

l. Observe the Unit Select number on the TM02 and type in that number.

m. The Teletype will print:

SLAVE NUMBER:

n. Observe the Unit Select number on the TU45 and type in that number.

o. The Teletype will print:

SERIAL NO: XXXXX where XXXXX is the actual serial number of the unit.

p. The Teletype will print:

RH11 or RH70:
Type a 1 followed by a CR.
RH only: (Type 0)
NRZ only: (Type 0)

q. Type a 0 followed by a CR.

r. The test will start. When it is completed, the Teletype will print:

Reset slave to on-line before continuing.
END OF PASS 0

2.9.2.3 TM02/TU45 Drive Function Timer (DECSPEC-11-AYVDD)

Acceptance Criteria:
Four passes per drive; no errors are allowed.

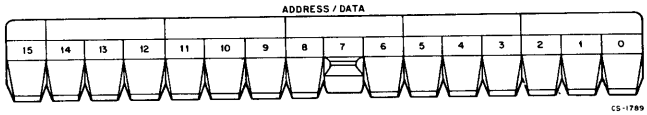
All printed times must be within specifications (see Paragraph A.4). Any nonconformance will be printed by the Teletype.

Procedure:

a. Load the program from the appropriate media.

b. Ensure that the TU45 is loaded, at load point (LD PT), and on-line.

c. Set the processor ADDRESS/DATA keys as shown:



d. Press and release the LOAD ADRS key.

e. Immediately put all ADDRESS/DATA keys down.

f. The Teletype will print:

TYPE FIRST ADDRESS OF CONTROLLER

g. Type in 172440 followed by a CR.

h. The Teletype will print:
TYPE TM02 DRIVE #'s TO BE TESTED

i. Observe the Unit Select number on the TM02 and type in that number followed by a CR.

j. The Teletype will print:

For TM02 DRIVE X-TYPE SLAVE #'s TO BE TESTED
(X is the TM02 Unit Select number)

k. Observe the Unit Select number on the TU45 and type in that number followed by a CR.

l. The Teletype will print:

"SPEED TESTS ONLY" (YES/NO = 1/0)
Type a 0.

m. The Teletype will print:

"NRZ ONLY" (YES/NO = 1/0)
Type a 0.
The test will start, the Teletype will print all times and automatically indicate any errors.

NOTE
Only one slave may be on-line at any time.

2.9.2.4 TU45 Data Reliability Program (DECSPEC-11-AYVAD)

Acceptance Criteria

For 1 Drive System

Drive	Density	Parity	Format	
0	3	0	14	1 pass
0	3	0	15	1 pass
Then Reload				
0	4	0	16	1 pass
0	4	0	14	1 pass

For 2 Drive System

Drive	Density	Parity	Format	
0	3	0	14	1 pass
0	3	0	15	1 pass
1	4	0	14	1 pass
1	4	0	16	1 pass
Then Reload				
0	4	0	14	1 pass
1	3	0	16	1 pass

Data Reliability Acceptance Criteria

Maximum allowable average errors per pass:

Density	Write	Read Forward	Read Reverse
NRZ (800 bpi)	4	1	1
PE (1600 bpi)	7	2	2

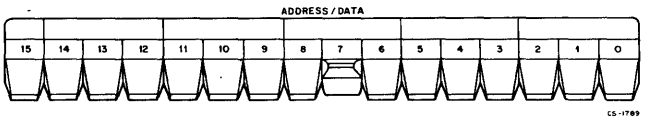
(Pass = BOT to EOT 2400 ft)

Procedure:

a. Load the program from the appropriate media.

b. Ensure that the TU45 is loaded, at Load Point (LD PT), and on-line.

c. Set the processor ADDRESS/DATA keys as shown:



d. Press and release the LOAD ADRS key.

e. Immediately put all ADDRESS/DATA keys down.

f. The Teletype will print:

TU45 Data Reliability test (AYVAD-)
MAKE ENTRIES IN OCTAL
REGISTER START = 172440

g. Type a CR.

h. The Teletype will print:

VECTOR ADDRESS = 224

i. Type a CR.

j. The Teletype will print:

DRIVE NUMBER =

k. Observe the Unit Select number on the TM02 and type in that number.

l. The Teletype will print:

SLAVE NUMBER =

m. Observe the Unit Select number on the TU45 and type in that number.

n. The Teletype will print:

SN: XXXXX*

o. The Teletype will print:

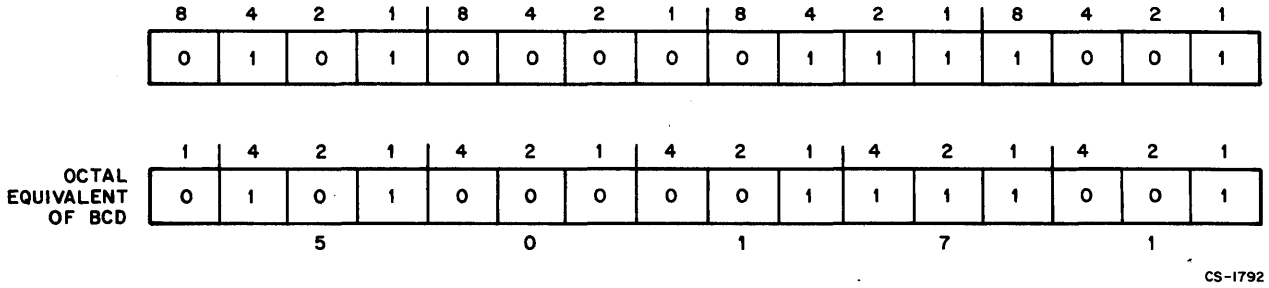
DENSITY =

p. Type in three for NRZ or four for PE.

q. The Teletype will print:

PARITY =
*XXXXX is the octal equivalent of the BCD Code of the decimal serial number. Example follows:

Decimal Serial Number of Unit – 5079
BCD (8421 code) Equivalent –



Serial Number Printed by Teletype – 50171

r. Type in 0.

s. The Teletype will print:

FORMAT =

t. Type in 14, 15, or 16 as called out in acceptance criteria.

u. The Teletype will print:

SLAVE NUMBER =

v. Go back to step 1 and input the information for the next pass to be made. If all of the information for the passes in this loading has been typed in, then type a CR and continue.

w. The Teletype will print:

RECORD COUNT = 0

x. Type in 200 followed by a CR.

y. The Teletype will print:

CHARACTER COUNT = 0

z. Type in 4000 followed by a CR.

aa. The Teletype will print:

PATTERN NUMBER = 1

bb. Type a CR.

cc. The Teletype will print:

TAPE MARK = 0

dd. Type in a 1 followed by a CR.

ee. The Teletype will print:

Single pass = 0
Type a CR.

The Teletype will print:

ENTER STALLS
READ = 1

ff. Type a CR.

gg. The Teletype will print:

WRITE = 1

hh. Type a CR.

ii. The Teletype will print:

TURN AROUND = 1

jj. Set processor ADDRESS/DATA keys 4, 8, and 10 on a "1".

NOTE

Put switch 9 up ONLY if the tape is not at BOT. Do not use switch 9 if the same drive is selected more than once.

SW 10 = Inhibit Error Printout
SW 9 = Rewind if not at BOT
SW 8 = Random Data
SW 4 = Write Retry

kk. Type a CR.

ll. If key 9 was up in step jj, put it down when tape begins to rewind.

mm. When the test is completed, return to step c, and run the remaining tests.

2.10 CHECKOUT PROCEDURE

Check the tape system to see that it is hooked up properly per the installation procedure and then go through the acceptance procedure to verify that the system is operating properly.

2.11 PREVENTIVE MAINTENANCE

The RH70, TM02, and MTA should be cleaned and checked periodically in a manner similar to that used for the CPU as described in the CPU Maintenance Manual.

The preventive maintenance for the TU45 Tape Drive is discussed in Chapter 6 of the Pertec Operating and Service Manual. (PERTEC #104597)

CHAPTER 3
OPERATION AND PROGRAMMING

3.1 GENERAL

Sixteen 16-bit registers are employed to interface the RH70 Massbus Controller to the TM02/TU45 tape system. These registers are loaded and read under program control via the Unibus. The tape system is monitored by status and error indicators in these registers. Figure 3-1 shows the various device registers and their locations. Six of the sixteen registers are located entirely in the RH70 and nine are located entirely in the TM02. The sixteenth register (MTCS1 control and status register) is shared by both the RH70 and the TM02. Bits 15 through 13 and bits 10 through 6 of this register are stored in the RH70 while bits 12, 11, and 5 through 0 are generated by the TM02. Table 3-1 shows the various subsystem registers and their respective addresses. The following paragraphs describe the registers and their bit usage in detail.

3.2 DEFINITIONS

This paragraph describes one of the Massbus signals that are used to operate status information.

Attention Active (ATA) – The ATA bit is a TM02 bit that indicates that the TM02/TU45 requires servicing 1) because it has become ready after completion of a non-data transfer operation, 2) because of an error condition, or 3) because of an important internal status change (Paragraph 3.7.8).

Transfer Error (TRE) – The TRE bit is located in the RH70 and indicates that an RH70 error or a TM02 error has occurred while a data transfer is in progress. Writing a 1 into TRE does not affect the ERR bit in any drive. Similarly, a Drive Clear command does not affect TRE in the RH70.

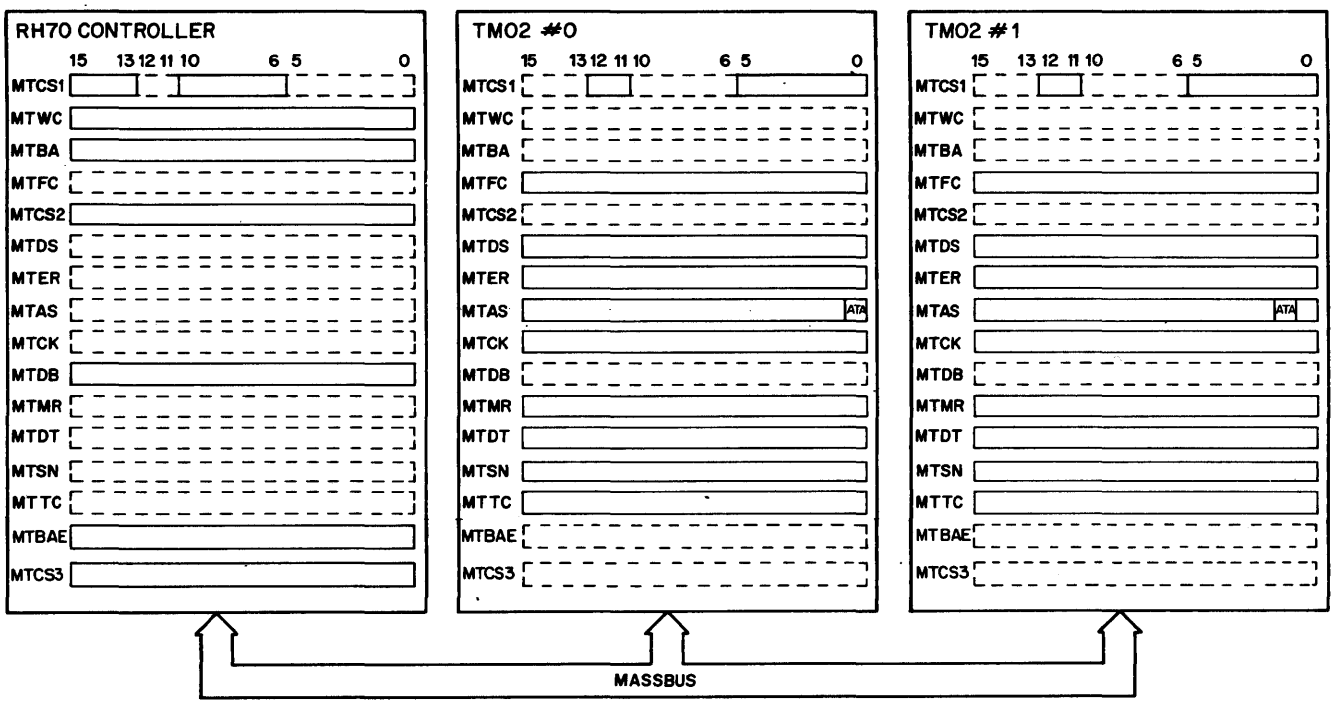
Special Conditions (SC) – The SC bit indicates that a TRE has occurred or that ATA has set on one of the drives.

Table 3-1
RH70 and TM02/TU45 Device Registers

Mnemonic	Register Name	Unibus Address
MTCS1*	Control and Status 1 (shared by RH70 and TM02)	772440
MTWC*	Word Count	772442
MTBA*	Bus Address	772444
MTFC	Frame Count	772446
MTCS2*	Control and Status 2	772450
MTDS	Drive Status	772452
MTER	Error	772454
MTAS	Attention Summary	772456
MTCK	Check Character	772460
MTDB*	Data Buffer	772462
MTMR	Maintenance	772464
MTDT	DriveType	772466
MTSN	Serial Number	772470
MTTC	Tape Control	772472
MTBAE	Bus Address Extension	772474
MTCS3	Control and Status 3	772476

*RH70 Registers

Ready, Drive Ready (RDY, DRY) – RDY is the "ready" indicator for the RH70 controller. When RDY is asserted, the RH70 is ready to accept a data transfer command. DRY is the "ready" indicator for each drive. To successfully initiate a data transfer command, both of these bits must be asserted. However, a non-data transfer command (e.g., Search, Drive Clear) may be issued to a drive any time DRY is asserted, regardless of the state of the RDY bit.



NOTES:

1. MTCS1 shared between RH70 and TM02
   bits 15-13 & 10-6 are stored in RH70
   bits 12, 11, & 5-0 are generated by TM02
2. Each drive is assigned an attention summary bit in the bit location corresponding to it's unit no.
3. Location of registers denoted by solid lines; dotted lines are for reference only

MTCS1, MTCS2, MTCS3 – Control and Status
MTWC – Word Count
MTBA – Unibus Address
MTFC – Frame Count
MTDS – Drive Status
MTER – Error
MTAS – Attention Summary
MTCK – Check Character
MTDB – Data Buffer
MTMR – Maintenance
MTDT – Drive Type
MTSN – Serial Number
MTTC – Tape Control
MTBAE – Bus Address Extension

11-2976

Figure 3-1 Device Registers

When a data transfer command is successfully initiated, both RDY and DRY become negated. When a non-data transfer command (such as Search) is successfully initiated, only the DRY bit becomes negated. Some non-data transfer commands (such as Drive Clear) take so little time to execute, that the program will never see the negation of the DRY bit.

The assertion of RDY after the execution of a data transfer command will not occur until the DRY bit is set and the controller (RH70) is done.

If any command other than Drive Clear is issued to a drive which has ERR (a summary error bit located in each drive) asserted, the command is ignored by the drive. If a data transfer command is issued to a drive that has ERR asserted, the drive does not execute the command, and the missed transfer error (MXF, bit 9 in the MTCS2 register) occurs in the RH70.

Clearing Methods

Controller Clear – Controller clear is the action of writing a 1 into the CLR control bit (bit 5 of MTCS2). This causes the following to be cleared:

a. All controller errors (MTCS1 – bits 15 through 13, MTCS2 – bits 15 through 8, MTCS3 – bits 15 through 11).

b. Data buffer

c. MTBA Bus Address register and MTBAE Bus Address Extension register.

d. Unit select U(02:00), IE, BAI, PAT, IPCK 0–3, and DBL.

e. Errors, function code, and MTDA register in all drives connected to the RH70 (by assertion of the Massbus INIT signal).

RH70 Error Clear – RH70 error clear is the action of writing a 1 into the TRE bit (bit 14 of MTCS1). This causes all controller errors to be cleared (MTCS2 – bits 15 through 8, MTCS1 bits 14 and 13, and MTCS3 – bits 15 through 11).

Drive Clear – Drive Clear is a command code (11_8) that causes errors and the function code to be cleared in the drive selected by U(02:00).

Table 3-2 shows the various methods used to clear the magnetic tape system.

Table 3-2
Results of Program-Controlled Clearing

	RESULTS					
Action	**Clear All RH70 Errors**	**Clear Data Buffer**	**Clear BA, BAE, U(02:00), IE, PAT, BAI, IPCK, DBL**	**Assert Massbus INIT**	**Clear GO, ATA, ERR, and errors in the drive**	**Clear SSC**
Unibus INIT (Reset instruction execution or console reset)	X	X	X	X	X (all 8 drives)	X (all 8 transports)
Controller Clear (Bit 5 in MTCS2←1)	X	X	X	X	X (all 8 drives)	X (all 8 transports)
Issue a Data Transfer command (with GO = 1)	X	X				
RH70 Error Clear (Bit 14 in MTCS1←1)	X					
Drive Clear (Function code with GO = 11_8)					X (selected drive only)	X (selected transport only)

3.3 INTERRUPT CONDITIONS

The RH70 generates an interrupt in the PDP-11 CPU due to the following conditions:

a. Upon termination of a data transfer (if interrupt enable is set when the RH70 becomes "ready").

   Interrupt=(RDY←1)•(IE)

b. Upon assertion of attention or occurrence of a controller error (while the controller is not busy and interrupt enable is set).

   Interrupt=(SC←1)•(RDY)•(IE)

c. When the program writes 1s into IE and RDY in MTCS1 at the same time.

   Interrupt=(IE←1)•(RDY←1)

CAUTION

Read-Modify-Write instruction (BIS, BIC, etc.) to MTCS1 with IE bit set will cause an immediate interrupt.

Read-Modify-Write instruction (BIS, BIC, etc.) to MTCS3 with the IE bit set will not cause an immediate interrupt. In these cases, the interrupt will occur upon normal completion of the operation.

3.4 TERMINATION OF DATA TRANSFERS

A data transfer that has been successfully started may terminate in the following ways:

Assertion of RDY – This is the normal termination and is caused by detection of the inter record gap.

Controller Error – An error is asserted in the MTCS2 register as indicated below:

Bit		Error Class
15	DLT (Data Late)	A
14	WCE (Write Check Error)	A
13	PE (Parity Error)	A
12	NED (Nonexistent Drive)	A
11	NEM (Nonexistent Memory)	A
10	PGE (Program Error)	A
9	MXF (Missed Transfer Error)	B
8	MDPE (Massbus Data Parity Error)	A

Any of these errors sets TRE. The RH70 terminates the data transfer immediately, but waits for DRY which occurs at the inter-record gap before becoming Ready.

Drive Error – An error occurs in the drive. The drive sets ERR in the MTDS register and at least one bit in the MTER register. The ERR bit causes TRE, SC, RDY, DRY, and the ATA bit to be asserted.

Program-caused Abort – By performing a controller clear or a reset instruction, the program can cause Massbus INIT to be asserted by the RH70, which aborts all operations on all drives attached to the controller. (A program-caused abort can also be caused by Drive Clear.) Status and error information is lost when any of the above conditions occur. The RH70 and TM02/TU45 become Ready immediately.

3.5 TWU45 COMMANDS

TWU45 commands are classified as data transfer or non-data transfer commands. Table 3-3 lists all the commands with a brief description of each. Before a command is initiated, certain parameters are specified by the program for each command. These parameters are listed in Table 3-4. For example, in an Erase operation, it is only necessary to specify the TM02 and the TU45.

Table 3-3
Command Function Codes

Function Code F(0–5) (octal)	Operation	Description
01	No Op	Performs no operation. Clears GO bit in Control register.
03	Rewind Off-line*	1. Initiates a rewind on selected transport and places it off-line, and unloads tape. 2. Clears GO bit. 3. Sets the following bits in the Status register: Drive Ready (DRY) Slave Status Change (SSC) Attention Active (ATA) Rewind off-line causes one interrupt only indicating rewind underway and transport off-line.
07	Rewind	1. Initiates a rewind to BOT marker on selected transport and clears the GO bit. 2. Sets DRY, PIP, and ATA bits in the Status register during rewind. 3. When BOT is sensed, sets SSC and clears PIP. Rewind causes two interrupts: a. Rewind underway b. SSC when BOT is sensed (rewind 'job done').
11	Drive Clear	Similar to Initialize. Resets all TM02 and selected transport logic only. Does not affect unselected transports.
25	Erase	Erases approximately 3 in. of tape. Clears GO bit and sets ATA on termination.
27	Write Tape Mark	Writes a special tape record on the selected transport. Clears GO bit and sets ATA bit on termination (Paragraph 1.6.1.2).
31	Space Forward	Moves tape forward (toward EOT) on the selected transport over the number of records specified by the Frame Count register. Aborts space operation if TM or EOT is detected prior to specified frame count. Clears GO bit and sets ATA on termination.

*Requires manual intervention to return transport on-line.

Table 3-3 (Cont)
Command Function Codes

Function Code F(0–5) (octal)	Operation	Description
33	Space Reverse	Moves tape in reverse (toward BOT) on the selected transport over the number of records specified by the Frame Count register. Aborts space operation if TM or BOT is detected prior to specified frame count. Clears GO bit and sets ATA on termination.
51	Write Check Forward	Does a word-by-word comparison of specified memory locations with the tape record read from tape in the forward direction.
57	Write Check Reverse	Same as write-check forward except for reverse tape motion.
61	Write Forward	Writes forward one tape record on the selected transport. Record length is determined by Frame Count register. Clears GO bit on command termination.
71	Read Forward	Reads forward one tape record on the selected transport. Clears GO bit on command termination.
77	Read Reverse	Reads reverse one tape record on the selected transport. Clears GO bit on command termination (see Note). **NOTE** **Do not use this mode unless whole PDP-11 data words were written in the record.**

3.5.1 Non-Data Transfer Commands

Non-data transfer commands do not cause the RH70 to become busy (RDY asserted). Therefore, other commands can be issued to other drives while a non-data transfer command is in progress. A non-data transfer command is terminated when the Attention bit for the specified drive is asserted. The assertion of the Attention bit, upon completion of a non-data transfer command, will cause an interrupt if the IE bit is set and RDY is asserted.

3.5.2 Data Transfer Commands

Data transfer commands cause the RH70 to become busy (RDY negated). No other commands can be issued while a data transfer command is in progress. Termination of a data transfer command is indicated by the re-assertion of RDY. Assertion of RDY, upon completion of a data transfer command, will cause an interrupt if IE is set. If a data transfer and a non-data transfer command are in progress (on different drives), an interrupt will occur only on the assertion of RDY even though the Attention bit (asserted on completion of the non-data transfer command) may be asserted before the RDY bit. Data transfer commands are read, write, and write check and cause the transfer of data over the data bus (synchronous) portion of the Massbus. The parameters specified by the program during the issuance of these commands are described as follows:

Bus Address – The bus address represents the starting memory location that the data will be read from (for a write) or written into (for a read). The address occupies the 16 bits of the MTBA bus address register and six bits of the MTBAE bus address extension register.

Selected TM02 Tape Controller – The TM02 is selected by writing the MTCS2 register in the RH70. Bits 0 through 2 of the register are the unit select bits that specify the desired TM02.

Word Count – The word count is a count of the number of words to be transferred to or from the tape drive. The MTWC word count register is loaded with the two's complement of the number of words to be transferred and is incremented toward zero for each word transferred to or from memory. Overflow to zero terminates the Unibus transfer.

Frame Count – The MTFC frame count register specifies the number of frames (bytes) to be written on tape. Each sixteen-bit PDP-11 word is divided into two frames. Consequently, the frame count register is loaded with twice the number in the MTWC register for normal or 15 mode or four times the number in the MTWC register for core dump mode. The frame count register is loaded with the two's complement of the number of frames to be written. Overflow to zero terminates transfers on the slave bus. Since the frame count register is located in the TM02 tape controller, writing this register requires the RH70 to perform a Massbus cycle. If the frame count register overflows before word count, the transfer may be terminated by FCE (see below). If word count overflows before frame count, the rest of the record is zero-filled.

Normally, the frame count register is set to twice the word count in normal and 15 mode. In core dump mode, the frame count is set to four times the word count. If less than two frames of the last word are desired in normal or 15 mode, the frame count register may be loaded with an odd number. If less than four frames of the last word are desired in core dump mode, the frame count register may be loaded to 1, 2, or 3 less than four times the word count. For example, if 21 frames were to be transferred in normal mode, the frame count register is set to the two's complement of 21 and the word count register is set to the two's complement of 11. Frame count would overflow before word count and the last byte would be transferred as 0s. No FCE occurs in this case. Frame count need not be specified in a read operation or a write-check operation and is automatically reset in these cases. At the end of a read or write-check operation, the frame count is equal to the number of frames read from tape.

Selected Tape Transport, Format Character Packing and Tape Density – These parameters are specified by the program by writing the MTTC tape control register. Bits 0 through 2 of this register are slave select bits which select the appropriate tape transport (designated slave). Bits 4 through 7 of this register are the format select bits which specify Massbus-to-tape character formatting during a write (or tape character-to-Massbus formatting during a read operation). Bits 8 through 10 of this register specify the tape density (1600 bpi for PE, 800 bpi for NRZI).

3.5.2.1 Write Data Transfer – After the above parameters are specified, the data transfer is initiated by loading a write command function code in the MTCS1 register in the RH70 and setting the GO bit. This process logically connects the data portion (synchronous) of the TM02 to the RH70 as this is the path that the data will be transferred over.

Memory cycles are initiated by the RH70 and the data words from memory are transferred to the input of the data buffer (Figure 1-5).

For each data word transferred, the word count is incremented by 1 and the bus address is incremented by 2. If double words are transferred, the bus address is incremented by 4. The data words are clocked into and "bubble" through the data buffer. When the first data word reaches the top, it is automatically clocked into the output buffer (OBUF). When the data buffer is filled and a word is in OBUF, the RH70 asserts the RUN signal which signals the TM02 to begin assembling characters and writing on tape.

The TM02 accepts the first data word, converts it into two tape characters, and outputs it to the TU45 tape transport. It then sends a sync clock (SCLK) signal to the RH70 requesting another data word. The RH70 receives SCLK and echoes it back as write clock (WCLK) along with the next data word. The TM02 assembles this into two tape characters, transfers it to the TU45, and issues another SCLK. The process continues until frame count overflow is detected indicating that the desired number of characters have been transferred.

NOTE

If the word count register is set to *less* than twice the frame count, word count overflow will occur first. This causes the run line to be negated and will cause 0s to be written in the rest of the record. If the word count register is set to *more* than twice the ~~word~~ frame count, frame count overflow will occur first and may cause a frame count error (FCE).

Table 3-4
TWU45 Commands and Required Parameters

Command	Word Count	Slave Select	Frame Count	Bus Address/Ext.	Unit Select	Density	Format	Function Code GO
Read, Read Reverse	X	X		X	X	X	X	X
Write	X	X	X	X	X	X	X	X
Write-check, Write Check Reverse	X	X		X	X	X	X	X
Space		X	X		X	X		X
Erase		X			X			X
Rewind, Rewind Off-line		X			X			X
Write Tapemark		X			X	X		X
NOP								X
Drive Clear		X			X			X

Notes: (1) Frame count for a space operation is loaded with 2's complement of number of records to be spaced.

(2) GO bit must be loaded last. The order of specifying the other parameters is immaterial.

(3) X indicates that the item must be specified, e.g., word count specified for read, write, and write check.

3.5.2.2 **Read Data Transfer** – In a read operation, the data words are transferred from the tape drive to memory via the TM02 and RH70 and cache. The data path functionally consists of the TM02/TU45, RH70 data buffer, cache memory and main memory (Figure 1-5).

The data transfer is initiated by loading a Read command function code in the MTCS1 register in the RH70 and setting the GO bit. This process logically connects the data portion (synchronous) of the TM02 to the RH70 as this is the path that the data will be transferred over.

The Run line is asserted by the RH70 and when the tape is up to speed, the TM02 receives two tape characters from the TU45 tape transport, assembles them into a 16-bit word, and sends it to the RH70 data buffer accompanied by SCLK. When the data word sequences through the data buffer to OBUF, the RH70 initiates a memory request to main memory via cache. When memory is ready, it will accept the data.

The TM02 waits for the next two characters and, on the negation of SCLK, transfers the second word to the RH70. The process continues until the inter-record gap is detected. At this point, the TM02 sends EBL to the RH70 to terminate the data transfer.

NOTE

If the Word Count register overflows before the inter-record gap, only the number of words designated in the Word Count register will be transferred. In this case, the RH70 will ignore the remaining words and wait for EBL in the drive to terminate the data transfer. If EBL occurs before word count overflow, a frame count error (FCE) is flagged.

3.5.2.3 Write-Check Data Transfer – The third type of data transfer is a write-check and is initiated when a write-check function is specified in the MTCS1 register and the GO bit is set. In this operation, a record which has previously been written onto the tape is read from the tape. This data is compared to the data in memory originally used to write on the tape. The comparison is accomplished by Exclusive OR gates, and if any of the bits fail to compare, a write-check error occurs. This method allows automatic verification that the data on tape agrees with the contents of memory.

3.5.2.4 Data Transfer Rates – The data transfer rate from the drive is determined by the frequency of the data on tape. The basic data transfer rates are listed below:

PE	1600 BPI – 8.4 μs/character
NRZI	800 BPI – 16.8 μs/character

3.6 REGISTER DESCRIPTIONS

The following paragraphs provide a description of each bit in the RH70 and TM02 registers. Figure 3-2 shows each register and the associated bits in each register.

3.6.1 Control and Status 1 (MTCS1) Register (772440)

This register is utilized by both the controller and the mass storage device to store the device commands and hold operational status. Register bits 0 through 5, 11, and 12 are dedicated for use by the drive and are physically located in each drive attached to the controller. When reading or writing this register, the selected drive (indicated by bits 2 through 0 in the MTCS2 register) will respond in those bit positions.

When the program reads, writes a word, or writes the low byte of this register, a register cycle will be initiated to the selected drive over the Massbus. If the unit selected does not exist or respond, a NED (non-existing drive) error will result. The program may, however, write the upper byte of this register without regard to the unit selected and without affecting any drive.

Register bits 0 through 5 indicate the command to be performed and are actually stored in the selected drive. The controller will always interrogate the command code being passed to the drive by the program and will prepare for the appropriate memory cycle required by data transfer operations. Data transfer command codes are designated by 51_8 through 77_8 (always odd since the GO bit must be asserted to execute the function) and will cause the controller to become busy (RDY negated) until the completion of the operation. When the controller is busy, no further data transfer commands may be issued (see PGE bit 10 in MTCS2). Non-data transfer commands, however, may be issued at any time and to any drive which is not busy.

While a data transfer is in progress, unit select bits U(02:00) in the MTCS2 register may be changed by the program to issue a non-data transfer command to another drive. This will not affect the data transfer.

When a non-data transfer command code is written into MTCS1 while a data transfer is taking place, only the even (low) byte of MTCS1 should be written. This will prevent the program from unintentionally changing MTCS1 status bits (A16, A17) if the transfer is completed just before the register is written. (While the RDY bit is negated, the RH70 prevents program modification of these control bits even when the write is done into the odd byte.)

Figure 3-3 shows the MTCS1 bit format and Table 3-5 provides a description of each bit.

3.6.2 Word Count (MTWC) Register (772442)

This register is loaded by the program with the 2's complement of the number of words to be transferred. During a data transfer, it is incremented by 1 each time a word is transmitted to or from memory.

Figure 3-4 shows the MTWC bit format, and Table 3-6 provides a description of each bit.

3.6.3 Bus Address (MTBA) Register (772444)

This device register is used by the RH70 to address the memory location in which a transfer is to take place. The MTBA register forms the lower 16 bits of address which combine with MTBAE bits 05 through 00 to create the 22-bit memory address. This register should be loaded by the program with the starting memory address. During forward operations, this register is loaded with the lowest value memory address, while in reverse operations, this register is loaded with the highest value memory address. Each time a data transfer is made, the register is incremented by 2. If a double data word is transferred, the register is incremented by 4. For read reverse operations, the register is decremented by two for a single word data transfer or four for a double word transfer. If the BAI (Bus Address Increment Inhibit) bit (bit 03 of MTCS2) is set, the incrementing of the MTBA register is inhibited and all transfers take place to or from the starting memory address. Figure 3-5 shows the MTBA bit usage, and Table 3-7 provides a description of each bit.

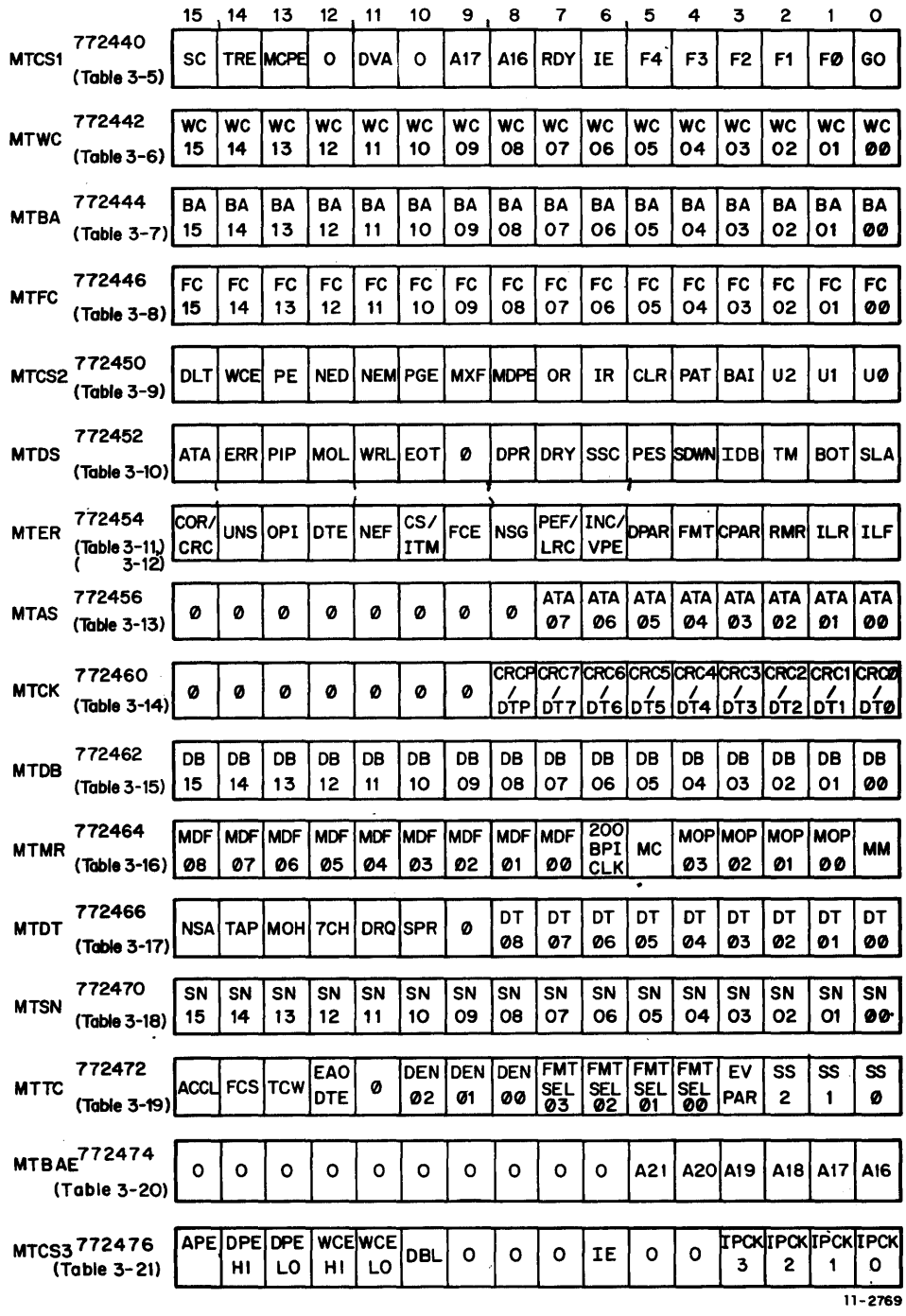


Figure 3-2 RH70/TM02 Register Summary

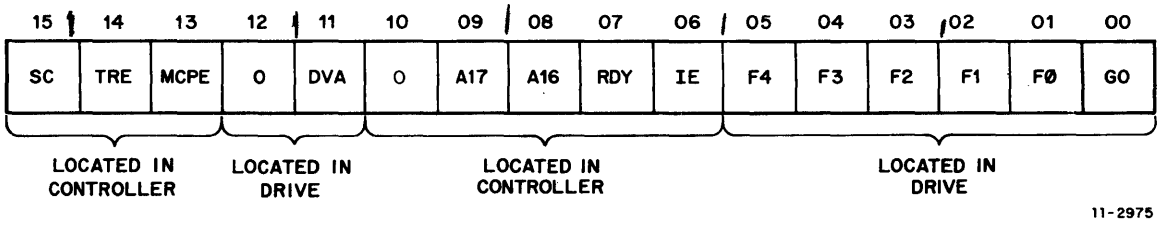


Figure 3-3 Control and Status Register 1-Bit Usage

Table 3-5
Control and Status 1 Register Bit Assignments

Bit		Set By/Cleared By	Remarks
15	SC Special condition Read only	Set by TRE, ATTN, or Massbus control parity error. Cleared by Unibus INIT, controller clear, or by removing the ATTN condition.	SC=TRE+ATTN+MCPE
14	TRE Transfer error Read/write	Set by DLT, WCE, PE, NED, NEM, PGE, MXF, MDPE, or a drive error during a data transfer. Cleared by Unibus INIT, controller clear, RH70 error clear, or by loading a data transfer command with GO set.	TRE=DLT+WCE+PE+NED+NEM +PGE+MXF+MDPE+(EXCP•EBL)
13	MCPE Massbus control bus parity error Read only	Set by parity error on Massbus control bus while reading a remote register (located in the drive). Cleared by Unibus INIT, controller clear, RH70 error clear, or loading a data transfer command with the GO bit set.	Parity errors that occur on the Massbus control bus while writing a drive register are detected by the drive and cause the PAR error (MTER register, bit 03) to set. Parity checking occurs at the completion of the register cycle (an MCPE, when reading the MTCS1 register, would not be indicated on the same cycle).
12	Not used	Always read as a 0.	
11	DVA Drive available Read only	Always a 1 in the TM02 when read from an existing drive. Unit number in MTCS2 is an existing drive.	Used in dual port drive applications.
10	Not used	Always read as a 0.	
09 08	A17 A16 Unibus address Read/write	Upper extension bits of the MTBA register. Cleared by Unibus INIT, controller clear or by writing 0s in these bit positions.	These bits cannot be modified while the RH70 is performing a data transfer (RDY negated). Incremented by a carry from the MTBA register during data transfers to/from memory. These bits can also be set/cleared through the MTBAE register.

Table 3-5 (Cont)
Control and Status 1 Register Bit Assignments

Bit	Set By/Cleared By	Remarks
07 RDY Ready Read only	RDY normally=1. During data transfers, RDY=0. The assertion of RDY (transfer complete or TRE) will cause an interrupt if IE=1.	Indicates controller status. When set, the controller will accept any command. When cleared, the controller is performing a data transfer command and will allow only non-data transfer commands to be executed.
06 IE Interrupt enable Read/write	IE is a control bit which can be set only under program control. When IE=1, an interrupt may occur due to RDY or ATTN being asserted (Paragraph 3.4). Cleared by Unibus INIT, controller clear, or automatically cleared when an interrupt is recognized by the CPU. When a 0 is written into IE by the program, any pending interrupts are cancelled.	A program-controlled interrupt may occur by writing 1s into IE and RDY at the same time. This bit can be set/cleared through the MTCS3 register.
05–00 F4–F0 and GO bit Read/write	F4–F0 are function (command) code control bits that determine the action to be performed by the RH70 and TM02/TU45 as shown below. The GO bit (MTCS1, bit 0) must be set to cause the controller or drive to respond to a command. The GO bit is reset by the drive at the end of the operation. Cleared by Unibus INIT or controller clear (will abort command execution in all drives).	The function code bits are stored in the selected drive. Data transfer commands, defined as F4·(F3+F2), always cause the RH70 to become busy. (RDY negated.) All other commands are ignored by the RH70 Controller.

	F4	F3	F2	F1	F0	GO	Function
01	0	0	0	0	0	1	No operation
03	0	0	0	0	1	1	Rewind off-line
07	0	0	0	1	1	1	Rewind
11	0	0	1	0	0	1	Drive clear
25	0	1	0	1	0	1	Erase
27	0	1	0	1	1	1	Write tape mark
31	0	1	1	0	0	1	Space forward
33	0	1	1	0	1	1	Space reverse
51	1	0	1	0	0	1	Write check forward
57	1	0	1	1	1	1	Write check reverse
61	1	1	0	0	0	1	Write forward
71	1	1	1	0	0	1	Read forward
77	1	1	1	1	1	1	Read reverse

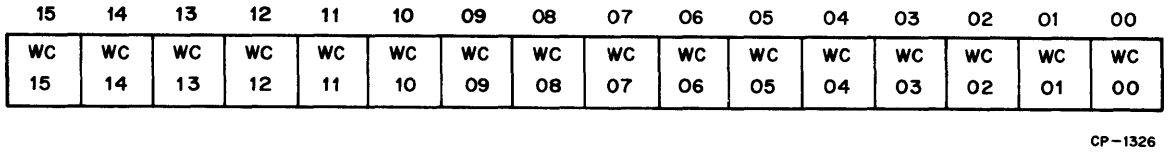


Figure 3-4 Word Count Register Bit Usage

Table 3-6
Word Count Register Bit Assignments

Bit	Set By/Cleared By	Remarks
15–00 WC Word count Read/write	Set by the program to specify the number of words to be transferred (2's complement form). This register is cleared only by writing 0s into it.	Incremented for each word transferred to or from memory.

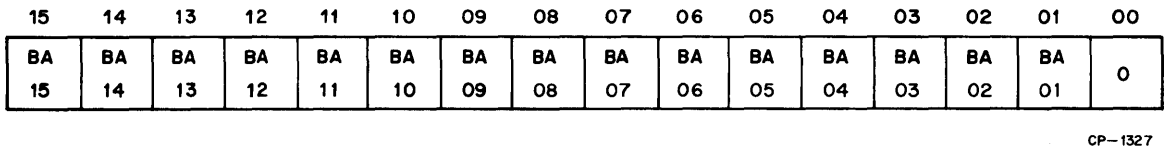


Figure 3-5 Bus Address Register Bit Usage

Table 3-7
Bus Address Register Bit Assignments

Bit	Set By/Cleared By	Remarks
15–01 BA 15–01 Bus address Read/write	Loaded by the program to specify the starting memory address of a transfer. Cleared by Unibus INIT or by controller clear.	The MTBA register is incremented or decremented by 4 for each double data word transferred to or from memory. For single-word operation, the register is incremented or decremented by 2.
00	Not used.	Always read as a 0.

3.6.4 Frame Count (MTFC) Register (772446)

The frame count register is a 16-bit, read/write register that counts tape events. During a data transfer operation (read/write), this register is incremented each time a tape character is transferred to or from the tape. However, during a space operation, this register is incremented each time a record is detected. The register output may be read by the controller at any time; but the controller can only write into this register when the transport is not performing a space or data transfer (GO negated).

For a write operation, the frame count register is loaded, prior to write initiation, with the 2's complement of the number of tape characters to be written. In NRZ mode, the minimum number of characters that can be written is 13. During the writing process, the frame count register is incremented each time a tape character is recorded. Normal write data transfer termination is accomplished when the frame count register overflows to zero. For a space operation, the frame count register functions similarly to a write, except it is loaded with the 2's complement of the number of records to be spaced and is then incremented each time a record is detected. Space termination is accomplished when the register overflows to zero. For a read or write check operation, this register is automatically reset prior to read initiation. The register is then incremented each time a tape character is read. The register is not incremented for check characters (LRCC, CRCC). Thus, at the end of the read operation, the frame count register contains a count of the number of characters read.

Figure 3-6 shows the frame count register bit usage and Table 3-8 provides a description of each bit.

3.6.5 Control and Status 2 (MTCS2) Register (772450)

This register indicates the status of the controller and contains the drive unit number U(02:00). The unit number specified in bits 02 through 00 of this register indicates which drive is responding when registers are addressed that are located in a drive.

These are:

MTCS1 (bits 5 through 0, 12 and 11)

MTDS	MTDT
MTER	MTCK
MTMR	MTTC
MTFC	MTSN

Figure 3-7 shows the MTCS2 bit usage, and Table 3-9 provides a description of each bit.

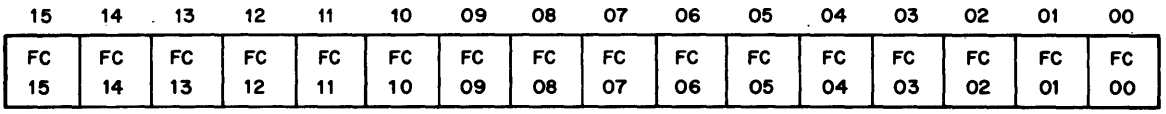


Figure 3-6 Frame Counter Bit Usage

Table 3-8
Frame Counter Bit Assignments

Bit	Set By/Cleared By	Remarks
15–00 FC 15–00 Frame count Read/write	Cleared by writing 0s in the bit locations	Designates in 2's complement form the number of records to be spaced over, characters to be written, or characters that have been read. Initiating a write or space command when the frame count register is loaded with zeros implies a count of 2^{16}.

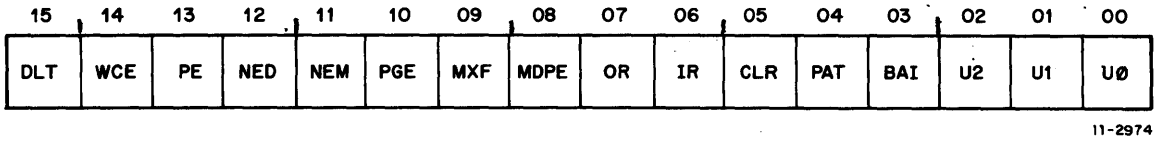


Figure 3-7 Control and Status Register 2-Bit Usage

Table 3-9
Control and Status Register 2 Bit Assignments

Bit	Set By/Cleared By	Remarks
15 DLT Data late Read only	Set when the controller is unable to supply a data word during a write operation or accept a data word during a read or write-check operation at the time the drive demands a transfer. Cleared by Unibus INIT, controller clear, RH70 error clear, or loading a data transfer command with GO set.	DLT causes TRE. Buffering is 8_{10} words deep in the controller, and a DLT error indicates a severely overloaded system.
14 WCE Write check error Read only	Set when the controller is performing a write-check operation and a word on the tape does not match the corresponding word in memory. Cleared by Unibus INIT, controller clear, RH70 error clear, or loading a data transfer command with GO set.	WCE causes TRE. If a mismatch is detected during a write-check command execution, the transfer terminates and the WCE bit is set. The mismatched data word from the tape drive is displayed in the data buffer (MTDB).
13 PE Parity error Read/write	Set if a data parity error from memory is detected while the controller is performing a write or write-check command. Cleared by Unibus INIT controller clear, RH70 error clear, or loading a data transfer command with GO set.	PE=APE+DPEOW+DPEEW APE – address parity error DPEOW – data parity error odd word DPEEW – data parity error even word
12 NED Non-existent drive Read only	Set when the program reads or writes a drive register (CS1, DS, ER, MR, FC, DT, CK, TC, or SN) in a drive [selected by U(02:00)] which does not exist or is powered down. (The drive fails to assert TRA within 1.5 μs after assertion of DEM.) Cleared by Unibus INIT, controller clear, RH70 error clear, or loading a data transfer command with GO set.	NED causes TRE.
11 NEM Non-existent memory Read only	Set when the controller is performing a data transfer and the memory address specified in MTBA and MTBAE is non-existent (does not respond to MSYN within 10 μs). Cleared by Unibus INIT, controller clear, RH70 error clear, or loading a data transfer command with GO set.	NEM causes TRE to set.

Table 3-9 (Cont)
Control and Status Register 2 Bit Assignments

Bit		Set By/Cleared By	Remarks
10	PGE Program error Read only	Set when the program attempts to initiate a data transfer operation while the RH70 is currently performing one. Cleared by Unibus INIT, controller clear, RH70 error clear, or loading a data transfer command with GO set.	PGE causes TRE to set. The data transfer command code is inhibited from being written into the drive.
09	MXF Missed transfer Read/write	Set if the drive does not respond to a data transfer command within 650 μs. Cleared by Unibus INIT, controller clear, RH70 error clear, or loading a data transfer command with GO set.	MXF causes TRE to set. This bit can be set or cleared by the program for diagnostic purposes. This error occurs if a data transfer command is loaded into a drive which has ERR set, or if the drive fails to initiate the command for any reason (such as a parity error).
08	MDPE Massbus data bus parity error Read only	Set when a parity error occurs on the Massbus data bus while doing a read or write-check operation. During maintenance operation, MDPE may occur when writing or reading the MTDB register if bad parity is detected as the word is propagated through the data buffer. Cleared by Unibus INIT, controller clear, RH70 error clear, or loading a data transfer command with GO set.	MDPE causes TRE to set. Parity errors on the Massbus data bus during write operations are detected by the drive and cause the PAR error (MTER register, bit 03).
07	OR Output ready Read only	Set when a word is present in the MTDB register and can be read by the program. Cleared by Unibus INIT, controller clear, or by reading DB (Paragraph 3.6.10).	Serves as a status indicator for diagnostic check of the data buffer.
06	IR Input ready Read only	Set when a word is written in the MTDB register by the program. Cleared when the data buffer (MTDB) is full (contains eight words).	Serves as a status indicator for diagnostic check of the data buffer.
05	CLR Controller clear Write only	When a 1 is written into this bit, the RH70 and all drives are initialized (Paragraph 3.2).	Unibus INIT also causes controller clear to occur.

Table 3-9 (Cont)
Control and Status Register 2 Bit Assignments

Bit	Set By/Cleared By	Remarks
04 PAT Parity test Read/write	While PAT is set, the RH70 generates even parity on both the control bus and data bus of the Massbus. When clear, odd parity is generated. Cleared by Unibus INIT or controller clear.	While PAT is set, the RH70 checks for even parity received on the data bus but not on the control bus. If PAT bit is set (IPCK bits are all 0s) during maintenance operations of the data buffer, the data word loaded in the data buffer will sequence through the buffer with parity being calculated by the hardware (controlled by IPCK bits). When the data word reaches the OBUF register, the parity checker (controlled by PAT) will detect inverse parity as an MDPE error.
03 BAI Unibus address increment inhibit Read/write	When BAI is set, the RH70 will not increment the BA register during a data transfer. This bit cannot be modified while the RH70 is doing a data transfer (RDY negated). Cleared by Unibus INIT or controller clear.	When set during a data transfer, all data words are read from or written into the same memory location.
02–00 U 02–00 Unit select Read/write	These bits are written by the program to select a drive. Cleared by Unibus INIT or controller clear.	The unit select bits can be changed by the program during data transfer operations without interfering with the transfer. The CS1, DS, ER, MR, FC, DT, CK, TC, and SN registers contain bits that come from the selected drive.

3.6.6 Drive Status (MTDS) Register (772452)

This register contains the various status indicators for the selected drive. The status indicators displayed are those of the tape drive which is specified by the unit select bits (02:00) of the MTCS2 register. The register is a read-only register. Figure 3-8 shows the MTDS bit usage, and Table 3-10 provides a description of each bit. Writing into this register will not cause an error and will not modify any of the status bits.

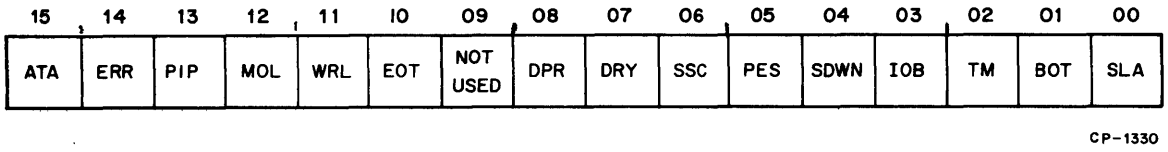


Figure 3-8 Drive Status Register Bit Usage

Table 3-10
Drive Status Register Bit Assignments

Bit		Set By/Cleared By	Remarks
15	ATA Attention active Read only	Set by the drive when there is an attention condition in that drive. Cleared by Unibus INIT, controller clear, drive clear, loading a command with the GO bit set, or loading a 1 in the MTAS register in the bit position corresponding to the drive's unit number. (The last two methods of clearing the ATA bit will not clear the error indicators in the drive.)	An attention condition indicates one of the following: 1. The TM02 and the selected transport require servicing due to SSC (see bit 6 in this Table). 2. The TM02 and the selected transport have become ready after a non-data transfer operation. 3. At the completion of any operation with EOT asserted.
14	ERR Error summary Read only	Set when one or more of the error bits is set in the MTER register of the selected drive. Cleared by Unibus INIT, controller clear, or by drive clear.	This bit is the logical OR of all the bits in the MTER register. This bit is not cleared by loading a command other than drive clear. While ERR is asserted, commands other than drive clear are not accepted by the drive.
13	PIP Positioning in progress Read only	Set by the drive while the space or rewind command is under way. Cleared at the completion of the operation.	
12	MOL Medium on-line Read only	Set when the selected slave is loaded and the on-line switch activated. This condition is necessary for response to any commands – if GO=1 and MOL=0, the command is aborted and UNS and ATA are asserted. This bit is not affected by drive clear or INIT.	Indicates selected slave is ready for immediate use. Any change in status of MOL will set ATA.
11	WRL Write locked Read only	Set whenever a reel of tape without a write enable ring is loaded on the selected slave. This bit is not affected by drive clear or INIT.	Indicates that the selected slave transport is write protected.
10	EOT End of tape Read only	Set when the EOT marker is recognized during forward tape motion. Cleared when the EOT marker is passed over during reverse tape motion. This bit is not affected by drive clear or INIT, however, execution of a rewind command causes EOT to be cleared.	

Table 3-10 (Cont)
Drive Status Register Bit Assignments

Bit		Set By/Cleared By	Remarks
09	Not used		
08	DPR Drive present Read only	Always set in the TU45/TM02 system.	This bit is a hardwired 1.
07	DRY Drive ready Read only	Set by INIT or at the completion of a command. Cleared whenever a valid command (with the GO bit asserted) is loaded into MTCS1.	Indicates that the drive is on-line and prepared to accept a command. It does not necessarily indicate that the slave is ready to accept a command (see SPR, MOL, PIP).
06	SSC Slave status change Read only	Set when any slave transport requires attention due to one of the following conditions: a) Completion of a rewind b) Power failure c) Coming on-line d) Going off-line Cleared by INIT. Drive clear will clear this bit if the SSC condition was raised by the selected slave and no other slaves are posting SSC.	Setting SSC causes ATA to be asserted as soon as DRY becomes asserted. ATA is asserted immediately if DRY is asserted. More than one slave can be asserting SSC simultaneously. Each drive must be polled (for changes in SPR, MOL, PIP), in turn, and after servicing, a drive clear should be used to clear the SSC on that slave. All drives must be polled when SSC is serviced since an interrupt will only occur on SSC transitioning to a 1.
05	PES Phase encoded status Read only	Set when the selected slave is in PE mode. Cleared when the selected slave is in NRZI mode. This bit is not affected by drive clear or INIT.	Reflects the format mode in which the formatter is operating.
04	SDWN Slowing down Read only	Set during the period when tape motion is stopping. This bit is not affected by drive clear or INIT.	DRY is asserted on the leading edge of SDWN.
03	IDB Identification burst Read only	Set in PE mode on recognition of the PE identification burst. Cleared when another command is issued, or cleared by drive clear or INIT.	In the forward direction, the bit remains set through the reading, writing, or spacing operation. On a PE tape, IDB should be asserted after any tape motion operation which began from BOT.

Table 3-10 (Cont)
Drive Status Register Bit Assignments

Bit		Set By/Cleared By	Remarks
02	TM Tape mark Read only	Set when a tape mark is detected and remains set until the next tape motion operation is initiated. Cleared by INIT or drive clear.	Indicates detection of tape mark. The phase encoded tape mark written by the TU45 consists of 40 characters with zeros in physical tracks 1, 2, 4, 5, and 8 with tracks 3, 6, 7, 9 dc erased. The NRZI filemark written by the TU45 consists of a single character record followed by the LRCC for that record. CRCC is held 0 for 9-track recording of tape mark. The single character contains octal 023. TM should be asserted after the completion of a write tape mark command.
01	BOT Beginning of tape Read only	Set when the selected slave detects the BOT marker. This bit is not affected by drive clear or INIT. Cleared by passing BOT (Beginning of Tape) in the forward direction.	
00	SLA Slave attention Read only	Set by a selected slave which requires attention due to coming on-line. Cleared by drive clear or INIT.	

3.6.7 Error (MTER) Register (772454)

There are 16 different error conditions that can be detected in the TM02/TU45 tape drive system. The error register is a 16-bit, read-only register which stores all of the tape system error indications.

TM02/TU45 errors are categorized as class A and class B. Class B errors will terminate an in-progress data transfer; a class A error will not. However, the Massbus controller is notified of any error during a data transfer by the immediate assertion of EXC H on the Massbus. If the TM02/TU45 is not performing any operation, or is performing a rewind (i.e., the GO bit is clear), the controller is immediately notified of an error condition by the assertion of ATTN H on the Massbus.

Figure 3-9 illustrates the error register bit usage and Table 3-11 provides a description of each bit. Table 3-12 lists the various operations and the associated error conditions which can occur during normal operation of the system. After performing one of the operations listed at the left of the table, only errors indicated by an X may be present in the MTER register. Presence of any other errors indicate a hardware malfunction.

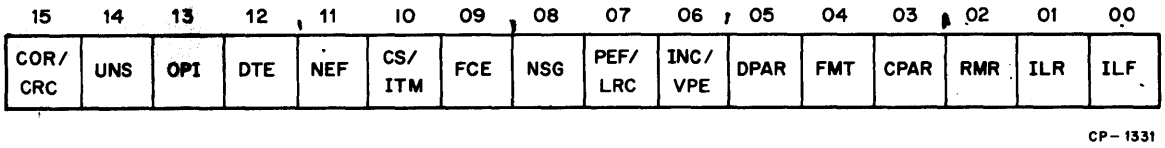


Figure 3-9 Error Register Bit Usage

Table 3-11
Error Register Bit Assignments (N) = hard Error

Bit		Set By/Cleared By	Remarks
15	COR/CRC Correctable data error/CRC error Read only	PE mode – set on a tape character. Therefore, PE error correction logic was able to correct the data on-the-fly and good data was transferred to memory. NRZI mode – set when the CRC character generated from read back data does not agree with the CRC read from tape. Cleared by drive clear or INIT.	In the PE case, when the single dead track is accompanied by a parity error, the data bit in the dead track is inverted. COR/CRC is a class A error.
(14)	UNS Unsafe Read only	Set if the GO bit in the MTCS1 register is set, the MOL bit in the MTDS register is reset, and a command code other than drive clear is issued. Also set if the TM02 detects an imminent power fail condition (AC LO asserted, DC LO not asserted). If UNS is caused by GO=1 while MOL=0, it is cleared by RH70 CLR or DRIVE CLEAR. If UNS is caused by a transient voltage-low condition, it can be cleared by INIT or drive clear when voltage returns to an acceptable level. If UNS is caused by a permanent voltage – low condition, it cannot be cleared.	UNS is a class B error.
(13)	OPI Operation incomplete Read only	A read or space operation indicates that a tape record has not been detected within 4.3 sec from command initiation. A write operation indicates that a read-after-write tape record has not been detected within 0.43 sec from command initiation. Can also indicate that NSG > 0.8 inches. Cleared by INIT or drive clear.	OPI is a class B error. Also, OPI can be set when a rewind command is issued at BOT.

Table 3-11 (Cont)
Error Register Bit Assignments

Bit	Set By/Cleared By	Remarks
12 DTE Drive timing error Read only	Set (1) during a write operation if WCLK was not received from the RH70 in time to provide a valid tape character, or (2) when a data transfer is attempted when the bus of the Massbus is already occupied (OCC=1). Cleared by INIT or drive clear.	When DTE is asserted, the drive also asserts EBL and EXC and aborts the command. Case 1 can be distinguished from case 2 by monitoring the MTFC frame count register. In case 1, this register is incremented at least once since it was loaded. In case 2, this register will contain the same number with which it was loaded prior to the issuance of the data transfer command. During a read operation, DTE can occur only due to case 2. DTE is a class B error.
11 NEF Non-executable function Read only	Set when: 1. A write operation is attempted on a write-protect transport. 2. A space reverse, read reverse, or write check reverse is attempted when the tape is at BOT. 3. The DEN 2 bit in the tape control register does not agree with the PES status bit (i.e., selected drive not capable of selected density). 4. A space or write operation is attempted when FCS=0 in the tape control register. 5. A read or write operation is attempted with DEN2=0 in the tape control register and the 2's complement of a number less than 13 is in the frame count register. Cleared by drive clear or INIT.	NEF is a class B error.

Table 3-11 (Cont)
Error Register Bit Assignments

Bit		Set By/Cleared By	Remarks
10	CS/ITM Correctable skew/ illegal tape mark Read only	In PE mode, this bit is set when excessive but correctable skew is detected in data read back from tape. It is a warning only, and does not indicate that bad data was read from tape. In NRZI mode, this bit is set when a bit pattern is detected on tape which has the general characteristics of an NRZI filemark (specifically, two single characters separated by seven blank character spaces) but which does not contain the exact data expected in an NRZI filemark. Cleared by drive clear or INIT.	When such a bit pattern is detected in NRZI mode, both tape marks in the DS register and CS/IFM in the ER register will become asserted.
09	FCE Frame count error Read only	Set when a space operation has terminated and the frame counter is not cleared. Also set when the RH70 fails to negate RUN when the TM02 asserts EBL. Cleared by drive clear or INIT.	FCE is a class A error.
08	NSG Non standard gap Read only	Set after a data transfer operation whenever any tape characters are read while the read head is scanning the first half of the interrecord gap. Cleared by drive clear or INIT.	NSG is a class A error.
07	PEF/LRC PE format error/LRC Read only	Set in PE mode when an invalid preamble or postamble is detected. Set in NRZI mode when the LRC character generated from readback data does not match the LRC character read from tape. Cleared by drive clear or INIT.	PEF/LRC is a class A error.
06	INC/VPE Incorrectable data/ vertical parity error Read only	A PE read operation indicates that one of the following has occurred: 1. Multiple dead tracks 2. Parity errors without dead tracks 3. Skew overflow During an NRZI read operation, indicates that a vertical parity error has occurred or that data has occurred after the skew delay is over. Cleared by drive clear or INIT.	INC/VPE is a class A error.

Table 3-11 (Cont)
Error Register Bit Assignments

Bit		Set By/Cleared By	Remarks
05	DPAR Data bus parity error Read only	Set when a parity error is detected on the Massbus data lines during a write operation. Cleared by drive clear or INIT.	DPAR is a class A error. Can be forced set by the PAT bit (bit 04 of MTCS2).
04	FMT Format error Read only	Set when a data transfer is attempted with an incorrect format code (i.e., the tape format code loaded in the MTTC register is not implemented on that TM02). Cleared by drive clear or INIT.	Tape motion is inhibited; EXC and EBL are asserted. DRY and ATA are asserted on the negation of EBL. FMT is a class B error.
03	CPAR Control bus parity error Read only	Set when a parity error is detected on the Massbus control lines during a control bus write operation. Cleared by drive clear or INIT.	Detection of CPAR does not interfere with the register write sequence except during a write to the MTCS1 register which suppresses setting of the GO bit. CPAR is a class A error. Can be forced set by the PAT bit (bit 04 of MTCS2).
02	RMR Register modification refused Read only	Set when the controller attempts to write into any implemented TU45 register except the maintenance register or the attention summary register while the GO bit is asserted. If RMR occurs, the addressed register is not modified. Cleared by drive clear or INIT.	RMR is a class A error.
01	ILR Illegal register Read only	Set when a read or write from a non-existent register is attempted. Cleared by drive clear or INIT.	No register modification should occur. On a control bus read, all zeros are gated onto the control lines. ILR is a class A error.
00	ILF Illegal function Read only	Set when the GO bit is asserted and a function code not implemented by the TM02/TU45 is attempted. Cleared by drive clear or INIT.	ILF is a class B error.

Table 3-12
Error Conditions

OPERATIONS	ERRORS															
	ILF [1]	ILR [1]	RMR [1]	CPAR [1]	FMT [1]	DPAR [1]	INC/VPE	PEF/LRC	PPE/NSG	FCE [1]	CS/IFM	NEF [1,2]	DTE	OPI	UNS [2]	COR/CRC
WRITE TO ANY REGISTER*		X	X	X												
READ FROM ANY REGISTER		X														
LOAD NO-OP WITH GO=1	X	X	X	X								X			X	
LOAD REWIND OFF LINE WITH GO=1	X	X	X	X								X			X	
LOAD REWIND ON LINE WITH GO=1	X	X	X	X								X			X	
LOAD DRIVE CLEAR WITH GO=1	X	X	X	X											X	
LOAD WRITE FMK WITH GO=1	X	X	X	X			X	X	X		X	X		X	X	
LOAD ERASE WITH GO=1	X	X	X	X							X	X			X	
LOAD SPACE FWD WITH GO=1	X	X	X	X						X		X		X	X	
LOAD SPACE REV WITH GO=1	X	X	X	X						X		X		X	X	
LOAD WRITE CHECK FWD WITH GO=1	X	X	X	X	X		X	X	X	X	X	X	X	X	X	X
LOAD WRITE CHECK REV WITH GO=1	X	X	X	X	X		X	X	X	X	X	X	X	X	X	X
LOAD WRITE FWD WITH GO=1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
LOAD READ FWD WITH GO=1	X	X	X	X	X		X	X	X	X	X	X	X	X	X	X
LOAD READ REV WITH GO=1	X	X	X	X	X		X	X	X	X	X	X	X	X	X	X
MASS BUS INIT															X	
WRITE TO AS OR MT REG		X		X												

*Except MTAS or MTMR registers

TM02 operations with errors that could be detected during those operations and remain asserted after the operation is complete:

[1] Most likely a programmer-caused error.

[2] Possible operator errors (WRL, off-line).

3.6.8 Attention Summary (MTAS) Register (772456)

The attention summary register is a read/write "pseudo-register," which consists of from one to eight bits depending on the number of TM02s in the system. The term "pseudo-register" refers to the fact that only one register bit position is physically contained in each TM02. This bit position reflects the state of the ATA status bit for that TM02. Hence, bit position 0 of the attention summary register is generated by the ATA bit of TM02 0, bit position 1 is generated by the ATA bit of TM02 1, and so on to bit 7. Bits 8 through 15 are not used.

Unlike the other drive registers, the attention summary register is directly selected by the RH70 controller without first addressing a particular TM02. Thus, for a single attention summary register read operation, every TM02 in the system responds by placing the state of its ATA bit in the appropriate bit position on the control bus and disabling its remaining 15 control bus transmitters. This control bus configuration appears as a single register output which collectively informs the controller of all TM02s that require attention (i.e., ATA=1). The programmer can then selectively examine the error or status registers of each of the affected TM02s to determine the cause of the individual attention conditions.

The programmer can also write into the attention summary register; however, the significance of the bits being written is unusual. Writing a 1 into a bit position resets the ATA bit in the TM02 assigned to that bit position; however, writing a 0 has no effect. This unique writing scheme allows the controller to reset, after inspection, all summary bits that were set, without accidentally resetting those bits that may have become set in the meantime. The following table illustrates the effects of writing into an attention summary bit position.

ATA Bit Before	Summary Bit Written	ATA Bit After
0	0	0
1	0	1
0	1	0
1	1	0

Figure 3-10 shows the bit usage of the attention summary register and Table 3-13 provides a description of each bit.

3.6.8.1 Setting the Attention Active (ATA) Bit – The ATA bit is displayed in bit 15 of the MTDS register, and indicates that the TM02/TU45 requires servicing (1) because it has become ready after completion of a non-data transfer operation (2) because of an error condition, or (3) because of an important internal status change. ATA is asserted only if the DRY (drive ready) bit is asserted. The setting of the ATA bit does not in itself prevent execution of commands. If the ERR (bit 14-MTDS) or the SSC (bit 06-MTDS) transitions from the negated to asserted state while the DRY bit is set, the ATA bit will become asserted. The ATA bit will also be asserted if the DRY bit transitions from the negated to the asserted state at the time one of the following conditions is met:

1. ERR is asserted
2. SSC is asserted
3. The function code in the MTCS1 register denotes a space, erase, write tape mark, rewind or read-in preset command.
4. EOT is asserted.

3.6.8.2 Clearing the Attention Active (ATA) Bit – The ATA bit may be cleared by writing a 1 into its position in the attention summary register. Parity is checked during the control bus transfer which controls the writing of the ATA bits, and if a parity error is detected, the ATA bit will be set at the completion of this transfer. The ATA bit will also be cleared by issuing a valid drive clear command, by asserting the INIT line, or by loading a GO bit into the MTCS1 register while the ERR bit is negated.

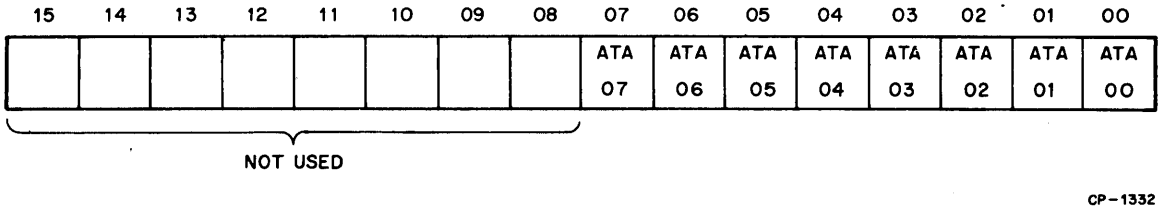


Figure 3-10 Attention Summary Register Bit Usage

Table 3-13
Attention Summary Register Bit Assignments

Bit	Set By/Cleared By	Remarks
15–08	Not used.	
07–00 ATA 07–00 Read/write	Each bit sets when the corresponding drive asserts its ATA bit. All bits are cleared by Unibus INIT, drive clear, or controller clear. Individual bits are cleared by loading a function code with the GO bit in the corresponding drive or by writing a 1 in the ATA bit positions of this register. Writing a 0 has no effect.	

The description below applies only to clearing the ATA bit by writing a 1 into it.

- Clearing the ATA bit while ERR is asserted will result in negation of ATA but will not affect the status of the error register. No commands except drive clear can be executed until the error register is cleared.

- Clearing the ATA bit when the attention condition is caused by normal completion of a space, rewind, read-in preset or write tape mark operation will result in negation of ATA and will result in no other drive status changes.

- Clearing the ATA bit when the attention condition is caused by assertion of SSC will result in negation of ATA. SSC will remain set, and unless it is cleared by drive clear or INIT, completion of the next command will cause ATA to become set.

  Note that SSC can be generated by up to eight slaves in the TM02/TU45 tape system and that its assertion may indicate status changes in several slaves including the selected slave. Thus, while a drive clear command will clear SSC and SLA in a selected slave, unselected slaves could continue to assert SSC. Moreover, if an unselected slave caused SSC to be asserted because of a power failure, issuance of drive clear may (and INIT will) succeed in clearing SSC while leaving a broken slave on the master-slave bus waiting to abort the next command issued it. *BECAUSE OF THIS, SSC SHOULD NEVER BE CLEARED BEFORE A DECISION IS MADE TO POLL ALL AVAILABLE SLAVES TO DETERMINE THEIR STATUS.*

- Clearing the ATA bit when the attention condition is caused by assertion of DRY while EOT is asserted will result in negation of ATA and will leave the drive ready to accept another command. Note that detection of EOT during tape motion will not generate an ATA and will not cause an abort. The EOT flag is a warning only, and it is the programmer's responsibility to go no more than 10 feet beyond the EOT marker.

3.6.9 Character Check (MTCC) Register (772460)

The check character register is a nine-bit, read-only register that permits the programmer to check the validity of a data transfer. At the end of an NRZI read operation, this register contains the CRC character for that operation. Hence, the programmer can determine if the CRCC generator logic is functioning properly. At the end of a PE read operation, however, this register contains a dead track indication (DT=1) of any track which may have dropped one or more bits during the operation.

3.6.9.1 CRC Character Storage – At the end of an NRZI Read or Write operation, the CRC character read from tape will be stored in bits 0 through 8 of the MTCC register. The least significant bit will be stored in bit 0, and the most significant bit in bit 7 of this register.

NOTE

The check character register will contain the check character described above at the end of a read or write operation when DRY transitions from a 0 to a 1. Bits 00 through 08 are guaranteed true only as long as DRY is equal to 1.

3.6.9.2 Dead Track – The dead track register is normally used for maintenance to determine which tracks are dropping data bits. The dropped data bits (read data) are oriented with the following binary weights.

Dead Track	Binary Weight
DT0	2^0
DT1	2^1
DT2	2^2
DT3	2^3
DT4	2^4
DT5	2^5
DT6	2^6
DT7	2^7
DTP	P

Figure 3-11 illustrates the check character register bit usage for both NRZI and PE modes and Table 3-14 provides a description of each bit.

3.6.10 Data Buffer (MTDB) Register (772462)

This register provides a maintenance tool to check the data buffer in the RH70. A total of eight words is accepted before the data buffer becomes full. Successive reads from data buffer will read out words in the same order in which they were entered into the data buffer.

The IR (input ready) and OR (output ready) status indicators in the MTCS2 register are provided so that the programmer can determine when words can be read from or written into the MTDB. IR should be asserted before attempting a write into DB; OR should be asserted before attempting a read from DB.

The MTDB register can be read and written only as an entire word. Any attempt to write a byte will cause an entire word to be written. Reading the DB register is a "destructive read-out" operation: the top data word in the data buffer is removed by the action of reading DB, and a new data word (if present) replaces it a short time later. Conversely, the action of writing the DB register does not destroy the "contents" of DB; it merely causes one more data word to be inserted into the data buffer (if it was not full). Figure 3-12 shows the MTDB bit usage, and Table 3-15 provides a description of each bit.

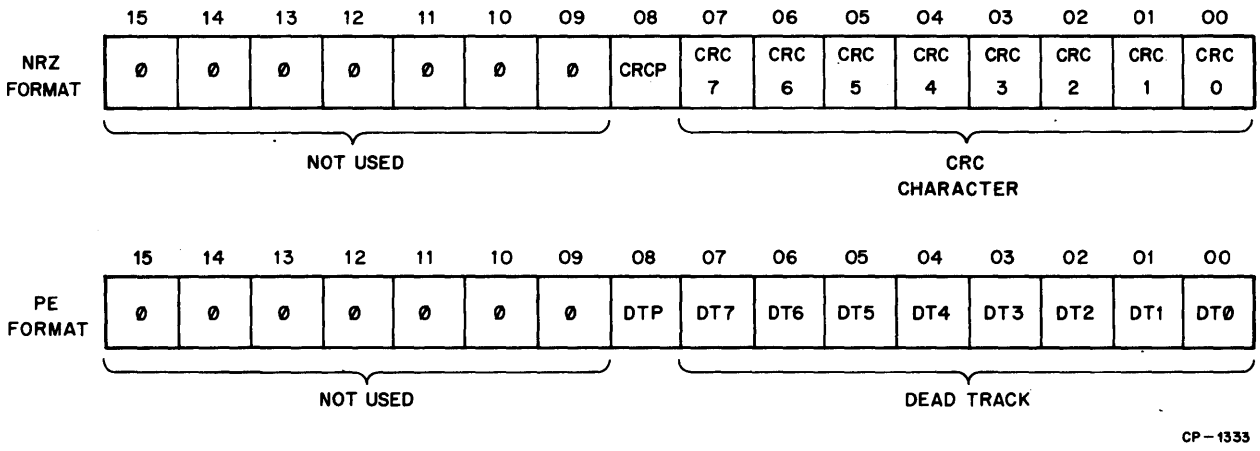


Figure 3-11 Check Character Register Format

Table 3-14
Check Character Register Bit Assignments

Bit	Set By/Cleared By	Remarks
15–09	Not used.	
08–00 CCD Check character/ dead track Read only		Contains the CRC character and parity bit in NRZI mode or the dead track register in PE mode.

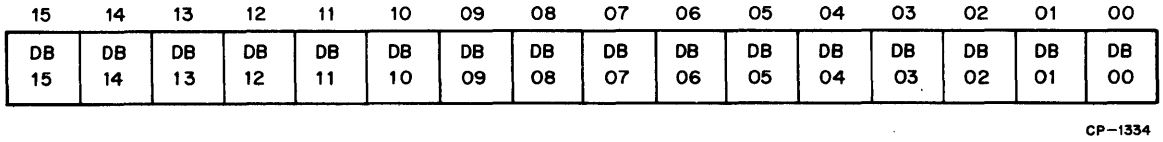


Figure 3-12 Data Buffer Bit Usage

Table 3-15
Data Buffer Bit Assignments

Bit	Set By/Cleared By	Remarks
15–00 DB 15–00 Data buffer Read/write	When read, the contents of OBUF (internal RH70 register) are delivered. Upon completion of the read, the next sequential word in the data buffer will be clocked into OBUF. When written, data is loaded into IBUF (internal RH70 register) and allowed to sequence into the data buffer if space is available.	Used by the program for diagnostic purposes. When the register is written into, IR is cleared until the DB is ready to accept a new word. When the register is read, it will cause OR to be cleared until a new word is ready. During a write-check error condition, the data word read from tape which did not compare with the corresponding word in memory is frozen in MTDB for examination by the program.

3.6.11 Maintenance (MTMR) Register (772464)

The maintenance register is a 16-bit read/write register which performs the following functions:

1. Provides data wraparound paths for checking the data formatting logic in the TM02.
2. Provides a means for testing error detection circuitry within the TM02.
3. Acts as a storage buffer for the longitudinal parity check (LRC) character when operating in NRZI mode and performing a forward read or forward write operation.

Figure 3-13 shows the maintenance register bit format and Table 3-16 provides a description of each bit.

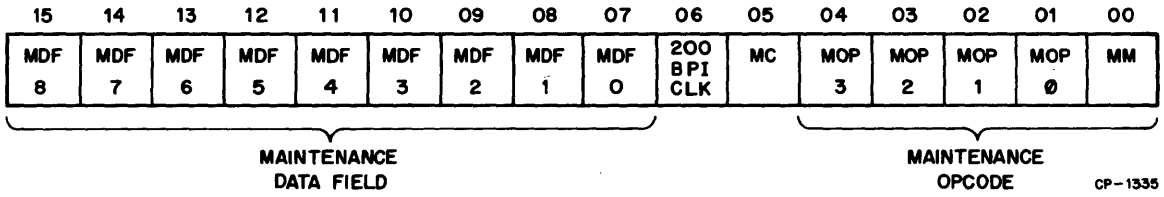


Figure 3-13 Maintenance Register Bit Usage

Table 3-16
Maintenance Register Bit Assignments

Bit	Set By/Cleared By	Remarks
15–7 MDF 8–0 Maintenance data field Read/write		These bits buffer the data generated during wraparound operations. At the end of normal NRZI transfers (except read reverse), these bits contain the LRC of the last record. MDF 0 contains the parity bit for the maintenance data character. MDF 1 contains the LSB of the maintenance data character and the remain bits are contained in order in MDF 2 through MDF 8.
6 BPICLK Two-hundred BPI clock Read only		Displays a clock signal derived from the crystal oscillator in the selected slave. The clock frequency is dependent on the read/write speed of the selected slave and is equal to the frequency at which a continuous succession of characters is written on tape when operating at 200 characters per inch density. BPICLK is displayed to aid in monitoring of drive functions during maintenance mode operations.
5 MC Maintenance clock Read/write	Cleared by drive clear or INIT.	This bit controls the sequencing of data through the TM02 data paths when operating in maintenance mode. If the GO bit is asserted and a maintenance op code of 4_8, 5_8, or 6_8 is contained in MOP bits 0 through 3, the MC bit changes state each time a control bus write to the maintenance register is executed. If the GO bit is asserted and an op code of 3_8 is contained in MOP bits 0 through 3, the MC bit changes state after each read strobe occurs. The maintenance op code is described under bits 4 through 1 in this table.

Table 3-16 (Cont)
Maintenance Register Bit Assignments

Bit	Set By/Cleared By	Remarks
4–1 MOP3–MOP0 Maintenance op code 03–00 Read/write		These bits control the maintenance function which will occur when the MM bit is set to 1 and the TM02 is loaded with the appropriate command. The following op codes will be implemented: a. 0000 – Null code b. 0001 – Interchange read In PE mode, this op code suppresses on-the-fly correction of data errors resulting from a single dead track. c. 0010 – Even parity Causes an even parity bit to be associated with data sent from the TM02 to the controller on either the data or control bus lines, thereby causing the controller to detect parity errors. d. 0011 – Data Wraparound, Global Causes execution of a write forward command to be executed as follows: Data is brought in on the data lines, divided into bytes using the algorithm defined by the format code in the tape control register, formatter as either NRZI or PE write data, multiplexed into the read circuitry and deposited in the maintenance register data field. In PE mode, every other character generates a read strobe to allow the programmer sufficient time to write and monitor a loop.

Table 3-16 (Cont)
Maintenance Register Bit Assignments

Bit	Set By/Cleared By	Remarks
4–1 (Cont)		e. 0100 – Data Wraparound, Partial Causes execution of a write forward command to be executed as follows: Data is brought in on the data lines, divided into bytes using the algorithm defined by the format code in the tape control register, formatted as either NRZI or PE write data, and deposited in the maintenance register data field. f. 0101 – Data Wraparound, Formatter Write Causes execution of a write forward command to be executed as follows: Data is brought in on the data lines, divided into bytes using the format code in the tape control register, and deposited in the maintenance register data field. g. 0110 – Data Wraparound, Formatter Read Causes execution of a read command to be executed as follows: Data is taken from the maintenance register data field, multiplexed into the formatting logic byte-by-byte, formed into data bus words using the algorithm defined by the format code in the tape control register, and transmitted to the RH70 controller. In addition, this op code suppresses reception of the Massbus WCLK signal. Thus, an attempt to perform a write operation with this op code in the maintenance register will result in detection of a drive timing error (DTE).

Table 3-16 (Cont)
Maintenance Register Bit Assignments

Bit	Set By/Cleared By	Remarks
4–1 (Cont)		h. 0111 – Cripple Reception of OCC An attempt to perform any data transfer operation with this op code in the maintenance register will result in detection of DTE. i. 1000 – In NRZI mode, this op code suppresses initialization of the CRC checking logic, resulting in CRC errors. In PE mode, this op code suppresses detection of data in logical track 1. j. 1001 – This op code causes bit 5 of tape data bytes to remain in the asserted state. In PE mode, this op code suppresses detection of data in logical tracks 1 and 2. k. 1010 – Maintenance Mode End of Record This op code is used to signal the end of a maintenance mode operation causing the GO bit to become negated. l. 1011 – Causes logical bit 1 of a PE preamble and postamble to be inverted during a write forward command, resulting in generation of invalid preambles and postambles.
0 MM Maintenance mode Read/write	Must be set to a 1 when any maintenance mode function is desired. Setting the MM bit to 1 does not initiate any action on the part of the drive but alters the manner in which the drive executes various commands. The manner in which the command execution is altered depends on the maintenance op code in bits 4 through 1 of this register.	

3.6.12 Drive Type (MTDT) Register (772466)

The drive type register is a 16-bit read-only register, the content of which identifies the particular type of storage device (transport) being used. Bits 0 through 8 (DT 0–8) of the drive type register identify the type and status of the selected transport. If a nonexistent transport is selected or if the selected transport is not powered up, DT 0–8 will contain 010_8. If the selected transport is powered up, but is not a TU45, DT 0–8 will contain 011_8 or 013_8 to 017_8, depending on the type of transport. If the selected transport is a TU45 and is powered up, these bit positions will contain 012_8.

Figure 3-14 shows the drive type register bit usage and Table 3-17 provides a description of each bit.

3.6.13 Serial Number (MTSN) Register (772470)

The serial number register is a 16-bit, read-only register which contains a BCD representation of the four least significant digits of the transport serial number.

Figure 3-15 shows the serial number register bit usage and Table 3-18 provides a description of each bit.

3.6.14 Tape Control (MTTC) Register (772472)

The tape control register is a 16-bit read/write register which selects an existing transport, the data format, and the density.

Figure 3-16 shows the tape control register bit usage and Table 3-19 provides a description of each bit.

3.6.15 Bus Address External (MTBAE) Register (772474)

The MTBAE register contains the upper 6 bits of the memory address and combine with the lower 16 bits located in MTBA to form the complete 22 bit address. This register should be loaded by the program in conjunction with the MTBA register to specify the starting memory address of a data transfer operation. The six bit field is incremented (decremented for specific function codes) each time a carry (borrow) occurs from the MTBA register during memory transfers.

Address bits A16 and A17 can also be set or cleared through the MTCS1 register. If an address extension field is written into MTBAE, the program should ensure that A16 and A17 are not altered when a command is loaded into MTCS1. This can be accomplished by either loading the command with a write low byte instruction to MTCS1 or by ensuring the proper value appears in the A16 and A17 bit positions of MTCS1.

Figure 3-17 shows the MTBAE register bit usage and Table 3-20 provides a description of each bit.

3.6.16 Control and Status 3 (MTCS3) Register (772476)

The MTCS3 register contains parity error information associated with the memory bus. Bit position 13 of the MTCS2, (PE) indicates that a parity error occurred during the memory transfer. Bits 15 through 13 of MTCS3 further localize the error for diagnostic maintenance. In addition, bits 3 through 0 provide the diagnostic program the ability to invert the sense of parity check and thereby verify correct operation of the parity circuits.

An Interrupt Enable bit in the MTCS3 register allows the program to enable interrupts without writing into a drive register as previously described. This bit also appears in the MTCS1 register for program compatibility and can be set or cleared by writing into either register.

Figure 3-18 shows the MTCS3 register bit usage, and Table 3-21 provides a description of each bit.

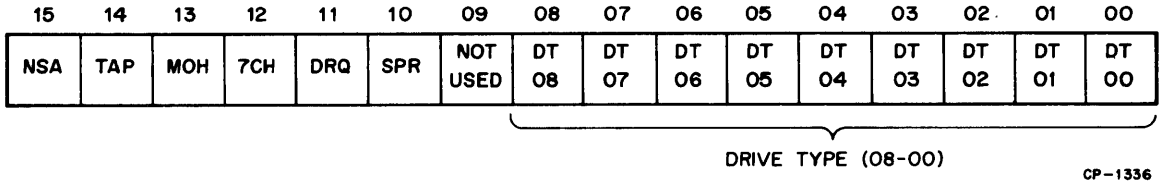


Figure 3-14 Drive Type Register Format

Table 3-17
Drive Type Register Bit Assignments

Bit	Set By/Cleared By	Remarks
15 NSA Not sector addressed Read only	Always set to indicate that the device is not sector addressable.	Neither drive clear or INIT affect this bit.
14 TAP Tape Read only	Always set to indicate that the device is a tape transport.	
13 MOH Moving head Read only	Always negated to indicate that the device is not a moving head unit.	
12 7CH 7 Channel Read only	Asserted if the selected transport is a 7-channel unit. Always negated if the selected transport is a TU45.	
11 DRQ Drive request required Read only	Always negated to indicate that the device is a single-port device.	
10 SPR Slave present Read only	Asserted when a transport is powered up and has been assigned the selection code contained in the MTTC tape control register.	
09	Not used.	
08–00 DT 08–00 Drive type Read only		Contains the drive type number for the selected slave (11_8 for the TM02/TU45). If no slave is assigned in bits 0–2 of the MTTC tape control register, the drive type code readback is 010_8. If a slave has been assigned a select code in bits 0–2 of this register, the drive type code will be a code from 11_8 to 17_8. Drive clear or INIT do not affect these bits.

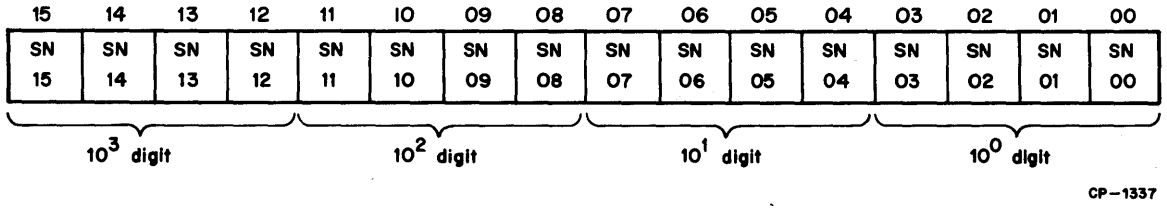


Figure 3-15 Serial Number Register Bit Usage

Table 3-18
Serial Number Register Bit Assignments

Bit	Set By/Cleared By	Remarks
15–12 SN15–SN12 Read only		Most significant BCD digit (10^3) of slave serial number.
11–08 SN11–SN08 Read only		10^2 digit of slave serial number.
07–04 SN07–SN04 Read only		10^1 digit of slave serial number.
03–00 SN03–SN00 Read only		Least significant BCD digit of slave serial number.

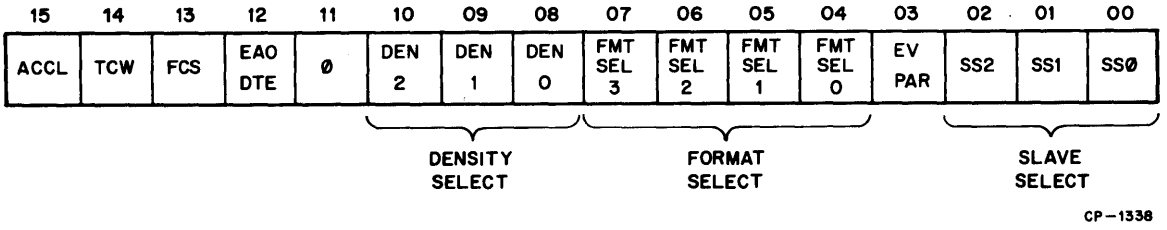


Figure 3-16 Tape Control Register Bit Usage

Table 3-19
Tape Control Register Bit Assignments

Bit	Set By/Cleared By	Remarks
15 ACCL Acceleration Read only	Set when the transport is not actively reading or writing data.	ACCL is not affected by drive clear or INIT.
14 FCS Frame count status Read only	Normally set at the end of a write into the frame count register. Cleared when frame count register overflows. Cleared by drive clear or INIT.	Loading a space or write command with the GO bit asserted and FCS equal to 0 will cause a non-executable function (NEF-bit 11 of drive status register) to be asserted and will cause the command to be aborted. No tape motion will occur.
13 TCW Tape control write Read only	Set when a control bus write operation to the tape control register is performed. Cleared by the initiation of any command requiring tape motion.	TCW is used by the TM02 to determine whether or not to wait for the completion of the settle down process (SDWN-bit 4 of the drive status register). If TCW is asserted, SDWN should be negated before issuing a new command to the selected slave.
12 EAODTE Enable abort on data transfer errors Read/write		This bit, when written to a 1, will cause a data transfer operation to be aborted as soon as one of the following errors is deleted: a. DPAR-bit 5 of MTER register b. COR/CRC-bit 15 of MTER register c. FMT/LRC-bit 7 of MTER register d. INC/VPE-bit 6 of MTER register
11	Not used.	
10–08 DEN2–DEN0 Density select		Specifies the tape character density during read or write operations as follows: DEN2 DEN1 DEN0 Density (bpi) 0 1 0 800 } NRZ 0 1 1 800 } 1 0 0 1600 PE 1 0 1 } Reserved 1 1 0 } 1 1 1 } Drive clear and INIT do not affect the density select bits.

Table 3-19 (Cont)
Tape Control Register Bit Assignments

Bit	Set By/Cleared By	Remarks
07–04 FMT SEL 3–0 Format select Read/write		Specifies Massbus-to-tape character formatting during a write operation, or tape character-to-Massbus formatting during a read operation. Data format is selected by the FMT SEL bits as follows: **FMT SEL Bit** **Mode** **3 2 1 0** 1 1 0 0 Normal mode 1 1 0 1 Core dump 1 1 1 0 15 mode If the FMT SEL bits specify a format not implemented on a TM02/TU45 system and a valid data transfer command is loaded in the MTCS1 register with the GO bit asserted, the format error bit (FMT-bit 4 of the MTER register) will be asserted and the operation will abort (Figure 1-10).
03 EV PAR Even parity Read/write		If this bit is set in NRZI mode, even parity will be written on tape and even parity is expected on read-back. If this bit is reset, odd parity will be written on tape and will be expected on read-back. When the TM02 is operating in NRZI with EV PAR set, it will not allow an all zeros character to be written on tape. If an all zeros character is presented to the TM02, the TM02 will invert binary bit 4 and the parity bit before writing the character on tape. This converts 000_8 to 020_8. This bit is ignored in phase encoded (PE) mode (DEN2=1). In PE mode, odd parity is always used.
02–00 SS2–0 Slave select Read/write		Specifies the unit number of the transport to be used. Drive clear or INIT does not affect SS2–0.

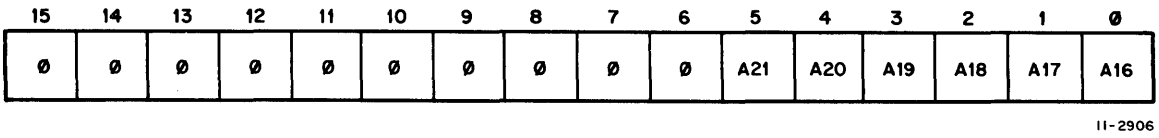


Figure 3-17 Bus Address Extension Register Format

Table 3-20
Bus Address Extension Register Bit Assignments

Bit		Set By/Cleared By	Remarks
15:06		Not Used	Always read as a 0.
05:00	A(21:16) Bus Address Read/Write	Loaded by the program to specify the starting memory address of a data transfer operation. Cleared by Unibus INIT or controller clear.	The MTBAE register is incremented (or decremented) each time a carry out (borrow out) of MTBA occurs. A16 and A17 can also be set or cleared through the MTCS1 register.

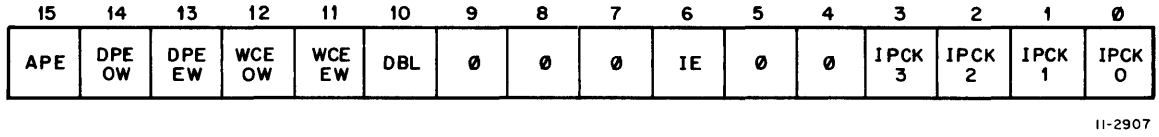


Figure 3-18 Control and Status 3 Register Format

3.7 PROGRAMMING EXAMPLES

The TWU45 tape system allows the software to monitor the status of all transports at all times (via SSC) and to monitor the readiness of all drives to receive new commands (via ATA bits). This, however, is a programmer's option. Actually there are four ways to program the TWU45 system.

Dedicated Processor – In this mode the interrupt enable bit (IE) is never set and the processor must check status on the RH70 controller, TM02 tape controller and the TU45 transport before initiating each command. The program must loop on RDY and DRY to establish when the job is done. This method is impractical in a sophisticated programming environment since it requires a dedicated CPU.

Device-Interactive with Unmonitored Status – In this method the programmer assumes the correct status exists (WRL, MOL, SPR, PIP) and issues a command without first checking status. If the wrong status exists, the command will abort and the system must have the facility to cause error correction through the error handler. This method has two disadvantages: (1) the error handler must be expanded to allow the status error recovery, and (2) IE should only be set when a command is to be executed; consequently, the system does not become aware of status changes through the interrupt facility. As a result, dequeuing of requests to a multi-transport system is not normally possible without use of a real time clock (RTC) and status polling.

Table 3-21
Control and Status 3 Register Bit Assignments

Bit		Set By/Cleared By	Remarks
15	APE Address Parity Error Read only	Set if the address parity error line indicates that the memory detected a parity error on address and control information during a memory transfer. Cleared by Unibus INIT, Controller Clear, Error Clear, or loading a data transfer command with GO set.	APE causes PE, bit 13 of MTCS2. When an APE error occurs the MTBA and MTBAE registers contain the address +4 of the double word address at which the error occurred during a double word operation or the address +2 during a single word operation.
14, 13	DPE, OW, EW Data Parity Error Odd Word, Even Word Read only	Set if a parity error is detected on data from memory when the RH70 is performing a Write or Write Check command. Cleared by Unibus INIT, Controller Clear, Error Clear, or loading a data transfer command with GO set.	DPE causes PE, bit 13 of MTCS2. When a DPE error occurs, the MTBA and MTBAE register contain the address +4 of the double word address at which the error occurred during a double word operation or the address +2 during a single word operation.
12, 11	WCE OW, EW Write Check Error Odd Word, Even Word Read only	Set when data fails to compare between memory and the drive. Cleared by Unibus INIT, Controller Clear, Error Clear, or loading a data transfer command with GO set.	Causes WCE, bit 14 of MTCS2. The word read from the drive which did not compare is locked in the data buffer and can be examined by reading the MTDB register.
10	DBL DouBLe word Read only	Set if the last memory transfer was a double word operation. Cleared by Unibus INIT, Controller Clear or loading a data transfer command with GO set.	
9–7	Not Used	Always read as a 0.	
6	IE Interrupt Enable Read/write	IE is a control bit which can be set under program control. When IE = 1, an interrupt may occur due to RDY or SC being asserted. Cleared by Unibus INIT, Controller Clear, or automatically cleared when an interrupt is recognized by the CPU. When a 0 is written into IE by the program, any pending interrupts are cancelled.	This bit can be set or cleared by writing into MTCS1 register. If written through MTCS3 register, a register write operation is not performed into a drive register simultaneously.
5–4	Not Used	Always read as a 0.	

Table 3-21 (Cont)
Control and Status 3 Register Bit Assignments

Bit	Set By/Cleared By	Remarks
3–0 IPCK (3:0) Invert Parity Check (3:0) Read/write	These bits are written by the program to control the data parity detection logic. When set inverse parity is checked with data during memory transfers of Write and Write Check operations.	Parity control is provided for each byte in double word addresses, i.e., IPCK 0 – Even Word, Even Byte IPCK 1 – Even Word, Odd Byte IPCK 2 – Odd Word, Even Byte IPCK 3 – Odd Word, Odd Byte During maintenance operation of the MTDB data buffer, if IPCK 0 or IPCK 1 is set when the first word is written into the MTDB, that data word (containing bad parity) will sequence through the data buffer and when it reaches OBUF, the parity checkers (controlled by the PAT bit) will detect the bad parity as an MDPE error. Note if both IPCK 0 and IPCK 1 are set, no bad parity will be generated. The same explanation applies for IPCK 2 and IPCK 3 which are associated with the alternate data word (i.e., the second data word loaded in the data buffer).

Device-Interactive with Monitored Status – In this method, the software checks the status previous to issuance of a command. The disadvantage is that IE should only be set during command execution and "multi-transport" dequeuing is not possible without use of a real time clock and polling of slave status.

Monitored Status via Interrupt Facility – In this method, IE is always set except while actually servicing an interrupt. Because the system is always monitoring "slave-status changes" and "attention active" on all TU45 and TM02s, dequeuing may occur as soon as the device becomes ready.

NOTE

This method is capable of controlling multi-drives and multi-transports simultaneously. In the other three modes, if dequeuing is to be done it must be done via the "system clock" facility, and the RH70, TM02, and TU45 must all be assigned to the user.

The following paragraphs show several typical programming examples. These are write, read, space, and tape mark operations.

3.7.1 Write Data Transfer

The write data transfer causes data words from memory to be transferred to the RH70 Massbus controller, then to the TM02 tape drive where they are converted into tape characters and finally to the slave transport where they are written on tape. A typical sequence of steps necessary to initiate a write data transfer is enumerated below. It is assumed that this is the first record to be written on tape. As a result, additional steps are required that would not be necessary when writing subsequent records.

1. Issue an RH70 clear by setting bit 5 in the MTCS2 register in the RH70. (First time only error bits should be cleared by the error handler and ATA bits by the interrupt handler).

2. Select a TM02 tape drive by writing bits 0 through 2 of the MTCS2 status register in the RH70.

3. Read the MTDT drive type register in the TM02 to see what type of drive is specified. In this case, bit 14 (TAP) should be set indicating a tape drive.

4. Read bit 12 (non-existent drive) of the MTCS2 status register to see if the drive that was addressed is an actual drive.

5. Read the following bits in the MTDT drive type register.

   Bit 10 (SPR) – This bit is set if the slave specified in bits 0 through 2 of the MTTC tape control register is powered up and properly assigned.
   Bits 0 through 7 – These bits specify the drive type and are designated 012_8 for the TU45 slave transports.

6. Read the following bits in the MTDS drive status register.

   Bit 12 (MOL) – If the medium on-line bit is set, the drive is powered up and ready to go.
   Bit 11 (WRL) – If the write locked bit is set, the write operation is inhibited and it is necessary to insert the write enable ring.
   Bit 07 (DRY) – If this bit is set, it indicates that the drive has concluded a previous operation (if one was specified) and is prepared to accept or send data.
   Bit 01 (BOT) – This bit is set if the tape is at the BOT.

NOTE

If the tape is not at BOT, issue a rewind command. However, the DRY bit must be set. To issue the rewind command, load a function code of 07_8 (GO bit asserted) into the MTCS1 control register. The DRY bit will temporarily be negated and will be reasserted as soon as the rewind function is transmitted to the slave. This allows the drive to accept another command before completion of the rewind.

7. Examine the MTER register for errors. If the error is a TM02/TU45 error, a drive clear should be issued which clears only the selected drive. The drive clear is issued by loading a 11_8 function code in the MTCS1 control register with the GO bit asserted. If the error is an RH70 error, an INIT should be issued. The INIT is issued by setting bit 5 (CLR) in the MTCS1 register.

8. When rewind is completed, the slave will assert SSC which will cause the TM02 to raise ATTN on the Massbus. In addition, the PIP bit will be negated and BOT asserted. The clear can be accomplished by performing a drive clear to the TM02.

9. Read the MTDS drive status register and monitor the following bits.

   Bit 15 (ATA) – This bit will set immediately (if DRY is set) to indicate status change (completion of the rewind operation). If DRY is negated, ATA will be asserted as soon as DRY is asserted.
   Bit 14 (ERR) – If this bit is set, it indicates an error condition that can be determined by reading the MTER error register. At this point, the software should enter the error recovery procedure.
   Bit 6 (SSC) – This bit will be set indicating completion of the rewind operation.
   Bit 1 (BOT) – This bit is set since the selected slave detects the BOT marker when the rewind is completed.

10. Select the format, density and type of parity by writing the MTTC tape control register in the TM02. The format is written into bits 4 through 7 of the MTTC register (Paragraph 1.7.1).

The density is selected by writing bits 8 through 10 in the MTTC register and is described in Paragraph 3.6.14. The parity can be specified even or odd for NRZI operation by writing bit 3 of the MTTC register. If this bit is set, even parity is read or written from tape. Odd parity is always performed during PE operation.

11. Select the starting memory address by writing the MTBA bus address register in the RH70.

12. Select the number of 16-bit data words to be transferred by writing the MTWC word count register in the RH70 with the two's complement of the number of words to be transferred.

13. Load the MTFC frame count register in the TM02 with twice the word count for normal format and with four times the word count for core dump format. For normal format, two tape characters are generated for each 16-bit word, and, for core dump, four tape characters are generated for each 16-bit word.

14. Load the MTCS1 register in the TM02 with the write function code (GO bit asserted) of 61_8. If the interrupt facility is employed, set the IE bit (bit 6 of the MTCS1 register in the RH70).

15. Read bit 4 (IDB) of the MTDS drive status register. Upon completion of writing the record, this bit should be set if PE density is selected and should be cleared if NRZI density is selected.

This procedure will cause one record to be written on tape. If it is desired to write another record, it is merely necessary to reload the MTBA bus address register, the MTWC word count register, and the MTFC frame count register. Then the data transfer can be implemented by loading the MTCS1 register with the 61_8 write function code (GO bit asserted).

3.7.2 Read Data Transfer

In order to do a read data transfer, a similar operation to that just described is followed with the exceptions listed below.

1. It is not necessary to write the MTFC frame count register, as this is automatically cleared for a read data transfer.

2. The read function code of 71_8 (with GO bit asserted) is loaded in the MTCS1 register instead of the write function code.

   If it is desired to do a read reverse operation, the MTBA bus address register should be loaded with the start of the buffer plus the size of the record since the RH70 decrements the bus address in a read reverse whereas it increments the bus address in a read forward operation.

3.7.3 Space Operation

When a space operation is desired, the software must specify the spacing length by loading the MTFC frame count register with the two's complement of the number of records it is desired to space.

A space operation will terminate either due to frame count overflow (desired records are spaced over) or when BOT, EOT, or TM (tape mark) is detected (signifying the end of the file). The space operation allows random access of any record within any file on tape.

3.7.4 Tape Mark Operation

To perform a write tape mark operation (to indicate the end of file for example), it is merely necessary to load a 27_8 function code (with GO bit asserted) into the MTCS1 control register. This can be monitored by reading bit 2 (TM) of the MTDS drive status register. When the bit is set, the tape mark is detected.

Tape marks can be used to indicate logical end of tape. A single tape mark indicates termination of the previous file while two tape marks indicate the logical end of tape (no more data has been written).

3.8 SUGGESTED ERROR RECOVERY

Table 3-22 gives the suggested procedures for recovering from drive or controller errors. The numbers in the column titled "Recovery Procedure" are keyed to the following steps:

1. If *not* programmer or operator error, then this condition is fatal. Disconnect from drive, report error to operator.

2. Tape position is lost, three possible recovery procedures are indicated.

   a. If physical position of desired record is known, Rewind, Space Forward to desired record and retry.

b. If each record contains an identifiable label (or sequence number), Read FWD and/or Read REV commands may be used to re-establish tape position.

c. If neither alternatives a or b are possible or practical, consider error fatal.

3. Step

a. Read Reverse

b. Read Forward

c. Repeat steps a and b until successful or re-try count overflows (suggest 20 re-tries)

d. If re-try count overflows, report to operator

4. Step

a. Back-space

b. Erase

c. Re-write record

d. Repeat steps a, b, and c until successful or re-try count overflows (suggest 20 re-tries)

e. If re-try count overflows, report error to operator

5. Report failure to operator

NOTE

The error classes are:

Class A: EXC is asserted immediately but transfer to the end of the current sector is completed and normal EBL is asserted.

Class B: EBL and EXC are asserted immediately. Data transfer stops.

The numbers in the "Possible Operator Error" column are keyed to the following steps:

Possible Operator Errors

1. Wrong unit number (plastic button) plugged into TM02.

2. Dirty read/write heads or tape path (operator PM). Also could be bad tape.

3. Operator did not insert rubber write-ring before mounting tape which was to be written on.

4. Wrong unit number (plastic button) plugged into TU45, or tape not loaded with vacuum on.

   Operator did not load tape to BOT, program initiated a rewind, and tape unloaded. Power was removed from TU45.

Table 3-22
Error Recovery Procedures

MTER Bit Position	Name	Description	Type	Recovery Procedure	Bad Data Transferred	Tape Position Lost	Possible Operator Error	Possible Programmer Error
00	Illegal Function (ILF)	Indicates that an illegal function code has been transmitted.	Class B	1	No	No	1	Program is selecting function code not implemented on TWU45.
01	Illegal Register (ILR)	Indicates that a read or write from a nonexistent register is attempted.	Class A	1	No	No	1	Program is selecting a register which does not exist on TM02.
02	Register Modification Refuse (RMR)	Indicates that while a transport operation is in progress (GO = 1), a write into one of the registers is attempted. (Does not apply for the Maintenance or Attention Summary registers.)	Class A	1	No	No	None	Program did not check for DRY = 1 before writing a register (other than AS or MR).
03	Control Bus Parity (CPAR)	Indicates that incorrect control bus parity was detected during an attempt to write a TM02 register.	Class A	1	No	No	None	None if programmer is not using Maintenance register.
04	Format (FMT)	Indicates that a data transfer with an incorrect format code is attempted.	Class B	1	No	No	None	Programmer is selecting a format code which does not exist.
05	Data Bus Parity Error (DPAR)	Indicates that incorrect data bus parity has occurred during a write data transfer (i.e., bad data transferred to the TM02 and written on tape.)	Class A	1	Yes	No	None	None if programmer is not using PAT bit in RH70.
06	Incorrectable Data Error or Vertical Parity Error (INC/VPE)	During a PE data transfer operation, indicates that an incorrectable data error has occurred.	Class A	(PE READ)–3 (PE WRITE)–4	Yes	No	2	None if programmer is not using Maintenance register.
		During an NRZI data transfer operation, indicates that a vertical parity error has occurred or that data has occurred after the skew delay is over.		(NRZI READ)–3 (NRZI WRITE)–4	Yes	No	2	None if programmer is not using Maintenance register.

Table 3-22 (Cont)
Error Recovery Procedures

MTER Bit Position	Name	Description	Type	Recovery Procedure	Bad Data Transferred	Tape Position Lost	Possible Operator Error	Possible Programmer Error
07	Format Error or LRC (PEF/LRC)	During a PE data transfer operation, indicates that an incorrect preamble or postamble is detected.	Class A	(PE READ)–3 (PE WRITE)–4	Maybe[1] Yes	No	2	None if programmer is not utilizing Maintenance register.
		Indicates that the LRCC which was written on tape does not agree with the LRCC calculated on the data during a "read" command execution or during the read after write operation which happens on a "write" command execution.	Class A	(NRZI READ)–3 (NRZI WRITE)–4	Maybe[2] Yes	No	2	
08	Nonstandard Gap (NSG)	Indicates that a tape character is detected during the first half of the inter-record gap. (i.e., tape unit thought it saw end of record but detected more data after shut-down process began.)	Class A	(READ)–3 (WRITE)–4	Maybe[1] Yes	No	2	None if programmer is not utilizing Maintenance register.
09	Frame Count Error (FCE)	Indicates that either: 1) a space operation has terminated and the Frame Counter is not cleared. (This is not a hardware failure if space operation was terminated by TM, EOT, or BOT if that termination was expected.)	Class A	(SPACE)–2	No	Yes	2	Programmer loaded wrong frame count on space command.
				(WRITE)–1	Yes	No	None	Programmer loaded a word count value which was not proportional to the frame count.
		2) A write command was executed and the frame count overflowed before the word count.						
		3) A read command was executed and the end of record was detected before word count overflow.						

Table 3-22 (Cont)
Error Recovery Procedures

MTER Bit Position	Name	Description	Type	Recovery Procedure	Bad Data Transferred	Tape Position Lost	Possible Operator Error	Possible Programmer Error
10	Correctable Skew or Illegal Tape Mark (CS/ITM)	During a PE data transfer operation, indicates that excessive but correctable skew is detected for read. (This condition is only a warning and does not indicate bad data.) For a write, it indicates that data of questionable quality was written and the record should be re-written.	Class A	(PE READ)–None (PE WRITE)–4	No Yes	No No	2 2	None
		In NRZI mode, indicative of illegal tape mark written on tape after a "write tape mark" command, or Read from tape after a Read or Space command.		(NRZI Read or Space), TMK expected–None	No	No	2	None
				(NRZI Read or Space) TMK not expected–5	Yes	Yes	2	Software lost track of tape position
				(NRZI Write TMK)–4	Yes	No	2	None
11	Nonexecutable Function (NEF)	Indicates one of the following:	Class B					
		1) A write operation is attempted on a write-protected transport.		5	No	No	3	Programmer did not check WRL status.
		2) A Space Reverse, Read reverse, or Write Check Reverse is attempted when the tape is at BOT.		2	No	Yes	None	Program did not keep track of tape position.
		3) The DEN2 bit in the Tape Control register does not agree with the PES status bit.		1	No	No		Program selected a transport incapable of density mode specified.
		4) A space or write operation is attempted when FCS = 0 in the Tape Control register.		1	No	No		Program is trying to write without specifying record length.
		5) An NRZI write operation is attempted with the 2s complement of a number less than 13 in the Frame Count register.		1	No	No		Program is specifying record length shorter than minimum of 13 characters.

Table 3-22 (Cont)
Error Recovery Procedures

MTER Bit Position	Name	Description	Type	Recovery Procedure	Bad Data Transferred	Tape Position Lost	Possible Operator Error	Possible Programmer Error
12	Drive Timing Error (DTE)	Indicates one of the following: 1) During a write operation, the controller did not supply a tape character to TM02 in time for it to be written.	Class B	4	Yes	No	None	None
		2) A data transfer (read/write) was attempted when the data bus of the Massbus was already occupied (i.e., transfer in progress on some other drive).		1	No	No	None	Program did not check controller "RDY" before issuing data transfer command.
13	Operation Incomplete (OPI)	1) During a read or space operation, indicates that a tape record has not been detected within 4.3 sec from command initiation. Assume that the drive is beyond valid data on the tape. 2) During a write operation, indicates that a read-after-write tape record has not been detected within 0.43 sec from command initiation. Assume write operation has failed. 3) Additional data has been detected after minimum gap length has been traversed. This condition causes a loss of tape position. 4) Rewind command initiated, tape already at BOT	Class B	2	Yes	Yes	2	None on a write operation. On a Read or Space, programmer did not keep track of tape position. On a Rewind operation, programmer did not check for BOT before issuing command.

Table 3-22 (Cont)
Error Recovery Procedures

MTER Bit Position	Name	Description	Type	Recovery Procedure	Bad Data Transferred	Tape Position Lost	Possible Operator Error	Possible Programmer Error
14	Unsafe (UNS)	Indicates one of the following: 1) A program-controlled operation is attempted on a selected transport which is not powered up, on-line, vacuum on. 2) An imminent power failure is detected (AC LO L).	Class B	1	Yes (If transfer was in progress)	Yes	4	Program did not check MOL before issuing command.
15	Correctable Data Error or CRC Error (COR/CRC)	During a PE read operation, indicates that a single dead track has occurred. (Data is corrected, this is only a warning.) PE Write questionable quality. Re-write. During an NRZI operation, indicates that the CRCC read off the tape does not match the CRCC computed from the data read off the tape.		(PE READ) None (PE WRITE) 4 (NRZI READ)–3 (NRZI WRITE)–4	No Yes Maybe[2] Yes	No	2	None

Table 3-22 (Cont)
Error Recovery Procedures

MTCS2 Bit Position	Name	Description	Type	Recovery Procedure	Bad Data Transferred	Tape Position Lost	Possible Operator Error	Possible Programmer Error
8	Massbus Data Bus Parity Error (MDPE)	Set when a parity error occurs on the Massbus data bus while doing a read or write-check operation.	Class A	1	Yes	No	None	None if programmer is not using PAT bit in RH70.
9	Missed Transfer (MXF)	Set if the drive does not respond to a data transfer command within 650 μs.	Class B	1	No (No data has been transferred)	No	None	Programmer loaded a data transfer command into a drive which has ERR set.
10	ProGram Error (PGE)	Set when the program attempts to initiate a data transfer operation while the RH70 is currently performing one.	Class A	1	No	No	None	Program did not check RDY prior to issuance of data transfer command.
11	Non-Existent Memory (NEM)	Set when the controller is performing a DMA transfer and the memory address specified in MTBA is non-existent (does not respond to MSYN within 10 μs.	Class A	1	Yes (Transfer incomplete)	No	None	Program specified memory locations (via WC & BA registers) which did not exist.
12	Non-Existent Drive (NED)	Set when the program reads or writes a drive register (CS1, DS, ER, MR, FC, DT, CK, TC, or SN) in a drive [selected by U(02:00)] which does not exist or is powered down. (The drive fails to assert TRA within 1.5 μs after assertion of DEM.)	Class A	1	No	No	1	Program attempted to read or write a drive register on a drive that did not exist.
13	Parity Error (PE)	Set if the RH70 detects bad data parity for a write or write check command or if cache notifies RH70 that memory detected a bad address or control parity on any data transfer.	Class A	1	Yes	No	None	(See CS3 register bits 15 – 13.

Table 3-22 (Cont)
Error Recovery Procedures

MTCS2 Bit Position	Name	Description	Type	Recovery Procedure	Bad Data Transferred	Tape Position Lost	Possible Operator Error	Possible Programmer Error
14	Write Check Error (WCE)	Set when the controller is performing a write-check operation and a word on the tape does not match the corresponding word in memory.	Class A	4	Yes	No	None	None
15	Data LaTe (DLT)	Set when the controller is unable to supply a data word during a write operation or accept a data word during a read or write-check operation at the time the drive demands a transfer.	Class A	WRITE–4 READ–3	Yes	No	None	
MTCS1 Bit Position	**Name**	**Description**	**Type**	**Recovery Procedure**	**Bad Data Transferred**	**Tape Position Lost**	**Possible Operator Error**	**Possible Programmer Error**
13	Massbus Control Bus Parity Error (MCPE)	Set by parity error on Massbus control bus while reading a remote register (located in the drive).	Class A	1	No	No	None	None if programmer is not using maintenance register.
14	Transfer Error (TRE)	Set by DLT or WCE or PE or NED or NEM or PGE or MXF or MDPE or a drive error during a data transfer.	See associated error bits above					

Notes: [1] If the programmer knows how many frames should have been read and the FC equals that number and there are no other errors, the data is valid.

[2] Possibility exists that CRCC character is in error so if software checksum tallies, data is valid.

CHAPTER 4
TWU45 COMMAND REPERTOIRE

4.1 INTRODUCTION

This chapter contains a description of the TWU45 commands and provides a flow diagram of each command showing the interaction between the RH70 Massbus Controller and the TU45/TM02 Tape System.

4.2 REWIND

A program-controlled rewind operation may be initiated by one of two commands from the processor. One of these commands (07_8) performs the rewind operation and retains the transport on-line. The other command (03_8) places the transport off-line immediately after command initiation. Following completion of the 03_8 command, the operator must reload tape and return it to the on-line status.

To initiate a program-controlled rewind operation, the address of the desired TM02 is placed on the Drive Select lines of the Massbus via the MTCS2 Control and Status 2 Register in the RH70 (see Figure 4-1). The RH70 then performs a register write into the MTTC Tape Control register, selecting the slave TU45 desired to perform the rewind operation. The TM02 places the Slave Select bits of the Tape Control register on the slave bus. The RH70. Massbus Controller then writes the operational function code of the rewind command (03_8 or 07_8) into the MTCS1 Control and Status 1 register. The TM02 decodes the function code and asserts RWND L on the slave bus. (If a rewind/off-line operation has been specified, the TM02 also asserts WRITE L.) It then checks for errors, and, if there are none, initiates tape motion. The TM02 asserts DRY (drive ready) which, in turn, asserts ATA and PIP (bit 13 MTDS register). If the Interrupt Enable (IE-bit 6 of MTCS1 register) bit is set in the RH70, the ATTN will cause the RH70 to interrupt the CPU.

The TU45, enabled by its address code on the Slave Select lines (SS 0–2), activates the capstan drive for a high-speed (250 in./sec) rewind operation. The TU45 completes the rewind operation independently, and the Massbus Controller and TM02 may divert attention to other transports.

When the reflective beginning-of-tape (BOT) marker is detected, the TU45 terminates its high-speed reverse motion, but will overshoot the BOT marker. The TU45 then initiates forward tape motion at read/write speed (75 in./sec). When it encounters the BOT marker again, the capstan motor is deactivated. When the TU45 has completed its rewind operation, it asserts SET SSC (Slave Status Change) on the slave bus and clears PIP. This causes the Attention bit in the TM02 to be set, which results in ATTN H being asserted on the Massbus thereby notifying the Massbus Controller. If the Interrupt Enable (IE-bit 6 of MTCS1) bit is set, the RH70 will interrupt the CPU.

4.3 SPACE

To initiate a space operation, the address of the desired TM02 is placed on the Drive Select lines of the Massbus via the MTCS2 Control and Status 2 Register in the RH70 (see Figure 4-2). The RH70 then performs a register write into the MTTC Tape Control register selecting the slave TU45 desired to perform the space operation. The TM02 places the Slave Select bits of the Tape Control register on the slave bus.

The RH70 Massbus Controller then loads the 2s complement of the number of tape records to be spaced into the TM02 Frame Count register. Following this, the RH70 loads the MTCS1 Control and Status 1 register with the operational function code of the space command (31 for space forward, 33 for space reverse). The TM02 decodes the function code and asserts FWD L or REV L on the slave bus. It then checks for errors and, if there are none, initiates tape motion.

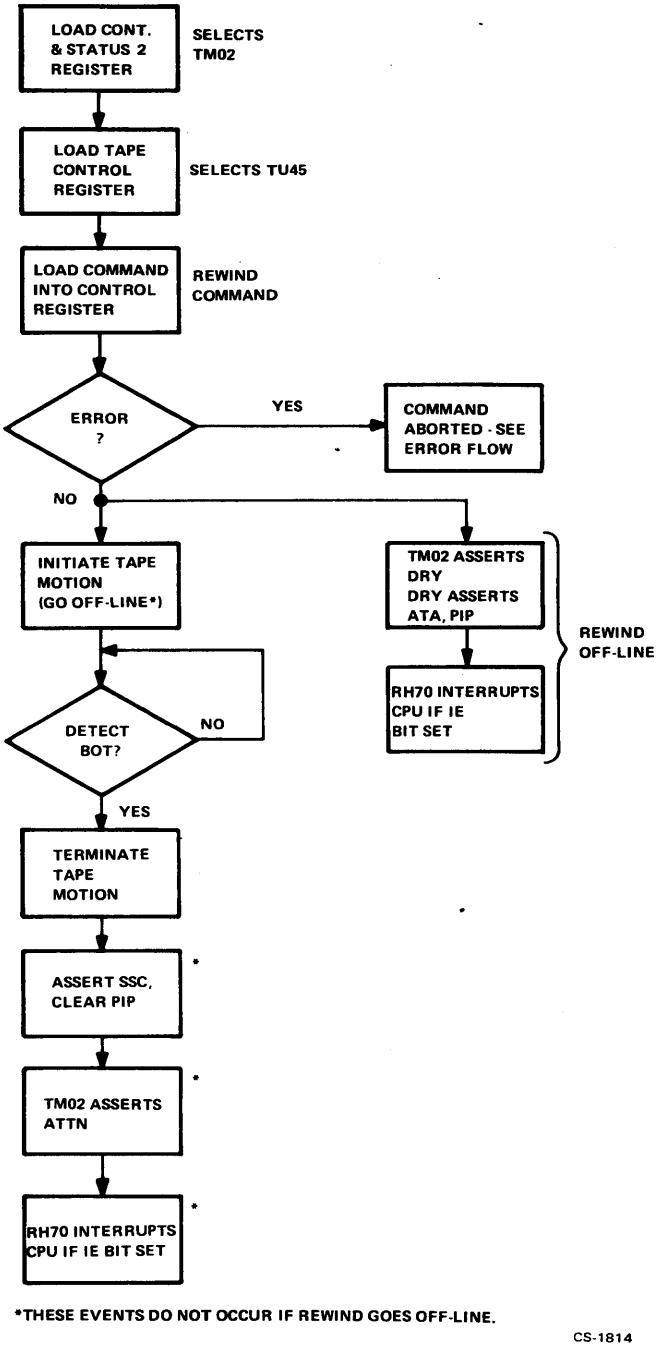


Figure 4-1 Rewind Operation Flowchart

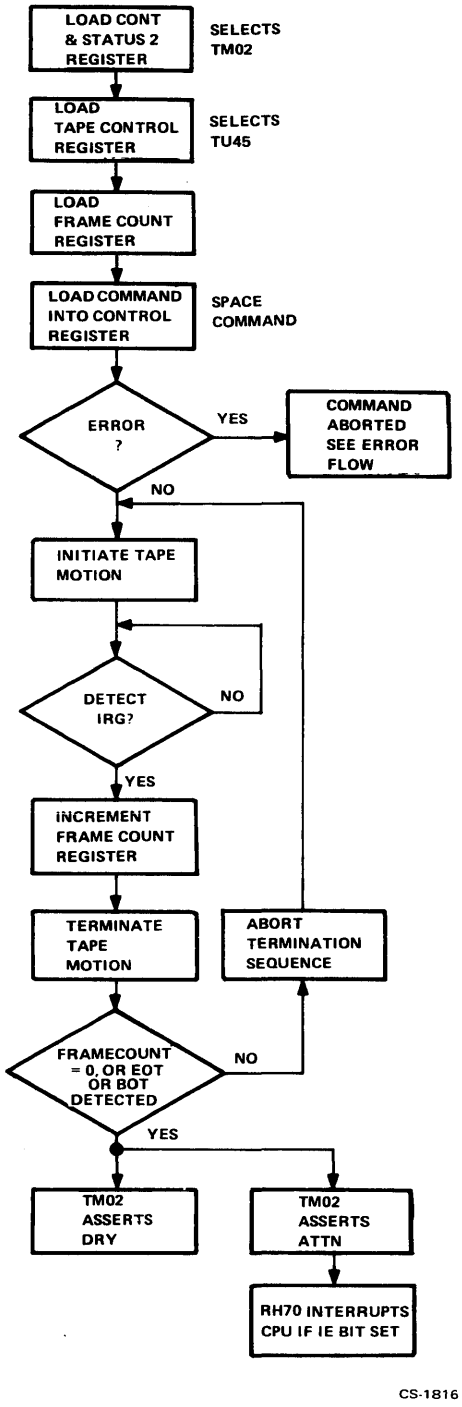


Figure 4-2 Space Operation Flowchart

If end-of-tape (EOT), beginning-of-tape, or tape mark is detected, tape motion is terminated. If not, spacing continues until the interrecord gap (IRG) is reached. This causes the MTFC Frame Count register to increment and a motion delay to occur which terminates tape motion. If the frame count is not equal to zero, or EOT or BOT is not detected, tape motion is initiated again until an interrecord gap is detected again which reincrements the Frame Count register. This sequence continues until the Frame Count register is equal to zero or until EOT or BOT is detected indicating that the desired number of records has been spaced over. The space operation is performed at a constant speed of 75 in./sec.

When frame count overflow, or EOT or BOT is detected, the TM02 asserts DRY indicating completion of the operation by the drive. The TM02 also asserts ATTN to the RH70. If the Interrupt Enable (IE-bit 6 of MTCS1) is set, the RH70 will interrupt the CPU.

4.4 ERASE

To initiate an erase operation, the address of the desired TM02 is placed on the Drive Select lines of the Massbus via the MTCS2 Control and Status 2 Register in the RH70 (see Figure 4-3). The RH70 then performs a register write into the MTTC Tape Control register selecting the slave TU45 desired to perform the erase operation. The TM02 places the slave select bits on the Tape Control register on the slave bus. The RH70 then loads the MTCS1 Control and Status 1 register with the operational function code (25_8) of the erase command. The TM02 decodes the function code and asserts FWD L and WRITE L on the slave bus. It then checks for errors, and, if there are none, causes the TU45 to energize the write and erase heads and initiates tape motion.

The TU45, which is enabled by its address code on the Slave Select lines, responds to SLAVE SET Pulse by activating the capstan drive (starting forward tape motion) and by activating the write and erase heads.

Since the erase head is activated and the write heads receive no data input during an erase operation, all the tape moving past the erase head will be dc erased.

The erase operation is terminated by the TM02 asserting STOP L on the slave bus which deactivates the capstan motor in the TU45. When tape motion has ceased, the write and erase heads are deenergized. The TM02 asserts DRY indicating completion of the operation by the drive. The TM02 also asserts ATTN to the RH70. If the Interrupt Enable (IE-bit 6 of MTCS1) bit is set, the RH70 will interrupt the CPU.

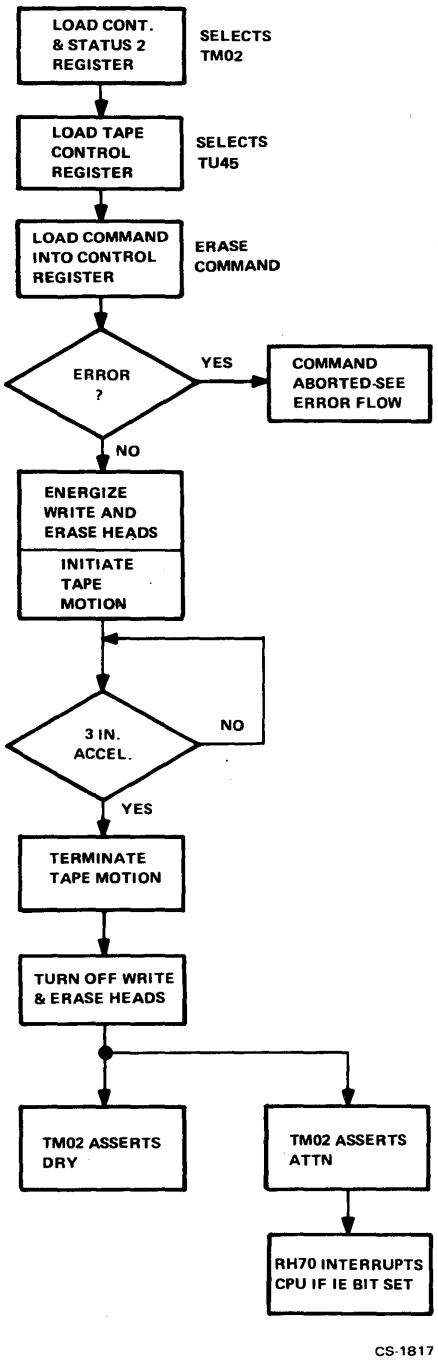


Figure 4-3 Erase Operation Flowchart

4.5 PE DATA READ

To initiate PE read operation, the address of the desired TM02 is placed on the Drive Select lines of the Massbus via the MTCS2 Control and Status 2 register in the RH70 (see Figure 4-4). The RH70 then performs a register write into the MTTC Tape Control register specifying the selected TU45 slave, tape character format, and tape density (1600 bpi for PE).

The TM02 places the slave selects (SS 0–2) and density (DEN 0–2) bits of the Tape Control register on the slave bus. The RH70 then loads the MTCS1 Control and Status 1 register with the operational function code of a read operation (71_8 read forward, 77 read reverse, 51 write check forward, or 57 write check reverse) and asserts RUN on the Massbus. The TM02 decodes the function code and asserts FWD L or REV L on the slave bus. It then checks for errors, and, if there are none, asserts OCC on the Massbus to notify the controller and other drives that it is occupying the data bus of the Massbus. The TM02 then transmits SLAVE SET Pulse to the TU45.

The TU45, which is enabled by its address code on the Slave Select lines (SS 0–2) of the slave bus, responds to SLAVE SET Pulse by activating the capstan drive motor and initiating tape motion.

The TU45 read amplifiers are on continuously. Even as the tape accelerates, the TM02 PE read circuitry checks for a PE identification burst (IDB) and begins looking for a preamble. When the tape is at speed, the preamble will be detected and read; the tape characters immediately after the preamble all-1s character are data characters.

The characters are assembled into 18-bit words and placed on the data bus of the Massbus. This action continues until the first character of the postamble is detected.

The TM02 reads the postamble which signifies the end of the record and asserts EBL H (end-of-block) on the Massbus. When the gap has been detected, the TM02 terminates tape motion, asserts DRY, and negates EBL. The negation of EBL causes the RH70 to go to the RDY (Ready) state causing the RH70 to interrupt the CPU if the Interrupt Enable (IE-bit 6 of MTCS1) bit is set.

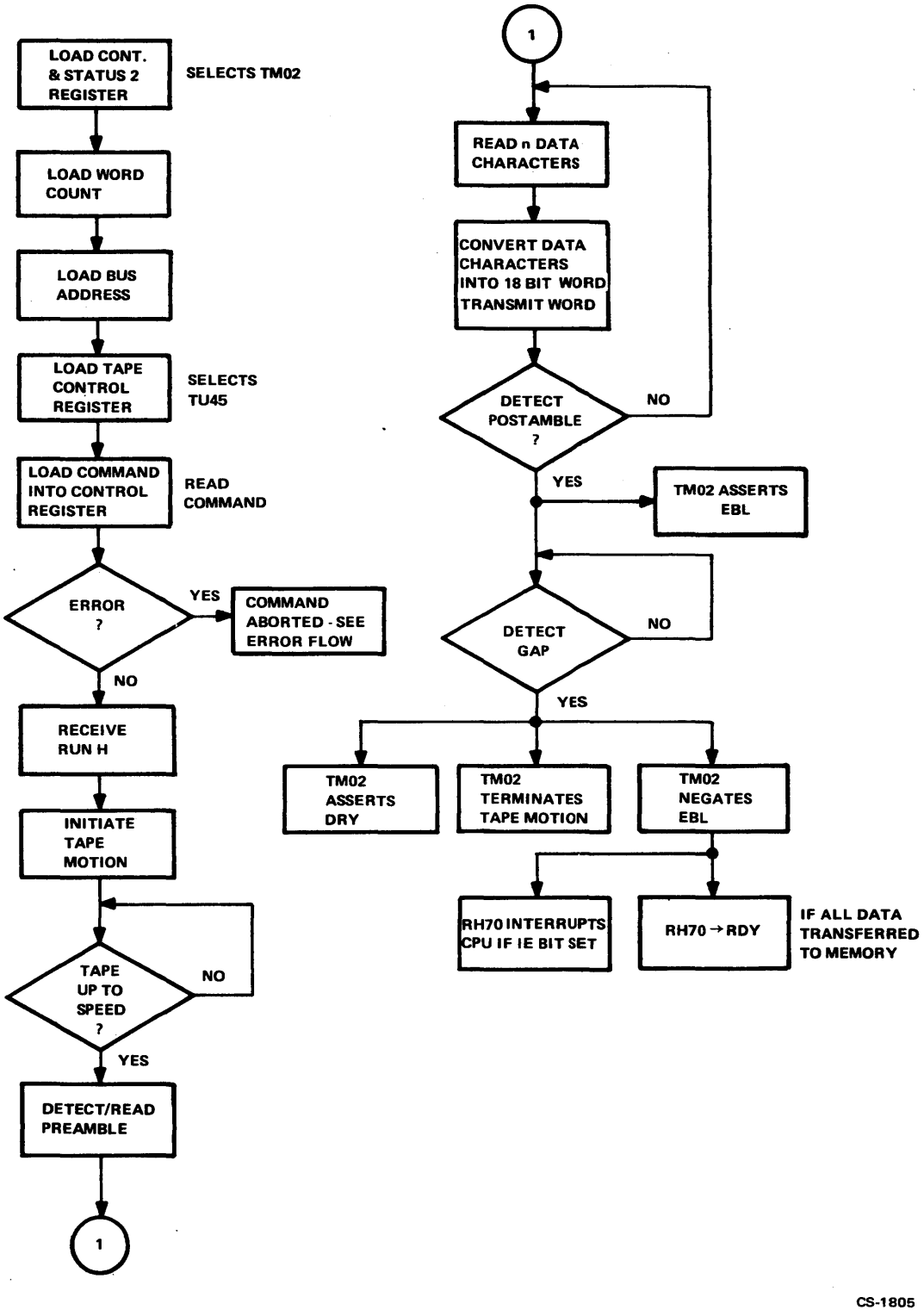


Figure 4-4 PE Data Read Operation Flowchart

4.6 NRZI DATA READ

To initiate an NRZI read operation, the address of the desired TM02 is placed on the Drive Select lines of the Massbus via the MTCS2 Control and Status 2 register in the RH70 (see Figure 4-5). The RH70 then performs a register write into the MTTC Tape Control register, specifying selected slave TU45, tape character format, and tape data density. The TM02 places the slave select (SS 0–2) and density (DEN 0–2) bits of the Tape Control register on the slave bus. The RH70 then loads the MTCS1 Control and Status 1 register with the operational function code of a read operation (71_8 read forward, 77 read reverse, 51 write check forward, or 57 write check reverse) and asserts RUN H on the Massbus. The TM02 decodes the function code and asserts FWD L or REV L on the slave bus. The TM02 then checks for errors, and, if there are none, asserts OCC on the Massbus to notify the controller and other drives that it is occupying the data bus of the Massbus. The TM02 then transmits SLAVE SET Pulse to the TU45. The TU45, which is enabled by its address code on the Slave Select lines (SS 0–2) of the slave bus, responds to SLAVE SET Pulse by activating the capstan drive motor and initiating tape motion.

When a tape character is detected by the TU45, it is multiplexed onto the slave bus Read Data lines and is strobed into the TM02. LRCC and CRCC are generated from the data and will be used to check the validity of the data read.

The TM02 assembles the characters into 18-bit data words and places them on the data bus of the Massbus. When a data word is assembled by the TM02, the TM02 notifies the RH70 which strobes the word from the data bus. The assembling of data characters into 18-bit words continues until the end of the data record as represented by an all-0s tape character.

During a forward read, the rest of the read circuitry continues its operation, reading the CRCC and strobing it into the Check Character register, and then reading the LRCC. Discrepancies between generated CRCC/LRCC and detected CRCC/LRCC cause their respective error bits to be set.

During a reverse read, the LRCC character is encountered first at the start of the read operation, but is ignored. The CRCC is encountered next, and strobed into the Check Character register, but otherwise it is ignored. No CRC or LRC error is generated. Then the data is read; assembly of characters into data words may differ when reading in the reverse direction, but this depends on the data format selected.

When the data and LRCC/CRCC have been read, the TM02 asserts EBL. When the interrecord gap is detected, the TM02 asserts DRY, terminates tape motion, and negates EBL. The negation of EBL causes the RH70 to go to the RDY (Ready) state and will cause the RH70 to interrupt the CPU if the Interrupt Enable (IE-bit 6 of MTCS1) bit is set.

4.7 PE DATA WRITE

To initiate a PE write operation, the address of the desired TM02 is placed on the Drive Select lines of the Massbus via the MTCS2 Control and Status 2 register in the RH70 (see Figure 4-6). The RH70 then performs a register write into the MTTC Tape Control register, specifying selected slave TU45 tape character format, and tape data density (PE – 1600 bpi). The TM02 places the slave select (SS 0–2) and density (DEN 0–2) bits of the Tape Control register on the slave bus. The RH70 then loads the 2s complement of the number of tape characters to be written into the TM02 Frame Count register. Following this, the RH70 Controller loads the MTCS1 Control and Status 1 register with the operational function code (61) of the data write command. The TM02 decodes the function code and assets FWD L and WRITE L on the slave bus. It then checks for errors, and, if there are none, asserts OCC on the Massbus to notify the controller and other drives that it is occupying the data bus of the Massbus.

When the RH70 has data available for transfer, it asserts RUN H on the Massbus. The TM02 responds by asserting SLAVE SET Pulse on the slave bus and accepting the first data word from the RH70.

The TU45, which is enabled by its address code on the Slave Select lines (SS 0–2) of the slave bus, responds to SLAVE SET by activating the capstan drive motor for forward tape motion and by turning on the write and erase heads. The first data word, loaded on the Massbus when RUN is asserted, is accepted by the TM02.

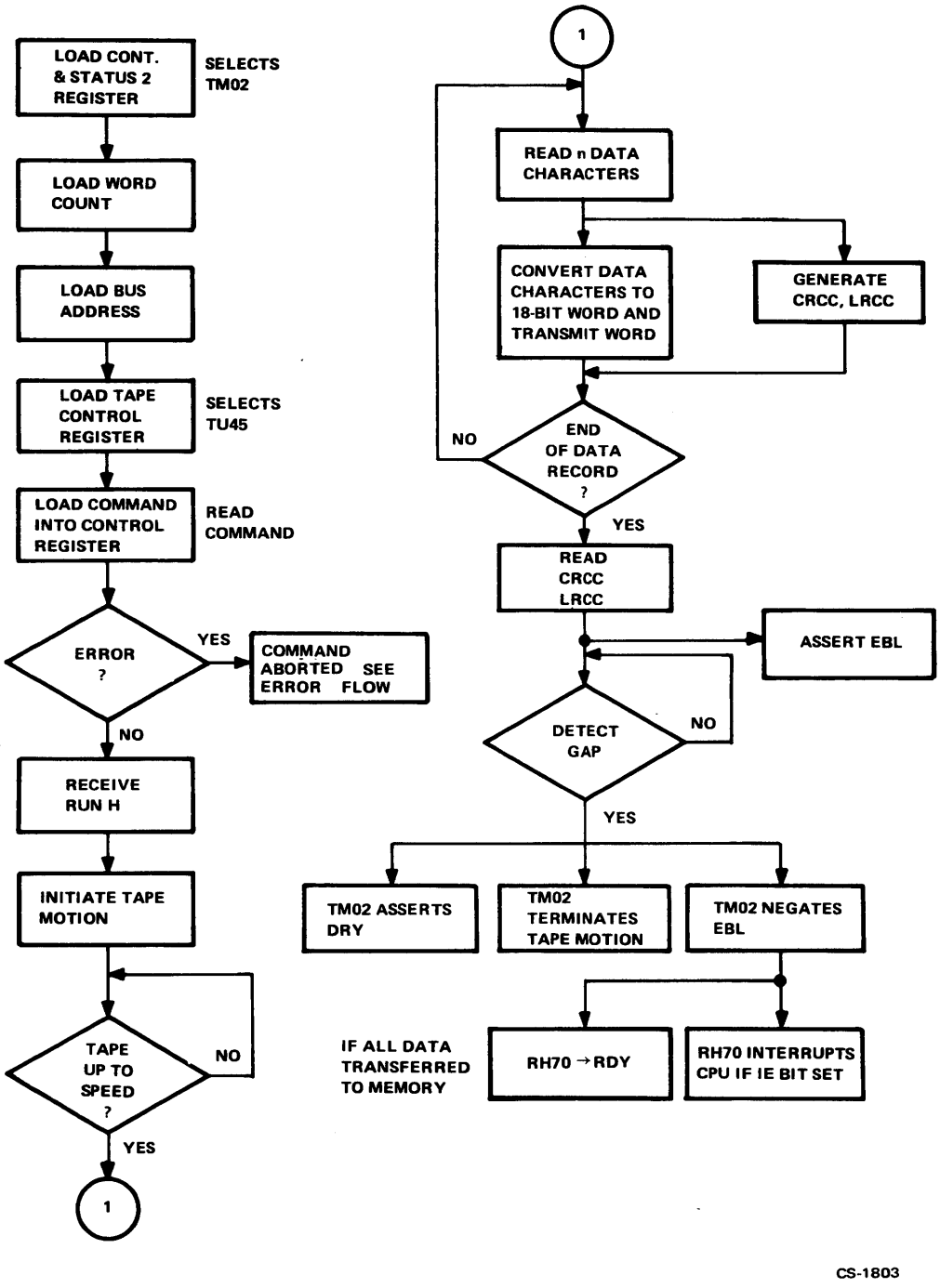


Figure 4-5 NRZI Data Read Operation Flowchart

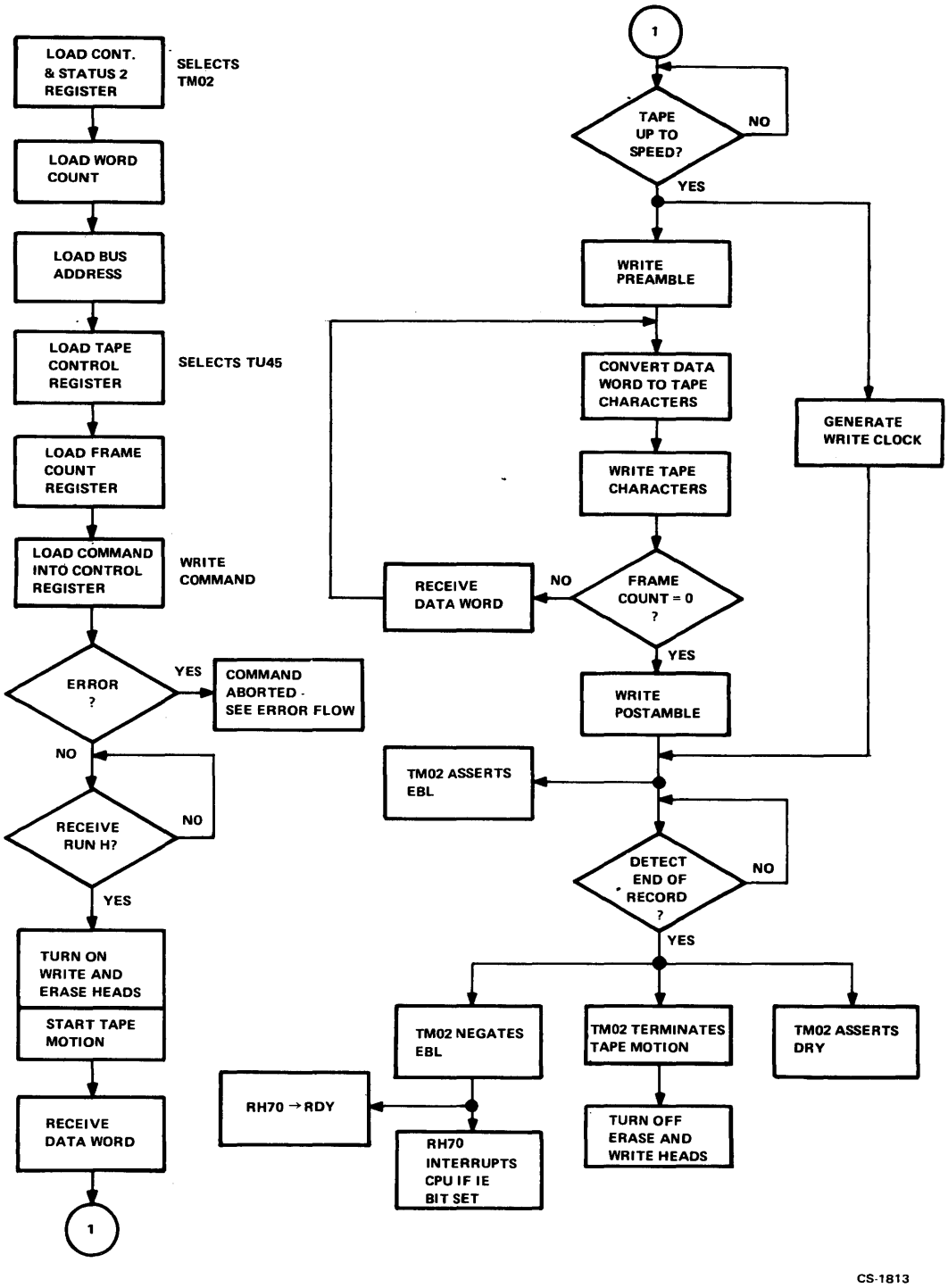


Figure 4-6 PE Data Write Operation Flowchart

When the TU45 is up to speed, it transmits a WRT CLK signal to the TM02. Upon receipt of WRT CLK, the TM02 begins generating a preamble. When forty all-0 characters and one all-1 characters have been written, the TM02 begins disassembling the first data word into characters. When it has disassembled the first data word, it requests the next data word from the RH70 Massbus Controller and continues to do so until all the data words have been transferred. Each time the TM02 generates a character, the Frame Count register is incremented, a vertical parity bit is generated, and the tape character is converted to PE mode and transmitted to the write circuitry of the TU45. When the Frame Count register overflows to zero, the TM02 generates a postamble which is written on tape and asserts EBL. During the entire operation, the TU45/TM02 read operation is active and reads the record being written.

When the TU45/TM02 read circuitry detects the end of the record, the TM02 asserts DRY, terminates tape motion, and negates EBL. The negation of EBL causes the RH70 to go to the RDY state, and causes the RH70 to interrupt the CPU if the Interrupt Enable (IE-bit 6 of MTCS1) bit is set.

4.8 NRZI DATA WRITE

To initiate an NRZI write, the address of the desired TM02 is placed on the Drive Select lines of the Massbus via the MTCS2 Control and Status 2 register in the RH70 (see Figure 4-7). The RH70 then performs a register write into the MTTC Tape Control register specifying selected slave TU45, tape character format, and tape data density. The TM02 places the slave select (SS 0–2) and density (DEN 0–2) bits of the Tape Control register on the slave bus. The RH70 then loads the 2s complement of the number of tape characters to be written into the TM02 Frame Count register. Following this, the RH70 loads the MTCS1 Control and Status 1 register with the operational function code (61) of the data write command. The TM02 decodes the function code and asserts FWD L and WRITE L on the slave bus. It then checks for errors, and, if there are none, asserts OCC on the Massbus to notify the controller and other drives that it is occupying the data bus of the Massbus.

When the controller has data available for transfer, it asserts RUN H on the Massbus. The TM02 responds by asserting SLAVE SET Pulse on the slave bus and accepting the first data word from the RH70.

The TU45, which is enabled by its address code on the Slave Select lines (SS 0–2) of the slave bus, responds to SLAVE SET by activating the capstan drive motor for forward tape motion and by activating the write and erase heads. The first data word, loaded on the Massbus when RUN is asserted, is accepted by the TM02.

When the TU45 is up to speed, it transmits a WRT CLK signal to the TM02. Upon receipt of WRT CLK, the TM02 begins disassembling the first data word into characters.

When it has disassembled the first data word, it requests the next data word from the RH70 Massbus Controller, and continues to do so until all the data words have been transferred. Each time the TM02 generates a character, the Frame Count register is incremented, a vertical parity bit is generated, the CRCC is generated, and the tape character is transmitted to the write circuitry of the TU45 where it is converted from binary to NRZI mode (1s become transitions) and written on the tape. When the Frame Count register overflows to zero, the TM02 transmits EBL (end-of-block) to the RH70. It then generates the timing to write the generated CRCC and the LRCC.

During the time that the tape is moving at speed, the TU45/TM02 performs a read-after-write operation.

When the TU45/TM02 read circuitry detects the end of a record, the TM02 asserts DRY, terminates tape motion, and negates EBL. When tape motion stops, the write and erase heads are deenergized.

The negation of EBL (end-of-block) causes the RH70 to go to the RDY (Ready) state and causes the RH70 to interrupt CPU if the Interrupt Enable (IE-bit 6 of MTCS1) is set.

4.9 WRITE TAPE MARK

To initiate a write tape mark operation, the address of the desired TM02 is placed on the Drive Select lines of the Massbus via the MTCS2 Control and Status 2 register in the RH70 (see Figure 4-8). The RH70 then performs a register write into the MTTC Tape Control Register, selecting the slave TU45 to perform the write tape mark operation and the density at which the tape mark characters are to be written. The TM02 places the slave select (SS 0–2) and density select (DEN SEL 0–3) bits of the Tape Control register on the slave bus.

The RH70 Massbus Controller then loads the MTCS1 Control and Status 1 register with the operational function code (27) of the write tape mark command. The TM02 decodes the function code and asserts FWD L and WRITE L on the slave bus. It then checks for errors, and, if there are none, issues SLAVE SET to the TU45.

The TU45, which is enabled by its address code on the Slave Select lines, responds to SLAVE SET by activating the capstan drive (starting tape motion) and by activating the write and erase heads. As tape moves past the heads, it is erased. After a 3 inch acceleration delay, the TM02 generates the tape mark.

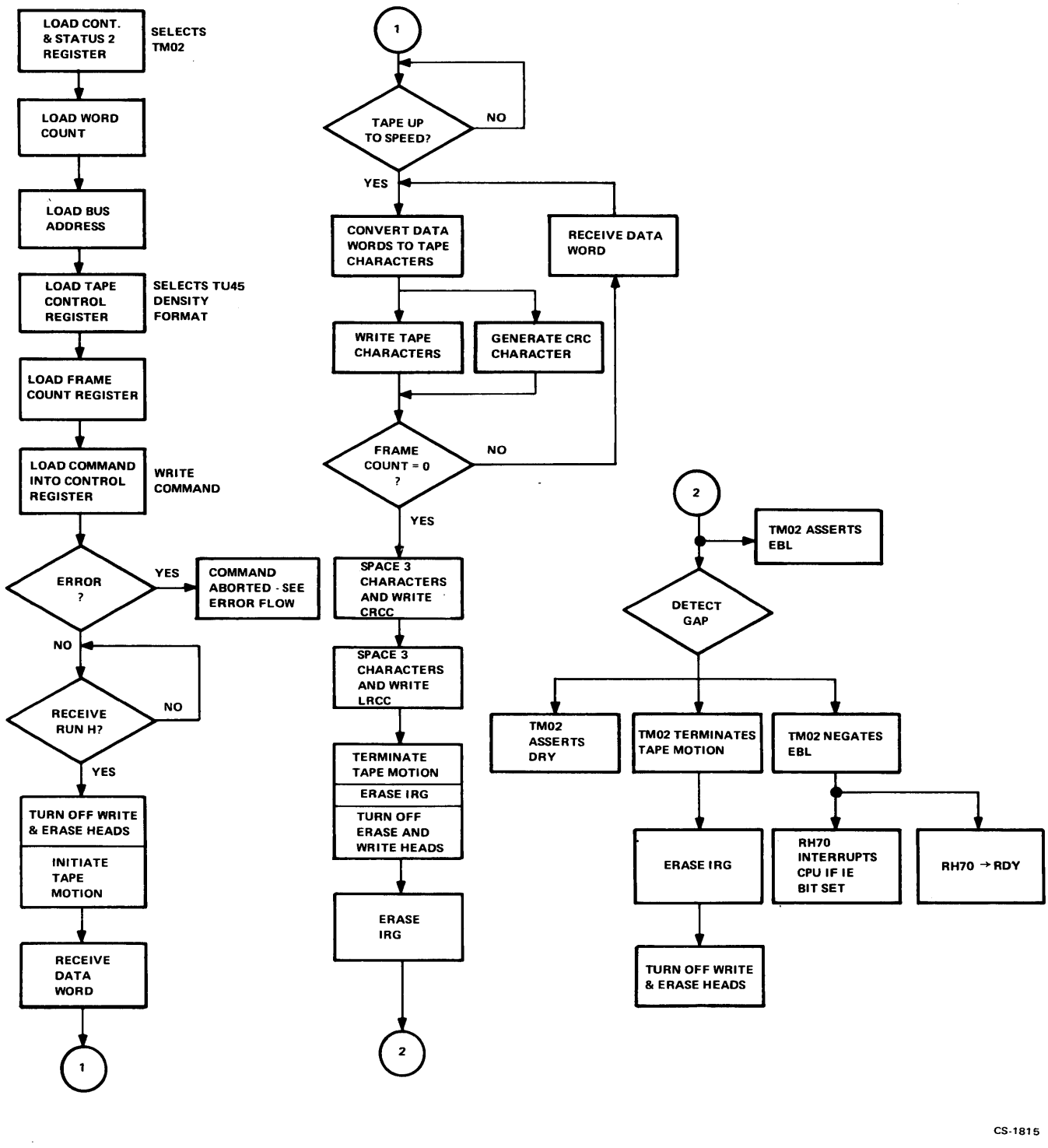


Figure 4-7 NRZI Data Write Operation Flowchart

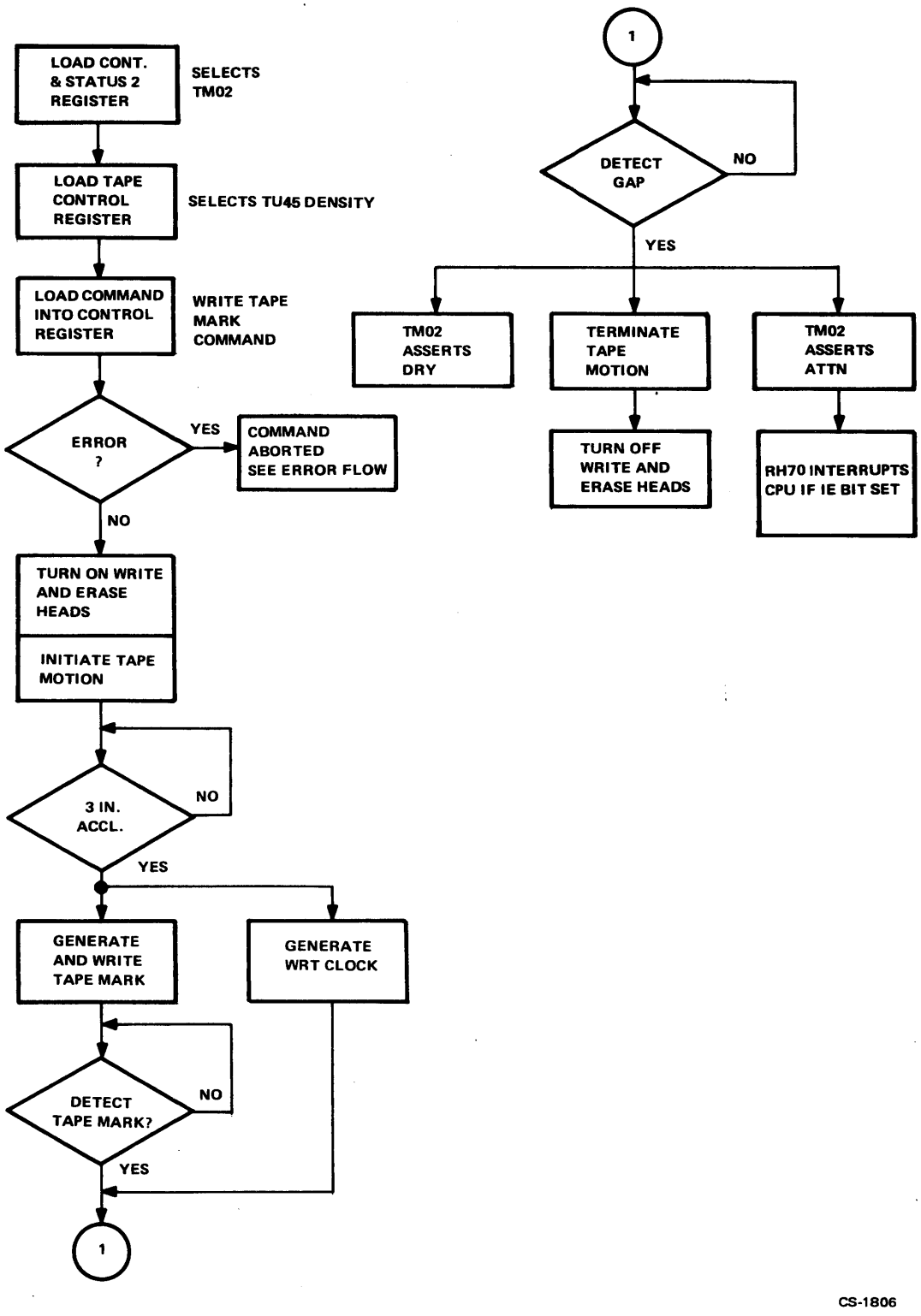


Figure 4-8 Write Tape Mark Operation Flowchart

If the TU45/TM02 is operating in PE mode, slave bus write lines WD 3, 4, 6, and 7 are forced high, while PE 0s are generated for WD 0, 1, 2, and 5. At the same time record pulses (40 X 2 = 80) are transmitted to the TU45. As a result, forty 0s are written in tracks 1, 2, 4, 5, and 8, and the remaining tracks are erased.

If the TU45/TM02 is operating in NRZI mode, the tape mark character is forced onto the slave bus WD lines, and a record pulse is transmitted to the TU45. The TU45 is then allowed to erase seven character lengths of tape at which time it receives LRC STROBE on the slave bus and writes an LRCC (which will be the same as the tape mark character).

After writing the NRZI or PE tape mark, the TU45/TM02 continues to erase tape. As the write tape mark operation is performed, the read circuitry performs a read-after-write.

After the read circuitry has detected the written tape mark, the TM02 transmits STOP L to the TU45. This signal deactivates the capstan motor to terminate tape motion. When tape motion has stopped, the write and erase heads are deenergized. The TM02 asserts DRY indicating that the drive is ready to perform another function. The TM02 also asserts ATTN to the RH70. The RH70 will interrupt the CPU if the Interrupt Enable (IE-bit 6 of MTCS1) bit is set.

4.10 ERRORS

TM02 errors may occur at command initiation or at command execution. The error handling for each type is described below.

Command Initiation – Any error that occurs when a command is initiated (GO bit asserted) will cause an immediate abort. The error will assert EXC (if it is a data transfer command) and during command initiation will also assert ATTN and EBL. The assertion of EBL and ATTN will cause the RH70 to interrupt the CPU if the IE bit is set. The assertion of EXC causes TRE in the RH70 to set. TRE is monitored in bit 14 of the MTCS1 register.

Command Execution – During the execution of a command, Class A or Class B errors may occur and are handled in the following manner.

Class A: If a class A occurs during execution of a data transfer command, EXC is raised immediately but the command will not terminate until the operation is completed. This occurs at the end of the record when ATTN and EBL are asserted. Note that EXC asserts TRE which can be monitored via bit 14 of the MTCS1 register.

Class B: If a class B error occurs during execution of a command, EXC, ATTN and EBL are raised immediately and the command is terminated. If the command is a data transfer command, EXC is also asserted which sets TRE in the RH70.

APPENDIX A
TEST TYPEOUTS

A.1 GENERAL

This appendix provides error-free typeouts for each on-line test, with the exception of the Data Reliability Program (DECSPEC-11-AYVAD).

A.2 TM02/TU45 LOGIC TEST (DECSPEC-11-AYVCD)

Error-Free Typeout

```
TM02/TU45 CONTROL LOGIC TEST (AYVCD-E)
REGISTER START: 172440
VECTOR ADDRESS: 224
NRZ ONLY: 0
STATIC TESTS ONLY: 0

FOR DRIVE ADDRESS TEST;
 ENTER EXPT DRIVE NUMBER, ALL OTHERS SHOULD BE NON-EXISTENT.
DRIVE NUMBER 0
DRIVE NUMBER

FOR SLAVE ADDRESS TEST;
 ENTER EXPT SLAVE NUMBER, ALL OTHERS SHOULD BE NON-EXISTENT.
SLAVE NUMBER 0 SN: 0001
SLAVE NUMBER

END OF PASS 0
END OF PASS 1
END OF PASS 2
END OF PASS 3
```

A.3 TU45 BASIC FUNCTION TEST (DECSPEC-11-AYVBD)

Error-Free Typeout

```
TM02/TU45 BASIC FUNCTION TEST (AYVBD-B)
ENTER CONDITIONS IN OCTAL

REGISTER START = 172440
VECTOR = 224
DRIVE NUMBER: 0
SLAVE NUMBER: 0 SERIAL NO: 0001
RH11 or RH70: 1
RH ONLY: 0
NRZ ONLY: 0
END OF PASS 0
END OF PASS 0
```

A.4 TM02/TU45 DRIVE FUNCTION TIMER (DECSPEC-11-AYVDD)

Error-Free Typeout

```
TU45 DRIVE FUNCTION TIMER (AYVDD-C)
TYPE FIRST ADDRESS OF CONTROLLER 172400
TYPE TM02 DRIVE #'S TO BE TESTED 0
FOR TM02 DRIVE 0-TYPE SLAVE #'S TO BE TESTED 00
SPEED TESTS ONLY? (YES/NO = 1/0) 0
NRZ ONLY? (YES/NO = 1/0) 0

*****************************************************************************

*  TM02 DRIVE FUNCTION TIMES – DRIVE # 0 SLAVE # 0  9 CHAN. SER #????
*
*  FUNCTION                 TIME (SPECIFICATION)        TIME (ACTUAL)
*  WRITE FROM BOT           RANGE=<076000-073000>       ACTUAL=074120
*  WRITE START              RANGE=<005740-005400>       ACTUAL=005570
*  WRITE SHUTDOWN           RANGE=<005390-005070>       ACTUAL=005230
*  WRITE SETTLEDOWN         RANGE=<006500-004500>       ACTUAL=005100
*  READ FROM BOT            RANGE=<062000-060000>       ACTUAL=060920
*  READ START               RANGE=<001700-001580>       ACTUAL=001630
*  READ SHUTDOWN            RANGE=<002730-002570>       ACTUAL=002650
*  READ SETTLEDOWN          RANGE=<006500-004500>       ACTUAL=005100
*  READ REV START           RANGE=<001700-001580>       ACTUAL=001630
*  READ REV SHUTDOWN        RANGE=<002200-001940>       ACTUAL=002100
*  READ REV SETTLEDOWN      RANGE=<006500-004500>       ACTUAL=005100
*  TURN AROUND DELAY F-R    RANGE=<008000-006000>       ACTUAL=006730
*  TURN AROUND DELAY R-F    RANGE=<008000-006000>       ACTUAL=006660
*  GAP SIZE-STOP HALF       RANGE=<009000-007800>       ACTUAL=008220
*  GAP SIZE-START HALF      RANGE=<008200-006900>       ACTUAL=007270
*  GAP SIZE-INTERRECORD     RANGE=<008890-008370>       ACTUAL=008630
*  GAP CONSISTANCY          RANGE=<008260-007780>       ACTUAL=008090
*  DATA TIME-200BPI         RANGE=<014640-013780>       ACTUAL=014210
*  DATA TIME-556BPI         RANGE=<014560-013710>       ACTUAL=014140
*  DATA TIME-800BPI         RANGE=<014560-013710>       ACTUAL=014140
*  DATA TIME-1600BPI        RANGE=<015000-013000>       ACTUAL=014820
*  ERASE GAP TIME           RANGE=<062190-058560>       ACTUAL=060380
*  WRITE FILE MARK          RANGE=<064920-061140>       ACTUAL=063030
```

A.5 TU45 DATA RELIABILITY PROGRAM (DECSPEC-11-AYVAD)

```
TU45 DATA RELIABILITY TEST (AYVAD-C)
MAKE ENTRIES IN OCTAL

REGISTER START = 172440
VECTOR ADDRESS = 224
DRIVE NUMBER = 1
SLAVE NUMBER = 6  SN:  50022
DENSITY = 3
PARITY = 0
FORMAT = 14
SLAVE NUMBER =
RECORD COUNT = 0 200
CHARACTER COUNT = 0 4000
PATTERN NUMBER = 1
TAPE MARK = 0 1
SINGLE PASS = 0

ENTER STALLS
READ = 1
WRITE = 1
TURN AROUND = 1

DRIVE NO. 0 *SLAVE NO. 0 *D 3 *P 0 *F 14 *PATRN R
*BN 1 *RN 3700 -77777 *RS 4000 EOT NO:  1
REWIND TAPE; RESTART AT BLOCK ONE
DROPS :     0  0  0  0  0  0  0  0
PICKS  :    0  0  0  0  0  0  0  0
RETRY :     0
WTERR :     0
REFWD :     0
 SOFT  :    0
 HARD :     0
DEFWD :     0
REREV :     0
 SOFT  :    0
 HARD :     0
DEREV :     0
0  BAD TAPE SPOTS
```

DIGITAL EQUIPMENT CORPORATION

MAYNARD, MASSACHUSETTS

SHIPPING LIST

ITEM NO.	DWG NO. / PART NO.	DESCRIPTION	QUANTITY VARIATION											
			TWU45-EA	TWU45-EB										
1	B-DD-TWU45-0	TWU45-EA/EB Customer Print Set	1	1										
2	Dec #ER-00016/ Pertec #104597	Pertec Operating and Service Manual	1	1										
3	CSS-MO-F-5.2-22	TM02-FE/FF Magtape System Manual	1	1										
4	CSS-MO-F-5.2-23	M.T.A. Option Description	1	1										
5	CSS-MO-F-5.2-25	TWU45 Magtape System Manual	1	1										
6	CSS-MO-F-5.2-27	RH70/Special Option Description	1	1										
7	TUC01	Tape Cleaning Kit	1	1										
8	18-09543-03	Magtape – 2400' Reel	1	1										
9	70-08288-8F	Remote Turn-On Cable	1	1										
10	DECSPEC-11-AYVAD	TU45 Data Reliability	1	1										
11	DECSPEC-11-AYVBD	Basic Function Test	1	1										
12	DECSPEC-11-AYVCD	Logic Test	1	1										
13	DECSPEC-11-AYVDD	Drive Function Timer	1	1										
14	DECSPEC-11-AYVED	Utility Driver	1	1										
15	DECSPEC-11-AYVFD	Data Create Tape	1	1										
16	12-11902	Unit Select Keys (0–7)	8	8										

TITLE	DOCUMENT NUMBER	REV.
DECMAGTAPE W/CONTROL – PDP11/70 (800/1600 BPI)	A-SH-TWU45-0-0	A

DIGITAL EQUIPMENT CORPORATION

MAYNARD, MASSACHUSETTS

SHIPPING LIST

ITEM NO.	DWG NO. / PART NO.	DESCRIPTION	QUANTITY VARIATI											
			TU45-EE	TU45-EF										
1	B-DD-TU45-0	TU45-EE/EF Customer Print Set	1	1										
2	Pertec #104597/ DEC # ER-00016	Pertec Operating and Service Manual	1	1										
3	CSS-MO-F-5.2-23	M.T.A. Option Description	1	1										
4	TUC01	Tape Cleaning Kit	1	1										
5	18-09543-03	Magtape - 2400' Reel	1	1										
6	70-08288-8F	Remote Turn-On Cable	1	1										

TITLE	DOCUMENT NUMBER	REV.
DEC MAGTAPE W/O CONTROL (800/1600) BPI	A-SH-TU45-0-0	A