K84

DATARAM

CORE MEMORY SYSTEM

DR-118A

06017 A

DATARAM CORPORATION P.O. BOX 7528 PRINCETON, NJ 08543-7528 (609) 799-0071 FAX: (609) 799-6734

Proprietary rights of DATARAM CORPORATION are involved in this subject matter and all manufacturing, reproduction, use and sales rights pertaining to such subject matter are expressly reserved. It is submitted in confidence for a specified purpose and the recipient, by accepting this material, agrees that this material will not be used, copied or reproduced in whole or in part, nor its contents revealed in any manner or to any person except to meet the purpose for which it was delivered.

TABLE OF CONTENTS

SECTION I

DESCRIPTION

1.1 General

The Dataram Corporation model DR-118A memory systems are designed to operate in Digital Equipment Corporation's PDP-8/A* computers. The memories are available in 16K and 8K word by 12 bit versions.

The DR-118A module occupies two OMNIBUS* card slots. The DR-118A memory may be operated with, or in place of, the DEC* model MM8-AA or MM8-AB memory. Note that the DR-118A can only be used in core machines such as the PDP-8/A-400 and PDP-8/A-500 which are equipped with G8018 power supply modules and dedicated core memory slots.

*Registered trademarks of Digital Equipment Corporation

SECTION II

SYSTEM SPECIFICATIONS

2.1 Capacity

The storage capacity of the DR-118A memory module is either 8,192 words or 16,384 words by 12 bits.

The PDP-8/A may be expanded to 32K by adding Dataram DR-118A modules as required, provided the DEC KM8-AA Extended Option Board (M8317) or KM8-E Memory Extension Control (M837) is present. The M8317 or M837 is supplied as standard with core PDP-8/A's.

2.2 Cycle Time

The cycle time of the DR-118A memory while installed in the PDP-8/A computer is 1500 nanoseconds for full cycle operations.

2.3 Access Time

The access time of the DR-118A memory is 300 nanoseconds or less. The access time is measured at the connector of the memory module. The time delay between the +1.5 volt levels of the source pulse and all data lines during memory Read cycles is defined as "access time".

2.4 Addressing

The DR-118A accepts a 15 bit address from the MA and EMA bus lines. Provision for expansion to 128K via the TPST signal (OMNIBUS Pin AB1) is included. The EMA lines originate on the M837 or M8317 module. The starting address for the DR-118A memory may be assigned to any of the eight 4K memory fields by wiring the 16 pin dual-in-line address plug (TB1) as follows:

16K DR-118A

Address Assignment	TB1 Pin Numbers 14	13	12	11
0-16K	1	2	3	4
4-20K	2	3	4	5
8-24K	3	4	5	6
12-28K	4	5	6	7
16-32K	5	6	7	8

8K DR-118A

Address Assignment	TB1 Pin Numbers 14	13	12	11
0-8K	1	1	2	2
4-12K	2	2	3	3
8-16K	3	3	4	4
12-20K	4	4	5	5
16-24K	5	5	6	6
20-28K	6	6	7	7
24-32K	7	7	8	8

2.4.1 Expanded Address

An additional address or enable signal is received on TPST (AB1). TPST (AB1) is used only when the KT8A memory management option is used to provide total memory of greater than 32K. In this situation, TPST (AB1) is wired to the appropriate Bank Select either on the backplane or on the DR-118A as follows:

Bank Select 0	Wire AB1 to EB2 (1st 32K)
Bank Select 1	Wire AB1 to ED2 (2nd 32K)
Bank Select 2	Wire AB1 to EL2 (3rd 32K)
Bank Select 3	Wire AB1 to ER2 (4th 32K)

Jumper E to F must also be inserted on the memory.

2.5 Operating Modes

The DR-118A memory, when used in the PDP-8/A computer, operates in a Read half cycle followed by a Write half cycle mode. The data read from the memory is restored if the MD DIR signal line is low. If the MD DIR signal is high, then data on the MDXX lines is written into the memory.

2.6 Power Requirements

The DR-118A memory system requires the same DC voltages as the DEC memory. The current requirements for each 16,384 x 12 memory assembly are as follows:

	Operating Amps*	Standby Amps	Voltage Tolerance
+5V	1.7	1.3	±5%
+20V	2.4	.1	±5%
-5V	.15	.15	±5%

*Worst Case - All Zeros

2.7 Interface

The memory interfaces with the processor or other memories or peripherals via the OMNIBUS. The OMNIBUS signals used by the DR-118A are listed below.

2.7.1 Input Signals

Signals required by the memory are:

MA0 - MA11	Address Lines
EMA0 - EMA2	Extended Address Lines
ROM ADDRESS	Inhibits Memory Cycles
SOURCE	Drive Current Timing Signal
WRITE	Mode Line
INHIBIT	Inhibit Timing Signal
POWER FAIL	Data Save Signal
MD0 - MD11	Bi-directional Data Lines
MD DIR	Memory Data Direction

All signals except INHIBIT terminate at the memory in National Semiconductor 8837 or equivalent integrated circuits.

2.7.2 Output Signals

Output signals from the memory are the 12 data lines, MD0-MD11.

All output signals from the memory are driven by National Semiconductor Type 8838 or equivalent integrated circuits.

2.8 Mechanical

The DR-118A memory assembly is designed to fit mechanically into the PDP-8/A computer utilizing the space of two DEC standard hex modules. The DR-118A memory assembly plugs into one card slot; one additional slot, however, is used as clearance for the magnetics which is plugged onto the back of the memory printed circuit board using Amp Mod I pins and receptacles. The dimensions of the memory assembly are .78" x 8.94" x 15.688".

2.9 Memory Location in Computer Chassis

The DR-118A memory module must be installed ONLY in OMNIBUS slots specifically wired for core memory. Such slots have the normal OMNIBUS connector positions A through D plus connector E which is wired to provide +20V and -5V. The DR-118A may be installed in slots 4 through 8 of core PDP-8/A's.

2.10 Environmental

The DR-118A memory is capable of sustained operation in the PDP-8/A computer over the temperature range of 0°C to +55°C and 0 to 90% relative humidity without condensation.

2.11 Ordering Information

The DR-118A part numbers and models are:

61805	16K x 12
61806	8K x 12

SECTION III

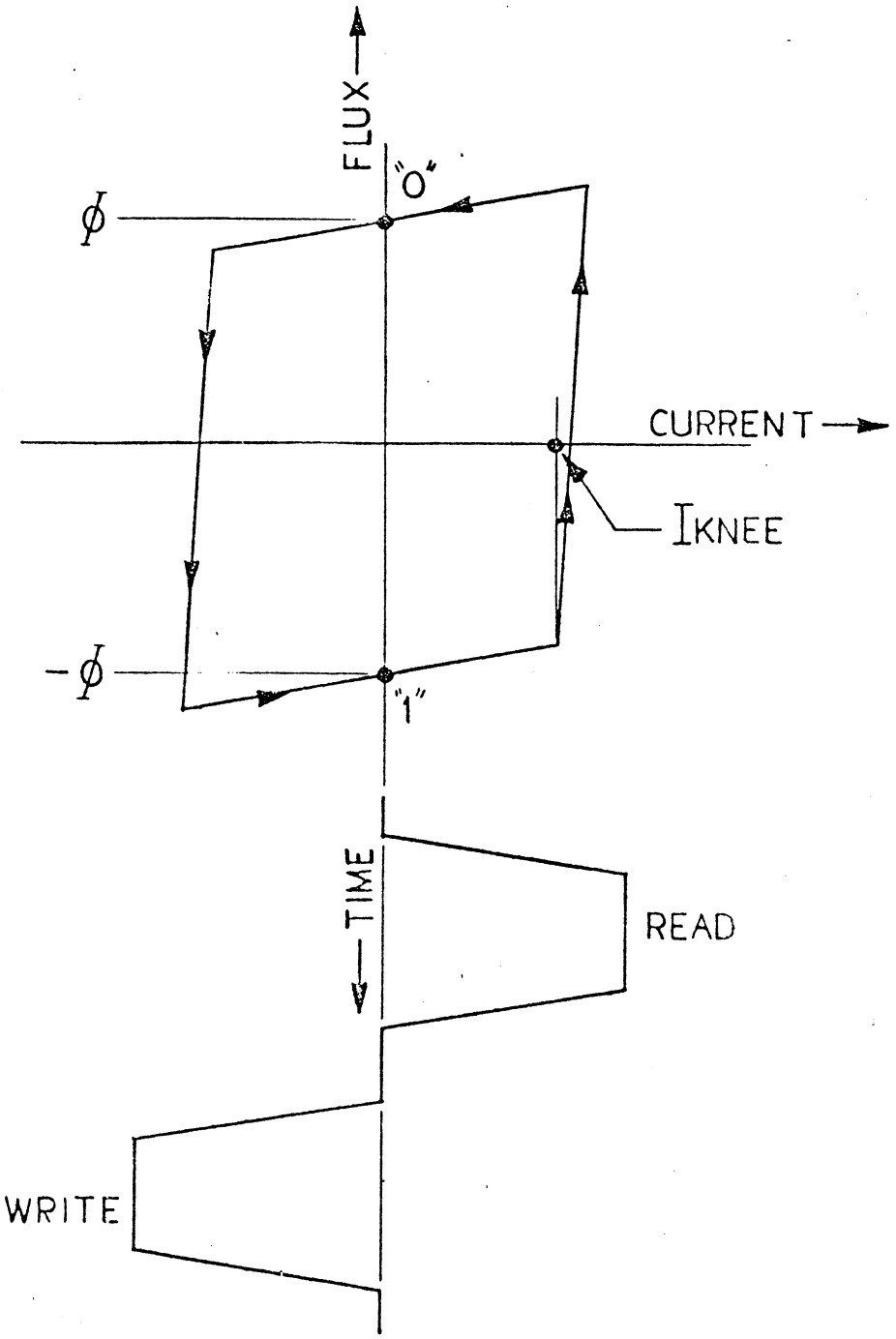
THEORY OF OPERATION

3.1 3D-3 Wire Operation

A coincident-current core memory, such as the DR-118A has, as its basic storage element, a ferrite core which has a well-defined switching characteristic. Its operation will be explained by referring to Figure 1. This figure defines the switching characteristic of the core and is known as the "hysteresis loop". It shows the relationship of the flux (magnetic field strength) in the core with respect to the total current flowing through the core aperture. Flux above the origin can arbitrarily be defined as flux in the clockwise direction and flux below the origin will be counterclockwise. The direction of flux will define the storage of a "1" or a "0". Currents on either side of the origin will have opposite directions of current flow through the core. In this explanation, current to the right of the origin will be considered "Read" current and to the left will be "Write" current. A core can be in a "1" or "0" state as shown on the hysteresis loop.

If it is in the "1" state, a Read current will put it in the "0" state and the flux will change from $-\Phi$ to $+\Phi$ which means the flux will flip from a counterclockwise orientation to clockwise. This change in flux ($2\ \Phi$) will cause a voltage to be induced on the sense wire which threads the core being interrogated by the Read current and this voltage will be detected as a "1" by the sensing circuitry connected to the sense wire. In the DR-118A system, the "1" output is approximately 30 millivolts. If the core had been in the "0" state, Read current would cause only a relatively small (approximately 4 millivolts in DR-118A) change in flux and, therefore, the induced voltage would be seen as a "0" by the sensing circuitry since it is below some minimum detection level.

To Write, the switching current polarity will be opposite in polarity in relation to the Read current. The Write current will cause the flux to go to a counterclockwise orientation which defines the core as being in the "1" state. When the core does not receive a full Write current during a Write operation, it will stay in the "0" state.



HYSTERESIS LOOP

FIGURE 1

Selection of a particular word in a memory array is shown in Figure 2. The intersection of selected X and Y drive lines in an array will cause the same corresponding core in each bit plane to be pulsed by full Read and full Write currents. In Figure 2, the top left core of each bit plane is selected and the number of bit planes defines the number of bits per word. Some unselected cores may experience half-amplitude currents, but the amplitude of these half-amplitude currents will not be sufficient to exceed the knee on the hysteresis loop (See Figure 1) and the core will remain in its previous state.

The coincidence of half-Write currents at the selected core location in each bit would cause the selected core to experience full Read and Write currents. This is desired during a Read operation, but during a Write operation, it is necessary to control the Write current so that either a "1" or a "0" may be written. This is accomplished by using the sense winding as an inhibit winding during Write time and an inhibit driver per bit array. The sense/inhibit winding threads every core in the bit array and the inhibit driver will pulse current through this winding when a "0" is to be written. The inhibit current has the opposite polarity to Write current and when it is "on" it cancels one of the two half-Write currents. The resultant current will be a half-Write, which will be insufficient to switch the core and it will remain in the "0" state.

3.2 System Description

The DR-118A memory system may be broadly divided into four basic subdivisions.

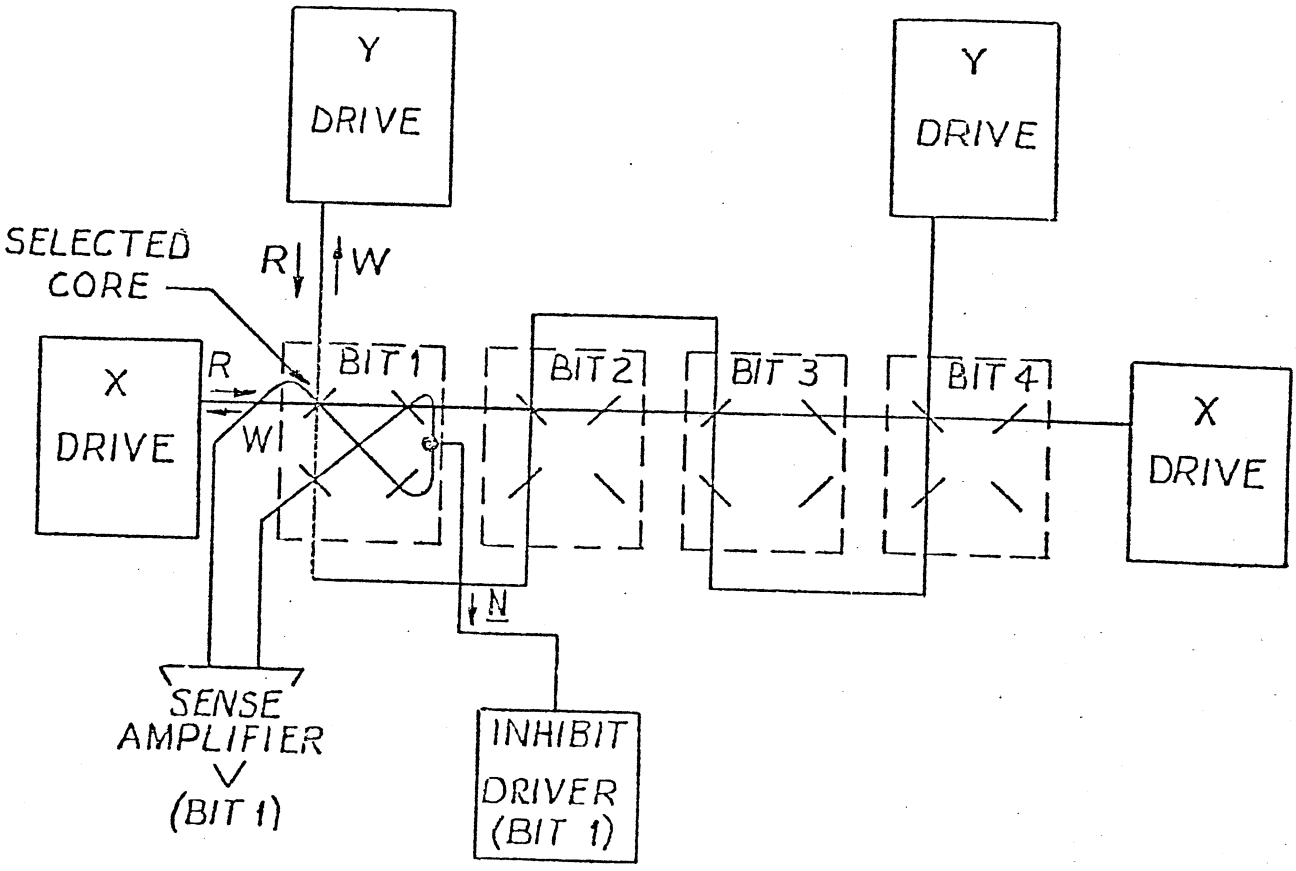
a. Timing and Control Circuitry
b. Planar Core Array
c. X and Y Current Drive Circuitry
d. Data Loop Circuitry

3.2.1 Timing and Control Circuitry

The memory, which can only act as a slave to the processor or I/O device, receives commands, address and data information on the memory bus. The internal circuitry of the memory responds to these signals in the following sequence:

a. The address information on the memory bus is examined.

b. If the address does not fall within the address block to which the memory is strapped, it continues to remain in its non-cycling state. Otherwise, the mode information on the memory bus is decoded.



3D-3 WIRE SCHEME

FIGURE 2

Timing signals necessary to perform the required mode are generated simultaneously and address bits 1 through 12 are stored. If the required mode happens to be a WRITE operation, then the data bits are also stored at the same time. (Figures 3 and 4)

3.2.1.1 Modes of Operation

Control lines SOURCE, WRITE and INHIBIT in conjunction with MD DIR line select the mode of operation.

3.2.1.1.1 Read/Restore (Data Out)

This is the conventional Read/Restore mode where the data read out of (and thus destroyed from) the core during the first half of the memory cycle at a selected address is automatically restored into the cores at the same location during the second half of the cycle.

3.2.1.1.2 Clear/Write (Data In)

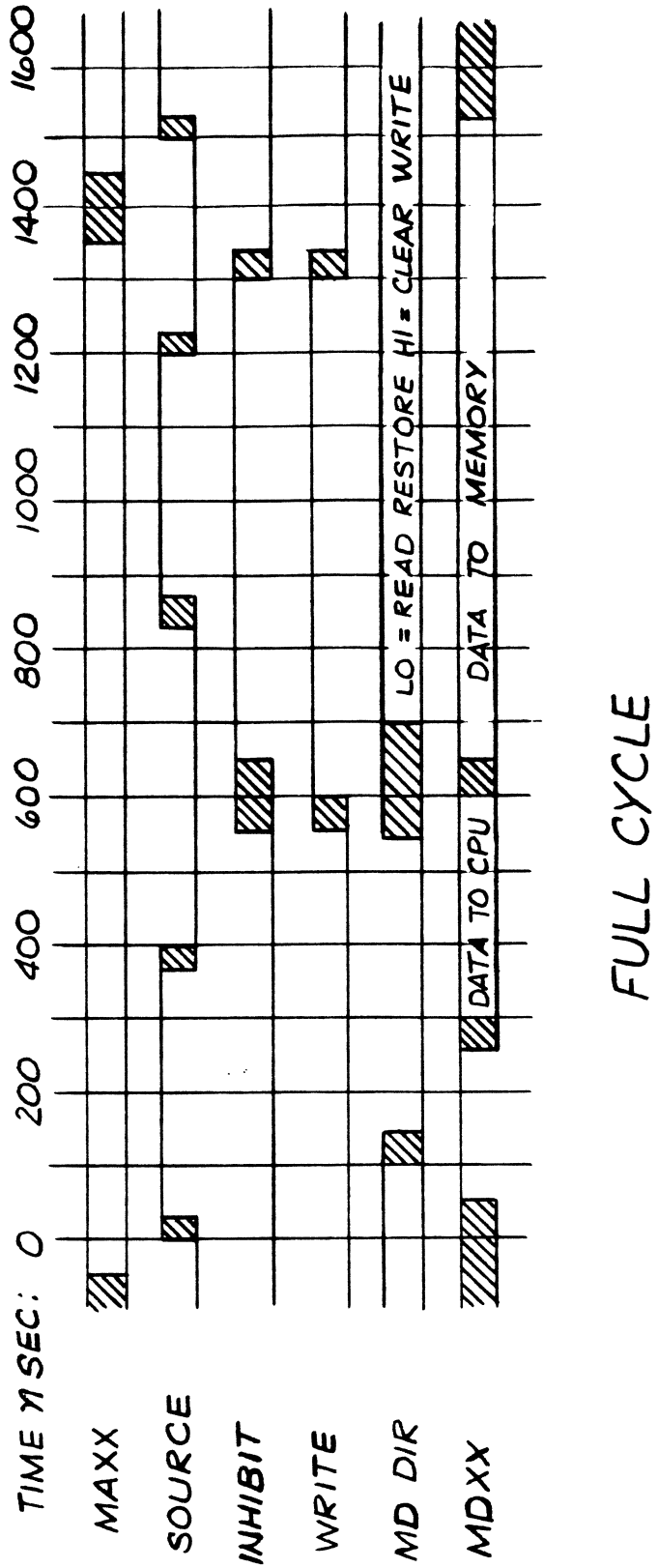
This is the conventional Clear/Write mode where the cores at a selected location are first cleared and then new data is written during the second half of the cycle.

3.2.1.1.3 Read/Modify/Write (Split Cycle)

The processor will always initiate a Read half-cycle followed by a Write half-cycle to perform the Read/Modify/Write operation.

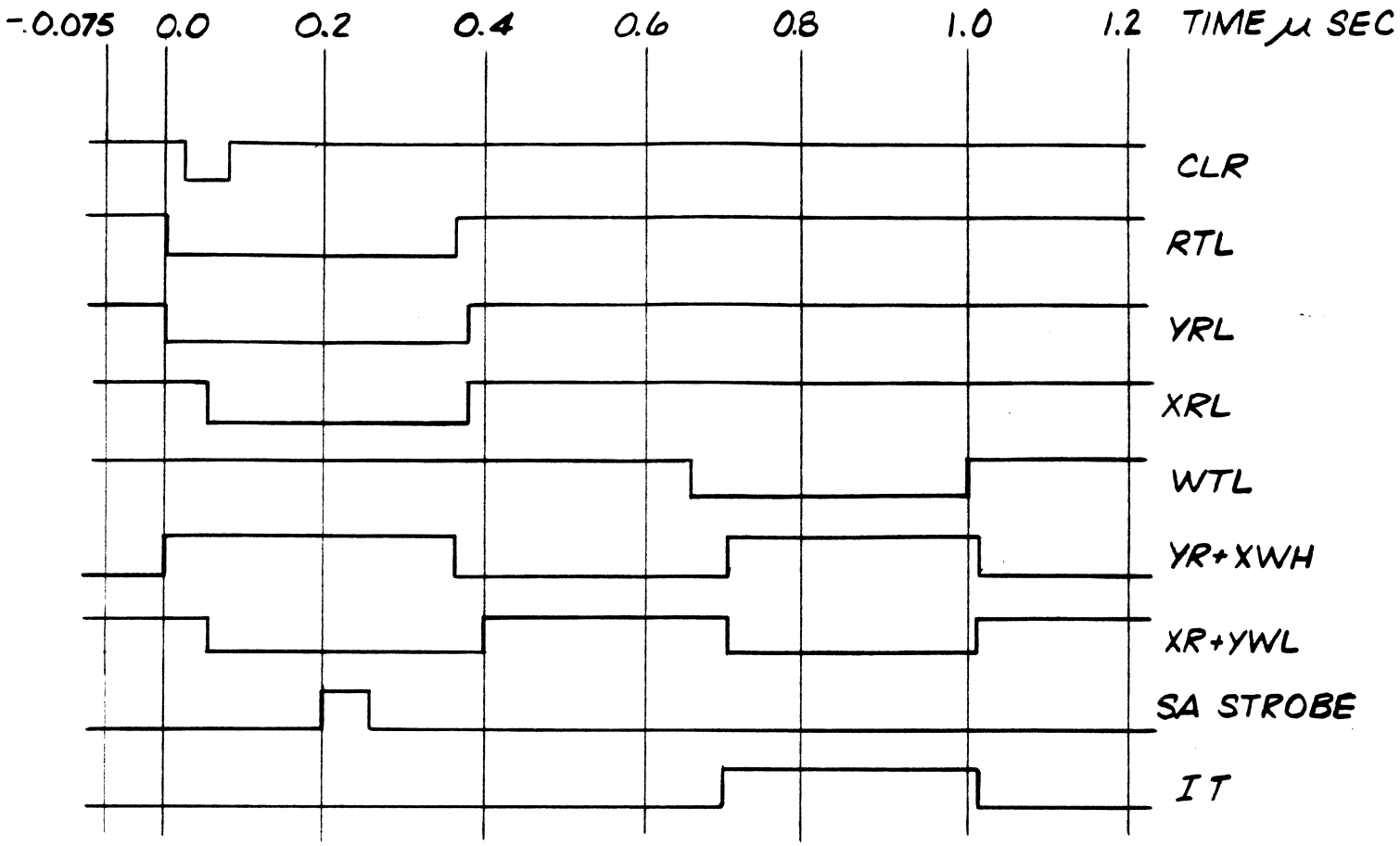
3.2.2 Planar Core Array

This array is of a dual 3D-3 wire organization and uses 18 mil lithium ferrite cores. The X:Y aspect ratio of the array is 128:128 with 8 drives and 16 sinks. Each sense/inhibit line threads through a full complement of 8,192 cores. The sense/inhibit lines are terminated with two 150 ohm resistors to ground at the sense amplifier and at the inhibit switch. The array is driven with positive X and negative Y current during a Read operation and with negative X, positive Y and positive inhibit current during the Write operation. This arrangement of the core array permits a "shared drive" scheme to be used in the DR-118A system minimizing the number of components used and thus improving the system reliability. See Figure 5 for stack pin function.



DR-118A INTERFACE TIMING

FIGURE 3



DR-118A
INTERNAL MEMORY TIMING

FIGURE 4

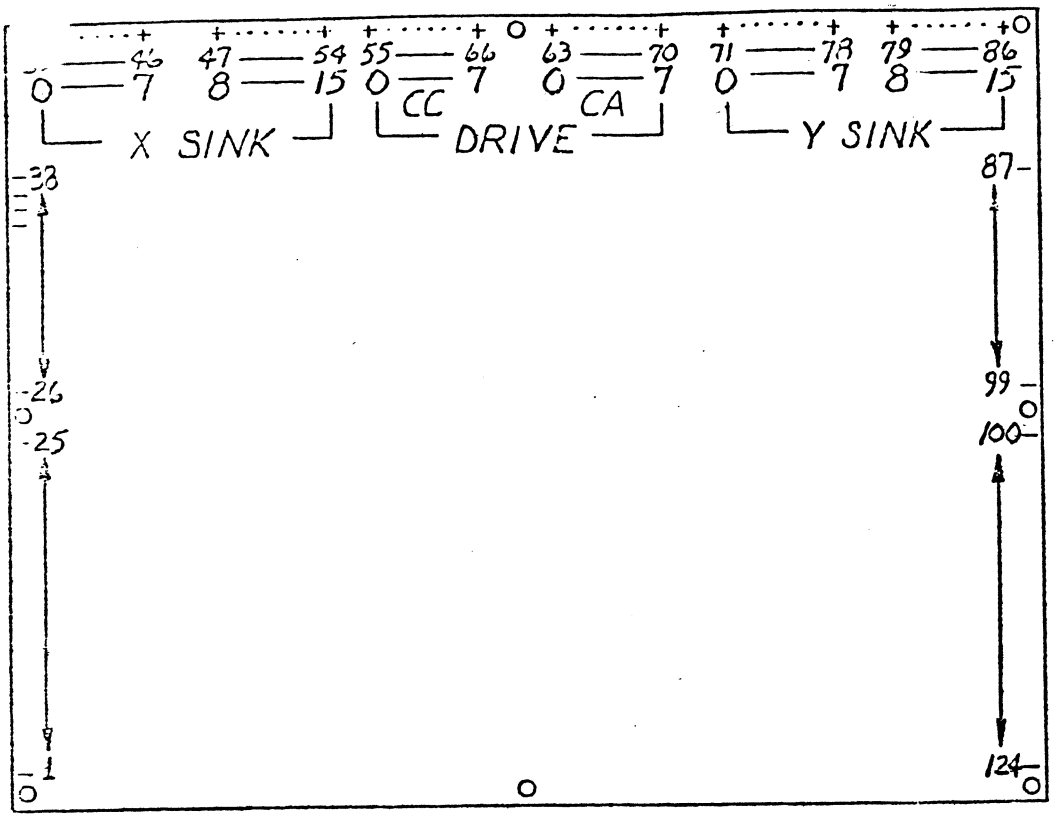


FIGURE 5

1	GND	87	GND
2	I0A	88	I6A
3	S0A	89	S6A
4	S0A'	90	S6A'
5	S0B	91	S6B
6	S0B'	92	S6B'
7	I0B	93	I6B
8	I1A	94	I7A
9	S1A	95	S7A
10	S1A'	96	S7A'
11	S1B	97	S7B
12	S1B'	98	S7B'
13	I1B	99	I7B
14	I2A	100	I8A
15	S2A	101	S8A
16	S2A'	102	S8A'
17	S2B	103	S8B
18	S2B'	104	S8B'
19	I2B	105	I8B
20	I3A	106	I9A
21	S3A	107	S9A
22	S3A'	108	S9A'
23	S3B	109	S9B
24	S3B'	110	S9B'
25	I3B	111	I9B
26	I4A	112	I10A
27	S4A	113	S10A
28	S4A'	114	S10A'
29	S4B	115	S10B
30	S4B'	116	S10B'
31	I4B	117	I10B
32	I5A	118	I11A
33	S5A	119	S11A
34	S5A'	120	S11A'
35	S5B	121	S11B
36	S5B'	122	S11B'
37	I5B	123	I11B
38	GND	124	GND

1. WORST PATTERN IS X SINK Ø-7 ⊕ YD Ø,2,4,6.

NOTES: UNLESS OTHERWISE SPECIFIED

3.2.3 X and Y Current Drive Circuitry (Figures 6, 7 and 8)

Figure 6 depicts the X and Y current scheme used in the DR-118A memory system. The circuitry may be broadly divided into three basic sections:

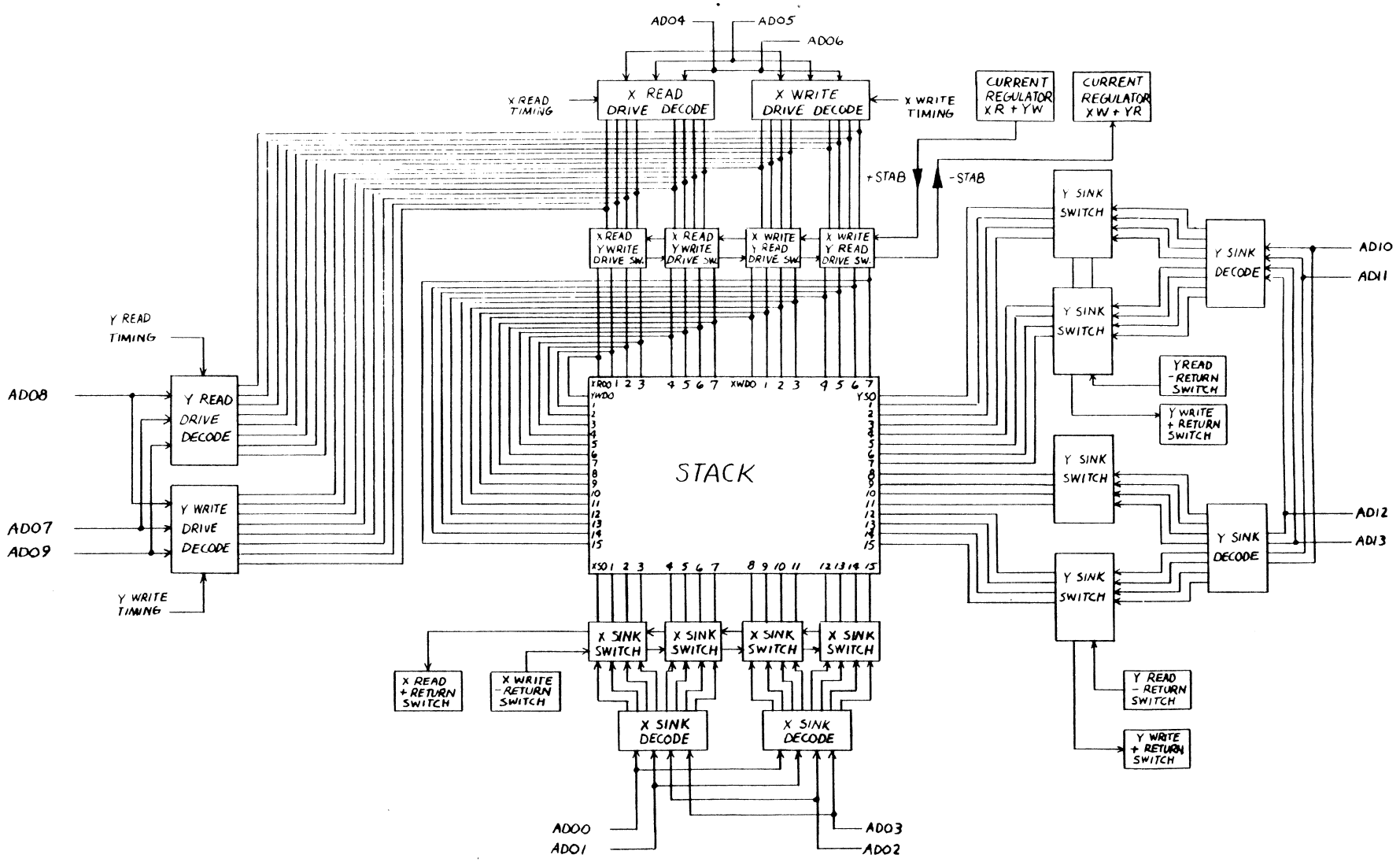
a. Current Regulator
b. Address Decoders
c. Current Switches

3.2.3.1 Current Regulator

The current regulator section consists of two regulated current sources +STAB and -STAB. The +STAB source is used to drive positive current into the stack required by X Read and Y Write operations. The regulation of this source is done at the +20V end of the drive path. The -STAB source drives negative currents from the stack during Y Read and X Write operations and is regulated at the 0V end of the drive path. Both +STAB and -STAB sources are regulated against a common reference voltage so that the X and Y currents in both the Read and Write operations remain in balance once they have been set. The common reference voltage is controlled by a sensistor which changes its resistance with temperature and causes the drive currents to be compensated for the changes in ambient temperature. The current drive is a factory set level of approximately 390mA at 25°C ambient temperature.

3.2.3.2 Address Decoders

The address decoders convert the address information from the address receivers to actual core locations as seen by the memory. The address bits 07, 08, 09 are decoded to select one of eight Y drive switches while the address bits 10, 11, 12 and 13 are decoded to select one of sixteen Y sink switches. One of eight X drive switches is selected by decoding address bits 04, 05 and 06 and address bits 00, 01, 02 and 03 select one of sixteen X sink switches.



DR118A: X-Y BLOCK DIAGRAM

FIGURE 6

3.2.3.3 Current Switches

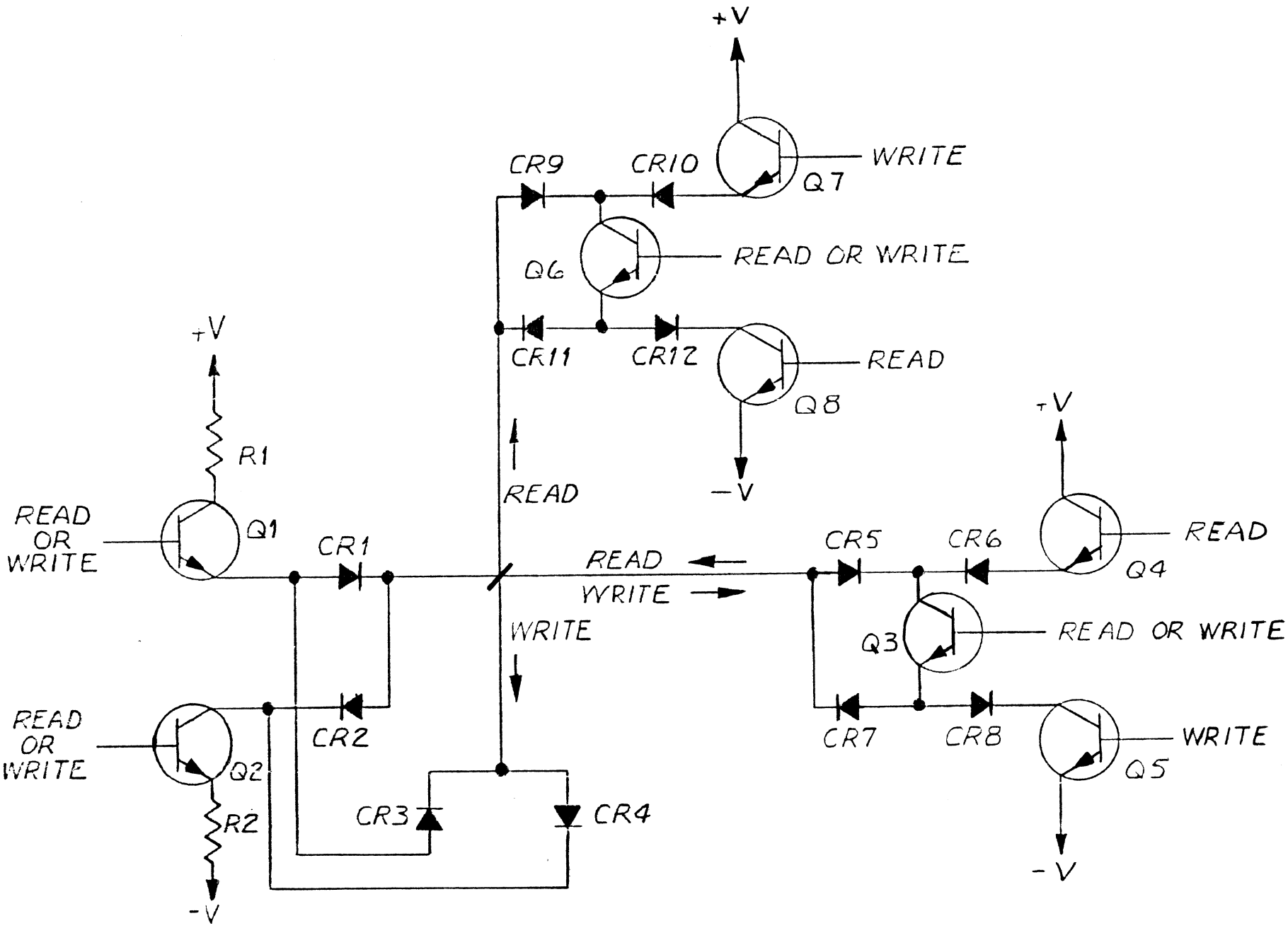
All the current switches (including the inhibit switches) used in the DR-118A system are similar in electrical design. They are floating switches using a transformer-coupled transistor as the switch. The decoders, when activated by the timing pulses, draw current through the primary of the transformer in the selected switch. This primary current induces current in the secondary connected across the base and the emitter of the transistor switching the transistor ON.

One unique feature of the drive organization is the "shared drive" scheme. The same current switch that drives Y Read current also drives X Write current. Also, one current switch drives both Y Write and X Read currents. Thus, by time sharing one current switch between the X and Y dimensions, the DR-118A memory uses only half the drive switches used by a conventional design approach to drive an identical size core array.

Another unique feature of the drive organization is the "bridge sink" scheme. The sink switches are arranged so that a sink node is only serviced by one sink switch rather than two as in conventional drive schemes. This scheme uses only half the sink switches required by conventional design approaches to drive an identical size core array.

Figure 7 shows a generalized version of this "shared drive-bridge sink" arrangement. A shared drive scheme is shown in which Q_1 supplies current in the Write direction for the X lines and in the Read direction for the Y lines. Transistor Q_2 performs the complementary function by supplying current in the Read direction for the X lines or in the Write direction for the Y lines. Thus, during a Read cycle, Q_2 drives the X lines and Q_1 drives the Y lines. During a Write cycle, Q_1 drives the X lines and Q_2 drives the Y lines.

The direction of current through the drive lines is determined by the bridge switch arrangement on the sink end of the lines. For the X line, this consists of transistors Q_3-Q_5 and diodes CR5-CR8.



SIMPLIFIED DRIVE SINK SCHEMATIC

FIGURE 7

Transistor Q_3 is turned on for both the Read and Write cycles. Transistor Q_4 is turned on during the Read cycle only and Q_5 during Write only. Thus, the path for X Read current is through Q_4, CR6, Q_3, CR7, CR2, Q_2 and R2. Resistor R2 determines the magnitude of the current. The path for X Write current is through R1, Q_1, CR1, CR5, Q_3, CR8 and Q_5. A similar determination establishes the path of current flow in the Y lines.

Figure 8 shows the complete current path for the DR-118A.

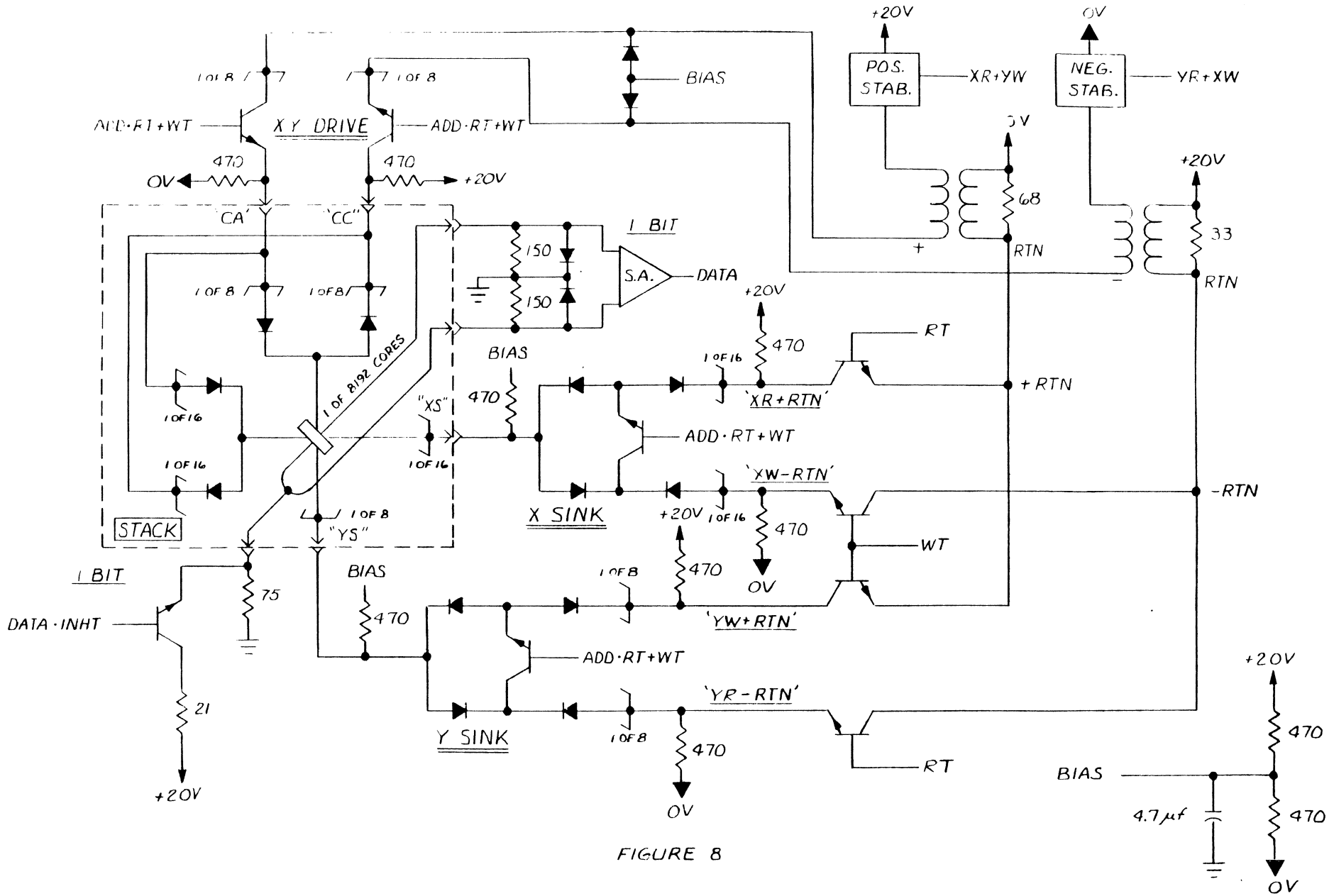

1 OF 8
ADD·RT+WT
XY DRIVE
ADD·RT+WT
BIAS
+20V
POS. STAB.
XR+YW
0V
NEG. STAB.
YR+XW
470
0V
470
+20V
68
33
"CA"
"CC"
1 BIT
150
150
S.A.
DATA
RTN
1 OF 8192 CORES
"XS"
"YS"
BIAS
470
1 OF 16
'XR+RTN'
RT
+RTN
ADD·RT+WT
'XW-RTN'
-RTN
STACK
X SINK
WT
'YW+RTN'
DATA·INHT
75
21
Y SINK
'YR-RTN'
RT
4.7μf

FIGURE 8

3.2.4 Data Loop Circuitry (Figures 9 and 10)

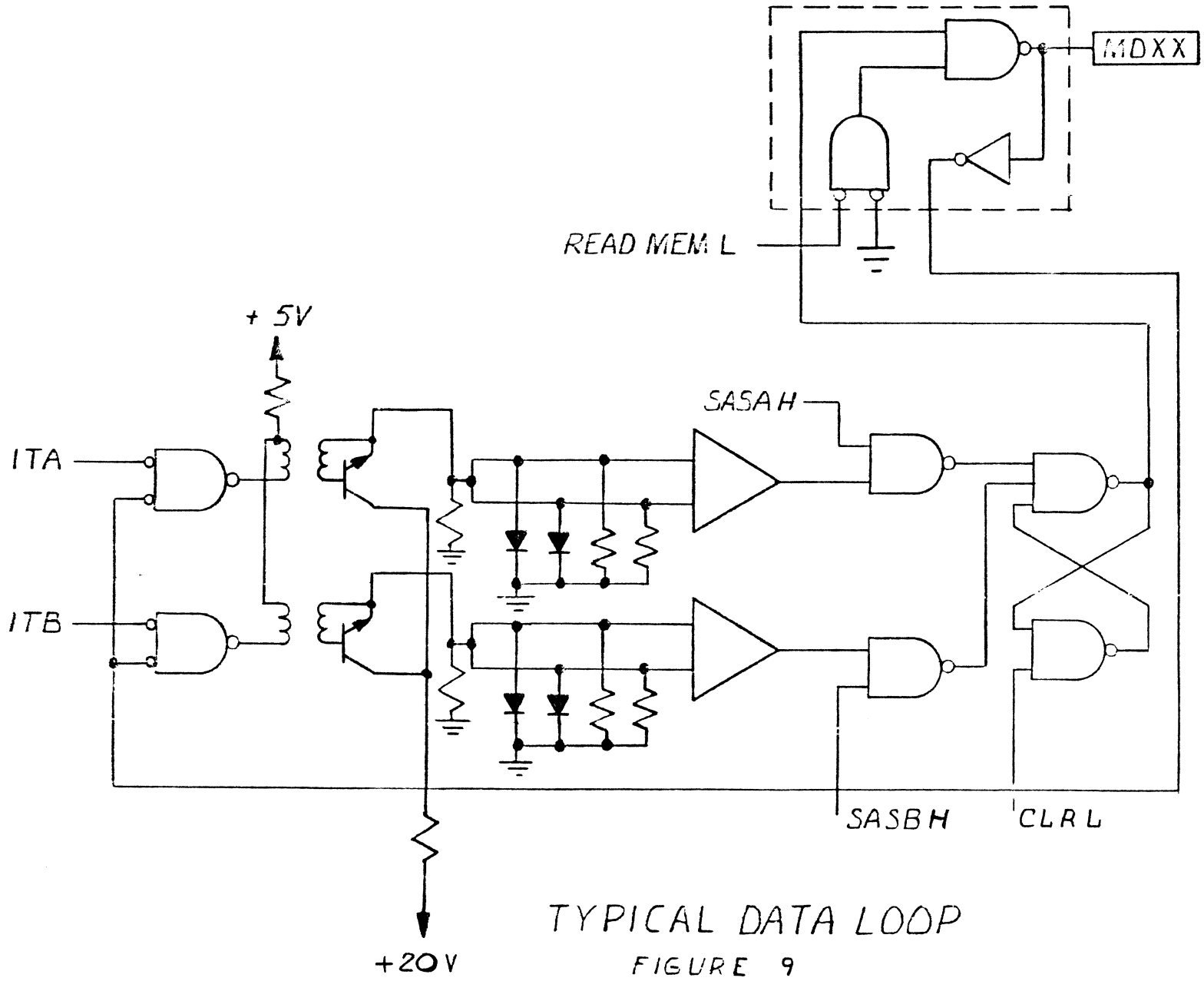
The data loop circuitry consists of the receiver, register, sense amplifier, inhibit driver and output buffer. The timing signals required for the Data Loop are generated in the Timing and Control Section.

A Clear/Write cycle requires resetting the data register, then gating the data in from the processor. During the Clear half of the cycle, the data in the memory is cleared, i.e., the cores are set to zero. During the Write half of the cycle, the selected address receives a half select current in both the X and Y axes, thereby switching the core to a "1". If a "0" is to be written into a selected core location, the Inhibit Driver is turned on. This opposes the Y Write current and the selected core location is therefore left in the "0" state.

A Read/Restore cycle requires reading out of a selected core location and restoring the same information. At the start of the Read half of the cycle, the data register is reset. The sense amplifiers are strobed during the peak of the core output and, if the core signal exceeds the preset threshold, the sense amplifier goes to a "1", setting that bit of the data register. A "0" signal will not exceed the threshold voltage during the strobe time, leaving that bit of the data register in the reset state. During the Restore half of the cycle, the data just read into the data register controls the inhibit drivers, rewriting the original data back into the addressed location.

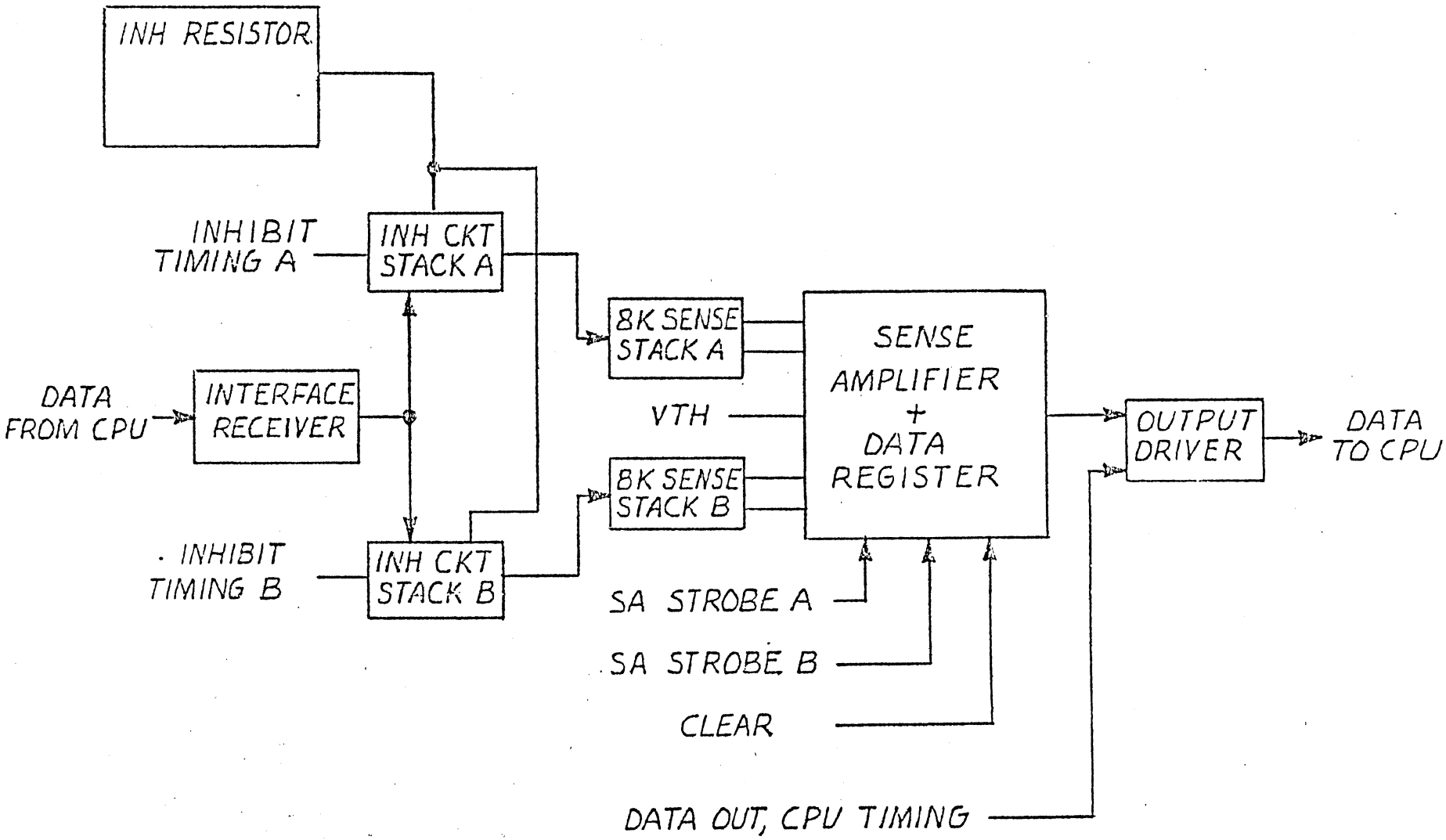
The strobe adjustment is critical and should only be changed when absolutely necessary. It is factory set to approximately 300 ns from Source. The threshold voltage to the sense amplifier is approximately 18 millivolts and is generated by a voltage divider network connected to +5V.

The inhibit driver is a floating, transformer-coupled transistor switch. The primary is driven from a 75453 integrated circuit. Primary current flows in the transformer when the output from the data bus (Data "0") and the inhibit timing signals are both low at the input to the gate.



TYPICAL DATA LOOP

FIGURE 9



BLOCK DIAGRAM - DATA LOOP

FIGURE 10

SECTION IV

DOCUMENTATION

REV. L

DWG. NO. 61805 SHEET 1 OF 7

REVISIONS

SYM.	SHEET	DESCRIPTION	APPROV.	DATE
A		RELEASED TO DRC PRODUCTION	JPD	3-31-76
B		ECN 861	[illegible]	[illegible]
C		ECN 884	[illegible]	[illegible]
D		ECN 898	[illegible]	[illegible]
E		ECN 1203	RK	4JAN78
F		ECN 1596	RK	30JAN79
G		ECN 1540	RK	30JAN79
H		ECN 1614	RK	27MAR79
J		ECN 2131 M.O.	RK	26AUG81
K		ECN 2390	RK	26AUG81
L		ECN 2483 BL	RK	9JUL82

DRAWN MAS	DATE 3-2-76	TITLE BILL OF MATERIAL
CHECKED B.S.	DATE 3-31-76	DR-118A 16K x 12
ENGR. [signature]	DATE 3-31-76	
APPROVED [signature]	DATE 3/31/76	

DATARAM CORPORATION
PRINCETON NEW JERSEY

DWG. NO. 61805 REV. L
SHEET 1 OF 7

BRUNING 40-107 11829

TITLE: B/M DR-118A 16K x 12

ITEM NO.	QTY.	PART NUMBER	DESCRIPTION	SUGGESTED MANUFACTURER	REFERENCE NOTES
1	67	18101	DIODE, SILICON, HIGH CONDUCTANCE		CR1-64,66-68
2	1	18205	DIODE, ZENER, 5.1 VOLT, 1N751A		CR69
3			NOT USED		
4	12	10213	RESISTOR, FILM, 1/10 WATT, 2.74K, 1%		R2,4,6,8,10,12,
					38,40,42,44,46,48
5	2	10219	RESISTOR, FILM, 1/10 WATT, 562 OHMS,1%		R75,88
6	1	10208	RESISTOR, FILM, 1/10 WATT, 475 OHMS,1%		R89
7	12	10201	RESISTOR, FILM, 1/10 WATT, 10 OHMS, 1%		R1,3,5,7,9,11,37,
					39,41,43,45,47
8	1	10210	RESISTOR, FILM, 1/10 WATT, 1K, 1%		R80
9	3	10121	RESISTOR, CC, 1/4 WATT, 4.7K, 5%		R97,104,105
10	1	10119	RESISTOR, CC, 1/4 WATT, 3.3K, 5%		R74
11	6	10113	RESISTOR, CC, 1/4 WATT, 1K, 5%		R79,81,96,98,
					102,108
12	9	10111	RESISTOR, CC, 1/4 WATT, 470 OHMS, 5%		R49-54,93,94,
					101
13	5	10164	RESISTOR, CC, 1/4 WATT, 330 OHMS, 5%		R65,66,73,95,100
14	4	10105	RESISTOR, CC, 1/4 WATT, 100 OHMS, 5%		R60,64,87,103
15	1	10144	RESISTOR, CC, 1/4 WATT, 68 OHMS, 5%		R76
16	3	10102	RESISTOR, CC, 1/4 WATT, 47 OHMS, 5%		R78,85,86
17	12	10174	RESISTOR, CC, 1/4 WATT, 39 OHMS, 5%		R19-30
18	1	10151	RESISTOR, CC, 1/4 WATT, 33 OHMS, 5%		R62

*INDICATES PART TO BE FROM SUGGESTED MANUFACTURER ONLY.

DATARAM CORPORATION
PRINCETON NEW JERSEY

DWG. NO. B/M 61805
SHEET 2 OF 7

REV. L

BRUNING 40-105 11402

TITLE: B/M DR-118A 16K x 12

ITEM NO.	QTY.	PART NUMBER	DESCRIPTION	SUGGESTED MANUFACTURER	REFERENCE NOTES
19	8	10175	RESISTOR, CC, 1/4 WATT, 15 OHMS, 5%		R57,58,59,67,68,
					69,72,77
20	2	10177	RESISTOR, CC, 1/4 WATT, 680 OHMS, 5%		R92,107
21	2	10161	RESISTOR, CC, 1/2 WATT, 220 OHMS, 5%		R61,63
22	1	10117	RESISTOR, CC, 1/4 WATT, 2K OHMS, 5%		R109
23					
24					
25			NOT USED		
26	2	10321	RESISTOR, WW, NI, 2.5 WATT, 7.5 OHMS, 1%		R56,70
27	12	10340	RESISTOR, POWER, 5 WATT, 21 OHMS, 1%		R13-18,31-36
28			NOT USED		
29	1	10402	RESISTOR, VARIABLE, 10K		R99
30	4		RESISTOR, SELECT AT TEST		R55,71,90,106
31			NOT USED		
32	7	11903	RESISTOR MODULE, 470 OHMS, 5%		RM13,15,17,18,19
					22,24
33	12	11902	RESISTOR MODULE, 150 OHMS, 5%		RM1-12
34	6	11901	RESISTOR MODULE, 47 OHMS, 5%		RM14,16,20,21,23,
					25
35			NOT USED		
36			NOT USED		
37	3	12323	CAPACITOR, CERAMIC, .015μF, 10%		C53,56,68
38	1	12102	CAPACITOR, TANTALUM, 15μF, ±20%		C71

*INDICATES PART TO BE FROM SUGGESTED MANUFACTURER ONLY.

DATARAM CORPORATION
PRINCETON NEW JERSEY

DWG. NO. B/M 61805
SHEET 3 OF 7

REV. L

BRUNING 40-105 11402

TITLE: B/M DR-118A 16K x 12

ITEM NO.	QTY.	PART NUMBER	DESCRIPTION	SUGGESTED MANUFACTURER	REFERENCE NOTES
39	1	12506	CAPACITOR, SILVER MICA, 470pF, 5%		C67
40	1	12517	CAPACITOR, SILVER MICA, 220pF, 5%		C59
41	12	12513	CAPACITOR, SILVER MICA, 100pF, 5%		C1-6,41-46
42	1	12516	CAPACITOR, SILVER MICA, 47pF, 5%		C52
43	1	12515	CAPACITOR, SILVER MICA, 22pF, 5%		C63
44	1	12522	CAPACITOR, SILVER MICA, 10pF, 5%		C62
45	14	12106	CAPACITOR, TANTALUM, 6.8µF, 35 VOLTS		C10-15,23,24,
					32-37
46	21	12105	CAPACITOR, TANTALUM, 4.7µF, 10 VOLTS,20%		C7,8,9,22,25,38,
					39,40,47,48,49,
					50,51,54,57,58,
					60,61,65,66,69
47	1	12523	CAPACITOR, SILVER MICA, 820pF, ±5%		C64
48	20	14204	TRANSFORMER, PULSE, QUAD 10µH		TM1-20
49	1	12316	CAPACITOR, CERAMIC, 0.1µF, ±20%		C70
50	19	20401	TRANSISTOR, QUAD, DIP		MHQ1-19
51			NOT USED		
52	5	20202	TRANSISTOR, NPN, CORE DRIVER, 2N3725		Q1-5
53	8	20203	TRANSISTOR, PNP, 2N2905		Q6,9,11,12,13,
					15,17,18
54	7	20104	TRANSISTOR, NPN, 2N2369A		Q8,10,14,16,19
					20,21
55			NOT USED		

*INDICATES PART TO BE FROM SUGGESTED MANUFACTURER ONLY.

DATARAM CORPORATION
PRINCETON NEW JERSEY

DWG. NO. 61805
B/M
SHEET 4 OF 7

REV. L

BRUNING 40-105 11402

TITLE: B/M DR-118A 16K x 12

ITEM NO.	QTY.	PART NUMBER	DESCRIPTION	SUGGESTED MANUFACTURER	REFERENCE NOTES
56			NOT USED		
57	4	18307	DIODE MODULE, COMMON ANODE (8)		CRM 13,15,17,19
58	4	18308	DIODE MODULE, COMMON CATHODE (8)		CRM 14,16,18,20
59	12	18309	DIODE MODULE, COMMON CATHODE (4)		CRM1-12
60	1	10506	THERMISTOR, 1K		RT1
61			NOT USED		
62			NOT USED		
63			NOT USED		
64	6	16513	I.C. QUAD, 2 I/P NAND GATE 74S00		Z 35,36,37,38,39
					41
65	5	16501	I.C. HEX INVERTER 74S04		Z40,42,46,50,56
66	1	16516	I.C. DUAL, 4 I/P NAND GATE 74S20		Z45
67	1	16326	I.C. DUAL MONOSTABLE MULTIVIBRATOR 74123		Z43
68	1	16520	I.C. 3-TO-8 DECODER/DEMUX 74S138		Z44
69	8	16312	I.C. BCD TO DECIMAL DECODER (O.C.) 74145		Z25-32
70	12	16603	I.C. DUAL SENSE AMPLIFIER 7520		Z1-6,19-24
71	14	16607	I.C. DUAL PERIPHERAL OR DRIVER 75453		Z7-18,33,34
72	3	16334	I.C. HEX UNIFIED BUS RECEIVER 8837		Z49,51,52,
73	4	16345	I.C. QUAD UNIFIED BUS TRANSCEIVER 8641		Z47,48,53,54
74	1	16606	I.C. DUAL PERIPHERAL DRIVER 75451B		Z55
75	1	16324	I.C. QUAD 2 I/P NAND SCHMITT TRIG 74132		Z57
76	5	22214	BEAD PIN		
77	1	23003	I.C. SOCKET 16 PIN		TB1

*INDICATES PART TO BE FROM SUGGESTED MANUFACTURER ONLY.

DATARAM CORPORATION
PRINCETON NEW JERSEY

DWG. NO. 61805
B/M
SHEET 5 OF 7

REV. L

BRUNING 40-105 11402

TITLE: B/M DR-118A 16K x 12

ITEM NO.	QTY.	PART NUMBER	DESCRIPTION	SUGGESTED MANUFACTURER	REFERENCE NOTES
78	124	22801	RECEPTACLE, AMP		
79	14	27305	TRANSIPAD TO-5		
80			NOT USED		
81	1	50433	ASSEMBLY, CORE STACK		
82	5	26105	NUT, HEX, NYLON, 4-40		
83	1	40545	PRINTED CIRCUIT BOARD		
84					
85					
86	1	42654	INSULATOR, CIRCUIT CARD, DR-118		
87	1	23009	ADAPTER PLUG, 16 PIN, W/COVER		
88	A/R	24302	WIRE, TINNED COPPER, BUS #24 AWG		
89	A/R	24108	TUBING, CLEAR #24		
90	1	30601	NAMEPLATE		
91	6	27204	SPACER, RND, THD, NYL, WHT #2-56 .100LG.		
92	1	23013	MINI-BUS		
93	1	42665	STIFFENER BAR		
94	1	42978	BAR SUPPORT DR118A		
95					
96	2	42069	PROTECTIVE SHIELD		
97	2	42650	HANDLE-INSERTOR, EXTRACTOR		
98	2	26306	SCREW, 2-56 x 5/16 LG.		
99	2	26107	NUT, HEX #2 SELF-LOCKING		
100	2	42651	SPACER, HANDLE MOUNT		

*INDICATES PART TO BE FROM SUGGESTED MANUFACTURER ONLY.

DATARAM CORPORATION
PRINCETON NEW JERSEY

DWG. NO. B/M 61805
SHEET 6 OF 7

REV. L

BRUNING 40-105 11402

TITLE: B/M DR-118A 16K x 12

ITEM NO.	QTY.	PART NUMBER	DESCRIPTION	SUGGESTED MANUFACTURER	REFERENCE NOTES
101	2	26212	WASHER, BELLEVILLE SPRING		
102	6	26301	SCREW, PNH PHL, STEEL, 2-56 x 1/4 LG.		
103	5	26609	SPACER, RND, NYL WHT .115 ID x 5/16 LG.		
104	3	26503	SCREW, FH PHL, 100° STEEL, 4-40 x 3/16 LG.		
105	5	26501	SCREW, FH PHL, 100° STEEL, 4-40 x 5/8 LG.		
106	5	30604	PAD, SOLID		
107	11	26201	WASHER FLAT, NYLON, WHT, #4		
108	5	22601	CONTACT, MALE		
109	A/R	24802	WIRE, SOLID, TW/PR, B&W, TEFLON,	#30 AWG	
110	3	26513	SCREW, F.H PHL 100° STEEL 4-40 x 5/16 LG		

*INDICATES PART TO BE FROM SUGGESTED MANUFACTURER ONLY.

DATARAM CORPORATION
PRINCETON NEW JERSEY

DWG. NO. B/M 61805
SHEET 7 OF 7

REV. L

BRUNING 40-105 11402