TECHNICAL MANUAL

DATARAM INCORPORATED
MODEL C03
CARTRIDGE DISC CONTROLLER

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INTRODUCTION

1.1 GENERAL DESCRIPTION

The Dataram Incorporated model C03 is a moving head cartridge disc controller designed for compatible operation with a wide variety of industry standard disc drives on the LSI-11 microcomputer.

1.2 FEATURES

- The controller design incorporates an internal bipolar microprocessor which performs the basic control and sequencing of data transfers between the LSI-11 and the disc drive. Through the use of this advanced technology, the DI-C03 provides many features and advantages to the user which are not presently available elsewhere in a single, integrated unit.

  Of primary advantage is the compact physical package which incorporates all controller circuitry on a single quad-height printed circuit board. The board mounts directly into any available quad option slot of the H9270 (or equivalent) backplane, with the drive connected by means of a single flat ribbon cable and connector. The board dimensions permit installation of option boards in adjacent slots which allows maximum utilization of available backplane space. Elimination of internal I/O bus adapters/converters and external mounting boxes and power supplies to accommodate the controller provides obvious cost savings, both direct and indirect, to the end user of the product.

  Of equal importance to the user is the full functional compatibility of the DI-C03 with the DEC® RK-11/RK-05 Disc System. This compatibility is achieved without modification or "patches" to the manufacturer's standard software as written. The DI-C03 has been extensively tested under, and is designed to be fully compatible with, the DEC®RT-11 and RSX-11M operating systems. In addition, the DI-C03 will execute all current RK-11/RK-05 diagnostics supplied by the computer manufacturer.

  Total system storage capacity may be up to 20 megabytes contained on from one to four physical drives. A physical drive may contain from 2.5 — 20 megabytes. The appropriate system configuration is selectable by simple slide switch programming on the board, thus permitting easy system reconfiguration in the field.

  A wide variety of industry standard drives from various manufacturers have been interfaced to the LSI-11®using the DI-C03. Drive adaptation is provided by means of individual adapter boards (not always required) which attach to the drive cable and mount in the drive itself. This simple mechanism eliminates changing to the controller board for each drive type, and therefore the user of several types of disc drives may purchase, stock, and maintain only one basic controller.

  The controller will accommodate both 100 and 200 track per inch densities in the same system. Drive speed may be either 1500 or 2400 rpm. Track density is switch selectable; drive speed programming requires only a clock crystal selection and an on-board jumper connection.

  The unit requires only 3.5 amps at 5 VDC from the computer (or external) power supply. In addition, it incorporates computer I/O bus drivers and receivers which meet the specifications stated for the LSI-11®to insure complete electrical interface compatibility. All interface lines present less than one unit load to the bus.

  Two spare bus address bits are implemented in the design to provide direct bus addressing of up to 128K words for upward compatibility with follow-on versions of the basic LSI-11®.

  Pin connections and circuitry are also provided to permit expansion of the number of interrupt levels as anticipated in follow-on versions of the basic LSI-11®.

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A sixteen-byte FIFO buffer memory is incorporated to protect against data loss due to DMA latency times. Data is recorded using a crystal-controlled oscillator which compensates for operating extremes to insure reliable data recovery and media interchangeability with other systems.

High speed execution of bus control sequences results in efficient use of I/O bus band width. The controller requires only about 2 microseconds to execute a DMA transfer after gaining mastership of the bus.

The controller provides a drive polling feature which permits overlap of seek operations with data transfers in multi-drive configurations. The controller automatically performs protective operations such as data checksum verification, head location verification, read and write check sequences, write protect lockout, and other error checks. The use of stored program logic in the microprocessor provides the ability to automatically perform sophisticated error recovery procedures in the controller itself.

Two other optional features (selectable by slide switch setting on the board) provide potential system enhancements in certain applications. The first option permits selection of read/write/seek status and operations on the basis of either physical drive or logical drive (several logical drives of 2.5 MBytes each may be contained on a single physical drive). The second option provides an effective high-speed seek whereby sectors of odd-numbered cylinders are physically offset by an amount which permits crossing adjacent cylinder boundaries without the loss of a full drive rotation period.

Finally, and most importantly, the DI-C03 uses a conservative design approach which insures that the unit works and works reliably over a wide range of voltage margins and clock duty cycles and over the complete range of physical environments that can be handled by all other elements of the system.

1.3 FUNCTIONAL AND PERFORMANCE CHARACTERISTICS

Table 1-1 summarizes the functional and performance characteristics of the DI-C03 controller. The various disc drive types and manufacturers which are currently supported by the DI-C03, together with cross references to other applicable information, are summarized in Appendix A of this manual.

1.4 PHYSICAL DESCRIPTION

The DI-C03 basic controller is physically contained on a single quad height printed circuit board measuring 10.43" by 8.92" and is identical to the card size of the LSI-11®microprocessor. The card is a 4-layer printed wiring board having its power and ground distribution planes on the inner layers and all signal lines on the outer layers.

Refer to Figure 1-1 which shows the front and back sides of the board for identification of the contact fingers inserted into the four processor backplane connectors. The A and B connector slots contain all processor interface signals; power and ground connections only are made via the C and D connectors except for the interrupt and DMA grant signals which are jumpered by etch on the board. A numeric indicator is used to differentiate between the component side (side 1) and the solder side (side 2). Letters from A through V (excluding G, I, O, and Q) identify a particular pin on a side of a connector slot.

Disc drives are connected to the controller via the 50-pin disc interface connector (J1) at the rear of the board. All installations, regardless of the particular model disc drive used, are connected by means of a standard 50-conductor flat cable assembly which is terminated at both ends by a crimp-on 50-pin female connector. At the drive end of the cable, a specialized adapter board is normally used to adapt the physical and/or electrical characteristics of the DI-C03 cable termination to those of the particular disc drive used. Figure 1-2 shows a photograph of the cable assembly and several standard adapter boards presently available. Consult the applicable Dataram Applications Manual for specific details of these assemblies.

TABLE 1-1
FUNCTIONAL AND PERFORMANCE CHARACTERISTICS

Function	Characteristics
Type	Cartridge disc controller
Application	Direct interface to LSI-11 bus and to most industry standard cartridge disc drives
Software Compatibility	DEC®RK-11/RK-05 System: Standard diagnostics RT-11 RSX-11M
Data Format:	
Logical Drive	203 cylinders—2 tracks (surfaces) per cylinder 12 sectors/track 256 data words/sector (512 bytes) 1.25 million words/drive (2.5 million bytes)
Data Word	16 bits
Physical Drive Configurations:	
Drive Format	1-8 logical drives/physical drive (2.5-20.0 million bytes)
Platters	1-4
Track Density	100 or 200 TPI (Can mix in one system)
Cylinders	203 (100 TPI) or 406 (200 TPI)
Bit Density	2040 or 2200 BPI
Speeds	1500 or 2400 RPM
Capacities	4 Physical drives 8 Logical drives (20.0 million bytes)
Electrical:	
Power	3.5 amps @ +5 VDC
LSI-11 Bus Load	Less than 1 unit load, all lines
Physical:	
Dimensions	10.43" x 8.92" (quad height)
Mounting	Plugs directly into LSI-11®compatible back-plane via A, B, C, D connectors
Drive Cable	3M 50-conductor flat cable, 25 ft. max.

TABLE 1-1 (Continued)

Function	Characteristics
LSI-11® Interface:	
Compatibility	Direct to LSI-11® bus
Addressing	To 128K words without modification
Interrupt Levels	Level 4 standard; strappable to Levels 5, 6, or 7 (for follow-on LSI-11)
Interrupt Vector	220g
Data Transfers	DMA to/from controller
Options (Switch Selectable):	
Physical/Logical Status	Permits selection of read/write/seek status for either logical or physical drive
Mixed Density	Permits mixing of 100 and 200 TPI drives in one system
High Speed Seek	Provides sector offset between adjacent tracks for reduced time in crossing cylinder boundaries

The board has card pullers permanently attached to the board to facilitate insertion and removal from the computer. The slide switch (SW1) is used for configuring the controller for the various number, capacity, and track density of drives connected to the system. Jumper pins E1-E5 are used to configure the controller to the required operating frequency (in conjunction with the crystal frequency). The test socket (J2) provides conveniently located test and control signal access points for maintenance and trouble-shooting functions.

1.5 ORGANIZATION AND USE OF THE MANUAL

This manual contains all technical information required for the installation, operation, and field-level maintenance of the basic DI-C03 disc controller. Appendix A contains a set of tables which summarize, in convenient form, details generally required for quick reference by the user and/or field maintenance personnel. Also available is a drawing package which contains the detailed engineering data, schematics, assembly drawings, parts list, etc. required for field-level trouble-shooting and maintenance. Appendix B contains application notes and other miscellaneous useful information.

In addition to this manual, there is a separate Applications Manual available for each particular type or series of disc drive(s) which may be used with the DI-C03 controller. The Applications Manual, used in conjunction with the technical information supplied by the disc manufacturer, contains the details needed to configure the DI-C03 with the drive to form a complete, integrated storage system.

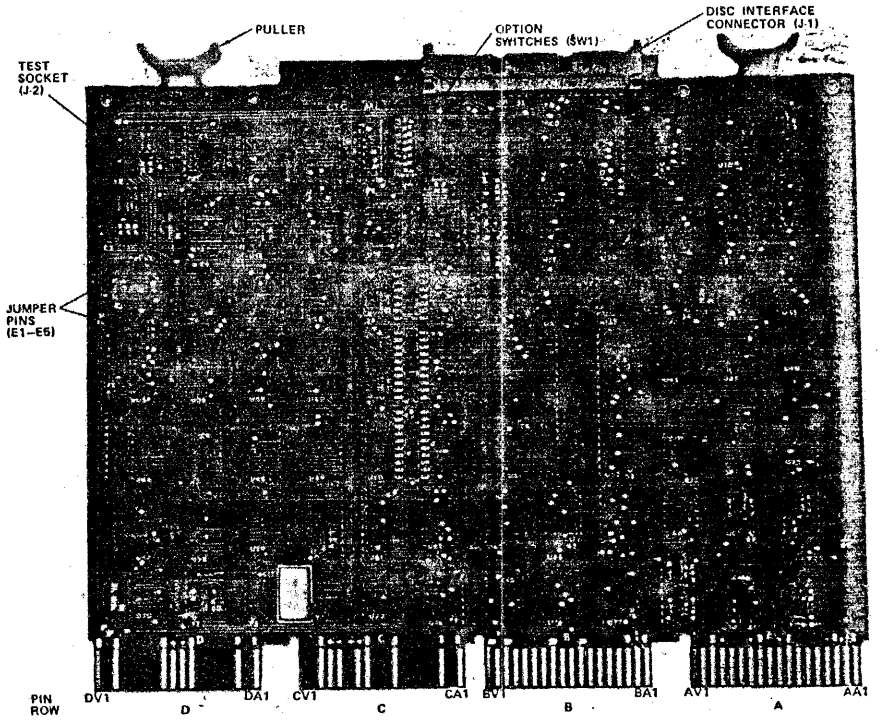
Contents of this manual are based on the assumption that the user is completely familiar with the LSI-11® product line series, including the various options and configurations available. No attempt is made to define specific terminology and model/part numbers related to the LSI-11® product line, and the reader should consult appropriate documentation available on the LSI-11® for such purposes.

The following publications are applicable and recommended for use with this manual:

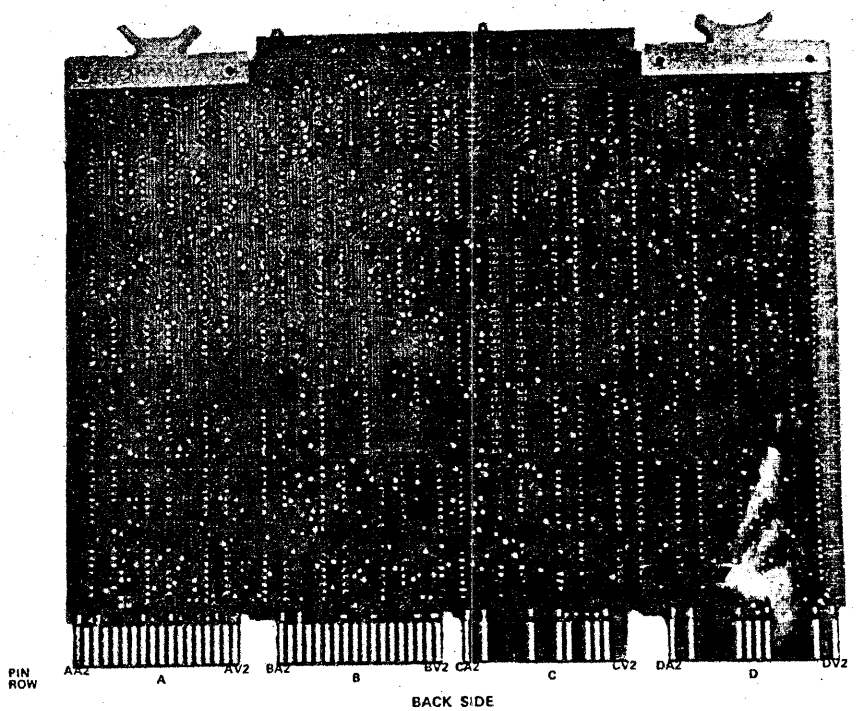
Microcomputer Handbook, 1977-78, Second Edition, Digital Equipment Corporation.

PDP-11® Peripheral Handbook, Digital Equipment Corporation.

RK11-D and RK11-E Moving Head Disc Drive Controller Manual, Digital Equipment Corporation.



FRONT SIDE



BACK SIDE

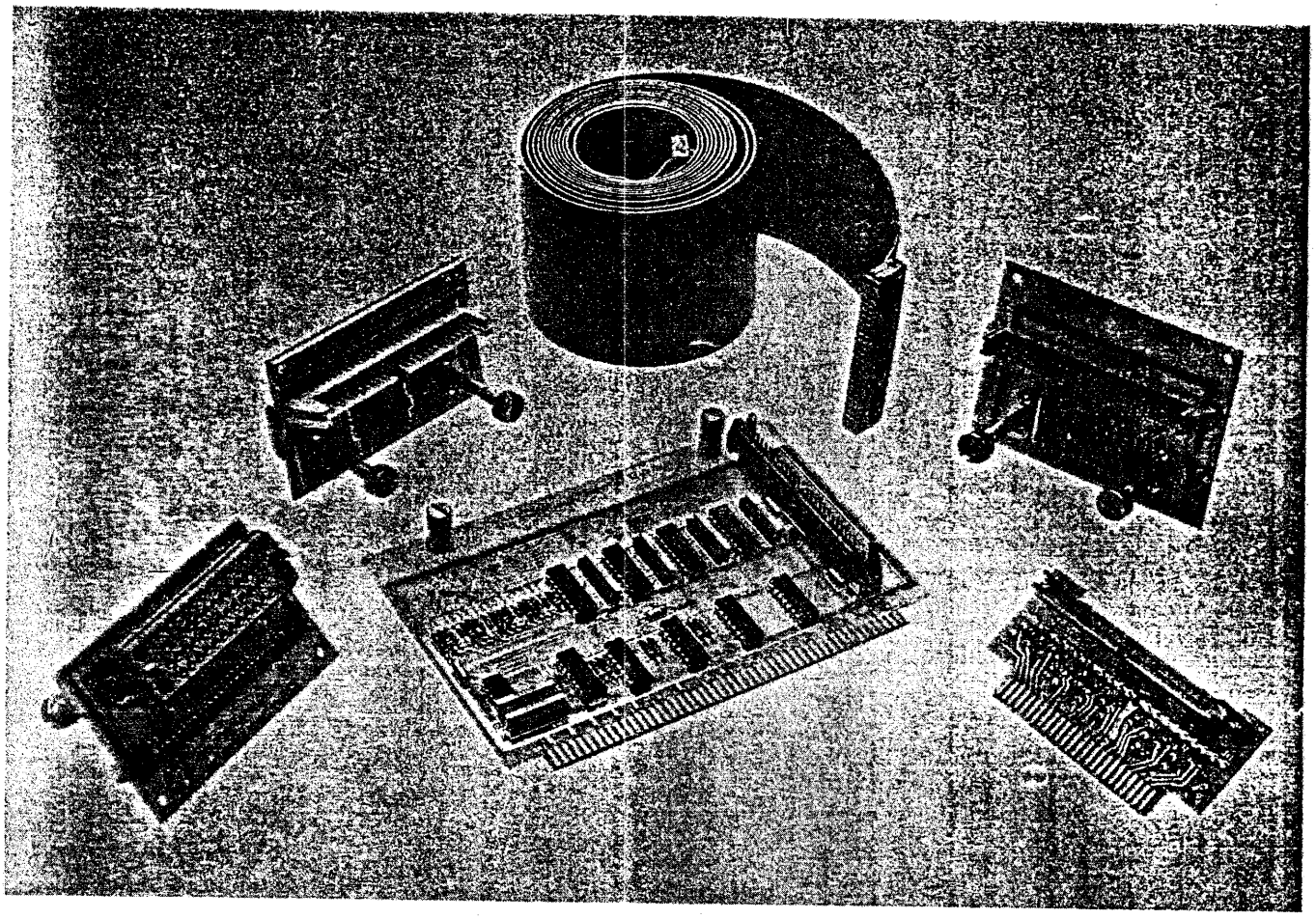


Figure 1–2 Disc Drive Cable and Adapter Assemblies

SECTION 2
INSTALLATION AND OPERATION

2.1 INSTALLATION

This section contains general information required for installation and operation of the DI-C03 controller. Consult the appropriate Applications Manual for details related to a particular disc type.

2.1.1 General

A major advantage of the DI-C03 is its simplicity of installation. Since it is completely contained on a single quad height board, it is physically installed the same as a standard LSI-11® quad interface board.

The user is referred to the DEC® Microcomputer Handbook, 1977-78, Second Edition, Section 1, Chapter 6 for specific checklist items which should be observed in the installation of standard LSI-11® components as well as the DI-C03 controller. Initial problems with the disc controller when imbeded in a system are, more often than not, the result of failure to observe all necessary installation procedures for all system elements, not just the disc controller. Often, various oversights will not be detected with some system elements connected and will appear only with the addition of new components. Some specific steps to avoid often-incurred problems of a general nature are noted below:

(1) Verify that the capacity of the power source is not exceeded, and that the source meets the tolerances specified for the microcomputer (and any other system elements of a special nature). An overloaded power source may produce intermittent failures which are difficult to detect.

(2) Insure that the bus interrupt and DMA grant daisychain lines are properly propagated. Unused option slots should have these lines (BIAK and BDMG) jumpered.

(3) Verify that pins DK1 and DL1 are jumpered together (the crystal oscillator on the board is connected via these pins). Note: If a nonstandard backplane is used, this is a necessary step.

(4) Check to see that all boards in the processor are properly oriented and that boards and drive cables are properly seated in the connectors.

(5) Insure that all necessary signals, including power and ground inputs, are connected as required to the backplane assembly.

(6) Check all option switches, option jumpers, and other variable items for proper settings/connections; consult the reference manual for each specific item for this purpose.

(7) If the system contains a REV11 or a TEV11, verify that the manufacturer's ECO. No. M9400-00007 has been installed (refer to Application Note No. C03514002).

2.1.2 Inspection

A visual inspection of the unit is recommended after unpacking. Specific checks should be made for such items as bent or broken pins or component leads, damaged components, or any other visual evidence of physical damage. The cable and associated drive adapter unit (if included) should likewise be visually inspected prior to installation.

The simplicity of the controller board makes such visual inspection most worthwhile because physical damage incurred in shipment will usually be obvious. Should any damage be detected, you may wish to immediately return the unit for repair prior to further handling.

2.1.3 Installation

After visual inspection, prior to insertion in the computer assembly, it is recommended that the controller be checked for proper configuration. The optional selections on the board which control configuration are:

- Slide switch setting (Tables A-2 and A-3).
- Jumper pin E1-E5 wiring (Table A-5).
- Crystal frequency (Table A-5).

In some cases, the proper adapter board assembly and drive cable terminators for the drive being interfaced must be available.

Appendix A of this manual contains reference tables which permit a convenient check of these configuration settings.

Physical installation of the controller is simple: select the proper slot and insert the board with components oriented in the proper direction.

CAUTION

An attempt to force the board into a slot with components facing in the wrong direction may damage the backplane connectors.

CAUTION

Always insert and remove the board with computer power OFF to avoid possible electrical damage to board components.

It is strongly recommended that the general installation hints given in Section 2.1 of this manual, plus the recommendations and checklist items contained in the DEC® Microcomputer Handbook (Section 1, Chapter 6), be double checked in all cases. In addition, installation requirements for other foreign (Non-DEC) devices in the system should also be thoroughly reviewed and observed. Most installation difficulties prove to be failure to observe a rule or requirement given in these guides rather than the presence of a defective system component.

The drive is connected by inserting the drive cable into the drive interface connector on the controller board. The other end of the drive cable is connected to the adapter board (if required), and that assembly is installed into the drive. Generally, a terminator is required at the physical end of the drive cable. The adapter board supplied by Dataram will contain the proper components for physical connection, signal conditioning, termination, and daisy-chaining. Consult the appropriate Dataram Applications Manual for details of installation for a particular make and model of disc drive.

CAUTION

Use care when inserting into and removing from the drive cable connector because the connector material can be easily damaged. A connector tool is available from the manufacturer and is recommended.

After physical installation of the controller and connection of the drives, make a final check to insure that the board is properly seated, that all necessary cable connectors are secure, and that required termination has been installed.

> **NOTE**
>
> Pin 1 of the cable is denoted by a diamond shaped mark on both cable connector and the circuit board connectors. This diamond also corresponds to conductor number 1 which is marked with a black stripe. Proper orientation of the cable is necessary.

Figure 2-1 shows a typical installation in a system chassis.

2.2 OPERATION

After installation and initial checkout, there are no further steps required to operate the controller per se; only the usual procedures used for computer console, software, and disc drive initialization and control are needed since there are no separate controls or indicates on the controller itself.

After installation, it is recommended that diagnostics be run to insure that the controller/disc drive subsystem is operating properly. Refer to Application Note No. C03514001 for diagnostic application information.

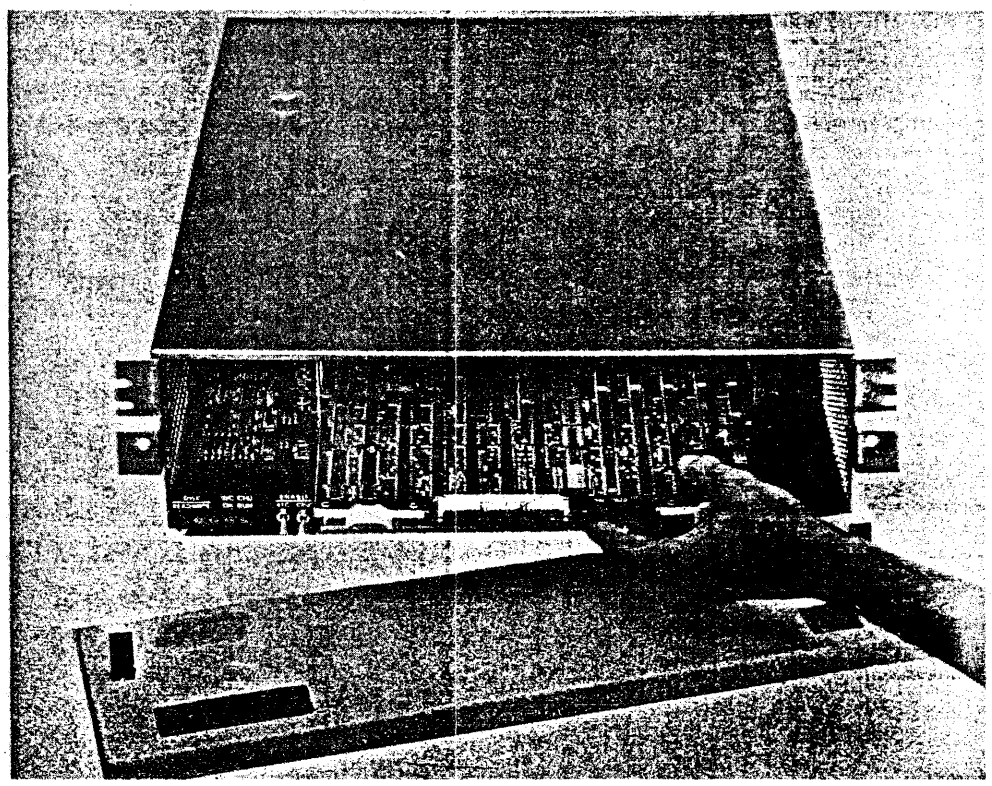


Figure 2–1 Model C03 System Installation

SECTION 3
TECHNICAL DESCRIPTION

3.1 GENERAL

The Dataram Model C03 emulates the functional capability of the DEC®RK 11-D Controller and one or more DEC®RK-05 disc drives. The controller is capable of operating with most of the available industry standard disc drives in the 2.5-20 megabyte capacity range. Up to four physical disc drive units may interface to the controller by means of a 50-conductor flat daisy-chained cable. A block diagram of a typical multi-drive installation configured around the DI-C03 is shown in Figure 3-1.

3.2 FUNCTIONAL DESCRIPTION

This section presents a functional description of the DI-C03 Controller. It includes hardware and software details typically required for application and field-level maintenance of the system.

3.2.1 Block Diagram

A block diagram of the controller is shown in Figure 3-2. The heart of the system is a fast bipolar microprocessor incorporating such features as a powerful multi-function/address command word, 8-bit common data bus, internal high-speed storage registers, and sophisticated control memory interrupt and addressing architecture. This unit performs all control sequences required to transfer data, commands, and status between the LSI-11®bus and the disc drive daisychain. Control inputs received from the LSI-11® and the disc drive(s) are interpreted as status inputs by the microprocessor which executes programmed sequences to transfer data, address and status and to issue control signals to the appropriate I/O devices at the proper time.

The microprocessor is supported by signal transceivers and buffer registers in which very high speed operations are executed. In particular, the 16-byte FIFO performs high-speed parallel-to-serial/serial-to-parallel conversions and in addition queues data bytes to avoid data overflows caused by latency times on the computer bus or in the disc drives. The D register is a 2-byte buffer used to hold address, data, and interrupt vectors transferred between the controller and the LSI-11.

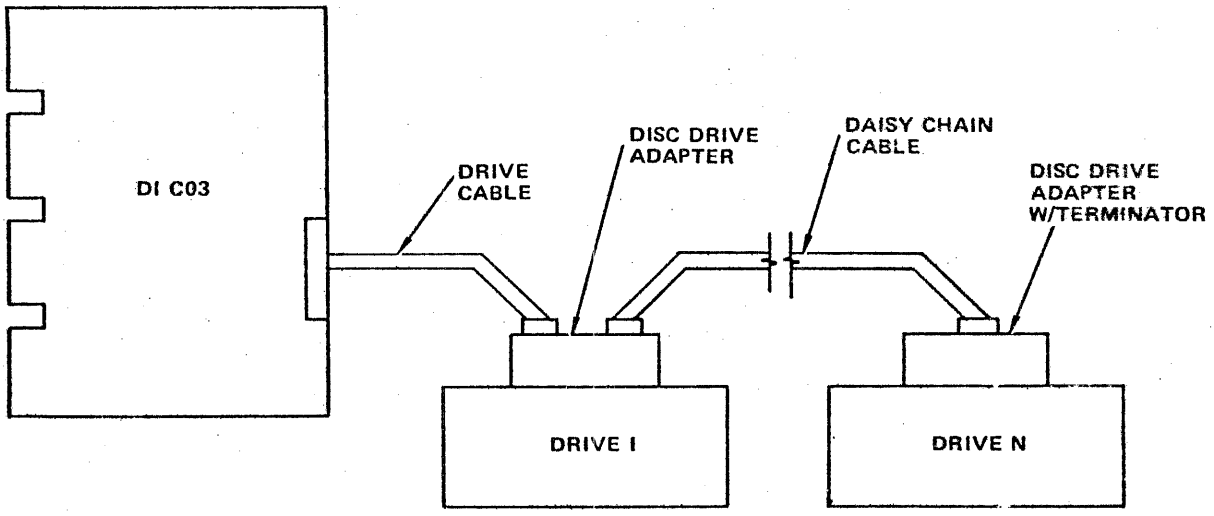


Figure 3-1 Typical System Configuration

3.2.2 Disc Interface

The interface to the disc drive(s) attached to the controller is via a set of interface lines which are common (at the controller) in definition, function, and electrical characteristics, regardless of the make and model of drive being used. As shown in Figure 3-2, the interface elements are:

(1) The 16-byte FIFO which: (a) converts parallel data bytes on the controller data bus side to a serial bit stream on the disc side; (b) provides a queueing buffer to accommodate instantaneous timing differences in the data transfer rates between the disc drive and the computer; and (c) is used to generate precise preamble read timing related directly to disc drive speed and bit packing density.

(2) Disc input register which stores sector count and attention inputs from the drive;

(3) Disc status inputs which are input to the microprocessor test multiplexer for interpretation by the microprocessor program;

(4) Disc output register which stores select, address, and control line parallel outputs to the disc.

A summary of the disc cable interface signal names, mnemonics, and connector pin numbers is given in Table A-1.

3.2.2.1 Disc Interface Connector

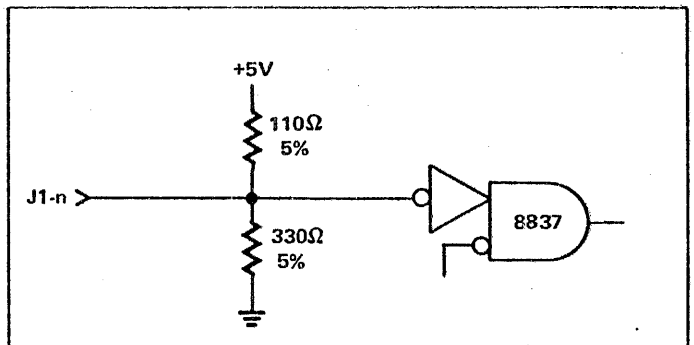
The controller uses a 3M, 50 pin, flat cable connector, 3M P/N 3496-1002. The recommended cable is a 50 conductor flat cable with a built in shield ground plane exibiting a characteristic impedance of 80 ohms (3M P/N 3476/50). The disc drive end of the daisy-chain cable must terminate all signal lines with a 110 ohm, 5% resistor to +5 volts and a 330 ohm, 5% resistor to ground. It is recommended that the total drive cable length to all drives not exceed twenty-five (25) feet.

3.2.2.2 Input Circuits

(1) Parallel inputs to the disc input register are not terminated in the controller; the input receiver for these signals is a 74S240. The signals are:

(4) Attention Lines (ATTN1*—ATTN4*)
(4) Sector Address (SA1*—SA8*)

(2) Other inputs (disc status to the microprocessor test multiplexer) are terminated as shown below into an 8837 receiver:



DISC STATUS INPUT TERMINATION

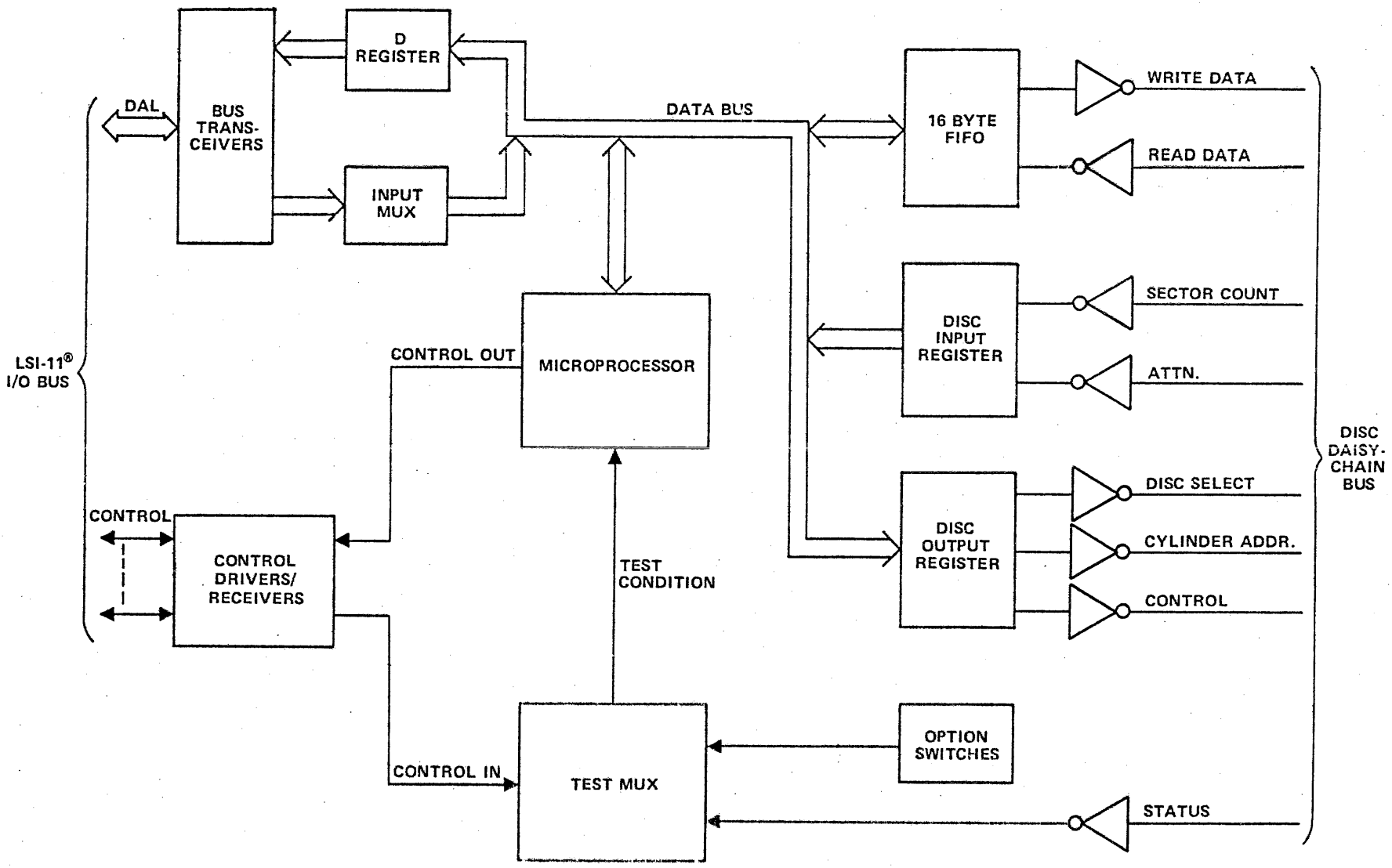


Figure 3-2 C03 Block Diagram

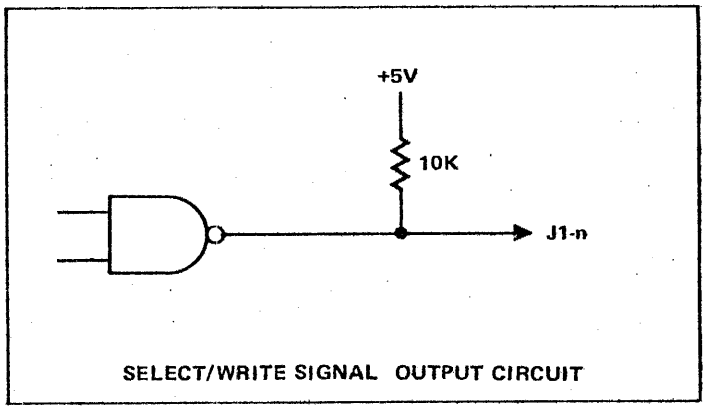
3.2.2.3 Output Circuits

(1) All outputs to the disc except those given in 3.2.2.3(2) below are driven by 74S240 line drivers.

(2) The following signals:

(4) Unit Select (SELU1*—SELU4*)
(1) Disc Select (REMVD*)
(1) Write Data and Clock (WDCK*)

are driven by a 75452 open collector driver with a 10K pullup resistor to +5V.



SELECT/WRITE SIGNAL OUTPUT CIRCUIT

3.2.2.4 Lines to Disc Drive (Levels are all voltage levels.)

(1) **Unit Select Lines:** SELU1—SELU4
A low level on one of the four (4) unit select lines selects a disc drive. The select lines are a decoding of bits 13 and 14 of the RKDA register (refer to Paragraph 3.3.2.1).

(2) **Disc Select (Removable Cartridge):** REMVD
For a dual platter drive, a low level selects the removable cartridge, and a high level selects the fixed disc.

(3) **Head Select (Top Head):** TOPS
A low level selects the upper surface head; a high level selects the lower surface head.

(4) **Cylinder Address:** CA1—CA256
These eight (8) lines are used to transmit the cylinder address to the drive. A low level represents a binary 1-bit. The cylinder address lines are reset by the controller to a high level except when the controller is commanding the drive to perform a seek. For drives operating at 100 tpi, the cylinder address is equal to the contents of bits 12-5 of the RKDA register (refer to paragraph 3.3.2.6). For drives operating at 200 tpi, the cylinder address is equal to twice the contents of bits 12-5 of the RKDA register plus the low-order drive number bit (bit 13 of RKDA). (This places the even numbered drive on even cylinders and the odd numbered drive on odd cylinders.)

(5) **Strobe (Cylinder Address Strobe):** STROBE
This line is used to strobe the Cylinder Address and Restore lines in the selected disc drive, and to initiate a seek operation. The Strobe pulse is a low level which starts a minimum of 0.2 microseconds after the Cylinder Address and Restore lines are set up, and has a minimum duration of 1.0 microseconds. The Cylinder Address and Restore lines remain stable for a minimum of 0.4 microseconds after the Strobe.(1)

(6) **Restore (Return to Zero Seek):** RESTOR
A low level causes the drive head positioner to seek cylinder 0 (zero). If it is accompanied by Strobe, this line will go to a high level within 1 microsecond of Strobe.

(7) **Read Gate:** RDGT
A low level enables the Read Clock and Read Data signals to the controller. This signal is turned on 53 ± 5 microseconds (for 2400 rpm operation) or 85 ± 5 microseconds (for 1500 rpm operation) after the Sector Mark, and is turned off sometime after reading the checksum.

(8) **Write Gate:** WTGT
A low on this line turns on write current in the selected head. The first Write Clock pulse occurs one-quarter of a bit period later. The Write Gate is turned on approximately 10 microseconds after the Sector Mark. The Write Gate is turned off 8 bit times after writing the checksum.

(9) **Erase Gate:** ERGT
A low on this line turns on erase current to the selected head. It is turned on at the same time as the Write Gate and is turned off 15 microseconds after the Write Gate.

(10) **Write Data and Clock:** WDCK
This line transmits the double frequency encoded clock and data information when the Write Gate is on. Low level pulses are approximately one-fourth of the bit period.

(11) **Write Protect:** WTPRO
A 1 microsecond low pulse is placed on this line when the controller is performing a write lockout function.

3.2.2.5 **Lines from Disc Drive** (Levels are all voltage levels.)

(1) **Drive Ready:** DRDY
A low level on this input signifies that the drive is ready. No operations should be attempted on a drive which is not ready; if an operation is commanded, a nonexistant drive error condition will result.

(2) **Ready to Seek, Read or Write (On Cylinder):** RWS
A low level on this input signifies that the drive is in a ready condition and is not seeking. This input must go to a high level within 1 microsecond of the leading edge of Strobe unless the present cylinder is readdressed or an illegal cylinder address is given. This signal is used to determine when a new function may commence or when functions may continue after performing a seek.

(1) This timing for STROBE holds for all drives except the Diablo Mod. 30 series. In that case, STROBE is reset by receipt of an address acknowledgement signal from the drive which occurs 22.5—47.5μs after the leading edge of STROBE.

(3) **Logical Address Interlock:** LAIL
A low level on this input signifies that an illegal cylinder address was rejected by the drive and the seek cannot be executed. The level must be at least 9.5 milliseconds in duration and occur within 0.5 microseconds of the leading edge of the Strobe.(2)

(4) **Seek Incomplete:** SINC
A low level on this input signifies that a malfunction has caused an incomplete seek operation. This low level must be at least 0.5 millisecond in duration.

(5) **Write Check:** WTCH
A low level on this input signifies a write check and prevents any further operations except a Reset Drive command.

(6) **Read Clock:** RDCK
A low pulse with a duration of 15-60% of the clock period. The controller uses the leading edge of the pulse.

(7) **Read Data:** RDATA
A low pulse with a duration of 15-60% of the clock period which occurs with the clock input at a high level signifies data 1-bit. The clock and data pulses may overlap by 10% of the clock period.

(8) **Attention Lines:** ATTN1—ATTN4
A low level input to one of the four (4) attention lines signifies that the corresponding drive has completed a seek operation. These lines must go high within 2.0 microseconds after Strobe if the drive is to perform a seek.(3)

(9) **200 TPI:** T200
A low level on this input signifies that the drive is configured for 200 tracks per inch operation. A high level signifies 100 tpi operation. This input is interrogated by the controller only for a drive which is in a ready condition.

(10) **Write Protect Status:** DWP
A low level on this input prevents any write operation and will cause an error condition if a write operation is attempted.

(11) **Sector Mark:** SM
A low level pulse of at least 5 microseconds on this input signifies the sector mark. The leading edge of this pulse is used as a reference by the controller.

(12) **Sector Address:** SA1—SA16
These five (5) lines input the current sector under the heads. A low is a binary 1-bit. The sector address must be stable 3 microseconds after the sector mark.

(2) This signal is used as the Address Acknowledge input for the Diablo Mod. 30 series.

(3) The Attention Lines are not implemented in the Diablo Model 30 series.

3.2.3 LSI-11 Interface

The DI-C03 interfaces directly to the internal I/O bus of the LSI-11 (refer to Paragraph 1.4 for a description of the physical bus interface and definition of the module contact finger identification). The following types of I/O transfers occur between the controller and the processor and/or memory modules via the bus:

(1) Programmed I/O transfers. These operations are executed by either single or double operand instructions; transfers to the controller may be either an 8-bit byte or a full 16 bit word. Programmed transfers are always for the purpose of exchanging control and status between the controller and the processor. The controller executes the following specific types of programmed bus cycles: DATI, DATO, DATOB, DATIO, DATIOB.

(2) DMA transfers. All data read or write transfers, including read check and write check operations, are performed as full word DMA transfers between the controller and a memory device on the bus. The DI-C03 acts as the bus master controlling the transfer in all cases, using control information previously supplied by programmed instructions from the processor.

(3) Interrupts. The controller generates several types of interrupts to the processor to flag the occurrence of various events (end of block, error condition, etc.). The controller generates a common interrupt vector to location 220_8 for all interrupt conditions.

3.2.3.1 Device Priority

Controller priority for DMA and interrupt requests is established by its physical position on the bus. The selection of device priorities is a system consideration. Since a disc memory involves relatively high peak transfer rates, and because delays in servicing data transfer requests may result in loss of information, the disc controller will normally be located in a relatively high priority position. The board can physically mount in any quad height card slot after the processor.

3.2.3.2 Bus Signals

The LSI-11 bus signals to and from the DI-C03 via the A, B, C, D connectors are tabulated in Table A-7. The following should be noted.

(1) All data and control signals used by the controller are interfaced via the A and B connectors, even though the unit plugs into all four connectors.

(2) Power and ground connections are made via standard pins in the C and D connectors. In addition, the following jumper connections are made via etch on the DI-C03 board (but not on the standard LSI-11 backplane):

PINS	SIGNALS
CR2 to CS2	BDMGIL to BDMGOL
CM2 to CN2	BIAKIL to BIAKOL

(3) The controller oscillator signal, OSC, appears on pins DK1 and DL1 which must be jumpered together on the backplane. This connection is incorporated in the H9270 backplane but may not be made on a custom backplane.

(4) Designated spare pins BP1, AA1, and AB1 are implemented in the DI-C03 controller with signals designated BIRQ5L, BIRQ6L, and BIRQ7L respectively. These pins will be used to permit installation of the DI-C03 in follow-on versions of the LSI-11 which provide interrupt levels 5, 6 and/or 7.

(5) Pins AC1 and AD1 are implemented with extended address bits BAD16L and BAD17L; these signals will be used to permit the DI-C03 to be installed in follow-on versions of the LSI-11 which will provide extended addressing beyond 32K words.

3.2.3.3 Interrupts

The controller generates an interrupt request upon the occurrence of several conditions as defined in paragraph 3.2.4.5.

All interrupt conditions cause an interrupt at vector location 220_8.

The basic LSI-11 has a single interrupt level which is physically located on the pins assigned to level 4 in the PDP-11 computer series. The DI-C03 is configured with on-board jumper points to permit selection of other interrupt levels (5-7) for follow-on LSI-11 series computers which provide a multi-level interrupt structure.

3.2.3.4 Intialization and Power Sequencing

The controller responds to an Initialize (INIT) signal on the LSI-11 bus by executing a Control Reset function (paragraph 3.2.4.1). Response is immediate and will terminate any function being executed by any drive except one which is executing a Write Operation. In this case, the controller will continue to write Zero bytes to the end of the current sector and will then execute the Control Reset for that drive. No further transfers take place over the bus after the INIT, and the zero bytes are generated by the controller itself.

The controller monitors the dc power status line on the LSI-11 bus, BDCOKH (DC Power OK). In the event that BDCOKH falls, indicating that system DC power is unstable, the controller will (if able) terminate and clear the controller unconditionally. The DI-C03 has its own on-board dc power sensing circuit, independent of the bus signal. When dc power to the controller is stabilized, it will perform an automatic initialization so that it is ready to execute the initial software commands received.

3.2.3.5 Electrical Specifications

The DI-C03 bus interface circuitry conforms to the bus specifications for the LSI-11 The logic levels specified by the manufacturer are:

Input Levels

TTL Logical Low: +0.8 Vdc max.
TTL Logical High: +2.0 Vdc min.

Output Levels

TTL Logical Low: +0.4 Vdc max.
TTL Logical High: +2.4 Vdc min.

The DI-C03 uses the following device types for the LSI-11 bus interface:

Receiver: National 8837. Equivalent types include Signetics 8T37, Motorola 3437.

Driver: TI 7438.

Transceiver: National 8641. Equivalent types include Signetics 8T38, Motorola 3438.

A standard unit load as specified by the manufacturer is equal to one receiver and two drivers and less than 10pf of circuit board etch. At nominal termination to 3.4V, this would represent approximately 130μa leakage in the logical high state.

All bidirectional lines terminate in the DI-C03 to an 8641 transceiver which presents one receiver and one driver load. All unidirectional inputs to the C03 are terminated to a single 8837 receiver, and all unidirectional outputs from the C03 are driven by a single open-collector 7438. Thus, the DI-C03 presents less than a single unit load (as defined) to the LSI-11 bus.

3.2.4 Functional Operations

This section defines the functional operations and capability of the DI-C03 controller. The programming considerations related to these functions, including a definition of the control and status register bit assignments referenced in this paragraph, are covered in Section 3.3.

3.2.4.1 Control Functions

The controller executes a total of eight different functions: four control and four data transfer. One function at a time is commanded by a programmed instruction by setting up the appropriate function code in the RKCS register (refer to paragraph 3.3.2.3) and setting the GO bit (Bit 00 of RKCS). A firmware poll feature enables the system to execute simultaneous Seek and/or Drive Reset functions on separate drives.

(1) Control Reset. This function initializes the controller and effects the bits of the seven programmable registers as follows:

RKCS 07 (READY)—Set
RKDS 00-15—Unaffected
All other register bits—Cleared

The function is executed immediately except when the Write Gate is on, in which case the write operation will continue to the end of the sector. This function will cause an immediate abort of any other function in process. However, if Control Reset is executed while the drive heads are in motion, a hard error will result. Therefore, RKDS 06 should be set (R/W/S RDY) before executing. The Control Reset is the only function which can be performed on a drive after hard error condition (refer to paragraph 3.3.2.2), and this function must be performed before the drive can be used again.

(2) **Seek.** This function directs the selected disc drive to move its head mechanism to the cylinder address specified by RKDA. When this portion of a Seek has been initiated, the controller returns to the Ready state (RKCS 07 is set). If the specified cylinder address is greater than 312_8, the function is aborted and bit RKER 06 (nonexistent Cylinder) is set; the state of RKCS 06 (Interrupt Done Enable) determines whether a program interrupt will be generated. When the selected disc drive completes the Seek function by moving its head mechanism to the desired cylinder, RKDS 06 (R/W/S RDY) is set.

(3) **Drive Reset.** The Drive Reset function causes the selected disc drive to move its head mechanism to cylinder address 000 and to reset all error status lines. RKDS 06 (R/W/S RDY) is set at the completion of the function.

(4) **Write Lock Function.** The Write Lock function causes the Write Protect line to the drive to be pulsed.

(5) **Write Function.** For a Write function, the controller first performs a seek operation (referred to as an "implied seek;" note that an interrupt will not be generated as a result of this seek operation). When that is completed, the next header word is read and checked for correct cylinder identification (cylinder address).

If the cylinder address read from disc is correct, the controller begins the Write operation when the Sector Counter (RKDA 00 through 03) equals the Sector Address (RKDS 00 through 03), hereafter referred to as SC = SA. A preamble consisting of 15 words of zeros is written followed by a sync bit (refer to paragraph 3.4.1.). Then the header word is rewritten automatically, followed immediately by the data words for the sector. As the data words pass through the controller, a one-word checksum word is calculated and automatically written after the last sector data word, and the checksum is followed by one word of zeros for the postamble.

If the cylinder address initially read from disc is incorrect, the controller makes 15 additional read attempts to establish the correct cylinder address before aborting the function and setting RKER 12 (Seek Error).

A word count (RKWC) overflow (i.e. last word of block has been transferred) at any time from the start of the Write function stops the DMA data transfers and sets RKCS 07 (Ready, RDY) at the end of the current sector. If the RKWC has not overflowed at the end of a given sector, the write function is continued at the next contiguous sector. If the last word of the last sector of the disc cartridge is transferred and RKWC has not overflowed, then RKER 14 (OVR, Overrun) is set, indicating that an attempt was made to exceed the capacity of the drive.

(6) **Read Function.** For a Read function, the controller first performs a seek operation ("implied seek" as defined above). When that is completed, the controller waits for SC = SA, then reads and checks the header word. If the cylinder address read from disc is correct, the controller continues reading the sector and DMA transfers the data words onto the LSI-11 bus. If the cylinder address initially read from disc is incorrect, the controller makes 15 additional attempts to establish the correct cylinder address before aborting

the function and setting RKER 12 (Seek Error). As the data words of a sector pass through the controller, a one-word checksum word is calculated and compared with the checksum read from the disc drive. If there is a discrepancy between the two checksums, RKER 01 (Checksum Error) is set, and the controller reaction is determined by RKCS 06 (IDE, Interrupt on Done Enable) and RKCS 08 (SSE, Stop on Soft Error). A word count (RKWC) overflow at any time from the start of the Read function stops the DMA data transfers and sets RKCS 07 (RDY) at the end of the current sector. If the RKWC has not overflowed at the end of a given sector, the function is continued at the next contiguous sector.

(7) **Write Check Function.** The Write Check function is used to compare the contents of a continuous block of memory to the contents of a continuous block of data on a disc cartridge. The controller first performs the "implied seek" function as defined above, just as for a Write function, and then reads and checks the next header word. If the cylinder address is correct, the controller waits for SC = SA, then begins reading the rest of the sector (Data and Checksum) while simultaneously performing a DMA transfer of a word from memory for each data word read from disc. Each data word read from the disc drive is compared, word by word, with the data read from memory via the LSI-11 bus. The data checksum read from disc is compared with a checksum calculated by the controller for the data read from memory. If any bit is found to be in error, RKER 00 (Write Check Error) is set. Controller reaction is then determined by RKCS 06 (IDE) and RKCS 08 (SSE). The Write Check function may be performed on a short sector (less than 256 data words) as long as the number of words checked is equal to the number of words previously written into the sector.

(8) **Read Check Function.** The Read Check function is identical to a normal Read function, except that no data words are transferred from the disc to memory by the controller. A checksum is calculated by the controller and compared with the checksum read from the disc drive. Error conditions and interrupts are generated in the same manner as in the Read function. This function enables the program to verify in advance that a given block of data is readable and error free. The Read Check function must be performed on a whole-sector basis only.

3.2.4.2 Firmware Poll

The controller is capable of permitting any or all physical drives to perform a Seek or Drive Reset function simultaneously. The firmware poll feature in the Disc Control identifies the logical disc drive in RKDS 13-15 (DRIVE IDENT) for any disc drive that has completed a Seek or Drive Reset function. This poll causes an interrupt if RKCS 06 (IDE) is set, the controller is in the Ready state (RKCS 07 set), and the controller is not already attempting to initiate an interrupt from other function. If two or more disc drives complete a Seek or Drive Reset function simultaneously, the controller interrupts once for each disc drive and identifies each in turn to the RKDS. Back-to-back interrupts will also result from directing the heads to a cylinder over which they are already positioned, with the first interrupt coming from the initiation of a Seek function and the second coming from notification from the firmware poll that the heads are at the desired cylinder address. In either situation, if the processor interrupt status is

not raised by the interrupt service routine to a level equal to or greater than that of the controller, a second interrupt will occur immediately thereafter which interrupts the first service routine. The DI-C03 controller can be set to respond to Seek and/or Drive Reset commands for multiple logical drives which are on the same physical drive, even though the heads will physically respond only to the first command (refer to paragraph 3.2.5.1).

3.2.4.3 200 TPI.

When the drive is configured for 200 tracks per inch (200 tpi), there will be 406 tracks per surface. The even numbered tracks are assigned to even logical drive numbers, and the odd tracks are assigned to odd logical drive numbers. Operation at 200 tpi is specified either by setting Switch 8 to the ON position or by assertion of the T200 signal by the drive being accessed.

3.2.4.4 Interrupt Conditions.

A program interrupt request is generated if RKCS 06 (IDE) is set and one or more of the following conditions exist:

(1) Hard error (RKCS 14 Set)

(2) Soft error (RKER 00 or RKER 01 Set) and RKCS 08 is set.

(3) A data transfer function (Read, Read Check, Write, Write Check) is completed.

(4) A Seek or Drive Reset function is accepted by the controller.

(5) A Write Lock function is initiated.

(6) Completion of a polling operation.

The identity (RKDS 15-13) and the Search Complete status bit (RKCS 13) for the interrupting drive are updated at the time of interrupt acknowledge from the computer when the controller supplies the interrupt vector to the computer.

3.2.4.5 Power Fail.

If the disc controller senses a loss of AC power, the controller waits for AC power to return before starting operation on the next sector. If AC power is sensed before a seek operation, a Drive Error and Drive Power Low error condition are generated and the current function is aborted.

3.2.4.6 Bus INIT.

When the controller receives an INIT from the bus, it causes a DC reset of the controller if the Write Gate is not on. If the Write Gate is on, the balance of the current sector is filled with zero bytes, and the reset occurs as soon as the controller turns the Write Gate off. To facilitate power-up clear, the DCLO on the bus is used to reset the controller, including the Write Gate flip-flop.

3.2.4.7 Function Timing.

If the controller is not busy, it responds to a new function (GO, RKCS 00 set) within 10 microseconds of receiving the function. When the controller is busy, a new function (except Control Reset) is not initiated until the completion of the current function. If the controller is not writing a sector, the Control Reset is initiated within 10 microseconds; if the controller is in the process of writing a sector, execution of Control Reset is delayed until the Write Gate is turned off.

3.2.5 Option Switches

Eight option switches are contained on switch SW1 located at the top of the controller (refer to Figure 1-1). The switch numbers and ON position are marked on the switch. Five of these switches are used (three are unused) in connection with the clock crystal frequency and jumper selections to configure the system for various drive types/capacities and to select other optional functions. A complete description of the switch functions is given below, with a summary given in Table A-2.

3.2.5.1 Switch 1 — Logical Drive Status.

Normally (SW1-1 OFF) the controller will reflect the Read/Write/Seek status of a selected physical drive, regardless of which logical drive is addressed. Since there may be multiple logical drives on a single physical drive, the operating software will encounter a busy condition if a logical drive is accessed on a physical drive where another logical drive is performing an operation.

If SW1-1 is placed in the ON position, the controller will reflect the Read/Write/Seek status of the selected logical drive. Thus, even if a physical drive is busy performing a function, selection of a non-busy logical drive on that physical drive will result in a ready status condition in the status register. However, if a function is issued to that logical drive, it will be ignored since the physical drive is already busy, but the controller will generate the normal completion interrupts for all such commands to insure that no software hangups occur. These interrupts will occur at the time the physical drive completes the function in process.

If a subsequent Read or Write operation is issued to a logical drive for which a Seek was ignored because of the previous condition, the head will not be on the desired cylinder. Since the controller automatically performs a seek function before initiating a Read or Write operation, the head will be moved at the time such operation is commanded.

3.2.5.2 Switch 2 — Dual Platter.

If SW1-2 is in the OFF position, the controller assumes the drive is a two-platter configuration. If a drive has only a single platter, SW1-2 must be placed in the ON position.

3.2.5.3 Switch 3 — Configuration 15.

Placing SW1-3 in the ON position forces the controller polling logic to operate in configuration 15 (refer to Table A-3). This is the only use for this switch, and normally it should be in the OFF position.

3.2.5.4 Switch 4 — High Speed Seek.

In normal operation (SW1-4 OFF) the sector numbers transmitted to the controller by software will match the physical sectors on the disc (as referenced to the sector mark) for all logical cylinders. Because of delays in positioning the head when moving from cylinder-to-cylinder, a full rotation of the disc is usually lost when crossing a cylinder boundary.

If SW1-4 is set to ON, the controller will automatically introduce a 6-sector offset between the logical (software) sector and the physical sector on odd logical cylinder numbers; i.e. on cylinder numbers 1, 3, 5, etc., logical sector 0 corresponds to physical sector 6, logical sector 1 corresponds to physical sector 7, etc. Thus, when multiple sector operations cross cylinder boundaries,

the next physical sector will be located within half a revolution of the disc and can result in considerable block transfer time reductions in some applications.

3.2.5.5 Switch 8—200 TPI.

With SW1-8 in the ON position, the 200T* status line to disc connector J1-12 is forced to the asserted state, and the controller will treat all drives as operating at 200 tpi track densities. Since some 200 tpi drives do not provide this signal, SW1-8 should be set ON when all physical drives are 200 tpi.

If all physical drives are not 200 tpi, then SW1-8 must be OFF. For systems containing drives with mixed track densities, the 200 tpi drives must assert the 200T* signal when the drive is selected, and the 100 tpi units must never assert this signal. Units at 200 tpi which do not provide the 200T* signal either cannot be used in mixed systems, or a special adapter board or other disc logic adaptation must be provided.

3.2.6 Maintenance Connector

The Maintenance Connector (J2) is a 14 pin, dual in-line socket located at the top of the board (refer to Figure 1-1). Its primary purpose is to provide a tester interface to the disc controller's microprocessor. Table A-7 is a summary of the maintenance connector signals. A description of these signals, including recommended interface circuits for use of these signals, is given below.

3.2.6.1 Output Lines.

(1) Clock (CKEXT*)

This is a free running version of the microprocessor clock which is in the frequency range of 5.0 to 3.84 MHz, depending on disc drive rpm and track bit packing density. The positive going edge is the start of a microprocessor cycle. External termination for the CKEXT* line should be a 220 ohm resistor to +5 volts and a 330 ohm resistor to ground. The recommended receiver circuit is a 74S240.

(2) Reading (READING*)

This signal is derived directly from the Read Gate signal (on J1) through a 1K ohm resistor. Its intended purpose is to drive an activity indicator light on a system panel. A high impedance receiver, such as a National 8837, is recommended.

(3) Writing (WRITING*)

This signal is derived directly from the Write Gate signal (on J1) through a 1K ohm resistor. Its intended purpose is to drive an activity indicator light on a system panel. A high impedance receiver, such as a National 8837, is recommended.

3.2.6.2 Input Lines

(1) Stop (STOP+)

This signal will stop the disc controller's microprocessor. The transitions of this signal must be synchronized with the clock signal from the disc controller. All transitions of the Stop signal must occur after the positive going edge of CKEXT* and no later than 10 nanoseconds before the negative going edge of CKEXT* as measured at J2.

The recommended driver circuit for the Stop+ signal is either a 74S140 or a 74S240 with a 100 ohm resistor to +5 volts.

(2) Disable Read Only Memory (DISROM+)
This signal will turn off the 3-state outputs of the PROMS on the disc controller board. It is used when an external control memory is connected to the disc controller. The recommended driver circuit for this line is a 74S140.

(3) Disable Pipeline Register (DISPL+)
This signal will turn off the 3-state outputs of the Pipeline Register. It is used to permit external microcommand inputs to be substituted for commands from control memory. The recommended driver circuit for this line is a 74S140.

(4) Reset (EXTRS*)
Grounding the Reset Line will cause the unconditional reset of the disc controller. The recommended driver circuit is an open collector TTL driver such as a 7438.

3.3 PROGRAMMING

3.3.1 Introduction

This section discusses the software interface for the disc controller including device registers and their addresses, the interrupt process, timing considerations, and data format.

3.3.2 Device Register and Address

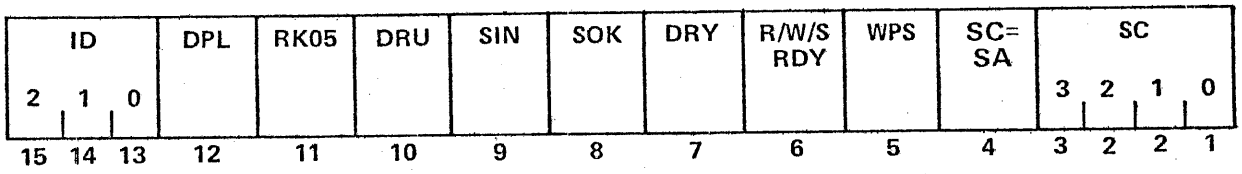
All DI-C03 software control is accomplished by seven (7) device registers. These registers are assigned memory addresses and can be read or written into (except as noted) using instructions that refer to the respective register addresses. Transfers to these registers may be made as full words or as bytes. The seven (7) device registers, their bit assignments, and their memory addresses are defined below. Unassigned and write-only bits are always read as zeros. Any attempt to manipulate unassigned or read-only bits has no effect.

Register Name	Mnemonic	Address	Type
Drive Status	RKDS	777400	Read Only
Error	RKER	777402	Read Only
Control Status	RKCS	777404	Read/Write
Word Count	RKWC	777406	Read/Write
Bus Address	RKBA	777410	Read/Write
Disc Address	RKDA	777412	Read/Write
Data Buffer	RKDB	777416	Read/Write

NOTE: Address 777414 is not implemented but will respond with all zeros if a read is attempted. A write operation will result in a reply to the computer but will have no effect on the controller.

3.3.2.1 Drive Status Register (RKDS) — Address =777400

This is a read-only register containing status of the selected drive.

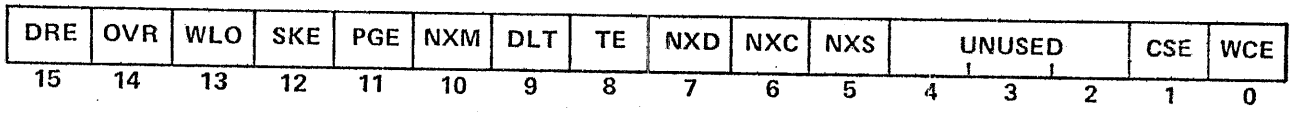


BIT	DESIGNATION	DESCRIPTION AND OPERATION
00-03	Sector Counter (SC)	These four (4) bits contain the current sector address of the selected drive. Sector address 00 is defined as the sector following the sector that contains the index pulse.
04	Sector Countor Equals Sector Address (SC = SA)	When set, indicates that the disc heads are positioned over the disc address currently held in the sector address field (SA), of RKDA, i.e. SC = SA.
05	Write Protect Status (WPS)	When set, indicates that the selected disc is in the write-protected mode.
06	Read/Write/Seek Ready (R/W/S RDY)	When set, indicates that a Seek or Drive Reset function is not in process, and that the drive is ready to accept a new function. Refer to paragraph 3.2.5.1 for use of switch SW1 to select logical or physical drive status.
07	Drive Ready (DRY)	When set, usually indicates that the selected disc drive complies with all the following conditions (not all conditions may be included for a particular drive): **a.** The drive is properly supplied with power. **b.** The drive is loaded with a disc cartridge. **c.** The disc drive door is closed. **d.** The LOAD/RUN switch is set to RUN. **e.** The disc is rotating at a proper speed. **f.** The heads are properly loaded. **g.** The disc is not in an unsafe condition (i.e. DRU, RKDS 10 is not set).
08	Sector Counter OK (SOK)	When set, indicates that the Sector Counter (SC) operating on the selected drive is not in the process of changing, and is ready for examination. If this bit is not set, the Sector Counter is not ready for examination, and a later attempt should be made to read SC.
09	Seek Incomplete (SIN)	When set, indicates that due to some unusual condition, a Seek function cannot be completed. May be accompanied by RKER 15 (Drive Error). Cleared by a Drive Reset function.

10	Drive Unsafe (DRU)	When set, indicates that an unusual condition has occurred and that the disc drive is unable to properly perform any operations. This bit is reset by setting the drive RUN/LOAD switch to LOAD. If the bit is again set when the switch is returned to RUN, it should be assumed that the drive is inoperative and in need of maintenance. May be accompanied by RKER 15 (Drive Error).
11	RK05 Disc on Line (RK05)	Always set to identify the selected disc as being RK05 compatible.
12	Drive Power Low (DPL)	Normally assigned as Drive Power Low (DPL) indicator from RK05 drive. Since the drives used with the DI-C03 do not provide this signal, the controller mcnitors the state of the bus ac power status (BPOKH) and sets DPL if BPOKH is in the unasserted state.
13-15	Identification of Drive (ID)	If an interrupt occurs, these bits will contain the binary representation of the logical drive number that caused the interrupt.

3.3.2.2 Error Register (RKER) — Address = 777402

This is a read-only register containing all error status indicators for the selected drive.



BIT	DESIGNATION	DESCRIPTION AND OPERATION
00	Write Check Error (WCE)	When set, indicates that an error was encountered during a Write Check function as a result of a faulty bit comparison between disc data and memory data. Reset by the initiation of a new function. This is a soft error condition.
01	Checksum Error (CSE)	When set, indicates that an error was encountered while performing a Read Check or a Read function as a result of a mismatch between the checksum read from disc and that calculated by the controller. Reset by the initiation of new function. This is a soft error condition.
02-04	Unused	

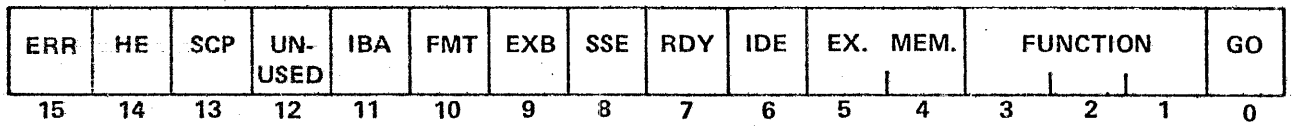
The remaining bits of the RKER are all hard errors, and are cleared only by a BUS INIT or a Control Reset function.

05	Nonexistent Sector (NXS)	When set, indicates that an attempt was made to initiate a transfer to a sector number larger than 13_8.
06	Nonexistent Cylinder (NXC)	When set, indicates that an attempt was made to initiate a transfer to a cylinder number larger than 312_8.
07	Nonexistent Disc (NXD)	When set, indicates that an attempt was made to initiate a function on a nonexistent or not ready drive.

08	Timing Error (TE)	When set, indicates that a loss of drive read clock has been detected.
09	Data Late (DLT)	Set during a Write or Write Check function if the multibuffer file (FIFO) is empty at the time a write clock occurs. Set during a Read function if the multibuffer file (FIFO) is filled at the time a read clock occurs.
10	Nonexistent Memory (NXM)	Set if memory does not respond with REPLY within 10 microseconds after the controller becomes bus master during a DMA sequence. Because of the speed of the disc drive, it is possible that NXM will be accompanied by RKER 09 (Data Late).
11	Programming Error (PGE)	When set, indicates that RKCS 10 (Format) was set while initiating a function other than Read or Write.
12	Seek Error (SKE)	Set if the disc head mechanism is not properly positioned while executing a normal Read, Write, Read Check, or Write Check function. The controller checks sector address 16 times before flagging this error.
13	Write Lockout Violation (WLO)	Set if an attempt is made to write on a disc that is currently write-protected.
14	Overrun (OVR)	When set, indicates that during a Read, Write, Read Check or Write Check function, operations in sector number 13_8, surface number 1 (bottom), of cylinder address number 312_8 were finished, and the RKWC has not yet overflowed. This error flags an attempt to overflow out of a logical disc drive.
15	Drive Error (DRE)	Set if a function is either initiated or is in process when the selected drive is either not ready or is in some error condition.

3.3.2.3 Control Status Register (RKCS) — Address = 777404

This is a read/write register which holds control codes to the controller supplied by the computer and the current state of these control codes, plus control status generated in the controller. Some bits are read only and some are write only as defined below.



BIT	DESIGNATION	DESCRIPTION AND OPERATION
00	GO (Write Only)	Loaded by the program. When set, causes the controller to execute the function contained in bits 01 through 03 of the RKCS (Function). Remains set until the controller actually responds to GO, which may take from 1 microsecond to 3.3 milliseconds depending on the current operation of the selected disc drive; reset when execution is initiated.

01-03 Function (Read/Write)

Loaded by the program with the binary representation of the function to be performed by the controller when a GO command is initiated, reset by BUS INIT. The function is retained until altered by the program or cleared, enabling the user to continue from a soft error condition with GO. A description of each of the eight functions is given in paragraph 3.2.4. The binary function codes are as follows:

Bit 2	Bit 1	Bit 0	Operation
0	0	0	Control Reset
0	0	1	Write
0	1	0	Read
0	1	1	Write Check
1	0	0	Seek
1	0	1	Read Check
1	1	0	Drive Reset
1	1	1	Write Lock

04-05 Memory Extension (MEX) (Read/Write)

Reserved for extended bus addresses used in conjunction with the RKBA. This 2-bit counter increments each time the RKBA overflows. A bus DATO to these bits overrides an RKBA overflow. Loaded by the program and cleared by BUS INIT. Use of these bits is intended for systems which are equipped with a memory larger than 32K words.

06 Interrupt on Done Enable (IDE) (Read/Write)

When set, causes the control to issue a bus interrupt request and interrupt to vector address 220_8 if:

a. A function has completed activity.

b. A hard error is encountered.

c. A soft error is encountered and bit 08 of the RKCS (SSE) is Set.

d. RKCS 07 (RDY) is Set and GO is not set.

07 Control Ready (RDY) (Read Only)

When set, indicates that the controller is ready to perform a function. Set by INIT, a hard error condition, or by the termination of a function. Cleared when GO is set.

08 Stop on Soft Error (SSE) (Read/Write)

If a soft error is encountered when this bit is set:

a. If RKCS 06 (IDE) is reset, all control action will stop at the end of the current sector.

b. If RKCS 06 (IDE) is set, all control action will stop and a bus interrupt request will occur at the end of the current sector.

09 Extra Bit (EXB)

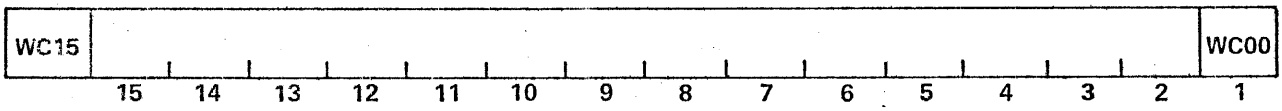
Unused by the DI-C03.

10 Format (FMT) (Read/Write)

FMT is under program control and must be used only in conjunction with normal Read and Write functions. Used to format a new disc pack or to reformat any sector erased due to controller or drive failure. Alters the normal Write operation, under which the header is rewritten each time the associated sector is rewritten, in that the head positioner is not checked for proper positioning before the Write. Alters the normal Read operation in that only the header word is transferred to memory out of each sector read from disc. Header words from contiguous sectors will be read into contiguous memory locations.

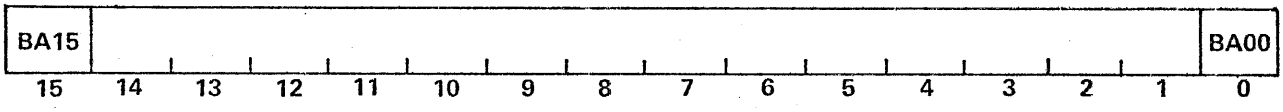
11	Inhibit Incrementing the RKBA (IBA) (Read/Write)	Inhibits the RKBA from incrementing during a normal function. This allows data transfers to occur to or from the same memory location throughout the entire operation.
12	Unused	
13	Search Complete (SCP) (Read Only)	When set, indicates that the previous interrupt was the result of some previous Seek or Drive Reset function. Cleared at the initiation of any new function.
14	Hard Error (HE) (Read Only)	Set when any of RKER 05-15 are set and stops all control action. Processor reaction is dictated by the state of RKCS 06 (IDE) until this bit, along with RKER 05-15, are all cleared either by INIT or a Control Reset function.
15	Error (ERR) (Read Only)	Set when any bit of the RKER is Set. Processor reaction is dictated by the states of RKCS 06 and RKCS 08 (IDE and SSE). Cleared if all bits in the RKER are cleared.

3.3.2.4 Word Count Register (RKWC) — Address = 777406



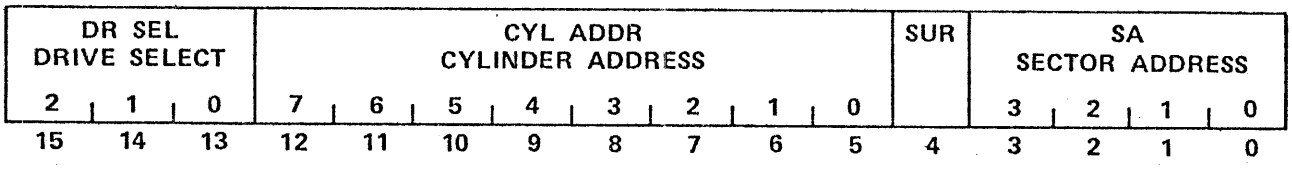
BIT	DESIGNATION	DESCRIPTION AND OPERATION
00-15	WC00-WC15 (Read/Write)	Loaded by the program initially with the 2's complement of the total number of words to be affected or transferred by a given function. The controller increments this register by one after each word transfer. When the register overflows (all WC bits go to zero), the transfer is complete and the operation is terminated at the end of the present disc sector. However, only the number of words specified in the RKWC are transferred.

3.3.2.5 Current Bus Address Register (RKBA) — Address = 777410



BIT	DESIGNATION	DESCRIPTION AND OPERATION
00-15	BA00-BA15 (Read/Write)	The bits in this register specify the bus address to or from which the next data word will be transferred. The register is incremented by two at the end of each transfer. If the system has extended memory, the RKBA will overflow to the EX MEM (bits 04 and 05 of the RKCS) to reflect the extended bus addresses.

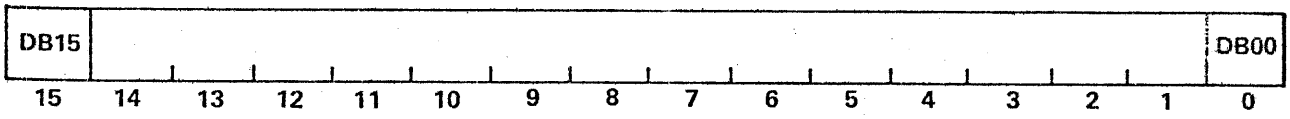
3.3.2.6 Disc Address Register (RKDA) — Address = 777412



This register will not respond to write commands from the processor while the controller is busy. Therefore, RKDA bits may be loaded from the bus data lines only when the Control Ready (RDY, RKCS 07) is set. The register is cleared by BUS INIT or Control Reset.

BIT	DESIGNATION	DESCRIPTION AND OPERATION
00-03	Sector Address (SA)	Loaded initially by the program. Holds the disc sector to be addressed for the next operation. During operations, SA is incremented after each sector and counts Mod 14_8. If SA is initially loaded with a number greater than 13_8 and an operation is initiated (GO), a hard error occurs and RKER 05 (NXS) is set.
04	Surface (SUR)	When set, selects the lower surface disc head; when reset, selects the upper surface disc head. This bit is automatically toggled by the controller at the end of each track.
05-12	Cylinder Address (CYL ADDR)	Loaded initially by the program. Holds the cylinder currently being selected. During operation, CYL ADDR is incremented after each cylinder and counts Mod 313_8. If CYL ADDR is initially loaded with a number greater than 312_8 and an operation is initiated (GO set), a hard error occurs and RKER 06 (NXC) is set.
13-15	Drive Select (DR SEL)	Binary representation of the logical drive number currently being selected. If a nonexistent drive is addressed, a hard error occurs and RKER 07 (NXD) is set.

3.3.2.7 Data Buffer Register (RKDB) — Address = 777416



BIT	DESIGNATION	DESCRIPTION AND OPERATION
00-15	DB00-DB15 (Read Only)	All data words transferred between the controller and the disc drive(s) pass through this register. Loadable from the computer only via the bus while the controller is bus master during a DMA sequence (i.e. cannot be loaded directly by the program, but can be read by the program).

3.4 DATA FORMAT AND DRIVE CONFIGURATION

This section defines the data formats as written and recovered by the DI-C03 plus the basic aspects of configuring a system of disc drives of varying types with the controller. Additional configuration information may be obtained from the Dataram Applications Manual available for the particular drive(s) being used.

3.4.1 Data Format

Data is stored on the disc cartridge in groups of 12 sectors per track. Each of the twelve disc sectors contain 256 data words and is defined by a sector mark which generates a sector pulse. All sectors are formatted identically in five parts; preamble (terminated with a sync bit), header, data, checksum, and postamble as shown below. Each word (excluding sync) is 16 bits.

Preamble	SYNC	Header	Data	Checksum	Postamble
Zeros (13 Words)	1 (1 bit)	Cylinder Address (1 Word)	(256 Words)	Sector Checksum (1 Word)	Zeros (1 Word)

→ Reading Direction

The preamble and postamble areas of a sector serve as boundaries surrounding the information words (header, data, and checksum) to ensure compatibility between disc drives at the cartridge level despite variations in sector pulse positioning.

The preamble consists of 13 words of zeros to insure that the data read circuitry in the drive will lock on during a known zero data field. For a Read operation, the controller waits for the sync bit to occur and then begins to read with the header word. For a Write function, the sync bit is automatically written by the controller following 13 words of zeros.

The header area of a sector consists of a single word containing the cylinder address. Before a data transfer function is performed, the header word is read and checked against the cylinder address portion of the RKDA to ensure that the disc drive heads are positioned above the proper cylinder. The Write function always rewrites the header on the disc, using the cylinder address portion of the RKDA. The sector format for a raw (unformatted) cartridge is written under program control in conjunction with RKCS 10.

The data area consists of 256 data words, 16 bits per word. The checksum area of a sector consists of a single word that is the checksum of all 256 data words. This recorded checksum is compared by the controller to a computed checksum whenever a Write Check, Read, or Read Check function is performed within a given sector. For a Write function, the controller calculates a checksum and writes it on the disc cartridge following the last data word of a sector.

Short portions (less than 256 data words) of a sector may be read or written as long as this short sector is the last sector of the data transfer. When a short sector is written, the remainder of the sector is automatically written with zeros. The Write Check function may be performed on a short sector as long as the number of words write checked is equal to the number of words previously written into the sector. Because the Read Check function is essentially a parity check, it must be performed on a whole-sector basis only.

3.4.2 Drive Configuration

The DI-C03 controller is designed for operational compatibility with the RK-11/RK-05 disc system, even though the disc drives available for interfacing to the LSI-11® via the DI-C03 differ in many respects from the original RK-05 drive itself. The following is a definition of the basic logical unit drive configuration for that system:

Cylinders/Drive:	203
Surfaces/Cylinder:	2
Tracks/Cylinder:	2
Sectors/Track:	12
Data Words/Sector:	256 (512 Bytes)
Data Words/Drive:	1.25 Million Words (2.5 million bytes) approximately
Drives/System:	8 maximum
Data Words/System:	10 Million Words (20 million bytes) approximately.

Since the RK-05 is a single platter, 100 tpi device, the logical unit drive defined above also corresponds to a physical drive in that system. Bits 15-13 of RKDA would therefore specify drive numbers 0-7 which ordinarily select the appropriate physical drive in the system.

The DI-C03 is designed to interface to all generally available disc drives in the range of 2.5-20.0 megabyte (formatted) capacities. Recent advances in technology have made available greater total capacities within a physical drive than can be obtained with the RK-05, and the DI-C03 may therefore be configured in a variety of ways, depending on the drive(s) attached. The following range of capacities can be handled by the DI-C03:

Capacity/Drive:	2.5-20.0 MBytes
Physical Drives:	4 maximum
Track Densities:	100 and 200 TPI, including mixed-density systems
Platters:	One, two, or four
Total System Capacity:	20 MBytes maximum

Because of the above possible combinations, the basic logical drive generally does not correspond to a physical drive in the DI-C03 system. The limitation of a maximum of four physical drives is the result of a limit of four unit select lines in the various drives available today. Therefore, the mapping of logical drives, as defined by bits 15-13 of the RKDA Register, is somewhat complex to define in a general sense.

To facilitate user definition of the various configuration of drives supported by the DI-C03, Table A-3 lists the various possibilities supported, in terms of a Configuration Number, presently 1 through 19. Associated with each Configuration Number is a definition of: (1) The total system capacity, (2) the number of physical drives included and their track densities, (3) the number of platters for each drive, (4) the range of physical drive addresses, and (5) the required setting of the option switches (SW1) which are applicable for drive configuration (Switches 2, 3, and 8).

Table A-4 is provided to indicate the location of logical drives on the physical drives in a given system configuration. The physical drive number corresponds to the drive number programmed in the drive (i.e. the unit Select Line recognized by the drive), not to the physical location of the drive on the daisychain cable. Unit Select Lines are numbered 1-4, corresponding to physical drive numbers 1-4.

3.4.3 Clock Rates

The DI-C03 presently handles two different bit packing densities, 2040 and 2200 bpi, and two different drive rotation speeds, 1500 and 2400 rpm. This results in four versions of the controller since the internal clock rate must be adjusted to accommodate the different serial/parallel data rates encountered. Each version requires selection of crystal frequency and jumper programming on the board. The controller is designed for operation up to 2400 rpm at 4400 bpi.

Table A-5 defines the controller versions presently available.

3.5 LOGIC CONVENTIONS

Nominal logic voltage levels in the controller are between OV (low) and +5V (high).

The basic convention followed in this document is that of positive True logic, that is, a high voltage corresponds to a logic One (or True, or Asserted) condition, and a low voltage corresponds to a logic zero (or False, or Unasserted) condition.

To avoid confusion, all signal Mnemonic designations have either a + or a * suffix to designate the normally true state of a signal. For example, the mnemonic FUNCT+ would imply that the function is asserted when the corresponding signal is at a positive (high) level. The logical complement of FUNCT+ could be designed FUNCT* and would be considered to be asserted when the FUNCT* was at a zero (low) level.

The only deviation from this convention is relative to the LSI-11 I/O bus interface signals. In this case, the suffix designator H is used to denote positive true functions, and the suffix designator L is used to denote assertion at the low level, i.e., the signal FUNCTH is asserted at a high level, and the signal FUNCTL is asserted at a low level.

APPENDIX A

TABLES

TABLE A-1
DISC CABLE INTERFACE SIGNALS
(CONNECTOR J-1)

3M Pin	Mnemonic	Signal Name	Alternate Name
1	GND	Ground	
2		Unused	Sector Address Bit 32
3	SA2*	Sector Address Bit 2	
4		Unused	
5	SINC*	Seek Incomplete	
6	ATTN1*	Attention 1	Note 1
7	ATTN4*	Attention 4	Note 1
8	ATTN3*	Attention 3	Note 1
9	LAIL*	Logical Address Interlock	Note 2
10	ATTN2*	Attention 2	Note 1
11	CA128*	Cylinder Address Bit 128	
12	T200*	200 TPI	
13	REMVD*	Disk Select	Removable Cartridge
14	RESTOR*	Restore	Return to Zero Seek
15	GND	Ground	
16	SA16*	Sector Address Bit 16	Note 3
17	CA2*	Cylinder Address Bit 2	
18	STROBE*	Strobe	Cylinder Address Strobe
19		Unused	
20	SA8*	Sector Address Bit 8	
21	SA4*	Sector Address Bit 4	
22	WTCH*	Write Check	
23	WTGT*	Write Gate	
24	CA256*	Cylinder Address Bit 256	
25	SA1*	Sector Address Bit 1	
26	TOPS*	Head Select	Top Head
27		Unused	
28	CA16*	Cylinder Address Bit 16	
29	SM*	Sector Mark	
30	DRDY*	Drive Ready	
31	CA64*	Cylinder Address Bit 64	
32	GND	Ground	
33	CA8*	Cylinder Address Bit 8	
34	DWP*	Write Protect Status	

TABLE A-1 (Continued)
DISC CABLE INTERFACE SIGNALS
(CONNECTOR J-1)

3M Pin	Mnemonic	Signal Name	Alternate Name
35	CA32*	Cylinder Address Bit 32	
36		Spare	
37	ERGT*	Erase Gate	
38	WTPRO*	Write Protect	
39	CA1*	Cylinder Address Bit 1	
40	CA4*	Cylinder Address Bit 4	
41	RDGT*	Read Gate	
42	RDATA*	Read Data	
43		Spare	
44	RDCK*	Read Clock	
45	RWS*	Ready to S/R/W	On Cylinder
46	SELU1*	Unit Select 1	
47	SELU2*	Unit Select 2	
48	SELU3*	Unit Select 4	
49	SELU4*	Unit Select 3	
50	WDCK*	Write Data and Clock	

Notes:

1. Attention lines not used for Diablo Mod 30 series drives.
2. Logical address interlock used as Address Acknowledge for Diablo Mod 30 series drives.
3. Normally reserved for extended sector addressing. Line must be grounded for operation with Diablo Mod 30 series drives.

TABLE A-2
OPTION SWITCH FUNCTIONS (SW1)

Switch No.	Ref. Par.	State	Function
1	3.2.5.1	OFF	Read/Write/Seek status is for selected physical drive.
		ON	Read/Write/Seek status is for selected logical drive.
2	3.2.5.2	OFF	Selects dual platter operation
		ON	Selects single platter operation
3	3.2.5.3	OFF	Normal setting (other than Configuration 15)
	Table 5-3	ON	Selects Configuration 15
4	3.2.5.4	OFF	Selects normal seek
		ON	Selects high-speed seek (6-sector physical offset on odd cylinders)
5-7	—	—	Unused
8	3.2.5.5	OFF	200 tpi operation is determined by state of 200T* level on J1-12.
		ON	Forces Controller to 200 tpi mode

TABLE A-3
SYSTEM CONFIGURATIONS

Config. Number	System Capacity (MB)	Physical Drives				Opt. Switches (SW1)		
		No.	Tr. Density (TPI)	Platters/ Drive	Physical Drive Addresses	2	3	8
1	10	1	200	2	1	OFF	OFF	ON
2	20	2	200	2	1,2	OFF	OFF	ON
3	5	1	200	1	1	ON	OFF	ON
4	10	2	200	1	1,2	ON	OFF	ON
5	15	3	200	1	1, 2, 3	ON	OFF	ON
6	20	4	200	1	1, 2, 3, 4	ON	OFF	ON
7	5	1	100	2	1	OFF	OFF	OFF
8	10	2	100	2	1, 2	OFF	OFF	OFF
9	15	3	100	2	1, 2, 3	OFF	OFF	OFF
10	20	4	100	2	1, 2, 3, 4	OFF	OFF	OFF
11	2.5	1	100	1	1	ON	OFF	OFF
12	5	2	100	1	1, 2	ON	OFF	OFF
13	7.5	3	100	1	1, 2, 3	ON	OFF	OFF
14	10	4	100	1	1, 2, 3, 4	ON	OFF	OFF
15	15	1	200(2)	2	1	OFF	ON	OFF
		1	100	2	4			
16	7.5	1	200(2)	1	1	ON	OFF	OFF
		1	100	1	3			
17	12.5	2	200(2)	1	1, 2	ON	OFF	OFF
		1	100	1	3			
18	15	2	200(2)	1	1, 2	ON	OFF	OFF
		2	100	1	3, 4			
19	20	1	200	4	1, 2(1)	OFF	OFF	ON

NOTES:

(1) Configuration 19 corresponds to a single 20 MB drive with one removable and 3 fixed platters. It is treated by the controller as two 10 MB drives (Configuration 2), with the transition board at the drive recognizing both Unit Select Lines 1 and 2 as addressing the single physical drive.

(2) The 200 TPI drive must assert its T200* status line on pin J1-12 when selected since SW1-8 must be left in the OFF position. Since some drives do not have this signal available, a special adapter may be required using such a drive in mixed track density systems.

TABLE A-4
LOGICAL DRIVE LOCATION

Config. Number	Physical Drive (Unit Sel. Line)							
	1		2		3		4	
	RMV	FIX	RMV	FIX	RMV	FIX	RMV	FIX
1	0, 1	2, 3	—	—	—	—	—	—
2	0, 1	2, 3	4, 5	6, 7	—	—	—	—
3	0, 1	—	—	—	—	—	—	—
4	0, 1	—	2, 3	—	—	—	—	—
5	0, 1	—	2, 3	—	4, 5	—	—	—
6	0, 1	—	2, 3	—	4, 5	—	6, 7	—
7	0	1	—	—	—	—	—	—
8	0	1	2	3	—	—	—	—
9	0	1	2	3	4	5	—	—
10	0	1	2	3	4	5	6	7
11	0	—	—	—	—	—	—	—
12	0	—	2	—	—	—	—	—
13	0	—	2	—	4	—	—	—
14	0	—	2	—	4	—	6	—
15	0, 1	2, 3	—	—	—	—	6	7
16	0, 1	—	—	—	4	—	—	—
17	0, 1	—	2, 3	—	4	—	—	—
18	0, 1	—	2, 3	—	4	—	6	—
19	0, 1	2-7[1]	—	—	—	—	—	—

NOTE: (1) Unit has 3 fixed platters; logical drives 4, 5 are treated as a removable platter by the controller.

TABLE A—5
CLOCKING AND STRAPPING CHART

Track BPI	Speed RPM	Crystal Freq. MHZ	Jumper Connections
2200	2400	20.0	E3 to E5
2200	1500	12.5	E1 to E2, E3 to E5
2040	1500	11.52	E1 to E2, E3 to E5
2040	2400	18.43	E3 to E5

NOTE: E3 to E4 jumper for future 4400 bpi operation.

TABLE A—6
MAINTENANCE SIGNALS (CONNECTOR J—2)

Pin No.	Ref. Par.	Signal Name	Mnemonic
1	3.2.7.2(1)	Stop	STOP+
2	3.2.7.2(2)	Disable Read Only Memory	DISROM+
3	3.2.7.2(3)	Disable Pipeline Register	DISPL+
4	3.2.7.1(1)	Clock	CKEXT*
5	3.2.7.2(4)	Reset	EXTRS*
6	3.2.7.1(2)	Reading	READING*
7	3.2.7.1(3)	Writing	WRITING*
8-14		Ground	

TABLE A—7 LSI—11® INTERFACE SIGNALS

Bus Pin	Mnemonic	Description
AA1	BIRQ6L	Reserved for interrupt level expansion.
AB1	BIRQ7L	
AC1	BAD16L	Extended address bits (implemented for bus address expansion)
AD1	BAD17L	
AE1		Unused
AF1		
AH1		
AJ1	GND	Ground
AK1		Unused
AL1		
AM1	GND	Ground
AN1	BDMRL	Direct Memory Access (DMA) Request.
AP1		Unused
AR1		
AS1		
AT1	GND	Ground.

TABLE A—7 LSI—11® INTERFACE SIGNALS (Continued)

Bus Pin	Mnemonic	Description
AU1 AV1		Unused
BA1	BDCOKH	DC Power OK.
BB1	BPOKH	AC Power OK.
BC1 BD1 BE1 BF1 BH1		Unused
BJ1	GND	Ground
BK1 BL1		Unused
BM1	GND	Ground
BN1	BSACKL	Bus Master.
BP1	BIRQ5L	Reserved for interrupt level expansion.
BR1 BS1		Unused
BT1	GND	Ground
BU1		Unused
BV1	+5	+5 V Power
AA2	+5	+5 V Power
AB2		Unused
AC2	GND	Ground
AD2		Unused
AE2	BDOUTL	Data Output
AF2	BRPLYL	Reply
AH2	BDINL	Data Input
AJ2	BSYNCL	Synchronize
AK2	BWTBTL	Write/Byte
AL2	BIRQ4L	Interrupt Request
AM2	BIAKIL	Interrupt Acknowledge Input
AN2	BIAKOL	Interrupt Acknowledge Output
AP2	BBS7L	Bank 7 Select
AR2	BDMGIL	DMA Grant-Input
AS2	BDMGOL	DMA Grant-Output
AT2	BINITL	Initialize

TABLE A–7 LSI–11® INTERFACE SIGNALS (Continued)

Bus Pin	Mnemonic	Description
AU2	BDAL00L	Data/Address Lines
AV2	BDAL01L	
BA2	+5	+5 V Power
BB2		Unused
BC2	GND	Ground
BD2		Unused
BE2	BDAL02L	Data/Address Lines
BF2	BDAL03L	
BH2	BDAL04L	
BJ2	BDAL05L	
BK2	BDAL06L	
BL2	BDAL07L	
BM2	BDAL08L	
BN2	BDAL09L	
BP2	BDAL10L	
BR2	BDAL11L	
BS2	BDAL12L	
BT2	BDAL13L	
BU2	BDAL14L	
BV2	BDAL15L	
CJ1	GND	Ground
CM1	GND	
CT1	GND	
CV1	+5	+5 V Power
CA2	+5	+5 V Power
CC2	GND	Ground
CR2	BDMGIL	DMA Grant Input (jumpered to CS2 on DI-CO3)
CS2	BDMGOL	DMA Grant Output (jumpered to CN2 on DI-C03)
CM2	BIAKIL	Interrupt Acknowledge Input (jumpered to CN2 on DI-C03)
CN2	BIAKOL	Interrupt Acknowledge Output (jumpered to CM2 on DI-C03)
DJ1	GND	Ground
DK1	OSC*	Oscillator Input/Output; DK1 and DL1 must be jumpered for operation of DI-C03.
DL1	OSC*	
DM1	GND	Ground
DT1	GND	Ground
DA2	+5	+5 V Power
DC2	GND	Ground

TABLE A-8
DISC DRIVE CROSS REFERENCE CHART

Disc Drive Adapter		Disc Drives	Dataram Appl. Manual	Comments
P/N	Name			
C03104002	Diablo 44 (50 Male Pin Adapter)	Diablo, Mod. 44B	C03511001	Daisy Chain Adapter
		CDC 9427 (Hawk) CDC 9414 (Falcon)	C03511002	Winchester I/O Board, Diablo 44 Interface
C03104003	Diablo 44 (50-Pin Female Socket Adapter)	Diablo, Mod 44B	C03511001	Controller-to-Drive Adapter
		CDC 9427 (Hawk) CDC 9414 (Falcon)	C0351102	Winchester I/O Board, Diablo 44 Interface
C03104004	Pertec Adapter	D3X1X, D3X2X, D3X3X, D3X4X, D3X5X, D3X7X, N Type I/O	C03511003	5 & 10 MByte, Pertec Std. Interface, w/Terminators
C03104005	Pertec Adapter			5 & 10 MByte, Pertec Std. Interface, Daisychain Connector
C03204006	Pertec Adapter	D3X1X, D3X2X, D3X3X, D3X4X, D3X5X, D3X7X C Type I/O		5 & 10 MByte, Diablo 30 Interface, w/Terminators
C03104007	Pertec Adapter			5 & 10 MByte, Diablo 30 Interface, Daisychain Connector
C03104008	Pertec Adapter	D3X6X, D3X8X N Type I/O		20 MByte, Pertec Std. Interface, w/Terminators
C03104009	Pertec Adapter	D3X6X, D3X8X, C Type I/O		20 MByte, Diablo 30 Interface, w/Terminators
C03104010	Diablo 30 (42 Male Pin Adapter)	Diablo, Mod. 30	C03511001	Controller-to-drive adapter, male connector, mates with female receptacle on drive
C03104011	Caelus, 100 TPI Adapter	Caelus 206/306	C03511004	100 TPI Version
C03104012	Caelus, 200 TPI Adapter	Caelus 206/306		200 TPI Version
C03104013	Western Dynex Adapter	Western Dynex 6000	C03511005	Configuration No. 24 (Dynus Configuration)
C03112001 C03112002 C03112003	Disc Drive Cable: 5 ft. 8 ft. 10 ft.	All Disc Drives	N/A	50-conductor flat cable with connectors for connection of C03 and C33 controllers to all applicable disc drives

APPENDIX B

APPLICATION NOTES

APPLICATION		REVISION			
NEXT ASSY	USED ON	LTR	DESCRIPTION	DATE	APPROVED
N/A	Model C03 & C33	A	Official Release Per EC002	4/30/78	

APPLICATION NOTE

1. GENERAL

This Application Note provides information required and/or useful for operation of current RK-11/RK-05 diagnostics.

2. SYSTEM DEFINITION

The Dynus Model DI-C03 and DI-C33 controllers fully emulate the functions and operations of the RK-11 disc controller. The DI-C03 or DI-C33 is the control element of a system which emulates the original RK-11/RK-05 subsystem, but uses industry standard cartridge disc drives.

The basic RK-05 drive is a 2.5 MByte (formatted), single-platter, 100 TPI, 1500 RPM, front-load unit. Drives used with the DI-C03 or DI-C33 generally contain more than 2.5 MBytes of storage capacity per drive. These drives are, therefore, organized by the controller into logical 2.5 MByte units so that functional compatibility with the RK-05 is preserved.

A later version of the original 2.5 MByte drive, designated the RK-05F, increases track density to 200 TPI on a fixed platter to provide 5 MBytes on a single drive. Current diagnostics have, therefore, been written to check for the presence of RK-05F drives and to automatically adapt the tests to the version of drive being used. For example, the diagnostics will delete overlapped seeks on two logical drives which would be on the same physical drive in a system incorporating a RK-05F.

The controller will properly recognize and execute all functional and performance tests included in the current diagnostic programs.

However, the various ways in which the current diagnostics check for the presence of a RK-05F drive requires a specific response from the drive itself. The industry standard drives used do not, however, always behave in the same way. For this reason, the current diagnostics must be "Patched" to modify the checks for presence of a RK-05F present test. The actual diagnostic test operations performed are not modified.

MATERIAL

FINISH

DO NOT SCALE DRAWING

DRAWN K. Melton 4/30/78
CHECKED
ENGINEER Jack Cox 5/26/78
APPROVED
APPROVED

DYNUS INCORPORATED COSTA MESA, CALIF.

TITLE: DYNUS MODEL C03 & C33 DIAGNOSTIC OPERATIONS

SIZE	CODE IDENT. NO.	DRAWING NO.	REV.
A		C03514001	A

SCALE | WORK ORDER NO. | SHEET 1 OF 3

The inserts required to alter the check for presence of a RK-05F are given below. Also included are some additional program inserts which are useful in various situations for testing the system.

3. DIAGNOSTIC DEFINITIONS

The DI-C03 is designed to run the following diagnostics according to the instructions given in Paragraph 4 below:

a. RK-11 Basic Logic Test I, DZRKJ-D-D, December 1976.
This program checks the controller only and is independent of the disc drive. All RK registers, including word and byte addressing, are tested.

b. RK-11 Basic Logic Test II, DZRKK-D-D, December 1976.
This program checks the controller logic used for control of the disc drive.

c. RK-11/RK-05 Dynamic Test, DZRKL-D-D, December 1976.
This test checks the electro-mechanical integrity, linear positioning and speed control, read/write logic, and seek function timing of the disc drive.

d. RK-11/RK-05 Performance Exerciser, DZRKH-F, December 1976.
This program exercises the controller and all drives as a system and checks the error logging and data transfer operations between the drives and the processor via the controller.

4. DIAGNOSTIC OPERATIONS

a. The following changes should be made to modify the check for presence of a RK-05F in the system:

(1) RK-11 Basic Logic Test II, DZRKK-D-D (TEST 55).

LOC	CHANGE FROM	CHANGE TO
17702	1403	0403

This patch causes the diagnostic to delete the check for presence of a RK-05F drive.

(2) RK-11 Dynamic Test, DZRKL-D-D, (FCHECK).

LOC	CHANGE FROM	CHANGE TO
24146	1010	0240

(3) RK-11/RK-05 Performance Exerciser, DZRKH-F:

LOC	CHANGE FROM	TO
04610	1010	0240

b. The following are useful for diagnostic operations:

(1) Basic Logic Test II

(a) In response to Drives To Be Tested?, enter 0F, 2F, etc.
(b) 1 pass on 1 drive takes approximately 5 minutes on a LSI-11.

(2) Dynamic Test

To adjust graph outputs for 2400 RPM operation (1500 RPM is standard):

LOC	CHANGE FROM	TO
15124	0512	0320
15142	0245	0150

(3) Performance Exerciser

(a) Switch options for CRT system are 100420.
(b) If random data is 0F, restart at 0210.
(c) The following are useful for specified operations:

LOC	CHANGE FROM	TO	EFFECT
02376	6400	1700	Home cursor on status printout.
17016	104414	0207	Eliminate read compare.
16612 16614	104414 16504	0137 17004	Eliminate random data generation for write.
10240	11410	0100	Write random data on Cyl.0 & 1. Reduce cylinders tested from 203:
10114	0504	1210	To 102 cylinders.
10114	0504	2420	To 51 cylinders.
10114	0504	5040	To 26 cylinders.
10240 10114	11410 0504	0600 12100	Run 13 cylinders only.

APPLICATION		REVISION			
NEXT ASSY	USED ON	LTR	DESCRIPTION	DATE	APPROVED
N/A	Model C03 & T03	A	Official Release Per EC002	4/30/78	

APPLICATION NOTE

1. GENERAL

The REV11 and TEV11 Manufacturer has issued an ECO as follows:

ECO No.: M9400-00007
Date: 11 October 1977
Product Families: M9400, used on REV11 and TEV11

Use of either of these products without incorporation of the referenced ECO in a system with the DI-C03 or DI-T03 may cause improper bus operation. This Application Note describes the nature of the problem and references the procedures recommended for correction.

2. DEFINITION OF THE PROBLEM

The unmodified M9400 module has the following two possible problems:

a. If any device is holding BRPLY asserted greater than 1.8 microseconds after the M9400 raises DMR, it is possible for the M9400 to hang the bus by dropping DMR after asserting SACK, even though it has not yet set Master. The symptom of the problem is bus hang-up waiting for a non-existent Master signal.

b. It is possible for an instruction to reset a device interrupt enable bit between BIRQL and IAKL, resulting in no RPLY to IAK. The symptom of this problem is that the system goes to Halt (ODT) mode with a maintenance command M=0000X1 (bus time-out while waiting for interrupt).

The design of the DI-C03 or DI-T03 is such that the unmodified REV11 and TEV11 units caused the bus hang-up symptom as described above.

3. CORRECTIONS REQUIRED

A copy of the first-issue ECO required to correct the above problems is availabe from Dynus. However, it is recommended that the Manufacturer be contacted to insure that the included information is up to date before making the change, or that unmodified units be returned directly to the Manufacturer for correction.

MATERIAL

FINISH

DO NOT SCALE DRAWING

DRAWN K. Melton 4/30/78
CHECKED
ENGINEER 5/26/78
APPROVED
APPROVED

DYNUS INCORPORATED COSTA MESA, CALIF.

TITLE
REQUIRED MODIFICATION TO DEC REV11 AND TEV11 BUS INTERFACE DESIGNS

SIZE	CODE IDENT. NO.	DRAWING NO.	REV.
A		C03514002	A

SCALE | WORK ORDER NO. | SHEET 1 OF 1

APPLICATION		REVISION			
NEXT ASSY	USED ON	LTR	DESCRIPTION	DATE	APPROVED
N/A	Model C03 & C33	A	Official Release Per EC024	9/14/78	F. Cox

APPLICATION NOTE

1. GENERAL

DYNUS offers a configuration option which permits expansion of addressing up to 40 MBytes contained on up to four physical drives on the disc cable daisychain. This option applies to both the Model C03 (LSI-11) and C33 (PDP-11) cartridge disc controller products.

The only difference between the controllers configured for standard 20 MByte capacity and those configured for 40 MByte capacity is in the firmware contained in control memory; no other changes are required to the controller itself. (Note: Some adapters do require a wiring revision for use in a 40 MByte system). The 40 MByte capacity will handle many drive configurations, including both 100 and 200 TPI densities; the number of configurations available is, however, more limited than the number available in the standard 20 MByte configuration.

2. SOFTWARE CONSIDERATIONS

a. Diagnostics

Standard DEC diagnostics related to the disc drives are defined to a 20 MByte maximum limit. The basic technique used to increase system capacity to 40 MBytes is to place logical drives in the range of 2.5-20 MBytes on even tracks (of 200 TPI discs) and logical drives in the 22.50-40 MByte range on odd tracks. Therefore, standard disc diagnostics will normally perform operations only on the even numbered tracks of the physical drives in the system. This is generally adequate to confirm proper, or improper, operation of the physical drive.

MATERIAL: N/A

FINISH:

DO NOT SCALE DRAWING

DRAWN M. Velderrain

CHECKED

ENGINEER F. Cox 9/14/78

APPROVED

APPROVED

Dynus INCORPORATED COSTA MESA, CALIF.

TITLE: 40 MEGABYTE SYSTEM CAPACITY OPTION FOR MODELS C03 AND C33 CONTROLLERS

SIZE	CODE IDENT. NO.	DRAWING NO.	REV.
A		C03514003	A

SCALE N/A WORK ORDER NO. SHEET 1 OF 4

To permit execution of disc diagnostics on physical odd numbered tracks (i.e. in the logical range above 20 MBytes), an option switch (SW3) on the board may be set to force the controller to operate on physical odd tracks. Therefore, to exercise odd tracks, the board must be removed and the switch set.

CAUTION

After performing diagnostics with the odd track option switches set, the switch must be turned OFF for normal system software operations. Improper operation will result if the switch is left set.

Except for the above provision for testing odd tracks, diagnostic software and procedures are identical to those for the standard RK-11 emulation (refer to DYNUS Application Note C03514001).

b. Systems Software

Extended adressing to 40 MBytes (16 logical 2.5 MByte drives) is achieved by use of RKCS bit 9 as the odd/even track select bit. Normally, this bit is OFF, and the system operates in the 0-20 MByte address range.

Standard system software drivers are not set up to manipulate Bit 9 and must therefore be modified. In essence, the driver must determine the address range called for, and set or reset Bit 9 of RKCS accordingly. There may be other operating software modifications, external to the disc driver, required, depending upon the operating system in use.

DYNUS does not presently support any system software modifications, therefore application of the extended addressing capability is left to the discretion of the user.

3. IMPLEMENTATION

As previously described, extended addressing is implemented by using Bit 9 of RKCS as an even (Bit 9=0) or odd (Bit 9=1) track (cylinder) select bit when the extended addressing mode is selected. This mode is selected by use of option switch 2 (SW1-2).

When SW1-2 is OFF, the controller performs standard RK-11 emulation which limits addressing to 20 MBytes. RKCS Bit 9 is ignored in this mode. Also, with SW1-2 OFF, switch SW1-3 is used to permit operation with 100 TPI single platter drives

(i.e. RK-05 media compatable).

If SWI-2 is ON, the controller is set for 40 MByte operation, and RKCS Bit 9 is now used to determine the lower (0-20 MByte) and upper (20-40) MByte) address range. In addition, SWI-3 is then used for selecting the upper range (i.e. odd numbered tracks) for diagnostic operations. In normal operation, SWI-3 must be left in the OFF position.

Implementation of the 40 MByte capability is completely in firmware, and no hardware changes other than the PROM set are made to the controller board. Therefore, existing units may be retrofitted for this capability if desired. Contact DYNUS for further information.

4. DOCUMENTATION CHANGES

The following technical manuals are affected for users of the 40 MByte expansion:

C03510001 - Model C03

C33510001 - Model C33

The changes described below apply to both manuals except where noted.

a. Table 1-1. Change specification to reflect 40 MByte optional capacity. Note software/diagnostic considerations given in Paragraph 2 above.

b. Section 3.2.5. Replace in its entirety by Addendum A of this Application Note.

c. Table A-2 . Replace in its entirety by Addendum B of this Application Note.

d. Table A-3. Replace in its entirety by Addendum C of this application Note.

e. Table A-4. Replace in its entirety by Addendum D of this Application Note.

f. Ammend Section 3.3.2.3. as follows:

Bit 09 Extra Bit (EXB). When the 40 MByte address is selected (SW1-2 ON), this bit controls even (Bit 09=0) or odd (Bit 09=1) cylinder selection. State of this bit may be tested by software. However if SW1-3 is ON when SW1-2 is ON, the Controller is forced

SIZE	CODE IDENT NO.	DRAWING NO.
A		C03514003
SCALE		SHEET 3 of 4

to operate only on odd cylinders even though the state of EXB in the register is not changed; therefore, software cannot determine the state of SW1-3.

f. Section 3.4.2. Replace in its entirity by Addendum E to this Application Note.

5. ADAPTER CHANGES

Different adapters are required for 20 MByte drives used in the 40 MByte emulation than those available for the standard RK-11 emulation (Adapter Part Numbers C03104009 and C03104014; refer to table A-8). New part numbers will be announced for these adapters, but users with existing 20 MByte drives are cautioned to change or modify the existing adapters when changing to the 40 MByte version.

3.2.5 Option Switches

Eight option switches are contained on switch SW1 located at the top of the controller (refer to Figure 1-1). The switch numbers and ON position are marked on the switch. Five of these switches are used (three are unused) in connection with the clock crystal frequency and jumper selections to configure the system for various drive types/capacities and to select other optional functions. A complete description of the switch functions is given below, with a summary given in Table A-2.

3.2.5.1 Switch 1 - Logical Drive Status.

Normally (SW1-1 OFF) the controller will reflect the Read/Write/Seek status of a selected physical drive, regardless of which logical drive is addressed. Since there may be multiple logical drives on a single physical drive, the operating software will encounter a busy condition if a logical drive is accessed on a physical drive where another logical drive is performing an operation.

If SW1-1 is placed in the ON position, the controller will reflect the Read/Write/Seek status of the selected logical drive. Thus, even if a physical drive is busy performing a function, selection of a non-busy logical drive on that physical drive will result in a ready status condition in the status register. However, if a function is issued to that logical drive, it will be ignored since the physical drive is already busy, but the controller will generate the normal completion interrupts for all such commands to insure that no software hangups occur. These interrupts will occur at the time the physical drive completes the function in process.

If a subsequent Read or Write operation is issued to a logical drive for which a Seek was ignored because of the previous condition, the head will not be on the desired cylinder. Since the controller automatically performs a seek function before initiating a Read or Write operation, the head will be moved at the time such operation is commanded.

3.2.5.2 Switches 2 and 3 - Drive Configuration.
If SW1 - 2 and 3 are in the OFF position, the controller will map odd numbered logical drives on odd cylinders. SW1-8 must be on to force 200 TPI status.

If SW1-2 is OFF and SW1-3 is ON, the controller will assume that 1 platter, 100 TPI drives are connected. SW1-8 must be off and the drives must not drive the T200 line.

If SW1-2 is ON, SW1-3 is OFF, and SW1-8 is ON, the 40 megabyte addressing mode is selected. The RKDA cylinder address bits are shifted left one bit before being sent to the drives. RKCS bit 9 is mapped into cylinder address bit 0. If SW1-8 is OFF and T200 is not asserted, the controller will assume the drive is dual platter and 100 TPI.

If SW1-2 and 3 are both ON, the controller will operate exactly like the previous configuration except it will assume that RKCS bit 9 is always ON.

3.2.5.3 Switch 4 - High Speed Seek.
In normal operation (SW1-4 OFF) the sector numbers transmitted to the controller by software will match the physical sectors on the disc (as referenced to the sector mark) for all logical cylinders. Because of delays in positioning the head when moving from cylinder-to-cylinder, a full rotation of the disc is usually lost when crossing a cylinder boundary.

If SW1-4 is set to ON, the controller will automatically introduce a 6-sector offset between the logical (software) sector and the physical sector on off logical cylinder numbers; i.e. on cylinder numbers 1, 3, 5, etc., logical sector 0 corresponds to physical sector 6, logical sector 1 corresponds to physical sector 7, etc. Thus, when multiple sector operations cross cylinder boundaries, the next physical sector will be located within half a revolution of the disc and result in considerable block transfer time reductions in some applications.

3.2.5.4 Switch 8 - 200 TPI.
With SW1-8 in the ON position, the 200T* status line to disc connector J1-12 is forced to the asserted state, and the controller will treat all drives as operating at 200 tpi track densities. Since some 200 tpi drives do not provide this signal, SW1-8 should be set ON when all physical drives are 200 tpi.

If all physical drives are not 200 tpi, then SW1-8 must be OFF. For systems containing drives with mixed track densities, the 200 tpi drives must assert the 200T* signal when the drive is selected, and the 100 tpi units must never assert this signal. Units at 200 tpi which do not provide the 200T* signal either cannot be used in mixed systems, or a special adapter board or other disc logic adaptation must be provided.

TABLE A-5

With SW1-1, SW1-2, SW1-8 ON, the following results:

RKDA= (7777412)	Bit 9 Of RKCS =	Removable Platter Sel	Unit Sel 1	Unit Sel 2	Unit Sel 3	Unit Sel 4	CAI*
0	0	1	1	0	0	0	-0
0	1	1	1	0	0	0	1
20,000	0	0	1	0	0	0	0
20,000	1	0	1	0	0	0	1
40,000	0	1	0	1	0	0	0
40,000	1	1	0	1	0	0	1
60,000	0	0	0	1	0	0	0
60,000	1	0	0	1	0	0	1
100,000	0	1	0	0	1	0	0
100,000	1	1	0	0	1	0	1
120,000	0	0	0	0	1	0	0
120,000	1	0	0	0	1	0	1
140,000	0	1	0	0	0	1	0
140,000	1	1	0	0	0	1	1
160,000	0	0	0	0	0	1	0
160,000	1	0	0	0	0	1	1
	J1-13 REMVD* = LOW=1	J1-46 SELV1* = LOW=1					CAI * = 1 = LOW

ATTACHMENT B

TABLE A-2
OPTION SWITCH FUNCTIONS (SW1)
(40MB Firmware)

Switch No.	Ref. Par.	State	Function	
1	3.2.5.1	OFF	Read/Write/Seek status is for selected physical drive.	
		ON	Read/Write/Seek status is for selected logical drive.	
2	3.2.5.2	OFF	Selects RK11 compatible operation	
		ON	Selects 40 megabyte operation	
3	3.2.5.2	OFF	Switch No. 2 off	Selects 2 platter, 200 TPI operation
			Switch No. 2 on	Selects 40MB operation at 200 TPI or 2 platter, 100 TPI operation
		ON	Switch No. 2 off	Selects 1 platter, 100 TPI operation
			Switch No. 2 on	Selects 40MB operation on odd cylinders for testing.
4	3.2.5.4	OFF	Selects normal seek	
		ON	Selects high-speed seek (6-sector physical offset on odd cylinders)	
5-7	-	-	Unused	
8	3.2.55	OFF	200 tpi operation is determined by state of 200T* level on J1-12.	
		ON	Forces Controller to 200 tpi mode	

ATTACHMENT C

TABLE A-3
SYSTEM CONFIGURATIONS
(40MB Firmware)

Config. Number	System Capacity (MB)	Physical Drives				Opt. Switches (SW1)		
		No.	Tr. Density (TPI)	Platters/ Drive	Physical Drive Addresses	2	3	8
1A	10	1	200	2	2	OFF	OFF	ON
2A	20	2	200	2	1,2	OFF	OFF	ON
3A	5	1	100	2	1	ON	OFF	OF
4A	10	2	100	2	1,2	ON	OFF	OF
5A	15	3	100	2	1,2,3	ON	OFF	OF
6A	20	4	100	2	1,2,3,4	ON	OFF	OF
7A	2.5	1	100	1	1	OFF	ON	OF
8A	5	2	100	1	1,2	OFF	ON	OF
9A	7.5	3	100	1	1,2,3	OFF	ON	OF
10A	10	4	100	1	1,2,3,4	OFF	ON	OF
11A	20	1	200	4	1,2	OFF	OFF	ON
12A	10(1)	1	200	2	1	ON	OFF	ON
13A	20(1)	2	200	2	1,2	ON	OFF	ON
14A	30(1)	3	200	2	1,2,3	ON	OFF	ON
15A	40(1)	4	200	2	1,2,3,4	ON	OFF	ON
16A	20(1)	1	200	4	1,2(2)	ON	OFF	ON
17A	40(1)	2	200	4	1,2,3,4(2)	ON	OFF	ON

NOTES:

(1) Odd cylinders addressed by setting bit 9 of RKCS.

(2) Adapters on 20MB drives "OR" 2 physical drive selects to select drive and correct second platter select line to one of the 2 physical drive selects.

TABLE A-4
LOGICAL DRIVE LOCATION

CONFIG. NUMBER	PHYSICAL DRIVE 1		2		3		4	
	RMV	FIX	RMV	FIX	RMV	FIX	RMV	FIX
1A	0,1	2,3	–	–	–	–	–	–
2A	0,1	2,3	4,5	6,7	–	–	–	–
3A	0	1	–	–	–	–	–	–
4A	0	1	2	3	–	–	–	–
5A	0	1	2	3	4	5	–	–
6A	0	1	2	3	4	5	6	7
7A	0	–	–	–	–	–	–	–
8A	0	–	2	–	–	–	–	–
9A	0	–	2	–	4	–	–	–
10A	0	–	2	–	4	–	6	–
11A	0,1	2-7 (1)	–	–	–	–	–	–
12A (2)	0	1	–	–	–	–	–	–
13A (2)	0	1	2	3	–	–	–	–
14A (2)	0	1	2	3	4	5	–	–
15A (2)	0	1	2	3	4	5	6	7
16A (2)	0	1-3 (1)	–	–	–	–	–	–
17A (2)	0	1-3 (1)	4	5-7 (3)	–	–	–	–

NOTES:

(1) UNIT HAS 3 FIXED PLATTERS; ADAPTER BOARD 'OR'S' UNIT SELECT LINES 1 AND 2 TO SELECT ONE PHYSICAL DRIVE. UNIT SELECT 2 DRIVES THE SECOND PLATTER SELECT LINE INTO THE DRIVE.

(2) ODD CYLINDERS ADDRESSED BY SETTING BIT 9 OF RKCS.

(3) UNIT HAS 3 FIXED PLATTERS; ADAPTER BOARD 'OR'S' UNIT SELECT LINES 3 AND 4 TO SELECT ONE PHYSICAL DRIVE. UNIT SELECT 4 DRIVES THE SECOND PLATTER SELECT LINE INTO THE DRIVE.

NOTES ON MIXING 100 AND 200TPI DRIVES ON ONE CONTROLLER

(1) OPTION SWITCH 8 MUST BE OFF. ALL 200TPI DRIVES MUST ASSERT T200 (TABLE 1-A) AND 100TPI DRIVES MUST NOT ASSERT T200 WHEN SELECTED.

(2) THE SAME PHYSICAL MEDIA MAY BE MAPPED INTO MORE THEN ONE LOGICAL DRIVE ON THE 100TPI DRIVE.

(3) IF THE 100TPI DRIVE IS 1500RPM AND THE 200TPI DRIVE(S) ARE 2400RPM, THE 100TPI DRIVE MUST OPERATE AS A 'READ ONLY' UNIT.

(4) RECOMMENDED CONFIGURATIONS:

2A - SINGLE PLATTER. 100TPI REPLACES PHYSICAL DRIVE NO. 2. THE SAME 2.5 MB MEDIA WILL BE MAPPED INTO LOGICAL DRIVES 4,5,6,&7.

2A - DUAL PLATTER. 100TPI REPLACES PHYSICAL DRIVE NO. 2. THE REMOVABLE MEDIA WILL BE MAPPED INTO LOGICAL DRIVES 4&5 AND THE FIXED MEDIA WILL BE MAPPED INTO LOGICAL DRIVES 6&7.

13A - SINGLE PLATTER. 100TPI REPLACES PHYSICAL DRIVE NO. 2. THE SAME 2.5 MB MEDIA WILL BE MAPPED INTO LOGICAL DRIVES 2&3. BIT 9 OF RKCS HAS NO EFFECT ON THE 100TPI DRIVE.

13A - DUAL PLATTER. 100TPI REPLACES PHYSICAL DRIVE NO. 2. THE LOGICAL TO PHYSICAL MAPPING IS THE SAME AS A 200TPI DRIVE. BIT 9 OF RKCS HAS NO EFFECT ON THE 100TPI DRIVE.

14A AND 15A. SAME AS 13A EXCEPT THE LAST PHYSICAL AND LOGICAL DRIVE NUMBERS ARE AFFECTED.

17A - SINGLE PLATTER. 100TPI REPLACES PHYSICAL DRIVE NO. 2. THE 100TPI DRIVE MUST RESPOND TO DRIVE SELECT 3. THE SAME 2.5MB MEDIA WILL BE MAPPED INTO LOGICAL DRIVES 4&5. BIT 9 OF RKCS HAS NO EFFECT ON THE 100TPI DRIVE.

17A - DUAL PLATTER. 100TPI REPLACES PHYSICAL DRIVE NO. 2. THE 100TPI DRIVE MUST RESPOND TO DRIVE SELECT 3. THE REMOVABLE PLATTER WILL BE LOGICAL DRIVE NO. 4 AND THE FIXED PLATTER WILL BE LOGICAL DRIVE NO. 5.

3.4.2. Drive Configuration

For controllers incorporting the 40 MByte expansion firmware, the definition and configuration of logical drives is determined by whether or not the 40 MByte addressing is enabled or disabled by use of option switch SW1-2.

3.4.2.1. 20 MByte System

When SW1-2 is OFF, addressing is limited to 20 MBytes maximum, and the definition of a logical drive is identical to that of the standard RK-11/RK-05 disc system.

The DI-C03 (and C33) Controllers are designed for operational compatibility with the RK-11/RK-05 disc system, even though the disc drives available for interfacing to the LSI-11 (and PDP-11) via the DI-C03 (and C33) differ in many respects from the original RK-05 drive itself. The following is a definition of the basic logical unit drive configuration for that system.

Cylinders/Drive:	203
Surfaces/Cylinder:	2
Tracks/Cylinder:	2
Sectors/Track:	12
Data Words/Sector:	256 (512 Bytes)
Data Words/Drive:	1.25 Million Words (2.5 Million Bytes) approximately.
Drives/System:	8 Maximum
Data Words/System:	10 Million Words (20 Million Bytes) approximately.

Since the RK-05 is a single platter, 100 TPI device, the logical unit drive defined above also corresponds to a physical drive in that system. Bits 15-13 of RKDA would therefore specify drive numbers 0-7 which ordinarily select the appropriate physical drive in the system. The DI-C03 (and C33) are designed to interface to all generally available disc drives in the range of 2.5-20.0 MByte (formatted) capacities. Recent advances in technology have made available greater total capacities within a physical drive than can be obtained with the RK-05 and the DI-C03 (and C33) may therefore be configured in a variety of ways, depending on the drive(s) attached. The following range of capacities can be handled by the DI-C03 (and C33).

Capacity/Drive	2.5-20.0 MBytes
Physical Drives:	4 Maximum
Track Densities:	100 and 200 TPI, including mixed-density systems.
Platters:	One, two, or four.
Total System Capacity:	20 MBytes Maximum

Because of the possible combinations, the basic logical drive generally does not correspond to a physical drive in the DI-C03 (and C33) system. The limitation of a maximum of four physical drives is the result of a limit of four unit select lines in the various drives available today. Therefore, the mapping of logical drives, as defined by bits 15-13 of the RKDA Register, is somewhat complex to define in a general sense.

To facilitate user definition of the various configuration of drives supported by the DI-C03 (and C33) Table A-3 lists the various possibilities supported, in terms of a Configuration Number. Configuration Numbers 1A-11A correspond to the 20 MByte system capacity, and the 2.5 MByte logical drive definition given above applies. Associated with each Configuration Number is a definition of: (1) The total system capacity, (2) the number of physical drives included and their track densities, (3) the number of platters for each drive, (4) the range of physical drive addresses, and (5) the required setting of the option switches (SW1) which are applicable for drive configuration (Switches 2, 3, and 8).

Table A-4, Configurations 1A-11A, is provided to indicate the location of 2.5 MByte logical drives on the physical drives in a given system configuration. The physical drive number corresponds to the drive number programmed in the drive (i.e. the unit Select Line recognized by the drive), not to the physical location of the drive on the daisychain cable. Unit Select lines are numbered 1-4, corresponding to physical drive numbers 1-4.

3.4.2.2. 40 MByte System

When SW1-2 is ON, the Controller is placed in the 40 MByte addressing mode. In this case, the definition of a logical drive is changed to relfect a 5 MByte increment as follows:

Cylinders/Drive:	406
Surfaces/Cylinder:	2
Tracks/Cylinder:	2
Sectors/Track:	12
Data Words/Sector:	256 (512 Bytes)
Data Words/Drive:	2.5 Million (5 Million Bytes) approximately.
Drives/System:	8 Maximum
Data Words/System:	20 Million Words (40 Million Bytes) approximately.

In the 40 MByte mode (SW1-2 ON), the DI-C03 (and C33) Controllers are designed to handle all generally available disc drives in the range of 5.0-20.0 MByte (formatted capacities.

The following physical drives may be interfaced:

Capacity/Drive:	5-20 MBytes
Physical Drives:	4 Maximum
Track Densities:	200 TPI
Platters:	One, two, or four
Total System Capacity:	40 MBytes Maximum

Table A-3, Configuration Numbers 12A-17-A, lists the available combinations of drives supported by the DI-C03 (and C33) Controllers in the 40 MByte addressing mode. Table A-4 indicates the location of the 5 MByte logical drives on the physical drives for the corresponding Configuration Number given in Table A-3.

In using the 40 MByte system, the definition of a 5.0 MByte logical drive in essence permits the programmer to select a data block which is twice the size of the standard RK-05 block. Since the call to a driver is made by specifying a (logical) drive number and a block number, the driver must be revised to break the block number into three components, depending upon the block number specified in the call: Cylinder Address, Sector Number, and RKCS Bit 09 state.

Table A-5 summarizes the action of the key drive address and select lines for the range of addresses in RKDA and Bit 9 of RKCS.

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	OFFICIAL RELEASE PER EC036	12/5/79	[illegible]

1	A	2
BIRQ5L	A	+5V
BIRQ6L	B	
BADI6L	C	GND
BADI7L	D	
	E	BDOUTL
	F	BRPLYL
	H	BDINL
GND	J	BSYNCL
	K	BWTBTL
	L	BIRQ4L
GND	M	BIAKIL
BDMRL	N	BIAKOL
	P	BBS7L
	R	BDMGIL
	S	BDMGOL
GND	T	BINITL
	U	BDALOOL
	V	BDALOIL

1	B	2
BDCOKH	A	+5V
BPOKH	B	
	C	GND
	D	
	E	BDALO2L
	F	BDALO3L
	H	BDALO4L
GND	J	BDALO5L
	K	BDALO6L
	L	BDALO7L
GND	M	BDALO8L
BSACKL	N	BDALO9L
BIRQ7L	P	BDALIOL
	R	BDALIIL
	S	BDALI2L
GND	T	BDALI3L
	U	BDALI4L
+5V	V	BDALI5L

1	C	2
	A	+5V
	B	
	C	GND
	D	
	E	
	F	
	H	
GND	J	
	K	
	L	
GND	M	BIAKIL
	N	BIAKOL
	P	
	R	BDMGIL
	S	BDMGOL
	T	
GND	U	
	V	

1	D	2
	A	+5V
	B	
	C	GND
	D	
	E	
	F	
	H	
GND	J	
OSC*	K	
OSC*	L	
GND	M	
	N	
	P	
	R	
	S	
GND	T	
+5V	U	
	V	

LAST DESIGNATION USED	
INTEGRATED CIRCUIT	U81
RESISTORS	R28
CAPACITORS	C15
SWITCH	SW1
RESISTOR MODULE	RM6
OSC	Y1
DIODE	CR1

REFERENCE DESIGNATION	GATES USED PER TOTAL	PART NUMBER
U12	1/2	75452
U27	3/4	74S00
U44	5/6	74S04
U70	3/4	74S08
U72	3/4	74S02
U73	5/6	74S04

(4) VERSION AND STRAPPING CHART

VERSION	BPI.	RPM	FREQ	JUMPER
A	2200	2400	20.0MHZ	E3 TO E5
B	2200	1500	12.5 MHZ	E1 TO E2, E3 TO E5
C	2040	1500	11.52 MHZ	E1 TO E2, E3 TO E5
D	2040	2400	18.43 MHZ	E3 TO E5

NOTE: E3 TO E4 JUMPER FOR 4400 BPI

(4) INTERRUPT CHART

PROCESSOR	JUMPER
11/2	E6 TO E8
11/23	E6 TO E9

J1 - DISC CONNECTOR	
1	GND
2	
3	SA2*
4	
5	SINC*
6	ATTN1*
7	ATTN4*
8	ATTN3*
9	LAIL*
10	ATTN2*
11	CA128*
12	T200*
13	REMVD*
14	RESTOR*
15	GND
16	SC16*
17	CA2*
18	STROBE*
19	
20	SA8*
21	SA4*
22	WTCH*
23	WTGT*
24	CA256*
25	SAI*
26	TOPS*
27	
28	CA16*
29	SM*
30	DRDY*
31	CA64*
32	GND
33	CA8*
34	DWP*
35	CA32*
36	
37	ERGT*
38	WTPRO*
39	CA1*
40	CA4*
41	RDGT*
42	RDATA*
43	
44	RDCK*
45	RWS*
46	SELU1*
47	SELU2*
48	SELU4*
49	SELU3*
50	WDCK*

J2 - TEST CONNECTOR	
1	STOP+
2	DISROM+
3	DISPL+
4	CKEXT*
5	EXTRS*
6	READING*
7	WRITING*
8	GND
9	GND
10	GND
11	GND
12	GND
13	GND
14	GND

NOTES: UNLESS OTHERWISE SPECIFIED:

1. CAPACITANCE TOLERANCES AND VOLTAGES ARE AS FOLLOWS; PICOFARADS - ± 5%, 100V; 4.7 MICROFARADS - ± 20%, 10V; .15 MICROFARADS - ± 20% 20V.
2. CAPACITANCE VALUES ARE IN MICROFARADS
3. RESISTANCE VALUES ARE IN OHMS, ± 5%, 1/4W

(4) SEE CONFIGURATION SPECIFICATION C03500001 FOR (P)ROM, OSCILLATOR AND INTERRUPT VERSIONS.

C03304001	MODEL C03301	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES ±1/64 .XX ± .020 ±0°30' .XXX ± .010	DRAWN HAMPTON 11-79
NEXT ASSY.	USED ON	MATERIAL	CHECKED D. PASTERNAK 12-5-79
APPLICATION		FINISH	ENGINEER 12-5-79
		DO NOT SCALE DRAWING	APPROVED 12-5-79
			APPROVED

Dynus COSTA MESA, CALIF.

TITLE SCHEMATIC DIAGRAM - MODEL C03301 CARTRIDGE DISC CONTROLLER

SIZE	CODE IDENT. NO.	DRAWING NO.	REV.
D		C0330600I	A

SCALE NONE | WORK ORDER NO. | SHEET 1 OF 6

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
		SEE SHEET ONE		

(4) BS2901*
(3) P22+
(3) P23+
(3) P24+
(3) P25+
(4) BS2901L*
(SHEET 2,5) DATA BUS 7 6 5 4 3 2 1 0
(4) BD FILE*
U31 74LS 257
U32 AM 29701
U52 2901 (VCC=10 GND=30)
U33 AM 29701
U30 74LS 257
U28 74LS 257
U51
U16 74S 175
U19 74S 240
U29 74LS 153
U27 74S00
U6 8837
RM5 110
RM4 330
R8 1K
R10 1K
+5V
DM
CK
I0 I1 I2 AS
I3 I4 I5 ALU
I6 I7 I8 AD
B0 B1 B2 B3 A0 A1 A2 A3
CN RAM Q
OE
F=Z
D0+ D1+ D2+ D3+
D4+ D5+ D6+ D7+
Z0+
CO+
CN+
SM+
LD+
G7+
CN4+ RAM3+ Q3+
(4) CKG*
(3) P41+
(3) P42+
(3) P43+
(3) P44+
(3) P45+
(3) P46+
(3) P38+
(3) P39+
(3) P40+
(3) P31+
(3) P26+
(3) P27+
(3) P28+
(3) P29+
(3) P35+
(3) P36+
(3) P37+
(4) FILE CS*
(4) CKG*
J1-29 SM*
AMS*
P32+ P33+ P34+
(2) C+
(2) L+
(3) P47+ (C) P31+ (H)
RAM7+
J1-25 SA1* 2
J1-23 SA2*15
J1-21 SA4* 6
J1-20 SA8* 11
J1-6 ATTN 1*17
J1-10 ATTN2*4
J1-8 ATTN3*13
J1-7 ATTN4*8
(4) BSIR*
C1,2,4-9,11-14 4.7

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS DECIMALS ANGLES
±1/64 .XX ± .020 ±0°30'
.XXX ± .010

MATERIAL	DRAWN
FINISH	CHECKED
	ENGINEER
	APPROVED
	APPROVED

C03304001 NEXT ASSY. | MODEL C03301 USED ON | APPLICATION | DO NOT SCALE DRAWING

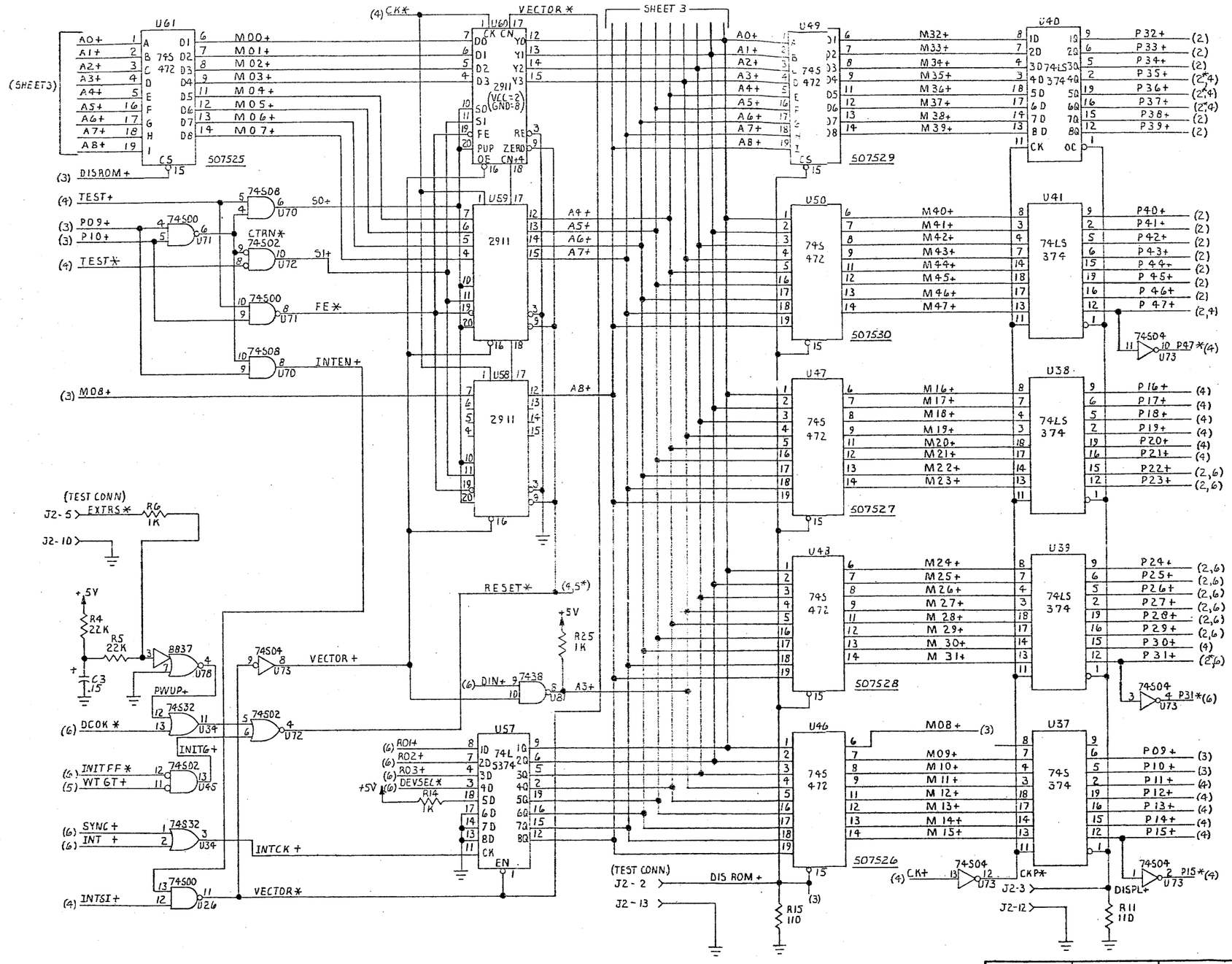
Dynus COSTA MESA, CALIF.

TITLE SCHEMATIC DIAGRAM — MODEL C03301 CARTRIDGE DISC CONTROLLER

SIZE D | CODE IDENT. NO. | DRAWING NO. C03306001 | REV. A

SCALE NONE | WORK ORDER NO. | SHEET 2 OF 6

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
		SEE SHEET ONE		



C0330400I	MODEL C0330I	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTION±.DECIMALS ANGLES ±1/64 .XX ±.020 ±0°30' .XXX±.010	DRAWN	Dynus COSTA MESA, CALIF.
NEXT ASSY.	USED ON	MATERIAL	CHECKED	TITLE SCHEMATIC DIAGRAM – MODEL C0330I CARTRIDGE DISC CONTROLLER
APPLICATION		FINISH	ENGINEER	SIZE D · CODE IDENT. NO. · DRAWING NO. C0330600I · REV. A
		DO NOT SCALE DRAWING	APPROVED	SCALE NONE · WORK ORDER NO. · SHEET 3 OF 6
			APPROVED	

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
		SEE SHEET ONE		

RM2 RM3 +5V
330 110
J1-30 DRDY* 8837 U5
RM4 RM5
J1-45 RWS* 8837 U5
RM2 RM3
J1-22 WTCH* 8837 U5
J1-9 LAIL* 8837 U5
RM4 RM5
J1-5 SINC* 8837 U5
J1-34 DWP* 8837 U5
RM4 RM5
J1-12 T200* 8837 U6
J1-16 SC16* 8837 U6
+5V
RM1 10K
SW1
SW4* SW3* SW2* SW1*

DRDY+ RWS+ WTCH+ LAIL+ SINC+ DWP+ T200+ SC16+
(3) P47+
U18 74S 251
(6) POK+ (6) RDIO* (6) WDL+ (5) RDL+
U17 74S 251
(3) P35+ (3) P36+ (3) P37+ (3) P47*

(4) CK+ U4 74S 374 (4) CK*
ATEST+
(6) MSTS+ (6) RPLY+ (5) ORE* (5) IRF* (6) INTSD+ (3) RESET* (2) SMI*
U3 74LS 374
ATST+ (2) Z+ (2) C+
INTS1+ (3) RESET1* (6) MSTR+ (6)
MSTR+ REPLY+ ORE1* IRF1* INTS1+ RESET1* SECTM*
U2 74S 251
(3) P15+
U1 74S 251
TEST* (3) TEST+ (3,4)

(6) MO+ (6) WB+ 74S08 U13 NWL0* NWH1*
(6) MO* 74S08 U15
(3) P12+ (3) P13+ (3) P14+ (3) P15*

(3) P30+ 74S08 U70 DMAEN+ (6)
(3) P11+ (4) TEST+ 74S00 U26
EXEC+

U15 74S 138
(4) CKB* (4) CK*
(3) P16+ (3) P17+ (3) P18+
BDFILE* BDDR1* BDDR2* BDDR3*
(2) (3) P19+ (3) P20+ (3) P21+
U14 74S 138
BS2901* (2) BS2901L* (2) BSDAL* (6) BSFIFO* (5) BSFILE* BSIR* (2)
74S08 U13
FILECS* (2)
74S04 U44 BDFIFO+ (5)
BDDAL* (6) BDFIFO*
J1-1 J1-15 J1-32
+5V R7 1K

CX 1K +5V R9
CKA* 74S00 U26 CK+
U25 74S 175
E2 E1 E0 E4 E3 (4)
CKA+ CKB+
+5V Y1 OSC OSC* DK1 DL1
CKCD+
CKB* (4)
STOP+ J2-1
110 R20 J2-14
74S00 U27 CKEXT* J2-4 J2-11
CKD+ (5) CKD* (5)
74S00 U26 CKG* (2,5)
74S00 U27 CK* (3,5,6)
74S02 U72 CK+ (4,6,3)

C03304001	MODEL C03301	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES ±1/64 .XX ±.020 ±0°30' .XXX±.010	Dymus COSTA MESA, CALIF.
NEXT ASSY.	USED ON	MATERIAL / FINISH	DRAWN / CHECKED / ENGINEER / APPROVED / APPROVED
APPLICATION	DO NOT SCALE DRAWING		TITLE SCHEMATIC DIAGRAM - MODEL C03301 CARTRIDGE DISC CONTROLLER
			SIZE D · CODE IDENT. NO. · DRAWING NO. C03306001 · REV. A
			SCALE NONE · WORK ORDER NO. · SHEET 4 OF 6

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
		SEE SHEET ONE		

FIFO & DISK OUTPUT REGS

C0330400I	MODEL C0330I	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES ±1/64 .XX ±.020 ±0°30' .XXX±.010	DRAWN	Dynus COSTA MESA, CALIF.
NEXT ASSY.	USED ON	MATERIAL	CHECKED	TITLE SCHEMATIC DIAGRAM- MODEL C0330I CARTRIDGE DISC CONTROLLER
APPLICATION		FINISH	ENGINEER	SIZE D / CODE IDENT. NO. / DRAWING NO. C0330600I / REV. A
		DO NOT SCALE DRAWING	APPROVED	SCALE NONE / WORK ORDER NO. / SHEET 5 OF 6
			APPROVED	

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
		SEE SHEET ONE		

(SHEET 25) DATA BUS 7 6 5 4 3 2 1 0

U74 8641: BDAL15 L (BV2), BDAL14 L (BU2), BDAL13 L (BT2), BDAL12 L (BS2) → R15+, R14+, R13+, R12+, T15+, T14+, T13+, T12+

U75 8641: BDAL11 L (BR2), BDAL10 L (BP2), BDAL09 L (BN2), BDAL08 L (BM2) → R11+, R10+, R09+, R08+, T11+, T10+, T09+, T08+

U76 8641: BDAL07 L (BL2), BDAL06 L (BK2), BDAL05 L (BJ2), BDAL04 L (BH2) → R07+, R06+, R05+, R04+, T07+, T06+, T05+, T04+

U77 8641: BDAL03 L (BF2), BDAL02 L (BE2), BDAL01 L (AV2), BDAL00 L (AU2) → R03+, R02+, R01+, T03+, T02+, T01+, T00+

(6) INITFF+

(6) BS7+

(6) DALEN *
(4) BDDAL *
(3) P31 * (H)
(3) P31 + (H)
(4) BSDAL *

BDMGOL (CS2)
BDMGIL (CR2)
BIAKOL (CN2)
BIAKIL (CM2)

U62 74LS 257: R15+ → D7+, R14+ → D6+, R13+ → D5+, R12+ → D4+

U63 74LS 377: R11+, R10+, R09+, R08+, T11+, T10+, T09+, T08+

74LS30 U66: BS7+, R12+, R11+, R10+, R09+, R08+

74S02 U67: T07+, T06+

74S02 U67: T05+, T04+

U64 74LS 377: R03+, R02+, R01+, T03+, T02+, T01+, T00+

U65 74LS 257: T03+ → D3+, T02+ → D2+, T01+ → D1+, T00+ → D0+

R03+ (3)
R02+ (3)
R01+ (3)

U55 74LS 377: (3) P24+, P25+, P26+, P27+, P28+, P29+ → TWB+, TDOUT+, TDIN +, TSACK+, TSYNC+, TDMR +

(3) P22+

(4) CK+
(4) DMAEN+ → 74S00 U71 → DMACK * (6)

74S02 U56: RDID* (4) → PID+

DEVSEL* (3)

SRN+

U69 74LS 375: SEL*, RDO+, (3) P23+, (3) P26+ → MD+ (6), MD* (6), DET (6)

74S02 U56: RPLY+ (4)

74LS08 U54: CLAIM +

DMACK+

(6) DMACK* → 74S00 U71

(5) INTR+
(6) IRQ67* → 74S08 U63

TSACK*
DMG+

74LS08 U54: 180 R13, DMG2+, 820PF C10

74S74 U53: CLAIM * / DMG +

CLAIM D+ (5)

180 R23, 390 R24, 180 R21, 390 R22, +5V

AR2 BDMGIL
AM2 BIAKIL
AT2 BINITL
(4) CK*
BA1 BDCOKH
BB1 BPOKH

8837 U78: DIN+, IAK+, INIT+, POK*

+P(S)

74S74 U42: IAKA+, IAKA *

74S74 U13

74LS08 U54: INT+ (3), INITFF* (36)

74S32 U34: INTSD+ (4)

DCOK* (3)
POK + (4)

PIO +

74S04 U44

(4) RESET1*

U79 8641: TWB+, IRQ6+, IRQ7+ → BWTBTL (AK2), BBS7L (AP2), BIRQ6L (AB1), BIRQ7L (BP1)

74S02 U67: (6) DE+, (4) MSTR+ → DALEN* (6,5), IRQ67* (6), BS7 + (6), WB + (4), SYNC + (3)

R28 10K +5V
R26 10K +5V

U80 8641: INITFF+ (6), TDOUT+, TDIN +, TSYNC+, (5) TRPLY+, DOUT +, DIN +, SYNC +, RPLY+ → BDOUTL (AE2), BDINL (AH2), BSYNCL (AJ2), BRPLY L (AF2)

DIN+ (3)
MSTS+ (9)

TSACK → 7438 U28 → BSACKL (BN1)

TDMR+ → 7438 U68 → BDMRL (AN1)

BDMGOL (AS2)

BIAKOL (AN2)

DAL INTERFACE

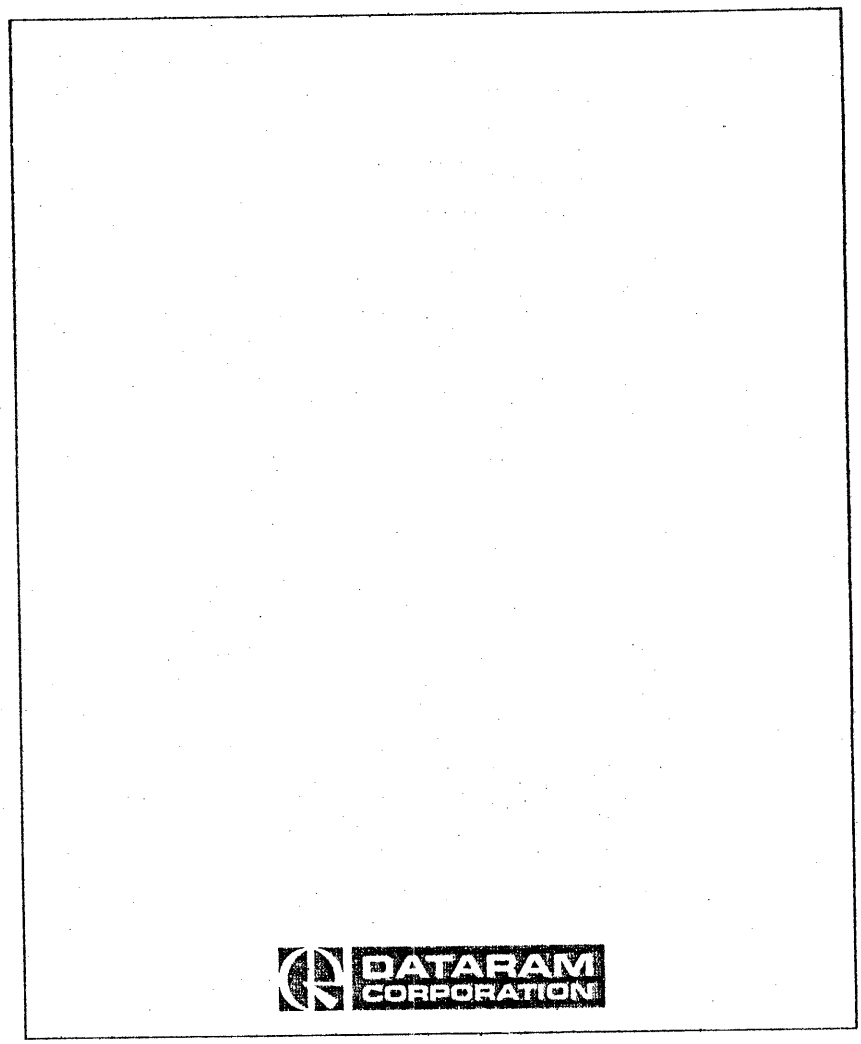
C0330400I	MODEL C0330I	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES ±1/64 .XX ± .020 ±0°30' .XXX ± .010	THE DRAWING CONTAINS INFORMATION PROPRIETARY TO DYNUS INCORP. PUBLISHED AND NOT TO BE DISCLOSED, COPIED OR USED FOR OTHER THAN THE PURPOSE FOR WHICH IT IS FURNISHED WITHOUT PRIOR WRITTEN PERMISSION FROM AN OFFICER OF THE ABOVE FIRM.
NEXT ASSY.	USED ON	MATERIAL / FINISH	DRAWN / CHECKED / ENGINEER / APPROVED / APPROVED
APPLICATION		DO NOT SCALE DRAWING	

Dynus COSTA MESA, CALIF.

TITLE SCHEMATIC DIAGRAM MODEL C0330I CARTRIDGE DISC CONTROLLER

SIZE	CODE IDENT. NO.	DRAWING NO.	REV.
D		C0330600I	A

SCALE NONE | WORK ORDER NO. | SHEET 6 OF 6



PRINCETON-HIGHTSTOWN ROAD
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