

DATA TRANSLATION

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DT212 DUAL D/A CONVERTER-POINT PLOTTER

USER INSTRUCTION GUIDE

INTRODUCTION

The DT212 is the first commercially available module for controlling analog X-Y devices such as CRT displays and pen plotters. The 212 contains two 12-bit D/A converters which translate digital data words into analog position and control signals. Intensify logic is incorporated for handling the overhead functions for timing and generating CRT intensify pulses. Two bits are also stored and decoded into four control lines for ancillary functions such as pen-up pen-down, erase, store, and any other control elements in the equipment driven by the DT212.

This guide explains the circuit functions employed in the DT212 so that applications can be implemented rather quickly. The second section describes troubleshooting and calibration with the final chapter oriented toward specific hardware the DT212 may interface with.

CHAPTER I FUNCTIONAL DESCRIPTIONS

The DT212 requires 12 bits (or less) of input data to control the two D/A converters. Each converter has a separate register for latching and holding the digital word presented. The D/A converters respond immediately to the data stored in the registers and settle the converted analog output voltage within 1 μ s (to 0.1% accuracy; 3 μ s to .01%) from the time the data word is strobed into the register. The X or Y register to store the data is first selected by the select bit (pin 17L). A TTL LO will select X, a HI select Y. The select bit is stored in a latch which enables the appropriate 12-bit register selected to "receive" the incoming data word. The select bit is applied to pin 17L and clocked into the select flop by applying a positive going edge (0 to 5 volts) to pin 28u. The select bit must be stable 30ns during and after the clock select edge to guarantee proper loading into the select flop. After the X or Y storage register has been selected,

data may be loaded into the selected register. This is accomplished by generating a positive edge (0 to +5 volts) on the clock data pin (29L). The data must be stable 50ns during and after the clock data signal for accurate loading of the data word. The data must not be loaded until the X-Y select has been accomplished. Data may be loaded 50ns after X-Y select is loaded.

The coding for the data word is selected by appropriate routing of the most significant bit (MSB). The input data is positive true (HI=1, LO=0 1 T²L load.) The coding will be 2's compliment. If offset or straight binary is desired, the MSB must be inverted. This can be done by utilizing the inverter provided in the DT212 (pin 24U input, pin 25U output) and tying the inverted output to the MSB (pin 25U to pin 23U). The range of full scale analog voltage is selected by appropriate jumping of pins per range chart, Fig. 1*. Both D/A outputs have power amplifiers to facilitate driving coaxial and other high capacitance loads. The amplifiers can deliver $\pm 25\text{mA}$ at full output voltage and will maintain risetimes and settling characteristics through up to 50 feet of cable. When using coaxial cables, the remote end must be terminated in order to eliminate reflections and ringing. The cables should be terminated with 470Ω on the ± 10 volt and 0 to +10 volt ranges, and 270Ω on the ± 5 volt ranges. This will insure $3\mu\text{s}$ settling to .01%.

An additional input is provided on the output amplifier for summation of analog signals with the converted analog signal from each D/A. These inputs are pin 10L for X and pin 4U for Y. These inputs, labeled "character", allow analog voltages to be algebraically summed with the D/A position voltage and are useful when adding character or vector signals in more sophisticated CRT display applications. The character inputs have an impedance of 5000Ω and are inverting at the output of each D/A (i.e. a positive going character signal produce a negative going output from the D/A). The character input gain depends upon the D/A output range selection and is -0.5 for 10 volts and -1.0 for ± 5 volts.

Less Resolution can be utilized (but 12-bit linearity will be maintained) by simply not using LSB's (least significant bits). For 10 bit words, tie bits 11(26L) and 12(27L) to ground (logic low).

The intensify section of the DT212 has been designed for the control of blanking and unblanking of CRT's. All CRT displays require a finite time to position the beam with the internal deflection amplifiers. The longest settling time will be for full screen deflections, Magnetically deflected scopes are the slowest taking from 15 to 20 μs for a refresh type, up to 70 μs for a storage type such as the Tektronix 611 and 613. Electrostatic displays like those available from both

* Fig. 1 of DT212 data sheet

Hewlett Packard and Tektronix take from 1 to 5us. When position information is presented to display, an appropriate delay must be employed before attempting to intensify the screen. If this is not done, the beam may be turned on while still in motion to its final position creating a smeared dot that is incorrectly positioned. The DT212 allows an intensify command to be issued concurrent with the loading of the second position D/A as it incorporates a built in delay to allow the scope to settle before actual issuance of the intensify pulse. This alleviates a software burden of having to time out the required set up delay and also allows one computer word to both set up the second D/A position and issue an intensify command (it is assumed that the first D/A position information had already been loaded.)

The beam start command is a positive going edge (0 to +5V) and initiates an intensify cycle (which includes a set up delay and then issuance of an intensify pulse). Two set up delays may be selected, set 1=3 us (tie pin 16L to pin 18L) and set 2=70us (tie pin 16U to pin 18L). Other setup delays can be selected by incorporating an external capacitor (between pin 32U and 34L) with or without an external resistor (between pin 34L and +5 volts).

The external resistor may be added as a trim. A decrease in resistance between pin 34L and +5V will shorten the delay.

After the delay has timed out an intensify signal pulse will be generated. Both polarities of this pulse are available and may be applied to the input of the pulse amplifier (which inverts). The (Z-) will produce a "negative" pulse output (HI, LO, HI) the Z+ will produce a positive going pulse (LO, HI, LO). The pulse amplifier can drive up to 50 feet of coaxial cable while maintaining 100ns risetime, but again the remote end must be terminated (with 47 Ω) to prevent ringing and reflections. The Z output is TTL compatible. The pulse widths may be selected by addition of an external capacitor between pin 19U and pin 18L.

The addition of a resistor between pin 18L and +5 volts will allow the width to be adjusted. Decreasing the resistance will shorten the pulse width.

Two bits of control information may be supplied to the DT212. These bits can be loaded and stored by applying a positive going edge (0 to +5 volts) to pin 26U mode clock. The two bits must be stable 30ns during and after mode clock. The two bits are positive true and will appear decoded at pins 31L(mode 0), pin 28L(mode 1), pin 33U(mode 2), and pin 27U(mode 3).

The mode outputs are LO when asserted and can drive 10 TTL loads.

For XY recorders, one of the decoded mode bits may be used for pen-up, pen down.

Note 1: Analog and digital ground are not tied together in the module. These grounds must be tied together at one point in the system to avoid errors in the D-A outputs.

Note 2: Device select, pin 29U must be low to enable all clock inputs a high will gate off all clock inputs (Mode 26U, X-Y Select 28U, Clock Data 29L). Master clear, 30L, when low allows normal operation, when high forces mode to mode zero and X-Y select to X.

CHAPTER 2 CALIBRATION

The D/A outputs have a relative accuracy and linearity of 0.025%. This means each bit will represent its weight to within .025% of full scale, i.e. the MSB is 0.5000 of full scale, next MSB (bit 2) is 0.2500 of full scale, etc. The absolute value of the output voltage may be adjusted as well as the offset to achieve better than $\pm 0.5\%$ output absolute accuracy. Potentiometers are applied as shown on page 2 of DT212 data sheet.

The offset is always adjusted first. Apply (MSB 100 000 000 000 (LSB) (2's complement coding) to the D/A being calibrated, and adjust the offset pot for 0 volt output on 0 to +10 volt range, -5.000 volts on ± 5 volt range and -10.000 volts on ± 10 volt range. If offset binary coding is used, employ the internal inverter for the MSB and apply 000 000 000 000 (the MSB being applied to the input of the inverter).

The full scale adjustment can be made by applying 011 111 111 111 (2's complement) to the D/A being adjusted and trim the range pot for 9.9976 volts 0-10V, 4.9951 for ± 5 and 9.9951 for ± 10 volts. Again if offset binary is utilized, use the internal inverter to complement the MSB.

0 to +10V, f.s. = 9.9976V ± 10 V, f.s. = 9.9951 ± 5 V, f.s. = 4.99

The linearity may be checked now by applying the MSB with all other bits off and seeing exactly half scale (5.000V 0-10, 0 for ± 5 and ± 10 volts.)

TROUBLESHOOTING

Input Data

Registers

D/A's

Load select bit X (LO at Pin 17L) and load and full scale code while monitoring X's output for proper response. Be sure clear pin 30L and Device Select 29U are LO or data will not be loaded. Repeat for Y by loading a HI at pin 17L.

Issue a Beam Start (LO to HI) and monitor Z(+) pin and Z(-).

Z amp

Apply Z(-) pin 15U to Z amplifier input (pin 17U). The Z out should invert and follow the Z(-). Apply Z (+) pin 19L to Z amplifier input (pin 17U). The same but opposite response should occur. Be sure Device Select and Clear (pins 29U and 30L) are LO.

Mode Select

Apply 00 to pins 32L and 34U and clock mode bits in at pin 26U.
Pin 31L (mode 0 out) should be a Low.
01 will produce a Low at pin 28L (mode 1).
10 will produce a Low at pin 33U (mode 2).
11 will produce a Low at pin 27U (mode 3).