DPC 233730N

TECHNICAL MANUAL

FOR

LINE PRINTER
MODELS
2420/2440/2470

VOLUME II

Dataproducts

6219 DE SOTO AVENUE

WOODLAND HILLS, CALIFORNIA 91364

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SECTION VII

LOGIC DIAGRAMS

7-1 INTRODUCTION

7-2 This section is provided primarily as an aid to personnel engaged in maintenance or troubleshooting procedures and in support of the printer circuit descriptions given in the Theory of Operations section of Volume I of this manual. It contains detailed information representing the functional logic used in the printer.

7-3 ORGANIZATION

7-4 This section is organized into the following parts:

a. Logic Diagram Alphabetical Index and Locator

b. Glossary of Mnemonic Terms

c. Logic Diagram Sheets

(1) Circuit Card and Assembly Locator

(2) Interconnect Diagrams

(3) System Flow Charts

(4) Circuit Card and Assembly Logic Diagram Sheets

7-5 LOGIC DIAGRAM ALPHABETICAL INDEX AND LOCATOR (table 7-1)

7-6 This index alphabetically lists the logic diagrams by circuit card or assembly description, card type, logic sheet number, reference location figure, and applicability to model configuration. Using the circuit card or assembly name, the user can quickly locate the appropriate logic diagram and determine its reference assembly designation and model applicability.

7-7 GLOSSARY OF MNEMONIC TERMS (table 7-2)

7-8 This glossary alpha-numerically lists the coded terms used to identify the logic circuit signals, the equation for the term, the logic diagram sheet point of origin, and a definition of the term. Primarily, each mnemonic term is an acronym or abbreviated composite of the words in the phrase defining that term. These terms are derived from the input or inputs to its logic element. The definition of the term describes the function of the logic signals in the printer. As an example, table 7-2 defines the term TAST as logic output signal "Tape Advance Step" derived from input signals CONT, VFTA, and SLFF* and appears in logic diagram sheet 27.

7-9 LOGIC DIAGRAM SHEETS

7-10 Included in the logic diagram sheets are the circuit card and assembly locators, interconnection diagrams, system flow charts, and the logic diagrams of the circuit cards and assemblies used in the printer.

7-11 Circuit Card and Assembly Locator (sheets 1, 1A, and 1B)

7-12 Depending on the model configuration, the circuit card and assembly locations are shown in logic diagrams 1 (2420), 1A (2440), and 1B(2470). Circuit card locations are assigned as an alpha-numeric suffix to the location assigned its next higher assembly which is also assigned alpha-numerically. Each card slot location shown is identified with a particular alpha-numeric type circuit card, description of the card and the applicable logic diagram sheet number.

7-13 Interconnection Diagrams (sheets 2, 2A, and 2B)

7-14 Interconnection diagrams for the 2420, 2440, and 2470 printers are shown in logic diagram sheets 2, 2A, and 2B respectively. They are provided to aid the user in determining the interconnection between major assemblies in the printer and between circuits which contribute to a certain operation or function of the printer.

7-15 System Flow Charts (sheets 4 - 4C)

7-16 Flow charts 4 through 4C depict sequentially the logic functions that occur during the different modes of printer operation. Tie points on each sheet are cross-referenced to their mutual connections within a sheet and/or between sheets for ease of continuity when personnel are tracing through the functions. Each operation or decision symbol in the flow charts is identified with its mnemonic term and the appropriate logic diagram sheet(s) which functionally describes the operation. Any mnemonic term noted in the flow charts can also be found in the glossary of mnemonic terms for its definition.

7-17 Circuit Card and Assembly Logic Diagram Sheets (sheets 5 - 57)

7-18 These logic diagram sheets symbolize the printer circuits according to function, identify the input and output signals with the appropriate mnemonic terms, provide the mnemonic term source and destination information, and indicate the location of the circuit assembly referenced on the sheet. Pulse durations of the various single-shot circuits contained in the logic diagrams are also shown.

7-19 LOGIC SYMBOLS. With two exceptions, the logic symbols in the drawings throughout this manual are standard and described in MIL-STD-806B.

7-20 A small circle at the input of a logic element indicates that the relatively low (L) input signal activates the function. Conversely, the absence of a small circle indicates that the relatively high (H) input signal activates the function.

7-21 A small circle at the output of a logic element indicates that the output of the activated function is relatively low. Conversely, the absence of a small circle indicates that the output of the activated function is relatively high.

7-22 Examples of some common functions of two variables and their equivalents are shown below in figure 7-1.

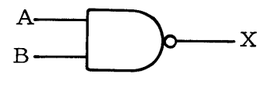
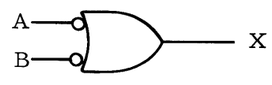
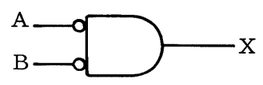
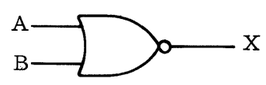
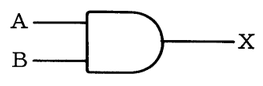
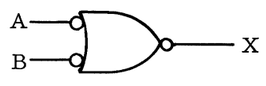
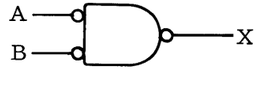
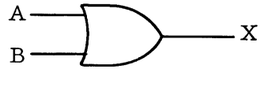
AND Symbol	OR Symbol	Inputs A	Inputs B	Outputs X
		H	H	L
		H	L	H
		L	H	H
		L	L	H
		H	H	L
		H	L	L
		L	H	L
		L	L	H
		H	H	H
		H	L	L
		L	H	L
		L	L	L
		H	H	H
		H	L	H
		L	H	H
		L	L	L

Figure 7-1. Common Functions of Two Variables and Equivalents

7-23 The exceptions to MIL-STD-806B are as follows:

a. An asterisk (*) replaces the overbar used to denote the inverted or "not" function of a term.

b. The symbol for a J-K flip-flop is shown in figure 7-2 below:

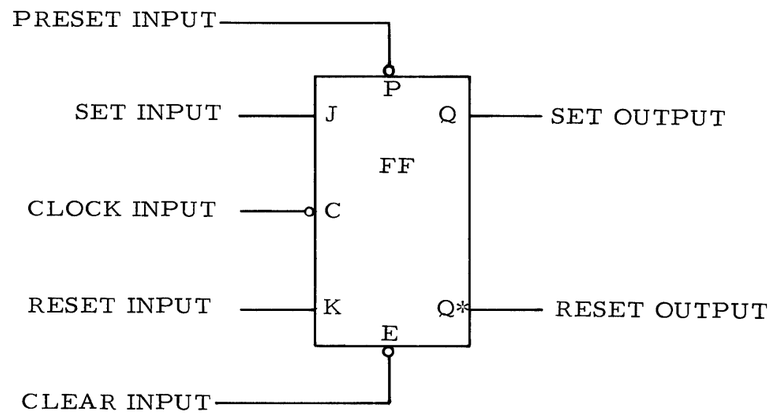


Figure 7-2. J-K Flip-Flop

7-24 J-K FLIP-FLOP (figure 7-3). The following paragraphs are intended as an aid in understanding and troubleshooting the J-K master/slave flip-flop (hereafter called the J-K flip-flop) used throughout the printer logic.

7-25 Two J-K flip-flops, each consisting of two distinct flip-flops (master/slave) and associated gates and diodes, are housed in one integrated circuit chip.

7-26 Each J-K flip-flop has five distinct inputs and two outputs as follows:

a. J = Set input with clock

b. K = Reset input with clock

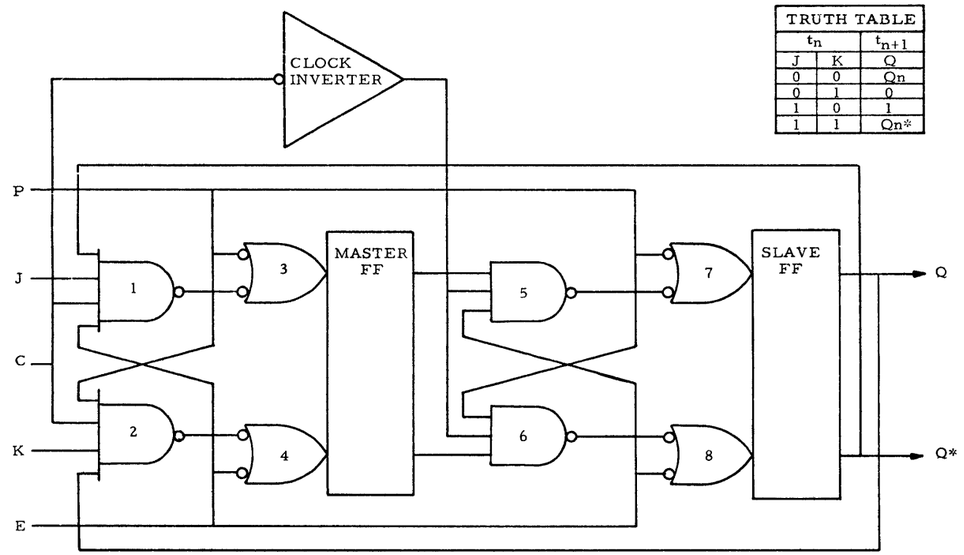
c. E = DC clear (reset) input without clock

d. P = DC set input without clock

e. C = Clock input (clocks on trailing edge of positive pulse)

f. Q = Set output

g. Q* = Reset output



TRUTH TABLE		
t_n		t_{n+1}
J	K	Q
0	0	Qn
0	1	0
1	0	1
1	1	Qn*

Figure 7-3. J-K Flip-Flop Logic

7-27 Since the J-K flip-flop consists of two flip-flops (master and slave), the master is conditioned first and the slave flip-flop is conditioned at a later time to reflect the initial state of the master flip-flop. The conditioning of the master and subsequent transferring of intelligence to the slave flip-flop is accomplished under the control of the clock input. The possible operating conditions of the J-K flip-flop are described in the following paragraphs.

7-28 DC Set. If input P goes low, NAND gates 2 and 6 are inhibited and NOR gates 3 and 7 are enabled, setting both the master and slave flip-flops. Output Q goes high and remains high until P goes high and another operating state is initiated.

7-29 DC Reset. If input E goes low, NAND gates 1 and 5 are inhibited, and NOR gates 4 and 8 are enabled, resetting both the master and slave flip-flops. Output Q* goes high and remains high until E goes high and another operating state is initiated.

7-30 Set With Clock. Assuming input J is high, all other inputs are inhibited, and the J-K flip-flop is at present reset, the following takes place.

7-31 Since J, E, and Q* are high, NAND gate 1 is enabled when C (clock) goes high and the master flip-flop is set. The output of the clock inverter goes low and disables NAND gate 5. The slave flip-flop is thus prevented from responding to the master flip-flop output for the duration of the clock. Once the master flip-flop is set, J can go low as it has no further effect on the J-K flip-flop state in this operation.

7-32 When C goes low, the clock inverter output goes high, enabling NAND gate 5 and setting the slave flip-flop. Output Q goes high and remains high until another operating state is initiated. Since Q* is now low, NAND gate 1 is inhibited and the present state is maintained if J again goes high. To change state requires that K go high or E go low.

7-33 Reset With Clock. Assuming input K is high, all other inputs are inhibited, and the J-K flip-flop is at present set, the following takes place.

7-34 Since K, P, and Q are high, NAND gate 2 is enabled when C (clock) goes high and the master flip-flop is reset. The output of the clock inverter goes low and disables NAND gate 6. The slave flip-flop is thus prevented from responding to the master flip-flop output for the duration of the clock. Once the master flip-flop is set, K can go low as it has no further effect on the J-K flip-flop state in this operation.

7-35 When C goes low, the clock inverter output goes high, enabling NAND gate 6 and resetting the slave flip-flop. Output Q* goes high and remains high until another operating state is initiated. Since Q is now low, NAND gate 2 is inhibited and the present state is maintained if K again goes high. To change state requires that J go high or P go low.

7-36 Inputs J and K High. If J and K are high simultaneously, and E and P are inhibited, then the J-K flip-flop toggles to the state opposite that which it was prior to the arrival of the clock.

7-37 Inputs J and K Low. If J and K are low simultaneously and E and P are inhibited, then the J-K flip-flop cannot toggle and remains at the state that it was prior to the arrival of the clock.

7-38 Inputs E and P Low. This is an abnormal operating condition but if E and P should go low simultaneously, the J-K flip-flop acts on both conditions and outputs Q and Q* go high at the same time.

7-39 SIGNAL FLOW (SOURCE/DESTINATION) AND MNEMONIC TERMS (figure 7-4). Signal flow information on most logic diagram sheets in this section is from left to right. Inputs to a logic circuit element begin on the left with one or more mnemonic terms. The output, as a composite or function of the input, flows out the right side of the logic element (or, in many cases, a series of elements interconnected) as a single mnemonic term. Thus, the signal source (output) will provide the mnemonic term and one-or-more logic sheet destinations for that term. At the logic sheet destination (input), the mnemonic term is again shown along with the source logic sheet number and pin number. Cross-referencing is thus provided to enable the reader to work swiftly between logic diagram sheets for troubleshooting, maintenance, or circuit analysis purposes. Figure 7-4 illustrates the signal flow methods presented in the logic diagram sheets.

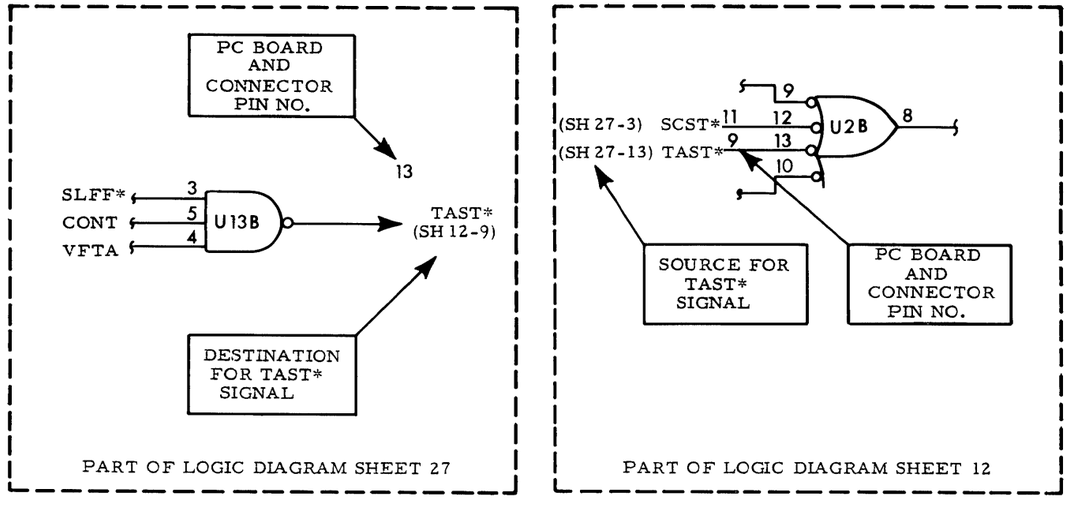


Figure 7-4. Example, Signal Source and Destination and Mnemonic Term

7-40 REFERENCE LOCATIONS. Each logic diagram sheet notes the location of its particular assembly or circuit card according to an alpha-numeric assignment which is its assembly number in the printer. The assembly number is placed as a suffix to its next higher assembly number in which it is included. For example, sheet 12 references A3A15 as the location for its circuit card assembly and can be interpreted as follows:

A3	A	15
Electronics Gate Assembly A3 (Major Assembly)	Card Cage Assembly A	Card Slot 15 in Card Cage A

NOTE

In some cases the major assembly only is provided as the reference location on certain diagram sheets.

7-41 Location drawings are shown in logic diagrams 1, 1A, and 1B which start with a major assembly and include circuit-card assemblies.

TABLE 7-1. LOGIC DIAGRAM ALPHABETICAL INDEX & LOCATOR

Circuit Card or Assembly Description	Card Type	Logic Sheet No.*	Ref Assembly	Model		
				2420	2440	2470
AC Primary Circuits		42, 42A		x		
AC Primary Circuits		43, 43A			x	x
Auxiliary Control Panel (Option)		57			x	x
Bit Memory, 150 x 4	AM-26	7	A3A22	x	x	x
Bit Memory, 150 x 4	AM-26	8	A3A23	x	x	x
Circuit Card Complement		1 - 1B		x	x	x
Code Conversion (Option)		53, 53A	A3A9	x	x	x
Code Set, 64-Character		44		x	x	x
Code Set, 96-Character (Option)		52		x	x	x
Counter Compare	AC-16	14	A3A21	x	x	x
Counter Compare (136 and 120 Column Option)	AC-19	51	A3A21	x	x	x
Data Register	AG-33	6	A3A24	x	x	x
DC Distribution Diagram		28A		x		
DC Distribution Diagram		32A			x	x
Diode Board, Hammer Driver Circuits		23A	A12	x		
Diode Board, Hammer Driver Circuits		24B	A12		x	

TABLE 7-1. LOGIC DIAGRAM ALPHABETICAL INDEX & LOCATOR (Contd)

Circuit Card or Assembly Description	Card Type	Logic Sheet No.*	Ref Assembly	Model		
				2420	2440	2470
Diode Board to Hammer Bank Interconnection		26		x	x	
Drum Gate Electronics		41	A1	x	x	x
Drum Speed, Phasing & Penetration Controls (Option)		49		x	x	x
Elapsed Time Meter (Option)		50		x	x	x
Hammer Bank Power Supply		36	A8		x	
Hammer Bank Power Supply		36A	A8			x
Hammer Current Monitor	AS-46	20	A3A2	x		
Hammer Driver Circuits Typical Interconnection		23	A3A1-A3A12	x		
Hammer Driver Circuits Typical Interconnection		24, 24A	A3A1-A3A12, A3B1-A3B12		x	
Hammer Driver Circuits Typical Interconnection		25-25D	A3A1-A3A12, A3B3-A3B25			x
Hammer Driver Protection	AS-40	21	A8A1		x	x
Hammer Fanout	AZ-116	19	A3A8	x	x	x
Interconnection Diagram		2		x		
Interconnection Diagram		2A			x	
Interconnection Diagram		2B				x

TABLE 7-1. LOGIC DIAGRAM ALPHABETICAL INDEX & LOCATOR (Contd)

Circuit Card or Assembly Description	Card Type	Logic Sheet No.*	Ref Assembly	Model		
				2420	2440	2470
Main Harness & Printer Mechanics		38, 38A	A3A	x		
Main Harness & Printer Mechanics		39-39B	A3A		x	x
Master Clear Switch	AZ-115	9	A3A13	x	x	x
Mode Logic	AG-34	10, 10A	A3A25	x	x	x
Operator Control Panel		40	A4	x	x	x
Paper Feed Amplifier	AP-15	34	A6A1		x	x
Paper Feed Control	AP-16	29	A5A1	x		
Paper Feed Control Power Supply		33	A6		x	x
Paper Feed Logic	AC-17	12	A3A15	x	x	x
Paper Feed Power Amplifier	AP-33	35	A6A5, A6A6		x	x
Paper Feed Power Amplifier	AP-34	35A	A6A3, A6A4		x	x
Paper Motion Sensor		55	A2A2		x	x
Parity (Option)	AL-11	46	A3A18	x	x	x
Power & Frequency Kit (Option)		50		x	x	x
Power Supply		28	A5	x		
Protect	AG-55	54	A3B26		x	x

TABLE 7-1. LOGIC DIAGRAM ALPHABETICAL INDEX & LOCATOR (Contd)

Circuit Card or Assembly Description	Card Type	Logic Sheet No.*	Ref Assembly	Model		
				2420	2440	2470
Receiver & Positive Driver & I/O Harness	AL-25	5	A3A20	x	x	x
Regulated Power Supply		32	A5		x	x
Ribbon Control	AZ-15	31	A5A3	x		
Ribbon Control	AP-17	37	A8A2		x	x
Ribbon Servo Assembly		56	A2A1		x	x
Self Test (Option)	AL-23	48	A3A19	x	x	x
Static Eliminator (Option)		50		x	x	x
System Flow Charts		4-4C		x	x	x
Timing Board	AT-24	11	A3A26	x	x	x
Transducer Amplifier	AS-26	13	A3A14	x	x	x
Vertical Format Unit, 8 Channel	AG-44	27	A3A17	x	x	x
Vertical Format Unit, 12 Channel	AZ-164	47	A3A16	x	x	x
Voltage Regulator	AV-10	30	A5A2	x		
Zone Logic, 6	AG-36	15	A3A10	x		
Zone Logic, 2	AG-37	16	A3A10		x	
Zone Select	AH-24	17	A3A11	x		
Zone Select	AG-25	18	A3A11		x	

* Sheet numbers not assigned are 3, 22, and 45.

TABLE 7-2. GLOSSARY OF MNEMONIC TERMS

Term	Equation	Logic Diagram	Definition
ADVANCE	= CHCK		(Count Up)
BFSTR(R)	= LOAD TS04 (CLK) + PRINT TS07 (CLK) +SCEN TS07 (CLK) + MC2	SH 11	Buffer Strobe
BFSTR(S)	= LOAD CONTFF* TS02 (CLK) + PRINT TS05 (CLK) + SCEN TS05 (CLK)		
BFTC	= CC00. CC01. CC06. CC07	SH 14	Buffer Top Count Count 149 (MOD 12)
BPOR	= ON LN SW	SH 19	Bottom Paper Out Override
BTSW		SH 39	Bottom Paper Out Switch
CC00 thru CC07		SH 14	Column Counter
CC12(R)	= CCAV (CLK) + CCCL	SH 14	Column Counter Twelve
CC12(S)	= CC00 CC02 CC03 (CLK)		
CCAV	= LOAD TS04 CONT F/F* (CLK) + SCEN BFTC* TS08 (CLK) + PRINT TS08 (CLK)	SH 14	Column Counter Advance
CCCL	= MC2 + CONT + CCRS	SH 14	Column Counter Clear
CCRS(R)	= CCRC (CLK) + MC2	SH 14	Column Counter Reset
CCRS(S)	SCEN BFTC TS08 (CLK)		
CENF(R)	= MC1F + CONT	SH 9	Control Enable Flip-Flop

TABLE 7-2. GLOSSARY OF MNEMONIC TERMS (Contd)

Term	Equation	Logic Diagram	Definition
CENF(S)	= ONLN* (PSSW) + ONLN* (FFSW)		
CH01 thru CH07		SH 14	Character Counter (Binary Counter)
CHCK(R)	= CHST* (CLK)	SH 13	Character Clock, Character Counter Advance
CHCK(S)	= CHST (CLK)		
CHCKPO		SH 41	Character Clock Pickoff
CHRS	= CIF1 CIF2 CHCK	SH 13	Character Counter Reset
CHS1(R)	= TS07 (CLK) CHCK* + MCLD	SH 13	Character Clock Sync Enable
CHS1(S)	= CHCK		
CHSN(R)	= TS01	SH 13	Character Clock Sync
CHSN(S)	= CHSN* (CHS1)		
CHSS	= CHCKPO	SH 13	Character Clock Single Shot (character phasing adjustable)
CHST(R)	= CHCK	SH 13	Character Clock Trigger
CHST(S)	= (CHSS)		
CIF1(R)	= (CHRS) CIF1 + MC1	SH 13	Character Index Flip-Flop No. 1
CIF1(S)	= (CIND) CIF1*		
CIF2(R)	= CIF2 (CHCK) + MC1	SH 13	Character Index Flip-Flop No. 2
CIF2(S)	= DSLO + CIF1 (CHCK)		

TABLE 7-2. GLOSSARY OF MNEMONIC TERMS (Contd)

Term	Equation	Logic Diagram	Definition
CIND		SH 13	Character Index
CINDPO		SH 41	Character Index Pickoff
CLK		SH 11	Master Clock
COMP	= CH01 DR01 + CH01* DR01*. CH02 DR02 +CH02* DR02*. CH03 DR03 + CH03* DR03*. CH04 DR04 + CH04* DR04*. CH05 DR05 + CH05* DR05*. CH06 DR06 + CH06* DR06*. CH07 DR07 + CH07* DR07*	SH 14	Compare Data Register to Character Counter
CONT	= MC00* MC01* MC02* MC03	SH 10	Hammer Recovery Control Mode
CONTFF	= LFFF + FFFF + CRFF + VFTA + VFSC	SH 12	Control Flip-Flop
CREN	= DR01 DR02* DR03 DR04 DR05* DR06* DR07* LDCN	SH 6	Carriage Return Enable
CRFF(R)	= CONT (CLK) + MC1	SH 12	Carriage Return Flip-Flop
CRFF(S)	= CREN		
CT143	= CC00 CC02 CC03 CC04 CC05 CC07	SH 17 or SH 18	Top Count 143 (same as HMTC2 on 2470)
DASTRB		SH 5	Received Data Strobe
DATA1 thru DATA 7		SH 5	Received Data Outputs

TABLE 7-2. GLOSSARY OF MNEMONIC TERMS (Contd)

Term	Equation	Logic Diagram	Definition
DCFT		SH 32	DC Voltage Fault
DEM	= MC00 MC01* MC02* MC03*	SH 10	Demand Mode
DEM(A)	= DEM OFL2*	SH 9	Demand Line to Interface
DEM(B)	= DEM(A) CIND-3	SH 54	Demand Line to Interface -3
DGINT		SH 38, 39	Drum Gate Interlock Switch
DIBF(R)	= PRINT CT143 TS08 (CLK) + MC2	SH 11	Data in Buffer Flag
DIBF(S)	= PRINT TS03 PRCH (CLK) OKTOPR +LOAD TS02 CONTFF* (CLK)		
DR01(R) thru DR07(R)	= PRTS1 MEMx* (CLK) + DRCL + DRSS2 (CLK) + DRRS1 (CLK)	SH 6	Data Register Flip-Flops
DR01(S) thru DR07(S)	= DRLD DATAx + PRTS1 MEMx (CLK)		
DRCL	= MC1 + SCEN + IDLE1	SH 10	Data Register Clear
DRLD	= DEM DASTRB + STRB DASTRB	SH 6	Data Register Load
DRRS		SH 46	Data Register Reset
DRRS1	= PRINT PRCH* TS03 + PRINT HDDA TS04	SH 11	Data Register Reset 1
DRRS2	= LOAD TS01 (DRRS + space + PRCH*)	SH 11	Data Register Reset 2

TABLE 7-2. GLOSSARY OF MNEMONIC TERMS (Contd)

Term	Equation	Logic Diagram	Definition
DSFF1(R)	= DSLO* CHRS + (CHCK) 2MS(A) DSFF1	SH 13	Drum Speed Counter No. 1
DSFF1(S)	= DSLO CHRS + (CHCK) 2MS DSFF1*		
DSFF2(R)	= DSFF1 DSFF2 (CHCK) 2MS(A) + CHRS	SH 13	Drum Speed Counter No. 2
DSFF2(S)	= DSFF1 DSFF2* (CHCK) 2MS		
DSFLT(R)	= DSFF1 DSFF2 (CIND)	SH 13	Drum Speed Fault Detection
DSFLT(S)	= MC1 + (DSFF1 DSFF2)* (CIND)		
DSLO		SH 49	Drum Speed Switch (Hi/Lo Speed)
ENCT	= TS08 CONTFF* HDLY*	SH 10	End Control
ENDCYC	= PRINT TS08 HMTC2 DIBF* CLK	SH 10	End of Print Cycle
FFCONT		SH 47	Form Feed Control
FFEN	= DR01* DR02* DR03 DR04 DR05* DR06* DR07* LDCN	SH 6	Form Feed Enable
FFFF(R)	= TC00 CONT (CLK) PASL* + MCRA	SH 12	Form Feed Flip-Flop
FFFF(S)	= FFEN (CLK) + FFSW		
FFSW		SH 40	Top of Form Switch

TABLE 7-2. GLOSSARY OF MNEMONIC TERMS (Contd)

Term	Equation	Logic Diagram	Definition
HCFLT		SH 20	Hammer Current Fault
HDCLR	= CHSN + MC2	SH 19	Hammer Driver Clear
HDDA(R)	= TS05 (CLK) + MC2	SH 13	Hammer Driver Data Flip-Flop
HDDA(S)	= COMP HDDF (CLK)		
HDDF	= TS03 OKTOPR LEGAL PRINT	SH 11	Set Hammer Driver Data Flip-Flop
HDICx		SH 23, 24, 25	Hammer Driver Inter-connect
HDLY	= ENDCYC	SH 12	Hammer Driver Delay (2.25 msec)
HDSST	= OKTOPR PRINT TS04 CLK	SH 9	Hammer Driver Shift Clk
HDSTR	= CHCK ONLN	SH 19	Hammer Driver Strobe
HM01 thru HM136		SH 23, 24, 25	Hammer Driver Outputs
HMINT		SH 28, 32	Hammer Interlock (+20v)
HMPROT		SH 21	Hammer Protect
HMTC	= CC00 CC01 CC03 CC05 CC07	SH 14	Hammer Top Count Count 131
HMTC2	= CC01 CC04 CC05 CC07		Hammer Register Top Count Count 134
HRCY(R)	= PAST	SH 12	Hammer Recovery Single Shot (20 msec)
HRCY(S)	= END CYC		

TABLE 7-2. GLOSSARY OF MNEMONIC TERMS (Contd)

Term	Equation	Logic Diagram	Definition
IDLE1	= MC00* MC01* MC02* MC03*	SH 10	Idle 1 Mode
IDLE 2	= MC00* MC01* MC02 MC03*	SH 10	Idle 2 Mode
LDCN	= LOAD TS01 PARER*	SH 11	Load Control
LEGAL	= DR06 DR07* + DR07 DR06*	SH 6	Legal Character in Data Register
LFEN	= LDCN DR01* DR02 DR03* DR04 DR05* DR06* DR07*	SH 6	Line Feed Enable
LFFF(R)	= PAST* PASL* CONT (CLK) + DIBF* LSF2 CONT (CLK) + MCRA	SH 12	Line Feed Flip-Flop
LFFF(S)	= LFSW* + LFEN (CLK)		
LFSW		SH 9	Paper Step Switch
LNSTPO		SH 41	Line Strobe Pickoff
LOAD	= MC00 MC01 MC02* MC03*	SH 10	Load Mode
LSF1(R)	= LSF2	SH 13	Line Strobe Flip-Flop No. 1
LSF1(S)	= LSF1* (LNSTPO) PFST		
LSF2(R)	= LSF1* (CLK)	SH 13	Line Strobe Flip-Flop No. 2 (synchronized to Clk)
LSF2(S)	= LSF1 (CLK)		
LSF2D	= LSF2 (CLK)	SH 13	Line Strobe Flip-Flop No. 2 Delayed

TABLE 7-2. GLOSSARY OF MNEMONIC TERMS

Term	Equation	Logic Diagram	Definition
MCCK	= CLK ONLN IDLE1 DASTRB* + CLK ONLN DEM DASTRB + CLK ONLN LOAD TS04 + CLK ONLN LOAD TS04 + CLK ONLN IDLE2 + CLK ONLN SCEN BFTC TS08 +CLK ONLN SCAN CHSN RCFF* + CLK ONLN PRINT TS08 HMTC2	SH 10A	Mode Counter Clock
MCLD	= MC2F + LOAD	SH 11	Master Clear or Load
MC00(R)	= MC00 (MCCK) + MC03 + MC1	SH 10	Mode Counter Flip-Flops
MC00(S)	= MC00* (MCCK)		
MC01(R)	= MC01 (MC00) + MC03 + MC1	SH 10	
MC01(S)	= MC01* (MC00)		
MC02(R)	= MC02K (MCCK) + MC03 + MC1	SH 10	
MC02(S)	= OFEN + MC02J (MCCK)		
MC02J	= CONTFF LOAD DIBF + LOAD HMTC1	SH 10	
MC02K	= HMTC2 PRINT ZRTC DIBF*	SH 10	(Buffer Full option only)

TABLE 7-2. GLOSSARY OF MNEMONIC TERMS (Contd)

Term	Equation	Logic Diagram	Definition
MC03(R)	= ENCT (CLK) + CONTFF* MC2F CLK + MC1	SH 10	
MC03(S)	= MC03J (CLK)		
MC03J	= CENF + LOAD CONTFF DIBF* TS04 + ZRTC PRINT HMTC2 DIBF* TS08	SH 10	
MC1F(R)	= VOMN* MCSW* (CLK) HMPROT*	SH 9	Master Clear Flip-Flop No. 1
MC1F(S)	= VOMN + MCSW (CLK) + HMPROT (CLK)		
MC2F(R)	= MC1F* DGINT* DSFLT* PFLTM* (CLK) ONLN*	SH 9	Master Clear Flip-Flop No. 2
MC2F(S)	= MC1F + DGINT (CLK) + DSFLT (CLK)		
MCRA	= MC1 + RAFF	SH 12	Master Clear on Runaway
MCSW		SH 40	Master Clear Switch
MEM1 thru MEM7		SH 7, 8	Memory Outputs
MOTION		SH 55	Paper Motion Sensor Output
OFEN	= OFL1 OFL2 CHCK	SH 9	Off-Line Enable
OFL1(R)	= RUN* CHCK OFL1 + ONLN* + DASTRB + RCFF + MC2	SH 9	Off-Line Flip-Flop No. 1

TABLE 7-2. GLOSSARY OF MNEMONIC TERMS (Contd)

Term	Equation	Logic Diagram	Definition
OFL1(S)	= RUN* CHCK OFL1*		
OFL2(R)	= OFL1 CHCK + ONLN* + DASTRB + RCFF + MC2	SH 9	Off-Line Flip-Flop No. 2
OFL2(S)	= OFL1 CHCK		
OKTOPR	= TRUE = CC04* CC05* CC06* Zone 1 + CC04 CC05* CC06* Zone 1 + CC04* CC05 CC06* Zone 1 + CC04 CC05 CC06* Zone 2 + CC04* CC05* CC06 Zone 2 + CC04 CC05* CC06 Zone 2 = CC04* CC05* CC06* Zone 1 + CC04 CC05* CC06* Zone 2 + CC04* CC05 CC06* Zone 3 + CC04 CC05 CC06* Zone 4 + CC04* CC05* CC06 Zone 5 + CC04 CC05* CC06 Zone 6	SH 15, 16	Okay to Print (2470) Okay to print (2440) Okay to print (2420)
ONLN(R)	= ENCT CONT RUN* (CLK) + ENCT CONT PFLTM PINHLT* (CLK) + MC2	SH 9	On-Line Flip-Flop
ONLN(S)	= MC2F* RUN (CLK)		
ONLNLT	= ONLN PINHLT*	SH 9	On-Line Light

TABLE 7-2. GLOSSARY OF MNEMONIC TERMS (Contd)

Term	Equation	Logic Diagram	Definition
ONLNSW		SH 40	On-Line Switch
PASL(R)	= LSF2 FFFF TC00 (CLK) + TARS (CLK) + SCRS (CLK) + MCRA	SH 12	Paper Advance Slew
PASL(S)	= CONT FFFF TC00* (CLK) + TASK (CLK) + SCSL (CLK)		
PAST(R)	= CONT* LSF2 VFCE* (CLK) + MCRA	SH 12	Paper Advance Step
PAST(S)	= CONT LFFF SLTC00* (CLK) + CONT FFFF 12 CHANNEL (CLK) + SCST (CLK) + TAST (CLK)		
PEFF		SH 46	Parity Error Flip-Flop
PENTRA		SH 19	Penetration Control A
PENTRB		SH 19	Penetration Control B
PENTRW		SH 19	Penetration Control W
PFLTM	= RAFF + POFLT + BTSW. ONLN . ONLNSW*	SH 12	Paper Fault Modified
PFOT		SH 30	Paper Feed Over-temperature
PFSL	= PASL PFDL*	SH 12	Paper Feed Slew Command

TABLE 7-2. GLOSSARY OF MNEMONIC TERMS (Contd)

Term	Equation	Logic Diagram	Definition
PFST	= PAST PFDL*	SH 12	Paper Feed Step Command
PHADJA		SH 14	Phase Adjust Potentio-meter
PINHLT		SH 9	Print Inhibit Light
PINST	= RECPI	SH 5	Paper Instruction
PLINT		SH 39	Plenum Chamber Inter-lock
POFLT	= TOP PAPER SWITCH + TAPE READER OPEN	SH 38, 39	Paper Out Fault
POFLT(A)	= MOTION* + PLINT* + PAST*	SH 54	Paper Out Fault
POLT	= PFLTM PINHLT*	SH 9	Paper Out Light
PRCH(R)	= TS04 (CLK) + MC2	SH 11	Printable Character Flip-Flop
PRCH(S)	= STRB LEGAL (CLK) + LEGAL PRINT TS02 (CLK)		
PRDLY		SH 12	Printer Delay
PRESET	= CHRS		(preset to 40)
PRINH	= PINHLT + MC2F	SH 9	Print Inhibit
PRINT	= MC00 MC01 MC02 MC03*	SH 10	Print Mode
PRTS1	= TS01 PRINT	SH 11	Print Time Slot 1
PSSW		SH 39	Paper Step Switch
PSTD		SH 21	Power Supply Time Delay

TABLE 7-2. GLOSSARY OF MNEMONIC TERMS (Contd)

Term	Equation	Logic Diagram	Definition
RCDL	= PAST ENDCYC ZRTC	SH 12	Recovery Delay Single Shot (2.5 to 9 milli-seconds adjustable)
RCFF(R)	= (RCDL) RCFF + MCRA	SH 12	Recover Delay Flip-Flop
RCFF(S)	= PAST + ZRTC ENDCYC		
RDY	= MC2F*	SH 9	Printer Ready
RDYLT	= PINHLT* RDY	SH 9	Ready Light
RECDATA		SH 5	Receiver Data Strobe Input
REC1 thru REC8		SH 5	Receiver Data Inputs
RECPAR		SH 5	Receiver Parity Input
RECREF		SH 5	Receiver Reference
RUN(R)	= ONLNSW RUN + MC2	SH 9	On-Line Switch Latch
RUN(S)	= ONLNSW RUN*		
SCAN	= MC00* MC01 MC02 MC03*	SH 10	Scan Mode
SCEN	= MC00 MC01* MC02 MC03*	SH 10	Scan Enable Mode
SCRS	= VFSC VFUR 1*	SH 27	Step Count Reset
SCSL	= CONT VFSC VFUR 1	SH 27	Step Count Slew
SCST	= CONT VFSC VFUR=0*	SH 27	Step Count Step
SDIBF		SH 27	

TABLE 7-2. GLOSSARY OF MNEMONIC TERMS (Contd)

Term	Equation	Logic Diagram	Definition
SLFF*	= CONT PRINTED* VFU1* VFU2* VFU3* TN00 + CONT PRINTED* VFU1 VFU2* VFU3* TN01 + CONT PRINTED* VFU1* VFU2 VFU3* TN02 + CONT PRINTED* VFU1* VFU2 VFU3* TN03 + CONT PRINTED* VFU1* VFU2* VFU3 TN04	SH 47	Selected Flip-Flop
SLTC	= VFUR1* VFUR2* VFUR3* TC00 + VFUR1 VFUR2* VFUR3* TC01 + VFUR1* VFUR2 VFUR3* TC02 + VFUR1 VFUR2 VFUR3* TC03 + VFUR1* VFUR2* VFUR3 TC04 + VFUR1 VFUR2* VFUR3 TC05 + VFUR1* VFUR2 VFUR3 TC06 + VFUR1 VFUR2 VFUR3 TC07	SH 27	Selected Tape Channel
SPACE	= DR01* DR02* DR03* DR04* DR05* DR06 DR07*	SH 6	Space Decode
STRB	= MC00* MC01 MC02* MC03*	SH 10A	Strobe Mode
SWTF		SH 40	Top-Of-Form Switch
TARS	= SLTC LSF2 VFTA	SH 27	Tape Advance Reset

TABLE 7-2. GLOSSARY OF MNEMONIC TERMS (Contd)

Term	Equation	Logic Diagram	Definition
TASL	= CONT VFTA SLTC* SLFF*	SH 27	Tape Advance Slew
TAST	= CONT VFTA SLFF*	SH 27	Tape Advance Step
TC00 thru TC07		SH 27	Tape Channel
TF01(R)	= IDLE1* DEM* STRB* TF01 (CLK) + MC2	SH 11	Timing Flip-Flops
TF01(S)	= IDLE1* DEM* STRB* TF01* (CLK)		
TF02(R)	= TF01 TF02 (CLK) +MC2		
TF02(S)	= TF01 TF02* (CLK)		
TF03(R)	= TF01 TF02 TF03 (CLK)		
TF03(S)	= TF01 TF02 TF03*(CLK)		
TN00	= TC00* LSF2D* (CLK) LFS2 (CLK)	SH 47	Tape Channel Now
TS01	= TF01* TF02* TF03*	SH 11	Time Slot 1
TS02	= TF01 TF02* TF03*	SH 11	Time Slot 2
TS03	= TF01* TF02 TF03*	SH 11	Time Slot 3
TS04	= TF01 TF02 TF03*	SH 11	Time Slot 4
TS05	= TF01* TF02* TF03	SH 11	Time Slot 5
TS06	= TF01 TF02* TF03	SH 11	Time Slot 6
TS07	= TF01* TF02 TF03	SH 11	Time Slot 7
TS08	= TF01 TF02 TF03	SH 11	Time Slot 8

TABLE 7-2. GLOSSARY OF MNEMONIC TERMS (Contd)

Term	Equation	Logic Diagram	Definition
TW01*	= TC01* LSF2D* (CLK) + TC01* LSF2 (CLK)	SH 47	Tape Channel will-be 1
TW02*	= TC02* LSF2D* (CLK) + TC02* LSF2 (CLK)	SH 47	Tape Channel will-be 2
TW03*	= TC03* LSF2D* (CLK) + TC03* LSF2 (CLK)	SH 47	Tape Channel will-be 3
TW04*	= TC04* LSF2D* (CLK)	SH 47	Tape Channel will-be 4
TW05*	= TC05* LSF2D* (CLK) + TC05* LSF2 (CLK)	SH 47	Tape Channel will-be 5
TW06*	= TC06* LSF2D* (CLK) + TC06* LSF2 (CLK)	SH 47	Tape Channel will-be 6
TW07*	= TC07* LSF2D* (CLK) + TC07* LSF2 (CLK)	SH 47	Tape Channel will-be 7
TW11*	= TC11* LSF2D* (CLK) + TC11* LSF2 (CLK)	SH 47	Tape Channel will-be 8
VCL		SH 19	Voltage Clamp
VFCE(R)	= LSF2 (CLK) + VFUR=0 (CLK) + MCRA	SH 27	Vertical Format Count Enable Flip-Flop
VFCE(S)	= PAST DIBF* DR05 STRB PEFF* VFIF (CLK)		
VFIF(R)	= LOAD (CLK + MCRA	SH 27	Vertical Format Input Flip-Flop
VFIF(S)	= PINST DRLD		
VFSC(R)	= CONT VFUR 1* (CLK) + MCRA	SH 27	Vertical Format Step Count Flip-Flop
VFSC(S)	= VFIF STRB PEFF* DR05 (CLK)		

TABLE 7-2. GLOSSARY OF MNEMONIC TERMS (Contd)

Term	Equation	Logic Diagram	Definition
VFTA(R)	= CONT SLTC PFSL* (CLK) + MCRA	SH 27	Vertical Format Tape Flip-Flop
VFTA(S)	= VFIF STRB PEFF* DR05* (CLK)		
VFU1 thru VFU4		SH 27	Vertical Format Unit Register
VFUx (Clock)	= VFSC LSF2 CONT VFCE* CLK		
VFUx (Load)	= STRB PEFF* VFIF		
VFUx (Clear)	= MCRA		
VFUR 1	= VFUR2 + VFUR3 + VFUR4	SH 27	Vertical Format Unit Register greater than one
VFUR=0	= VFUR1* VFUR2* VFUR3* VFUR4*	SH 27	Vertical Format Unit Register equals zero
VFZS	= VFIF*	SH 27	Vertical Format Zone Select
VOMN		SH 19	Voltage Monitor
XDEM	= DEM(A)	SH 5	Transmitted Demand Line
XONLN	= XONLN(A)	SH 5	Transmitted On-Line
XPEFF	= PEFF	SH 5	Transmitted Parity Error
XRDY	= RDY	SH 5	Transmitted Ready
ZAVN	= LOAD TS04 CONTFF*	SH 14	Zone Advance

TABLE 7-2. GLOSSARY OF MNEMONIC TERMS (Contd)

Term	Equation	Logic Diagram	Definition
ZCH1	= PAST + ENDCYC ZRTC	SH 12	Zone Change 1
ZRTC	= True	SH 17, 18	Zone Register Top Count (2470)
	= ZR00 ZR01 ZR02 ZR03 +MC1		(2440)
	= MC1 + ENDCYC ZRTC* (CLK)		(2420)
ZSEL 1 thru ZSEL 6		SH 17, 18	Zone Select (Zone SR1 6)
ZS1G thru ZS6G		SH 17, 18	Zone Select Gate
ZS1K thru ZS6K		SH 17, 18	Zone Select Cathode
2MS(A)		SH 13	

MODEL 2420-CIRCUIT CARD AND ASSEMBLY LOCATOR

ELECTRONICS GATE ASSEMBLY A3

CARD CAGE A

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26
P1 - HAMMER BANK HARNESS (SH 23A)	AS-46 (SH 20)	AH-22 (SH 23)	AH-22 (SH 23)	AH-22 (SH 23)	AH-22 (SH 23)	AH-22 (SH 23)	AZ-116 (SH 19)	CODE CONVERSION (SH 53/OPTION)	AG-36 (SH 15)	AH-24 (SH 17)	P12 - MAIN HARNESS (SHS 38 & 38A)	AZ-115 (SH 9)	AS-26 (SH 13)	AC-17 (SH 12)	AZ-164: 12 CHAN VFU (SH 47/OPTION)	AG-44 (SH 27)	AL-11: PARITY (SH 46/OPTION)	P19 - I/O HARNESS (SH 5)	AL-25 (SH 5)	AC-16 (SH 14) OR AC-19 /AC-20 (SH 51/OPTION)	AM-26 (SH 7)	AM-26 (SH 8)	AG-33 (SH 6)	AG-34 (SHS 10 & 10A)	AT-24 (SH 11)

POWER SUPPLY ASSEMBLY A5

A5 (SH 28)

A8	A7	A6	A5	A4	A3	A2	A1
AZ-49 (SH 28)	AZ-49 (SH 28)	AZ-49 (SH 28)	AZ-51 (SH 28)	AZ-49 (SH 28)	AZ-15 (SH 31)	AV-10 (SH 30)	AP-16 (SH 29)

LOGIC DIAGRAM SHEET 1

MODEL 2420
CIRCUIT CARD
AND ASSEMBLY LOCATOR

MODEL 2440-CIRCUIT CARD AND ASSEMBLY LOCATOR

ELECTRONICS GATE ASSEMBLY A3

CARD CAGE B

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26
P1 - HAMMER BANK HARNESS (SH 24B)	BLANK	AH-22 (SH 24A)	AH-22 (SH 24A)	AH-22 (SH 24A)	AH-22 (SH 24A)	AH-22 (SH 24A)	AH-22 (SH 24A)	AH-22 (SH 24A)	AH-22 (SH 24A)	AH-22 (SH 24A)	AH-22 (SH 24A)	BLANK	←	←	←	←	←	←	←	←	←	←	←	BLANK	AG-55 (SH 54)

CARD CAGE A

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26
P1 - HAMMER BANK HARNESS (SH 24B)	BLANK	AH-22 (SH 24)	AH-22 (SH 24)	AH-22 (SH 24)	AH-22 (SH 24)	AH-22 (SH 24)	AZ-116 (SH 19)	CODE CONVERSION (SH 53/OPTION)	AG-37 (SH 16)	AH-25 (SH 18)	P12 - MAIN HARNESS (SHS 39, 39A & 39B)	AZ-115 (SH 9)	AS-26 (SH 13)	AC-17 (SH 12)	AZ0164: 12 CHAN VFU (SH 47/OPTION)	AG-44 (SH 27)	AL-11: PARITY (SH 46/OPTION)	P19 - I/O HARNESS (SH 5)	AL-25 (SH 5)	AC-16 (SH 14) OR AC-19 /AC-20 (SH 51/OPTION)	AM-26 (SH 7)	AM-26 (SH 8)	AG-33 (SH 6)	AG-34 (SHS 10 & 10A)	AT-24 (SH 11)

REGULATED POWER SUPPLY ASSEMBLY A5

A5 (SH 32)

A1	A2	A3	A4	A5
AV-17 (SH 32)	AZ-113 (SH 32)	AZ-111 (SH 32)	AZ-111 (SH 32)	AZ-126 (SH 32)

*SEE SCHEMATIC IN SECTION VIII

PAPER FEED CONTROL ASSEMBLY A6

A6 (SH 33)

A1	A2	A3	A4	A5	A6
AP-15 (SH 34)	AV-21 (SH 33)	AP-34 (SH 35A)	AP-34 (SH 35A)	AP-33 (SH 35)	AP-33 (SH 35)

HAMMER BANK POWER SUPPLY ASSEMBLY A8

A8 (SH 36)

*	A1	A2
AV-18 (SH 36A)*	AS-40 (SH 21)	AP-17 (SH 37)

*BOLTED TO CHASSIS, SEE SECTION VIII(TABLE I) FOR SCHEMATIC

LOGIC DIAGRAM SHEET 1A

MODEL 2440
CIRCUIT CARD
AND ASSEMBLY LOCATOR

MODEL 2470-CIRCUIT CARD AND ASSEMBLY LOCATOR

ELECTRONICS GATE ASSEMBLY A3

CARD CAGE B

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26
P1 - HAMMER BANK HARNESS (SH 25D)	P2 - HAMMER BANK HARNESS (SH 25D)	AH-22 (SH 25A)	AH-22 (SH 25A)	AH-22 (SH 25A)	AH-22 (SH 25A)	AH-22 (SH 25A)	AH-22 (SH 25A)	AH-22 (SH 25A)	AH-22 (SH 25A)	AH-22 (SH 25A)	AH-22 (SH 25A)	AH-22 (SH 25B)	AH-22 (SH 25B)	AH-22 (SH 25B)	AH-22 (SH 25B)	AH-22 (SH 25B)	AH-22 (SH 25B)	AH-22 (SH 25B)	AH-22 (SH 25B)	AH-22 (SH 25B)	AH-22 (SH 25B)	AH-22 (SH 25C)	AH-22 (SH 25C)	AH-22 (SH 25C)	AG-55 (SH 54)

CARD CAGE A

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26
P1 - HAMMER BANK HARNESS (SH 25D)	BLANK	AH-22 (SH 25)	AH-22 (SH 25)	AH-22 (SH 25)	AH-22 (SH 25)	AH-22 (SH 25)	AZ-116 (SH 19)	CODE CONVERSION (SH 53/OPTION)	BLANK	BLANK	P12 - MAIN HARNESS (SHS 39, 39A & 39B)	AZ-115 (SH 9)	AS-26 (SH 13)	AC-17 (SH 12)	AZ-164: 12 CHAN VFU (SH 47/OPTION)	AG-44 (SH 27)	AL-11; PARITY (SH 46/OPTION)	P19 - I/O HARNESS (SH 5)	AL-25 (SH 5)	AC-16 (SH 14) OR AC-19 /AC-20 (SH 51/OPTION)	AM-26 (SH 7)	AM-26 (SH 8)	AG-33 (SH 6)	AG-34 (SHS 10 & 10A)	AT-24 (SH 11)

NOT USED (BLANK) IN 120 COL PRINTERS

NOT USED (BLANK) IN 132 COL. PRINTERS

REGULATED POWER SUPPLY ASSEMBLY A5

A5 (SH 32)

A1	A2	A3	A4	A5
AV-17 (SH 32)	AZ-113 (SH 32)	AZ-111 (SH 32)	AZ-111 (SH 32)	AZ-126 (SH 32)

PAPER FEED CONTROL ASSEMBLY A6

A6 (SH 33)

A1	A2	A3	A4	A5	A6
AP-15 (SH 34)	AV-21 (SH 33)	AP-34 (SH 35A)	AP-34 (SH 35A)	AP-33 (SH 35)	AP-33 (SH 35)

HAMMER BANK POWER SUPPLY ASSEMBLY A8

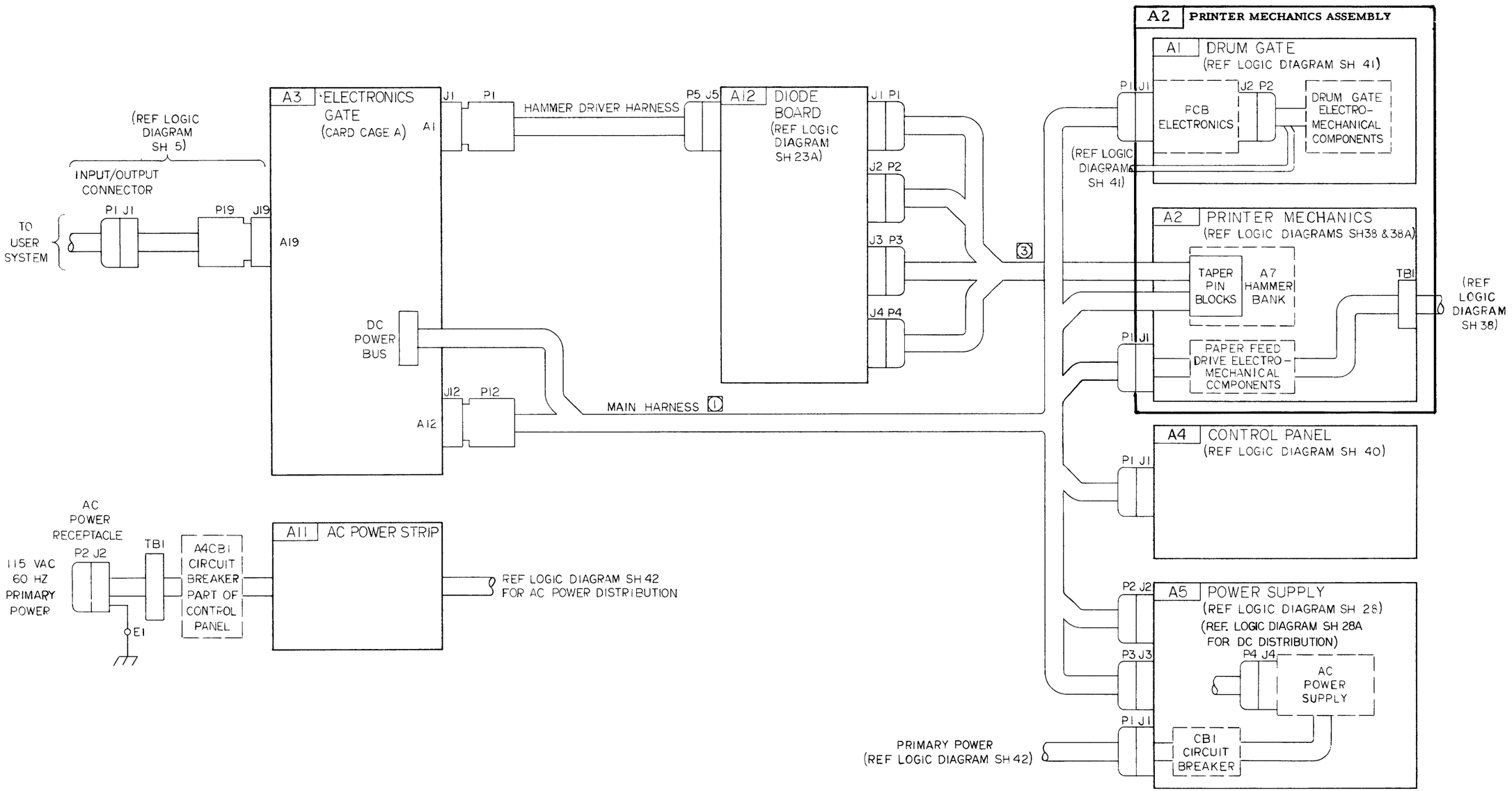
A8 (SH 36A)

*	A1	A2
AV-18 (SH 36A)*	AS-40 (SH 21)	AP-17 (SH 37)

*BOLTED TO CHASSIS, SEE SECTION VIII(TABLE I) FOR SCHEMATIC

LOGIC DIAGRAM SHEET 1B

MODEL 2470
CIRCUIT CARD
AND ASSEMBLY LOCATOR



(3) REFER TO LOGIC DIAGRAM SHEET 26.

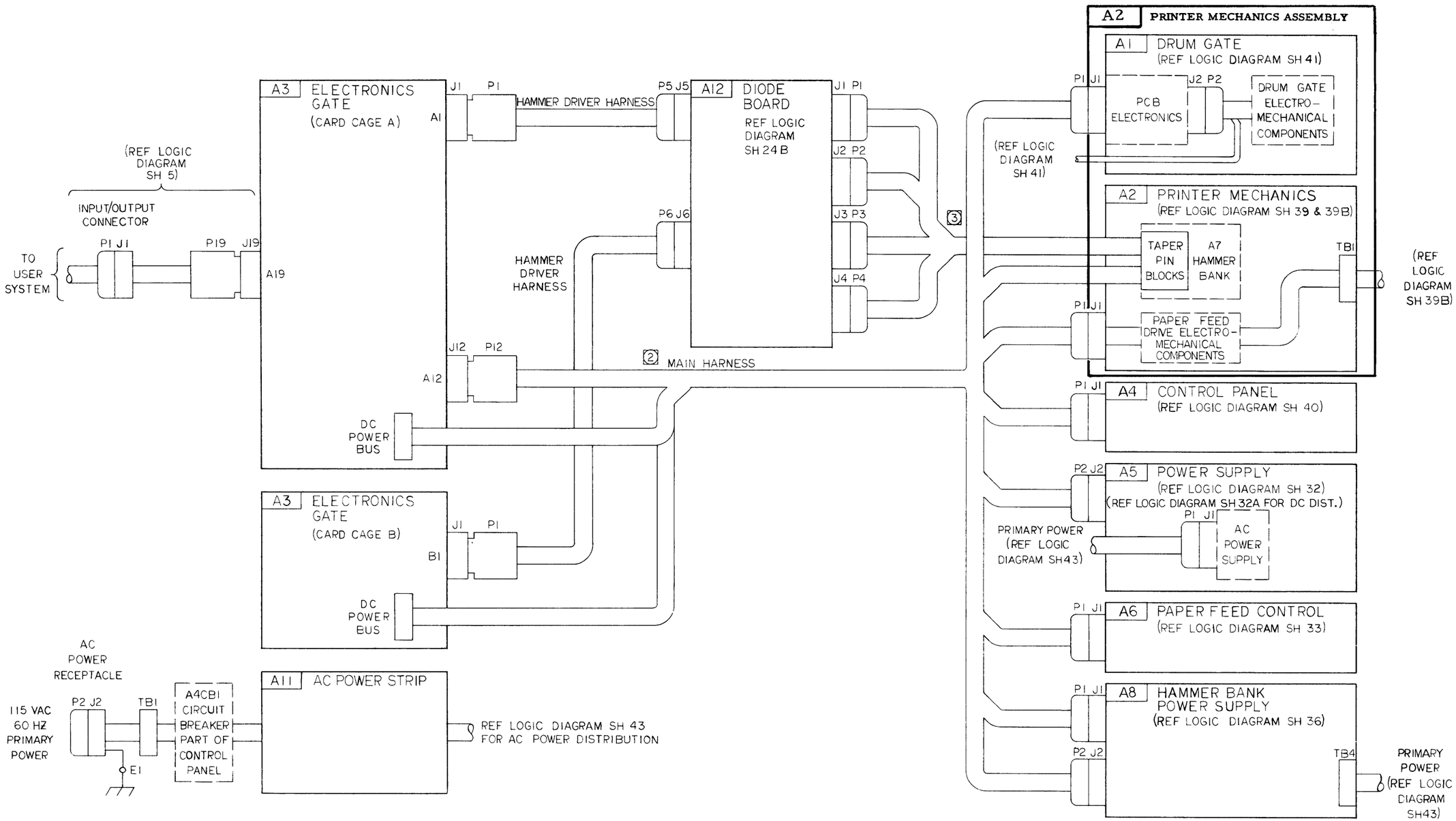
(2) REFER TO LOGIC DIAGRAM SHEETS 39, 39A & 39B FOR DETAILED INTERCONNECTION DATA.

(1) REFER TO LOGIC DIAGRAM SHEETS 38 & 38A FOR DETAILED INTERCONNECTION DATA.

NOTES: UNLESS OTHERWISE SPECIFIED

LOGIC DIAGRAM SHEET 2

INTERCONNECTION DIAGRAM (MODEL 2420) MAJOR ASSEMBLIES



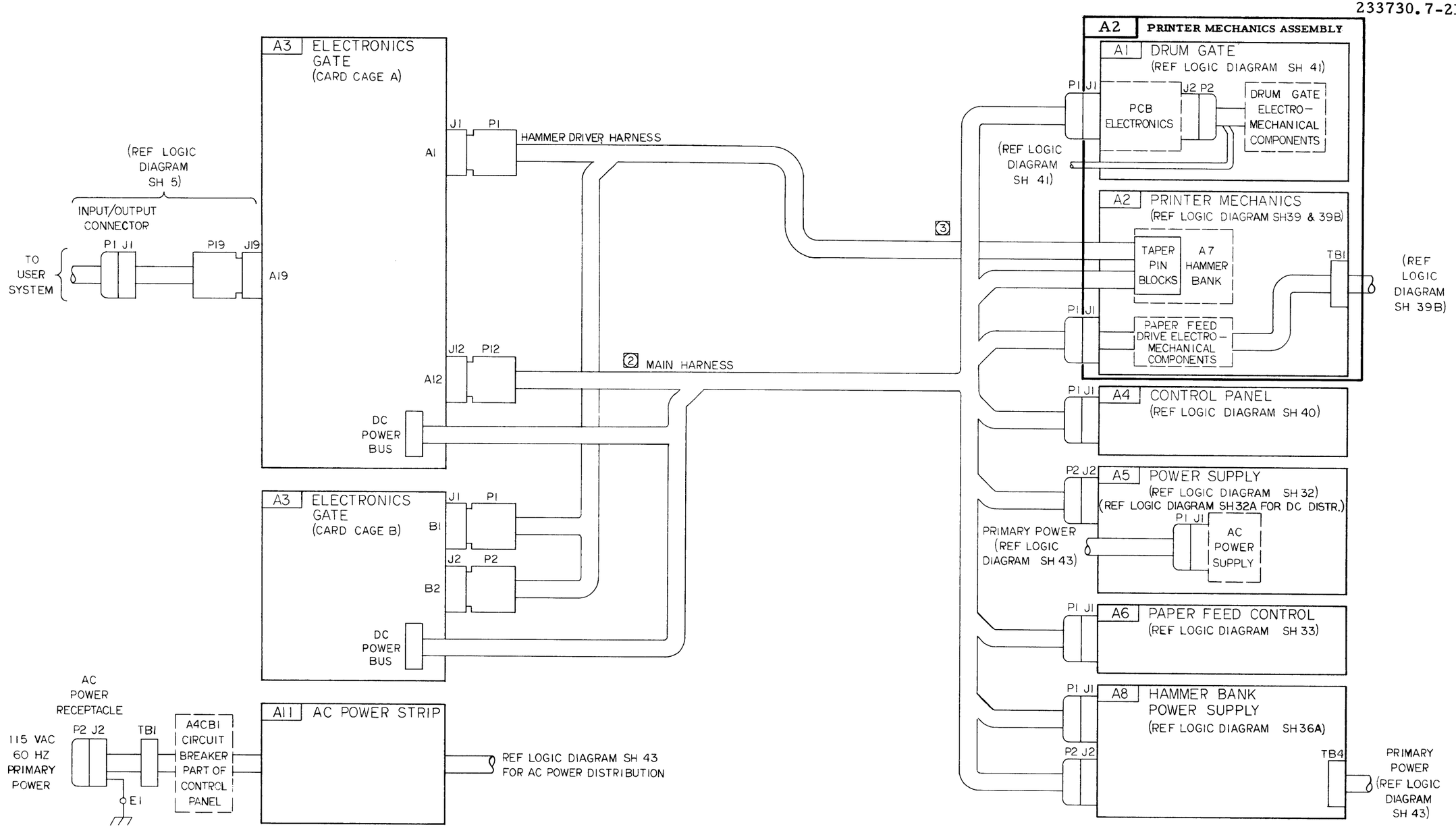
3 REFER TO LOGIC DIAGRAM SHEET 26.

2 REFER TO LOGIC DIAGRAM SHEETS 39, 39A & 39B FOR DETAILED INTERCONNECTION DATA.

NOTES: UNLESS OTHERWISE SPECIFIED

LOGIC DIAGRAM SHEET 2A

INTERCONNECTION DIAGRAM (MODEL 2440) MAJOR ASSEMBLIES



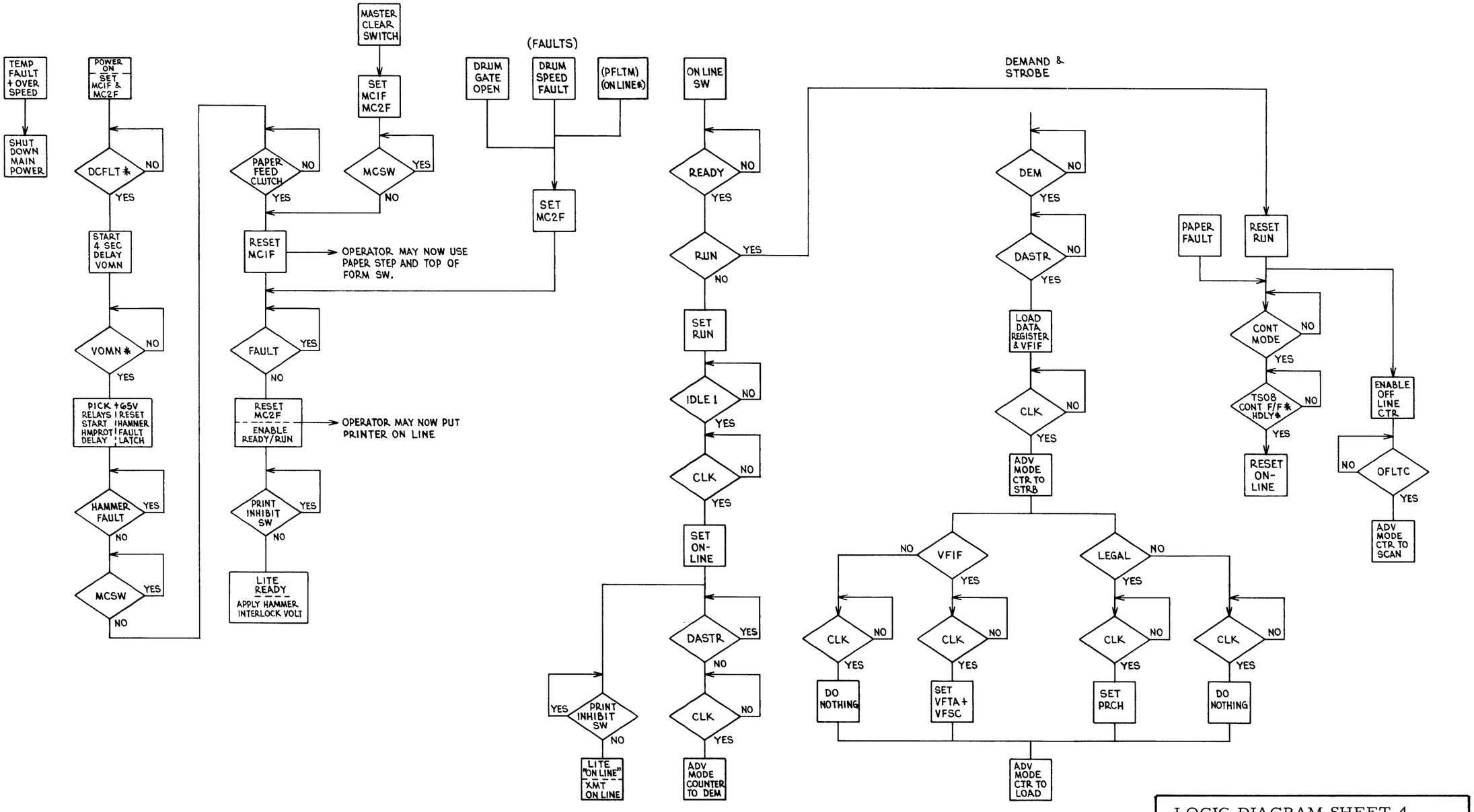
3 REFER TO LOGIC DIAGRAM SHEET 26.

2 REFER TO LOGIC DIAGRAM SHEETS 39, 39A & 39B FOR DETAILED INTERCONNECTION DATA.

NOTES: UNLESS OTHERWISE SPECIFIED

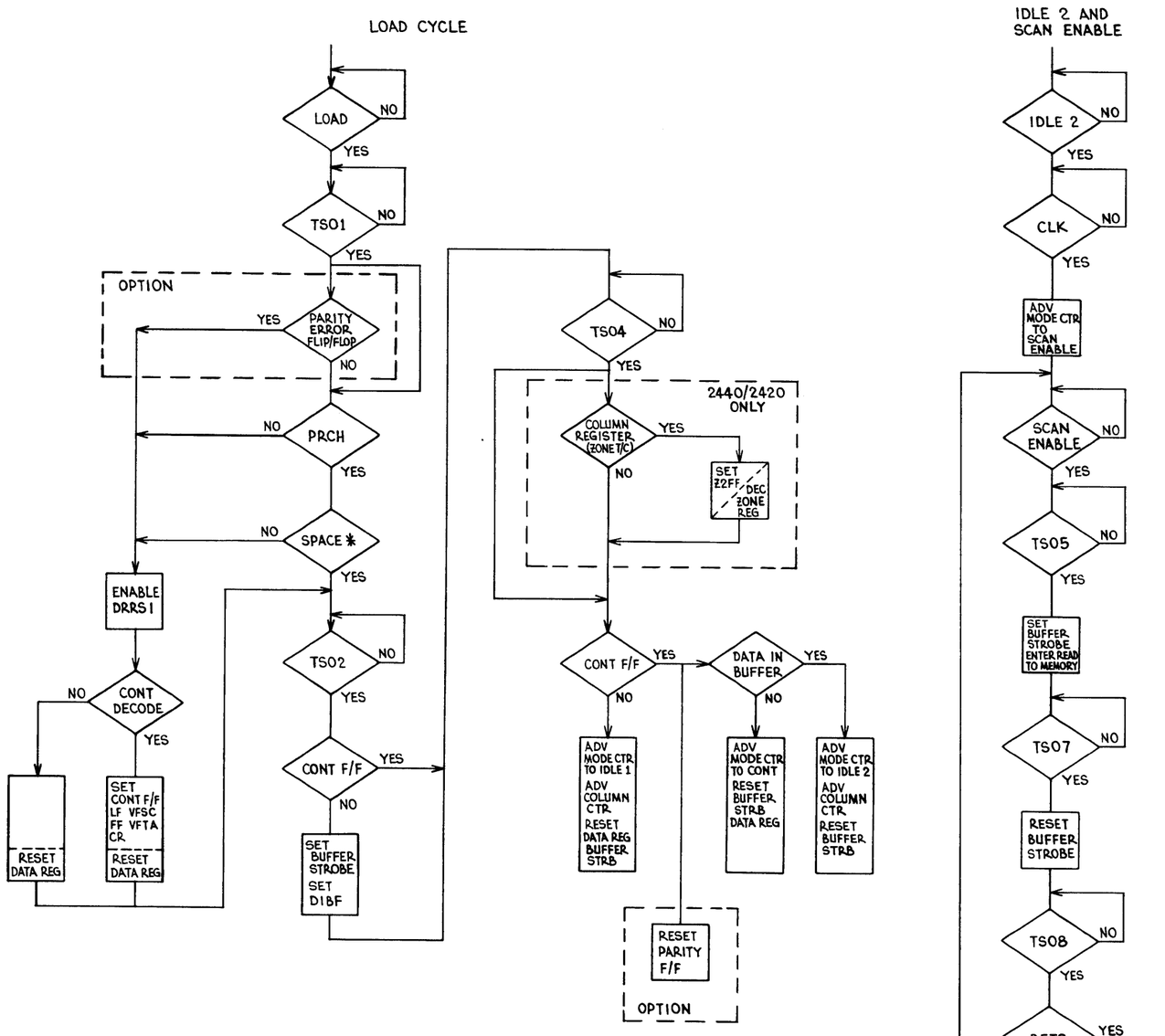
LOGIC DIAGRAM SHEET 2B

INTERCONNECTION DIAGRAM
(MODEL 2470)
MAJOR ASSEMBLIES



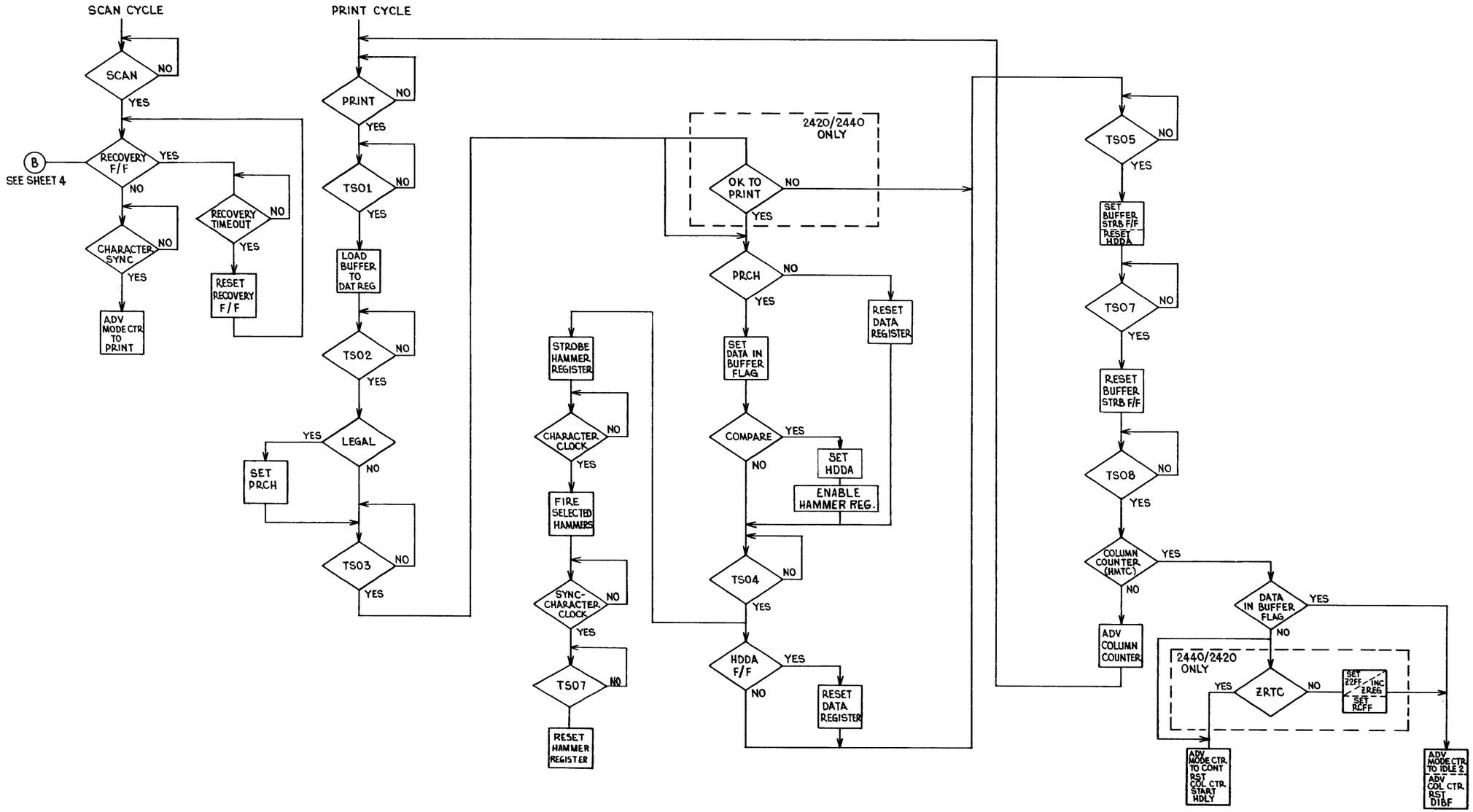
LOGIC DIAGRAM SHEET 4

SYSTEM FLOW CHART
Power On , Interlocks,
Faults, Demand & Strobe



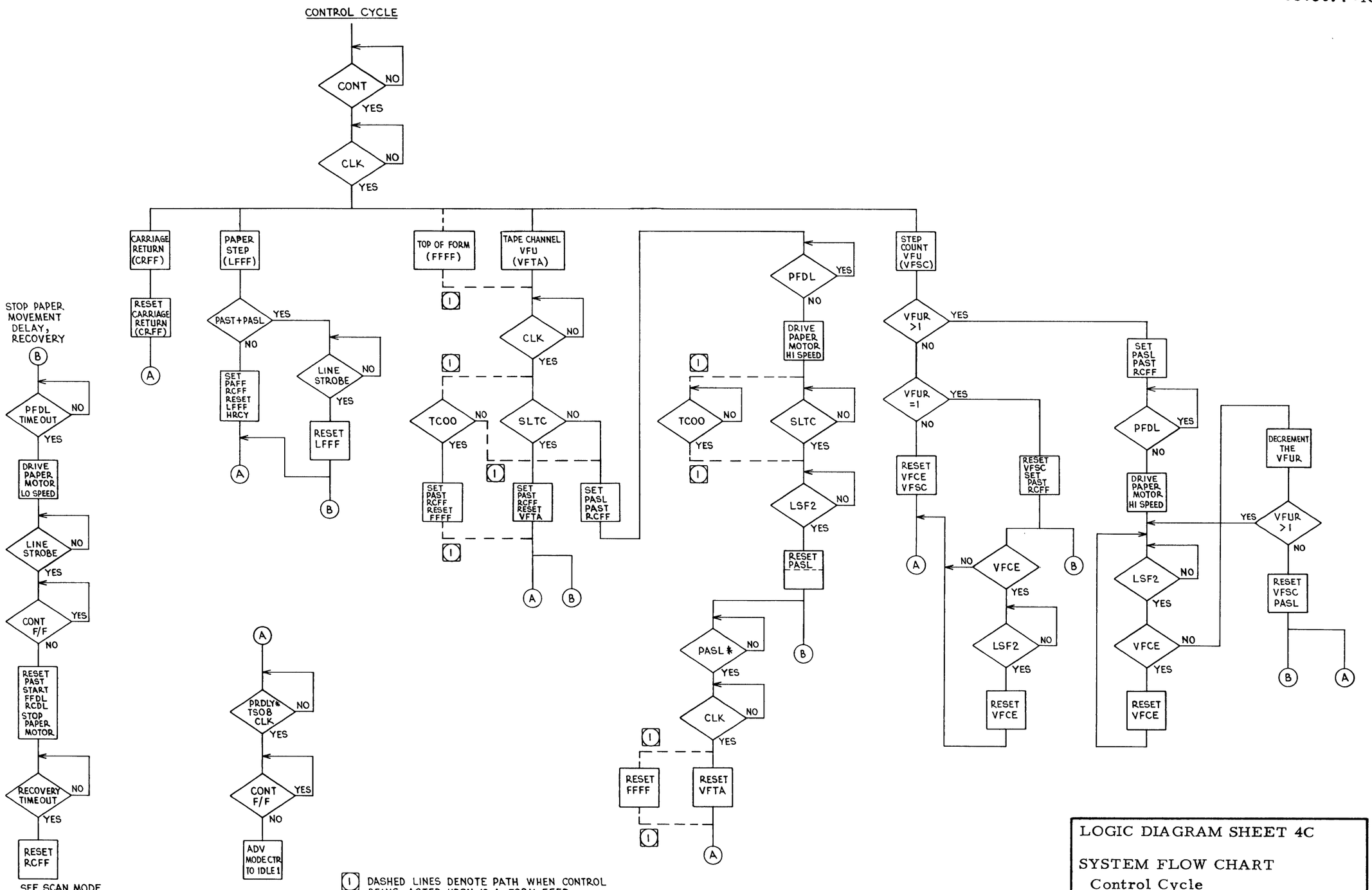
LOGIC DIAGRAM SHEET 4A

SYSTEM FLOW CHART
Load Cycle, Idle 2 & Scan Enable



LOGIC DIAGRAM SHEET 4B

SYSTEM FLOW CHART
Print Cycle, Scan Cycle

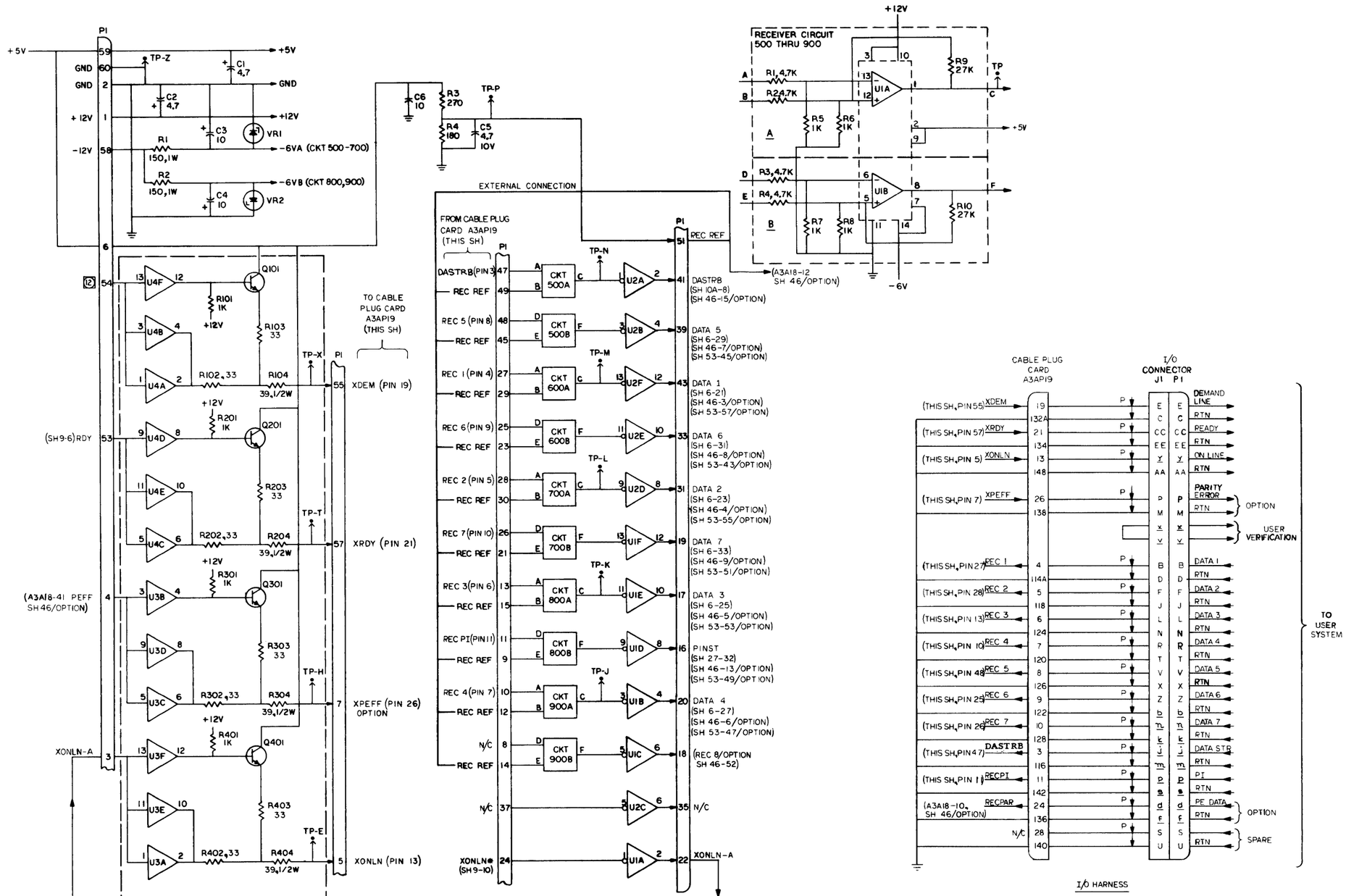


I DASHED LINES DENOTE PATH WHEN CONTROL BEING ACTED UPON IS A FORM FEED.

NOTES:

LOGIC DIAGRAM SHEET 4C

SYSTEM FLOW CHART
Control Cycle



9. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION PREFIX WITH CIRCUIT NO.
8. THE FOLLOWING CONNECTOR PINS ARE NOT USED: 24, 32, 34, 36, 37, 38, 40, 42, 44, 46, 50, 52, 56.
7. ASSEMBLY DRAWING NUMBER 218490, REV L
6. INTERPRET ELECTRONIC SYMBOLS PER USAS Y32.2.
5. INTERPRET REFERENCE DESIGNATIONS PER USAS Y32.16.
4. ALL TRANSISTORS ARE 800132-001.
3. ALL DIODES ARE 800592-001.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS, 10%, 20 VOLTS.
1. ALL RESISTANCE VALUES ARE IN OHMS, 5%, 1/4 WATT.

NOTES: UNLESS OTHERWISE SPECIFIED

11. INTEGRATED CIRCUITS ARE AS FOLLOWS:

REFERENCE DESIGNATIONS	PART NO. AL-25
U1, U2	800387-001
U3, U4	800806-001
U500A, B THRU U900A, B	800805-001

FOR COMPLETE IC PIN ASSIGNMENTS SEE LOADING DIAGRAMS IN APPENDIX A

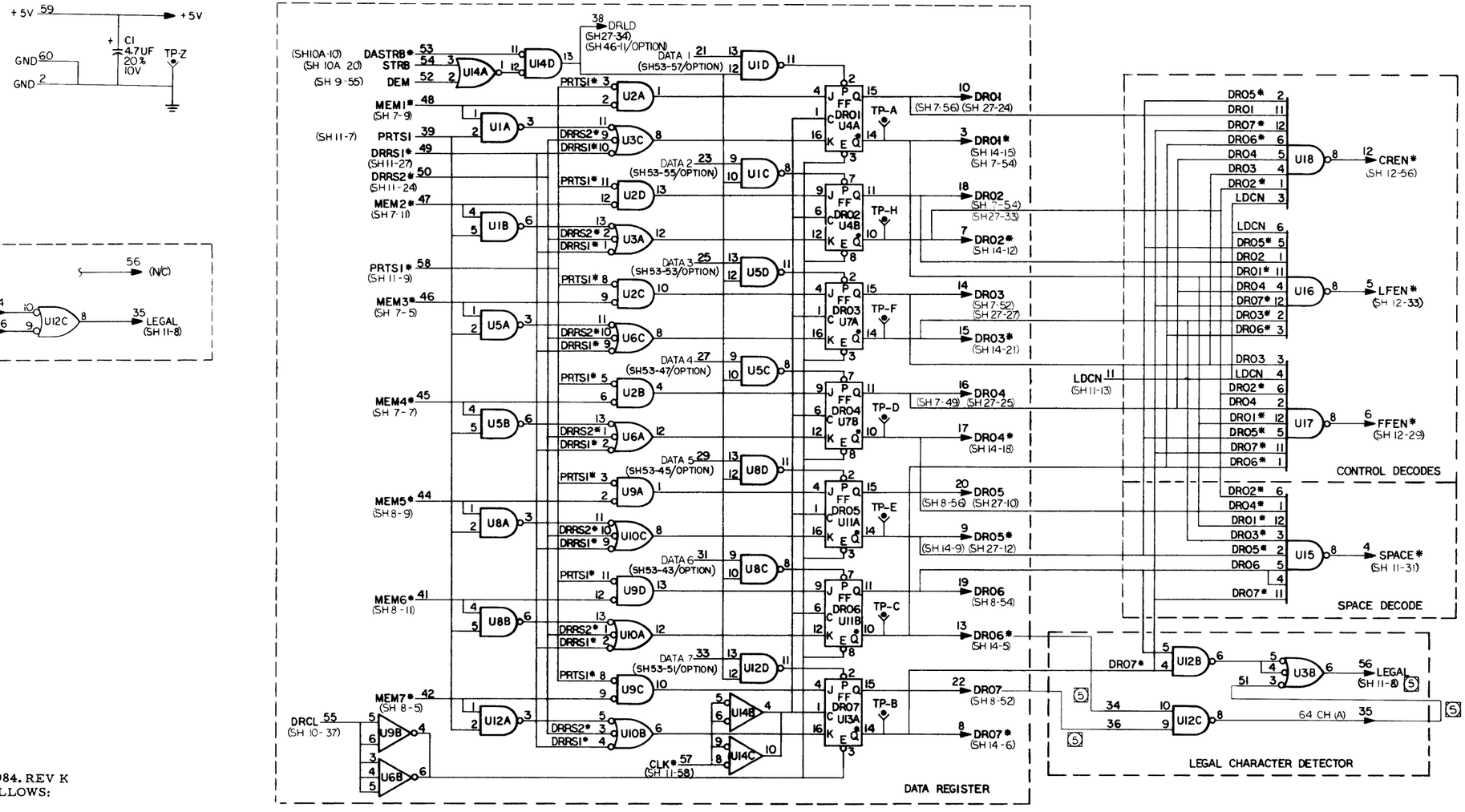
10. FOR SCHEMATIC SEE DWG NO. 218494.

CIRCUIT CARD LOCATION: A3A20 & A3AP19 (ALL MODELS, ELECTRONICS GATE ASSEMBLY A3, CARD CAGE A, SLOTS 20 & 19)

(12) MODEL 2420: SH9-13 DEM(A) OR SH53-15 OPTION.
MODELS 2440/2470: SH5A-31 DEM(B).

LOGIC DIAGRAM SHEET 5

AL-25
RECEIVER & POSITIVE DRIVER & I/O HARNESS



8. FOR SCHEMATIC SEE DWG NO. 217984. REV K
7. INTEGRATED CIRCUITS ARE AS FOLLOWS:

REFERENCE DESIGNATION	PART NO. AG-33
U1, U5, U8, U12	800024-001
U2, U9, U14	800080-001
U3, U6, U10	800023-001
U4, U7, U11, U13	800081-001
U15, U16, U17, U18	800021-001

FOR COMPLETE IC PIN ASSIGNMENTS
SEE LOADING DIAGRAMS IN APPENDIX A

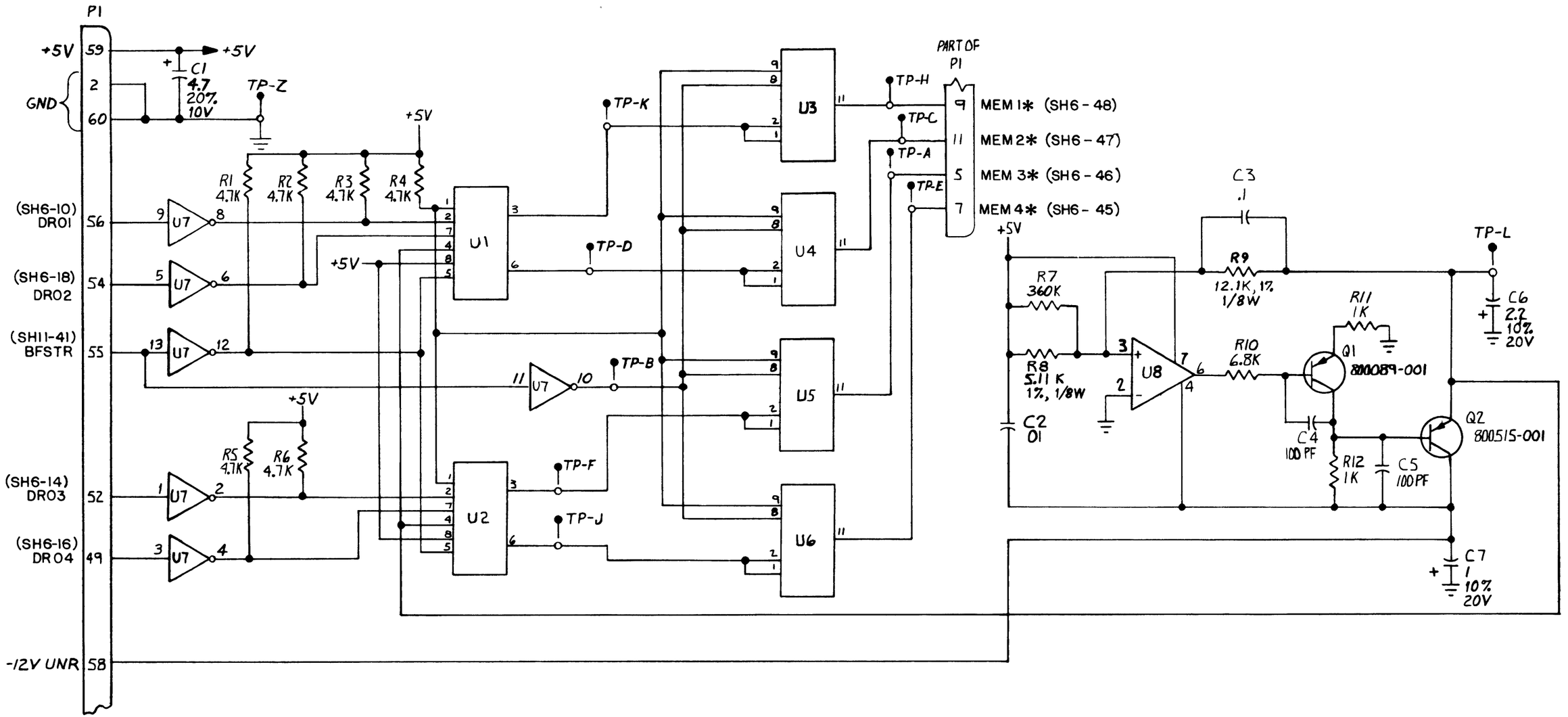
6 CONNECTIONS FOR 96 CHARACTER OPTION.
5 EXTERNAL CONNECTIONS FOR STANDARD 64 CHARACTER.
4. THE FOLLOWING CONNECTOR PINS ARE NOT USED: 1, 24, 26, 28, 30, 32, 37, 40, 43.
3. ASSEMBLY DRAWING NUMBER 217980, REV H
2. INTERPRET ELECTRONIC SYMBOLS PER 850026.
1. INTERPRET REFERENCE DESIGNATIONS PER 850027.

NOTES: UNLESS OTHERWISE SPECIFIED

CIRCUIT CARD LOCATION: A3A24
(ALL MODELS, ELECTRONICS GATE ASSEMBLY A3, CARD CAGE A, SLOT 24)

LOGIC DIAGRAM SHEET 6

AG-33
DATA REGISTER



7. FOR SCHEMATIC SEE DWG NO. 237214, REV D
6. INTEGRATED CIRCUITS ARE: U1, U2: 800940-001; U3 THRU U6: 800698-001; U7: 800387-001; U8: 800732-001.

   FOR COMPLETE IC PIN ASSIGNMENTS SEE LOADING DIAGRAMS IN APPENDIX A

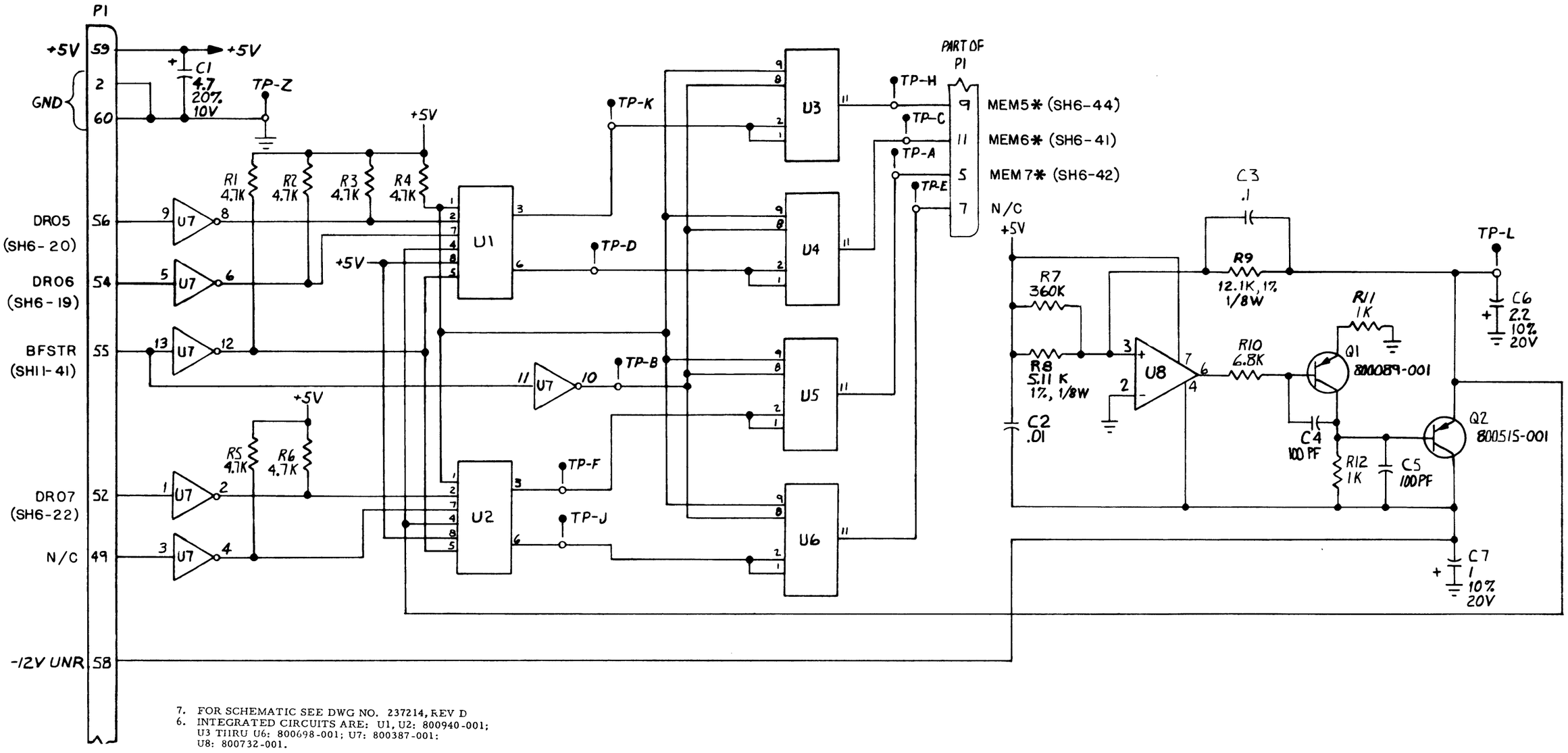
5. ASSEMBLY DRAWING NUMBER 237210-001, REV D
4. INTERPRET ELECTRONIC SYMBOLS PER 850026.
3. INTERPRET REFERENCE DESIGNATIONS PER 850027.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS, 15%, 100 VOLTS.
1. ALL RESISTANCE VALUES ARE IN OHMS, 5%, 1/4 WATT.

NOTES: UNLESS OTHERWISE SPECIFIED

CIRCUIT CARD LOCATION: A3A22
(ALL MODELS, ELECTRONICS GATE ASSEMBLY A3, CARD CAGE A, SLOT 22)

LOGIC DIAGRAM SHEET 7

AM-26
150 X 4 BIT MEMORY



7. FOR SCHEMATIC SEE DWG NO. 237214, REV D
6. INTEGRATED CIRCUITS ARE: U1, U2: 800940-001; U3 THRU U6: 800698-001; U7: 800387-001; U8: 800732-001.

   FOR COMPLETE IC PIN ASSIGNMENTS SEE LOADING DIAGRAMS IN APPENDIX A

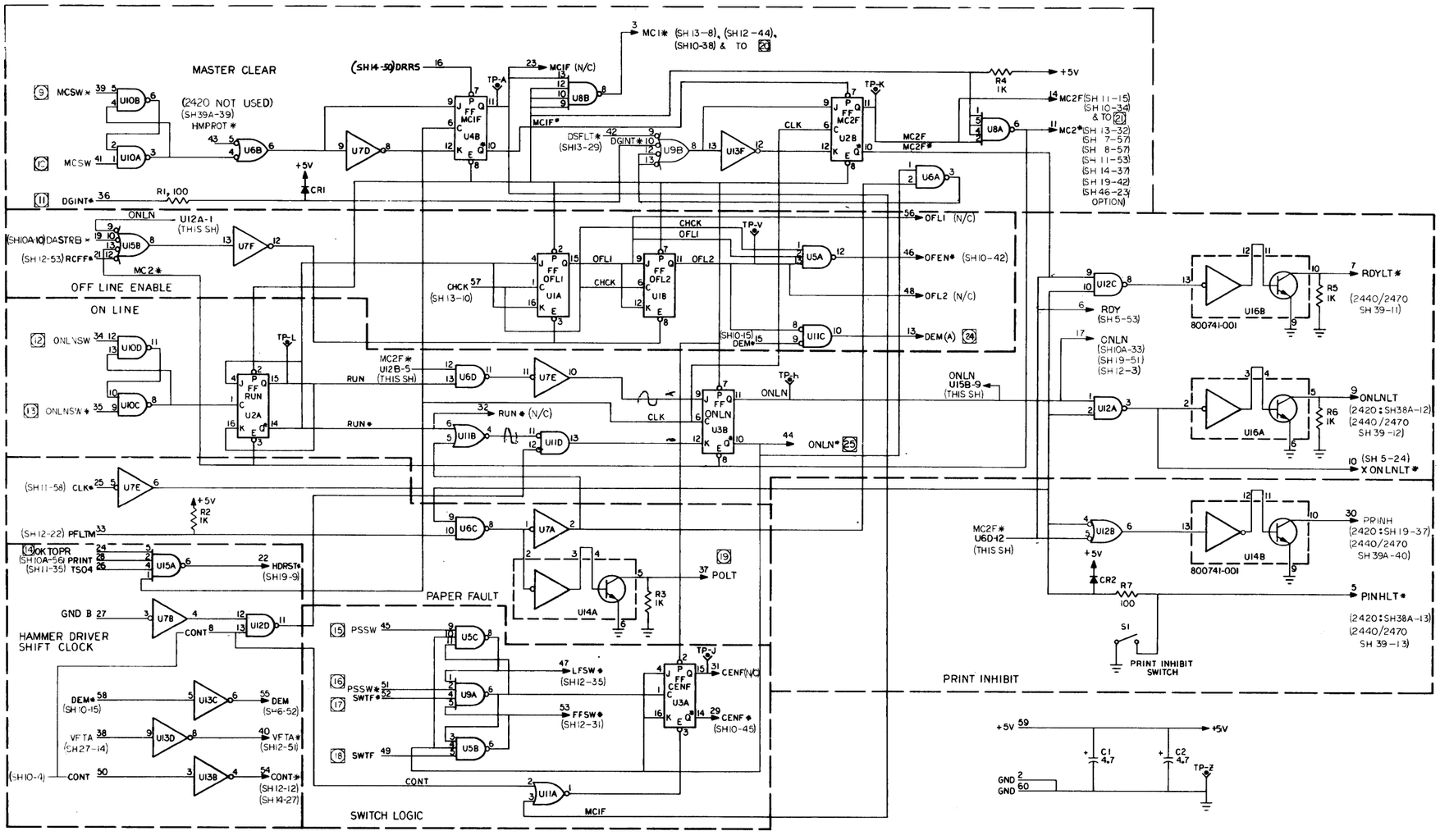
5. ASSEMBLY DRAWING NUMBER 237210-001, REV D
4. INTERPRET ELECTRONIC SYMBOLS PER 850026.
3. INTERPRET REFERENCE DESIGNATIONS PER 850027.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS, 15%, 100 VOLTS.
1. ALL RESISTANCE VALUES ARE IN OHMS, 5%, 1/4 WATT.

NOTES: UNLESS OTHERWISE SPECIFIED

CIRCUIT CARD LOCATION: A3A23
(ALL MODELS, ELECTRONICS GATE ASSEMBLY A3, CARD CAGE A, SLOT 23)

LOGIC DIAGRAM SHEET 8

AM-26
150 X 4 BIT MEMORY



21 MODEL 2420: SH15-48
MODEL 2440: SH16-48
MODEL 2470: NOT USED

20 MODEL 2420: SH15-3, -31
MODEL 2440: SH16-5, -31, -36
MODEL 2470: NOT USED

19 MODEL 2420: SH38A-14
MODELS 2440/2470: SH39-14

18 MODEL 2420: SH38A-30
MODELS 2440/2470: SH39-30

17 MODEL 2420: SH38A-29
MODELS 2440/2470: SH39-29

16 MODEL 2420: SH38A-38
MODELS 2440/2470: SH39-38

15 MODEL 2420: SH38A-28
MODELS 2440/2470: SH39-28

14 MODEL 2420: SH15-41
MODEL 2440: SH16-41
MODEL 2470: NOT USED

13 MODEL 2420: SH38A-5
MODELS 2440/2470: SH39-5

12 MODEL 2420: SH38A-4
MODELS 2440/2470: SH39-4

11 MODEL 2420: SH38A-10
MODELS 2440/2470: SH39

10 MODEL 2420: SH38A-6
MODELS 2440/2470: SH39-6

9 MODEL 2420: SH38A-3
MODELS 2440/2470: SH39-3

8. THE FOLLOWING CONNECTOR PINS ARE NOT USED: 1, 9, 12, 18, & 20.
7. ASSEMBLY DRAWING NUMBER 218025, REV C
6. INTERPRET ELECTRONIC SYMBOLS PER 850026.
5. INTERPRET REFERENCE DESIGNATIONS PER 850027.
4.
3. ALL DIODES ARE 800093-001.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS, ±20%, 10 VOLTS.
1. ALL RESISTANCE VALUES ARE IN OHMS, ±5%, 1/4 WATT.

NOTES: UNLESS OTHERWISE SPECIFIED

25 W12 CHANNEL VFU OPTION (SH47-11).

24 MODEL 2420: SH5-54
MODEL 2440/2470: SH54-28

23. FOR SCHEMATIC SEE DWG NO. 218029, REV S
22. INTEGRATED CIRCUITS ARE AS FOLLOWS:

REFERENCE DESIGNATIONS	PART NO. AZ-115
U1, U2, U3, U4	800081-001
U5	800023-001
U6, U10, U12	800024-001
U7, U13	800387-001
U8, U9, U15	800022-001
U11	800080-001
U14, U15	800741-001

FOR COMPLETE IC PIN ASSIGNMENTS SEE LOADING DIAGRAMS IN APPENDIX A

CIRCUIT CARD LOCATION: A3A13
(ALL MODELS, ELECTRONICS GATE A3, CARD CAGE A, SLOT 13)

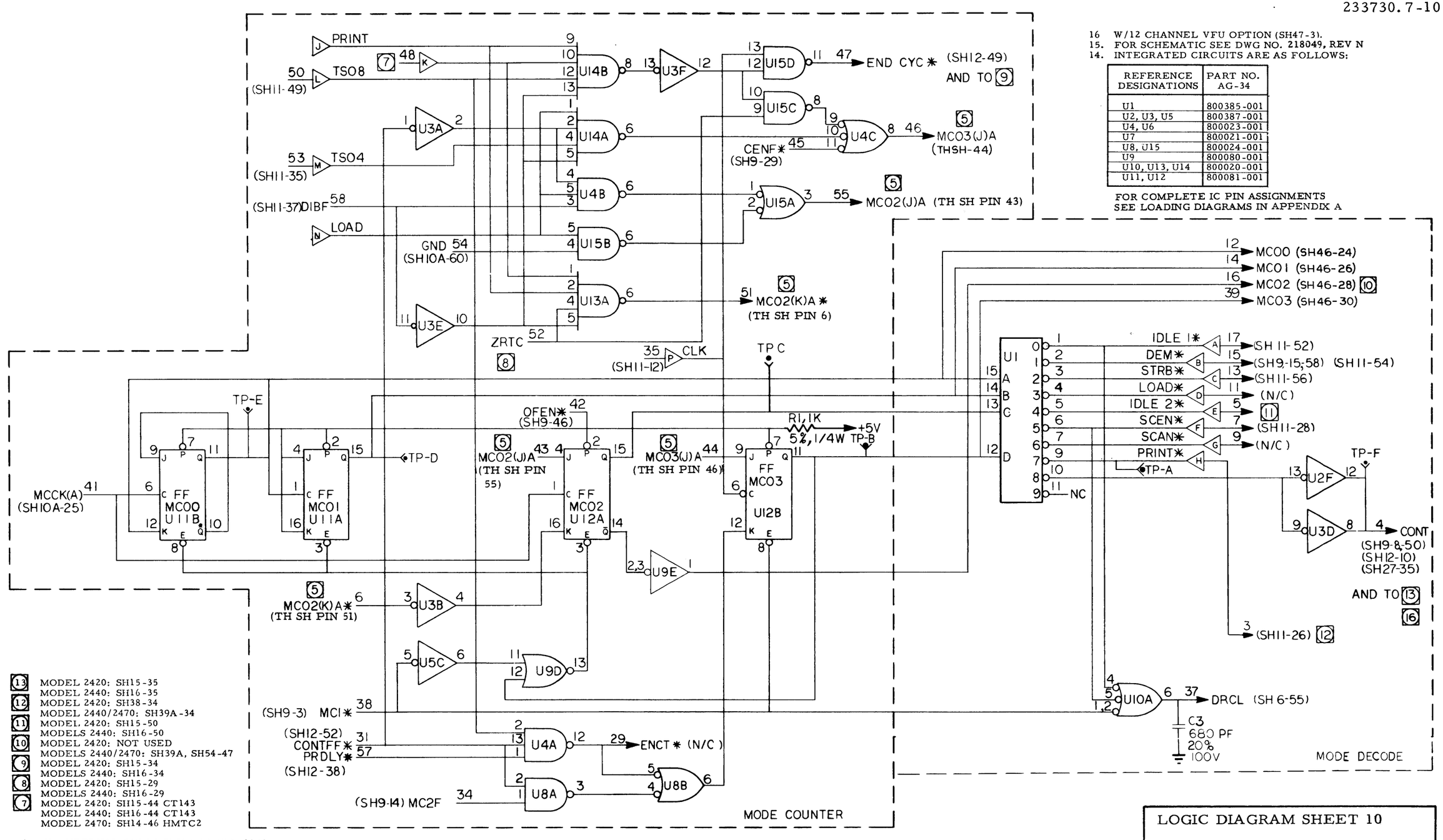
LOGIC DIAGRAM SHEET 9

AZ-115
MASTER CLEAR SWITCH

16 W/12 CHANNEL VFU OPTION (SH47-3).
15. FOR SCHEMATIC SEE DWG NO. 218049, REV N
14. INTEGRATED CIRCUITS ARE AS FOLLOWS:

REFERENCE DESIGNATIONS	PART NO. AG-34
U1	800385-001
U2, U3, U5	800387-001
U4, U6	800023-001
U7	800021-001
U8, U15	800024-001
U9	800080-001
U10, U13, U14	800020-001
U11, U12	800081-001

FOR COMPLETE IC PIN ASSIGNMENTS SEE LOADING DIAGRAMS IN APPENDIX A



13 MODEL 2420: SH15-35
MODEL 2440: SH16-35
12 MODEL 2420: SH38-34
MODEL 2440/2470: SH39A-34
11 MODEL 2420: SH15-50
MODELS 2440: SH16-50
10 MODEL 2420: NOT USED
MODELS 2440/2470: SH39A, SH54-47
9 MODEL 2420: SH15-34
MODELS 2440: SH16-34
8 MODEL 2420: SH15-29
MODELS 2440: SH16-29
7 MODEL 2420: SH15-44 CT143
MODEL 2440: SH16-44 CT143
MODEL 2470: SH14-46 HMTC2

6. X INTERNAL CONNECTION (REF SH10A).

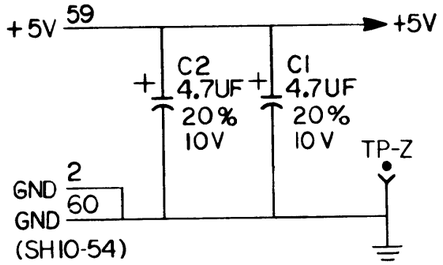
5 EXTERNAL CONNECTION
4. THE FOLLOWING CONNECTOR PINS ARE NOT USED: 1, 30, & 32.
3. ASSEMBLY DRAWING NUMBER 218045, REV F
2. INTERPRET ELECTRONIC SYMBOLS PER USAS Y32.2.
1. INTERPRET REFERENCE DESIGNATIONS PER USAS Y32.16.

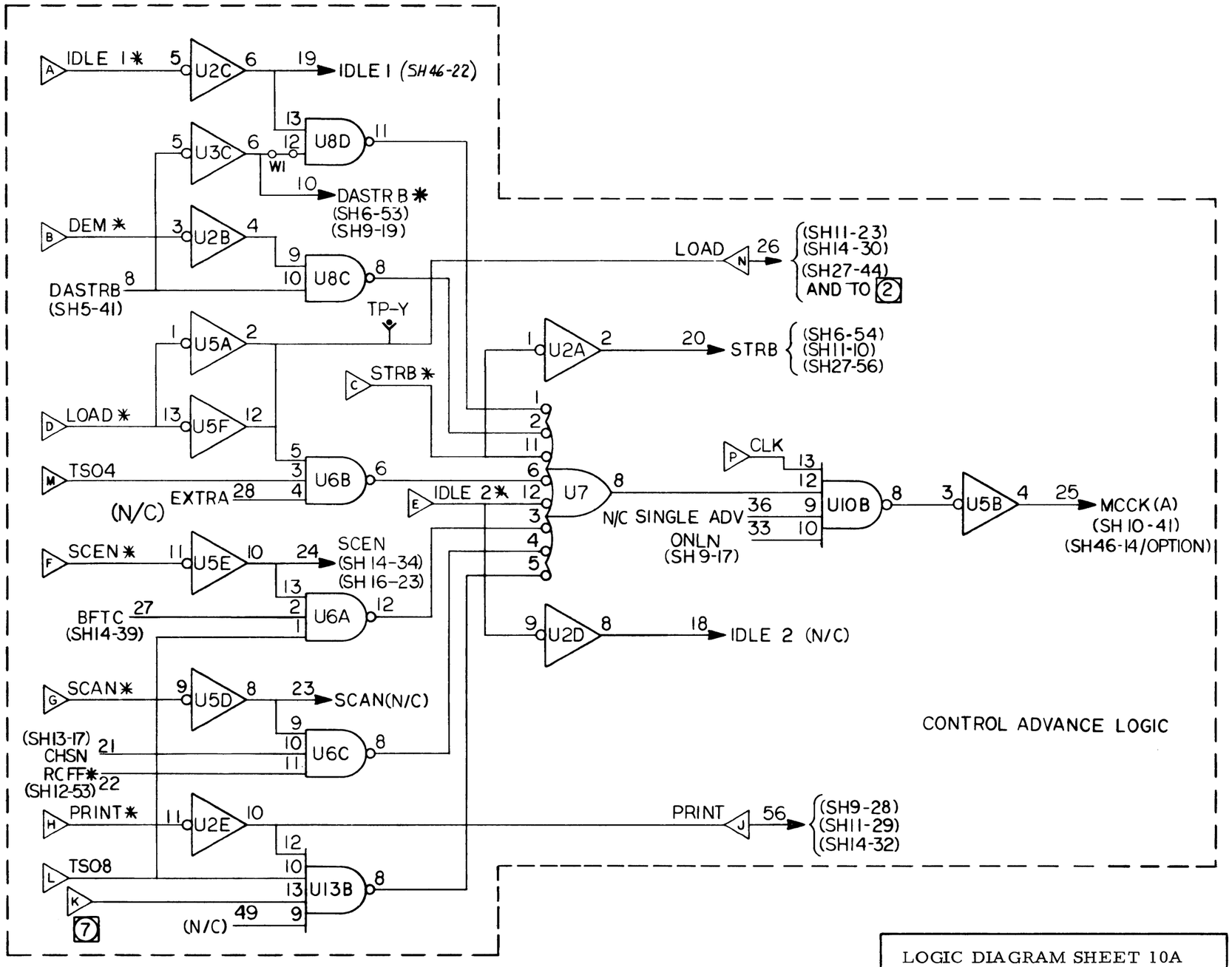
NOTES: UNLESS OTHERWISE SPECIFIED

CIRCUIT CARD LOCATION: A3A25
(ALL MODELS, ELECTRONICS GATE ASSEMBLY A3, CARD CAGE A, SLOT 25)

LOGIC DIAGRAM SHEET 10

AG-34
MODE LOGIC

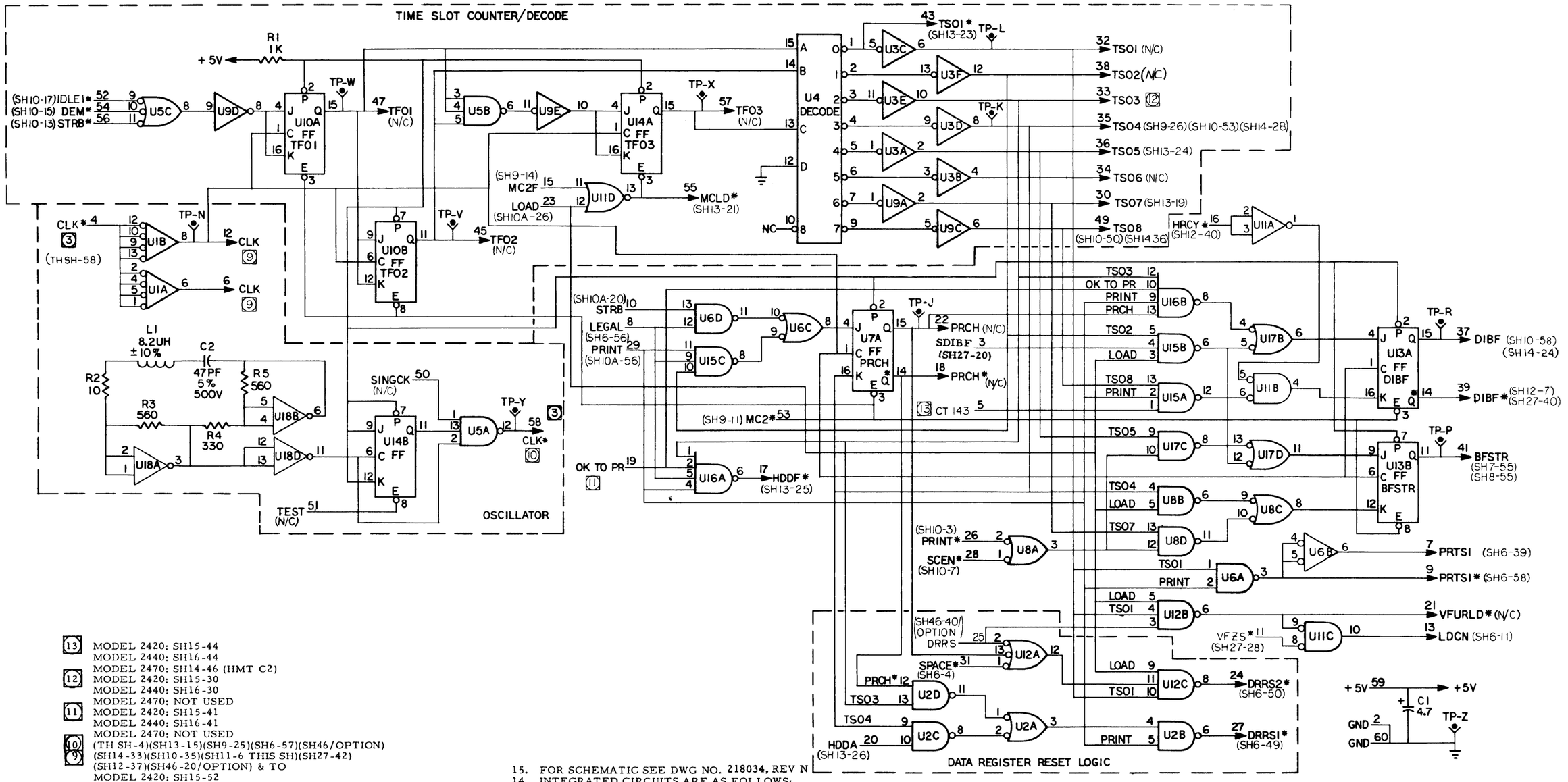




LOGIC DIAGRAM SHEET 10A

AG-34
MODE LOGIC

CIRCUIT CARD LOCATION: A3A25
(ALL MODELS, ELECTRONICS GATE ASSEMBLY A3, CARD CAGE A, SLOT 25)



(13) MODEL 2420: SH15-44
MODEL 2440: SH16-44
MODEL 2470: SH14-46 (HMT C2)

(12) MODEL 2420: SH15-30
MODEL 2440: SH16-30
MODEL 2470: NOT USED

(11) MODEL 2420: SH15-41
MODEL 2440: SH16-41
MODEL 2470: NOT USED

(10) (9) (TH SH-4)(SH13-15)(SH9-25)(SH6-57)(SH46/OPTION)
(SH14-33)(SH10-35)(SH11-6 THIS SH)(SH27-42)
(SH12-37)(SH46-20/OPTION) & TO
MODEL 2420: SH15-52
MODEL 2440: SH16-52
MODEL 2470: NOT USED
W/12 CHANNEL VFU OPTION (SH47-12)

8. THE FOLLOWING CONNECTOR PINS ARE NOT USED: 1, 4, 14, 16, 40, 42, 44, 46, 48, 50, 58
7. ASSEMBLY DRAWING NUMBER 218030, REV F
6. INTERPRET ELECTRONIC SYMBOLS PER 850026.
5. INTERPRET REFERENCE DESIGNATIONS PER 850027.
4. U18-C IS A SPARE GATE (DO NOT USE).
3 EXTERNAL CONNECTION.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS, 20%, 10 VOLTS.
1. ALL RESISTANCE VALUES ARE IN OHMS, 5%, 1/4WATT.

NOTES: UNLESS OTHERWISE SPECIFIED

15. FOR SCHEMATIC SEE DWG NO. 218034, REV N
14. INTEGRATED CIRCUITS ARE AS FOLLOWS:

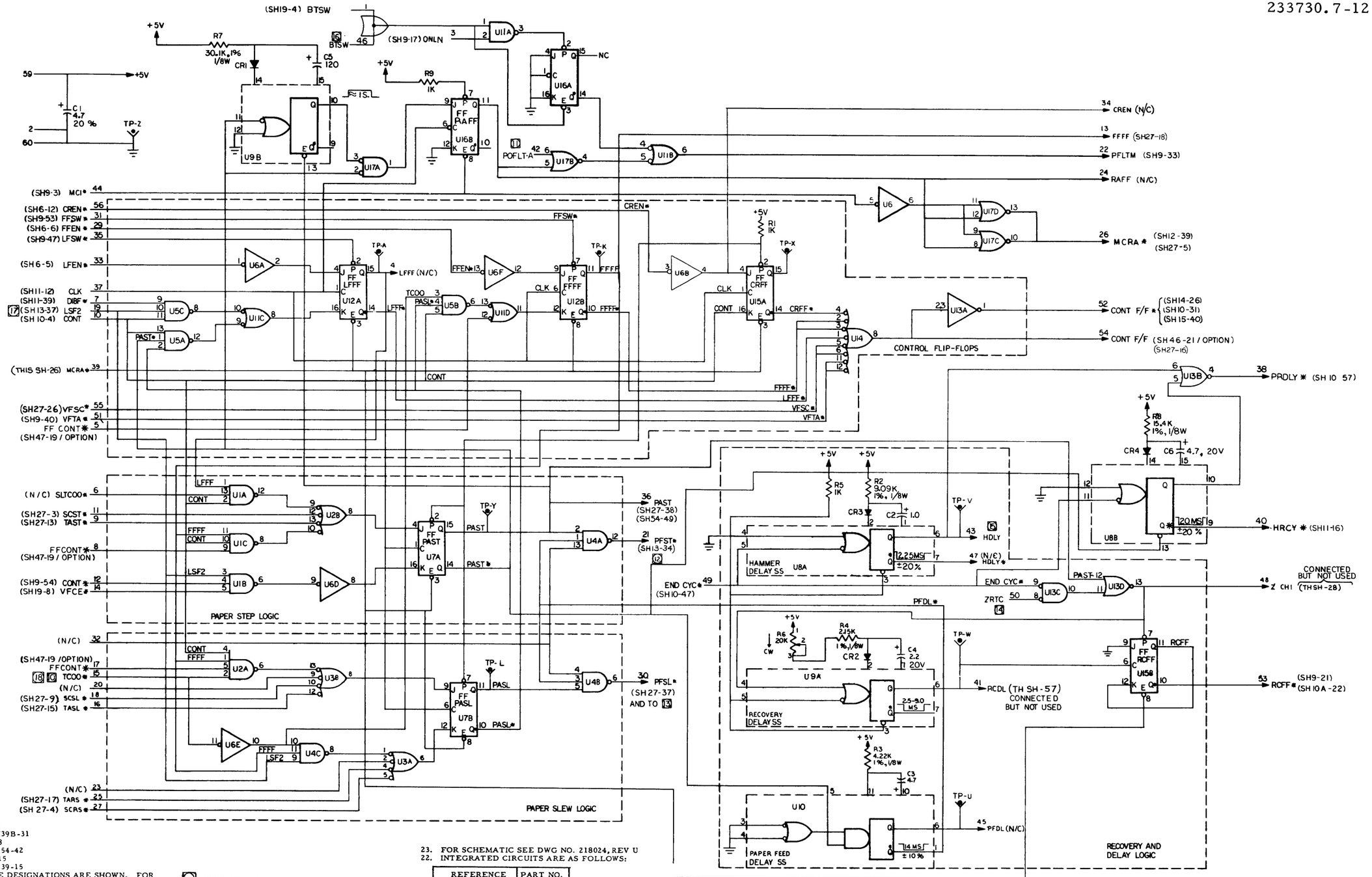
REFERENCE DESIGNATIONS	PART NO. AT-24
U1	800022-001
U2, U6, U8, U17	800024-001
U3, U9	800387-001
U4	800385-001
U5, U12, U15	800023-001
U16	800020-001
U18	800920-001

FOR COMPLETE IC PIN ASSIGNMENTS SEE LOADING DIAGRAMS IN APPENDIX A

CIRCUIT CARD LOCATION: A3A26
(ALL MODELS, ELECTRONICS GATE ASSEMBLY A3, CARD CAGE A, SLOT 26)

LOGIC DIAGRAM SHEET 11

AT-24
TIMING BOARD



(12) MODEL 2420: SH38-31
MODEL 2440/2470: SH39B-31
(11) MODEL 2420: SH38A-8
MODEL 2440/2470: SH54-42
(10) MODEL 2420: SH38A-15
MODEL 2440/2470: SH39-15

9. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION PREFIX WITH CIRCUIT NO.
8. THE FOLLOWING CONNECTOR PINS ARE NOT USED: 28, 46, 57, 58
7. ASSEMBLY DRAWING NUMBER 218020, REV J
6. INTERPRET ELECTRONIC SYMBOLS PER 850026.
5. INTERPRET REFERENCE DESIGNATIONS PER 850027.
4.
3. ALL DIODES ARE 800093-001.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS, 10%, 10 VOLTS.
1. ALL RESISTANCE VALUES ARE IN OHMS, 5%, 1/4 WATT.

NOTES: UNLESS OTHERWISE SPECIFIED

(18) W/12 CHANNEL OPTION (SH47-9) TW00*.
(17) W/12 CHANNEL OPTION (SH47-35) LSF2D.
(16) MODEL 2420: SH38A-1
MODEL 2440/2470: SH39-1
(15) MODEL 2420: NOT USED
MODEL 2440: SH16-7, SH39A-33
MODEL 2470: SH39A-33
(14) MODEL 2420: SH15-29
MODEL 2440: SH16-29
MODEL 2470: NOT USED
(13) MODEL 2420: SH38-32
MODEL 2440/2470: SH39B-32

23. FOR SCHEMATIC SEE DWG NO. 218024, REV U
22. INTEGRATED CIRCUITS ARE AS FOLLOWS:

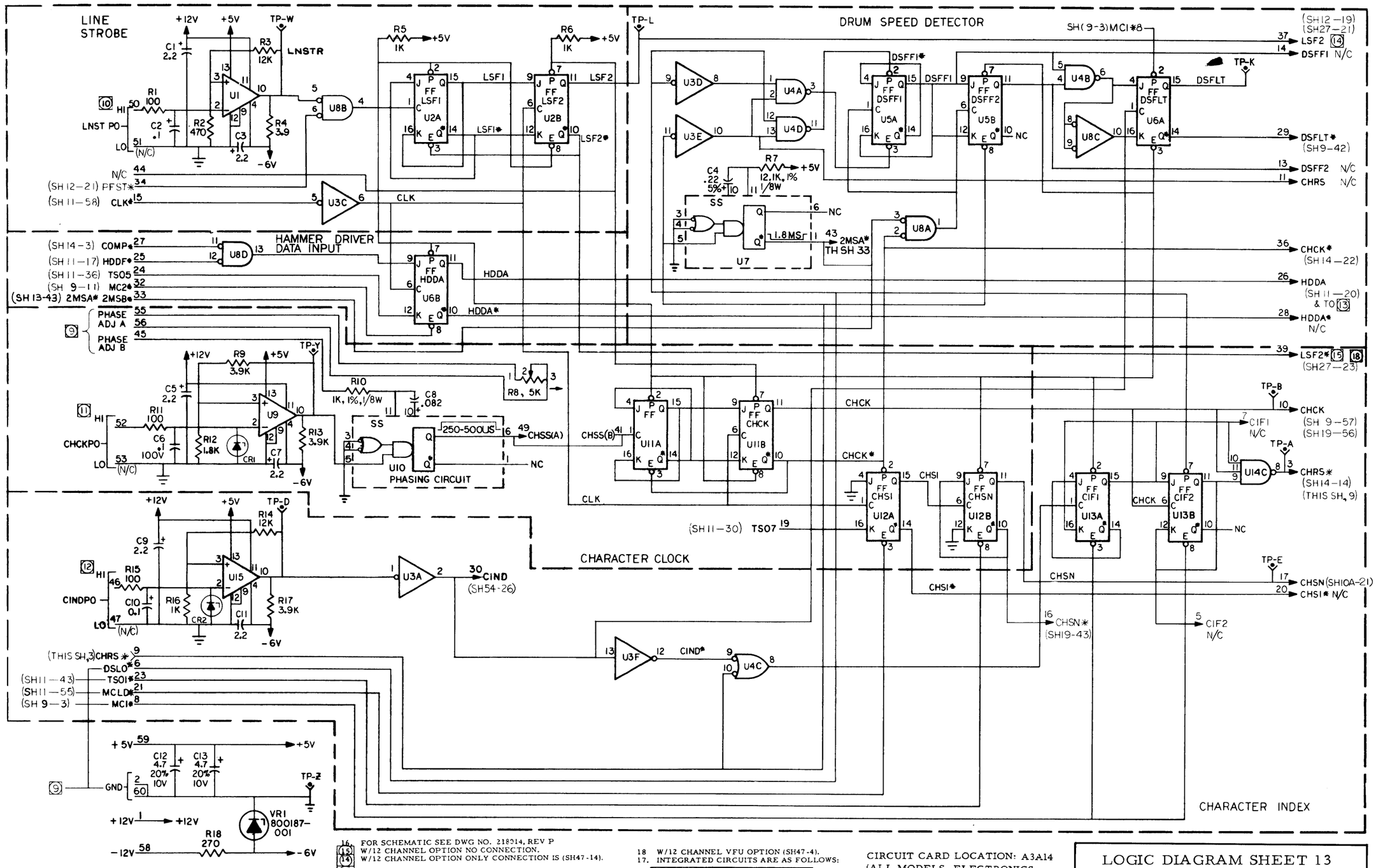
REFERENCE DESIGNATIONS	PART NO. AC-17
U1, U4, U5	800023-001
U2, U3	800020-001
U6	800387-001
U7, U12, U15, U16	800081-001
U8, U9	800810-001
U10	800491-001
U11	800024-001
U13, U17	800080-001
U14	800021-001

FOR COMPLETE IC PIN ASSIGNMENTS SEE LOADING DIAGRAMS IN APPENDIX A

CIRCUIT CARD LOCATION: A3A15
(ALL MODELS, ELECTRONICS GATE ASSEMBLY A3, CARD CAGE A, SLOT 15)

LOGIC DIAGRAM SHEET 12

AC-17
PAPER FEED LOGIC



7. ASSEMBLY DRAWING NUMBER 218010, REV G
6. INTERPRET ELECTRONIC SYMBOLS PER 850026.
5. INTERPRET REFERENCE DESIGNATIONS PER 850027.
4.
3. ALL DIODES ARE 800999-001.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS, 10%, 20 VOLTS.
1. ALL RESISTANCE VALUES ARE IN OHMS, 5%, 1/4 WATT.

NOTES: UNLESS OTHERWISE SPECIFIED

16. FOR SCHEMATIC SEE DWG NO. 218014, REV P
(15) (14) W/12 CHANNEL OPTION NO CONNECTION.
W/12 CHANNEL OPTION ONLY CONNECTION IS (SH47-14).

(13) MODEL 2420: SH23-11
MODEL 2440: SH24-11
MODEL 2470: SH25-11

(12) MODEL 2420: SH38A-56
MODELS 2440/2470: SH39A-56

(11) MODEL 2420: SH38A-55
MODELS 2440/2470: SH39A-55

(10) MODEL 2420: SH38A-54
MODELS 2440/2470: SH39-54

(9) SEE LOGIC DIAGRAM SHEET 49 FOR PHASE OPTION DRUM SPEED.

8. THE FOLLOWING CONNECTOR PINS ARE NOT USED: 4, 12, 18, 22, 31, 35, 38, 40, 42, 48, 54, & 57.

18 W/12 CHANNEL VFU OPTION (SH47-4).

17. INTEGRATED CIRCUITS ARE AS FOLLOWS:

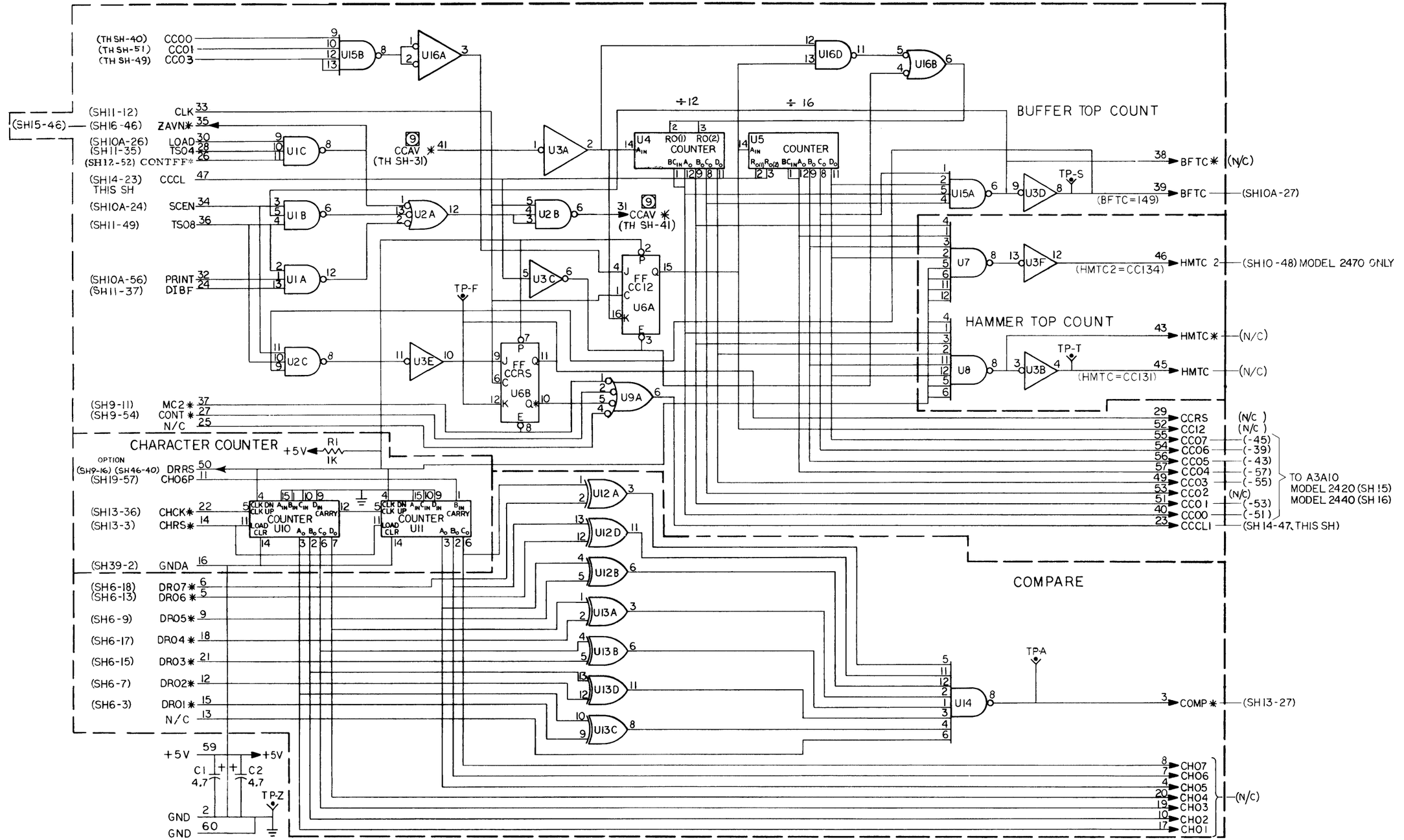
REFERENCE DESIGNATIONS	PART NO. AS-26
U1, U9, U15	800186-001
U2, U5, U6, U11, U12, U13	800081-001
U3	800387-001
U4	800024-001
U7, U10	800491-001
U8	800080-001
U14	800023-001

FOR COMPLETE IC PIN ASSIGNMENTS SEE LOADING DIAGRAMS IN APPENDIX A

CIRCUIT CARD LOCATION: A3A14 (ALL MODELS, ELECTRONICS GATE ASSEMBLY A3, CARD CAGE A, SLOT 14)

LOGIC DIAGRAM SHEET 13

AS-26
TRANSDUCER AMPLIFIER



10. FOR SCHEMATIC SEE DWG NO. 218019, REV N
9. EXTERNAL CONNECTION.
8. THE FOLLOWING CONNECTOR PINS ARE NOT USED: 11, 42, 44, 48, & 58.
7. ASSEMBLY DRAWING NUMBER 218015, REV J
6. INTERPRET ELECTRONIC SYMBOLS PER 850026.
5. INTERPRET REFERENCE DESIGNATIONS PER 850027.
4.
3.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS, 20%, 10 VOLTS.
1. ALL RESISTANCE VALUES ARE IN OHMS, 5%, 1/4 WATT.

NOTES: UNLESS OTHERWISE SPECIFIED

11. INTEGRATED CIRCUITS ARE AS FOLLOWS:

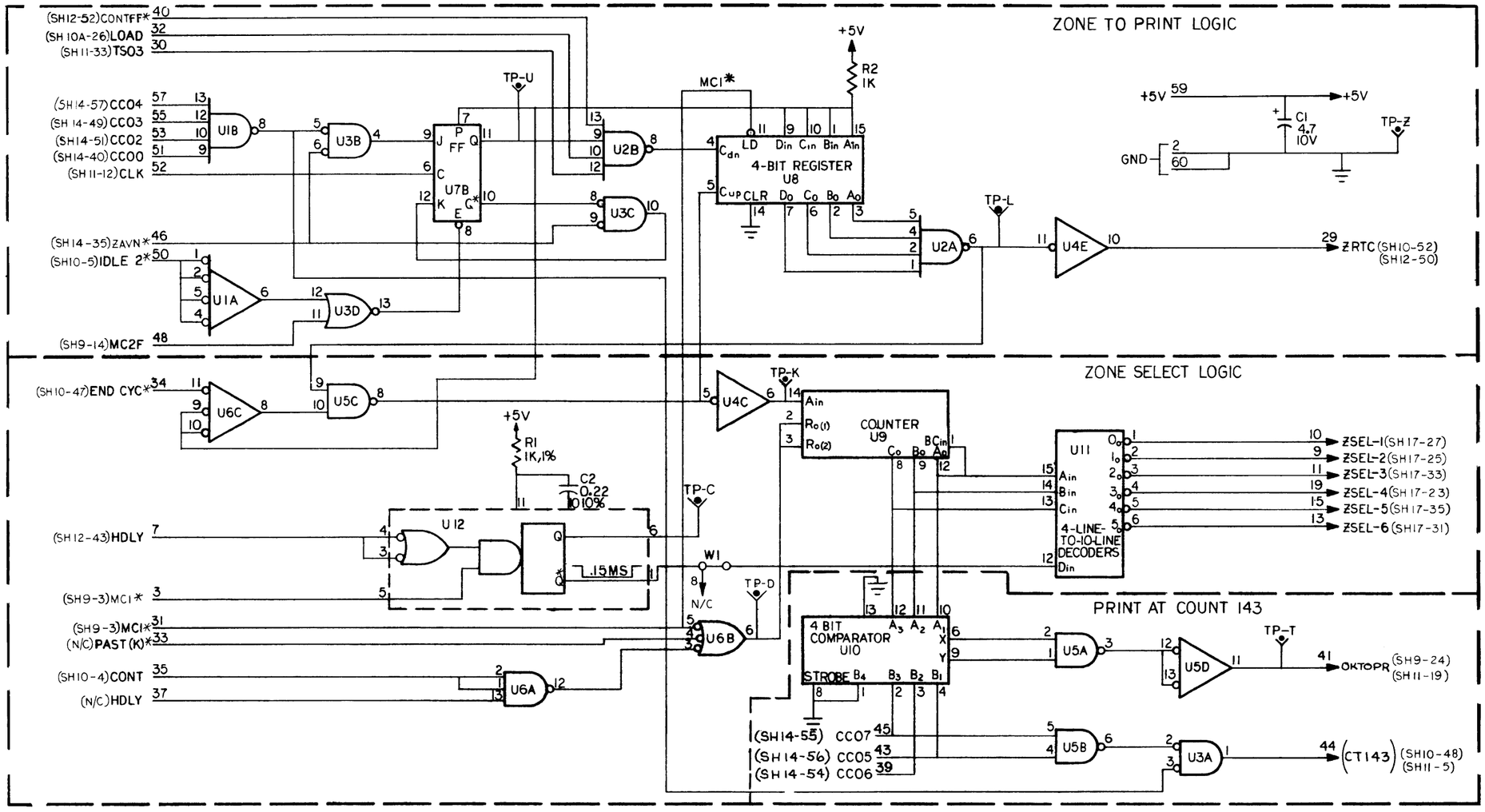
REFERENCE DESIGNATIONS	PART NO. AC-16
U1, U2	800023-001
U3	800387-001
U4, U5	800591-001
U6	800081-001
U7, U8, U14	800021-001
U9, U15	800020-001
U10, U11	800386-001
U12, U13	800370-001
U16	800024-001

FOR COMPLETE IC PIN ASSIGNMENTS SEE LOADING DIAGRAMS IN APPENDIX A

CIRCUIT CARD LOCATION: A3A21
(ALL MODELS, ELECTRONICS GATE ASSEMBLY A3, CARD CAGE A, SLOT 21)

LOGIC DIAGRAM SHEET 14

AC-16
COUNTER/COMPARE



8. THE FOLLOWING CONNECTOR PINS ARE NOT USED: 1, 4, 5, 6, 12, 14, 16, 17, 18, 20 THRU 28, 34, 36, 38, 42, 47, 49, 54, 56, 58.
7. ASSEMBLY DRAWING NUMBER 217100, REV C
6. INTERPRET ELECTRONIC SYMBOLS PER 850026.
5. INTERPRET REFERENCE DESIGNATIONS PER 850027.
4.
3.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS, 20%, 20 VOLTS.
1. ALL RESISTANCE VALUES ARE IN OHMS, 5%, 1/4 WATT.

NOTES: UNLESS OTHERWISE SPECIFIED

10. FOR SCHEMATIC SEE DWG NO. 217104, REV L
9. INTEGRATED CIRCUITS ARE AS FOLLOWS:

REFERENCE DESIGNATIONS	PART NO.
U1, U2	800020-001
U3	800080-001
U4	800387-001
U5	800024-001
U6	800023-001
U7	800081-001
U8	800386-001
U9	800591-001
U11	800385-001
U12	800491-001

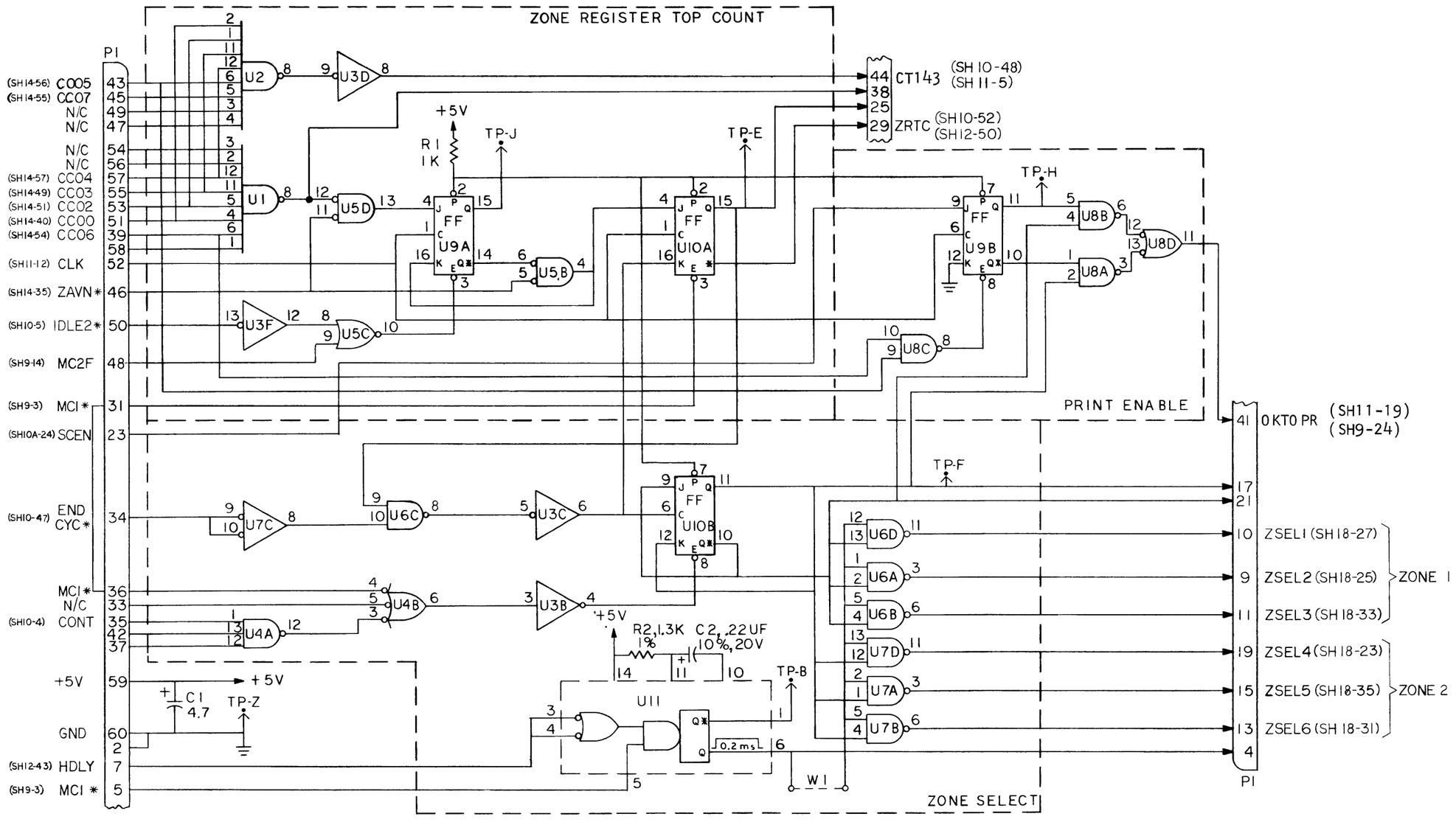
FOR COMPLETE IC PIN ASSIGNMENTS SEE LOADING DIAGRAMS IN APPENDIX A

CIRCUIT CARD LOCATION: A3A10
(MODEL 2420 ONLY, ELECTRONICS GATE ASSEMBLY A3, CARD CAGE A, SLOT 10)

LOGIC DIAGRAM SHEET 15

AG-36
6 ZONE LOGIC

(MODEL 2420)



10. FOR SCHEMATIC SEE DWG NO. 217109, REV K

7. INTEGRATED CIRCUITS ARE AS FOLLOWS:

REFERENCE DESIGNATIONS	PART NO.
U1, U2	800021-001
U3	800387-001
U4	800023-001
U5	800080-001
U6, U7, U8	800024-001
U9, U10	800081-001
U11	800491-001

FOR COMPLETE IC PIN ASSIGNMENTS SEE LOADING DIAGRAMS IN APPENDIX A

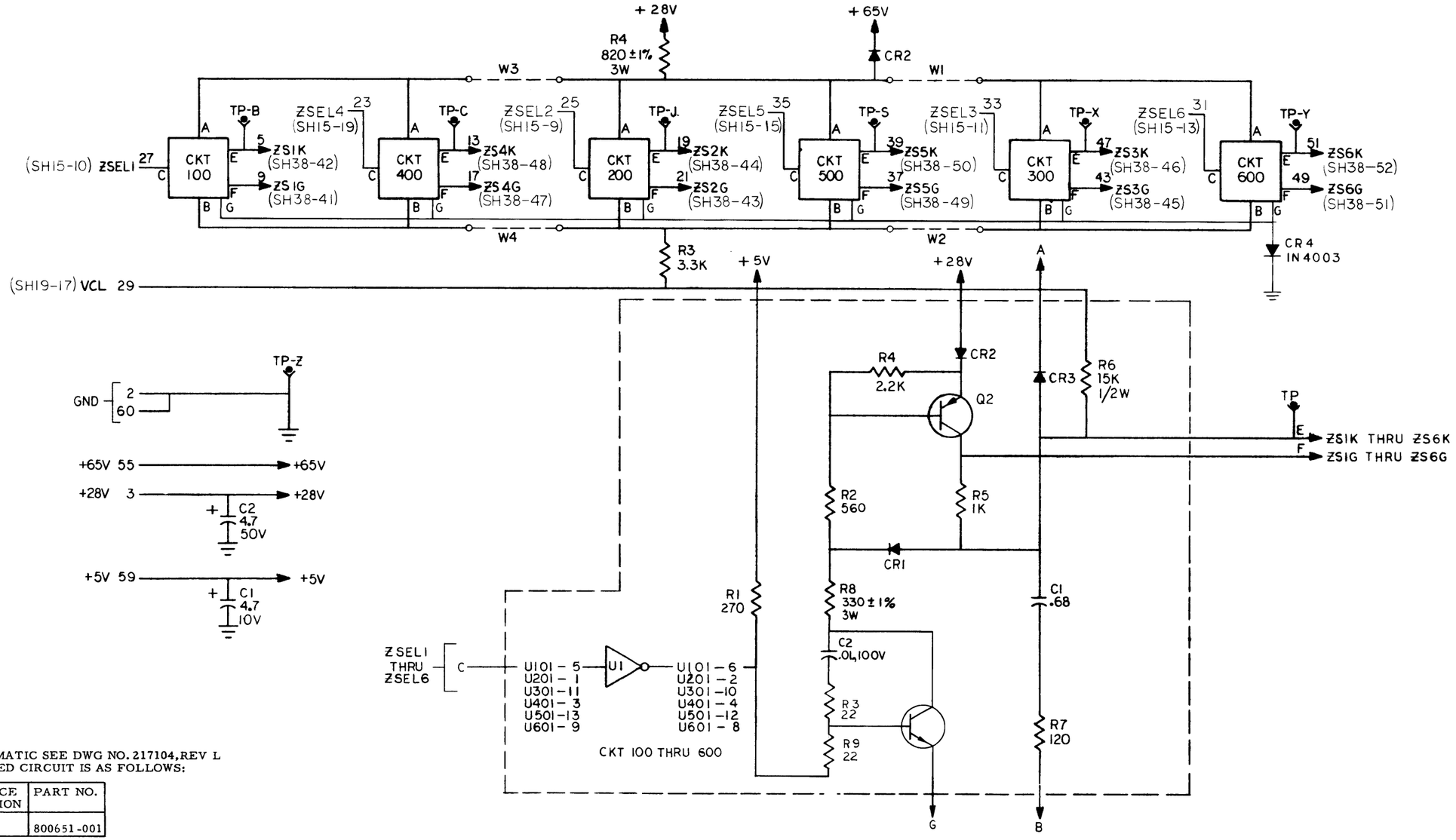
6. THE FOLLOWING CONNECTOR PINS ARE NOT USED: 1, 3, 8, 12, 14, 16, 18, 20, 22, 24, 26, 27, 28, 30, 31, 32, 38, 40
5. ASSEMBLY DRAWING NUMBER 217105, REV B
4. INTERPRET ELECTRONIC SYMBOLS PER USAS Y32.2.
3. INTERPRET REFERENCE DESIGNATIONS PER USAS Y32.16.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS, 20%, 10 VOLTS.
1. ALL RESISTANCE VALUES ARE IN OHMS, 5%, 1/4 WATT.

NOTES: UNLESS OTHERWISE SPECIFIED

CIRCUIT CARD LOCATION: A3A10
(MODEL 2440 ONLY,
ELECTRONICS GATE ASSEMBLY
A3, CARD CAGE A, SLOT 10)

LOGIC DIAGRAM SHEET 16

AG-37
2 ZONE LOGIC
(MODEL 2440)



11. FOR SCHEMATIC SEE DWG NO. 217104, REV L
10. INTEGRATED CIRCUIT IS AS FOLLOWS:

REFERENCE DESIGNATION	PART NO.
U1	800651-001

FOR COMPLETE IC PIN ASSIGNMENTS SEE LOADING DIAGRAMS IN APPENDIX A

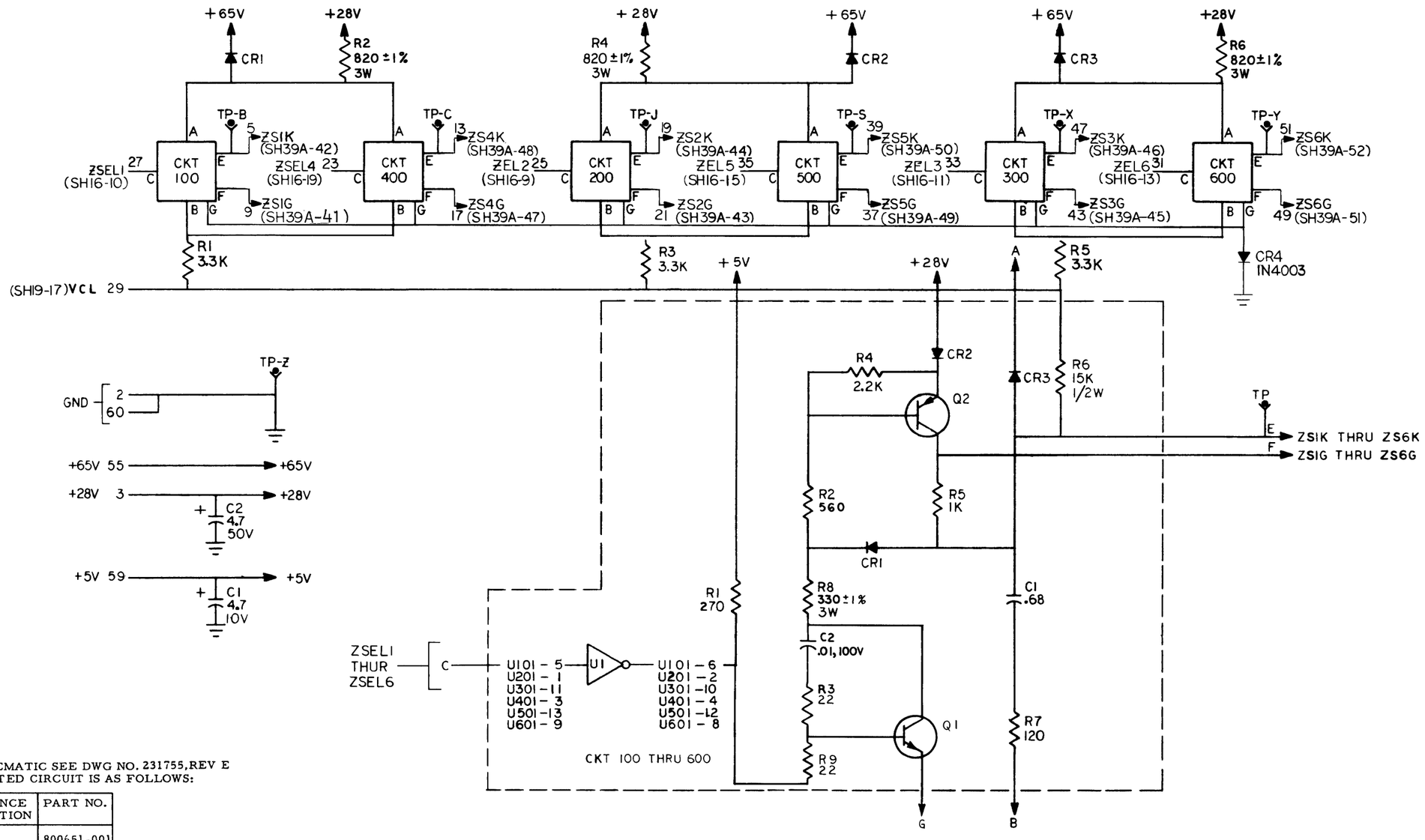
9. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION PREFIX WITH CIRCUIT NO.
8. THE FOLLOWING CONNECTOR PINS ARE NOT USED: 1, 4, 6, 7, 8, 10, 11, 12, 14, 15, 16, 18, 20, 22, 24, 26, 28, 30, 32, 34, 36, 38, 40, 41, 42, 44, 45, 46, 48, 50. 52. 53. 54. 56. 57, 58
7. ASSEMBLY DRAWING NUMBER 231750-1 ,REV C
6. INTERPRET ELECTRONIC SYMBOLS PER USAS Y32. 2.
5. INTERPRET REFERENCE DESIGNATIONS PER USAS Y32. 16.
4. ALL TRANSISTORS ARE 800089-001.
3. ALL DIODES ARE 1N4148.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS, 10%, 75 VOLTS.
1. ALL RESISTANCE VALUES ARE IN OHMS, ±5%, 1/4 WATT.

NOTES: UNLESS OTHERWISE SPECIFIED

CIRCUIT CARD LOCATION: A3A11
(MODEL 2420 ONLY, ELECTRONICS GATE ASSEMBLY A3, CARD CAGE A, SLOT 11)

LOGIC DIAGRAM SHEET 17

AH-24
ZONE SELECT



11. FOR SCHEMATIC SEE DWG NO. 231755, REV E
10. INTEGRATED CIRCUIT IS AS FOLLOWS:

REFERENCE DESIGNATION	PART NO.
U1	800651-001

FOR COMPLETE IC PIN ASSIGNMENTS SEE LOADING DIAGRAMS IN APPENDIX A

9. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION PREFIX WITH CIRCUIT NO.
8. THE FOLLOWING CONNECTOR PINS ARE NOT USED: 1, 4, 6, 7, 8, 10, 11, 12, 14, 15, 16, 18, 20, 22, 24, 26, 28, 30, 32, 34, 36, 38, 40, 41, 42, 44, 45, 46, 48, 50, 52, 53, 54, 56, 57, 58
7. ASSEMBLY DRAWING NUMBER 231750-2 REV C
6. INTERPRET ELECTRONIC SYMBOLS PER USAS Y32.2.
5. INTERPRET REFERENCE DESIGNATIONS PER USAS Y32.16.
4. ALL TRANSISTORS ARE 800089-001.
3. ALL DIODES ARE 1N4148.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS, 10%, 75 VOLTS.
1. ALL RESISTANCE VALUES ARE IN OHMS, ±5%, 1/4 WATT.

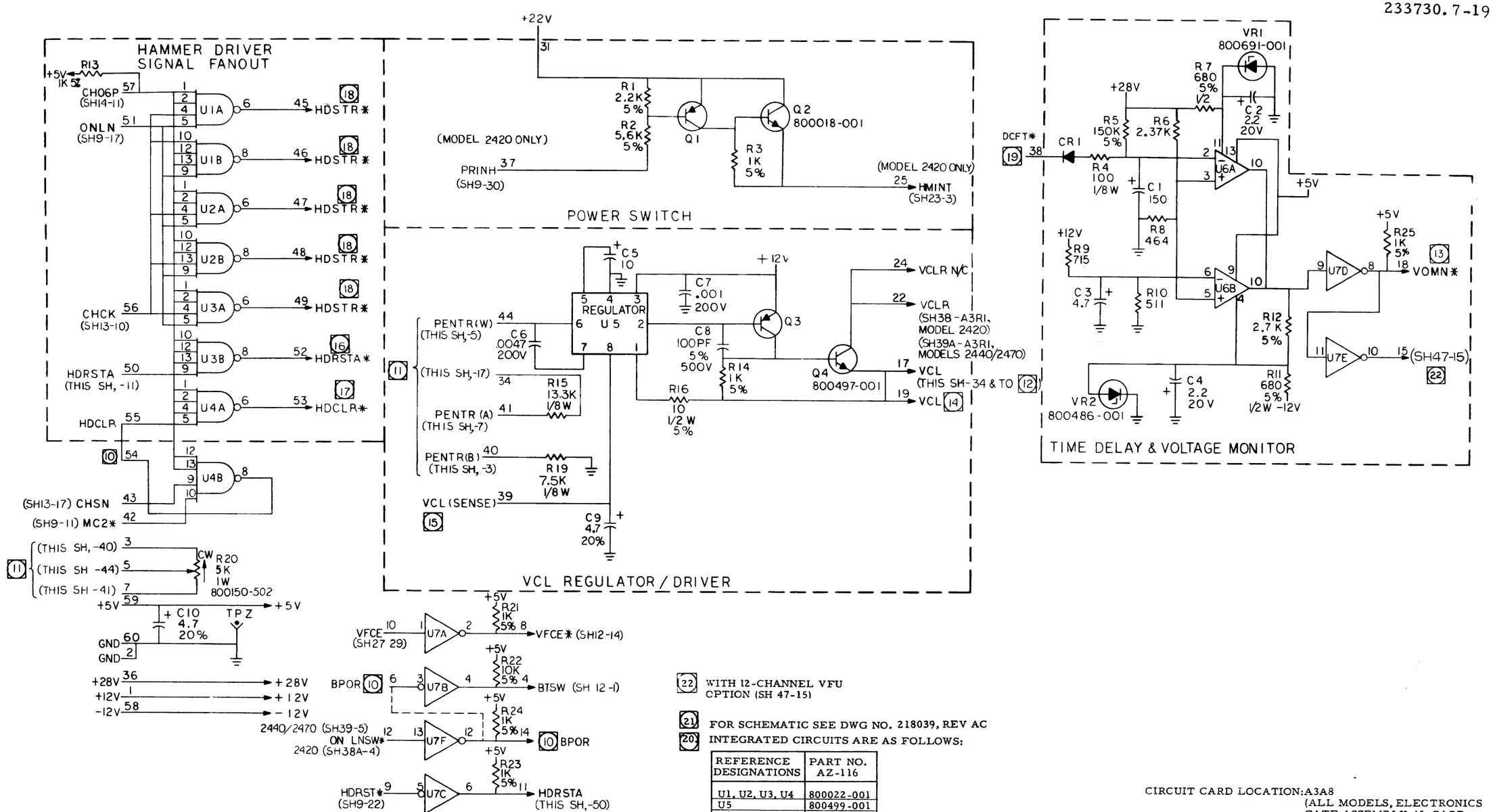
NOTES: UNLESS OTHERWISE SPECIFIED

CIRCUIT CARD LOCATION: A3A11
(MODEL 2440 ONLY, ELECTRONICS GATE ASSEMBLY A3, CARD CAGE A, SLOT 11)

LOGIC DIAGRAM SHEET 18

AH-25

ZONE SELECT



(11) CONNECTIONS SHOWN ARE FOR STANDARD PRINTERS. IF PENETRATION CONTROL OPTION IS INSTALLED, REFER TO LOGIC DIAGRAM 49 FOR ALTERNATE CONNECTIONS.

(10) EXTERNAL CONNECTION.

9.

8. THE FOLLOWING CONNECTOR PINS ARE NOT USED: 13, 16, 20, 21, 23, 26, 27, 28, 29, 30, 32, 33, 35
7. ASSEMBLY DRAWING NUMBER 218035,REV S
6. INTERPRET ELECTRONIC SYMBOLS PER 850026.
5. INTERPRET REFERENCE DESIGNATIONS PER 850027.
4. ALL TRANSISTORS ARE 800089-001.
3. ALL DIODES ARE 800094-001.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS, 10%, 10 VOLTS.
1. ALL RESISTANCE VALUES ARE IN OHMS, 1%, 1/4 WATT.

NOTES: UNLESS OTHERWISE SPECIFIED

(17) MODEL 2420: SH23-13
MODEL 2440: SH24-13
MODEL 2470: SH25-13

(16) MODEL 2420: SH23-9
MODEL 2440: SH24-9, SH24A-9
MODEL 2470: SH25C-9

(15) MODEL 2420: SH23-A3E3
MODEL 2440: SH'S25A, B, C(VCL BUS)
MODEL 2470: SH25A (VCL BUS)

(14) MODEL 2420: NOT USED
MODEL 2440: SH24A (VCL BUS)
MODEL 2470: SH'S25A, B, C(VCL BUS)

(13) MODEL 2420: SH9-16

(12) MODELS 2440/2470: SH39A-53
MODEL 2420: SH17-29
MODEL 2440: SH18-29, 24A
MODEL 2470: NOT USED

(22) WITH 12-CHANNEL VFU OPTION (SH 47-15)

(21) FOR SCHEMATIC SEE DWG NO. 218039, REV AC

(20) INTEGRATED CIRCUITS ARE AS FOLLOWS:

REFERENCE DESIGNATIONS	PART NO. AZ-116
U1, U2, U3, U4	800022-001
U5	800499-001
U6	800186-001
U7	800651-001

FOR COMPLETE IC PIN ASSIGNMENTS SEE LOADING DIAGRAMS IN APPENDIX A

(19) MODEL 2420: THIS SHEET +5V
MODELS 2440/2470: SH39A-9 (DCFT*)

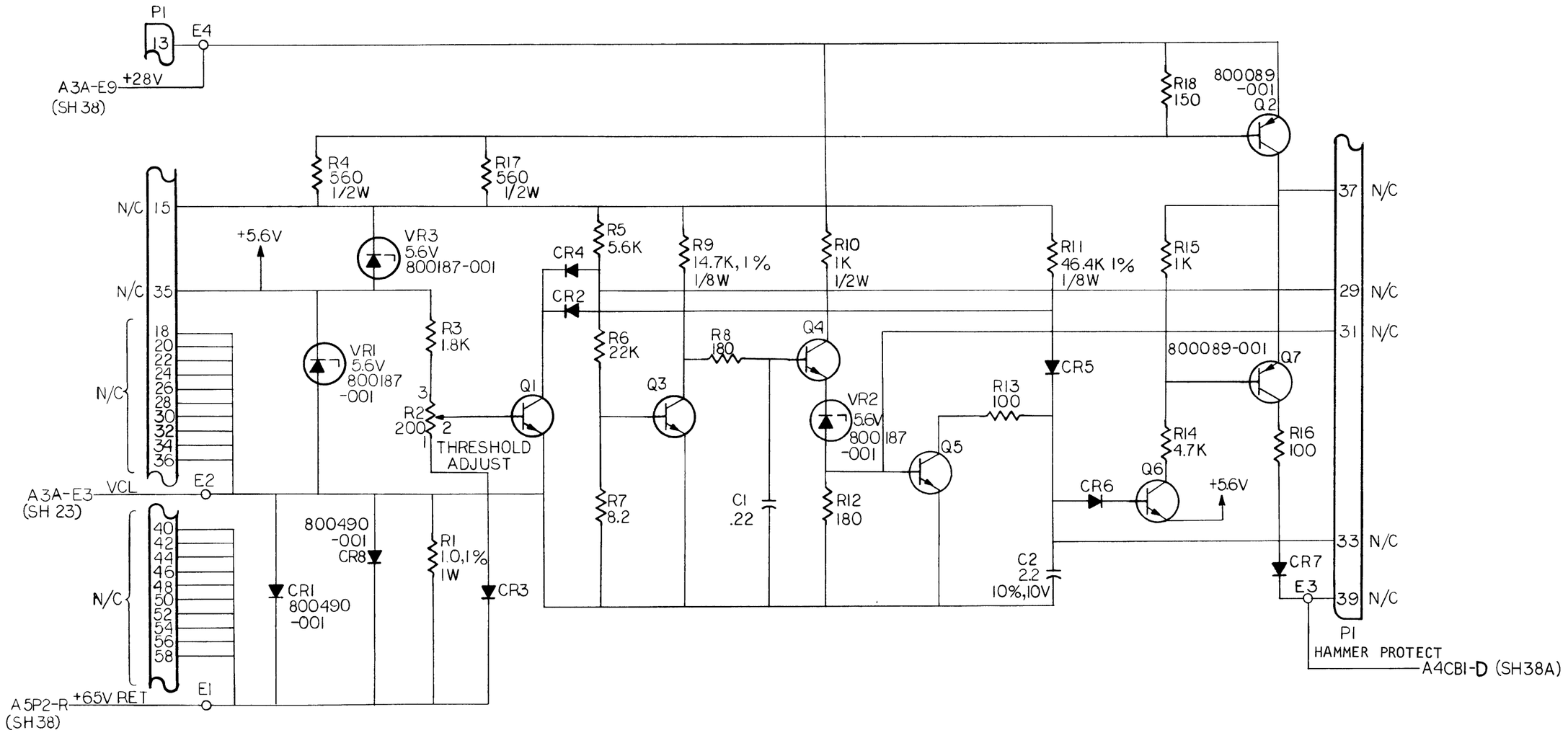
(18) HDSTR*

FROM PIN	TO 2420	2440	2470
-45		SH24A-41	SH25A-41
-46		SH24A-41	SH25A-41
-47			SH25A-41
-48			SH25A-41
-49	SH23-4	SH24-41	SH25-41

CIRCUIT CARD LOCATION: A3A8
(ALL MODELS, ELECTRONICS GATE ASSEMBLY A3, CARD CAGE A, SLOT 8)

LOGIC DIAGRAM SHEET 19

AZ-116
HAMMER FANOUT



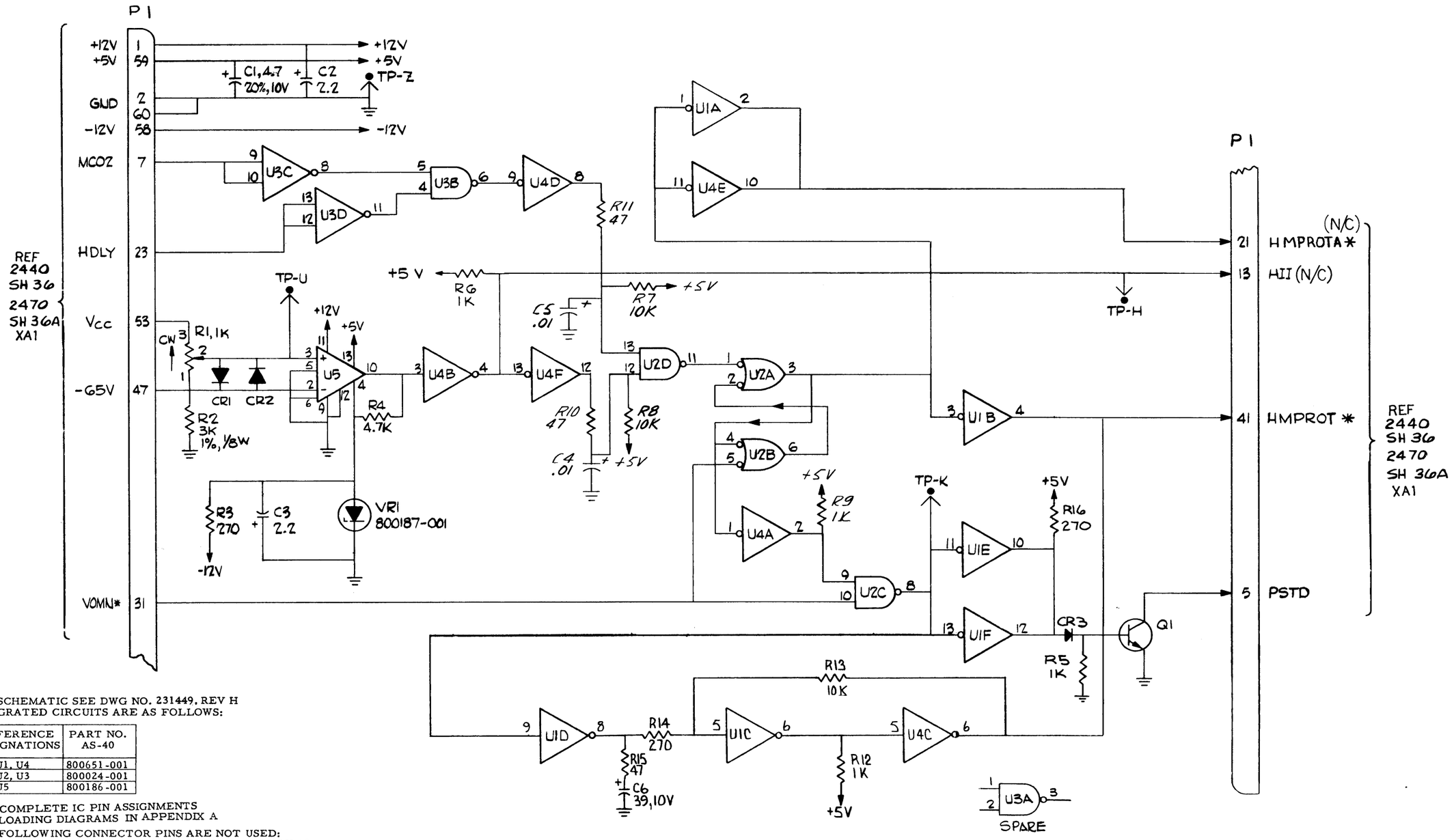
9. FOR SCHEMATIC SEE DWG NO. 232443, REV C
8. THE FOLLOWING CONNECTOR PINS ARE NOT USED: 1 THRU 12, 14, 16, 17, 19, 21, 23, 25, 27, 38, 41, 43, 45, 47, 49, 51, 53, 55, 57, 59, 60
7. ASSEMBLY DRAWING NUMBER 216790-2, REV F
6. INTERPRET ELECTRONIC SYMBOLS PER USAS Y32.2.
5. INTERPRET REFERENCE DESIGNATIONS PER USAS Y32.16.
4. ALL TRANSISTORS ARE 800231-001.
3. ALL DIODES ARE 800093-001.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS, 5%, 20 VOLTS.
1. ALL RESISTANCE VALUES ARE IN OHMS, 5%, 1/4 WATT.

NOTES: UNLESS OTHERWISE SPECIFIED

CIRCUIT CARD LOCATION: A3A2
(MODEL 2420 ONLY,
ELECTRONICS CATE ASSEMBLY
A3, CARD CAGE A, SLOT 2)

LOGIC DIAGRAM SHEET 20

AS-46
HAMMER CURRENT
MONITOR
(MODEL 2420)



10. FOR SCHEMATIC SEE DWG NO. 231449, REV H
9. INTEGRATED CIRCUITS ARE AS FOLLOWS:

REFERENCE DESIGNATIONS	PART NO. AS-40
U1, U4	800651-001
U2, U3	800024-001
U5	800186-001

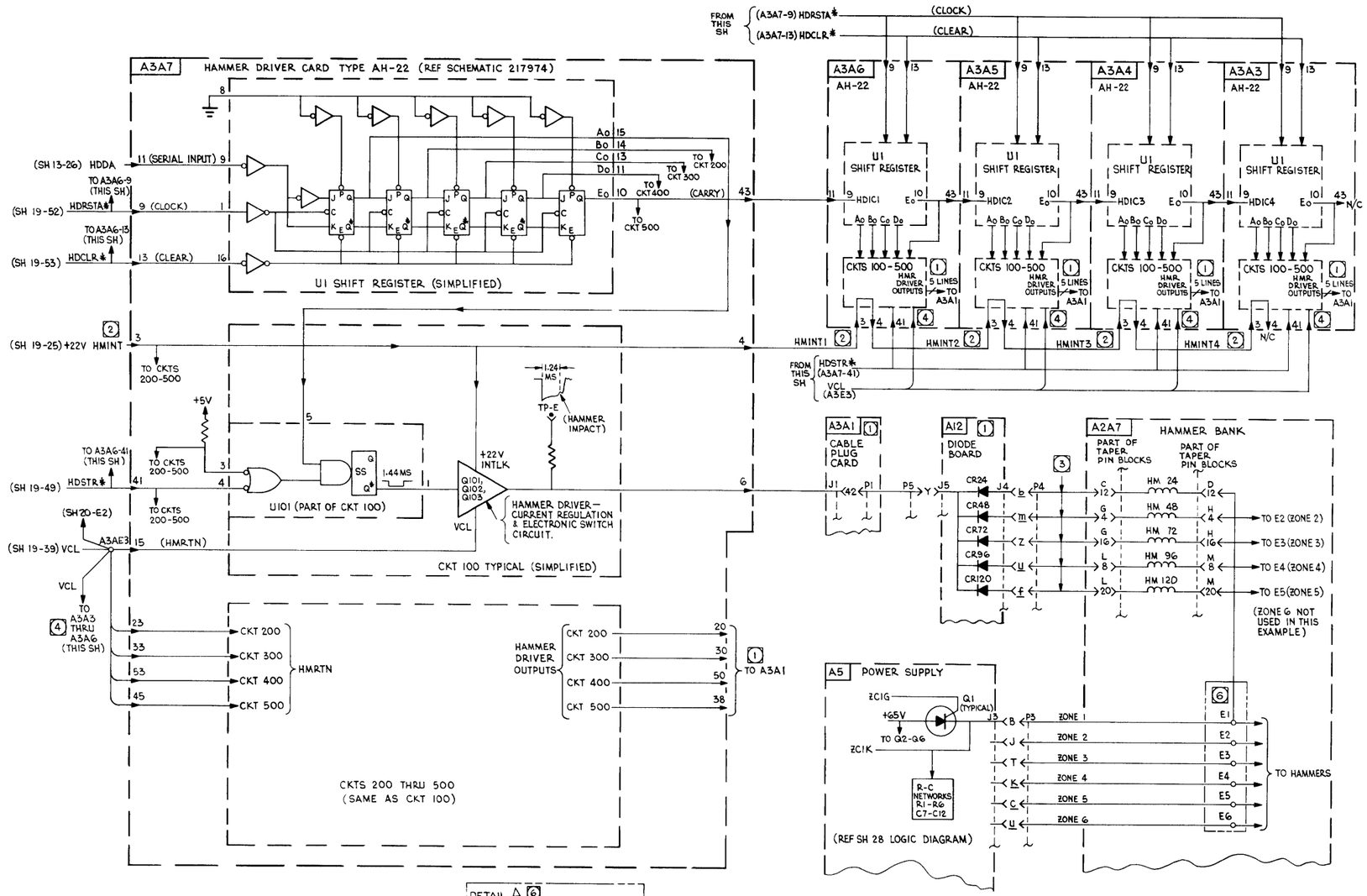
FOR COMPLETE IC PIN ASSIGNMENTS SEE LOADING DIAGRAMS IN APPENDIX A

8. THE FOLLOWING CONNECTOR PINS ARE NOT USED: 3, 4, 6, 8 THRU 12, 14 THRU 20, 22, 24 THRU 30, 32 THRU 40, 42 THRU 46, 48 THRU 52, 54 THRU 57
7. ASSEMBLY DRAWING NUMBER 231445, REV E
6. INTERPRET ELECTRONIC SYMBOLS PER USAS Y32.2.
5. INTERPRET REFERENCE DESIGNATIONS PER USAS Y32.16.
4. ALL TRANSISTORS ARE 800018-001.
3. ALL DIODES ARE 800093-001.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS, 10%, 20 VOLTS.
1. ALL RESISTANCE VALUES ARE IN OHMS, 5%, 1/4 WATT.

NOTES: UNLESS OTHERWISE SPECIFIED

CIRCUIT CARD LOCATION: A8A1
(MODELS 2440/2470 HAMMER BANK POWER SUPPLY ASSEMBLY A8, CARD CAGE SLOT A1)

LOGIC DIAGRAM SHEET 21
AS-40
HAMMER DRIVER PROTECTION
(MODELS 2440/2470)



[1] TAB LIST A
SOURCE OF HAMMER DRIVER OUTPUTS TO A3A1 (J1)

FROM HAMMER DRIVER CARD TYPE AH-22				TO CABLE PLUG CARD P1 (A3A1) PIN NO.	RELATED HAMMERS					
LOCATION	PIN NO.	CKT NO.	TP		ZONE 1	ZONE 2	ZONE 3	ZONE 4	ZONE 5	ZONE 6
A3A3	50	400	Y	19	1	25	49	73	97	121
	30	300	R	20	2	26	50	74	98	122
	20	200	L	21	3	27	51	75	99	123
	6	100	E	22	4	28	52	76	100	124
A3A4	38	500	V	23	5	29	53	77	101	125
	50	400	Y	24	6	30	54	78	102	126
	30	300	R	25	7	31	55	79	103	127
	20	200	L	26	8	32	56	80	104	128
	6	100	E	27	9	33	57	81	105	129
A3A5	38	500	V	28	10	34	58	82	106	130
	50	400	Y	29	11	35	59	83	107	131
	30	300	R	30	12	36	60	84	108	132
	20	200	L	31	13	37	61	85	109	133
	6	100	E	32	14	38	62	86	110	134
A3A6	38	500	V	33	15	39	63	87	111	135
	50	400	Y	34	16	40	64	88	112	136
	30	300	R	35	17	41	65	89	113	—
	20	200	L	36	18	42	66	90	114	—
	6	100	E	37	19	43	67	91	115	—
A3A7	38	500	V	38	20	44	68	92	116	—
	50	400	Y	39	21	45	69	93	117	—
	30	300	R	40	22	46	70	94	118	—
	20	200	L	41	23	47	71	95	119	—
	6	100	E	42	24	48	72	96	120	—

[6] REFER TO DETAIL "A" FOR WIRING APPLICABLE TO SERIAL NUMBERS 6088 AND SUBSEQUENT.

5. INTEGRATED CIRCUITS ARE AS FOLLOWS:

REFERENCE DESIGNATIONS	PART NO.
U1	800638-001
U101, U201, U301, U401, U501	800491-001

FOR COMPLETE IC PIN ASSIGNMENTS SEE LOADING DIAGRAMS IN APPENDIX A

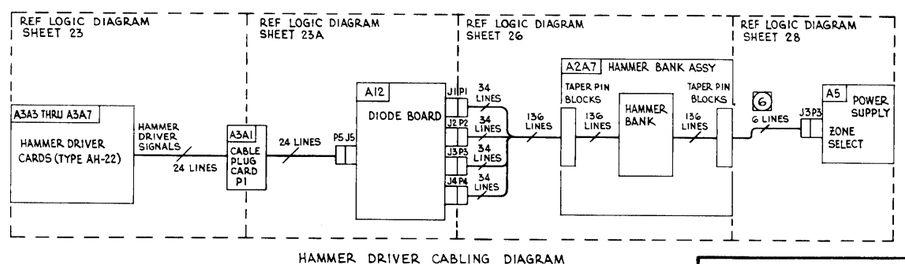
[4] VCL CONNECTS TO PINS 15, 23, 33, 53, & 45 OF EACH CARD.

[3] REFER TO LOGIC DIAGRAM SHEET 26 FOR INTERCONNECTION OF ALL HAMMERS.

[2] +22V HMINT (HAMMER INTERLOCK) SUPPLY IS CONNECTED IN SERIES THROUGH AN INTERNAL CONNECTION ON AH-22 CARD TYPES. REMOVAL OF AN AH-22 CARD RESULTS IN AN OPEN SUPPLY TO CARDS IN SERIES-STRING FOLLOWING IT.

[1] REFER TO TABULAR LIST A AND LOGIC DIAGRAM 23A FOR INTERCONNECTION OF ALL HAMMER DRIVER CIRCUITS TO CABLE PLUG CARD A3A (P1) & TO DIODE BOARD A12.

NOTES: UNLESS OTHERWISE SPECIFIED

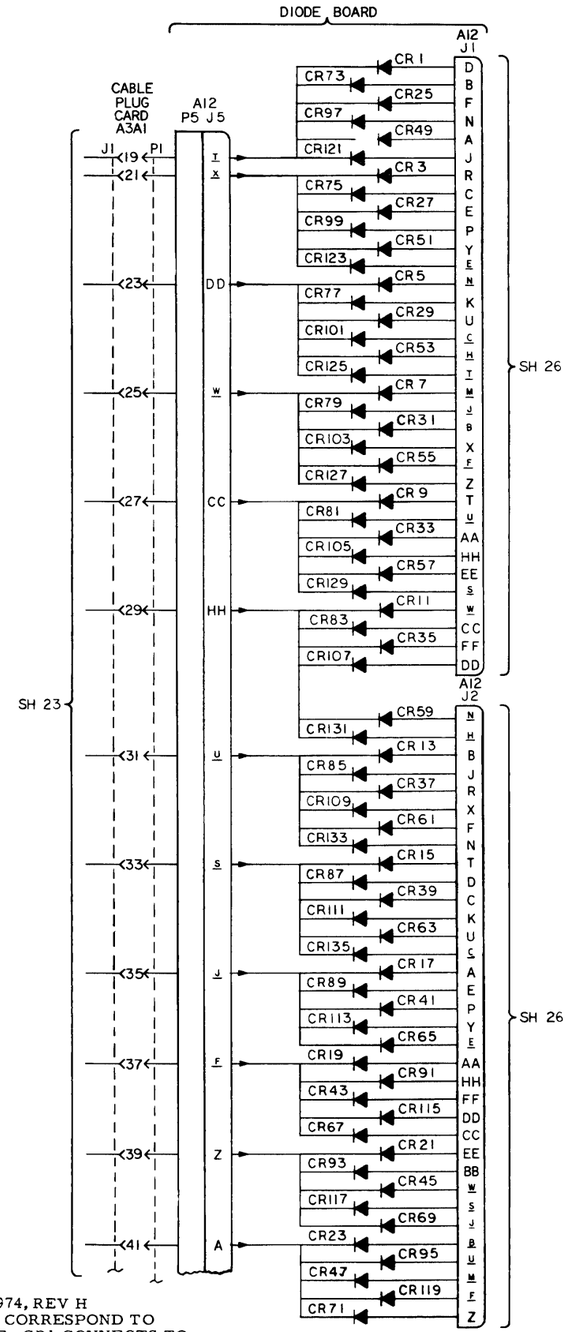


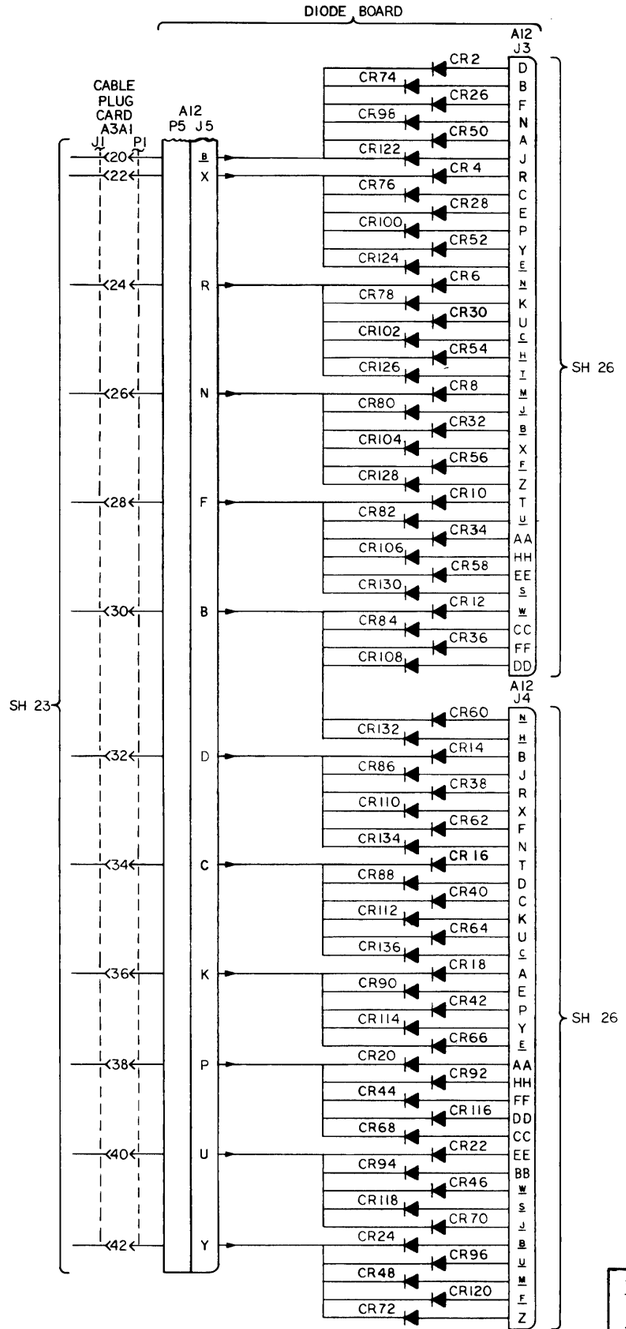
HAMMER DRIVER CABLING DIAGRAM

CIRCUIT CARD LOCATION: A3A1 TO A3A12
(MODEL 2420 ONLY,
ELECTRONICS GATE ASSEMBLY
A3, CARD CAGE A, SLOTS
1 TO 12)

LOGIC DIAGRAM SHEET 23

HAMMER DRIVER CIRCUITS, TYPICAL INTERCONNECTION (MODEL 2420)





6. FOR SCHEMATIC SEE DWG NO. 217974, REV H
5. DIODE REFERENCE DESIGNATIONS CORRESPOND TO HAMMER NUMBERS (FOR EXAMPLE, CR1 CONNECTS TO HAMMER NO. 1, ETC.).
4. ASSEMBLY DRAWING NUMBER 230540, REV C
3. INTERPRET ELECTRONIC SYMBOLS PER USAS Y32.2.
2. INTERPRET REFERENCE DESIGNATIONS PER USAS Y32.16.
1. ALL DIODES ARE 800095-001.

NOTES: UNLESS OTHERWISE SPECIFIED

DIODE BOARD LOCATION: A12
(MODEL 2420 ONLY,
DIODE BOARD ASSEMBLY A12)

LOGIC DIAGRAM SHEET 23A

DIODE BOARD,
HAMMER DRIVER CIRCUITS
(MODEL 2420)

(1) TAB LIST A

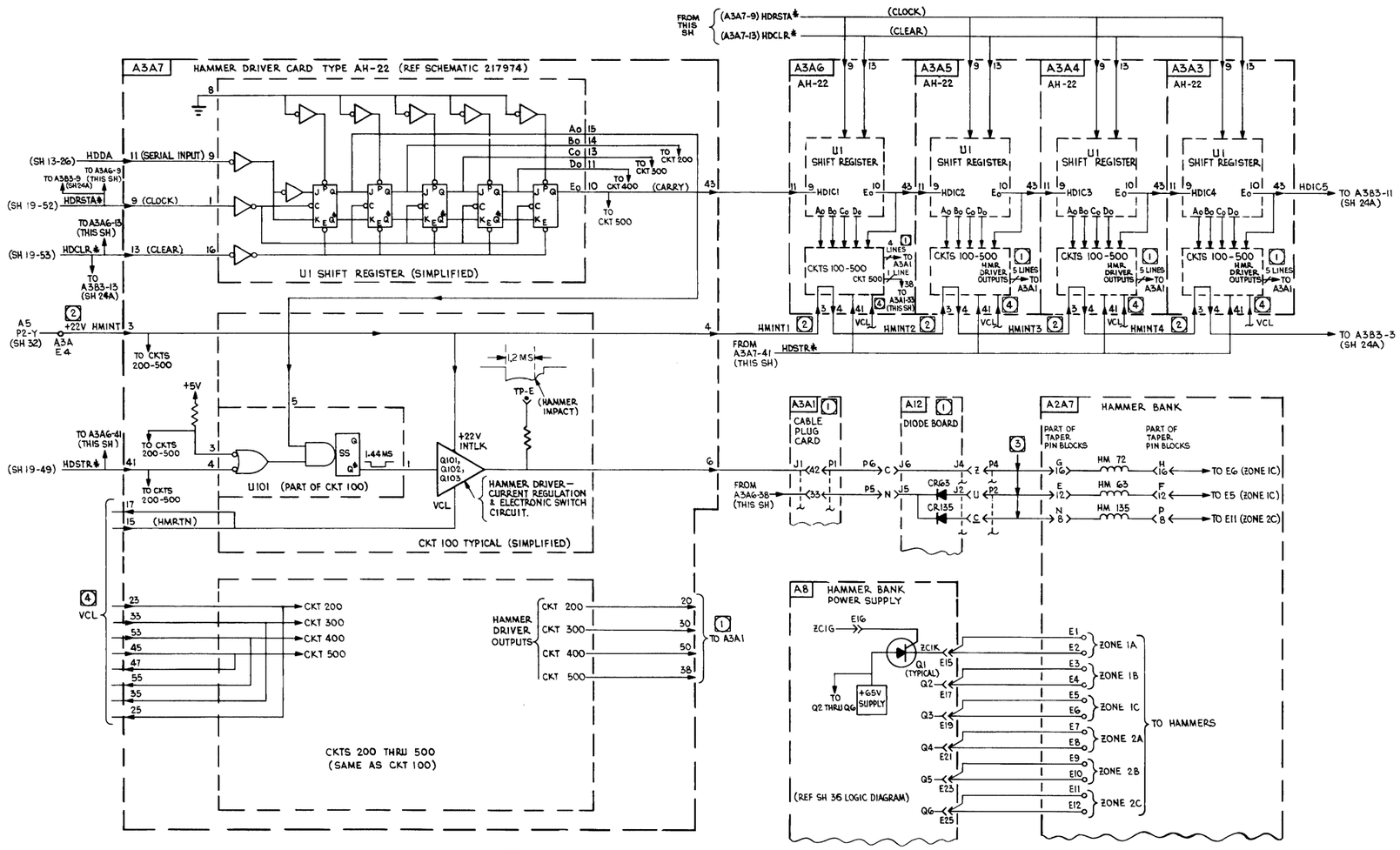
SOURCE OF HAMMER DRIVER OUTPUTS

TO A3B1(J1)

FROM HAMMER DRIVER CARD TYPE AH-22				TO CABLE PLUG CARD P1 (A3B1) PIN NO.	RELATED HAMMERS	
LOCATION	PIN NO.	CKT NO.	TP		ZONE 1	ZONE 2
A3B12	20	200	L	4	1	73
	6	100	E	6	2	74
A3B11	38	500	V	8	3	75
	50	400	Y	10	4	76
	30	300	R	12	5	77
	20	200	L	18	6	78
	6	100	E	20	7	79
A3B10	38	500	V	22	8	80
	50	400	Y	24	9	81
	30	300	R	26	10	82
	20	200	L	28	11	83
	6	100	E	30	12	84
A3B9	38	500	V	32	13	85
	50	400	Y	34	14	86
	30	300	R	36	15	87
	20	200	L	38	16	88
	6	100	E	40	17	89
A3B8	38	500	V	42	18	90
	50	400	Y	44	19	91
	30	300	R	50	20	92
	20	200	L	52	21	93
	6	100	E	54	22	94
A3B7	38	500	V	56	23	95
	50	400	Y	58	24	96
	30	300	R	19	25	97
	20	200	L	21	26	98
	6	100	E	23	27	99
A3B6	38	500	V	25	28	100
	50	400	Y	27	29	101
	30	300	R	29	30	102
	20	200	L	31	31	103
	6	100	E	33	32	104
A3B5	38	500	V	35	33	105
	50	400	Y	37	34	106
	30	300	R	39	35	107
	20	200	L	41	36	108

TO A3A1(J1)

FROM HAMMER DRIVER CARD TYPE AH-22				TO CABLE PLUG CARD P1 (A3A1) PIN NO.	RELATED HAMMERS	
LOCATION	PIN NO.	CKT NO.	TP		ZONE 1	ZONE 2
A3B5	6	100	E	44	37	109
A3B4	38	500	V	4	38	110
	50	400	Y	50	39	111
	30	300	R	6	40	112
	20	200	L	52	41	113
	6	100	E	8	42	114
A3B3	38	500	V	54	43	115
	50	400	Y	10	44	116
	30	300	R	56	45	117
	20	200	L	12	46	118
	6	100	E	58	47	119
A3A3	38	500	V	18	48	120
	50	400	Y	19	49	121
	30	300	R	20	50	122
	20	200	L	21	51	123
	6	100	E	22	52	124
A3A4	38	500	V	23	53	125
	50	400	Y	24	54	126
	30	300	R	25	55	127
	20	200	L	26	56	128
	6	100	E	27	57	129
A3A5	38	500	V	28	58	130
	50	400	Y	29	59	131
	30	300	R	30	60	132
	20	200	L	31	61	133
	6	100	E	32	62	134
A3A6	38	500	V	33	63	135
	50	400	Y	34	64	136
	30	300	R	35	65	-
	20	200	L	36	66	-
	6	100	E	37	67	-
A3A7	38	500	V	38	68	-
	50	400	Y	39	69	-
	30	300	R	40	70	-
	20	200	L	41	71	-
	6	100	E	42	72	-



5. INTEGRATED CIRCUITS ARE AS FOLLOWS

REFERENCE DESIGNATORS	PART NO.
U1	800638-001
U101, U201, U301, U401, U501	800491-001

FOR COMPLETE IC PIN ASSIGNMENTS SEE LOADING DIAGRAMS IN APPENDIX A

(4) REFER TO TABULAR LIST B FOR VCL INTERCONNECTION.

(3) REFER TO LOGIC DIAGRAM SHEET 26 FOR INTERCONNECTION OF ALL HAMMERS.

(2) +22V HMINT (HAMMER INTERLOCK) SUPPLY IS CONNECTED IN SERIES THROUGH AN INTERNAL CONNECTION ON AH-22 CARD TYPES. REMOVAL OF AN AH-22 CARD RESULTS IN AN OPEN SUPPLY TO CARDS IN SERIES-STRING FOLLOWING IT.

(1) REFER TO TABULAR LIST A AND LOGIC DIAGRAM 24B FOR INTERCONNECTION OF ALL HAMMER DRIVER CIRCUITS TO CABLE PLUG CARDS A3A (P1) AND A3B1 (P1) AND TO DIODE BAORD A12.

NOTES: UNLESS OTHERWISE SPECIFIED

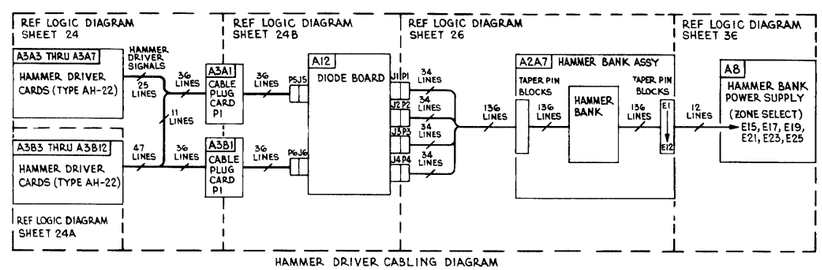
(4) TAB B

VCL INTERCONNECTION DATA

(REF SH 2 A, VCL BUS)

FROM	TO
A3B3-15	A3A3-15
A3B3-17	A3A3-17
A3B3-23	A3A3-23
A3B3-25	A3A3-25
A3B3-33	A3A3-33
A3B3-35	A3A3-35
A3B3-45	A3A3-45
A3B3-47	A3A3-47
A3B3-53	A3A3-53
A3B3-55	A3A3-55
A3B4-15	A3A4-15
A3B4-17	A3A4-17
A3B4-23	A3A4-23
A3B4-25	A3A4-25
A3B4-33	A3A4-33
A3B4-35	A3A4-35
A3B4-45	A3A4-45
A3B4-47	A3A4-47
A3B4-53	A3A4-53
A3B4-55	A3A4-55
A3B5-15	A3A5-15
A3B5-17	A3A5-17
A3B5-23	A3A5-23
A3B5-25	A3A5-25
A3B5-33	A3A5-33

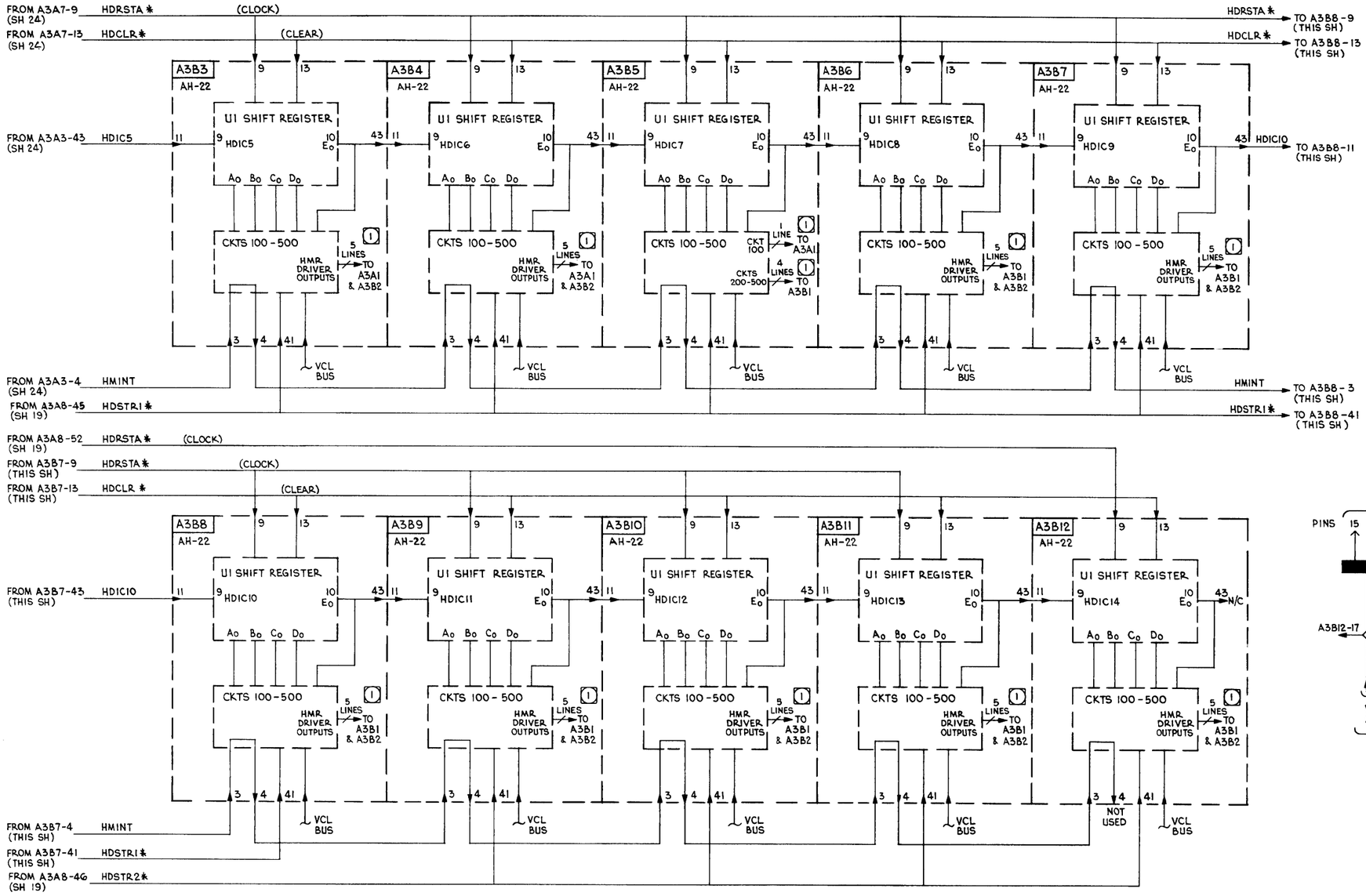
FROM	TO
A3B5-35	A3A5-35
A3B5-45	A3A5-45
A3B5-47	A3A5-47
A3B5-53	A3A5-53
A3B5-55	A3A5-55
A3B6-15	A3A6-15
A3B6-17	A3A6-17
A3B6-23	A3A6-23
A3B6-25	A3A6-25
A3B6-33	A3A6-33
A3B6-35	A3A6-35
A3B6-45	A3A6-45
A3B6-47	A3A6-47
A3B6-53	A3A6-53
A3B6-55	A3A6-55
A3B7-15	A3A7-15
A3B7-17	A3A7-17
A3B7-23	A3A7-23
A3B7-25	A3A7-25
A3B7-33	A3A7-33
A3B7-35	A3A7-35
A3B7-45	A3A7-45
A3B7-47	A3A7-47
A3B7-53	A3A7-53
A3B7-55	A3A7-55

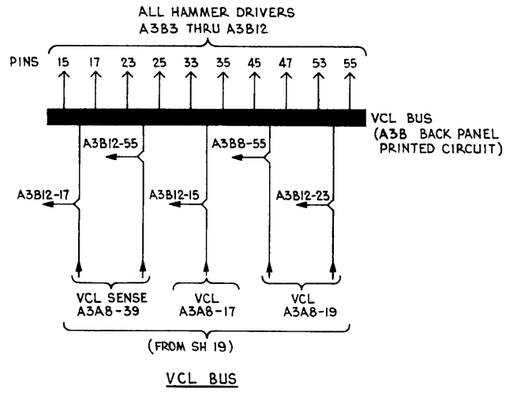


CIRCUIT CARD LOCATION:
A3A1 TO A3A12
(MODEL 2440 ONLY,
ELECTRONICS GATE ASSEMBLY
A3, CARD CAGE A, SLOTS 1 TO 12)

LOGIC DIAGRAM SHEET 24

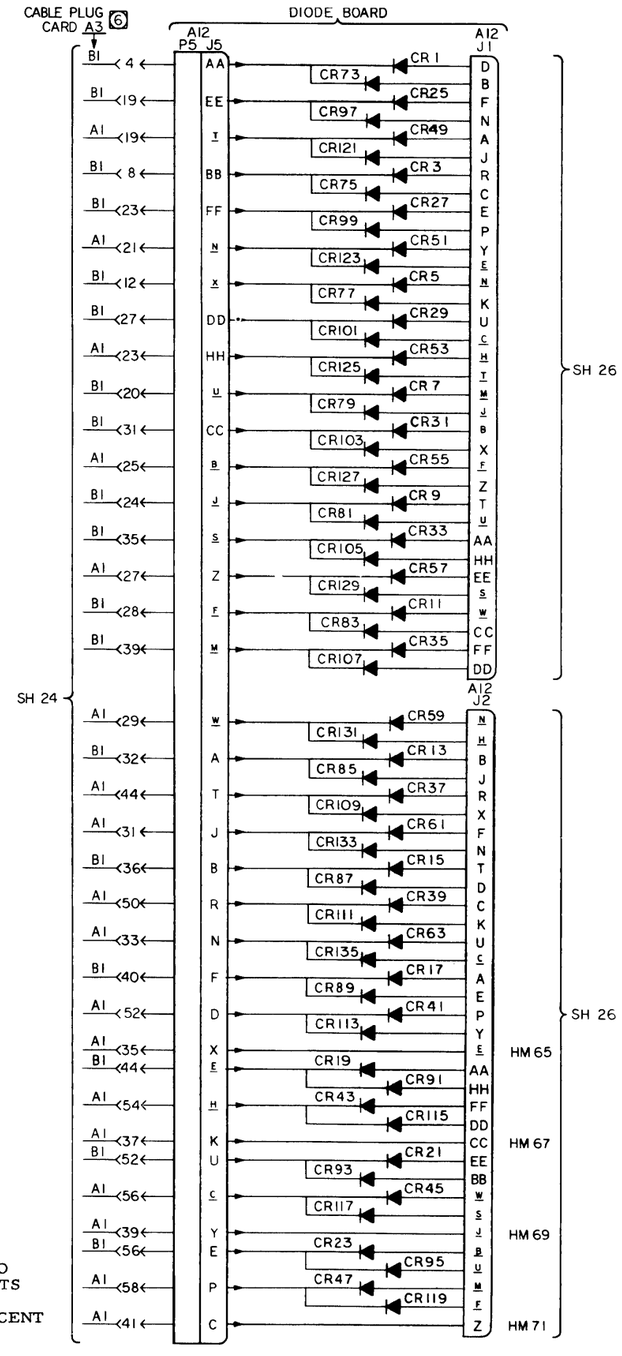
HAMMER DRIVER CIRCUITS
TYPICAL INTERCONNECTION
(MODEL 2440)

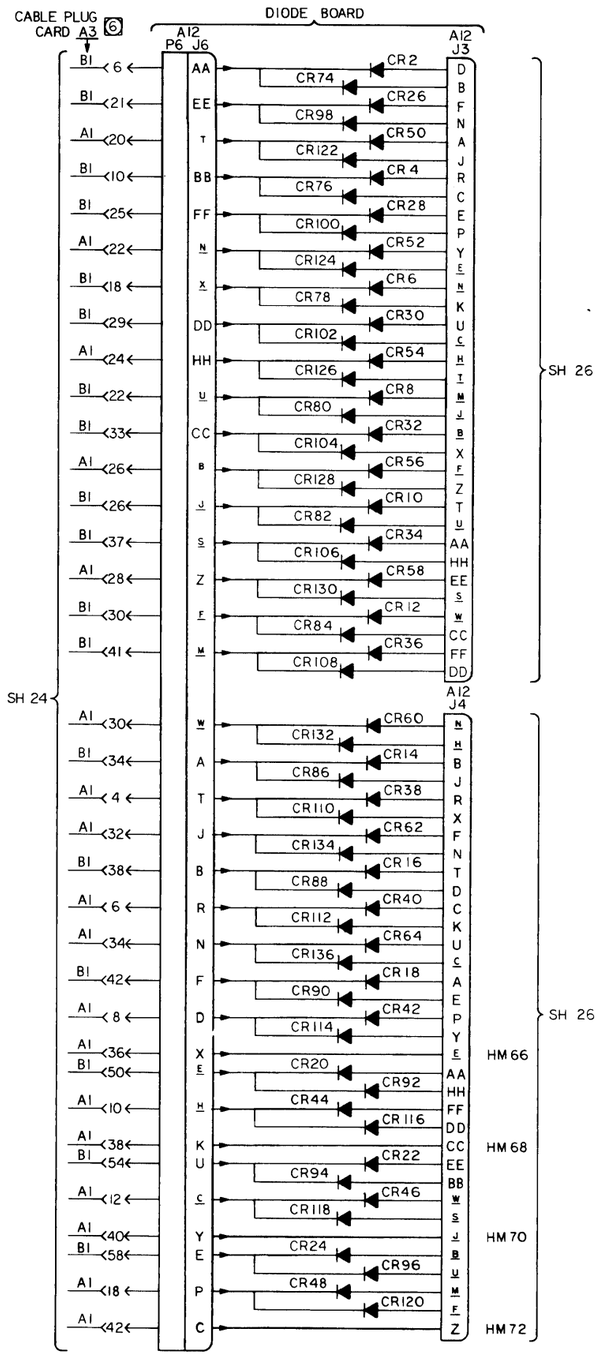




LOGIC DIAGRAM SHEET 24A

HAMMER DRIVER CIRCUITS, TYPICAL INTERCONNECTION (MODEL 2440)





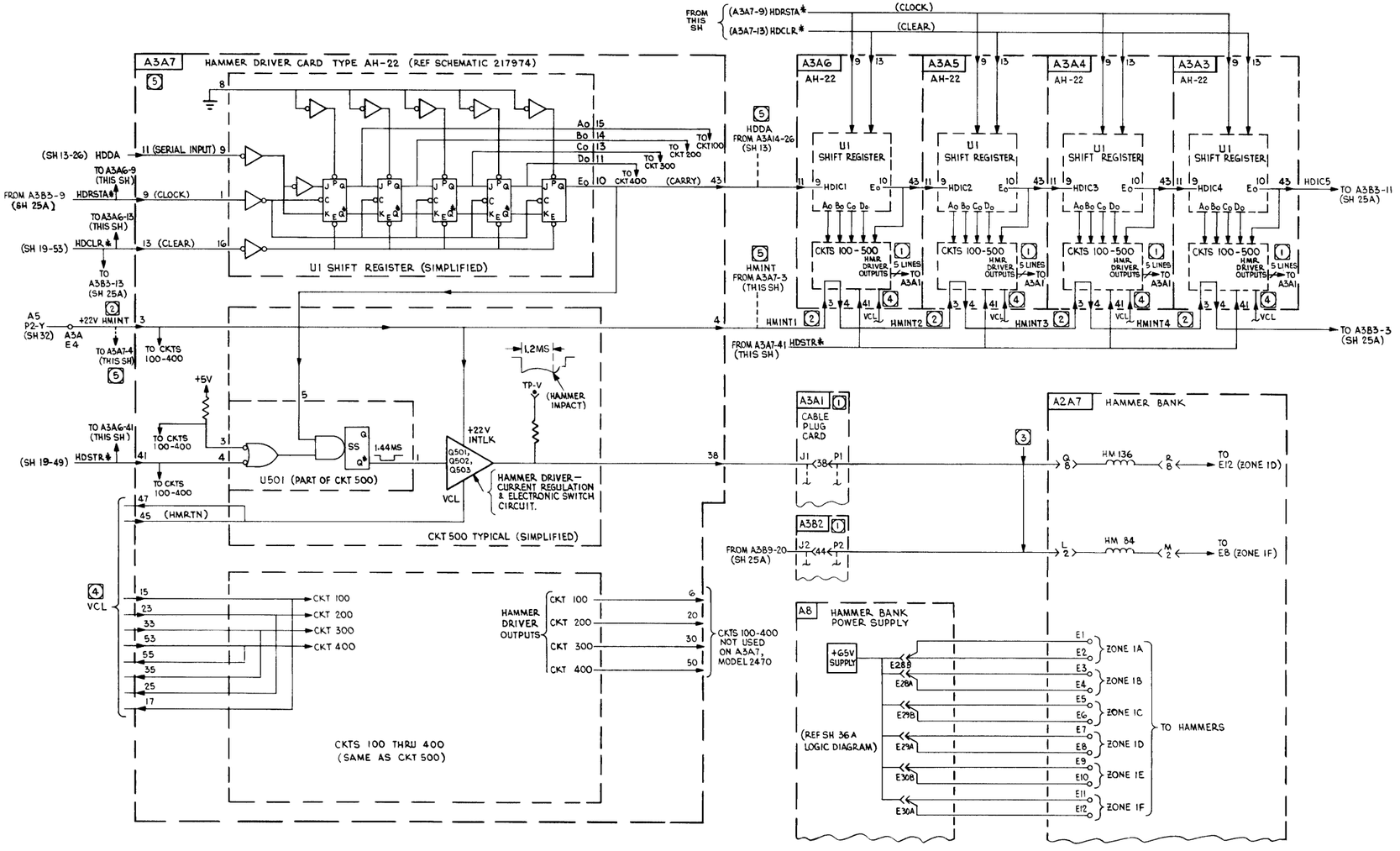
8. FOR SCHEMATIC SEE DWG NO. 217974, REV H
7. DIODE REFERENCE DESIGNATIONS CORRESPOND TO HAMMER NUMBERS (FOR EXAMPLE, CR73 CONNECTS TO HAMMER NO. 73).
6. SOURCE IS A3A1 (J1) OR A3B1 (J1), AS NOTED ADJACENT TO EACH PIN.
5. REF DES NOT USED: CR65 THRU CR72.
4. ASSEMBLY DRAWING NUMBER 230545, REV C
3. INTERPRET ELECTRONIC SYMBOLS PER USAS Y32.2.
2. INTERPRET REFERENCE DESIGNATIONS PER USAS Y32.16.
1. ALL DIODES ARE 800095-001.

NOTES: UNLESS OTHERWISE SPECIFIED

DIODE BOARD LOCATION: A12
(MODEL 2440 ONLY,
DIODE BOARD ASSEMBLY A12)

LOGIC DIAGRAM SHEET 24B

DIODE BOARD,
HAMMER DRIVER CIRCUITS
(MODEL 2440)



4 TAB B
VCL INTERCONNECTION DATA (REF SH 25A, VCL BUS)

FROM	TO
A3B3-15	A3A3-15
A3B3-17	A3A3-17
A3B3-23	A3A3-23
A3B3-25	A3A3-25
A3B3-33	A3A3-33
A3B3-35	A3A3-35
A3B3-45	A3A3-45
A3B3-47	A3A3-47
A3B3-53	A3A3-53
A3B3-55	A3A3-55
A3B4-15	A3A4-15
A3B4-17	A3A4-17
A3B4-23	A3A4-23
A3B4-25	A3A4-25
A3B4-33	A3A4-33
A3B4-35	A3A4-35
A3B4-45	A3A4-45
A3B4-47	A3A4-47
A3B4-53	A3A4-53
A3B4-55	A3A4-55
A3B5-15	A3A5-15
A3B5-17	A3A5-17
A3B5-23	A3A5-23
A3B5-25	A3A5-25
A3B5-33	A3A5-33
A3B5-35	A3A5-35
A3B5-45	A3A5-45
A3B5-47	A3A5-47
A3B5-53	A3A5-53
A3B5-55	A3A5-55
A3B6-15	A3A6-15
A3B6-17	A3A6-17
A3B6-23	A3A6-23
A3B6-25	A3A6-25
A3B6-33	A3A6-33
A3B6-35	A3A6-35
A3B6-45	A3A6-45
A3B6-47	A3A6-47
A3B6-53	A3A6-53
A3B6-55	A3A6-55
A3B7-15	A3A7-15
A3B7-17	A3A7-17
A3B7-23	A3A7-23
A3B7-25	A3A7-25
A3B7-33	A3A7-33
A3B7-35	A3A7-35
A3B7-45	A3A7-45
A3B7-47	A3A7-47
A3B7-53	A3A7-53
A3B7-55	A3A7-55

7. FOR SCHEMATIC SEE DWG NO. 217974, REV H
6. INTEGRATED CIRCUITS ARE AS FOLLOWS

REFERENCE DESIGNATORS	PART NO. AH-22
U1	800638-001
U101, U201, U301, U401, U501	800491-001

FOR COMPLETE IC PIN ASSIGNMENTS SEE LOADING DIAGRAMS IN APPENDIX A

(5) AH-22 CARD IS INSTALLED IN A3A7 ONLY FOR PRINTERS WITH 136 COLUMN OPTION. DASHED LINES SHOW SIGNAL INTERCONNECTION FOR STANDARD 132 COLUMN PRINTERS.

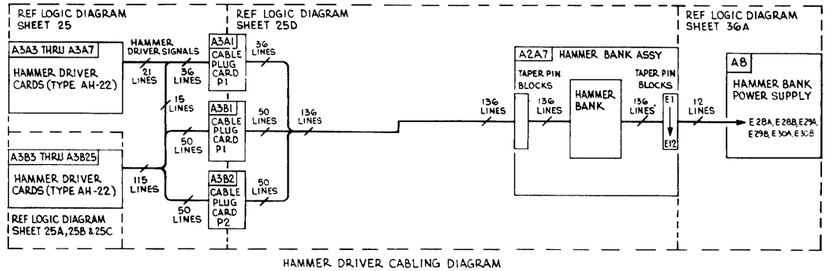
(4) REFER TO TABULAR LISTING FOR VCL INTERCONNECTION DATA.

(3) REFER TO LOGIC DIAGRAM SHEET 26 FOR INTERCONNECTION OF ALL HAMMERS.

(2) +22V HMINT (HAMMER INTERLOCK) SUPPLY IS CONNECTED IN SERIES THROUGH AN INTERNAL CONNECTION ON AH-22 CARD TYPES. REMOVAL OF AN AH-22 CARD RESULTS IN AN OPEN SUPPLY TO CARDS IN SERIES-STRING FOLLOWING IT.

(1) REFER TO LOGIC DIAGRAM 25D FOR INTERCONNECTION OF ALL HAMMER DRIVER CIRCUITS TO CABLE PLUG CARDS A3A1 (P1), A3B1 (P1) AND A3B2 (P2).

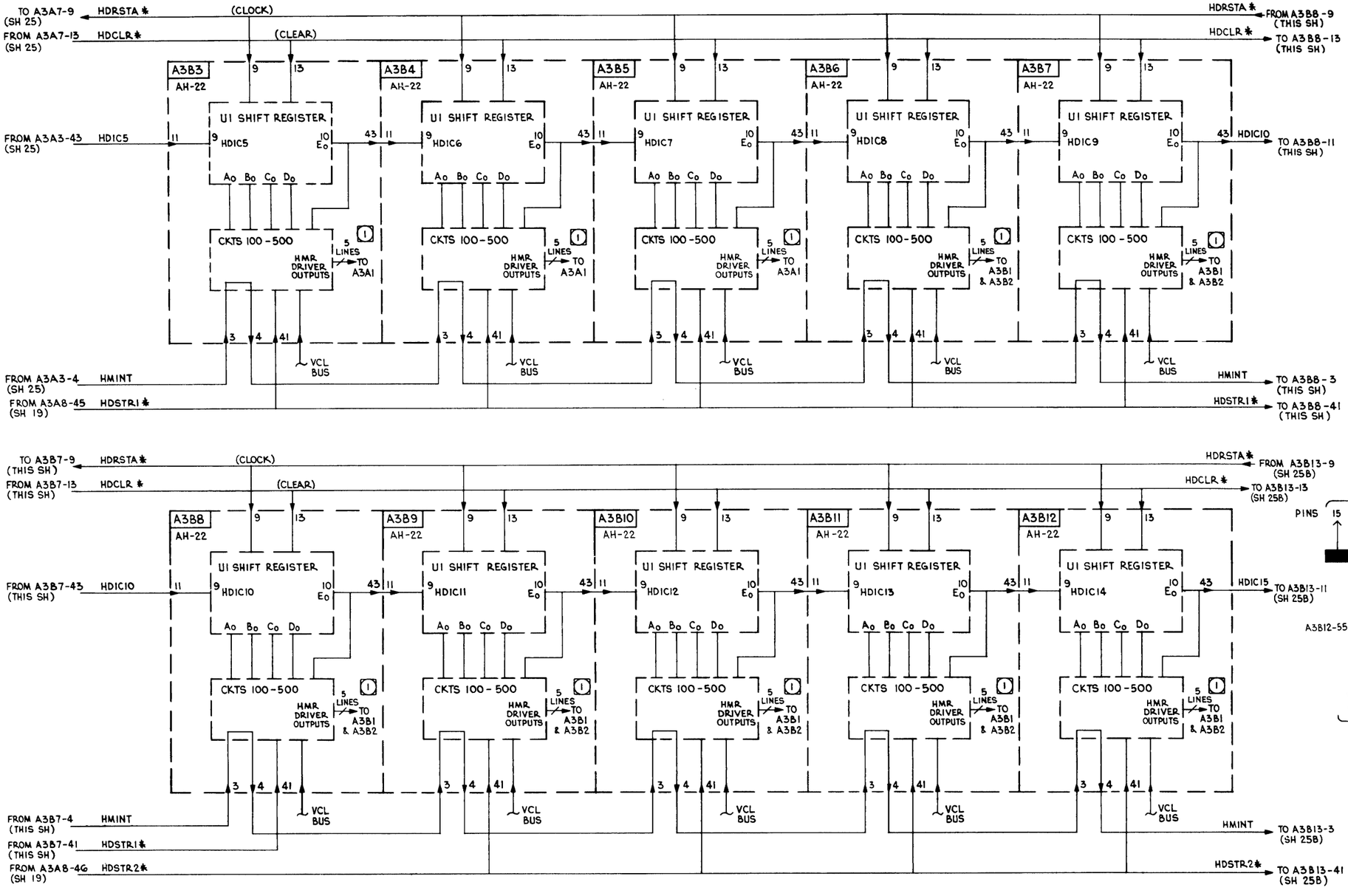
NOTES: UNLESS OTHERWISE SPECIFIED



HAMMER DRIVER CABLING DIAGRAM

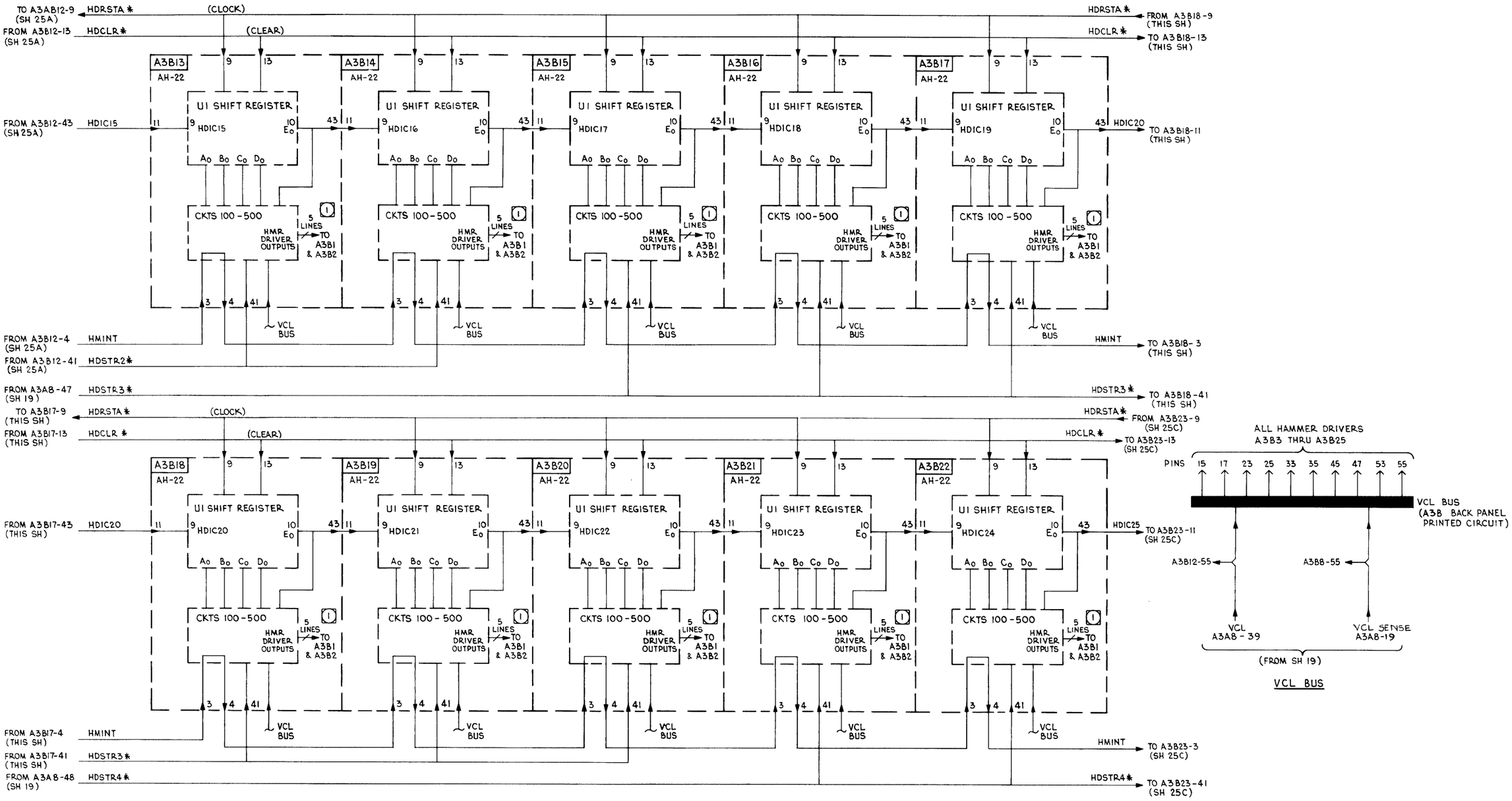
LOGIC DIAGRAM SHEET 25

AH-22
HAMMER DRIVER CIRCUITS, TYPICAL INTERCONNECTION (MODEL 2470)



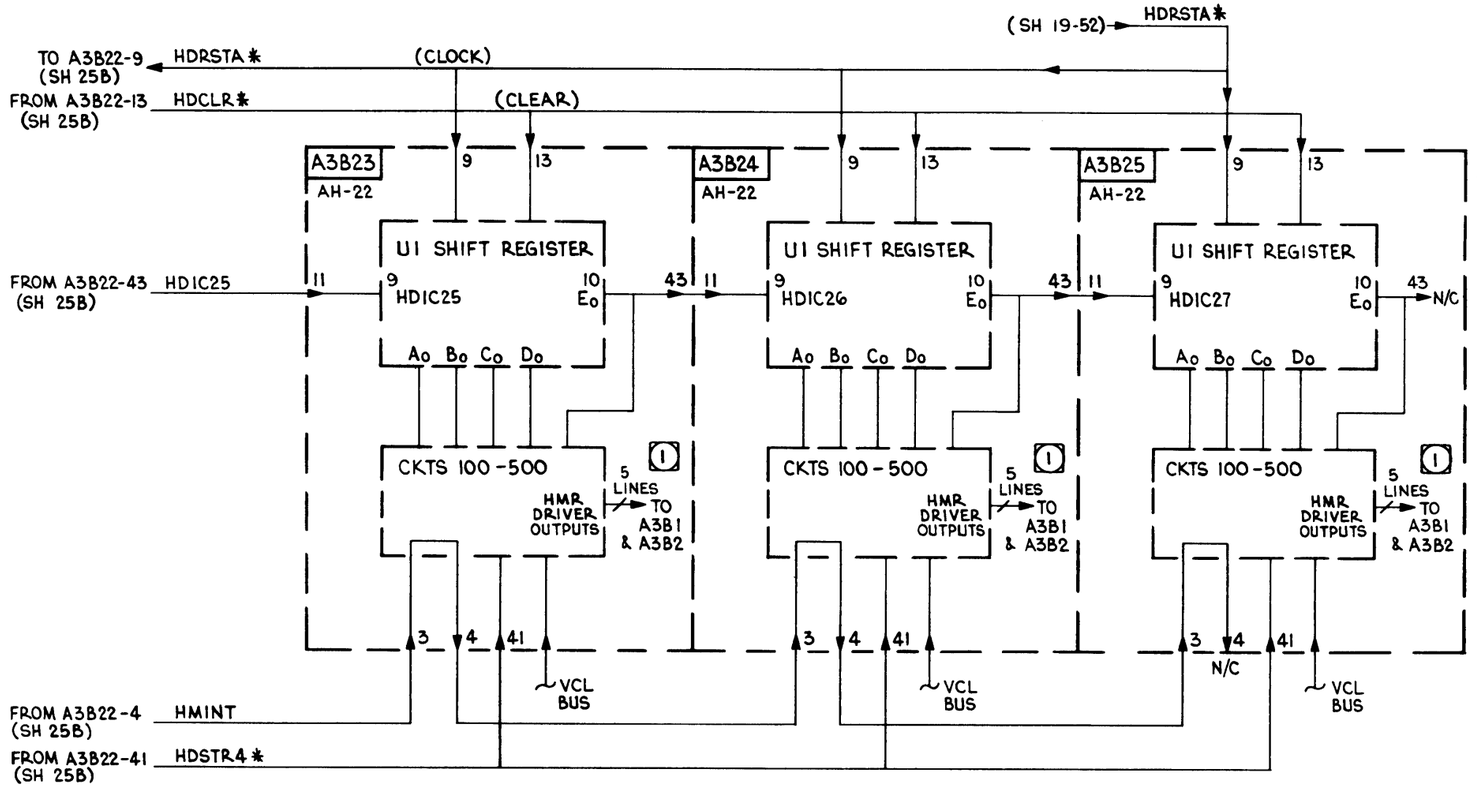
LOGIC DIAGRAM SHEET 25A

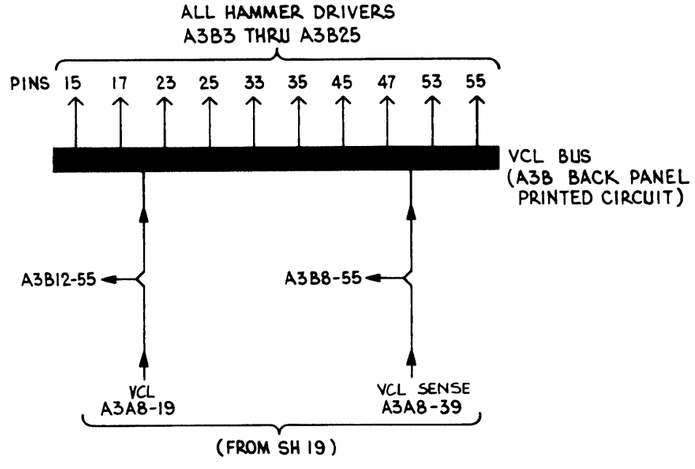
HAMMER DRIVER CIRCUITS, TYPICAL INTERCONNECTION (MODEL 2470 ONLY)



LOGIC DIAGRAM SHEET 25B

HAMMER DRIVER CIRCUITS, TYPICAL INTERCONNECTION (MODEL 2470 ONLY)





VCL BUS

LOGIC DIAGRAM SHEET 25C

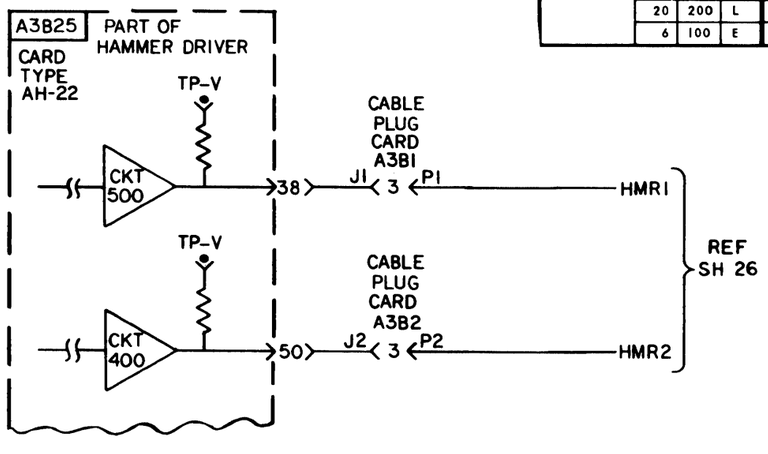
HAMMER DRIVER CIRCUITS, TYPICAL INTERCONNECTION (MODEL 2470 ONLY)

FROM HAMMER DRIVER CARD TYPE AH-22				TO CABLE PLUG CARD A3				HAMMER
LOCATION	PIN NO.	CKT NO.	TP	REF DES	PIN NO.			
A3B4	38	500	V	A1	8			106
	50	400	Y	A1	9			107
	30	300	R	A1	10			108
	20	200	L	A1	11			109
	6	100	E	A1	12			110
A3B3	38	500	V	A1	13			111
	50	400	Y	A1	14			112
	40	300	R	A1	15			113
	30	200	L	A1	16			114
	6	100	E	A1	17			115
A3A3	38	500	V	A1	18			116
	50	400	Y	A1	19			117
	30	300	R	A1	20			118
	20	200	L	A1	21			119
	6	100	E	A1	22			120
A3A4	38	500	V	A1	23			121
	50	400	Y	A1	24			122
	30	300	R	A1	25			123
	20	200	L	A1	26			124
	6	100	E	A1	27			125
A3A5	38	500	V	A1	28			126
	50	400	Y	A1	29			127
	30	300	R	A1	30			128
	20	200	L	A1	31			129
	6	100	E	A1	32			130
A3A6	38	500	V	A1	33			131
	50	400	Y	A1	34			132
	30	300	R	A1	35			133
	20	200	L	A1	36			134
	6	100	E	A1	37			135
A3A7	38	500	V	A1	38			136

FROM HAMMER DRIVER CARD TYPE AH-22				TO CABLE PLUG CARD A3				HAMMER
LOCATION	PIN NO.	CKT NO.	TP	REF DES	PIN NO.			
A3B11	38	500	V	B1	38			71
	50	400	Y	B2	38			72
	30	300	R	B1	39			73
	20	200	L	B2	39			74
	6	100	E	B1	40			75
A3B10	38	500	V	B2	40			76
	50	400	Y	B1	41			77
	30	300	R	B2	41			78
	20	200	L	B1	42			79
	6	100	E	B2	42			80
A3B9	38	500	V	B1	43			81
	50	400	Y	B2	43			82
	30	300	R	B1	44			83
	20	200	L	B2	44			84
	6	100	E	B1	45			85
A3B8	38	500	V	B2	45			86
	50	400	Y	B1	46			87
	30	300	R	B2	46			88
	20	200	L	B1	47			89
	6	100	E	B2	47			90
A3B7	38	500	V	B1	48			91
	50	400	Y	B2	48			92
	30	300	R	B1	49			93
	20	200	L	B2	49			94
	6	100	E	B1	50			95
A3B6	38	500	V	B2	50			96
	50	400	Y	B1	51			97
	30	300	R	B2	51			98
	20	200	L	B1	52			99
	6	100	E	B2	52			100
A3B5	38	500	V	A1	3			101
	50	400	Y	A1	4			102
	30	300	R	A1	5			103
	20	200	L	A1	6			104
	6	100	E	A1	7			105

FROM HAMMER DRIVER CARD TYPE AH-22				TO CABLE PLUG CARD A3				HAMMER
LOCATION	PIN NO.	CKT NO.	TP	REF DES	PIN NO.			
A3B18	38	500	V	B2	20			36
	50	400	Y	B1	21			37
	30	300	R	B2	21			38
	20	200	L	B1	22			39
	6	100	E	B2	22			40
A3B17	38	500	V	B1	23			41
	50	400	Y	B2	23			42
	30	300	R	B1	24			43
	20	200	L	B2	24			44
	6	100	E	B1	25			45
A3B16	38	500	V	B2	25			46
	50	400	Y	B1	26			47
	30	300	R	B2	26			48
	20	200	L	B1	27			49
	6	100	E	B2	27			50
A3B15	38	500	V	B1	28			51
	50	400	Y	B2	28			52
	30	300	R	B1	29			53
	20	200	L	B2	29			54
	6	100	E	B1	30			55
A3B14	38	500	V	B2	30			56
	50	400	Y	B1	31			57
	30	300	R	B2	31			58
	20	200	L	B1	32			59
	6	100	E	B2	32			60
A3B13	38	500	V	B1	33			61
	50	400	Y	B2	33			62
	30	300	R	B1	34			63
	20	200	L	B2	34			64
	6	100	E	B1	35			65
A3B12	38	500	V	B2	35			66
	50	400	Y	B1	36			67
	30	300	R	B2	36			68
	20	200	L	B1	37			69
	6	100	E	B2	37			70

FROM HAMMER DRIVER CARD TYPE AH-22				TO CABLE PLUG CARD A3				HAMMER
LOCATION	PIN NO.	CKT NO.	TP	REF DES	PIN NO.			
A3B25	38	500	V	B1	3			1
	50	400	Y	B2	3			2
	30	300	R	B1	4			3
	20	200	L	B2	4			4
	6	100	E	B1	5			5
A3B24	38	500	V	B2	5			6
	50	400	Y	B1	6			7
	30	300	R	B2	6			8
	20	200	L	B1	7			9
	6	100	E	B2	7			10
A3B23	38	500	V	B1	8			11
	50	400	Y	B2	8			12
	30	300	R	B1	9			13
	20	200	L	B2	9			14
	6	100	E	B1	10			15
A3B22	38	500	V	B2	10			16
	50	400	Y	B1	11			17
	30	300	R	B2	11			18
	20	200	L	B1	12			19
	6	100	E	B2	12			20
A3B21	38	500	V	B1	13			21
	50	400	Y	B2	13			22
	30	300	R	B1	14			23
	20	200	L	B2	14			24
	6	100	E	B1	15			25
A3B20	38	500	V	B2	15			26
	50	400	Y	B1	16			27
	30	300	R	B2	16			28
	20	200	L	B1	17			29
	6	100	E	B2	17			30
A3B19	38	500	V	B1	18			31
	50	400	Y	B2	18			32
	30	300	R	B1	19			33
	20	200	L	B2	19			34
	6	100	E	B1	20			35



TYPICAL EXAMPLES OF INTERCONNECTION INFORMATION SHOWN IN TABULAR LISTINGS

LOGIC DIAGRAM SHEET 25D

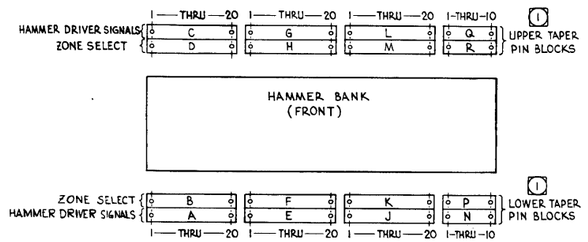
HAMMER DRIVER CIRCUITS, TYPICAL INTERCONNECTION (MODEL 2470 ONLY)

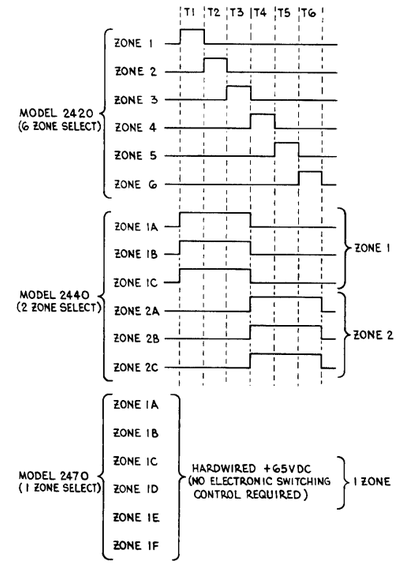
TABLE A - INTERCONNECTING INFORMATION, HAMMER BANK A7

TAPER PIN BLOCKS (ALL MODELS)

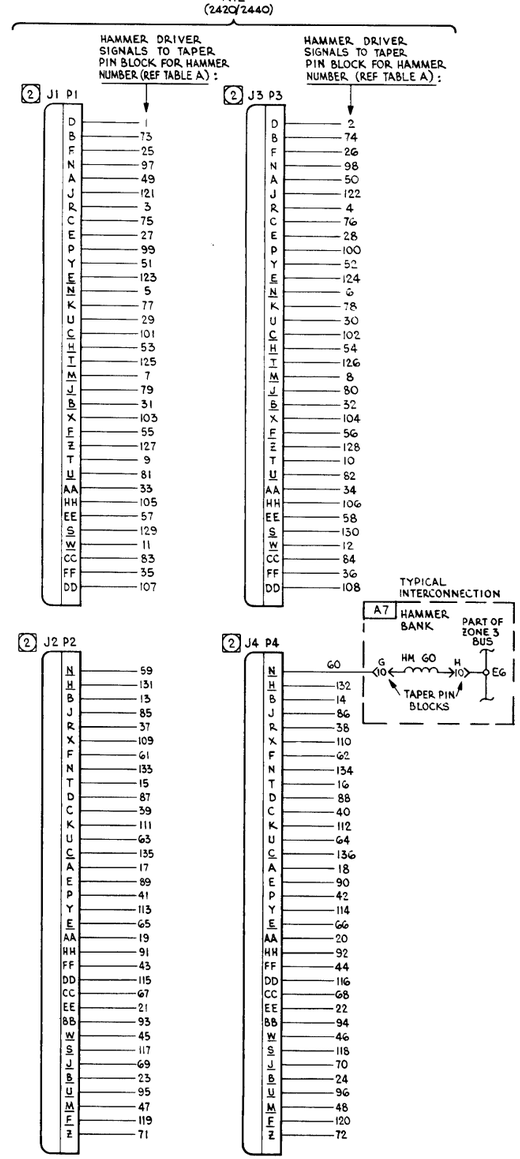
HAMMER NO.	HAMMER DRIVER SIGNAL (1) TAPER PIN BLOCK	HAMMER DRIVER SIGNAL TERMINAL NO.	ZONE SELECT CONTROL (1) TAPER PIN BLOCK	ZONE SELECT CONTROL (4) BUS	ZONE SELECT CONTROL TERMINAL NO.	(3) ZONE MODEL 2420	(3) ZONE MODEL 2440	(3) ZONE MODEL 2470
1	A	1	B	E1	1	1	1	ONE ZONE
3		2			2			
5		3			3			
7		4			4			
9		5			5			
11		6			6			
13		7			7			
15		8			8			
17		9			9			
19		10			10			
21		11			11			
23		12		E1	12			
25		13		E3	13	2		
27		14			14			
29		15			15			
31		16			16			
33		17			17			
35		18			18			
37		19			19			
39	A	20	B		20			
41	E	1	F		1	3		
43		2			2			
45		3			3			
47		4		E3	4			
49		5		E5	5			
51		6			6			
53		7			7			
55		8			8			
57		9			9			
59		10			10			
61		11			11			
63		12			12			
65		13			13			
67		14			14			
69		15			15			
71		16		E5	16			
73		17		E7	17	4		
75		18			18			
77		19			19			
79	E	20	F		20			
81	J	1	K		1	5		
83		2			2			
85		3			3			
87		4			4			
89		5			5			
91		6			6			
93		7			7			
95		8		E7	8			
97		9		E9	9	6		
99		10			10			
101		11			11			
103		12			12			
105		13			13			
107		14			14			
109		15			15			
111		16			16			
113		17			17			
115		18			18			
117		19			19			
119	J	20	K	E9	20			
121	N	1	P	E11	1	6		
123		2			2			
125		3			3			
127		4			4			
129		5			5			
131		6			6			
133		7			7			
135	N	8	P	E11	8			

HAMMER NO.	HAMMER DRIVER SIGNAL (1) TAPER PIN BLOCK	HAMMER DRIVER SIGNAL TERMINAL NO.	ZONE SELECT CONTROL (1) TAPER PIN BLOCK	ZONE SELECT CONTROL (4) BUS	ZONE SELECT CONTROL TERMINAL NO.
2	C	1	D	E2	1
4		2			2
6		3			3
8		4			4
10		5			5
12		6			6
14		7			7
16		8			8
18		9			9
20		10			10
22		11			11
24		12		E2	12
26		13		E4	13
28		14			14
30		15			15
32		16			16
34		17			17
36		18			18
38		19			19
40	C	20	D		20
42	G	1	H		1
44		2			2
46		3			3
48		4		E4	4
50		5		E6	5
52		6			6
54		7			7
56		8			8
58		9			9
60		10			10
62		11			11
64		12			12
66		13			13
68		14			14
70		15			15
72		16		E6	16
74		17		E8	17
76		18			18
78		19			19
80	G	20	H		20
82	L	1	M		1
84		2			2
86		3			3
88		4			4
90		5			5
92		6			6
94		7			7
96		8		E8	8
98		9		E10	9
100		10			10
102		11			11
104		12			12
106		13			13
108		14			14
110		15			15
112		16			16
114		17			17
116		18			18
118		19			19
120	L	20	M	E10	20
122	Q	1	R	E12	1
124		2			2
126		3			3
128		4			4
130		5			5
132		6			6
134		7			7
136	Q	8	R	E12	8





(3) TIMING DIAGRAM A

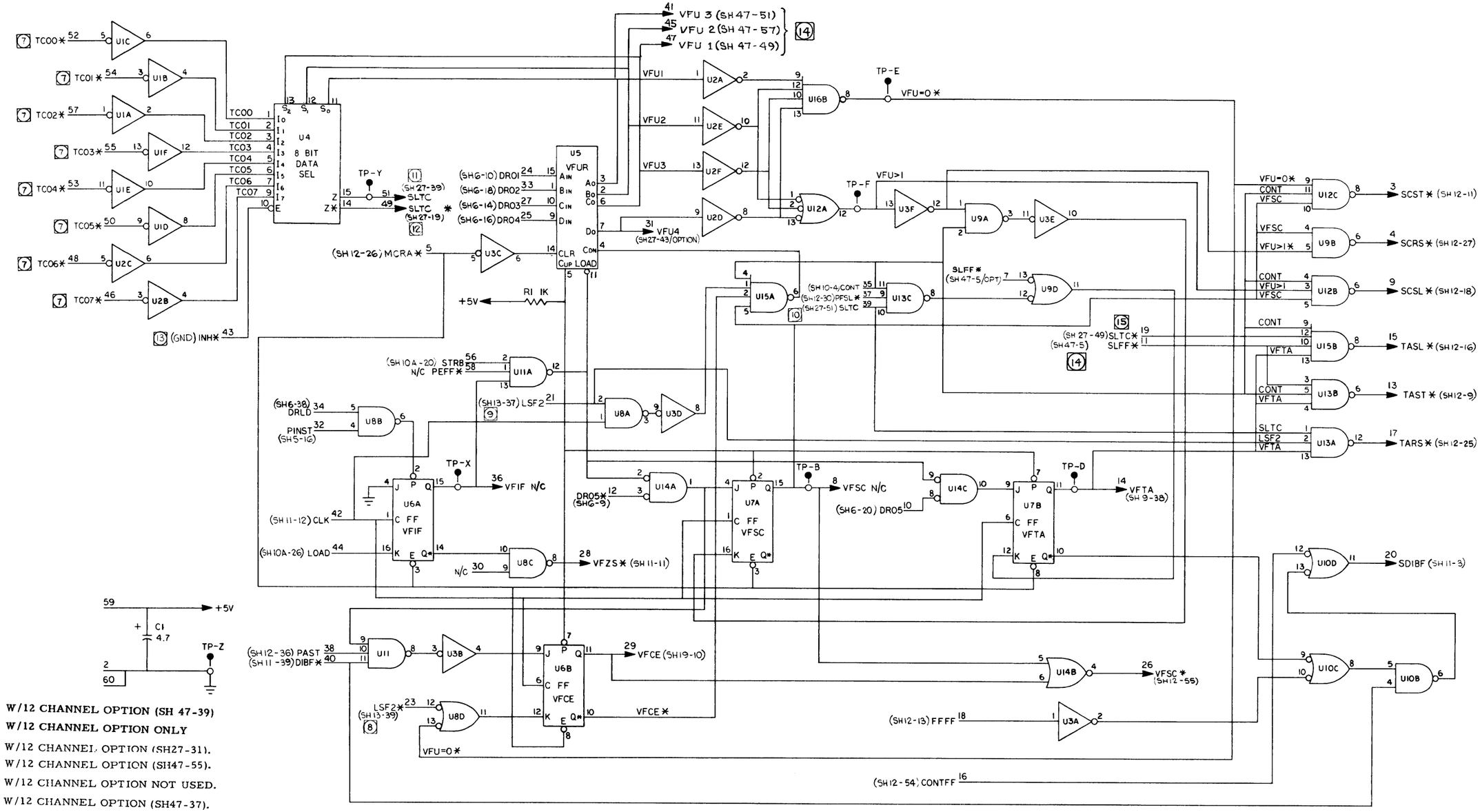


(4) EACH ZONE SELECT BUS IS CONNECTED INTERNALLY WITHIN TAPER PINE BLOCKS.
(3) TIMING DIAGRAM A - ZONE SELECTION COMPARISON (FOR INFORMATION ONLY).
(2) REF LOGIC DIAGRAM SHEETS: 23A, FOR MODEL 2420; 24B, FOR MODEL 2440; AND 25D, FOR MODEL 2470.
(1) THE LETTER-DESIGNATIONS A THROUGH Q ARE NOT ACTUALLY MARKED ON THE TAPER PIN BLOCKS, AND ARE ONLY USED IN THIS DRAWING FOR LOCATING TAPER PIN TERMINALS ASSOCIATED WITH ANY GIVEN HAMMER (REF TABLE A).

NOTES: UNLESS OTHERWISE SPECIFIED

LOGIC DIAGRAM SHEET 26

DIODE BOARD TO HAMMER BANK INTERCONNECTION (2420/2440)



15. W/12 CHANNEL OPTION (SH 47-39)
14. W/12 CHANNEL OPTION ONLY
13. W/12 CHANNEL OPTION (SH27-31).
12. W/12 CHANNEL OPTION (SH47-55).
11. W/12 CHANNEL OPTION NOT USED.
10. W/12 CHANNEL OPTION (SH47-37).
9. W/12 CHANNEL OPTION (SH47-35) LSF2D.
8. W/12 CHANNEL OPTION (SH47-33) LSF2D*.
7. MODEL 2420: SH38A
   MODELS 2440/2470: SH39
   W/12 CHANNEL OPTION, SH47 (TW00* THRU TW07*)
   ALL MODELS
6. FOR SCHEMATIC SEE DWG NO. 233129, REV F
5. ASSEMBLY DRAWING NUMBER 233125, REV D
4. INTERPRET ELECTRONIC SYMBOLS PER 850026.
3. INTERPRET REFERENCE DESIGNATIONS PER 850027.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS, 10%, 10 VOLTS.
1. ALL RESISTANCE VALUES ARE IN OHMS, 5%, 1/4 WATT.

NOTES: UNLESS OTHERWISE SPECIFIED

14. INTEGRATED CIRCUITS ARE AS FOLLOWS:

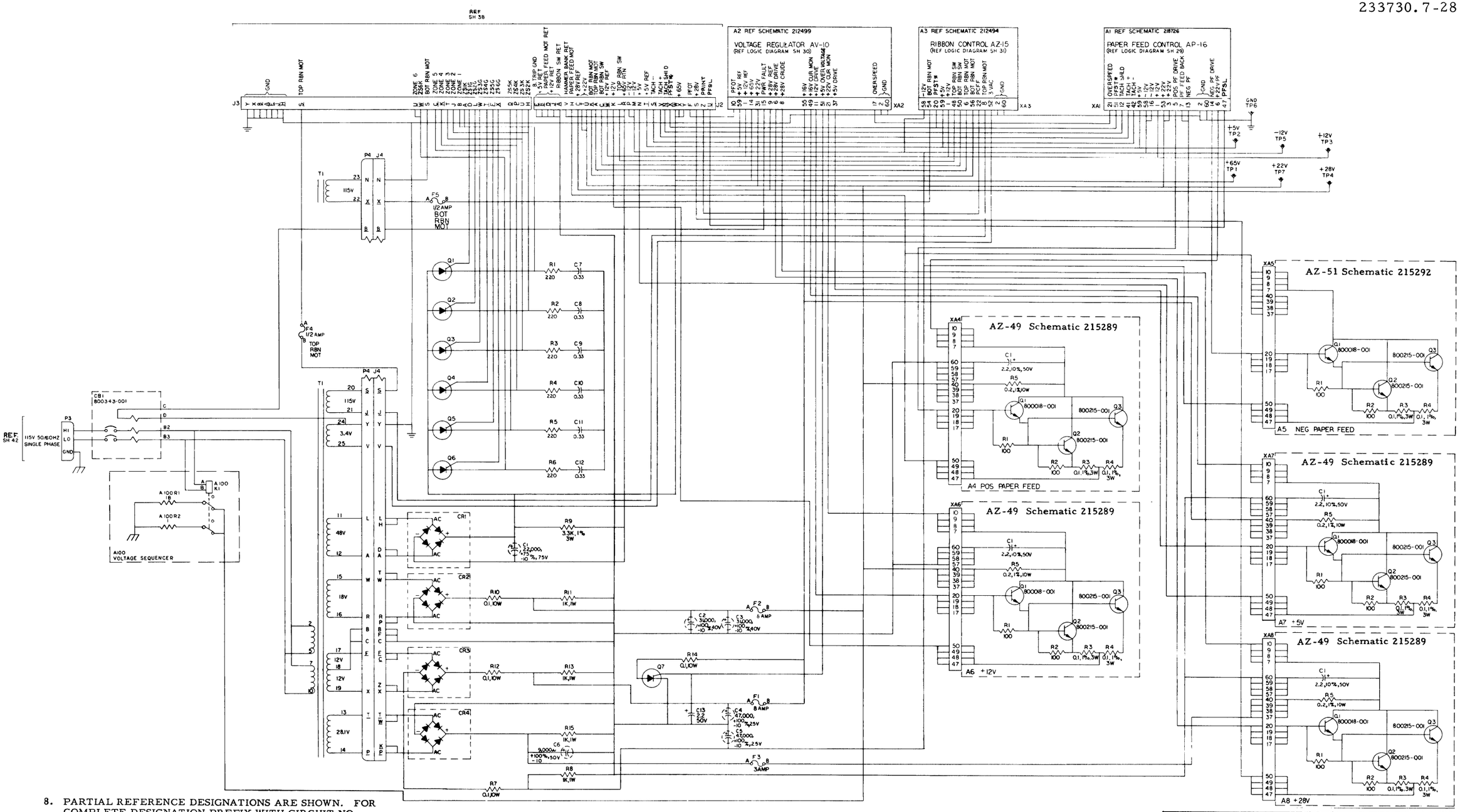
REFERENCE DESIGNATIONS	PART NO. AG-44
U1, U2, U3	800387-001
U4	800703-001
U5	800386-001
U6, U7	800081-001
U8, U9, U10	800024-001
U11, U12, U13	800023-001
U14	800080-001
U15, U16	800020-001

FOR COMPLETE IC PIN ASSIGNMENTS SEE LOADING DIAGRAMS IN APPENDIX A

CIRCUIT CARD LOCATION: A3A17
(ALL MODELS, ELECTRONICS GATE ASSEMBLY A3, CARD CAGE A, SLOT 17)

LOGIC DIAGRAM SHEET 27

AG-44
VERTICAL FORMAT UNIT
8 CHANNEL



8. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION PREFIX WITH CIRCUIT NO.
7. ASSEMBLY DRAWING NUMBER 214540, REV J
6. INTERPRET ELECTRONIC SYMBOLS PER USAS Y32.2.
5. INTERPRET REFERENCE DESIGNATIONS PER USAS Y32.16.
4. ALL SCRS ARE 800192-001.
3. ALL DIODES BRIDGES ARE 800516-001.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS, 10%, 100 VOLTS.
1. ALL RESISTANCE VALUES ARE IN OHMS, 5%, 1/4 WATT.

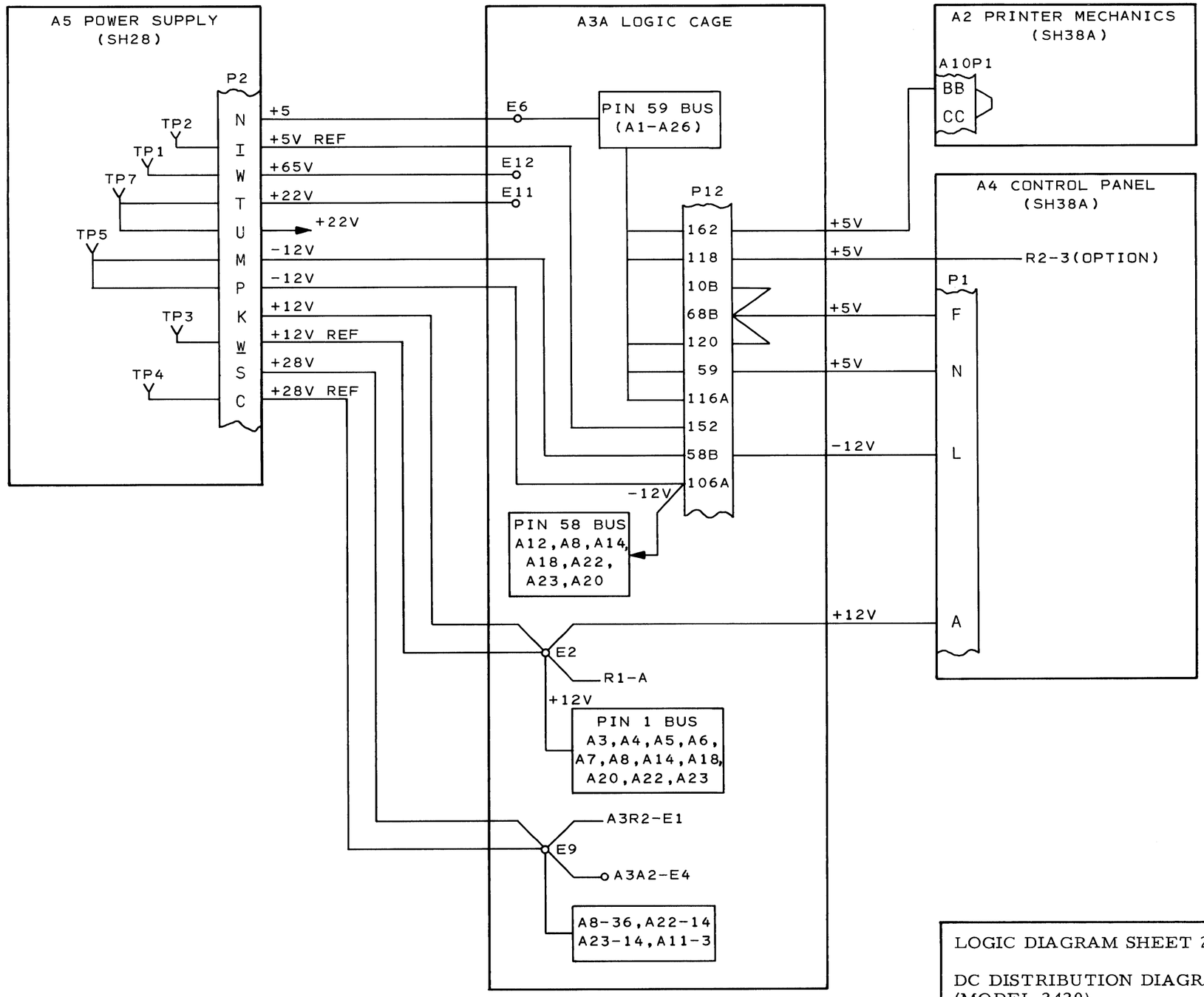
NOTES: UNLESS OTHERWISE SPECIFIED

11. FOR SCHEMATIC SEE DWG NO. 218728, REV E
10. ALL COMPONENTS EXCEPT CB1, T1 & A§ THRU A8 MOUNTED ON MOTHER BOARD ASSEMBLY NO. 215471-1.
9. THE FOLLOWING CONNECTOR PINS ARE NOT USED:
J2: B, D, E, J, F, H, M, P, R
J3: C, E, F, K, M, N, P, R, V, Z, M, N, R, V
J4: E, J, K, M, S, J, A, D, E, H, M, N, R, J, V

ASSEMBLY LOCATION: A5
(MODEL 2420)

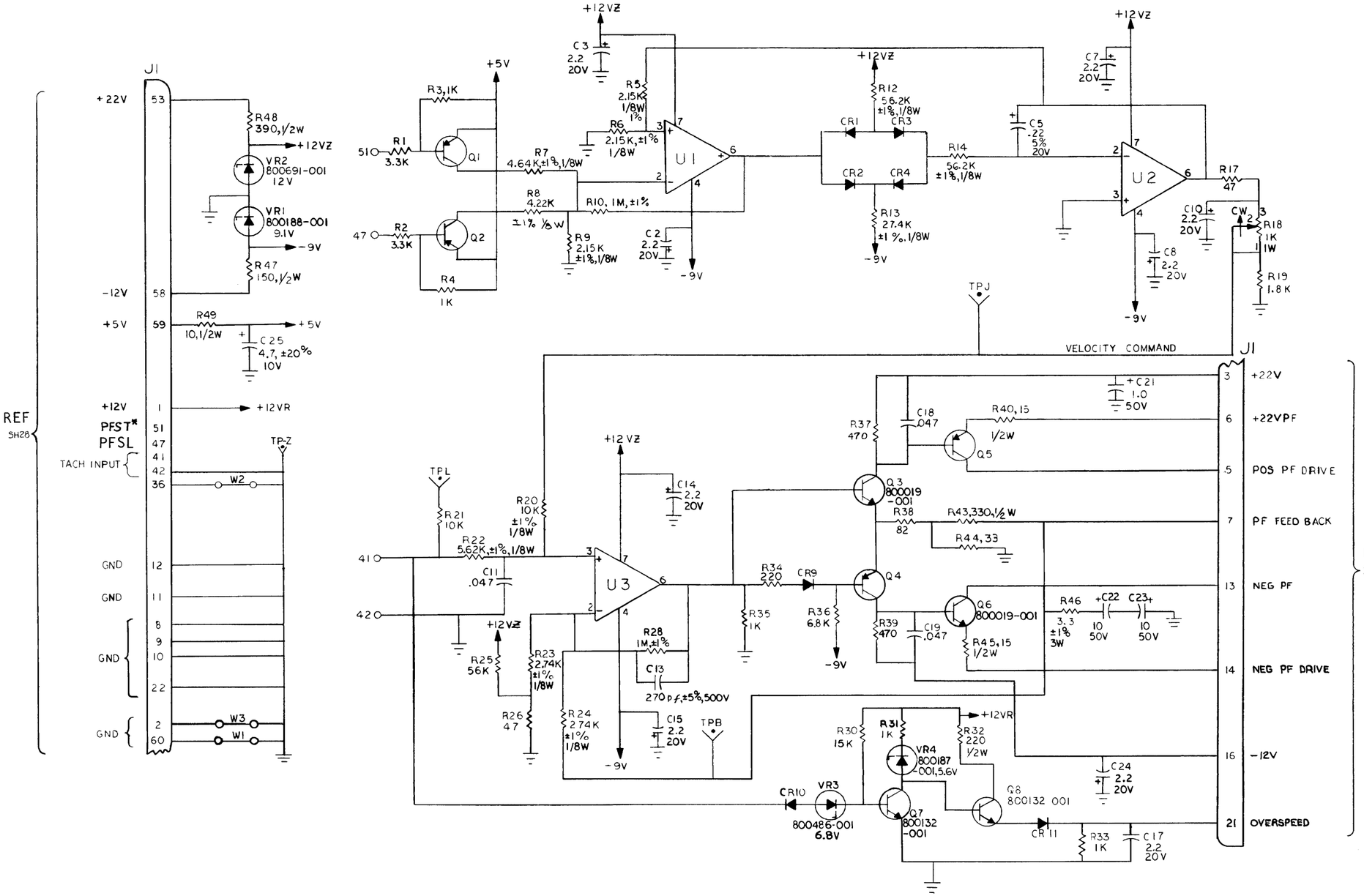
LOGIC DIAGRAM SHEET 28

POWER SUPPLY



LOGIC DIAGRAM SHEET 28A

DC DISTRIBUTION DIAGRAM
(MODEL 2420)



9. REFERENCE DESIGNATIONS NOT USED: R42 & C20.
8. THE FOLLOWING CONNECTOR PINS ARE NOT USED: 4, 15, 17, 18, 19, 20, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 37, 38, 39, 40, 43, 44, 45, 46, 48, 49, 50, 52. 54. 55, 56, 57
7. ASSEMBLY DRAWING NUMBER 218727, REV D
6. INTERPRET ELECTRONIC SYMBOLS PER USAS Y32.2.
5. INTERPRET REFERENCE DESIGNATIONS PER USAS Y32.16.
4. ALL TRANSISTORS ARE 800093-001.
3. ALL DIODES ARE 800516-001.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS, 10%, 100 VOLTS.
1. ALL RESISTANCE VALUES ARE IN OHMS, 5%, 1/4 WATT.

NOTES: UNLESS OTHERWISE SPECIFIED

11. FOR SCHEMATIC SEE DWG NO. 218726, REV F
10. INTEGRATED CIRCUITS ARE AS FOLLOWS:

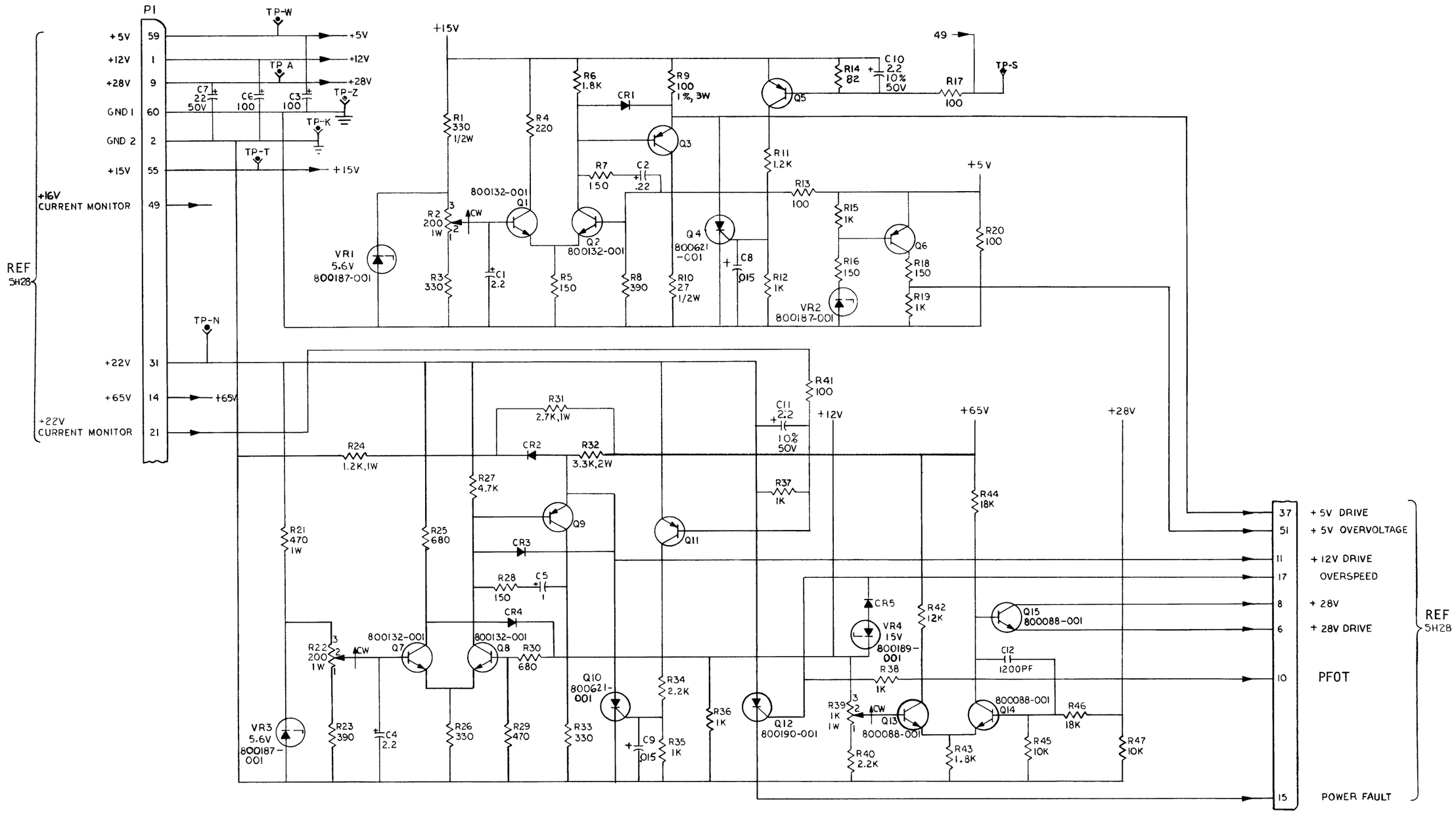
REFERENCE DESIGNATIONS	PART NO.
U1, U2, U3	800732-001

FOR COMPLETE IC PIN ASSIGNMENTS SEE LOADING DIAGRAMS IN APPENDIX A

CIRCUIT CARD LOCATION: A5A1
(MODEL 2420 ONLY, POWER SUPPLY ASSEMBLY A5, CARD CAGE SLOT A1)

LOGIC DIAGRAM SHEET 29

AP-16
PAPER FEED CONTROL



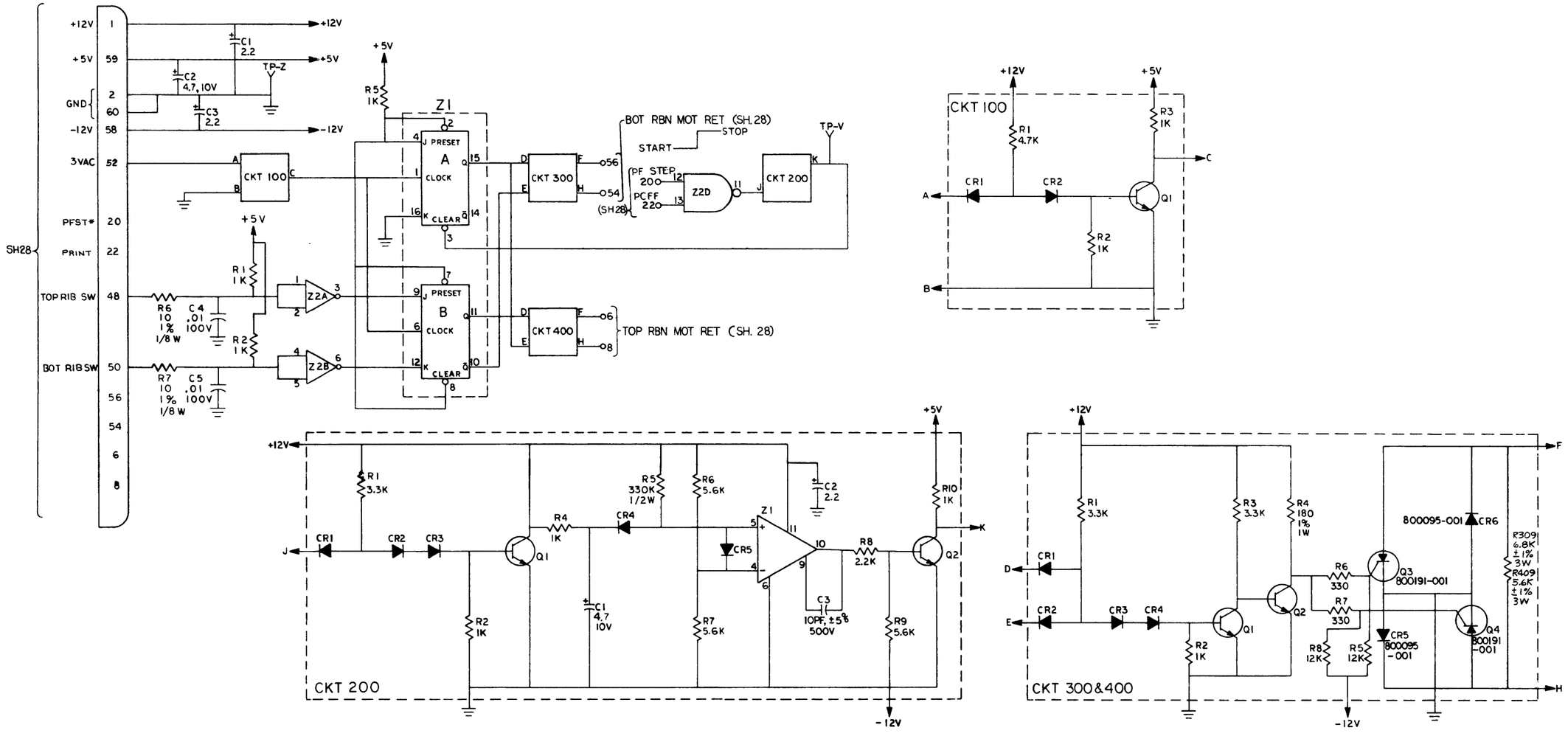
9. FOR SCHEMATIC SEE DWG NO. 212499, REV H
8. THE FOLLOWING CONNECTOR PINS ARE NOT USED: 3, 4, 5, 7, 12, 13, 16, 18, 19, 02, 22, 23, 24, 25, 26, 27, 28, 29, 30, 32, 33, 34, 35, 36, 38, 39, 40, 41, 42, 43, 44, 45, 46, 47, 48, 50, 52, 53, 54, 56, 57, 58
7. ASSEMBLY DRAWING NUMBER 212495, REV M
6. INTERPRET ELECTRONIC SYMBOLS PER 850026.
5. INTERPRET REFERENCE DESIGNATIONS PER 850027.
4. ALL TRANSISTORS ARE 800089-001.
3. ALL DIODES ARE 800093-001.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS, ± 10%, 20 VOLTS.
1. ALL RESISTANCE VALUES ARE IN OHMS, ± 5%, 1/4 WATT.

NOTES: UNLESS OTHERWISE SPECIFIED

CIRCUIT CARD LOCATION: A5A2
(MODEL 2420 ONLY,
POWER SUPPLY ASSEMBLY
A5, CARD CAGE SLOT A2)

LOGIC DIAGRAM SHEET 30

AV-10
VOLTAGE REGULATOR



9. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION, PREFIX WITH CIRCUIT NO. (I. E. R101).

8. THE FOLLOWING CONNECTOR PINS ARE NOT USED: 3, 4, 5, 7, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 21, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46, 47, 51, 52, 53, 55, 57
7. ASSEMBLY DRAWING NUMBER 212490, REV G
6.
5.
4. ALL TRANSISTORS ARE 800132-001
3. ALL DIODES ARE 800093-001.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS, ± 10%, 20 VOLTS.
1. ALL RESISTANCE VALUES ARE IN OHMS, ± 5%, 1/4 WATT.

NOTES: UNLESS OTHERWISE SPECIFIED

11. FOR SCHEMATIC SEE DWG NO. 212494, REV G
10. INTEGRATED CIRCUITS ARE AS FOLLOWS:

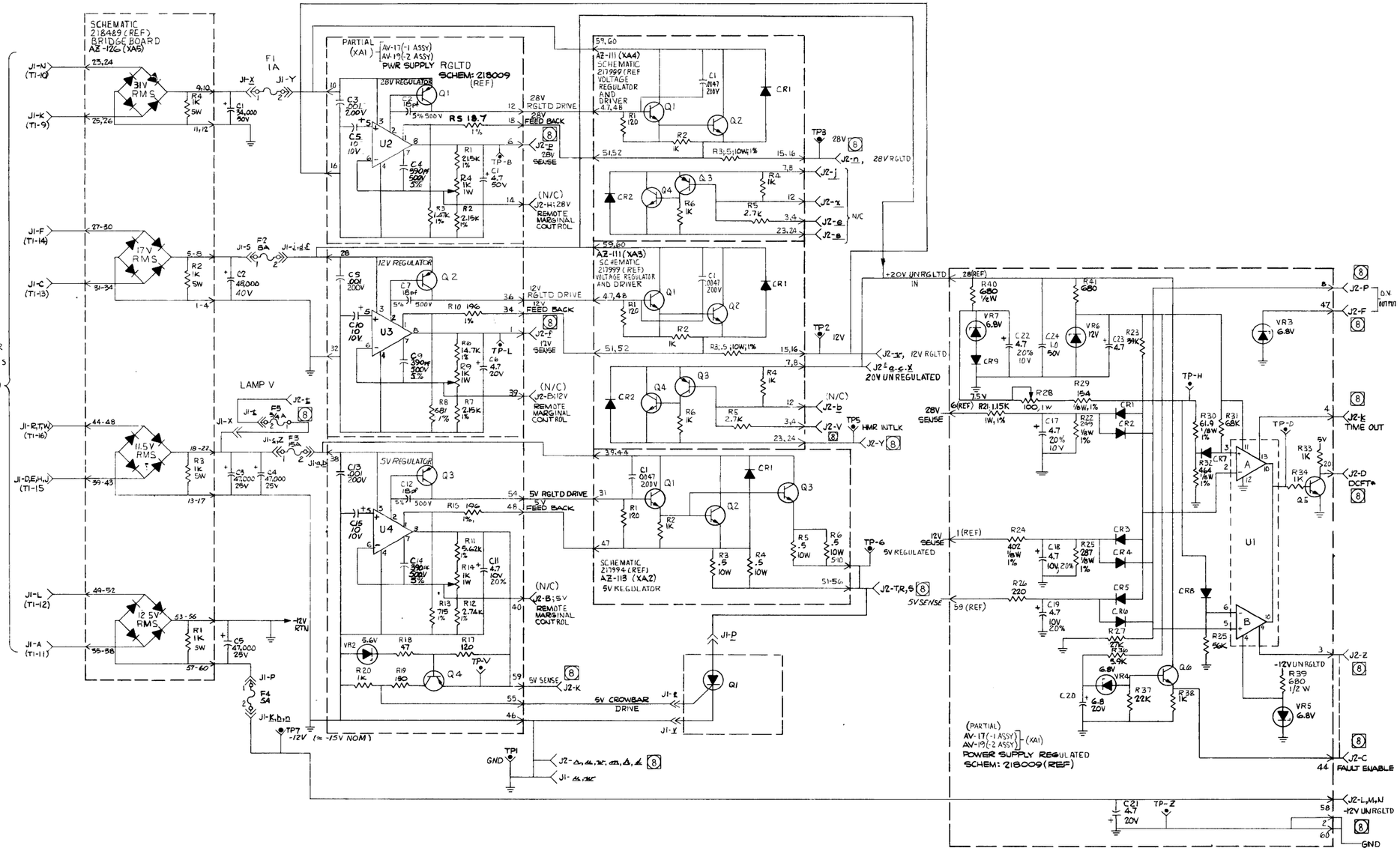
REFERENCE DESIGNATIONS	PART NO.
Z1	800081-001
Z2	800024-001
Z201	800195-001

FOR COMPLETE IC PIN ASSIGNMENTS SEE LOADING DIAGRAMS IN APPENDIX A

CIRCUIT CARD LOCATION: A5A3 (MODEL 2420 ONLY, POWER SUPPLY ASSEMBLY A5, CARD CAGE SLOT A3)

LOGIC DIAGRAM SHEET 31

AZ-15
RIBBON CONTROL



8 REFER TO LOGIC DIAGRAM SHEET 39A (232488).

7. CIRCUITS AV-17, AV-19, AZ-111, AZ-113, AZ-126 ARE FOR REFERENCE ONLY. REFER TO INDIVIDUAL SCHEMATICS FOR CURRENT CIRCUIT INFORMATION.
6. INTERPRET ELECTRONIC SYMBOLS PER 850026.
5. INTERPRET REFERENCE DESIGNATIONS PER 850027.
4. ALL TRANSISTORS ARE LISTED ON 218424.
3. ALL DIODES ARE LISTED ON 218424.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS, 10%, 25 VOLTS.
1. ALL RESISTANCE VALUES ARE IN OHMS, 5%, 1/4 WATT.

NOTES: UNLESS OTHERWISE SPECIFIED

10. FOR SCHEMATIC SEE DWG NO. 218424, REV V
9. INTEGRATED CIRCUITS ARE AS FOLLOWS:

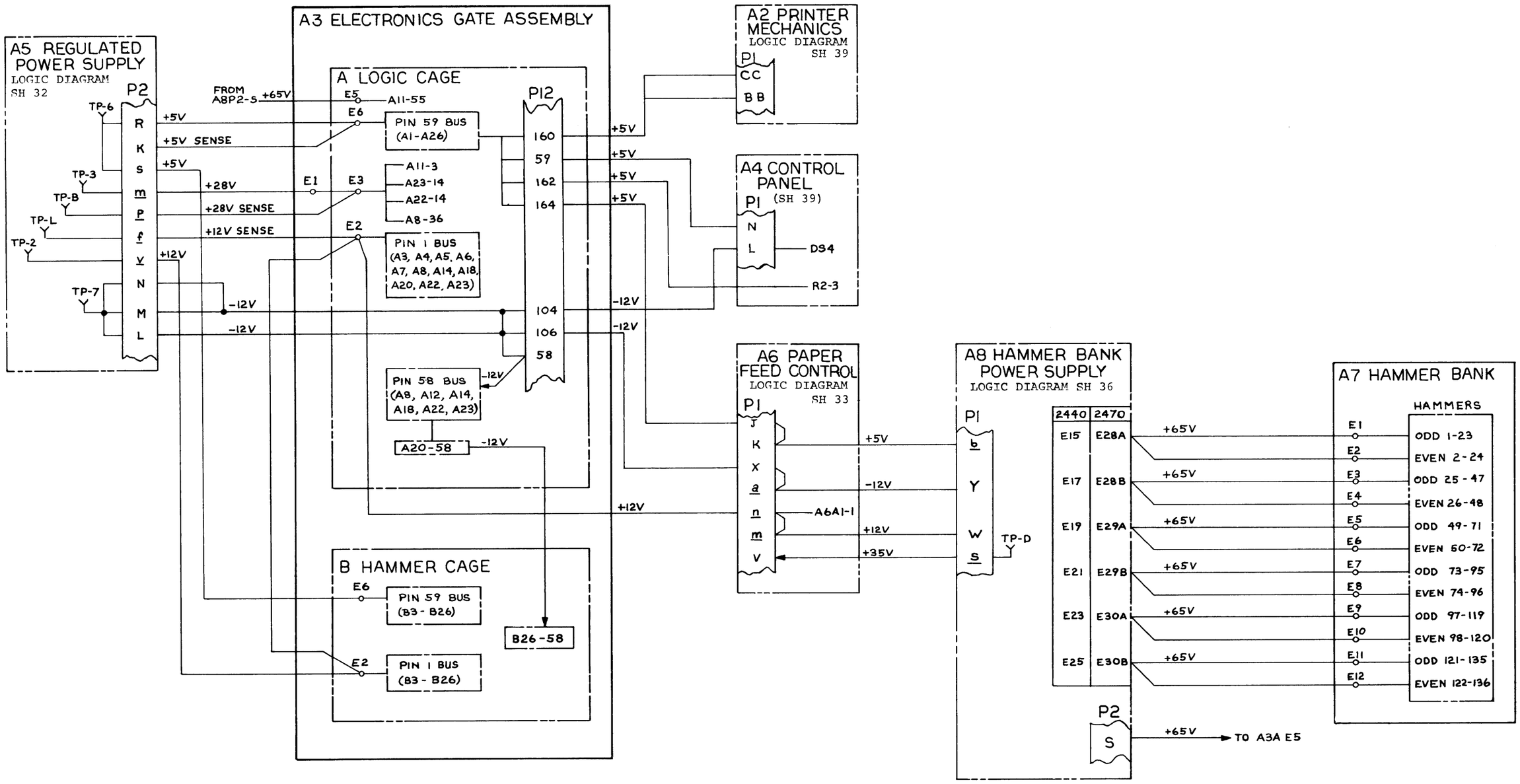
REFERENCE DESIGNATIONS	PART NO. AV-17; AV-19
U1	800186-001
U2, U3, U4	800499-001

FOR COMPLETE IC PIN ASSIGNMENTS SEE LOADING DIAGRAMS IN APPENDIX A

ASSEMBLY LOCATION: A5 (MODELS 2440/ 2470)

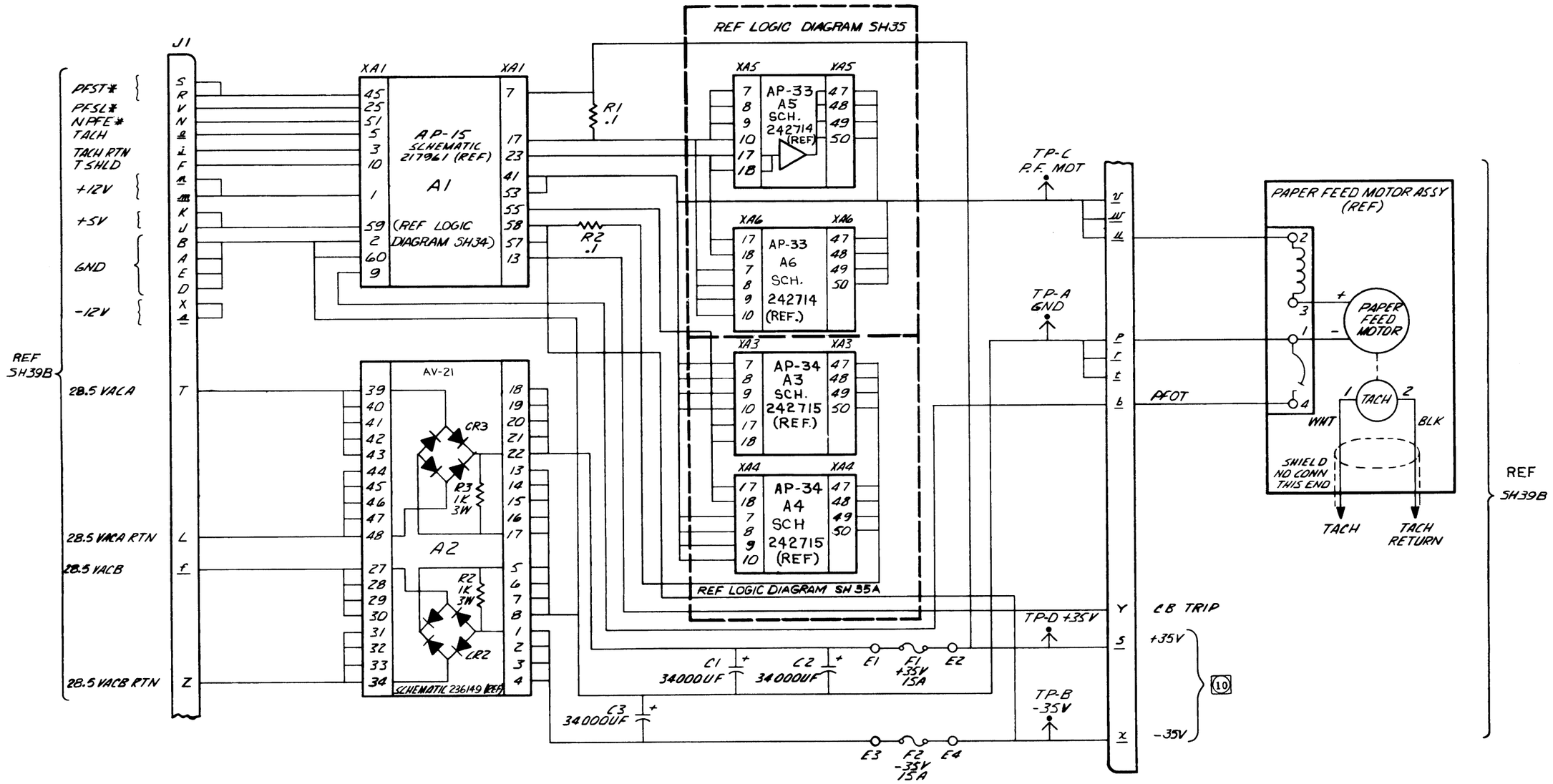
LOGIC DIAGRAM SHEET 32

REGULATED POWER SUPPLY



LOGIC DIAGRAM SHEET 32A

DC DISTRIBUTION DIAGRAM
(MODELS 2440/2470)



(10) +35V NOMINALLY +40 TO 45V

9. FOR SCHEMATIC SEE DWG NO. 219684, REV G
8. ZENER DIODES ARE 1N5612.
7. ASSEMBLY DRAWING NUMBER 219680, REV C
6. INTERPRET ELECTRONIC SYMBOLS PER 850026.
5. INTERPRET REFERENCE DESIGNATIONS PER 850027.
4.
3.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS, 10%, 50 VOLTS.
1. ALL RESISTANCE VALUES ARE IN OHMS, 1%, 10 WATTS.

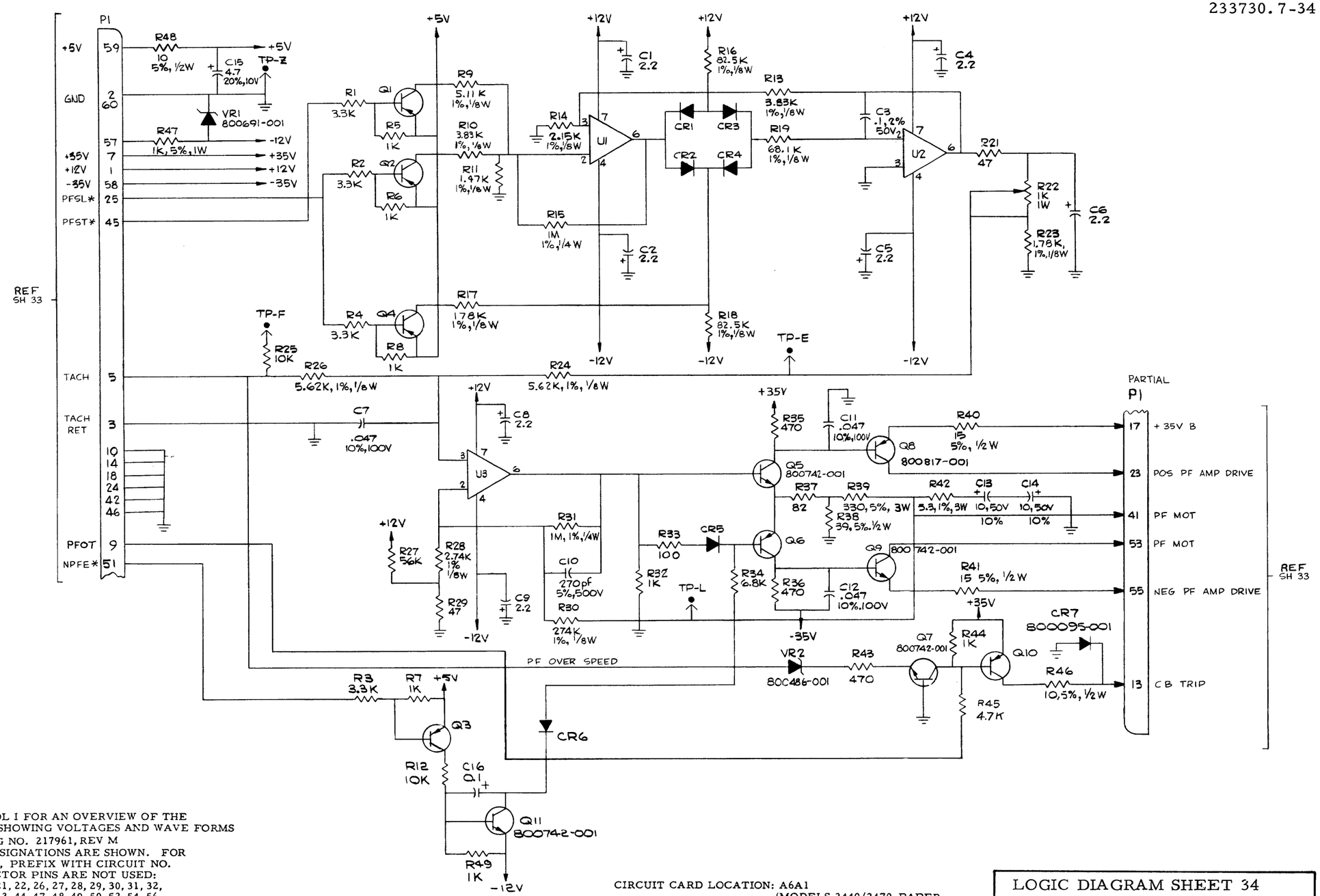
NOTES: UNLESS OTHERWISE SPECIFIED

UNUSED CONNECTOR PINS USED FOR CIRCUIT CONNECTIONS ON MOTHER BOARD	
CONN REF DES	PIN NO.
XA1	11,12,15,16,19-22,26,54,56
XA2	9-12,35,36,51,52,55,56
XA3	11-16,27-32,35,36,43,44,55
XA4	11-16,25,27-32,35,36,43,44
XA5	11-16,27-32,35
XA6	5

ASSEMBLY LOCATION: A6

LOGIC DIAGRAM SHEET 33

A6
PAPER FEED CONTROL
POWER SUPPLY
(MODELS 2440/2470)



11. SEE PAGE 5-21/5-22 IN VOL I FOR AN OVERVIEW OF THE PAPER FEED CIRCUITRY SHOWING VOLTAGES AND WAVE FORMS
10. FOR SCHEMATIC SEE DWG NO. 217961, REV M
9. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION, PREFIX WITH CIRCUIT NO.
8. THE FOLLOWING CONNECTOR PINS ARE NOT USED: 4, 6, 8, 11, 12, 15, 16, 19, 20, 21, 22, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 43, 44, 47, 48, 49, 50, 52, 54, 56
7. ASSEMBLY DRAWING NUMBER 217985, REV H
6. INTERPRET ELECTRONIC SYMBOLS PER 850026.
5. INTERPRET REFERENCE DESIGNATIONS PER 850021.
4. ALL TRANSISTORS ARE 800515-001
3. ALL DIODES ARE 800093-001.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS, 10%, 20 VOLTS.
1. ALL RESISTANCE VALUES ARE IN OHMS, 5%, 1/4 WATT.

NOTES: UNLESS OTHERWISE SPECIFIED

11. INTEGRATED CIRCUITS ARE AS FOLLOWS:

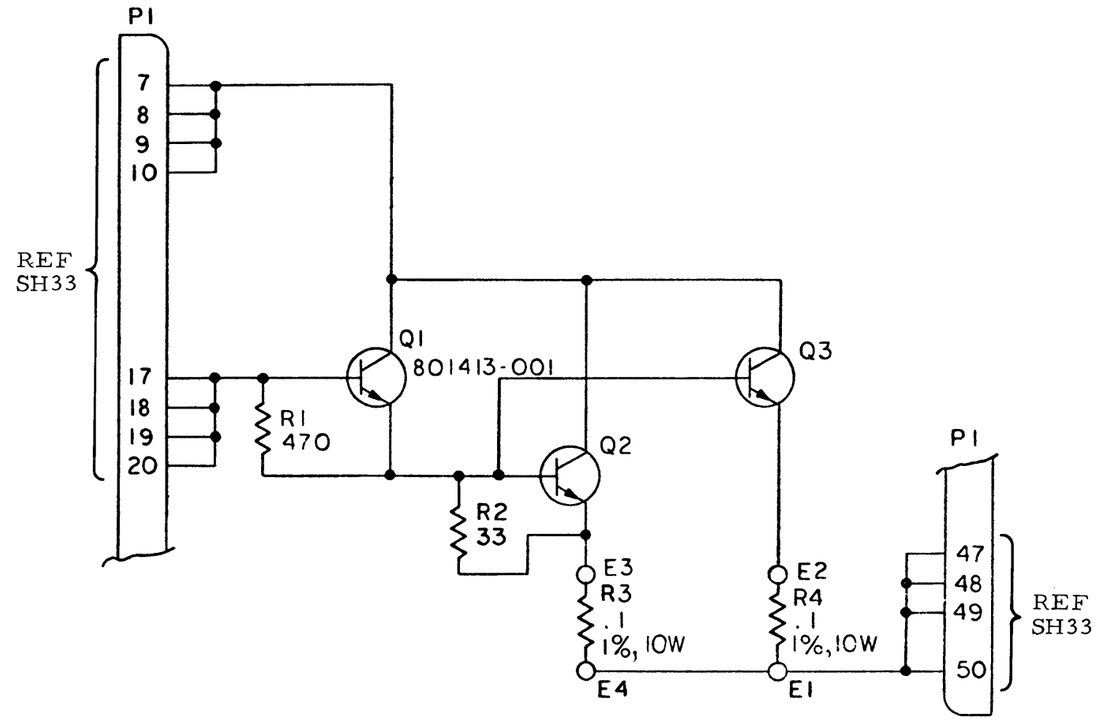
REFERENCE DESIGNATIONS	PART NO.
U1, U2, U3	800732-001

FOR COMPLETE IC PIN ASSIGNMENTS SEE LOADING DIAGRAMS IN APPENDIX A

CIRCUIT CARD LOCATION: A6A1 (MODELS 2440/2470, PAPER FEED CONTROL POWER SUPPLY ASSEMBLY A6, CARD CAGE A1)

LOGIC DIAGRAM SHEET 34

AP-15
PAPER FEED AMPLIFIER
(6/8 LPI)



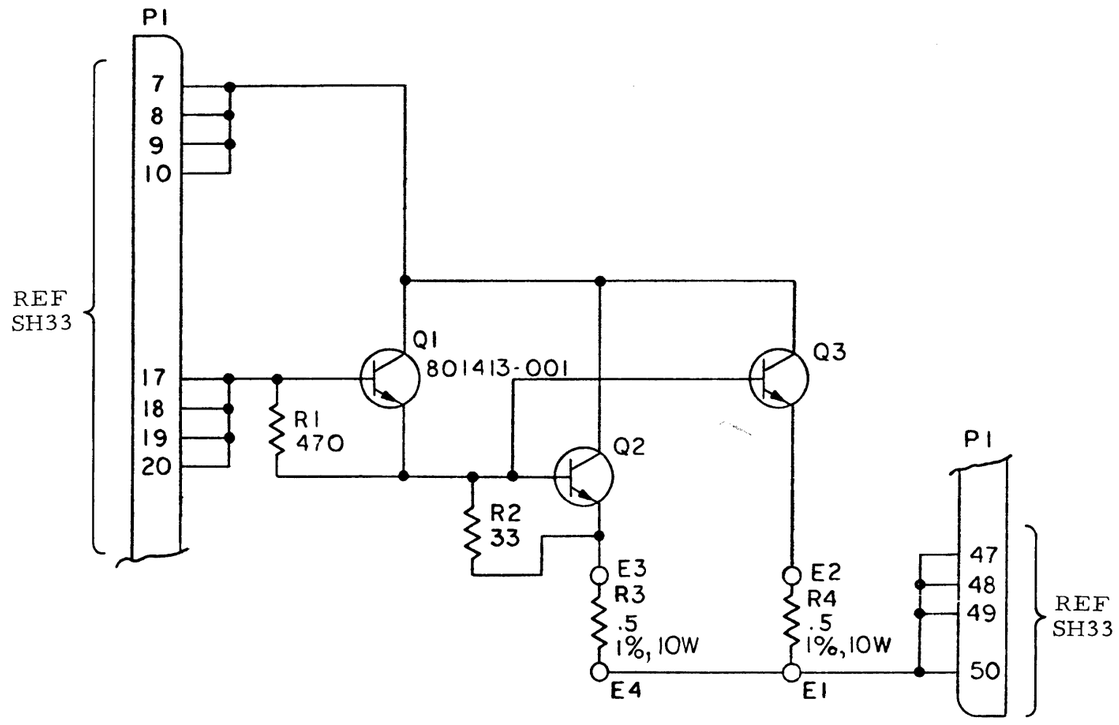
6. FOR SCHEMATIC SEE DWG NO. 242714, REV XA
5. ASSEMBLY DRAWING NUMBER 242710, REV XB
4. INTERPRET ELECTRONIC SYMBOLS PER 850026.
3. INTERPRET REFERENCE DESIGNATIONS PER 850027.
2. ALL TRANSISTORS ARE 801414-001
1. ALL RESISTANCE VALUES ARE IN OHMS, 5%, 1/4 WATT.

NOTES: UNLESS OTHERWISE SPECIFIED

CIRCUIT CARD LOCATION: A6A5 & A6A6
(MODELS 2440/2470,
PAPER FEED CONTROL POWER
SUPPLY ASSEMBLY A6, CARD
CAGE SLOTS A5 & A6)

LOGIC DIAGRAM SHEET 35

AP-33
PAPER FEED POWER AMPLIFIER
(MODELS 2440/2470)



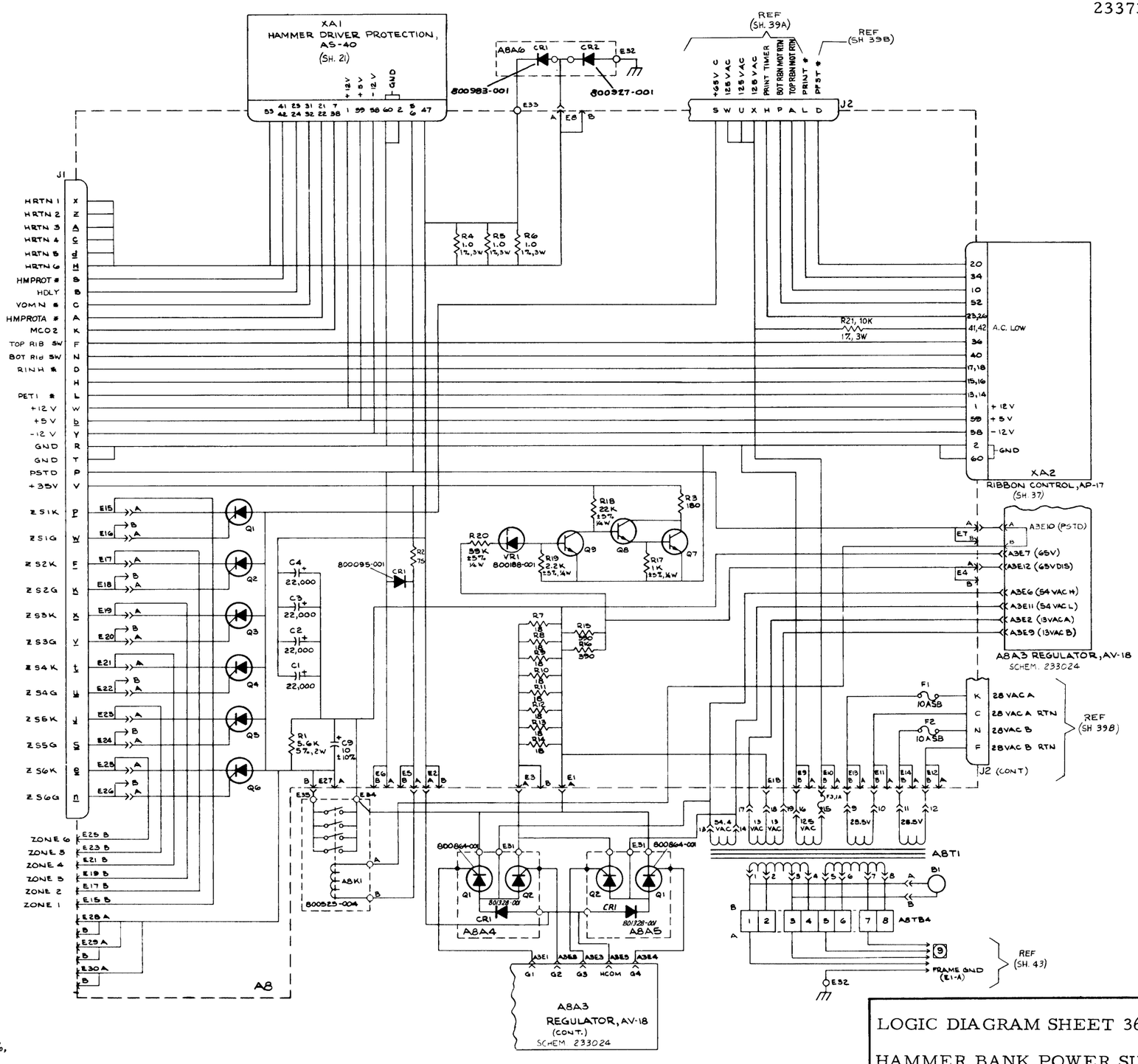
6. FOR SCHEMATIC SEE DWG NO. 242715. REV XA
5. ASSEMBLY DRAWING NUMBER 242710, REV XB
4. INTERPRET ELECTRONIC SYMBOLS PER 850026.
3. INTERPRET REFERENCE DESIGNATIONS PER 850027.
2. ALL TRANSISTORS ARE 801414-001
1. ALL RESISTANCE VALUES ARE IN OHMS, 5%, 1/4 WATT.

NOTES: UNLESS OTHERWISE SPECIFIED

CIRCUIT CARD LOCATION: A6A3 & A6A4
(MODELS 2440 & 2470,
PAPER FEED CONTROL
POWER SUPPLY ASSEMBLY
A6, CARD CAGE SLOTS A3 & A4)

LOGIC DIAGRAM SHEET 35A

AP-34
PAPER FEED POWER AMPLIFIER
(MODELS 2440/2470)



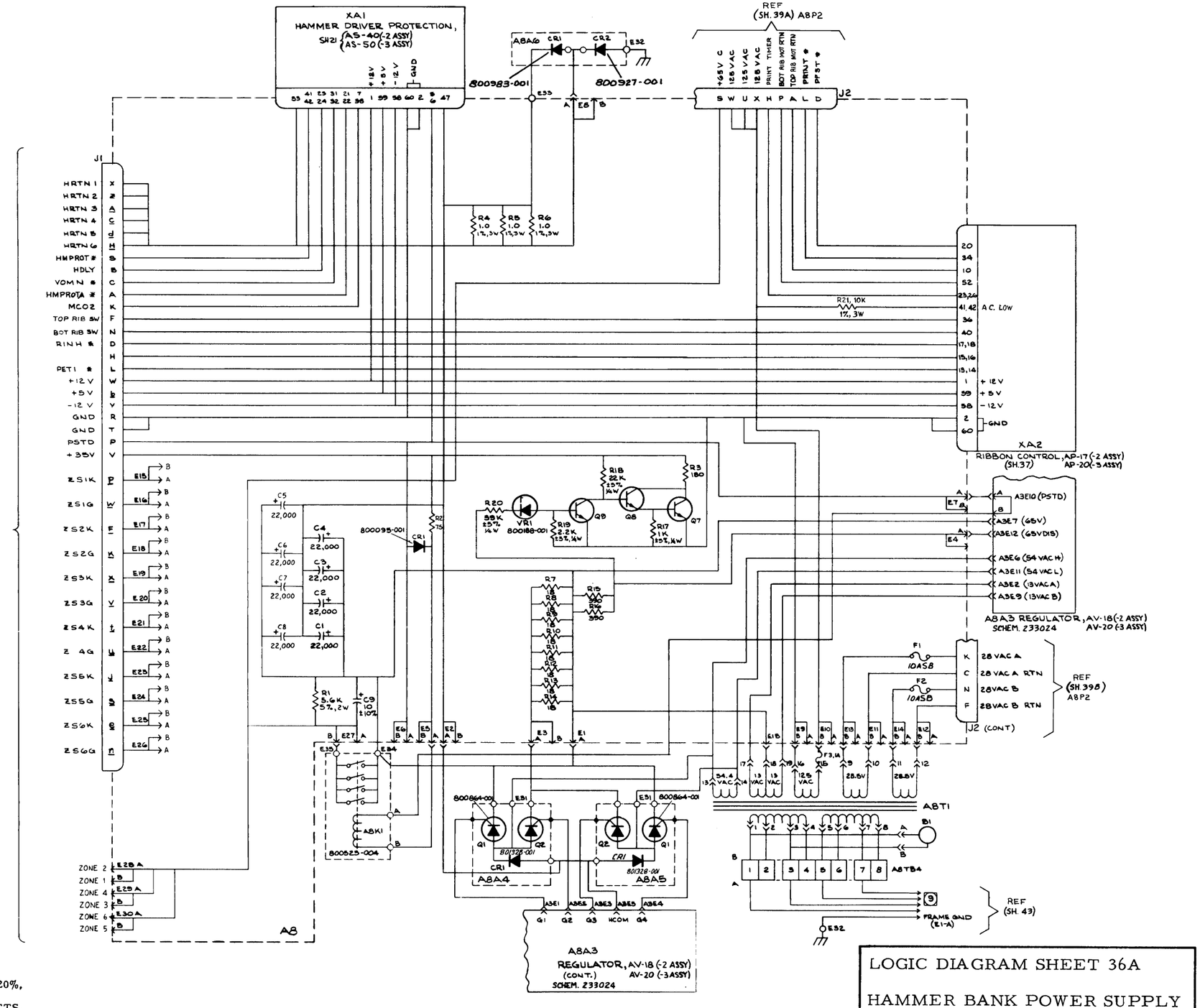
10. FOR SCHEMATIC SEE DWG NO. 233169, REV L
9. CONNECTION FOR 115VAC OPERATION SHOWN. FOR OTHER INPUT VOLTAGES SEE DWG 233312.
8. ASSEMBLY DRAWING NUMBER 233154, REV AC
7. INTERPRET ELECTRONIC SYMBOLS PER 850026.
6. INTERPRET REFERENCE DESIGNATIONS PER 850027.
5. ALL THYRISTORS ARE 800192-001.
4. ALL DIODES ARE 800297-001
3. ALL TRANSISTORS ARE 800019-001.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS, +120%, -10%, 75 VOLTS.
1. ALL RESISTANCE VALUES ARE IN OHMS, ± 10%, 10 WATTS.

NOTES: UNLESS OTHERWISE SPECIFIED

ASSEMBLY LOCATION : A8 (MODEL 2440 ONLY)

LOGIC DIAGRAM SHEET 36

HAMMER BANK POWER SUPPLY



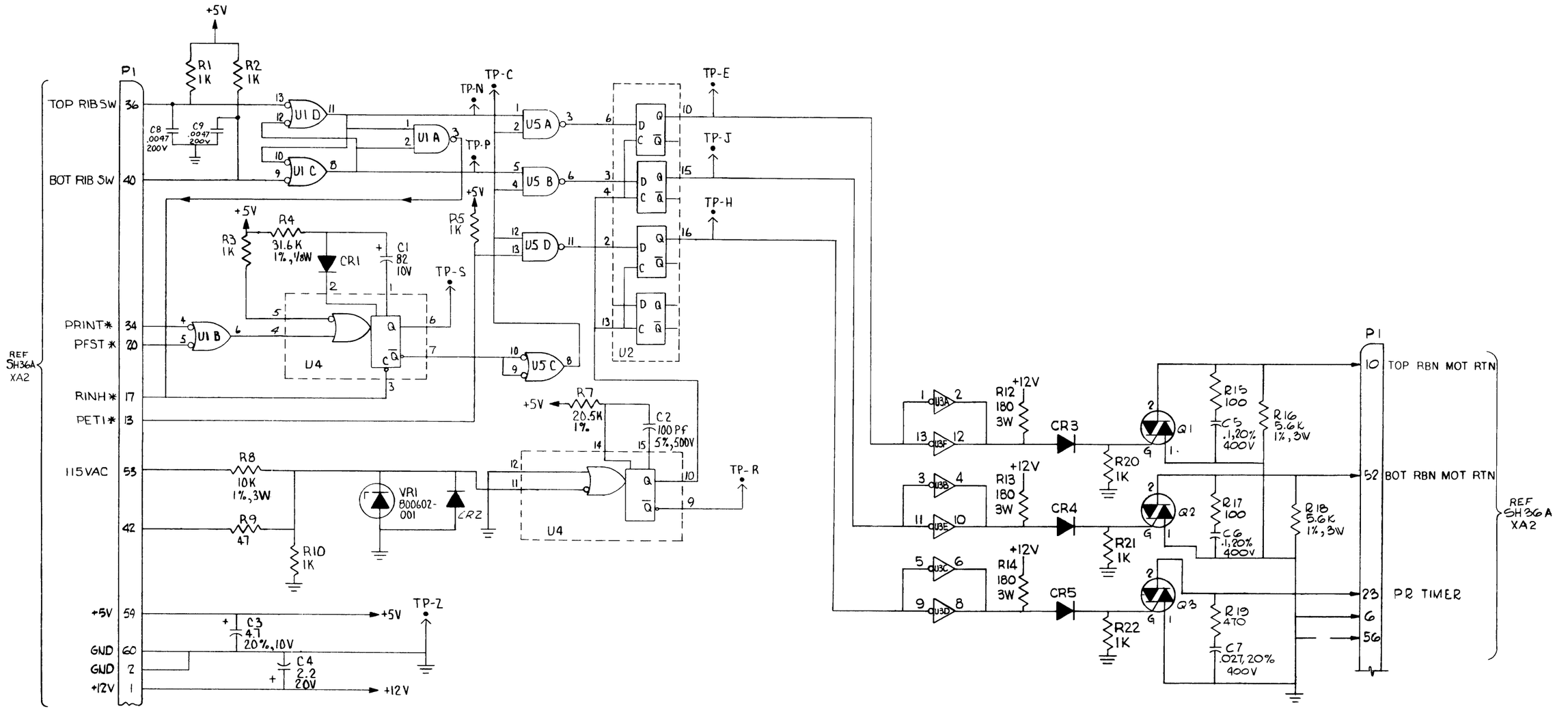
10. FOR SCHEMATIC SEE DWG NO. 233170, REV N
9. CONNECTION FOR 115VAC OPERATION SHOWN. FOR OTHER INPUT VOLTAGES SEE DWG 233312.
8. ASSEMBLY DRAWING NUMBER 233154, REV AC
7. INTERPRET ELECTRONIC SYMBOLS PER 850026.
6. INTERPRET REFERENCE DESIGNATIONS PER 850027.
5. ALL THYRISTORS ARE 800192-001.
4. ALL DIODES ARE 800297-001
3. ALL TRANSISTORS ARE 800019-001.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS, +120%, -10%, 75 VOLTS.
1. ALL RESISTANCE VALUES ARE IN OHMS, ± 10%, 10 WATTS.

NOTES: UNLESS OTHERWISE SPECIFIED

ASSEMBLY LOCATION: A8
(MODEL 2470 ONLY)

LOGIC DIAGRAM SHEET 36A

HAMMER BANK POWER SUPPLY



9. THE FOLLOWING CONNECTOR PINS ARE USED FOR FEED-THRUS: 3, 4, 5, 14, 16, 18, 19, 22, 26, 29, 30, 31, 32, 37, 38, 43, 44, 48, 49, 57, 58
8. THE FOLLOWING CONNECTOR PINS ARE NOT USED: 7, 8, 9, 11, 12, 21, 24, 25, 27, 28, 33, 35, 39, 41, 45, 46, 47, 50, 51, 54, 55
7. ASSEMBLY DRAWING NUMBER 219805, REV J
6. INTERPRET ELECTRONIC SYMBOLS PER USAS Y32.2.
5. INTERPRET REFERENCE DESIGNATIONS PER USAS Y32.16.
4. ALL THYRISTORS ARE 800525-001.
3. ALL DIODES ARE 800093-001
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS, 10%, 100 VOLTS.
1. ALL RESISTANCE VALUES ARE IN OHMS, 5%, 1/4 WATT.

NOTES: UNLESS OTHERWISE SPECIFIED

11. FOR SCHEMATIC SEE DWG NO. 219809, REV J
10. INTEGRATED CIRCUITS ARE AS FOLLOWS:

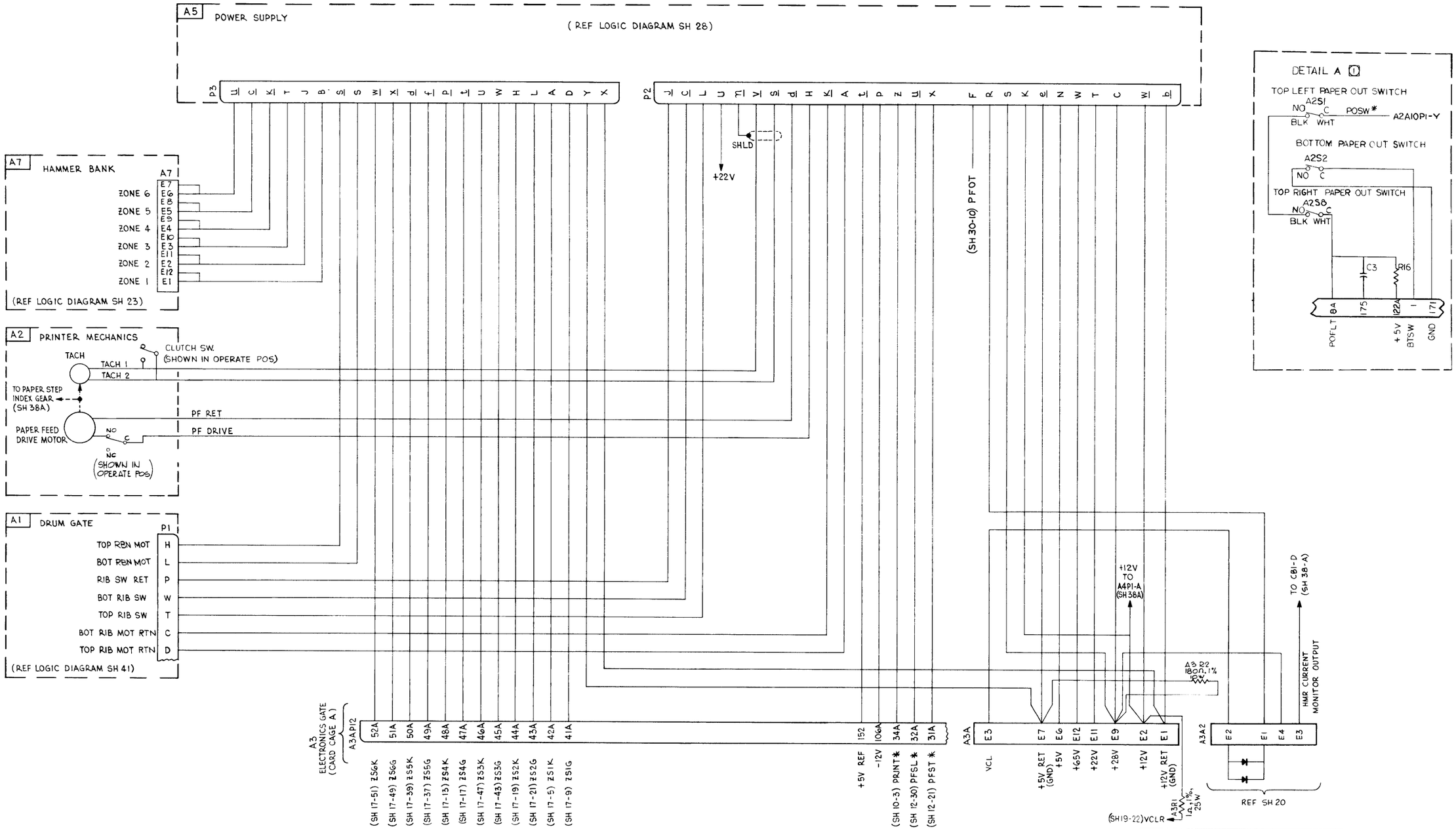
REFERENCE DESIGNATIONS	PART NO. AP-17
U1, U5	800024-001
U2	800382-001
U3	800651-001
U4	800810-001

FOR COMPLETE IC PIN ASSIGNMENTS SEE LOADING DIAGRAMS IN APPENDIX A

CIRCUIT CARD LOCATION: A8A2
(MODELS 2440/2470, HAMMER BANK POWER SUPPLY ASSEMBLY A8, CARD CAGE SLOT A2)

LOGIC DIAGRAM SHEET 37

AP-17
RIBBON CONTROL



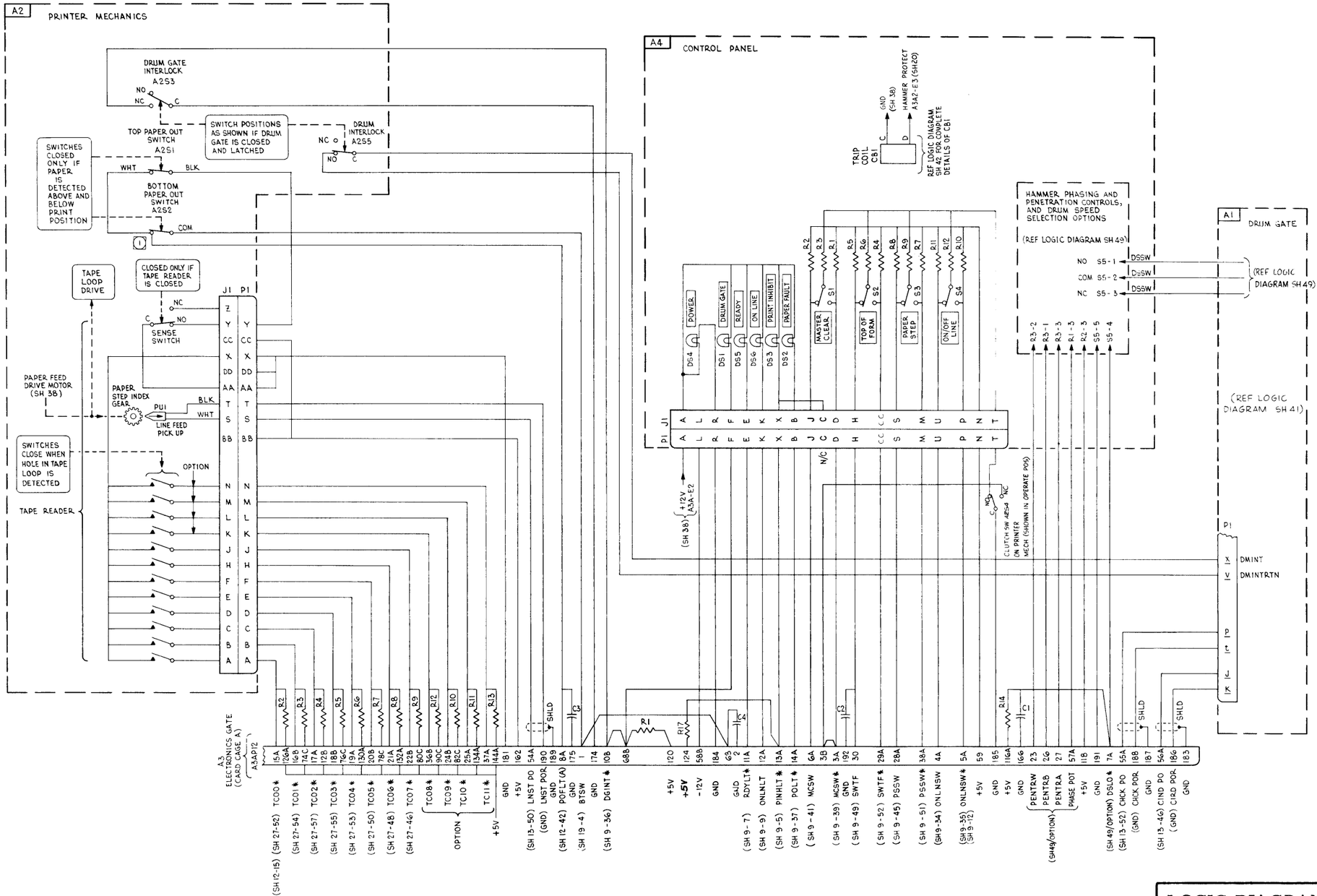
CIRCUIT CARD LOCATION: A3AP12
(MODEL 2420 ONLY,
ELECTRONICS GATE ASSEMBLY
A3, CARD CAGE A, SLOT 12)

LOGIC DIAGRAM SHEET 38

MAIN HARNESS & PRINTER MECHANICS
(MODEL 2420)

[1] SEE DETAIL A FOR SERIAL NUMBERS 6162 AND SUBSEQUENT (MODEL 2420).

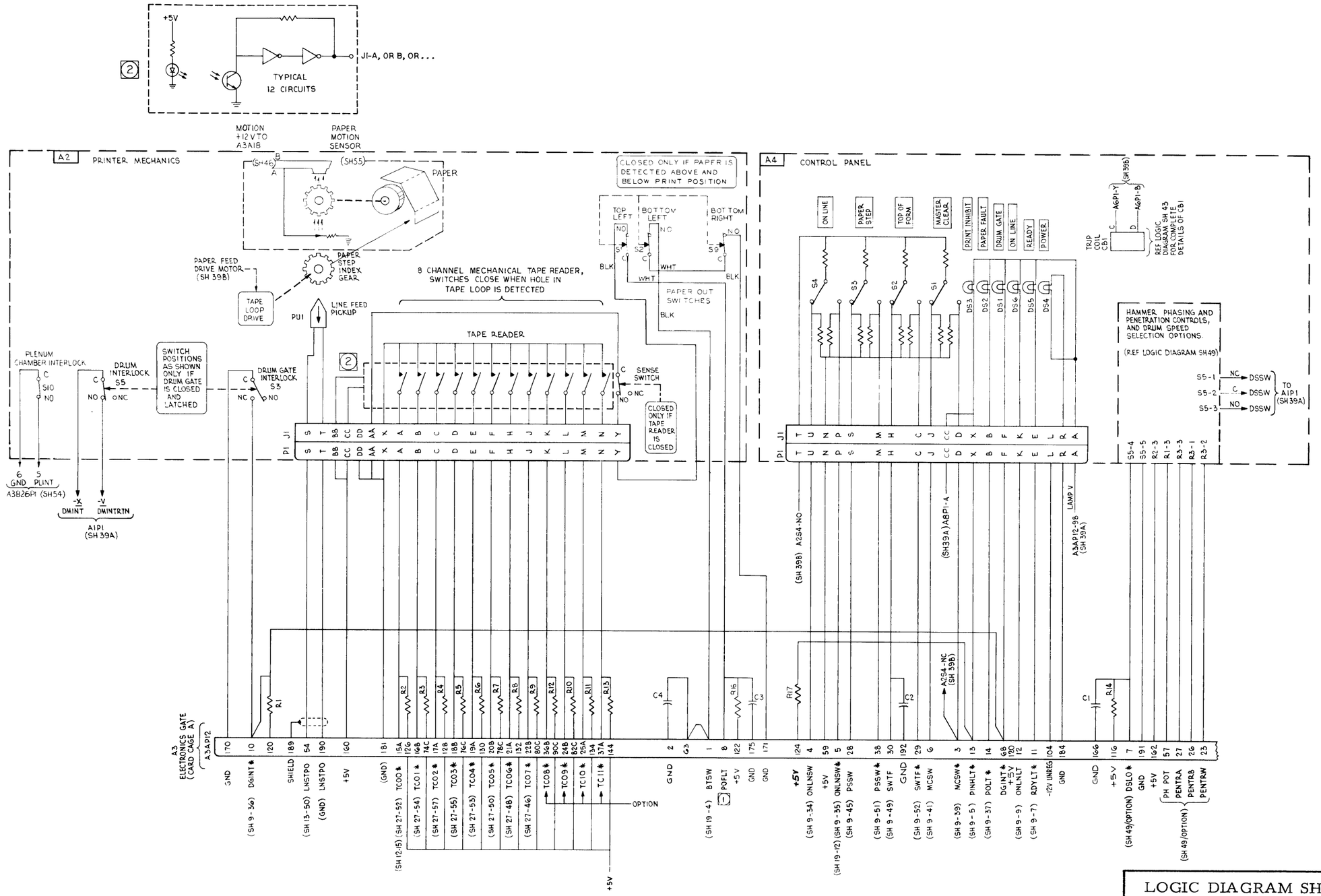
NOTES: UNLESS OTHERWISE SPECIFIED



CIRCUIT CARD LOCATION: A3AP12
(MODEL 2420 ONLY,
ELECTRONICS GATE ASSEMBLY
A3, CARD CAGE A, SLOT 12)

LOGIC DIAGRAM SHEET 38A

MAIN HARNESS & PRINTER MECHANICS
(MODEL 2420)



(2) OPTICAL 12-CHANNEL TAPE READER OPTION CAN BE SUBSTITUTED FOR 8-CHANNEL TAPE READER.

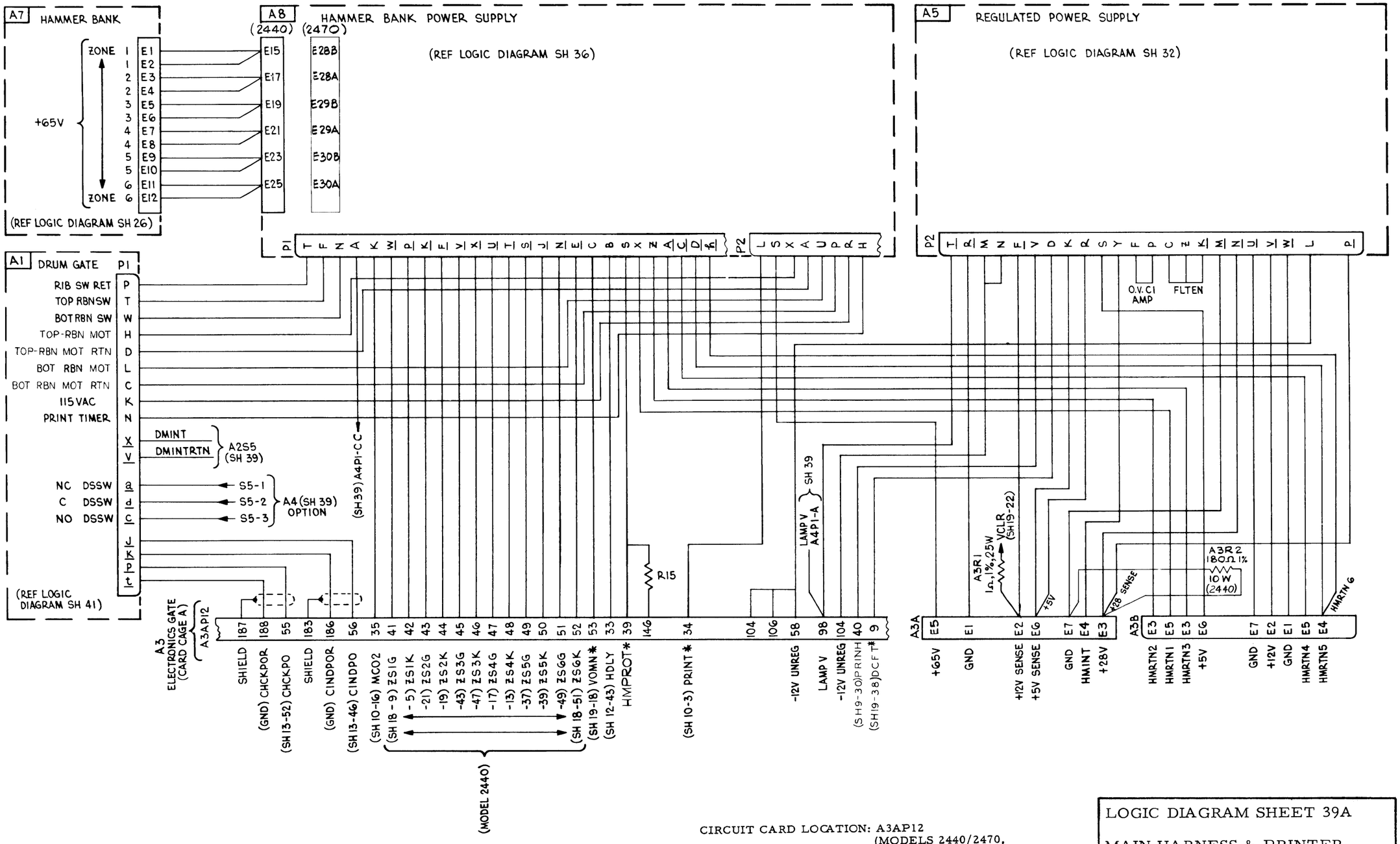
(1) MODEL 2420: SH12-42.
MODELS 2440/2470: SH54-53.

NOTES: UNLESS OTHERWISE SPECIFIED

CIRCUIT CARD LOCATION : A3AP12
(MODELS 2440/2470 ONLY,
ELECTRONICS GATE ASSEMBLY
A3, CARD CAGE A, SLOT 12)

LOGIC DIAGRAM SHEET 39

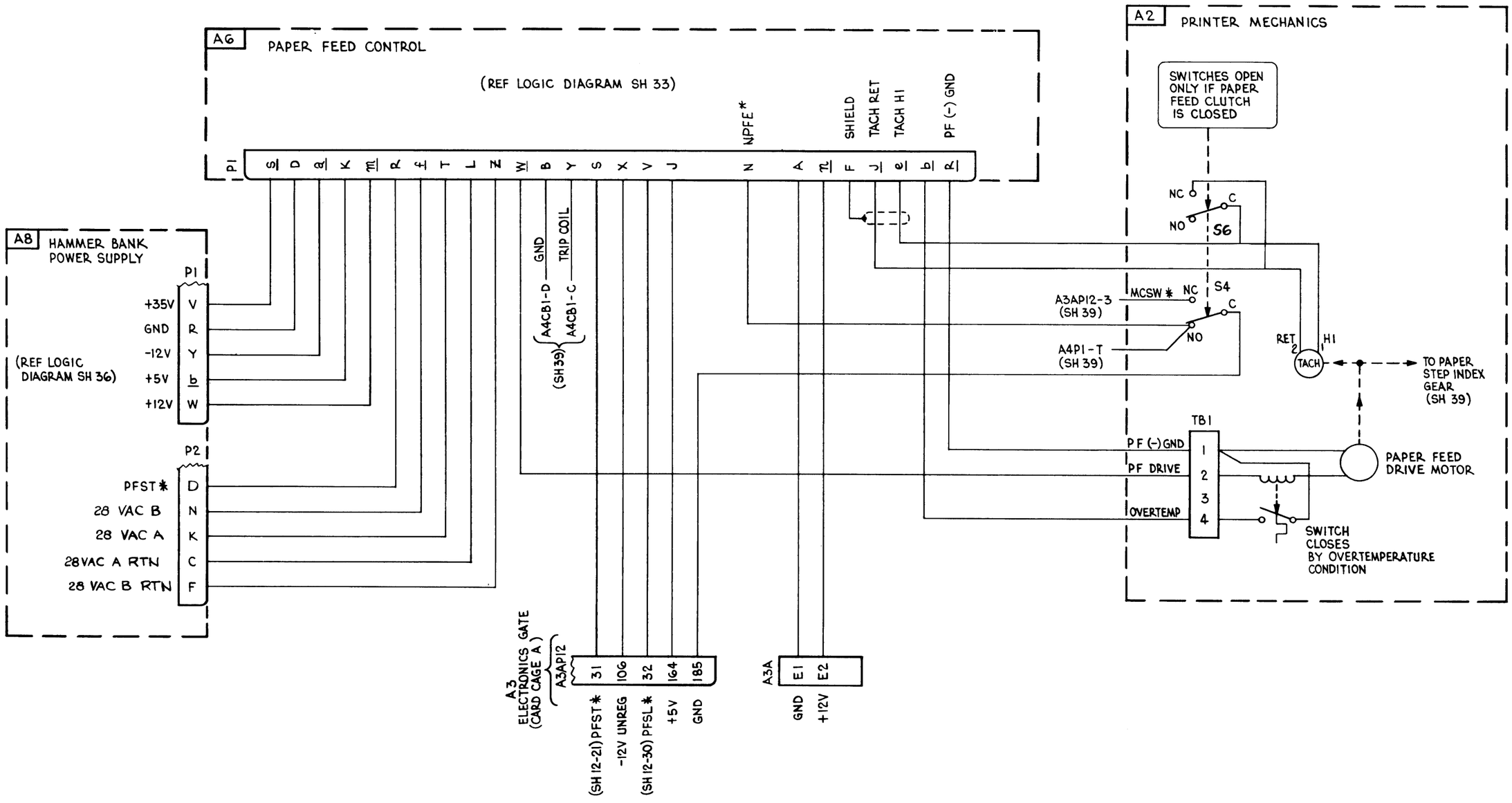
MAIN HARNESS & PRINTER MECHANICS
(MODELS 2440/2470)



CIRCUIT CARD LOCATION: A3AP12
(MODELS 2440/2470,
ELECTRONICS GATE ASSEMBLY
A3, CARD CAGE A, SLOT 12)

LOGIC DIAGRAM SHEET 39A

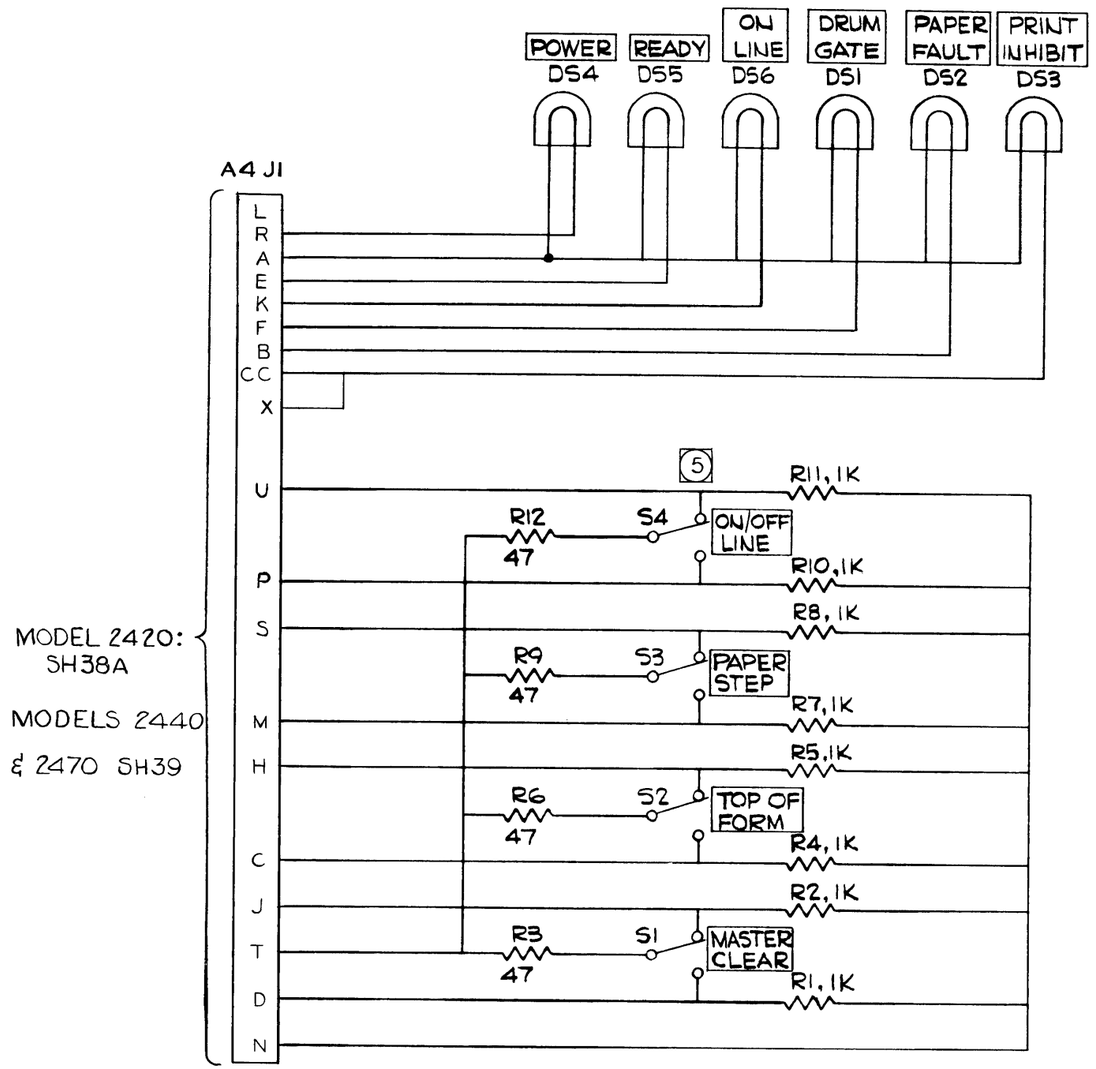
MAIN HARNESS & PRINTER MECHANICS
(MODELS 2440/2470)



CIRCUIT CARD LOCATION: A3AP12
(MODELS 2440/2470,
ELECTRONICS GATE ASSEMBLY
A3, CARD CAGE A, SLOT 12)

LOGIC DIAGRAM SHEET 39B

MAIN HARNESS & PRINTER MECHANICS
(MODELS 2440/2470)



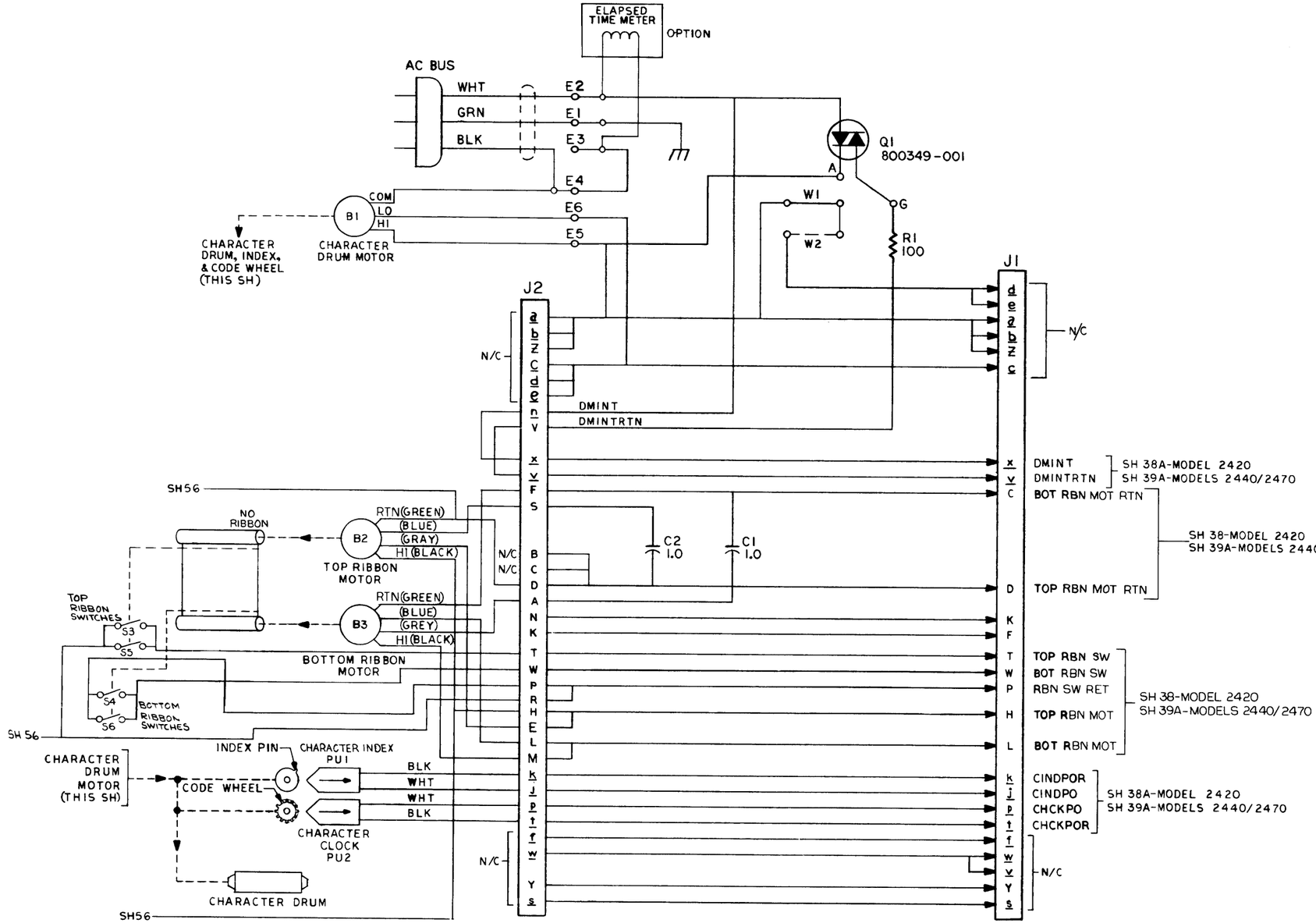
6. FOR SCHEMATIC SEE DWG NO. 219809, REV J
(5) ALL SWITCHES ARE MOMENTARY & SHOWN IN DEACTUATED POSITION.
4. ASSEMBLY DRAWING NUMBER 233232, REV D
3. INTERPRET ELECTRONIC SYMBOLS PER USAS Y32.2.
2. INTERPRET REFERENCE DESIGNATIONS PER USAS Y32.16.
1. ALL RESISTANCE VALUES ARE IN OHMS, 5%, 1/4 WATT.

NOTES: UNLESS OTHERWISE SPECIFIED

ASSEMBLY LOCATION: A4
(ALL MODELS)

LOGIC DIAGRAM SHEET 40

OPERATOR CONTROL PANEL



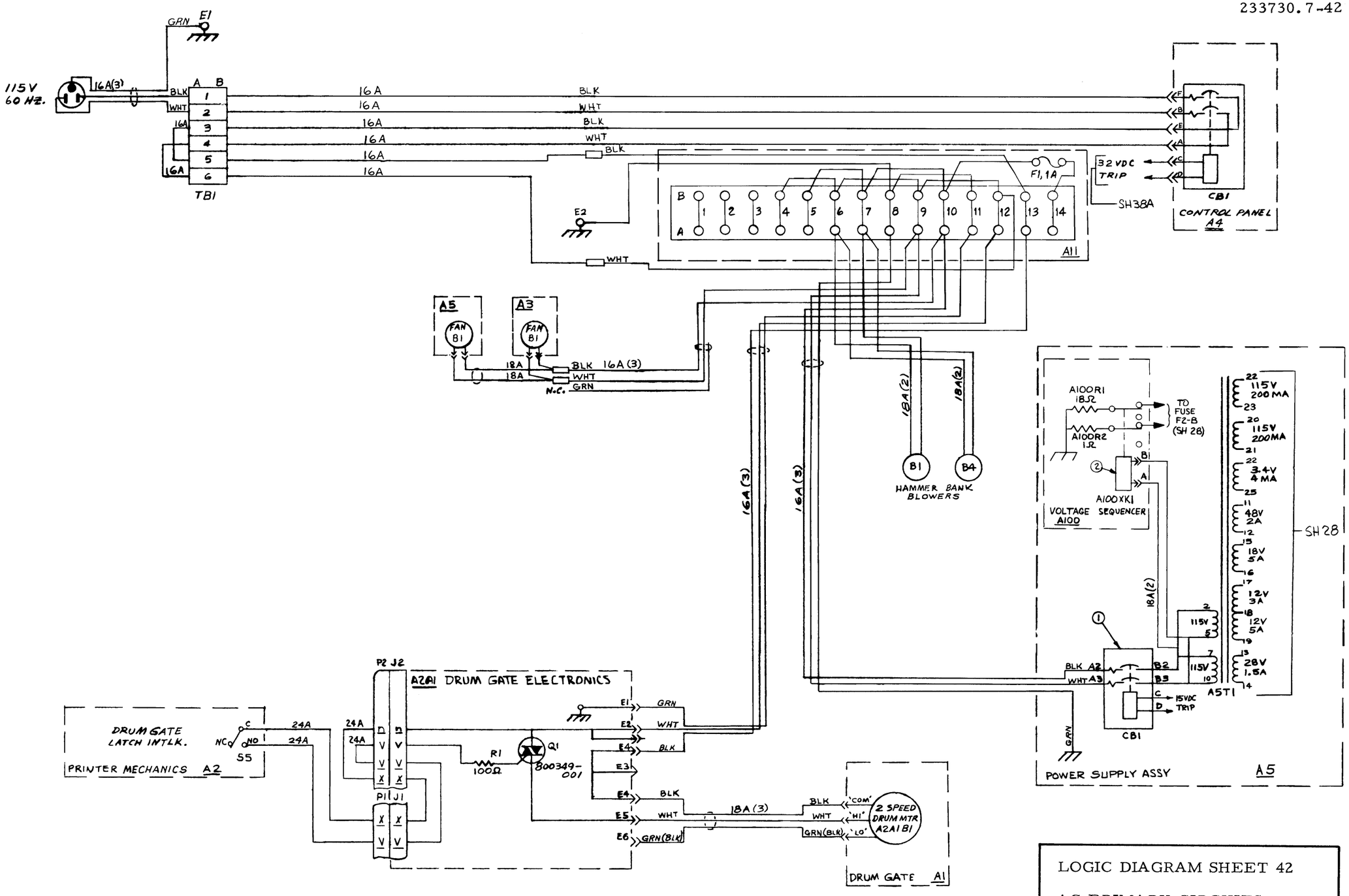
6. FOR SCHEMATIC SEE DWG NO. 218509. REV K
5. ASSEMBLY DRAWING NUMBER 218505, REV K
4. INTERPRET ELECTRONIC SYMBOLS PER USAS Y32.2.
3. INTERPRET REFERENCE DESIGNATIONS PER USAS Y32.16.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS, 10%, 400 VOLTS.
1. ALL RESISTANCE VALUES ARE IN OHMS, 5%, 1/2 WATT.

NOTES: UNLESS OTHERWISE SPECIFIED

ASSEMBLY LOCATION: A2
(ALL MODELS)

LOGIC DIAGRAM SHEET 41

DRUM GATE ELECTRONICS

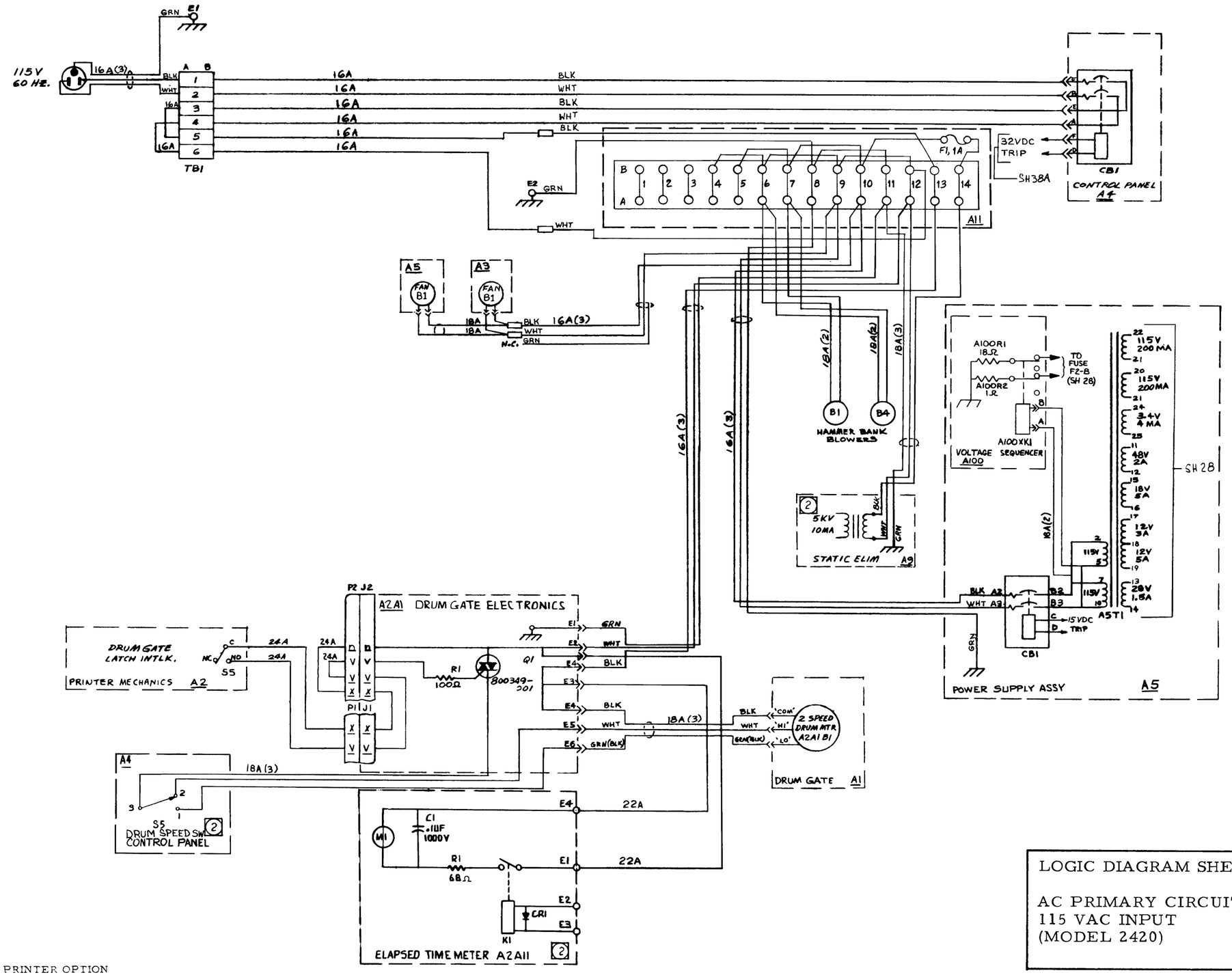


1. FOR SCHEMATIC SEE DWG NO. 850112, REV F

NOTES: UNLESS OTHERWISE SPECIFIED

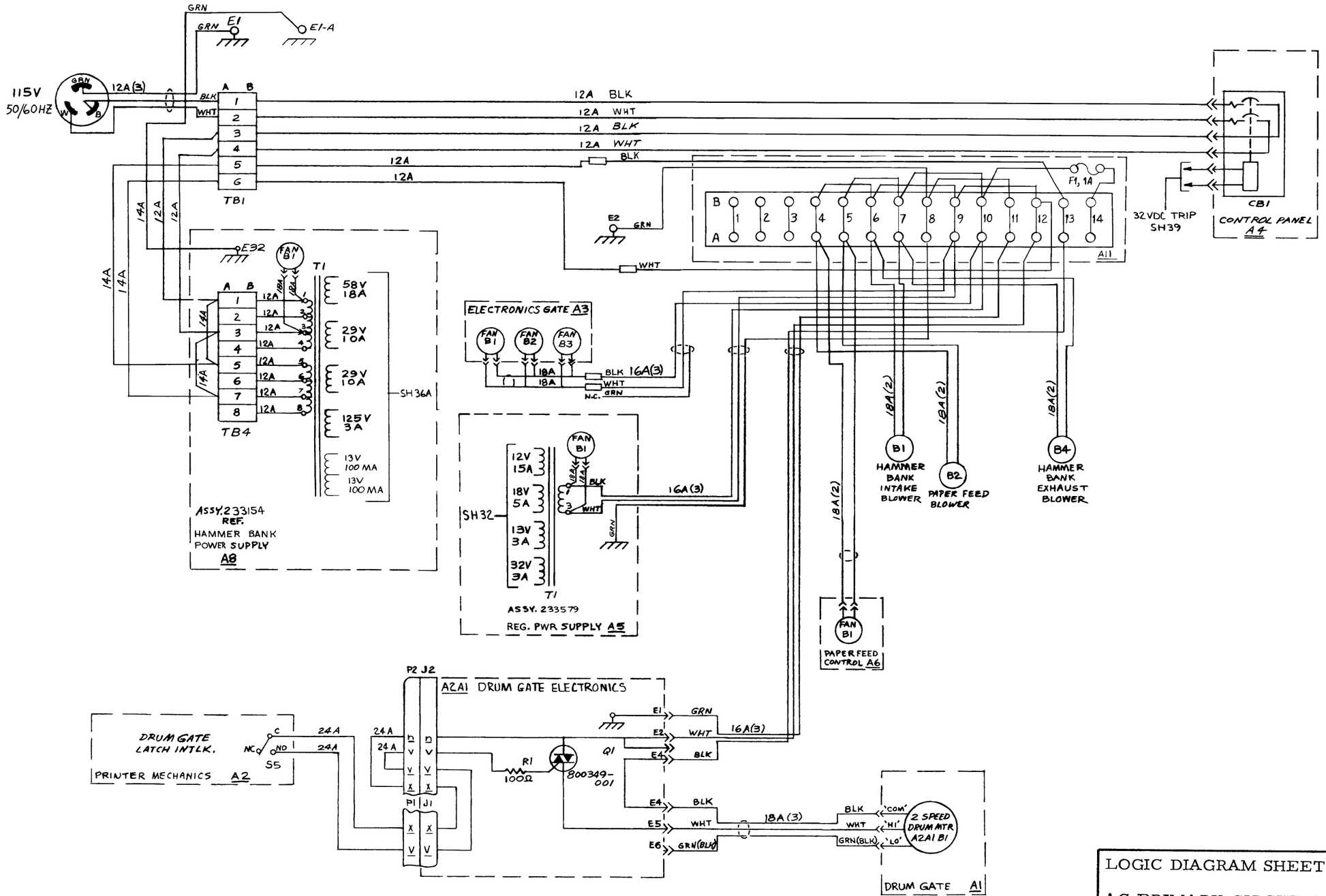
LOGIC DIAGRAM SHEET 42

AC PRIMARY CIRCUITS,
115 VAC INPUT
(MODEL 2420)



LOGIC DIAGRAM SHEET 42A

AC PRIMARY CIRCUITS,
115 VAC INPUT
(MODEL 2420)

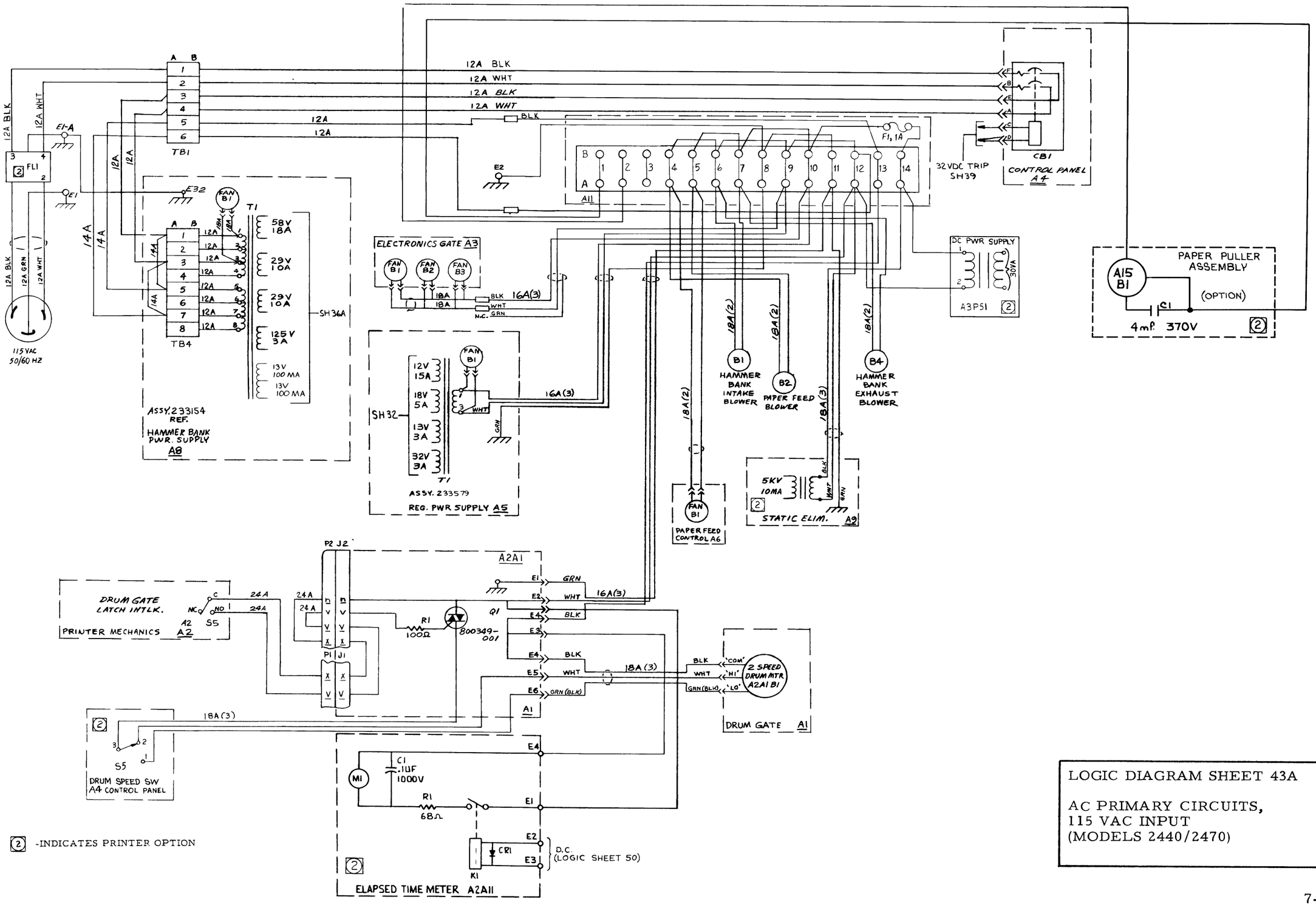


LOGIC DIAGRAM SHEET 43

AC PRIMARY CIRCUITS
115 VAC INPUT
(MODELS 2440/2470)

NOTES: UNLESS OTHERWISE SPECIFIED

1. FOR SCHEMATIC SEE DWG NO. 850111, REV F



(2) -INDICATES PRINTER OPTION

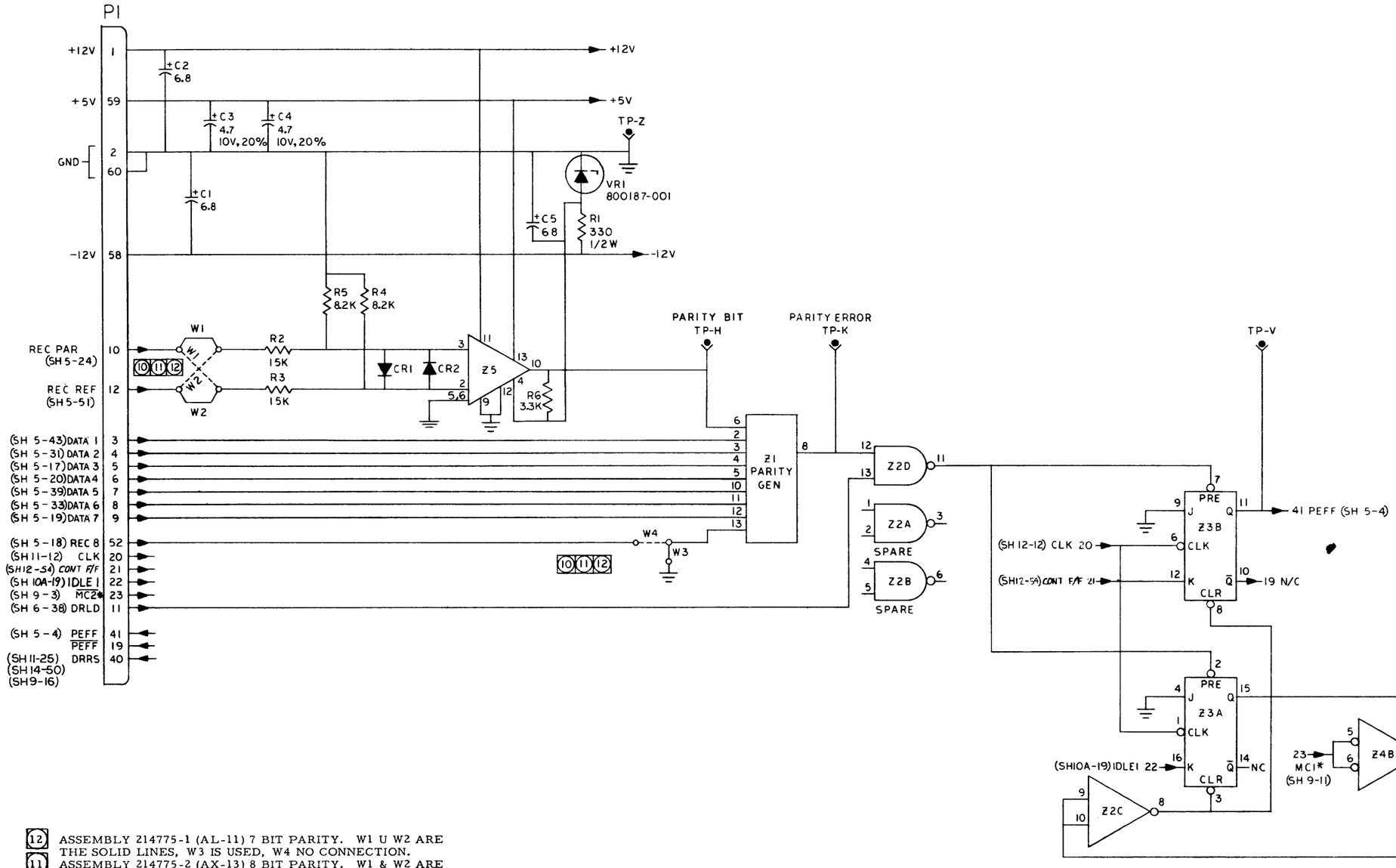
LOGIC DIAGRAM SHEET 43A

AC PRIMARY CIRCUITS,
115 VAC INPUT
(MODELS 2440/2470)

b^7				0	0	1	1	0	1
	b^6			0	1	0	1	0	1
		b^5		0	0	0	1	1	1
b^4	b^3	b^2	b^1						
0	0	0	0		SPACE	0	@	P	
0	0	0	1		!	1	A	Q	
0	0	1	0		"	2	B	R	
0	0	1	1		#	3	C	S	
0	1	0	0		$	4	D	T	
0	1	0	1		%	5	E	U	
0	1	1	0		&	6	F	V	
0	1	1	1		'	7	G	W	
1	0	0	0		(	8	H	X	
1	0	0	1		)	9	I	Y	
1	0	1	0	LF	*	:	J	Z	
1	0	1	1		+	;	K	[	
1	1	0	0	FF	,	<	L	\	
1	1	0	1	CR	-	=	M	]	
1	1	1	0		.	>	N	↑	
1	1	1	1		/	?	O	←	

LOGIC DIAGRAM SHEET 44

CODE SET, 64 CHARACTER
(ALL MODELS)



(12) ASSEMBLY 214775-1 (AL-11) 7 BIT PARITY. W1 U W2 ARE THE SOLID LINES, W3 IS USED, W4 NO CONNECTION.

(11) ASSEMBLY 214775-2 (AX-13) 8 BIT PARITY. W1 & W2 ARE THE SOLID LINES, W4 IS USED, W3 NO CONNECTION.

(10) ASSEMBLY 216808 (AL-18) NEGATIVE LOGIC. W1 & W2 ARE THE CROSSED DASHED LINES, W3 IS USED, W4 NO CONNECTION.

9. THE FOLLOWING CONNECTOR PINS ARE NOT USED: 13, 14, 15, 16, 17, 18, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 42, 43, 44, 45, 46, 47, 48, 49, 50, 51, 53, 54, 55, 56, 57
8. REFERENCE DESIGNATION Z IDENTIFIES INTEGRATED CIRCUIT PACKAGE.
7. INTERPRET LOGIC SYMBOLS PER 850025.
6. INTERPRET ELECTRONIC SYMBOLS PER 850026.
5. INTERPRET REFERENCE DESIGNATIONS PER 850027.
4.
3. ALL DIODES ARE 800093-001.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS, ± 10%, 20 VOLTS.
1. ALL RESISTANCE VALUES ARE IN OHMS, ± 5%, 1/4 WATT.

NOTES: UNLESS OTHERWISE SPECIFIED

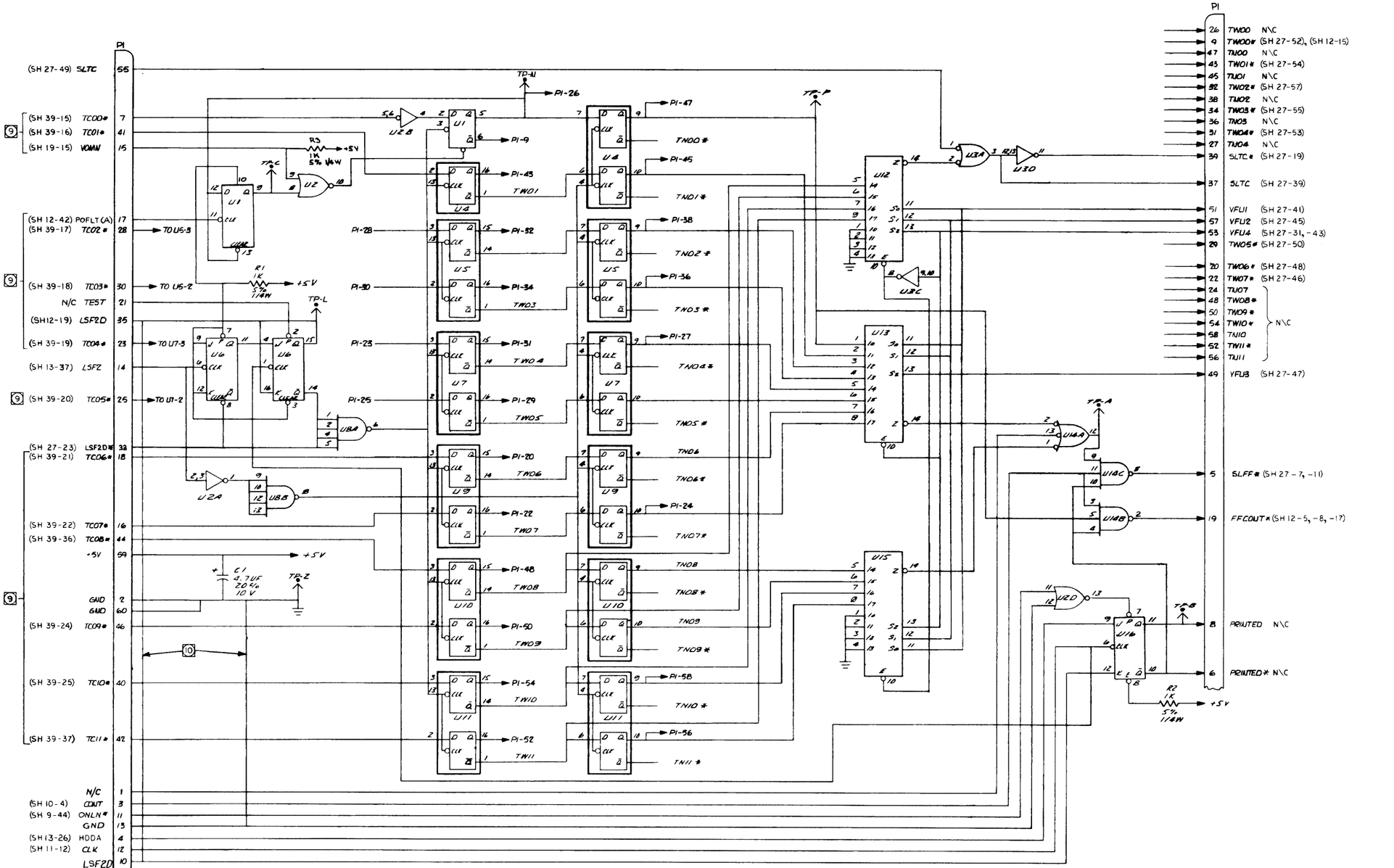
14. FOR SCHEMATIC SEE DWG NO. 214779, REV K
13. INTEGRATED CIRCUITS ARE AS FOLLOWS:

REFERENCE DESIGNATIONS	PART NO.
Z1	800393-001
Z2	800024-001
Z3	800081-001
Z4	800080-001
Z5	800186-001

FOR COMPLETE IC PIN ASSIGNMENTS SEE LOADING DIAGRAMS IN APPENDIX A

CIRCUIT CARD LOCATION:
A3A18
(ALL MODELS, ELECTRONICS GATE ASSEMBLY A3, CARD CAGE A, SLOT 18)

LOGIC DIAGRAM SHEET 46
AL-11
PARITY
(OPTION)



10 EXTERNAL CONNECTIONS.
9 REFERENCES SHOWN ARE FOR MODELS 2440 & 2470. REFER TO SHEET 38A FOR MODEL 2420.

8.
7. ASSEMBLY DRAWING NUMBER 219765, REV D
6. INTERPRET ELECTRONIC SYMBOLS PER USAS Y32.2.
5. INTERPRET REFERENCE DESIGNATIONS PER USAS Y32.16.
4.
3.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS, 20%, 10 VOLTS.
1. ALL RESISTANCE VALUES ARE IN OHMS, 5%, 1/4 WATT.

NOTES: UNLESS OTHERWISE SPECIFIED

12. FOR SCHEMATIC SEE DWG NO. 214779, REV K
11. INTEGRATED CIRCUITS ARE AS FOLLOWS:

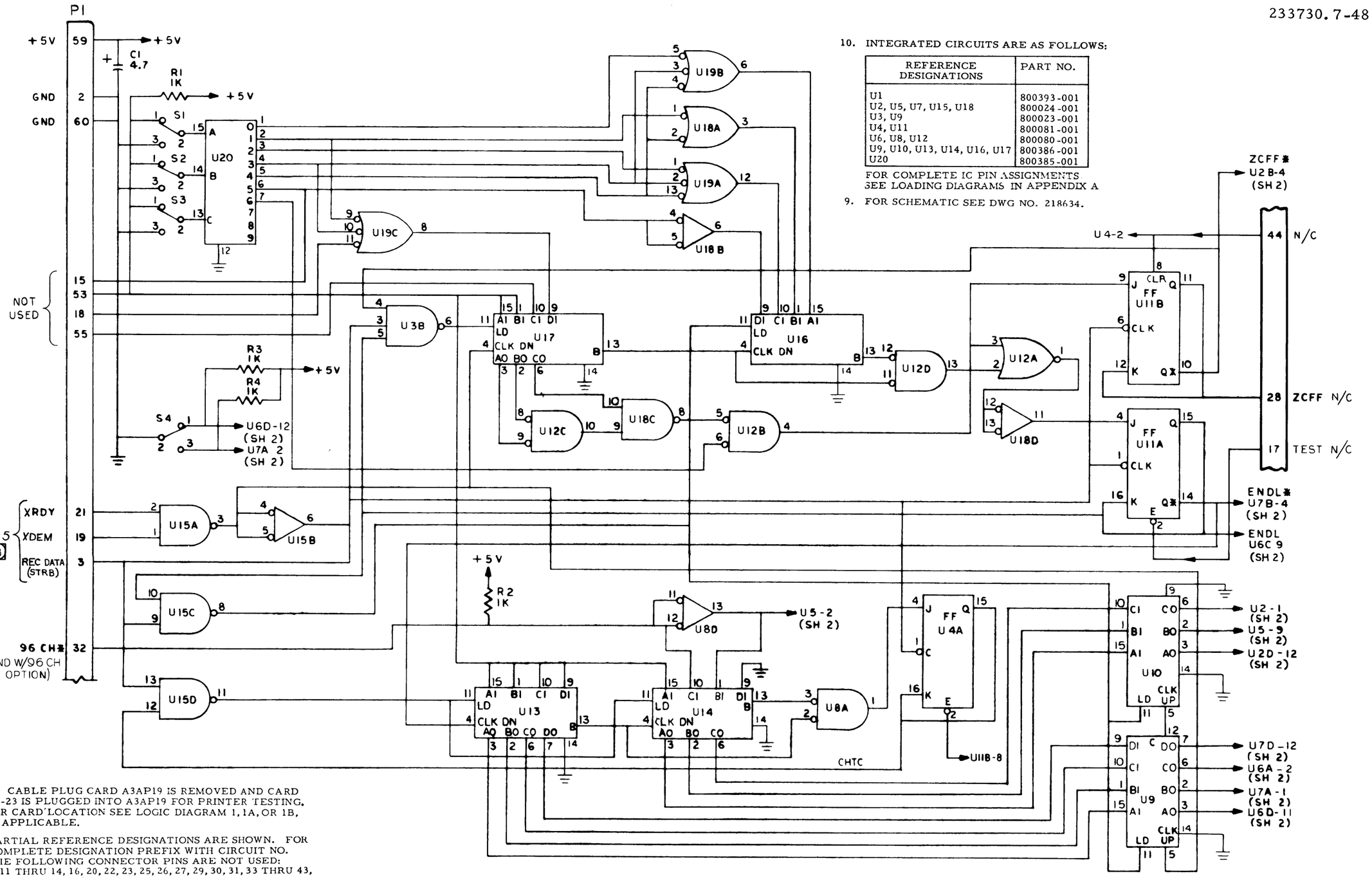
REFERENCE DESIGNATIONS	PART NO. AZ-164
U1	800400-001
U2	800080-001
U3	800024-001
U4, U5, U7, U9, U10, U11	800382-001
U6, U16	800081-001
U8	800022-001
U12, U13, U15	800703-001
U14	800023-001

FOR COMPLETE IC PIN ASSIGNMENTS SEE LOADING DIAGRAMS IN APPENDIX A

CIRCUIT CARD LOCATION:
A3A16
(ALL MODELS, ELECTRONICS GATE ASSEMBLY A3, CARD CAGE A , SLOT 16)

LOGIC DIAGRAM SHEET 47

AZ-164
VERTICAL FORMAT UNIT
12 CHANNEL (OPTION)



10. INTEGRATED CIRCUITS ARE AS FOLLOWS:

REFERENCE DESIGNATIONS	PART NO.
U1	800393-001
U2, U5, U7, U15, U18	800024-001
U3, U9	800023-001
U4, U11	800081-001
U6, U8, U12	800080-001
U9, U10, U13, U14, U16, U17	800386-001
U20	800385-001

FOR COMPLETE IC PIN ASSIGNMENTS SEE LOADING DIAGRAMS IN APPENDIX A

9. FOR SCHEMATIC SEE DWG NO. 218634.

(8) I/O CABLE PLUG CARD A3AP19 IS REMOVED AND CARD AL-23 IS PLUGGED INTO A3AP19 FOR PRINTER TESTING. FOR CARD LOCATION SEE LOGIC DIAGRAM 1, 1A, OR 1B, AS APPLICABLE.

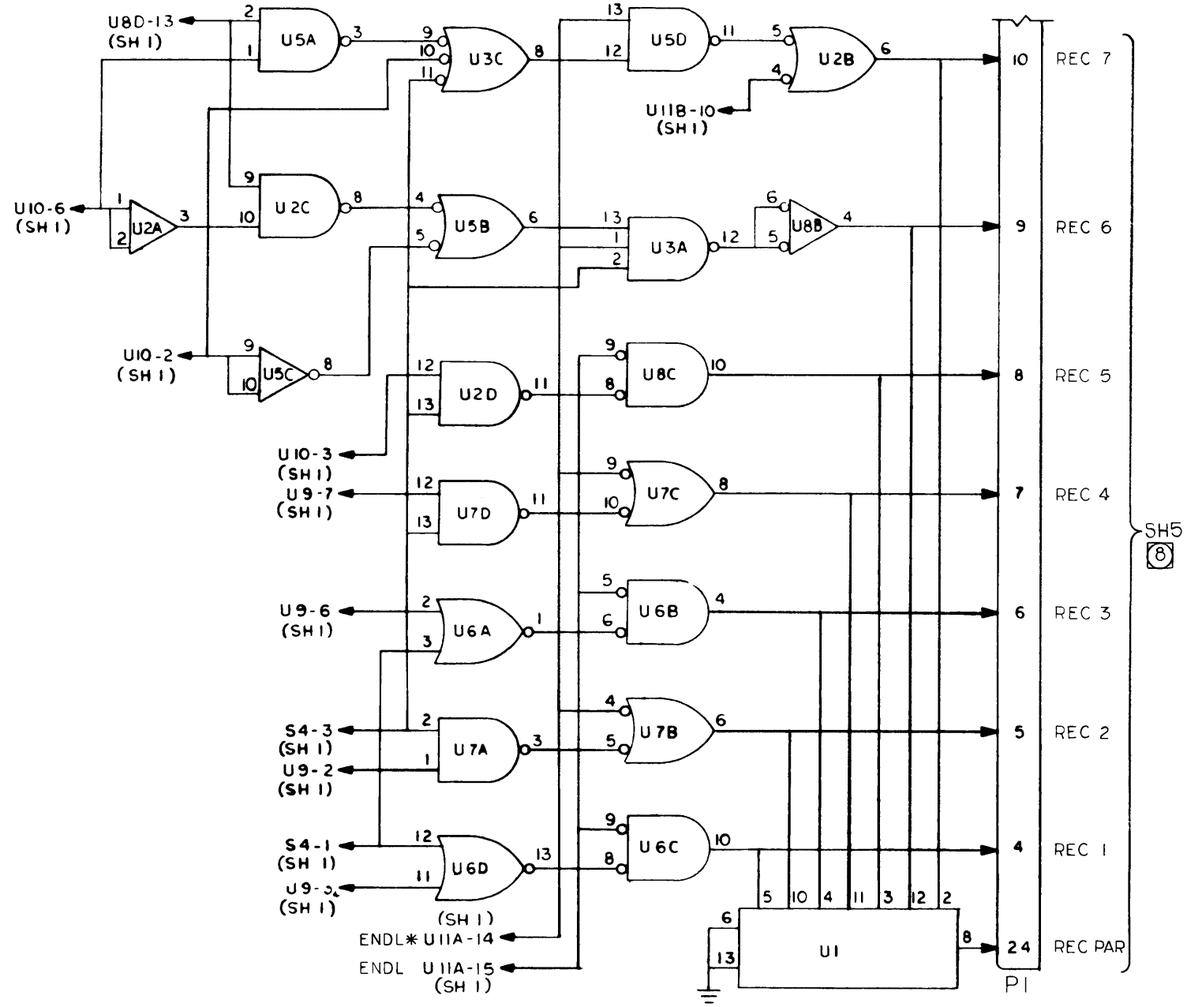
7. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION PREFIX WITH CIRCUIT NO.
6. THE FOLLOWING CONNECTOR PINS ARE NOT USED: 1, 11 THRU 14, 16, 20, 22, 23, 25, 26, 27, 29, 30, 31, 33 THRU 43, 45 THRU 52, 54, 56, 57, 58
5. ASSEMBLY DRAWING NUMBER 218630, REV H
4. INTERPRET ELECTRONIC SYMBOLS PER USAS Y32.2.
3. INTERPRET REFERENCE DESIGNATIONS PER USAS Y32.16.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS, 20%, 10 VOLTS.
1. ALL RESISTANCE VALUES ARE IN OHMS, 5%, 1/4 WATT.

NOTES: UNLESS OTHERWISE SPECIFIED

CIRCUIT CARD LOCATION: A3A19
(ALL MODELS, ELECTRONICS GATE ASSEMBLY A3, CARD CAGE A, SLOT 19)

LOGIC DIAGRAM SHEET 48

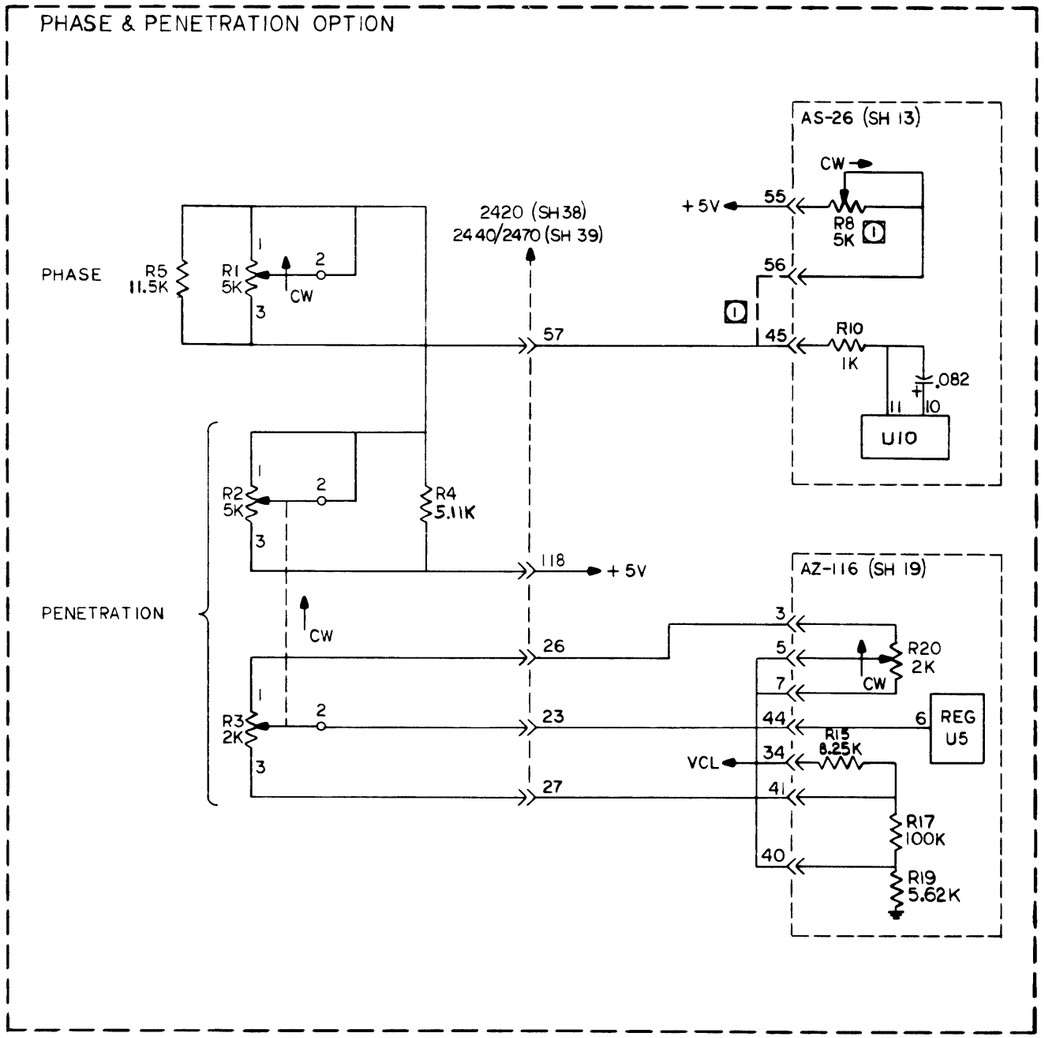
AL-23
SELF TEST (OPTION)
(SH 1 OF 2)

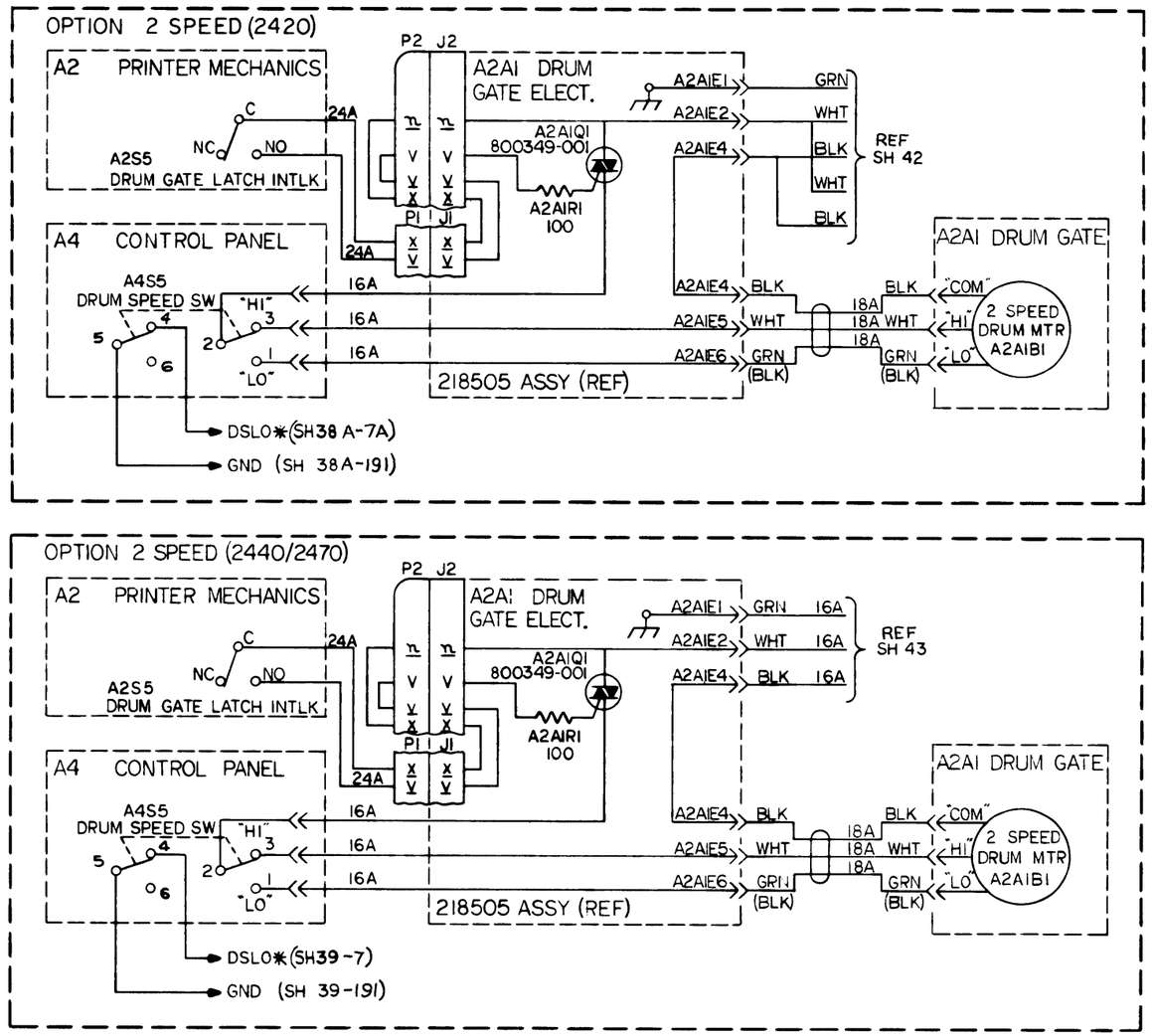


CIRCUIT CARD LOCATION: A3A19
(ALL MODELS, ELECTRONICS GATE ASSEMBLY A3, CARD CAGE A, SLOT 19)

LOGIC DIAGRAM SHEET 48

AL-23
SELF TEST (OPTION)
(SH 2 OF 2)





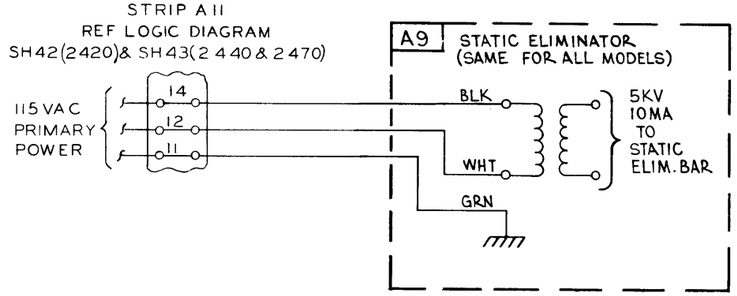
[1] R8 AND DOTTED CONNECTION ARE USED ONLY WHEN THERE ARE NO PHASE OR PENETRATION OPTIONS.

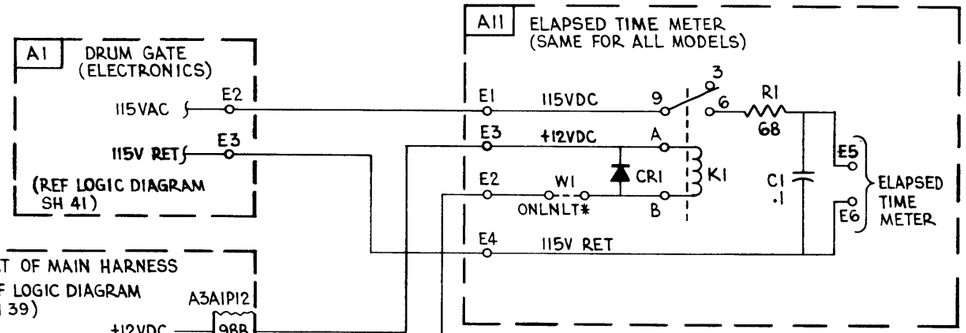
NOTES: UNLESS OTHERWISE SPECIFIED

LOGIC DIAGRAM SHEET 49

DRUM SPEED, PHASING, & PENETRATION CONTROLS (OPTION)

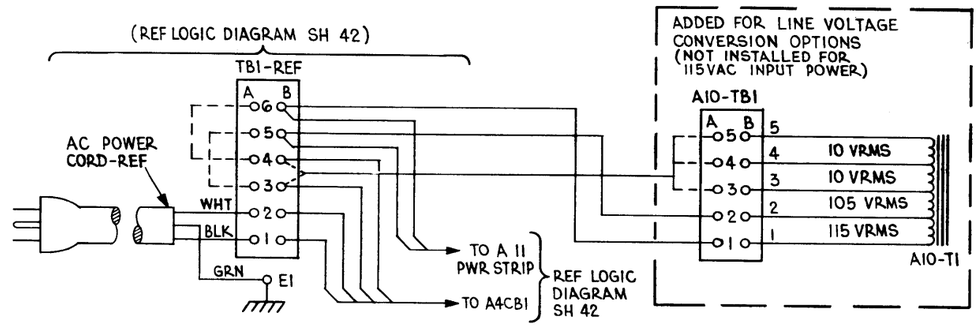
POWER DISTRIBUTION
STRIP A11
REF LOGIC DIAGRAM
SH42(2420)& SH43(2440&2470)





MODEL 2420 - LINE VOLTAGE CONVERSION OPTIONS

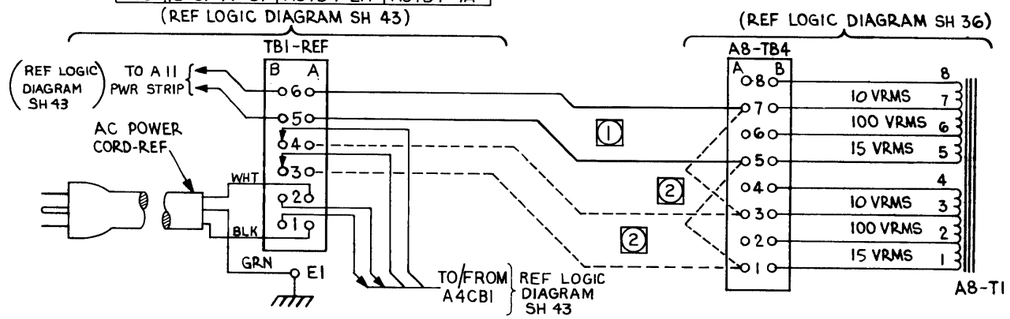
AC INPUT VRMS	JUMPER-TBI TERMINALS:	ADD WIRES: FROM	TO	FROM	TO
115	(3A-5A)(4A-6A)	NONE	NONE	NONE	NONE
230	(4A-6A)	TB1-3B	A1OTB1-4A		
220	(4A-6A)	TB1-3B	A1OTB1-3A	TB1-5B	A1OTB1-2A
240	(4A-6A)	TB1-3B	A1OTB1-5A	TB1-6B	A1OTB1-1A
100	(3A-5A)	TB1-4B	A1OTB1-3A		



MODELS 2440 AND 2470-LINE VOLTAGE CONVERSION OPTIONS

INPUT A.C. VRMS	JUMPER TERMINALS ON A8TB4:	HAMMER BANK POWER SUPPLY AC INPUT WIRES FROM: TBI-3A TO:	FROM: TBI-4A TO:
115	(1-5) (3-7)	A8TB4-1A	A8TB4-3A
230	(3-5)	-1A	-7A
220	(4-6)	-2A	-8A
240	(4-5)	-1A	-7A
100	(2-6) (3-7)	-2A	-3A
210	(4-6)	-2A	-7A
110	(2-6) (4-8)	A8TB4-2A	A8TB4-4A

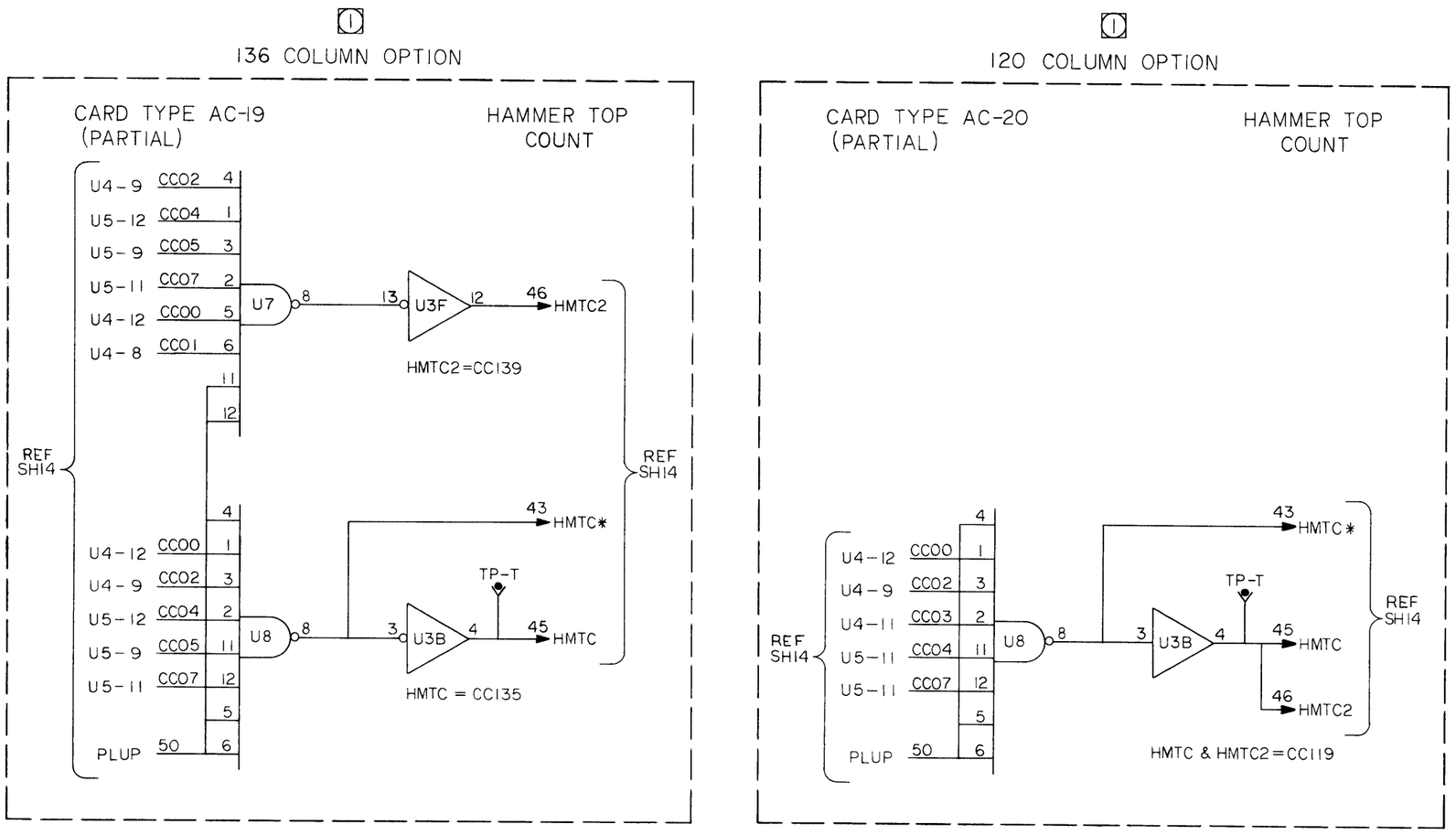
INPUT A.C. VRMS	JUMPER TERMINALS ON A8TB4:	HAMMER BANK POWER SUPPLY AC INPUT WIRES FROM: TBI-3A TO:	FROM: TBI-3A TO:
125	(1-5) (4-8)	A8TB4-1A	A8TB4-4A
200	(3-6)	-2A	-7A
215	(3-6)	-1A	-7A
225	(3-6)	-1A	-8A
235	(4-6)	-1A	-8A
250	(4-5)	A8TB4-1A	A8TB4-8A



[1] Solid Wires denote same interconnections for all voltage levels shown in chart above.

[2] Dotted Lines denote interconnection for 115V RMS only; may be changed as required by other voltage levels shown in chart above.

LOGIC DIAGRAM SHEET 50
STATIC ELIMINATOR, ELAPSED TIME METER, POWER & FREQUENCY KIT (LINE VOLTAGE CONVERSION) (OPTIONS)



3. FOR SCHEMATIC SEE DWG NOS. 231503, REV B AND
2. INTEGRATED CIRCUITS ARE AS FOLLOWS:

REFERENCE DESIGNATIONS	PART NO.
U1, U2	800023-001
U3	800387-001
U4, U5	800591-001
U6	800081-001
U7, U8, U14	800021-001
U9, U15	800020-001
U10, U11	800386-001
U12, U13	800370-001
U16	800024-001

FOR COMPLETE IC PIN ASSIGNMENTS SEE LOADING DIAGRAMS IN APPENDIX A

(1) CARD TYPES AC-19 & AC-20 ARE IDENTICAL TO CARD TYPE AC-16 EXCEPT FOR LOGIC DETAILS SHOWN IN THIS DRAWING. REFER TO AC-16 LOGIC DIAGRAM SHEET 14 FOR LOGIC & INTERCONNECTION DATA COMMON TO ALL THREE CARD TYPES.

NOTES: UNLESS OTHERWISE SPECIFIED

CIRCUIT CARD LOCATION: A3A21
(ALL MODELS, ELECTRONICS GATE ASSEMBLY A3, CARD CAGE A, SLOT 21)

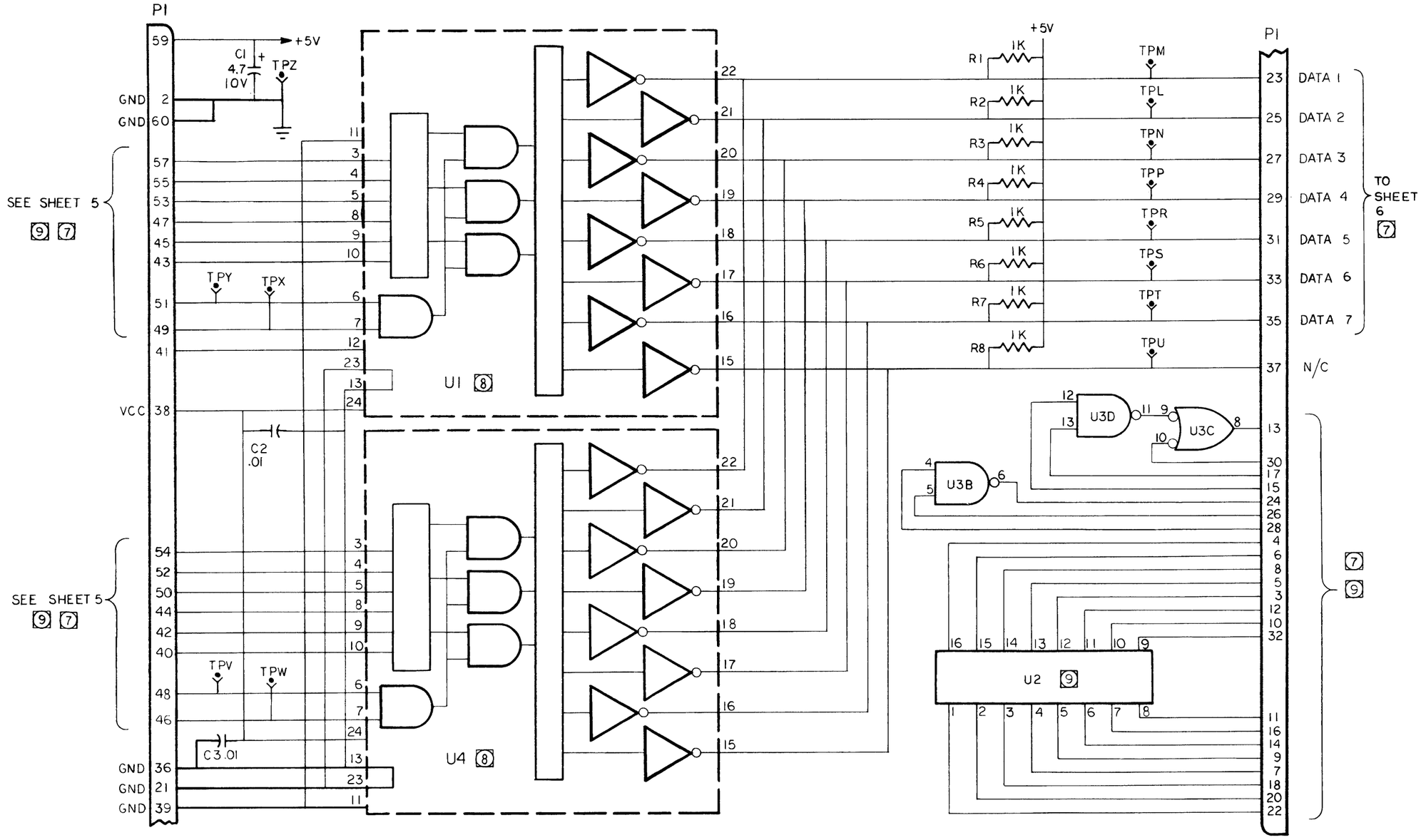
LOGIC DIAGRAM SHEET 51

AC-19
COUNTER COMPARE
(HAMMER TOP COUNT LOGIC ONLY)

b^7 b^6 b^5	0 0 0	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
b^4 b^3 b^2 b^1							
0 0 0 0		SPACE	0	@	P		p
0 0 0 1		!	1	A	Q	a	q
0 0 1 0		"	2	B	R	b	r
0 0 1 1		#	3	C	S	c	s
0 1 0 0		$	4	D	T	d	t
0 1 0 1		%	5	E	U	e	u
0 1 1 0		&	6	F	V	f	v
0 1 1 1		'	7	G	W	g	w
1 0 0 0		(	8	H	X	h	x
1 0 0 1		)	9	I	Y	i	y
1 0 1 0	LF	*	:	J	Z	j	z
1 0 1 1		+	;	K	[	k	{
1 1 0 0	FF	,	<	L	\	l	|
1 1 0 1	CR	-	=	M	]	m	}
1 1 1 0		.	>	N	↑	n	~
1 1 1 1		/	?	O	←	o	□

LOGIC DIAGRAM SHEET 52

CODE SET, 96 CHARACTER (OPTION)



9 U2 PART TYPE AND NOTED PIN CONNECTIONS ARE DETERMINED AT TIME OF ORDER. REFER TO ADDENDA FOR INFORMATION REGARDING THESE ITEMS.

8 U1 & U4 ARE READ-ONLY-MEMORY INTEGRATED CIRCUITS THAT ARE CUSTOM-PROGRAMMED AT TIME OF SALES ORDER. REFER TO ADDENDA FOR CODE CONVERSION APPLICABLE FOR A SPECIFIC PRINTER.

7 FOR BLOCK DIAGRAM SEE SHEET 53A.

6. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION PREFIX WITH CIRCUIT NO.
5.
4. INTERPRET ELECTRONIC SYMBOLS PER USAS Y32.2.
3. INTERPRET REFERENCE DESIGNATIONS PER USAS Y32.16.
2.
1. ALL RESISTANCE VALUES ARE IN OHMS, 5%, 1/4 WATT.

NOTES: UNLESS OTHERWISE SPECIFIED

10. INTEGRATED CIRCUITS ARE AS FOLLOWS:

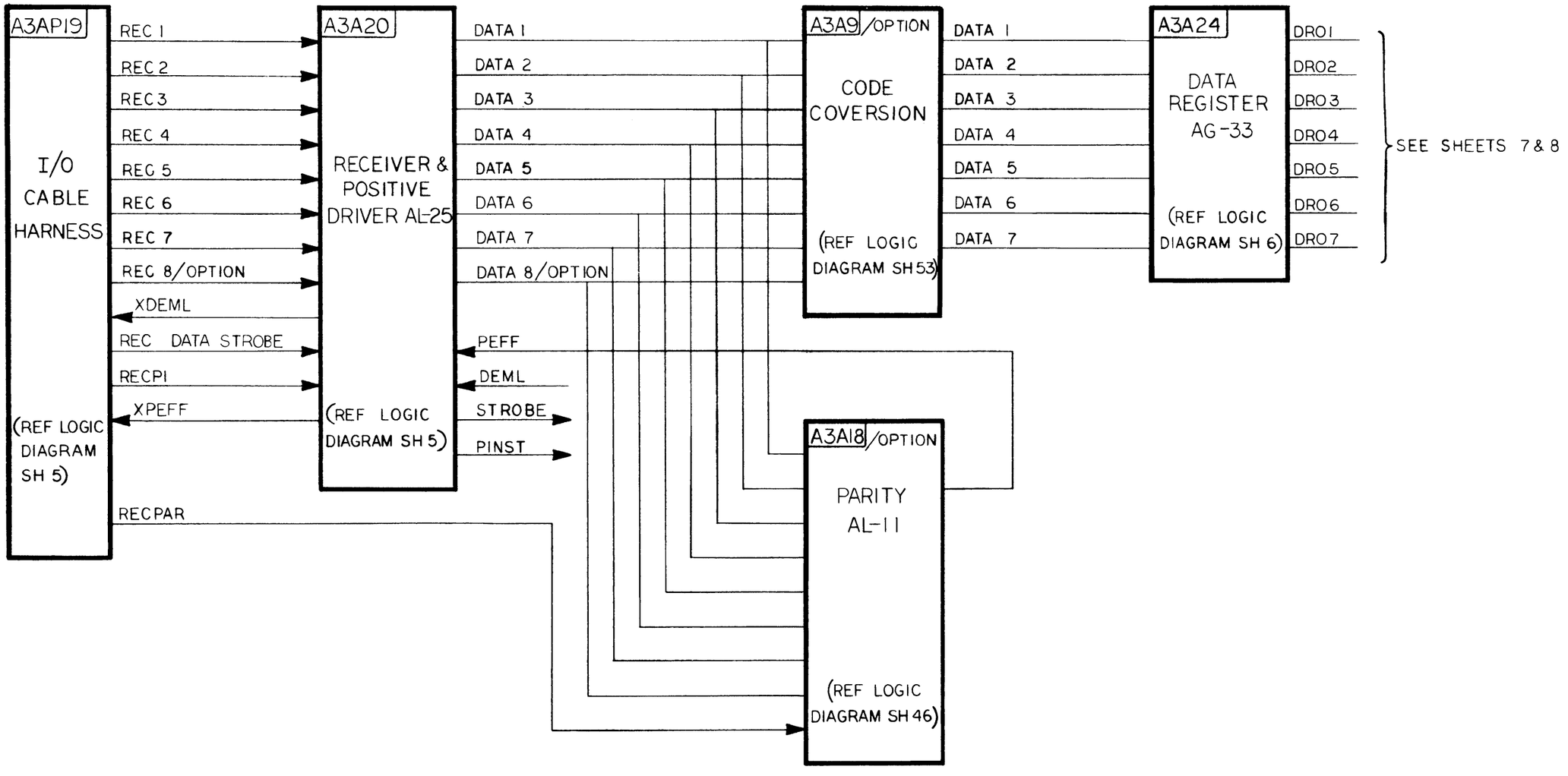
REFERENCE DESIGNATIONS	PART NO.
U1	800814-XXX
U3	800024-001
	800370-001
U2	800385-001
	800081-001
U4	801310-XXX

FOR COMPLETE IC PIN ASSIGNMENTS SEE LOADING DIAGRAMS IN APPENDIX A

CIRCUIT CARD LOCATION:
A3A9
(ALL MODELS, ELECTRONICS GATE ASSEMBLY A3, CARD CAGE A, SLOT 9)

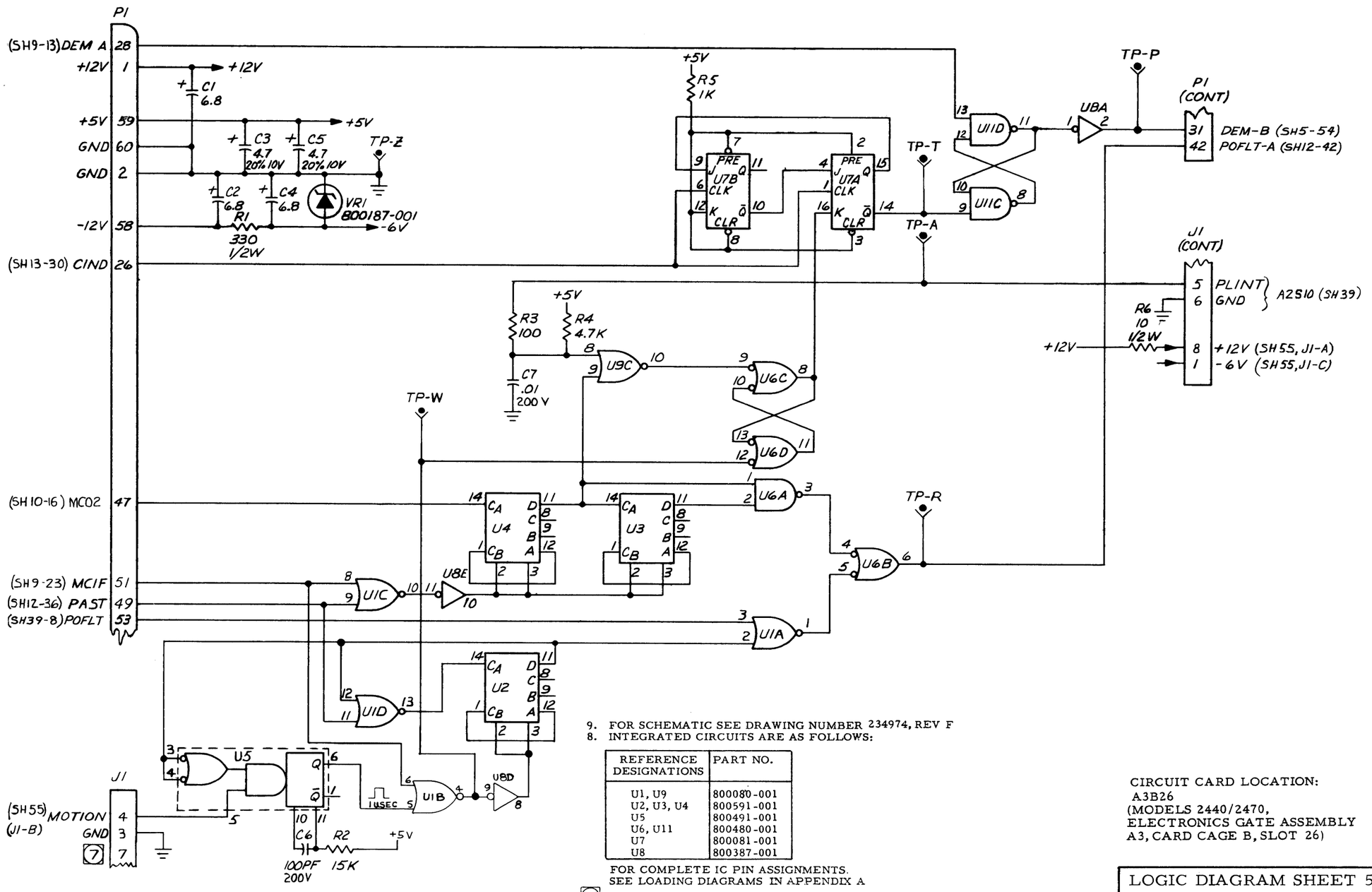
LOGIC DIAGRAM SHEET 53

CODE CONVERSION (OPTION)



LOGIC DIAGRAM SHEET 53A

CODE CONVERSION
(OPTION)



9. FOR SCHEMATIC SEE DRAWING NUMBER 234974, REV F
8. INTEGRATED CIRCUITS ARE AS FOLLOWS:

REFERENCE DESIGNATIONS	PART NO.
U1, U9	800080-001
U2, U3, U4	800591-001
U5	800491-001
U6, U11	800480-001
U7	800081-001
U8	800387-001

FOR COMPLETE IC PIN ASSIGNMENTS.
SEE LOADING DIAGRAMS IN APPENDIX A

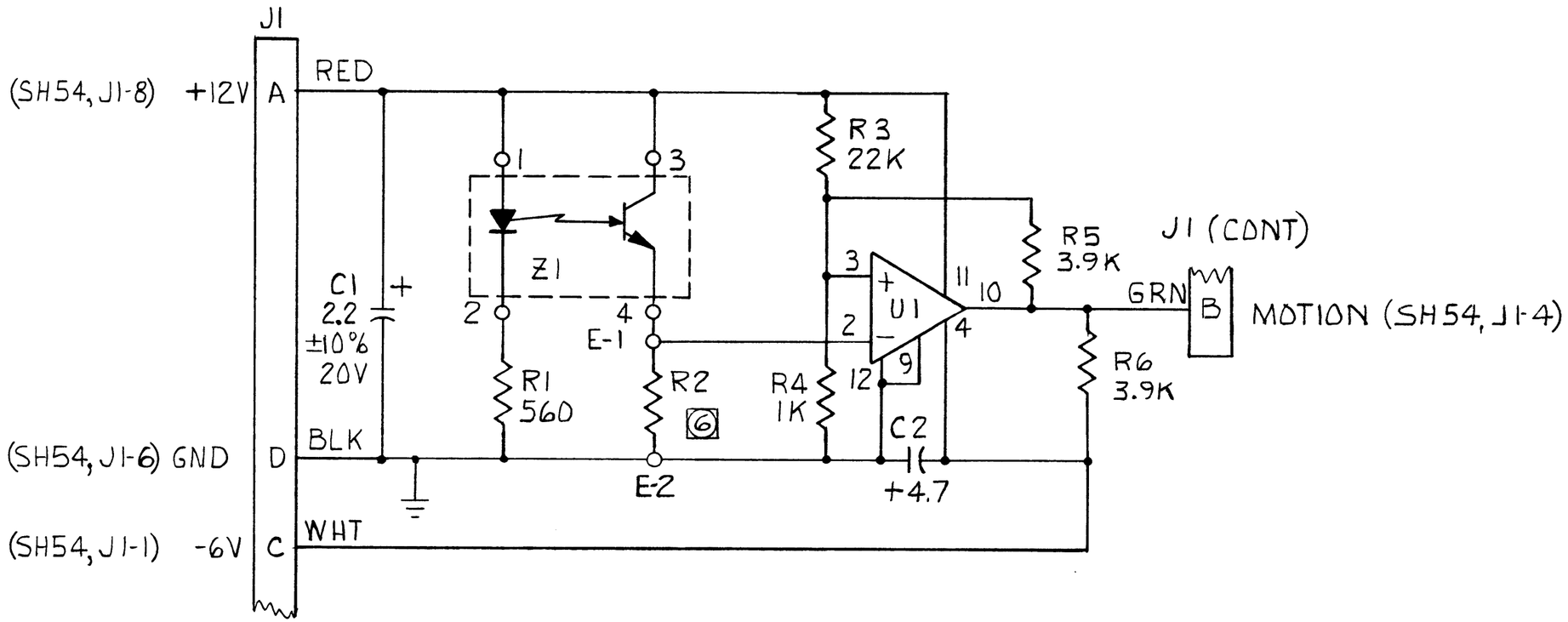
(7) PIN 7 IS KEY.
6. ASSEMBLY DRAWING NUMBER 234970, REV B
5. INTERPRET ELECTRONIC SYMBOLS PER 850026.
4. INTERPRET REFERENCE DESIGNATIONS PER 850027.
3. ALL DIODES ARE 800093-001.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS, ±10%, 20 VOLTS.
1. ALL RESISTANCE VALUES ARE IN OHMS, ± 5%, 1/4 WATT.

NOTES: UNLESS OTHERWISE SPECIFIED

CIRCUIT CARD LOCATION:
A3B26
(MODELS 2440/2470,
ELECTRONICS GATE ASSEMBLY
A3, CARD CAGE B, SLOT 26)

LOGIC DIAGRAM SHEET 54

AG-55
PROTECT



FOR COMPLETE IC PIN ASSIGNMENTS
SEE LOADING DIAGRAMS IN APPENDIX A

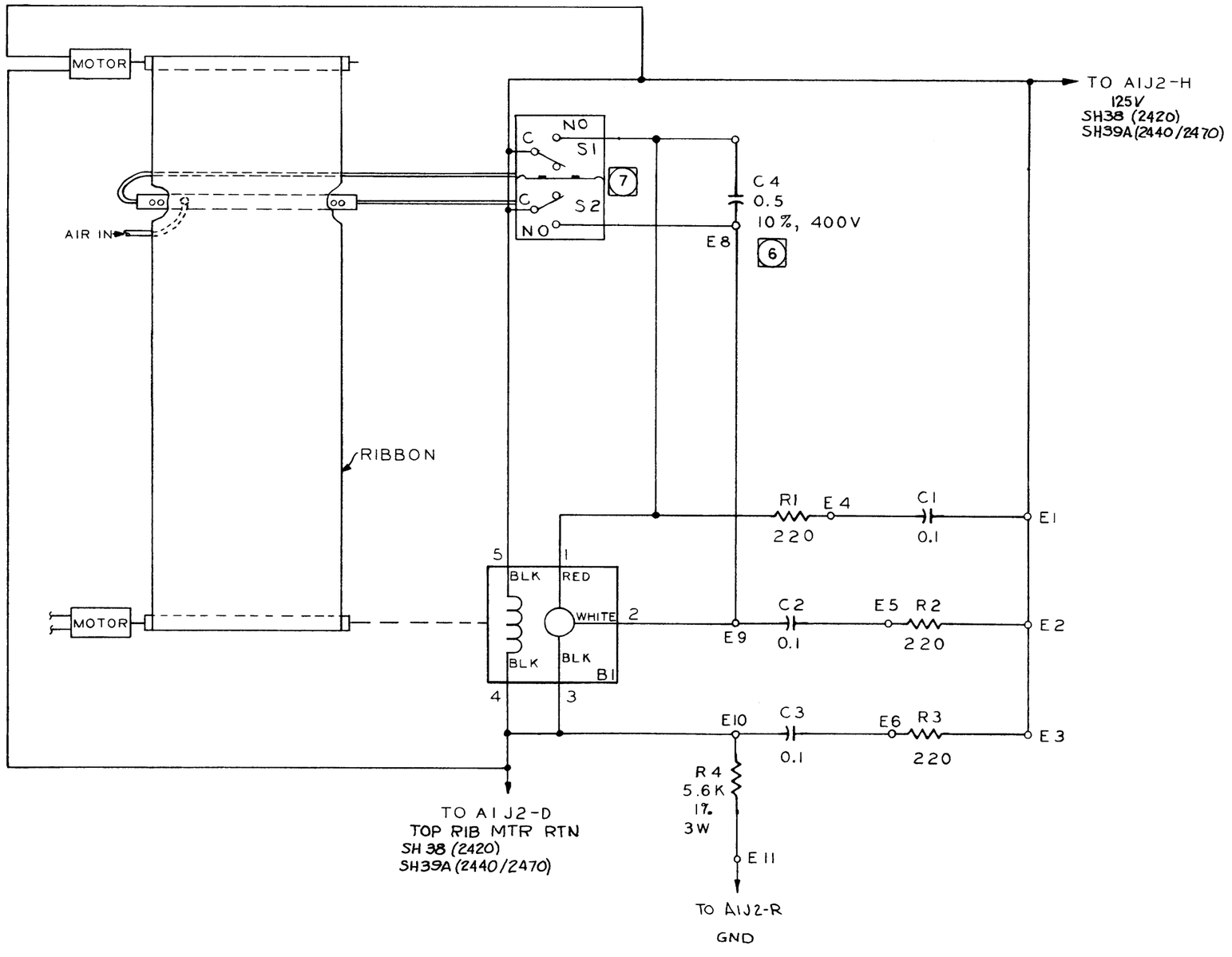
9. Z1 PART NO. 800961-001.
8. U1 PART NO. 800186-002.
7. FOR SCHEMATIC SEE DRAWING NUMBER 234974, REV F
6. R2 TO BE SELECTED AT TEST LEVEL.
5. ASSEMBLY DRAWING NUMBER IS 235215, REV C OR 235525, REV M
4. INTERPRET ELECTRONIC SYMBOLS PER 850026.
3. INTERPRET REFERENCE DESIGNATIONS PER 850027.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS, ±20%, 10 VOLTS.
1. ALL RESISTANCE VALUES ARE IN OHMS, ± 5%, 1/4 WATT.

NOTES: UNLESS OTHERWISE SPECIFIED

ASSEMBLY LOCATION:
A2A2
(MODELS 2440/2470,
PRINTER MECHANICS ASSEMBLY
A2)

LOGIC DIAGRAM SHEET 55

PAPER MOTION SENSOR



7 DIAPHRAGM SHOWN IN NON-ACTUATED POSITION.
6 CAPACITOR, C4, IS SUPPLIED WITH SYNCHRONOUS MOTOR B1.

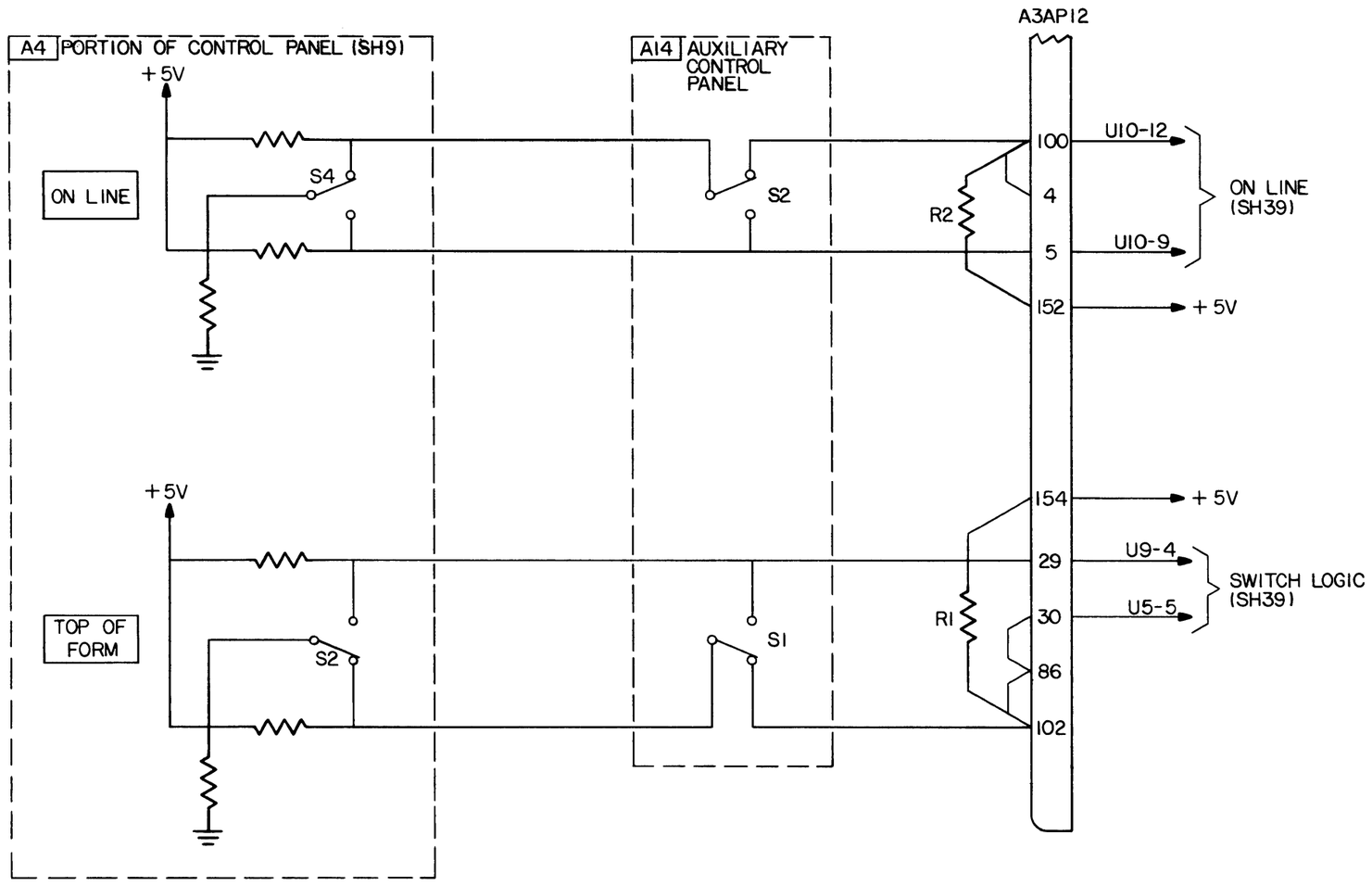
5. ASSEMBLY DRAWING NUMBER IS 236524, REV J
4. INTERPRET ELECTRONIC SYMBOLS PER 850026.
3. INTERPRET REFERENCE DESIGNATIONS PER 850027.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS, 20%, 400 VOLTS.
1. ALL RESISTANCE VALUES ARE IN OHMS, ± 5%, 1/2 WATT.

NOTES: UNLESS OTHERWISE SPECIFIED

ASSEMBLY LOCATION:
A2A1
(MODELS 2440/2470,
DRUM GATE ASSEMBLY
A2A1)

LOGIC DIAGRAM SHEET 56

RIBBON SERVO ASSEMBLY



4. ASSEMBLY DRAWING NUMBER 241785, REV A
3. INTERPRET ELECTRONIC SYMBOLS PER 850026.
2. INTERPRET REFERENCE DESIGNATIONS PER 850027.
1. ALL RESISTANCE VALUES ARE IN OHMS, ±5%, 1/4 WATT, R1 & R2 ONLY.

NOTES: UNLESS OTHERWISE SPECIFIED

LOGIC DIAGRAM SHEET 57

AUXILIARY CONTROL PANEL (OPTION)

SECTION VIII

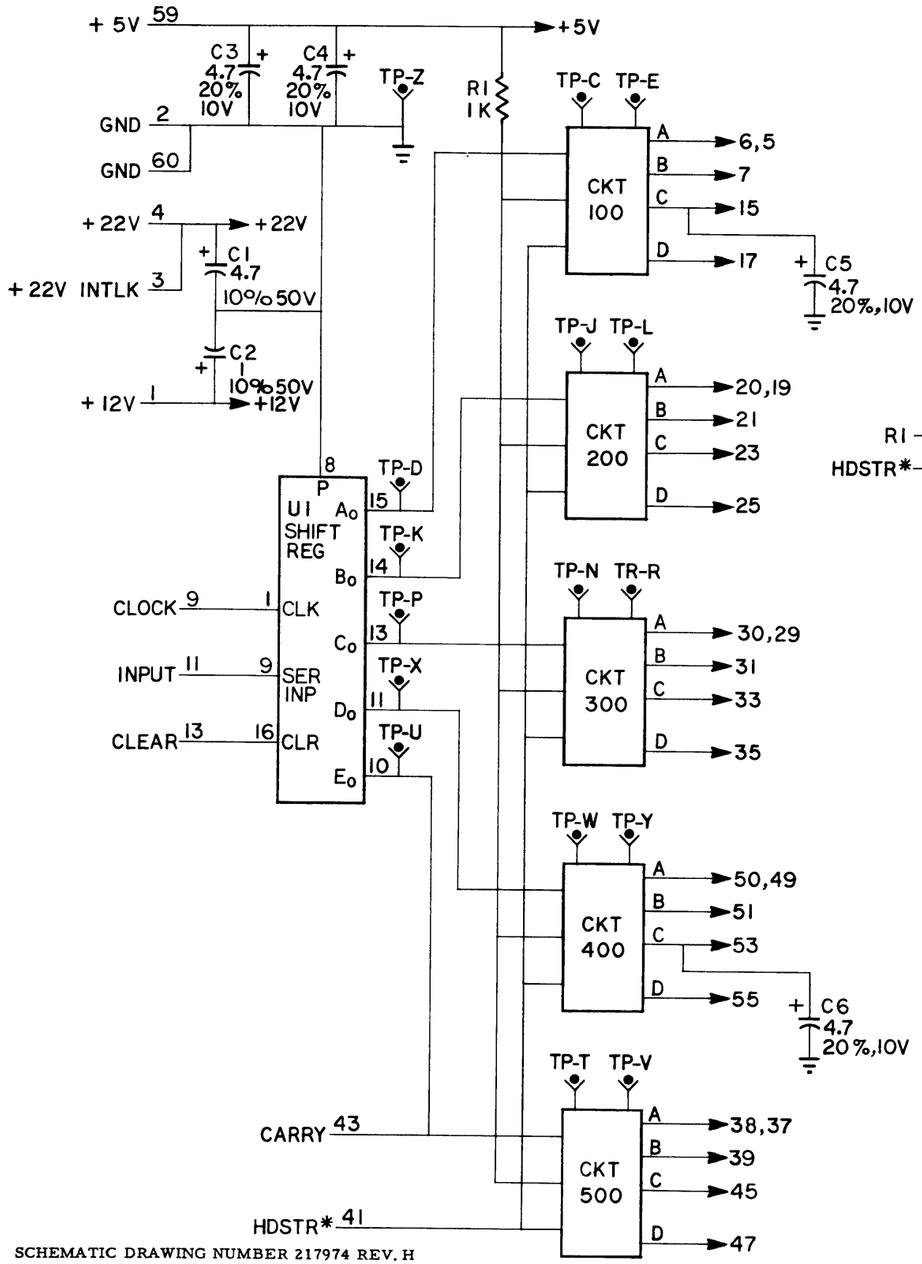
SCHEMATIC DIAGRAMS

8-1 INTRODUCTION

8-2 This section contains schematic diagrams of circuit assemblies not represented in detail in section VII (logic diagrams). They support those logic diagram sheets shown only in block form or in simplified form as in the case of the AH-22 Hammer Driver Card. Table 8-1 lists the schematic diagrams contained in this section and also provides a reference column for the applicable logic diagrams.

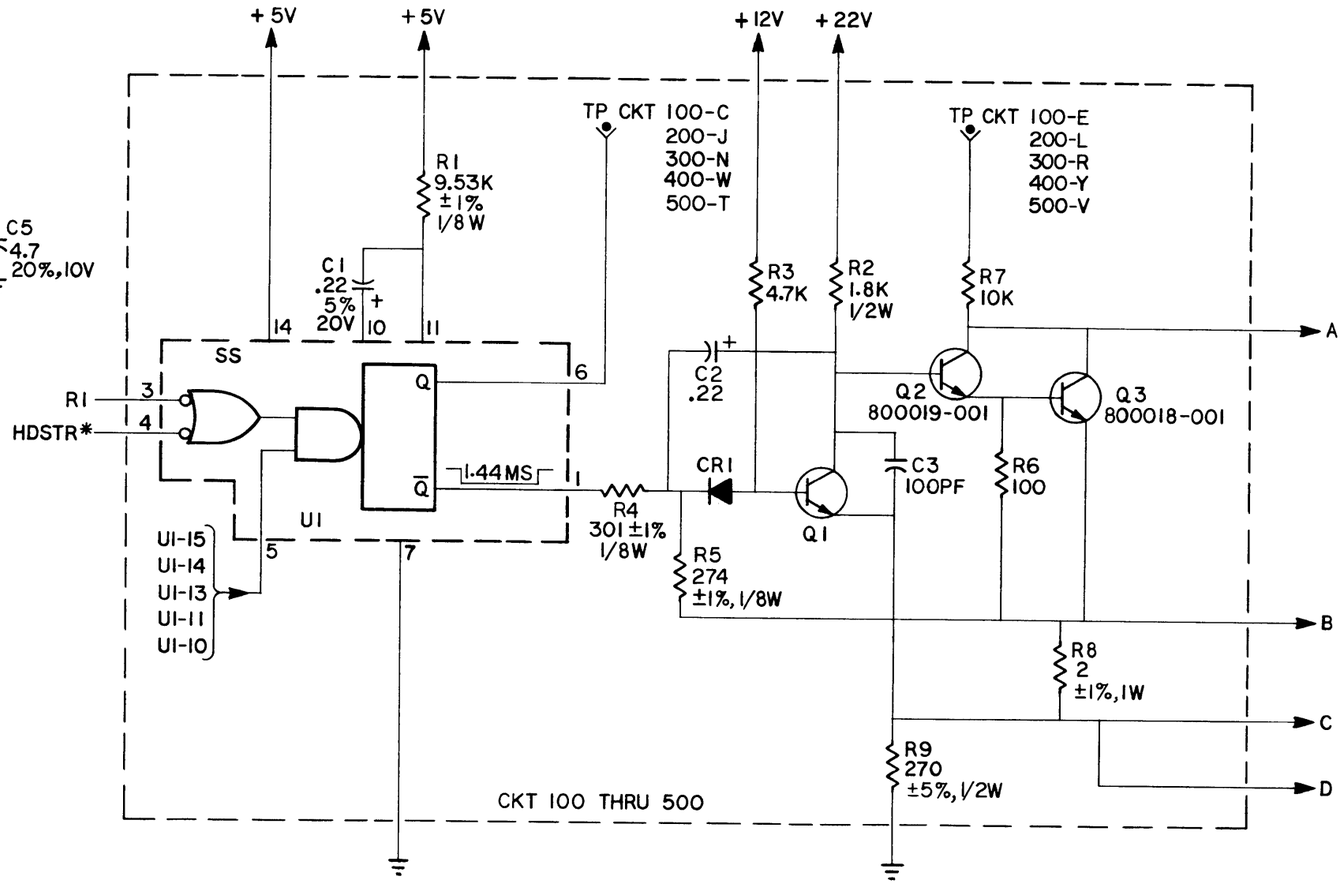
TABLE 8-1. SCHEMATIC DIAGRAMS

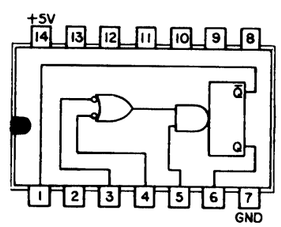
Circuit Card Assembly	Page	Applicable Logic Diagram Sheet
Hammer Driver AH-22	8-2	23, 24, or 25
Bridge Board AV-21	8-3	33
Power Supply Regulator AV-17	8-4	32
Voltage Regulator and Driver AZ-111	8-5	32
+5V Regulator AZ-113	8-6	32
Bridge Board AZ-126	8-7	32
Hammer Bank Power Supply Regulator AV-18	8-8	36
Positive Paper Feed Power Amplifier AZ-49	8-9	28
Negative Paper Feed Power Amplifier AZ-51	8-10	28



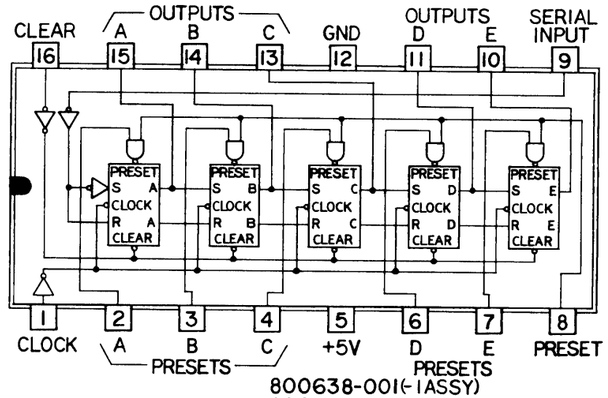
10. SCHEMATIC DRAWING NUMBER 217974 REV. H
9. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION PREFIX WITH CIRCUIT NO.
8. THE FOLLOWING CONNECTOR PINS ARE NOT USED: 8, 10, 12, 14, 16, 18, 22, 24, 26, 27, 28, 32, 34, 36, 40, 42, 44, 46, 48, 52, 54, 56, 57, 58
7. ASSEMBLY DRAWING NUMBER 217970.
6. INTERPRET ELECTRONIC SYMBOLS PER USAS 32.2.
5. INTERPRET REFERENCE DESIGNATIONS PER USAS Y32.16.
4. ALL TRANSISTORS ARE 800132-001.
3. ALL DIODES ARE 800093-001.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS, 5%, 50 VOLTS.
1. ALL RESISTANCE VALUES ARE IN OHMS, 5%, 1/4 WATT.

NOTES: UNLESS OTHERWISE SPECIFIED





U101, U201, U301, U401, U501
800491-001(-1ASSY)
800491-002(-2ASSY)

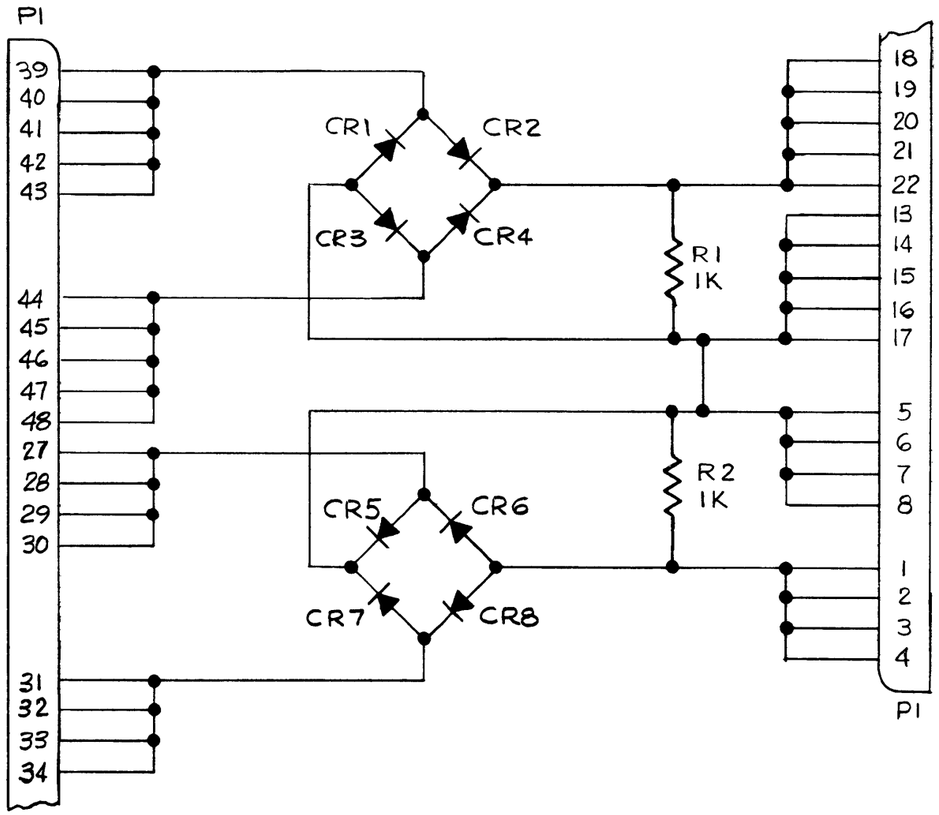


800638-001(-1ASSY)
800638-002(-2ASSY)
UI

FOR WIRING INTERCONNECTIONS SEE LOGIC DIAGRAM SHEET 23, 24, OR 25, AS APPLICABLE

CIRCUIT CARD LOCATION: A3A3 TO A3A7 (MODEL 2420)
A3A3 TO A3A12
A3B3 TO A3B7
(MODELS 2440/2470)

SCHEMATIC DIAGRAM
AH-22
HAMMER DRIVER
(ALL MODELS)



7. SCHEMATIC DRAWING NUMBER 236149 REV A
6. RECTIFIER DIODES CR1, CR3, CR6, CR8 ARE 801075-001.
   RECTIFIER DIODES CR2, CR4, CR5, CR7 ARE 801075-001.
5. ALL RESISTORS ARE 800084-103.
4. ASSEMBLY DRAWING NUMBER 236145.
3. INTERPRET ELECTRONIC SYMBOLS PER 850026.
2. INTERPRET REFERENCE DESIGNATIONS PER 850027.
1. ALL RESISTANCE VALUES ARE IN OHMS, 1%, 3 WATTS.

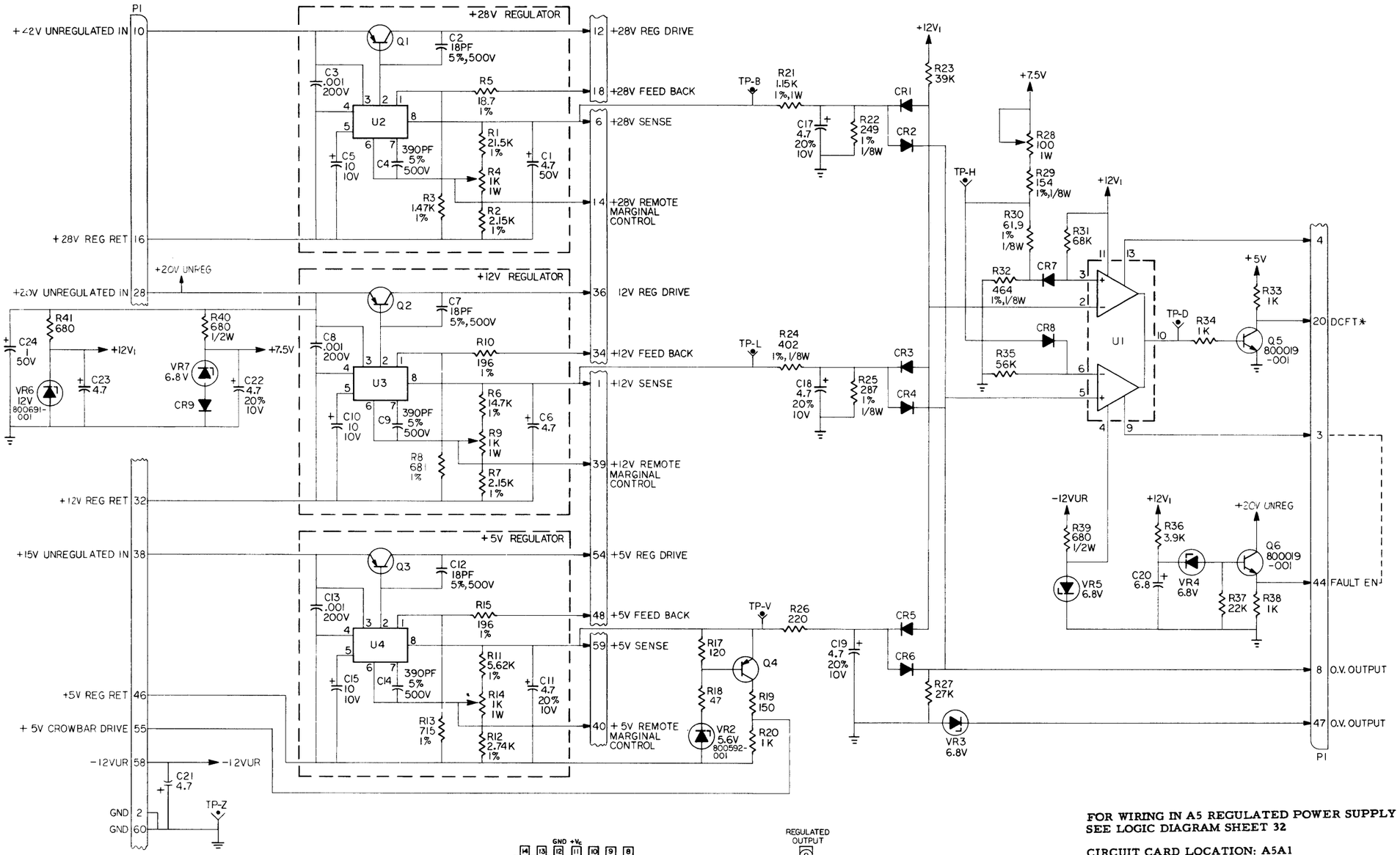
NOTES: UNLESS OTHERWISE SPECIFIED

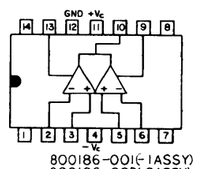
FOR WIRING IN A6 PAPER FEED CONTROL
SEE LOGIC DIAGRAM SHEET 33

CIRCUIT CARD LOCATION:A6A2

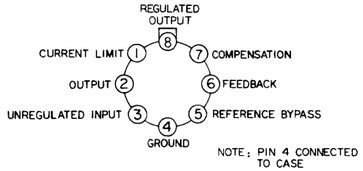
SCHEMATIC DIAGRAM

AV-21
BRIDGE BOARD
(MODELS 2440/2470)





800186-001(-1ASSY)
800186-002(-2ASSY)
U1



800499-001(-1&-2ASSY)
U2, U3, U4

FOR WIRING IN A5 REGULATED POWER SUPPLY SEE LOGIC DIAGRAM SHEET 32

CIRCUIT CARD LOCATION: A5A1

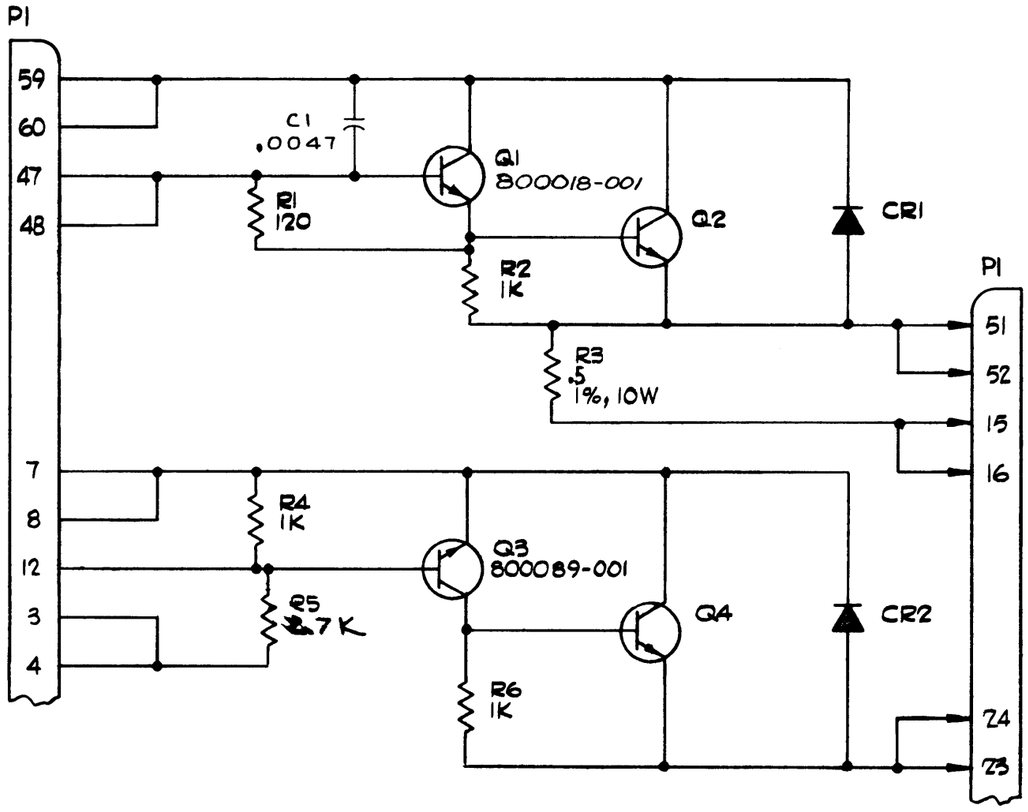
10. SCHEMATIC DRAWING NUMBER 218009 REV. P

9. ALL ZENER DIODES ARE 800486-001.
8. THE FOLLOWING CONNECTOR PINS ARE NOT USED: 5, 7, 9, 11, 13, 15, 17, 19, 21, 22, 23, 24, 25, 26, 27, 29, 31, 33, 35, 37, 41, 42, 43, 45, 50, 52, 53, 56, 57
7. ASSEMBLY DRAWING NUMBER 218005.
6. INTERPRET ELECTRONIC SYMBOLS PER USAS 32. 2.
5. INTERPRET REFERENCE DESIGNATIONS PER USAS Y32. 16.
4. ALL TRANSISTORS ARE 800089-001.
3. ALL DIODES ARE 800093-001.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS, 10%, 20 VOLTS.
1. ALL RESISTANCE VALUES ARE IN OHMS, 5%, 1/4 WATT.

NOTES: UNLESS OTHERWISE SPECIFIED

SCHEMATIC DIAGRAM

AV-17
POWER SUPPLY REGULATOR
(MODELS 2440/2470)



10. SCHEMATIC DRAWING NUMBER 217999 REV. G

9. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION PREFIX WITH CIRCUIT NO.
8. THE FOLLOWING CONNECTOR PINS ARE NOT USED: 5, 6, 9, 10, 11, 13, 14, 17 THRU 22, 25 THRU 30, 32 THRU 46, 49, 50, 55 THRU 58.
7. ASSEMBLY DRAWING NUMBER 217995.
6. INTERPRET ELECTRONIC SYMBOLS PER USAS Y32.2.
5. INTERPRET REFERENCE DESIGNATIONS PER USAS Y32.16.
4. ALL TRANSISTORS ARE 800497-001.
3. ALL DIODES ARE 800094-001.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS, 10%, 200 VOLTS.
1. ALL RESISTANCE VALUES ARE IN OHMS, 5%, 1/4 WATT.

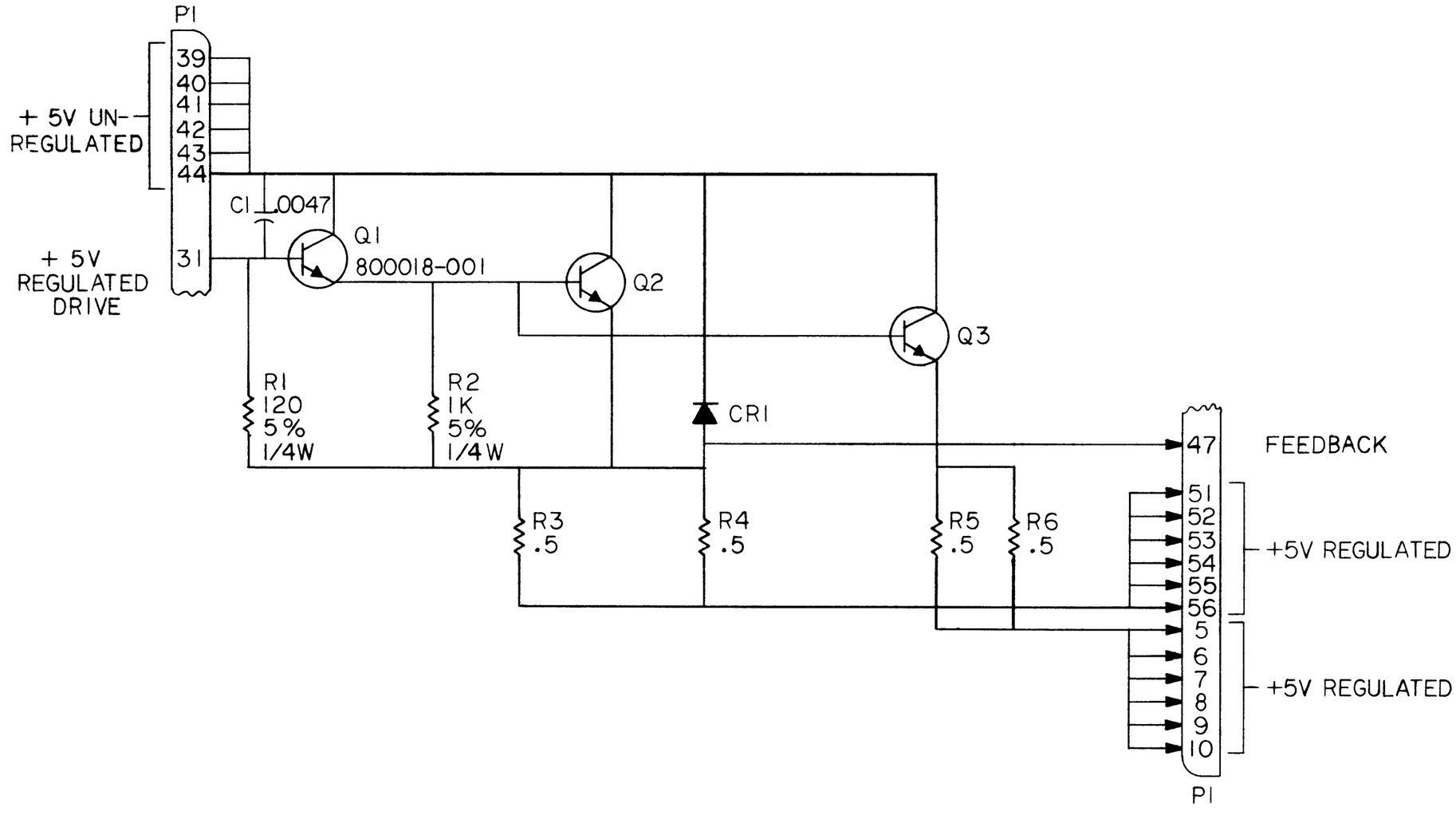
NOTES: UNLESS OTHERWISE SPECIFIED

FOR WIRING IN A5 REGULATED POWER SUPPLY SEE LOGIC DIAGRAM SHEET 32

CIRCUIT CARD LOCATION: A5A3, A5A4

SCHEMATIC DIAGRAM

AZ-111
VOLTAGE REGULATOR & DRIVER
(MODELS 2440/2470)



9. SCHEMATIC DRAWING NUMBER 217994 REV. D
8. ALL CAPACITANCE VALUES ARE IN MICROFARADS, 10%, 200 VOLTS.
7. THE FOLLOWING CONNECTOR PINS ARE NOT USED: 1, 2, 3, 4, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 32, 33, 34, 35, 36, 37, 38, 45, 46, 48, 49, 50, 57, 58, 59, 60
6. ASSEMBLY DRAWING NUMBER 217990.
5. INTERPRET ELECTRONIC SYMBOLS PER USAS Y32. 2.
4. INTERPRET REFERENCE DESIGNATIONS PER USAS Y32. 16.
3. ALL TRANSISTORS ARE 800019-001.
2. ALL DIODES ARE 800743-001.
1. ALL RESISTANCE VALUES ARE IN OHMS, 1%, 10 WATTS.

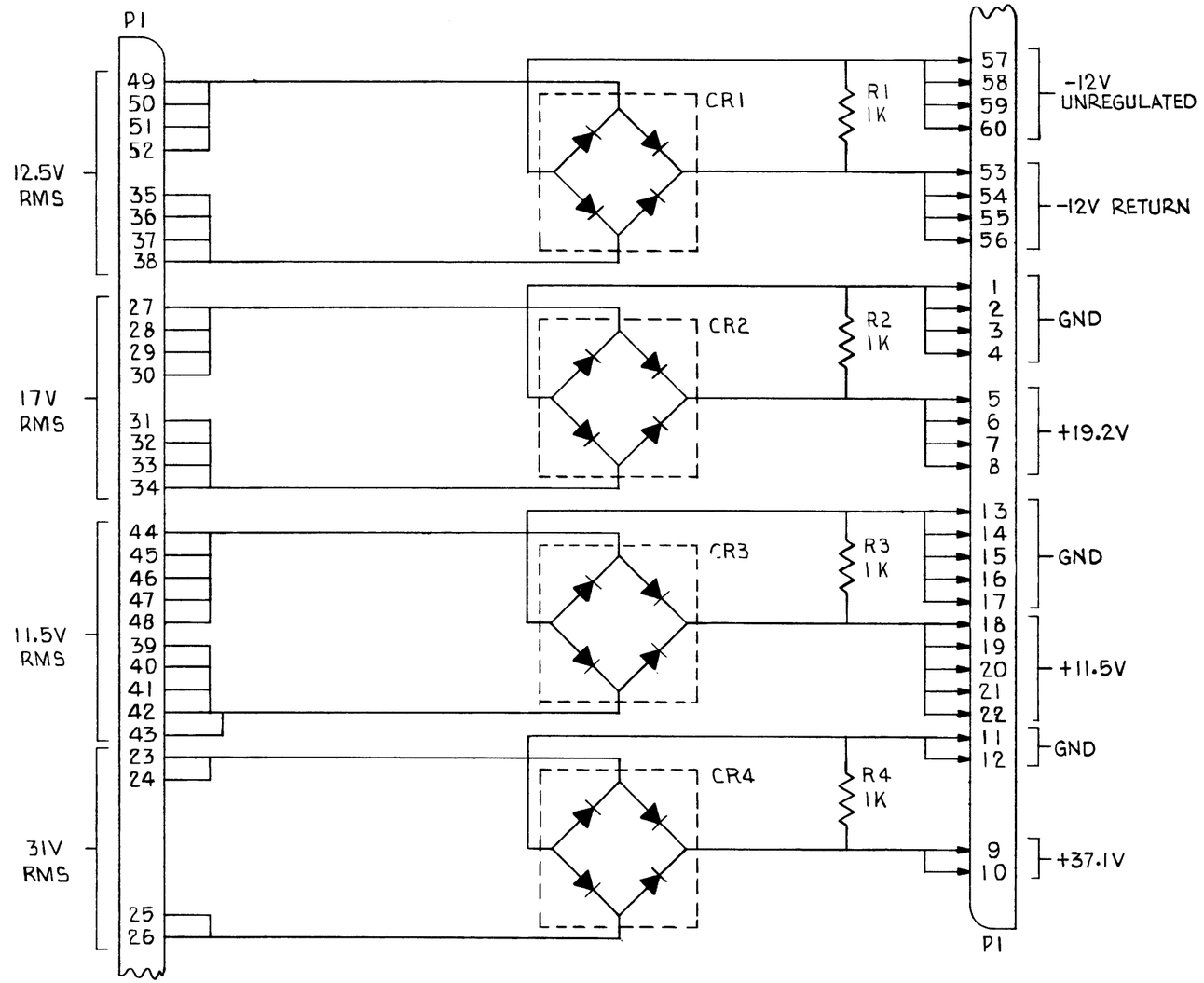
NOTES: UNLESS OTHERWISE SPECIFIED

FOR WIRING IN REGULATED POWER SUPPLY SEE LOGIC DIAGRAM SHEET 32

CIRCUIT CARD LOCATION:A5A2

SCHEMATIC DIAGRAM

AZ-113
+5V REGULATOR
(MODELS 2440/2470)



8. SCHEMATIC DRAWING NUMBER 218489 REV. E
7. ASSEMBLY DRAWING NUMBER 218485.
6. INTERPRET ELECTRONIC SYMBOLS PER USAS Y32.2.
5. INTERPRET REFERENCE DESIGNATIONS PER USAS Y32.16.
4.
3. ALL DIODES ARE 800516-001.
2.
1. ALL RESISTANCE VALUES ARE IN OHMS, 1%, 3 WATTS.

NOTES: UNLESS OTHERWISE SPECIFIED

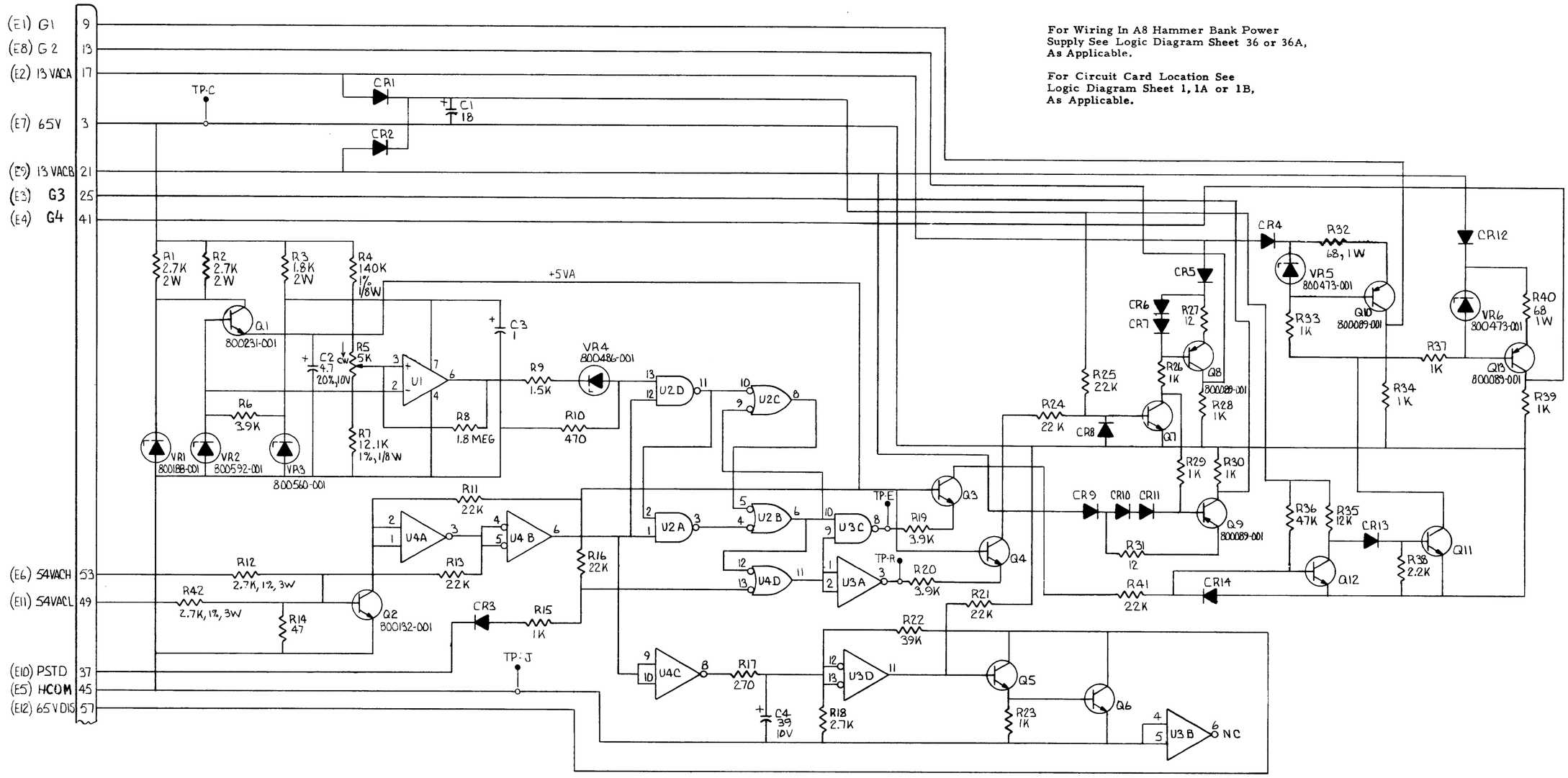
FOR WIRING IN A5 REGULATED POWER SUPPLY SEE LOGIC DIAGRAM SHEET 32

CIRCUIT CARD LOCATION: A5A5

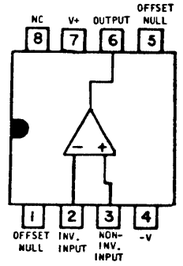
SCHEMATIC DIAGRAM
AZ-126
BRIDGE BOARD
(MODELS 2440/2470)

For Wiring In A8 Hammer Bank Power Supply See Logic Diagram Sheet 36 or 36A, As Applicable.

For Circuit Card Location See Logic Diagram Sheet 1, 1A or 1B, As Applicable.

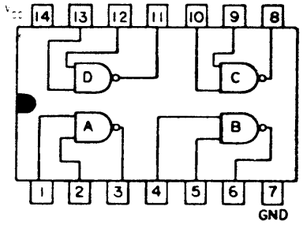


800732-001 (-1 ASSY)
U1 (-2 ASSY)



800480-001 (-1 ASSY)
800480-002 (-2 ASSY)
U3

800024-001 (-1 ASSY)
800024-002 (-2 ASSY)
U2, U4



8. **SCHEMATIC DRAWING NUMBER 233024 REV. F**
7. ASSEMBLY DRAWING NUMBER IS 233020.
6. INTERPRET ELECTRONIC SYMBOLS PER 850026.
5. INTERPRET REFERENCE DESIGNATIONS PER 850027.
4. ALL DIODES ARE 800743-001.
3. ALL TRANSISTORS ARE 800019-001.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS, 10%, 50 VOLTS.
1. ALL RESISTANCE VALUES ARE IN OHMS, 5%, 1/4 WATT.

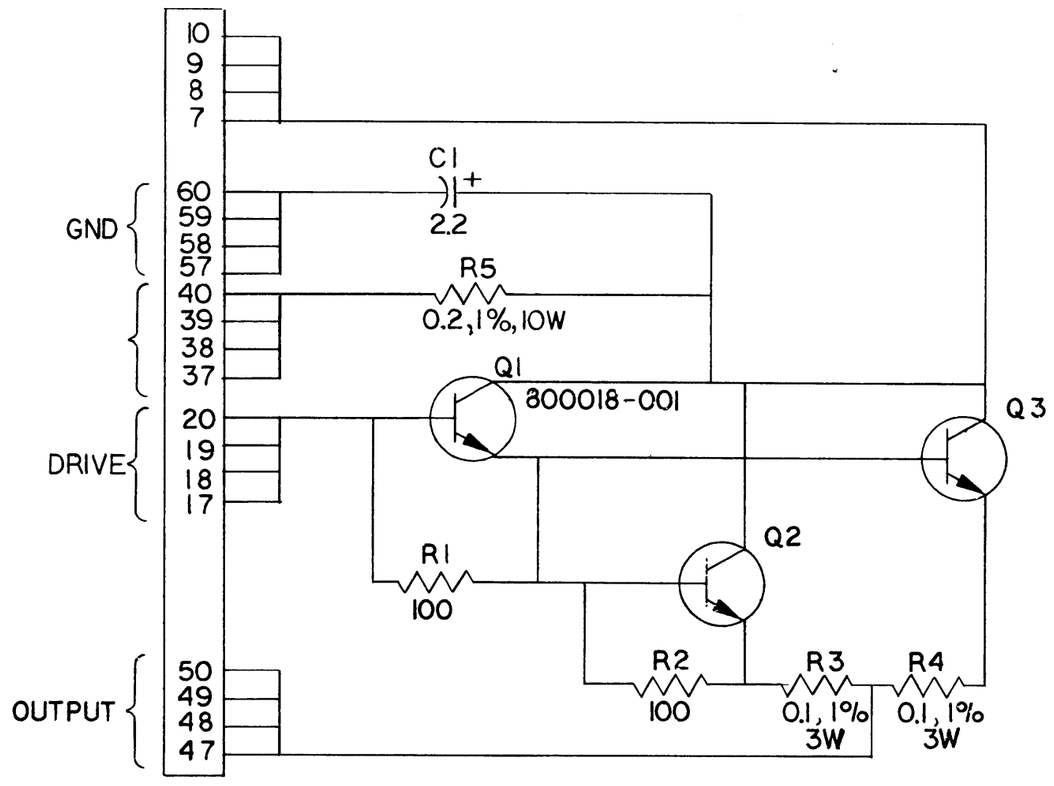
NOTES: UNLESS OTHERWISE SPECIFIED

FOR WIRING IN A8 HAMMER BANK POWER SUPPLY SEE LOGIC DIAGRAM SHEET 36 OR 36A, AS APPLICABLE

CIRCUIT CARD LOCATION· A8A3

SCHEMATIC DIAGRAM

AV-18
HAMMER BANK POWER SUPPLY REGULATOR
(MODELS 2440/2470)



10. SCHEMATIC DRAWING NUMBER 215289 REV. A
9. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION PREFIX WITH CIRCUIT NO.
8. THE FOLLOWING CONNECTOR PINS ARE NOT USED: 1 THRU 6, 11 THRU 16, 21 THRU 36, 41 THRU 46, 51 THRU 56
7. ASSEMBLY DRAWING NUMBER 215285.
6. INTERPRET ELECTRONIC SYMBOLS PER USAS Y32. 2.
5. INTERPRET REFERENCE DESIGNATIONS PER USAS Y32. 16.
4. ALL TRANSISTORS ARE 800215-001.
3.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS, 10%, 50 VOLTS.
1. ALL RESISTANCE VALUES ARE IN OHMS, 5%, 1/4 WATT.

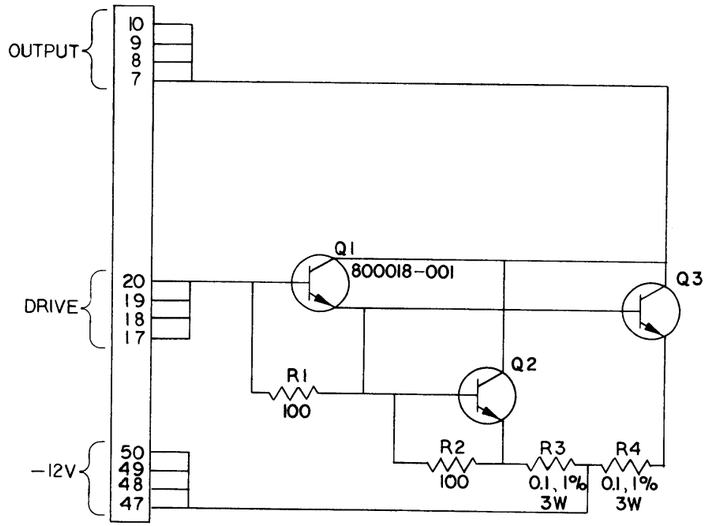
NOTES: UNLESS OTHERWISE SPECIFIED

FOR WIRING IN A5 POWER SUPPLY
SEE LOGIC DIAGRAM SHEET 28

CIRCUIT CARD LOCATION: A5A4, A5A6, A5A7, A5A8

SCHEMATIC DIAGRAM

AZ-49
+5V, +12V, +28V
POSITIVE PAPER FEED
POWER AMPLIFIER
(MODEL 2420)



10. SCHEMATIC DRAWING NUMBER 215292 REV. A
9. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION PREFIX WITH CIRCUIT NO.
8. THE FOLLOWING CONNECTOR PINS ARE NOT USED: 11 THRU 16, 21 THRU 46, 51 THRU 60
7. ASSEMBLY DRAWING NUMBER 215290.
6. INTERPRET ELECTRONIC SYMBOLS PER USAS Y32.2.
5. INTERPRET REFERENCE DESIGNATIONS PER USAS Y32.16.
4. ALL TRANSISTORS ARE 800215-001.
3.
2.
1. ALL RESISTANCE VALUES ARE IN OHMS, 5%, 1/4 WATT.

NOTES: UNLESS OTHERWISE SPECIFIED

FOR WIRING IN A5 POWER SUPPLY
SEE LOGIC DIAGRAM SHEET 28
CIRCUIT CARD LOCATION: A5A5

SCHEMATIC DIAGRAM

AZ-51
NEGATIVE PAPER FEED
POWER AMPLIFIER
(MODEL 2420)

APPENDIX A

LOADING DIAGRAMS

A-1 INTRODUCTION

A-2 This appendix contains complete loading diagrams of the integrated circuits (IC's) depicted in the logic diagram and schematic diagram sheets of section VII and section VIII. Table A-1 lists sequentially the IC's by DPC drawing numbers and provides the corresponding package style, IC type number, and loading diagram figure number. Each loading diagram contains complete pin assignments and, in most cases, the functional symbols associated with its circuit elements.

TABLE A-1. INTEGRATED CIRCUIT LOADING DIAGRAMS

DPC Dwg No.	Style	IC Type No.	Figure No.
800020-	A	7420	1
800021-	A	7430	2
800022-	A	7440	1
800023-	A	7410	3
800024-	A	7400	4
800025-	A	7453	5
800026-	A	74550	6
800080-	A	7402	7
800081-	A	7476	8
800186-	A	711C	9
800195-	A	709C	10
800232-	B	25-BIT ST REG	11
800233-	B	32-BIT ST REG	11
800370-	A	7486	12
800382-	A	7475	13

A - Dual Inline Package
B - Can Type Package

TABLE A-1. INTEGRATED CIRCUIT LOADING DIAGRAMS (Contd)

DPC Dwg No.	Style	IC Type No.	Figure No.
800383-	A	7483	14
800385-	A	7442	15
800386-	A	74193	16
800387-	A	7404	17
800393-	A	7220/ 8220	18
800394-	A	8200	19
800398-	A	201A	20
800399-001	A	710	58
800399-002	B	710	59
800400-	A	7474	21
800458-	B	3003	11
800480-	A	7403	4
800481-	B	711C	57
800491-	A	74121	22
800499-	B	2050	23
800503-	A	733	24
800512-	A	8210	25
800526-	A	75109	26
800527-	A	75107	27
800591-	A	7493	60
800638-	A	7496	28
800639-	A	7494	29
800651-	A	7406	17
800698-	A	74164	30
800703-	A	9312	31
800732-001	A	741	32
800732-002	B	741	33
800741-	A	75450	34
800788-	B	3002	11
800805-	A	1414/ 72514	35
800806-	A	7407	17
800810-	A	9602	36
800814-	A	0512	37
800818-	A	74192	38
800861-	A	74155	39
800862-	A	7489	40
800882-	A	944	41
800883-	A	946	4
800916-	A	HEX INV BUFFER	17
800920-	A	7437	4
800940-	A	5060/ 3120	42
800947-	A	74157	43
800949-	A	8820A	44

TABLE A-1. INTEGRATED CIRCUIT LOADING DIAGRAMS (Contd)

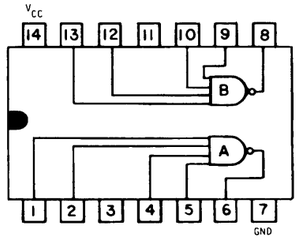
DPC Dwg No.	Style	IC Type No.	Figure No.
800950-	A	8830	45
800951-	A	2318	46
800952-001	A	1458/ 72558	47
800952-002	B	1458/ 72558	48
800956-	A	935	17
800959-	A	7414	17
800979-	A	74123	49
800998-	A	9318/ 74148	50
801000-	A	74180	51
801006-	A	RES NET	61
801007-	A	RES NET	62
801008-	A	RES NET	63
801009-	A	RES NET	64
801012-	A	74177	52
801014-	A	74136	12
801023-	A	74221	53
801077-	A	74151A	54
801100-	A	3203	65
801112-	A	74H01	4
801113-	A	74H05	17
801114-001	A	565	55
801114-002	B	565	56
801179-	A	723	66
801180-	A	74154	67
801186-	A	74393	68
801209-	A	1406	72
801219-	A	75140	70
801220-	A	3341	78
801221-	A	74125	71
801230-	A		17
801231-	A	7488	77
801242-	A	7426	4
801257-	A	339	73
801278-	A	74163	74
801279-	A	74175	75
801280-	A	74153	76
801282-	A	10125	81
801283-	A	10124	82
801300-	A	5020	83
801308-	A	7408	80
801309-	A	74279	79
801310-	A	74186	69

A - Dual Inline Package
B - Can Type Package

DUAL 4-INPUT NAND GATE
800020-001 DPC 7420
800020-002 (HERMETICALLY SEALED)

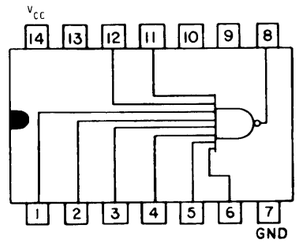
DUAL 4-INPUT NAND BUFFER
800022-001 DPC 7440
800022-002 (HERMETICALLY SEALED)

FIG 1



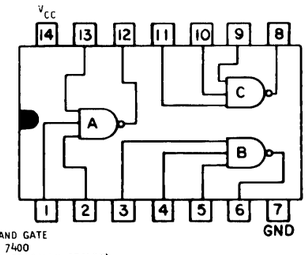
SINGLE 8 INPUT NAND GATE
800021-001 DPC 7430
800021-002 (HERMETICALLY SEALED)

FIG 2



TRIPLE 3-INPUT NAND GATE
800023-001 DPC 7410
800023-002 (HERMETICALLY SEALED)

FIG 3

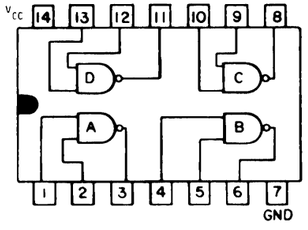


QUAD 2-INPUT NAND GATE
800024-001 DPC 7400
800024-002 (HERMETICALLY SEALED)
800480-001 DPC 7403
800480-002 (HERMETICALLY SEALED)
800883-001 DPC 946
800883-002 (HERMETICALLY SEALED)

QUAD 2-INPUT POS. NAND BUFFER
800920-001 DPC 7437
800920-002 (HERMETICALLY SEALED)

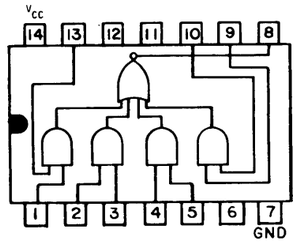
QUADRUPLE 2-INPUT POSITIVE NAND GATE (WITH OPEN-COLLECTOR OUTPUT)
801112-001 DPC 74H01
801112-002 (HERMETICALLY SEALED)

FIG 4



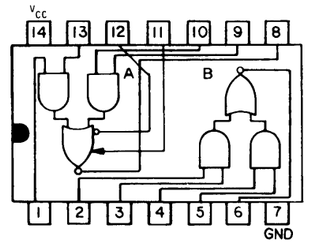
EXPANDABLE SINGLE 2-2-2-2 AND-OR-INVERT
800025-001 DPC 7453
800025-002 (HERMETICALLY SEALED)

FIG 5



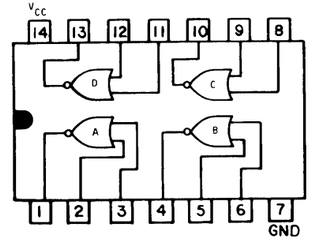
EXPANDABLE DUAL 2-WIDE 2-INPUT AND-OR-INVERT GATE
800026-001 DPC 7450
800026-002 (HERMETICALLY SEALED)

FIG 6



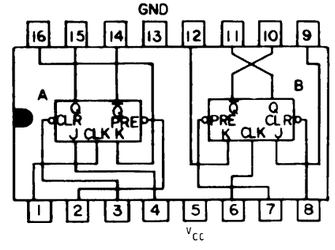
QUAD 2-INPUT NOR GATE
800030-001 DPC 7402
800080-002 (HERMETICALLY SEALED)

FIG 7



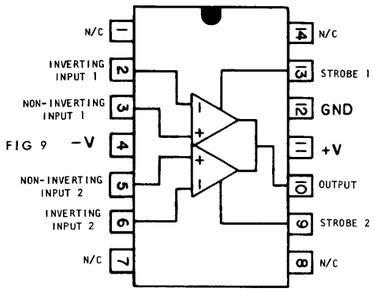
DUAL J-K FLIP FLOP
800081-001 DPC 7476
800081-002 (HERMETICALLY SEALED)

FIG 8



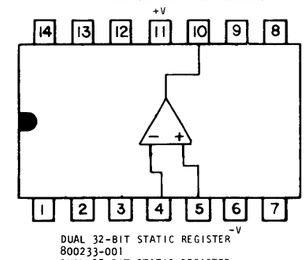
DUAL DIFFERENTIAL COMPARATOR
800186-001 DPC 711C
800186-002 (HERMETICALLY SEALED)

FIG 9



OPERATIONAL AMPLIFIER
800195-001 DPC 709C
800195-002 (HERMETICALLY SEALED)

FIG 10



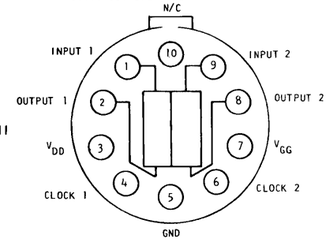
DUAL 32-BIT STATIC REGISTER
800233-001

DUAL 25-BIT STATIC REGISTER
800232-001

DUAL 100-BIT STATIC REGISTER
800458-001 DPC 3003

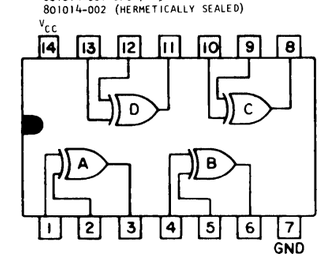
MOS DUAL 50-BIT STATIC SHIFT REGISTER
800788-001 DPC 3002

FIG 11



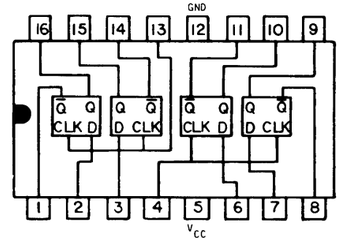
QUAD 2-INPUT EXCLUSIVE-OR GATE
800370-001 DPC 7486
800370-002 (HERMETICALLY SEALED)
QUAD 2-INPUT EXCLUSIVE-OR GATE W/OPEN COL.
801014-001 DPC 74136
801014-002 (HERMETICALLY SEALED)

FIG 12



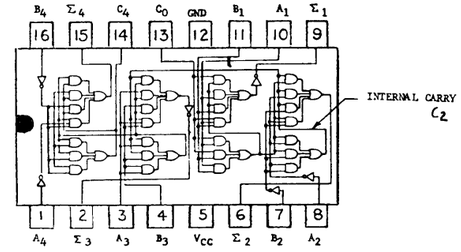
QUAD BISTABLE LATCH
800382-001 DPC 7475
800382-002 (HERMETICALLY SEALED)

FIG 13



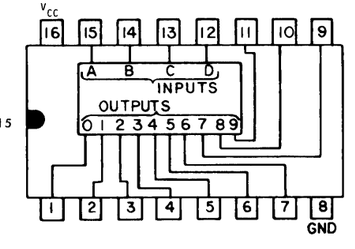
4-BIT BINARY FULL ADDER
800383-001 DPC 7483
800383-002 (HERMETICALLY SEALED)

FIG 14



BCD TO DECIMAL DECODER
800385-001 DPC 7442
800385-002 (HERMETICALLY SEALED)

FIG 15



LOADING DIAGRAMS

FIGURES 1-15
(Sheet 1 of 5)

UP/DOWN BINARY COUNTER
800386-001 DPC 74193
800386-002 (HERMETICALLY SEALED)

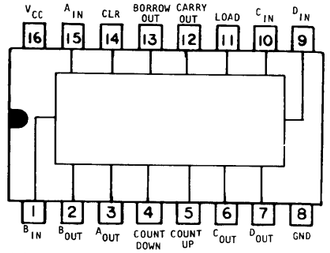


FIG 16

HEX INVERTERS
800387-001 DPC 7404
800387-002 (HERMETICALLY SEALED)
DTL HEX INVERTER EXTENDABLE
800956-001 DPC 935
800956-002 (HERMETICALLY SEALED)
HEX INVERTER, BUFFER
800916-001
800916-002 (HERMETICALLY SEALED)
HEX BUFFER/DRIVER
800806-001 DPC 7407
800806-002 (HERMETICALLY SEALED)

HEX INVERTER, BUFFER/DRIVER
800651-001 DPC 7406
800651-002 (HERMETICALLY SEALED)
HEX SCHMITT TRIGGERS
800959-001 DPC 7414
800959-002 (HERMETICALLY SEALED)
HEX INVERTERS
(WITH OPEN-COLLECTOR OUTPUT)
801113-001 DPC 74H05
801113-002 (HERMETICALLY SEALED)

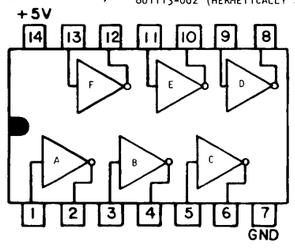


FIG 17

PARITY GENERATOR AND CHECKER
800393-001 DPC 7220/8220
800393-002 (HERMETICALLY SEALED)

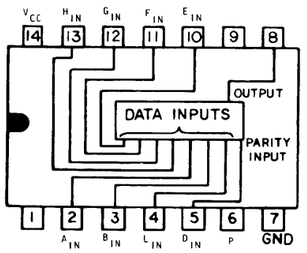


FIG 18

FOUR BIT COMPARATOR
800394-001 DPC 8200
800394-002 (HERMETICALLY SEALED)

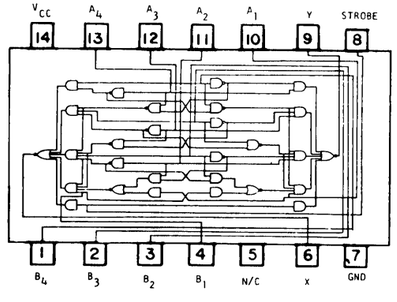


FIG 19

OPERATIONAL AMPLIFIER, HI PERFORMANCE
800398-001 DPC 201A

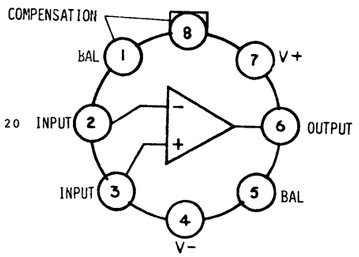


FIG 20

DUAL D-TYPE FLIP FLOP
800400-001 DPC 7474
800400-002 (HERMETICALLY SEALED)

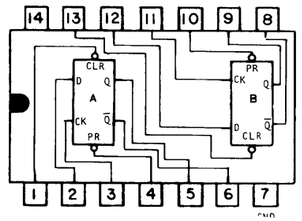


FIG 21

MONOSTABLE MULTIVIBRATOR
800491-001 DPC 74121
800491-002 (HERMETICALLY SEALED)

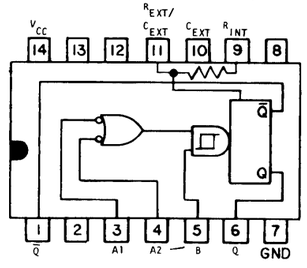


FIG 22

VOLTAGE REGULATOR
800499-001 DPC 2050

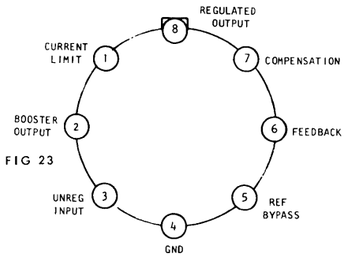


FIG 23

VIDEO AMPLIFIER
800503-001 DPC 733
800503-002 (HERMETICALLY SEALED)

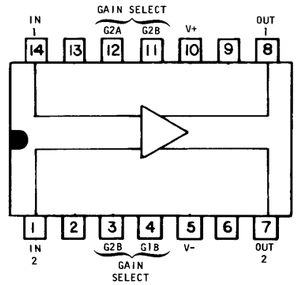


FIG 24

EIGHT CHANNEL SWITCH
800512-001 DPC 8210
800512-002 (HERMETICALLY SEALED)

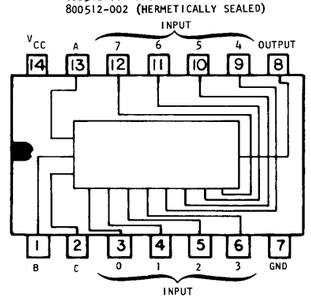


FIG 25

DUAL LINE DRIVER
800526-001 DPC 75109
800526-002 (HERMETICALLY SEALED)

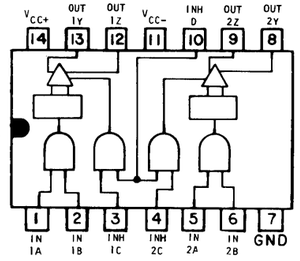


FIG 26

DUAL LINE RECEIVER
800527-001 DPC 75107
800527-002 (HERMETICALLY SEALED)

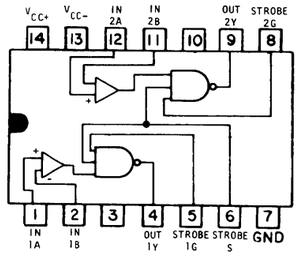


FIG 27

5-BIT SHIFT REGISTER
800638-001 DPC 7496
800638-002 (HERMETICALLY SEALED)

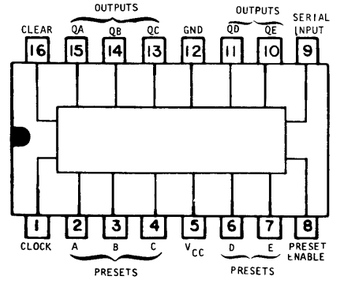


FIG 28

4-BIT SHIFT REGISTER
800639-001 DPC 7494
800639-002 (HERMETICALLY SEALED)

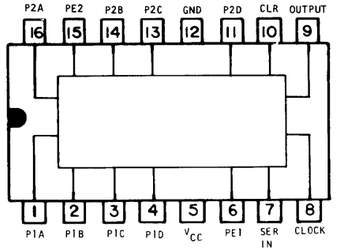


FIG 29

8-BIT S-IN, P-OUT, SHIFT REGISTER
800698-001 DPC 74164
800698-002 (HERMETICALLY SEALED)

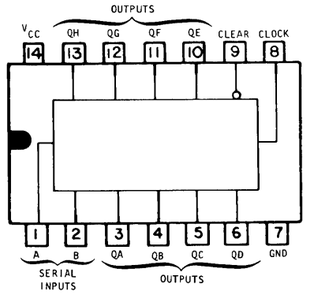


FIG 30

8 INPUT DIGITAL MULTIPLEXER
800703-001 DPC 9312
800703-002 (HERMETICALLY SEALED)

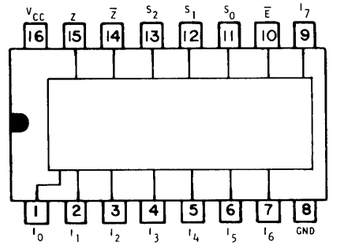


FIG 31

OPERATIONAL AMPLIFIER
800732-001 DPC 741

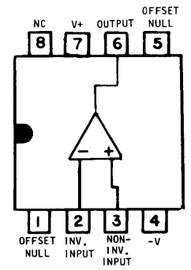


FIG 32

800732-002 (HERMETICALLY SEALED)

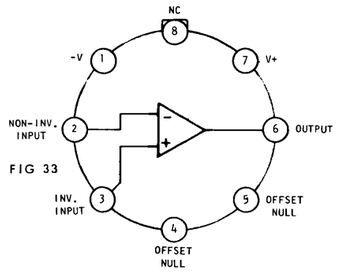


FIG 33

LOADING DIAGRAMS

FIGURES 16-33
(Sheet 2 of 5)

DUAL INTERFACE DRIVER
800741-001 DPC 75450
800741-002 (HERMETICALLY SEALED)

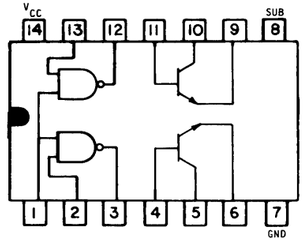


FIG 34

DUAL DIFFERENTIAL COMPARATOR
800805-001 DPC 72514
800805-002 (HERMETICALLY SEALED)

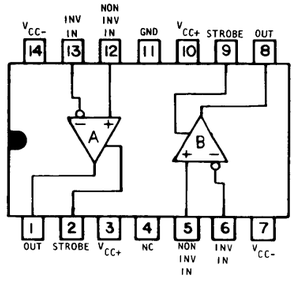


FIG 35

DUAL RETRIGGERABLE MONOSTABLE
800810-001 DPC 9602
800810-002 (HERMETICALLY SEALED)

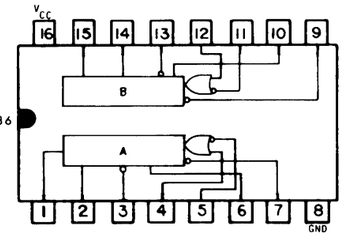


FIG 36

64 WORD 8-BIT PROGRAMMABLE ROM
800814-001 DPC 0512
THRU 800814-036
800814-040 & 800814-041

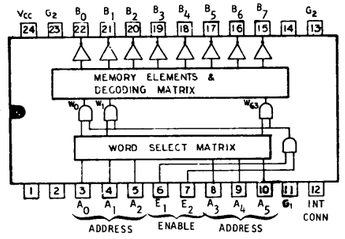


FIG 37

UP/DOWN DECADE COUNTER
800818-001 DPC 74192
800818-002 (HERMETICALLY SEALED)

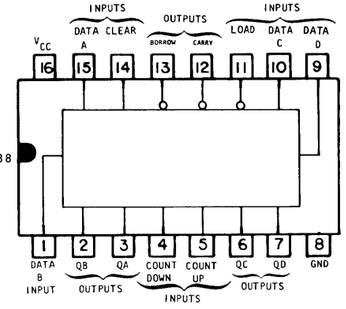


FIG 38

DUAL DECODER/DEMULTIPLEXER
800861-001 DPC 74155
800861-002 (HERMETICALLY SEALED)

FIG 39

64-BIT R/W MEMORY
800862-001 DPC 7489
800862-002 (HERMETICALLY SEALED)

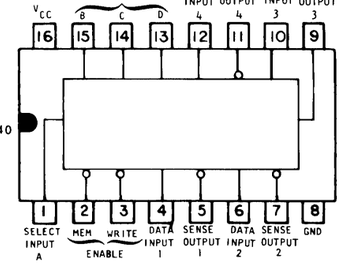


FIG 40

DUAL 4-INPUT POWER NAND BUFFER GATE
800882-001 DPC 944
800882-002 (HERMETICALLY SEALED)

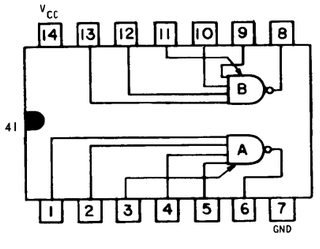


FIG 41

MOS DUAL 144-BIT STATIC S/R
800940-001 DPC 5060
800940-002 (HERMETICALLY SEALED)

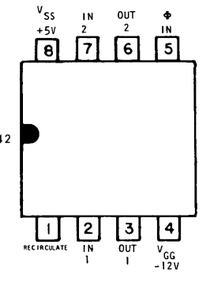


FIG 42

QUAD 2-LINE-TO-1-LINE SELECTOR
800947-001 DPC 74157
800947-002 (HERMETICALLY SEALED)

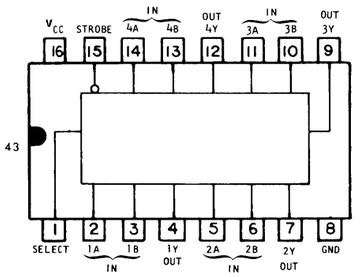


FIG 43

DUAL LINE RECEIVER
800949-001 DPC 8820A
800949-002 (HERMETICALLY SEALED)

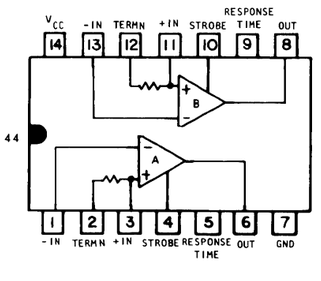


FIG 44

DUAL DIFFERENTIAL LINE DRIVER
800950-001 DPC 8830
800950-002 (HERMETICALLY SEALED)

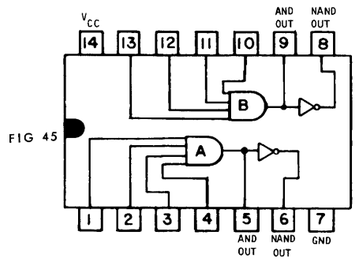


FIG 45

MOS HEX 32-BIT STATIC S/R
800951-001 DPC 2518
800951-002 (HERMETICALLY SEALED)

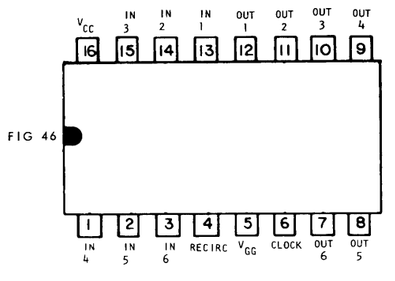


FIG 46

DUAL OP AMP HI-PERFORMANCE
800952-001 DPC 1458

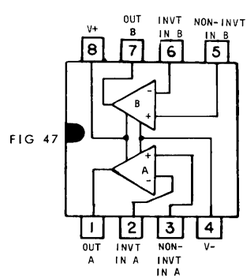


FIG 47

800952-001 (HERMETICALLY SEALED)

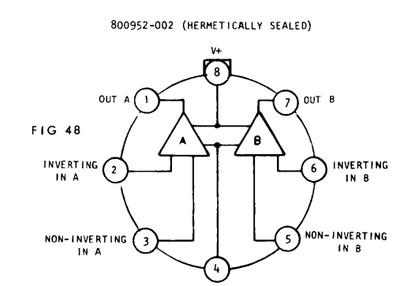


FIG 48

DUAL RETRIGGERABLE MONOSTABLE MV
800979-001 DPC 74123
800979-002 (HERMETICALLY SEALED)

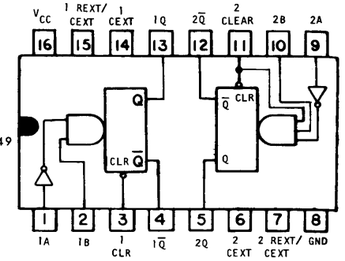


FIG 49

8-TO-3 PRIORITY ENCODER
800998-001 DPC 9318/74148
800998-002 (HERMETICALLY SEALED)

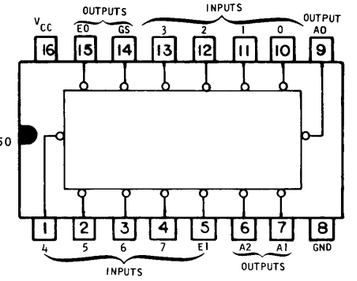


FIG 50

9-BIT PARITY GEN/CHECKER
801000-001 DPC 74180
801000-002 (HERMETICALLY SEALED)

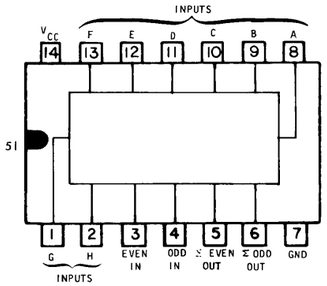


FIG 51

PRESETTABLE COUNTER
801012-001 DPC 74177
801012-002 (HERMETICALLY SEALED)

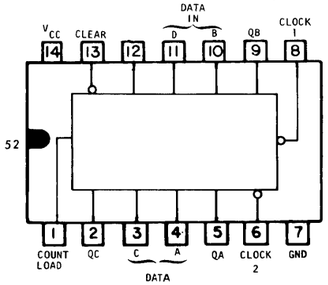


FIG 52

LOADING DIAGRAMS

FIGURES 34-52
(Sheet 3 of 5)

DUAL MONOSTABLE MULTIVIBRATOR W/CLEAR
801023-001 DPC 74221
801023-002 (HERMETICALLY SEALED)

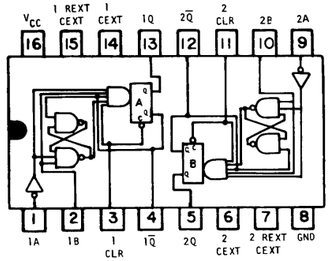


FIG 53

DUAL DIFFERENTIAL COMPARATOR
800481-001 DPC 711C

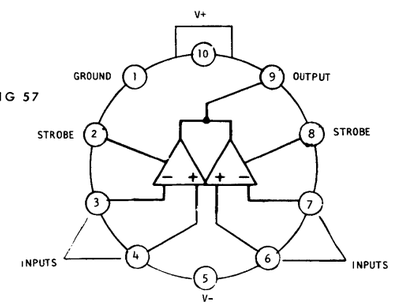


FIG 57

RESISTOR, NETWORK PULL-UP,
13 RESISTORS
801006-

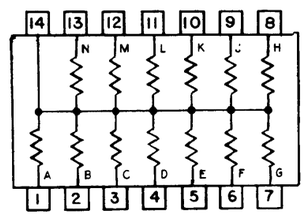


FIG 61

2048-BIT STATIC READ ONLY MEMORY (pROM)
801100-001 DPC 5203
801100-002
801100-003

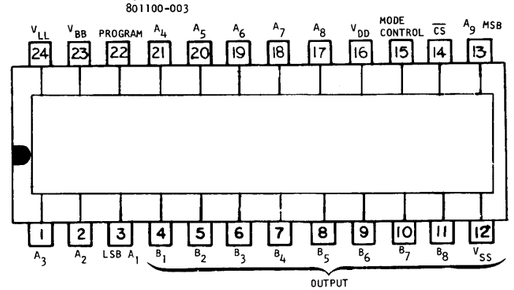


FIG 65

DATA SELECTOR/MULTIPLEXER
801077-001 DPC 74151
801077-002 (HERMETICALLY SEALED)

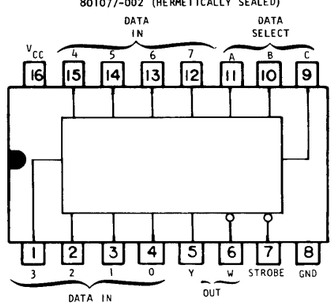


FIG 54

DIFFERENTIAL COMPARATOR
800399-001 DPC 710

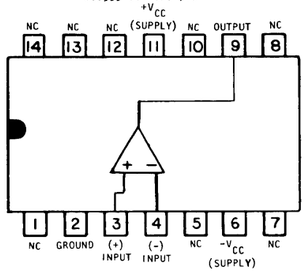


FIG 58

RESISTOR, NETWORK FEED-THRU,
7 RESISTORS
801007-

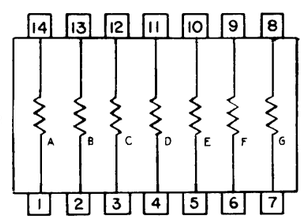


FIG 62

VOLTAGE REGULATOR
801179-001;002

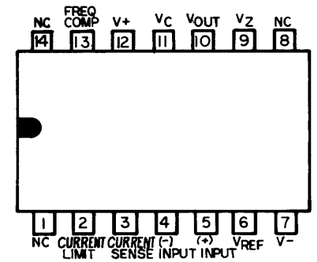


FIG 66

64 WORD 8-BIT PROGRAMMABLE ROM
801310-001 DPC 74186
THRU 801310-036
801310-040 & 801310-041

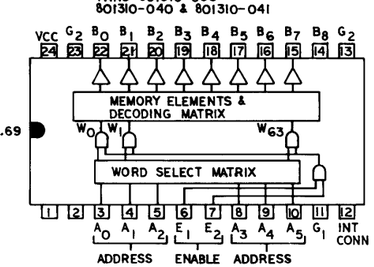


FIG.69

4-LINE-TO-16-LINE DECODER/DEMULTIPLEXER
801180-001;002

PHASE LOCKED LOOP
801114-001 DPC 565

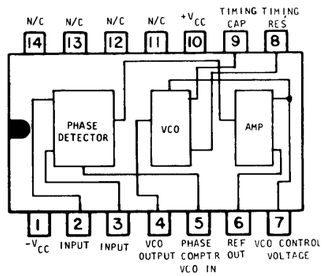


FIG 55

800399-002 (HERMETICALLY SEALED)

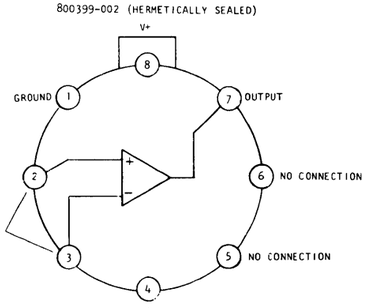


FIG 59

RESISTOR, NETWORK PULL-UP
15 RESISTORS
801008-

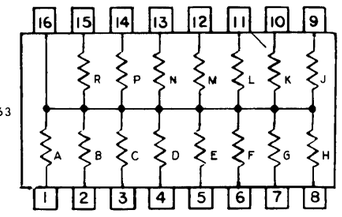


FIG 63

INPUTS OUTPUTS

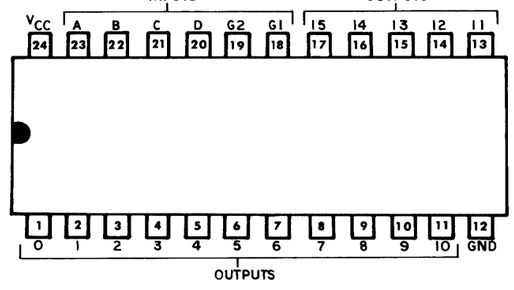


FIG67

801114-002 (HERMETICALLY SEALED)

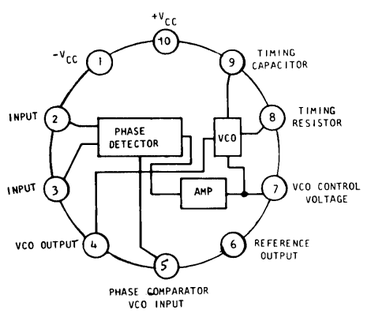


FIG 56

4 BIT BINARY COUNTER
800591-001 DPC 7493
800591-002 (HERMETICALLY SEALED)

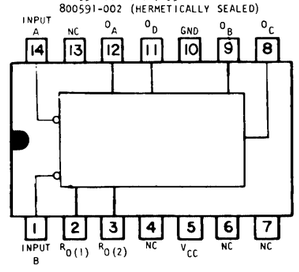


FIG 60

RESISTOR, NETWORK FEED-THRU,
8 RESISTORS
801009-

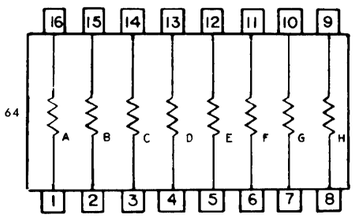


FIG 64

DUAL 4-BIT BINARY COUNTER
801186-001;002

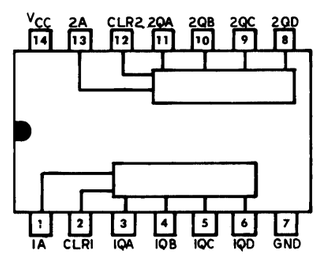
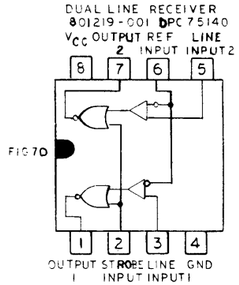


FIG 68

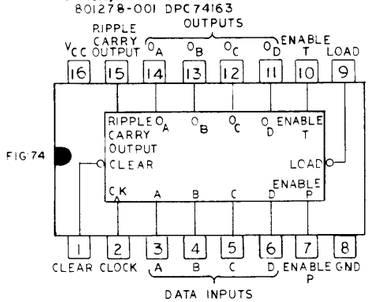
LOADING DIAGRAMS

FIGURES 53-69
(Sheet 4 of 5)

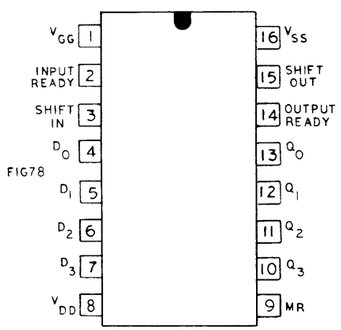
DUAL LINE RECEIVER
801219-001 DPC 75140



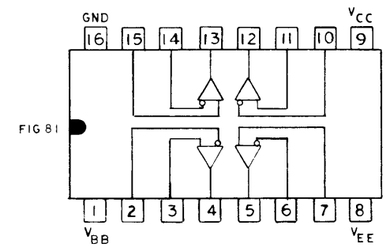
SYNCH, 4-BIT BINARY CNTR
801278-001 DPC74163



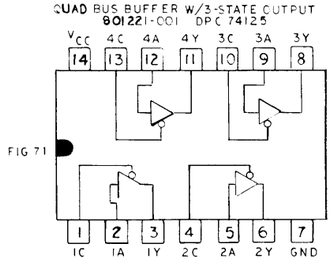
64 WORD X 4 BIT F I F O
SERIAL MEM
801220-001 DPC3341



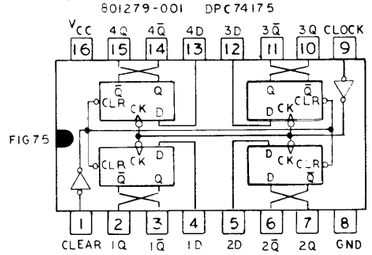
QUAD ECL TO TTL TRANSLATOR
801282-001 DPC10125



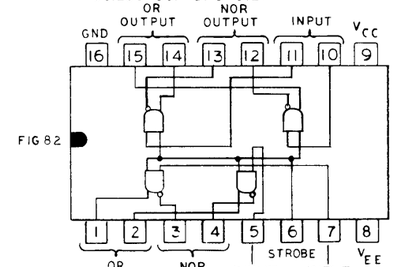
QUAD BUS BUFFER W/3-STATE OUTPUT
801221-001 DPC 74125



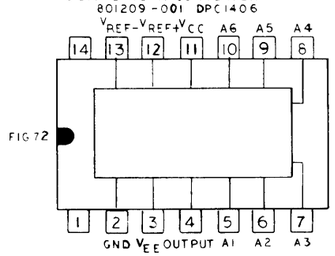
QUAD D F-F W/CLEAR
801279-001 DPC74175



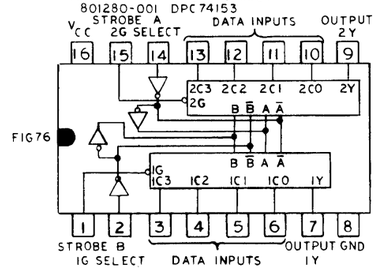
QUAD TTL TO ECL TRANSLATOR
801283-001 DPC 10124



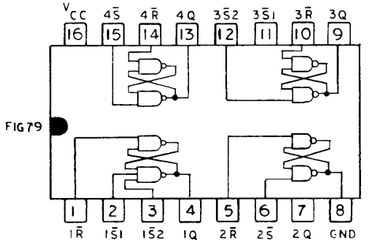
6 BIT D-TO-A CONVERTER
801209-001 DPC1406



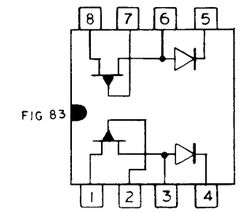
DUAL 4-L-2-I-L DATA/MULT
801280-001 DPC74153



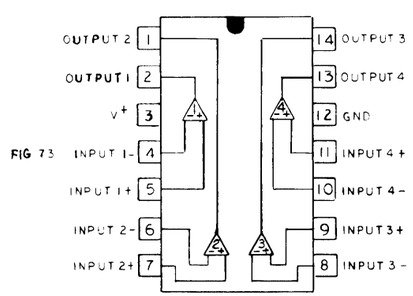
QUAD LATCH
801309-001 DPC 74279



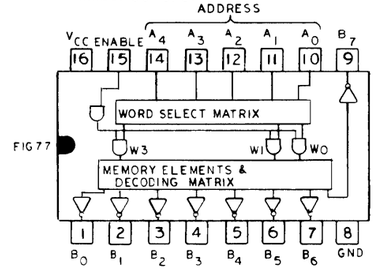
ANALOG CURRENT SWITCH
801300-001 DPC 5020



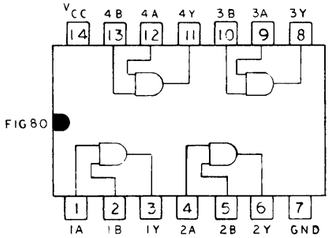
QUAD VOLTAGE COMPARATOR/BUFFER
801257-001 DPC 339



PROGRAMMABLE READ/ONLY MEMORY
801231-001 DPC7488



QUAD 2-INPUT POS AND GATE
801308-001 DPC7408



LOADING DIAGRAMS

FIGURES 70-83
(Sheet 5 of 5)