PUBLICATIONS REVIEW

Workslate Hardware and Service Manual

First Draft Theory of Operations

November 9, 1983

Return to Paul Woodside (Building 7) by:

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Please review the enclosed section for technical and editorial accuracy, and for general clarity. Return this draft by the date indicated above or at the review meeting, which will take place one of these days. Notice of the meeting will be sent to you by separate memo.

Reviewers, if you don't see all of what you want here, write it in and make your comments as clear as possible. Complete sentences help a great deal. You have all been a tremendous help to me but I don't have a lot of time left here...

Also, please pay special attention to the figures (so-called art) that I've included here. The artist is coming in soon to do layouts and I would like to get all the changes in as early as possible.

Reviewers:

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THEORY OF OPERATIONS

Introduction

This section is written for the engineer or service technician who desires an understanding of the Workslate circuitry at a component level. The circuitry within the Workslate can be divided in several major areas as follows:

- the Digital System includes the microprocessor, RAM, ROM, and peripheral logic necessary to control all of the digital and analog functions for the Workslate

- The Telephone and Modem Circuits provide a 300 baud full duplex modem, a status filter to decode various status tones from the telephone system, and a standard telephone circuit capable of either pulse or tone dialing

- The Tape and Audio Circuits control the tape and head motors on the tape transport, tape counting, recording and playback of both voice and data on the tape, multiplexing of

multiple audio sources to multiple destinations, and amplification of the audio source to the speaker.

- The Power Supplies generate +5 Vdc and -12 Vdc to power the Workslate when it is fully powered up. and backup voltages to preserve certain functions and the content of RAM in the Workslate when it is in the standby mode (off).

Figure 3-1 shows the overall functional block diagram of the Workslate. In the following subsections, more detailed block diagrams are provided to cover the circuits being described. For a component-level layout of the Workslate, see Figure 3-2, the Main Logic Board schematic, and Figure 3-5, the Display Board schematic.

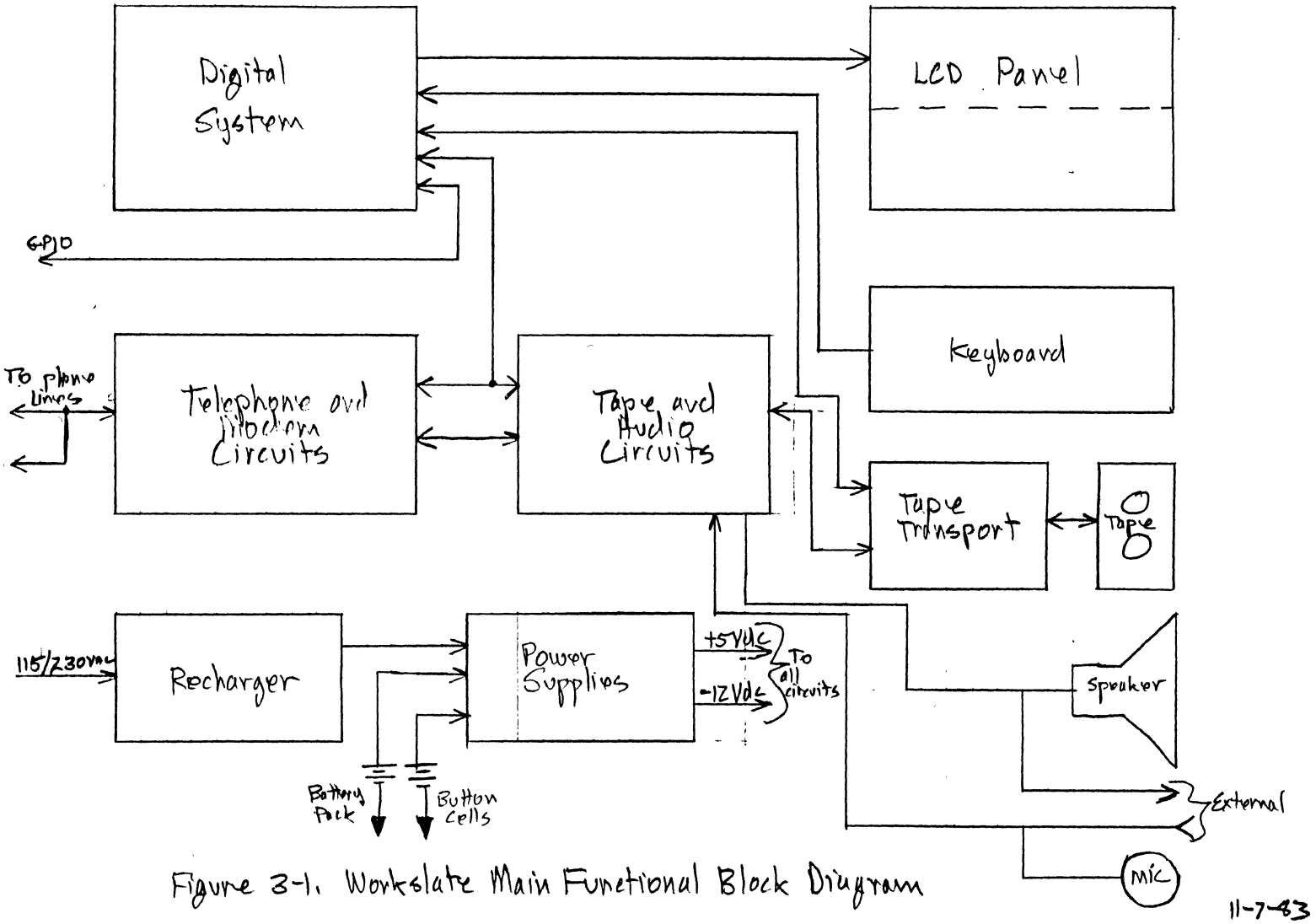

Figure 3-1. Workslate Main Functional Block Diagram

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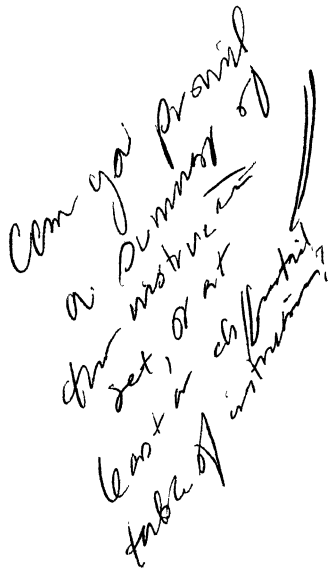

As shown on page x of Figure 3-3, the Main Logic board schematic, the microprocessor at U20 is a Hitachi HD63A03-V0. It is eight-bit HMOS CPU, similar in architecture and instruction set to a Motorola 6800-series microprocessor. U20 generates the basic system clock for the digital system and contains 128 bytes of scratchpad RAM, and an internal timer. U20 also provides two input/output ports: one parallel port to operate the modem and telephone circuits, and one serial port to carry data to and from the gate array, modem, and GPIO port.

Figure 3-3. Main Logic Board Schematic.

Timing. The basic timing for U20 is X1, a 4.915 MHz crystal across pins 2 and 3 of U20. U20 internally divides the crystal frequency by four to get the basic system clock frequency of [redacted] MHz. The basic system clock is distributed throughout the digital system as E (Enable) at pin 54 to synchronize data transfers on the multiplexed address and data bus.

Address and Data Busses. The multiplexed address and data bus at pins 7 through 14, and the non-multiplexed address bus at pins 15 through 18 and pins 23 through 26 provide 16 bits of address (64K-byte range) and 8 bits of data. The address and data bus connects all of the addressable circuit elements in the Workslate, such as the LCD controller, RAM, ROM, real-time clock, etc. As shown in Figure 3-4, Processor Bus Cycle Timing, during the first part of a read or write cycle the AD0 through AD7 (Address and Data) lines carry the lower eight bits of the memory or I/O address, and the A8 through A15 (Address) lines carry the upper eight bits of the address. During this time, AS (Address Strobe) line is high at pin 53 of U20. The lower eight bits of the address are latched in the decoder gate array

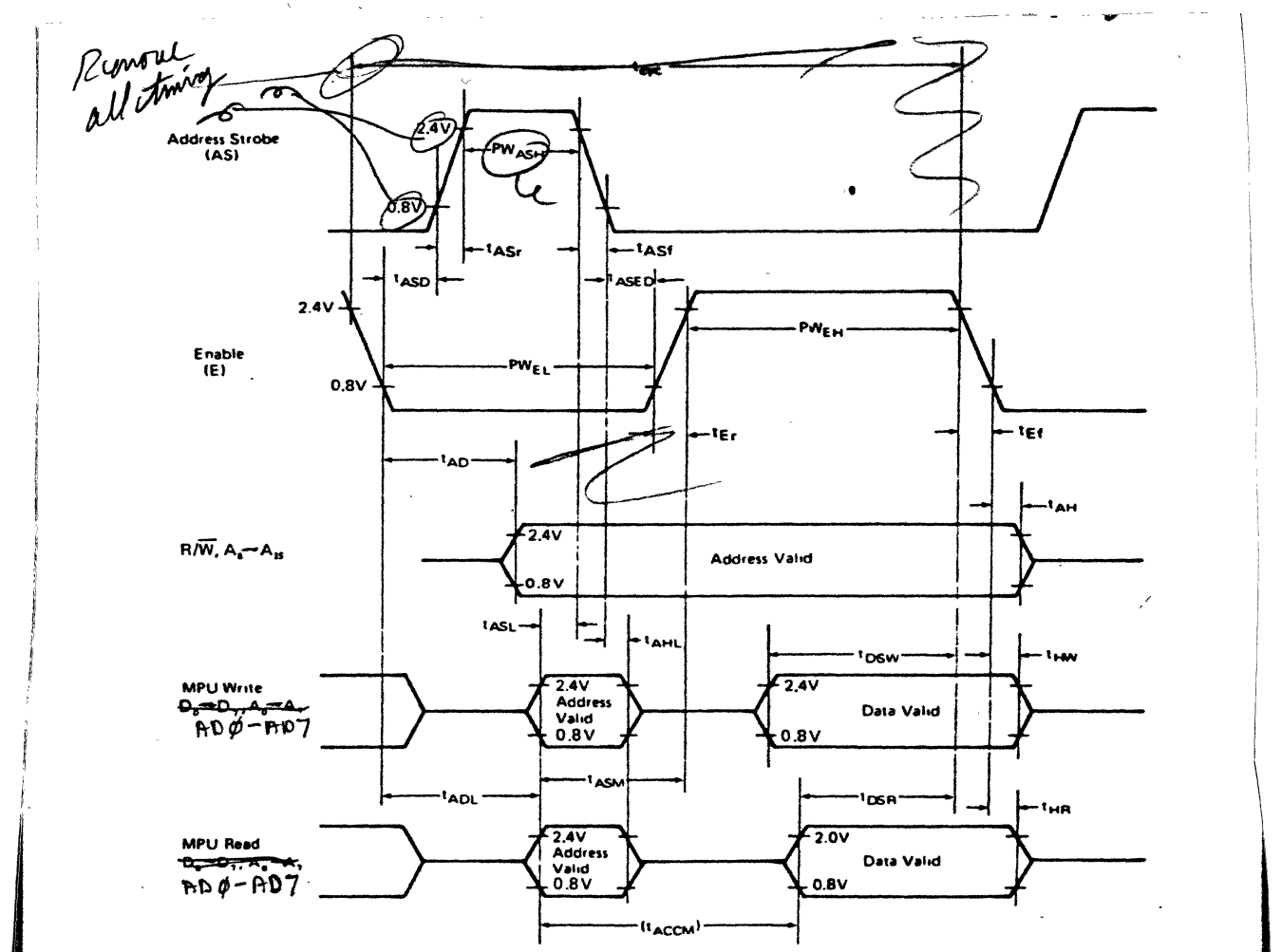

Figure 1 Multiplexed Bus Timing

Figure 3-4. Processor Bus Cycle Timing.

at U13. During the second half of the read or write cycle, data appears on the AD0 through AD7 lines either from or to the addressed memory location or I/O device. The R/W- (Read/Write-) line is a level, which indicates the direction of data transfer as a read (high) or write (low). The actual read and write data strobes are generated in conjunction with the E clock in the decoder gate array.

Processor Modes. The CPU operates in four basic modes: normal, sleep, standby, and reset. Sleep and standby are low-power modes.

When U20 is in normal mode, it is fully powered and can perform all of its functions.

To go into sleep mode, which uses only a fraction of the power used in the normal mode, U20 must execute the SLP (Sleep) instruction. When U20 is in the sleep mode, the E clock is still running so that other devices in the digital system can operate. However, the CPU does not access internal or external memory or I/O devices. The CPU wakes up upon receipt of an interrupt request from a device on the IRQ- (Interrupt Request) line at pin 2 of U20, or upon an interrupt from

the internal timer. An example of how the sleep mode is used with the CPU is when the Workslate is on and the user is not performing an operation. During this time, the CPU is interrupted from the sleep mode by the internal timer every 10 milliseconds to scan the keyboard for a key being pressed. If no key is being pressed, the CPU executes the SLP command until the internal timer wakes it up again. The sleep mode can also be exited by entry into the standby mode or the reset mode, both discussed below.

The standby mode is used when the Workslate is in an power-off state to reduce the power demands of the CPU to an absolute minimum level while still preserving the content of its internal RAM. When the user presses the On/Off key to turn the Workslate off, the tape gate array sets the ON/OFF- signal to pin 32 of U20 low. Upon receipt of ON/OFF, the CPU goes into a housekeeping routine to save the contents of its registers and data in its 128 bytes of RAM. When the CPU has executed the routine, it writes to the tape gate array at I/O port 20 indicating that it is safe to go into standby mode. The tape gate array then pulls the STBY- (Standby) line low at pin 9 of U20. When the CPU senses

that STBY- is low, it goes into a routine to disable the E clock and set all of its high. The only input the CPU examines is RES- (Reset) at pin 40 of U20.

When the user presses the On/Off key to power up the Workslate, the CPU goes into the reset mode. The On/Off key press is detected by the tape gate array, which then holds RES- low for at least 20 milliseconds. When RES- goes low and then high again, the CPU resets its operating mode, (multiplexed address and data), starts the E clock, enables its address and data busses, masks the IRQ- interrupt bit, and loads the contents of two start addresses, FFFEh and FFFFh into its program counter. Once the E clock has stabilized, the tape gate array sets the On/Off- signal high to indicate that normal-mode operation should start.

Processor Parallel Port. U20 has an eight-bit parallel I/O port are used for discrete control line to and from the modem, decoder gate array, and tape gate array. The pin assignments are as follows:

U20 Pin	Name	Function

18	BANKA-	Bank A. Similar to BANKB- (see below).
19	BANKB-	Bank B. Used in conjunction with BANKA-, Bank B selects which of the three ROMs data will be read from. BANKA- and BANKB- are sent to the decoder gate array at U13 to provide the appropriate chip select line for the ROMs. When the Workslate is first powered up, BANKA- and BANKB- are pulled high to select the CSROM0- chip select (ROM Bank 0).
20	ON/OFF-	On or Off. This input from the tape gate array informs the CPU that a user is requesting either power on (high) or power off (low).
22	RI-	Ring Indicator. When this input is low, a ringing signal is present on the telephone line.

23	DCD-	Data Carrier Detect. When the DCD- input is low, data carrier energy is present on the telephone line.
24	ONH	On Hook. When this output is low, the telephone circuitry in the Workslate has seized (picked up)the telephone line. When ONH is high, the telephone line is open (on the hook).
25	O/A-	Originate/Answer. The modem has two space/mark (1/0) frequency pairs associated with it depending on whether it is originating a call or answering one. When the O/A- output is low, the modem is placed in the answer mode. When O/A- is high, the modem is placed in the originate mode.

26	SQT	Squelch Transmitter. When SQT is high, the transmitter in the modem is off.

Processor Serial Port. A five-bit serial port at pins 35 through 39 of U20 are used for communication with the modem, tape gate array (tape read/write circuits), and the GPIO (General Purpose Input/Output) port, as well as providing an input and an output for the timer inside U20. The pin assignments are as follows:

U20 Pin	Name	Function
11	TIN	Timer Input. The timer input to the serial port is the STATUS- line from the status filter described below. The timer is used to count the width of the pulses from the status filter to determine what type of tones (busy, ring, etc.) are being received by the telephone circuits.

12	TOT	Timer Output. Unused.
13	CCK	Channel Clock. The channel clock allows the serial channel to operate in a synchronous mode in communications with the tape gate array. The modem and GPIO port do not use CCK.
14	CRX	Channel Receive. This input is the receive line for the serial channel.
15	CTX	Channel Transmit. This input is the transmit line for the serial channel.

Timer Counter. The internal timer/counter in the CPU has two functions. Every 10 milliseconds, the timer interrupts the CPU to remind it that it must scan the keyboard for depressed keys. Also the timer measures the widths of pulses coming from the telephone status filter.

Digital System

The Digital System includes the microprocessor, RAM, ROM, and peripheral logic necessary to control all of the digital and analog functions for the Workslate. As Figure 3-2 shows, the major functional blocks in the digital system are as follows:

- an eight-bit microprocessor that centrally controls digital functions, such as keyboard scanning, telephone and modem functions, and commuunication with Workslate peripheral devices

- a real-time clock that provides clock, calendar, and alarm functions

- a liquid crystal display controller that generates timing for the liquid crystal display.

- a liquid crystal display that displays the data in two 64-pixel by 276-pixel arrays

- a decoder gate array that demultiplexes the address and data bus for the microprocessor

and provides device selection lines for peripheral functions

- a tape gate array that provides the digital interface for the tape system, and control power-on and power-off sequencing.

- keyboard logic that enables the CPU to scan the keyboard for pressed keys.

- 16K bytes of RAM providing storage for worksheets and other data. The RAM is protected against loss by backup batteries for up to one year.

- 64K bytes of bank selected ROM containing the operating system for the Workslate

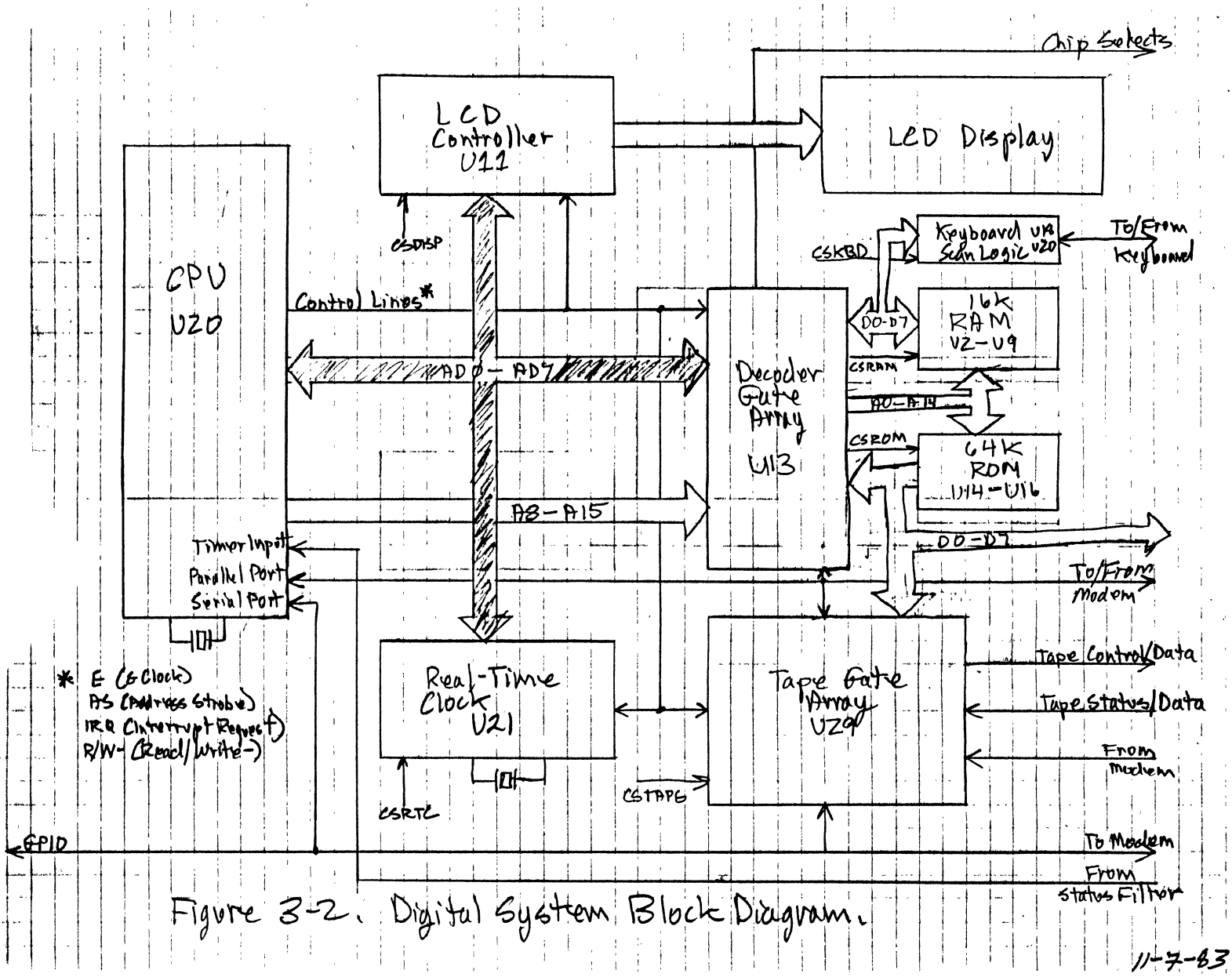

Figure 3-2. Digital System Block Diagram.

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Figure 3-2. Digital System Block Diagram.

The modem in the Workslate is a Bell 103-compatible, 300 baud, full-duplex type with originate/answer capability.

For transmission or reception of data or voice over standard telephone systems (500- or 2500-type telsets), the modem and audio circuits in the Workslate are supported by the DAA (Data Access Arrangement) section. The DAA can detect a ringing signal from the central office, and can detect tones present on the telephone line, such as busy, dialtone, etc. (The firmware in the Workslate is presently designed to decode a dial tone from the telephone line.) The DAA has the ability to either pulse dial or tone dial a telephone number. The block diagram for the Telephone and Modem circuits is shown as Figure 3-9.

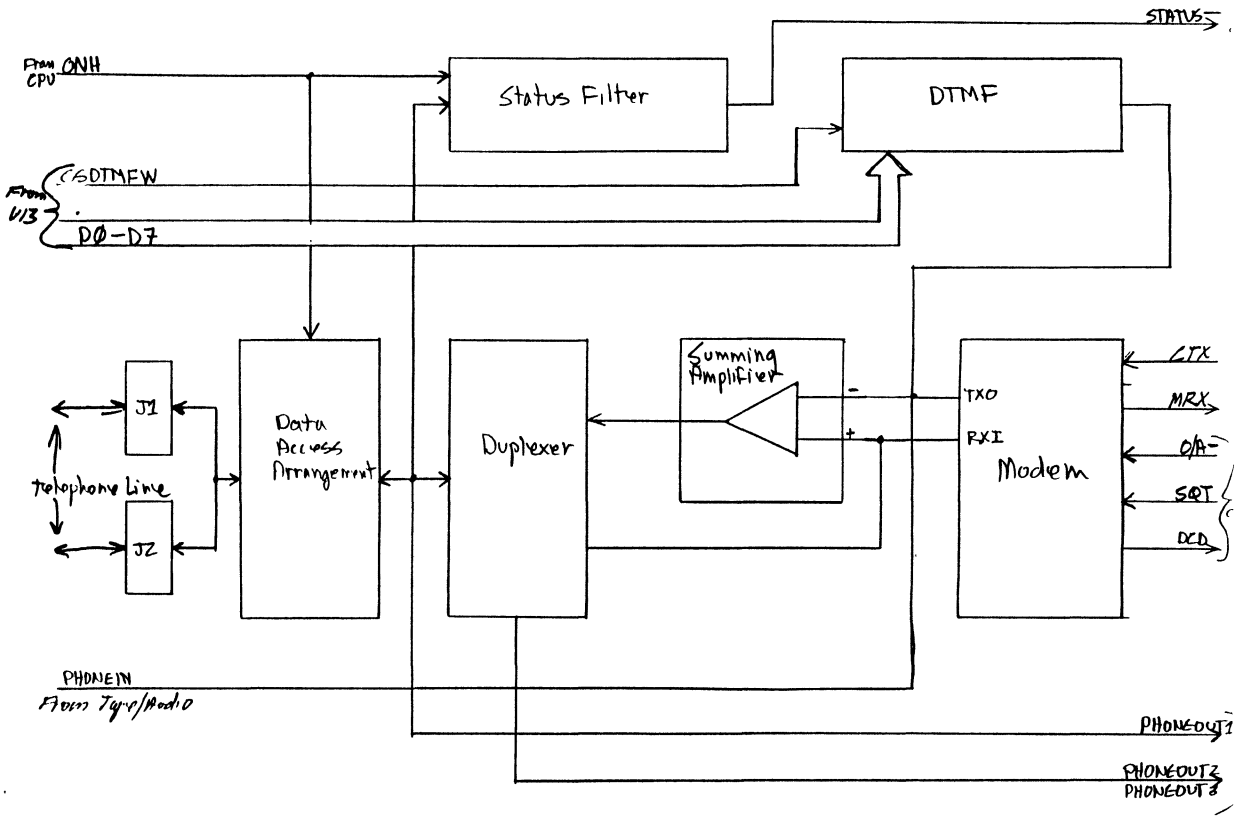

Figure 3-9. Telephone and Modem Circuits Block Diagram.

Figure 3-9. Telephone and Modem Circuits Block Diagram.

Data Access Arrangement. As shown on page x of Figure 3-3, two standard RJ-11 telephone jacks at J1 and J2 are wired so that the user can connect a Workslate and a standard telephone in parallel to a single telephone line. When an external telephone or modem tries to access a Workslate, the ring energy is present across the Tip and Ring inputs of J1 and J2 at pins 4 and 5, respectively. The ring energy, which can be as high as 90 Vac, is applied to the bridge rectifier made up of diodes CR5 through CR8. The rectified voltage from the opposite side of the bridge is applied to the LED in the opto-isolator at Q4. At the pin 5 collector of Q4, ringing causes RI (Ring Indicator) to go low to pin 22 of U20's parallel port. To seize (pickup) the phone line, U20 sets pin 24, ONH (On Hook) to low. ONH causes, through Q2, relay K1 to close, thus connecting the Workslate to the telephone line. Transformer T1 has a 1:1 turns ratio and provides isolation from the DAA to the Workslate telephone and modem circuits. The secondary of T1 at pin3 3 is sent to the duplexer circuit and then to the modem and audio circuits. Note that diodes CR10 and CR11 clamp the output peaks of the isolation transformer to plus or minus 3.9 volts. Also, if tone dialing facilities are not available, pulse

dialing is accomodated by U20 simply opening and closing the relay through the ONH signal as many times as required to "dial" the number.

Since the user needs to hear the phone ringing before the telephone line is actually seized, the ring energy is also ac-coupled through R35 and C11 to T1. At the pin 3 output of T1, the ringing signal is sent through the input side of the duplexer circuit and then to the audio circuits as PHONEOUT2 (Telephone Ouput 2).

Status Filter. The status filter provides a signal STATUS-, which is used by the Workslate software to decode the dialtones on the telephone line. The negative rail of the status filter is powered by VEE only when the ONH signal is low through transistors Q2 and Q3, that is, when the telephone line is siezed by relay K1. The positive rail is powered by VDDSW and is active only when the modem is in use. (See "Power Supplies.")

The input for the status filter is PHONEOUT1 (Telephone Output 1) from the secondary of isolation transformer T1. The signal first passes through a 400 to 850-Hz bandpass filter

composed of both halves of U32. Each output of U32 at pins 7 and 1 provides 20 dB of rolloff for frequencies outside of the 400 to 850-Hz band. The bandpass signal is then sent to a limiter at pin 5 U31, which compares the input level to a threshold reference at pin 6 and, if the input is above the threshold, generates a high (+5 Vdc) level at pin 7. If the input at pin 6 level is below the threshold, pin 7 of U31 goes to ground. This output at pin 7 of U31 is further coupled through CR14 and current-limiting resistor R194 to the pin 2 input of U31. Capacitor C18 in the feedback path between pins 1 and 2 of U31 is charged through R194 to generate a +5 to -12-Vdc level at the pin 1 output. Some clicks, pops, and other noise from the telephone line can pass through the bandpass filter to the pin 7 output of U31. Since this noise can also charge C18, and thus cause a false STATUS- signal, R194 at pin 2 of U31 limits the amount of charge that can be pumped into capacitor C18. At pin 1 of U31, the signal can range from +5 to -12 Vdc. To convert the signal to a logic level, CR15 prevents the signal from going more than one diode voltage drop below ground. At this point, the signal is called STATUS- and is sent to the pin 11 TIN (Timer Input) of the CPU at U20. The

timer can measure the duration of the STATUS- signal to determine which tone is coming from the telephone line but, at the present time, only recognizes the dial tone.

Dual-Tone Multi-Frequency Dialing. Two types of dialing can be accomodated by the telephone circuits. When tone dialing is desired, the DTMF (Dual-Tone Multi-Frequency) generator at U22 is used to generate the pair of tones that are the number tones used by the telephone system. The CPU at U20 writes a byte into DTMF latch U23 when CSDTMFW- (DTMF Write Chip Select) is low. The bits correspond to the row and column inputs of DTMF generator U22 to generate the tone. CSDTMFW- is selected by the decoder gate array at address 0030h. The tones originate at the pin 16 output of U22 by division of the 3.579545-MHz crystal frequency generated at X3. The tones, corresponding row and column inputs, key codes, etc. are listed in Table 2-x in the "Arichitecture" section.

The tone output of U22 is ac-coupled through C31 and R69 to the pin 15 A- summing amplifier input of the switched capacitor filter at U26. The tone at A- is summed with two other signals,

PHONEIN- (Telephone Input) and TXO (Transmit Output) at pin 2 of U26. TXO originates at TCARR (Transmit Carrier) from pin 9 of U24.

The tone at the pin 16 output of the summing amplifier is sent to the pin 2 input to duplexer U30. The duplexer provides conversion from the four-wire (transmit, receive, and two grounds) to the two wire (signal and return) used in telephone systems. The pin 1 output of U30 is sent to isolation transformer T1 and onto the telephone line.

Modem. The modem (modulator/demodulator) is composed of a integrated circuit modem at U24 and a switched-capacitor filter at U26. U26 is driven by a 4.0-MHz crystal at X4, tied across pins 7 and 8. U26 internally develops a 5th-order bandpass filter to allow detection of the receive data frequencies, and to filter the transmit frequencies. U26's internal oscillator also provides a 1.0-MHz clock at pin 11 to the pin 4 clock input to the modem at U24.

Data to be transmitted to the telephone line is sent from U20 on the CTX (Channel Transmit) serial channel. The format is as asynchronous

10-bit words, with each word containing one start bit, eight data bits, and one stop bit. The eighth data bit can be a parity bit or else ignored when no parity is used. When TXEN (Transmit Enable) at pin 12 is high from SQT- (Squelch), U20 modulates each bit of the words into audio tones. The words are sent via the pin 9 TXCARR (Transmit Carrier) line to pin 3 of U26 and referenced to VREF (one-half of the VDDF supply, or 2.5 Vdc) through R60. As shown in Figure 3-10, four frequencies can be sent to U26 depending on a one (mark) or zero (space) condition, and the mode that the modem is in (originate or answer).

At pin 3 of U26, the transmit signal is filtered of all its harmonics. The filtered, fundamental mark or space frequency is sent to the TXO (Transmit Output) line at pin 3 of U26 where it is ac-coupled through C20 and R54 to the pin 15 A- summing amplifier input of U26. At the pin 16 AO output of U26, the signal passes through duplexer U30 at pins 2 and 1, to pin 3 of isolation transfor T1, and then out on the telephone line.

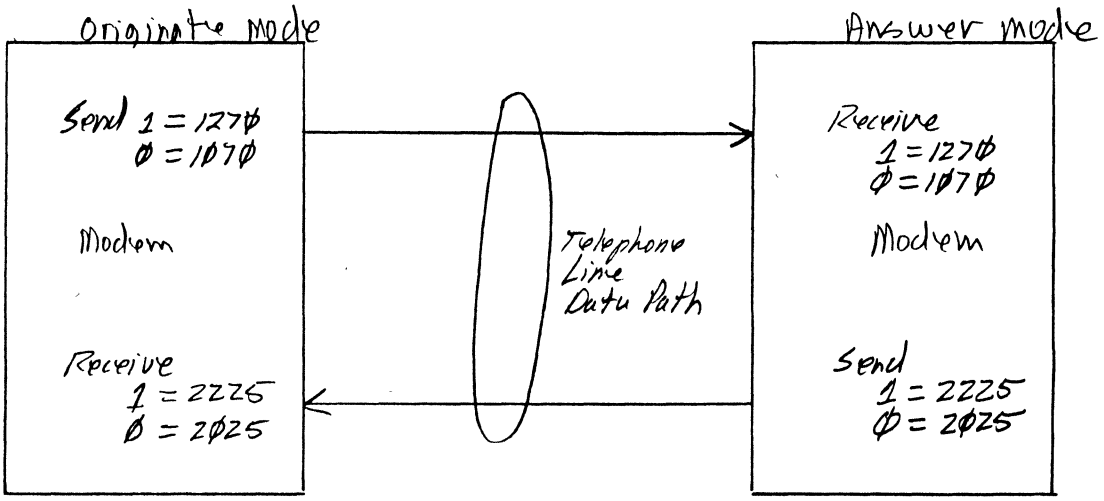

Figure 3-10. Originate/Answer Modem Frequencies (Bell 103)

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Figure 3-10. Originate/Answer Modem Frequencies (Bell 103).

Receive data signal from pin 3 of isolation transformer T1 appears at the pin 6 input of duplexer U30. The signal passes through U30 at pin 7 to the pin 13 RXI (Receive Input) of U26. At U26, the receive frequencies are detected, corresponding to the mode the filter is in at pin 12 (originate or answer), filtered, and sent to pin 14 RXO (Receive Output) of U26. The filtered receive data signal is then ac-coupled to the pin 3 input of U25. U25 performs two functions, the first of which is to pass any frequencies between 189 Hz and 7 kHz. The bandpass filter is composed of R61, R62, C26, and C27. The second function of U25 is to square up the analog signal coming from RXO. U26 is supplied power by VDDF (VDD Filtered) at +5 Vdc and grounded at VSS. Since the dc bias of the analog signals coming into U26 are different from those of U24, all analog signals are referenced to an analog ground set by VREF (Reference Voltage) at pin 5 of U26. VREF is +2.5 Vdc, or half of the supply voltage VDDF. VREF is tied to VAG (Analog Ground Voltage).

The output of U25 at pin 1 sends a logic-level square-wave to pin 1 of U24, RXCARR (Receive Carrier), whereupon they are demodulated and

converted to a serial bit stream. The data is then sent on the RXD (Receive Data) output to the MRX (Modem Receive) input at pin 8 of the tape gate array, where it is channeled to the CPU at U20.

To ensure data integrity through the modem, the data carrier from the modem on the telephone line is constantly monitored. The carrier signal is sent from the pin 14 RXO output of U26 to the input of a low-pass filter at U27. The pin 7 output of U27 only passes frequencies that are below 2500 Hz. That output is sent to a level detector at pin 3 of U27. If the level of the carrier is over 250 millivolts, pin 1 of U27 goes low as DCD- (Data Carrier Detect) to pin 31 of CPU U20. This level of 250 millivolts is the minimum required level for reliable performance of the modem. If the carrier level is below 250 millivolts, DCD- will stay high to the CPU and thus will not permit operation of the modem.

Tape and Audio Circuits

The tape and audio circuits control the tape and head motors on the tape transport, tape counting, recording and playback of both voice and data on the tape, multiplexing of multiple audio sources to multiple destinations, and amplification of the audio source to the speaker. The block diagram for the Tape and Audio circuits is shown below as Figure 3-11.

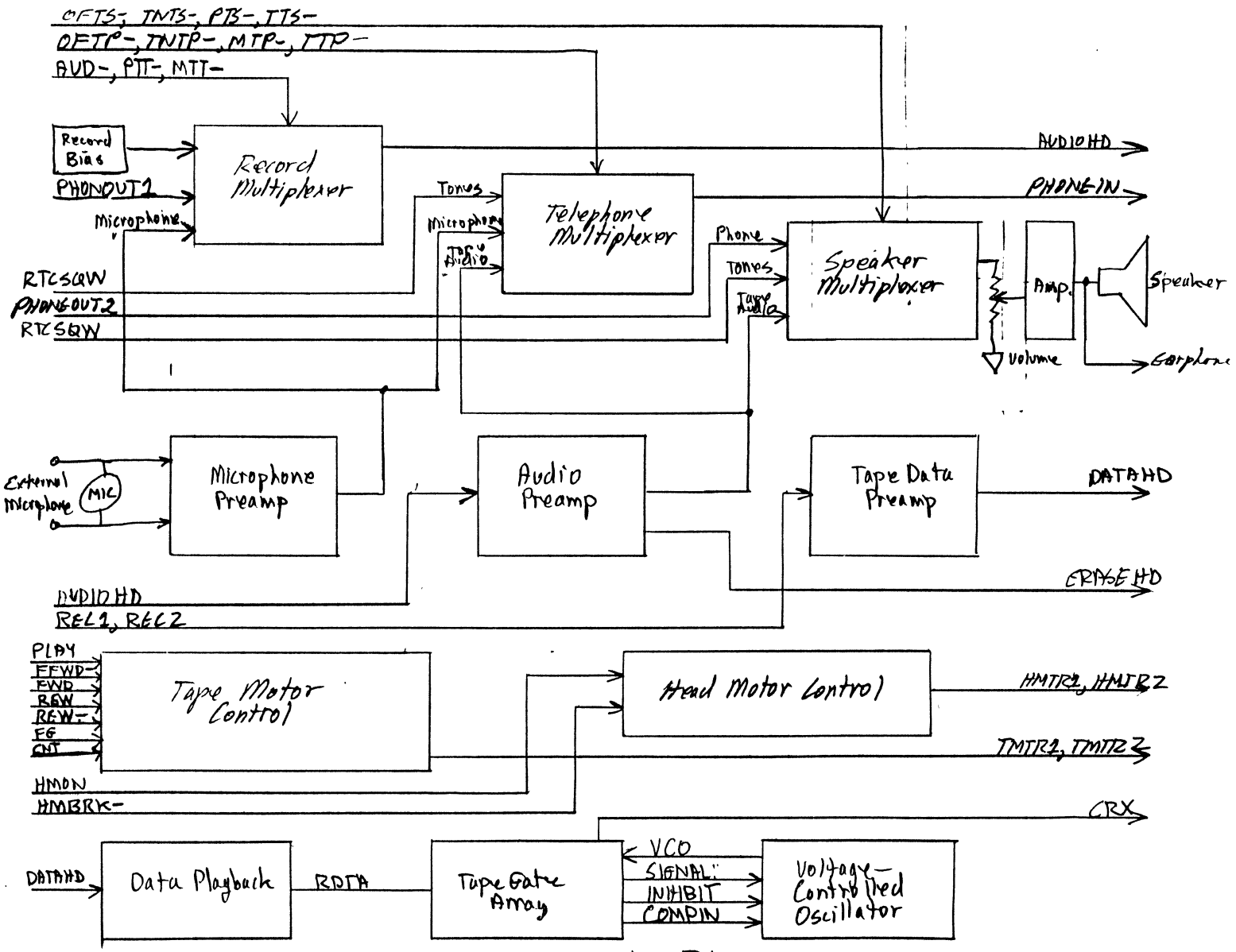

Figure 3-11. Tape and Audio Circuits Block Diagram.

Figure 3-11. Tape and Audio Circuits Block Diagram.

As shown on page x of Figure 3-3, The control circuitry for the tape motor operates in four modes: rewind, fast forward, play, and stop. The tape gate array decodes commands from software to generate the control signals to operate the tape motor.

Rewind, Fast Forward, and Stop Modes. When the tape motor is in the rewind and fast forward modes, four transistors at Q9, Q10, Q31, and Q32 provide power for the motor. Also, when the play mode is in progress, a tachometer provides feedback to the motor control circutry to regulate the speed of the tape motor. When the tape motor is stopped, Q9, Q10, Q31, and Q32 are all turned off.

Transistors Q9, Q10, Q31, and Q32 provide power to the tape motor in the fast forward and rewind modes and are configured in a standard "H" design. When the fast forward mode is selected, the tape gate array sets the FFWD- (Fast Forward) line low to the base of Q31 and the FWD (Forward) line high to the base of Q10. Q31 then supplies current to the tape motor through the TMTR1 (Tape

Motor 1) line and Q10 provides a ground return for the circuit. When the rewind mode is selected, the tape gate array sets REW (Rewind) high to the base of Q32 and REW- (Rewind-) low to the base of Q9. Q32 provides current to the tape motor through the TMTR2 (Tape Motor 2) line and Q9 provides the ground return.

Play Mode. When the play mode is used, Q8 turns on to provide a voltage ranging from 1.25 - 2.0 Vdc to Q31 to control the speed of the tape motor. The control for this servo circuit originates at a frequency generator located on the shaft of the tape motor. The frequency generator supplies a sine wave whose amplitude and frequency are proportional to the shaft speed of the tape motor. The output from the frequency generator arrives at the pin 5 input of peak detector U28 as FG (Frequncy Generator). The negative peaks of FG are detected and stored at C35, then fed to pin 2 of U28. The pin 3 input of U28 is driven by a 1.25 Vdc voltage reference supplied by zener diode CR25 through an adjustment potentiometer at R92. The CR25 voltage reference is powered by a 3.0 Vdc regulator at Q6 and Q7 from the switched +B (Battery) supply. R92 is set up by placing a

cassette, prerecoded with a 1 kHz sine wave, into the tape transport and monitoring the data output at pin 7 of U44. R92 is adjusted until the output is exactly 1 kHz. The result at pin 1 of U28 is the error voltage sent to Q8, which controls Q31 during the play mode.

Transistor Q5 disables the servo circuit when the fast forward or rewind modes are used. When the PLAY signal from the tape gate array is high, it turns on Q5, which charges C35 up to the +5 Vdc VDDSW (VDD Switched) power level. A charge this high on C35 and sent to pin 2 of U28 means that the tape motor is running too fast. In this case, pin 1 of U28 turns off, which keeps Q8 off, leaving FFWD- from the tape gate array in control of Q31.

Head Motor Control

Control of the head motor is performed by four transistors, Q11 through Q14. Q12 and Q14 operate in response to a control signal from the tape gate array, HMON (Head Motor On), to turn the head motor on and off. Transistors Q11 and Q13 apply an electronic brake to the head motor

to stop it quickly when it arrives at its position against the tape. The control signal from the tape gate array used for this purpose is HMBRK- (Head Motor Brake).

The head motor runs in one direction only. To position (load) the head against the tape, the tape gate array turns the head motor on with HMON through transistor Q13. Q13 drives Q11, which provides current to the HMTR1 and HMTR2 (Head Motor) lines. When the head motor is in position, a switch located on the head carriage mechanism opens. The signal is sent to pin 51 of the tape gate array as HPOSW (Head Position Switch). When the tape gate array gets the indication that the head is in position, it drops the HMON line and sets HMBRK- low. HMBRK- turns on Q13, which drives Q11 to brake the head motor by grounding its windings.

When the head is unloaded, the tape gate array expects that the head position switch is open. The tape gate array then runs the head motor until it gets an indication that the head position switch has closed, which it will do when the carriage gets to the other end of its travel. The tape gate array then applies the brake.

Tape Counter

A measure of the tape position is given by the tape counter circuits. Attached to the back of the takeup reel on the tape transport is a hub with four sets of alternating shiny and dark surfaces. A phototransistor, in conjuction with an LED, detects the shiny surfaces and sends this data to transistor Q15 as a sine wave. Q15 alternately saturates or turns off, thus amplifying and sqareing the sine wave. C40 is in the Q15 circuit to remove sharp transistions. The output of Q15, TCTR (Tape Counter) is sent to the pin 6 of comparator U25, which provides a logic-level signal at its pin 7 output to pin 20 of the CPU as NMI- (Non Maskable Interrupt), and to pin 52 of the tape gate array.

Tape Data Read/Write Circuits

The tape data write circuits are composed of transistors Q21, Q22, and Q23 while the tape data read circuits are composed of U44, U34, and U35. The two data tracks on the tape (one for each

side) are located on the two inside tracks of the tape. Any edge damage that may occur to the tape cassette will not affect data integrity.

Data Recording. To record data on the tape, the gate array sends two signals containing the data to the tape data write circuits, REC1 (Record) and its complement, REC2. REC1 or REC2 can never be on at the same time. Transistor Q21 turns on when REC1 is low. Q21 drives Q23, a constant current source, which generates a flux change on the tape in the negative direction through the DATAHD (Data Head) line to the tape head. REC2 turns on Q22 to generate a flux change on the tape in the positive direction.

Data Playback. Data that has been previously recorded on a tape is read back on the DATAHD input to pin 3 of amplifier U44. The first stage of U44 sends the data signal from its pin 1 output through capacitor C63 to the second stage of amplification at pin 6 of U44. C63 differentiates the data signal to convert the analog peaks to zero crossings. At the pin 7 output of U44, the data signal at 2 V peak-to-peak level and is fed to the pin 2 input of comparator U35. U35 provides some hystereis

generated by R167 and R170 at its pin 3 input. Capacitor C66 at pin 2 of U35 removes high frequency noise from the data signal. The output signal at pin 1 of U35 swings from a +5 V peak to a -5 V peak. Resistors R172, R173, and R174, and diode CR62 converts the signal to a CMOS logic level, which is applied to pin 2 of U34. The first half of U34 at pins 1, 2, and 3 of U34 inverts the data signal and applies it to pin 5 of U34. The data signal is also sent to pin 6 of U34 but it is delayed through resistor R175 and capacitor C69. This second half of U34 at pins 5, 6, and 4 functions as an edge detector to provide a positive pulse at every transition of the data signal. The result at pin 4 of U34 is applied to the tape gate array as RDTA (Read Data).

Tape Data Format and Separation

Data written on the tape comes from the pin 15 CPU serial channel CTX (Channel Transmit) line to pin 12 of the tape gate array. The data is transmitted as asynchronous 10-bit words, with each word containing one start bit, eight data bits, one stop bit, and no parity. Inside the

tape gate array, the data are converted to a format suitable for writing on the tape. A Frequency Modulation (FM) technique is used to encode data on the tape at 2.4 kHz. The rules for FM encoding are as follows:

- A flux change (transistion) occurs at every 2.4 kHz clock edge.

- If a zero is written, another transistion occurs at the mid-cell position.

The 2.4 kHz clock generated in the tape gate array is shown as the top waveform in Figure 3-12. An example of data written on the tape is shown below the clock waveform, and the resulting FM code is shown below that. Notice from the code waveform that, even if a long string of zeros occurs in the data wave form, a low dc component does not have to be written on the tape.

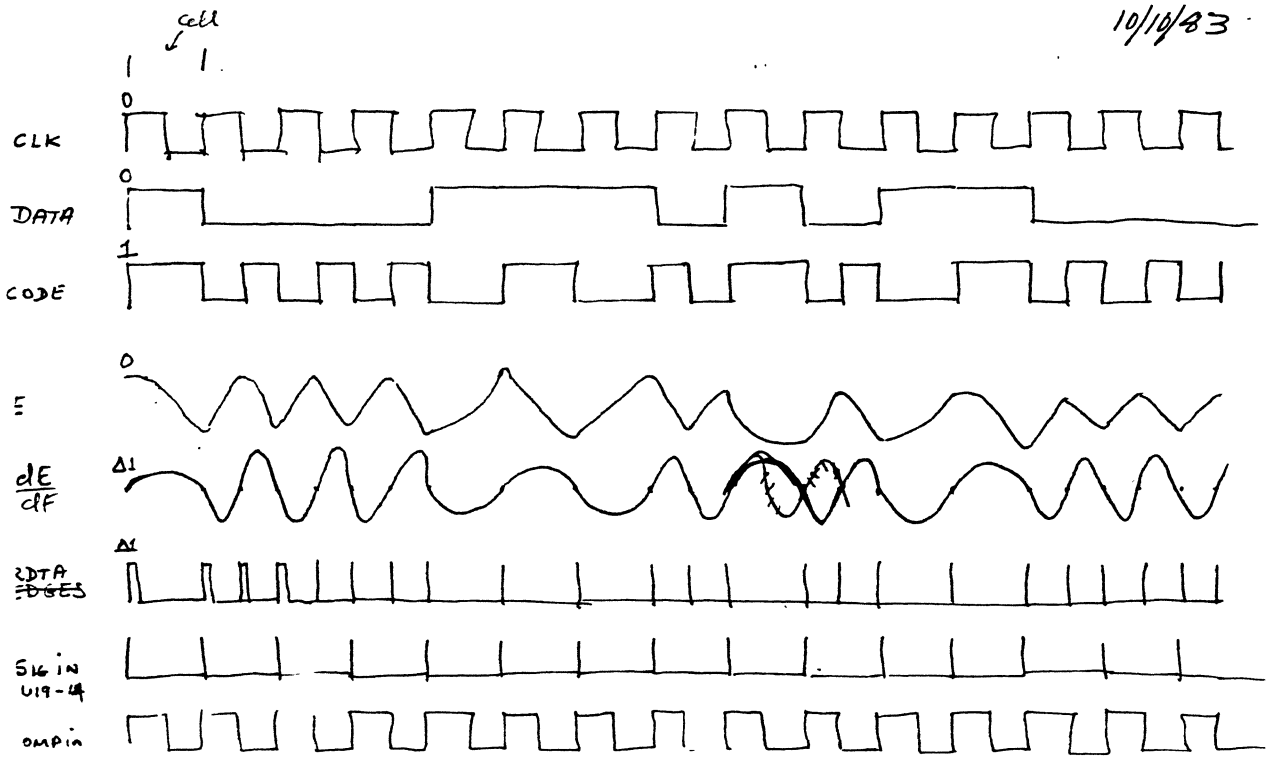

Figure 3-12. Tape Data Encoding/Decoding.

Figure 3-12. Tape Data/Clock Separation.

As discussed above, the tape gate array supplies two signals to the tape data write circuits, REC1 and REC2, to write the code waveform on the tape. REC1 and REC2 writes a waveform similar to the one identified as E in the figure.

When the data is read back from the tape, the pin 4 output of U34 detects the edges of the analog waveform written on the tape an applies this waveform to pin 56 of the tape gate array as RDTA (Read Data). At the tape gate array, the data is separated from the 2.4 kHz clock and sent to the CPU via U21's pin 21 CRX (Channel Receive) line.

Because the data stream coming from the tape is subject to motor speed variations, a Voltage-Controlled Oscillator (VCO) at U19 is used to lock the speed of the data separation circuitry in the tape gate array to the speed of the actual data stream being read from the tape.

Pin 4 of U19, SIGNAL, is sent from the tape gate array as the actual data stream being read from the tape, except that the zero pulses have been removed. In the VCO, the frequency of SIGNAL is compared to COMPIN (Comparator Input) at pin 3 of U19. COMPIN is the locking signal originally

provided by pin 4 VCO (Voltage-Controlled Oscillator Output) of U19 to the tape gate array, except that it is divided by eight inside the tape gate array. When the phase of these two signals are compared, the resulting error voltage is sent through a low-pass filter made up of R201, R202, C80, and C81 to the VCO input at pin 9 of U19. The error voltage adjusts the output frequency of the VCO at pin 4, and thus adjusts the frequency at which data is separated from the clock in the tape gate array.

Audio Recording Circuits

Audio can be recorded on tape from two sources, a microphone or the telephone. A multiplexer controlled by the tape gate array selects the source for recording. Recording is performed using a standard method, where the audio waveform is mixed with the output of a bias oscillator and applied to the audio tape head. Also, since a dc erase technique is used, a complementary dc signal must be recorded to negate the effect of the erase head on the tape. The two audio tracks are physically located at the outside edges of the tape.

Record Mode. As shown on page x of Figure 3-3, transistors Q18 and Q19 are turned on by a low AUD- (Audio) from the tape gate array when the record mode is selected. Q19 turns on Q20 to supply (along with Q18) power to a 40-kHz bias oscillator at Q17. The output at the collector of Q17 is sent to the tape head AUDIO HD (Audio Head) line through L2, C54, R143, and R240.

Microphone Circuit. As shown on page x of Figure 3-3, the microphone circuit consists of a microphone and two gain stages. The output of the microphone is applied to pin 6 of the gain stage at U46 where it is amplified and sent to the next stage at pin 2 of U46. The resulting amplified waveform is applied to pin 13 of record multiplexer U39. If an external microphone is used at microphone jack J5, the internal microphone is disconnected from the circuit.

Record Multiplexer. At the record multiplexer U39, if MTT- (Microphone To Tape) at pin 14, PTT- (Phone to Tape) at pin 8, and AUD- (Audio) control analog switches within the multiplexer. When the microphone circuit is used as the audio source for tape recording, the audio waveform

from the microphone is sent to another gain stage at pin 6 of U42 through U39's pin 11 output. The pin 7 output of U39 is sent through R140 and L3 to the audio head via the signal AUDIO HD. If PTT- is used as the audio source, MTT- is high at pin 14 and PTT- is low at pin 8. The telephone input to U39 is from the signal PHONE OUT 1 (Phone Output 1) and is discussed below.

At all times during the recoding process, AUD- is low at pin 7 of U39. As described above, AUD- from the tape gate array turns on power to the bias oscillator during tape operation. AUD- also enables a summing dc bias from pin 6 of U39 to be added to the audio source output at pin 11. The dc bias is provided by R127, R128, and R130 to negate the effect of the dc erase head.

When recording is not taking place MTT-, PTT- and AUD- are high. A high AUD- also removes power from the bias oscillator through transistors Q18, Q19, and Q20 so that no signals from the recording circutry can pass through to the audio head.

Audio Playback Circuits

As shown on page x of Figure 3-3, audio from the AUDIO HD line is coupled to transistor amplifier Q52 through capacitor C73 when the play mode is selected. At the collector of Q52, the output is sent to two more gain stages at pin of U45 and then pin 7 of U45 where the audio signal has a voltage of 1.0 to 2.0 V peak-to-peak. From pin 7 of U45, the audio signal has two paths that it can take, the telephone multiplexer at U40 or the speaker multiplexer at U41.

Telephone Multiplexer. At telephone multiplexer U40, the audio signal from the tape appears at pin 13. It is switched to the pin 11 output by the TTP- (Tape to Phone) control signal from the tape gate array. From pin 11, the output goes through a gain stage at pin 1 of U43 and is sent to the telephone circuts as PHONE IN.

Two other audio sources for the the telephone pass through U40. The first is the microphone output from pin 1 of U46 at pin 9 of U40. MTP- (Microphone to Phone) is the control signal from the tape gate array used to select this input. The second audio source is the tone output from

pin 23 of the real-time clock, U21 at pin 6 of U40. TNTP- (Tones to Phone) is the control signal from the gate array which selects the tone input. When the telephone is not being used, OFTP- (Off To Phone) is sent low by the tape gate array to turn off U41's output.

Speaker Multiplexer. At speaker multiplexter U41, the audio signal from the tape appears at pin 13. When low, the TTS- (Tape to Speaker) control line from the tape gate array sends the the tape audio to the pin 11 output of U41. At pin 11 of U41, the tape audio is sent through a gain stage at pin 7 of U43 and sent to the audio amplifier circuitry described below.

One of two other inputs to speaker multiplexer U41 are the telephone output to the audio ampliflier at pin 9 of U41. The telephone output, PHONEOUT 2 comes from pin 7 of U30, part of the audio duplexer circuit. The signal PTS- (Phone To Speaker) at pin 8 of U41 is used to select the telephone output for the audio amplifier. The other input to U41 is the tone output from pin 23 of the real-time clock, U21 at pin 6 of U41. TNTS- (Tones to Speaker) is the control signal from the gate array which selects

the tone input. When audio output is not being used, OFTS- (Off To Speaker) is sent low by the tape gate array to turn off U40's output.

Audio Amplifier

Power amplifier U48 is used to amplify the selected signal from the speaker multiplexer, U41. U48 is powered by the -12 Vdc switched power supply VEESW and can provide a gain factor of about 20 at its pin 5 output. Before the pin 3 input to U48 is the volume control, potentiometer R217. The control lug of R2 allows the user of the Workslate to control the input level to pin 3 of U48. R222, R223, and C92 after the pin 5 output of U48 are required to keep the amplifier stable. The output of U48 then passes through the earphone jack at J6 and to the speaker as SPKR. The return line for the speaker is SPKRGND (Speaker Ground). If an external speaker is plugged into J6, the internal speker connections are opened.

Power Supplies

The power suppies in the Workslate operate in two modes: Normal and Standby.

In the Normal mode, almost all of the circuits in the Workslate are powered by the two main power supplies, VDD (+5 Vdc) and VEE (-12 Vdc). VDD and VEE supply all of the power required by the circuitry, and power other sources of power within Workslate. VDD and VEE are generated from power supplied by a battery pack or a recharger plugged into the wall.

In the Standby mode, the VDD and VEE supplies are turned off. Another standby regulator operates the VDC and VDR power supplies to power the RAMs, real-time clock, tape gate array, and the CPU. All other circuitry within the Workslate is turned off. The standby regulator operates only as long as the battery pack can provide at least 3.0 Volts. Below that point, the VDC power supply is turned off and only the VDR power supply, powered by two button cell batteries, remains to preserve the content of RAM.

As shown in Figure 3-13, the Power Supplies Block Diagram the power supply circuits are composed of the following circuits:

- recharger and recharging circuit
- main power supply switch
- VDD and VEE (Normal) power supplies
- VDC and VDR (Standby) power supplies
- battery sensing circuits
- switched and filtered power supplies

During the following component-level discussion, refer to Figure 3-3, the Main Logic Board Schematic.

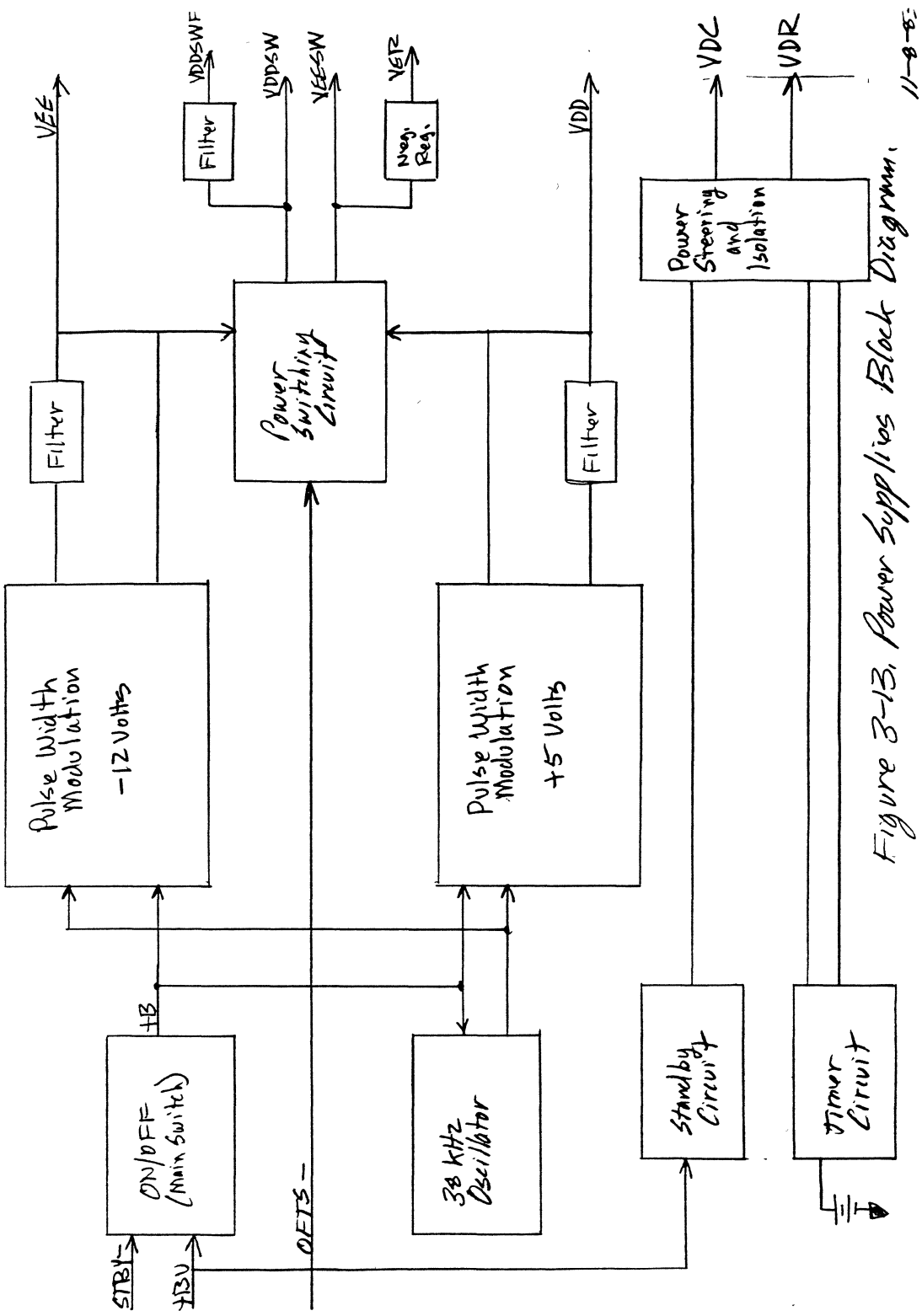

Figure 3-13. Power Supplies Block Diagram.

Recharging Circuit

On page x of Figure 3-3, transistor Q33 operates in the linear mode to provide a constant 100 mA current source for recharging the battery pack. Q33 operates only when R247 is shorted to ground by the rechargable battery pack. If a set of nonrechargable batteries is installed, R247 will never short to ground. When R247 is grounded, two diode voltage drops occurs across CR42 and CR43, and roughly one diode voltage drop across the pair of 12 ohm resistors, R248 and R249. This results in a continuous charging current of about 100 mA, regardless of the recharger voltage or the rechargeable battery pack voltage. The recharger output voltage is about 8 or 9 Vdc under normal load and no less than +6 Vdc under 800 mA load.

On/Off Circuit

To turn the power supply on and off, STBY- (Standby) from the tape gate array goes high to drive Q36, which in turn drives Q35, the main power switching transistor for the power supply. Q35 switches +BU (Battery Unswitched) from the

recharger or the battery pack to +B (Battery Switched) to supply current for the various low-power components in the power supply. In some places, note that +BU is used instead of B+ when relatively high current values are required. Those components that use +BU directly cause no current drain when +B is off (STBY- is low).

VDD and VEE Generation (Normal Mode)

To generate the VDD (+5 Vdc) and VEE (-12 Vdc) power supplies, square-wave generator U38 supplies a 38 to 40-kHz square wave for the power converter circuits. U38's output at pin 7 is clamped to +5.6 V by zener diode CR3. CR3 also eliminates most of the 60 Hz ripple present at the recharger's output. If the ripple is not removed at this point, it will eventually impose itself on the VDD and VEE supplies. If the Workslate is operated from the battery pack, the square wave peak voltage will be less than 5.6 V so that CR3 will never conduct. However, there will also be no ripple imposed on the square wave since the recharger is not in the circuit.

The pin 7 output of U38 is sent to three places, first through R264, C103, and C104 to be turned into a sawtooth wave. Secondly, an inverted copy of the sawtooth wave is generated at R272, C106, and C105 through the inverter at Q53. These components also help eliminate 60 Hz ripple. The sawtooth waves both have a voltage level of from 50 to 100 mV peak-to-peak., and also contribute to the elimination of 60 Hz ripple. The sawtooth waves are ac coupled to a reference voltage of +1.235 Vdc generated from +B by zener diode CR50. The result at pins 2 and 5 of the comparators at U36 is that of the sawtooth wave riding on top of the reference voltage. At the complementary inputs of the comparators are sample voltages of VEE at pin 1 of U36 and VDD at pin 6 of U36.

The outputs of the comparators at pins 1 and 7 generate pulses having a width proportional to the amount of time that the sawtooth wave is greater or less in amplitude to the sample voltage. For example, if the sample of VDD at pin 6 of U36 is too high in amplitude when compared with the reference at pin 5, the pulse width appearing at the pin 7 output of U36 will be shorter, since the amount of time that the sawtooth wave is greater than VDD is less. In

this way, the comparators at U36 control pulse-width modulation to regulate the VEE and VDD power supplies. There is some compliance with power supply load or input voltage using this technique. As the power supply load increases, the output voltage must decrease somewhat to increase the pulse width at the outputs of U36. In this circuit, a swing of usually 0.3 to 0.4 Vdc can be expected from a no-load, best-case situation to a full-load, worst-case situation.

From the pin 7 output of U36, VDD is generated through transistors Q34 driving Q42, which switches inductor L5 to ground. When Q42 is on, energy from +BU is stored in L5. When Q42 is turned off, the side of L5 closest to Q42 swings positive. The energy at L5 is coupled through C111 and rectified by Schottky diodes CR47 and CR48, and turned into +5 Vdc at the plus side of C113. Inductor L7 and capacitor C126 filter high frequency noise at the output. C111 is included in the circuit to prevent a direct current path to the output, since the recharger can have a voltage of as high as +12 Vdc.

From the plus side of C126, VDD is sent directly to the circuits that are powered when the

Workslate is on. The +5 Vdc from VDD is sent to steering diodes CR56 and CR59 to the VDC and VDR power supplies. These other two +5 Vdc power supplies power certain parts on the Main Logic board even when VDD is off. They are discussed below under "VDC and VDR Generation."

The -12 Vdc power supply, VEE, is generated from the variable-width pulse at the pin 1 output of U36 in a manner similar to that of VDD except that, because VEE is a negative power supply, all of the components used to generate it are functionally inverted in the circuit. Q38 drives two parallel switching transistors, Q39 and Q40 to switch inductor L6 to +BU. When Q39 and Q40 turn off, the side of L6 closest to Q39 and Q40 generates a negative voltage, which is rectified by CR49 and filtered by C107, L4, and C127. VEE sent to the circuits that require it, and is sampled at R276 to be sent back to pin 3 of U36 as a sample voltage.

The third place that the pin 7 output of U38 (the square-wave generator) is sent to is the pin 3 clock input of flip-flop U37. U37 provides a clamping mechanism for the outputs of the comparators at U36, so that they have a maximum

duty cycle of 50 percent. Also, since the Q and Q- outputs of U36 are 180 degrees out of phase, the VDD and VEE power supplies generate their outputs on alternate cycles.

U37 divides the 38 kHz square wave from U38 by two to 19 kHz. The Q output of U37 drives transistor Q41 to clamp the pin 7 output of U36 to ground on every other sawtooth appearing at pin 7 U36. Therefore, pin 7 of U36 can drive Q34 (and thus Q42 and L5) only on alternate cycles. During the time that pin 7 of U36 is clamped, the pin 1 output of U36 is allowed to drive Q38 (and thus Q39, Q40, and L6).

U37 also helps the power supply start when the Workslate is first powered up, by limiting the duty cycle of the comparator outputs of U36 to 50 percent. When VDD or VEE is at 0 volts, all that the comparators in U36 see is a very low voltage. To compensate, the comparators generate an output with a 100 percent duty cycle in an attemp to raise the voltage. This will not only fail to raise the power supply voltage but will damage Q42 (VDD) or Q39 and Q40 (VEE). Therefore, U37 is necessary to allow a maximum of half-on, half-off operation for the VDD and VEE power supplies.

Capacitor C114, connected to the pin 3 and pin 6 inputs of U36, ensures isolation between the regulation functions of VDD and VEE provided by U36. In addition, C114 allows VDD to come up to its operating voltage first, when the Workslate is powered up. The VEE power supply then follows. This reduces the turn on surge current required from the battery pack or the recharger.

VDC and VDR Generation (Standby Mode)

As was mentioned above, VDC and VDR still power certain parts of the Workslate when it is in the Standby mode. While the battery pack has adequate power, VDC and VDR supply power to the tape gate array at U29, RAM, the real-time clock at U21, and the CPU at U20 to preserve memory and provide the on/off function. If the battery pack's output goes below about 3.0 Vdc or the battery pack is disconnected, two alkaline button cells at B2 provide only VDR, which preserves the content of the RAMs for up to a year.

When the Workslate is turned off, a low-power switched regulator composed of Q44, Q45, and Q46 provides about 3.0 Vdc to keep some circuits in

the Workslate powered. This requlator eliminates the need to keep the VDD generation circuits active, thus reducing the standby power requirements of the Workslate substantially. Q45 and Q46 are a differential transistor pair driving Q44 from +BU. The zener diode at CR53 provides the 1.235 Vdc voltage reference for Q45 through Q43. From the collector of Q44, about 3.5 Vdc is sent to the steering diodes at CR57 to supply VDR, and CR60 to supply VDC. Roughly 0.5 Vdc is dropped across the diodes to the output of VDR and VDC. Note the capacitors at C119 and C130 on the VDR outputs, and C122 and C131 at the VDC outputs. These capacitors absorb transient voltages when the power supplies start up and prevent a situation in which they momentarily can become acutely current-limited upon start up. Without the capacitors, the momentary lack of adequate current can cause data to be lost in the RAMs.

When the battery pack's voltage drops to about 3.0 Vdc, Q43 turns off the regulator to avoid damaging the battery pack. One last circuit is available to power the RAM when the battery pack voltage either gets too low or the battery pack is pulled out of the Workslate. Composed of

transistors Q47, Q48, and Q49, the regulator draws power from two 90 mA/h alkaline cells at B2. Q49 stays saturated and keeps the regulator off anytime that +BU is above 3.0 Vdc, meaning that the battery pack and its regulator is still operating. Just before Q43 turns off and disables its regulator, Q49 turns off and turns on Q48 and Q47. Up until this time, +BU has kept C118 charged. C118 will discharge through Q48 and Q47 to keep VDC at 3.0 Vdc for about three minutes, which gives the owner of the Workslate enough time to install another battery pack or set of alkaline batteries before VDC goes away completely. After three minutes, Q48 and Q47 turn off and B2 powers VDR at 3.0 Vdc through steering diode CR55.

On page x of Figure 3-3, Q25 and Q26 prevent outputs from devices that are powered in Workslate's Standby mode from sinking current into the inputs of unpowered devices. When Workslate is on, that is, when VDD is at +5 Vdc, Q26 is on and the decoder gate array can select a RAM by pulling its CSRAM- line low. This reverse-biases diodes CR63 through CR70 and allows R14 through R21 to act as pulldown resistors to cause the selection. In Standby

mode, Q26 goes off, which causes R14 through R21 to act as pullup resistors through R179 connected to VDR. This reverse-biases CR63 through CR70 so that the pull-up resistors will not leak current back into the CSRAM- output of the decoder gate array. Q25, diodes CR71 through CR74, R208 through R210, and R22 operates in a manner similar to that of the Q26 circuit except, that they operate for the CSTAPE- and CSRTC- inputs to U13. Also, the power supply for the Standby mode is VDC.

Power Sensing

The tape gate array has the ability to sense the voltage of the button cells at B2 and the battery pack or recharger. This sensing circuit is made up of two comparators at U33 and two transistors, Q50 and Q51. Q50 and Q51 are used to minimize the amount of power required to operate the circuit and are normally off. When the tape gate array sets RDB (Read Battery) high, Q50 and Q51 turn on, enabling a sample of +BU and the plus side of B2 to appear at the pin 2 and pin 6 negative inputs of U33, respectively. The positive input of U33 at pins 3 and 5 are tied to

the 1.235 Vdc voltage reference supplied by CR50. If the battery pack is low, pin 1 of U33 goes high as LMT (Low Main Tank). If the button cells are low, pin 7 of U33 goes high as LST (Low Spare Tank). LMT and LST are both sent back to the tape gate array.

Switched and Filtered Power Supplies

To preserve power in the battery pack, power to the tape and audio circuits is disabled when they are not in use. The circuit that does this is controlled by OFTS- (Off To Speaker) from pin 31 of the tape gate array. OFTS- goes high anytime the software tells the tape gate array to enable a tape or audio circuit. A high OFTS- saturates Q60, which turns on Q55 and Q57. Q55 generates VDDF (VDD Filtered) required for the modem filter circuit U26, and VDDSWF (VDD Switched and Filtered). The filtering at L8, C125, C172, and L11 remove high frequency noise that might be encounterd between the power supply and the point of use and also removes the residual switching noise from the power supply. Q57 turns on Q58 and Q59, which generate VEESW (VEE Switched) for use by the tape and audio circuits.

The only other regulator used in the power supply of Workslate is Q54, a monolithic regulator, which generates VER at a maximum of 100 mA. VER is a -5 Vdc power supply and is fed by VEESW. The output of Q54 is also filtered by L9 and C59 to generate VERF (VER Filtered), which is also referenced to the ground at the point of use.

Tape Counter Input. The edge-triggered NMI- (Non-Maskable Interrupt) input at pin 20 of U20 is part of the tape counting circuitry. When NMI- is taken low, the CPU places the contents of addresses FFFCh and FFFDh into its program counter and executes the tape counter routine.

Real-Time Clock

The Hitachi HD146818 real time clock (RTC) at U21 provides the clock, calender, and alarm functions for the Workslate. The tones generated for the speaker are also generated by U21. U21 provides 64 bytes of RAM, 14 of which are used to store timing, calender, and alarm data. The other 50 bytes are available to the workslate for storage.

RTC/Processor Communication. The real-time clock is selected when the decoder gate array at U29 sets the CSRTC- line low at pin 13 of U21. Once selected, data is read from or written to U21's registers on the AD0 through AD7 lines on pins 4 to 11 of U21, respectively. From the CPU, a combination of the E clock at the pin 17 DS (Data Strobe) input and the R/W- (Read/Write) signal at

the pin 15 input are used to read or write data from or to U21. The AS (Address Strobe) input at pin 14 differentiates between address and data on the AD0 through AD7 lines. IRQ- (Interrupt Request) is sent to the CPU when U21 must get the CPU's attention for any reason. An example of U21 interrupting the CPU is when the single internal alarm timer expires. When U21 interrupts the CPU for an alarm, the CPU sets the alarm timer in U21 for the next alarm to take place. The IRQ- line to the CPU is cleared when the CPU reads register C (address 0040h).

At pins 2 and 3 of U21 is a 32.768 crystal oscillator made up of crystal X2, capacitors C6, C8 and C149, and R27. The oscillator is used to provide the time base for the clock, calendar, and alarm functions.

To prevent data in the real-time clock from being destroyed upon a power-up reset, the RESET- line at pin 18 of U21 is tied to the VDC power supply through R25. This arrangement allows U21 to be reset only when the batteries are first installed, or upon a cold start when the user inserts a pencil into the reset hole on the back of the unit.

The PS- (Power Sense) input at pin 22 of U21 is tied to VDC to determine if U21's RAM and time information is intact. PS- is tied to the VRT (Valid RAM and Time) bit in register D (address 0C4Dh) of U21. Upon a power-up reset, the VRT bit is low to indicate to the CPU that the contents of U21's RAM cannot be guaranteed. When the VDC power supply ramps to full power, and the CPU writes the proper information into U21's RAM, the CPU sets the VRT bit high.

Also tied to VDC is the CKFS input, which allows a 32.768 kHz square wave to appear at pin 21 of U21 for test purposes.

The RTCSQW (Real-Time Clock Square Wave) output at pin 23 generates the tones heard through the speaker. The frequency of RTCSQW is determined by the value in register A (address 0C4Ah). The RTCSQW output is sent to the speaker multiplexer at U41 and the telephone multiplexer at U40.

Liquid Crystal Display Controller

As shown on page 4 of Figure 3-3, the LCD (Liquid Crystal Display) controller at U11 works in conjunction with the display RAM at U1 and the display ROM at U12 to provide character data for the LCD panel. The CPU at U20 stores in the RAM the sequential list of character codes as they are to appear on the LCD panel. The LCD controller sequentially reads each RAM address and, in turn, uses that data to address a single pixel line of 8 characters out of the ROM to be shifted to the column drivers on the display.

LCD Display Organization. As shown in Figure 3-5, the display itself is organized as a pair of 64-pixel by 276-pixel fields. Each character fits into an eight-pixel by six-pixel cell, which therefore allows both halves of the display to contain a total of 16 rows, with each row containing 46 characters. Since LCD cells are, in a capacitive sense, similar to the elements in dynamic RAMs or the phosphor dots on the face of a cathode ray tube, they must be refreshed at regular intervals if they are to appear without flickering. The reason for the top and bottom LCD displays is to address them separately to allow the duty cycle (or refresh time) of any pixel to be 1/64th of the time it takes to write all of the pixel data into the LCD cells.

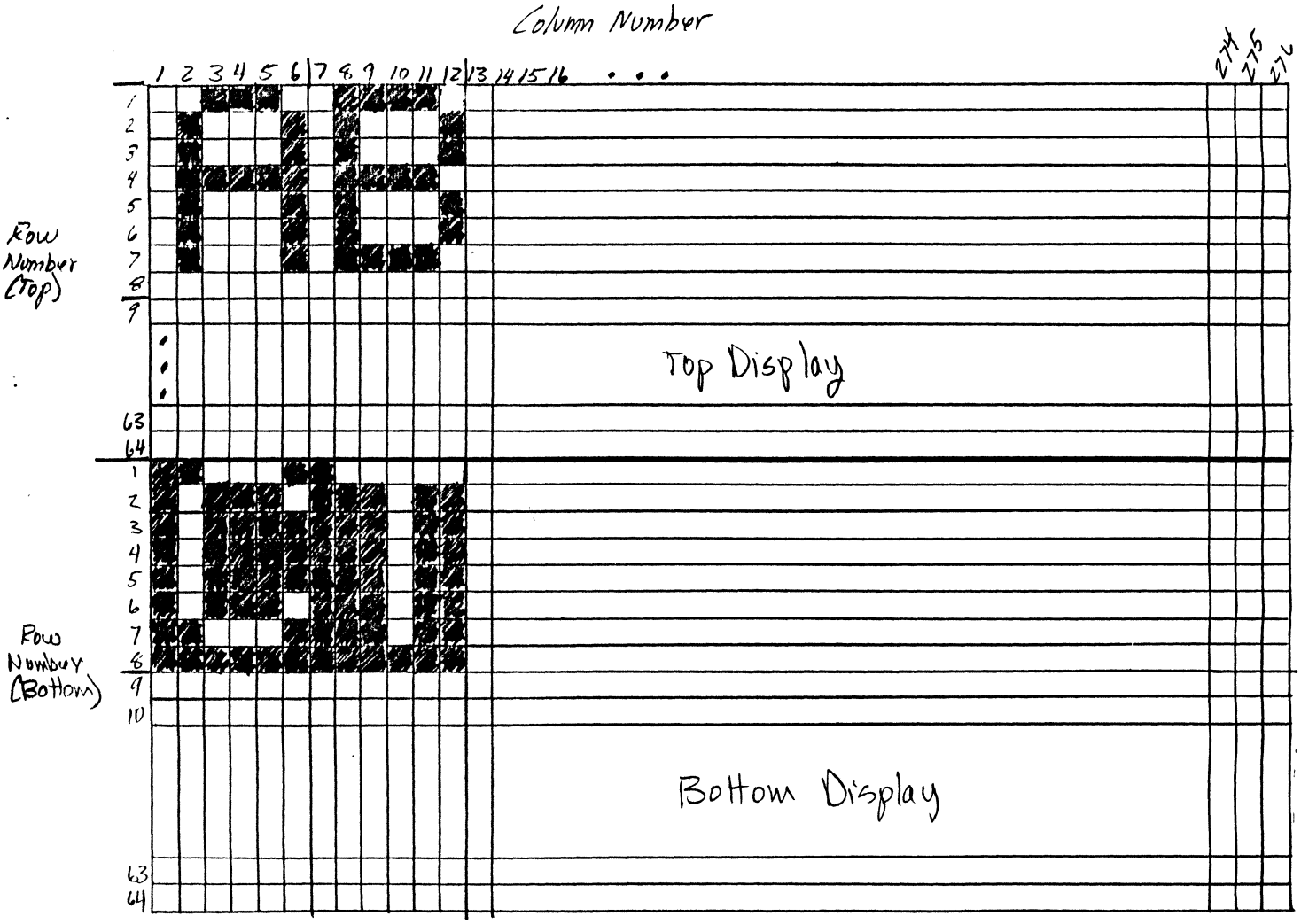

Figure 3-5. LCD Display Organization

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Figure 3-5. LCD Display Organization.

The LCD controller at U11 writes an entire row (276 bits) of serial pixel data into the LCD panel's column drivers for the top and bottom halves of the display before going on to the next row. U11 actually writes one bit to the top half of the panel's column drivers and then writes the next pixel bit in the same column position in the lower half of panel's column drivers, exactly 64 pixel rows down.

When the last pixel has been written to the column drivers, all 276 bits for both halves of the display are sent to their corresponding positions of a row of LCD cells. At the same time, the row drivers are incremented by one and the next row of pixel bits are shifted into the column drivers. Therefore, 64 rows are written in each half of the display before the controller gets around to writing the first row of pixels again. This is where the 1/64th duty cycle figure comes from.

LCD Cortroller Operation. The CPU at U20 communicates with U11 directly through its AD0 through AD7 address and data lines when CS1ISP- (from the decoder gate array) is low at pin 15 of U11. U20 writes instructions into the internal

registers of U11 and ASCII (American Standard Code for Information Interchange) character data into the display RAM at U1. The R0 line (address line A0) at pin 18 of U11 distinguishes between the instruction and data registers inside U11. The characters written into U1 form an ASCII-coded "image" of the characters displayed on the top and bottom halves of the LCD panel. U11 addresses each location in U1 with the MA0 through MA10 memory address lines. When CS- (Chip Select) is low at pin 18 of U1, the data from the RAM appears on the MD0 through MD7 data lines to U1.

The first byte written into U1 at address 0000 is the ASCII equivalent of the character that appears on the first row on the top half of the LCD panel in the left-most character position. The next character code read from the RAM (this time for the bottom half of the display) has its address offset by 368 (170h), and appears as the left-most character on the ninth row. (The number 368 is exactly half of the characters allowed on the panel.) Next, address 0001 is read, which corresponds to the character just to the right of the first character on the first row. The LCD controller uses these ASCII codes

as addresses into the display ROM at U12 to look up the actual pixel pattern of the characters to send to the LCD panel.

When U11 reads an ASCII character code from the display RAM, it sets an internal three-bit row counter. The three row bits are appended to the character code and used as the address for the display ROM at U12. Starting from the first pixel on the first line of the display, the row counter bits are all zero.

U11 addresses U12 through the MD0 through MD7 (Memory Data) lines corresponding to U11's A3 through A10 address lines, and the MA12 through MA14 (Memory Address) lines corresponding to the A0 through A2 address lines. Data from the ROM appears on U11's MD0 through MD7 lines when CE- (Chip Enable) is low at pin 18 of U12. The display RAM at U1 and the display ROM at U12 are alternately selected by the flip-flop at U17.

As the first line of the first character on the first row of the display is read out of the display RO , U11 reads the next ASCII character out of the RAM for the first line of the first character on the ninth row of the display. U11

then addresses the display ROM for that character and so on until the first line of all 46 characters are shifted into the column drivers for the first and ninth rows of the display. At that time, the row counter inside U11 increments to the next row (001) and the same character codes are again read out of the RAM. U11 addresses the second row of character data from the ROM using the modified address. This operation continues until the display is fully refreshed.

Liquid Crystal Display

The two serial bit streams, one for the top half of the display and one for the bottom half, are sent to the LCD panel column drivers as D1 and D2, respectively at connector J8. D1, D2, and other signals sent to the LCD panel through J8 are as follow :

Signal	J8 Pin	Description
FC	1	Frame ground (to power supply)
VDD	2	+5 Vdc display supply
VSS	3	-12 Vdc display supply

V-	4	-10 Vdc display supply (variable)
D1	5	Top display pixel data
FLM	6	Frame synchronization signal
D2	7	Bottom display pixel data
MB	8	Square wave
CL1	9	Display data latch clock
CL2	10	Display data shift clock
FG	11	Frame ground (to power supply)

Note that V0 is supplied by Q1 through the CONTRAST potentiometer R24. CONTRAST adjusts the negative level of V0 and thus adjusts the angle at which light is reflected from the LCD panel.

LCD Column Drivers. On the LCD Display Board (see Figure 3-6) are 14 MSM5839GSK column drivers, seven for the top half of the LCD panel (U4 through U10) and seven for the bottom half of the panel (U11 through U17). Each column driver controls 40 columns of LCD cells at its outputs and contains a pair of 20-bit shift registers, two 20-bit latches, a 40-bit level shifter, and 40 four-level drivers. Pixel data is shifted

Figure 3-6. LCD Display Board Schematic.

into and through shift registers in the column drivers on D1 and D2 by the CL2 data shift clock. For example, at the pin 44 D1 input of U4, pixel data arrives at the pin 51 DI1 (Data Input 1) input and is shifted by CL2 through the first 20-bits shift register, out through pin 44 to the pin 43 DI2 (Data Input 2) input, through the second 20-bit shift register, and out to the next column driver at U5. A total of 276 cycles of the CL2 clock occur when the column drivers are being loaded with pixel data. Simultaneously, pixel data from the D2 line of the LCD controller is being shifted into U11 through U17 for the bottom half of the LCD panel. Once the pixel data is loaded, CL1 (Clock 1), the data latch clock makes a transition to parallel load all 276 bits of pixel data into the latches and thus to the 40-bit level shifter and drivers. The purpose of the four-level drivers and their associated voltages is described below.

LCD Row Drivers. On the right side of Figure 3-6 are two MSM5838GSK row drivers at U1 and U2, one for each half of the LCD panel. Each row driver drives 32 rows of LCD cells at its outputs and contains a pair of 32-bit shift registers, a 32-bit level shifter, and 32 four-level drivers.

Each of the outputs of U1 and U2 go to two LCD row conductors on the 128 pin connector, because two rows of pixels are turned on or off at one time. FLM, the frame synchronization signal, is used as the data input for U1 and U2. As CL1 loads the pixel data onto the display from the column drivers, it also shifts the FLM bit over in the U1 and U2 shift registers, thus changing the two rows on the display that are active.

In the LCD cells, the voltages sent from the row and column drivers turn on (darken) or turn off (keep transparent) the cell.

LCD Pixel Behavior. The LCD material is a twisted nematic type. The natural state of the material is its twisted form, which appears transparent to the viewer. When the correct difference of potential (voltage) is applied across the row and column metalization areas that define the cell, the nematic molecules line up vertically across the metalization areas, causing a darkening effect. The voltages applied to the display originate at a voltage divider made up of R1 through R5. The voltages V0 through V4 are buffered at U3 and sent, along with VDD, to the four-level driver inputs of the row and column drivers.

Figure 3-7 shows, for one pixel cell, the voltages applied to the row driver, column driver, and the resulting pixel voltage. The voltage across the pixel is a combination of the row voltage minus the column voltage. To darken the pixel, that is, to turn it on, a voltage of VDD - V5 is required. To leave the pixel off, a voltage of V4 - V5 is required. Note that the "off" voltage is below the threshold level required to turn the pixel on.

In the row and column waveforms, the controlling voltage for the pixel is superimposed on a square wave. During half the time that a pixel is being refreshed, the square wave allows the controlling voltage to be positive. The other half of the time the controlling voltage is negative. The square wave is generated by the M3 signal from the LCD controller and is used to ensure a <u>net</u> dc bias of 0 volts on the pixel cell. If a net plus or minus dc bias was allowed to exist in the cell, the metalization areas defining the cell would eventually be damaged through a plating action, and the display would lose contrast.

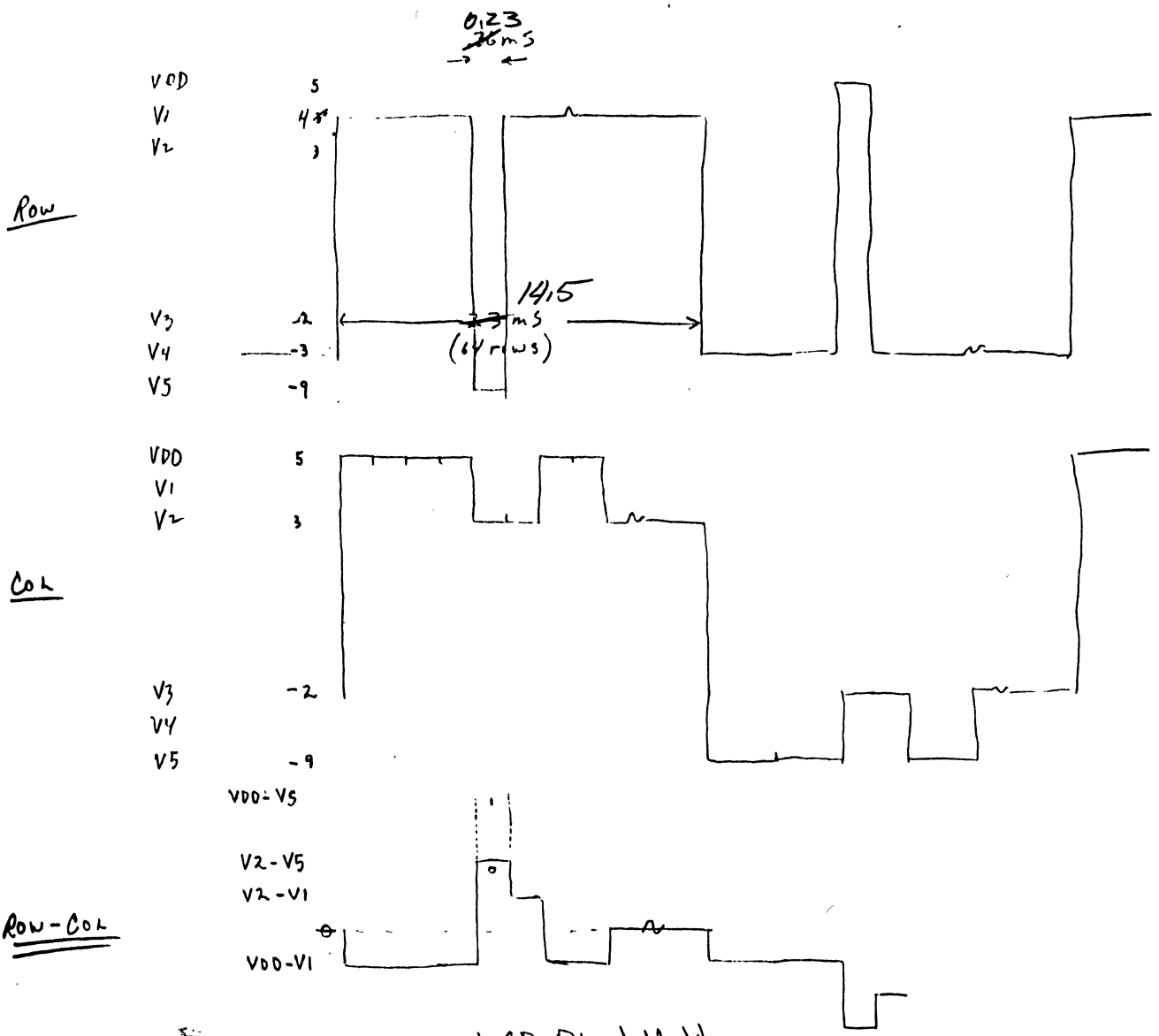

Figure 3-7. LCD Pixel Voltage.

Figure 3-7. LCD Pixel Voltage.

The period of the pulses that turn on the pixel correspond to the 69 Hz refresh rate of the display. On the row waveform in Figure 3-7, each pixel in every row position is refreshed one time between the leading edge of the positive pulse to the leading edge of the negative pulse, which is enountered the next time that the pixel is refreshed, about 14.5 milliseconds later.

The width of the controlling pulses themselves are determined by the 1/64th duty cycle of the display and the refresh rate. To refresh the display 69 times a second, the display data latch signal CL1 from the LCD controller must load all of the pixel information into the column drivers and increment the row 64 times (0.23 milliseconds) within the period of 14.5 milliseconds.

Decoder Gate Array

As shown on page x of Figure 3-3, the decoder gate array at U13 provides device (chip) selection lines and read and write strobes for the various addressable devices within the digital system. U13 also acts as an buffer for

the address and data busses from the CPU, and generates READ- and WRITE- strobes from the CPU's E clock and R/W- line.

Decoder Chip Select Outputs. The decoder gate array decodes chip select lines by monitoring the AD0 through AD7 and A8 through A15 lines when the AS (Address Strobe) line from the CPU is high. The chip selects are as follows:

Chip Select	Function
CSRAM0- to CSRAM7-	RAM Chip Selects. The eight available RAM chip select lines CSRAM0- to CSRAM7- are at pins 37 to 30, respectively. If 2K by 8-bit RAMs are used, all eight lines are used to address a total of 16K bytes of data. If 8K by 8-bit RAMs are used, only the first four lines (CSRAM0- through CSRAM3-) are used to address a total of 32K bytes of RAM. The remaining CSRAM- lines are always high.

CSROM0- to CSROM2-

ROM Chip Selects. The three available ROM chip select lines CSROM0- to CSROM3- are at pins 41 to 39, respectively. ROM addressing itself starts at address 8000h. The three ROMs are 32K by 8-bit types. Since 32K-bytes of the total address space is allocated to the RAM complement, and the available address range is 64K bytes, the addresses of the ROMs overlap each other and must therefore be bank switched. Bank switching is performed by the BANKA- (Bank A) and BANKB- (Bank B) lines from the CPU. Assuming that an address higher than 8000h is present on the address lines from the CPU, when BANKA- and BANKB- are high at pins 28 and 29, respectively, CSROM0- goes low to select ROM 0 at U14. (Note that CSROM0- is always low when the Workslate is first turned on.) If BANKA- is low and BANKB- is high, CSROM1- goes low to select

ROM1 at U15. If BANKA- is high and BANKB- is low, CSROM2- goes low to select ROM2 at U16.

CSKBDR-
CSKBDW-

Keyboard Chip Selects. Two chip selects are decoded for keyboard scanning. When CSKBDW- is low, the CPU writes a 1 to one of the eight bit positions in keyboard latch U10. The CPU then sets CSKBDW- high and CSKBDR- low to read the contents of keyboard buffer U18. In this way, the CPU can determine which keys on the keyboard are being pressed. A complete keyboard scan occurs every 10 milliseconds.

CSTAPER0-
CSTAPEW0-
CSTAPEW1-

Tape Gate Array Chip Selects. Three chip selects are used to select functions inside the tape gate array; one for read functions, such as the tape counter input; and two for write functions, such as selecting motor control and multiplexer functions.

CSDTMFW- Dual-Tone Multi-Frequency Generator Chip Select. When CSDTMFW- is low, the CPU can write an eight-bit code into the DTMF latch at U23 corresponding to the tone it wants to send to the telephone circuits. The DTMF at U22 is used for tone dialing.

CSRTC- Real-Time Clock Chip Select. When CSRTC- is low, it selects the real-time clock for a read or write operation by the CPU.

CSDISP- Liquid Crystal Display Chip Select. When CSDISP- is low, it selects the liquid crystal display controller for a read or write operation by the CPU.

Tape Gate Array

The tape gate array at U29 provides control functions for several areas of the Workslate. The tape gate array:

- o decodes control signals for tape and head motor control, tape sensing, and tape and audio source multiplexing,

- o provides encoding and decoding circuits for conversion of serial data to and from the FM (Frequency Modulation) format used for data recording on the tape drive,

- o controls power-up and power-down sequencing.

- o channels data received by the modem and the GPIO (General-Purpose Input/Output) to the CPU.

Control Signal Decoding. To decode control signals, the CPU addresses U29 (see page x of Figure 3-3) with the CSTAPEW0-, CSTAPEW1-, and CSTAPER0- chip select lines originating at the decoder gate array. The three chip selects control the selection of three registers inside U29 to provide the following signals:

CSTAPEW0-

U29 Pin	Function
2 and 3	REW and REW- (Rewind). When high and low respectively, these lines set the tape motor control circuitry in the rewind mode.
4	FFWD- (Fast Forward). When low, this line sets the tape motor control circuitry in the fast forward mode.
5	PLAY- (Play). When low, this line sets the tape motor control circuitry in the fast forward mode.
61	HMON (Head Motor On). When high, this line turns the head carriage motor on.
62	HMBRK- (Head Motor Brake). When low, this line abruptly stops the head carriage motor.

63 AUD- (Audio). When low, this line turns on the audio recording circuits and also permits the record bias voltage to pass through the record multiplexer to be mixed with the audio source.

64 ERASE- (Erase). When this line is low, it turns on the erase head on the head carriage.

65 PTT- (Phone to Tape). When this bit is low, it allows audio from the telephone circuits to be recorded on tape.

66 MTT- (Microphone to Tape). When this bit is low, it allows audio from the microphone circuit to be recorded on tape.

67 FWD (Forward). This line, when high, is used in conjunction with the PLAY line to set the tape motor control circuitry in the play mode.

U29 Pin	Function
31	OFTS- (Off to Speaker). When OFTS- is low, it turns off the power supplies associated with the audio circuitry (VEESW, VDDF, VDDSWF, and VER) and also disables the speaker multiplexer at U41 to the speaker.
32	TNTS- (Tones to Speaker). When TNTS- is low, it permits the square-wave output from the real-time clock (RTCSQW) to pass through the speaker multiplexer at U41 to the speaker.
33	PTS- (Phone to Speaker. When PTS- is low, it permits the PHONEOUT2 line from the audio duplexer circuit to pass through the speaker multiplexer at U41 to the speaker.

36 TTS- (Tape to Speaker). When TTS- is low, it permits the output from the tape playback circuits to pass through the speaker multiplexer at U41 to the speaker.

37 OFTP- (Off to Phone). When OFTP- is low, it disables the telephone multiplexer at U40.

38 TNTP- (Tones to Phone). When TNTP- is low, it permits the square-wave output from the real-time clock (RTCSQW) to pass through the telephone multiplexer at U40 to the telephone.

39 MTP- (Microphone to Phone). When MTP- is low, it permits audio from the microphone circuit to pass through the telephone multiplexer at U40 to the telephone.

40 TTP- (Tape to Phone). When TTP- is low, it permits audio from the

	tape playback circuits to pass through the telephone multiplexer at U40 to the telephone.
43	RDB (Read Battery). When high, this line permits the level of the batteries to be read.

CSTAPERO-

U29 Pin	Function
46	Unused.
47	Unused.
48	LST (Low Spare Tank). When this input is high, the button cells are almost exausted.
49	LMT (Low Main Tank). When this input is high, the rechargable battery pack (or alkaline cells) are almost exausted.

50 COUT (**Can't find this one on the schematic, and I don't remember it being discussed. What is it?**

51 HPOSW (Head Position Switch). This input toggles to indicate that the tape read/write head is either at the top of its travel or is positioned aginst the tape.

52 TCTR (Tape Counter). When high, this input indicates a tape count pulse. The CPU counts TCTR to determine tape position.

Tape Data Encoding/Decoding. The role of the tape gate array in encoding and decoding data for tape recording and playback is discussed in the "Tape and Audio Circuits" subsection under "Tape Data Format and Separation."

Power Sequencing. Power-up and power-down sequencing is also performed by circuits in the tape gate array. The Workslate is in an off when the two major power supplies, VDD and VEE, are not running. When off, power required to retain the contents of RAM and several other functions is provided by the battery pack or recharger, which still operates the VDC and VDR power supplies. During this time, the tape gate array has power applied to it.

When the user presses the ON/OFF key on the keyboard to power up the Workslate, the ON/OFF switch causes PB- at pin 44 of the tape gate array to go low. (Note on the schematic that the ON/OFF switch is not part of the keyboard matrix but is directly tied to the gate array input.) The tape gate array sets STBY- low at pin 42 to turn on the main power supplies, VDD and VEE. About 4.7 milliseconds later, the time constant set by R47 and C32 across the pin 16 RES1 (Reset 1) and pin 17 (Reset 0) inputs of U29 expires, which causes RES- (Reset) at pin 18 to go low for at least 20 milliseconds. RES- resets the CPU at U20 and the LCD controller at U11. When RES- goes high again, the CPU loads the contents of addresses FFFEh and FFFFh into its program

counter and begins to execute the software power-up routine.

One of the elements of the power-up routine is an examination in RAM of the ROM checksum. If the ROM checksum was found to be correct from the last time the Workslate successfully powered down, the software will to do a warm start in which the it essentially continues with the work it was performing before with the contents of RAM intact. If the ROM checksum was found to be incorrect, the software will do a cold start, in which the software assumes that no information concerning date or time is correct and performs a destructive RAM test.

A cold start can also be initiated through reset switch S1. When S1 is grounded as COLDST- (Cold Start), the software executes the same power-up routine. When the software finds the incorrect ROM checksum, it will perform the cold start.

When the user presses the ON/OFF key to power down the Workslate, the tape gate array sets the ON/OFF- signal to pin 32 of U20 low. Upon receipt of this signal, CPU goes into a housekeeping routine to save the contents of

registers and data in RAM. When the CPU has executed the routine, it writes to the tape gate array at I/O port 2Ch, indicating that it is safe to power down. The tape gate array then pulls the STBY- (Standby) line low at pin 9 of U20. When the CPU senses that STBY- is low, it goes into a routine to save the contents of its internal registers in its own 128 bytes of RAM.

Tape Gate Array Serial Channel. Finally, U29 channels serial data to and from the CPU for the tape read and write circuits, and to and from the GPIO port. Also, read data from the modem at U24 is sent along the serial channel.

Serial data sent to U29 intended for the tape read and write circuits or the GPIO is received at pin 12 of the tape gate array as CTX (Channel Transmit). The destination is selected by bits 4 and 5 of the register selected when CSTAPEW1- is selected by the decoder gate array. Data sent to the tape write circuits is first encoded into an FM (Frequency Modulation) format and sent to the write circuits at 2400 baud on the pin 55 REC1 line and the complementary pin 54 REC2 (Record) line. If the GPIO is selected, data is sent on the pin 6 GTX (GPIO Transmit) line to the J4 GPIO connector.

Data input from the tape read circuits arrives at the tape gate array as RDTA (Read Data) and is decoded from its FM format to asynchronous 10-bit words, with each word containing one start bit, eight data bits, one stop bit, and no parity. The decoded tape read data is sent to the CPU on the pin 21 CRX (Channel Receive) line to the CPU at 2400 baud. Data from the pin 7 GPIO GRX (GPIO Receive) is sent to the CPU on the CRX line at 9600 baud. Likewise, data from the modem is sent from the pin 8 MRX (Modem Receive) line to the CPU on CRX at 300 baud. The source for CRX is selected by bits 4 and 5 of the register selected when CSTAPEW1- is selected by the decoder gate array. Note that data is not sent to the modem through the tape gate array. When the modem is not in use, no power is applied to it and therefore, data on the serial channel has no effect on the modem.

Keyboard

As shown on page x of Figure 3-3, the keyboard scanner is composed of latch U10 and buffer U18. When CSKBDW- is low, the CPU writes a 1 to one of

the eight bit positions in keyboard latch U10. The CPU then sets CSKBDW- high and CSKBDR- low to read the contents of keyboard buffer U18. In this way, the CPU can determine which keys on the keyboard are being pressed. A complete keyboard scan occurs every 10 milliseconds. The keyboard matrix appear as shown in Figure 3-8.

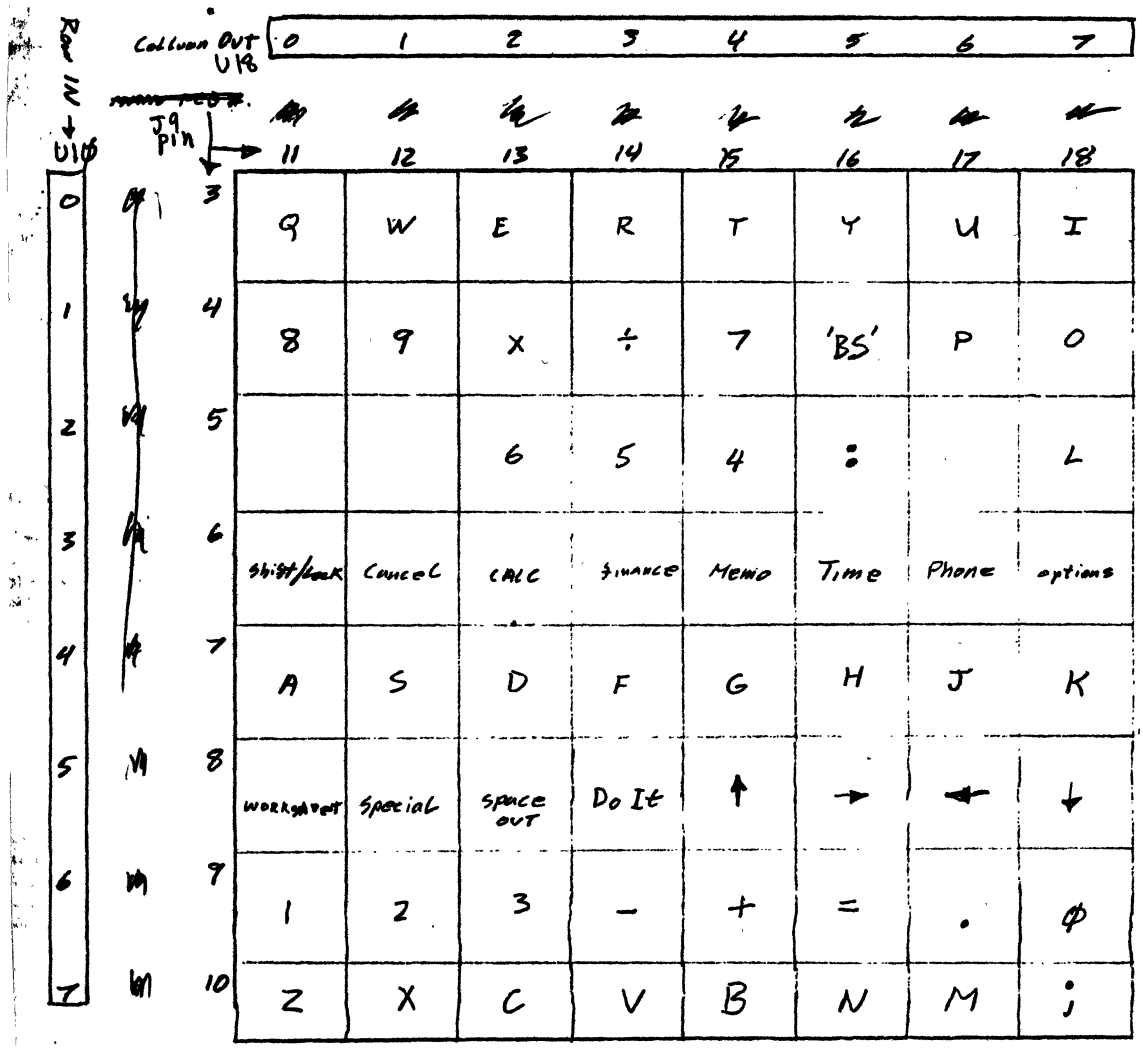

Figure 3-8. Keyboard Matrix.

Figure 3-8. Keyboard Matrix.

RAM Complement

The Workslate can contain either eight 2K-bit by eight-bit static CMOS RAMs for a total of 16K bytes of storage, or four 16K-bit by eight bit static CMOS RAMs for a total of 32K bytes of storage. In either case, the RAMs have power applied to them always, as long as the two button cells are not exhausted.

The RAMs at U2 through U9 (see page x of Figure 3-3) are selected using the CSRAM- chip select lines from the decoder gate array at U13. If 2K by 8-bit RAMs are used, all eight lines are used to address a total of 16K bytes of data. If 8K by 8-bit RAMs are used, only the first four lines (CSRAM0- through CSRAM3-) are used to address a total of 32K bytes of RAM. The remaining CSRAM- lines are always high.

The A0 through A7 address lines for the RAMs originates at the decoder gate array. The A8 through A10 address lines (or A8 through A13 address lines) originate directly from the CPU at U20. The eight D0 through D7 data lines for the RAMs originate at the decoder gate array. WE- (Write Enable) at pins 21 of the RAMs, and OE-

(Output Enable) at pins 20 of the RAMs correspond to the WRITE- and READ- strobes from pins 62 and 63, respectively, on the decoder gate array.

ROM Complement

As shown on page x of Figure 3-3, the Workslate uses three CMOS ROMs at U14, U15, and U16 that arranged to hold 32K bits by 8 bits. Because the ROMs are 32K-bit types, they must be bank-switched by the CPU since 32K-bytes of the total address space is allocated to the RAM complement and the CPU has an available address range is 64K bytes. Bank switching is performed by the BANKA- (Bank A) and BANKB- (Bank B) lines from the CPU. The decoder gate array decodes the BANKA- and BANKB- lines from the CPU into chip selects for the three ROMs, CSROM0-, CSROM1-, and CSROM2, which correspond to OE (Output Enable) input at pins 22 on U14, U15, and U16.

The A0 through A7 address lines for the ROMs originates at the decoder gate array. The A8 through A14 address lines originate directly from the CPU at U20. The eight D0 through D7 data lines for the ROMs originate at the decoder gate