Workstation Hardware

First Edition Revised, Update Notice 5
A-09-00228-01-A

The attached pages update: (1) edition A-09-00016-01-A and Update Notices A-09-00058-01-A, A-09-00066-01-A, A-09-00091-01-A, and A-09-00177-01-A or (2) edition A-09-00016-01-B and Update Notices A-09-00066-01-A, A-09-00091-01-A, and A-09-00177-01-A of the Workstation Hardware Manual.

Insert these pages according to the collating instructions on the back of this Notice.

Updated pages are indicated by a date at the bottom of the page.

Throughout this Manual, change bars in the margins indicate technical additions and changes. Asterisks indicate deletions. Editorial changes are not identified. All changes will be incorporated into the next editions of this Manual.

Insert this page after the title page of your Manual to provide a record of this update.

Convergent Technologies

COLLATING INSTRUCTIONS

These instructions apply to Volume 2 of the Workstation Hardware Manual.

VOLUME 2

Delete	Replace with
iii to v	iii to vi
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DESCRIPTION OF CHANGES

Section 14 describes architecture and theory of operation of the Multiline Communications Processor (MLCP) board.

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10. Video Monitor (CRT)

11. Console Switches

12. Power Supply

13. Communications I/O Processor Board

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14. MULTILINE COMMUNICATIONS PROCESSOR BOARD

OVERVIEW

Introduction

This section of the Workstation Hardware Manual provides a hardware description of the Multiline Communications Processor (MLCP) board, which is designed to expand the serial communications capabilities of the IWS and the monitor form of the IWS workstations. This section is divided into the following three parts:

- Overview
- Architecture
- Theory of Operation

The "Overview" describes the capabilities of the MLCP board in hardware and, to some extent, software control.

The second part, "Architecture," covers memory mapping of the local bus, CT-BUS, and Multibus, and discusses the various programmable components of the MLCP board.

"Theory of Operation" details the component-level circuit description of the applicable board hardware.

General Description

The MLCP board is designed for applications requiring expanded communications capabilities of the IWS and the monitor form of the IWS workstations. Up to five MLCP boards, each containing a dedicated 5-MHz 8085A-2 processor, 4K bytes of bootstrap ROM, and 64K bytes of local dynamic RAM, can be installed in the monitor form of the IWS workstation to support a total of 20 serial communications channels. In addition, two MLCP boards supporting a total of eight communications channels can be installed in an IWS workstation.

In the monitor form of the IWS workstation, up to 20 external cables connect directly into the MLCP boards via standard RS-232-C connectors on the rear of the workstation electronics box. Up to

eight external cables can be plugged into the IWS workstation through one or two interface boxes, which connect to the MLCP boards within the workstations via ribbon cables. Each interface box contains four standard RS-232-C connectors that can be connected to peripheral devices. (Refer to the Multiline Communications Processor Board for the IWS Workstation: Installation Instructions and the Multiline Communications Processor Board for the Monitor Form of the IWS Workstation: Installation Instructions.)

Communications software (that is, the Multiline Executive and MLCP link-level drivers) executes directly in the board's own local RAM to allow the workstation CPU to perform other tasks more efficiently. A simplified block configuration of the MLCP board is shown in Figure 14-1.

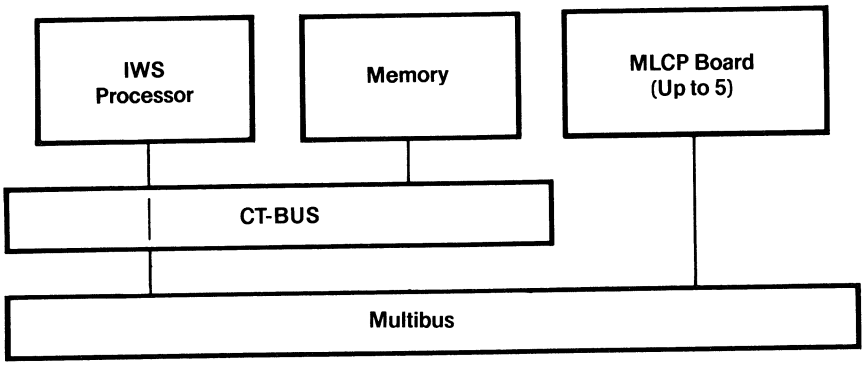


Figure 14-1. MLCP Block Configuration.

Communications Capabilities

Each MLCP, which acts as a slave processor (Figure 14-2), supports four independent RS-232-C channels (ports) with two full-duplex Multi-Protocol Serial Controllers (MPSCs). Each channel supports asynchronous, byte-synchronous, and bit-synchronous protocols. The MPSCs transfer data to and from the communications channels under control of the local 8085A-2 processor. The transmit and receive clocks for each channel may be generated internally for use by asynchronous modems or externally by synchronous modems. The baud rate of each channel is software programmable up to 9.6 kilobaud in a full-duplex mode. The total aggregate baud rate for

an MLCP board, with full-duplex channels counting as twice the channel rate, is 38.4 kilobaud. The MPSCs may operate in polled or interrupt mode, depending upon the application.

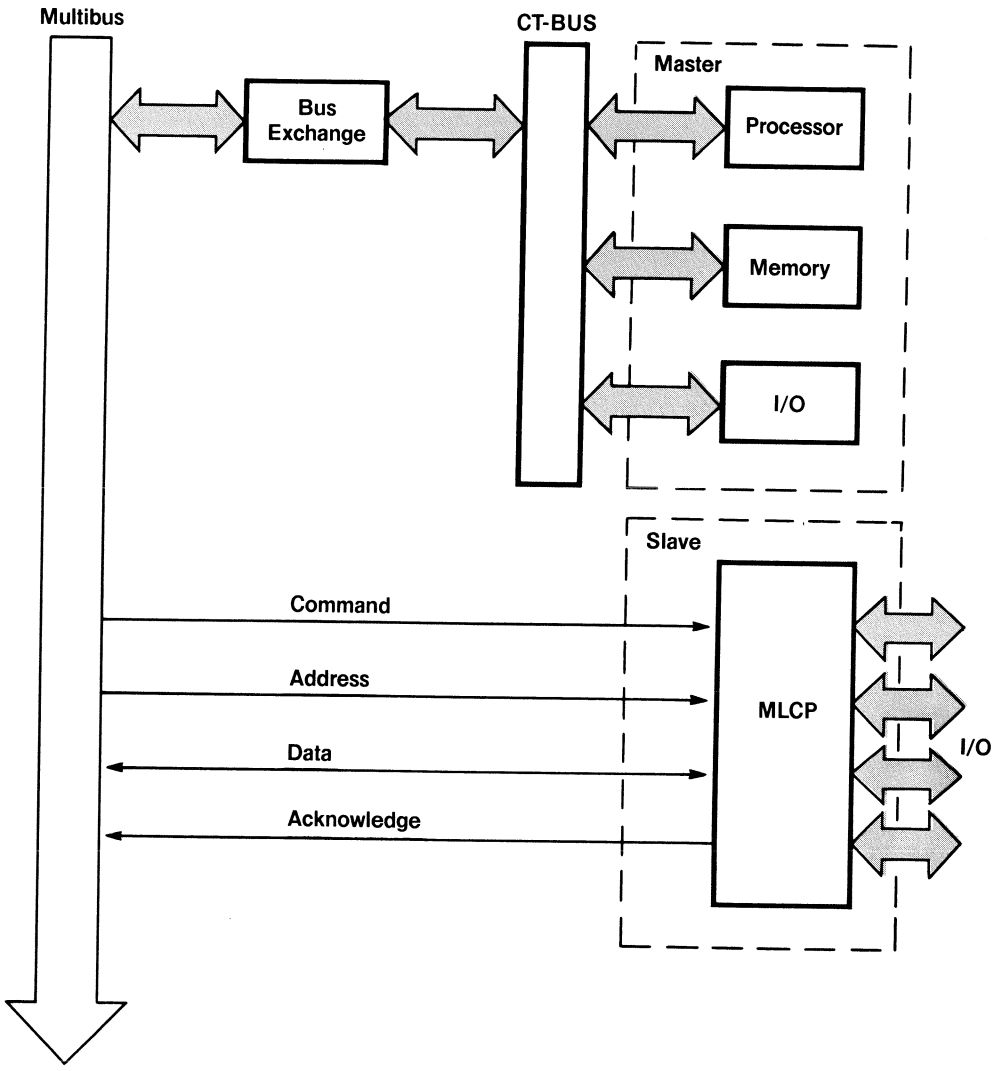


Figure 14-2. MLCP Slave Relationship.

Software Interfaces

The Multiline Communications Server, which is used by IWS-resident programs to gain access to MLCP-board-resident processes, operates in conjunction with the MLCP Executive and its associated link-level drivers to

- offload link-level communications tasks (for example, frequent interrupts, polling) from the IWS CPU
- allow more connections of peripheral devices to workstations and more connections between workstations as a result of RS-232-C port expansion

The communications server, an installed system service accessed through the request interface of the CTOS operating system, provides several CTOS operating system operations to allow convenient access from Convergent-generated communications products and customer-developed processes to the services of the MLCP. Operations to open and close paths among MLCP resident channels and processes are provided, along with the ability to read/write data.

The communications server is not a standalone software product, but must be installed along with MLCP hardware and associated software. It is capable of interfacing to and managing up to 20 communications lines per workstation. The communications server does not handle the IWS on-board communications channels.

ARCHITECTURE

Introduction

This section provides information to the programmer who writes system software for use with the MLCP board. In addition, interrupt and address settings are provided for users installing and configuring the MLCP board. The following topics are covered as subsections:

- Memory mapping: provides a physical representation of the local bus, CT-BUS, and Multibus memory maps, and how each bus is related to the others.
- Memory components: describes EPROM and RAM addresses, including applicable input/output (I/O) registers.
- Interrupts: describes local and Multibus interrupt sources.
- Switch selection: provides switch settings for Multibus interrupt levels and for mapping the MLCP board interprocessor communications window.
- Programmable board components: breaks down individual programmable components, which include the following:
  - 8085A-2 CPU
  - Device controllers (MPSC, interval timer)

Memory Mapping

Local Map

The MLCP local memory address space consists of 64K bytes and is partitioned as shown in Figure 14-3.

The first 4K bytes provide firmware for bootstrapping and self-testing the MLCP. The ROM bootstrap routine loads the MLCP software from the workstation's memory to the local RAM on the MLCP board via the Multibus. The next 4K bytes of memory on the MLCP board are mapped for I/O. The local dynamic RAM consists of the remaining 56K bytes of memory space on the board.

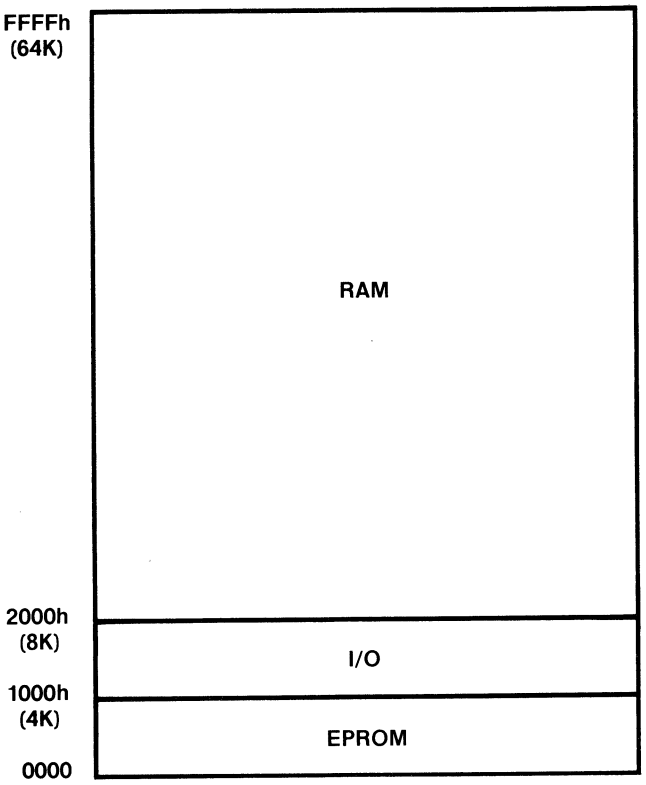


Figure 14-3. Local MLCP Memory Space.

CT-BUS and Multibus Mapping

Both the CT-BUS memory address space and the Multibus address space consist of 1M byte. A common area (window) of mutually addressable space is created on the CT-BUS to allow the Multibus to be accessed. Within this window, each MLCP board uses a 64K-byte space as shown in Figure 14-4.

Bus Interfaces

The MLCP board, which acts as an 8-bit Multibus memory slave, has a maximum of 64K bytes of shared local memory. This memory is accessible via one of two addressing schemes given below.

Scheme 1: Workstation Memory up to 512K Bytes. If the IWS workstation contains up to 512K bytes of memory and the CPU board has switches set for no ROM expansion, a 0 to 480K Multibus window translates to a local CT address range of 512K to

992K. One of eight 64K-byte Multibus address segments can be selected via switch settings on the MLCP board. (Refer to "Switch Selection," below.)

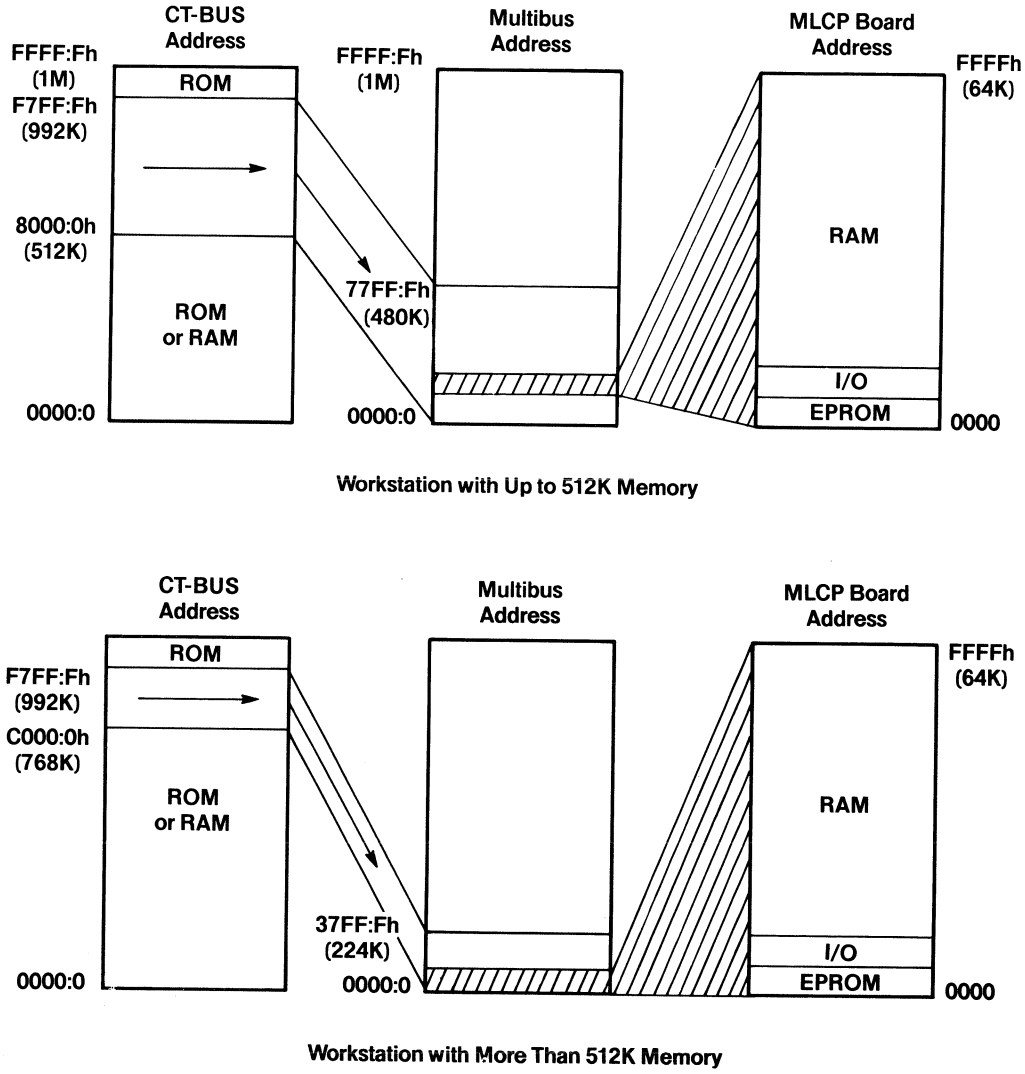


Figure 14-4. MLCP Board Address Mapping.

Scheme 2: Workstation Memory Greater Than 512K Bytes. If the IWS workstation contains more than 512K bytes of memory and the CPU board has switches set for no ROM expansion, a 0 to 224K Multibus window translates to a local CT address range of 768K to 992K. One of eight 64K-byte Multibus address segments can be selected via switch settings on the MLCP board. (Refer to "Switch Selection," below.)

The workstation mainframe can also access the local ROM and memory-mapped I/O on the MLCP board for diagnostic purposes.

Memory Components

Erasable Programmable Read-Only Memory

One 32K-byte 2732 EPROM (4K by 8 bits) contains firmware at addresses 0000h to 0FFFh that bootstraps and self-tests the MLCP. Code executes out of the 8085A-2 at 5 MHz. The IWS 8086 CPU may read from the local EPROM; however, access time depends upon the time it takes to acquire the Multibus. The EPROM is byte readable.

I/O Memory

The second 4K of memory space (1000h to 1FFFh) is memory mapped for local I/O. The port addresses are provided in Table 14-1.

The Control, Line Status, and Secondary Data registers are described below.

Control Register. The Control register (address 1010h) contains positive-true enable bits for Multibus interrupt and external baud-rate clock generation. Bit functions of the Control register port, which is both readable and writable, are as follows:

Control Bit	Function
0	Channel 1 external baud rate
1	Channel 2 external baud rate
2	Channel 3 external baud rate
3	Channel 4 external baud rate
4	Multibus interrupt
5	Unused
6	Unused
7	Unused

During a power-up reset, all the above bits are reset to zero.

Table 14-1. Local I/O Memory Allocation.

Address	Port	Access
1000	MPSC 1 channel A data (line 1)	R/W
1001	MPSC 1 channel A control (line 1)	R/W
1002	MPSC 1 channel B data (line 2)	R/W
1003	MPSC 1 channel B control (line 2)	R/W
1004	MPSC 2 channel A data (line 3)	R/W
1005	MPSC 2 channel A control (line 3)	R/W
1006	MPSC 2 channel B data (line 4)	R/W
1007	MPSC 2 channel B control (line 4)	R/W
1008	Timer 1 channel 1 baud rate (line 1)	R/W
1009	Timer 1 channel 2 baud rate (line 2)	R/W
100A	Timer 1 channel 3 software timer 1	R/W
100B	Timer 1 Mode register	W
100C	Timer 2 channel 1 baud rate (line 3)	R/W
100D	Timer 2 channel 2 baud rate (line 4)	R/W
100E	Timer 2 channel 3 software timer 2	R/W
100F	Timer 2 Mode register	W
1010	Control register	R/W
1014	Line Status register	R
1018	Secondary Data register	R/W

Line Status Register. The Line Status register (address 1014h) is a readable port that is used to read the positive-true status of the DSR (Data Set Ready) lines and the RI (Ring Indicator) lines for all four channels. Bit functions of the Line Status register are as follows:

Control Bit	Function
0	Channel 1 DSR
1	Channel 1 RI
2	Channel 2 DSR
3	Channel 2 RI
4	Channel 3 DSR
5	Channel 3 RI
6	Channel 4 DSR
7	Channel 4 RI

Secondary Data Register. The Secondary Data register (address 1018h), which is readable and writable, controls the state of the low-speed Secondary Transmit Data lines and reads the state of the low-speed Secondary Receive data lines. Positive-true bit functions of the Secondary Data register are as follows:

Control Bit	Function	R/W
0	Channel 1 secondary receive data	R
1	Channel 2 secondary receive data	R
2	Channel 3 secondary receive data	R
3	Channel 4 secondary receive data	R
4	Channel 1 secondary transmit data	W
5	Channel 2 secondary transmit data	W
6	Channel 3 secondary transmit data	W
7	Channel 4 secondary transmit data	W

During a power-up reset, all of the above transmit data bits reset to zero.

Random Access Memory

Eight 200-nsec 64K-bit dynamic RAMs (2000h to FFFFh) provide the MLCP 8085A-2 CPU with the capability of passing command and status information between the IWS 8086 CPU and the MLCP 8085A-2 CPU. An 8202A-1 dynamic RAM controller controls the RAM. If no refresh cycle is pending, two or three wait states are inserted per machine cycle. No parity error detection is provided.

Interrupts

Local

The following local maskable interrupt sources are provided on the MLCP board:

Interrupt	Address	Source	Edge/Level
RST7.5	3Ch	Multibus	Edge
RST6.5	34h	S/W timer 1	Level
RST5.5	2Ch	S/W timer 2	Level
INTR	Vector	MPSC 1 or 2	Level

The IWS mainframe can interrupt the MLCP via the Multibus at RST7.5 by writing to local RAM location FFFEh. This interrupt is edge triggered and therefore does not have to be cleared.

Channel 2 of both software timers (1 and 2) are programmable as level software interrupts at RST6.5 and RST5.5.

Both MPSCs (1 and 2) use daisy-chained priority interrupt schemes that generate vectored 8080-type level interrupts.

A nonmaskable interrupt (TRAP), located at address 24h, is not used on the MLCP board.

Multibus

The MLCP board can interrupt the CT mainframe when the Multibus interrupt bit in the Control register (port 1010h) is set. This switch-selectable Multibus interrupt can be set to four levels: 0, 2, 5, or 6. (Refer to "Switch Selection," below.)

This interrupt clears during a Multibus write to local RAM location FFFFh.

Switch Selection

One 8-bit DIP switch resident on the MLCP board selects Multibus interrupt levels and Multibus slave segment address ranges as shown in Tables 14-2 and 14-3.

Programmable Board Components

Central Processing Unit

The eight-bit 8085A-2 CPU performs the necessary control functions of the MLCP board. Features of the 8085A-2 include the following:

- 0.8 microsecond instruction cycle
- on-chip clock generator (with external crystal oscillator
- on-chip system controller (advanced cycle status information)
- three vectored interrupt inputs
- serial input/output port
- direct addressing capability to 64K bytes of memory

Device Controllers

Programmable Multi-Protocol Serial Controller. Two programmable 7201 dual-channel full-duplex MPSCs are provided for use with peripheral I/O devices. The MPSCs accept characters from the local 8085A-2 CPU in parallel format and convert

them into a continuous serial data stream for transmission. Simultaneously, the MPSCs can receive serial data streams and convert them into parallel data characters for the 8085A-2 CPU.

Table 14-2. Multibus Interrupt Level Selection.

Interrupt Level	SW1 5	6	7	8
0	ON	OFF	OFF	OFF
2	OFF	ON	OFF	OFF
5	OFF	OFF	ON	OFF
6	OFF	OFF	OFF	ON

Table 14-3. Multibus/CT Address Segment Selection.

SW1* 2	3	4	CT Segment (K)	Usable Segment (K)	Multibus Segment (K)
OFF	ON	ON	896-959	64	384-447
ON	OFF	ON	832-895	64	320-383
OFF	OFF	ON	768-831	64	256-319
ON	ON	OFF	704-767	64	192-255
OFF	ON	OFF	640-703	64	128-191
ON	OFF	OFF	576-639	64	64-127
OFF	OFF	OFF	512-575	64	00-63

*Assumes that the switch setting on the CPU board maps the Multibus memory addresses from 512K to 1023K onto the CT window of 0 to 511K.

The complete functional definition of the MPSCs is programmed by the systems software. The MPSCs can operate in polled or interrupt mode, depending upon the application. If the interrupt mode is used, 8080-type vectored interrupts should be used to provide fast interrupt service.

The two MPSCs provide a total of four RS-232-C communications ports. Each port is accessed through a 25-pin D-type connector. All four ports operate as data terminal equipment (DTE) for direct connection to a modem and support the following signals:

- TXD (Transmit Data)
- RXD (Receive Data)
- RTS (Request to Send)
- CTS (Clear to Send)
- DCD (Data Carrier Detect)
- TXC (Transmit Clock)
- RXC (Receive Clock)
- DTR (Data Terminal Ready)
- ETC (External Transmit Clock)

The following signals are also accessible through other registers:

- RI (Ring Indicator)
- DSR (Data Set Ready)
- STD (Secondary Transmit Data)
- SRD (Secondary Receive Data)

Each of the four RS-232-C communications ports can be programmed using ports 1000h through 1007h. (Refer back to Table 14-1.)

The Data registers (ports 1000h, 1002h, 1004h, and 1006h) can be either read from or written to when the RS-232-C port is receiving or transmitting data as follows:

Register A Bit (CPU)	Read Information
0 through 7	Receive data bits 0 through 7

Register A Bit (CPU)	Write Information
0 through 7	Transmit data bits 0 through 7

Each MPSC Control register (ports 1001h, 1003h, 1005h, and 1007h) contains a set of three Status (read) registers and eight Command (write) registers. They are all accessed via the command ports. (Refer back to Table 14-1.)

An internal Pointer register selects which read or write register is accessed for the appropriate channel. The register hierarchy is shown in Figure 14-5.

Summaries of asynchronous, byte-synchronous, and bit-synchronous mode register setups are provided below. For a detailed description of the NEC 7201 (or Intel 8274), refer to the 1981 Catalog published by NEC Microcomputers, Inc., or the Component Data Catalog published by Intel Corp.

For asynchronous operations, the data bits are set up as follows:

WRITE REGISTER 3

Data Bit	Setup
0	Receive enable
1 - 4	0
5	Auto enables
6, 7	Receive character length (see below)

Receive Character Length

7	6	Receive Bits Per Character
0	0	5
0	1	7
1	0	6
1	1	8

WRITE REGISTER 4

Data Bit	Setup
0	Parity enable
1	Even (1)/odd (0) parity
2, 3	Stop bits (see below)
4, 5	0
6, 7	Clock rate (see below)

Stop Bits

3	2	Stop Bits
0	0	Enable sync modes
0	1	1
1	0	1.5
1	1	2

Clock Rate

7	6	Rate
0	0	X1
0	1	X16
1	0	X32
1	1	X64

WRITE REGISTER 5

Data Bit	Setup
0	0
1	Request to Send
2	0
3	Transmit enable
4	Send break
5, 6	Transmit character length (see below)
7	Data Terminal Ready

Transmit Character Length

6	5	Transmit Bits Per Character
0	0	5
0	1	7
1	0	6
1	1	8

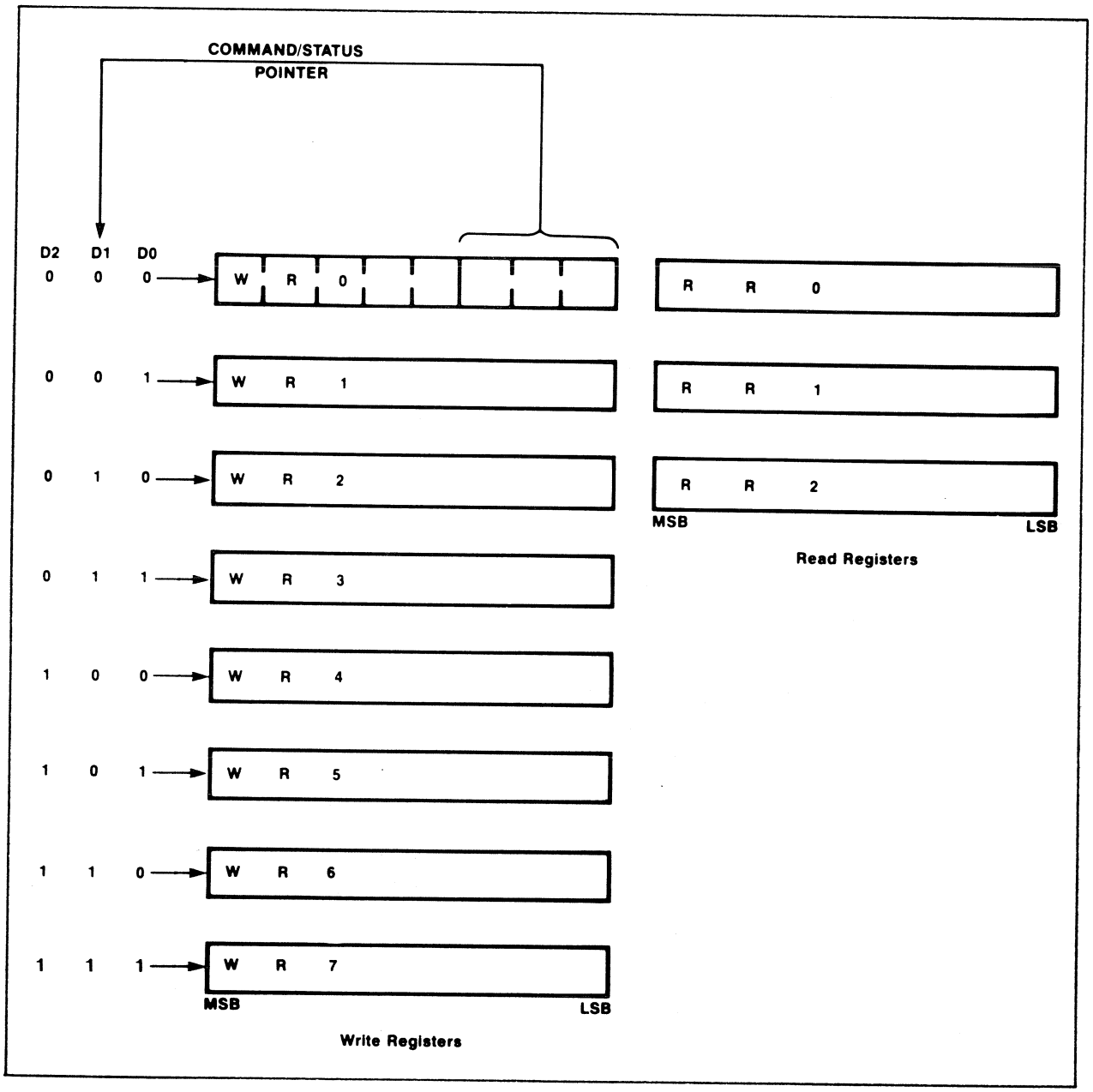


Figure 14-5. MPSC Hierarchy (Each Channel).

For byte-synchronous operations, the data bits are set up as follows:

WRITE REGISTER 3

Data Bit	Setup
0	Receive enable
1	Sync character load inhibit
2	0
3	Receive CRC enable
4	Enter hunt mode
5	Auto enables
6, 7	Receive character length (see below)

Receive Character Length

7	6	Receive Bits Per Character
0	0	5
0	1	7
1	0	6
1	1	8

WRITE REGISTER 4

Data Bit	Setup
0	Parity enable
1	Even (1)/odd (0) parity
2, 3	0
4, 5	Synchronous mode (see below)

Synchronous Mode

5	4	Sync
0	0	8 bit
0	1	16 bit
1	1	Ext

WRITE REGISTER 5

Data Bit	Setup
0	Transmit CRC enable
1	Request to Send
2	1 (CRC-16)
3	Transmit enable
4	Send break
5, 6	Transmit character length (see below)
7	Data Terminal Ready

Transmit Character Length

6	5	Transmit Bits Per Character
0	0	5
0	1	7
1	0	6
1	1	8

For bit-synchronous operations, the data bits are set up as follows:

WRITE REGISTER 3

Data Bit	Setup
0	Receive enable
1	0
2	Address search mode
3	Receive CRC enable
4	Enter hunt mode
5	Auto enables
6, 7	Receive character length (see below)

Receive Character Length

7	6	Receive Bits Per Character
0	0	5
0	1	7
1	0	6
1	1	8

WRITE REGISTER 4

Data Bit	Setup
0 - 3	0
4, 5	SDLC/HDLC mode (see below)
6, 7	0

SDLC/HDLC Mode

5	4	Mode
1	0	SDLC/HDLC

WRITE REGISTER 5

Data Bit	Setup
0	Transmit CRC enable
1	Request to Send
2	0 = SDLC/HDLC CRC
3	Transmit enable
4	0
5, 6	Transmit character length (see below)
7	Data Terminal Ready

Transmit Character Length

6	5	Transmit Bits Per Character
0	0	5
0	1	7
1	0	6
1	1	8

Programmable Interval Timer. The transmit and receive clocks for a channel can be generated locally (internal), as with asynchronous modems, or externally, as with synchronous modems. Selection of internal or external baud-rate clocks is software-programmable via a local I/O port (1010h) designated as the Control register. (Refer to "Control Register," above.)

Two 8253 programmable interval timers generate local internal baud-rate and interrupt clocks. Each counter can be programmed by writing the following three bytes of information into the internal Control Word register of the timer:

- mode control word
- low-order byte of the divisor
- high-order byte of the divisor

The mode control word is written to each channel when the CPU writes to port 100Bh (timer 1) or 100Fh (timer 2). Control definition is as follows:

Data Bit	Write Information
0	If 1, the counter counts in BCD; if 0, the counter operates as a binary counter
1 - 3	Mode (see below)
4, 5	Read/Load (see below)
6, 7	Select counter (see below)

Mode

3	2	1	Mode Selected
0	0	0	0 (interrupt on terminal count)
0	0	1	1 (programmable one-shot)
X	1	0	2 (rate generator)
X	1	1	3 (square-wave rate generator)
1	0	0	4 (software-triggered strobe)
1	0	1	5 (hardware-triggered strobe)

Read/Load

5	4	Function
0	0	Counter latching operation
0	1	Read/Load most significant byte
1	0	Read/Load least significant byte
1	1	Read/Load least significant byte first, then most significant byte

Select Counter

7	6	Counter Selected
0	0	0
0	1	1
1	0	2
1	1	Not used

After the mode control word is written, two divisor bytes are written to each of the counters to select the counter rate. The divisor bytes work by dividing the counter input clock of 1.23 MHz by a selected number.

For example, if counter 2 of timer 1 is to interrupt the CPU in 1 millisecond, 1230 counts (04CEh) are required. The complete programming sequence for counter 2 of timer 1 would be as follows:

1. Write B0h to port 100Bh (counter 2; Read/Load least significant divisor byte, then most significant divisor byte; interrupt on terminal count; binary counter).

2. Write CEh to port 100Ah (least significant byte of divisor).

3. Write 04h to port 100Ah (most significant byte of divisor).

The procedure for setting the baud rate for the RS-232-C communications ports is the same as that for counter 2 above, except that the CPU writes the divisor to I/O ports 1008h or 1009h for lines 1 or 2 of timer 1, respectively.

Assuming a required baud rate for RS-232-C communications channel (line) 2 of 1200 baud, 1025 counts (0400h) are required. An example programming sequence for timer 1, line 2, is as follows:

1. Write 76h to port 100Bh (counter 1; read/load least significant divisor byte, then most significant divisor byte; square wave; binary counter).

2. Write 00h to port 1009h (least significant byte of divisor).

3. Write 04h to port 1009h (most significant byte of divisor).

Note that counters 0, 1, and 2 can each be read independently by a CPU input instruction at any time without inhibiting the counter inputs.

Refer back to Table 14-1 for the appropriate I/O ports.

THEORY OF OPERATION

Introduction

This section, which is directed to the engineer who must understand the MLCP board at the component level, provides a detailed component-level description of the hardware incorporated on the MLCP board. Each functional block shown in Figure 14-6, the MLCP block diagram, is described in relation to the logic that performs the function. In addition, the schematic drawings (Figure 14-7) are provided to supplement the text.

Circuit Description

A detailed component-level circuit description is given for each of the following functional logic units:

- Clock-generator logic
  - System clock
  - Processor clock
  - Dynamic RAM controller clock
  - Communications clock
- Central processing unit logic
  - 8085A-2 CPU logic
  - Initialization logic
  - Ready logic
  - Interrupt logic
- Bus interface logic
  - Local address bus
  - Local data bus
  - Multibus address/data bus

- Memory logic
  - Dynamic RAM and RAM control
  - EPROM
- Device control logic
  - I/O decoder
  - Programmable MPSC
  - Programmable interval timer

Clock-Generator Logic

System Clock

A 19.6608-MHz crystal oscillator (Y1) provides the MLCP board with the MEMCLK+ (Memory Clock) pulses (Figure 14-7, page 3).

Processor Clock

The crystal frequency divides by two at D flip-flop 13D (Figure 14-7, page 2) to provide the 8085A-2 (14D) with a 9.83-MHz clock at X1 and X2 (pins 1 and 2). Two 470-ohm resistors (R1 and R2) are provided as pullup resistors. The 8085A-2 divides the clock internally to produce a processor clock of 5 MHz (pin 37). The processor clock is driven through 2E (pin 3) and inverter 19F (pin 4) to generate both phases of the clock, PCLK+ and PCLK-, respectively.

Dynamic RAM Controller Clock

The 19.6608-MHz MEMCLK+ from crystal Y1 (pin 8) provides clock pulses to the 8202A-1 dynamic RAM controller (1B) shown in Figure 14-7, page 3. For proper operation of 1B, the external oscillator connects at X1 (pin 37), while X0 (pin 36) straps to +12 V. A 1-kilohm resistor (R3) acts as a current limiter. Flip-flops at 3D (pins 3 and 11), shown in Figure 14-7, page 4, use MEMCLK+ to synchronize the MEMR- (Memory Read) at pin 6 and MEMW- (Memory Write) at pin 8 command inputs to 1B (pins 32 and 31, respectively) to avoid possible metastable conditions inside the older 8202 non-A parts.

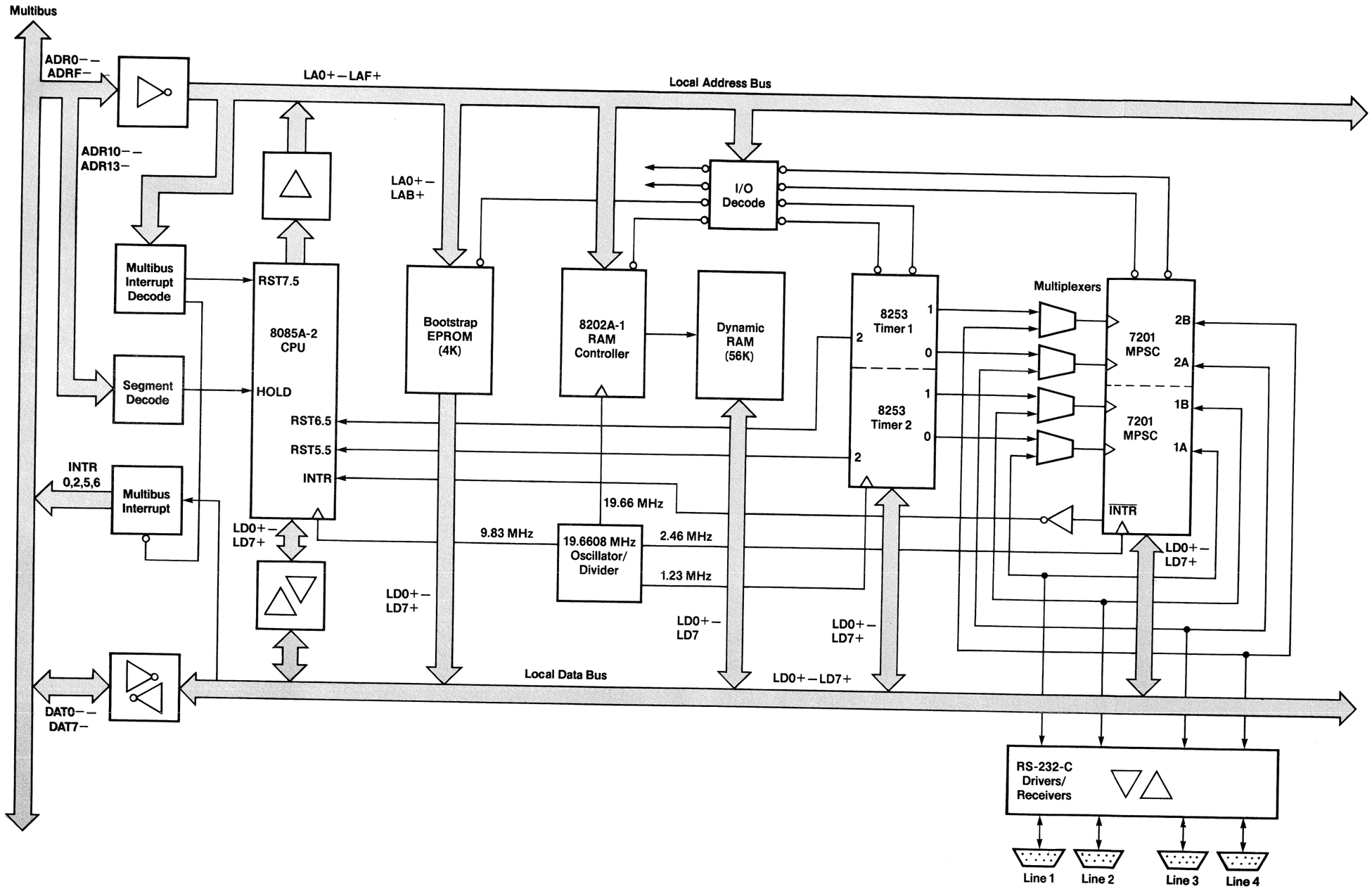


Figure 14-6. MLCP Block Diagram.

POWER AND GROUND LOCATOR CHART					
REF. DES.	TYPE	GND	+5V	+12V	-12V
1A - 8A	MB826A-20	16	8		
12A,13A,15A,16A,10B	1488	7		14	1
1B	8202A-1	20	40		
7C	2732	12	24		
10C,13C	7201	20	40		
19C,19D	8253	12	24		
4D	DELAY LINE 90 NS	1,14			
14D	8085A-2	20	40		

SPARE GATES		
TYPE	REF. DESIGNATION	QTY.
74LS175	9A	3
74LS244	17A,18A,17B,18B,20B,18C,3E	4,4,4,4,2,3
74LS32	20A,4C,18D	1,1,2
74LS08	2C,17E,19E	3,1,1
74LS74	2D	1
74LS27	9D	2
74LS14	1D	1
74S04	13E	2
74LS04	19F	2
74LS02	8D	2

REFERENCE DESIGNATORS	
LAST USED	NOT USED
C60	
RP6	
R4	
SW1	
Y1	

NOTES; UNLESS OTHERWISE SPECIFIED:
1. RESISTANCE VALUES ARE IN OHMS, 1/4W, 5%.
2. CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL DEVICES ARE STANDARD 4+8, 7+14, 8+16, 10+20 GROUND AND POWER CONNECTIONS.

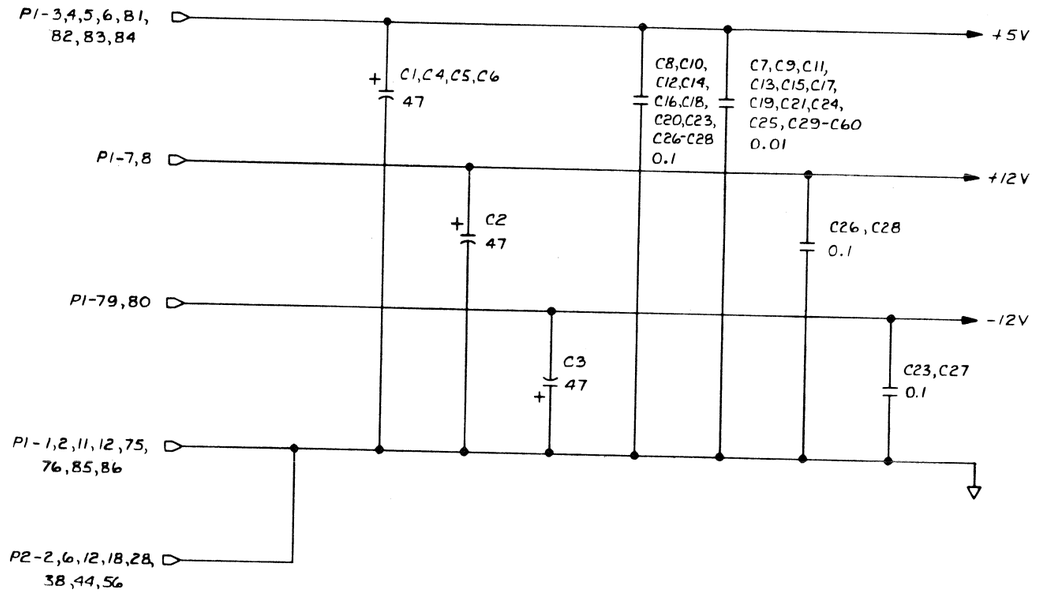


Figure 14-7. MLCP Board Schematic. (Page 1 of 8)

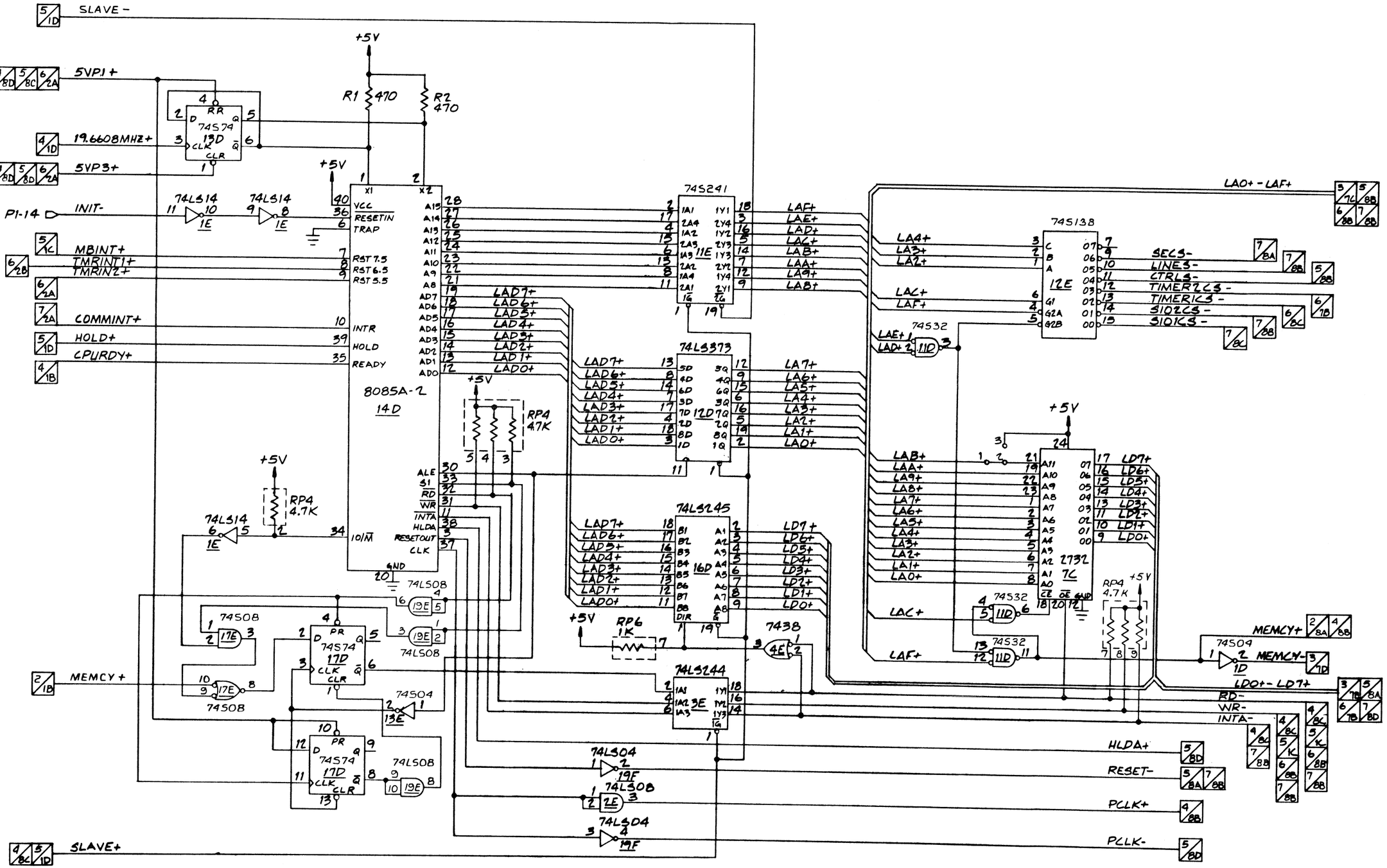


Figure 14-7. MLCP Board Schematic. (Page 2 of 8)

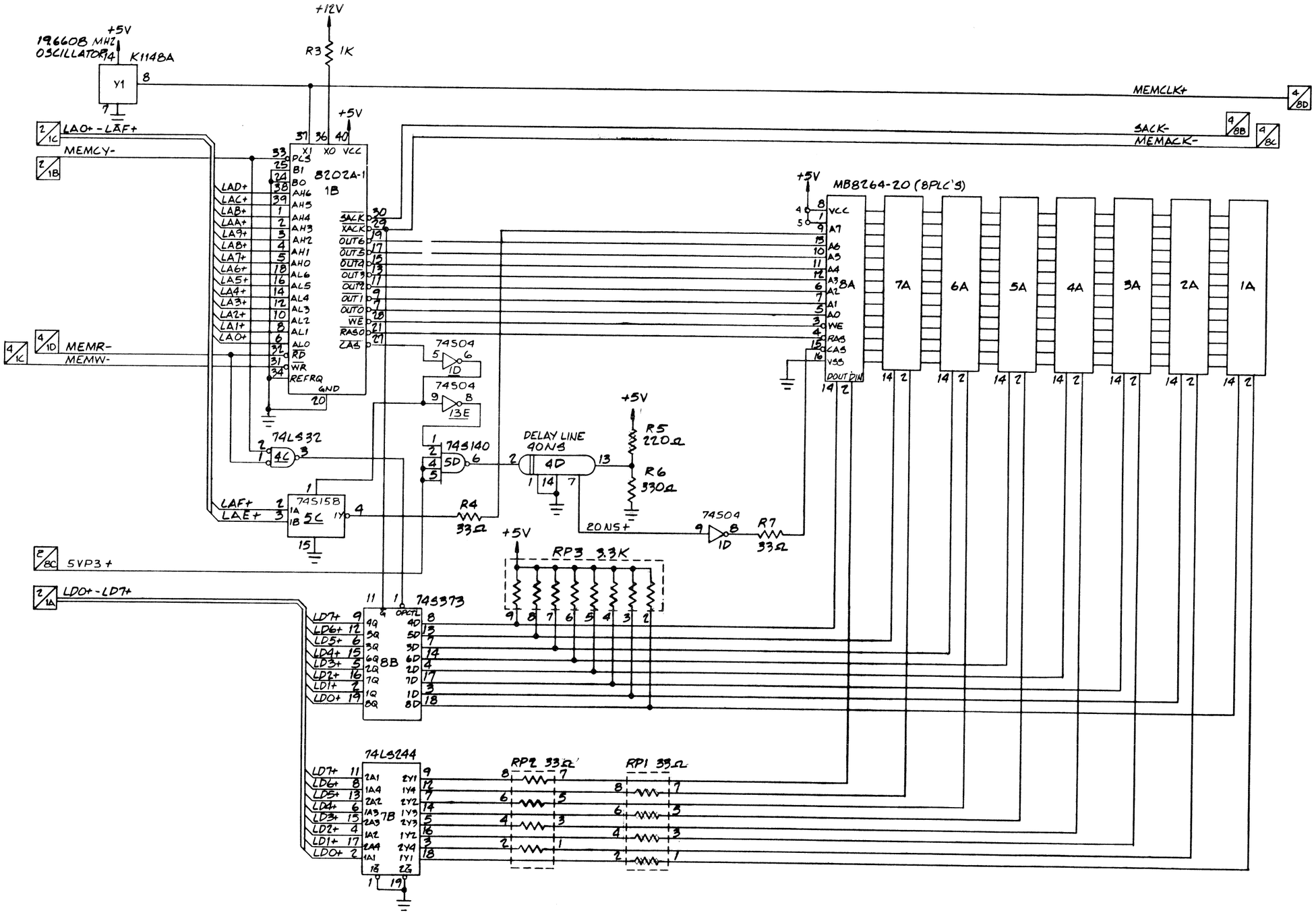


Figure 14-7. MLCP Board Schematic. (Page 3 of 8)

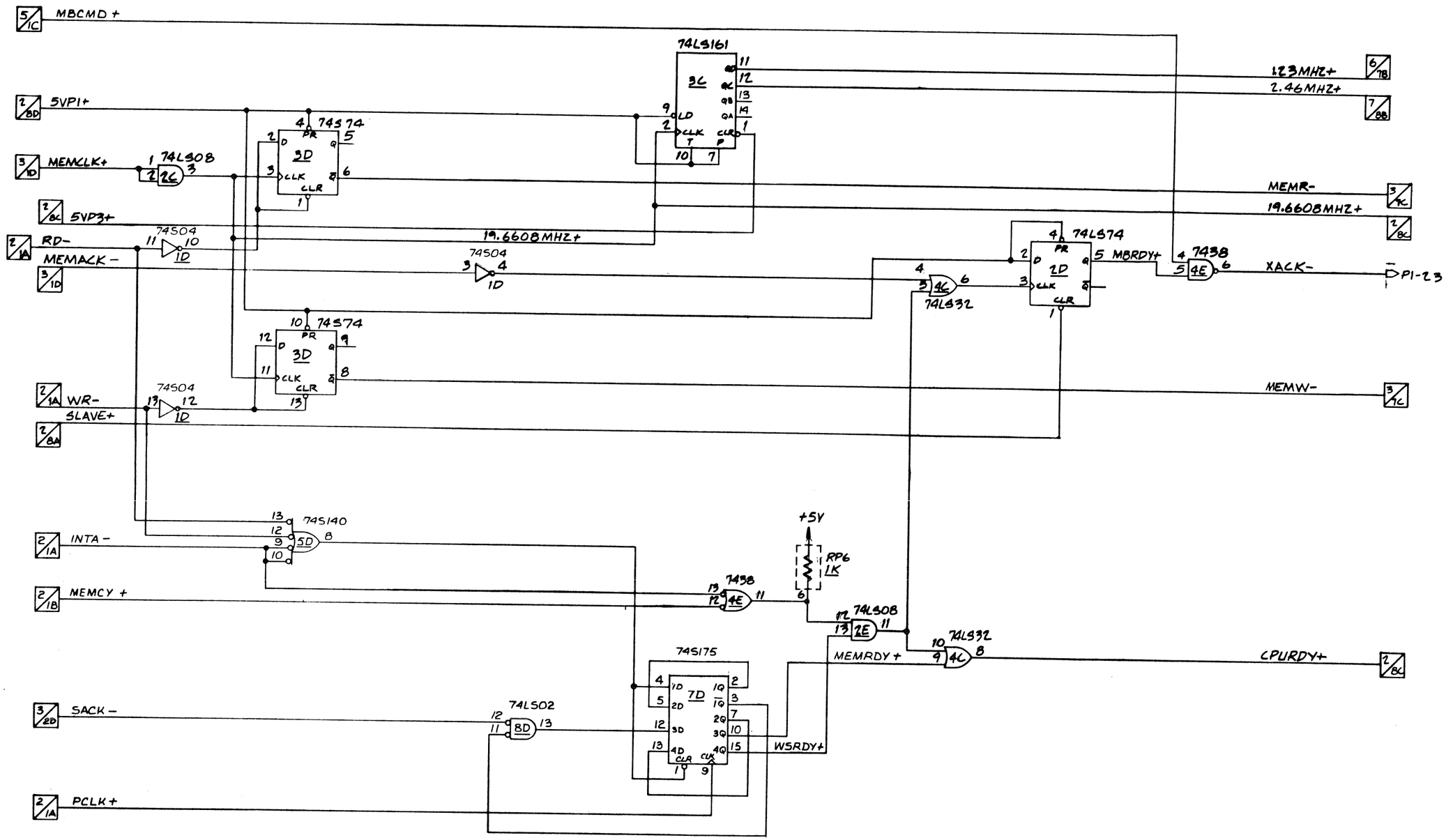


Figure 14-7. MLCP Board Schematic. (Page 4 of 8)

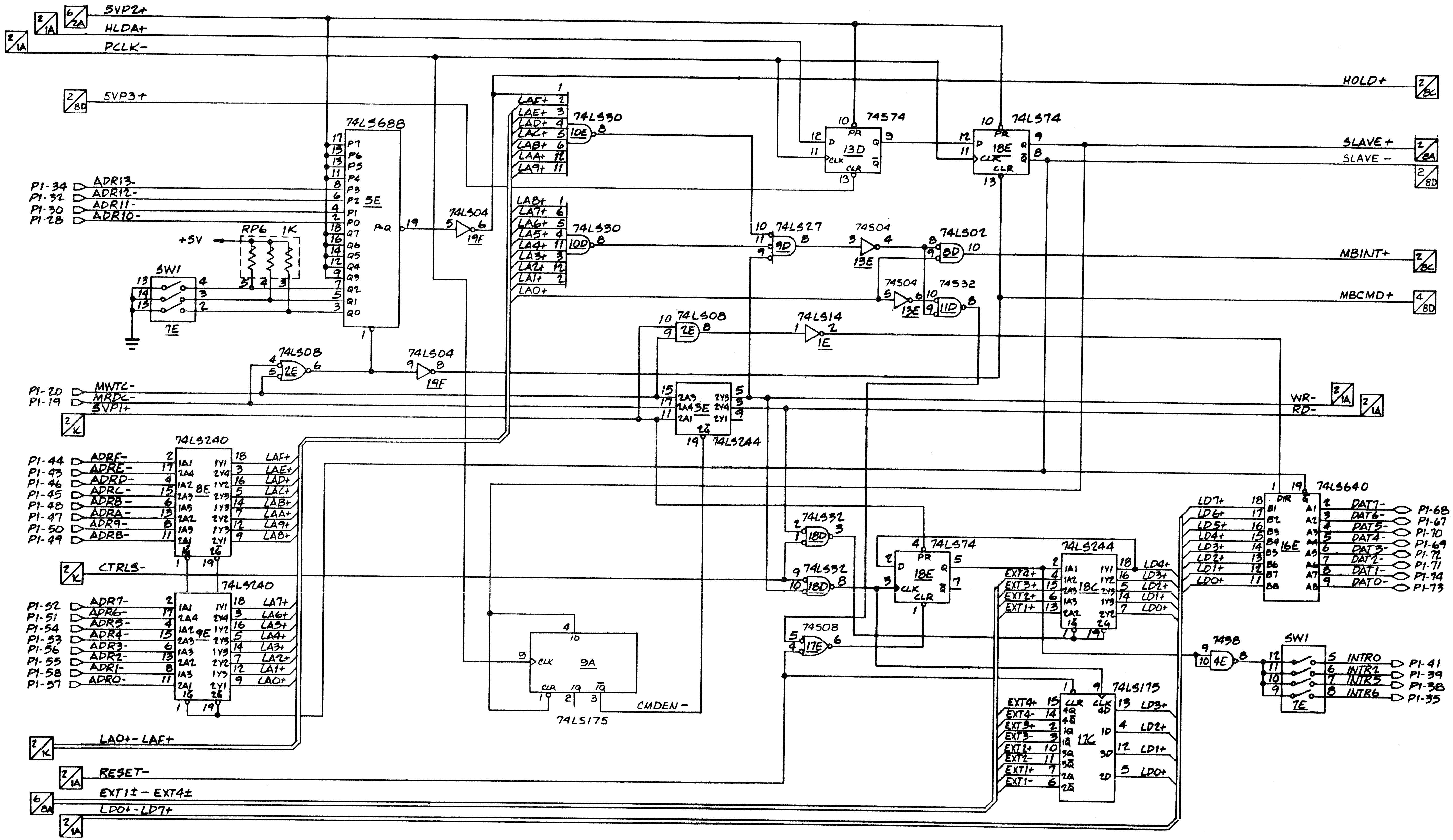


Figure 14-7. MLCP Board Schematic. (Page 5 of 8)

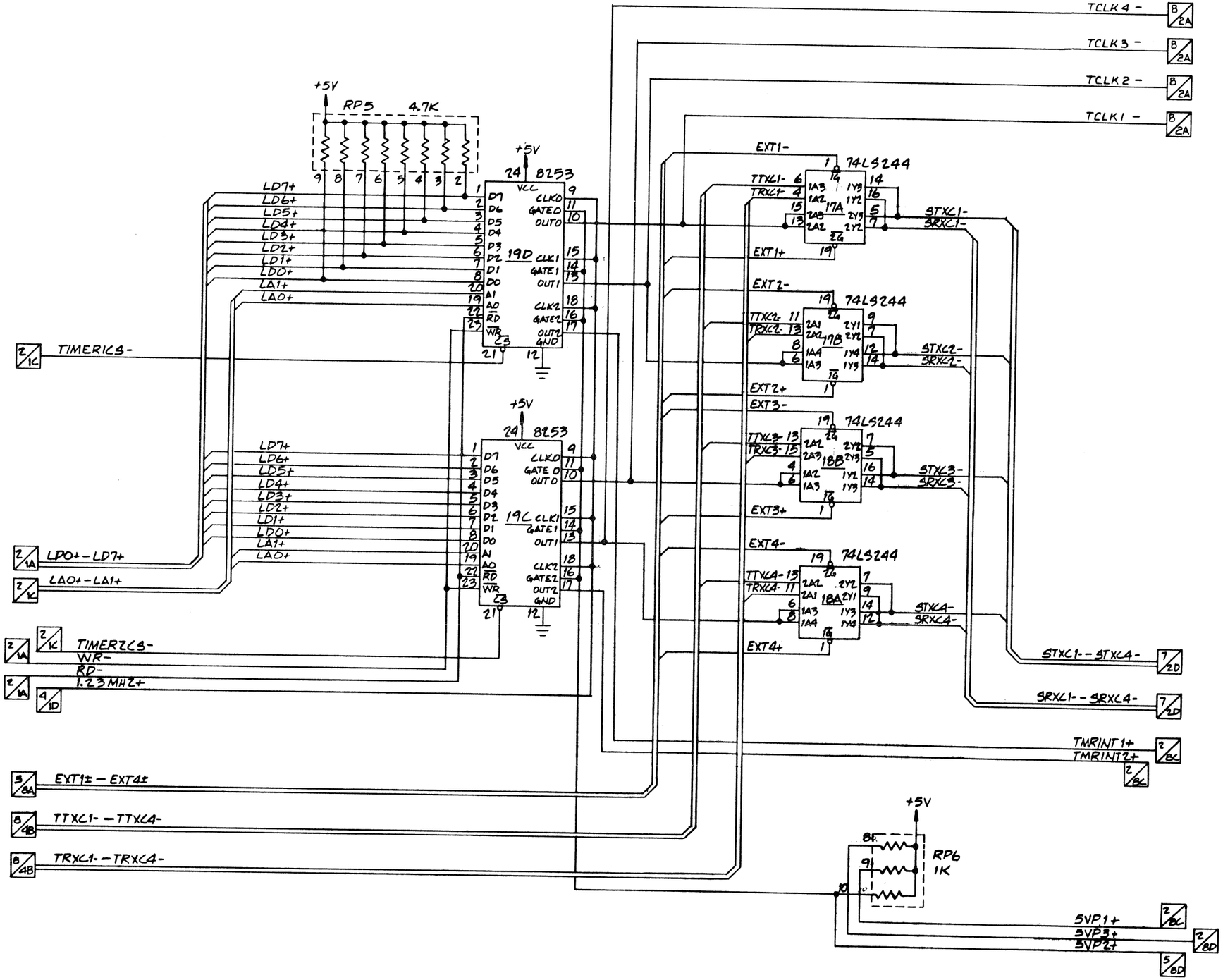


Figure 14-7. MLCP Board Schematic. (Page 6 of 8)

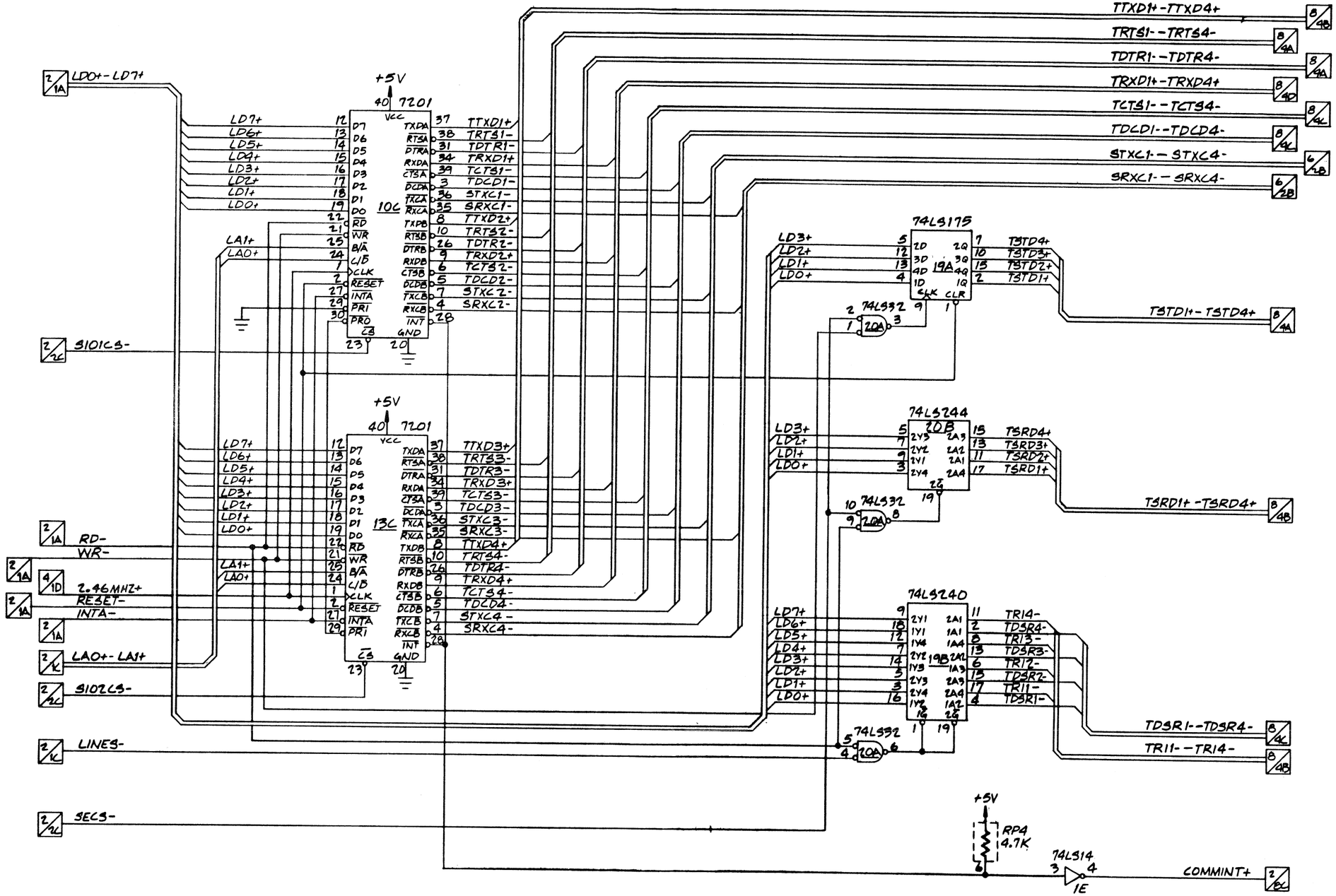


Figure 14-7. MLCP Board Schematic. (Page 7 of 8)

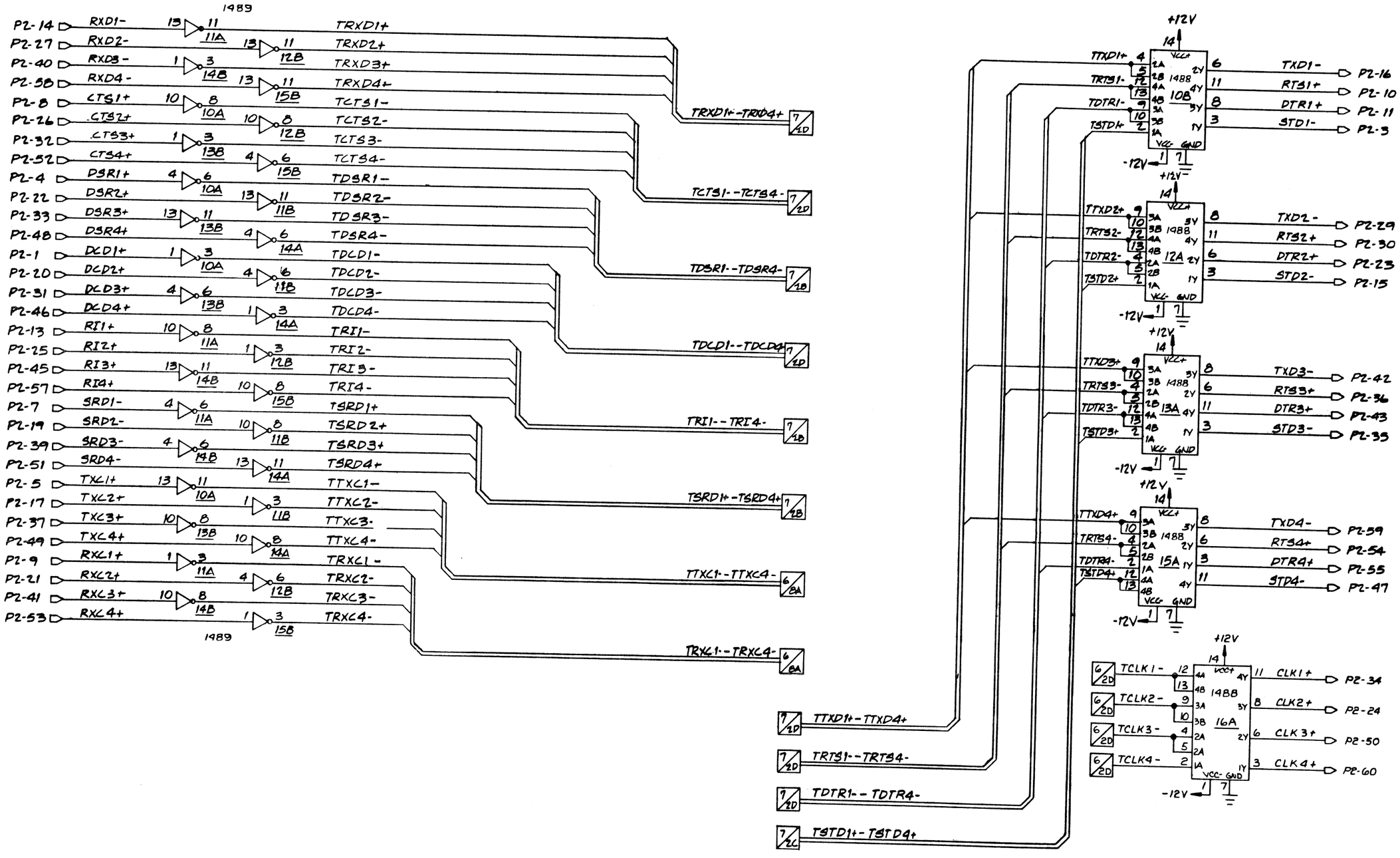


Figure 14-7. MLCP Board Schematic. (Page 8 of 8)

Communications Clock

Four-bit counter 3C (Figure 14-7, page 4) divides the 19.6608-MHz MEMCLK+ to form a 1.23-MHz clock (pin 11) and a 2.46-MHz clock (pin 12). The 1.23-MHz pulse clocks the internal clocks of the 8253 programmable interval timers (Figure 14-7, page 6), which determine the internal baud rates for the RS-232-C interfaces. The 2.46-MHz system clock controls the internal timing devices of the two 7201 MPSCs (Figure 14-7, page 7) at pin 1.

Central Processing Unit Logic

8085A-2 CPU Logic

The 8085A-2 (14D), shown in Figure 14-7, page 2, executes instructions at 5 MHz to perform control functions that would otherwise have to be administered by the IWS 8086 CPU. The pinouts and functions of 14D are provided in Table 14-4.

Initialization Logic

The MLCP board initializes when an INIT- (Initialize) signal connects from the Multibus (P1, pin 14) to the 8085A-2 (14D) RESETIN- (pin 36). Two Schmitt triggers (1E) allow connection to an RC network for power-on reset delay. The 8085A-2 produces a RESETOUT+ signal (pin 3), which is inverted at 19F (pin 2) and used as an active-low board reset.

After 14D resets, the 4K by 8 bit 2732 EPROM (7C) performs a bootstrap and self-test routine.

Ready Logic

During machine cycles, the CPURDY+ (CPU Ready) line of 14D (pin 35) can be used to extend the I/O and memory read and write pulse lengths for compatibility with slow memory or peripheral devices.

The CPURDY+ line is driven low to indicate that wait states must be added to the machine cycles; the CPURDY+ line returns to its active level when wait states are not required, signifying that the machine cycles can terminate according to the specified setup and hold times.

Table 14-4. 8085A-2 Functions. (Page 1 of 2)

Symbol	Pin	Function
A8+ - A15+	21 - 28	Address bus: most significant address lines (tristate)
AD0+ - AD7+	12 - 19	Multiplexed address/data bus: multiplexed least significant address lines/data lines (tristate)
ALE+	30	Address latch enable
S1+	33	Advanced read status (tristate)
RD-	32	Read command (tristate)
WR-	31	Write command (tristate)
INTR+	10	Interrupt request: vectored interrupt from 7201 MPSCs
INTA-	11	Interrupt acknowledge: replaces RD- during instruction cycle after INTR+ is accepted
HOLD+	39	Hold request during Multibus cycle
HLDA+	38	Hold acknowledge: indicates that HOLD+ was received and that 8085A-2 CPU will relinquish the bus
RESETIN-	36	Reset in: initializes program
RESETOUT+	3	Reset out: system reset

Table 14-4. 8085A-2 Functions. (Page 2 of 2)

Symbol	Pin	Function
CLK+	37	Processor clock
IO+/M-	34	I/O or memory control
READY+	35	When low, processor enters wait states
RST 7.5+ RST 6.5+ RST 5.5+	7 8 9	Restart interrupts
TRAP+	6	Not used; tied to ground
Vcc	40	Power
GND	20	Ground

Quad D flip-flop 7D (Figure 14-7, page 4) generates appropriate delays by acting as a shift register. When a RD- (Read), WR- (Write), or INTA- (Interrupt Acknowledge) occurs at pins 13, 12, or 9 of bubbled OR gate 5D (which acts as a NAND gate), 7D is enabled at pin 4 and generates a WSRDY+ (Wait-State Ready) signal three clocks (600 nsec) later (pin 15). This WSRDY+ signal qualifies with an I/O cycle (that is, I/O read, I/O write, interrupt acknowledge, or ROM) at 2E (pin 11) to generate the CPURDY+ signal. (Note that an I/O cycle is represented by INTA- or an inactive MEMCY+ at pin 13 or 12 of bubbled OR gate 4E, which acts as a NAND gate.)

After a RD-, WR-, or INTA- has occurred, a SACK- (System Acknowledge) signal generated from the 8202A-1 dynamic RAM controller qualifies with 1Q- stemming from 7D (pin 3) at 8D (pin 13) before delaying at 7D (pin 10) to conform to the 5-MHz clock cycle of the 8085A-2. This delayed MEMRDY+ (Memory Ready Signal) also initiates the CPURDY+ signal at OR gate 4C (pin 8).

In summary, any I/O ready or memory ready signal generates the CPURDY+ signal.

Local Interrupt Logic. The IWS mainframe interrupts the MLCP via the MBINT+ (Multibus Interrupt) at RST7.5 of the 8085A-2 (pin 7) as shown in Figure 14-7, page 2.

As shown in Figure 14-7, page 5, the MBINT+ signal originates at pin 10 of bubbled AND gate 8D, which acts as a NOR gate, when the Multibus writes to local RAM FFFEh. During this time, an inactive least significant local address line (that is, LA0-) stemming from the Multibus qualifies with LA1+ through LAF+, a WR- (Write Command) that originates from the Multibus (P1, pin 20), and a signal originating at comparator 5E (pin 19).

The WR- signal is generated from line driver 3E (pin 5) after a 200-nsec delay caused by D flip-flop 9A (pin 3). This delay allows the appropriate addresses to stabilize before the MWTC- (Memory Write Command) is output from 3E as WR-.

The signal stemming from 5E (pin 19) determines whether the address bits on the Multibus are within the local 64K window. (Refer to "Multibus Address/Data Bus," below.) This signal inverts at 19F (pin 6) to qualify with local address bits LA9+ through LAF+ at NAND gate 10E (pin 8).

The signals generated at 9D (pin 8) are inverted at 13E (pin 4) to NOR with LA0- at bubbled AND gate 8D, producing MBINT+ (Multibus Interrupt) at pin 10.

This interrupt is edge triggered and, therefore, does not have to be cleared.

Multibus Interrupt Logic. The MLCP interrupts the CT mainframe when the Multibus interrupt bit is set in the Control register at port 1010h. (Refer to "Control Register" under "Architecture," above.) As shown in Figure 14-7, page 2, 1-of-8-decoder 12E decodes address 1010h to generate a CTRLS- signal (pin 11) to the Control register. The most significant nibble (LAC+, LAD-, LAE-, and LAF-) enables 12E, and local address lines LA2-, LA3-, and LA4+ are decoded to produce CTRLS-.

As shown in Figure 14-7, page 5, data is written into Control register 17C, which clocks (pin 9) after CTRLS- qualifies with WR- at pin 8 of

bubbled NAND gate 18D (which acts as an OR gate). In addition, CTRLS- qualifies with RD- at 18D (pin 3) to enable latch 18C. Local data line 4 (LD4+), generated from 18C (pin 18), reads back from 18C to interrupt flip-flop 18E (pin 2), which generates the interrupt pulse (pin 5) driven by open-collector driver 4E (pin 8) to the applicable Multibus interrupt line (INTR0, INTR2, INTR5, or INTR6). Refer to Table 14-2 under "Architecture" for Multibus interrupt level switch positions.

Control register 17C resets (pin 1) during a RESET- (Reset) pulse from the 8085A-2 CPU. In addition, either a RESET- or a WR- to local RAM FFFFh clears the interrupt at 18E (pin 1). During a write to FFFFh, LA0+ inverts at 13E (pin 6) before qualifying with local address lines LA1+ through LAF+ and WR-, which all invert at 13E (pin 4), to generate an active-low signal out of pin 8 of bubbled NAND gate 11D (which acts as an OR gate). Bubbled NOR gate 17E ANDs the active-low signal from 11D (pin 8) with RESET- to generate an active-low pulse out of pin 6 to clear 18E (pin 1).

In summary, a low at pin 6 of 17E caused by a write to local RAM FFFFh or a RESET- clears 18E (pin 1).

Programmable MPSC Interrupt Logic. Both 7201 MPSCs shown in Figure 14-7, page 7, use daisy-chain interrupt priority schemes that generate 8-bit vectored level interrupts. Since PRI- (Priority Interrupt) of 10C (pin 29) is grounded, this MPSC has a higher priority interrupt than that of 13C.

To request an interrupt, 10C or 13C sends the INT- (Interrupt) signal (pin 28) to the 8085A-2 through line buffer 1E (pin 4), which inverts the signal to COMMINT+ (Communications Interrupt). This signal indicates that the highest priority internal interrupt requires service. A 4.7-kilohm pullup resistor (RP4) is required for the open-collector line.

The 8085A-2 responds with an INTA- (Interrupt Acknowledge), which allows the highest priority interrupt of 13C or 10C (pin 27) to generate the programmable interrupt vector.

Programmable Interval Timer Interrupt Logic. The OUT2 (counter 2 output) signals of both

programmable interval timers in Figure 14-7, page 6, are used as software interrupts. The TMRINT1+ (Timer 1 Interrupt) signal from 19D (pin 17) interrupts the 8085A-2 at RST6.5 and the TMRINT2+ (Timer 2 Interrupt) signal from 19C (pin 17) interrupts the 8085A-2 at RST5.5. Both interrupts are edge triggered and must be cleared. Refer to "Programmable Interval Timer" under "Architecture" for information pertaining to the programmable software.

Bus Interface Logic

Local Address Bus

Sixteen address lines are provided by the 8085A-2 (14D) as shown in Figure 14-7, page 2.

The high-order lines (pins 21 through 28) are buffered by 11E, which is enabled when the IWS 8086 CPU releases control of the local address lines (that is, during a SLAVE-) to generate local address lines LA8+ through LAF+.

The low-order lines of 14D (pins 12 through 19) consist of multiplexed addresses and data (LAD0+ through LAD7+). At the beginning of a new machine cycle, indicated by active ALE+ (Address Latch Enable) at pin 30, LAD0+ through LAD7+ stabilize as the low-order address lines. At the trailing edge of ALE+ (that is, when ALE+ becomes inactive), caused by a local read or write cycle, D flip-flop 12D latches the address lines to generate local address lines LA0+ through LA7+ during an inactive SLAVE+ (that is, when the IWS 8086 CPU has no control of the local address bus).

Local Data Bus

As shown in Figure 14-7, page 2, the LAD0+ through LAD7+ local address/data lines are buffered by transceiver 16D, which generates the local bidirectional data lines LD0+ through LD7+.

Transceiver 16D is enabled at pin 19 when SLAVE+ becomes inactive, indicating a local read or write cycle. The direction of data is determined by a RD- (Read) or INTA- (Interrupt Acknowledge) signal, which NANDs at bubbled OR gate 4E (pins 1 and 12) to control 16D (pin 1). When a RD- or INTA- signal becomes active, 16D directs the data

toward the 8085A-2 (that is, from the LD+ bus to the LAD+ bus). Otherwise, 1-kilohm pullup resistor RP6 directs the data from LAD+ to LD+.

Multibus Address/Data Bus

A Multibus read or write cycle, from or to local memory, starts when the IWS 8086 CPU addresses the MLCP board as shown in Figure 14-7, page 5. Eight-bit comparator 5E compares the incoming addresses on the four most significant address lines ADR10- through ADR13- with the three switch settings of DIP SW1 7E.

The SW1 switch settings encode a single 64K-byte address segment out of the 1M-byte Multibus address space available. (Refer to Table 14-3 under "Architecture" for appropriate address switch settings.) The output of 5E (pin 19) becomes active low when Multibus addresses ADR10- through ADR13- match the switch settings input at Q0, Q1, and Q2 (pins 3, 5, and 7) and either a MRDC- (Memory Read Command) or a MWTC- (Memory Write Command) is sent via the Multibus (P1, pins 20 or 19, respectively) through gate 2E (pin 6) to 5E (pin 1).

Inverter 19F (pin 6) inverts the active-low signal output from 5E (pin 19) to request a HOLD+ (Hold) from the 8085A-2 (pin 39) as shown in Figure 14-7, page 2. The 8085A-2 responds by sending a HLDA+ (Hold Acknowledge) from pin 38, which is synchronized to PCLK-. The HLDA+ undergoes two synchronization stages at D flip-flops 13D (pin 12) and 18E (pin 12), as shown in Figure 14-7, page 5, to allow the local bus to finish its current bus cycle. After a positive transition of PCLK- at 18E, SLAVE+ (pin 9) and SLAVE- (pin 8) are generated to enable the address and data drivers.

The SLAVE- generated from 18E (pin 8) enables drivers 9E and 8E (pins 1 and 19), allowing the 16 least significant address bits (ADR0- through ADRF-) of the Multibus to transfer onto the local bus (LA0+ through LAF+).

In addition, SLAVE- enables driver 16E, which allows byte transfers between the Multibus and local bus. The direction of the data is determined at 16E (pin 1), depending on whether the Multibus carries an MRDC- or MWTC-.

To allow the address lines to stabilize before the MRDC- or MWTC- releases at 3E (pins 3 or 5, respectively) as a RD- or WR-, SLAVE+, which is generated from 18E (pin 9), loads into D flip-flop 9A (pin 4), which acts as a 200-nsec delay before generating a CMDEN- (Command Enable) at pin 3 to enable driver 3E.

Memory Logic

Dynamic RAM and RAM Control

Dynamic RAM. The dynamic RAM array (1A through 8A) shown in Figure 14-7, page 3, consists of 64K words by 8 bits (64K bytes). Power (+5 Vcc) feeds into the RAM array at pin 8. In addition, pin 1, which is a no-connect, straps to +5 V to allow for future system upgrade. The CAS- (Column Address Strobe) signal line (pin 15) and all DIN (Data-In) lines (pin 2) to the array are in series with 33-ohm terminator resistors (RP7, RP1, and RP2) to avoid transmission line reflection and prevent double clocks. The DOUT (Data-Out) lines (pin 14) are pulled up to +5 V by 3.3-kilohm resistors (RP3).

Dynamic RAM Controller. As shown in Figure 14-7, page 3, the 8202A-1 Dynamic RAM Controller (1B) enables at the PCS- (Protected Chip Select) when MEMCY- (Memory Cycle), represented by 2000h through FFFFh, asserts at pin 33. During MEMCY-, the 8085A-2 sends a RD- or WR- command, which inverts at pin 10 or 12 of inverter 1D (Figure 14-7, page 4) before synchronizing to MEMCLK+ (Memory Clock) at D flip-flop 3D (pin 2 or 12). As shown by the timing diagrams in Figures 14-8 and 14-9, a 68-nsec delay (maximum) occurs before the RD- or WR- outputs at pin 6 or 8 as MEMR- (Memory Read) or MEMW- (Memory Write) to avoid possible metastable states inside the older 8202 non-A parts.

As shown in Figure 14-7, page 3, MEMR- or MEMW- inputs at the RD- (Memory Read Request) or WR- (Memory Write Request) of 1B (pin 32 or 31).

Fourteen bits of local addresses (LA0+ through LAD+) drive 16K addresses A0 through A6 of 8A through 1A. The two most significant address lines (LAE+ and LAF+) are multiplexed and inverted at 2-line-to-1-line multiplexer 5C (pin 4) to add an eighth line to drive 64K RAM. The

eighth line (A7), which is controlled by CAS- (Column Address Strobe) at pin 27, requires 33-ohm terminator resistor R4 to dampen line reflection. The strobe of 5C (pin 15) is tied to ground.

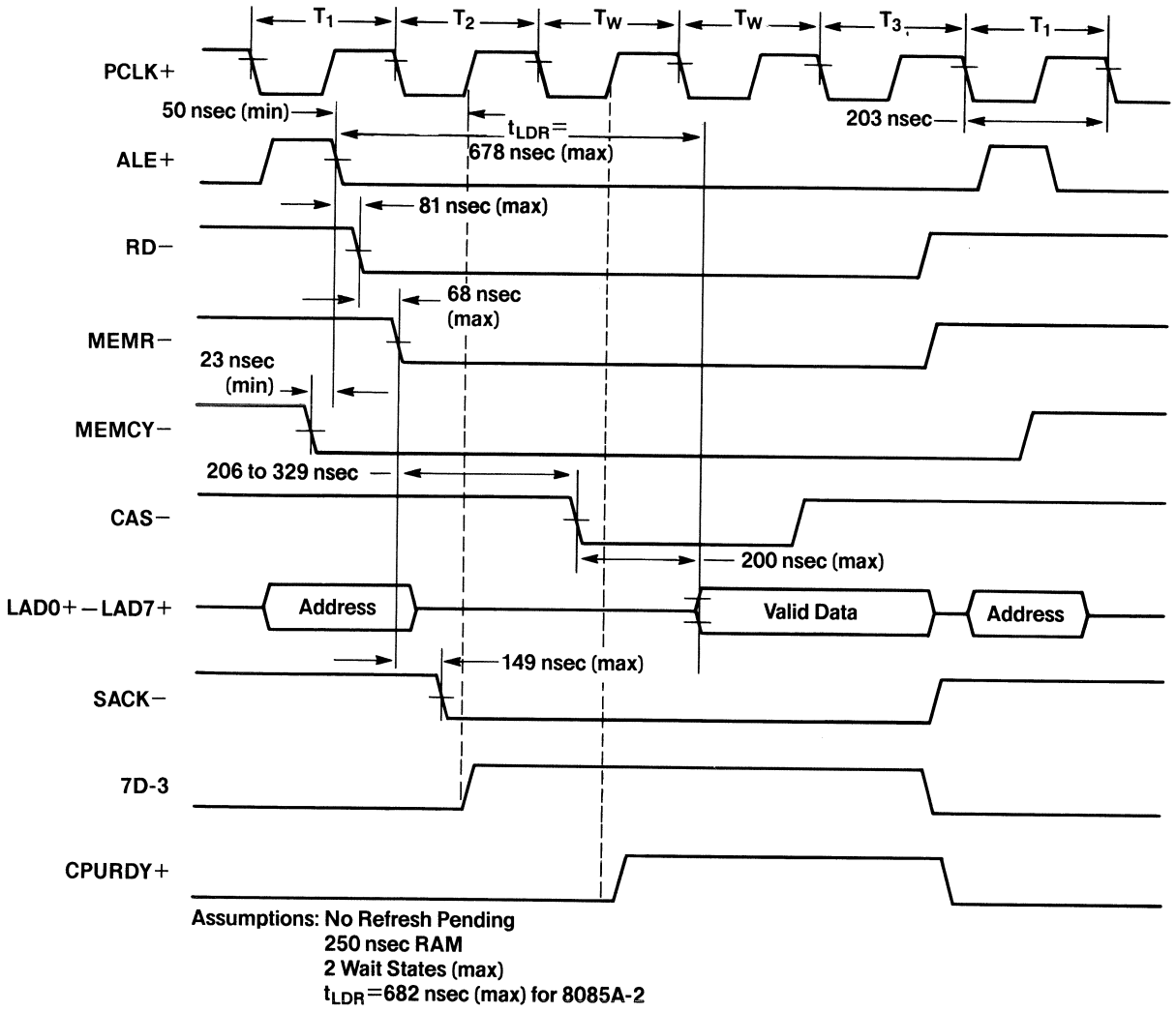


Figure 14-8. Multiline Controller RAM Read Cycle.

Since only one row of addresses is used by RAS0- (Row Address Strobe) at pin 21, B0+ and B1+ (Bank Selects) are tied to ground. After RAS0- latches the row address into the RAM array (pin 4), the CAS- drives through passive delay line 4D (pin 7) via inverter 1D (pin 6), inverter 13E (pin 8), and NAND gate 5D (pin 6) to latch the column addresses into the RAM.

Dynamic RAM refresh occurs within 1B and, therefore, is transparent to the 8085A-2. During a refresh cycle, the refresh row address is driven onto the dynamic RAM address lines and RAS- pulses, refreshing the bank. After each refresh cycle, the internal refresh row address counter increments and 1B reloads the refresh timer.

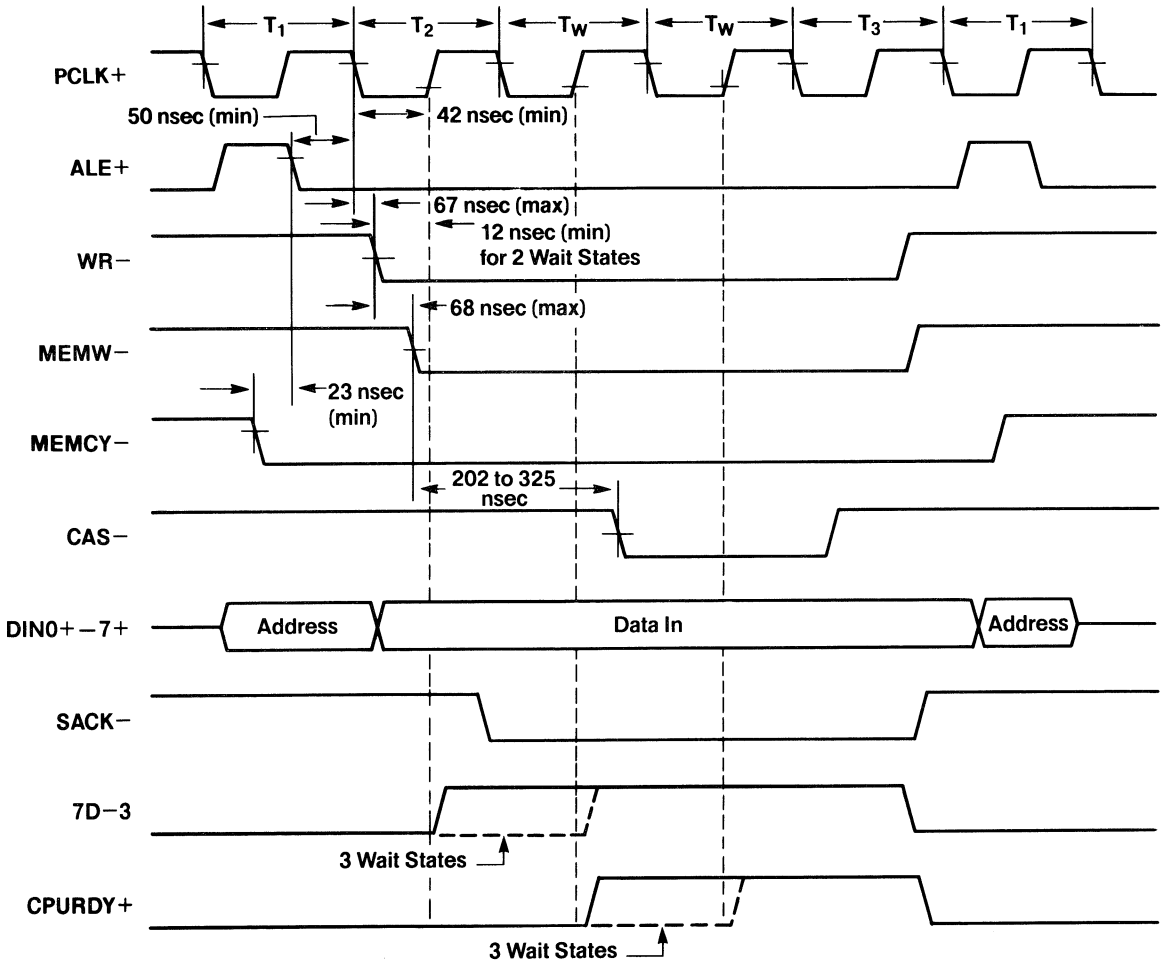
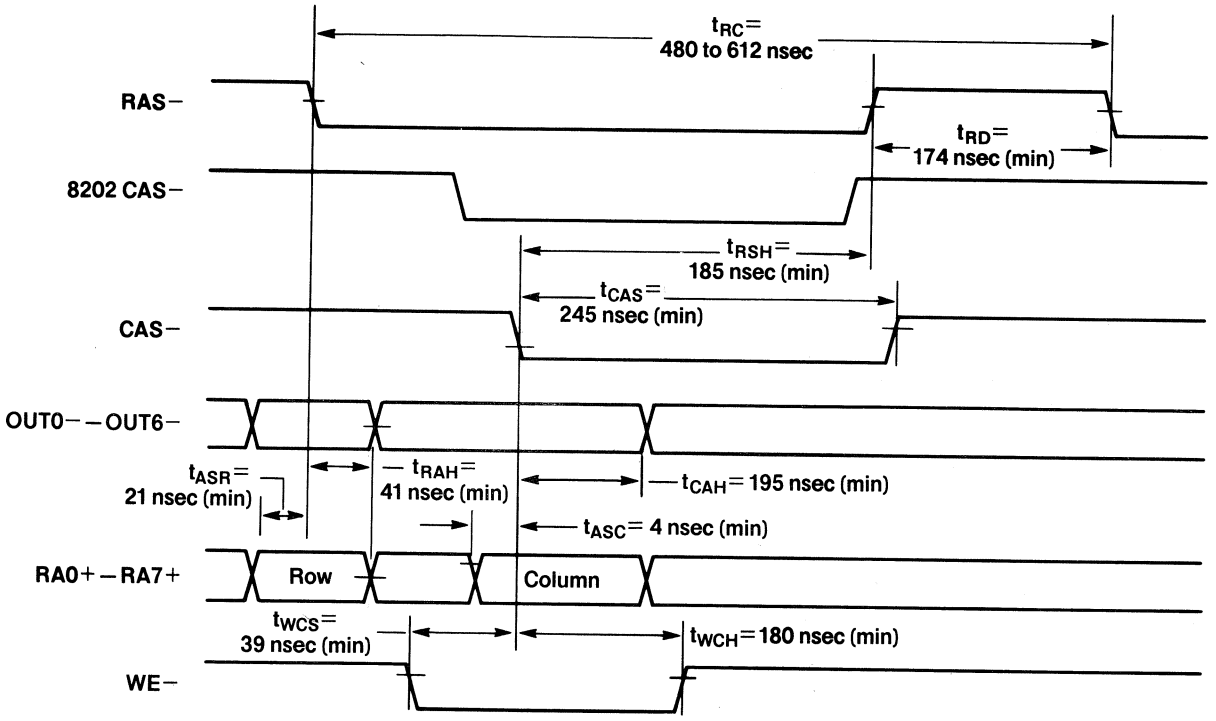


Figure 14-9. Multiline Controller RAM Write Cycle.

During a RAM write cycle, WE- (Write Enable) at pin 28 is asserted after the row address has been latched to enable the RAM WE- (pin 3), allowing data to be written. The timing diagram for memory compatibility is shown in Figure 14-10.

During a RAM read cycle, MEMR- ORs with MEMCY- at bubbled NAND gate 4C (pin 3) to enable the output of data latch 8B (pin 1).



NEC Conditions: t_{RC}=410 nsec (min) t_{RAH}=25 nsec (min)
t_{RP}=150 nsec (min) t_{ASC}=0 nsec (min)
t_{RSH}=165 nsec (min) t_{CAH}=75 nsec (min)
t_{CAS}=165 nsec (min) t_{WCS}=–20 nsec (min)
t_{ASR}=0 nsec (min) t_{WCH}=75 nsec (min)

Figure 14-10. Multiline Controller Memory Compatibility.

To indicate the beginning of a memory access cycle, 1B returns a SACK- (System Acknowledge) to the 8085A-2 CPU. As shown in Figure 14-7, page 4, SACK- NORs at bubbled AND gate 8D (pin 12) with 1Q- (pin 11), which represents a RD-, WR-, or INTA- at 5D (pin 8). The output at pin 13 of 8D delays at shift register 7D (pin 10) as MEMRDY+ (Memory Ready). MEMRDY+ flows to the 8085A-2 CPU as CPURDY+ via OR gate 4C (pin 8) to release the 8085A-2 CPU from its wait state. (Refer to Figures 14-8 and 14-9 for SACK- and

CPURDY+ timing diagrams.) The SACK+ signal is followed by an XACK- (Transfer Acknowledge) from 1B (pin 29), as shown in Figure 14-7, page 3. XACK- latches valid data from the RAM at 8B (pin 11) and signifies to the Multibus via MEMACK- (Memory Acknowledge) that the transfer cycle has been performed (that is, data has been latched or is valid). MEMACK- inverts at 1D (pin 4) as shown in Figure 14-7, page 4, to clock flip-flop 2D (pin 3), which generates MBRDY+ (Multibus Ready) at pin 5. MBRDY+ qualifies with MBCMD+ (Multibus Command) at NAND gate 4E (pin 6) during a Multibus cycle to acknowledge the transfer (XACK-) at the Multibus (P1, pin 23).

Data latch 8B (Figure 14-7, page 3) allows the valid data to enter local data bus LD0+ through LD7+ when requested by MEMR- during MEMCY-.

EPROM

After an 8085A-2 reset condition, local ROM (Read-Only Memory) bootstrap and self-testing is provided by 32K 2732 EPROM (4K by 8 bits) 7C, which accepts 12 bits of local addressing (LA0+ through LAB+) as shown in Figure 14-7, page 2. When local address lines LAC+ through LAF+ are low (that is, addresses 0000h through 0FFFh), 7C is enabled (pin 18). To eliminate bus contention, the outputs of 7C are held in a high-impedance tristate by a 4.7-kilohm pullup resistor (RP4) until a RD- signal enables the EPROM (pin 20), allowing data to be output onto the local data bus (LD0+ through LD7+).

Device Control Logic

I/O Decoder

All local input/output (I/O) is memory mapped at 1000h through 1FFFh. Address decoding is performed via 1-of-8 decoder 12E (Figure 14-7, page 2). When local address lines LAD+ through LAF+ are low and LAC+ is high, 12E is enabled (pins 4, 5, and 6). Local address lines LA2+ through LA4+ are decoded at 12E (pins 1, 2, and 3) to be output as the following I/O lines:

LA4+	LA3+	LA2+	Line	Pin
LOW	LOW	LOW	SIO1CS-	15
LOW	LOW	HIGH	SIO2CS-	14
LOW	HIGH	LOW	TIMER1CS-	13
LOW	HIGH	HIGH	TIMER2CS-	12
HIGH	LOW	LOW	CTRLS-	11
HIGH	LOW	HIGH	LINES-	10
HIGH	HIGH	LOW	SECS-	9

Each I/O function is described in the following list.

SIO1CS-. Enables programmable MPSC 10C (Figure 14-7, page 7), which controls RS-232-C interface lines 1 and 2.

SIO2CS-. Enables programmable MPSC 13C (Figure 14-7, page 7), which controls RS-232-C interface lines 3 and 4.

TIMER1CS-. Enables programmable interval timer 19D (Figure 14-7, page 6), which sets internal baud-rate clocks for lines 1 and 2, and which interrupts the 8085A-2 at RST6.5.

TIMER2CS-. Enables programmable interval timer 19C (Figure 14-7, page 6), which sets internal baud-rate clocks for lines 3 and 4, and which interrupts the 8085A-2 at RST5.5.

CTRLS-. Clocks Control register 17C and interrupt register 18E, and enables Read-Back register 18C (Figure 14-7, page 5) to select internal versus external baud rates and to provide for Multibus interrupt logic via interrupt flip-flop 18E (pin 5).

LINES-. Enables the read-only Line Select register 19B (Figure 14-7, page 7) to allow for additional RS-232-C TDSR- (Data Set Ready) and TRI- (Ring Indicator) lines that are not supported by MPSCs 10C and 13C.

SECS-. Enables Secondary Data register 20B and clocks Secondary Data register 19A (Figure 14-7, page 7) to provide for secondary receive and transmit channels (respectively), which generate low-speed baud rates independent of MPSCs 10C and 13C.

Port addresses for local I/O space are provided under "Architecture," above.

Programmable MPSC

The 7201 MPSCs (10C and 13C) are used to control the RS-232-C interface channels as shown in Figure 14-7, page 7. Either 10C or 13C is enabled (pin 23) after 8-to-1 line decoder 12E (Figure 14-7, page 2) outputs the appropriate local address signals (LA2+ through LA4+) to generate SIO1CS- or SIO2CS-, respectively.

The two least significant local address lines (LA0+ and LA1+) select the four programmable internal registers of 10C or 13C that are used (pins 24 and 25). Port addresses and internal register modes for 10C and 13C are provided under "Architecture," above.

To request an interrupt, 10C or 13C sends an eight-bit vectored INT- (Interrupt) request (pin 28), buffered by inverter 1E (pin 4), to the 8085A-2 as COMMINT+ (Communications Interrupt). A 4.7-kilohm pullup resistor (RP4) is required for the open-collector line. The 8085A-2 responds with INTA- (Interrupt Acknowledge) to 10C and 13C (pin 27).

MPSC 10C receives the highest priority within the daisy chain since PRI- (pin 29) is tied to ground.

Each MPSC is supplied with +5 Vcc at pin 40 and is grounded at pin 20.

The following RS-232-C interface lines are supported by each MPSC channel:

Line	Definition	Function
TTXD+	Transmit Data	Transmits serial data to the communications channel
TRTS-	Request to Send	Signifies that channel is ready to send
TDTR-	Data Term Ready	Modem control
TRXD+	Receive Data	Receives serial data from communications channel

TCTS-	Clear to Send	Signifies that modem is ready to accept data
TDCD-	Data Carrier Detect	Signifies start of line transmission
STXC-	Transmitter Clock	Controls transmission rate of output data
SRXC-	Receiver Clock	Controls transmission rate of input data

The following RS-232-C lines are supported by other registers:

Line	Definition	Function
TSTD+	Secondary Transmit Data	Transmits low-speed serial data
TSRD+	Secondary Receive Data	Receives low-speed serial data
TDSR-	Data Set Ready	Indicates status of modem
TRI-	Ring Indicator	Indicates that a ringing signal is being received

The TTXD+, TRTS-, TDTR-, and TSTD+ signals are inverted and generated from RS-232-C drivers 10B, 12A, 13A, and 15A (Figure 14-7, page 8) to the Multibus. The TRXD+, TCTS-, TDCD-, STXC-, SRXC-, TSRD+, TDSR-, and TRI- signals are derived from RS-232-C signals received at the 1489 receivers shown in Figure 14-7, page 8.

Programmable Interval Timer

Two 8253 programmable interval timers (19D and 19C) generate internal baud rate clocks and interrupts as shown in Figure 14-7, page 6. Either 19D or 19C is enabled (pin 21) after 8-to-1 line decoder 12E (Figure 14-7, page 2) outputs the appropriate local address signals (LA2+ through LA4+) to generate TIMER1CS- or TIMER2CS-, respectively.

The two least significant local address lines (LA0+ and LA1+) select the appropriate control modes (pins 19 and 20). Port addresses and control modes for 19D and 19C are provided under "Architecture," above.

Internal baud-rate clocks OUT0 and OUT1 (pins 10 and 13) are generated into appropriate multiplexer 17A, 17B, 18B, or 18A (depending on the channel), where either OUT0 and OUT1 or external clocks (TTXC/TRXC) may be selected as the RS-232-C interface clock.

When Control register 17C (Figure 14-7, page 5) generates the appropriate signals to cause EXT1+ through EXT4+ to go low at multiplexers 17A, 17B, 18B, and 18A (pin 19 of 17A, and pin 1 of 17B, 18B, and 18A) in Figure 14-7, page 6, 19D and 19C act as asynchronous modems and provide the internal clocks out to the RS-232-C interface. Otherwise, external clocks (that is, synchronous modems) are selected by 17A, 17B, 18B, and 18A.

Clocks TCLK1- and TCLK2- (branching from 19D, pins 10 and 13) and clocks TCLK3- and TCLK4- (branching from 19C, pins 10 and 13) connect to the RS-232-C interface connectors (Figure 14-7, page 8).

The OUT2 signals of 19D and 19C are sent to the 8085A-2 as TMRINT1+ or TMRINT2+ to interrupt the CPU at RST6.5 or RST5.5, respectively.

Multiline I/O Interconnect Wirelist

Signal	P5	P1	P2	P3	P4
DCD1+	1	8			
STD1-	3	14			
DSR1+	4	6			
TXC1+	5	15			
SRD1-	7	16			
CTS1+	8	5			
RXC1+	9	17			
RTS1+	10	4			
DTR1+	11	20			
RI1+	13	22			
RXD1-	14	3			
TXD1-	16	2			
STD2-	15		14		
TXC2+	17		15		
SRD2-	19		16		
DCD2+	20		8		
RXC2+	21		17		
DSR2+	22		6		
DTR2+	23		20		
RI2+	25		22		
CTS2+	26		5		
RXD2-	27		3		
TXD2-	29		2		
RTS2+	30		4		
DCD3+	31			8	
CTS3+	32			5	
DSR3+	33			6	
STD3-	35			14	
RTS3+	36			4	
TXC3+	37			15	
SRD3-	39			16	
RXD3-	40			3	

Signal	P5	P1	P2	P3	P4
RXC3+	41			17	
TXD3-	42			2	
DTR3+	43			20	
RI3+	45			22	
DCD4+	46				8
STD4-	47				14
DSR4+	48				6
TXC4+	49				15
SRD4-	51				16
CTS4+	52				5
RXC4+	53				17
RTS4+	54				4
DTR4+	55				20
RI4+	57				22
RXD4-	58				3
TXD4-	59				2
GND	2,6, 12, 18, 28, 38, 44, 56	1,7	1,7	1,7	1,7
CLK1+	34	24			
CLK2+	24		24		
CLK3+	50			24	
CLK4+	60				24