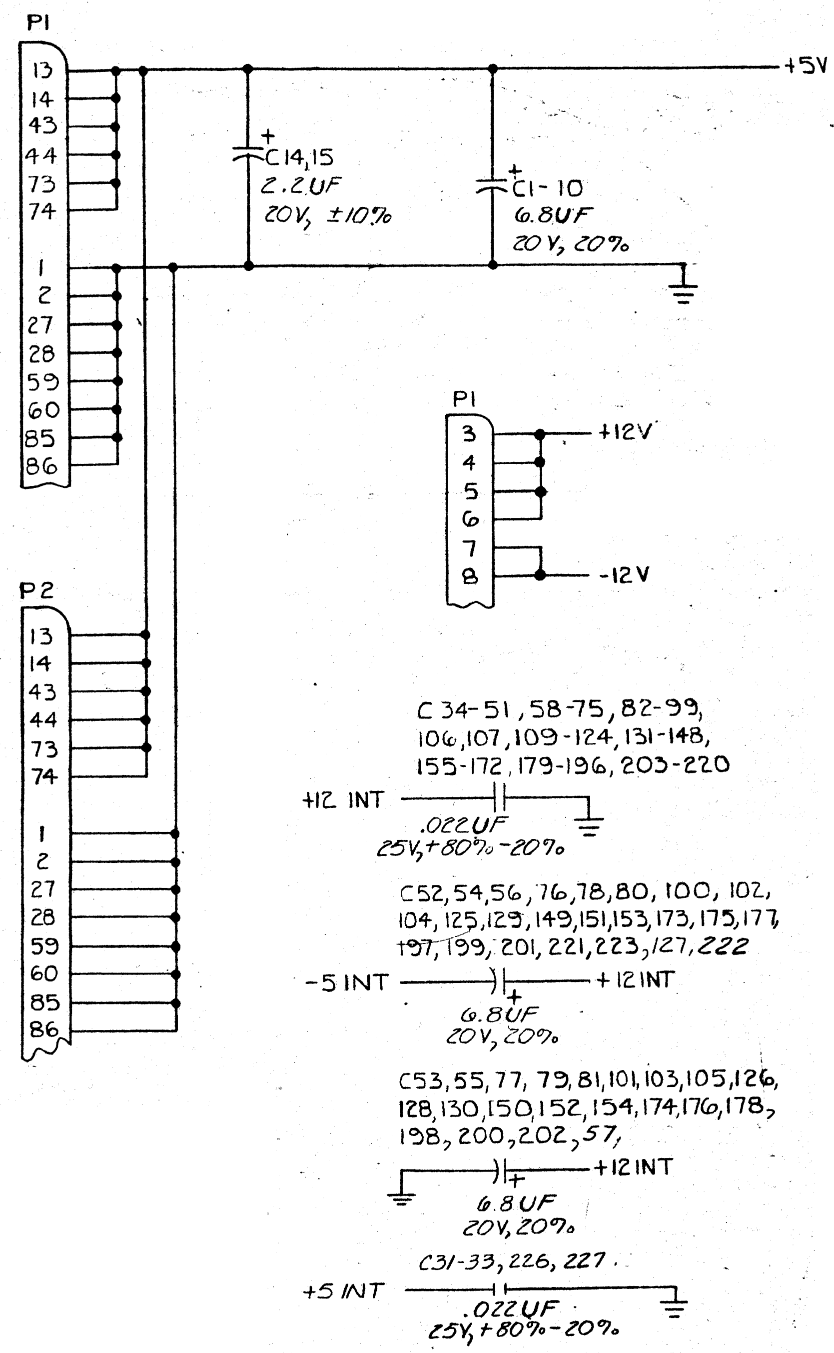
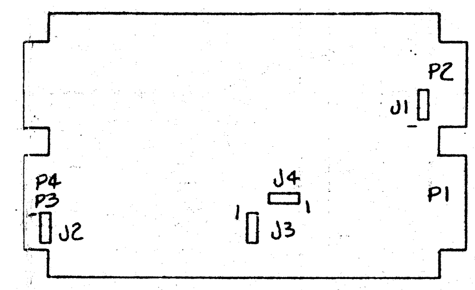
REVISIONS					
REV	DESCRIPTION	DR	CH	DATE	APPROVAL
F0	PRODUCTION RELEASE EN 10011R	BH	KZ	11 NOV 82	W Chung

TABULATION BLOCK

DASH NO.	DESCRIPTION
-01	4K, NO PARITY, NO BBU, MEDIUM SPEED
-02	8K, NO PARITY, NO BBU, MEDIUM SPEED
-03	16K, NO PARITY, NO BBU, MEDIUM SPEED
-04	32K, NO PARITY, NO BBU, MEDIUM SPEED
-05	4K, NO PARITY, WITH BBU, MEDIUM SPEED
-06	8K, NO PARITY, WITH BBU, MEDIUM SPEED
-07	16K, NO PARITY, WITH BBU, MEDIUM SPEED
-08	32K, NO PARITY, WITH BBU, MEDIUM SPEED
-09	32K, NO PARITY, WITH BBU, HIGH SPEED
-10	16K, PARITY, WITH BBU, MEDIUM SPEED
-11	32K, PARITY, WITH BBU, MEDIUM SPEED
-12	32K, PARITY, WITH BBU, HIGH SPEED
-15	16K, NO PARITY, NO BBU, HIGH SPEED
-17	16K, MOS RAM, HIGH SPEED MEMORY
-18	16K, MOS RAM, HIGH SPEED, BBU
-19	16K, MOS RAM, HIGH SPEED, BBU, PARITY
-20	24K, MOS RAM, MED. SPEED, MEMORY
-21	24K, MOS RAM, MED. SPEED, W/ BBU
-22	24K, MOS RAM, MED. SPEED, BBU, PARITY
-23	32K, MOS RAM, HIGH SPEED





COMPONENT SIDE

IC DESIG	IC TYPE	UNUSED PINS IN	UNUSED PINS OUT
80	74S03	1,2	3
80	74S03	4,5	6
82	96L02	1,2,3,4,5	6,7
86	74LS14	11	10
95	74128	5,6	4
95	74128	8,9	10

UNUSED GATES / IC

IC DESIG	IC TYPE	UNUSED PINS IN	UNUSED PINS OUT
4	74S08	4,5	6
13	74S132	12,13	11
20	74125	1,2	3
20	74125	4,5	6
30	74S10	9,10,11	8
36	74S00	4,5	6
36	74S00	1,2	3
37	7438	1,2	3
37	7438	12,13	11
44	74LS08	1,2	3
49	74S00	9,10	8
56	74LS00	4,5	6
56	74LS00	9,10	8
56	74LS00	12,13	11
58	74S04	3	4
58	74S04	9	8
58	74S04	11	10
62	74LS86	1,2	3
71	74S03	4,5	6
71	74S03	9,10	8

10. THESE IC'S ARE CONNECTED TO +5V INT: IC'S 1,2,5,7,8,23,24,29,35,44,50,51,52,54,55,56,67,82,84,85,87-102.
9. COMPONENTS & CIRCUITRY NOTED NOT USED ON -01 THRU -10,-12,-13,-17 THRU -23
8. FOR REQUIREMENT, TYPE, VALUE, OR ASSY POSITION OF OPTIONAL COMPONENTS SEE COMPONENT OPTION TABULATION BLOCK (ZONE AR-17).
7. ETCH REPRESENTED BY LINES A, B & C WILL BE CUT PRIOR TO INSTALLATION OF SW1
6. CAPACITOR VALUES ARE IN MICROFARADS ±5%, 100V.
5. REFERENCE DESIGNATIONS INTENTIONALLY OMITTED: C108, C18, R14.
4. RESISTOR PACK VALUES ARE IN OHMS.
3. RESISTOR VALUES ARE IN OHMS ±5% 1/4W.
2. LAST REF DESIGNATION USED: IC 248, Q14, CR13, RP2, R67, C227, L2, T1, SW2, J4, BT1, VR2, LED1, W3, E6.
1. FOR LOGIC DASH NO. SEE TABULATION BLOCK.

NOTES: UNLESS OTHERWISE SPECIFIED

31

NOTES UNLESS SPECIFIED
1. TOLERANCES .XX ±.03 .XXX ±.010 ANGULAR ±1/2°
2. BREAK ALL SHARP EDGES .010 APPROX.
3. ALL DIM. IN INCHES

DASH NO.	NEXT ASSEMBLYS

DR. RAY ...
CHK.
DSG. G
ENGR.

ComputerAutomation
18651 Von Karman, Irvine, Calif. 92664

TITLE
LOGIC DIAGRAM 32K MOS RAM HI SPEED MEMORY W/ BBU & PARITY

SIZE D | DWG. NO. 75-53707-XX | REV F0

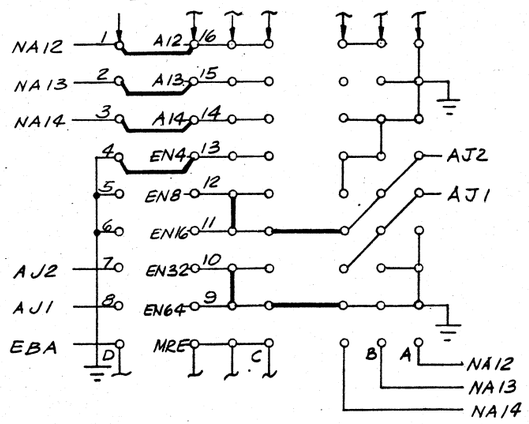
DO NOT SCALE DRAWING | SCALE = NONE | SHT. 1 OF 14

8 7 6 5 4 3 1

COMPONENT OPTION TABULATION BLOCK

DASH NO	IC 97	C11	C12	C13	C16	R5A	R5B	R7	R8	R60	R11A	R11B	R46	R61	R62	RP1	SW1	JUMPERS	CR14	R48
-01	-	510 PF	330 PF	-	-	-	100	100	-	A	-	10	6.8K	10	10	A	-	W1, W2	IN4448	10
-02	-	510 PF	330 PF	-	-	-	100	100	-	B	-	10	6.8K	10	10	B	-	W1, W2	↑	10
-03	-	510 PF	330 PF	-	-	-	100	100	-	C	-	10	6.8K	10	10	C	-	W1, W2	↑	10
-04	74128	510 PF	330 PF	-	-	-	100	100	-	D	-	10	6.8K	10	10	D	-	W1, W2	↑	10
-05	-	510 PF	330 PF	-	-	-	100	100	-	A	-	10	6.8K	10	10	A	-	-	↑	10
-06	-	510 PF	330 PF	-	-	-	100	100	-	B	-	10	6.8K	10	10	B	-	-	↑	10
-07	-	510 PF	330 PF	-	-	-	100	100	-	C	-	10	6.8K	10	10	C	-	-	↓	10
-08	74128	510 PF	330 PF	-	-	-	100	100	-	D	-	10	6.8K	10	10	D	-	-	IN4448	10
-09	74128	150 PF	200 PF	-	-	-	100	100	-	D	-	10	6.8K	10	10	D	✓	-	-	10
-10	-	-	-	200 PF	330 PF	10	-	-	100	C	10	-	-	-	-	C	-	-	-	10
-11	74128	-	-	200 PF	330 PF	10	-	-	100	D	10	-	-	-	-	D	✓	-	-	10
-12	74128	150 PF	-	200 PF	330 PF	-	100	-	100	D	10	-	-	-	-	D	-	-	-	10
-13	—	150 PF	200 PF	-	-	-	100	100	-	B	-	10	6.8K	10	10	B	✓	W1, W2	-	10
-17	—	150 PF	200 PF	—	—	—	100	100	—	C	—	10	6.8K	10	10	C	—	W1, W2	-	10
-18	—	150PF	200PF	—	—	—	100	100	—	C	—	10	6.8K	10	10	C	—	—	-	10
-19	—	150PF	—	200PF	330 PF	—	—	—	100	C	10	—	—	—	—	C	—	—	—	10
-20	74128	150PF	330PF	—	—	—	100	100	—	*	—	10	6.8K	10	10	*	—	W1, W2	IN4448	—
-21	74128	150PF	330PF	—	—	—	100	100	—	*	—	10	6.8K	10	10	*	—	—	IN4448	-
-22	74128	—	—	200PF	330PF	10	—	—	100	*	10	—	—	—	—	*	—	—	-	-
-23	74128	150PF	200PF	—	—	—	100	100	—	D	—	10	6.8K	10	10	D	—	W1, W2	—	10

* RP1 AND R60 ARE NOT USED ON 24K (DASH NOS. -20, -21, -22) AND BOARD IS CONNECTED WITH JUMPERS AS SHOWN BELOW.



* 24 K PATCH
-20, -21 AND -22 ONLY
JUMPERS REPRESENTED
BY HEAVY LINES

SIZE	DRAWING NO.	REV
D	75-53707-XX	F0
	SHT. 2A OF	

P1	SIGNAL	DIRECTION	LOCATION
PIN 1	GND	IN	C8
2	GND	IN	C8
3	+12 V		C6
4	+12 V		
5	+12 V		
6	+12 V		
7	-12 V	IN	C6
8	-12 V	IN	C6
9	DPIN -	IN	B9
10	DPOT-	OUT	B9
11	NU		
12	NU		
13	+5V	IN	D8
14	+5V	IN	D8
15	NU		
16	AL -	IN	B45
17	MACK-	OUT	B49
18	RD -	IN	A48
19	EBA -	IN	A48
20	SLB -	IN	A48
21	NU		
22	MDIS -	IN	C53
23	NU		
24	NU		
25	NU		
26	NU		
27	GND	IN	C8
28	GND	IN	C8
29	NU		
30			
31			
32			
33			
34			
35			
36	NU		
37	MBIN	IN	B11
38	MBOT	OUT	B11
39	DB00 -	OUT	D33
40	DB01 -	OUT	D33
41	DB02 -	OUT	C33
42	DB03 -	OUT	C33
PIN 43	+5V	IN	D8

P1	SIGNAL	DIRECTION	LOCATION
PIN 44	+5V	IN	D8
45	DB04 -	OUT	D33
46	DB05 -		D33
47	DB06 -		D33
48	DB07 -		C33
49	DB08 -		C33
50	DB09 -		C33
51	DB10 -		B33
52	DB11 -	OUT	B33
53	NU		
54	NU		
55	NU		
56	NU		
57	EXEC -	IN	A48
58	NU		
59	GND	IN	C8
60	GND	IN	C8
61	NU		
62	NU		
63	NU		
64	NU		
65	IVR -	OUT	C60
66	ILI -	OUT	C82
67	NU		
68			
69			
70			
71			
72	NU		
73	+5V	IN	D8
74	+5V	IN	D8
75	NU		
76			
77			
78			
79			
80			
81			
82	NU		
83	PRIN -	IN	B10
84	PROT -	OUT	B10
85	GND	IN	C8
PIN 86	GND	IN	C8

P2	SIGNAL	DIRECTION	LOCATION
PIN 1	GND	IN	B8
2	GND	IN	B8
3	NU		
4			
5			
6			
7			
8	NU		
9	DPIN -	IN	B11
10	DPOT -	OUT	B11
11	NU		
12	NU		
13	+5V	IN	C8
14	+5V	IN	C8
15	MST -	IN	D54
16	NU		
17			
18			
19			
20			
21	NU		
22	MDIS -	IN	C64
23	AB08 -		C48
24	AB09 -		B48
25	AB10 -		B48
26	AB11 -		B48
27	GND		B8
28	GND		B8
29	AB12 -		B48
30	AB13 -		B48
31	AB14 -		B48
32	AB15 -	IN	B48
33	DB16 -	OUT	B82
34	DB17	OUT	A82
35	NU		
36	NU		
37	MBIN	IN	D64
38	MBOT	OUT	C60
39	DB00 -		D33
40	DB01 -		D33
41	DB02 -		C33
42	DB03 -	OUT	C33
PIN 43	+5V	IN	C8

P2	SIGNAL	DIRECTION	LOCATION
PIN 44	+5V	IN	C8
45	DB04 -	OUT	D33
46	DB05 -	OUT	D33
47	DB06 -	OUT	D33
48	DB07 -	OUT	C33
49	NU		
50	NU		
51	NU		
52	NU		
53	DB12 -	OUT	B33
54	DB13 -	OUT	B33
55	DB14 -	OUT	A33
56	DB15 -	OUT	A33
57	NU		
58	NU		
59	GND	IN	B8
60	GND	IN	B8
61	NU		
62	NU		
63	CLK -	IN	D64
64	NU		
65	NU		
66	NU		
67	IAR -	IN	B85
68	NU		
69	RST -	IN	B85
70	NU		
71	PUSE -	IN	C85
72	NU		
73	+5V	IN	C8
74	+5V		B8
75	AB03 -		C48
76	AB04 -		
77	AB05 -		
78	AB06 -		
79	AB07 -		C48
80	AB00 -		D48
81	AB01 -		D48
82	AB02 -	IN	D48
83	PRIN -	IN	B10
84	PROT -	OUT	B10
85	GND	IN	B8
PIN 86	GND	IN	B8

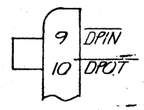
J1	SIGNAL	DIRECTION	LOCATION
PIN 1	DOSL -	OUT	C65
2	NU		
3	DISL -	OUT	C65
4	DOSF -		B65
5	DOSU -		C65
6	DISU -		B65
PIN 7	DISF -	OUT	B65

J2	SIGNAL	DIRECTION	LOCATION
PIN 1	BS13 -	IN	D46
2	BS12 -	IN	D46
3	BS19 -	IN	D46
4	NU		
5	INTER -	IN	C46
6	ØDD -		C46
7	ENABLELOW		C46
8	ENABLEHIGH		C46
9	GND		B46
10	GND		B46
11	GND		B46
12	GND	IN	B46
13	NU		
14	NU		
15	NU		
PIN 16	NU		

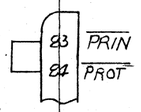
J3	SIGNAL	DIRECTION	LOCATION
PIN 1	FALL -	OUT	C65
2	WELBT -	OUT	C65
3	NU		
4	NU		
5	NU		
6	NU		
7	REF -	OUT	C65
8	CS7 -		D65
9	CS6 -		D65
10	CS5 -		D65
11	WEUBT -		C65
12	CS4 -		D65
13	CS3 -		D65
14	CS2 -		D65
15	CS1 -		D65
PIN 16	CS0 -	OUT	D65

J4	SIGNAL	DIRECTION	LOCATION
PIN 1	FRUN -	OUT	C65
2	NU		
3	NU		
4	REFI -	OUT	C65
5	REFC	OUT	C65
6	MB -	OUT	C65
PIN 7	FSTOP -	OUT	C65

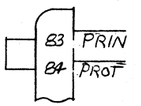
P2



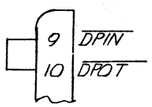
P2



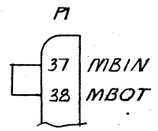
P1



P1



P1



SIZE		REV
D	75-53707-XX	F0
	SHT. 2 OF	

DRAWING NO. 75-53707-XX REV F0

LOWER RAM ARRAY TABULATION BLOCK	
DASH NO'S.	IC'S USED
-01, -05	103-118
-02, -06	103-118 121-136
-03, -04, -07, -08, -09, -13, -17, -18, -20, -21, -23	103-118 121-136 139-154 157-172
-10, -11, -12, -19, -22	103-174

LOWER RAM ARRAY

(SEE TABULATION BLOCK FOR IC'S USED IN EACH ASSY)

MA04L (C54)
MA05L (C54)
MA01L (D54)
MA00L (D54)
MA02L (D54)
MA03L (D54)
MA06 (B55)

5280'S/4060'S

-5 INT
+12 INT
+5 INT

103	104	105	106	107	108	109	110	111	112	113	114	115	116	117	118	119	120	
121	122	123	124	125	126	127	128	129	130	131	132	133	134	135	136	137	138	
139	140	141	142	143	144	145	146	147	148	149	150	151	152	153	154	155	156	
157	158	159	160	161	162	163	164	165	166	167	168	169	170	171	172	173	174	

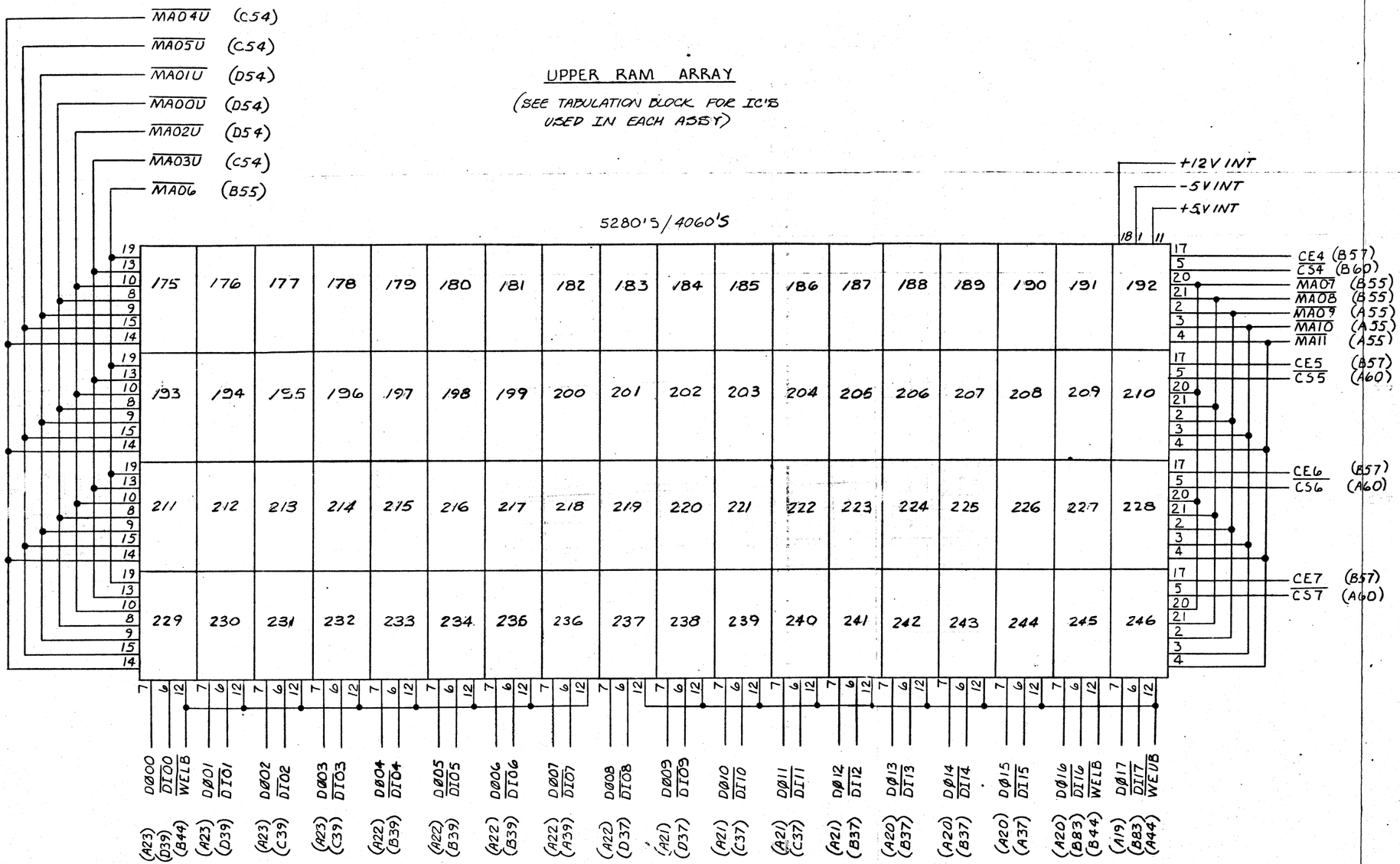
CE0 (D57)
CS0 (B60)
MA07 (B55)
MA08 (B55)
MA09 (B55)
MA10 (B55)
MA11 (B55)
CE1 (D57)
CS1 (B60)
CE2 (D57)
CS2 (B60)
CE3 (D57)
CS3 (B60)

(A31, D40) DØ00 (D39) DI00
(A31, D40) DØ01 (D39) DI01
(B44) WELB
(A31, C40) DØ02 (C39) DI02
(A31, C40) DØ03 (C39) DI03
(A30, B40) DØ04 (B39) DI04
(A30, B40) DØ05 (B39) DI05
(A30, B40) DØ06 (B39) DI06
(A30, A40) DØ07 (A39) DI07
(A30, D38) DØ08 (D37) DI08
(A29, D38) DØ09 (D37) DI09
(A29, C38) DØ10 (C37) DI10
(A29, C38) DØ11 (C37) DI11
(A29, B38) DØ12 (B37) DI12
(A28, B38) DØ13 (B37) DI13
(A28, B38) DØ14 (B37) DI14
(A37) DI15
(A28, B84) DØ16 (B83) DI16
(B44) WELB
(A27, B84) DØ17 (B83) DI17
(A44, B83) WEUB

UPPER RAM ARRAY TABULATION BY	
DASH NOS	ICS USE
-01,-02,-03,-05, -06,-07,-10,-13, -17, -18,-19	—
-04, -08, -09,-23	175-190, 193-208, 211-226, 229-244
-11, -12	175-246
-20, -21	175-190, 193-208
-22	175-210

UPPER RAM ARRAY

(SEE TABULATION BLOCK FOR IC'S USED IN EACH ASSY)



SIZE	DRAWING NO.	REV
D	75-53707-XX	F0
	SHT. 4 OF	

DATA INPUT-OUTPUT

LATCH

(A23) DØ00 → 74S03 (66) → 7432 (65) → $\overline{DI00}$ (A23, A31, D36, D88)

(A22) DØ08 → 74S03 (74) → 7432 (73) → $\overline{DI08}$ (A21, A29, C35, C36, D85)

(A23) DØ01 → 74S03 (66) → 7432 (65) → $\overline{DI01}$ (A23, A31, D36, D88)

(A21) DØ09 → 74S03 (74) → 7432 (73) → $\overline{DI09}$ (A21, A29, C35, C36, D85)

(A23) DØ02 → 74S03 (66) → 7432 (65) → $\overline{DI02}$ (A23, A31, D36, D88)

(A21) DØ10 → 74S03 (74) → 7432 (73) → $\overline{DI10}$ (A21, A29, B35, B36, D85)

(A23) DØ03 → 74S03 (66) → 7432 (65) → $\overline{DI03}$ (A23, A31, C36, D88)

(A21) DØ11 → 74S03 (74) → 7432 (73) → $\overline{DI11}$ (A21, A29, B35, B36, D85)

(A22) DØ04 → 74S03 (70) → 7432 (69) → $\overline{DI04}$ (A22, A30, A37, D88)

(A21) DØ12 → 74S03 (78) → 7432 (77) → $\overline{DI12}$ (A21, A29, D35, B35, D85)

(A22) DØ05 → 74S03 (70) → 7432 (69) → $\overline{DI05}$ (A22, A30, A37, D88)

(A20) DØ13 → 74S03 (78) → 7432 (77) → $\overline{DI13}$ (A20, A28, A35, D35, D85)

(A22) DØ06 → 74S03 (70) → 7432 (69) → $\overline{DI06}$ (A22, A30, A37, D88)

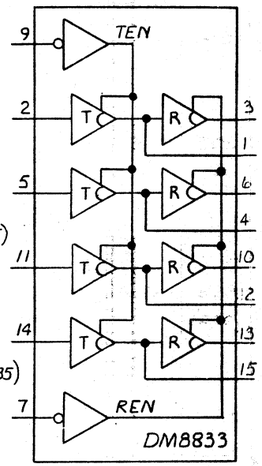
(A20) DØ14 → 74S03 (78) → 7432 (77) → $\overline{DI14}$ (A20, A28, A35, D35, D85)

(A22) DØ07 → 74S03 (70) → 7432 (69) → $\overline{DI07}$ (A22, A30, A37, C88)

(A20) DØ15 → 74S03 (78) → 7432 (77) → $\overline{DI15}$ (A20, A28, A35, C35, C85)

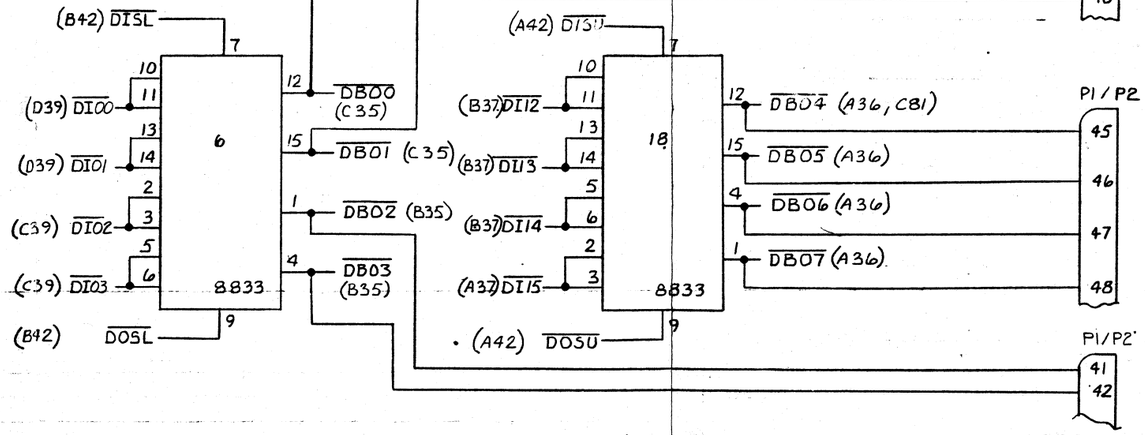
(A50) RDR

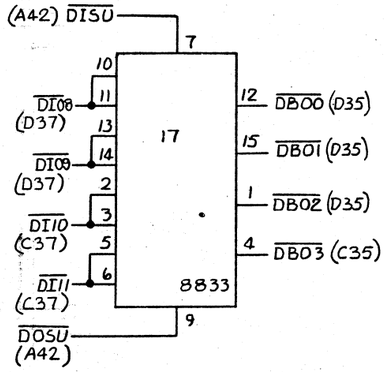
(B43) STRB

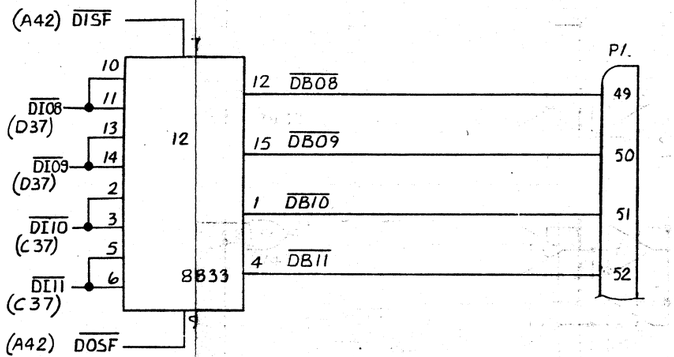


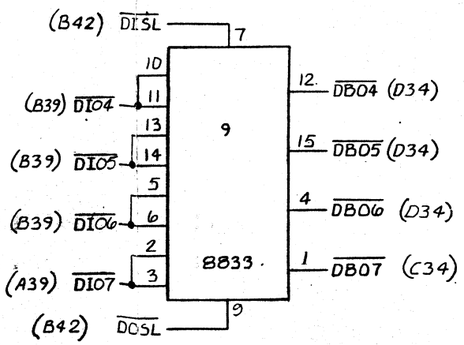
TYPICAL 6 PLACES

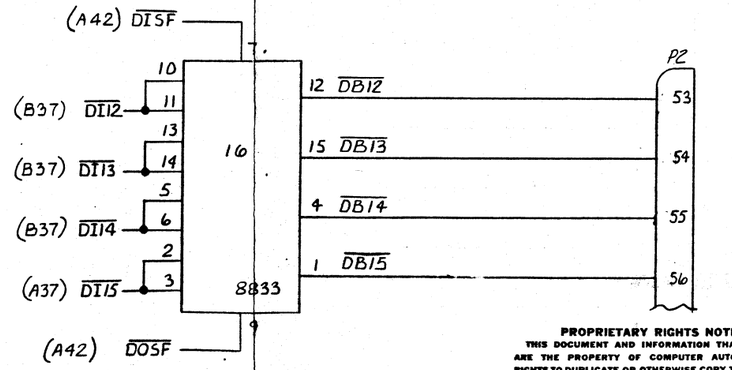
TRANSCEIVERS







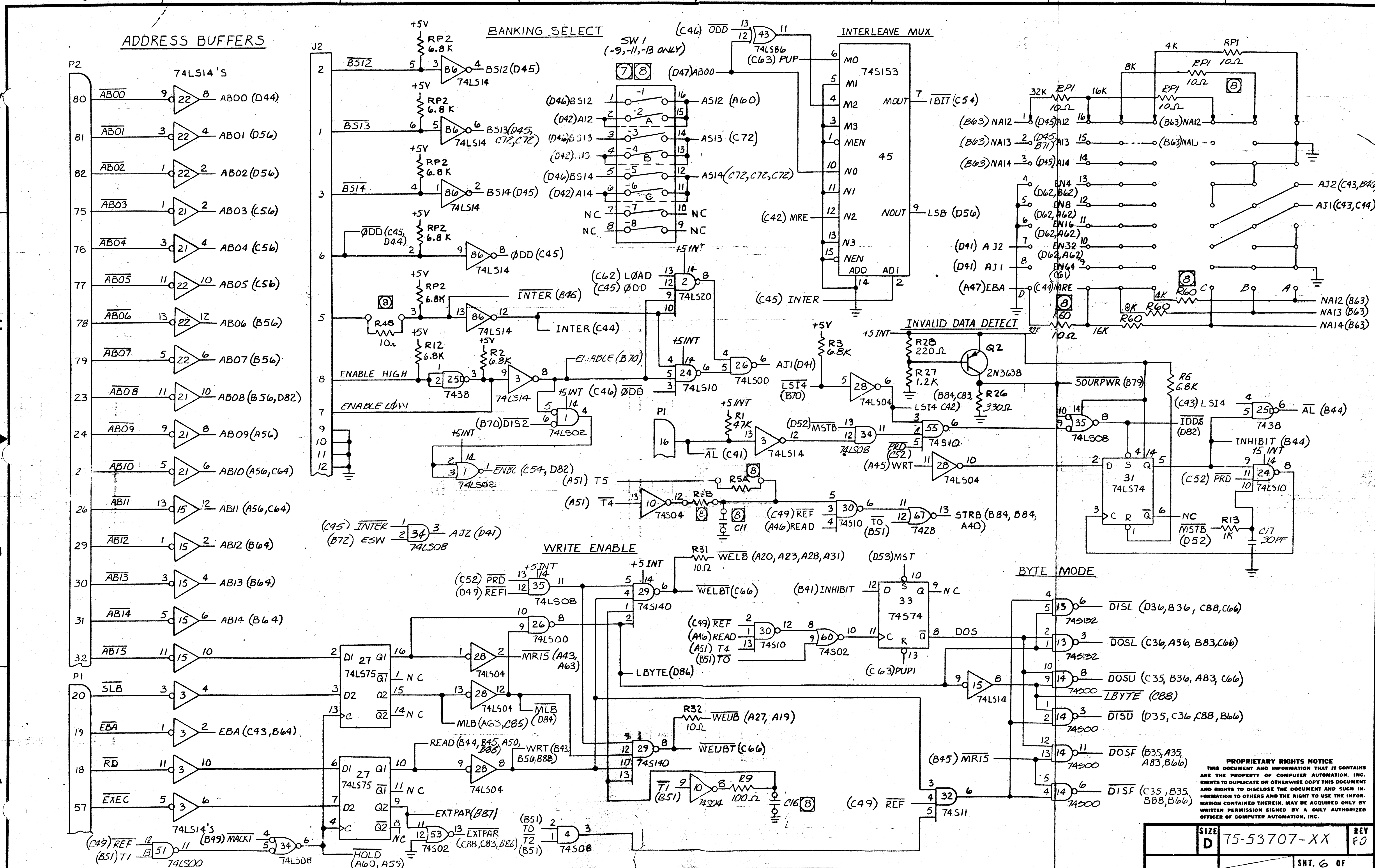




SIZE	DRAWING NO.	REV
D	75-73707-XX	FO
	SHT. 5 OF	

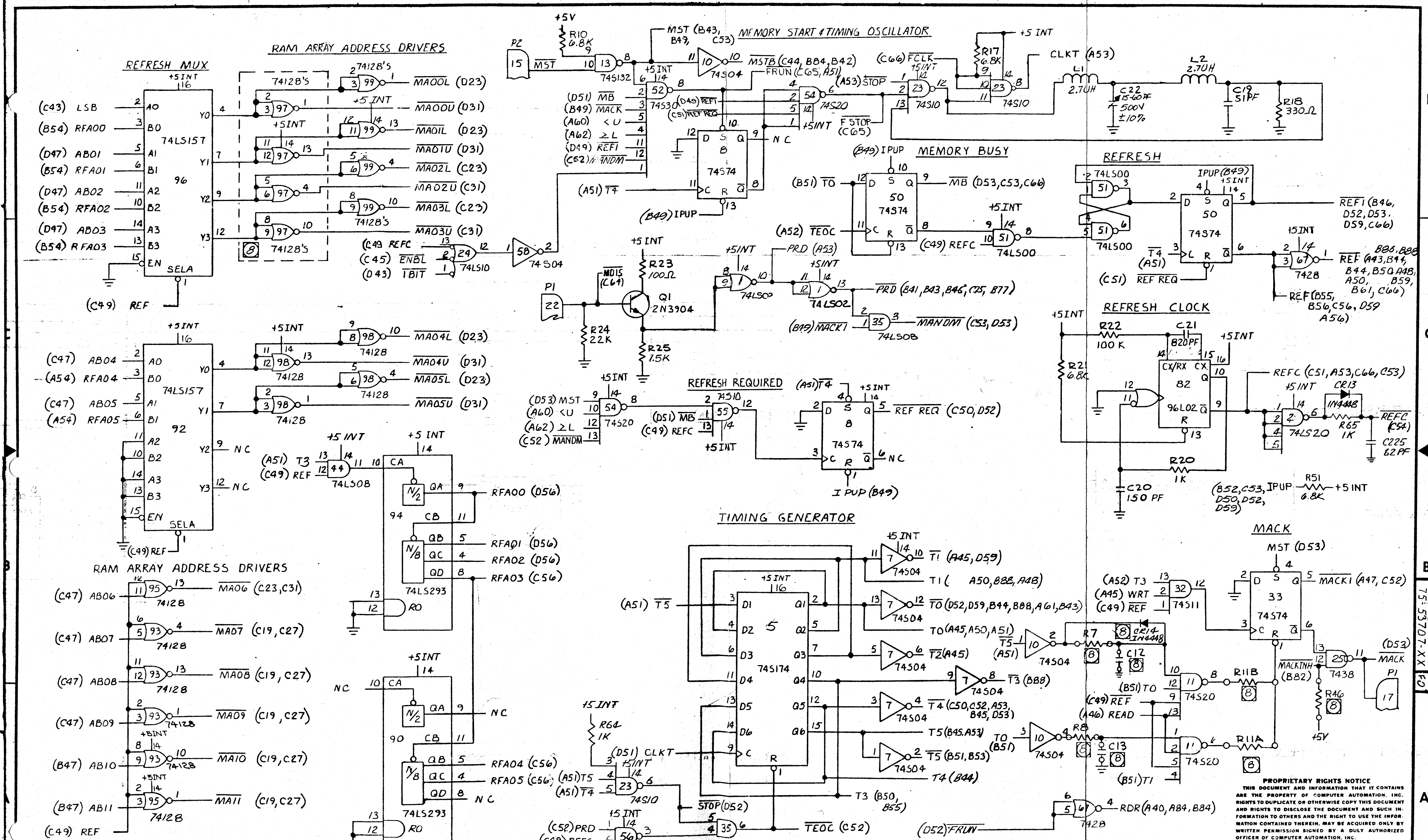
40 39 38 37 36 35 34 33

D C B A



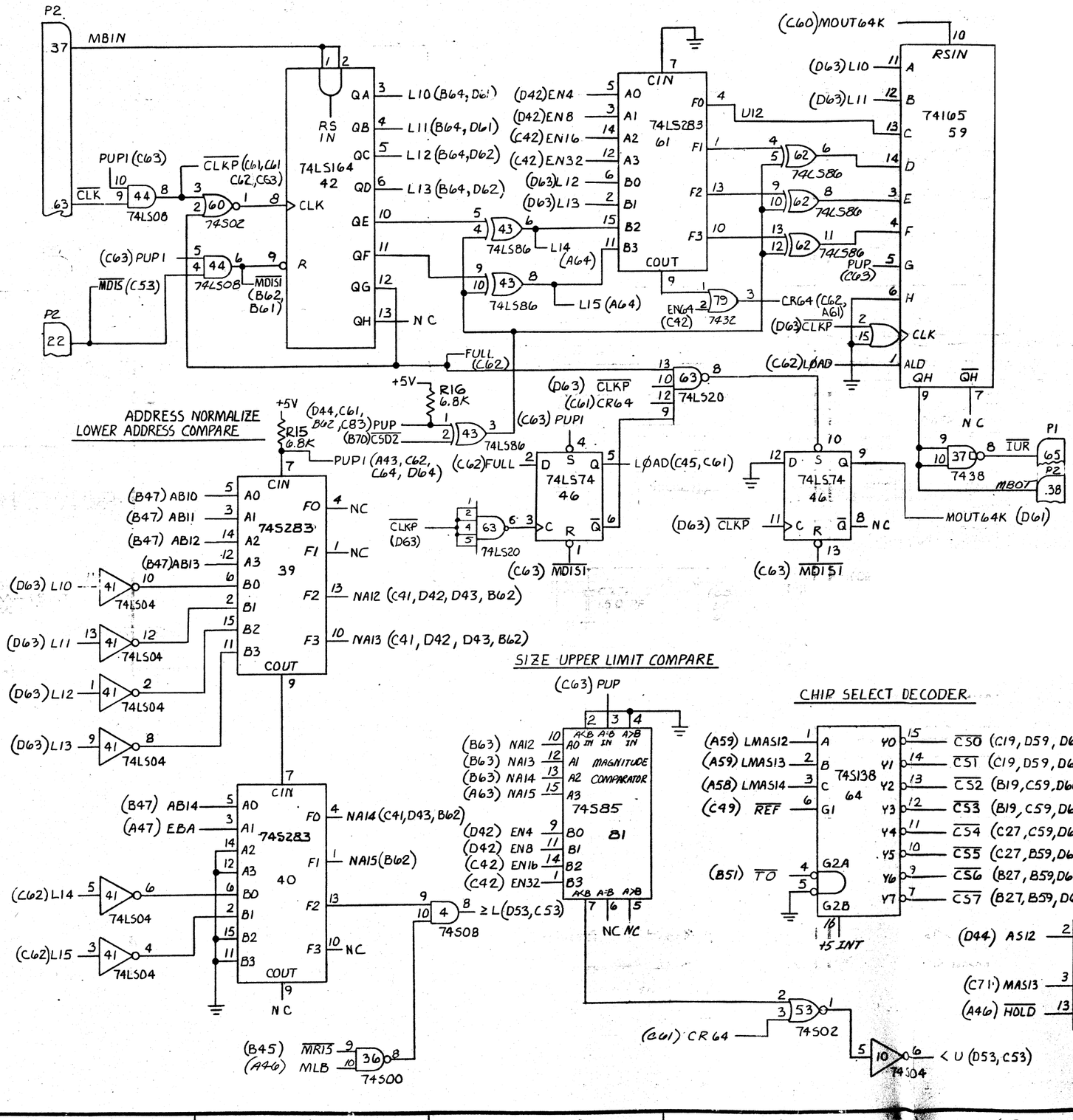
SIZE		REV
D	75-53707-XX	F0

SHT. 6 OF

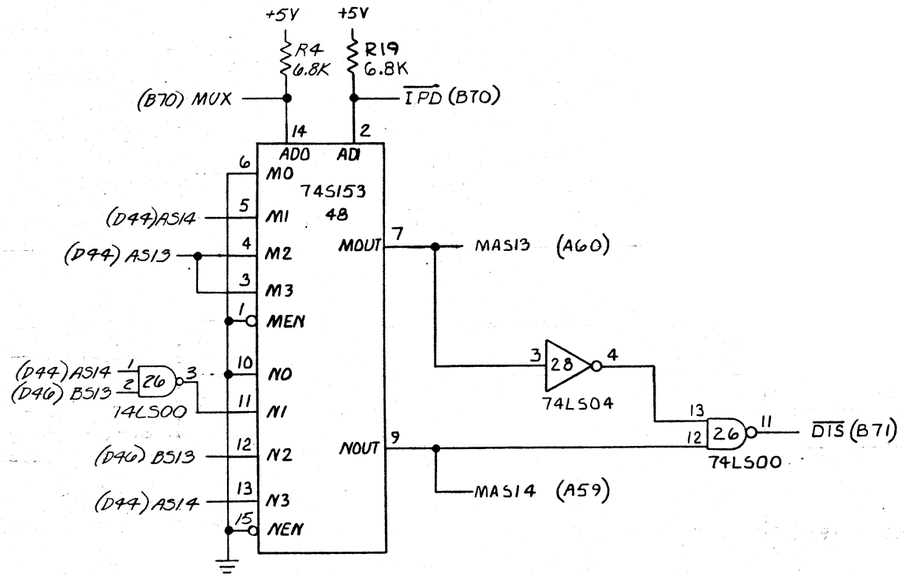


SIZE	DRAWING NO.	REV
D	75-53707-XX	F0

SHT. 7 OF


P2
37
MBIN
63
CLK
74LS08
PUP1 (C63)
CLKP (C61, C62, C63)
74S02
74LS164
42
CLK
R
RS IN
QA
QB
QC
QD
QE
QF
QG
QH
L10 (B64, D61)
L11 (B64, D61)
L12 (B64, D62)
L13 (B64, D62)
N C
(C63) PUP1
MDIS (C53)
74LS08
MDIS (B62, B61)
P2
22
74LS86
L14 (A64)
L15 (A64)
FULL (C62)
+5V
R16 6.8K
R15 6.8K
(D44, C61, B62, C83) PUP
(B70) C5D2
74LS86
PUP1 (A43, C62, C64, D64)
ADDRESS NORMALIZE
LOWER ADDRESS COMPARE
CIN
74S283
39
COUT
(B47) AB10
(B47) AB11
(B47) AB12
(B47) AB13
(D63) L10
(D63) L11
(D63) L12
(D63) L13
74LS04
NA12 (C41, D42, D43, B62)
NA13 (C41, D42, D43, B62)
(C62) L14
(C62) L15
(B47) AB14
(A47) EBA
74S283
40
NA14 (C41, D43, B62)
NA15 (B62)
NC
≥ L (D53, C53)
74S08
(B45) MR15
(A46) MLB
74S00
(C60) MOUT64K
RSIN
74165
59
(D63) L10
(D63) L11
(D63) L12
(D63) L13
(D42) EN4
(D42) EN8
(C42) EN16
(C42) EN32
74LS283
61
CIN
COUT
U12
74LS86
CRG4 (C62, AG1)
ENG4 (C92)
7432
(D63) CLKP
(C62) LOAD
CLK
ALD
QH
NC
74LS20
(D63) CLKP
(C61) CR64
(C63) PUP1
(C62) FULL
74LS74
46
LOAD (C45, C61)
(C63) MDIS1
(D63) CLKP
NC
MOUT64K (D61)
P1
65
P2
38
MBOT
7438
IUR
SIZE UPPER LIMIT COMPARE
(C63) PUP
(B63) NAI2
(B63) NAI3
(B63) NAI4
(A63) NAI5
(D42) EN4
(D42) EN8
(C42) EN16
(C42) EN32
74585
81
MAGNITUDE COMPARATOR
NC NC
CHIP SELECT DECODER
(A59) LMAS12
(A59) LMAS13
(A58) LMAS14
(C49) REF
(B51) TO
74S138
64
G1
G2A
G2B
+5 INT
CS0 (C19, D59, D66)
CS1 (C19, D59, D66)
CS2 (B19, C59, D66)
CS3 (B19, C59, D66)
CS4 (C27, C59, D66)
CS5 (C27, B59, D66)
CS6 (B27, B59, D66)
CS7 (B27, B59, D66)
(D44) AS12
(C71) MAS13
(A46) HOLD
74LS75
47
LMAS12 (B61)
LMAS13 (B61)
N.C
(C71) MAS14
(A46) HOLD
LMAS14 (E61)
CHIP ENABLE DRIVERS
(B49) IPUP
(D49) REFI
(B51) TO
(B51) TI
(C49) REF
(B49) IPUP
74S22
R50 1K
+5V INT
+12 INT
A5T4261
Q13
Q14
Q11
Q12
Q9
Q10
Q7
Q8
R59 10Ω
R58 10Ω
R57 10Ω
R56 10Ω
R55 10Ω
R54 10Ω
R53 10Ω
R52 10Ω
CE0 (C19)
CE1 (C19)
CE2 (B19)
CE3 (B19)
CE4 (C26)
CE5 (C26)
CE6 (B26)
CE7 (B26)
(B60) CS0
(B60) CS1
(B60) CS2
(B60) CS3
(B60) CS4
(A60) CS5
(A60) CS6
(A60) CS7
(C49) REF
74S00
75322
102
100
91
89
87
-02, -03, -04, -06 THRU -13, -17 THRU -23 ONLY
-03, -04, -07, -08, -09, -10, -11, -12, -13, -18 THRU -23 ONLY
-04, -08, -09, -11, -12, -20, -21, -22, -23 ONLY
-04, -08, -09, -11, -12, -23 ONLY
PROPRIETARY RIGHTS NOTICE
THIS DOCUMENT AND INFORMATION THAT IT CONTAINS ARE THE PROPERTY OF COMPUTER AUTOMATION, INC. RIGHTS TO DUPLICATE OR OTHERWISE COPY THIS DOCUMENT AND RIGHTS TO DISCLOSE THE DOCUMENT AND SUCH INFORMATION TO OTHERS AND THE RIGHT TO USE THE INFORMATION CONTAINED THEREIN, MAY BE ACQUIRED ONLY BY WRITTEN PERMISSION SIGNED BY A DULY AUTHORIZED OFFICER OF COMPUTER AUTOMATION, INC.
SIZE D
75-53707-XX
REV F0
SHT. 8 OF
DRAWING NO. 75-53707-XX REV F0

BANKING SELECT MUX



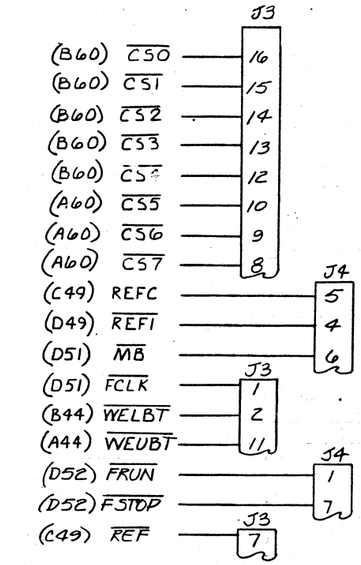
INTERNAL BANKING SWITCH SETTINGS

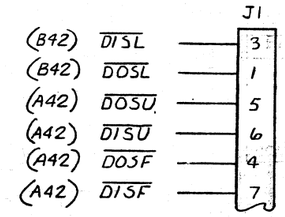
TABLE I

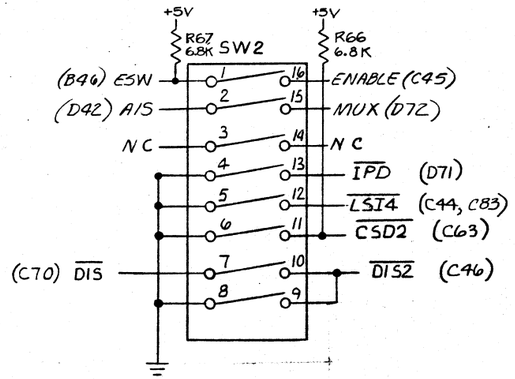
SIGNAL NAME	BS12	A12	BS13	A13	BS14	A14
BANK CONFIG.	SW1-1	SW1-2	SW1-3	SW1-4	SW1-5	SW1-6
2 X 4K	ON	OFF	OFF	ON	OFF	ON
4 X 4K	ON	OFF	ON	OFF	OFF	ON
8 X 4K	ON	OFF	ON	OFF	ON	OFF
2 X 8K	OFF	ON	ON	OFF	OFF	ON
4 X 8K	OFF	ON	ON	OFF	ON	OFF
2 X 16K	OFF	ON	OFF	ON	ON	OFF
ANY SIZE NORM	OFF	ON	OFF	ON	OFF	ON
IPD 1	OFF	ON	OFF	ON	ON	OFF
IPD 2	OFF	ON	OFF	ON	ON	OFF
CSD 1	OFF	ON	OFF	ON	OFF	ON
CSD 2	OFF	ON	ON	OFF	ON	OFF

TABLE 2

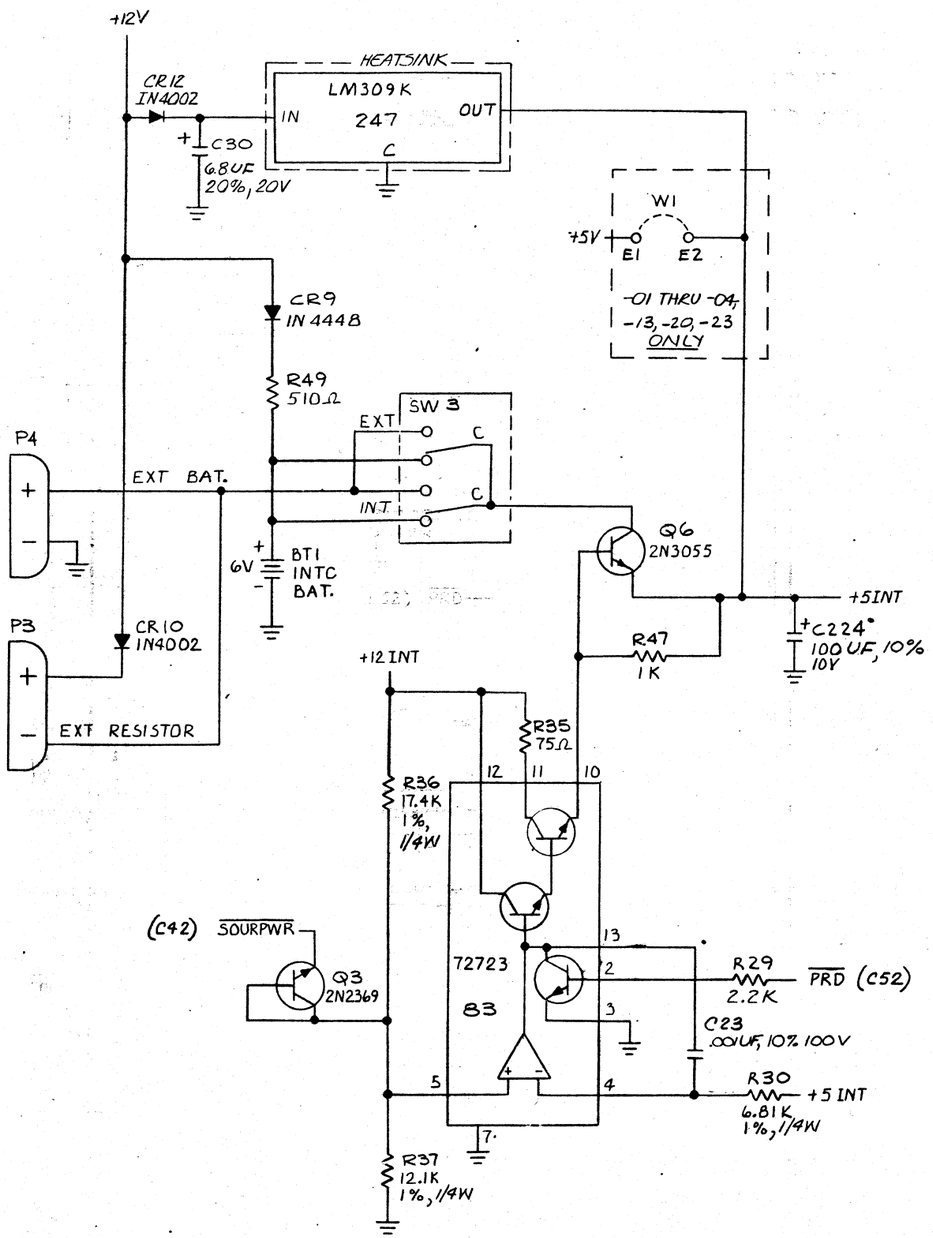
SIGNAL NAME	MUX	IPD-	CSD2-	DIS 2	GND	ESW
BANK CONFIG.	SW2-2	SW2-4	SW2-6	SW2-7	SW2-8	SW2-1
IPD 1	ON	ON	OFF	OFF	ON	ON
IPD 2	ON	OFF	OFF	OFF	ON	ON
CSD 1	OFF	OFF	OFF	ON	OFF	OFF
CSD 2	OFF	OFF	ON	OFF	ON	OFF
ALL OTHER CONFIG'S.	OFF	OFF	OFF	OFF	ON	ON

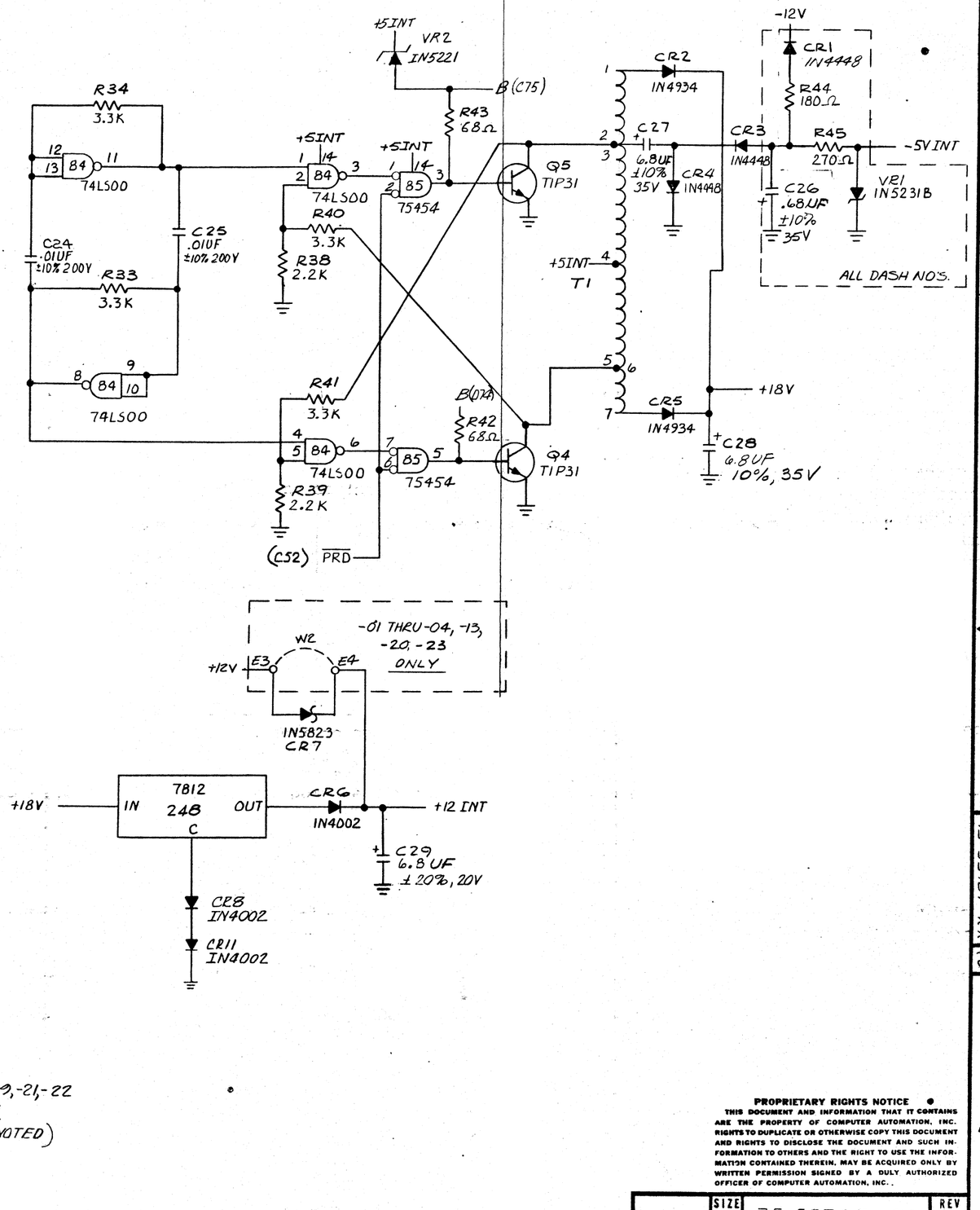






SIZE		REV
D	75-53707-XX	F0
	SHT. 9 OF	



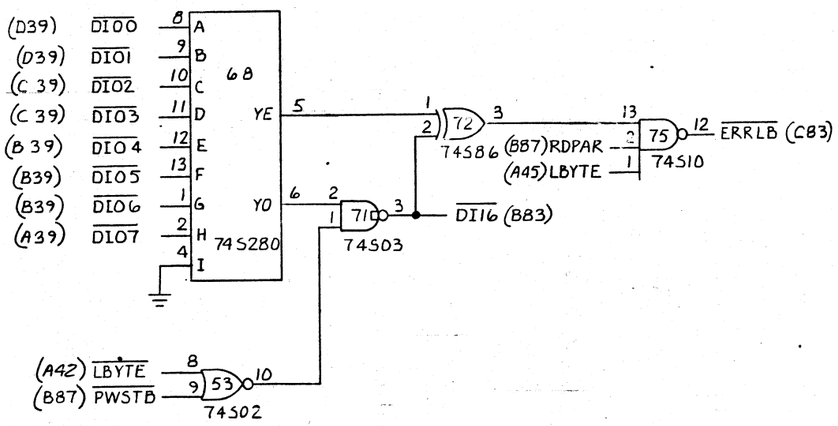


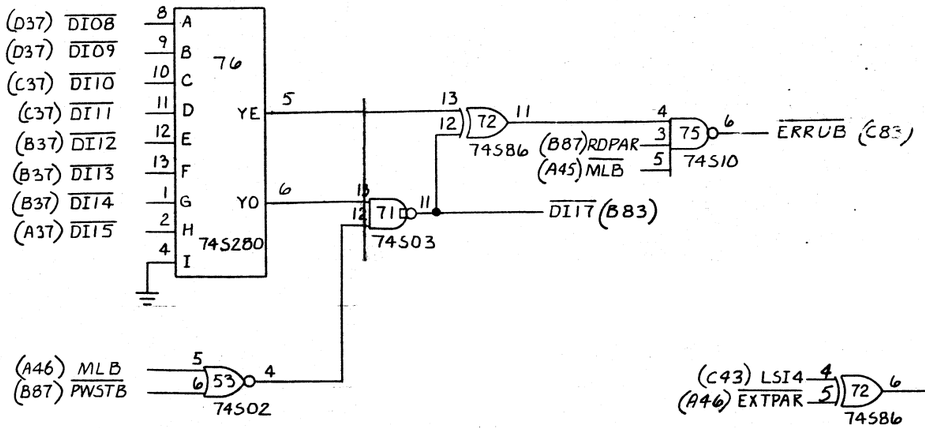
-05 THRU -12, -18, -19, -21, -22 ONLY (EXCEPT AS NOTED)

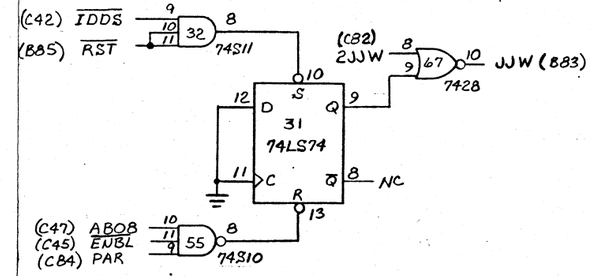
SIZE	75-53707-XX	REV
D		F0
		SHT. 10 OF

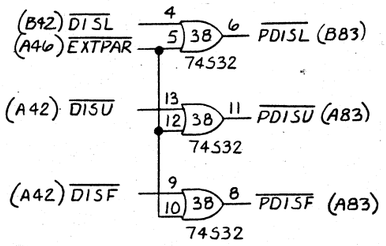
75-53707-XX

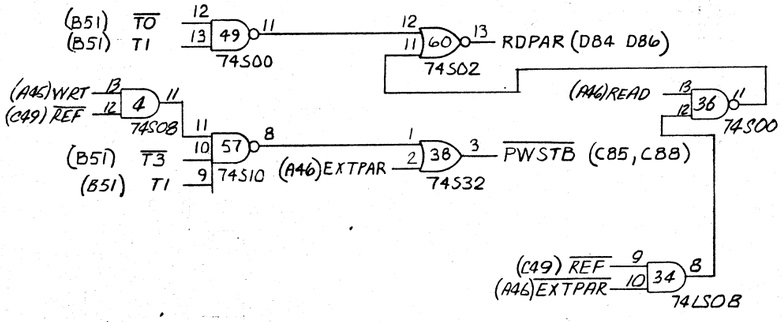
PARITY

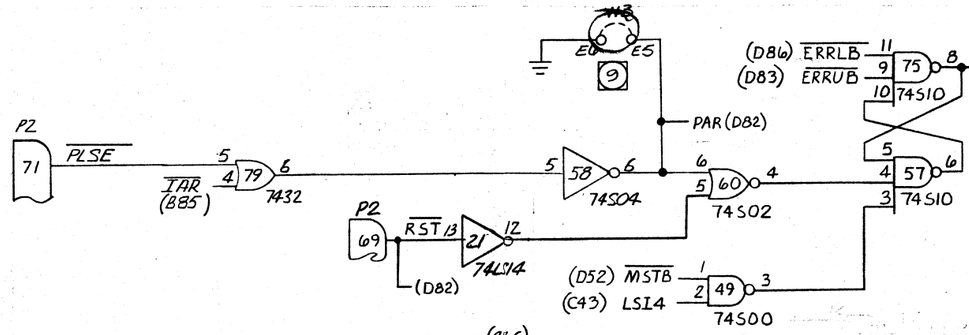


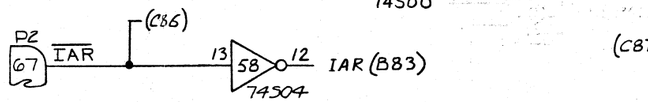


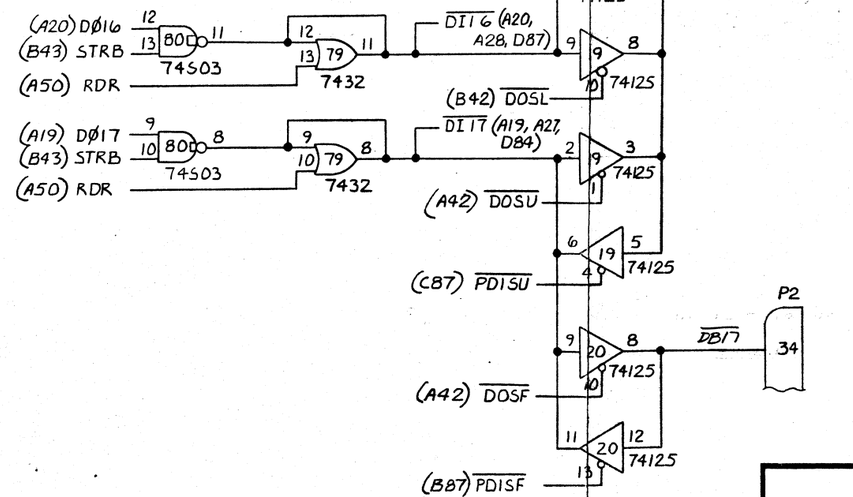








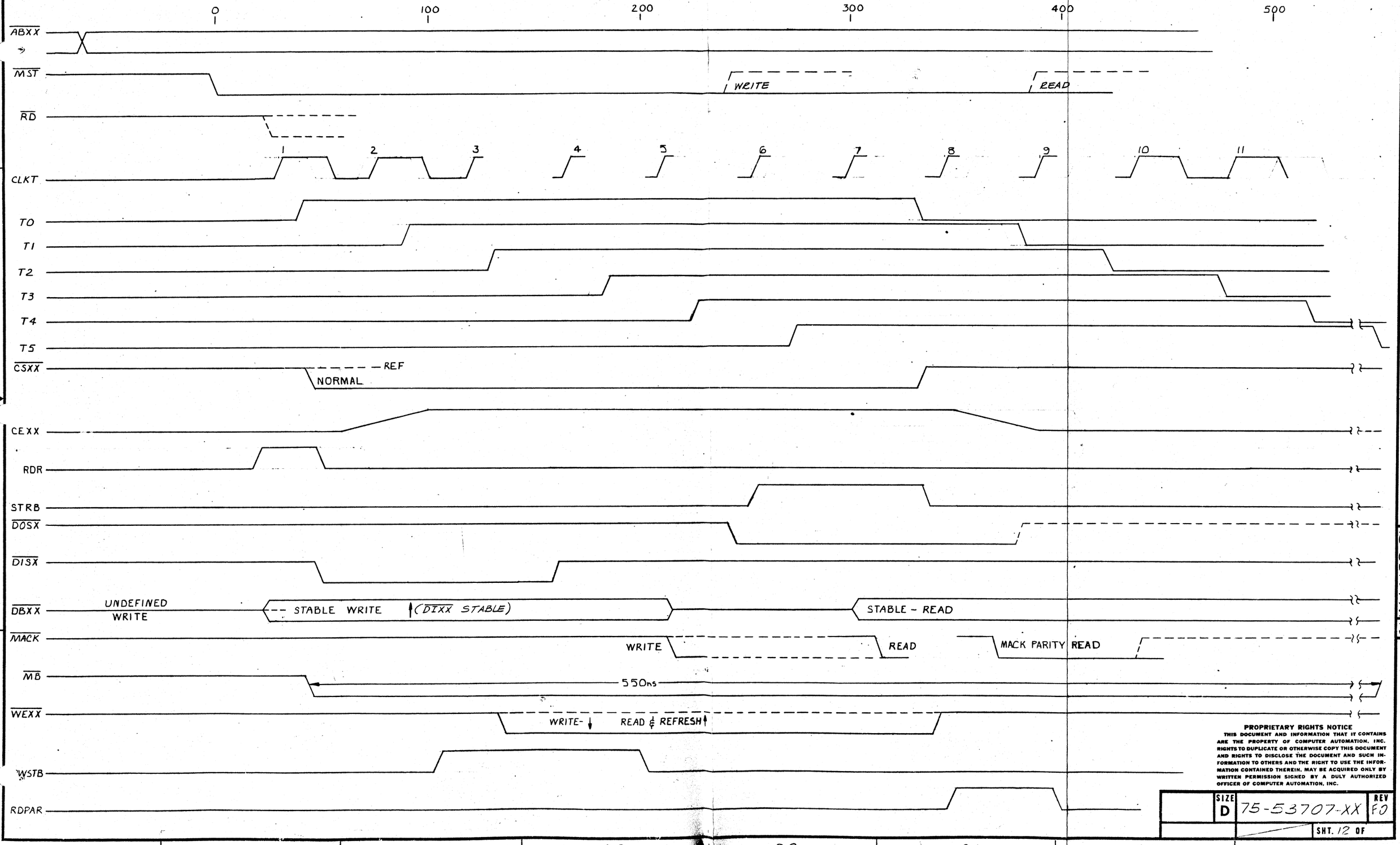




-10,-11,-12,-19,-22
ONLY

SIZE	DRAWING NO.	REV
D	75-53707-XX	F0
	SHT. 11 OF	

TIMING: 550 NS HIGH SPEED, 32 K MOS RAM

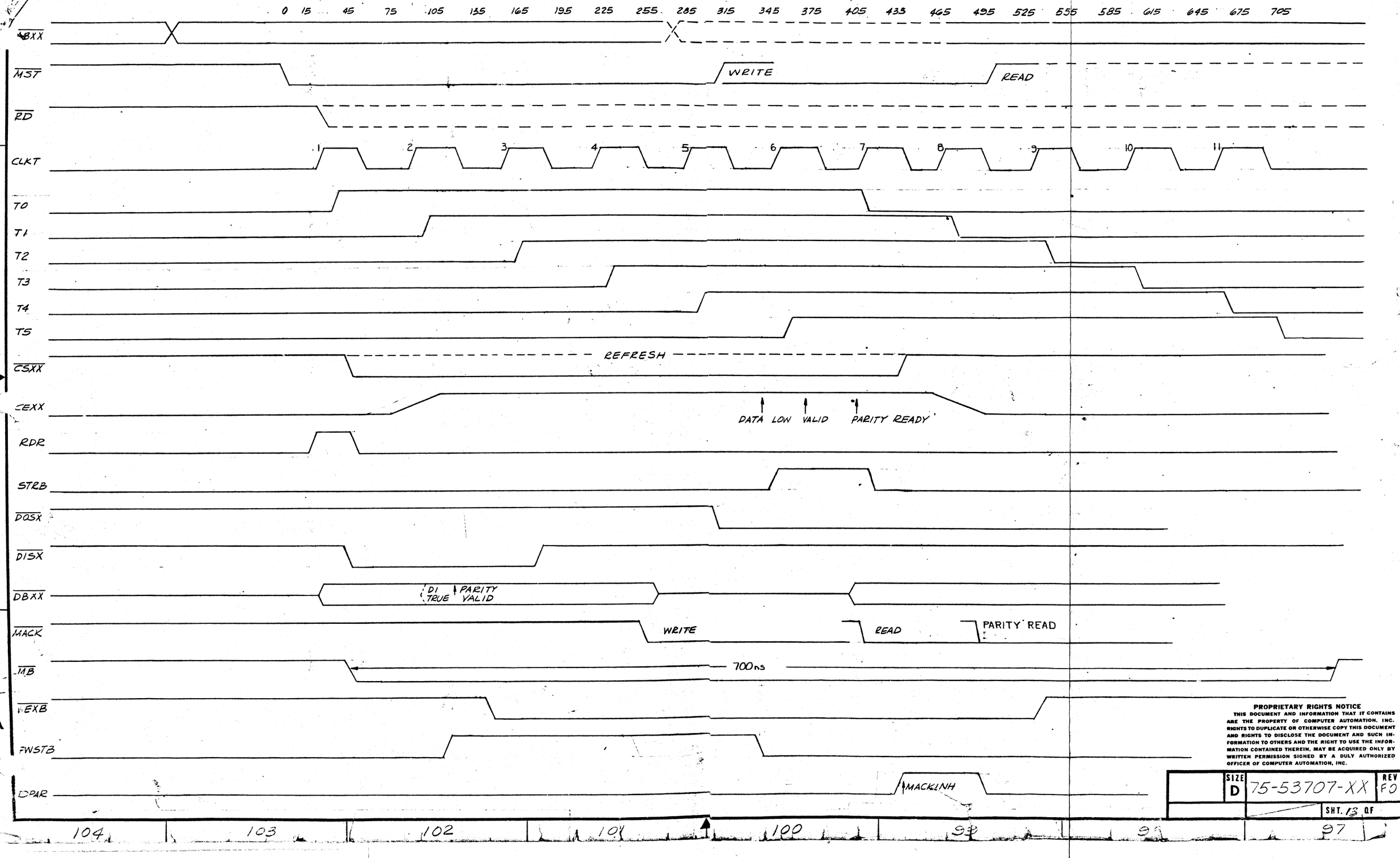


SIZE	DRAWING NO.	REV
D	75-53707-XX	F0

SHT. 12 OF

TIMING: 700 NS MEDIUM SPEED

32 K MOS RAM



SIZE	DRAWING NO.	REV
D	75-53707-XX	F0

SHT. 13 OF

104	103	102	101	100	99	98	97

MNEMONICS DEFINITIONS

A12 to A14	THESE ARE THE SELECTED ADDRESS LINES FROM THE STANDARD MEMORY PATCH THAT WILL BE USED AFTER PASSING THROUGH A LOT OF LOGIC TO SELECT ONE ROW IN THE RAM ARRAY.
AB00- to AB15-	ADDRESS BUSS BITS.
AL-	AUTOLOAD SIGNAL. RECEIVES AND DRIVES THIS LINE IN THE EVENT OF LOST POWER WHEN USING BATTERY BACKUP.
AJ1-AJ2	ADDRESS JUGGLER SIGNALS. THESE SIGNALS CHANGE THE MEMORY SIZE TEMPORARILY DURING THE ADDRESS ALLOCATION SEQUENCE WHEN IT IS INTERLEAVED AND/OR BANKED AS A PRIMARY OR ALTERNATE.
AS12 to AS14	SWITCHED ADDRESS LINES. THESE SIGNALS CAN BE EITHER NORMAL SIGNALS FROM THE COMPUTER ADDRESS BUSS OR BANKING SELECT LINES FOR INTERNAL BANKING.
BS12 to BS14	BANK SELECT LINES. THESE ARE EXTERNALLY CONTROLLED SIGNALS THAT WILL SELECT A ROW IN THE RAM ARRAY WHEN USING INTERNAL BANKING.
CEX	CHIP ENABLE SIGNALS. THIS IS A HIGH VOLTAGE (+12 VDC) SIGNAL USED TO SELECT AND START A ROW OF RAMS IN THE ARRAY.
CLK-	A 1 MHZ FREE RUNNING SIGNAL GENERATED BY THE PROCESSOR.
CLKP-	THE BUFFERED PROCESSOR CLOCK USED IN THE MEMORY ALLOCATION SEQUENCE.
CLKT	MEMORY TIMING CLOCK. THIS IS A GATED OSCILLATOR OUTPUT WHICH DRIVES THE SHIFT REGISTER THAT GENERATES ALL INTERNAL MEMORY TIMING.
CR64	CARRY 64. AN ENABLING SIGNAL USED TO INDICATE PRESENT MEMORY SIZE IS 64K.
CSD2	A SWITCHED SIGNAL INDICATING THE POSITION IS FOR ONE OF THE LSI SPECIAL CONFIGURATIONS.
CSX-	CHIP SELECT X. THESE ARE LOW TRUE SIGNALS THAT SELECT A PARTICULAR ROW IN THE RAM ARRAY.
DB00- to DB17-	DATA BUSS BITS.
DI0- to DI17	MEMORY INTERNAL DATA BUSS BITS. THE INTERNAL BUSS WHERE DATA INPUT FROM THE COMPUTER COMES TO AND WHERE DATA READ FROM THE MEMORY DEVICES WILL COME BEFORE GOING TO THE DATA BUSS.
DIS	DISABLE NOT. A SPECIAL DISABLE FOR CSD THAT STOPS THE MEMORY FROM RESPONDING TO ADDRESS SPACE 16K TO 24K.
DIS2-	DISABLE TWO NOT. A SWITCHED VERSION OF DIS-.
DISL-, DISU-, DISF-	DATA INPUT STROBES. ENABLES THE DATA BUSS RECEIVERS FOR WRITE OPERATIONS.
DO0 to DO17	DATA OUTPUT FROM 4K RAM DEVICES.
DOS	DATA OUTPUT STROBE. THE STROBE USED TO ENABLE THE GATES THAT CONTROL THE OUTPUT DATA DRIVERS.
DOSL-, DOSU-, DOSF	THESE STROBES ENABLE THE OUTPUT DATA DRIVERS DURING A READ CYCLE.
EBA-	EXTRA BIT OF ADDRESS. AN EXTENDED ADDRESS BIT TO ALLOW ADDRESSING OF 64K WORDS OF MEMORY.
EN4 to EN64	MEMORY SIZE ENABLES. THESE SIGNALS SELECT THE SIZE OF MEMORY THAT IS PRESENT ON THE MEMORY CARD. SELECTION IS ON THE STANDARD PATCH AREA ON THE MEMORY.
ENABLE HIGH	A MEMORY ENABLE SIGNAL USED TO ENABLE PRIMARY MEMORY MODULES IN EXTERNALLY BANKED CONFIGURATIONS.
ENABLE LOW	A MEMORY ENABLE SIGNAL USED TO ENABLE ALTERNATE MEMORY MODULES IN EXTERNALLY BANKED CONFIGURATIONS.
ENBL-	A DISABLE SIGNAL TO: 1) DISABLE PRIMARY MEMORY MODULES IN EXTERNALLY BANKED CONFIGURATIONS OR 2) DISABLE A SECTION OF MEMORY FROM RESPONDING IN CSD SPECIAL BANKED CONFIGURATIONS.
ENLO	A SWITCHED ENABLE LOW SIGNAL.
ERRLB, ERRUB	THESE ARE BYTE ERROR SIGNALS ACTIVATED ON PARITY READ ERRORS.
ERROR	THIS IS A LATCHED PARITY ERROR SIGNAL FROM EITHER ERRLB OR ERRUB.
EXEC-	SELECT COMMAND. THIS SIGNAL IS NORMALLY DRIVEN DURING ALL SELECT OR SELECT AND PRESENT INSTRUCTIONS, BUT IS USED BY THE MEMORY TO ALLOW PARITY TO BE GENERATED BY THE MEMORY DRIVING ONTO THE BUSS PARITY DATA BITS DURING A READ MEMORY CYCLE.
EXT BAT	EXTERNAL BATTERY CONNECTION. SNAP TERMINALS ARE PROVIDED OR INCREASING BATTERY BACKUP TIME.
EXT RES	EXTERNAL CHARGING RESISTOR. SNAP TERMINALS ARE PROVIDED TO ADD A POWER RESISTOR TO ALLOW CHARGING OF THE EXTERNAL BATTERY
EXT PAR	THIS IS THE LATCHED EXEC SIGNAL USED BY THE PARITY CIRCUITS TO ALLOW PARITY TO BE GENERATED AND CHECKED EXTERNALLY BY A MEMORY DRIVING DEVICE.
FCLK	FORCE CLOCK. THIS IS A CAPABLE TEST POINT TO FORCE THE TIMING SHIFT REGISTER TO SHIFT INTO NEW STATES.
FULL	THIS SIGNAL INDICATES A LOWER BOUNDARY HAS BEEN RECEIVED VIA THE MBIN LINE.
HOLD-	THIS SIGNAL HOLDS THE ENCODED RAM ARRAY SELECT LINES AS WELL AS AB15-, SLB-, RD- and EXEC- AT T1 AND UNTIL MACK GOES AWAY.
IAR	INTERRUPT ADDRESS REQUEST. PROCESSOR GENERATED SIGNAL TO ALLOW INTERRUPTING DEVICES TO PLACE INTERRUPT ADDRESS ON THE BUSS.
IL1-	THIS IS A HIGH LEVEL INTERRUPT HAVING PRIORITY THIRD TO ONLY POWER FAIL INTERRUPTS AND CONSOLE INTERRUPTS.
INHIBIT	THIS SIGNAL INHIBITS DOS WHEN DATA IN THE RAM IS NOT VALID.
INTER-	INTERLEAVED. THIS SIGNAL SELECTS INTERLEAVED MEMORY OPERATION.
IPD-	THIS IS A SIGNAL USED FOR IPD SPECIAL BANKING CONFIGURATIONS.
IPUP	A PULL-UP RESISTOR TO THE INTERNAL +5 VOLT BUSS.
IUR-	THIS IS THE INTERRUPT REQUEST LINE WHICH IS USED DURING THE ADDRESS ALLOCATION PROCESS TO SIGNAL THE PROCESSOR HOW MUCH MEMORY IS PRESENT.
JJW	THIS IS A CONNECTING SIGNAL WHOSE NAME DOES NOT DESCRIBE ITS FUNCTION, BUT THINKING OF CLEVER MNEMONICS ALL THE TIME IS IMPOSSIBLE. IT JUST GOES TO ALLOW MACKINH OR NOT WITH THE APPROPRIATE CONDITIONS.
L10 to L15	LOWER LIMIT LINES. THESE ARE THE MEMORY LOWER LIMIT LINES RECEIVED BY MBIN.
LBYTE	THIS SIGNAL IS TRUE ON ALL MEMORY OPERATIONS TO CONTROL LOWER BYTE DATA EXCEPT WHEN SELECTING THE UPPER BYTE IN BYTE MODE.
LMAS12 to LMAS14	LATCHED MEMORY ADDRESS SELECT. THESE ARE THE ENCODED ADDRESS LINES WHICH WIL SELECT, WHEN DECODED, ONE OF THE RAM ARRAY ROWS.
LOAD	THIS IS A SIGNAL WHICH LOADS THE PRESENT MEMORY UPPER LIMIT PLUS ONE INTO A SHIFT REGISTER TO SHIFT TO THE NEXT MEMORY AND TO THE PROCESSOR VIA THE MBOT AND IUR LINES RESPECTFULLY
LSB	LEAST SIGNIFICANT BIT. FOR NORMAL MEMORY OPERATION THE LSB IS AB00 BUT WHEN INTERLEAVED AB00 IS AN ODD/EVEN CONTROL BIT AND LSB IS DRIVEN BY MRE OR THE MOST SIGNIFICANT ADDRESS BIT
LS14	THIS IS THE NEW SERIES DESIGNATION FOR THE PI PRODUCT.
MAXX-, MAXXL-, MAXXU-	THESE ARE THE BUFFERED RAM ARRAY ADDRESS DRIVERS. THE UPPER AND LOWER DESIGNATION REFER TO EACH 16K WORD HALF OF THE ARRAY.
MACK-	MEMORY ACKNOWLEDGE. SIGNAL TO THE PROCESSOR THAT INDICATES DATA IS AVAILABLE (READ CYCLE) OR DATA HAS BEEN REGISTERED (WRITE CYCLE).
MACKI-	THIS IS THE MEMORYS OWN ACKNOWLEDGE SIGNAL USED INTERNALLY WHICH IS THEN BUFFERED TO FORM MACK-.
MACKINH-	MACK INHIBIT. THIS SIGNAL DISABLES MACK IN THE EVENT OF A PARITY ERROR WHEN THE INTERNAL CHECKING IS DONE BY THE MEMORY.
MANDM-	A FORMING OF MDIS AND MACKI- SIGNALS USED TO DISABLE THE MEMORY FROM RESPONDING DURING POWER FAIL CONDITIONS OR TO NEW MEMORY CYCLES UNTIL THE PREVIOUS CYCLE IS CLEARED. ITS ALSO A POPULAR CANDY FOR KIDS.
MAS13, MAS14	MULTIPLEXED ADDRESS SELECT. THESE SIGNALS ARE USED FOR INTERNALLY BANKED CONFIGURATIONS WHICH HAVE SPECIAL APPLICATIONS, I.E., CSD, IPD.
MB-	MEMORY BUSY. THIS SIGNAL INDICATES A MEMORY HAS BEGUN A MEMORY CYCLE AND CANNOT BE DISTURBED UNTIL IT'S FINISHED.
MBIN	MEMORY BOUNDARY IN. THE MEMORY MODULES LOWER LIMIT IS SEND IN ON THIS LINE FROM EITHER A PROCESSOR OR LOWER ADDRESS MEMORY MODULE.
MBOT	MEMORY BOUNDARY OUT. THIS SIGNAL IS THE NEXT MEMORY MODULES LOWER LIMIT WHICH IS FORMED FROM THE PRESENT MODULES UPPER LIMIT PLUS ONE.
MDIS-	MEMORY DISABLE. A PROCESSOR GENERATED SIGNAL USED WHEN SYSTEM POWER IS INTERRUPTED TO PREVENT SPURIOUS MEMORY CYCLES.
MDISI-	A TTL BUFFERED MDIS- SIGNAL.
MLB	MEMORY LOWER BYTE. THIS IS THE REGISTERED SLB SIGNAL WHEN TRUE IN BYTE MODE WILL SELECT THE LOWER BYTE OF DATA.
MOUT64K	THIS SIGNAL INDICATES THAT A MEMORY MODULE UPPER LIMIT PLUS ONE IS 64K AND BECOMES THE LEAST SIGNIFICANT BIT FOR THE MBOT DATA STREAM.
MR15-	THIS IS THE REGISTERED AB15 SIGNAL WHICH SELECTS BYTE MODE OPERATION.
MRE	THIS SIGNAL IS THE MOST SIGNIFICANT BIT OF THAT WILL ADDRESS A MEMORY MODULE.
MST-	MEMORY START. THIS IS THE GO SIGNAL FOR THE MEMORY BOARDS.
MSTB-	THIS IS A TTL BUFFERED MST- SIGNAL.
NA12 to NA15	NORMALIZED ADDRESS BITS. THESE BITS ARE FORMED FROM A SUBTRACTION OF THE MEMORY LOWEE LIMIT FROM THE ADDRESS BUSS VALUE. THEY ARE USED FOR UPPER LIMIT COMPARISON AND NA12 TO NA14 WILL BE DECODED TO SELECT A ROW IN THE RAM ARRAY.
ODD-	THIS SIGNAL SELECTS AN ODD ADDRESS MODULE WHEN INTERLEAVED.
PDISL-, PDISU-, PDISF-	PARITY DATA INPUT STROBES. THESE ARE THE SAME AS THE DISX SIGNAL EXCEPT WHEN EXTERNAL PARITY BITS ARE TO BE READ THEY ENABLE THE PARITY BIT RECEIVERS.
PLSE-	THIS IS A PROCESSOR OPERATED SIGNAL WHICH IS USED AS THE CONTROL FOR I/O INSTRUCTIONS.
PRD-	POWER DOWN. THIS SIGNAL INDICATES THAT POWER IS DOWN IN A SYSTEM AND THAT THE MEMORY IS TO BE DISABLED FROM OPERATING.
PUP, PUP1	THESE ARE LEVEL SIGNALS PULLED UP TO +6 VOLTS WITH RESISTORS.
PWSTB-	PARITY WRITE STROBE. THIS SIGNAL IS USED TO WRITE INTERNAL PARITY. IT IS TIMED TO WAIT FOR INTERNAL PROPAGATION DELAYS AND THEN ALLOW SETTING OF THE DATA LATCHES (DI16 or DI17).
RD-	READ/WRITE LINE. LOW TRUE PROCESSOR OR DMA CONTROLLER DRIVER LINE LOW TRUE FOR READ OPERATION.
RDPAR	READ PARITY. THIS SIGNAL STROBES THE EXCLUSIVE OR GATE FOR A PARITY ERROR. IF THE OUTPUT IS HIGH A PARITY ERROR (LOW, TRUE) WILL OCCUR.
RDR	RESET DATA REGISTER. THIS SIGNAL PRESETS THE DATA REGISTERS HIGH AT THE BEGINNING OF A MEMORY CYCLE AND AT THE END OF A MEMORY CYCLE.
READ	THE REGISTERED AND BUFFERED RD-LINE.
REF-, REFI-	REFRESH. THESE LINES INDICATE A REFRESH CYCLE IS IN PROGRESS WHEN THEY ARE LOW.
REFC-	REFRESH CLOCK. THIS SIGNAL OCCURS APPROXIMATELY EVERY 25 μSECONDS TO SIGNAL A REFRESH CYCLE IS DUE.
REF REQ-	REFRESH REQUIRED. THIS SIGNAL BECOMES LOW TRUE WHEN THE MEMORY IS NOT BUSY AND A REFRESH CLOCK OCCURS. IT THEN FORCES SIGNAL REF- TO BECOME TRUE AND HENCE A REFRESH CYCLE.
RFA00 to RFA05	REFRESH ADDRESS. THESE SIGNALS COME FROM THE REFRESH COUNTER TO SUPPLY THE ROW ADDRESS FOR THE 4K RAM ICS DURING REFRESH OPERATIONS.
RST-	MASTER RESET. THIS IS A COMPUTER GENERATED SIGNAL USED TO RESET THE PARITY ERROR LATCH.
SOURPWR-	SOURPOWER. THIS SIGNAL INDICATES THE +5 INT VOLTAGE HAS DROPPED BELOW 4.7 VOLTS INDICATING THE BATTERY CAN NO LONGER SUPPLY ENOUGH POWER FOR THE BATTERY BACKUP UNIT.
STOP-	THE STOP SIGNAL INDICATES THAT TIMING PHASES T5 AND T4- HAVE ARRIVED WHICH IS AN END OF CYCLE.
STRB	THIS SIGNAL READS DATA FROM THE RAMS BY ENABLING THE GATE FEEDING THE DATA LATCH.
T0- to T5-	INTERNAL MEMORY TIMING SIGNAL. THESE SIGNALS ARE DECODED TO SET UP ALL MEMORY TIMING.
TEOC-	TIME END OF CYCLE. THIS SIGNAL RESETS THE 6 BIT SHIFT REGISTER USED IN GENERATING THE MEMORY TIMING AT THE END OF A MEMORY CYCLE.
U12 to U15	UPPER LIMIT. THESE SIGNALS RESULT FROM ADDING THE MEMORY SIZE TO THE MEMORY MODULES LOWER LIMT.
WELB-, WEUB-	WRITE ENABLE LOWER AND UPPER BYTES. THESE ARE THE READ/WRITE LINES TO THE MEMORY DEVICES.
WRT	THIS IS THE REGISTERED-INVERTED RD- LINE WHEN HIGH INDICATES A WRITE CYCLE IS TO OCCUR.
LMIT-	THIS IS A SIGNAL TO INACTIVATE THE MEMORY WHEN INTERLEAVED SO IT WILL ONLY RESPOND TO THE PROPER ODD OR EVEN ADDRESS.
+6INT	THE INTERNAL +5 VOLT LINE SEPARATE FROM THE NORMAL +5 LINE. WHEN BATTERY BACKUP SYSTEM IT IS GENERATED FROM A +6 VDC BATTERY AND REGULATING CIRCUITS.
+12 INT	THIS IS THE RAM POWER BUSS WHICH IS GENERATED BY THE D.C. TO D.C. CONVERTER AND REGULATORS ON BATTERY BACKEDUP BOARDS.
-5VINT	THIS IS A RAM SUPPLY VOLTAGE THAT IS GENERATED BY THE D.C. TO D.C. CONVERTER OR FROM THE -12VDC POWER SOURCE.
≥L	GREATER THAN OR EQUAL TO THE LOWER LIMITS. THIS SIGNAL BECOMES TRUE WHEN THE ADDRESS ON THE BUSS IS GREATER THAN OR EQUAL TO THE MEMORY MODULE LOWER LIMIT.
<U	LESS THAN UPPER LIMIT. WHEN THE ADDRESS ON THE BUSS IS LESS THAN THE MEMORY UPPER LIMIT THIS SIGNAL BECOMES TRUE.