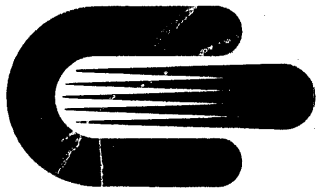


CLEARPOINT INC.

# Q-RAM 11

# USER INFORMATION MANUAL

106 South Street
Hopkinton, MA 01748
(617) 435-5395
Telex: 298281

# TABLE OF CONTENTS

TABLES



APPENDIXES

# CHAPTER 1

# GENERAL DESCRIPTION AND SPECIFICATIONS

## 1.1 INTRODUCTION

This manual supplies user information for the Q-RAM 11 family of memory modules. Q-RAM 11 modules (see Table 1) provide high density, low cost per bit storage for systems which utilize the Digital Equipment Corporation (hereafter referred to as DEC) Q-BUS. 64K MOS RAMS are used as individual storage devices to provide up to 1/2 mbyte on a single dual-height board. Features available on Q-RAM 11 are:

- Up to 1/2 MB memory capacity
- Jumper selectable 18 or 22 bit address
- Parity generation and checking on board
- Complete DEC* software-hardware compatable, parity control and status register on board locatable at any of 8 assigned I/O page address
- Battery backup support
- Single 5 volt power supply
- Starting address programmable at any 16K
- Parity error LED provides visual indication of board failure

Table 1 Q-RAM 11 Products

| Designation | Description |
|---|---|
| Q-RAM 11 | 512 KB board with parity |
| Q-RAM 11-1 | 512 KB board no parity |
| Q-RAM 11-2 | 256 KB board with parity |
| Q-RAM 11-3 | 256 KB board no parity |

* Registered trademark of Digital Equipment Corporation

## 1.2 GENERAL DESCRIPTION

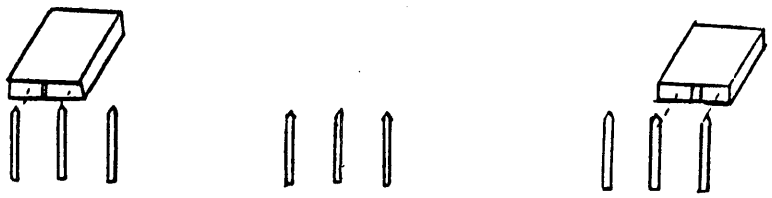
The Q-RAM 11 is a single dual-height memory module which interfaces to the LSI-11 Q-BUS. All timing and control logic for the memory, refresh circuitry, parity control, and status register are contained on board.

The MOS memory array consists of up to four rows of 65,536 X 1 bit dynamic RAM devices with 18 devices per row. Each row will accept 65,536 18 bit words consisting of (two) eight bit bytes and two parity bits (one per byte). Circuitry for refresh of the MOS memory devices is provided on board and operates transparently to the user.

The Q-RAM 11 module's starting address is selectable using program plugs P0 to P6 (see figure 1 and 2) to any 16K boundary within the Q-BUS 22 or 18 bit address space. Program plug P11 is used to select 18 bit or 22 bit addressing. BDAL 18, BDAL 19, BDAL 20, and BDAL 21 are ignored if 18 bit addressing is selected.

The module will not respond to BBS7 transfers to allow the top 4K addresses to be reserved for I/O peripherals. P16 is provided on board which allows the user to reclaim 2K of the I/O page for system memory (see figure 2).

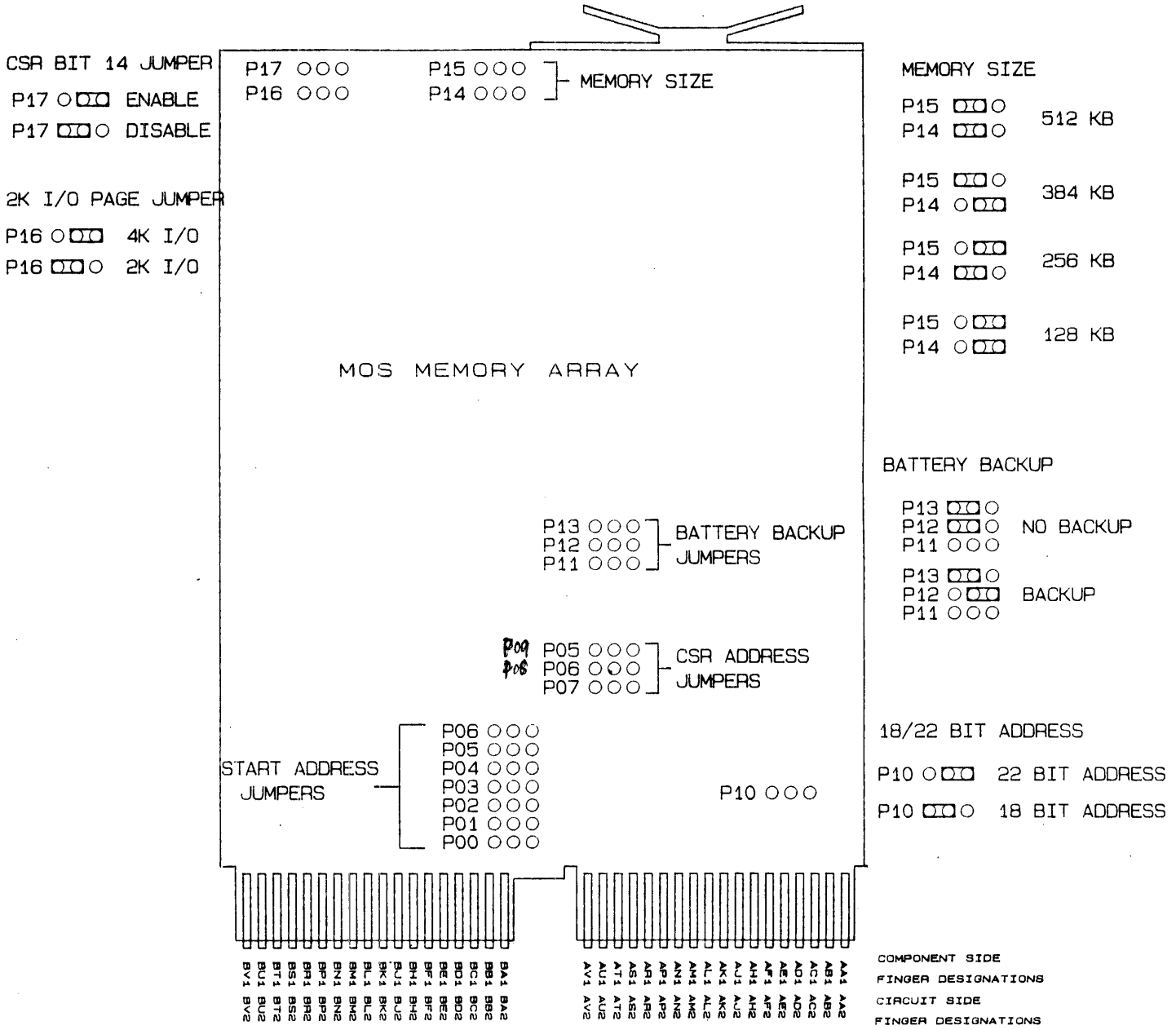
FIGURE 1 PROGRAM PLUG DESCRIPTION



ON OUT OFF

When holding board fingers down, program plugs positioned to left are defined as "ON." Those positioned to right are "OFF."

**FIGURE 2 Q-RAM 11 PROGRAM PLUG DESCRIPTION**




**MOS MEMORY ARRAY**

When any byte of data is written to Q-RAM 11 boards which contain parity, a parity bit is generated which is stored along with the byte of data in the memory array. Whenever a byte of data is read the parity logic checks it against the stored parity bit. If parity is bad, an error has occurred and data is assumed to be bad.

In order to utilize the parity generation and checking circuitry in the Q-RAM 11, a control and status register is provided on board which is both hardware and software compatable with LSI-11 systems.

The control and status register is used to enable the board to interrupt if an error has occurred, latch the upper address bits of the location with bad data, set the parity error flag on error, and force bad parity writing for diagnostic purposes.

## 1.3 BACKPLANE PIN UTILIZATION

Table 2 contains backplane power pins required for Q-RAM 11. Table 3 designates pins used for other signals. Board finger designations shown in figure 2 are equivalent to backplane pin designations.

Table-2 Backplane Power Pins Required

| Voltage | Pin |
|---|---|
| +5 normal | BV1 |
| | AA2 |
| | BA2 |
| ground | AT1 |
| | BT1 |
| | AC2 |
| | BC2 |
| +5 battery (if used) | AV1 |
| +5 battery spare (if used) | AS1 |
| | AE1 |

Table-3 Backplane I/O Signal Pins

| Signal | Pin |
|---|---|
| AC1 | BDAL 16 L |
| AD1 | BDAL 17 L |
| BA1 | BDCOK H |
| BC1 | BDAL 18 L |
| BD1 | BDAL 19 L |
| BE1 | BDAL 20 L |
| BF1 | BDAL 21 L |
| AE2 | BDOUT L |
| AF2 | BRPLY L |
| AH2 | BDIN L |
| AJ2 | BSYNC L |
| AK2 | BWTBT L |
| AM2 | BIAKI L |
| AN2 | BIAKO L |
| AP2 | BBS7 L |
| AR2 | BDMGI L |
| AS2 | BDMGO L |
| AU2 | BDAL 00 L |
| AV2 | BDAL 01 L |
| BE2 | BDAL 02 L |
| BF2 | BDAL 03 L |
| BH2 | BDAL 04 L |
| BJ2 | BDAL 05 L |
| BK2 | BDAL 06 L |
| BL2 | BDAL 07 L |
| BM2 | BDAL 08 L |
| BN2 | BDAL 09 L |
| BP2 | BDAL 10 L |
| BR2 | BDAL 11 L |
| BS2 | BDAL 12 L |
| BT2 | BDAL 13 L |
| BU2 | BDAL 14 L |
| BV2 | BDAL 15 L |

## 1.4 SPECIFICATIONS

| CHARACTERISTICS | SPECIFICATIONS |
|---|---|
| memory device type | MOS dynamic ram (65,536 X 1) |
| read access time | 225 ns typ. |
| write access time | 50 ns typ. |
| memory cycle time | 450 typ. |
| operating temperature | 0 to +65 C |
| storage temperature | -40 to +85 C |
| relative humidity | 0 to 90% (non-condensing) |
| voltages required | +5V ±5% pins BU1, AA2, BA2 |
| battery backkup voltage | +5V ±5% pins AV1, AS1*, AE1* |
| +5V operating current | 1.4 amp typ. |
| +5V standby current | 1.4 amp typ. |
| +5V battery backup current | .9 amp typ. |

* optional spares available on backplane

# CHAPTER 2

# HARDWARE INSPECTION, INSTALLATION, AND CHECKOUT

## 2.1 INTRODUCTION

This chapter provides information for configuring the Q-RAM 11 programmable plug options prior to system installation followed by installation and checkout procedures.

## 2.2 CONFIGURING THE Q-RAM 11 PROGRAM PLUGS

Figure 2 provides the locations of the various Q-RAM 11 option jumpers and Figure 1 illustrates how they are used. The module should be inspected prior to installation to assure that it has been properly configured. Sections 2.3 through 2.6 describe the various Q-RAM 11 program plug options.

## 2.3 ADDRESSING OPTIONS

Q-RAM 11 addressing logic is capable of either 22 or 18 bit operation. P10 is used to select the desired addressing mode as follows:

| | |
|---|---|
| P10 - ON | 18 bit address mode |
| P10 - OFF | 22 bit address mode |

BDAL 18, BDAL 19, BDAL 20, and BDAL 21 are ignored if 18 bit addressing mode is selected and the board may not be configured to respond to addresses above 128K.

The memory starting address may be programmed at any 16K boundary using jumpers P0 through P6. Depending on the size of the board, the memory will utilize up to 262,144 contiguous word addresses in the address space beginning at

the selected starting address. Q-RAM 11 board sizes are always multiples of 64 KW (see section 2.4).

To program the starting address of the memory, BDAL 21 through BDAL 15 must be reflected by the following program plug configurations:

| | |
|---|---|
| BDAL 21 1 | P6 ON |
| BDAL 21 0 | P6 OFF |
| BDAL 20 1 | P5 ON |
| BDAL 20 0 | P5 OFF |
| BDAL 19 1 | P4 ON |
| BDAL 19 0 | P4 OFF |
| BDAL 18 1 | P3 ON |
| BDAL 18 0 | P3 OFF |
| BDAL 17 1 | P2 ON |
| BDAL 17 0 | P2 OFF |
| BDAL 16 1 | P1 ON |
| BDAL 16 0 | P1 OFF |
| BDAL 15 1 | P0 ON |
| BDAL 15 0 | P0 OFF |

Appendix A may be used to determine starting addresses if the Q-RAM 11 is to be placed over existing resident memory. Table 4 may be used as an illustration of the above described formula. Table 4 may also be used to directly configure systems with multiple Q-RAM 11 2/3 MB boards.

Table-4 Multiple Q-RAM 11 Starting Addresses

| BRD | STARTING ADDRESS | | | | | | | PLUG CONFIGURATIONS | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| # | A21 | A20 | A19 | A18 | A17 | A16 | A15 | P6 | P5 | P4 | P3 | P2 | P1 | P0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | OFF | OFF | OFF | OFF | OFF | OFF | OFF |
| 2 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | OFF | OFF | ON | OFF | OFF | OFF | OFF |
| 3 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | OFF | ON | OFF | OFF | OFF | OFF | OFF |
| 4 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | OFF | ON | ON | OFF | OFF | OFF | OFF |
| 5 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | ON | OFF | OFF | OFF | OFF | OFF | OFF |
| 6 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | ON | OFF | ON | OFF | OFF | OFF | OFF |
| 7 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | ON | ON | OFF | OFF | OFF | OFF | OFF |
| 8 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | ON | ON | ON | OFF | OFF | OFF | OFF |

The BBS7 signal is used during the address portion of a data transfer cycle on the Q-BUS. It indicates that the bus master is requesting a data transfer with one of the I/O devices in the 4K I/O page space. BBS7 is asserted whenever and I/O page transfer is requested. The memory board should ignore all transfers requested with the I/O space. If, however, there are few peripherals on the system and it is desired by the user to reserve only 2K of the I/O page space, plug P16 may be used.

| | |
|---|---|
| P16 OFF | Normal 4K I/O Page |
| P16 ON | Reserve Only 2K I/O Page |

## 2.4 BOARD SIZE CONFIGURATION PLUGS

Plugs P14 and P15 are used to configure the board size. Q-RAM 11 boards have up to four rows of 65,536 X 1 bit dynamic RAM devices with 18 devices per row. Each row will accept 65,536 (64K) 18 bit words. A Q-RAM 11 may have 1, 2, 3, or 4 rows of memory chips corresponding to 64K, 128K, 192K, or 256K words respectively. P14 and P15 must be configured to match the size of the memory shown in Table 5.

Table 5 Memory Size Jumpers

| Board memory capacity | P14 | P15 |
|---|---|---|
| 64K words | OFF | OFF |
| 128K words | ON* | OFF |
| 192K words | OFF | ON* |
| 256K words (1/2 MB) | ON* | ON* |

*Plugs may be left out for "ON" configurations of P14 and P15.

## 2.5 CSR OPTION PLUG CONFIGURATIONS

The parity control and status register (hereafter referred to as CSR) has an I/O page address in the top 4K of memory. This address may be any one of eight specified locations reserved by DEC for this purpose. Program plugs P9, P8, and P7 are used to select one of the reserved addresses. Table 6 illustrates ;the use of these plugs. Note that each memory board used in a system must be configured to a different address.

Table 6 CSR Address Selection

| CSR Address | P9 | P8 | P7 |
|---|---|---|---|
| 772100 | ON | ON | ON |
| 772102 | ON | ON | OFF |
| 772104 | ON | OFF | ON |
| 772106 | ON | OFF | OFF |
| 772110 | OFF | ON | ON |
| 772112 | OFF | ON | OFF |
| 772114 | OFF | OFF | ON |
| 772116 | OFF | OFF | OFF |
| No CSR or Parity* | OUT | OUT | OUT |

*To disable parity, remove P9, P8, P7 plugs

For software which requires bit 14 of the CSR to be read only and always 0, P17 is provided:

| | | |
|---|---|---|
| P17 | OFF | CSR bit 14 may be set |
| P17 | ON | CSR bit 14 always 0 |

## 2.6 BATTERY BACKUP OPTION PLUGS

The MOS memory, unlike core memory, requires the 5 volt supply to retain data. If the 5V power is removed from the board, system memory data is lost.

The battery backup option is used if battery power is available to maintain system memory data during power failures. Battery backup 5V must be available on backplane pin AV1. AS1 or AE1 may be used as an additional battery backup 5 input pin. Table 7 shows the various configurations of the battery backup mode select plugs P13, P12, and P11.

Table 7 Battery Backup Mode Options

| Battery Backup Mode | P13 | P12 | P11 |
|---|---|---|---|
| No Backup | ON | ON | OUT |
| Battery Backup +5 AV1 (AS1, AE1 unused) | OFF | OFF | OUT |
| Battery Backup +5 AV1, AS1 | OFF | OFF | ON |
| Battery Backup +5 AV1, AE1 | OFF | OFF | OFF |

## 2.7 INSTALLATION PROCEDURE

The following procedure should be followed when a Q-RAM 11 board is received:

1. Visually inspect the module to make sure that it has arrived in good condition.

2. Set up program plug options for required operation.

3. Verify that the required power connections are available on the backplane (see Table 2).

4. Power down the system. Make sure that the system is powered off before plugging in a module.

5. Plug the module into the Q-BUS. Memories should installed in sequential slots following the CPU. Make sure that the module is not being inserted backwards. The component side must face in the same direction as other modules in the system.

6. Power up the system and run any DEC memory diagnostic as an initial test. If available, use the following diagnostics.

   MAINDEC-11 CUMSA (22 bit system diagnostic)
   MAINDEC-11 CZKMA (18 bit system diagnostic)

# CHAPTER 3

# CSR DESCRIPTION

## 3.1 INTRODUCTION

When any byte is written to Q-RAM 11 boards with parity option, a parity bit is generated which is stored along with the byte of data in the memory array. WHenever a byte of data is read, the parity logic checks it against the stored parity bit. If parity is bad, an error has occurred and data is assumed to be bad.

In order for software to utilize the parity generation and checking circuitry in the Q-RAM 11, a control and status register (CSR) is provided.

The CSR is assigned an address in the I/O page (see Table 6) which may be accessed by software. When a parity error is detected, the upper address bits of the bad memory location (A11 to A21) are latched in the CSR. Control bits are provided in the CSR to enable interrupt on error and write of bad parity for diagnostic purposes.

## 3.2 CSR BIT ASSIGNMENT

The CSR is a 16 bit register located in the I/O page. The function of the 16 bits in the CSR are as follows:

Bit 0 — Parity Error Interrupt Enable

If set to 1, the memory board will interrupt the processor on error, by setting bits BDAL 17 and BDAL 16 along with the data bits BDAL 0 to BDAL 15. This will result in an LSI-11 processor trap to location 114. BUS INIT clears this bit.

Bit 1 UNUSED

Bit 2 Write Wrong Parity

If this bit is set to 1, any word or byte written to the array will be stored along with an incorrect parity bit. This is for maintenance purposes. It enables diagnostics to check the boards ability to detect parity errors and interrupt when enabled. This bit is cleared by BUS INIT.

Bit 3 UNUSED

Bit 4 UNUSED

Bits 5 - 11 Latch Address Bits

When a parity error is detected, the upper address bits of the failing location are latched. These bits are not cleared by BUS INIT, but are writeable, as well as readable. When an error is detected, address bits 11 to 21 are displayed in these bits. Since there are only 7 bits and there are 11 latched address bits, they are multiplexed. Bit 14, in the CSR, controls which of the latched address bits are on display (see Table 8).

Bit 12 UNUSED

Bit 13 UNUSED

Bit 14 — Extended CSR Read Enable

(See Table 8) This bit is used to multiplex the extended latched address bits A18 to A21 into the CSR bits 5 to 11. This bit is cleared by BUS INIT. Program plug P17 may be used to disable setting of bit 14. If P17 is on, CSR bit 14 is always 0.

Bit 15 — Parity Error Flag

This bit is set if a parity error is detected and remains set until cleared by being written or by BUS INIT.

Table 8 CSR Bits 5 to 11

| CSR Bit | If CSR Bit 14=0 | If CSR Bit 14=1 |
|---|---|---|
| 05 | Latched A11 | Latched A18 |
| 06 | Latched A12 | Latched A19 |
| 07 | Latched A13 | Latched A20 |
| 08 | Latched A14 | Latched A21 |
| 09 | Latched A15 | 0 |
| 10 | Latched A16 | 0 |
| 11 | Latched A17 | 0 |

APPENDIX A

MEMORY STARTING ADDRESS CHART

| Resident Memory in K Words | Starting Address A21 | A20 | A19 | A18 | A17 | A16 | A15 |
|---|---|---|---|---|---|---|---|
| 0K | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 16K | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 32K | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 48K | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| 64K | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 80K | 0 | 0 | 0 | 0 | 1 | 0 | 1 |
| 96K | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| 112K | 0 | 0 | 0 | 0 | 1 | 1 | 1 |
| 128K (1/4 MB) | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 144K | 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| 160K | 0 | 0 | 0 | 1 | 0 | 1 | 0 |
| 176K | 0 | 0 | 0 | 1 | 0 | 1 | 1 |
| 192K | 0 | 0 | 0 | 1 | 1 | 0 | 0 |
| 208K | 0 | 0 | 0 | 1 | 1 | 0 | 1 |
| 224K | 0 | 0 | 0 | 1 | 1 | 1 | 0 |
| 240K | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| 256K (1/2MB) | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 272K | 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| 288K | 0 | 0 | 1 | 0 | 0 | 1 | 0 |
| 304K | 0 | 0 | 1 | 0 | 0 | 1 | 1 |
| 320K | 0 | 0 | 1 | 0 | 1 | 0 | 0 |
| 336K | 0 | 0 | 1 | 0 | 1 | 0 | 1 |
| 352K | 0 | 0 | 1 | 0 | 1 | 1 | 0 |
| 368K | 0 | 0 | 1 | 0 | 1 | 1 | 1 |
| 384K (3/4 MB) | 0 | 0 | 1 | 1 | 0 | 0 | 0 |
| 400K | 0 | 0 | 1 | 1 | 0 | 0 | 1 |
| 416K | 0 | 0 | 1 | 1 | 0 | 1 | 0 |
| 432K | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| 448K | 0 | 0 | 1 | 1 | 1 | 0 | 0 |
| 464K | 0 | 0 | 1 | 1 | 1 | 0 | 1 |

| Resident Memory in K words | Starting address A21 | A20 | A19 | A18 | A17 | A16 | A15 |
|---|---|---|---|---|---|---|---|
| 480K | 0 | 0 | 1 | 1 | 1 | 1 | 0 |
| 496K | 0 | 0 | 1 | 1 | 1 | 1 | 1 |
| 512K (1 MB) | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 528K | 0 | 1 | 0 | 0 | 0 | 0 | 1 |
| 544K | 0 | 1 | 0 | 0 | 0 | 1 | 0 |
| 560K | 0 | 1 | 0 | 0 | 0 | 1 | 1 |
| 576K | 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| 592K | 0 | 1 | 0 | 0 | 1 | 0 | 1 |
| 608K | 0 | 1 | 0 | 0 | 1 | 1 | 0 |
| 624K | 0 | 1 | 0 | 0 | 1 | 1 | 1 |
| 640K (1 1/4 MB) | 0 | 1 | 0 | 1 | 0 | 0 | 0 |
| 656K | 0 | 1 | 0 | 1 | 0 | 0 | 1 |
| 672K | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| 688K | 0 | 1 | 0 | 1 | 0 | 1 | 1 |
| 704K | 0 | 1 | 0 | 1 | 1 | 0 | 0 |
| 720K | 0 | 1 | 0 | 1 | 1 | 0 | 1 |
| 736K | 0 | 1 | 0 | 1 | 1 | 1 | 0 |
| 752K | 0 | 1 | 0 | 1 | 1 | 1 | 1 |
| 768K (1 1/2 MB) | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| 784K | 0 | 1 | 1 | 0 | 0 | 0 | 1 |
| 800K | 0 | 1 | 1 | 0 | 0 | 1 | 0 |
| 816K | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| 832K | 0 | 1 | 1 | 0 | 1 | 0 | 0 |
| 848K | 0 | 1 | 1 | 0 | 1 | 0 | 1 |
| 864K | 0 | 1 | 1 | 0 | 1 | 1 | 0 |
| 880K | 0 | 1 | 1 | 0 | 1 | 1 | 1 |
| 896K (1 3/4 MB) | 0 | 1 | 1 | 1 | 0 | 0 | 0 |
| 912K | 0 | 1 | 1 | 1 | 0 | 0 | 1 |
| 928K | 0 | 1 | 1 | 1 | 0 | 1 | 0 |
| 944K | 0 | 1 | 1 | 1 | 0 | 1 | 1 |
| 960K | 0 | 1 | 1 | 1 | 1 | 0 | 0 |
| 976K | 0 | 1 | 1 | 1 | 1 | 0 | 1 |
| 992K | 0 | 1 | 1 | 1 | 1 | 1 | 0 |
| 1008K | 0 | 1 | 1 | 1 | 1 | 1 | 1 |

| Resident memory in K words | Starting address A21 | A20 | A19 | A18 | A17 | A16 | A15 |
|---|---|---|---|---|---|---|---|
| 1024K | 1 | 0 | 0 | 0 | 0 | 0 | 0 |

If starting address greater than 2MB, subtract 2MB from the total. Set A21=1 and use table to determine state of A15 through A20 by finding remainder in table.