60448600

CONTROL DATA CORPORATION

CONTROL DATA®
94200
CORE MEMORY

GENERAL DESCRIPTION
APPLICATION SPECIFICATIONS
THEORY OF OPERATION
MAINTENANCE
DIAGRAMS
PARTS DATA

TECHNICAL MANUAL

REVISION RECORD

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or use Comment Sheet in the back of this manual.

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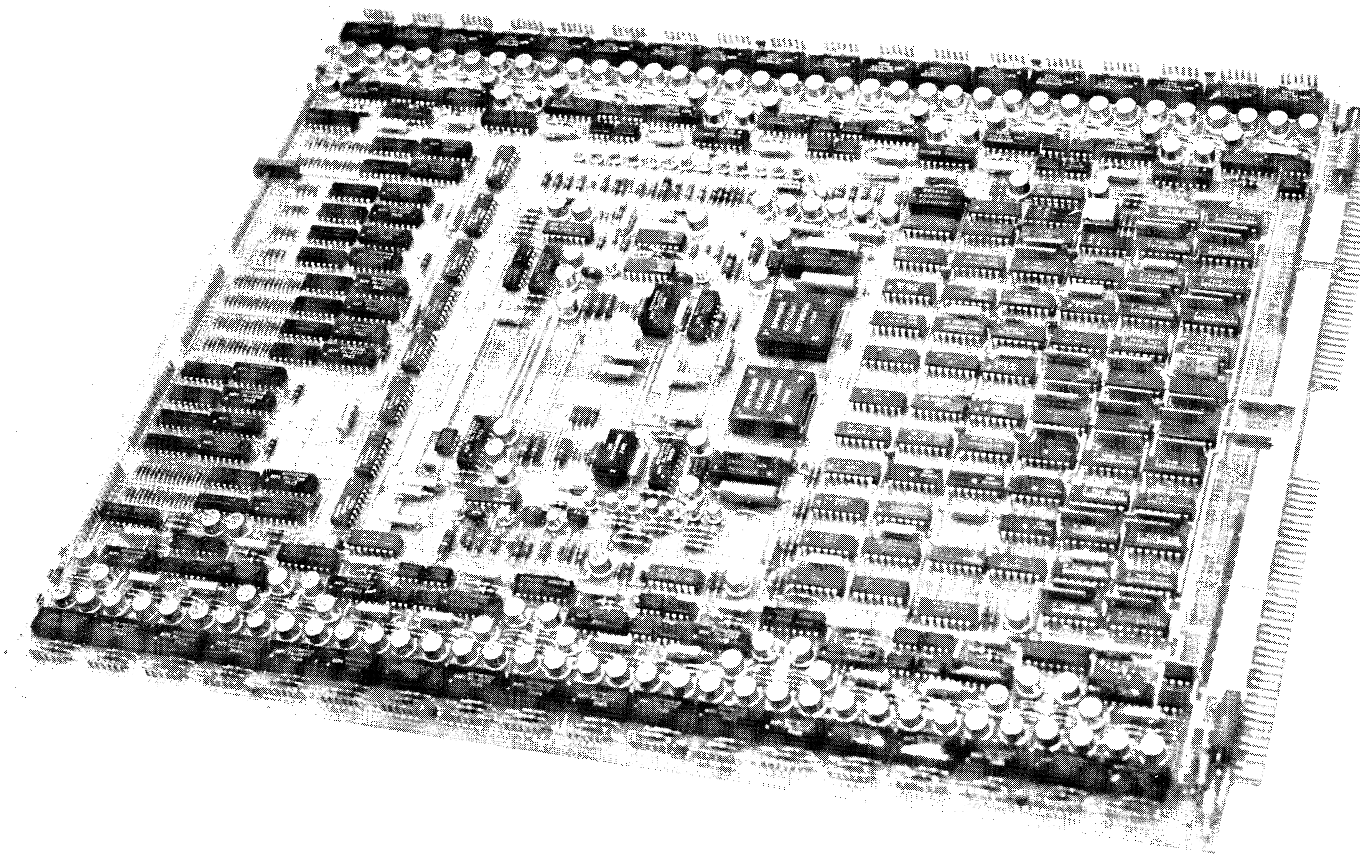


THE 94200 CORE MEMORY MODULE

INTRODUCTION

The CONTROL DATA® 94200 Core Memory Module is a coincident current, magnetic core memory intended for use by original equipment manufacturers.

FUNCTIONAL DESCRIPTION

The 94200 memory module as shipped has a capacity of 16,384 36-bit words. However, the configuration can be changed to 32,768 18-bit words by external wiring changes. Minimum core cycle time is 850 nanoseconds. Up to eight modules may be used in one system.

The 94200 memory module has two basic operating modes called full cycle and split cycle. The module performs three operations in the full cycle mode. These operations are read restore, clear write, and byte control. During a read restore operation, data words are read out of the memory and restored back into memory without modification. A clear write operation writes data words into memory replacing any information in the memory. Nine bits of data can also read out or write into memory. The remaining bytes in the location recirculate during a byte write operation.

In the split cycle mode, the memory does a read-modify-write operation. This means that data is read from memory during the read portion of a cycle, and new data is written into memory during the write portion of a cycle. The write portion of the cycle does not occur until an external signal starts it.

The system with which the 94200 memory module is used must supply data, adddresses, and control signals.

PHYSICAL DESCRIPTION

The 94200 memory module consists of two 17-3/4 inch by 13-7/8 inch (45 by 35.2 centimeters) fiberglass printed circuit (PC) cards held together by screws and spacers. The module is 1 inch (2.54 centimeters) thick. The core memory occupies the area between the PC cards, and semiconductor and passive components fasten to the outside of the PC cards. Connectors molded into the PC cards provide circuit continuity between the cards. An 80-pin connector provides data, address, and control signals and power to the module. Maximum weight of the module is 6 pounds.

The logic is TTL in dual in-line packages. Voltages required are +5 volts, +15 volts, and -15 volts. Nominal power consumption is 120 watts operating and 35 watts standby. Forced-air cooling is required.

POWER REQUIREMENTS

Voltages:	Standby current:	Operating current:
+15 volts	0.12 ampere	0.75 ampere
+5 volts	4.5 amperes (5.1 amperes)†	6.4 amperes (7.0 amperes)†
-15 volts	0.55 ampere	6.5 amperes

Voltage regulation	±2 percent
Voltage margins	± 5 percent of nominal

COOLING AND ENVIRONMENTAL REQUIREMENTS

Cooling:

Forced air at a minimum of 40 cubic feet/minute

Operating temperature range:

0° C to 55° C

Nonoperating temperature range:

-40° C to 80° C

Operating humidity:

10 percent to 90 percent without condensation

DIMENSIONS

Figure 2-1 illustrates the module dimensions.

INTERFACE DESCRIPTION

LOGIC LEVELS

Logic 1 (high) in/out of memory:

+2.4 vdc to +5.5 vdc

Logic 0 (low) into memory:

0 vdc to 0.8 vdc

Logic 0 (low) out of memory:

0 vdc to 0.5 vdc

†Includes terminating resistor.

DEFINITIONS

Access Time:

The time between the appearance of the cycle initiate signal at the input terminals of the memory and the data signals being available at the output terminals of the memory. Maximum access time is 350 nanoseconds.

Byte:

A group of 9 data bits.

Cycle Time:

The time between memory request signals.

Full Cycle Clear Write:

The clear-write operation clears data at a specified address and writes new data present on the data in lines into the address.

Full Cycle Read-Restore:

The read-restore operation reads data from a specified address, puts the data on the data out lines, and restores the data into the same address.

Full Cycle Time:

The maximum time required to do a clear-write or read-restore into memory. Minimum full cycle time is 850 nanoseconds.

Read-Modify-Write:

The read-modify-write operation provides modify time after the read portion of the memory cycle completes. The read portion of the memory cycle reads data from a specified address and puts the data on the data out lines. The module then remains quiescent until a write initiate input signal starts the write portion of the memory cycle. New data or the data read from memory is written into the specified address depending on the byte control inputs. Minimum split cycle time is 900 nanoseconds.

INPUT SIGNALS

The leading edge of the cycle initiate signal is defined as being t_0 in the following input signal description. All timing measurements are made at the 1.5-volt level of the signal transition.

The load driving requirements indicated below are standard TTL loads and do not include termination load.

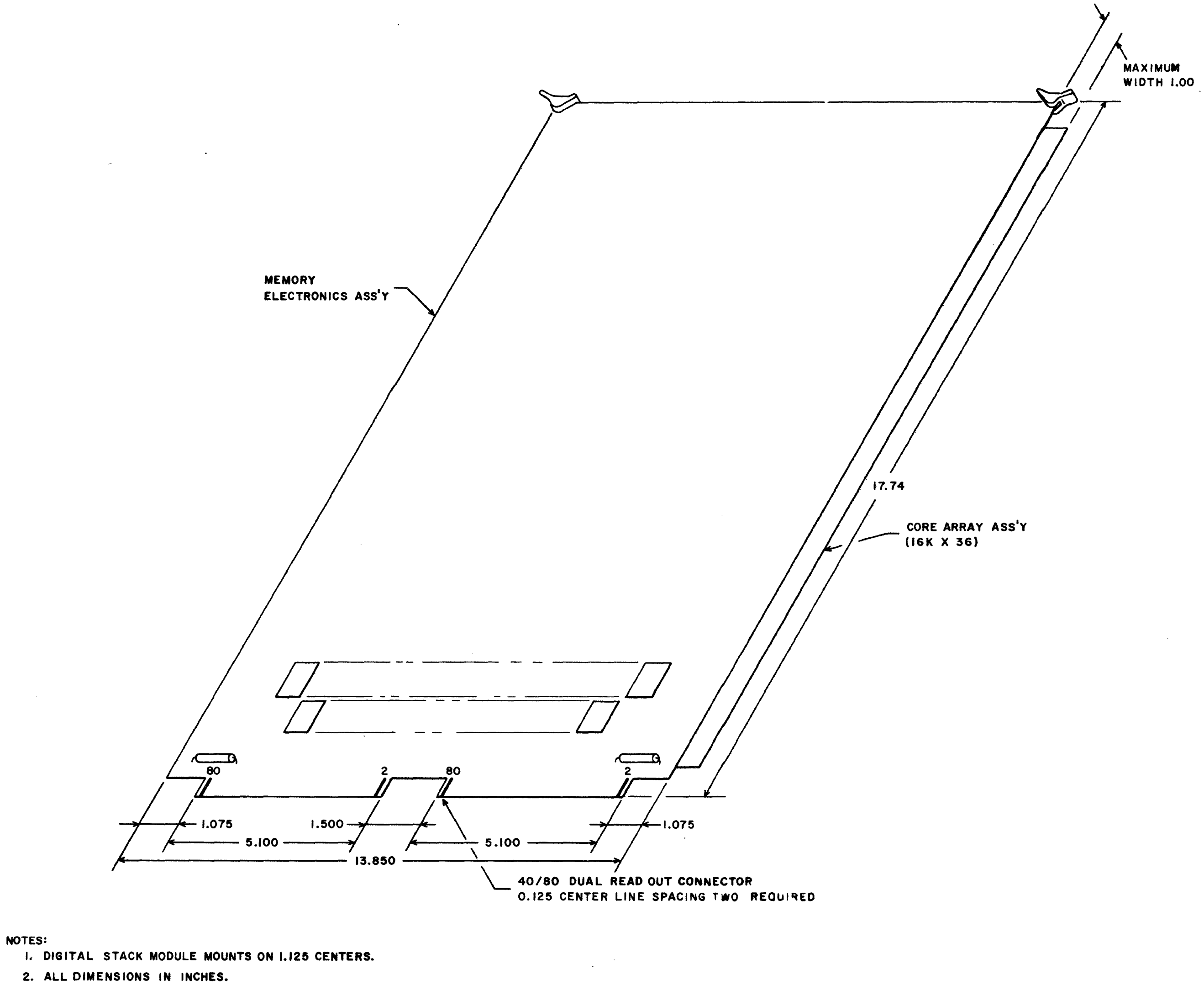


Figure 2-1. Module Dimensions

Address Lines (AD00 through AD13):

These lines select one of 16,384 36-bit word locations in memory. The leading edge of the address signal must be stable for a minimum of 100 nanoseconds after the leading edge of the $\overline{CI}$ signal. There are 14 address lines. Each address line drives one load.

Byte Control ($\overline{B0}$ through $\overline{B3}$):

These lines make possible transfers of 9-bit bytes of data. One or more of these lines being low causes corresponding bytes of data to write into memory upon receiving the cycle initiate ($\overline{CI}$) signal. If one or more of these lines is high, 9-bit bytes of data read out of memory upon receiving the $\overline{CI}$ signal. If full word transfers are desired, these inputs should be left open and the word write ($\overline{WW}$) input used. The byte control signals each drive one load. Refer to the byte timing description in the options subsection.

Cycle Initiate ($\overline{CI}$):

This signal going low initiates a memory cycle. The leading edge of this signal is defined as t_0. The signal must remain low for 100 nanoseconds and may remain low to a maximum of t_0 to 750 nanoseconds. The cycle initiate signal drives one load.

Data In (DI00 through DI35):

These lines transmit data into memory. Data must be stable to t_0 plus 150 nanoseconds during clear write cycles. During split cycles, data must be stable at the leading edge of write initiate ($\overline{WI}$) and remain for 150 nanoseconds. Each data in line drives one load when the memory is wired for 36-bit words and 16,384 locations. If the memory is wired for 18-bit words and 32,768 locations, each data in line drives two loads.

Data Save (DS):

This line must be high for the memory to operate. Data save should be low during power up and power down to retain data. A memory cycle will not start if the data save signal goes low before $\overline{CI}$. If data save goes low during a memory cycle, that cycle completes, and the next cycle does not occur. The data save signal drives three loads.

Module Select (AD14 through AD16):

These inputs provide addressing which allows a system to reference up to eight memory modules. Each module has a manual switch in a dual in-line package. This switch is set to decode an address assigned to the module. Each line drives one load. In single module applications, the switch must be closed and inputs AD14, AD15, and AD16 left open.

Reset:

This signal being negative for 100 nanoseconds resets the memory logic if it is not cycling. This signal is only used if an illegal signal condition has caused the memory logic to hang up. Reset drives three loads.

Word Write ($\overline{WW}$):

This signal allows full word data transfers. A read restore operation occurs when word write is high. If word write is low, a clear write operation occurs. If data transfer in 9-bit bytes is desired, the word write input should be left open and the byte control inputs used. Word write drives one load.

Write Initiate (WI):

This signal initiates the write portion of a read modify write operation. Write initiate may go negative at t_0 plus 450 nanoseconds or later, and remain for a minimum of 100 nanoseconds and maximum of 400 nanoseconds. The read portion of the cycle is complete at t_0 plus 450 nanoseconds. The write portion of memory requires 450 nanoseconds to complete. A read-modify-write operation requires a minimum of 900 nanoseconds when write initiate occurs at 450 nanoseconds. Write initiate drives one load.

OUTPUT SIGNALS

The leading edge of the cycle initiate signal (an input signal) is defined as being t_0 in the output signal descriptions that follow. All timing measurements are made at the 1.5 volts level of the signal transition.

Data Available ($\overline{DA}$):

This signal going low indicates that data from memory is available when any one byte is in a read restore or read modify write cycle. This signal occurs at t_0 plus 350 nanoseconds and remains until t_0 plus 450 nanoseconds.

Data Out (D000 Through D035):

Data read from memory is available at the data out pins of the interface connector 350 nanoseconds after t_0 and remains until t_0 plus 800 nanoseconds for full cycle operation. For a read-modify-write, data is available 350 nanoseconds after t_0 and remains until approximately 30 nanoseconds after write initiate. There are 36 data out pins.

End of Cycle ($\overline{EC}$):

This going low signal indicates the memory cycle is complete. This signal occurs at t_0 plus 800 nanoseconds and remains until t_0 plus 880 nanoseconds.

End of Read ($\overline{ER}$):

This signal going low indicates the read portion of the memory cycle is complete. This signal occurs at t_0 plus 450 nanoseconds and remains until t_0 plus 500 nanoseconds.

Memory Busy ($\overline{MB}$):

This signal being low indicates that a memory cycle is occurring. This signal occurs at t_0 plus 90 nanoseconds and remains until t_0 plus 800 nanoseconds.

OPTIONS

Byte Control Timing (BCT):

Grounding or leaving this input open allows adjustment of the timing of the byte control signals for read modify write operations. If J46-77 is grounded, the byte write control signal must occur at t_0 and remain stable for 100 nanoseconds. If J46-77 is open, the byte control signal must occur at write initiate time in the write portion of the cycle and remain stable for 100 nanoseconds. Refer to the byte control description in the input signals subsection.

Clear Data Out ($\overline{\text{CDO}}$):

This input allows an external signal to clear the data out lines. The signal should occur between t_0 plus 450 (data out lines active for 100 nanoseconds) and t_0 plus 800 nanoseconds. If this input is open, the data out signals operate as described in the output signals subsection.

External Current Control (ECC):

An external current regulator can provide bias current for a multimodule system. To operate the modules this way, remove jumper -1 and jumper -2 (shown on logic sheet 22) from each module. Connector pins J46-11 and J46-12 must then supply the bias current. Figure 2-2 shows how to connect the modules. Figure 2-3 shows a circuit for a regulator which can be used as an external current supply.

Late Data Timing (LDT):

Grounding this input allows the data in signals to be delayed. If J46-6 is grounded, data in must be present from t_0 plus 200 nanoseconds to t_0 plus 350 nanoseconds. If J46-6 is open, data in must be present from t_0 to t_0 plus 150 nanoseconds.

16K to 32K Capacity Option:

The memory configuration can be changed to 32,768 18-bit words by the following modifications.

- Grounding input J47-58.
- Providing address bit AD17 which is address 14. Module select addresses move to AD15-16-17. Refer to logic sheet 18.
- Connect the data inputs as indicated on page 5-1 of the logic diagrams. That is, connect J47-21 to J47-29, J47-23 to J47-49, and so forth.

CONNECTOR

The module plugs into dual edgeboard wire wrap connectors of 80 pins each. The pins are on 0.125 inch centers. The CDC part number is VPB01C40B00A1. A vendor part number is Amphenol 67878-7.

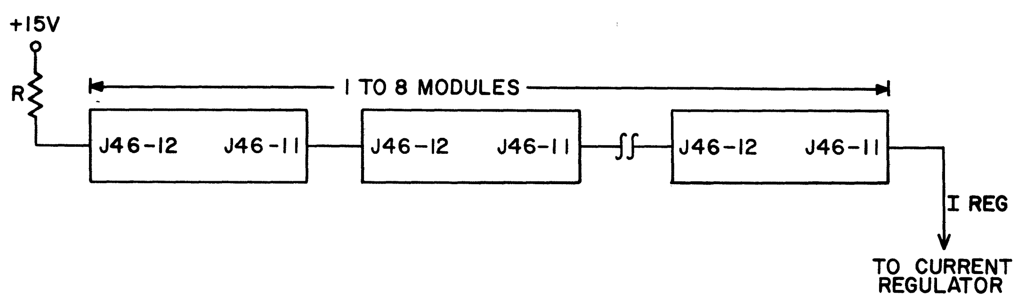
TERMINATION REQUIREMENTS

The inputs to the 94200 memory must have the proper termination resistors. Similarly, the inputs to the external equipment must be properly terminated. Refer to figure 2-4. The 94200 memory is available with or without terminators. Modules without terminators can be connected in parallel, and terminated using terminators located on the backpanel.

BIDIRECTIONAL DATA LINES

Tying the interface connector inputs and outputs together allows the use of one data input/output line per bit. To do this, the output drivers must be able to drive two termination networks (refer to figure 2-4). The 94200 output drivers can drive two termination networks.

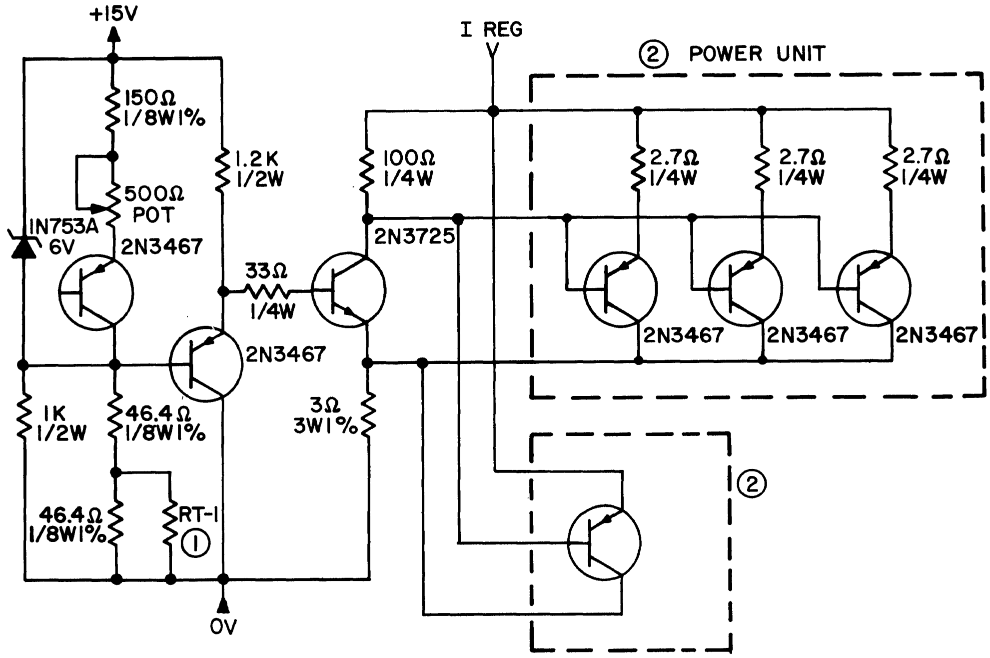
Operation with bidirectional data lines in read modify write mode can cause reflections to occur on the data lines. This happens if the 94200 output drive and the external input drive are on simultaneously (beginning of write initiate). When the memory driver turns off,



NOTE:

FOR 1 TO 2 MODULES R MUST BE 24.0Ω, 6 WATTS.
FOR 3 TO 4 MODULES R MUST BE 18.0Ω, 5 WATTS.
FOR 5 TO 6 MODULES R MUST BE 12.0Ω, 4 WATTS.
FOR 7 TO 8 MODULES R MUST BE 6.0Ω, 3 WATTS.

Figure 2-2. Connection of Modules for External Current Control



NOTES:

① RT-1 IS A THERMISTOR WHICH IS 100Ω AT 25°C. POSSIBLE THERMISTOR VENDORS ARE NATIONAL LEAD INC. 2D204 OR RODAN 2BD100.

② THE POWER UNIT CAN CONSIST OF A NUMBER OF TRANSISTORS OR ONE POWER TRANSISTOR. THE POWER REQUIRED IS 2.5 WATTS MAXIMUM.

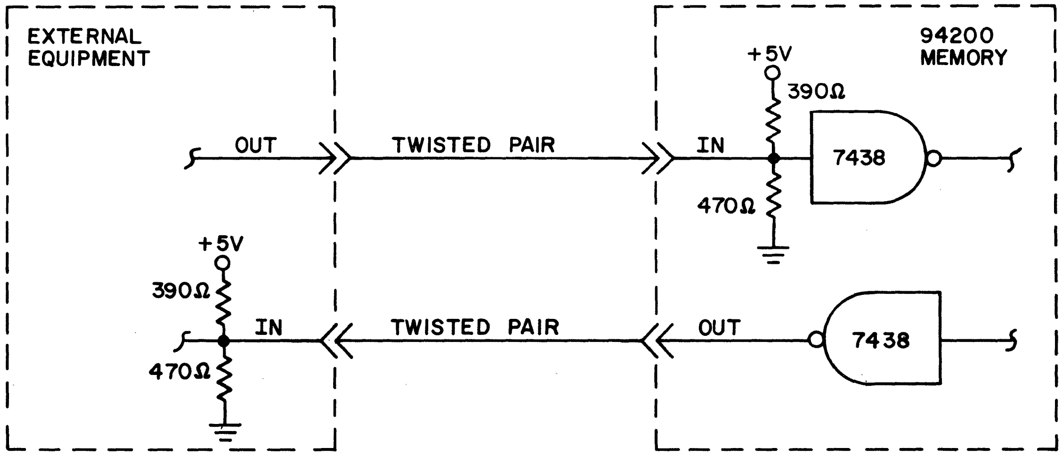
Figure 2-3. Current Regulator Circuit

a positive reflection occurs which could cause the memory to malfunction. The amplitude and duration of the reflection depend on the length of the data line.

There are two ways to eliminate the reflections. One way is to apply a negative pulse to the clear data out input 50 nanoseconds before write initiate. This clears the memory drivers before new data appears on the lines. Another way to eliminate the reflections is to connect the end of read output signal to the clear data out input. This causes data to be on the line from t_0 plus 350 nanoseconds to t_0 plus 500 nanoseconds.

TIMING DIAGRAMS

Timing diagrams for read restore, read-modify-write, clear write, and byte write operations are at the end of this section.



Notes:

1. The 94200-00 does not have input termination resistors.
2. The 94200-01 has input termination resistors.
3. The twisted pair lines should be a maximum of 10 feet long.
4. Control Data can supply plug-in terminator resistors.
5. The 7438 drivers can sink 48 ma.

Figure 2-4. 94200 Line Terminations

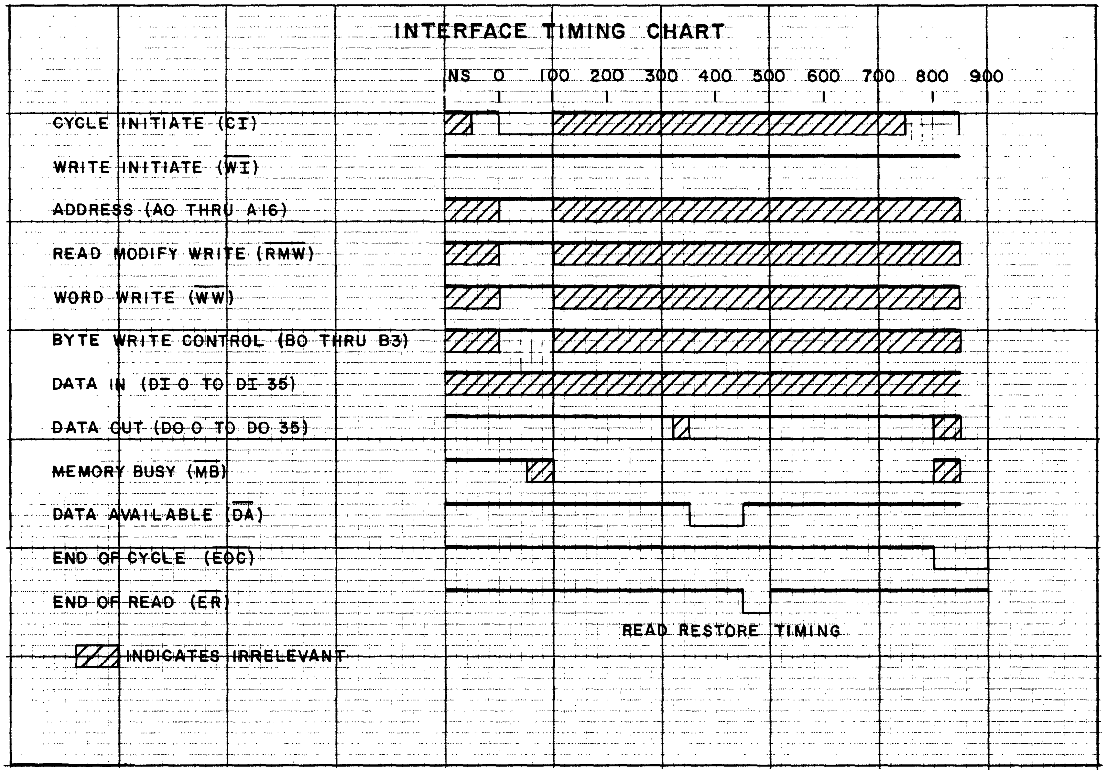


Figure 2-5. Read Restore Timing

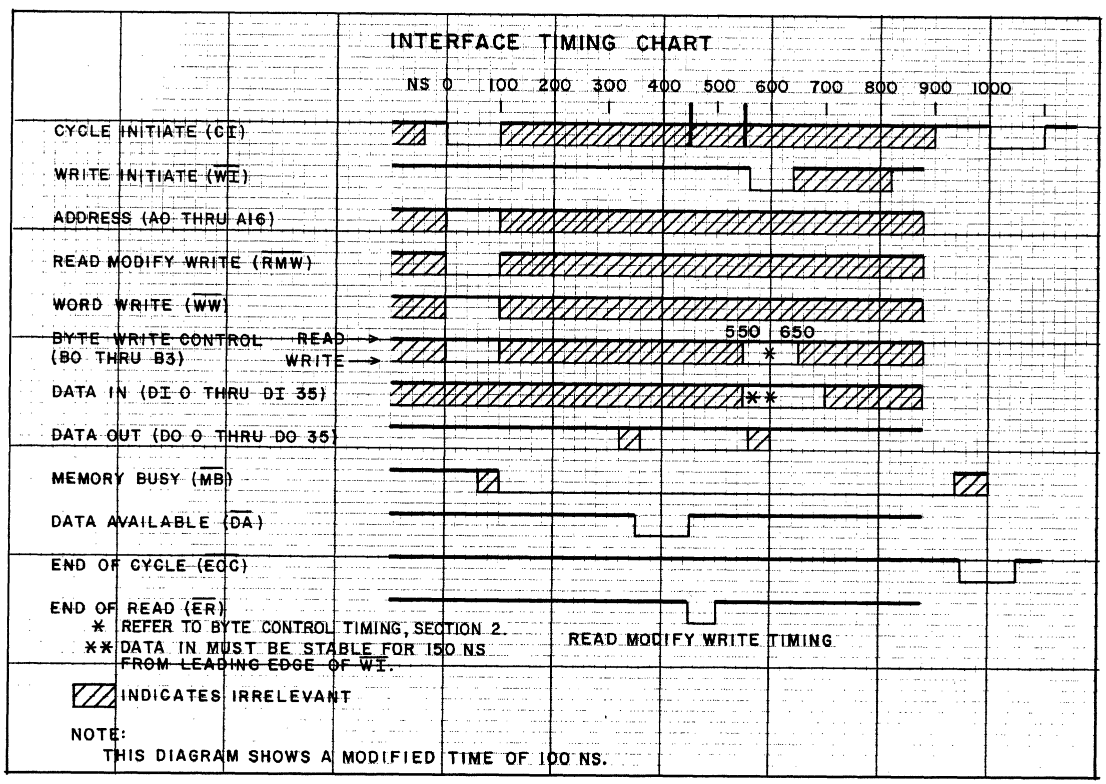


Figure 2-6. Read Modify Write Timing

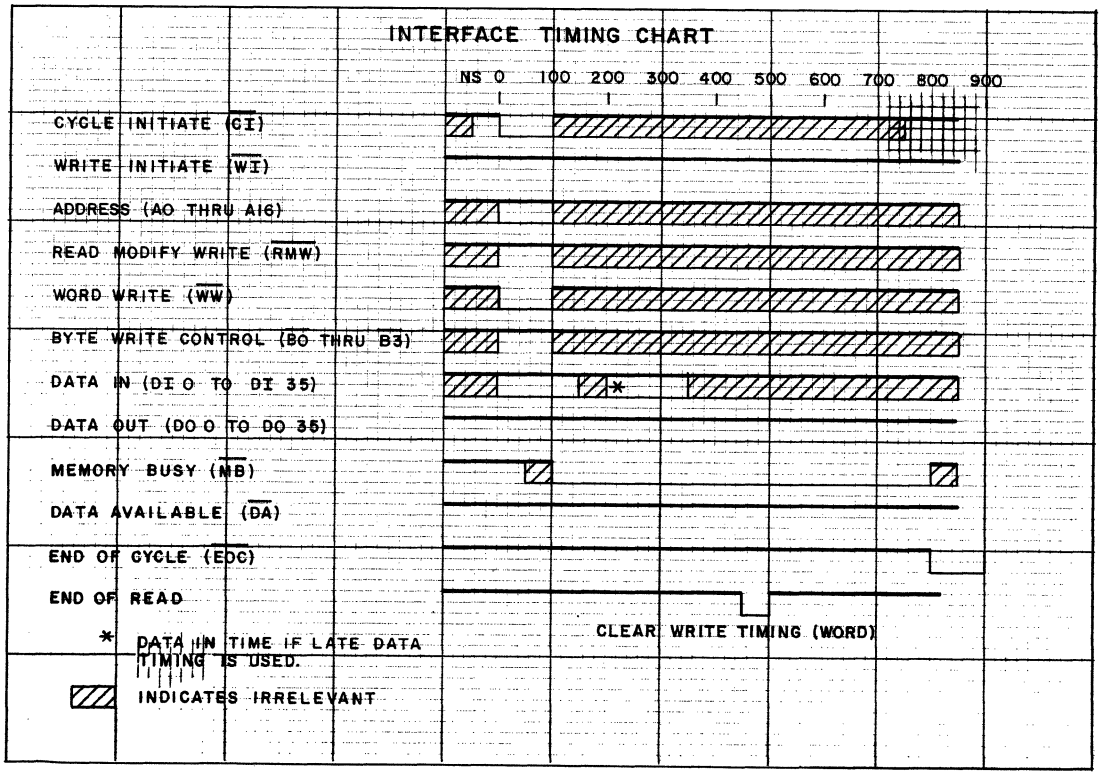


Figure 2-7. Clear Write Timing (Word)

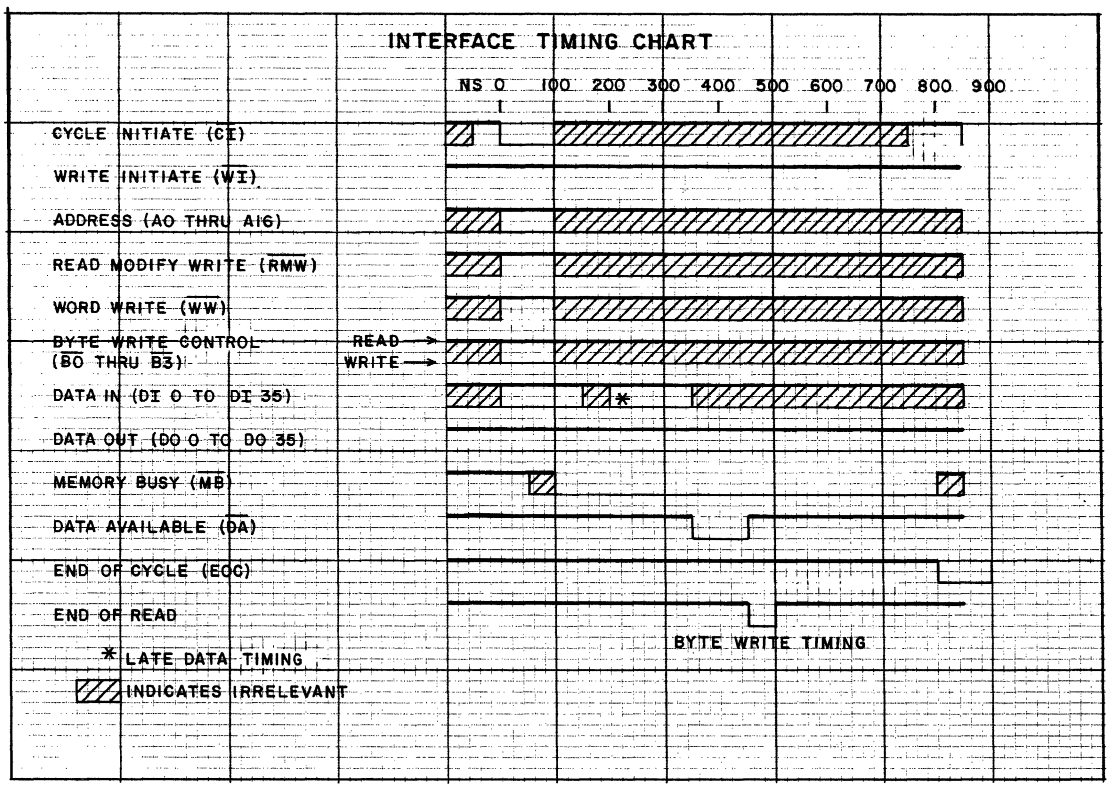


Figure 2-8. Byte Write Timing

INTRODUCTION

The 94200 memory module is a 3-D, 3-wire, random access core memory module with a common sense/inhibit line. The module contains timing, control, inhibit , and core drive circuits as well as data and address registers. Figure 3-1 shows a block diagram of the module.

MODULE SELECT

Module select decodes an address from the external equipment which specifies one module in a system that contains more than one module. A manual switch in a dual in-line package on each module must be set to decode the module address. In a single module application, the switch must be set closed and address inputs AD14, AD15, and AD16 left open. Logic page 5-21 shows the module select circuit.

ADDRESS REGISTER

The external equipment supplies information that determines at which location within the module an operation will take place. The address register stores this information and distributes it to the module select, core driver, byte control, and timing circuits. Address registers are shown on logic pages 5-18 through 5-20. The 74S157 chips compose the address register. When the hold input signal is low, the register gate is open. When hold goes high, the register latches.

TIMING AND BYTE REGISTER

The external equipment supplies control information that determines which operation the module performs. The cycle initiate input signal starts a read sequencer circuit. This circuit generates a sequence of signals that times the read portion of the memory cycle. When the read sequencer stops, a write sequencer starts to generate timing signals for the write portion of the memory cycle for a full cycle operation. During split cycle operations, the read sequencer completes the read portion of memory cycle and waits for a write initiate input signal to start the write sequencer. Both the read and write portion of a memory cycle occur during full and split cycle operations.

The timing diagrams (figures 3-2 and 3-3) show the read and write sequencer signals for one memory cycle. Other signals derive from the read and write sequencer signals through logical AND and OR functions. These signals cause the current source, sink discharge, core drive, and inhibit drive circuits to function at the proper times during a memory cycle. An explanation of the timing control logic on page 5-3 follows.

Output 8 of the gate at location Z106 and the delay line form a clock circuit. A factory-installed jumper from one of the delay line taps to input 13 of the gate completes the feedback loop. The clock period is 30 nanoseconds on and 30 nanoseconds off.

During a full cycle operation, inputs $\overline{\text{WI}}$ (write initiate) and $\overline{\text{MRMW}}$ (read modify write) are high. Input $\overline{\text{clear}}$ only goes low during power up or if the +15 volt and -15 volt power supplies malfunction. Input $\overline{\text{DS}}$ (data save) is high except at power up and power down. Inputs QT-12 and QT-24 are low at the start of a memory cycle while inputs $\overline{\text{QT-13}}$ and $\overline{\text{HOLD}}$ are high.

Input $\overline{\text{CI}}$ (cycle initiate) going low starts a memory cycle. Input MS (module select) goes high after the module select addressing is stable. Output $\overline{\text{RCLR}}$ then goes low setting the RST flip-flop and RST (Z95-8) output high which enables the read sequencer logic on page 5-4. Output $\overline{\text{RCLR}}$ going low causes output 6 of the gate at location Z106 to go high. The clock begins to oscillate and drives the sequencer logic.

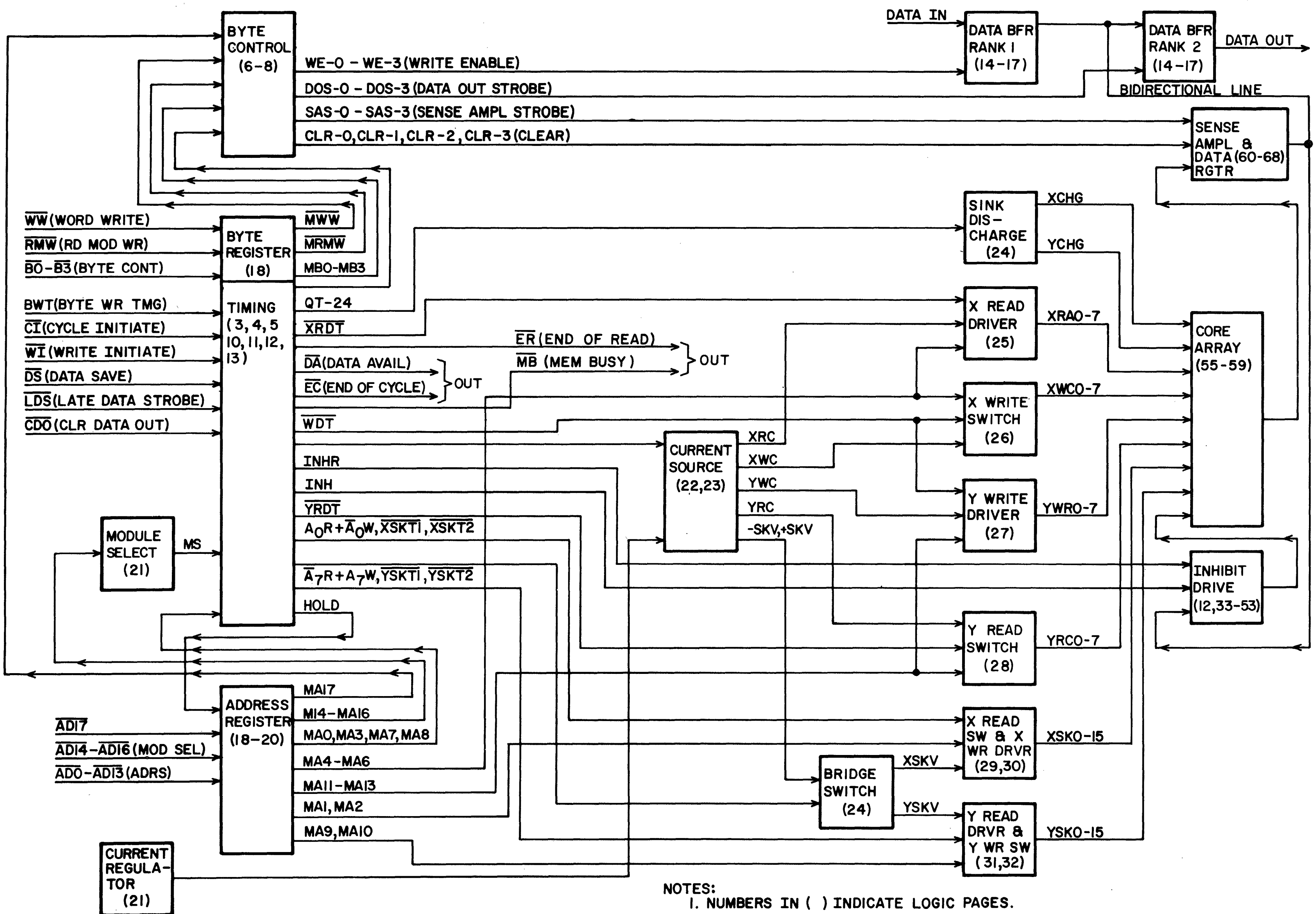
The RST flip-flop being set causes pin 2 of Z106 to go low. This holds inputs 9, 10, and 12 of the gate at location Z106 high enabling the clock (CPM) to operate. $\overline{\text{HOLD}}$ then goes low driving input 9 of the gate at location Z96 low for the duration of the memory cycle. This prevents any change at the $\overline{\text{CI}}$ input from affecting the cycle.

At the end of the read portion of the cycle, input QT-12 goes high causing output 8 of the flip-flop at location Z89 to go low. This resets the flip-flop which generates output RST, and the read sequencer inhibits. Z89-9 going high causes outputs WST-1 and WST-2 to go high and output $\overline{\text{ER}}$ (end of read) to go low. WST-2 going high enables the write sequencer logic. At the end of the write portion of the cycle, input QT24 goes high and Z89-6 goes low resetting WST-1 and WST-2. This stops the clock. QT-24 resets the hold flip-flop allowing another $\overline{\text{CI}}$ input signal to start a new memory cycle.

During a split cycle operation, input MRMW is low. This means that output 6 of the gate at location Z95 is always high. Consequently, input $\overline{\text{WI}}$ must go low to start the write portion of the memory cycle. Input $\overline{\text{WINH}}$ prevents $\overline{\text{WI}}$ from starting the write portion of the cycle if the read portion has not occurred.

BYTE CONTROL

The byte control logic combines external control signals and internal timing signals to generate data control signals. These signals cause the data buffer, sense amplifier, and data register to function at the proper times during a memory cycle. The byte control logic also determines from external control signals whether full words or 9-bit bytes transfer into or out of memory.



NOTES:
1. NUMBERS IN ( ) INDICATE LOGIC PAGES.
2. THE APPENDIX CONTAINS A LIST OF MNEMONICS.

Figure 3-1. Module Block Diagram

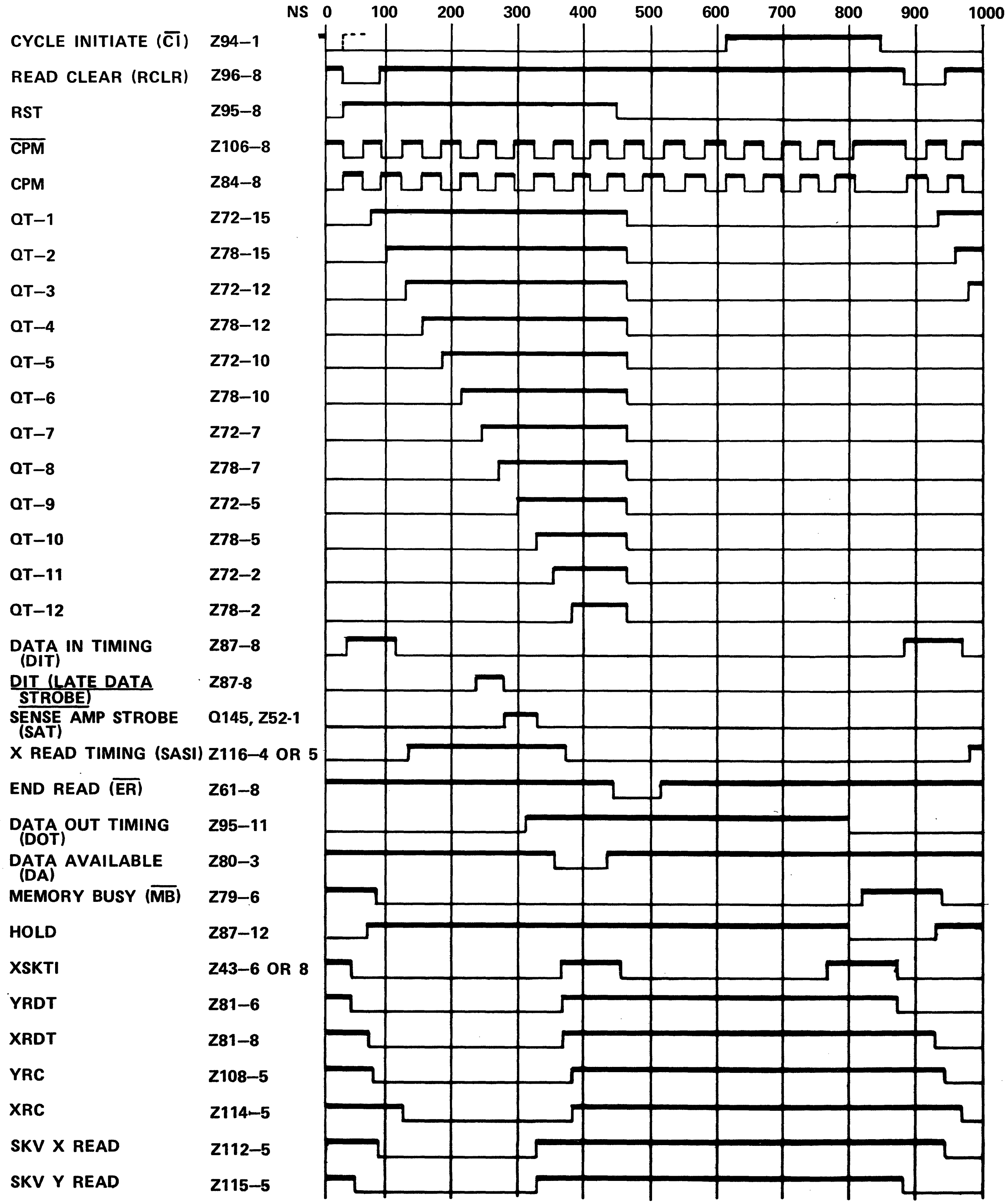


Figure 3-2. Memory Cycle Timing, Read Portion

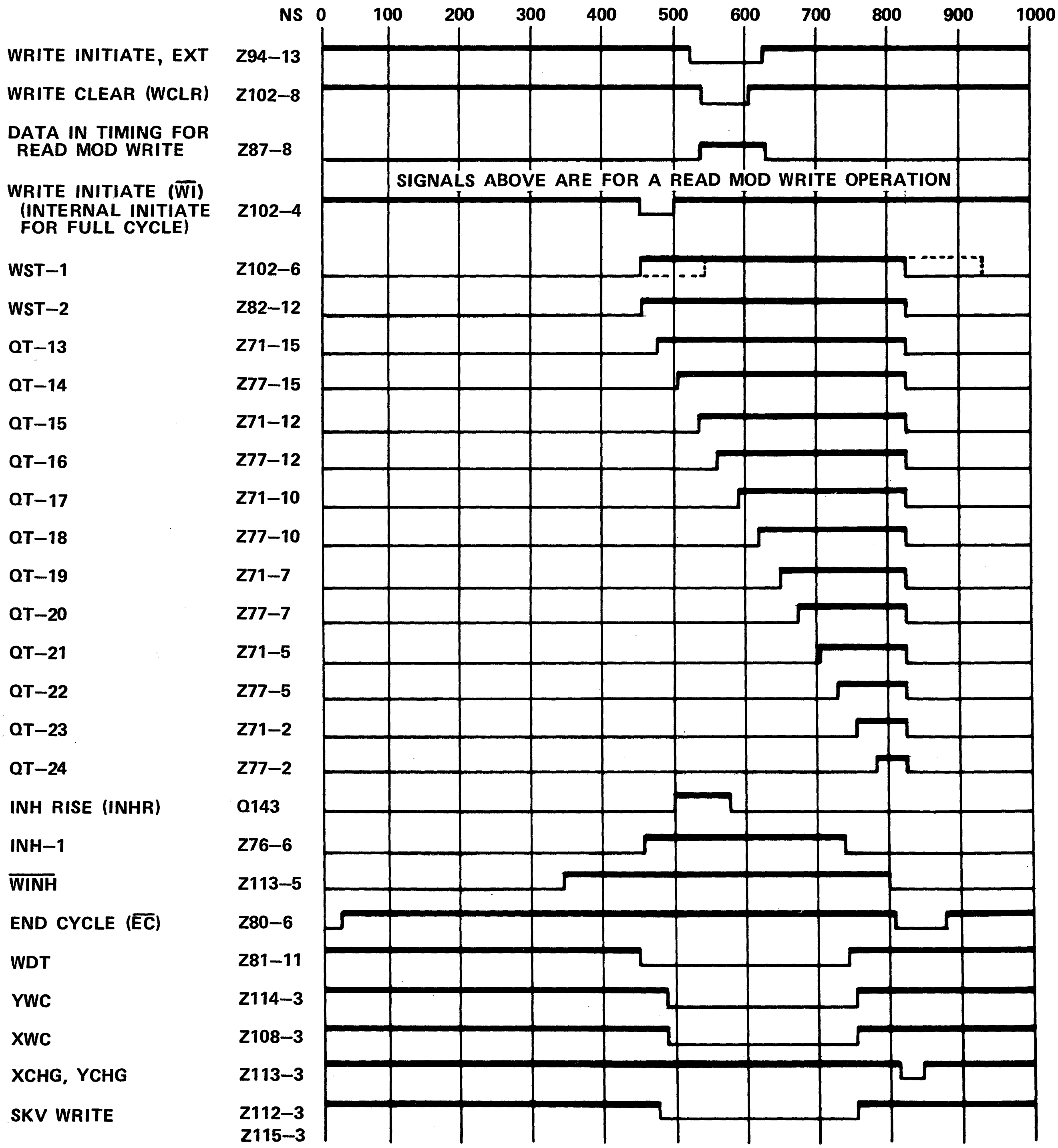


Figure 3-3. Memory Cycle Timing, Write Portion

Descriptions of the byte control logic during various operations follow.

BYTE TRANSFERS, 16K x 36-BIT CONFIGURATION

The memory is divided into four 9-bit bytes, MB-0 through MB-3 (refer to logic page 5-18). The 74S157 chip at location Z75 stores the four bits of byte information. When a byte input is high, the module performs a read-restore operation. A low byte input causes a clear-write function to occur. The byte register latches at 80 nanoseconds after the cycle initiate signal appears and remains latched until 800 nanoseconds into the cycle.

When the module is in the 16K x 36-bit configuration, the A inputs of the 74S157 at location Z47 on logic page 5-6 are selected. For a read-restore operation, MB-0 through MB-3 are high and $\overline{\text{MWW}}$ is high ($\overline{\text{WW}}$ input is open). Outputs WR-0 through WR-3 are then low. This holds the write enable gates (WE-0 through WE-3) off and enables the sense amplifier strobes (SAS-0 through SAS-3). When MB-0 through MB-3 are low (clear-write operation), the WR-0 through WR-3 signals are high. This causes the WE gates to enable and the SAS gates to inhibit.

WR-0 through WR-3 control the data out strobes (DOS, page 5-7). When the WR signals are low (read-restore), the DOS gates enable which samples the output buffers. Data then appears on the output lines.

FULL WORD TRANSFERS, 16K x 36-BIT CONFIGURATION

The word write ($\overline{\text{WW}}$) input controls all 36 bits in this case. Word write operates the memory in the same manner as the byte control inputs described in the preceding section. When word write is high, a read-restore operation occurs. Word write being low causes a clear-write operation.

BYTE TRANSFERS, 32K x 18-BIT CONFIGURATION

The B0 and B2 inputs control byte transfers in this configuration. The B1 and B3 inputs should be open, and the 16K/32K input should be grounded. Pin 1 of the 74S157 on logic page 5-6 being high enables the B inputs of the 74S147. When a clear-write operation is initiated, MB-0 is high. MA17 being high causes WR-0 to go high. $\overline{\text{MA17}}$ is then low causing WR-1 to be low (read-restore). Byte 1 (B2 input) which controls WR-2 and WR-3 operates in the same manner.

FULL WORD TRANSFERS, 32K x 18-BIT CONFIGURATION

Word write control ($\overline{\text{WW}}$) operates in the same way as the byte control inputs except that $\overline{\text{MWW}}$ controls the full word. The byte control inputs should be open.

The memory module always operates on a 36-bit word with address 17 determining what half of the word is to be operated (controlled) on.

DATA BUFFER

The data buffer receives data from the external equipment and transmits data to the external equipment. Logic pages 5-14 through 5-17 show the data buffer. Data on the input lines gates into memory when the write enable (WE) input goes high. If write enable is low and data out strobe goes high, data transmits from memory to the external equipment.

CURRENT REGULATOR

The current regulator provides a regulated bias current for the switch cores in the current source. Thermistor RT-1 causes the regulator to compensate for changes in memory core characteristics with temperature. If temperature increases, the regulator output decreases and vice versa. Logic page 5-21 shows the current regulator circuit.

CURRENT SOURCE

The current source provides current for switching the memory cores. Logic pages 5-22 and 5-23 show the current source. Outputs YRC, +SKV, XWC, XRC, -SKV, and YWC drive the cores through the bridge, read, and write switches. Timing signals cause the appropriate gates at locations Z108 and Z114 to turn on the current source after all of the appropriate core drive switches have turned on.

IREG from the current regulator flows through switch cores T68 and T80 in series. This current biases the switch cores and causes the current source to provide the proper drive current to the memory cores.

BRIDGE SWITCH

The bridge switches steer the direction of current flow in the XSKV and YSKV outputs for read and write operations. Timing signals drive the gates at locations Z112 and Z115. These gates cause a pair of transistors to turn on and effectively connect the outputs to -SKV or +SKV. Q126 effectively connects XSKV to -SKV and Q129 effectively connects YSKV to +SKV during a read operation. During a write operation, Q127 effectively connects XSKV to +SKV and Q140 effectively connects YSKV to -SKV. Logic page 5-24 shows the bridge switch.

X READ SWITCHES AND X WRITE DRIVERS, Y READ DRIVERS AND Y WRITE SWITCHES

These circuits connect the X and Y drive lines to the current source during read and write operations. Timing and address signals cause specified drive lines to activate at the proper time. These circuits are shown on logic pages 5-29, 5-30, 5-31, and 5-32. The circuit on page 5-29 is described below.

The 74145 decodes address and timing information. This causes a specified output to connect to the proper current source polarity at the proper time during read and write operations. Address inputs MA01 and MA02 specify a pair of transistor switches. AoR + $\overline{A}$oW specifies one of the pair of switches. Table 3-1 illustrates the various conditions. Assume the address specifies the uppermost pair of transistors. The uppermost transistor is Q_1, and the second transistor down is Q_2 (this half of QM-13 package).

TABLE 3-1. ADDRESS AND DRIVE CURRENT RELATIONSHIP

Operation	XSKV	AoR+$\overline{A}$oW	Decoder Output Low	Q_1	Q_2	Drive Current Flow
Read	-	Low	1	On	Off	From XSK0 through CR393, through Q_1, through CR368 to XSKV.
Write	+	High	2	Off	On	From XSKV through CR377, through Q_2, through CR396 to XSK0.
Read	-	High	2	Off	On	From XSK1 through CR395, through Q_2, through CR369 to XSKV.
Write	+	Low	1	On	Off	From XSKV through CR376, through Q_1, through CR394 to XSK1.

X READ DRIVER, X WRITE SWITCH, Y WRITE DRIVER, Y READ SWITCH

These circuits turn on specified X or Y drive lines during read and write operations. The 74145 decodes the address and causes one of the transistor switches to turn on. This effectively connects the selected drive line to the current source. Logic pages 5-25, 5-26, 5-27, and 5-28 show these circuits.

The diagram in figure 3-4 shows the core drive circuits.

INHIBIT

During a read operation, all one-state cores at the location being referenced switch to a zero state. These cores switch back to the one state during the write (restore) portion of the memory cycle. The inhibit circuit prevents the cores originally in the zero state from also switching to the one state during write portion of memory cycle.

Logic sheets 36 through 53 show the inhibit drive circuits. Refer to bit 3 on page 5-37 during the following discussion unless otherwise noted. The P27-1 input comes from the sense amplifier output. The INHT-4 input derives from address and timing signals. If inputs P27-1 and INHT-4 are high, transistor Q_{11} turns on causing current to flow in outputs P27-5 and P27-6. This inhibits the corresponding core from switching during restoration.

Q_{10} is turned on during the start of inhibit. This effectively shorts out part of the primary winding of the inhibit drive transformer. The turns ratio of the transformer thus effectively decreases. Consequently, the inhibit drive current builds up to the desired value. When the drive current reaches the desired value, Q_{10} turns off increasing the turns ratio again. The primary of the transformer then delivers a lower current. Because of current step up, the secondary produces the proper inhibit current.

The predrive for inhibit rise circuits on logic pages 5-33, 5-34, and 5-35 drive the transistors that effectively short part of the primary of the drive transformers. The inhibit rise time generator shown on page 5-12 provides a pulse to drive the predrive for inhibit rise circuits. This pulse is adjusted at the factory by selecting R279 in the inhibit rise time generator. Input QT-13 causes the inhibit rise time circuit to generate a pulse with the proper width.

SINK DISCHARGE

The sink discharge circuit is shown on page 5-24. Input QT-24 causes Q130 and Q131 to turn on and effectively tie the core drive lines to 0 volts at the end of a memory cycle. This leaves the stack at 0 volts until another cycle initiates.

CORE ARRAY

The 94200 core array is organized into 36 128 x 128 planes containing 16,384 bits each. Each plane correlates with one bit of the data word. An address drive line is strung through each row of cores in the X direction. Similarly, an address drive line is strung through each row of cores in the Y direction. The address drive lines are continuous from one plane to the next. The memory thus has a total of 128 X and 128 Y drive lines. Activating one X line and one Y line references one word location. Each plane has two sense/inhibit lines. This allows a faster memory cycle. Each sense/inhibit line is strung through one half of the cores (8192) in the plane. The sense/inhibit lines connect to dual sense amplifiers. Dual sense amplifiers and a data register are combined in the same package. There are 36 dual sense amplifier-data register packages.

During a read operation, all cores at the referenced location in the one state switch to the zero state. Pulses are induced into the corresponding sense/ inhibit lines when a core switches. The sense

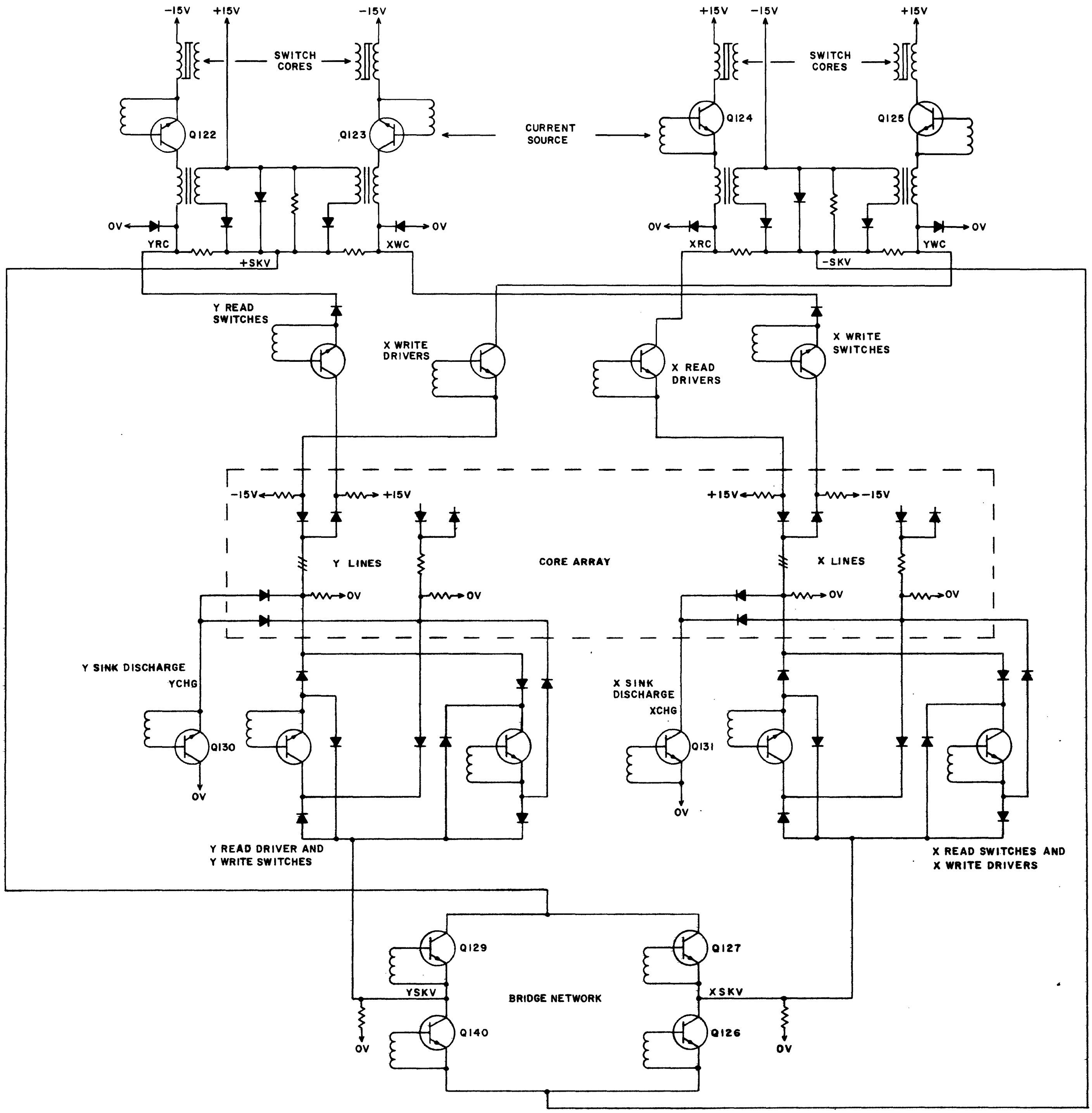


Figure 3-4. Core Drive Circuits

amplifiers receive the induced pulses and store ones in the data register. Cores which were in the zero state at the beginning of the operation do not switch. Therefore, those sense amplifiers store zeros in the data register.

Information stored at the referenced location is destroyed during a read operation. Consequently, the information must be restored into memory. During the write (restore) portion of a memory cycle, the sense/inhibit lines corresponding to zeros in the stored data word are driven. This prevents those cores from switching to a one state. The bits with no inhibit current cause these cores to switch to a one state.

Write operations perform by clearing data out of the referenced location and writing in new data. In this case, the input data word stores the information in the data buffer register. The data buffer register then controls the inhibit drive which determines which cores contain ones or zeros.

Figure 3-5 shows an example of X and Y line selection. Logic pages 5-56 through 5-59 are schematics of the core array.

SENSE AMPLIFIER AND DATA REGISTER

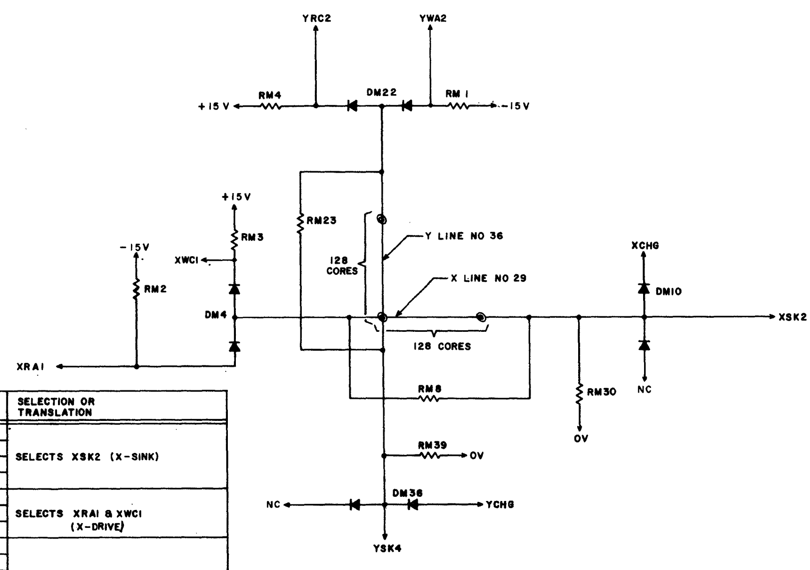
The sense amplifiers read data from the memory cores, and the data register causes data to restore into memory. Thirty-six microcircuits compose the sense amplifiers and data register. Each microcircuit package contains a dual sense amplifier and one bit of the data register. Logic pages 5-60 through 5-68 show the sense amplifiers and data register.

ONE-BIT DATA PATH

Figure 3-6 outlines the data path of bit 2 of the data word. Each half of a memory plane has a sense/ inhibit line (SA and SB). The two sense inhibit lines for each plane connect to a dual sense amplifier. Each dual sense amplifier also contains one bit of the data register. During a read operation, the sense/ inhibit line corresponding to the half of the memory plane in which the core referenced is located becomes active. If the core referenced had a one stored, the core switches to zero and generates a pulse in the sense/inhibit line. The pulse drives one input of the dual sense amplifier. When a strobe pulse (SAS-0 through SAS-3) samples the strobe gate in the sense amplifier-data register package, a one sets into the data register. Setting a one into the data register causes its output to go low.

If the core referenced had a zero stored, no pulse occurs in the sense/inhibit line, and the output of the data register remains high. Therefore, a zero (GND) appears at the output of the data buffer when the data out strobe signal occurs.

The output of the data register also drives the inhibit circuit. The outputs of the data register which correspond to zero-state cores are high. This partially enables one of the gates at location Z3, figure 3-6. Input INHT-3 or INHT-4 goes high causing current to flow in the sense/inhibit line in the half of the memory plane corresponding to the location referenced. In the read-modify-write mode, data is present at the data input buffer at the start of the write portion of the memory cycle. Write enable samples the data, and the information stores in the data buffer register. Zeros on the data input lines cause the corresponding data register outputs to be high. This enables the gates at location Z3 in figure 3-6. The proper sense/inhibit line then activates in the same manner as during the inhibit portion of a full cycle operation.



BIT NO	BIT EXAMPLE	SELECTION OR TRANSLATION
MA00	0	SELECTS XSK2 (X-SINK)
MA01	1	
MA02	0	
MA03	0	
MA04	1	SELECTS XRAI & XWCI (X-DRIVE)
MA05	0	
MA06	0	
MA07	0	SELECTS YSK4 (Y-SINK)
MA08	0	
MA09	1	
MA10	0	
MA11	0	SELECTS YRC2 & YWA2 (Y-DRIVE)
MA12	1	
MA13	0	

Figure 3-5. X and Y Line Selection Example

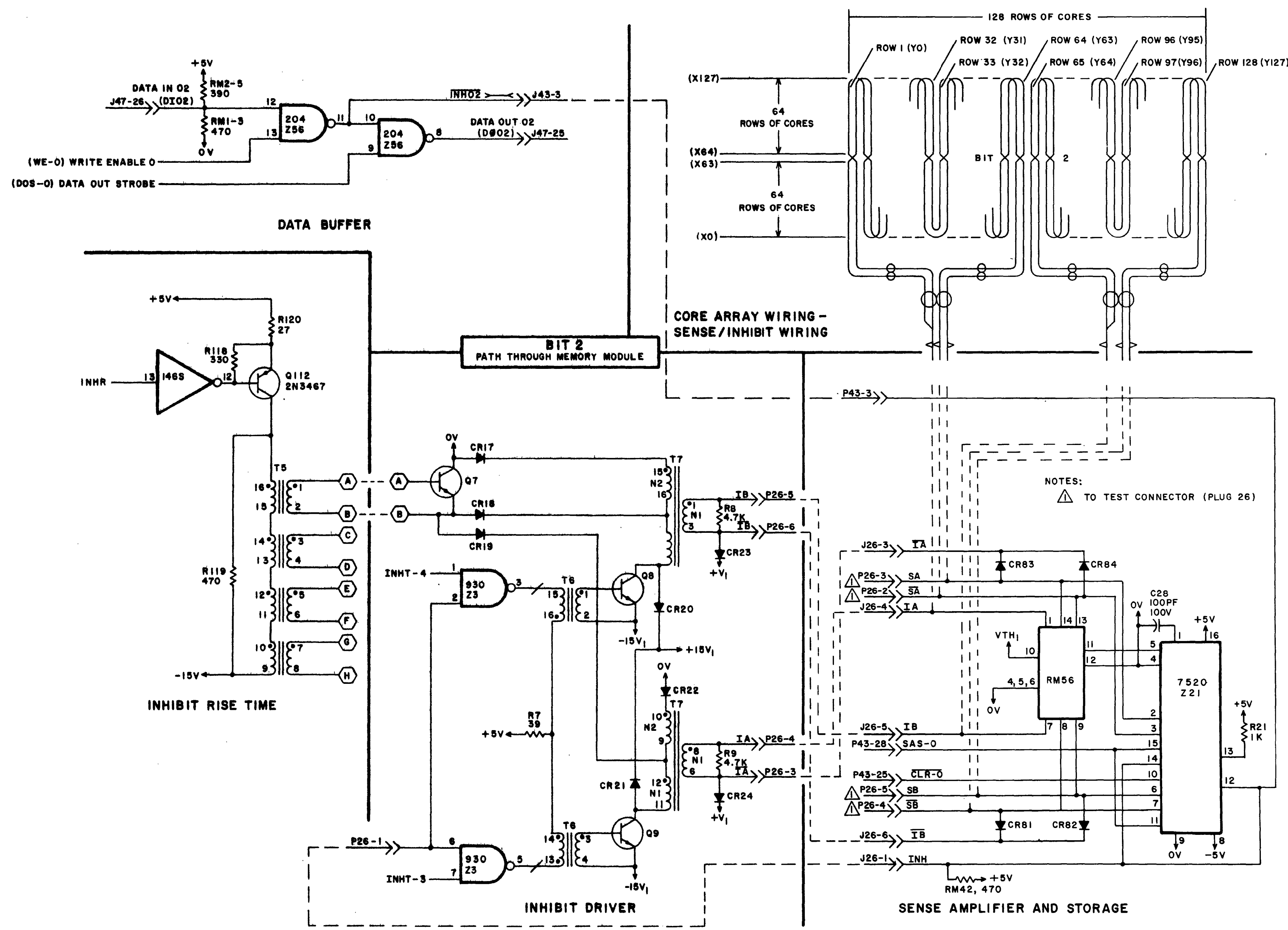


Figure 3-6. Bit 2 Data Path

INTRODUCTION

This section provides memory tests and troubleshooting charts to aid in finding problems. The memory tests usually indicate data, address, or control logic errors in the module. The charts provide possible causes of the trouble.

Before troubleshooting the module, be sure the problem is not external. Check the power supply voltages, and see that the power supply regulates properly. Improper programming causes errors. The accessibility of the interface lines makes this a reasonable place to start troubleshooting. Substituting a spare module isolates problems quickly.

RECOMMENDED TEST EQUIPMENT

Equipment	Manufacturer	Type
Oscilloscope	Tektronix	454 series or equivalent
Current probe	Tektronix	P6021 or equivalent
Voltage probe	Tektronix	10:1 attenuation or equivalent
Digital multimeter	Fairchild	Model 7050 or equivalent
VOM	Triplett	630-NA or equivalent

MEMORY TESTS

The following externally generated test patterns are useful for troubleshooting.

ALL ONES

Sequentially load the memory with logic ones. Next, do a read-restore operation. Ones should unload from the storage location of each address. Any zero on the data out lines is an error. Record the address and bit or bits in error.

ALL ZEROS

Proceed as in the all ones test, but load and unload the memory with zeros.

WORST PATTERN AND WORST PATTERN COMPLEMENT

These patterns cause the worst-case noise conditions on the output lines during read-out. The following logic equations relate addresses to data content for writing the worst patterns into memory:

$$\text{Worst Pattern} = \overline{2^6} \cdot \overline{2^7} + 2^6 \cdot 2^7$$

$$\overline{\text{Worst Pattern}} = 2^6 \cdot \overline{2^7} + \overline{2^6} \cdot 2^7$$

Read the memory and record any address and bit errors.

ERRORS

Errors discovered while running the test patterns are usually associated with the data, address, or control logic in the memory module.

CONTROL ERRORS

Failure to perform operations or erratic operations usually indicates a control problem. Control problems also cause data and address errors. Faulty signals from the external equipment can cause control malfunctions. Refer to figure 4-1 and the interface timing diagrams (figures 2-4 through 2-7) in section 2 when troubleshooting control errors.

ADDRESS ERRORS

Address errors affect all bits in a data word because decoded address information specifies an X and Y drive line in order to reference memory. Malfunctioning drive line control circuits cause errors at all addresses on the drive line. Failure of the address register, drive switches, or decoders causes address errors.

If the same address errors occur in all modules of a multimodule system, check the address input signals, line connections, and address registers. If all errors are associated with one module, substitute a spare module or swap with a module at a different location. This isolates the problem to one module. Refer to figure 4-2 when troubleshooting address errors.

Table 4-1 is an aid to troubleshooting to circuit and component levels. The table associates the address bits with circuits, components, and logic diagrams. The address bits are grouped to show the relationship to the X and Y memory drive lines. An example address (octal) of 0-4-3-11 is shown. The circuits and components which cause drive current to flow during a read operation do not necessarily cause current to flow during write operation.

DATA ERRORS

Data errors usually occur in the same bit position of all data words during either a read or write operation. Check the sense amplifier and related circuits for bit errors during a read operation. Check the inhibit driver and related circuits for bit errors during a write operation. Address 2^{13} divides the bit into two 8K segments for inhibit-sense. Refer to figure 4-3 when troubleshooting data errors.

MEMORY ERRORS SYMPTOM

Memory does not perform any operation after an initial period of error free operation

Replace with spare module

Error persists
(or spare not available)

Possible cause of error

- Logic zero on data save line
- Logic zero on external reset
- Voltage regulation out of tolerance (± 5%)
- Open interface connections
- Required control signals
- Required signal timing

Memory does not perform any operation during initial checkout

Check for:

- Interface signal timing errors
- Interface wiring errors
- Required voltages
- Required voltage regulation
- Required control signal levels
- Positive seating of module connectors
- Module select (switch is not set properly)
- Module not inserted properly in connectors

MEMORY PERFORMS AT LEAST ONE OPERATION, BUT NOT:

Clear-write

Check for:

- Logic one RMW signal
- Logic zero read-write signal

Read-restore

Check for:

- Logic one RMW signal
- Logic one read-write signal

Read-modify-write

Check for:

- Logic zero RMW signal
- Logic one or zero read-write signal
- Cycle continue signal

Figure 4-1. Control Errors

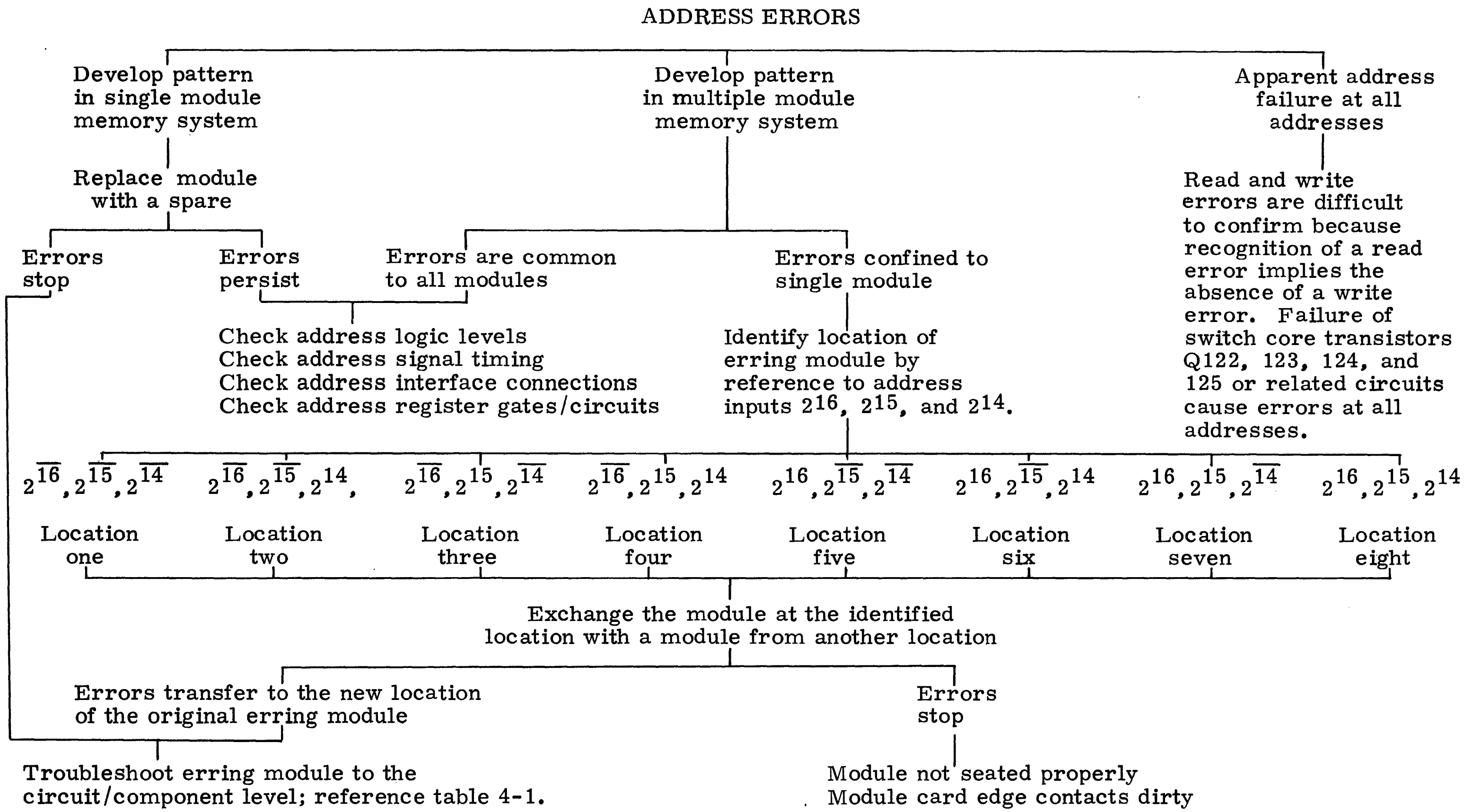


Figure 4-2. Address Errors

TABLE 4-1. RELATIONSHIP OF ADDRESS BITS, CIRCUITS, AND LOGIC DIAGRAMS

Address Bits	2^{16} 2^{15} 2^{14}	2^{13} 2^{12} 2^{11}	2^{10} 2^{9} 2^{8} 2^{7}	2^{6} 2^{5} 4	2^{3} 2^{2} 2^{1} 2^{0}
Function	Module 0 through 7.	Y read switches, logic page 5-28. Y write drivers, logic page 5-27. (diode end of stack)	Y read drivers and Y write switches, logic pages 5-31 and 5-32. (sink end of stack)	X read drivers, logic page 5-25. X write switches, logic page 5-26. (diode end of stack)	X read switches and X write drivers. Logic pages 29 and 30. (sink end of stack)
Address Octal Address		$\overline{2^{13}}$ $\overline{2^{12}}$ $\overline{2^{11}}$ 0	$\overline{2^{10}}$ 2^{9} $\overline{2^{8}}$ $\overline{2^{7}}$ 4	$\overline{2^{6}}$ 2^{5} 2^{4} 3	2^{3} $\overline{2^{2}}$ 2^{1} 2^{0} 11
X-Y designation logic page no. in ( ).		YRC0 (5-28) YWA0 (5-27)	YSK4 (5-31)	XRA3 (5-25) XWC3 (5-26)	XSK11 (5-30)
Possible circuitry for cause of problem		QM3, pin 5-7 CR454 T74 Z123 P4, term 9 QM1, pin 1, 2, 3 T72 Z118 P2, term 1	QM9, pin 1-7 CR306 CR324 CR315 CR327 T81 Z117 P1, term 14	QM5, pin 12-14 T76 Z119 P2, term 12 QM7, pin 8-10 CR462 T78 Z122 P4, term 4	QM15, pin 8-10 and 12-14 CR177 CR412 CR419 CR430 T87 Z121 P3, term 12

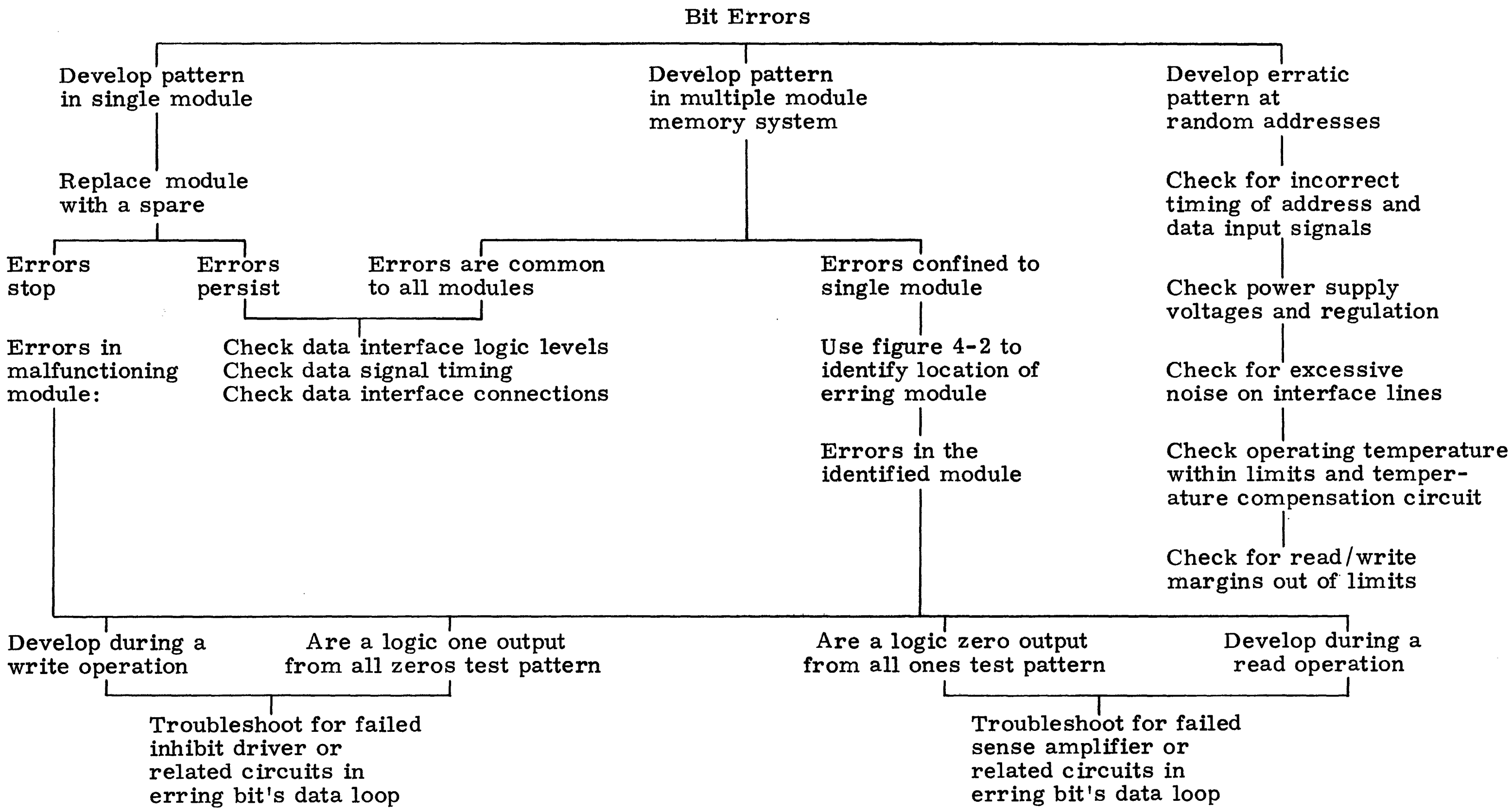


Figure 4-3. Data Errors

SHEET REVISION STATUS	REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
	01	—	RELEASED CLASS B	DWA	4-4-5		

REVISION RECORD

NOTES:

1. UNLESS OTHERWISE SPECIFIED
   - A. ALL RESISTORS ARE ¼W 5% AND IN OHMS
   - B. ALL CAPACITORS ARE IN MICRO FARADS
   - C. ALL TRANSISTORS ARE 2N3725
   - D. ALL DIODES ARE IN4607
2. PIN 1 OF ALL RESISTOR MODULES (RM) WILL CONNECT TO +5V OR 0 VOLTS
3. +5V CONNECTS TO ALL 390Ω MODULES AND 0V CONNECTS TO 470Ω MODULES
4. RESISTOR DESIGNATION R211 THRU R240 WAS NOT USED
5. ⇄ THIS SYMBOL REPRESENTS A MALE CONNECTOR SUCH AS CARD EDGE OR A MALE PIN THAT MATES TO CORE ARRAY
6. —< THIS SYMBOL REPRESENTS A FEMALE THAT MATES TO CORE ARRAY
7. ▶— THIS SYMBOL WILL BE FOUND ON LEFT BORDER, IT INDICATES DIRECTION OF SIGNAL FLOW. TO LEFT OF ARROW WILL BE SIGNAL NAME OR MNEMONIC AND IN PARENTHESIS ( ) THE ORIGINATING PAGE.
8. —▶ THIS SYMBOL WILL BE FOUND ON RIGHT BORDER, IT INDICATES DIRECTION OF SIGNAL FLOW. TO THE RIGHT OF ARROW WILL BE SIGNAL NAME OR MNEMONIC AND IN PARENTHESIS ( ) THE PAGE NUMBERS OF ALL DESTINATIONS
9. 32K X18 CONFIGURATION REQUIRES THAT TWO DATA IN AND DATA OUT BITS MUST BE CONNECTED TOGETHER SEE CHART.

	INTERNAL ADDRESS CONTROL			
	$\overline{MA17}$		MA17	
BYTE 0	PIN	INTERNAL BIT #	PIN	INTERNAL BIT #
DATA IN BIT 00	J47-21	00	J47-29	09
" " " 01	J47-23	01	J47-49	10
" " " 02	J47-26	02	J47-45	11
" " " 03	J47-31	03	J47-55	12
" " " 04	J47-37	04	J47-51	13
" " " 05	J47-33	05	J47-59	14
" " " 06	J47-44	06	J47-62	15
" " " 07	J47-28	07	J47-64	16
" " " 08	J47-39	08	J47-68	17
BYTE 1				
DATA IN BIT 09	J46-56	18	J46-40	27
" " " 10	J46-58	19	J46-38	28
" " " 11	J46-53	20	J46-34	29
" " " 12	J46-61	21	J46-28	30
" " " 13	J46-47	22	J46-31	31
" " " 14	J46-51	23	J46-26	32
" " " 15	J46-59	24	J46-22	33
" " " 16	J46-43	25	J46-19	34
" " " 17	J46-14	26	J46-16	35
BYTE 0				
DATA OUT BIT 00	J47-22	00	J47-30	09
" " " 01	J47-24	01	J47-50	10
" " " 02	J47-25	02	J47-46	11
" " " 03	J47-32	03	J47-56	12
" " " 04	J47-38	04	J47-52	13
" " " 05	J47-34	05	J47-57	14
" " " 06	J47-43	06	J47-61	15
" " " 07	J47-27	07	J47-63	16
" " " 08	J47-40	08	J47-67	17
BYTE 1				
DATA OUT BIT 09	J46-55	18	J46-39	27
" " " 10	J46-57	19	J46-37	28
" " " 11	J46-54	20	J46-33	29
" " " 12	J46-62	21	J46-27	30
" " " 13	J46-48	22	J46-32	31
" " " 14	J46-52	23	J46-25	32
" " " 15	J46-60	24	J46-21	33
" " " 16	J46-44	25	J46-20	34
" " " 17	J46-13	26	J46-15	35

DETACHED LISTS

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES

3 PLACE ± 2 PLACE ± ANGLES ±

DO NOT SCALE DRAWING

MATERIAL

FINISH

CONTROL DATA CMMD OPERATIONS

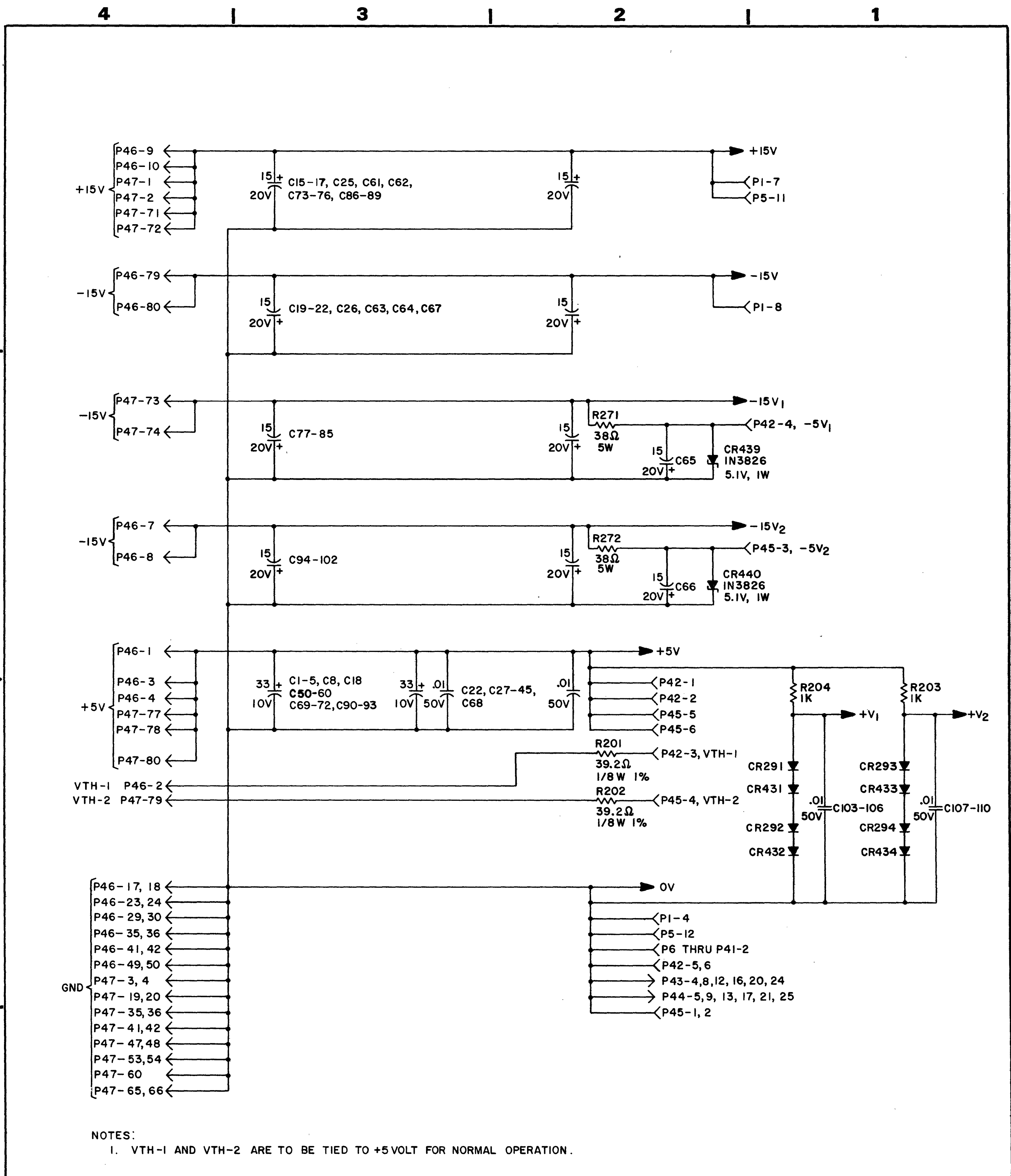
FIRST USED ON		
DWN	D. ANDERSON	4-4-75
CHKD	Dorothy G. Howard	4/4/75
ENGR		
MFG		
APPR		

TITLE

MEMORY ELECTRONICS
BOARD SCHEMATIC OEM
16K X 36 & 32K X 18

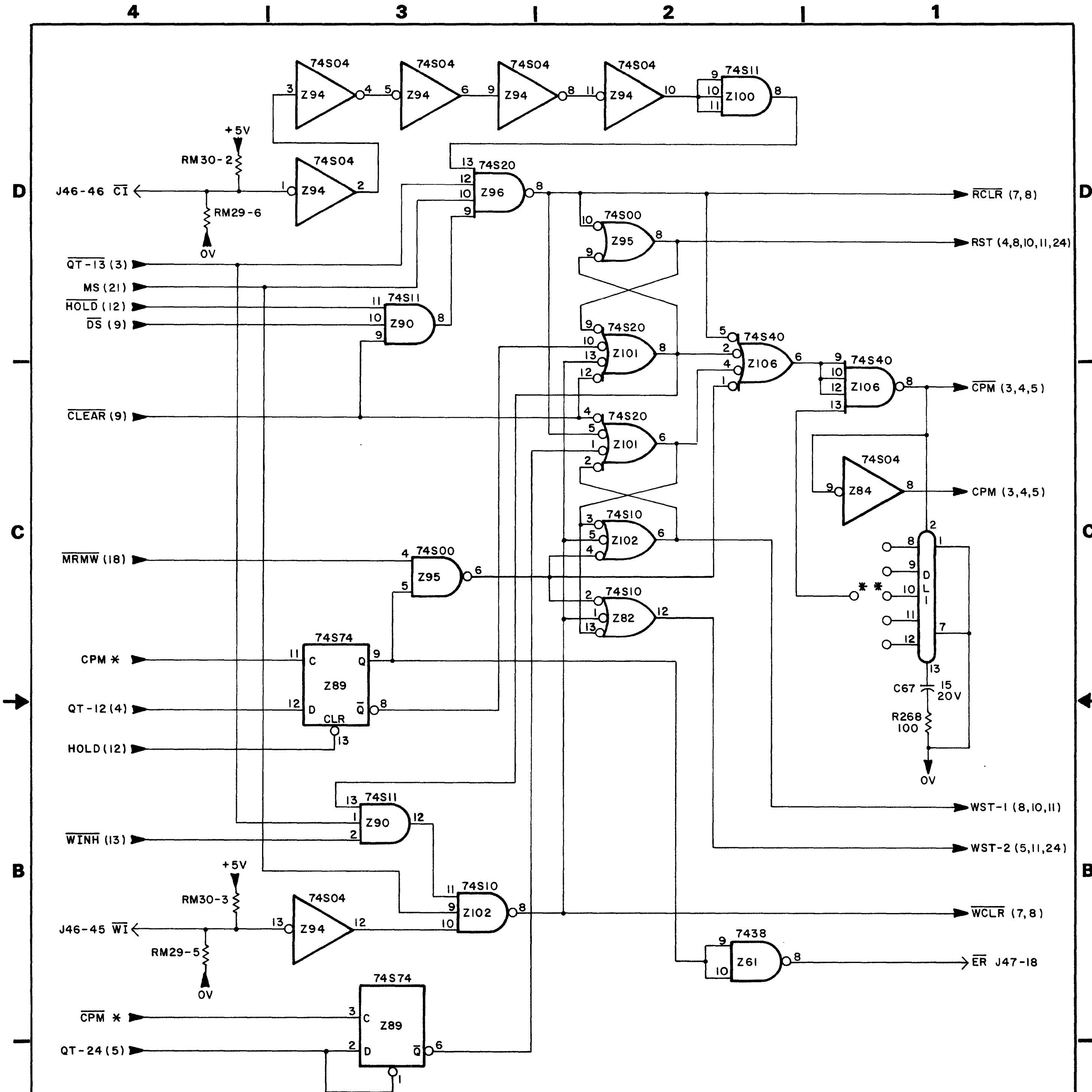
CODE IDENT | C | DRAWING NO 82843000

SCALE | SHEET 1 OF 54



NOTES:
1. VTH-1 AND VTH-2 ARE TO BE TIED TO +5 VOLT FOR NORMAL OPERATION.

CONTROL DATA CMMD OPERATIONS	MEMORY ELECTRONICS BOARD SCHEMATIC OEM 16K X 36 & 32K X 18	CODE IDENT 54211	C	DWG NO 82843000	REV 01
				SHEET 2	



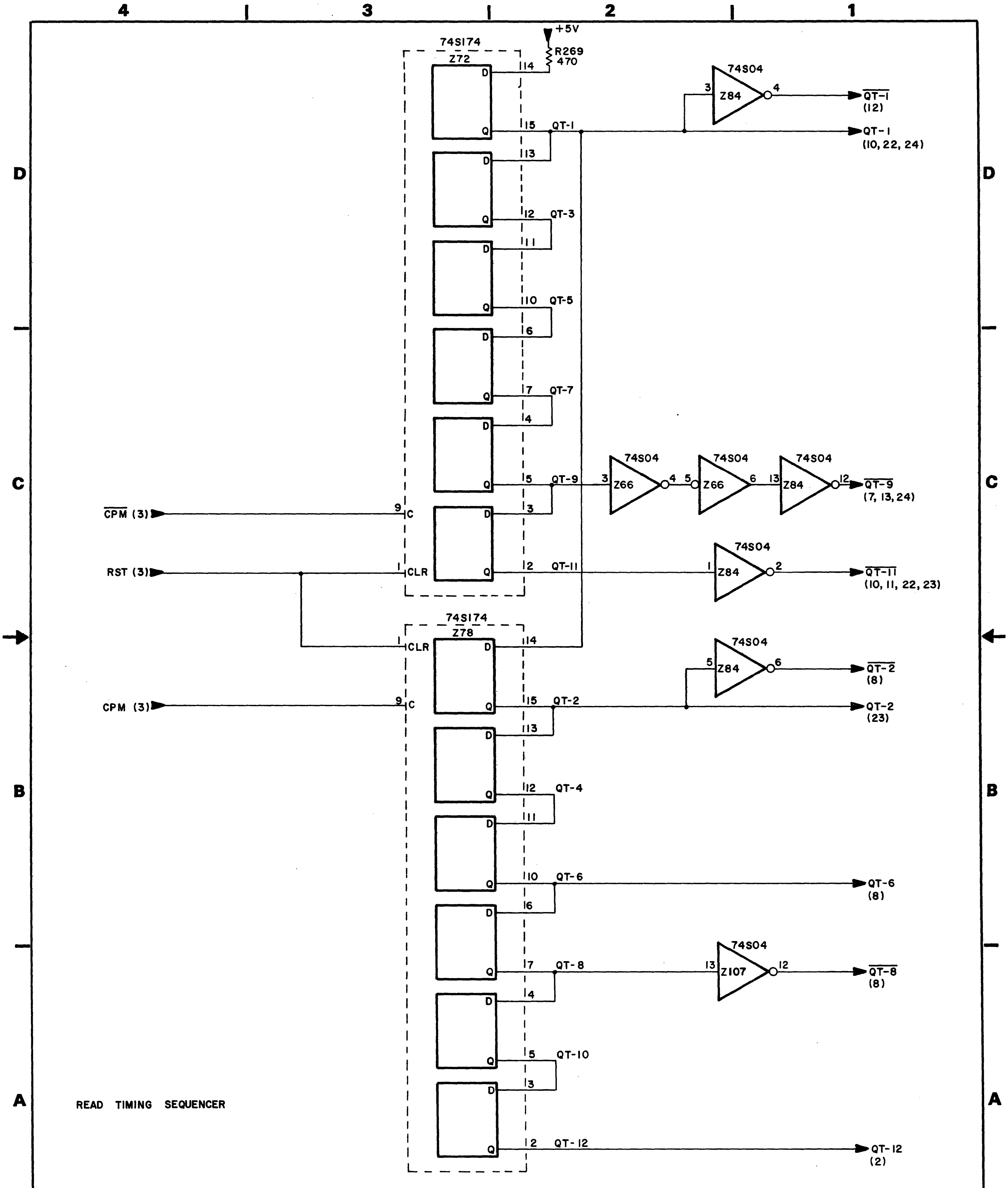
NOTE:

* OUTPUT LOCATED ON THIS PAGE.

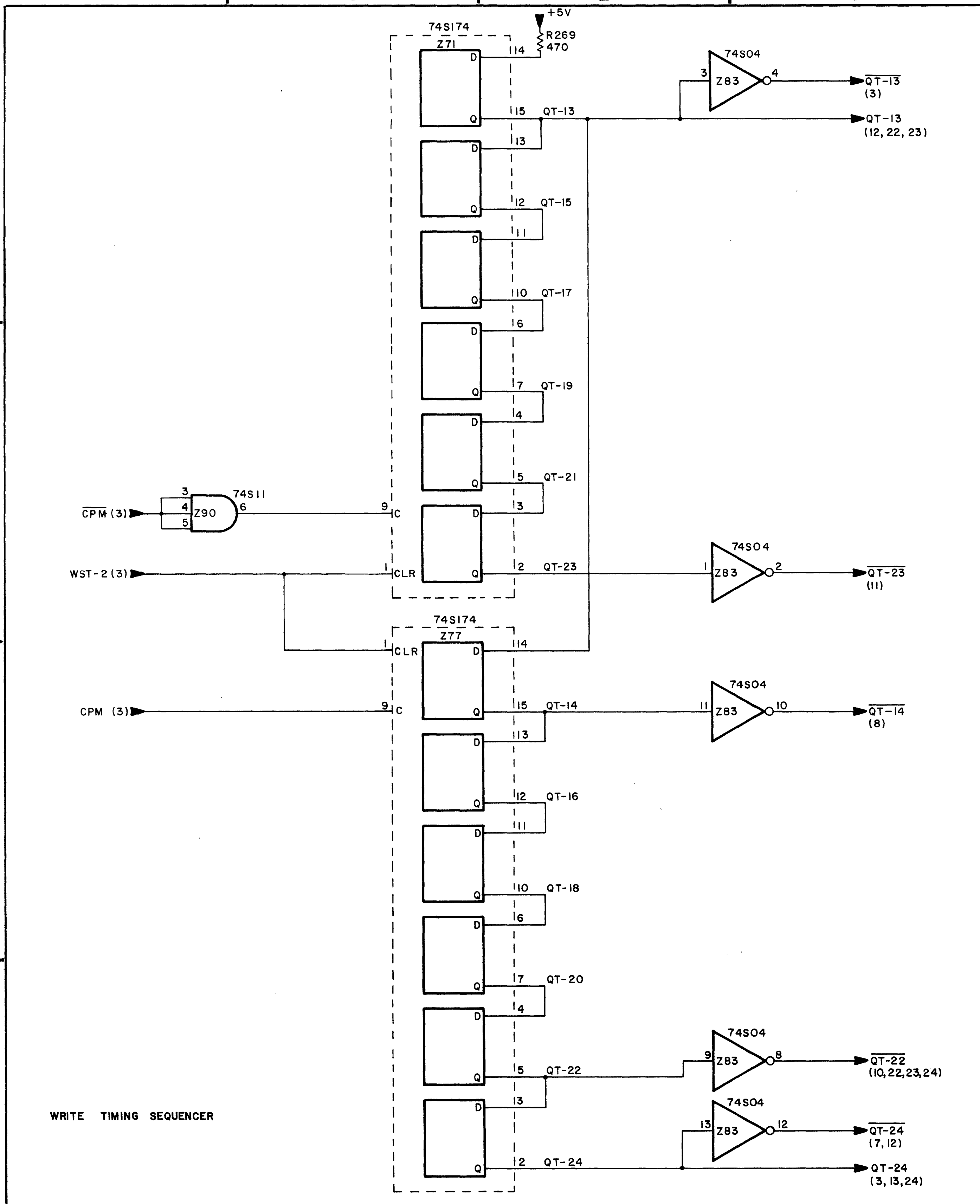
** WIRE JUMPER DETERMINED IN TEST.

TIMING CONTROL

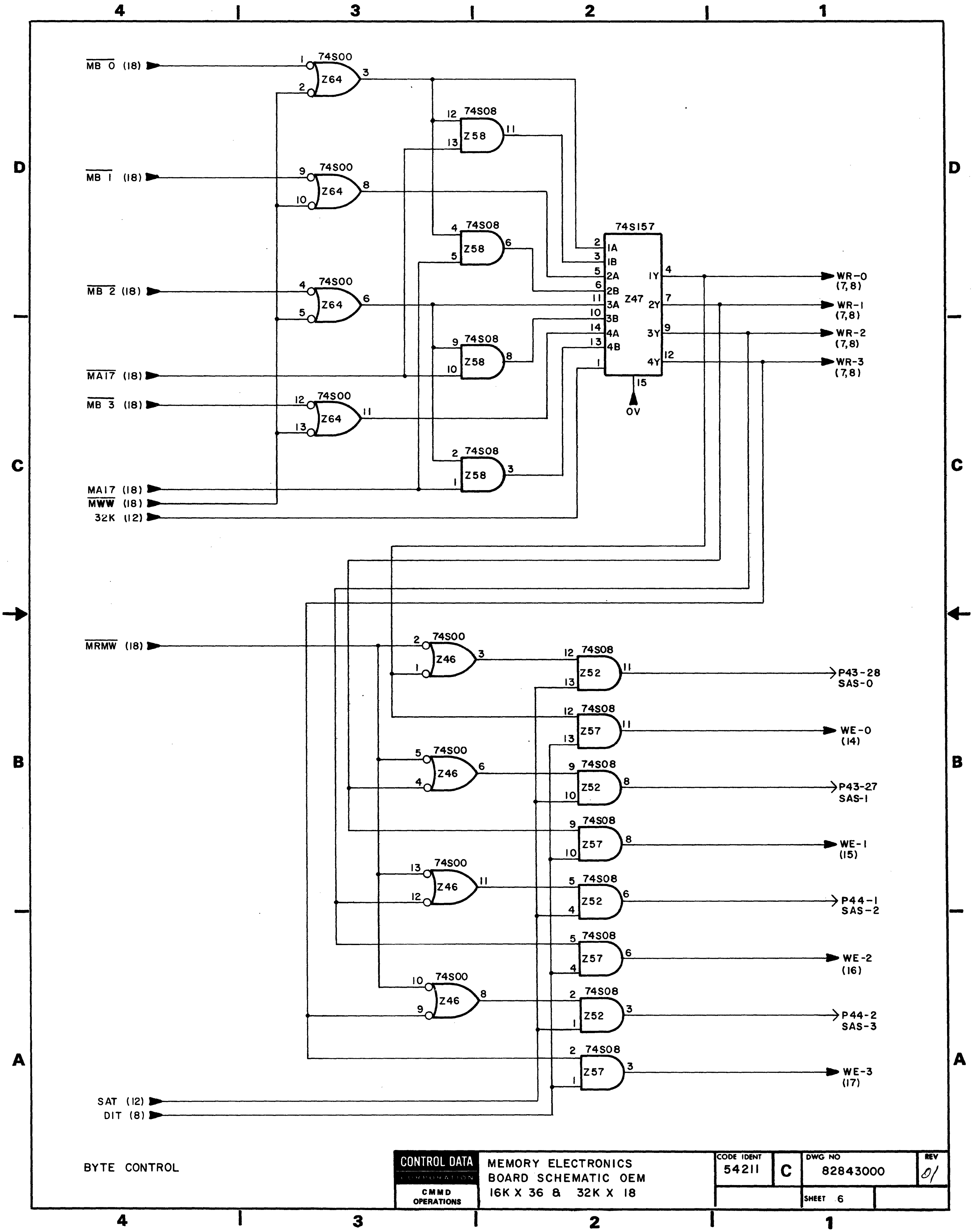
CONTROL DATA CMMD OPERATIONS	MEMORY ELECTRONICS BOARD SCHEMATIC OEM 16K X 36 AND 32K X 18	CODE IDENT 54211	C	DWG NO 82843000	REV 01
				SHEET 3	

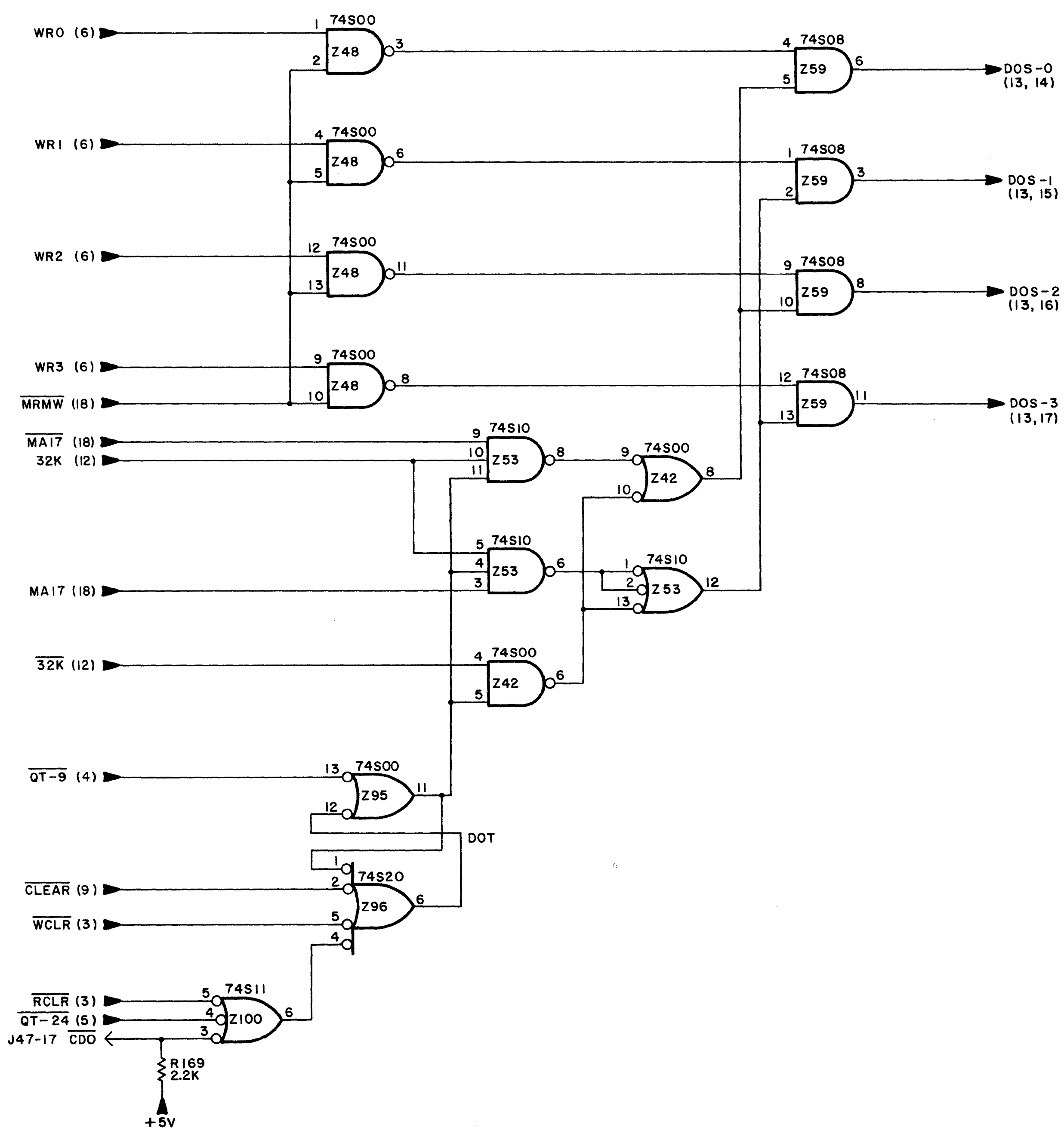


CONTROL DATA CMMD OPERATIONS	MEMORY ELECTRONICS BOARD SCHEMATIC OEM 16K X 36 & 32K X 18	CODE IDENT 54211	C	DWG NO 82843000	REV 01
				SHEET 4	



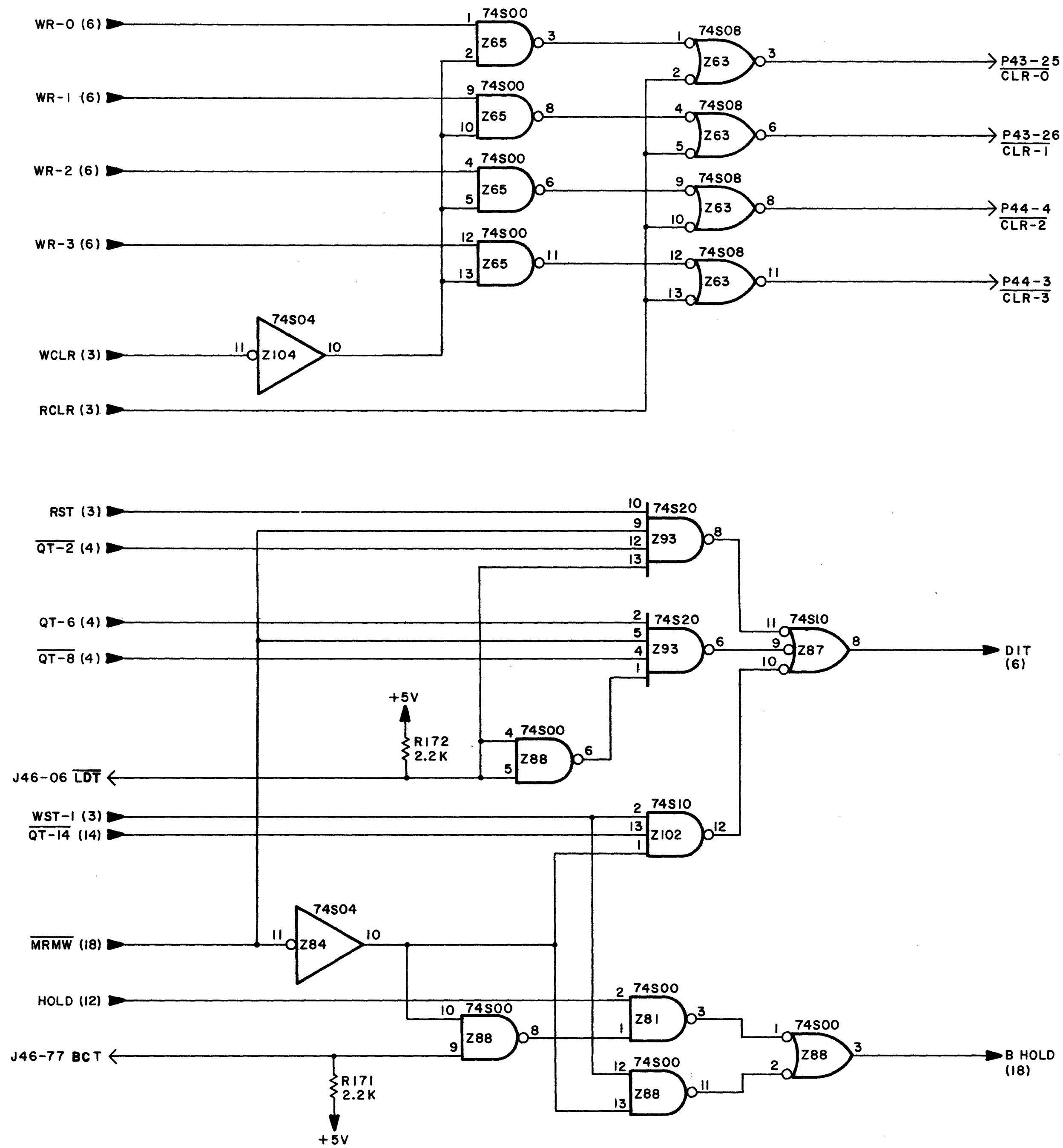
CONTROL DATA CMMD OPERATIONS	MEMORY ELECTRONICS BOARD SCHEMATIC OEM 16K X 36 & 32K X 18	CODE IDENT 54211	C	DWG NO 82843000 / REV 01 / SHEET 5


MB 0 (18)
MB 1 (18)
MB 2 (18)
MA17 (18)
MB 3 (18)
MA17 (18)
MWW (18)
32K (12)
MRMW (18)
SAT (12)
DIT (8)
74S00 Z64
74S08 Z58
74S157 Z47
74S00 Z46
74S08 Z52
74S08 Z57
0V
WR-0 (7,8)
WR-1 (7,8)
WR-2 (7,8)
WR-3 (7,8)
P43-28 SAS-0
WE-0 (14)
P43-27 SAS-1
WE-1 (15)
P44-1 SAS-2
WE-2 (16)
P44-2 SAS-3
WE-3 (17)
BYTE CONTROL
CONTROL DATA CORPORATION
CMMD OPERATIONS
MEMORY ELECTRONICS
BOARD SCHEMATIC OEM
16K X 36 & 32K X 18
CODE IDENT 54211
C
DWG NO 82843000
REV 01
SHEET 6



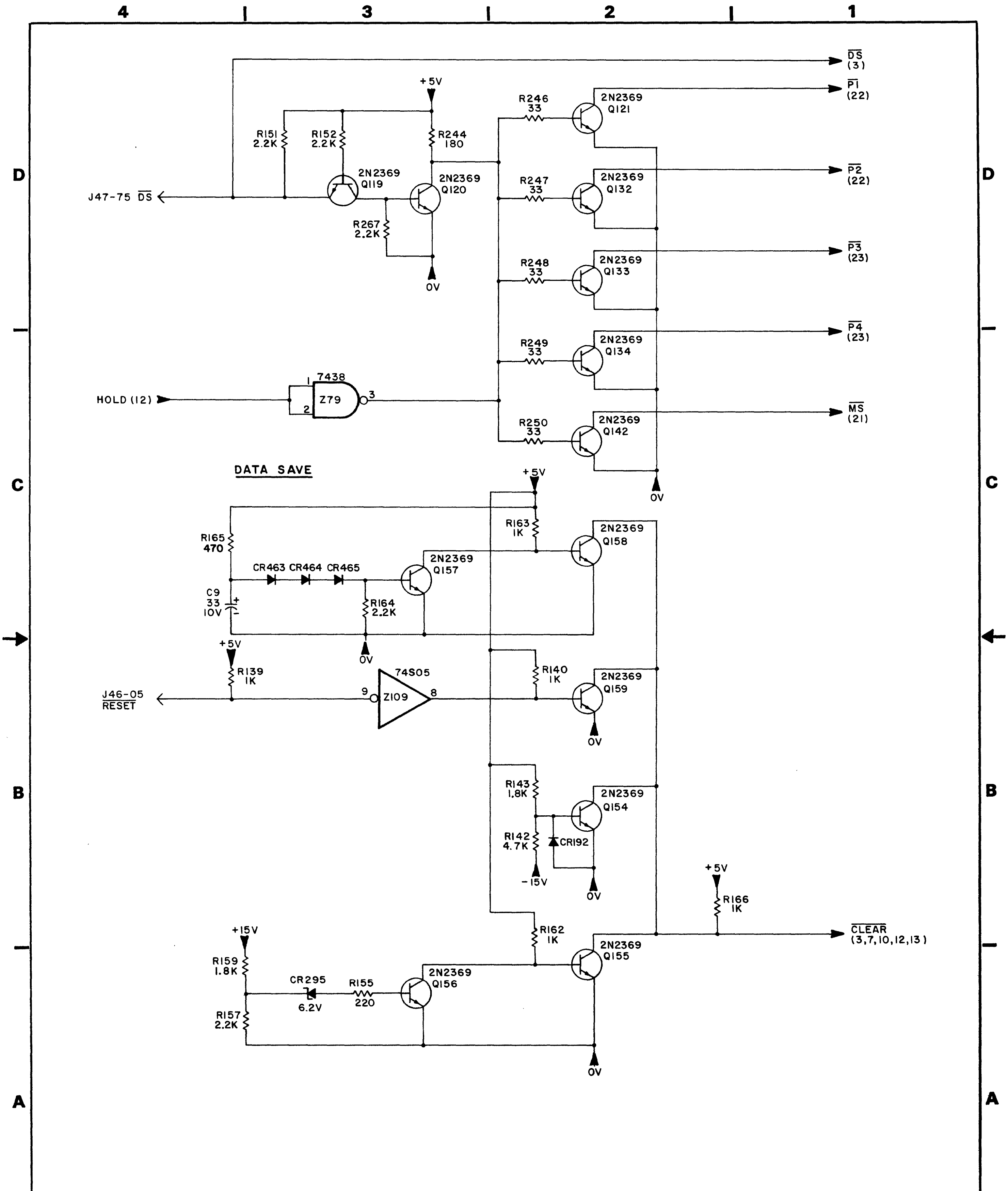
BYTE CONTROL

CONTROL DATA CORPORATION / CMMD OPERATIONS	MEMORY ELECTRONICS BOARD SCHEMATIC OEM 16K X 36 & 32K X 18	CODE IDENT 54211	C	DWG NO 82843000	REV 01
				SHEET 7	



BYTE CONTROL

CONTROL DATA CORPORATION CMMD OPERATIONS	MEMORY ELECTRONICS BOARD SCHEMATIC OEM 16K X 36 & 32K X 18	CODE IDENT 54211	C	DWG NO 82843000	REV 01
				SHEET 8	



CONTROL DATA CORPORATION
CMMD OPERATIONS

MEMORY ELECTRONICS BOARD SCHEMATIC OEM 16K X 36 AND 32K X 18

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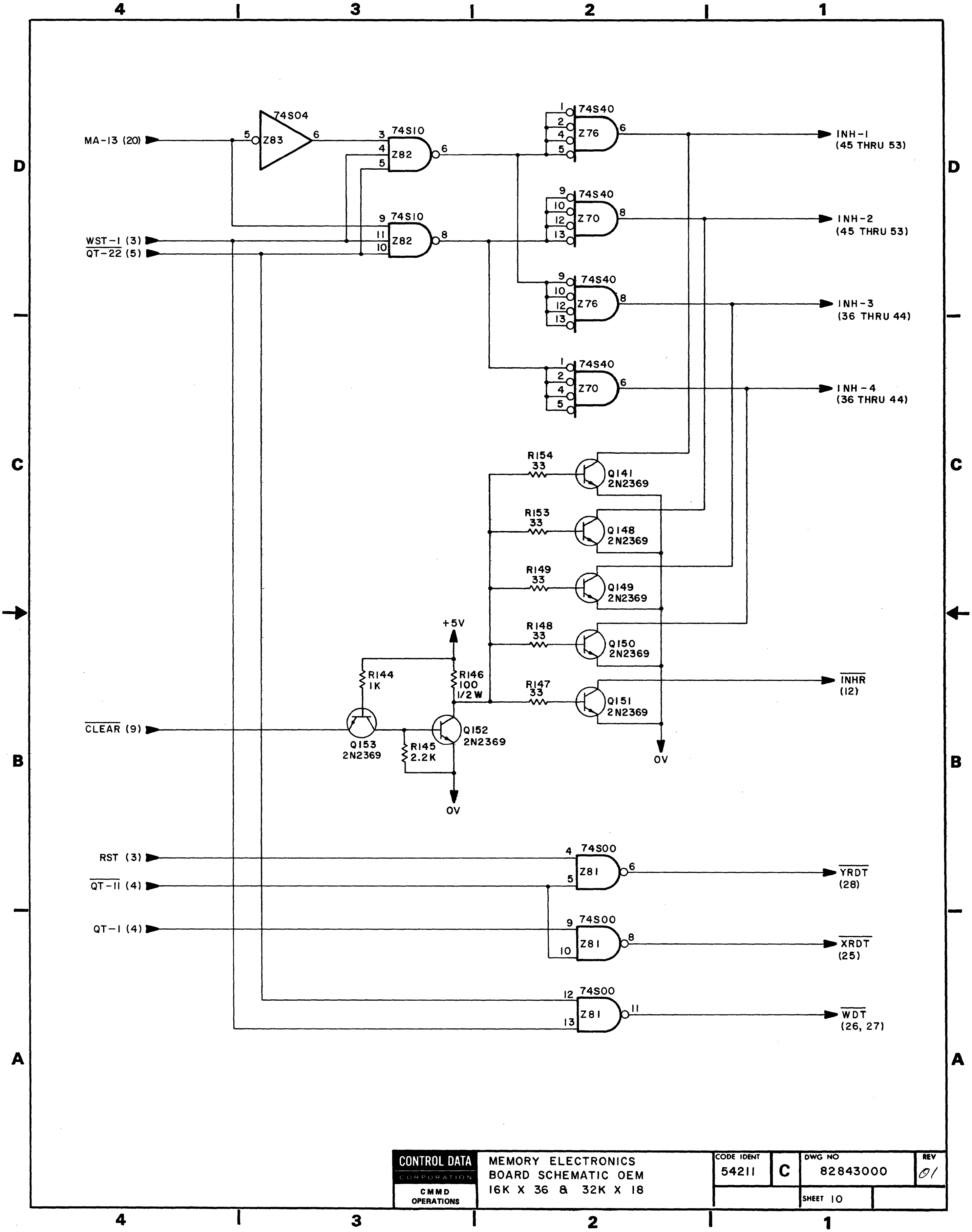
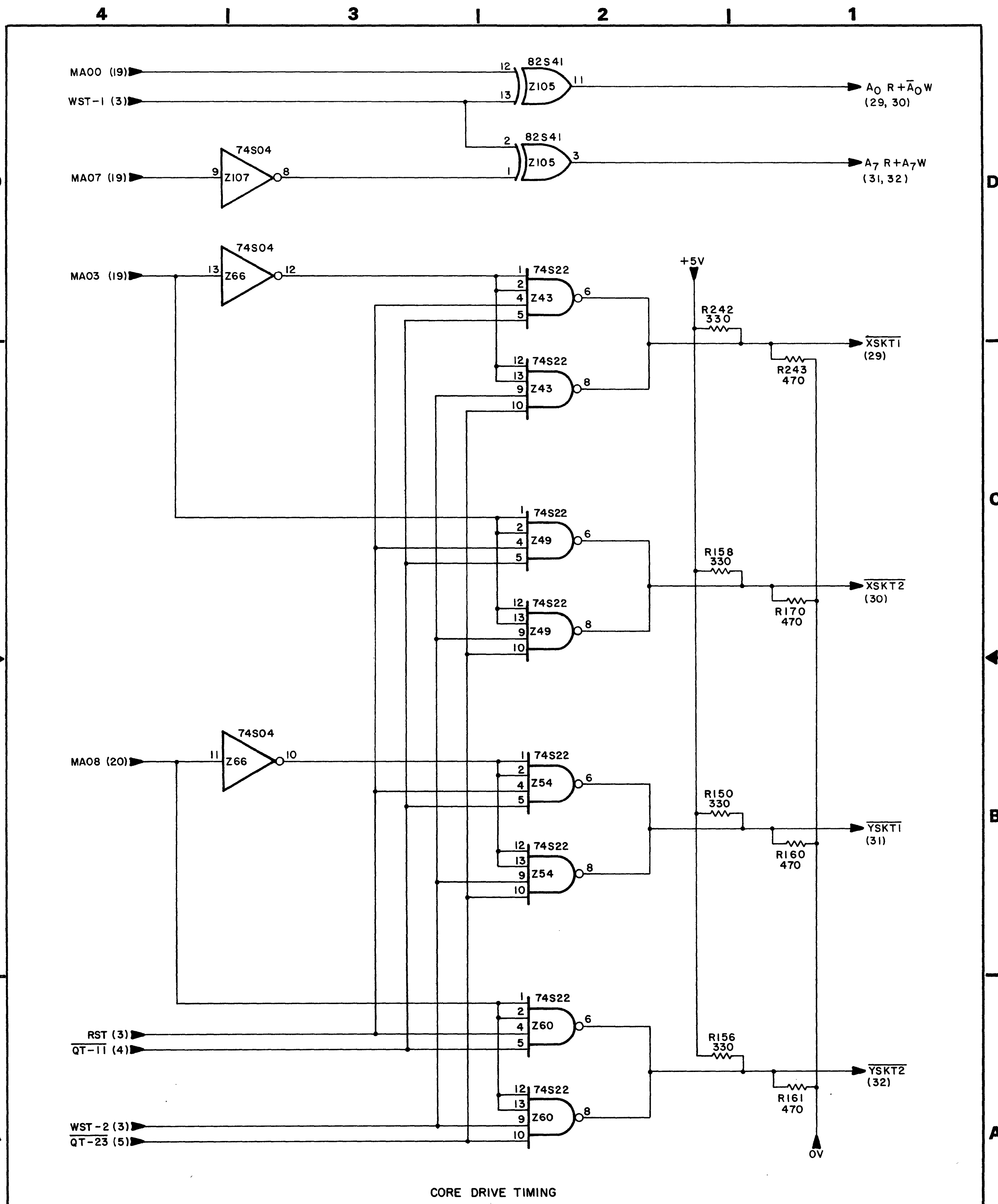
54211	C	82843000	01
		SHEET 9	

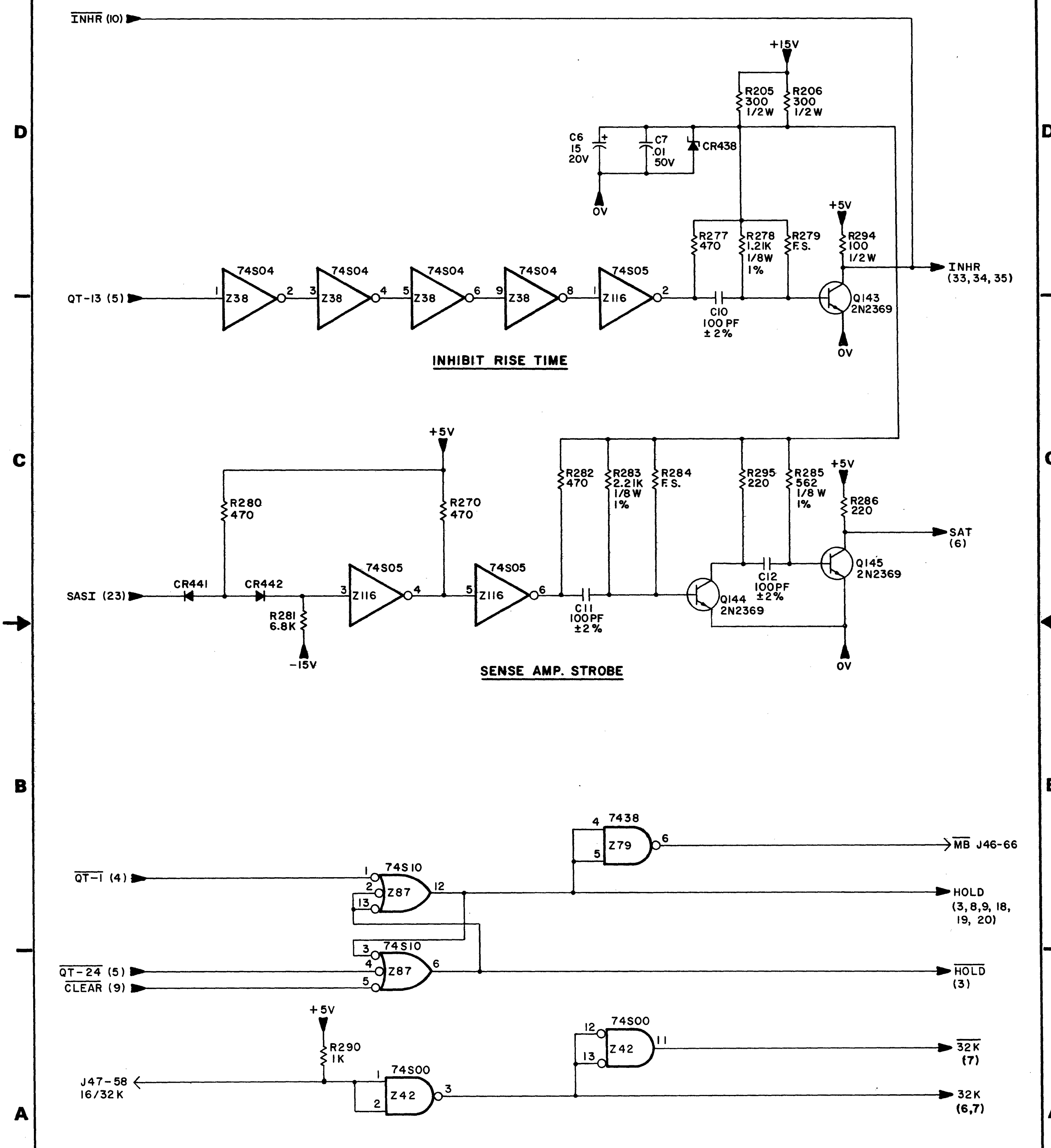


MA-13 (20)
WST-1 (3)
QT-22 (5)
74S04
Z83
74S10
Z82
74S40
Z76
Z70
INH-1
(45 THRU 53)
INH-2
(45 THRU 53)
INH-3
(36 THRU 44)
INH-4
(36 THRU 44)
R154
33
Q141
2N2369
R153
33
Q148
2N2369
R149
33
Q149
2N2369
R148
33
Q150
2N2369
R147
33
Q151
2N2369
INHR
(12)
+5V
R144
1K
R146
100
1/2 W
CLEAR (9)
Q153
2N2369
Q152
2N2369
R145
2.2K
0V
RST (3)
QT-11 (4)
QT-1 (4)
74S00
Z81
YRDT
(28)
XRDT
(25)
WDT
(26, 27)
CONTROL DATA
CORPORATION
CMMD
OPERATIONS
MEMORY ELECTRONICS
BOARD SCHEMATIC OEM
16K X 36 & 32K X 18
CODE IDENT
54211
C
DWG NO
82843000
REV
01
SHEET 10



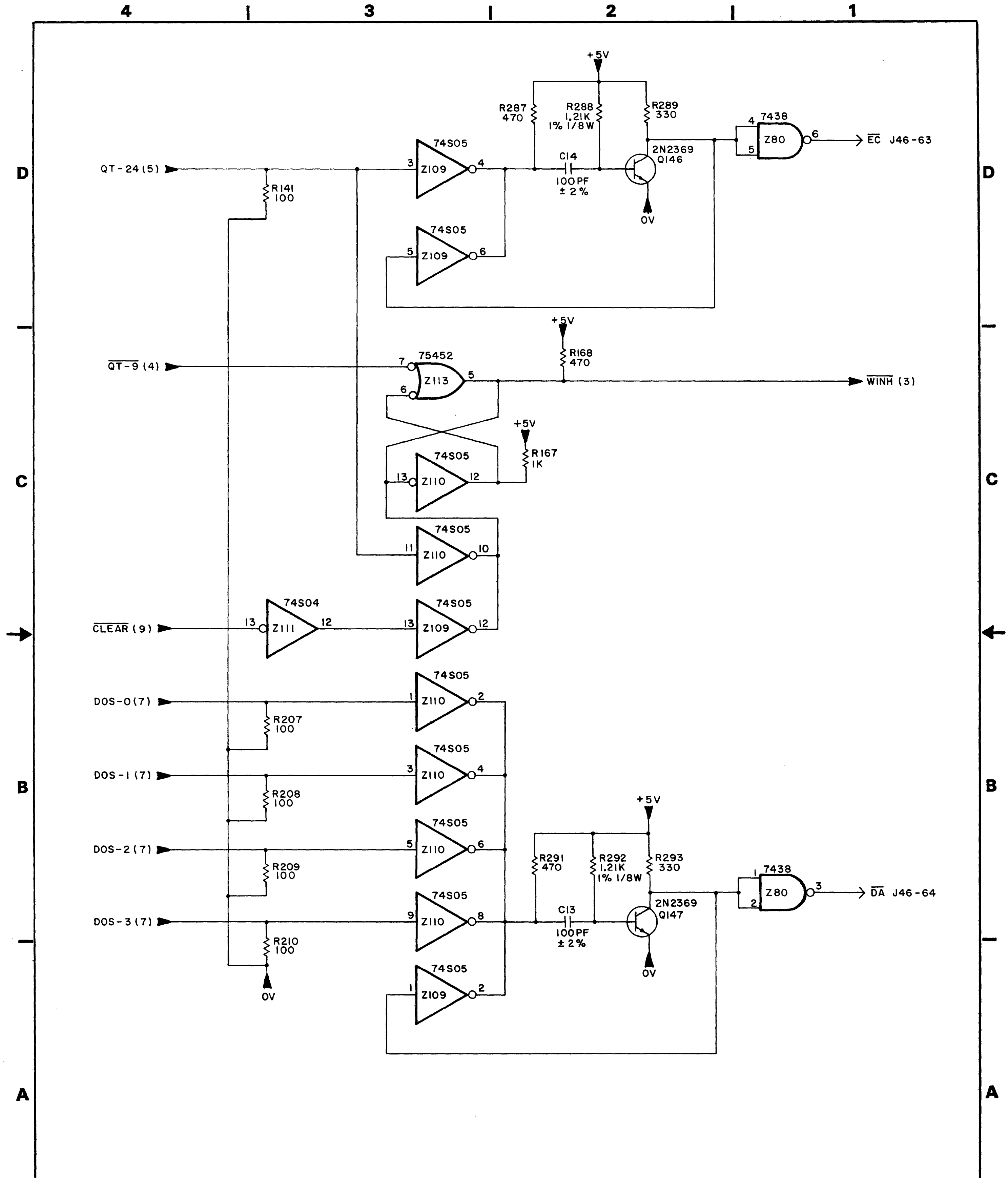
CORE DRIVE TIMING

CONTROL DATA CMMD OPERATIONS	MEMORY ELECTRONICS BOARD SCHEMATIC OEM 16K X 36 & 32K X 18	CODE IDENT 54211	C	DWG NO 82843000	REV 01
				SHEET 11	

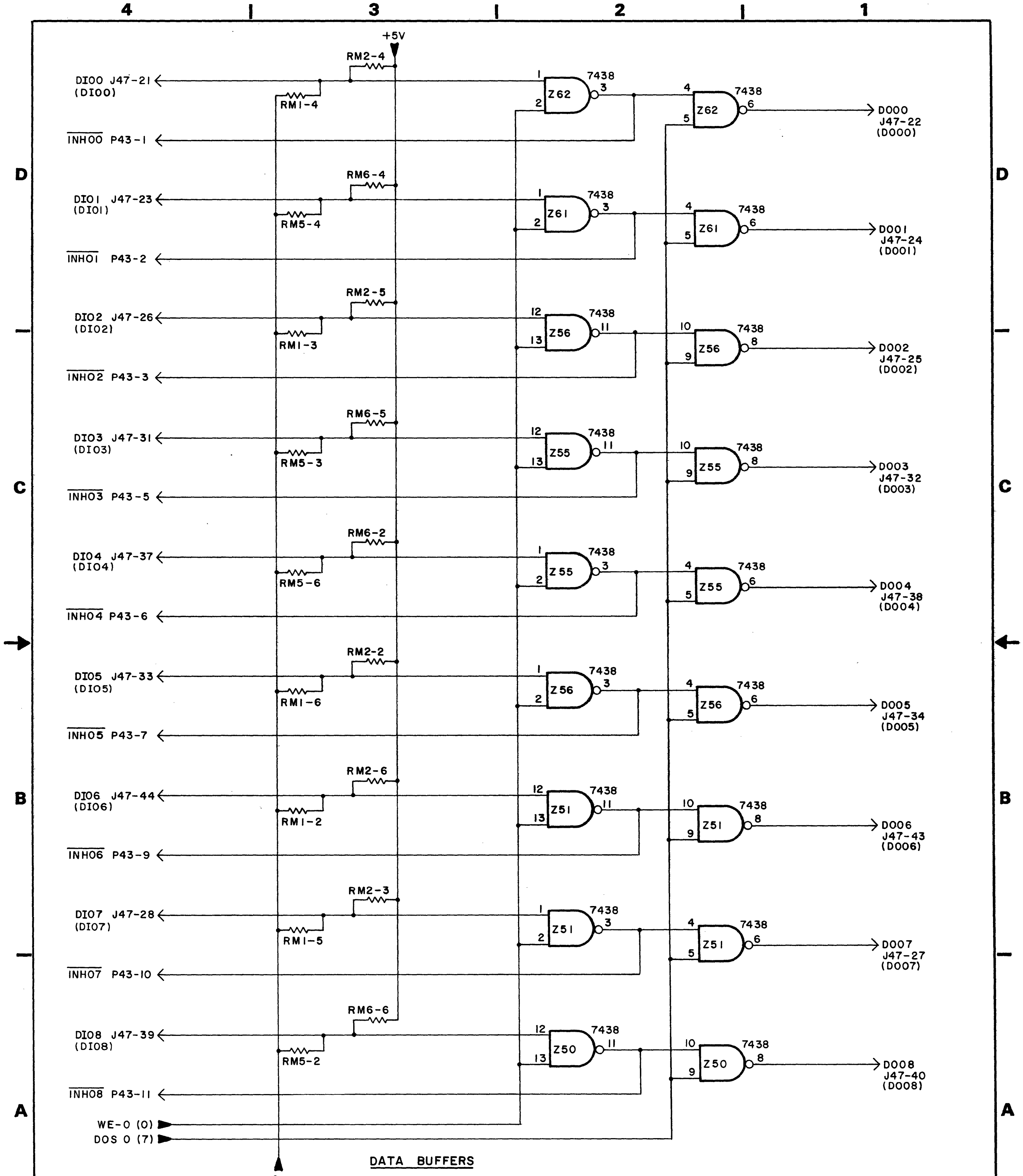


NOTES:
1. R279 AND 284 ARE FACTORY SELECT RESISTORS DETERMINED IN TEST.
2. WHEN J47-58 IS LEFT OPEN, 16K X 36 MEMORY MODULE IS CONFIGURATED AND WHEN J47-58 IS GROUNDED, 32K X 18 MEMORY MODULE IS CONFIGURATED.

CONTROL DATA CORPORATION CMMD OPERATIONS	MEMORY ELECTRONICS BOARD SCHEMATIC OEM 16K X 36 & 32K X 18	CODE IDENT 54211	C	DWG NO 82843000	REV 01
				SHEET 12	



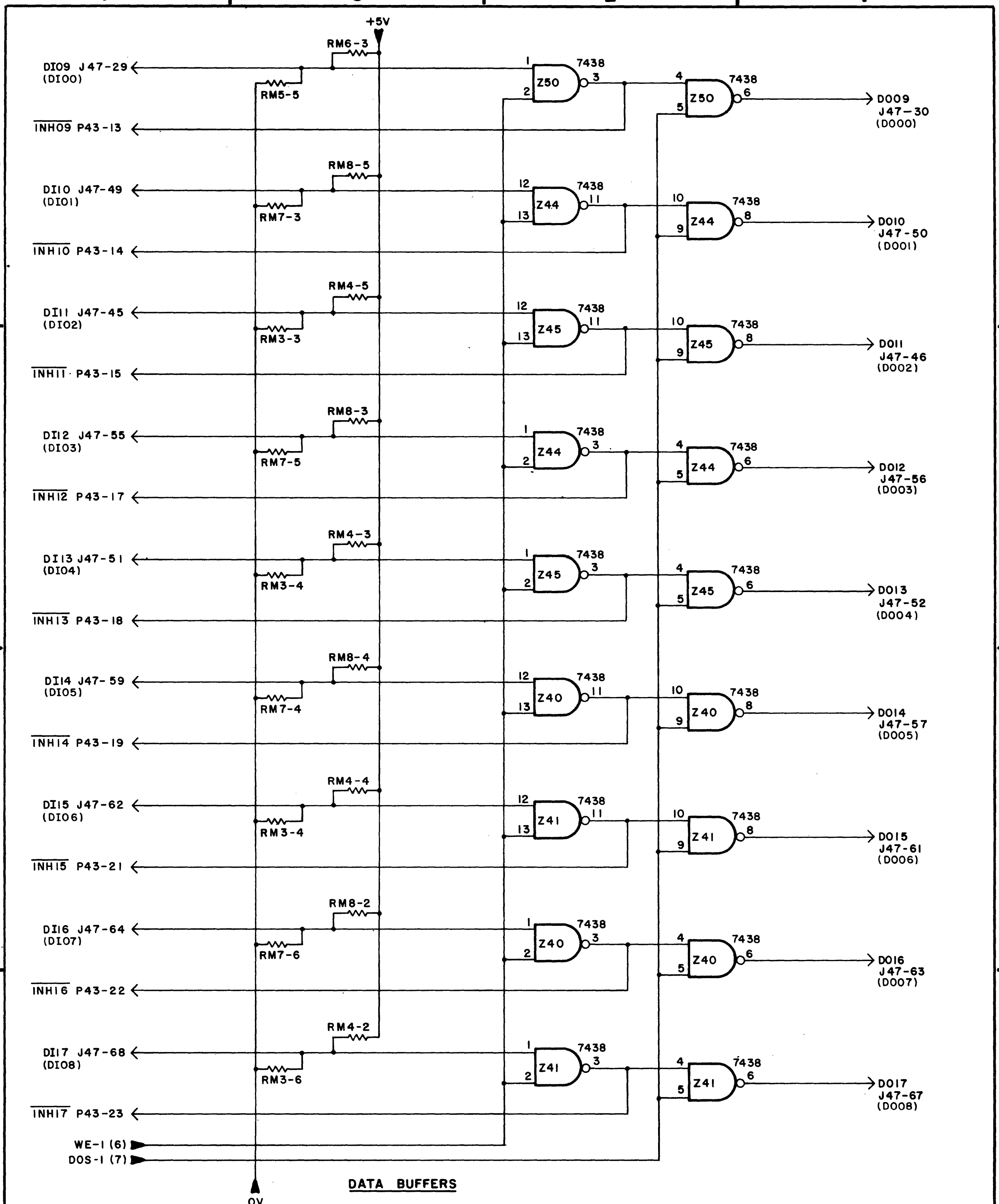
CONTROL DATA CORPORATION CMMD OPERATIONS	MEMORY ELECTRONICS BOARD SCHEMATIC OEM 16K X 36 AND 32K X 18	CODE IDENT 54211	C	DWG NO 82843000	REV 01
				SHEET 13	



NOTES:

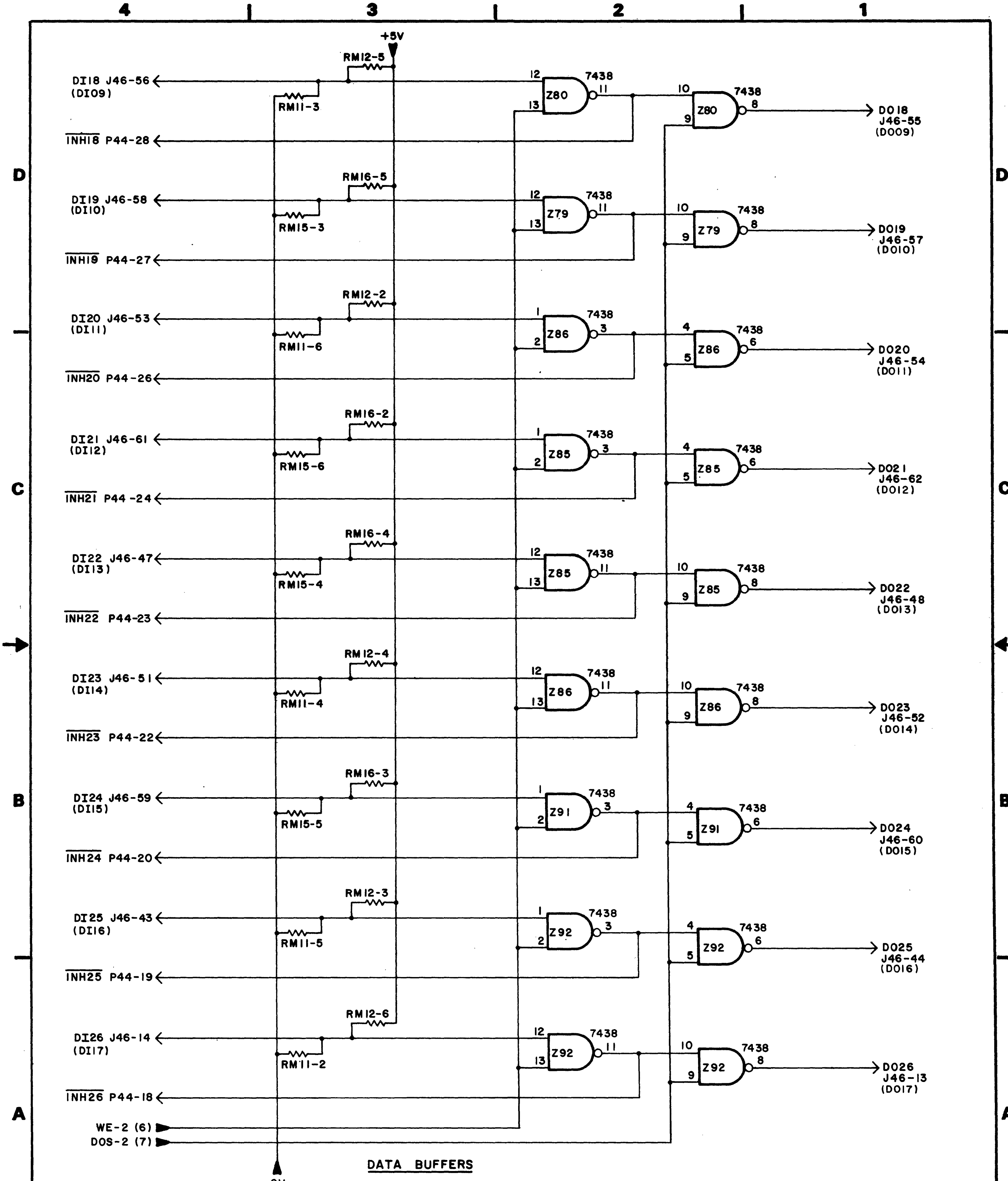
1. THE NUMBERS LOCATED ( ) ARE DATA IN AND DATA OUT FOR 32K X 18 SEE SHEET 1.

CONTROL DATA CORPORATION CMMD OPERATIONS	MEMORY ELECTRONICS BOARD SCHEMATIC OEM 16K X 36 & 32K X 18	CODE IDENT 54211	C	DWG NO 82843000	REV 01
				SHEET 14	



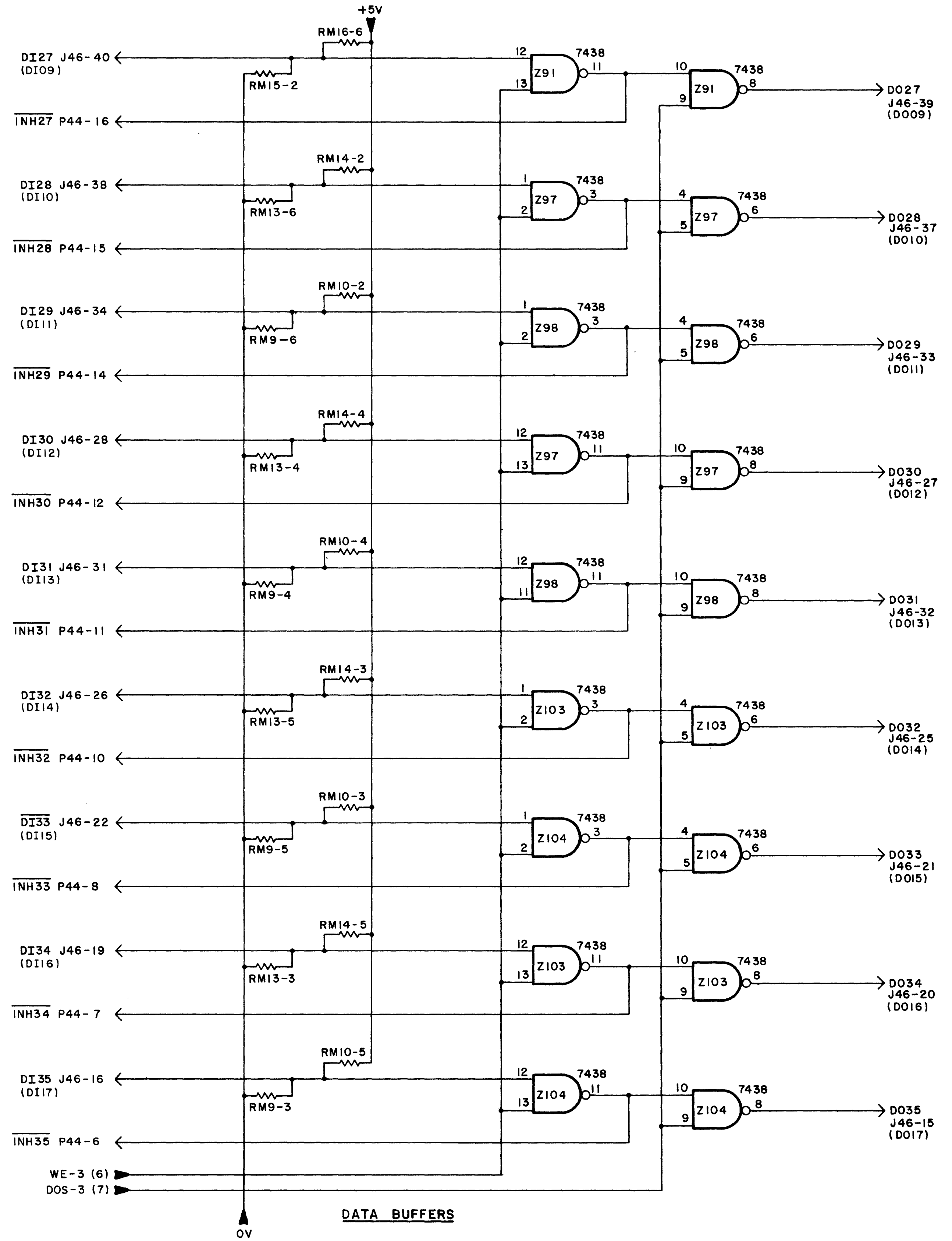
NOTES:
1. THE NUMBERS LOCATED ( ) ARE DATA IN AND DATA OUT FOR 32K X 18 SEE SHEET 1.

CONTROL DATA / CMMD OPERATIONS	MEMORY ELECTRONICS BOARD SCHEMATIC OEM 16K X 36 & 32K X 18	CODE IDENT 54211	C	DWG NO 82843000	REV 01
				SHEET 15	



NOTES:
1. THE NUMBERS LOCATED ( ) ARE DATA IN AND DATA OUT FOR 32K X 18 SEE SHEET 1.

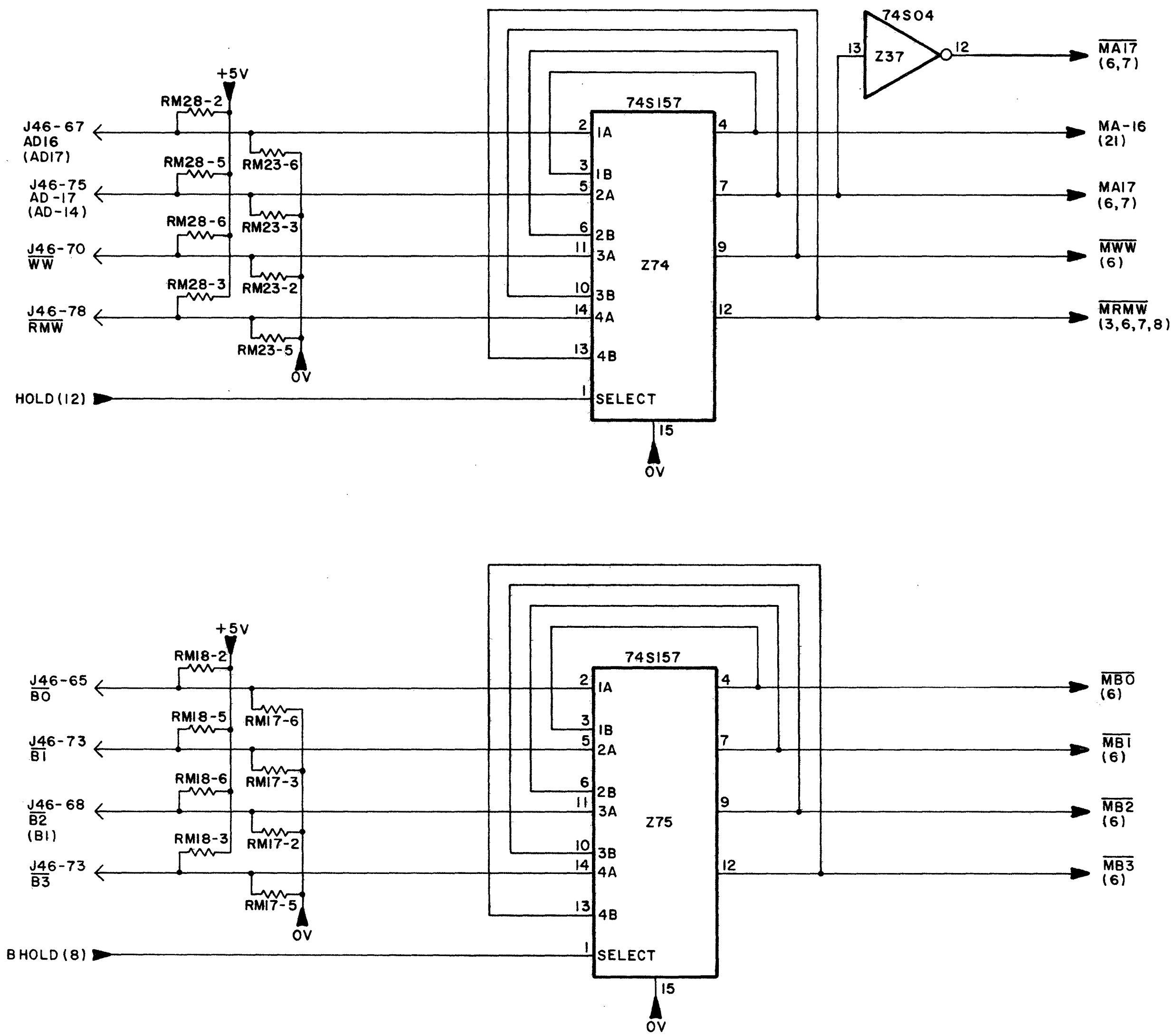
CONTROL DATA / CMMD OPERATIONS	MEMORY ELECTRONICS BOARD SCHEMATIC OEM 16K X 36 & 32K X 18	CODE IDENT 54211	C	DWG NO 82843000	REV 01
				SHEET 16	



DATA BUFFERS

NOTES:
1. THE NUMBERS LOCATED ( ) ARE DATA IN AND DATA OUT FOR 32K X 18 SEE SHEET 1.

CONTROL DATA CMMD OPERATIONS	MEMORY ELECTRONICS BOARD SCHEMATIC OEM 16K X 36 & 32K X 18	CODE IDENT 54211	C	DWG NO 82843000	REV 01
				SHEET 17	

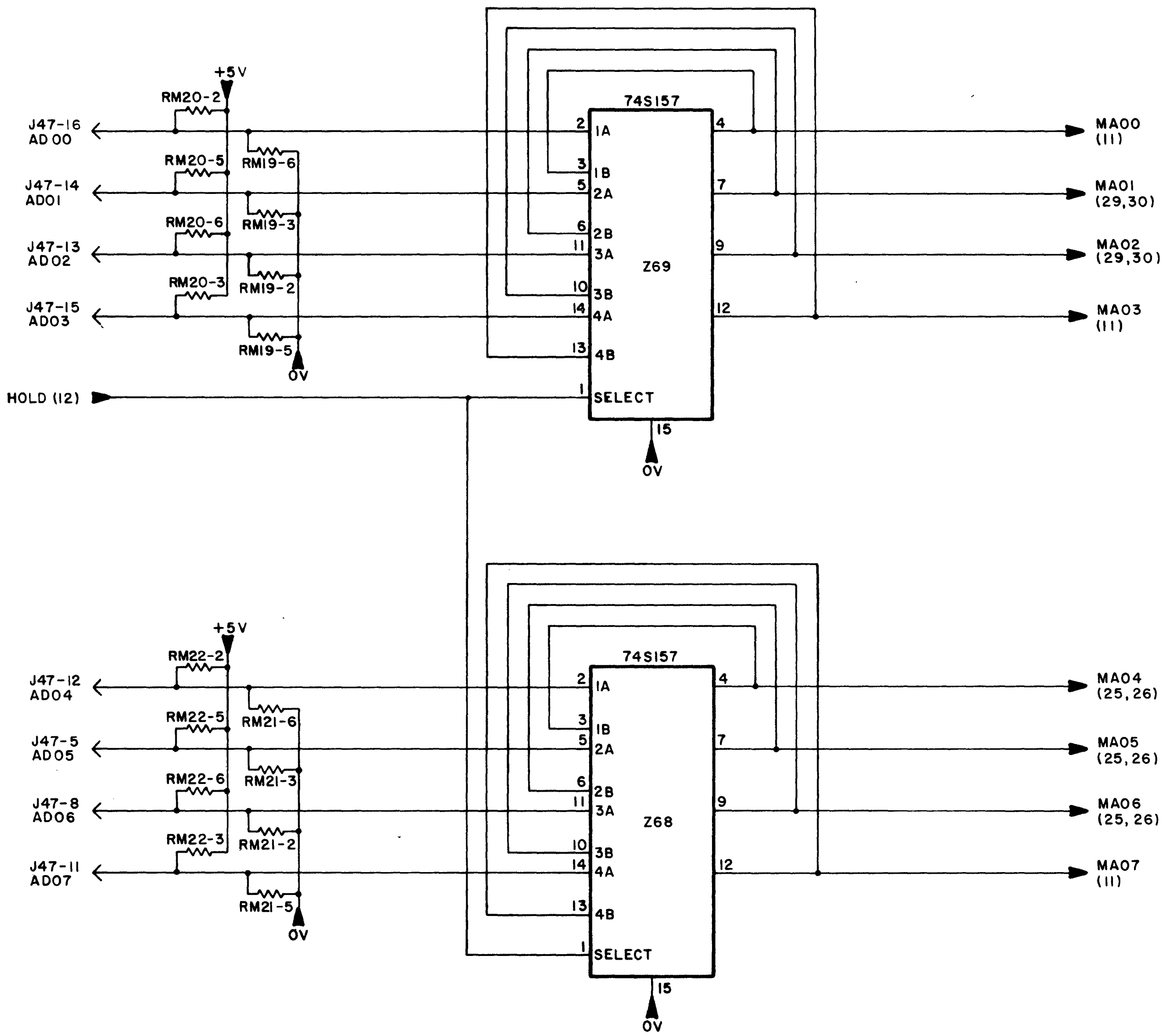


NOTES:

1. IN A 32K X 18 CONFIGURATION ADDRESSES AD-14-15-16 WILL SHIFT TO 15-16-17 AND ADDRESS AD-17 WILL BECOME AD-13. AD-17 IS NOT USED IN A 16K X 36 CONFIGURATION.
2. THE ( ) DENOTES THE ADDRESS INPUT TO BE USED IN A 32K X 18 CONFIGURATION.
3. BYTE 2 INPUT BECOMES BYTE 1 IN 32K X 18 CONFIGURATION AND BYTE 1 AND 3 ARE NOT USED. (OPEN)

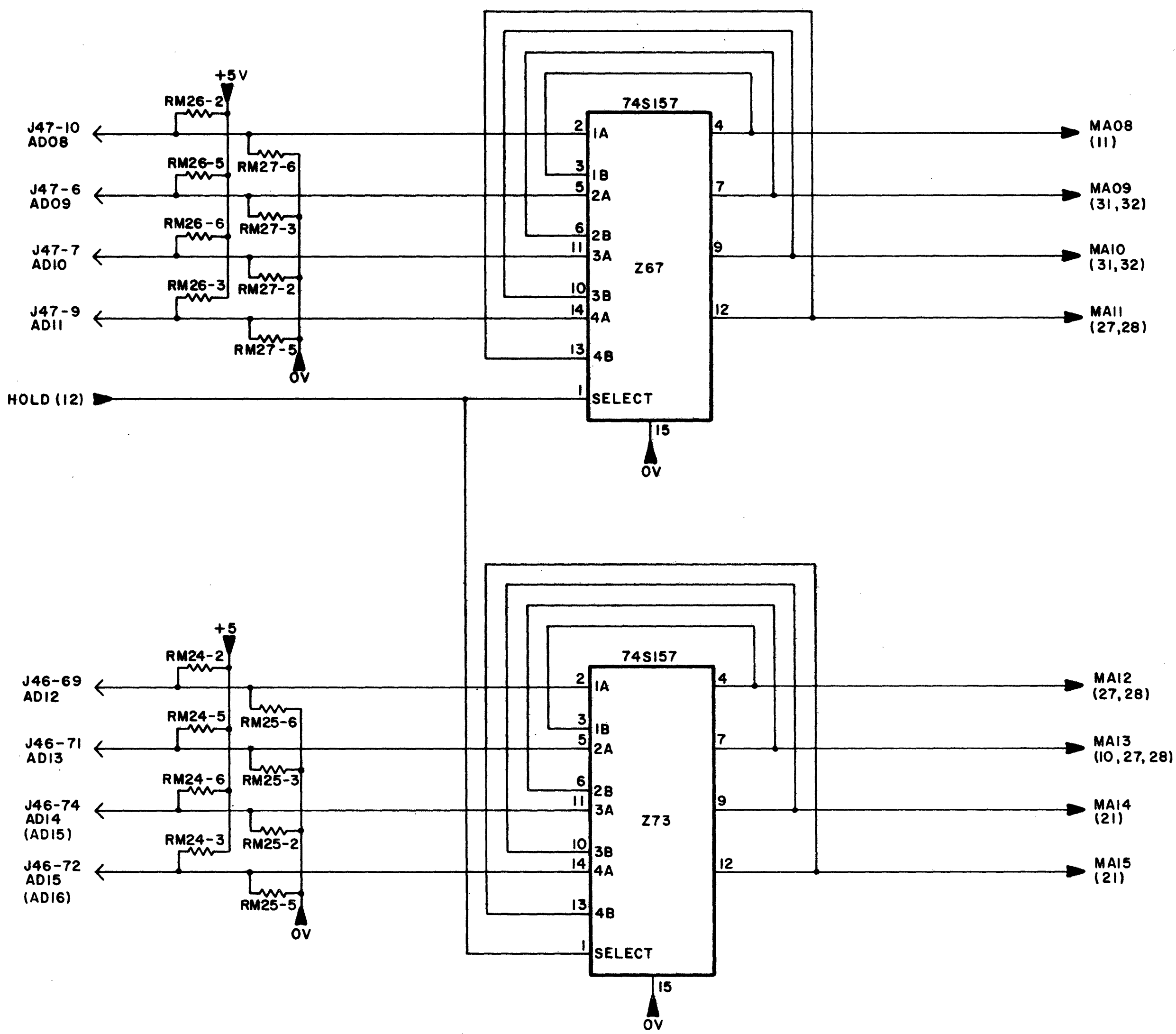
ADDRESS AND BYTE REGISTERS

CONTROL DATA CORPORATION CMMD OPERATIONS	MEMORY ELECTRONICS BOARD SCHEMATIC OEM 16K X 36 & 32K X 18	CODE IDENT 54211	C	DWG NO 82843000	REV 01
				SHEET 18	



ADDRESS REGISTERS

CONTROL DATA CMMD OPERATIONS	MEMORY ELECTRONICS BOARD SCHEMATIC OEM 16K X 36 & 32K X 18	CODE IDENT 54211	C	DWG NO 82843000	REV 01
				SHEET 19	

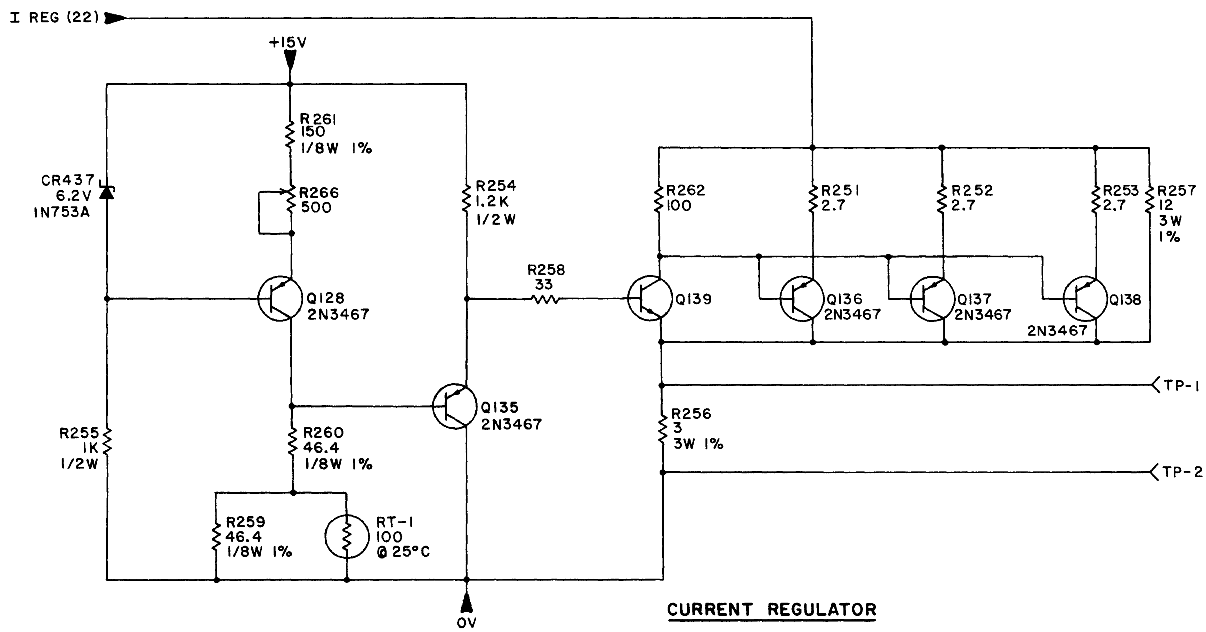


NOTES:

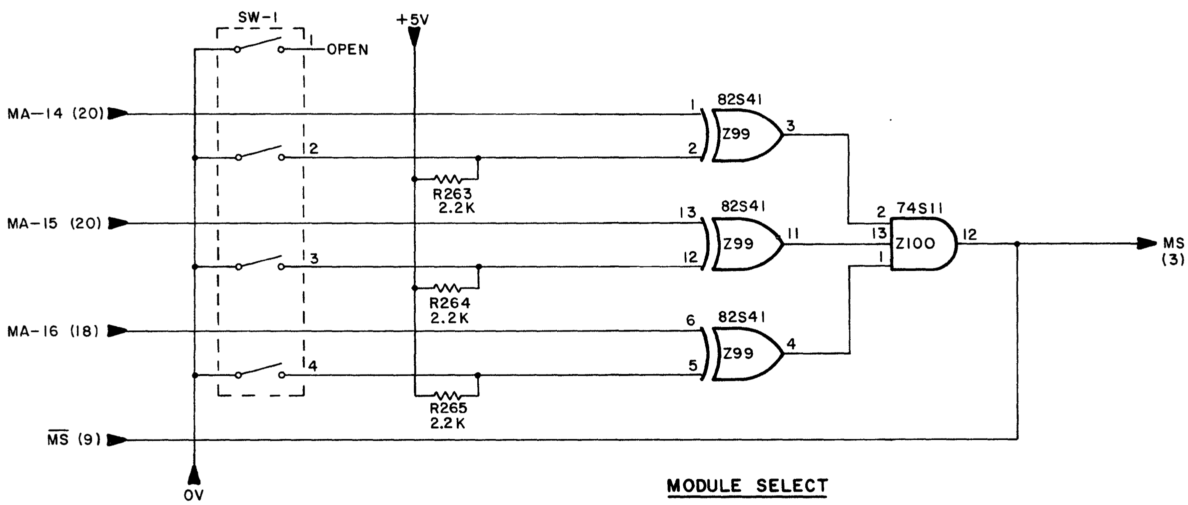
1. IN A 32K X 18 CONFIGURATION ADDRESSES AD-14-15-16 SHIFT TO AD-15-16-17.
2. THE ( ) DENOTES THE ADDRESS INPUTS TO BE USED IN 32K X 18 CONFIGURATION.

ADDRESS REGISTERS

CONTROL DATA / CMMD OPERATIONS	MEMORY ELECTRONICS BOARD SCHEMATIC OEM 16K X 36 & 32K X 18	CODE IDENT 54211	C	DWG NO 82843000	REV 01
				SHEET 20	



CURRENT REGULATOR



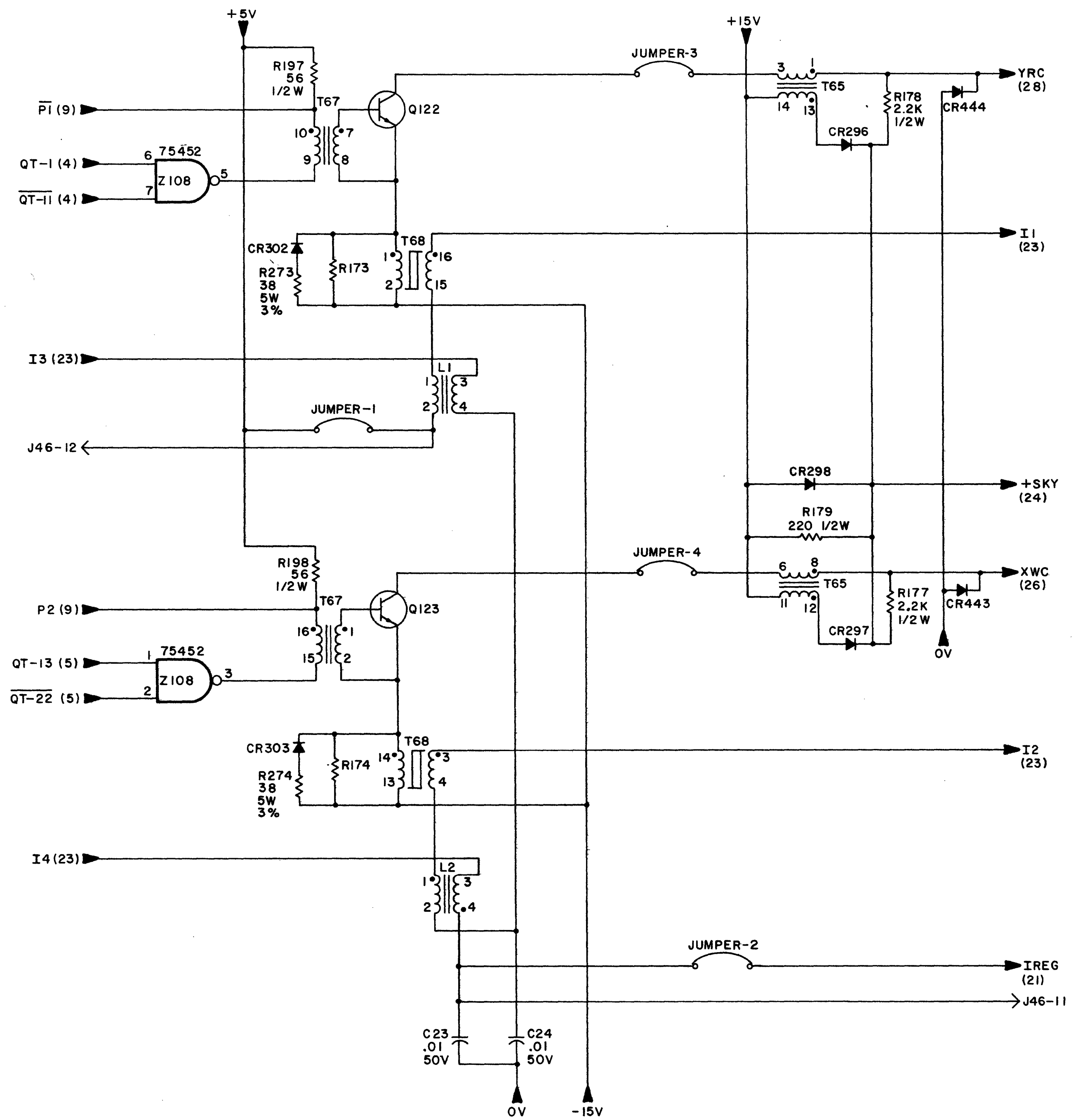
MODULE SELECT

MEMORY SELECT (MS)	POS-2	POS-3	POS-4
0			
1	X		
2		X	
3	X	X	
4			X
5	X		X
6		X	X
7	X	X	X

X = CLOSED SWITCH

WHEN AD 14-15-16 ARE LEFT OPEN MS-7 MUST BE USED.

CONTROL DATA — CMMD OPERATIONS	MEMORY ELECTRONICS BOARD SCHEMATIC OEM 16K X 36 & 32K X 18	CODE IDENT 54211	C	DWG NO 82843000	REV 01
				SHEET 21	

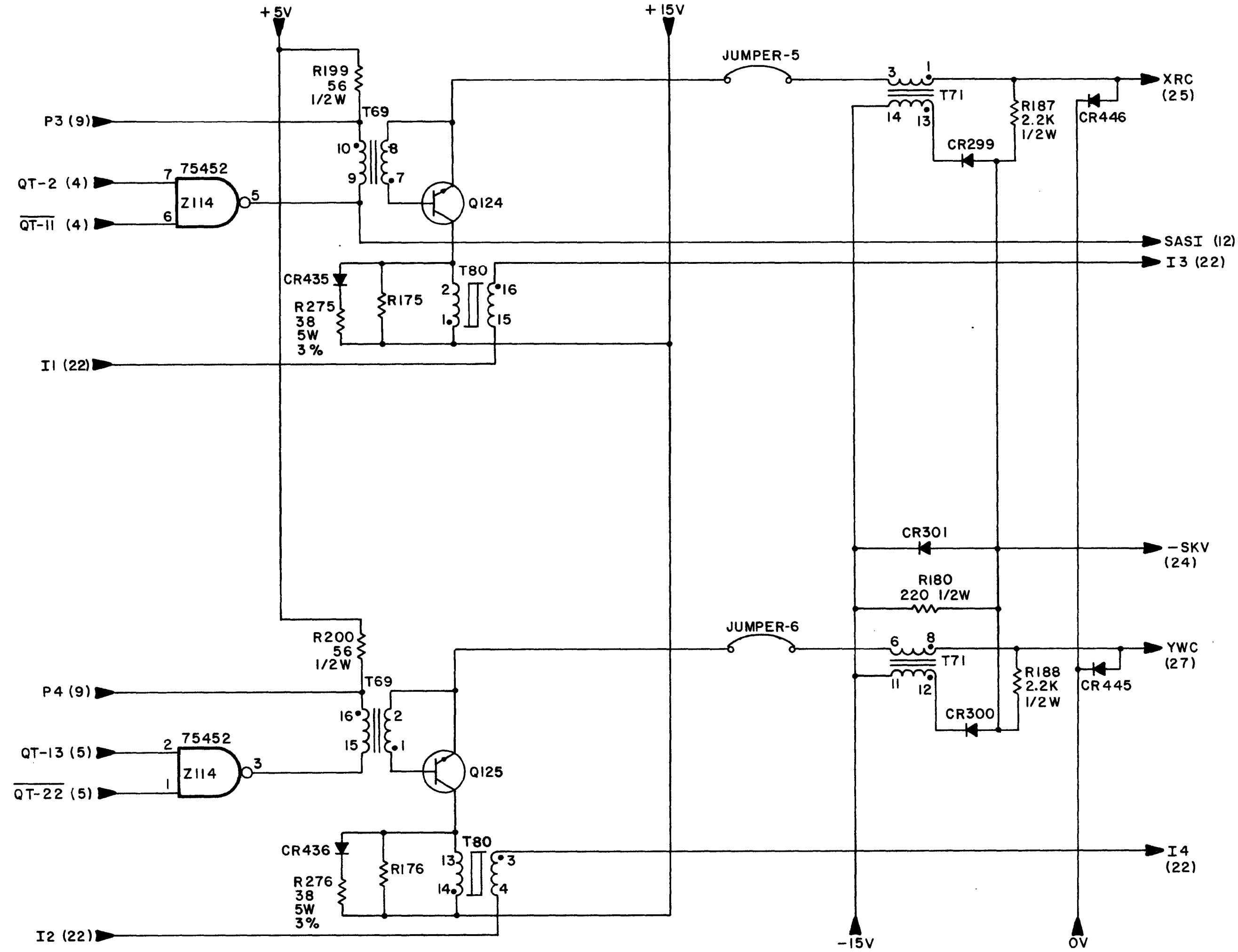


CURRENT SOURCE

NOTES:

1. J46-11 & 12 WILL BE USED ONLY WHEN AN EXTERNAL CURRENT SOURCE IS TO BE USED.
2. R173 & R174 ARE NOT REQUIRED.

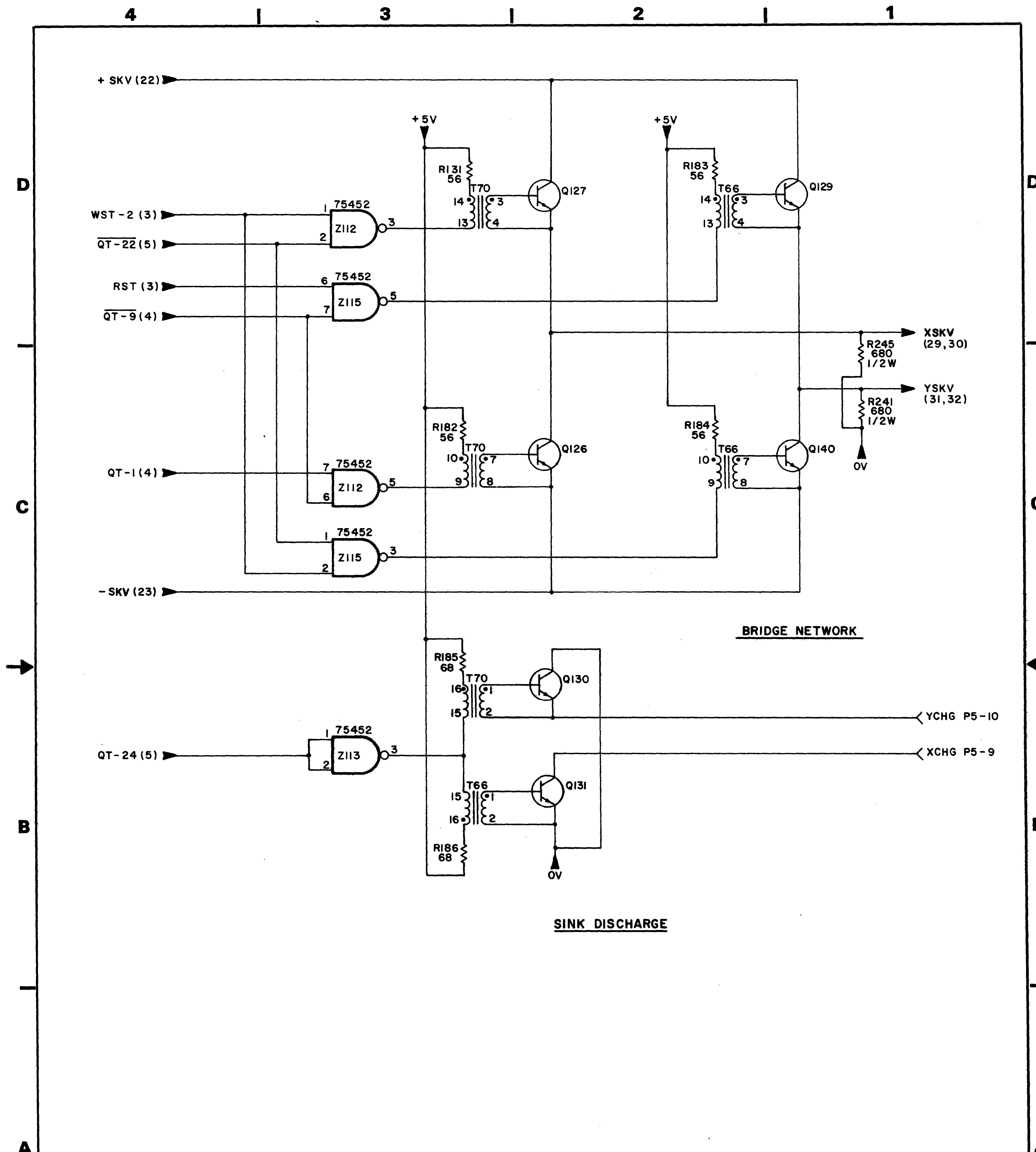
CONTROL DATA CORPORATION CMMD OPERATIONS	MEMORY ELECTRONICS BOARD SCHEMATIC OEM 16K X 36 & 32K X 18	CODE IDENT 54211	C	DWG NO 82843000	REV 01
				SHEET 22	



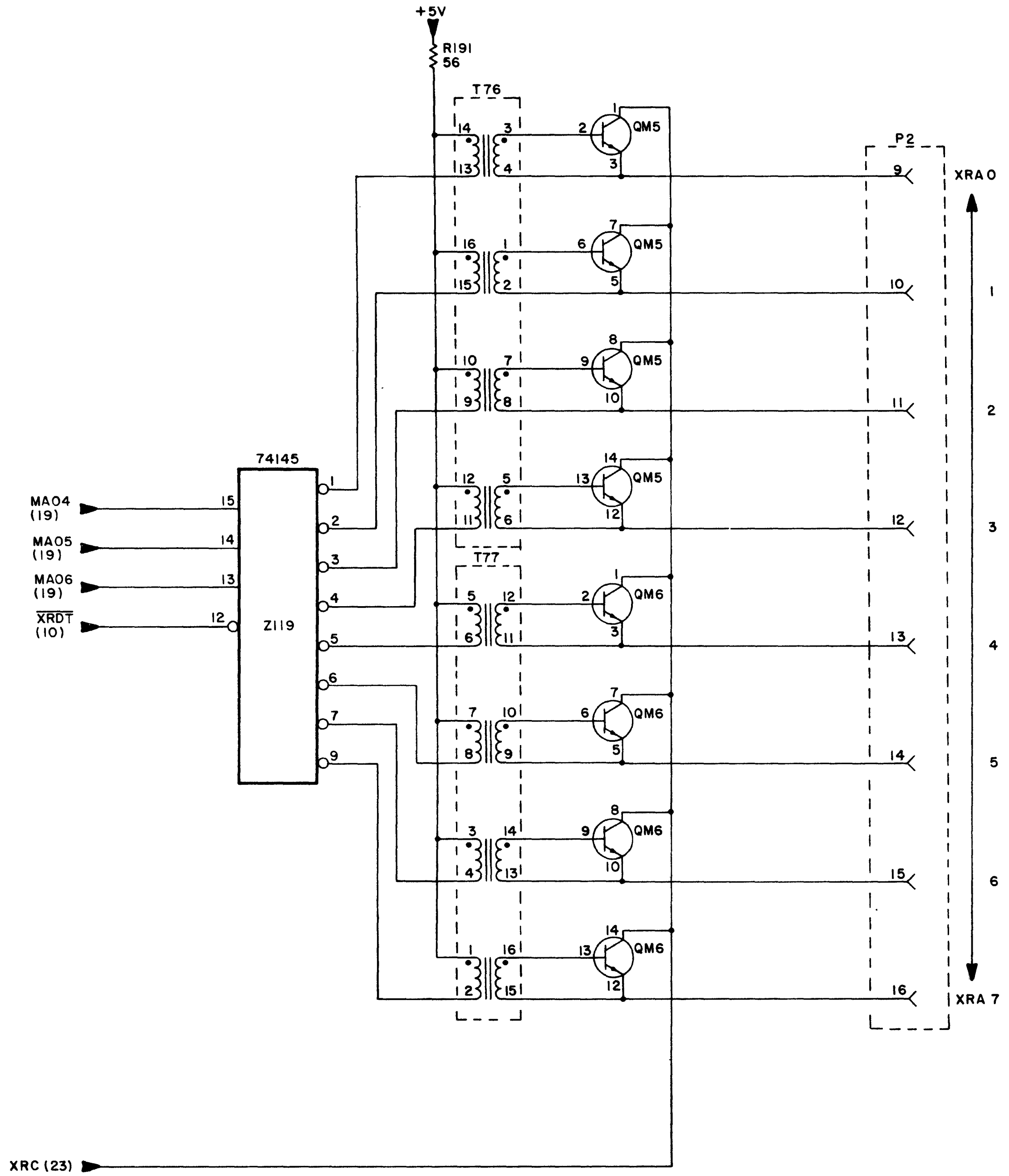
CURRENT SOURCE

NOTES:
1. R175 AND R176 ARE NOT REQUIRED.

CONTROL DATA CORPORATION / CMMD OPERATIONS	MEMORY ELECTRONICS BOARD SCHEMATIC OEM 16K X 36 & 32K X 18	CODE IDENT 54211	C	DWG NO 82843000	REV 01
				SHEET 23	

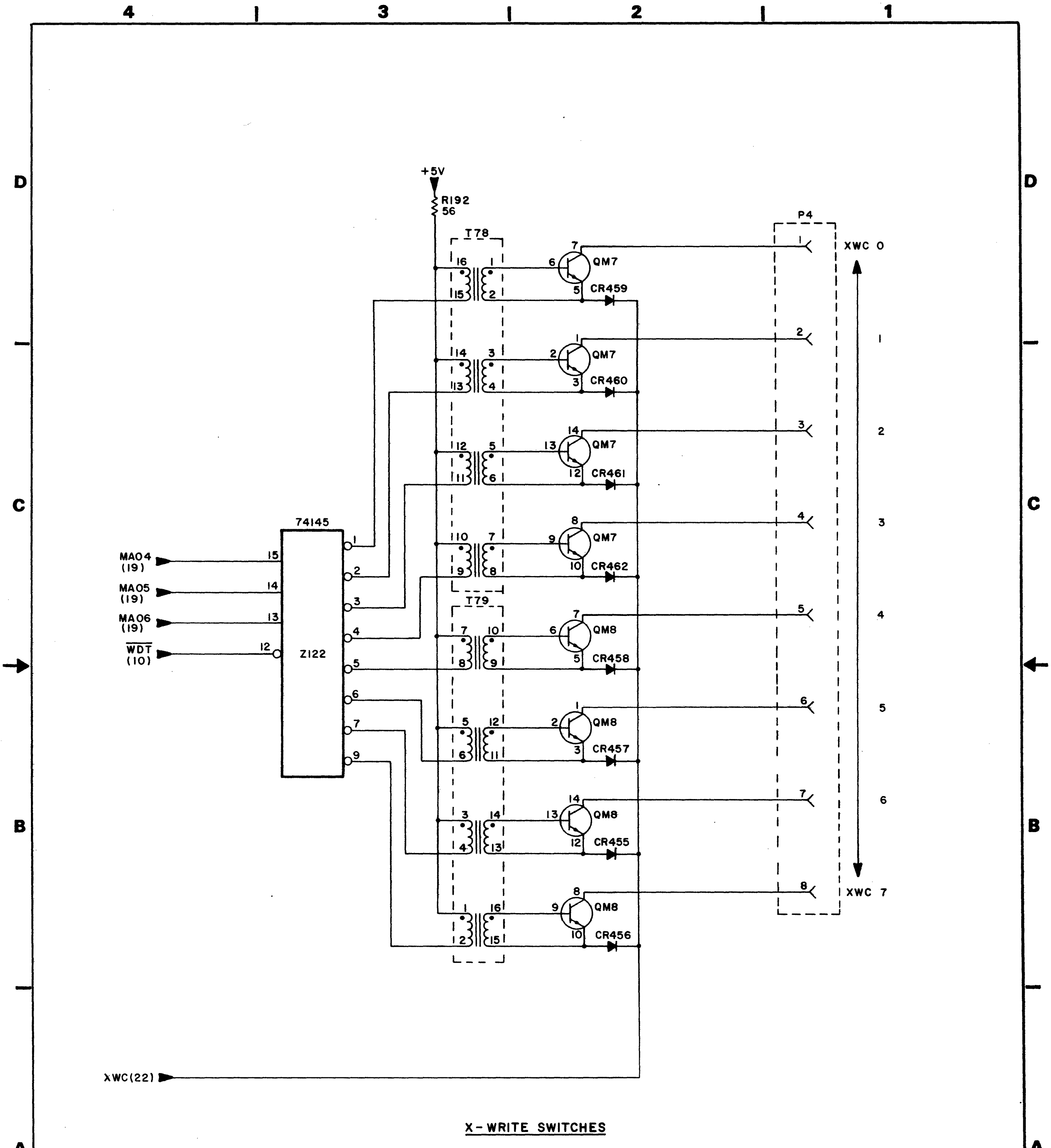


CONTROL DATA CORPORATION / CMMD OPERATIONS	MEMORY ELECTRONICS BOARD SCHEMATIC OEM 16K X 36 AND 32K X 18	CODE IDENT 54211	C	DWG NO 82843000	REV 01
				SHEET 24	



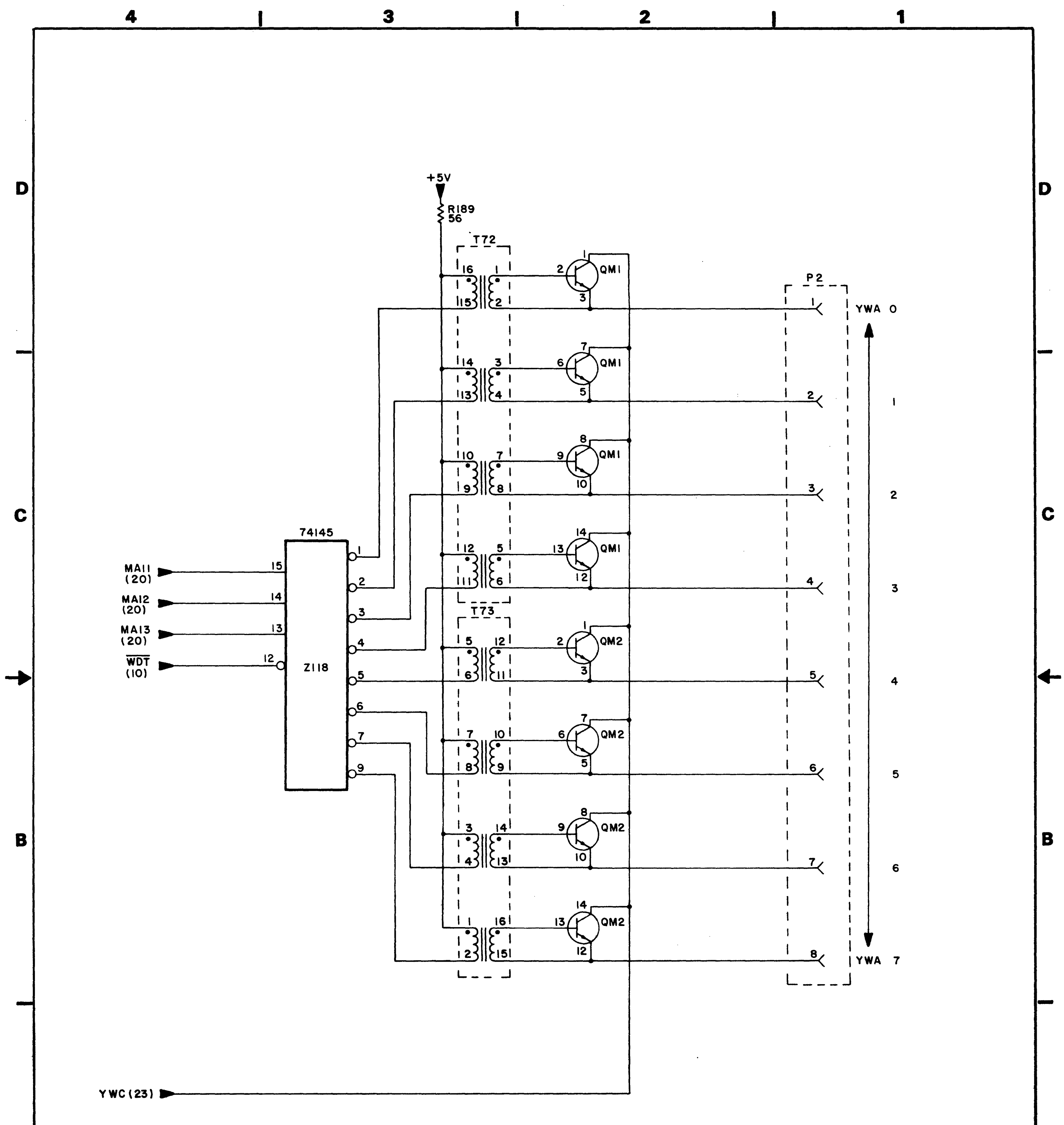
X-READ DRIVERS

CONTROL DATA CMMD OPERATIONS	MEMORY ELECTRONICS BOARD SCHEMATIC OEM 16K X 36 & 32K X 18	CODE IDENT 54211	C	DWG NO 82843000	REV 01
				SHEET 25	



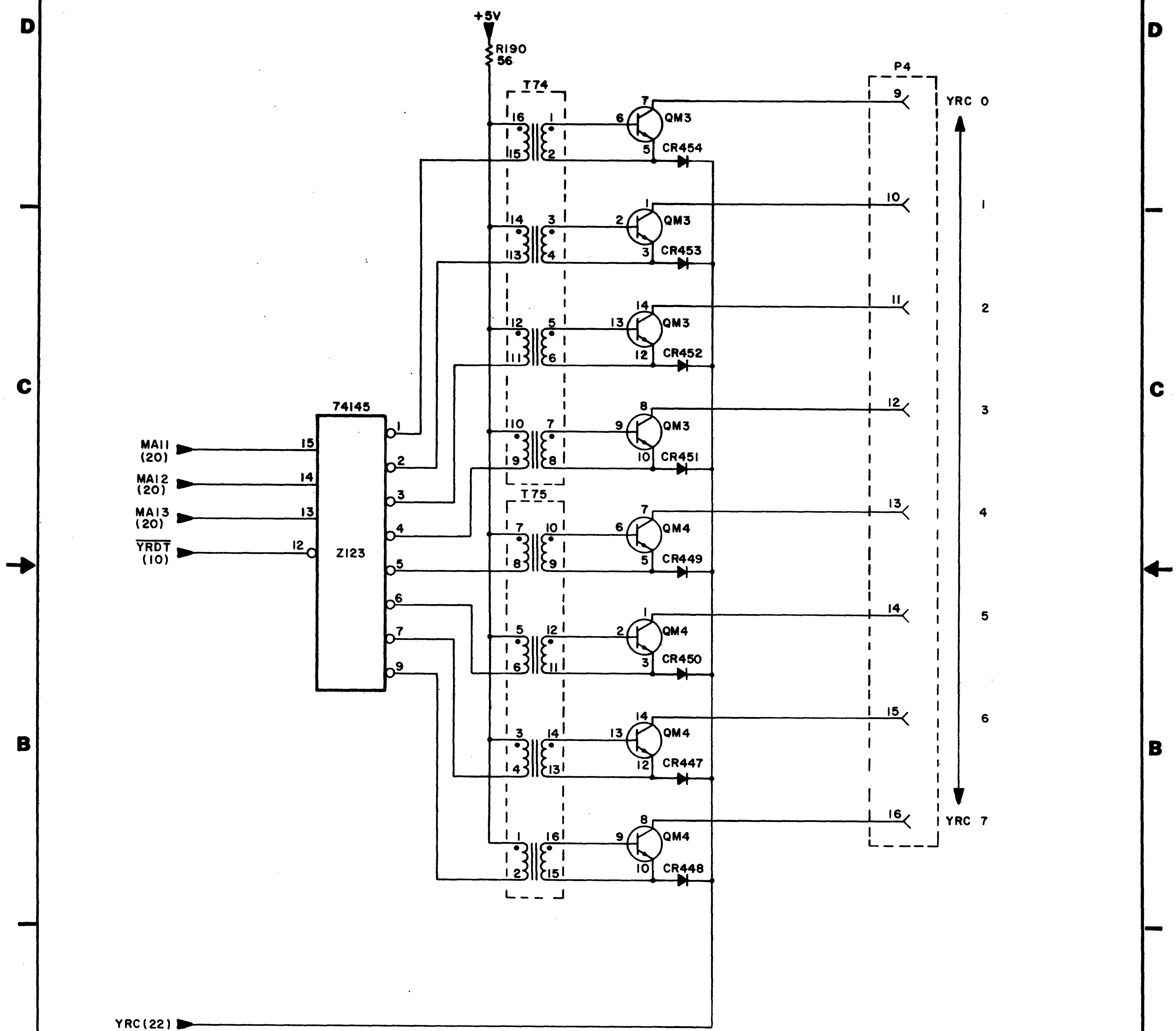
X-WRITE SWITCHES

CONTROL DATA CMMD OPERATIONS	MEMORY ELECTRONICS BOARD SCHEMATIC OEM 16K X 36 & 32K X 18	CODE IDENT 54211	C	DWG NO 82843000	REV 01
				SHEET 26	



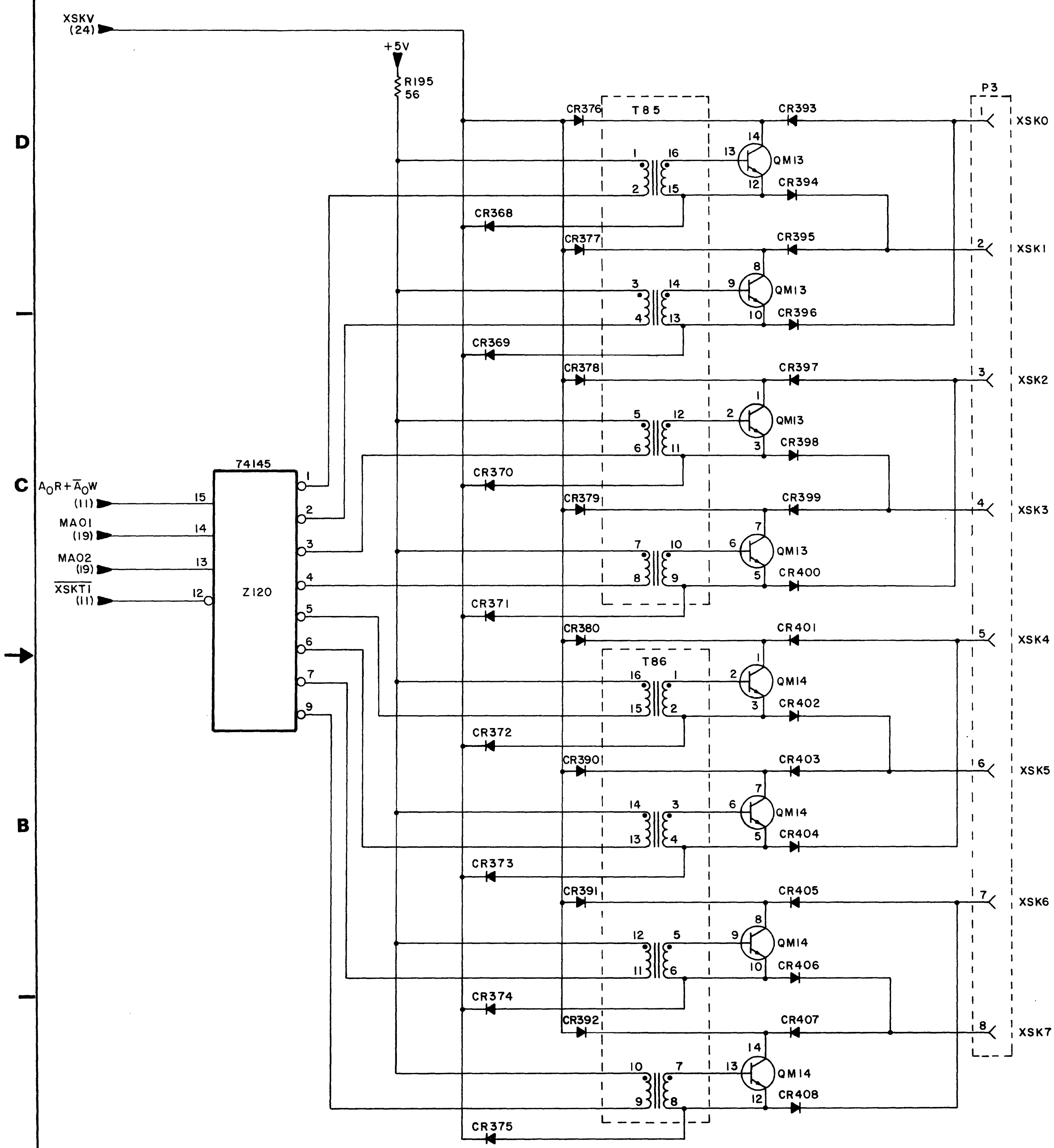
Y WRITE DRIVERS

CONTROL DATA CMMD OPERATIONS	MEMORY ELECTRONICS BOARD SCHEMATIC OEM 16K X 36 & 32K X 18	CODE IDENT 54211	C	DWG NO 82843000	REV 01
				SHEET 27	



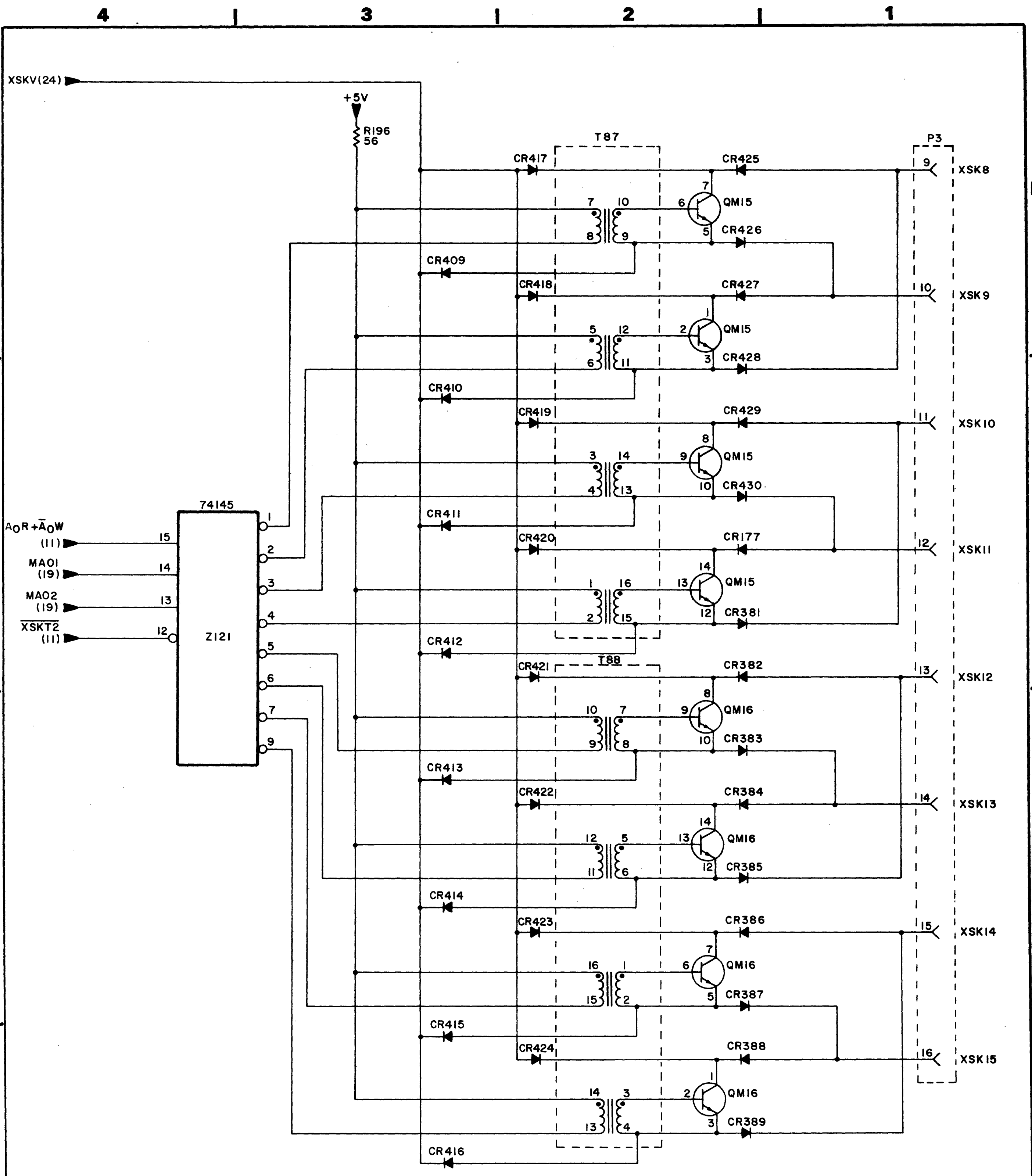
Y READ SWITCHES

CONTROL DATA / CMMD OPERATIONS	MEMORY ELECTRONICS BOARD SCHEMATIC OEM 16K X 36 & 32K X 18	CODE IDENT 54211	C	DWG NO 82843000 / REV 01 / SHEET 28



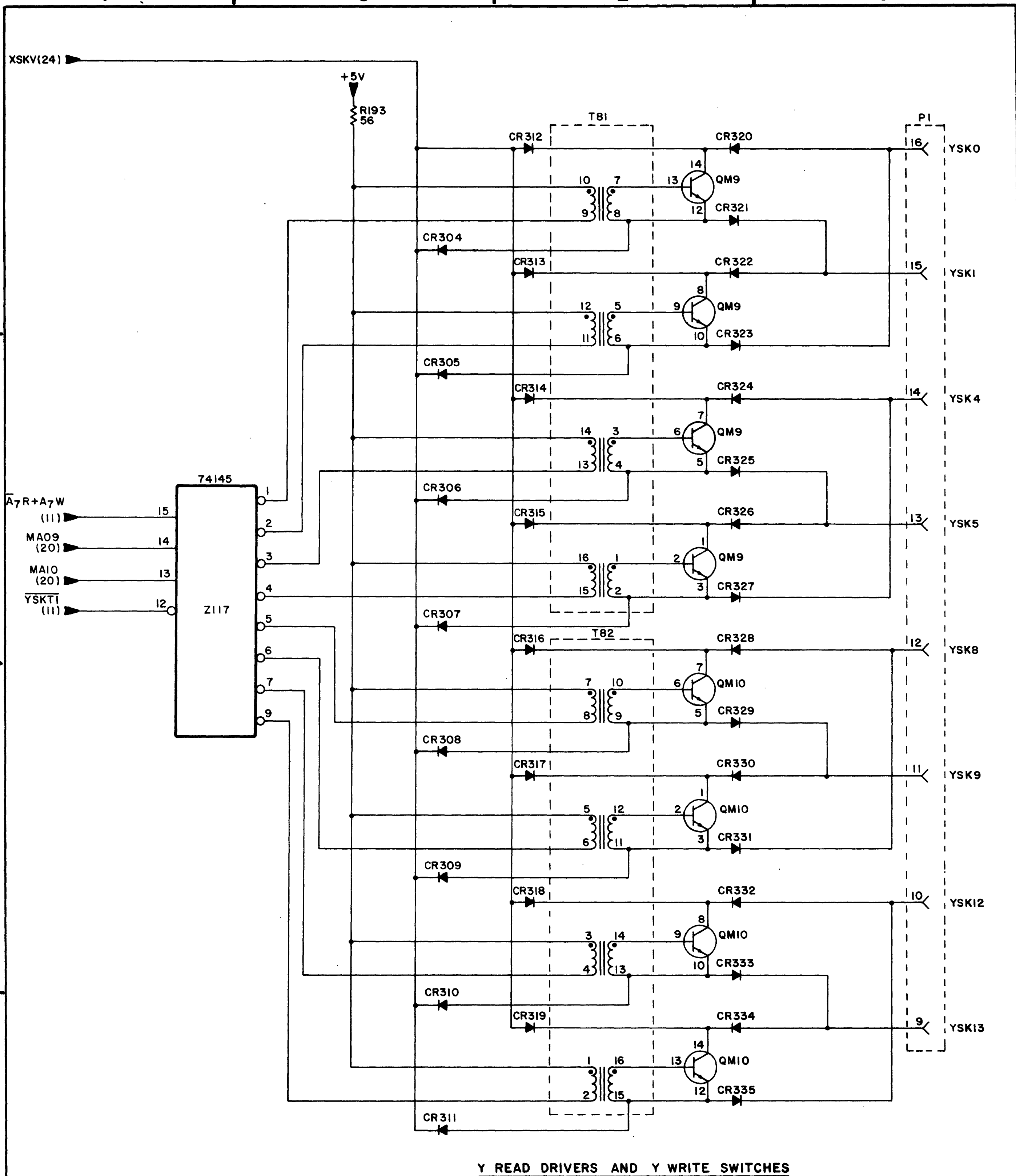
X READ SWITCHES AND X WRITE DRIVERS

CONTROL DATA CORPORATION CMMD OPERATIONS	MEMORY ELECTRONICS BOARD SCHEMATIC OEM 16K X 36 & 32K X 18	CODE IDENT 54211	C	DWG NO 82843000	REV 01
				SHEET 29	



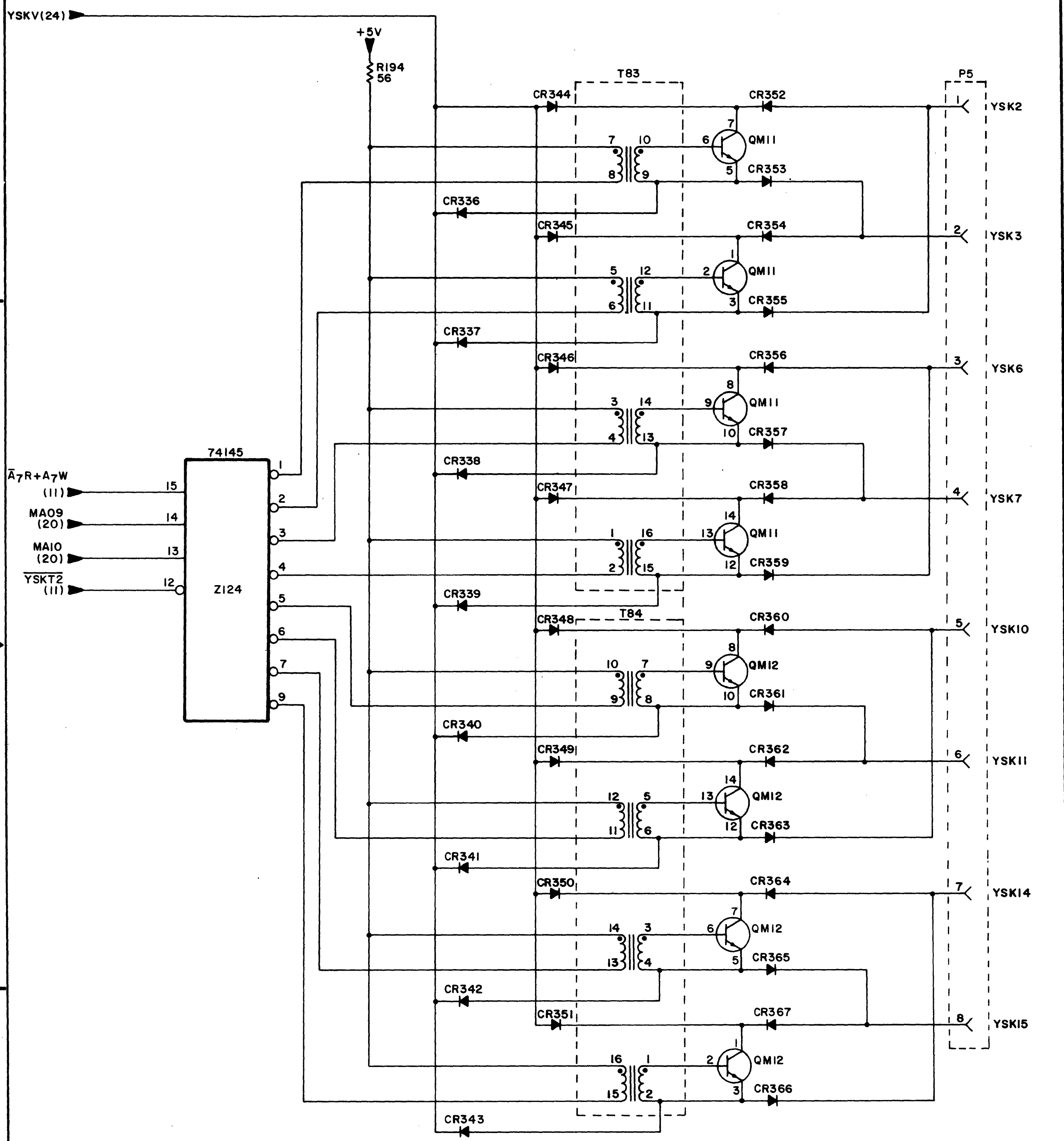
X READ SWITCHES AND X WRITE DRIVERS

CONTROL DATA / CMMD OPERATIONS	MEMORY ELECTRONICS BOARD SCHEMATIC OEM 16K X 36 & 32K X 18	CODE IDENT 54211	C	DWG NO 82843000	REV 01
				SHEET 30	



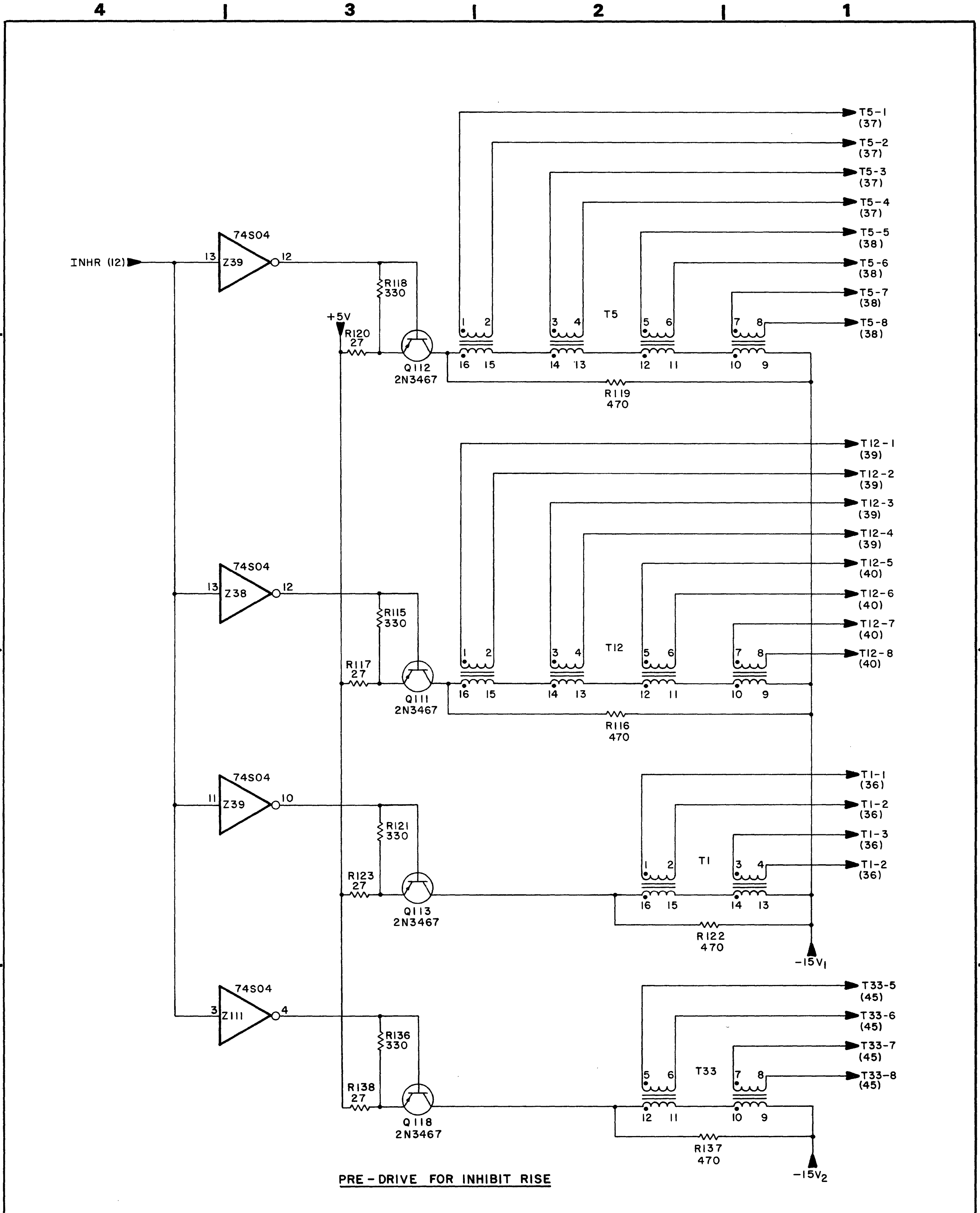
Y READ DRIVERS AND Y WRITE SWITCHES

CONTROL DATA CMMD OPERATIONS	MEMORY ELECTRONICS BOARD SCHEMATIC OEM 16K X 36 & 32K X 18	CODE IDENT 54211	C	DWG NO 82843000 REV 01 SHEET 31

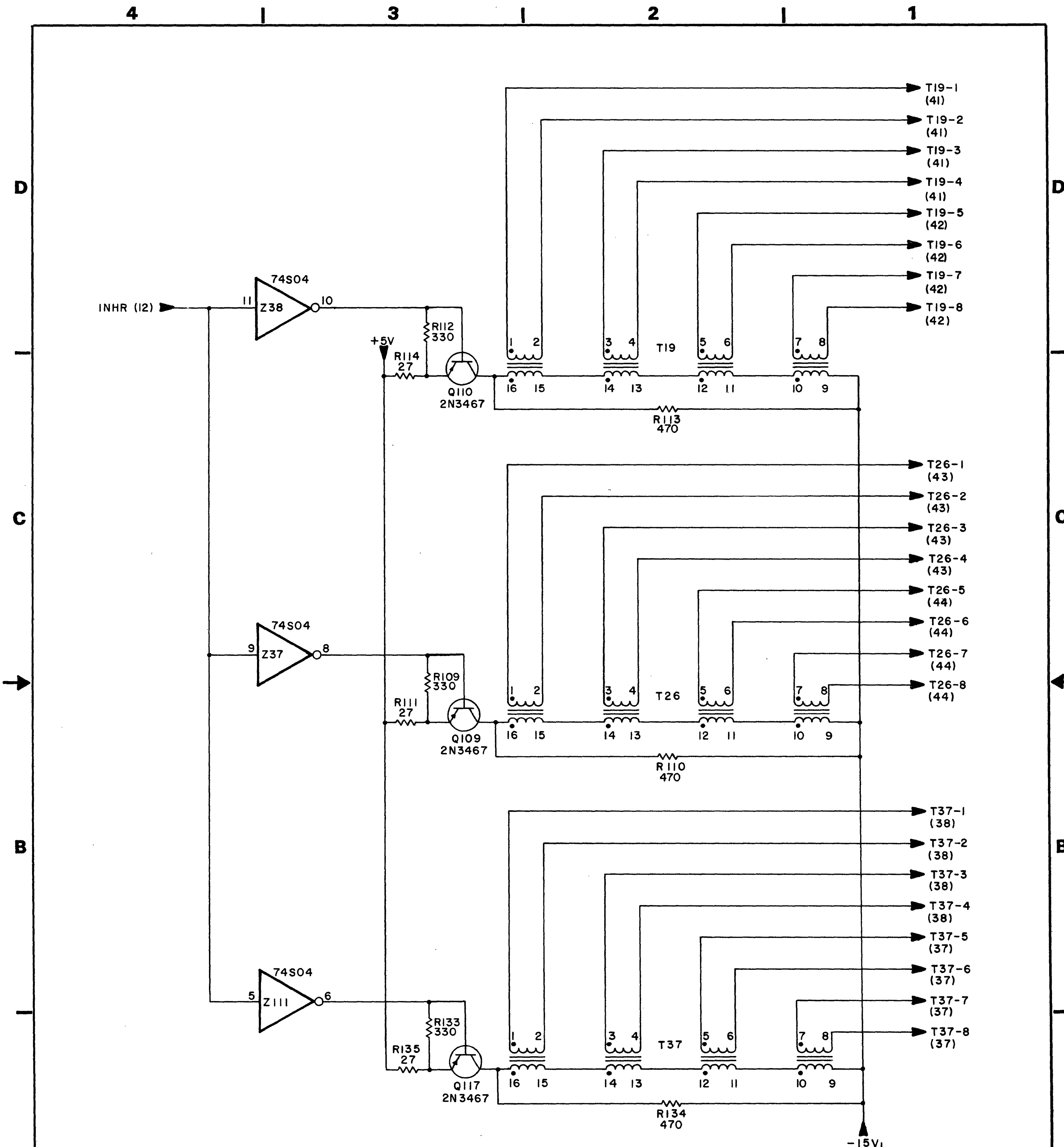


Y READ DRIVERS AND Y WRITE SWITCHES

CONTROL DATA CMMD OPERATIONS	MEMORY ELECTRONICS BOARD SCHEMATIC OEM 16K X 36 & 32K X 18	CODE IDENT 54211	C	DWG NO 82843000	REV 01
				SHEET: 32	

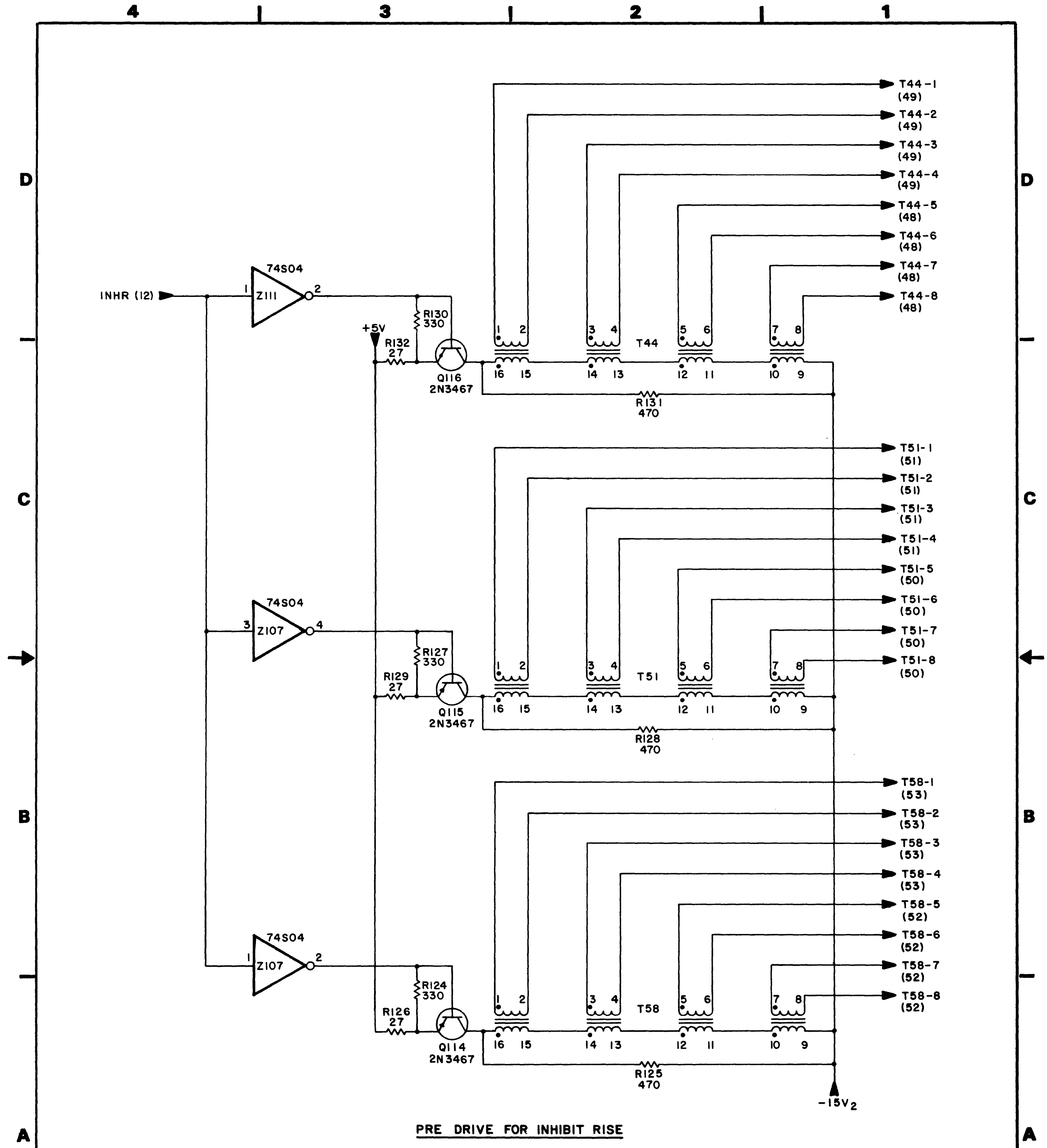


CONTROL DATA CORPORATION CMMD OPERATIONS	MEMORY ELECTRONICS BOARD SCHEMATIC OEM 16K X 36 & 32K X 18	CODE IDENT 54211	C	DWG NO 82843000	REV 01
				SHEET 33	

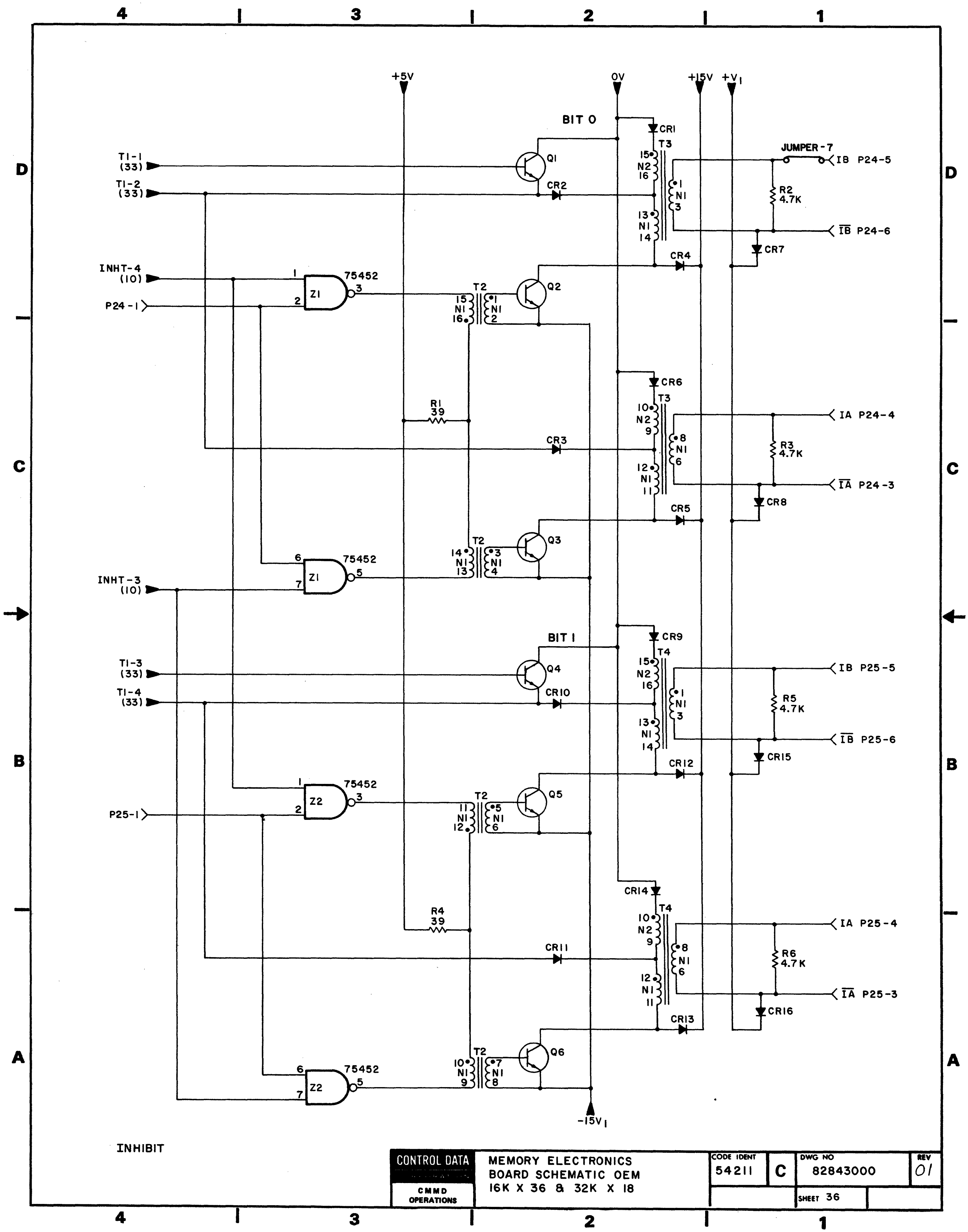


PRE DRIVE FOR INHIBIT RISE

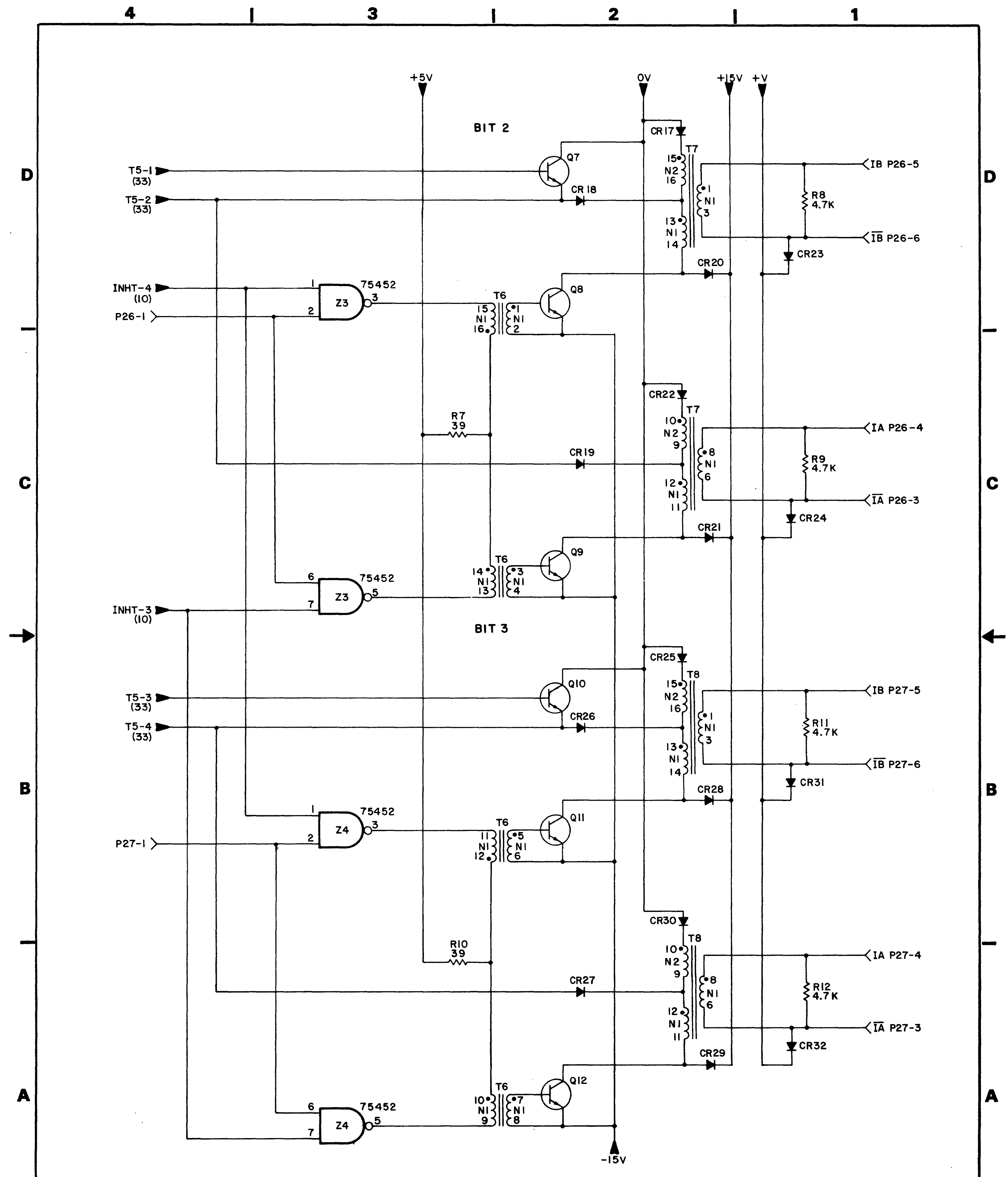
CONTROL DATA CORPORATION CMMD OPERATIONS	MEMORY ELECTRONICS BOARD SCHEMATIC OEM 16K X 36 & 32K X 18	CODE IDENT 54211	C	DWG NO 82843000	REV 01
				SHEET 34	



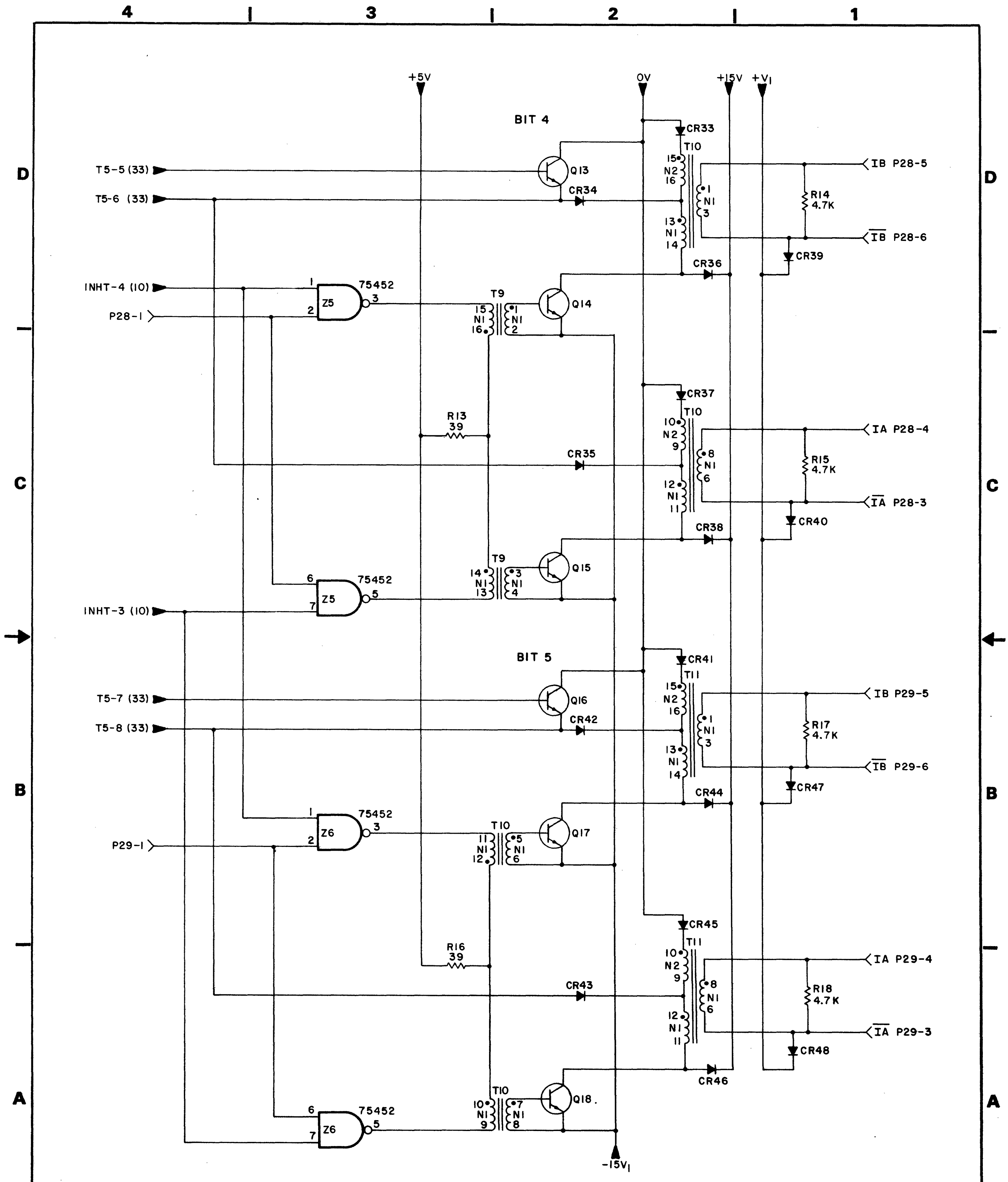
CONTROL DATA CMMD OPERATIONS	MEMORY ELECTRONICS BOARD SCHEMATIC OEM 16K X 36 & 32K X 18	CODE IDENT 54211	C	DWG NO 82843000	REV 01
				SHEET 35	



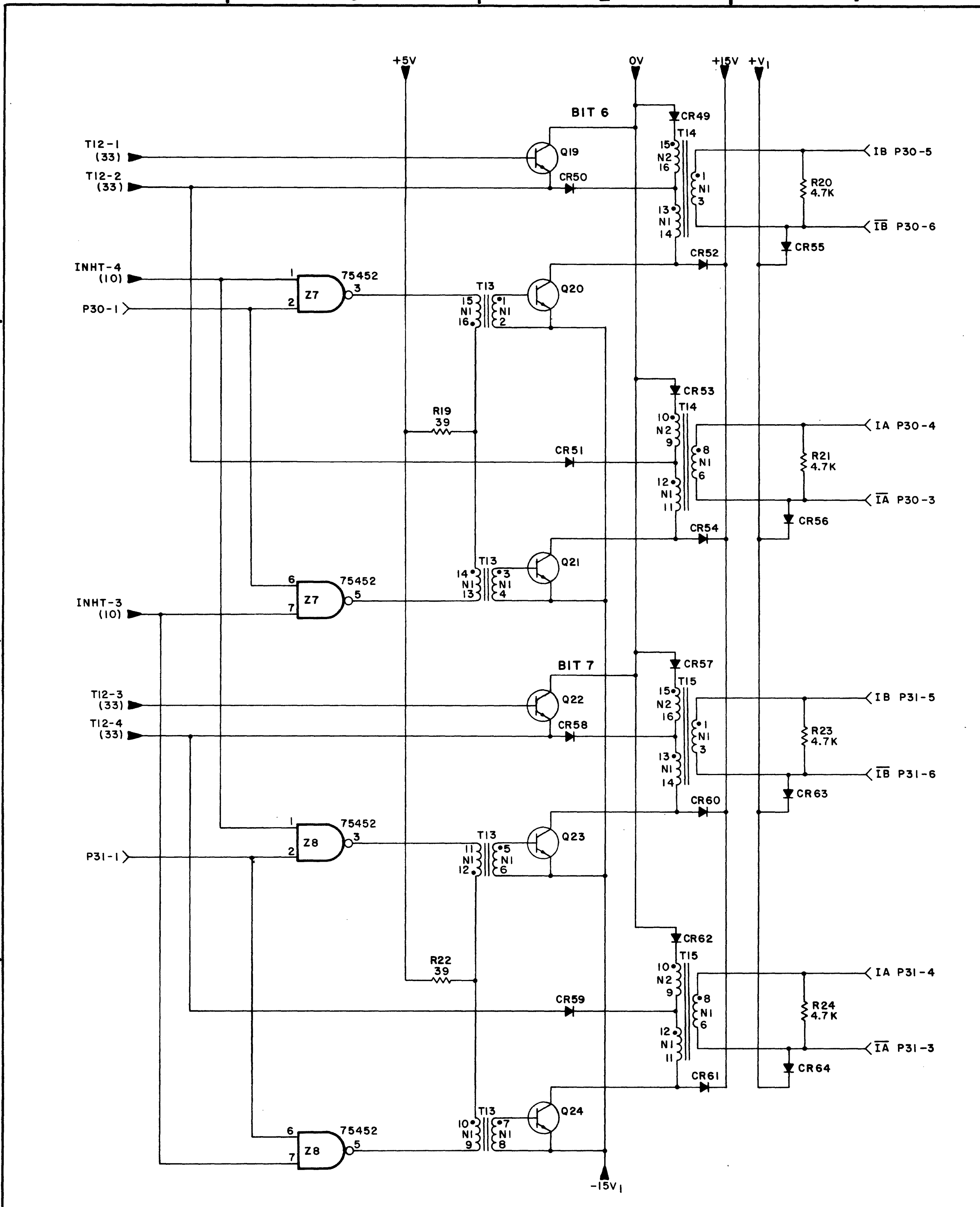
CONTROL DATA / CMMD OPERATIONS	MEMORY ELECTRONICS BOARD SCHEMATIC OEM 16K X 36 & 32K X 18	CODE IDENT 54211	C	DWG NO 82843000	REV 01
				SHEET 36	



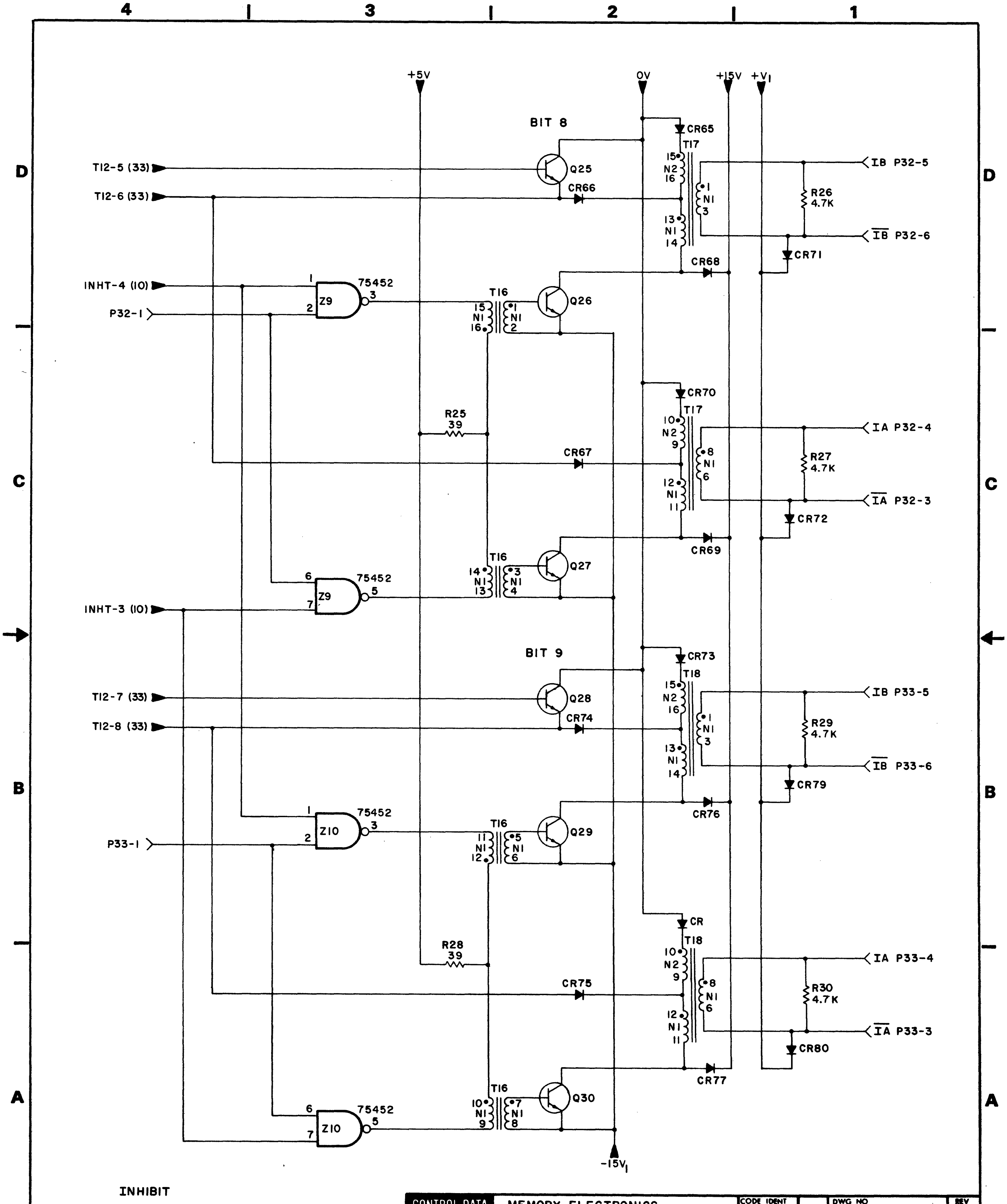
CONTROL DATA / CMMD OPERATIONS	MEMORY ELECTRONICS BOARD SCHEMATIC OEM 16K X 36 & 32K X 18	CODE IDENT 54211	C	DWG NO 82843000	REV 01
				SHEET 37	



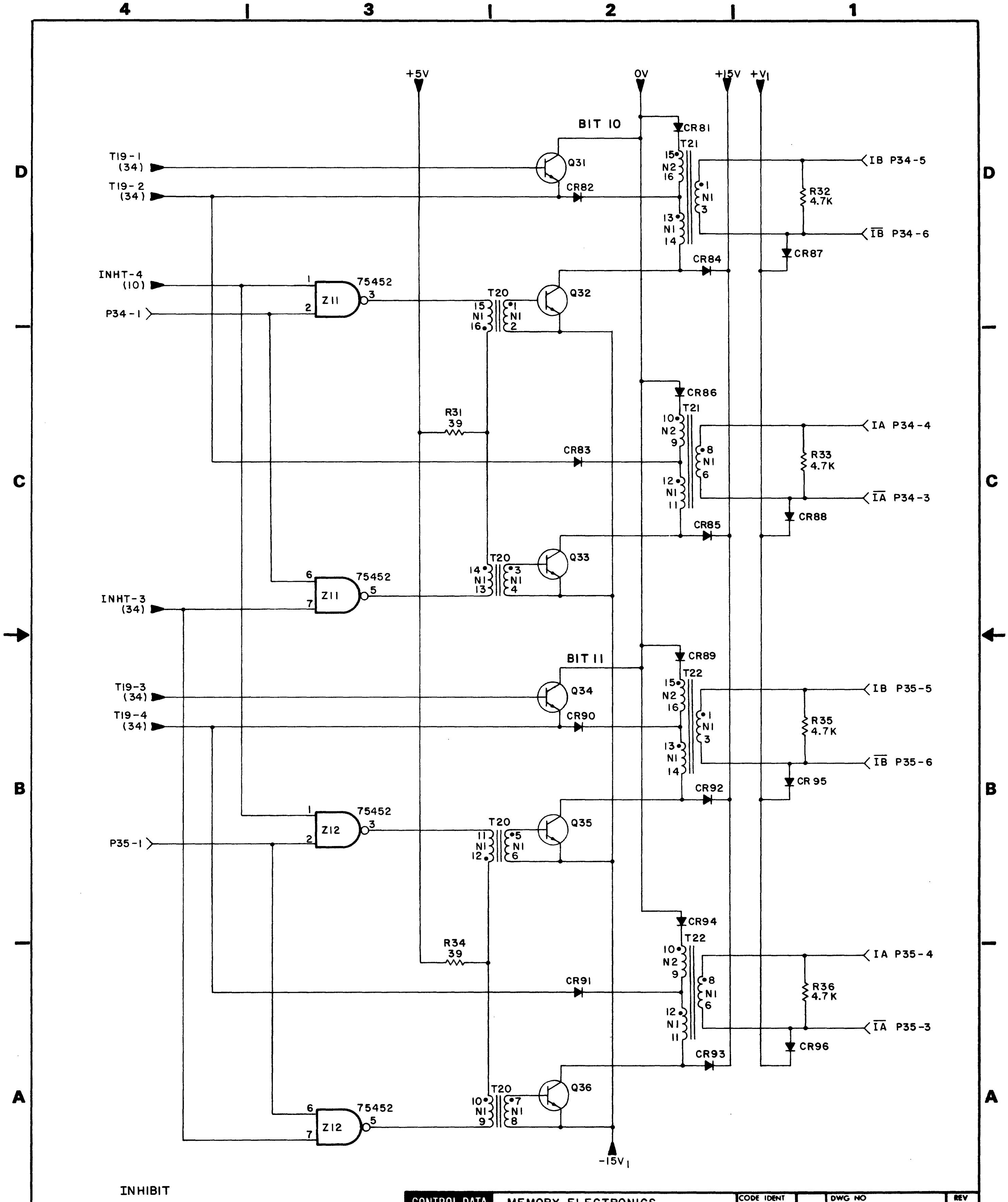
CONTROL DATA / CMMD OPERATIONS	MEMORY ELECTRONICS BOARD SCHEMATIC OEM 16K X 36 & 32K X 18	CODE IDENT 54211	C	DWG NO 82843000	REV 01
				SHEET 38	



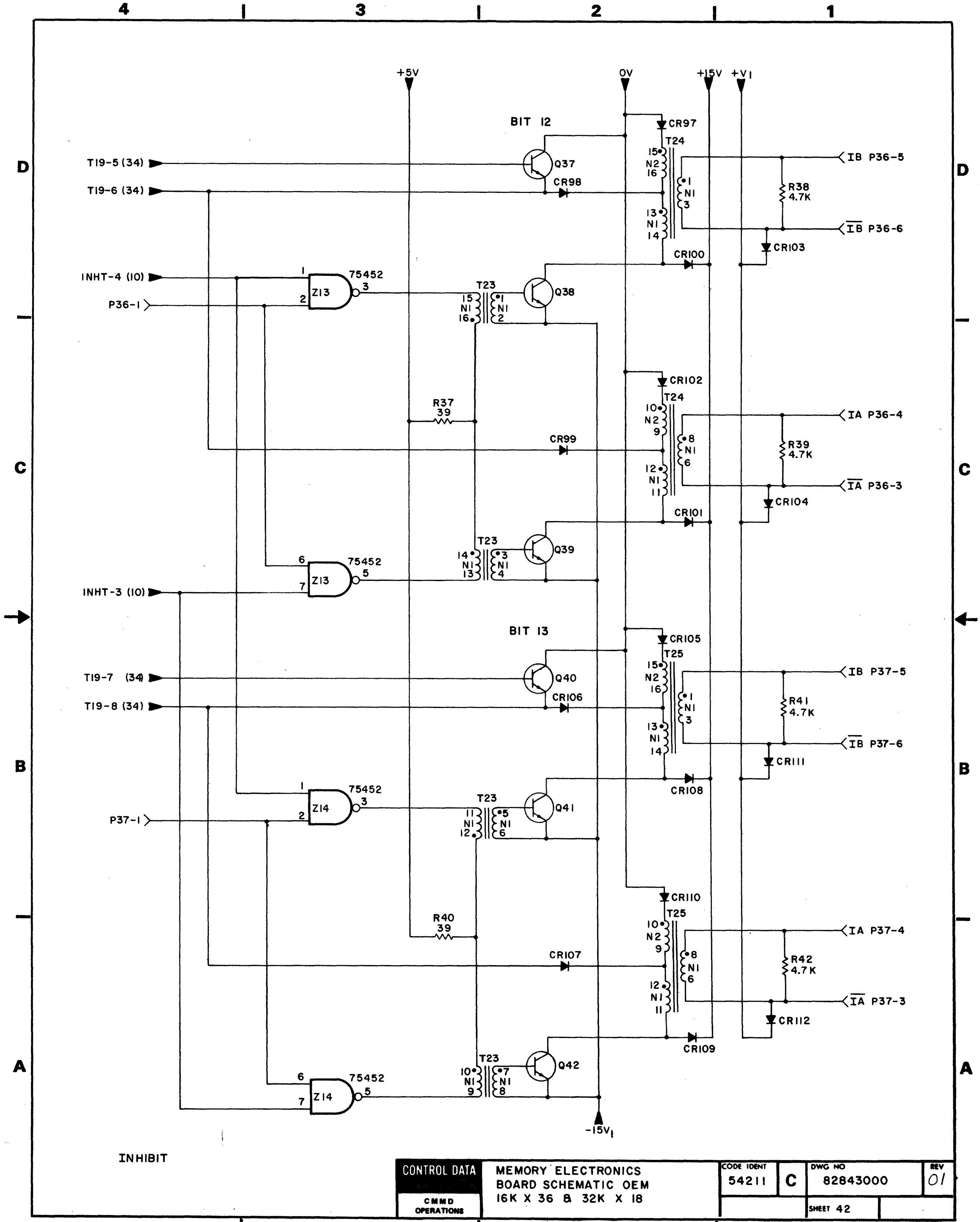
CONTROL DATA	MEMORY ELECTRONICS BOARD SCHEMATIC OEM 16K X 36 & 32K X 18	CODE IDENT 54211	C	DWG NO 82843000	REV 01
CMMD OPERATIONS				SHEET 39	



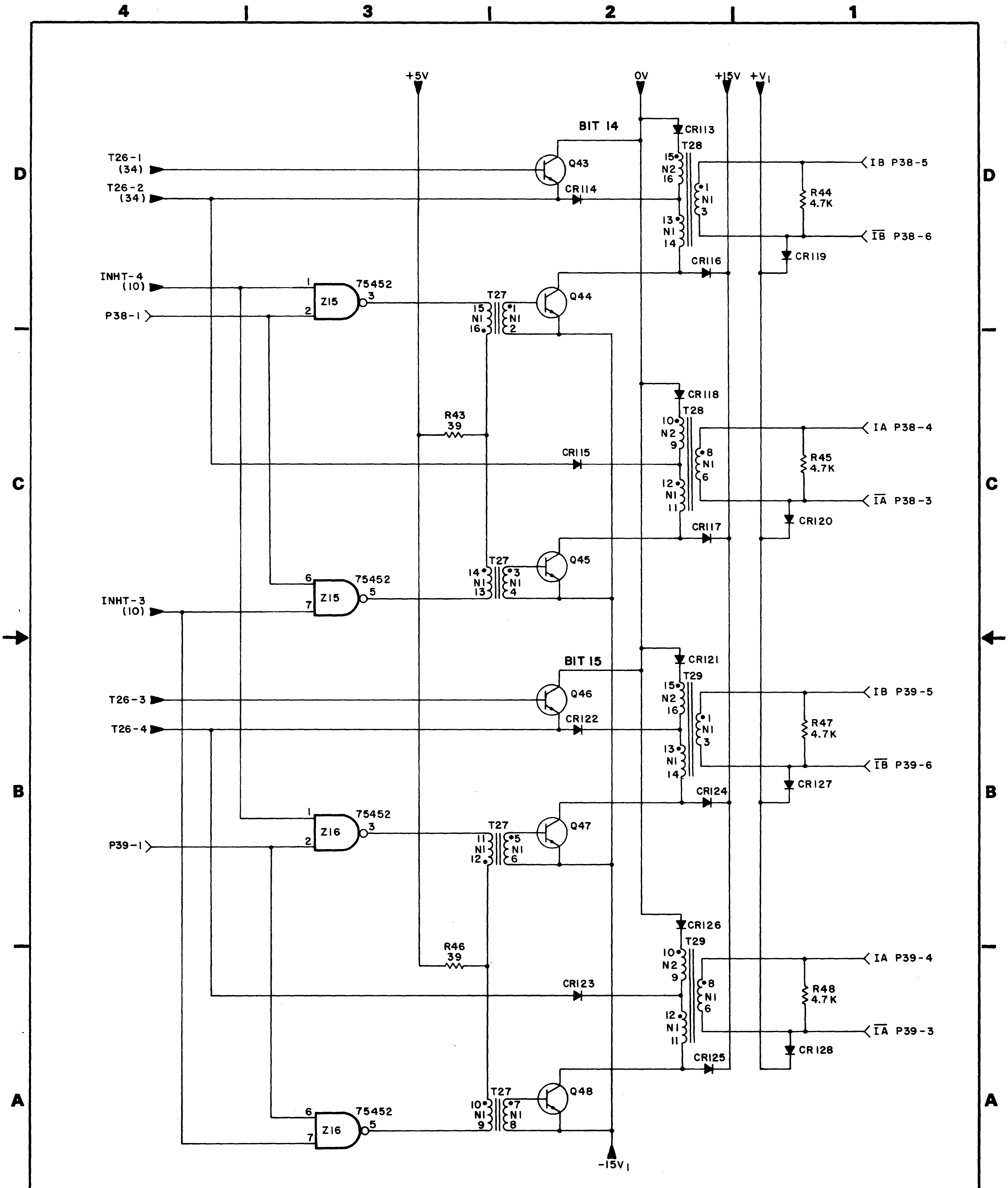
CONTROL DATA / CMMD OPERATIONS	MEMORY ELECTRONICS BOARD SCHEMATIC OEM 16K X 36 & 32K X 18	CODE IDENT 54211	C	DWG NO 82843000	REV 01
				SHEET 40	



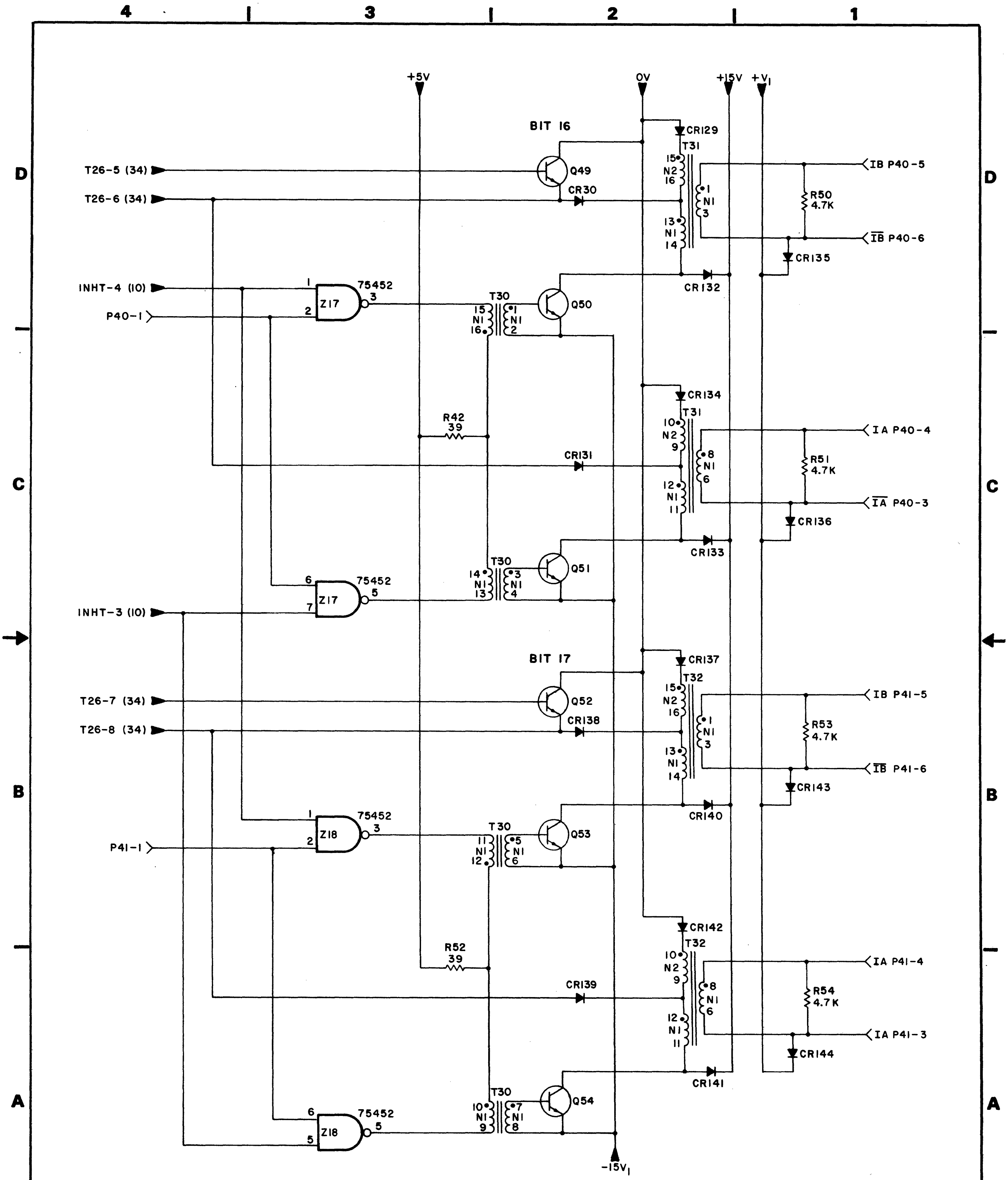
CONTROL DATA / CMMD OPERATIONS	MEMORY ELECTRONICS BOARD SCHEMATIC OEM 16K X 36 & 32K X 18	CODE IDENT 54211	C	DWG NO 82843000	REV 01
				SHEET 41	



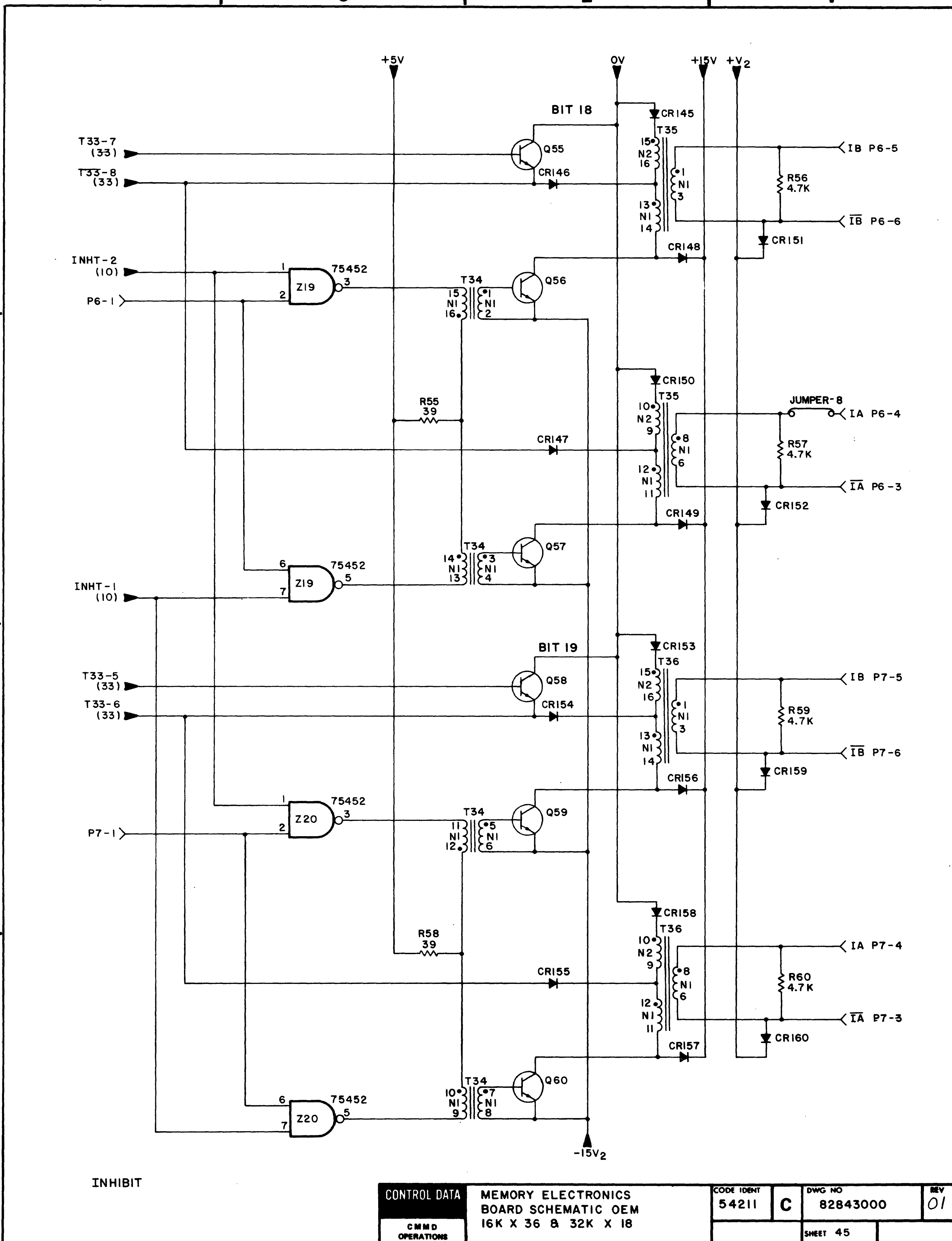
CONTROL DATA / CMMD OPERATIONS	MEMORY ELECTRONICS BOARD SCHEMATIC OEM 16K X 36 & 32K X 18	CODE IDENT 54211	C	DWG NO 82843000 / REV 01 / SHEET 42



CONTROL DATA CMMD OPERATIONS	MEMORY ELECTRONICS BOARD SCHEMATIC OEM 16K X 36 & 32K X 18	CODE IDENT 54211	C	DWG NO 82843000 / REV 01 / SHEET 43



CONTROL DATA CMMD OPERATIONS	MEMORY ELECTRONICS BOARD SCHEMATIC OEM 16K X 36 & 32K X 18	CODE IDENT 54211	C	DWG NO 82843000 / REV 01 / SHEET 44

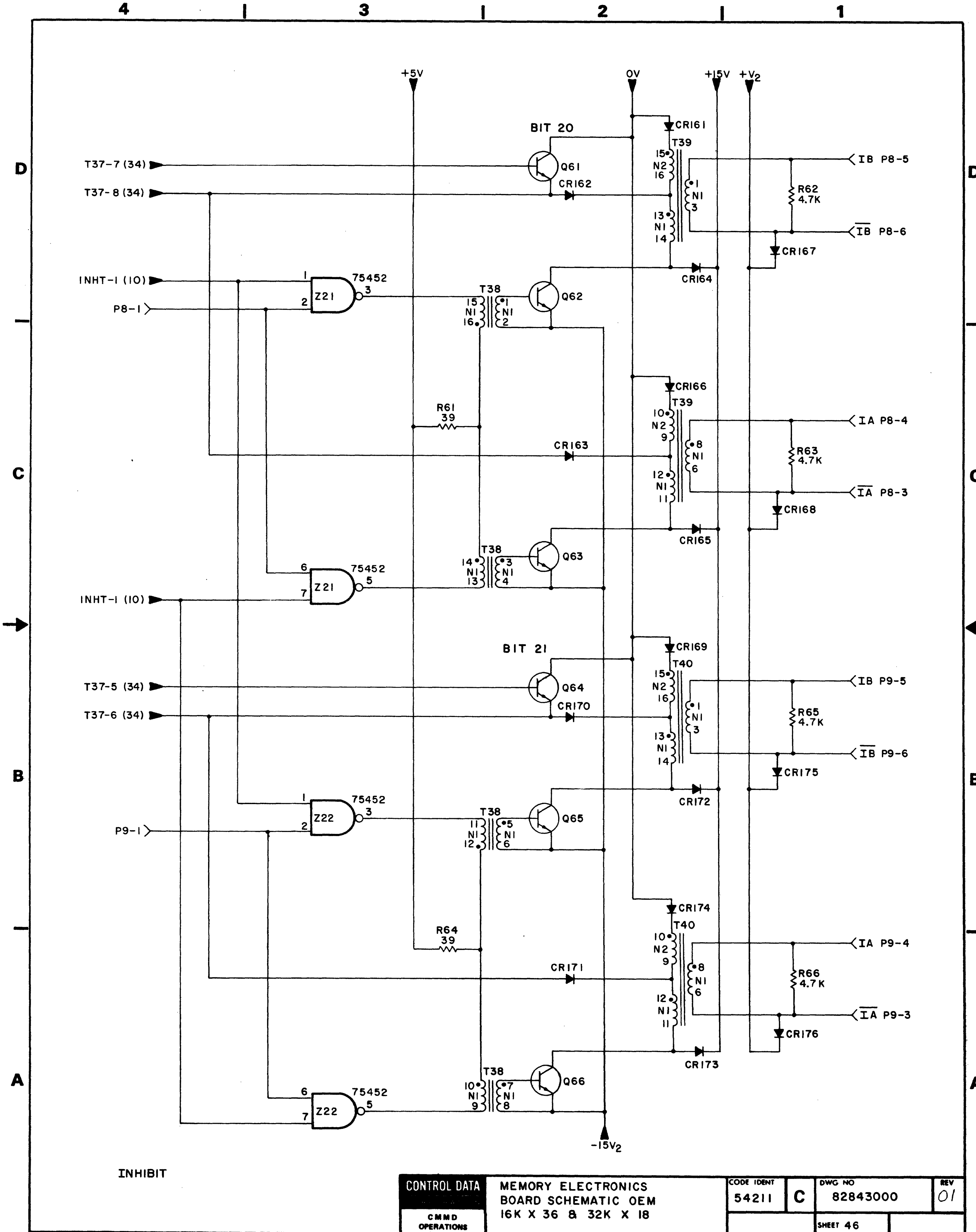


CONTROL DATA

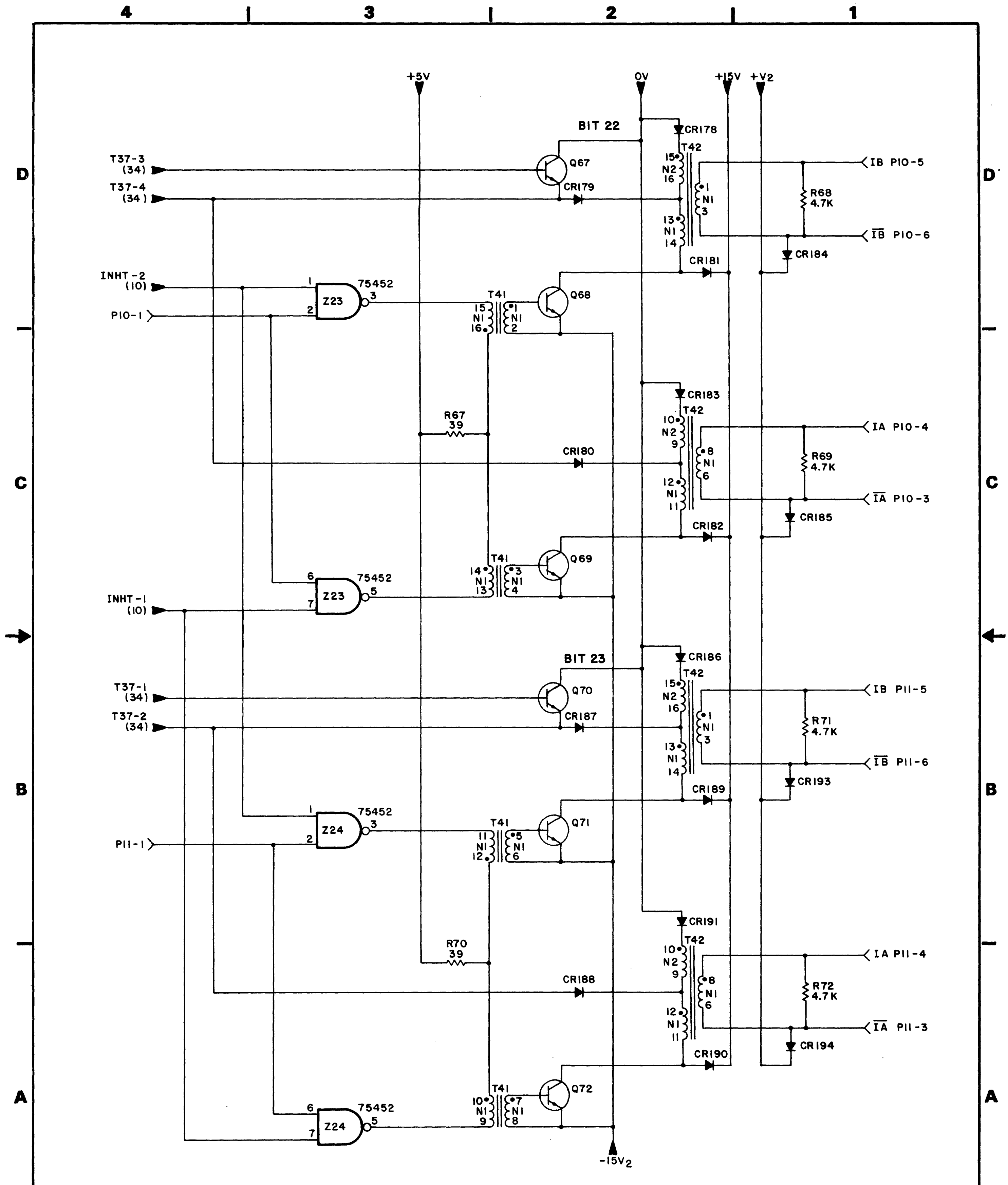
CMMD OPERATIONS

MEMORY ELECTRONICS BOARD SCHEMATIC OEM 16K X 36 & 32K X 18

CODE IDENT		DWG NO	REV
54211	C	82843000	01
		SHEET 45	



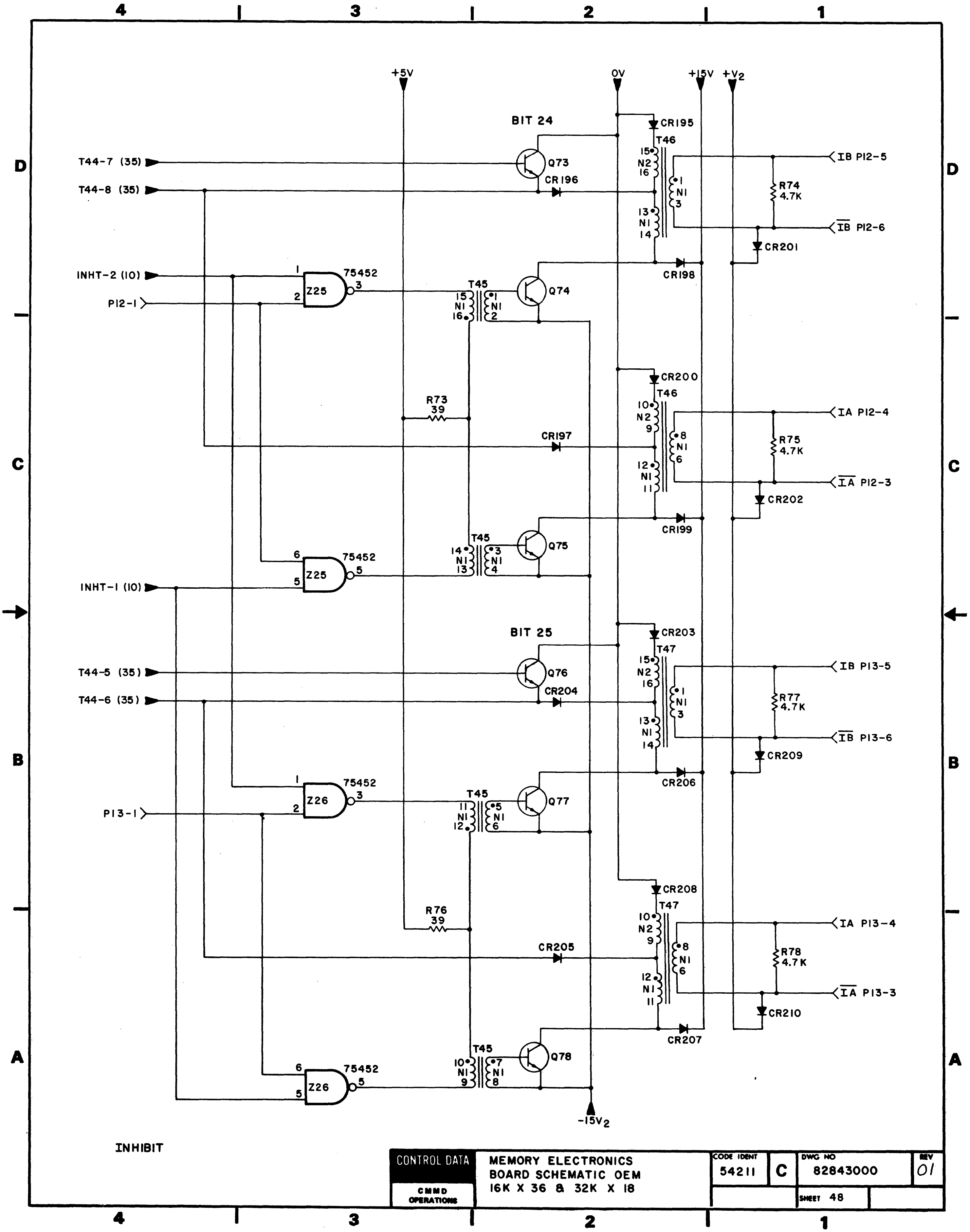
CONTROL DATA / CMMD OPERATIONS	MEMORY ELECTRONICS BOARD SCHEMATIC OEM 16K X 36 & 32K X 18	CODE IDENT 54211	C	DWG NO 82843000	REV 01
				SHEET 46	



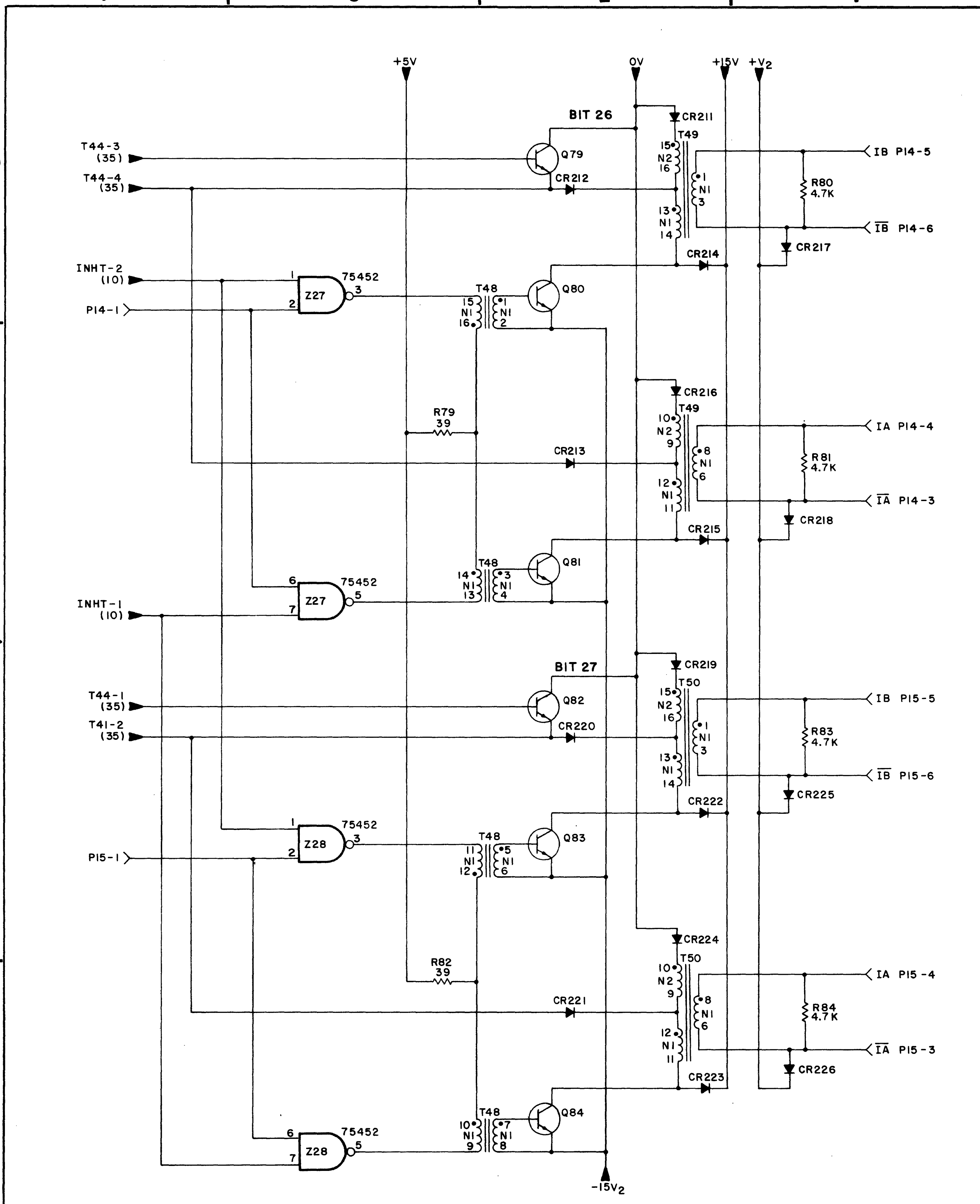
CONTROL DATA
CMMD OPERATIONS

MEMORY ELECTRONICS BOARD SCHEMATIC OEM 16K X 36 & 32K X 18

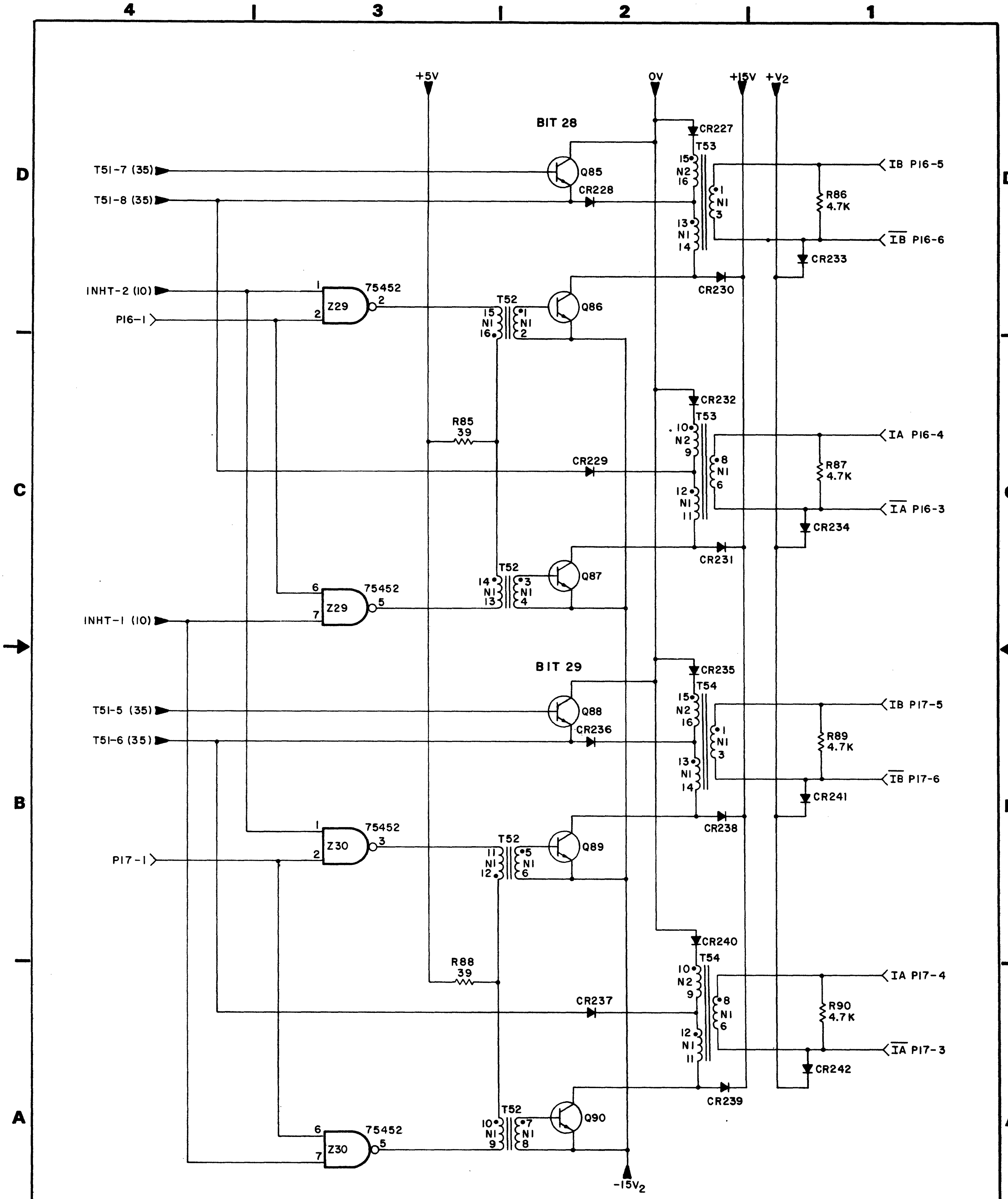
CODE IDENT		DWG NO	REV
54211	C	82843000	01
		SHEET 47	



CONTROL DATA CMMD OPERATIONS	MEMORY ELECTRONICS BOARD SCHEMATIC OEM 16K X 36 & 32K X 18	CODE IDENT 54211	C	DWG NO 82843000	REV 01
				SHEET 48	

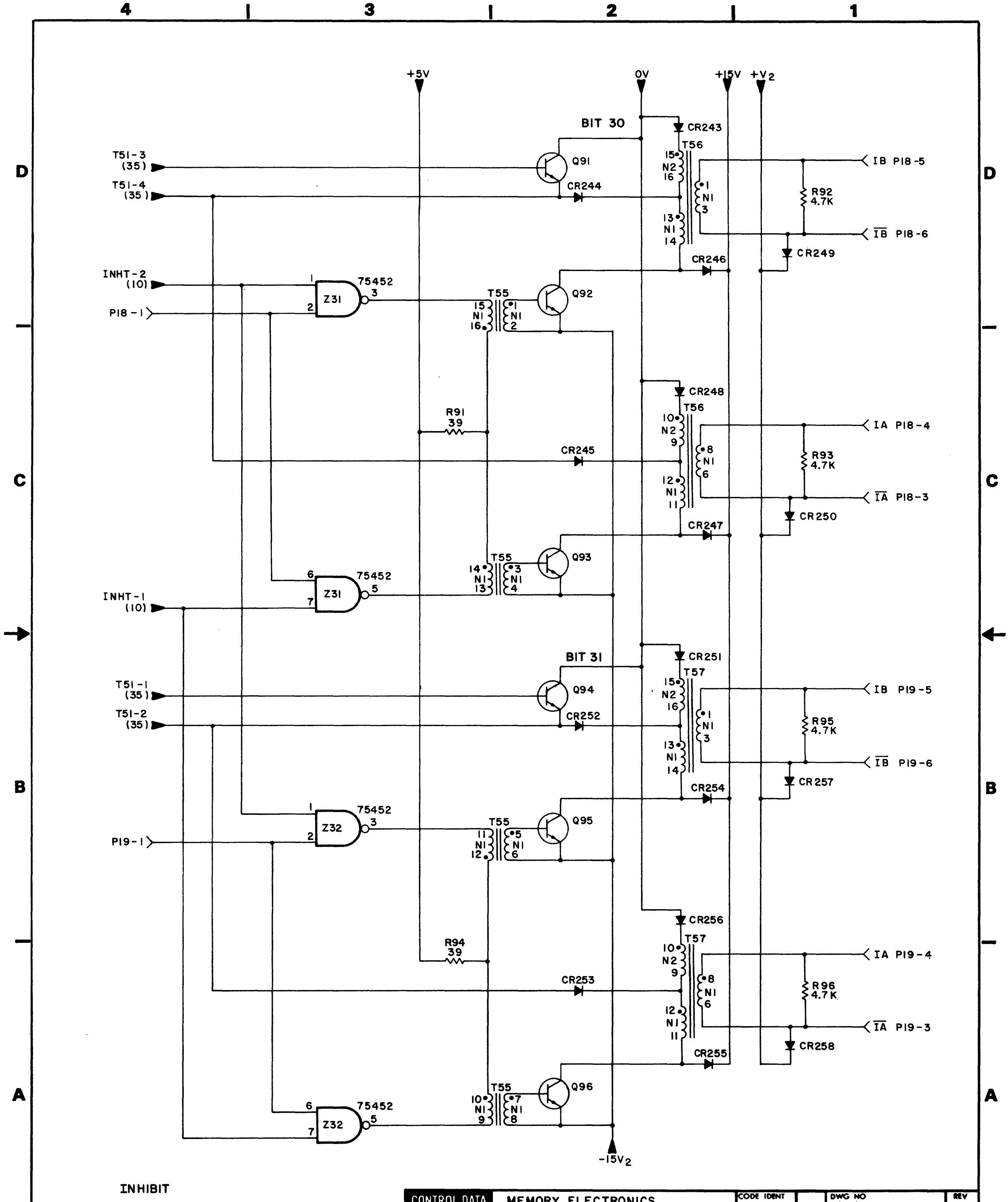


CONTROL DATA CMMD OPERATIONS	MEMORY ELECTRONICS BOARD SCHEMATIC OEM 16K X 36 & 32K X 18	CODE IDENT 54211	C	DWG NO 82843000	REV 01
				SHEET 49

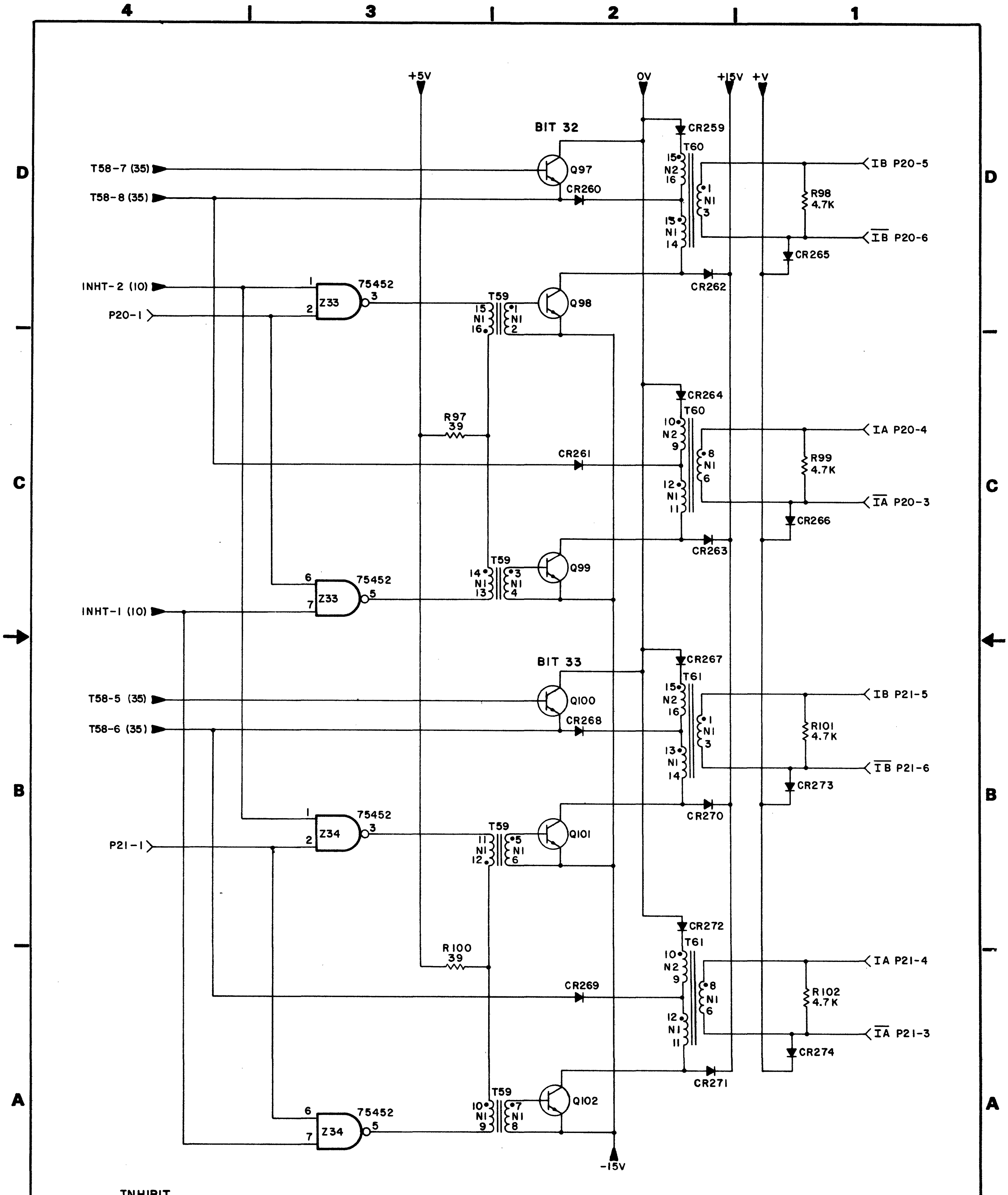


INHIBIT

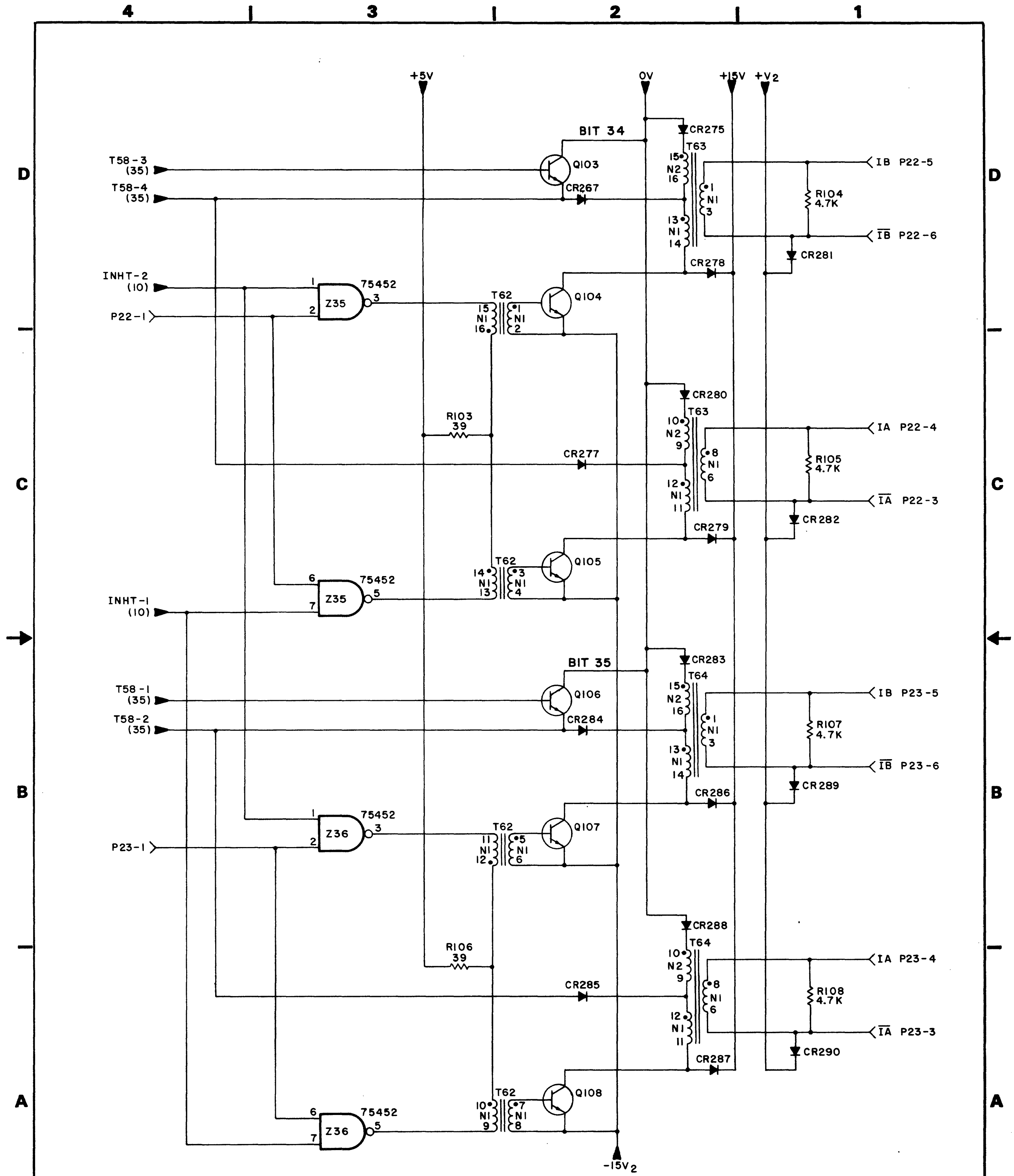
CONTROL DATA / CMMD OPERATIONS	MEMORY ELECTRONICS BOARD SCHEMATIC OEM 16K X 36 & 32K X 18	CODE IDENT 54211	C	DWG NO 82843000	REV 01
				SHEET 50	



CONTROL DATA CMMD OPERATIONS	MEMORY ELECTRONICS BOARD SCHEMATIC OEM 16K X 36 & 32K X 18	CODE IDENT 54211	C	DWG NO 82843000 REV 01 SHEET 51



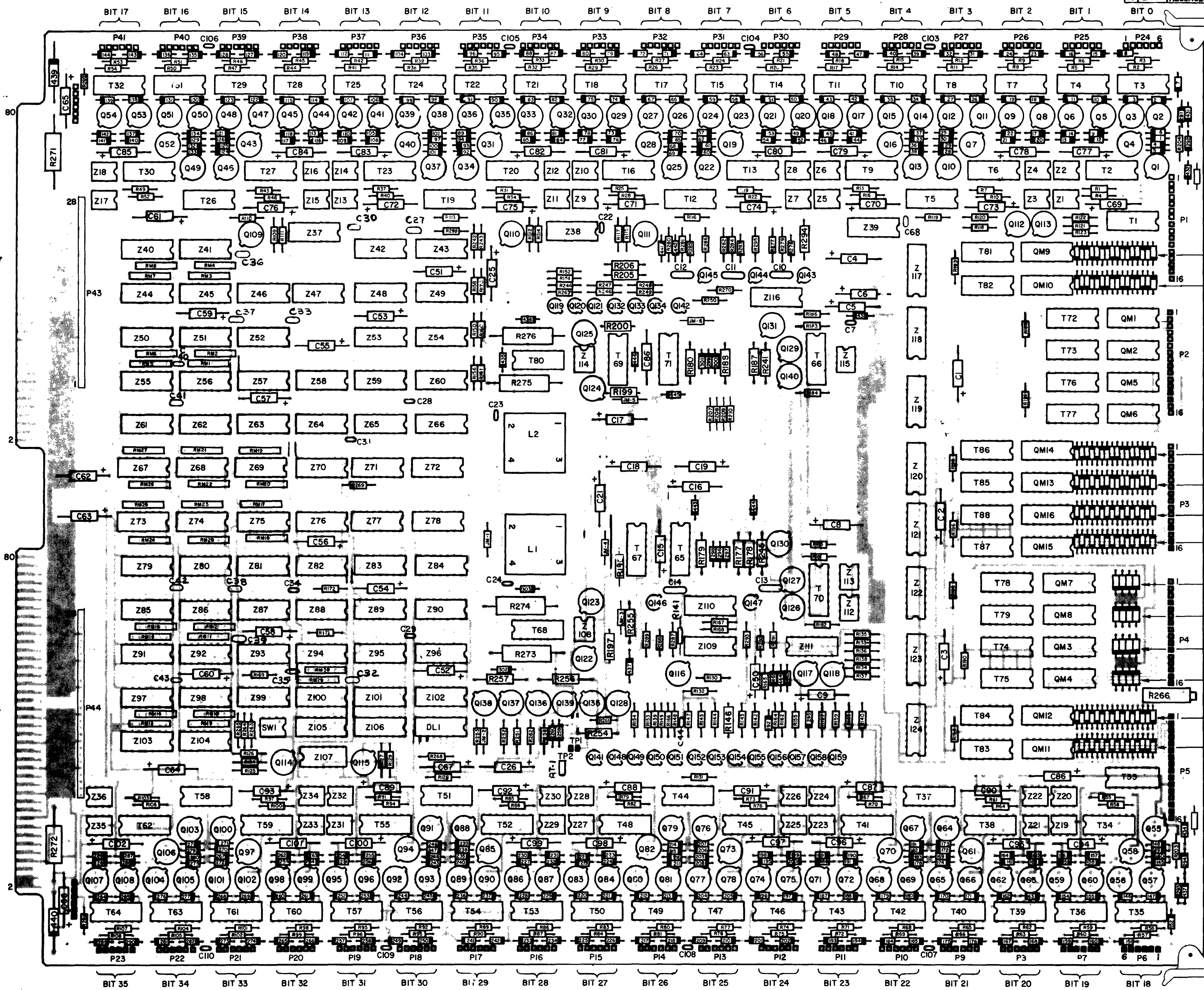
CONTROL DATA CMMD OPERATIONS	MEMORY ELECTRONICS BOARD SCHEMATIC OEM 16K X 36 & 32K X 18	CODE IDENT. 54211	C	DWG NO 82843000	REV 01
				SHEET 52	



INHIBIT

CONTROL DATA / CMMD OPERATIONS	MEMORY ELECTRONICS BOARD SCHEMATIC OEM 16K X 36 & 32K X 18	CODE IDENT 54211	C	DWG NO 82843000 / REV 01 / SHEET 53

LTR	DESCRIPTION	DRFT	DATE	CHKD	APP
01	RELEASED CLASS B	MM			



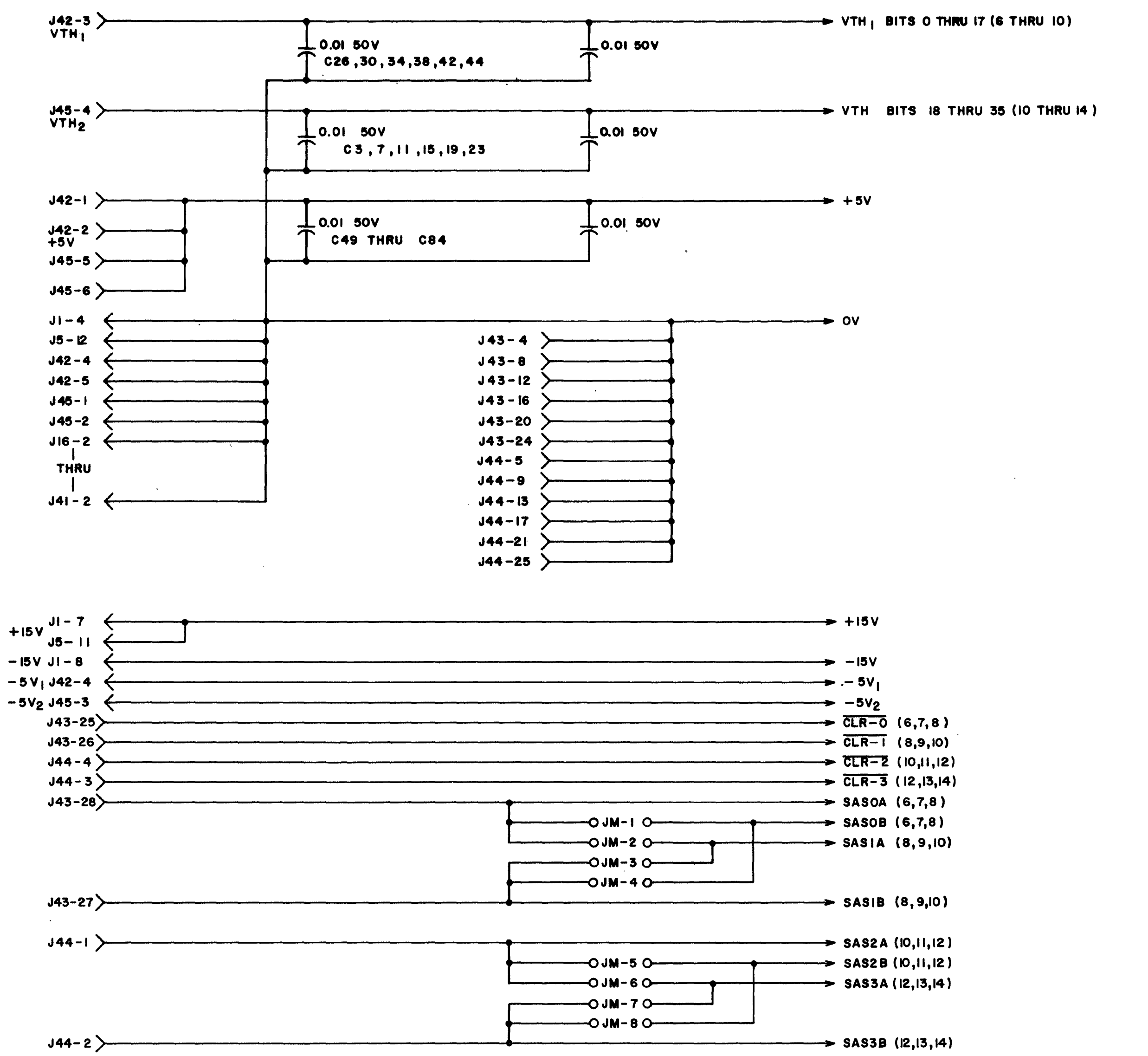
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	CONTROL DATA	CMMD OPERATIONS
FIRST USED ON	OEMMM	
DO NOT SCALE DRAWING	DWN	
MATERIAL	CHKD	
FINISH	ENGR / MFG / APPR	

TITLE MEMORY ELECTRONICS BOARD SCHEMATIC ASSEMBLY OEM 16K X 36 BIT

CODE IDENT 54211 | E | DRAWING NO 82843000

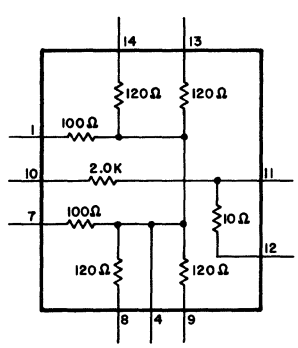
SCALE 2/1 | 82842600 | SHEET 54 OF 54

DETACHED LISTS



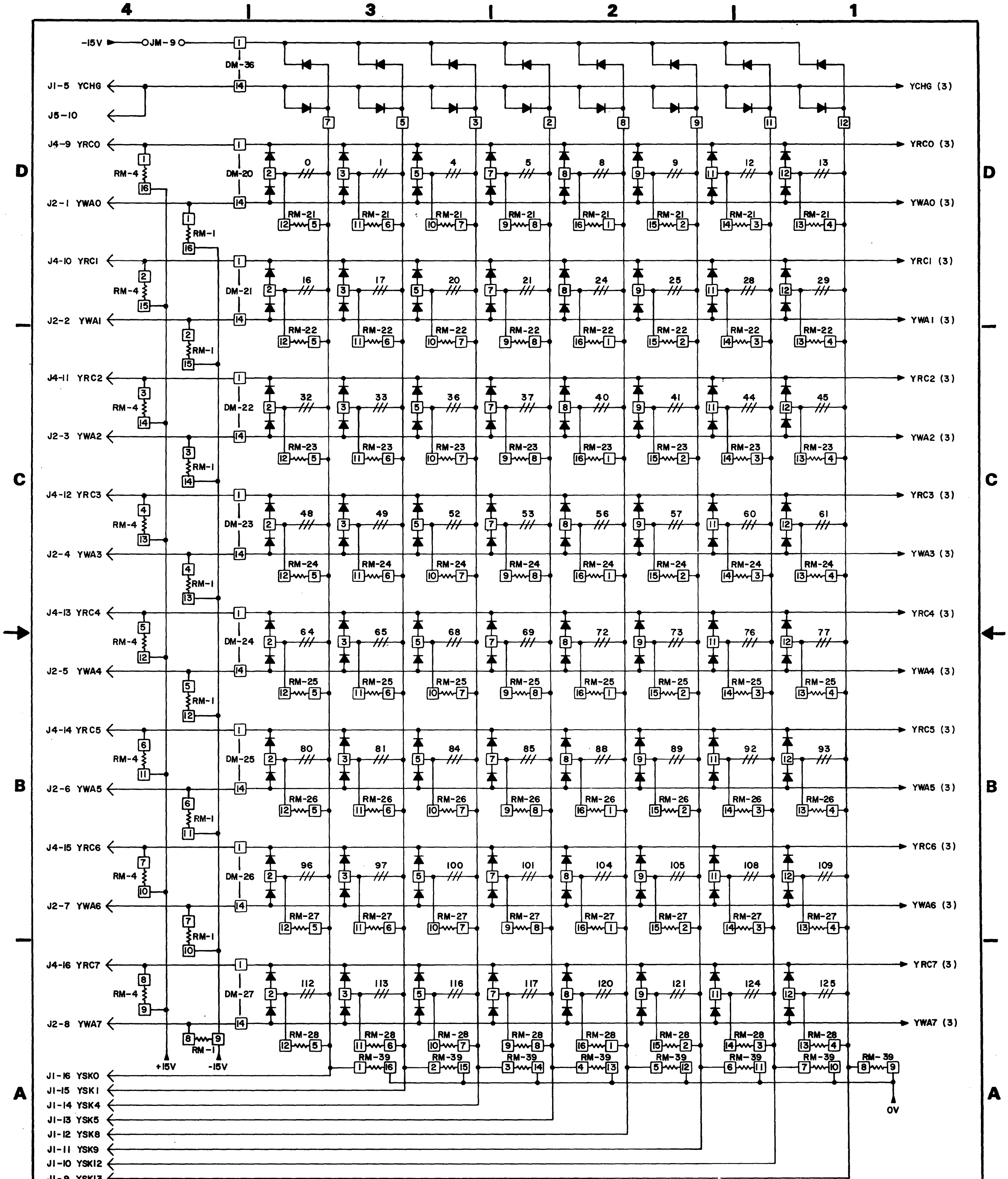
NOTES:

1. UNLESS OTHERWISE SPECIFIED. ALL RESISTORS ARE 1/4W, 5%, ALL DIODES ARE IN4607, ALL CAPACITORS ARE IN MICROFARADS.
2. THE FOLLOWING RESISTOR MODULES ARE 330 OHMS: RM-5 THRU RM-28, RM-31 THRU RM-38.
3. THE FOLLOWING RESISTOR MODULES ARE 470 OHMS: RM1 THRU RM4, RM39 THRU RM46.
4. RM47 THRU RM53 ARE NOT USED.
5. BELOW IS A SCHEMATIC DRAWING OF RM54 THRU RM89:



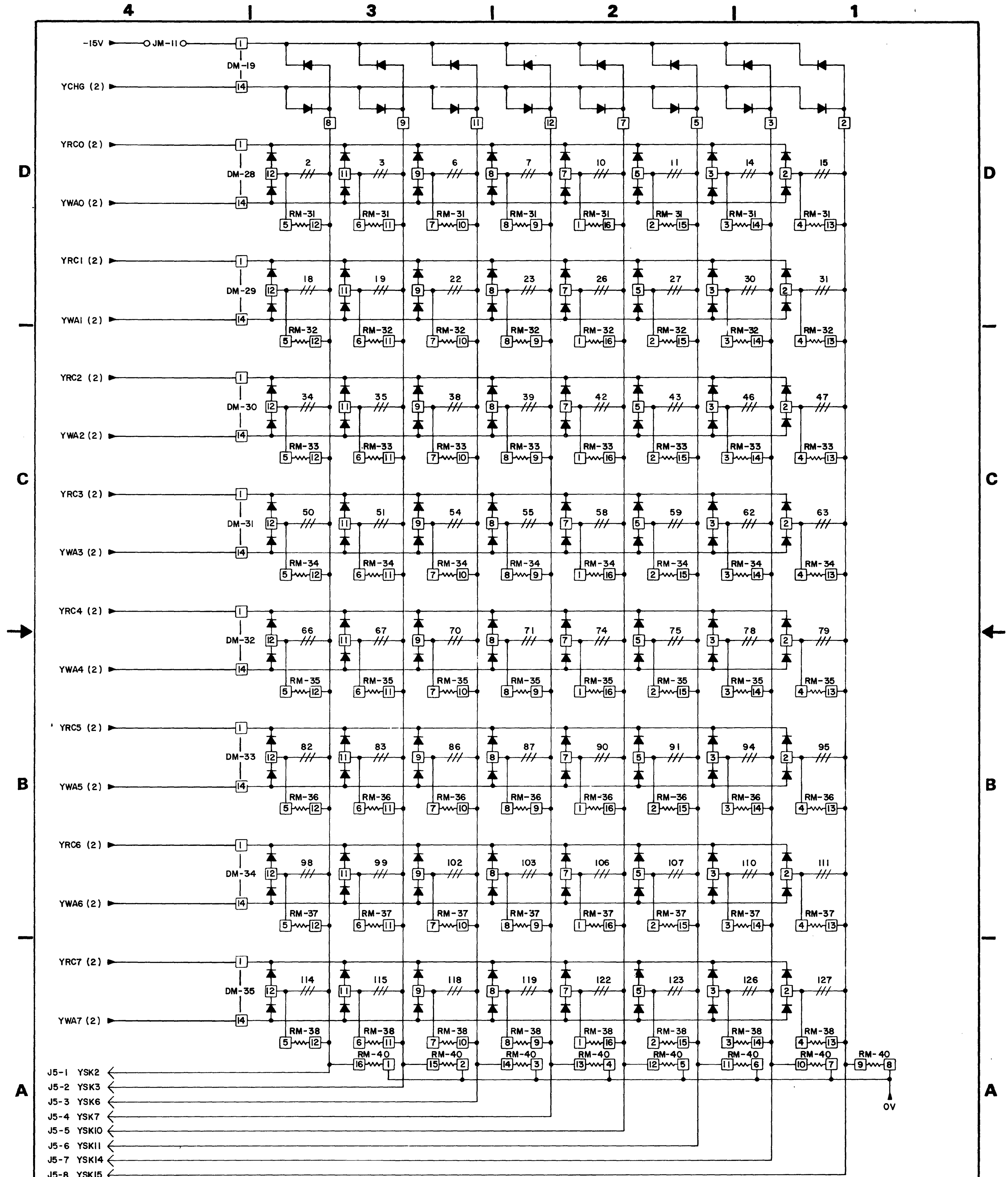
6. ⇆ THIS SYMBOL REPRESENTS A MALE PIN CONNECTOR.
7. THIS SYMBOL REPRESENTS A FEMALE PIN CONNECTOR.
8. ⟶ THIS SYMBOL WILL BE FOUND ON RIGHT BORDER, IT INDICATES DIRECTION OF SIGNAL FLOW. TO RIGHT OF ARROW WILL BE SIGNAL NAME OR MNEMONIC AND IN PARENTHESES ( ) THE PAGE NUMBER OF ALL DESTINATIONS.
9. ⟵ THIS SYMBOL WILL BE FOUND ON LEFT BORDER, IT INDICATES DIRECTION OF SIGNAL FLOW. TO LEFT OF ARROW WILL BE SIGNAL NAME OR MNEMONIC AND IN PARENTHESES ( ) THE ORIGINATING PAGE.
10. JM-1, JM-3, JM-5, AND JM-7 ARE INSTALLED FOR 82791402 ASSEMBLIES.
11. JM-2, JM-4, JM-6, AND JM-8 ARE INSTALLED FOR 82791400 & 82791401 ASSEMBLIES.

CONTROL DATA / CMMD OPERATIONS	CORE ARRAY SCHEMATIC 94200	CODE IDENT 54211	C	DWG NO 91965100	REV
				SHEET 1 OF 15	



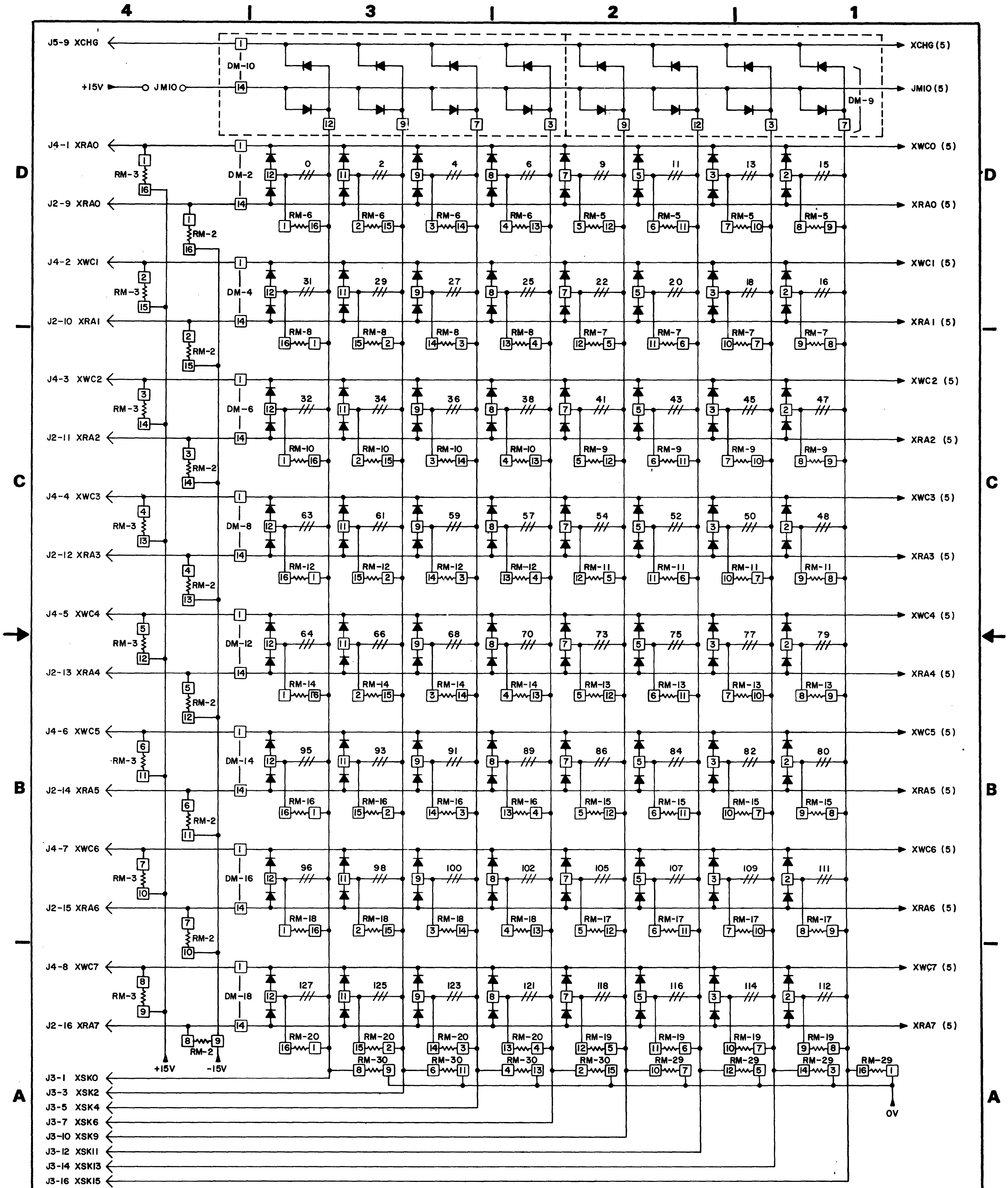
NOTES:
1. JM-9 IS NOT INSTALLED FOR 82791402 ASSEMBLIES.

CONTROL DATA CMMD OPERATIONS	CORE ARRAY SCHEMATIC 94200	CODE IDENT 54211	C	DWG NO 91965100	REV
				SHEET 2	



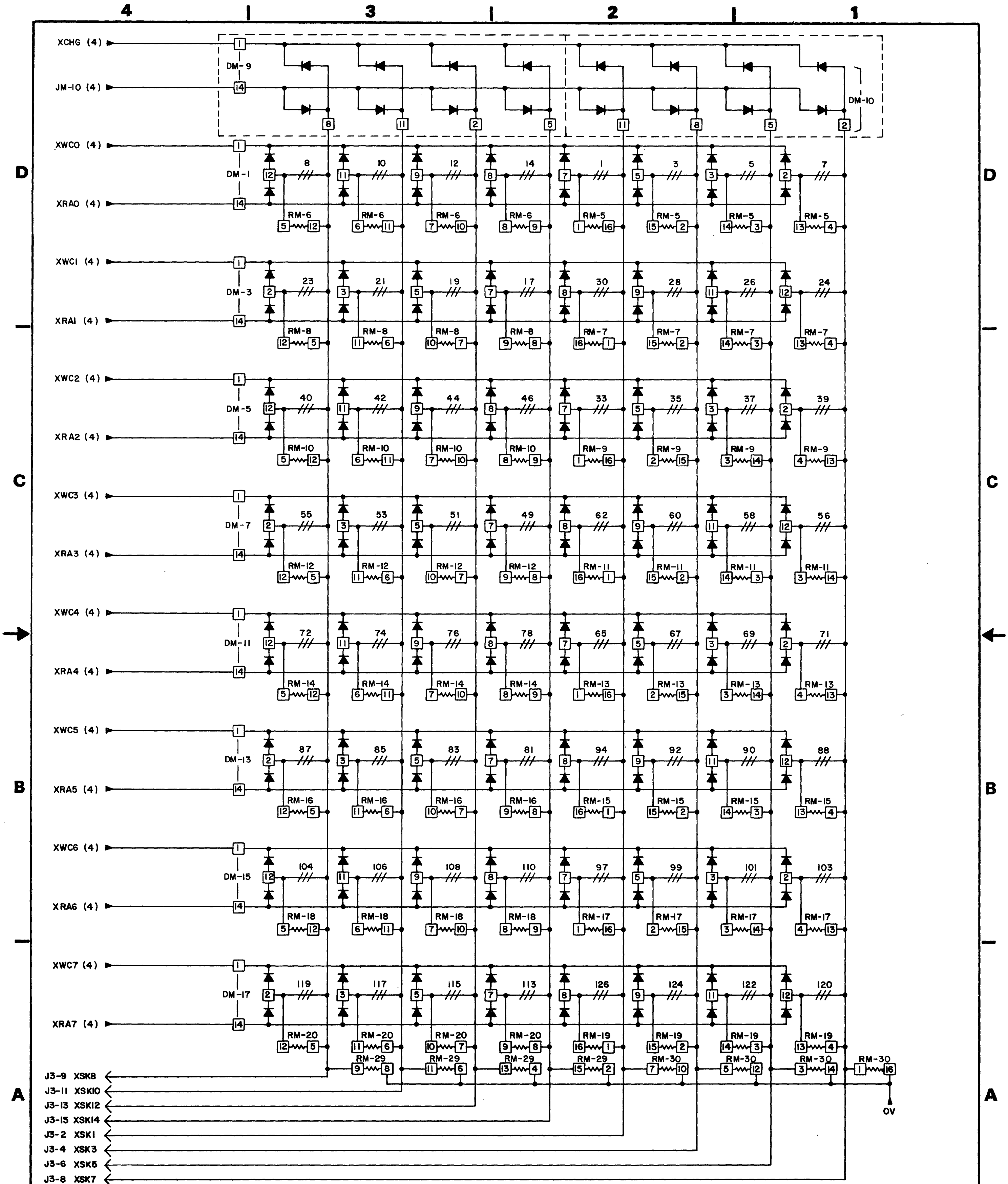
NOTES:
1. JM-11 IS NOT INSTALLED FOR 82791402 ASSEMBLIES.

CONTROL DATA CORPORATION CMMD OPERATIONS	CORE ARRAY SCHEMATIC 94200	CODE IDENT 54211	C	DWG NO 91965100	REV
				SHEET 3	

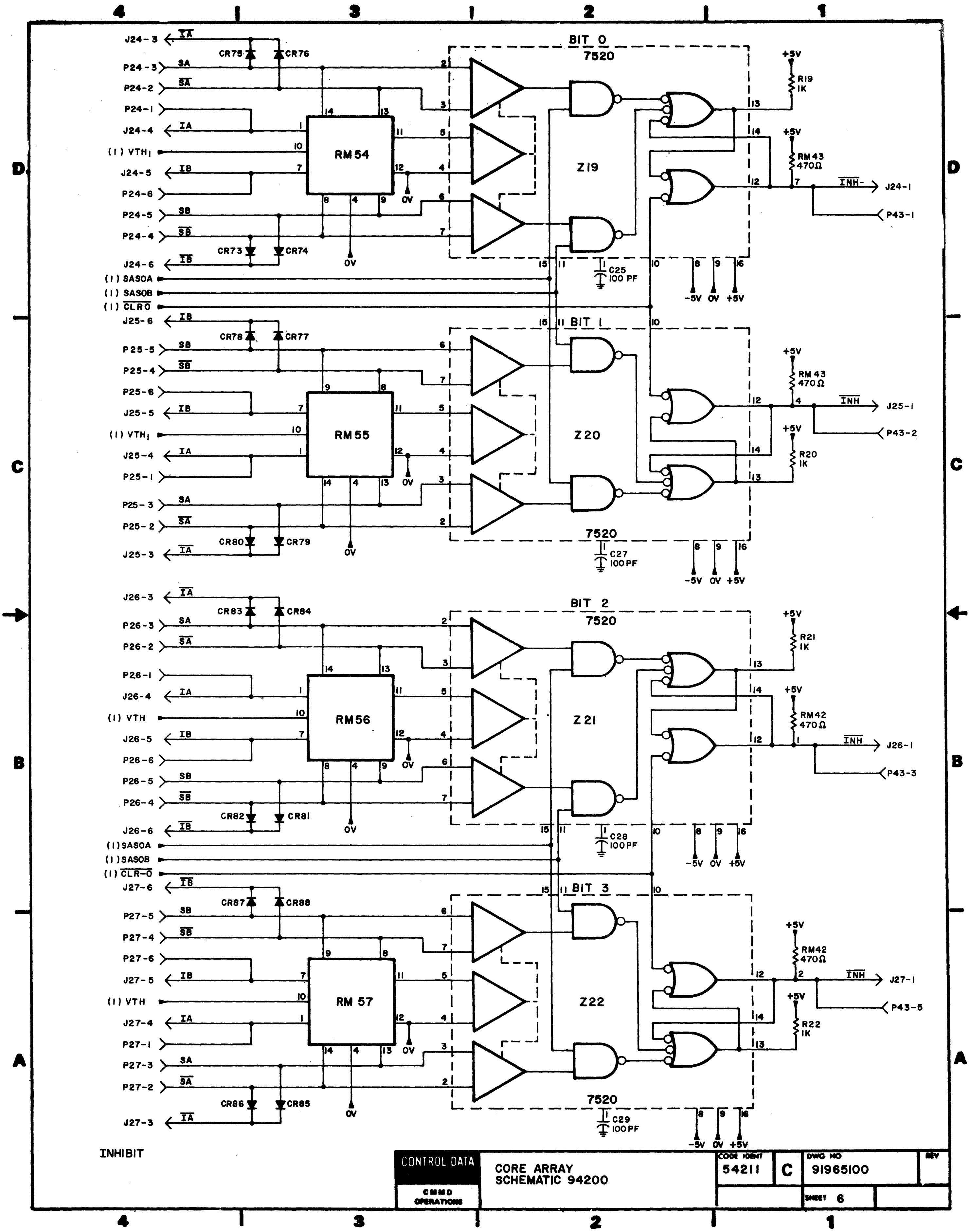


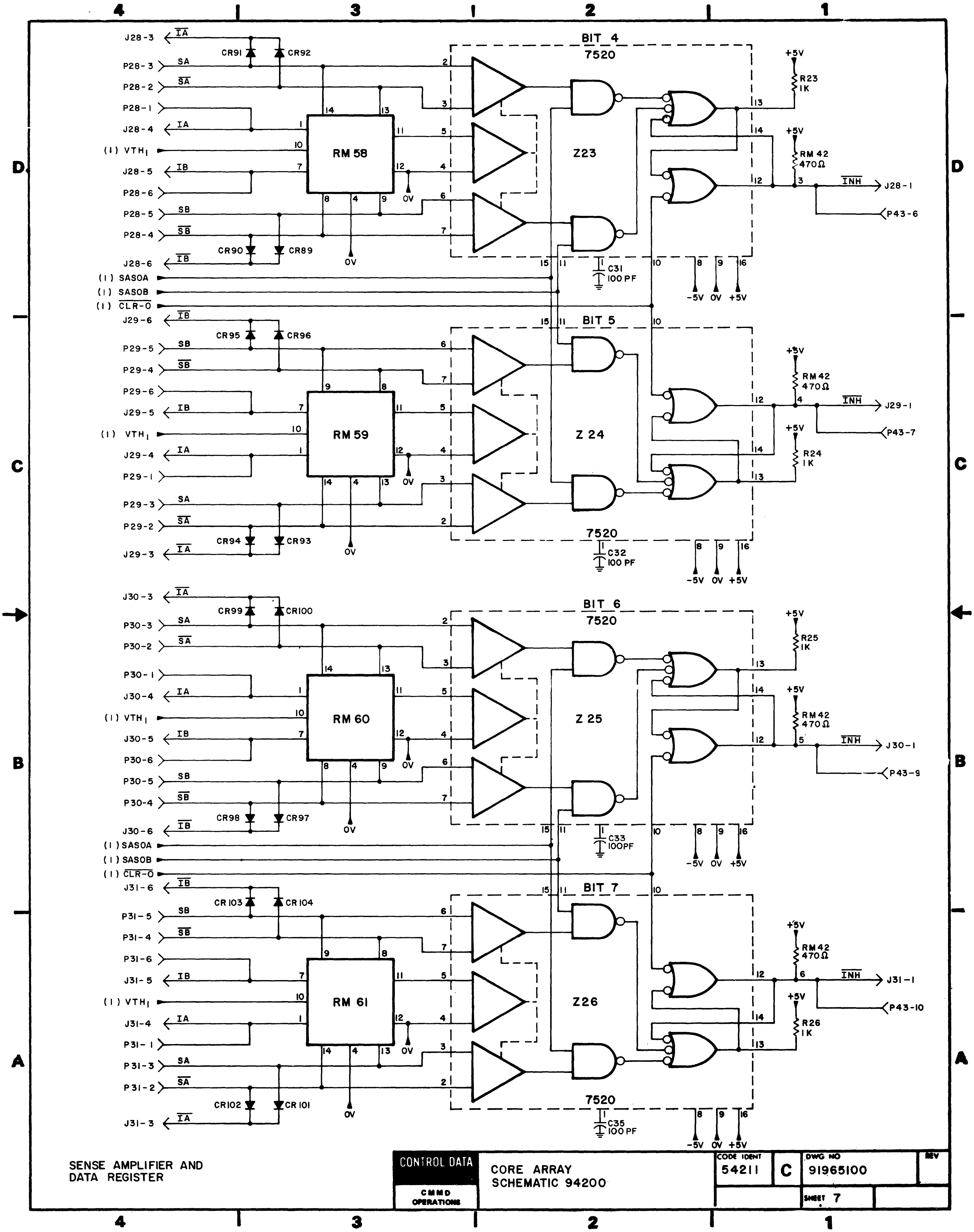
NOTES:
1. JM-10 IS NOT INSTALLED FOR 82791402 ASSEMBLIES.

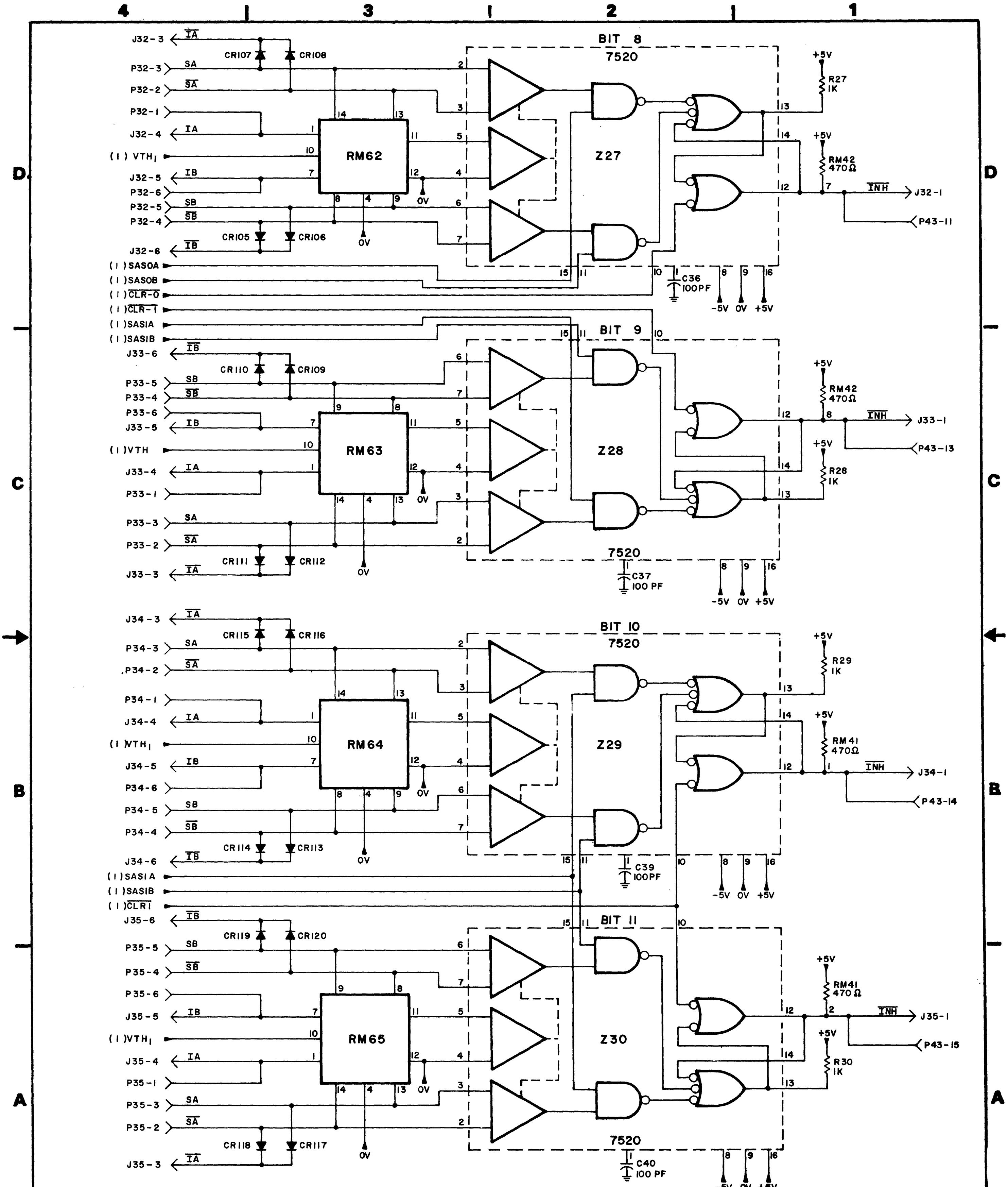
CONTROL DATA CMMD OPERATIONS	CORE ARRAY SCHEMATIC 94200	CODE IDENT 54211	C
DWG NO 91965100	REV	SHEET 4	



CONTROL DATA CMMD OPERATIONS	CORE ARRAY SCHEMATIC 94200	CODE IDENT 54211	C	DWG NO 91965100	REV
				SHEET 5	

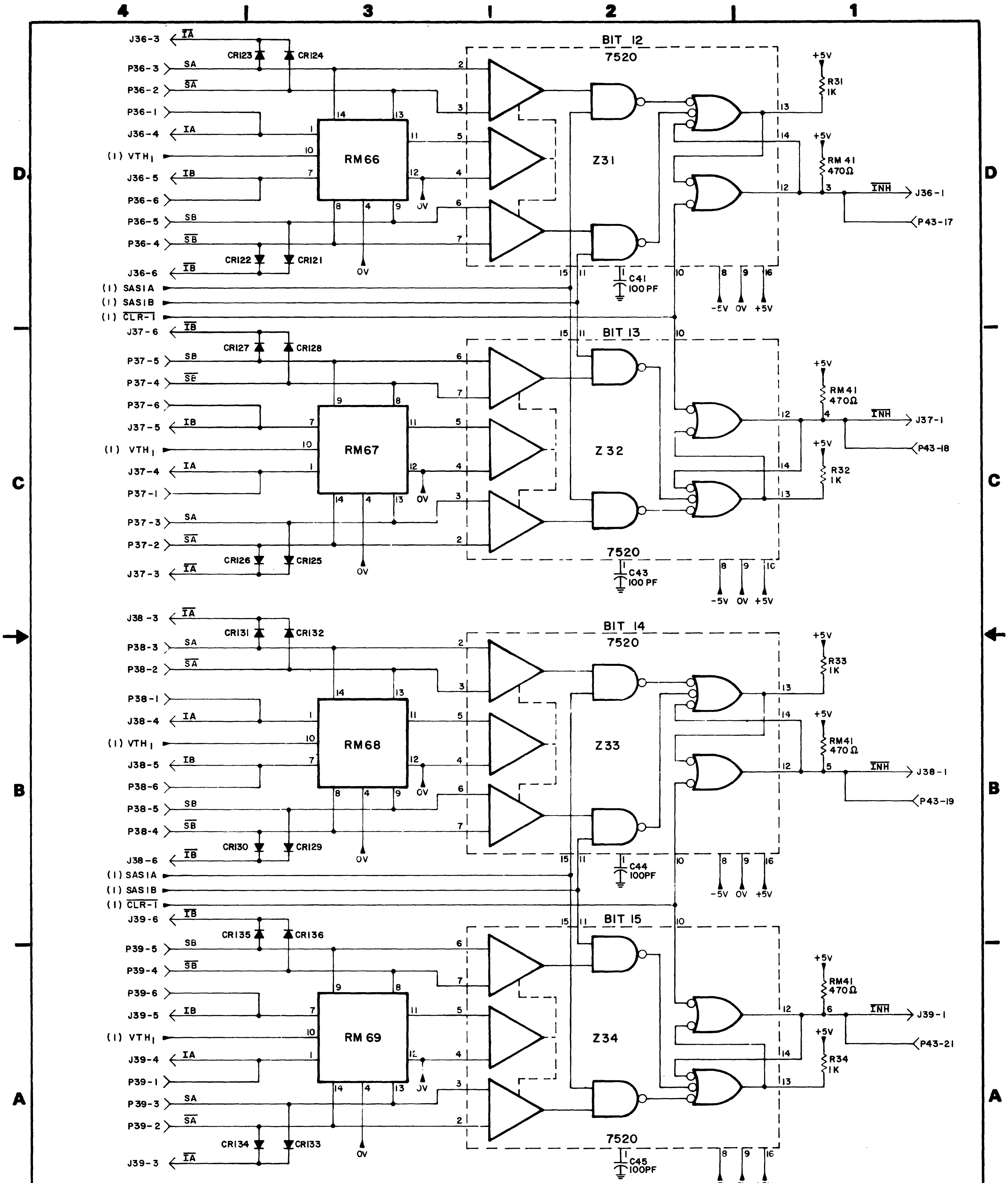

BIT 0
7520
RM54
Z19
J24-3
P24-3
P24-2
P24-1
J24-4
(1) VTH1
J24-5
P24-6
P24-5
P24-4
J24-6
(1) SASOA
(1) SASOB
(1) CLRO
CR75
CR76
CR73
CR74
C25 100 PF
R19 1K
RM43 470Ω
INH
J24-1
P43-1
BIT 1
RM55
Z20
J25-6
P25-5
P25-4
P25-6
J25-5
(1) VTH1
J25-4
P25-1
P25-3
P25-2
J25-3
CR78
CR77
CR80
CR79
C27 100PF
RM43 470Ω
R20 1K
J25-1
P43-2
BIT 2
RM56
Z21
J26-3
P26-3
P26-2
P26-1
J26-4
(1) VTH
J26-5
P26-6
P26-5
P26-4
J26-6
(1)SASOA
(1)SASOB
(1) CLR-O
CR83
CR84
CR82
CR81
C28 100PF
R21 1K
RM42 470Ω
J26-1
P43-3
BIT 3
RM 57
Z22
J27-6
P27-5
P27-4
P27-6
J27-5
(1) VTH
J27-4
P27-1
P27-3
P27-2
J27-3
CR87
CR88
CR86
CR85
C29 100PF
RM42 470Ω
R22 1K
J27-1
P43-5
-5V 0V +5V
INHIBIT
CONTROL DATA
CMMD OPERATIONS
CORE ARRAY
SCHEMATIC 94200
CODE IDENT 54211
C
DWG NO 91965100
REV
SHEET 6


BIT 4
7520
Z23
RM 58
J28-3
P28-3
P28-2
P28-1
J28-4
(1) VTH1
J28-5
P28-6
P28-5
P28-4
J28-6
(1) SASOA
(1) SASOB
(1) CLR-O
CR91
CR92
CR90
CR89
R23 1K
RM 42 470Ω
C31 100 PF
INH
J28-1
P43-6
BIT 5
7520
Z 24
RM 59
J29-6
P29-5
P29-4
P29-6
J29-5
J29-4
P29-1
P29-3
P29-2
J29-3
CR95
CR96
CR94
CR93
R24 1K
C32 100 PF
J29-1
P43-7
BIT 6
7520
Z 25
RM 60
J30-3
P30-3
P30-2
P30-1
J30-4
J30-5
P30-6
P30-5
P30-4
J30-6
CR99
CR100
CR98
CR97
R25 1K
C33 100PF
J30-1
P43-9
BIT 7
7520
Z26
RM 61
J31-6
P31-5
P31-4
P31-6
J31-5
J31-4
P31-1
P31-3
P31-2
J31-3
CR103
CR104
CR102
CR101
R26 1K
C35 100 PF
J31-1
P43-10
-5V
0V
+5V
SENSE AMPLIFIER AND DATA REGISTER
CONTROL DATA
CMMD OPERATIONS
CORE ARRAY SCHEMATIC 94200
CODE IDENT 54211
C
DWG NO 91965100
REV
SHEET 7



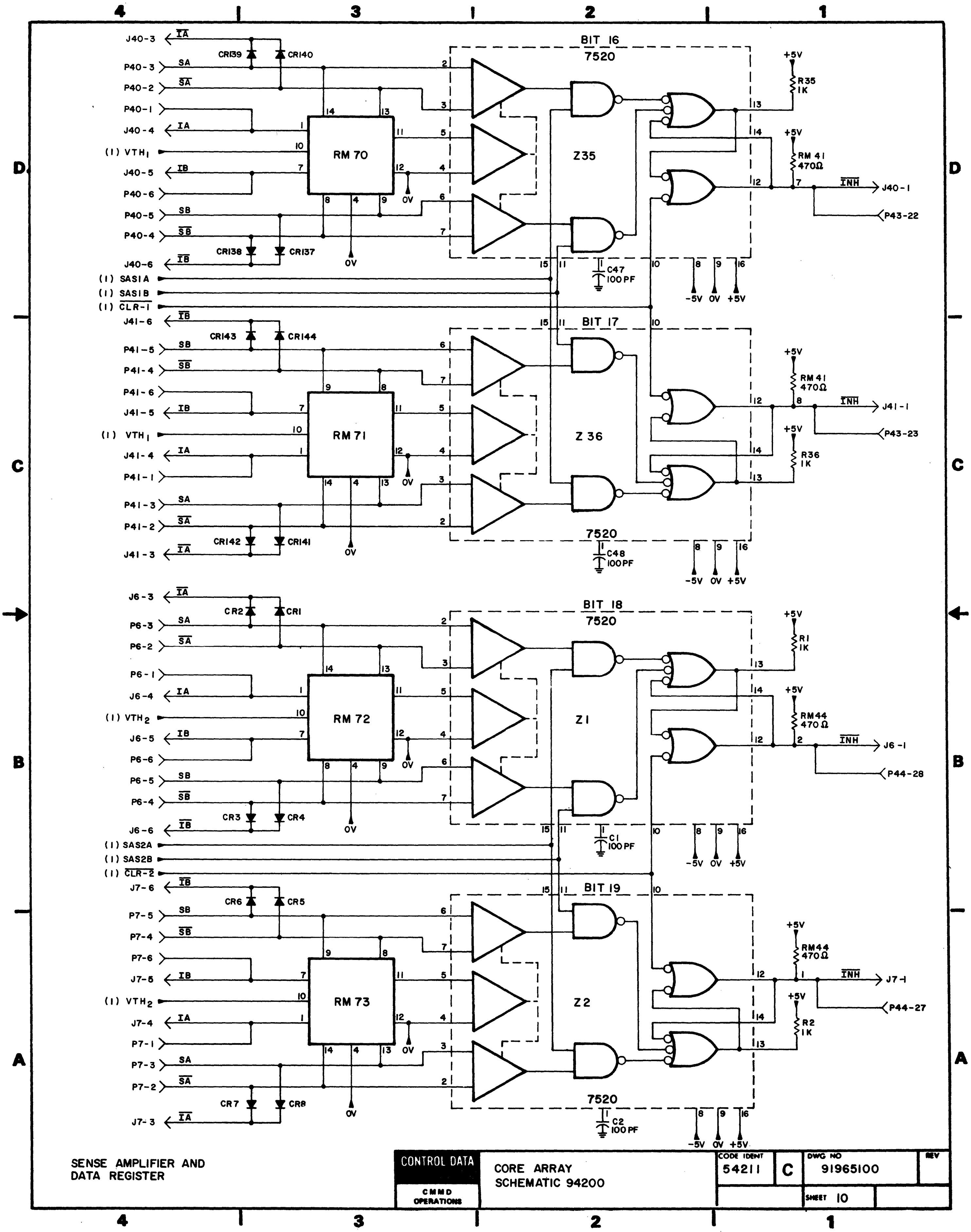
SENSE AMPLIFIER AND
DATA REGISTER

CONTROL DATA CMMD OPERATIONS	CORE ARRAY SCHEMATIC 94200	CODE IDENT 54211	C	DWG NO 91965100
				SHEET 8



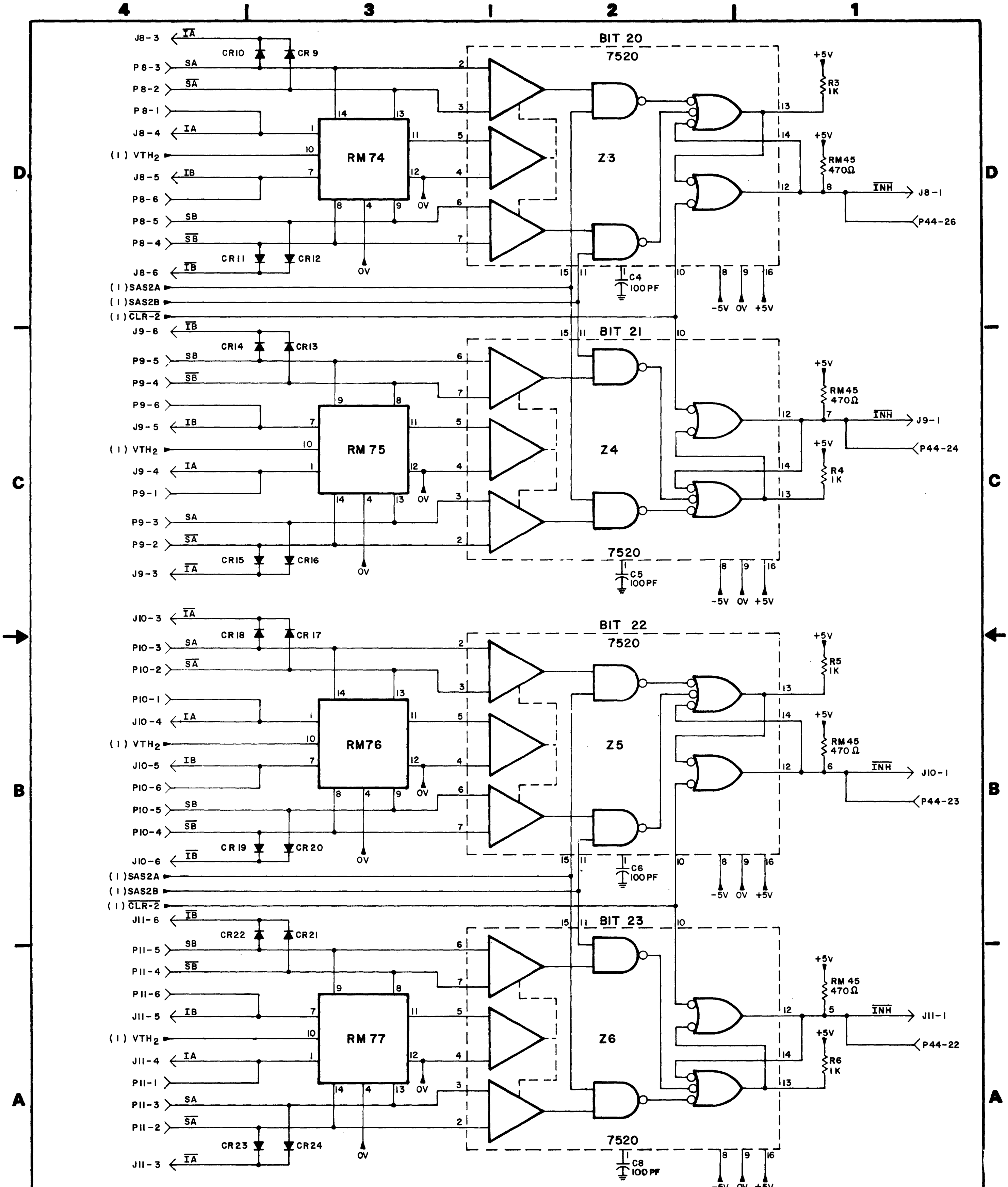
SENSE AMPLIFIER AND
DATA REGISTER

CONTROL DATA CMMD OPERATIONS	CORE ARRAY SCHEMATIC 94200	CODE IDENT 54211	C	DWG NO 91965100	REV
				SHEET 9	



SENSE AMPLIFIER AND DATA REGISTER

CONTROL DATA / CMMD OPERATIONS	CORE ARRAY SCHEMATIC 94200	CODE IDENT 54211	C	DWG NO 91965100	REV
				SHEET 10	

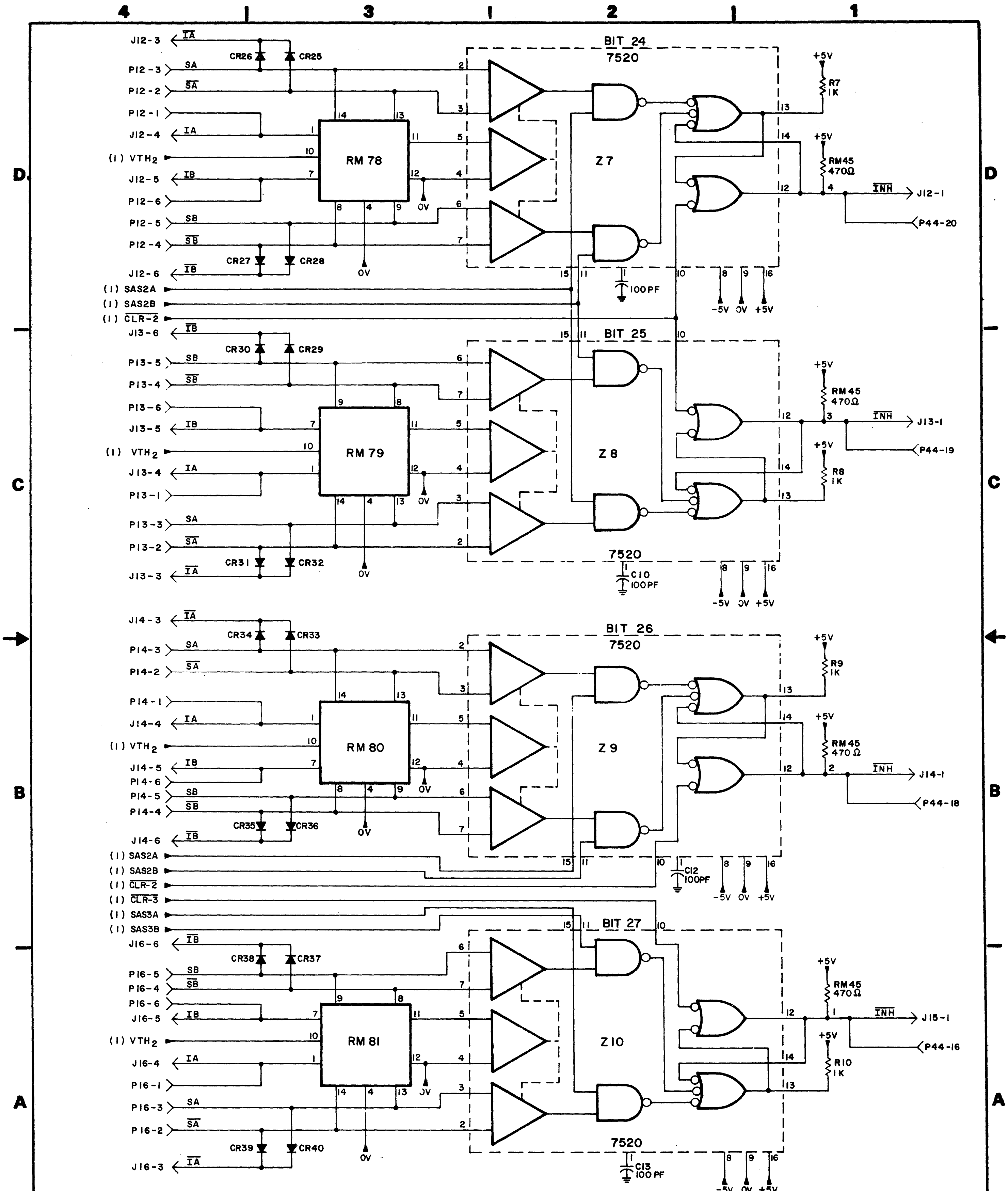


CONTROL DATA

CMMD OPERATIONS

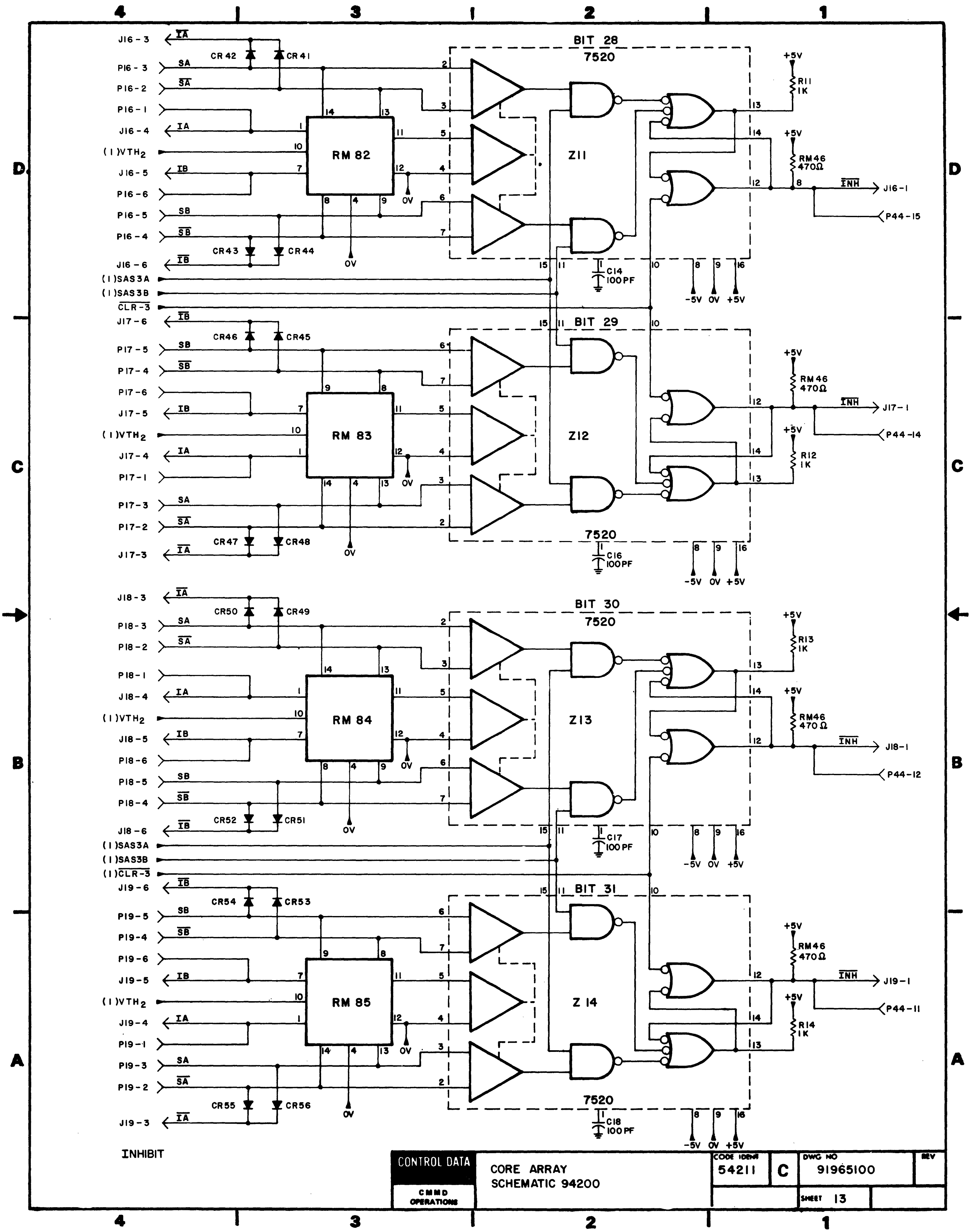
CORE ARRAY
SCHEMATIC 94200

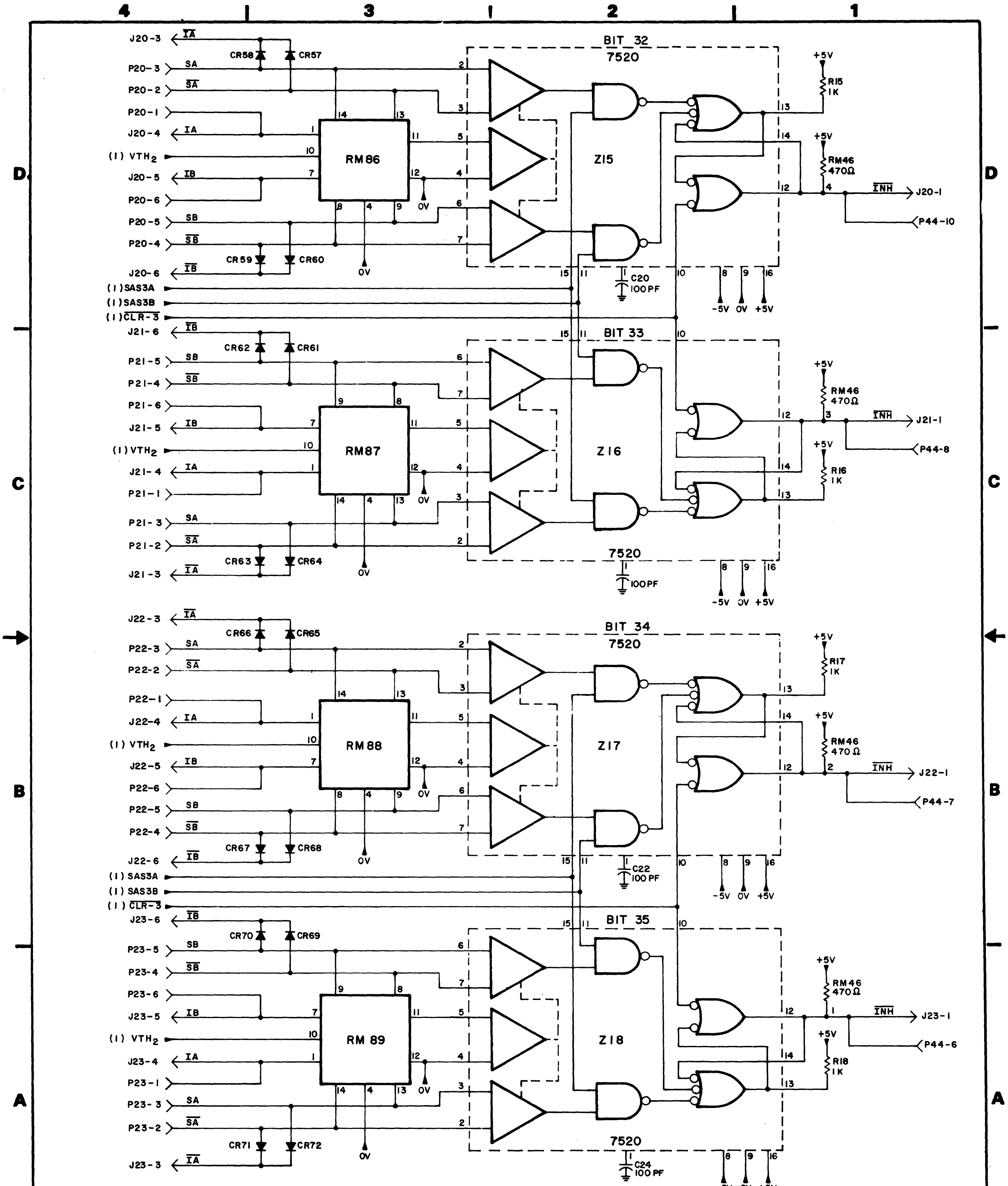
CODE IDENT		DWG NO	REV
54211	C	91965100	
		SHEET 11	



SENSE AMPLIFIER AND DATA REGISTER

CONTROL DATA CMMD OPERATIONS	CORE ARRAY SCHEMATIC 94200	CODE IDENT 54211	C	DWG NO 91965100
				SHEET 12

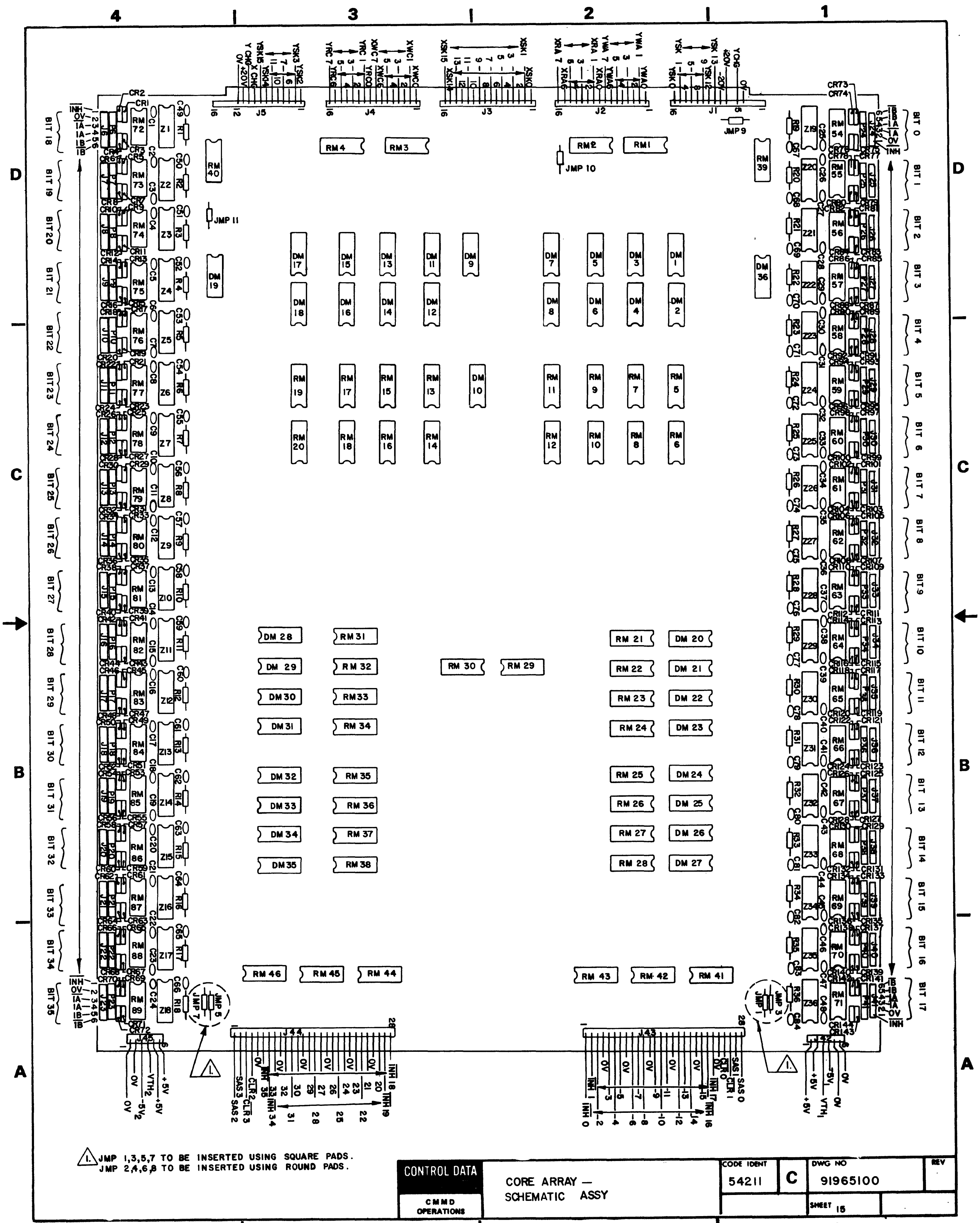

BIT 28
7520
Z11
RM 82
BIT 29
Z12
RM 83
BIT 30
7520
Z13
RM 84
BIT 31
Z 14
RM 85
INHIBIT
CONTROL DATA
CMMD OPERATIONS
CORE ARRAY
SCHEMATIC 94200
CODE IDENT 54211
C
DWG NO 91965100
SHEET 13



SENSE AMPLIFIER AND
DATA REGISTER

CORE ARRAY
SCHEMATIC 94200

CODE IDENT		DWG NO	REV
54211	C	91965100	
		SHEET 14	


JMP 1,3,5,7 TO BE INSERTED USING SQUARE PADS.
JMP 2,4,6,8 TO BE INSERTED USING ROUND PADS.
CONTROL DATA
CMMD OPERATIONS
CORE ARRAY — SCHEMATIC ASSY
CODE IDENT 54211
C
DWG NO 91965100
REV
SHEET 15

CONTROL DATA	MEMORY ELECTRONICS BOARD COMPONENT ASSEMBLY OEM 16K X 36 BIT	CODE IDENT	SHEET 1 of 6	PL	DOCUMENT NO. 82842600	REV. 02

FIND NO.	PART IDENTIFICATION	QUANTITY REQUIRED 00	01	UNIT OF MEAS	NOMENCLATURE OR DESCRIPTION	SPECIFICATIONS, NOTES, OR MATERIAL
1	82842700	1	1		MEMORY ELECTRONICS BD. BCP DETAIL	
2	82797000	2	2		HEADER, STRAIGHT 1-28, "BERG" 65274-3	
3	82813400	308	308		RECEPTACLE, MODD II. "AMP INC." 85861-2LP	
4	82826600	2	2		EJECTOR, CARD "SCANBE" S-200	
5	18653610	A/R	A/R		WIRE, 28 AWG TEFLON STRANDED, WHITE	
6						
7	82843000	-	-		MEMORY ELECTRONICS BD. SCHEMATIC	
8	62031200	20	20		SN7438J INTERGRATED CIRCUIT	Z40,41,44,45,50,51, 55,56,61,62,79,80
						85,86,91,92,97,98 103,104
9	50254600	8	8		SN74S00J INTERGRATED CIRCUIT	Z42,46,48,64,65,81, 88,95
10	15109200	9	9		SN74S04J INTERGRATED CIRCUIT	Z37,38,39,66,83,84 94,107,111
11	15117100	3	3		SN74S05J INTERGRATED CIRCUIT	Z109,110,116
12	15150900	5	5		SN74S08J INTERGRATED CIRCUIT	Z52,57,58,59,63
13	50254700	4	4		SN74S10J INTERGRATED CIRCUIT	Z53,82,87,102
14	15116400	2	2		SN74S11J INTERGRATED CIRCUIT	Z90,100
15	50254900	3	3		SN74S20J INTERGRATED CIRCUIT	Z93,96,101
16	15127300	4	4		SN74S22J INTERGRATED CIRCUIT	Z43,49,54,60
17	50254800	3	3		SN74S40J INTERGRATED CIRCUIT	Z70,76,106
18	15117900	2	2		SN82S41 INTERGRATED CIRCUIT	Z99,105
19	15109700	1	1		SN74S74J INTERGRATED CIRCUIT	Z89

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CONTROL DATA — MEMORY ELECTRONICS BOARD COMPONENT ASSEMBLY OEM 16K x 36 BIT

CODE IDENT | SHEET 2 of 6 | PL | DOCUMENT NO. 82842600 | REV. 02

FIND NO.	PART IDENTIFICATION	QUANTITY REQUIRED 00	QUANTITY REQUIRED 01	UNIT OF MEAS	NOMENCLATURE OR DESCRIPTION	SPECIFICATIONS, NOTES, OR MATERIAL
20	17186100	8	8		SN74145J INTERGRATED CIRCUIT	Z117 - 124
21	15117400	7	7		SN74S157J INTERGRATED CIRCUIT	Z47,67,68,69 73,74,75
22	15138800	4	4		SN74S174J INTERGRATED CIRCUIT	Z71, 72, 77, 78
23	15113000	41	41		SN75452 INTERGRATED CIRCUIT	Z1-36, 108,112,113, 114,115
24	82801100	16	16		420-9031 TRANSISTOR QUAD TMI	QM1-16
25	82796700	2	2		610-9035 INDUCTOR TMI	L1,2
26	82796600	2	2		500-9084 TRANSFORMER TMI	T68,80
27	82801200	10	10		500-1031 TRANSFORMER TMI	T1,5,12,19,26,33,37, 44,51,58
28	82796500	38	38		500-1033 TRANSFORMER TMI	T2,6,9,13,16,20,23, 27,30,34,38,41,45,
						48,52,55,59,62,66, 67,69,70,72-79,
						81,88
29	82796400	38	38		500-1093 TRANSFORMER TMI	T3,4,7,8,10,11,14, 15,17,18,21,22,24,
						25,28,29,31,32,35, 36,39,40,42,43,46,
						47,49,50,53,54,56, 57,60,61,63,64,65,
						71
30	82830900	1	1		620-9029 DELAY LINE TMI	DL1
31	82788000	15	15		SN3467 TRANSISTOR	Q109-118,135,136, 137,128,138
32	82787900	119	119		2N3725 TRANSISTOR	Q1-108,122-127,129- 131,139,140
33	82808300	25	25		2N2369 TRANSISTOR	Q119,120,121,132, Q134,Q141-159

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CONTROL DATA	MEMORY ELECTRONICS BOARD COMPONENT ASSEMBLY OEM 16K x 36 BIT	CODE IDENT	SHEET 3 of 6	PL	DOCUMENT NO. 82842600	REV. 02

FIND NO.	PART IDENTIFICATION	QUANTITY REQUIRED										UNIT OF MEAS		NOMENCLATURE OR DESCRIPTION	SPECIFICATIONS, NOTES, OR MATERIAL
		00	01												
34	50240106	1	1											IN751A DIODE ZENER 5.1V	CR438
35	50240108	2	2											IN753A DIODE ZENER 6.2V	CR295-437
36	16797605	2	2											IN3826 DIODE ZENER 5.1V 1W	CR439,440
37	82788100	460	460											IN4607 NDP127P DIODE UNITRODE	CR1-294,296,436, 441-465
38	82797300	31	31											CAPACITOR 01uf 50V 20%	C7,23,24,27-44,68, 103-110,22
39	82799501	5	5											CAPACITOR 100pf 500V 2%	C10-C14
40	24504353	27	27											CAPACITOR 33uf 10V 20%	C1-5,8,9,18,50-60, 69-72,90-93
41	24504383	42	42											CAPACITOR 15uf, 20V 20%	C6,15-17,19,21,25,26 61-67,73-89,94-102
42	24500001	3	3											RESISTOR 2.7 Ω 1/4W 5%	R251,252,253
43	24500025	10	10											RESISTOR 27 Ω 1/4W 5%	R111,114,117,120 123,126,129,132,
															135,138
44	24500027	11	11											RESISTOR 33 Ω 1/4W 5%	R147,148,149,153, 154,246-250,258
45	24500029	36	36											RESISTOR 39 Ω 1/4W 5%	R1,4,7,10,13,16,19, 22,25,28,31,34,37,
															40,43,45,39,52,55, 58,61,64,67,70,73,
															76,79,82,85,88,91 94,97,100,103,106
46	24500033	12	12											RESISTOR 56 Ω 1/4W 5%	R181-184,189-196
47	24500035	2	2											RESISTOR 68 Ω 1/4W 5%	R185,186
48	24500039	7	7											RESISTOR 100 Ω 1/4W 5%	R141,207,208,209, 210, R262,268
49	24500045	1	1											RESISTOR 180 Ω 1/4W 5%	R146,R244
50	24500047	3	3											RESISTOR 220 Ω 1/4W 5%	R155,286,295

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CONTROL DATA	MEMORY ELECTRONICS BOARD COMPONENT ASSEMBLY OEM 16K x 36 BIT	CODE IDENT	SHEET 4 of 6	PL	DOCUMENT NO. 82842600	REV. 02

FIND NO.	PART IDENTIFICATION	QUANTITY REQUIRED 00	QUANTITY REQUIRED 01	UNIT OF MEAS	NOMENCLATURE OR DESCRIPTION	SPECIFICATIONS, NOTES, OR MATERIAL
51	24500051	16	16		RESISTOR 330 1/4W 5%	R109,112,115,118, 121,124,127,130,133,
						136,150,156,158,242, 289,293
52						
53	24500055	23	23		RESISTOR 470 1/4W 5%	R110,113,116,119, 122, 125,128,131,
						134,137,160,161, 165,168,170,243,
						269,270,277,280,282, 287,291
54	24500063	10	10		RESISTOR 1K 1/4W 5%	R139,140,144,162,290, 163,166,167,203-04
55	24500069	2	2		RESISTOR 1.8K 1/4W 5%	R143,R159
56	24500071	12	12		RESISTOR 2.2K 1/4W 5%	R145,151,152,157, 164,169,171,172,
						263-265,267
57	24500079	73			RESISTOR 4.7K 1/4W 5%	R2,3,4,6,8,9,11,12, 14,15,17,18,20,21,23,
						24,26,27,29,30,32,33, 35,36,38,39,41,42,
						44,45,47,48,50,51, 53,54,56,57,59,60,
						62,63,65,66,68,69, 71,72,74,75,77,78,
						80,81,83,84,86,87, 89,90,92,93,95,96,
						98,99,101,102,104, 105,107,108,142
58						
59	24500083	1	1		RESISTOR 6.8K 1/4W 5%	R281
60	24500139	2	2		RESISTOR 100 1/2W 5%	R146, R294
61	24500147	2	2		RESISTOR 220 1/2W 5%	R179,180

CONTROL DATA	MEMORY ELECTRONICS BOARD COMPONENT ASSEMBLY OEM 16K x 36 BIT	CODE IDENT	SHEET 5 of 6	PL	DOCUMENT NO. 82842600	REV. 02

FIND NO.	PART IDENTIFICATION	QUANTITY REQUIRED 00	01	UNIT OF MEAS	NOMENCLATURE OR DESCRIPTION	SPECIFICATIONS, NOTES, OR MATERIAL
62	24500150	2	2		RESISTOR 300 1/2W 5%	R205,206
63	24500159	2	2		RESISTOR 680 1/2W 5%	R241,245
64	24500163	1	1		RESISTOR 1K 1/2W 5%	R255
65	24500165	1	1		RESISTOR 1.2K 1/2W 5%	R254
66	24500171	4	4		RESISTOR 2.2K 1/2W 5%	R177,178,187,188
67	68583315	2	2		RESISTOR 39.2 1/8W 1%	R201,202
68	68583384	2	2		RESISTOR 46.4 1/8W 1%	R259,260
69	68583329	1	1		RESISTOR 150 1/8W 1%	R261
70	68583344	1	1		RESISTOR 562 1/8W 1%	R285
71	68583352	3	3		RESISTOR 1.21K 1/8W 1%	R278,288,292
72	68583358	1	1		RESISTOR 2.21K 1/8W 1%	R283
73	82831003	1	1		RESISTOR 3 3W 1%	R256
74	82831021	1	1		RESISTOR 12 3W 1%	R257
75	82831019	6	6		RESISTOR 38 5W 3%	R271-276
76	82799400	1	1		POTENTIOMETER 500	R266
77	24500133	4	4		RESISTOR 56 1/2W 5%	R197,198,199,200
78	91938428	-	15		RESISTOR MODULE 470	RM-1,3,4,7,9,11,13, 15,17,19,21,23,25,
						27,29
79	91938426	-	15		RESISTOR MODULE 390	RM-2,4,6,8,10,12, 14,16,18,20,22,24,
						26,28,30

CONTROL DATA	MEMORY ELECTRONICS BOARD COMPONENT ASSEMBLY OEM 16K x 36 BIT	CODE IDENT	SHEET 6 of 6	PL	DOCUMENT NO. 82842600	REV. 02

FIND NO.	PART IDENTIFICATION	QUANTITY REQUIRED 00	01	UNIT OF MEAS		NOMENCLATURE OR DESCRIPTION	SPECIFICATIONS, NOTES, OR MATERIAL
80	23235200	25	25			TRANSISTOR PAD TO-18	
81	82815600	134	134			TRANSISTOR PAD TO-5	
82	91921200	8	8			CIRCUIT JUMPER	JM-1-8
83	82800700	1	1			THERMISTER 100 25°C	RT-1
84	91931601	1	1			SWITCH 4 POSITION	SW-1
85	91931701	1	1			COVER	FOR SW-1
86	82813401	2	2			RECEPTACLE MODD II "AMP INC" 85865-2LP	TP-1, TP-2
87		2	2			2-RESISTORS 1/4W 5% TO BE DETERMINED IN TEST	R179, R184

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CONTROL DATA	CORE ARRAY BOARD COMPONENT ASSEMBLY OEM 16K X 36	CODE IDENT	SHEET 1 of 2	PL	DOCUMENT NO. 82791402	REV.

FIND NO.	PART IDENTIFICATION	QUANTITY REQUIRED										UNIT OF MEAS		NOMENCLATURE OR DESCRIPTION	SPECIFICATIONS, NOTES, OR MATERIAL
1	82792200	1												PCB DETAIL	
2	24500063	36												RESISTOR 1.0K 1/4W 5%	R1-36
3	82797200	36												CAPACITOR 100Pf 100V 10%	C1,2,4-6,8-10,12-14, 16-18,20-22,24,25
															27-29,31-33,35-37, 39-41,43-45,47,48,
4	82797300	48												CAPACITOR 01uF 50V 20%	C3,7,11,15,19,23,26, 30,34,38,42,46,49-84
5	82780802	36												DIODE MODULES	DM1-36
6	82796300	32												RESISTOR MODULES 330Ω	RM5-28,31-38
7	82780700	14												RESISTOR MODULES 470Ω	RM1-4,29,30,39-46
8	82788100	144												DIODE IN4607	CR1-144
9	82834300	36												RECEPTACLE	
10	82797000	9												HEADER, STRAIGHT 1-28 BERG 65274-3	
12	82813400	56												RECEPTACLE MODD II AMPING 85861-2LP	
16	82795500	REF												CORE ARRAY TEST SPEC	
19	15127500	36												SN7520 INTEGRATED CIRCUIT	Z1-Z36
20	82800900	36												RESISTOR NETWORK	RM54-89
22	82795400	1												SUBSTRATE	
23	82795200	1												CORE COVER	
24	82795300	REF												WIRING DIAGRAM	
25	91965100	REF												SCHEMATIC	
27	24524418	-												MAG WIRE	

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CONTROL DATA	CORE ARRAY BOARD COMPONENT ASSEMBLY OEM 16K X 36	CODE IDENT	SHEET 2 OF 2	PL	DOCUMENT NO. 82791402	REV.

FIND NO.	PART IDENTIFICATION	QUANTITY REQUIRED	UNIT OF MEAS		NOMENCLATURE OR DESCRIPTION	SPECIFICATIONS, NOTES, OR MATERIAL
28	82822400	589,824			CORE 750-18MTA	
29	24524420	-			MAG WIRE	
30	24524441	-			MAG WIRE	
31	24524417	-			MAG WIRE	
32	18440206	-			ADHESIVE	
33	82785000	-			WAX F-145	
35	82834400	10			SCREW NYLON	
36	82834200	59			TERMINAL	
37	82807200	14			STAND OFF	
38	82807300	12			STAND OFF .125LG	

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ALPHABETICAL LISTING OF MEMORY MODULE MNEMONICS A

Mnemonic	Description
AD00-17	Address inputs 00 through 17
B0-B3	Byte inputs 0 through 3
B Hold	Byte hold
BCT	Byte control timing
CI	Cycle initiate
CLR 0-3	Clear 0 through 3
CPM	Clock pulses for memory
DA	Data available
DI 00-36	Data in 00 through 36
DIT	Data in timing
DO 00-36	Data out 00 through 36
DOT	Data out timing
DOS 0-3	Data out strobe
DS	Data save
EC	End of cycle
ER	End of read
INH 1-4	Inhibit timing 1 through 4
INHR	Inhibit rise time
LDT	Late data in timing
MA00-17	Memory address 00 through 17
MB	Memory busy
MB 0-3	Memory byte 0 through 3
MRMW	Memory read modify write
MWW	Memory word write
QT 1-24	Q clock timing 1 through 24
RCLR	Read clear
RMW	Read modify write
RST	Read start time
SAS 0-3	Sense amplifier strobe 0 through 3
VTH	Voltage threshold
WCLR	Write clear
WDT	Write data timing
WE 0-3	Write enable 0 through 3
WI	Write initiate
WINH	Write inhibit
WST	Write start time
WW	Word write
XRC	X read current
XRDT	X read timing
XWC	X write current
XSKT	X sink timing
YRC	Y read current
YRDT	Y read timing
YWC	Y write current
YSKT	Y sink timing

INTERFACE CONNECTOR CHART

Connector J46				Connector J47			
Pin No.	Signal	Pin No.	Signal	Pin No.	Signal	Pin No.	Signal
1	+5	41	0V	1	+15	41	0V
2	+5V	42	0V	2	+15V	42	0V
3	+5	43	DI25	3	0V	43	D006
4	+5	44	D025	4	0V	44	DI06
5	$\overline{\text{Reset}}$	45	$\overline{\text{WI}}$	5	AD05	45	DI11
6	$\overline{\text{LDT}}$	46	$\overline{\text{CI}}$	6	AD09	46	D011
7	-15V	47	DI22	7	AD10	47	0V
8	-15V	48	D022	8	AD06	48	0V
9	+15	49	0V	9	AD11	49	DI10
10	+15	50	0V	10	AD08	50	D010
11†		51	DI23	11	AD07	51	DI13
12†		52	D023	12	AD04	52	D013
13	D026	53	DI20	13	AD02	53	0V
14	DI26	54	D020	14	AD01	54	0V
15	D035	55	D018	15	AD03	55	DI12
16	DI35	56	DI18	16	AD00	56	D012
17	0V	57	D019	17	$\overline{\text{CD0}}$	57	D014
18	0V	58	DI19	18	$\overline{\text{ER}}$	58	16K/32K††
19	DI34	59	DI24	19	0V	59	DI14
20	D034	60	D024	20	0V	60	0V
21	D033	61	DI21	21	DI00	61	D015
22	DI33	62	D021	22	D000	62	DI15
23	0V	63	$\overline{\text{EC}}$	23	DI01	63	D016
24	0V	64	$\overline{\text{DA}}$	24	D001	64	DI16
25	D032	65	$\overline{\text{B0}}$	25	D002	65	0V
26	DI32	66	$\overline{\text{MB}}$	26	DI02	66	0V
27	D030	67	AD16	27	D007	67	D017
28	DI30	68	$\overline{\text{B2}}$	28	DI07	68	DI17
29	0V	69	AD12	29	DI09	69	Spare
30	0V	70	$\overline{\text{WW}}$	30	D009	70	Spare
31	DI31	71	AD13	31	DI03	71	+15V
32	D031	72	AD15	32	D003	72	+15V
33	D029	73	$\overline{\text{B1}}$	33	DI05	73	-15V
34	DI29	74	AD14	34	D005	74	-15V
35	0V	75	AD17	35	0V	75	$\overline{\text{Data Save}}$
36	0V	76	$\overline{\text{B3}}$	36	0V	76	Spare
37	D028	77	BCT†††	37	DI04	77	+5V
38	DI28	78	$\overline{\text{RMW}}$	38	D004	78	+5V
39	D027	79	-15	39	DI08	79	+5V
40	DI27	80	-15	40	D008	80	+5

† Used if external current control desired.
†† Pin is open for 16K by 36 bit operation, wired to ground for 32K by 18 bit operation.
††† Pin is open for BCT at WI time in RMW mode, wired to ground for BWT at t_0 in RMW mode. Refer to byte control timing in text.

COMMENT SHEET

MANUAL TITLE CDC 94200 Core Memory

Technical Manual

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