CONTROL DATA 606 MAGNETIC TAPE TRANSPORT

OEM REFERENCE MANUAL

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CONTROL DATA
606

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PREFACE

The Control Data 606 Magnetic Tape Transport is a high speed input/output unit specifically designed to provide the high performance storage capabilities required by Control Data computers and data processing systems. Although the information contained in this manual is based on the 606 transport, the discussion is generally applicable to all 600 Series Magnetic Tape Transports.

Information is stored in the 606 on magnetic tape in the form of magnetized spots or bits. Magnetic tape is used as the record media because modern data processing systems require extensive files of input data which can be permanently recorded on magnetic tape. The files, once stored on tape, can be used over and over as input information, thus eliminating the costly process of re-entering new input data. Although information recorded on tape is permanent, it may be erased and replaced by new information, when desired.

The 606 may be used with computers in an on-line capacity, or with external equipment in an off-line processing system. When used on-line, for example, the operation of the 606 may be externally controlled by the Control Data 160-A, 1604-A, 3600 or other computers. In an off-line system, the 606 is under manual (local) control and is used with other peripheral equipment such as the Control Data 1612 Line Printer, 167 Card Reader, etc. In both cases, the tape transport may function both as an input and output device. The transport, in other words, accepts and stores information from the computer or peripheral equipment and/or sends data to the computer or peripheral equipment.

Transfer of data and the exchange of control information from computers or off-line equipment to magnetic tape is via a separate external control unit. The control unit provides the timing information necessary to buffer and control the flow of information into and out of the tape transport.

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Description

The Control Data 606 Magnetic Tape Transport includes the operational features and logic found to be most desirable for efficient system operation. These advantages are being fully utilized in Control Data computer systems and can also be used in systems supplied by original equipment manufacturers.

PHYSICAL DESCRIPTION

The location of major components in the 606 tape unit is shown in figure 1-1. The tape unit is 72 inches high, 33 inches deep, 28 inches wide and weighs 800 pounds. Detailed specifications are given in table 1-1.

Each tape unit includes self-contained read/write electronics, control logic and power supplies. Because the use of shared components has been eliminated, each 606 operates independently of other units in the system. In multiple unit installations, for example, certain searching and positioning operations may be done simultaneously by two or more units. Any 606 may be removed from the line for testing and maintenance without affecting the operation of the remaining units.

A bank of switches and indicators on the front control panel allows the operator to monitor and manually control tape operations. A bank of switches and indicators on the rear maintenance panel provides complete operator control during test procedures.

The logic control section, mounted at the rear of the cabinet on a hinged chassis, controls the operation of the 606. The logic section consists of a number of circuits mounted on separate pluggable printed circuit cards. The circuits are similar in construction to those used in Control Data computers.

Power input to the 606 is provided by any standard 208 vac, three phase, 15 amp service line. All internal a-c and d-c voltages are developed and distributed by the power supply unit located at the lower rear of the cabinet.

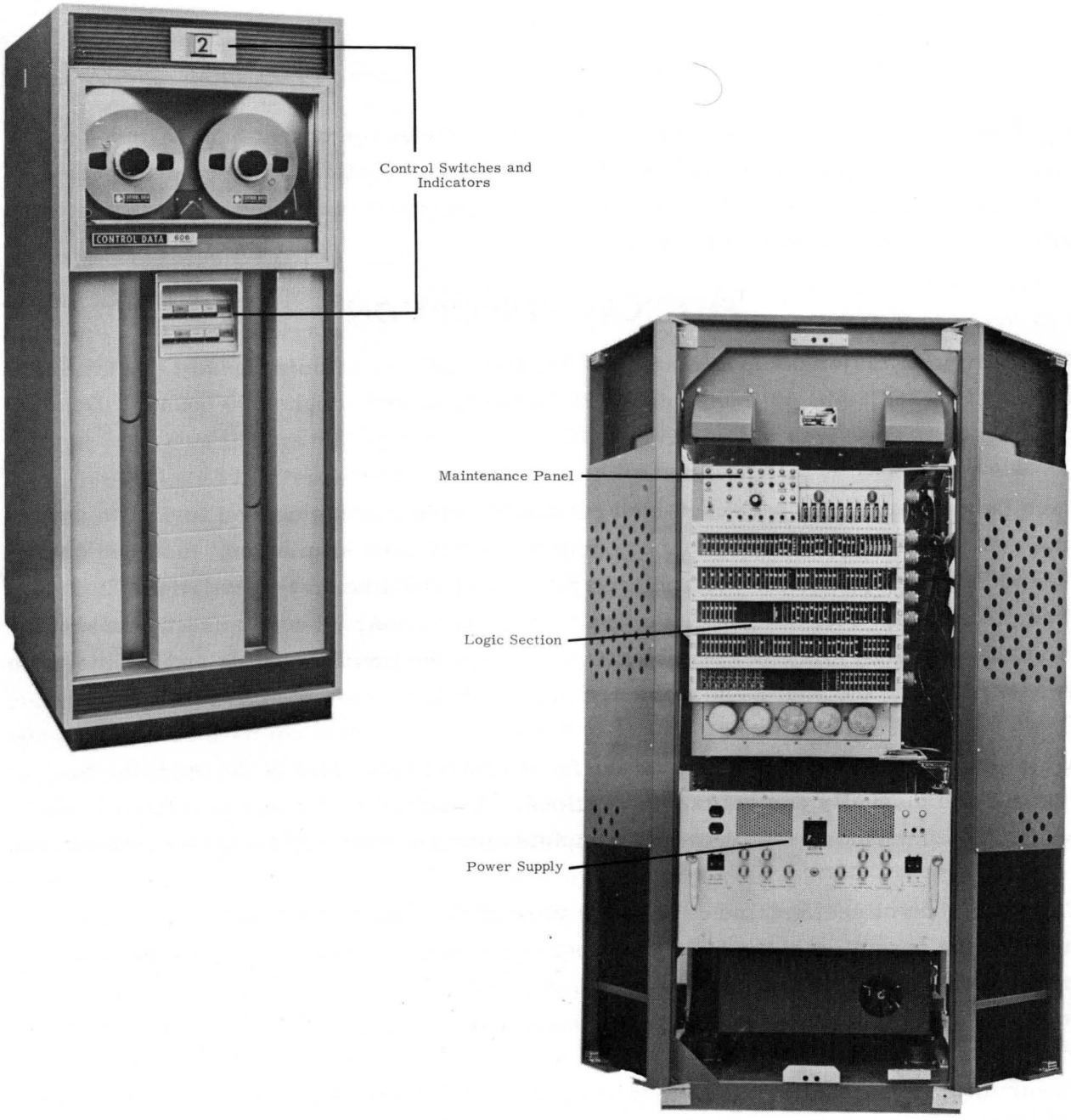


Figure 1-1. Tape Transport, Front and Rear View

FUNCTIONAL DESCRIPTION

TAPE FORMAT

Magnetic tape provides a high speed, non-volatile storage medium for recording and retaining information. The tape has a plastic base and is coated on one side with a magnetic oxide. The coating consists of minute particles of iron oxide mixed with a binding agent. It is upon this coating that information is recorded. Extreme care is taken in the manufacture of the tape in order to eliminate any imperfection that could cause errors. Each roll of Control Data magnetic tape is therefore thoroughly tested before being used to guarantee its recording characteristics and performance.

Information is read (detected) or written (stored) by passing the oxide side of the tape over read/write heads. Information may be written on any of seven independent tracks on the tape. During a read or write operation, seven recording heads are placed vertically across the tape; therefore 7 bits may be simultaneously recorded, 1 bit on each track.

A seven track non-return-to-zero (change-on-ones) recording scheme is used. In this system, magnetic particles on the tape are aligned in either the positive or negative direction. A binary "1" is recorded by reversing the alignment (polarity); no polarity reversal results in a "0". Thus, each track of the tape is fully magnetized and the polarity is reversed as each "1" bit is recorded.

A line (or frame) of tape data consists of a 6-bit character and a parity (check) bit. Tracks 0 through 5 specify the character while track 6 holds the parity bit (figure 1-2).

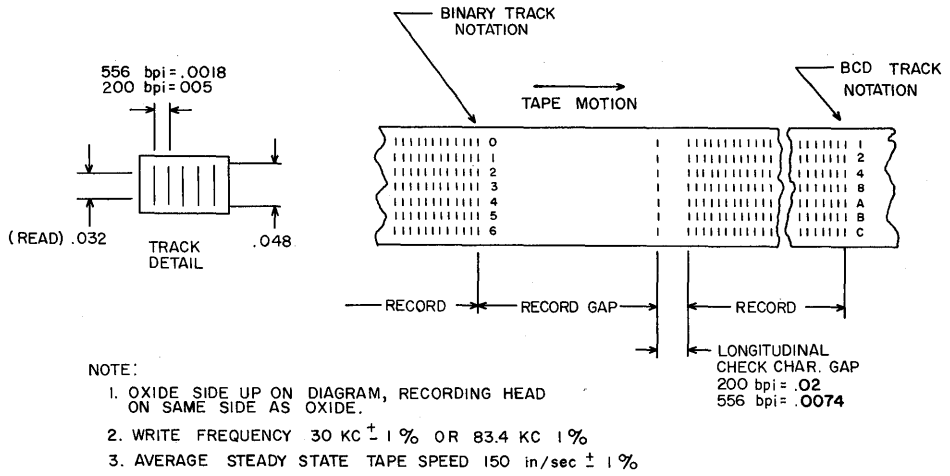


Figure 1-2. Bit Assignments on Tape

When used in Control Data systems, data is recorded in one of two formats: binary or binary coded decimal (BCD). Tape is binary if data is recorded just as it is represented in core storage. In BCD format, digits, characters and special symbols are represented in core storage by 6-bit binary numbers. The BCD codes are listed in table 1-2.

The formats also differ in the selection of parity bits. The parity bit in binary format is chosen so that the total number of "1" bits in any line is odd. In coded format the total number of "1" bits must be even. The format is selected by the control unit which also designates the correct parity bit that accompanies each character.

Recorded data on the tape is arranged in groups called records and files. A minimum of one line of information constitutes a record. Adjacent records are separated by a 3/4 inch unrecorded area (record gap). A longitudinal parity bit is recorded in coded format at the end of each record; the number of "1's" in each record track is made even.

A file consists of a group of records. Adjacent files are separated by recording an end of file mark six inches from the last record in the file. The file mark consists of an octal 17 (BCD) and its check character (also an octal 17).

REFLECTIVE SPOTS

Reflective spots are placed on the tape to enable sensing of the beginning and end of the useable portion of the magnetic tape. The markers also provide compatibility with other magnetic tape equipment. The reflective spots are plastic, 1 inch long by 3/16 inch wide, coated on one side with adhesive strips and on the other with vaporized aluminum. They are placed on the base or uncoated side of the tape and detected by photo-sensing circuits.

The load point marker must be placed at least 10 feet from the beginning of the tape on the supply reel (figure 1-3). This marker is placed with its 1-inch dimension parallel to, and not more than 1/32 inch from, the edge of the tape nearest the operator when the file reel is mounted.

The end of tape marker should be placed not less than 18 feet from the end of the tape attached to the take-up reel hub. This space includes approximately 10 feet of tape trailer and enough tape to hold a record of 20, 000 characters after the end of tape

marker is sensed. The marker is placed with its 1-inch dimension parallel to, and not more than 1/32 inch from, the edge of the tape nearest the tape unit (when reel is mounted).

Markers are applied while the reel is removed from the tape unit and must be properly aligned and firmly attached to the tape. Use care to avoid dust accumulating on the tape while attaching markers.

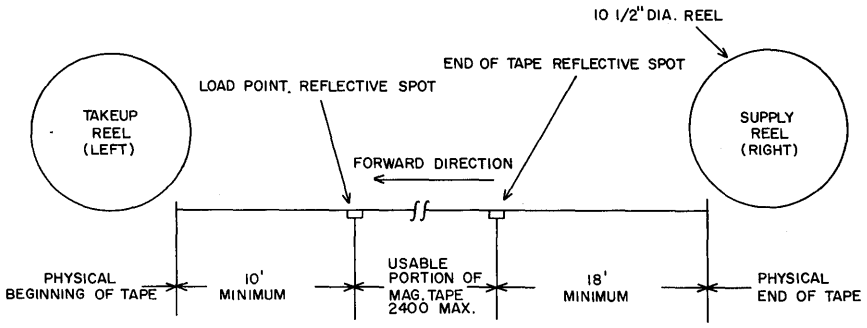


Figure 1-3. Physical Layout of Tape

FILE PROTECTION RINGS

The back of the file reel has a slot near the hub which accepts a plastic file protection ring (figure 1-4). Writing on a tape is possible only when the reel contains this file protection ring. The tape may be read with or without the ring. Presence of a ring on a reel of tape is signaled by the overhead lights which turn on immediately after the tape load procedure is executed. The lights remain on until the ring is removed or the tape unit is placed in the unload status. The ring should be removed from the file reel after writing is completed to avoid loss of valuable records through accidental rewriting.

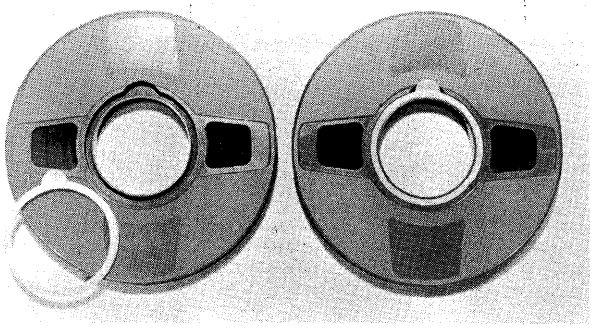


Figure 1-4. File Protection Ring

PRINCIPLES OF OPERATION

Tape Motion

During a read or write operation, tape is moved from the supply reel, past the read/write heads, to the take-up reel (figure 1-5). Tape motion is provided by two fluted capstans which rotate continuously in opposite directions. Tape is drawn against the drive capstan by vacuum and floated over the non-driving capstan by air pressure. If the tape is moving from the supply reel to the take-up reel (forward motion), the left capstan drives the tape. If tape motion is in the opposite (reverse) direction, the right capstan provides the drive.

Tape motion is quickly and smoothly stopped by means of a pneumatic brake port. Tape is drawn to and firmly held against the brake port by means of vacuum. Because pressure is applied to both capstans during this period, neither capstan contacts (drives) the tape.

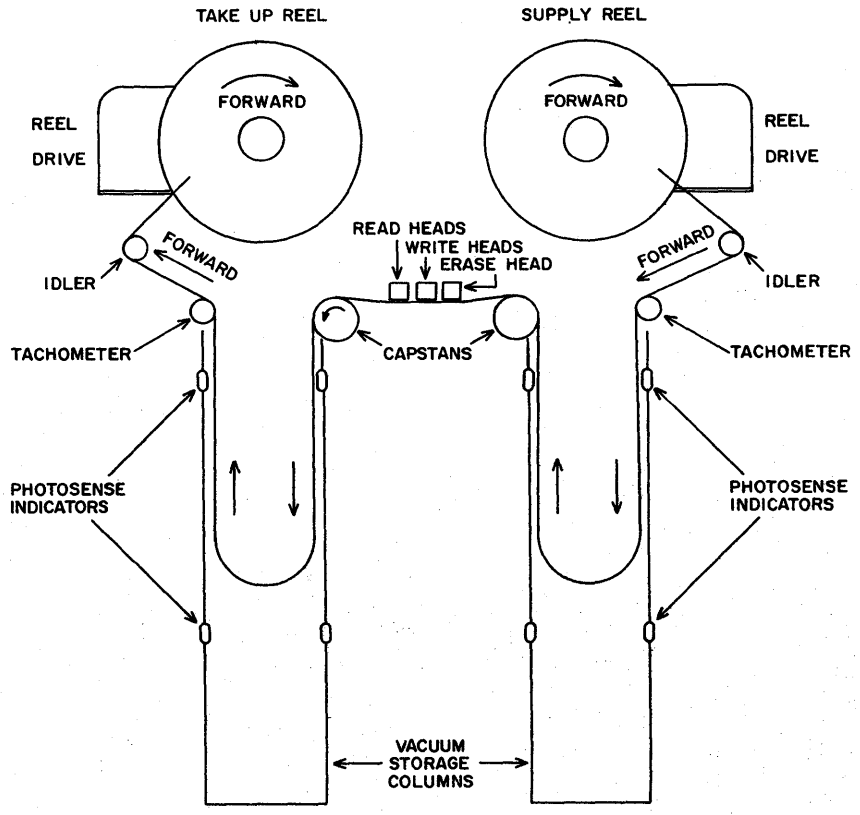


Figure 1-5. Tape Path Through 606 Tape Unit

Read/Write Heads

The head assembly consists of individual read and write heads, an erase head, tape cleaners and pneumatic pad. Each of the seven read/write heads used in the 606 tape transport has two magnetic gaps. One gap is used for writing; the other, for reading. The gaps are arranged so that during a write operation, the tape first passes under the write gap to record the data and then under the read gap to check the writing. This allows each line of information to be examined and verified immediately after it is written on the tape. Thus, if any discrepancy occurs during the write operation, it is immediately detected at the read head.

The tape cleaners and erase head clean the tape prior to a read or write operation. The broad band erase head removes any information recorded on the tape before new information is recorded by the write heads. The two tape cleaners, located on either side of the heads, pneumatically remove foreign particles on the tape surface during a read or write operation.

A pneumatic pad maintains precise contact pressure between the tape and the head gaps. This contact pressure is provided by means of air pressure which minimizes head and tape wear by blowing the tape against the heads.

Vacuum Buffer Columns

The 606 can accelerate tape to high speed within 3 ms. Conversely, tape motion is completely stopped within 3 ms. The 606 uses tape loops to reduce to a minimum the tape mass that must be accelerated during the 3 ms period. These loops separate the heavy tape reels from the portion of tape under the heads.

The two tape loops form tape reservoirs for the capstan drive system. During the first few milliseconds of acceleration, the actuated capstan pulls tape from one loop and places it in the second loop. As tape is drawn from one column, it is replaced from the reel above it. As tape is fed into the opposite column, the associated reel takes up the slack. The heavy tape reels are therefore given more time to accelerate and act to increase or reduce the amount of tape in the vacuum columns. In other words, tape loops buffer the heavy reels out of the high acceleration capstan drive system. This minimizes the inertia in the high acceleration system as the capstans need only accelerate the mass of a few feet of tape.

The vacuum columns also maintain tension throughout the system. Each loop fits snugly into a chamber and divides the chamber into two parts. The bottom portion of the column is under reduced pressure. The upper part is at atmospheric pressure and pushes the loop down, providing a small amount of tension on the loop.

Reel Drive and Servo Control

The reel drive controls the length of the tape loops in the vacuum columns. A servo-system between each loop and tape drive positions the tape reels by responding to signals from the vacuum column photosense indicators. If the tape loop in a column is too long, the photosense indicators signal the reel drive to take up tape. If the loop is too short, the indicators signal the reel drive to deliver tape.

TABLE 1-1. DETAILED SPECIFICATIONS

RECORDING FORMAT	Method	NRZI (non-return-to-zero - change-on-ones)
	Seven Track Recording	Data 6 bits, parity 1 bit, self clocking
	Inter-Record Gap	3/4 inch
	Tape Markers	End of tape and load point reflective spot
	Recording Density	High - 556 frames per inch Low - 200 frames per inch
	Compatibility	Compatible with IBM 727 and 729 I, II, III and IV Tape Units
TAPE SPEED	Read/Write	150 inches per second ± 1%
	Reverse Search	150 inches per second ± 1%
	Rewind and Unload	Over 320 inches per second average
	Start Time	3 ms
	Stop Time	2 ms
	Start Distance	0.225 inch ± 30%
	Stop Distance	0.225 inch ± 30%
CHARACTER RATE	High Density	83,400 lines per second
	Low Density	30,000 lines per second
TAPE	Width	1/2 inch
	Length	2400 feet with 1 1/2 mil base Mylar tape
	Reels	10 1/2 inch IBM hub with file protect ring
TAPE MECHANISM	Reel Drive	Individual DC shunt torque motors, digital control by reservoir sensors
	Reel Brakes	Electro-magnetic, mounted on drive motor shaft
	Tape Reservoir	Two 43 inch vacuum columns
	Reservoir Sensors	Photo electric, silicon solar cells for reel drive control; vacuum switches for fault sensing
	Tape Drive	Vacuum capstans, individually synchronous motor driven; voice coil pneumatic valves
	Tape Brake	Vacuum - voice coil pneumatic valve actuated
	Tape Guides	Full channel guiding throughout tape reservoirs and capstan drives
HEADS - PHYSICAL	Spacing (forward direction)	Forward Cleaner - vacuum controlled Erase Head - solid broad band DC (Erase gap to write gap: 7/16 inch)

TABLE 1-1. CONTINUED

HEADS - PHYSICAL	Spacing (forward direction)	Write Head - laminated 7 channel flat metal head (Write gap to read gap: 0.300 inch)	
		Read Head - laminated 7 channel flat metal head	
		Reverse Cleaner - vacuum controlled	
	Write Gap	0.00100 inch	
	Read Gap	0.00025 inch	
	Write Gap Width	0.048 inch (each track)	
	Read Gap Width	0.030 inch (each track)	
	Erase Gap Width	9/16 inch (full tape width)	
	Contact Recording	Maintained by jets of air on opposite side of tape	
	Head Gap Alignment	Mechanical gap parallel within 100 micro-inches	
	Static Skew	Over-all correction by mechanical adjustment of read/write head mounting - detail correction by adjustable electronic delays on each read channel and each write channel	
	Dynamic Skew	± 1 usec at first register input	
	Write Current	70 ma ± 10%	
	Read Voltage	25 mv approximately, dual level sensing for write verify	
OPERATION	Tape Loading Time	15 seconds to load point	
	Tape Unloading Time	5 seconds from load point	
	Tape Leaders	No machine leaders	
	Searching	Upon command, search forward or reverse to next end of record or file mark and stop without external monitoring	
FRONT CONTROL PANEL	Operator Controls With Indicators	Power	High-Low Density
		Forward	Ready
		Reverse	Clear/Fault
		Unload	Unit Number Selector
		Load Point	
	Operation Indicators Only	Read	Unit Select Status (2)
		Write	File Protect
PHYSICAL	Size and Weight	Height - 72 inches	Width - 28 inches
		Depth - 33 inches	1200 pounds

TABLE 1-1. CONTINUED

PHYSICAL	Construction	Steel frame on casters with removable front and side panels and hinged rear doors
	Environment	60° to 90° F, humidity 10° above dew point, dust free (typical computer room environment)
	Heat Dissipation	Unloaded Status - 100 BTU per hour Loaded/Ready - 6500 BTU per hour Operation - 8500 BTU per hour
ELECTRICAL	Power Source	208v ± 10%, 60 cycle, three phase, 15 amp circuit. Average load at 208v; Unloaded - 1 amp Loaded/Ready - 8 amps Operation - 11 amps
	Power Connector	One male connector (5 pole, 20 amp, Hubble Twistlock #3521) on short cord for connection inside back doors of cabinet to either a conduit post mounted receptacle or extension cord type female connector
	Pole Assignments	X - phase 1 Y - phase 2 Z - phase 3 N - Neutral Grd - chassis ground
	Input/Output	All input and output signals are digital as represented by nominal - 16v and 0v voltage levels. Signal voltages are presented and received on separate input and output circuit cards
	I/O Cards	Switching time of 606 input/output cards is: 1/2 - 1 usec, data & strobe; 2-4 usec, commands Logical "1": 0v or grd; ± 1/2v Logical "0": -16v; +2v, -4v 606 input load: 10 ma max. 606 output load: 75 ma max., 2000 uuf max. (50')
	I/O Lines	Refer to figure 3-2 and table 3-1 in the Logic Description for a listing of the 606 input/output lines. As listed therein: All signals and statements made exist or happen when a logical "1" appears on the line. All signals represent steady state (flip-flop) inputs or outputs except where noted as a pulse. Pulse signals are 4 usec duration.

TABLE 1-1. CONTINUED

ELECTRICAL — I/O Connectors

Two female plug connectors (Amphenol, Minni E, 24 pin, #67-02E18-24S) are provided on the side of the logic chassis for input and output. The pin assignments on the output connector (computer output - 606 input) and input connector (computer input - 606 output) are as follows:

Output Connector Connector #J208		Input Connector Connector #J209	
Pin	Service	Pin	Service
A	2^0 Write	A	2^0 Read
B	2^1 Write	B	2^1 Read
C	2^2 Write	C	2^2 Read
D	2^3 Write	D	2^3 Read
E	2^4 Write	E	2^4 Read
F	2^5 Write	F	2^5 Read
H	Parity Write	H	Parity Read
J	Write Sprocket	J	Read Sprocket
K	Address 6	K	Write Ready
L	Address 7	L	Address 4
M	Forward	M	End of Record
N	Reverse	N	File Mark
P	Stop on File Mark	P	Address 0
R	Select Hi Density	R	Address 1
S	Select Lo Density	S	Address 2
T	Write Select	T	Address 3
U	Read Start	U	Busy
V	Master Clear	V	Hi Density Selected
W	Rewind Unload	W	Load Point
X	Rewind	X	End of Tape
Y	Address 5	Y	Ready
Z	Unit Select Light #1	Z	
a	Unit Select Light #2	a	
b	Ground	b	Ground

2

Operation

This chapter contains information necessary to prepare the 606 tape unit for operation under external or manual control after all power and control cables have been connected.

GENERAL OPERATING INSTRUCTION

APPLICATION OF POWER

To initially energize the tape unit:

1) Open doors at back of cabinet.

2) Push the two line circuit breakers (on power supply) to the up position. If the neon indicator fails to light, notify maintenance.

3) Push the two reel power circuit breakers (on power supply) to the up position.

4) Hold the Power On switch on the maintenance panel in the up position for about two seconds. If the pump motor fails to start, notify maintenance.

5) The Power indicator on the front panel should turn on. If not, repeat the procedure (notify maintenance if the indicator does not light).

6) Close the back doors.

The Power key on the front control panel is used only to remove power from the unit. Once this key is pushed, the above procedure must be repeated in order to apply power to the unit.

TAPE LOAD PROCEDURE

1) Slide front door down to lowest position (figure 2-1).

2) Check that supply reel has been file protected as necessary.

3) Mount reel on supply reel hub and tighten hub knob. Caution: For proper alignment, push reel firmly against hub stop before tightening knob.

4) Make sure that tape load arms are in up position.

5) Pull sufficient tape from supply reel to reach take-up reel. Thread tape on the outside of the supply tape load arm, over the head assembly, around the outside of the take-up load arm and over the top of the take-up reel. Release tape and spin the take-up reel hub two or three times.

6) Slide tape under head assembly.

7) Snap tape load arms down.

8) Set Unit Selection switch to one of ten positions (0-7 or standby) to assign a logical program selection number.

9) Press Clear switch.

10) Press Load Point switch. Tape will drop in columns, move forward, and stop on load point marker. The Load Point light will turn on. (If the light does not turn on, notify maintenance.) If tape continues moving forward for more than 3 or 4 seconds, it indicates either no load point marker was placed on the tape or the operator manually wound the marker onto the take-up reel during step 5.

11) If the unit is to be externally controlled, press the Ready switch. If it is to be manually operated and the Ready switch has been pushed, press the Clear switch.

12) Push up door.

If the supply reel contains a file protection ring, the overhead lights should be on, indicating that a write operation may be performed. If the lights are not on, notify maintenance.

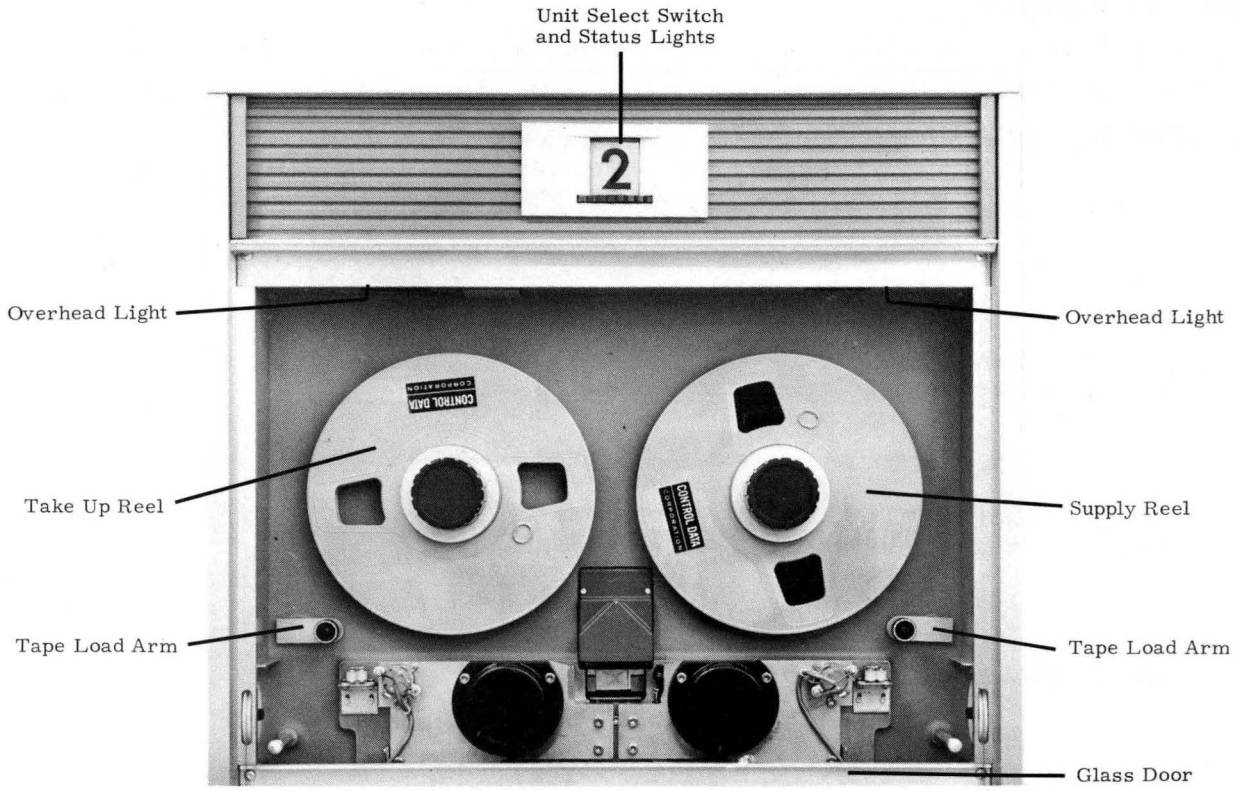


Figure 2-1. Tape Load and Unload Mechanics

TAPE UNLOAD PROCEDURE

1) Press Clear switch.

2) Press Unload switch. All tape will automatically be drawn from the take-up reel and wound on the supply reel. The Unload indicator will light.

3) Slide down front door.

4) Loosen supply reel hub knob and remove supply reel.

5) Check if reel needs to be file protected and if it is labeled adequately prior to storage.

MANUAL OPERATION

The manual controls and indicators for operating each tape unit are mounted on a panel located below the front door of the unit (figure 2-2). The functions of the controls are described in table 2-1.

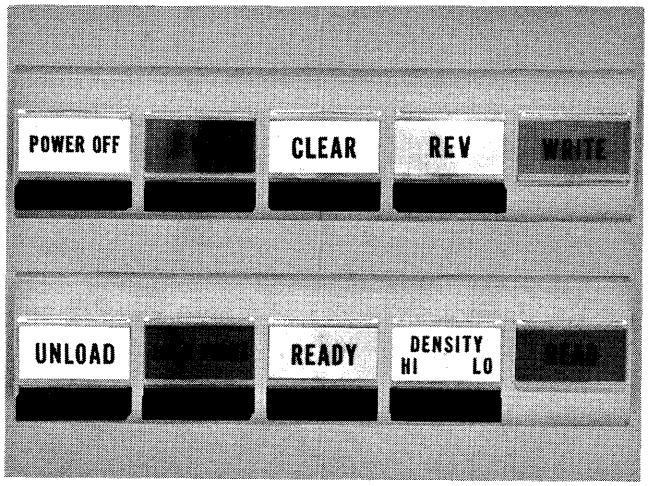


Figure 2-2. Operator Control Panel

TABLE 2-1. MANUAL CONTROLS AND INDICATORS

NAME		FUNCTION
POWER	S*	Removes power from all components and power supplies.
	I**	Power is available to components and power supplies.
FWD	S	Moves tape forward at 150 ips. Motion stops when end of tape marker is sensed.
	I	Tape is moving forward at 150 ips.
CLEAR	S	Master clears all previous settings and conditions. Stops (immediately) tape motion. New manual selections are necessary to reselect tape unit and/or operation required.
	I	606 is cleared.

TABLE 2-1. MANUAL CONTROLS AND INDICATORS (CONT'D)

NAME		FUNCTION
REV	S	Rewinds tape at 320 ips. Motion stops when load point marker is sensed.
	I	Tape is moving in reverse direction at 150 or 320 ips.
WRITE	I	Write operation is in progress
UNLOAD	S	Moves tape at 320 ips to unload position (all tape on supply reel). Tape Load procedure must be performed to resume operation.
	I	Tape is in unload status.
LOAD POINT	S	Moves tape forward at 150 ips to load point marker. Motion stops when marker is sensed.
	I	Tape is at load point marker.
READY	S	Places 606 under external control. Unit is placed under manual control only when master cleared.
	I	Unit is under external control.
DENSITY	S	Changes density mode selection.
	I (Hi) I (Low)	High density mode selected. Low density mode selected.
READ	I	Read operation is in progress (not on when reading for horizontal checking during write operation).
UNIT SELECTION	S	10-position switch; 0-7 provide input designation while two standby positions disconnect unit from external control.
	I (White) I (Red)	Unit Select Light #1. Unit Select Light #2.
OVERHEAD LIGHTS	I	File protection ring is on reel (unit can write) and tape unit is not in the unload position.

* Switch
** Indicator

SPECIAL INSTRUCTIONS

In order to simulate an unload condition without removing all tape from the take-up reel, simultaneously press the Clear and Unload switches (Clear switch must be released first). The unload condition will be simulated but tape will not move. In order to place the unit in operational status, remove all tape from the vacuum columns by revolving the take-up reel clockwise and the supply reel counterclockwise. Snap the tape load arms down and press the Load Point switch. The tape will move forward and stop on the nearest load point marker. The Load Point indicator will be turned on.

If all tape is unwound from the supply reel:

1) Snap tape load arms up, if necessary.
2) Guide tape around the tape load arms, over the head assembly, and wrap approximately ten turns around the supply reel.
3) Slide tape under head assembly.
4) Press the Load Point switch.
5) As soon as the Forward light turns on, press the Clear switch and then the Reverse switch. Tape will rewind on the nearest load point marker.

The following information is applicable when a number of load point or end of tape markers are used on a single tape.

To move forward from a reflective marker and stop at nearest end of tape marker, press the Forward switch.

To move forward off a reflective marker and stop at nearest load point or end of tape marker, press the Forward and then the Load Point switches. Load Point indicator will light if motion stops at load point marker.

To reverse from a reflective marker and stop at nearest load point marker, press the Unload, Clear, and Reverse switches in that order.

Tape motion may be stopped at any time by pressing the Clear switch. An unload operation may be performed by pressing the Unload switch.

3

Interface Considerations

INTRODUCTION

The Control Data 606 Magnetic Tape Transport is designed to provide straightforward electrical interconnections to other system equipment. Each 606 contains sufficient electronics for individual operation and yet provides full external control capabilities. The electronics include not only complete motion controls and read/write electronics with skew delays and dual level sensing, but also logic to independently search for file marks.

A simple block diagram of the 606 is given in figure 3-2. Table 3-1 describes the function of the input/output data and control lines. The following points summarize the functions of the input/output lines.

1) Seven interconnecting lines carry the information being read, including parity and a single associated read sprocket line carries a pulse which tells the system that information is on the lines. A duplicate set of eight lines is used for writing. An additional line, write ready, indicates the file protect status. Read information on the lines is in true binary format; write information is in change-on-ones (NRZ1) format. Write timing is established and parity is generated and checked external to the 606.

2) Three lines are used to select and indicate recording density.

3) Four lines are used to select tape motion. Upon selection of forward or reverse, a signal on either the write select or start read lines will start tape motion. The selection of rewind or rewind unload will automatically start tape motion.

4) The load point and end of tape lines indicate the tape status. A ready line states that the 606 is ready for external control and the busy line indicates when tape is in motion. The master clear line will immediately stop all tape motion and clear all 606 registers (except density and ready).

5) The end of record and file mark lines indicate when the tape has reached these positions. A stop on file mark line tells the 606 to proceed to the next file mark (forward or reverse) without stopping at the end of records.

6) Nine lines are used for address selection indication; eight plus separate return. Individual ground lines are available for each cable.

A signal on a line is represented by a binary "1" (0v). All signals are steady state except write sprocket, read sprocket, and end of record. These three are 4 usec pulses.

The following sections of the manual provide complete interface information:

Input/Output cable assignments - Detailed Specifications (CH. 1)
Input/Output voltages, impedance, etc. - Detailed Specifications (CH. 1)
Functions of I/O Lines - Table 3-1 in Logic Description
Interrelationship of 606 functions - Figure 3-2
Detailed discussion of 606 logic - Logic Description (CH. 3)
Explanation of terms and symbols used in Logic Description (appendix A)

This chapter describes the logic that controls the operation of the 606 magnetic tape transport. The descriptions are, in all cases, based on the logic diagrams included in the text. It is assumed that the reader is familiar with Control Data logic theory, diagrams, and symbols (appendix A and B).

For purposes of discussion, the 606 is divided into five general control sections: read, write, motion, servo drive, and local. Figure 3-2 shows the relationship of these sections to the control unit; table 3-1 describes the functions of the input/output data and control lines.

READ CONTROL

This portion of the logic controls the transfer of information from the 606 to the tape control unit (TCU) and consists of the following circuits (figure 3-1):

Select Read	Allows a read operation to be performed when selected by the TCU.
Read Data	Handles the flow of information from tape to output lines.
Select Density	Specifies the rate at which information is transferred to the TCU.
Read Gate	Allows the transmission of information to the TCU in response to signals from the select density circuit.
File Mark Stop	Stops tape motion when a selected file mark is detected.

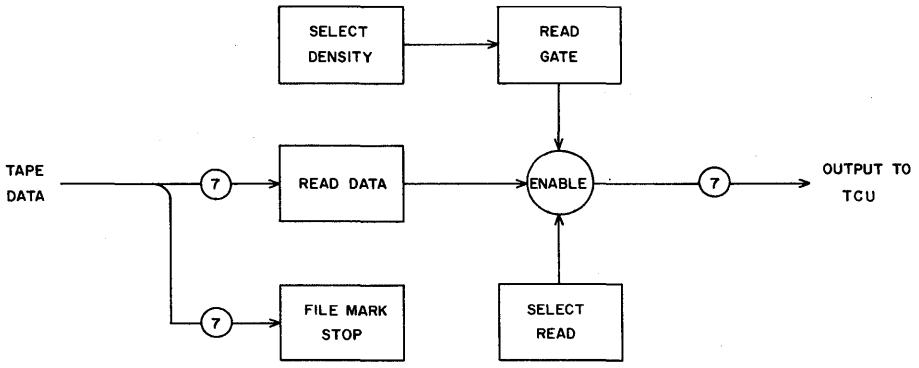


Figure 3-1. Read Control Circuits

TABLE 3-1. COMMUNICATION LINES

TCU TO 606	
Write Select	Enables write and read verify operations.
Write Sprocket	Indicates that write information is on the input lines and may be sampled by the 606.
Input Data (write bits)	Seven input data lines carry write information to 606 (6 information bits plus 1 parity bit).
Read Select	Enables read operation.
High Density	Selects high density operating mode (556 lines per inch).
Low Density	Selects low density operation mode (200 lines per inch).
Stop on File Mark	Stop at next file mark.
Forward	Moves tape forward at 150 ips. Tape stops at nearest end of tape marker.
Reverse	Moves tape reverse at 150 ips. Tape stops at nearest end of tape or load point marker.
Master Clear	Establishes initial operating conditions by clearing all select conditions. Immediately stops tape motion.
Rewind	Moves tape at 320 ips to nearest load point marker.
Rewind Unload	Reverse at 320 ips to tape unload condition (all tape on supply reel) and stop.
Status Light #1	Turns on white light on Unit Number Selection Switch.
Status Light #2	Turns on red light on Unit Number Selection Switch.
606 TO TCU	
Write Ready	Indicates that the file protect ring is in and tape has been loaded. Write and read verify operations may now be performed.
Output Data (read bits)	Seven output data lines carry read information to control unit (6 information bits plus 1 parity bit).
Read Sprocket	Indicates that read information is on output lines and may be sampled by control unit (5 usec pulse).
High Density	Indicates that high density mode is selected.
End of Operation	End of record or load point marker sensed.

TABLE 3-1. CONTINUED

606 TO TCU (Continued)	
File Mark	File mark sensed.
Busy	Indicates that tape is in motion. Signal dropped 4 ms after motion stops.
Ready	Indicates that the 606 is under external control and is prepared for next operation (no fault conditions exist).
Unit Number	Eight (0 through 7) unit number designation lines.
End of Tape	End of tape marker sensed.
Load Point	Indicates that tape is at load point.

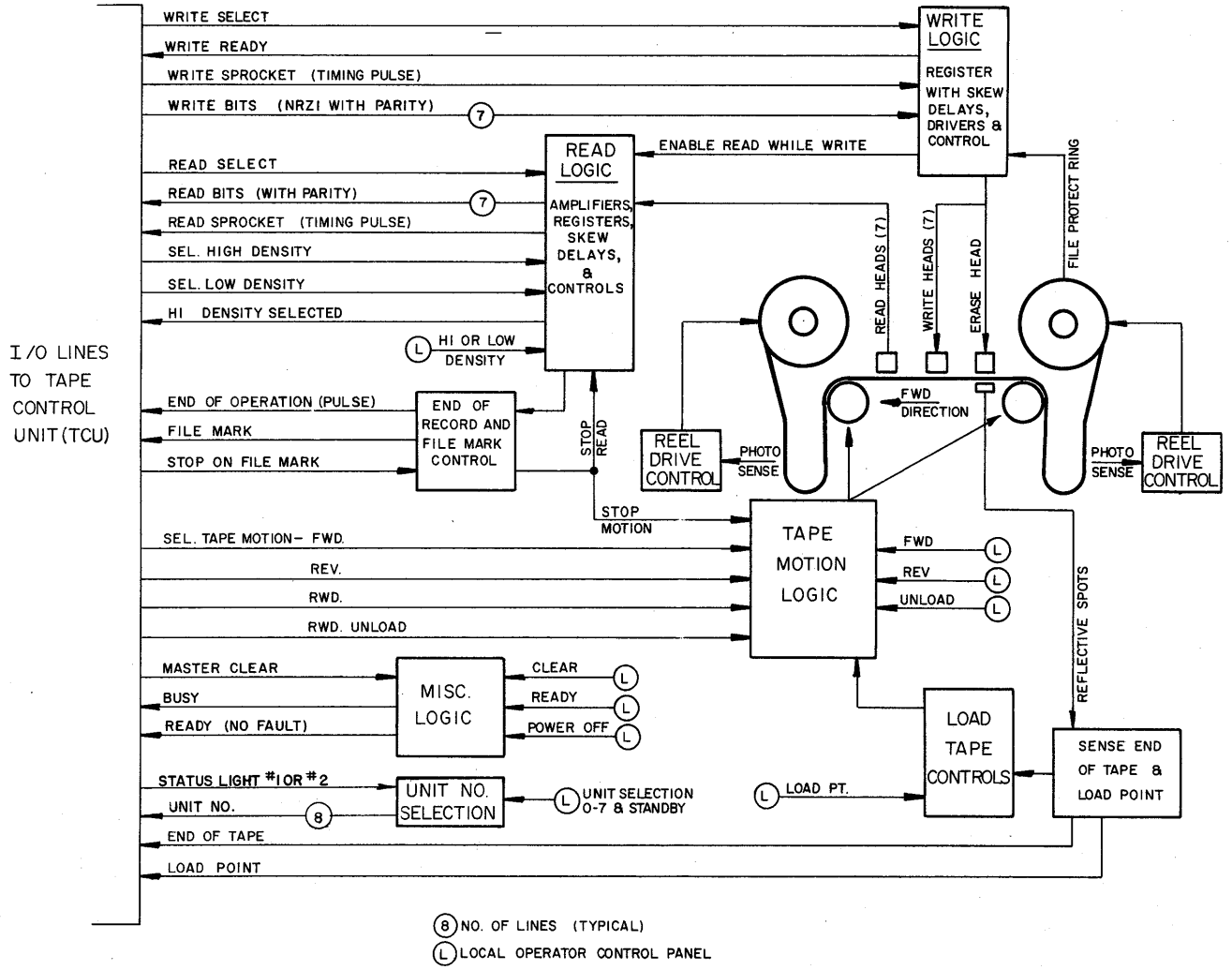


Figure 3-2. Block Diagram

SELECT READ CIRCUIT

The select read circuit (figure 3-3) permits:

1) A read operation to be performed when locally or externally selected.

2) The execution of externally selected motion operations.

The state of the Select Read FF (K166/167) determines whether or not a read operation will be performed. When cleared, this FF disables a read operation by disabling the AND gate to I114 (see read gate circuit). Rank I of the Read register is, in this case, held in the clear state and a read operation is disabled.

The Select Read FF is cleared when forward or reverse tape motion is terminated (see motion control circuit) or when an end of operation signal is produced by the file mark stop circuit. A read operation therefore, must be reselected, if desired, each time tape motion is stopped or an end of operation signal is sent to the TCU.

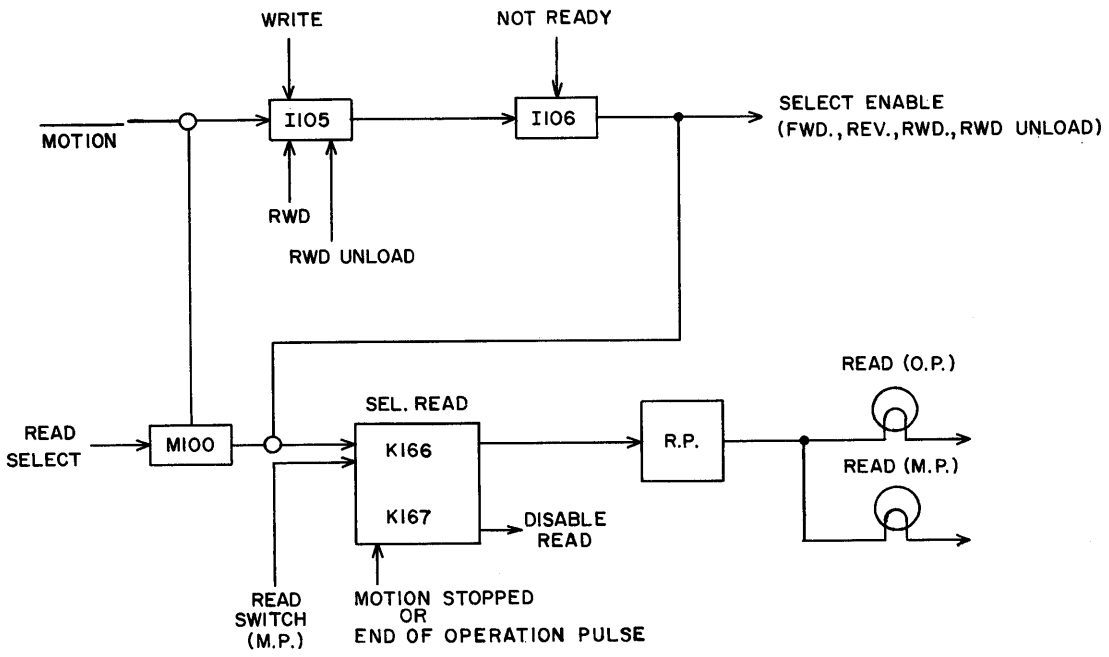


Figure 3-3. Select Read Circuit

The Select Read FF is set by the Read switch on the maintenance panel or by a read select signal from the external equipment. In the set state, the constant clear signal to rank I is removed, allowing a read operation to be performed. The Read indicators on the maintenance and control panels are turned on when the FF is set.

A "1" output from I106 allows the execution of an externally selected rewind, rewind unload, forward, or reverse operation. A "1" output from I106 indicates that the 606 is ready (under external control) and one of the following conditions is present at the same time:

1) External read select and no motion operation in progress
2) Write operation enabled
3) Rewind selected and no rewind in progress
4) Rewind unload selected and no rewind operation in progress

A forward or reverse motion operation cannot be initiated, therefore, until a read or write operation is selected. Also, a rewind or rewind unload operation cannot be initiated until a previously selected rewind or unload operation is completed. However, a rewind or rewind unload operation may be initiated while a read or write (forward or reverse) is in progress.

READ DATA CIRCUITS

The seven read data circuits route information from the tape to the external equipment. A typical circuit including representative waveforms is shown in figure 3-4.

During a read operation, tape data is detected by the read heads and amplified by level and peak detectors. After being read and amplified, the information bits are deskewed and placed in rank I of the 7-bit read register. The lower order six stages of the register receive the information character; the highest order stage receives the parity bit. The information bits are next gated from rank I to rank II by a pulse from the read gate control circuit. Rank II provides short term storage for the information bits while the bits are placed on the output lines for transfer to external equipment.

A "1" bit is read from the tape each time a change is sensed in the polarity of the tape flux pattern. The voltage induced in the head winding appears at each end of the winding to represent a "1" bit. Typical read head signals are represented by waveform 1.

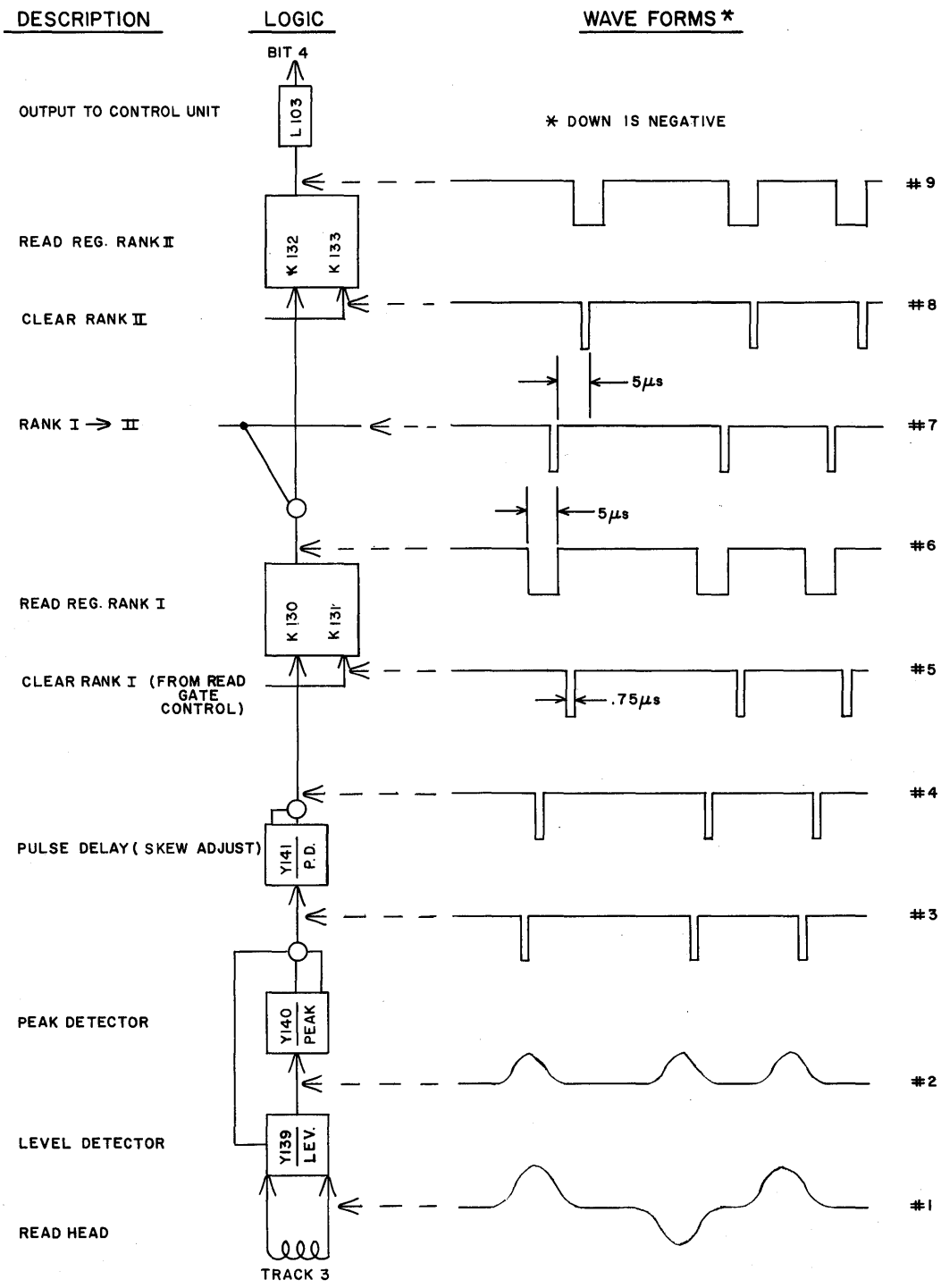


Figure 3-4. Typical Read Data Circuit

The signals from the read heads are amplified and converted to standard logic circuit voltage levels by the level and peak detectors which produce "1" outputs for each "1" bit read from the tape. The level detectors eliminate random noise, preamplify the read head signals from 25 mv to 5v, and rectify the signal.

The peak detector input uses the rectified output from the level detector (waveform 2). The output from the peak detector is a .75 usec pulse as shown in waveform 3.

The pulse delay cards compensate for timing differences in the read heads and peak and level detectors. The output from the pulse delay card is a .75 usec pulse (waveform 4) which is routed to the associated flip-flop in rank I. If an information bit on the tape is a "1", the Read register stage associated with that bit will be set. If the bit is a "0", the stage will remain cleared.

Information bits stored in rank I are gated to rank II by a 1 usec pulse (waveform 7) after all bits have been placed in rank I. Rank I is then cleared in preparation for the next information character (waveform 5). Rank II retains the synchronized read information bits for 5 usec to allow transmission to the control unit. Rank II is then cleared as shown in waveform 8.

Detailed information concerning the special purpose cards used in this circuit is in appendix B.

SELECT DENSITY CIRCUIT

The select density circuit (figure 3-5) specifies the rate at which information is to be transferred to the external equipment. The operation mode may be selected from either the control unit or the 606 control panel. If the mode is externally selected, the state of the Density FF (K164-165) will depend on which M10- card produces a "1" output. For example, if a high density read operation is externally selected, the Density FF will be set by the "1" output from M101.

The density mode selection may also be changed by pressing the Density key on the control panel. Pressing the Density key allows the switch capacitor to charge for approximately 20 usec. While the capacitor is charging, M102 and the delay card both produce "1" outputs. The output from the delay card fully enables the AND input to one of the XKA cards. Note that the selection of XKA cards is entirely dependent on the current state of the Density FF.

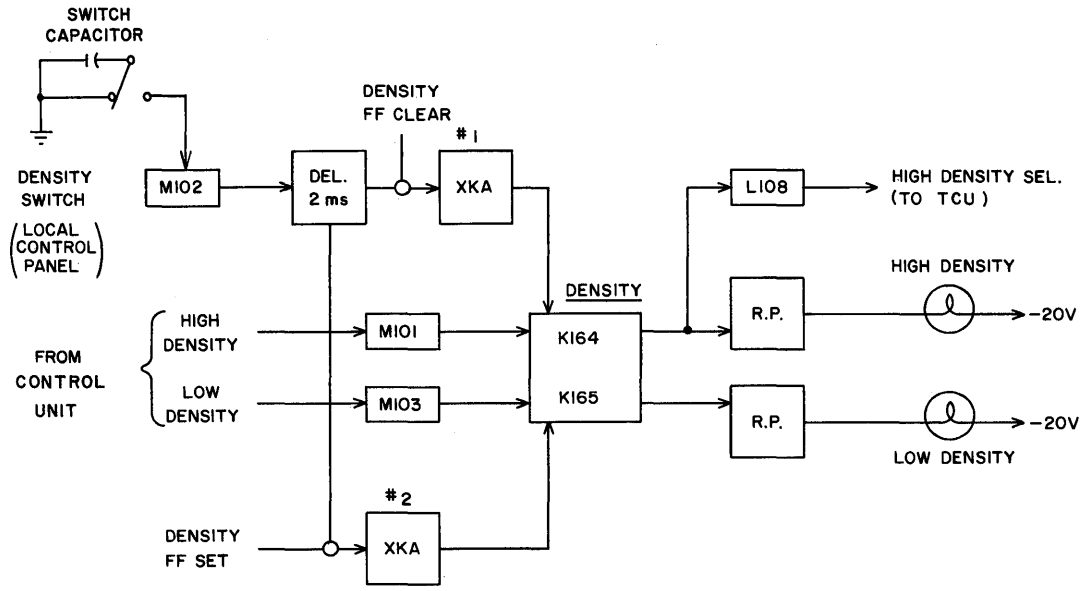


Figure 3-5. Select Density Circuit

The switch capacitor, when fully charged, allows a "0" output from M102 which is delayed for 2 ms by the delay card. This delay eliminates switch bounce and stabilizes the signal.

After the 2 ms delay has been depleated, the output to the selected XKA card changes from a "1" to a "0" resulting in a "1" output pulse from the card. This pulse toggles the Density FF which changes the density mode.

If, for example, the Density FF were initially in the clear (low density) state, the input to XKA #1 would be a "1" while the switch capacitor was charging (Density key down). After fully charging the capacitor and stabilizing the signal by means of the 2 ms delay, the input to XKA #1 would change from a "1" to a "0". The resulting "1" output from XKA #1 would set the Density FF, thus changing the mode selection from low density to high density.

The proper Density indicator will be lighted regardless of the density mode selected or the means by which it was selected. Also, if the high density mode is chosen, a signal will be sent to the adapter via L108 notifying the equipment of the selection.

READ GATE CIRCUIT

The read gate circuit (figure 3-6) controls the transmission of information to the Read register and output lines. The accompanying flow chart and table (figure 3-7 and table 3-2) describe the sequence of events executed during the operation.

The AND input to Y117 is disabled when information is placed in rank I of the Read register. The resulting "0" input to Y117 is delayed 7 usec by Y117 and Y116 before being applied as an input to I112. If a high density read operation is selected, I112 produces a "1" output immediately after exhausting the two delays. If a low density operation is selected, an additional delay of 15 usec caused by Y115 must elapse before I112 will produce a "1" output. These delays allow time for the information bits to be read from tape and placed in rank I before being gated to rank II.

The "1" output from I112 gates the 7 bits in rank I to rank II. The information is then placed on the output lines for sampling by the TCU.

Approximately 1 usec after I112 produces a "1" output, I113 produces a "0" output which, when inverted by I114, clears rank I of the Read register. The register is thus prepared to accept the next line of information to be read from the tape. Clearing rank I recycles Y117, Y116 and Y115 and the output from I112 reverts to "0".

The "0" output from I113, when inverted by I500, also sets K170/171 which allows L107 to produce a sprocket ready signal. This signal indicates that information is present on the output lines and may be sampled by the TCU.

Five usec after K170/171 is set, Y114 produces a "0" output which, when inverted by I110, clears rank II of the Read register and drops the sprocket ready signal by clearing the FF. Rank II can now accept the next character from rank I. During the time these actions are being performed, the next character is being read from tape and placed in rank I. The entire process is then repeated.

Note that if a read or write operation is not selected, the AND input to I114 is disabled resulting in a continuous "1" output from I114. Rank I of the Read register is, in this case, held in the clear state and the read operation is disabled. Also note that when a read or write operation is initially selected, the AND gate to I114 remains disabled for 2.2 ms. This precaution eliminates the possibility of transient noise being read as information while the tape is brought up to speed.

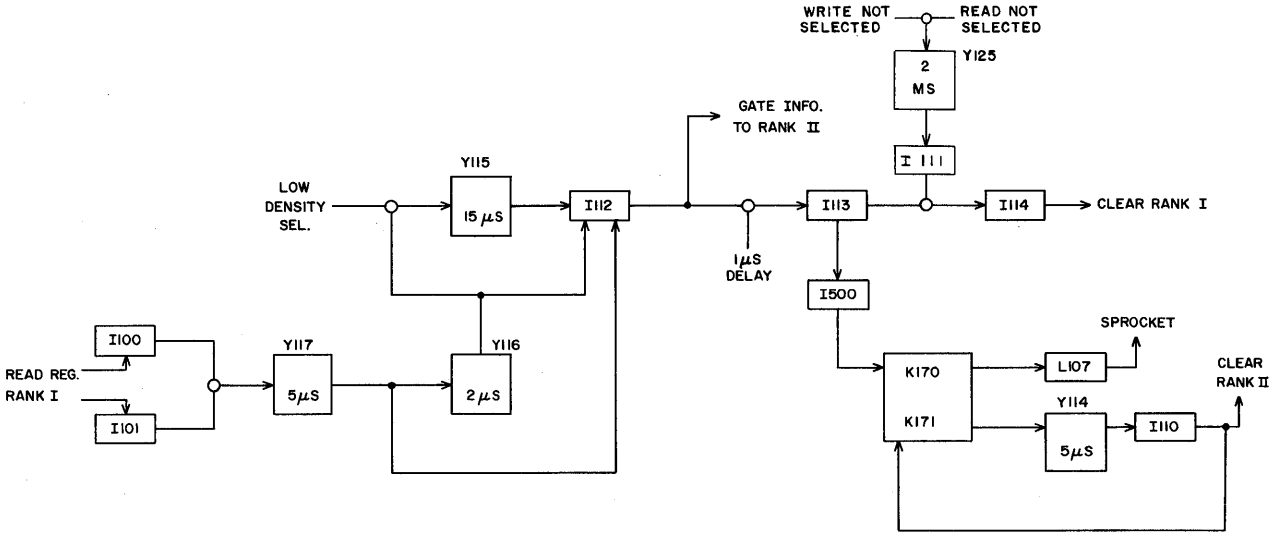


Figure 3-6. Read Gate Circuit

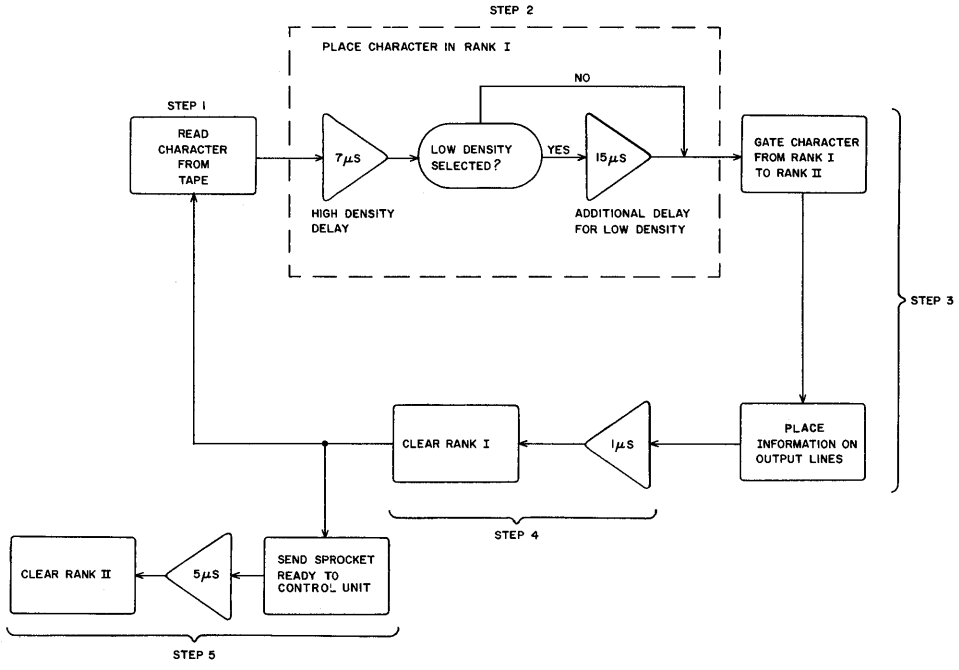


Figure 3-7. Read Sequence

TABLE 3-2. READ SEQUENCE

STEP	COMMENTS
1	An information character on the tape is detected by the read heads and amplified by peak and level detectors.
2	The bits are placed in rank I of the Read register. The time needed before all information bits are placed in rank I is determined by delays. If the high density mode is selected, a 7 usec delay is exhausted. An additional delay of 15 usec is necessary if low density is selected.
3	The bits in rank I are gated to rank II for short term storage. The information is then placed on the output lines for sampling by the external equipment.
4	Rank I is cleared in preparation for the next information character from tape. (The 1 usec delay allows information to be gated to rank II before rank I is cleared.)
5	A sprocket ready pulse is sent to the external equipment, notifying the equipment that information is available on the output lines for sampling. Five usec later, rank II is cleared in preparation for the next information character from rank I. During step five, the next character is read from the tape and placed in rank I. The entire process is then repeated.

FILE MARK STOP CIRCUIT

The file mark stop circuit (figure 3-8) performs the following functions:

1) Notifies the TCU by means of an end of operation pulse when an end of record, load point marker or file mark is detected. If a stop on file mark is selected, the TCU is notified only when a file mark is detected.

2) Stops tape motion when an end of record is sensed, unless a stop on file mark is selected. In this case, motion stops only when a file mark is detected.

Figure 3-9 illustrates the operation of the circuit. The following paragraphs describe the general sequence of events with respect to figures 3-8 and 3-9.

The End of Record FF (K504/505) is cleared when information is placed in rank I of the Read register. The FF is set when rank I is cleared (information gated from rank I to rank II). Thus, the FF is switched from one state to another while information is being read from tape and gated from rank I to rank II.

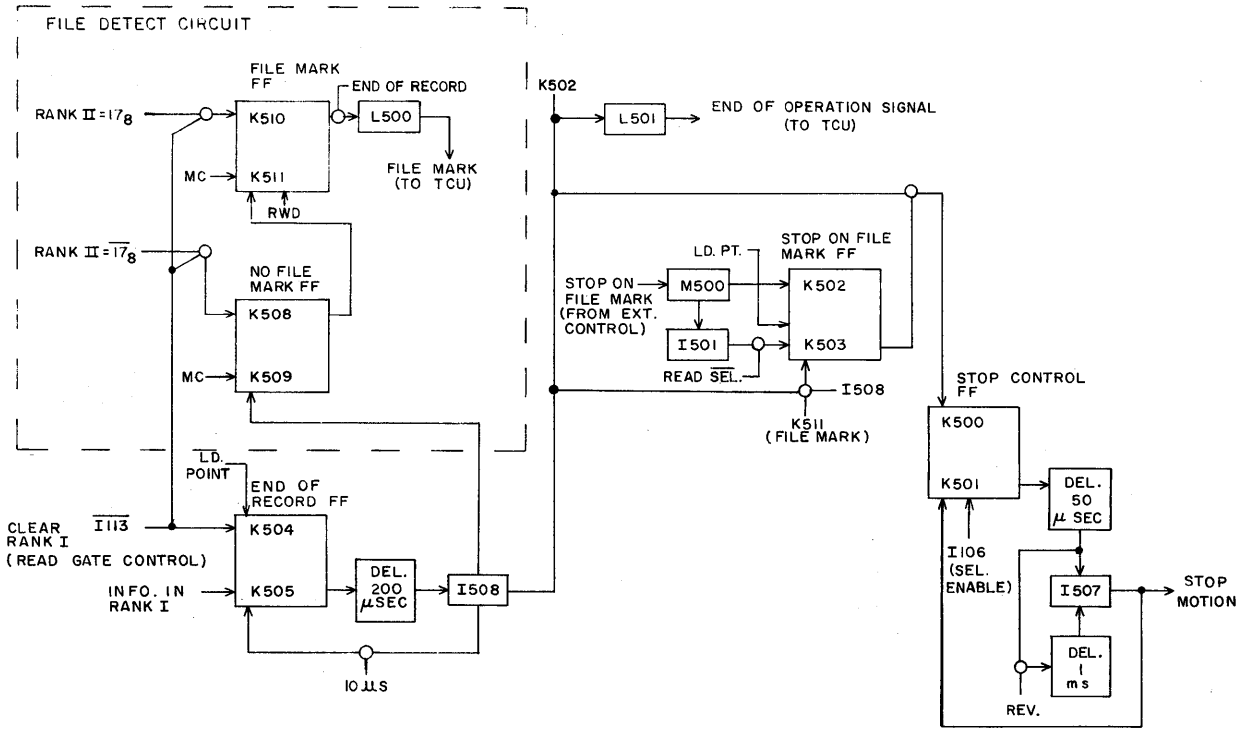


Figure 3-8. File Mark Stop Circuit

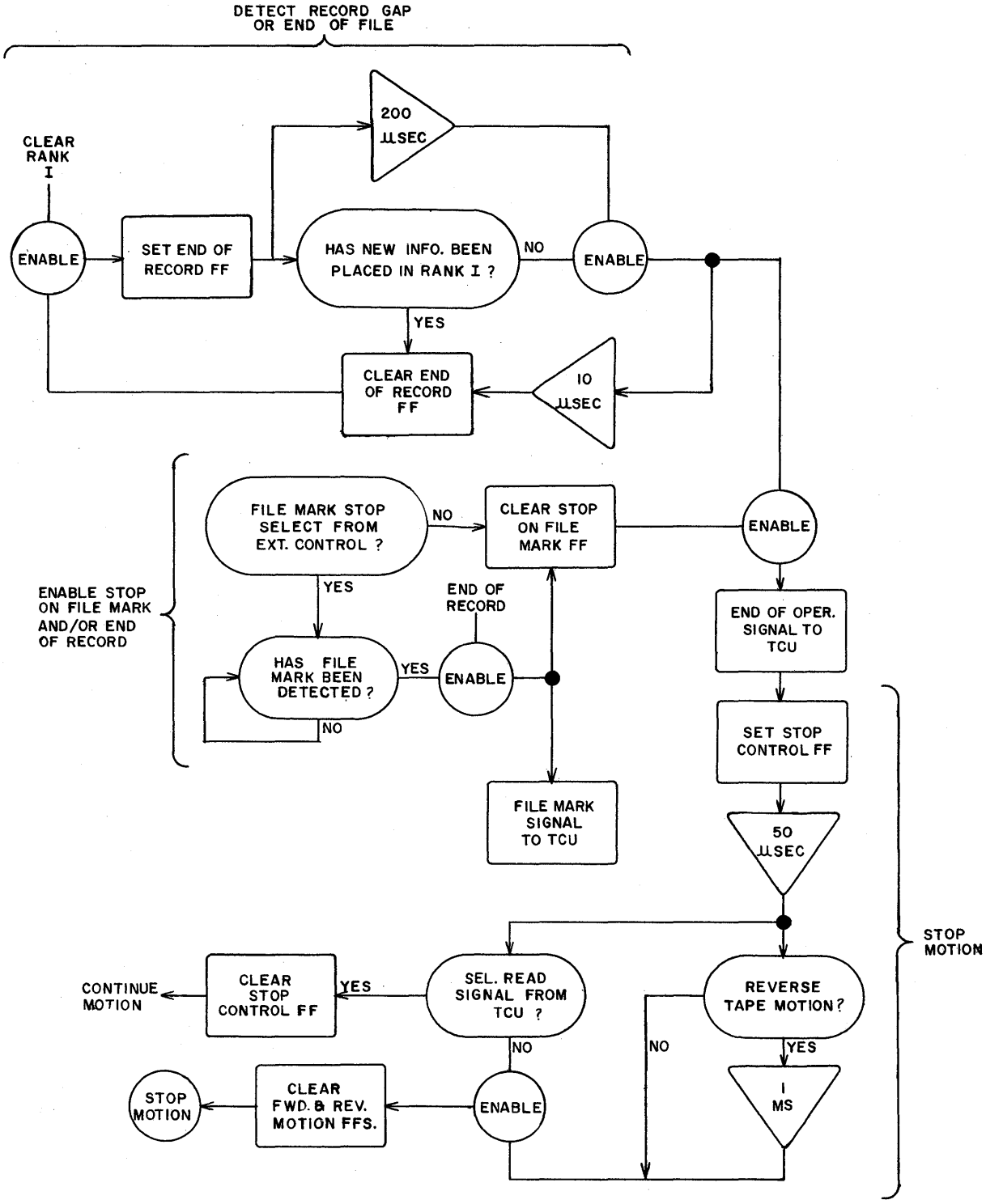


Figure 3-9. Operation Flow Chart - File Mark Stop Circuit

When the last character in a record is read, the End of Record FF remains set until the 200 usec delay (Y502) is depleated. The resulting "1" output from I508, after a delay of 10 usec, recycles the circuit by clearing the End of Record FF. During this 10 usec period, the "1" output from I508 enables an end of operation signal to be returned to the TCU if a stop on file mark has not been selected (Stop On File Mark FF cleared). If a stop on file mark was initially selected (Stop On File Mark FF set), the end of operation signal will be produced only when a file mark is detected which clears the Stop On File Mark FF.

Note that when a load point marker is detected during a rewind operation, the End of Record FF will also be set. This procedure allows the TCU to be notified by an end of operation pulse when the load point marker is sensed without monitoring the entire rewind operation.

In summary, the end of operation pulse indicates one of the following three conditions:

1) An end of record has been located and stop on file mark not selected.
2) A stop on file mark selected and a file mark located.
3) Rewind operation selected and load point detected.

The 10 usec "1" output from I508 also performs the following actions:

1) Clears the file mark detect circuit.
2) Partially enables the AND input to the Stop Control FF.
3) Clears K502/503 if a file mark was read in the last record.

The file detect circuit examines information placed in rank II of the Read register. The No File Mark FF is cleared by I508 each time an end of record is detected. If the next record contains any information characters unequal to 17_8 (BCD), the No File Mark FF will be set and will remain set until cleared by I508. If, however, the new record consists entirely of characters equal to 17_8 (BCD), the No File Mark FF will remain cleared and the File Mark FF will be set. The file mark signal will be gated to the TCU when the end of record is located. Note that the File Mark FF is cleared during a rewind operation. Thus, if a rewind operation is initiated immediately following the detection of a file mark, an additional file mark signal will not be sent to the TCU when the load point marker is located.

The set AND input to the Stop Control FF will be fully enabled only if the Stop On File Mark FF is cleared. When cleared, the Stop On File Mark FF indicates one of the following:

1) The FF was set by a stop on file mark signal from the external control and was subsequently cleared when the file mark and end of record were detected.

2) A stop on file mark operation was not selected, thus, the Stop On File Mark FF remained cleared.

In case one, the Stop Control FF will be set when a file mark and end of record are both detected. In case two, the FF will be set when only an end of record is detected.

When set, the Stop Control FF allows a "1" output from I507 which stops tape motion by clearing the Forward and Reverse Motion FFs. However, I507 does not stop motion until the 50 usec delay has been exhausted. Note that an additional delay of 1 ms must be depleted before reverse tape motion is stopped.

The 50 usec delay allows time for the TCU to clear the Stop Control FF by means of a new read select signal before tape motion stops. Thus, if the TCU produces a read signal before the 50 usec delay is exhausted, the output from I507 will remain a "0" and tape motion will continue. The 1 ms delay allows additional time during reverse tape motion to position the write heads in the inter record gap. This precaution insures that during a subsequent write operation, the entire record will be rewritten. Note that the file mark stop circuit is not allowed to terminate tape motion during write or rewind operations as the Stop Control FF is held in the clear state by I106 (see read select circuit).

WRITE CONTROL

The write control portion of the tape unit logic consists of write data circuits (figure 3-11) and an associated write enable circuit (figure 3-10). The write data circuits accept information in the form of 7-bit characters from the TCU and route the data to the write heads for recording. The enable circuit allows the information to be transferred from the external control to the write heads if a write operation is selected.

WRITE ENABLE CIRCUIT

A write operation is initiated by a write select signal from the external equipment. This signal remains up during the entire write operation. Before the actual write operation is performed, a number of initial conditions, specified by the AND inputs to I015 and Y017, must be satisfied.

Y017 receives a "1" input only if tape is not in the unload condition and the file reel contains a file protect ring (File Protect switch closed). The resulting ground output from the relay puller:

1) Returns a ready to write signal to the external control indicating that a write operation may be performed.
2) Holds the File Protect switch closed by means of the write enable solenoid.
3) Selects the Write enable relay which turns on the overhead lights. These lights are turned on only when the file protect ring is detected.

If all of the conditions comprising the AND input to I015 are present, Y015 receives a "1" input from I016 and performs the following:

1) Turns on the Write indicators on the operator and maintenance panels.
2) Allows current to flow through the erase head.

If a write operation is selected and enabled, the Write register is initially stabilized in the clear state due to the input delay circuit associated with I017. This circuit enables a 5 usec "1" output from I017. This output clears the entire Write register and permits write current to flow in the same direction as erase current. Tape particles are therefore initially aligned in the same direction as they are when tape is erased. This eliminates the possibility of "1" bits being recorded on the tape when a write operation is first selected.

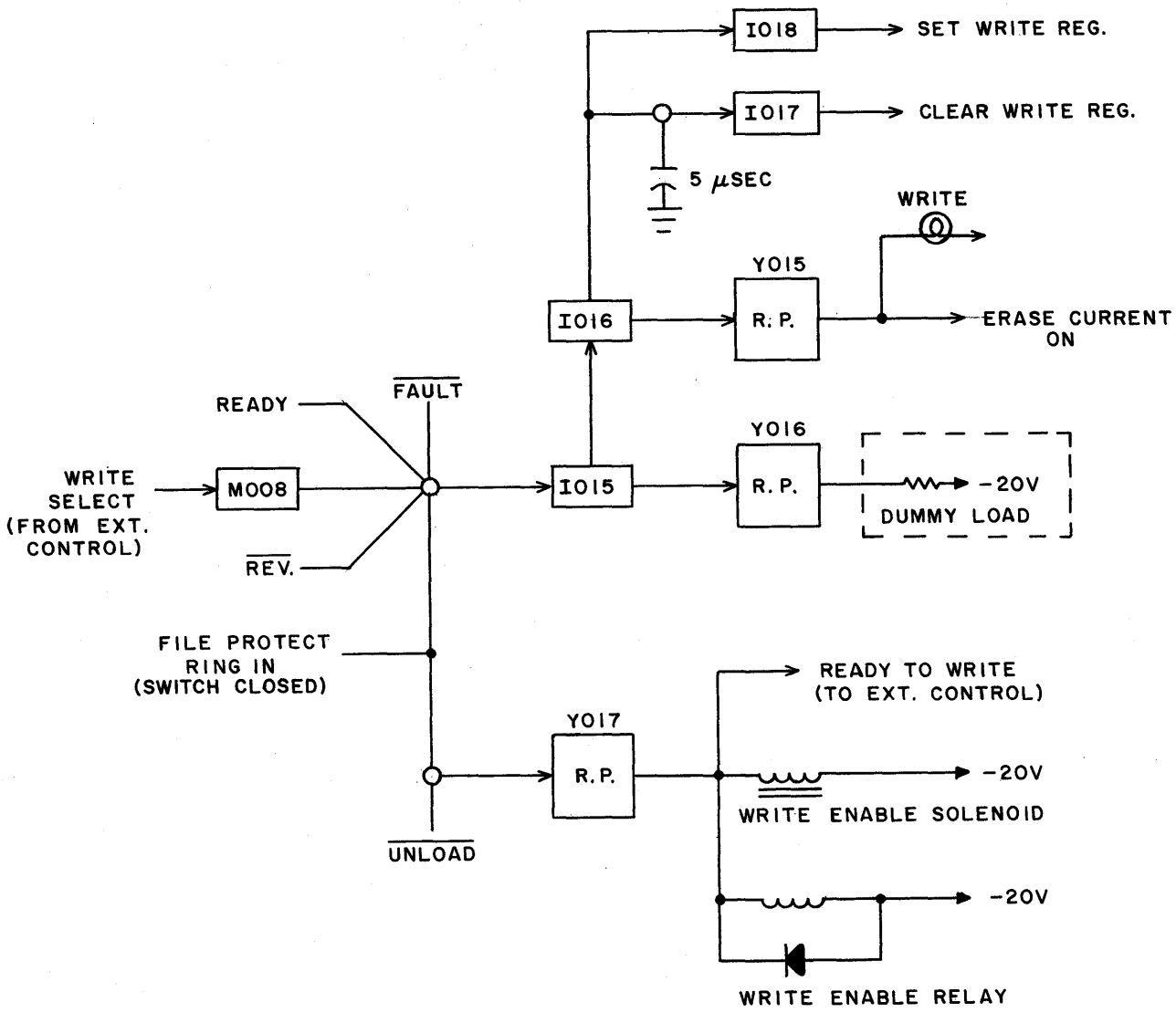


Figure 3-10. Write Enable Circuit

If a write operation is not selected or enabled, I018 and I017 produce "1" outputs which simultaneously set and clear all stages of the Write register. Each write driver receives a "0" input which effectively turns off head current. During non-write operations, Y016 receives a "1" input from I015 which allows dummy load current to flow through external load resistors. The power supply load is therefore approximately constant under non-writing conditions.

WRITE DATA CIRCUIT

A sprocket ready signal from the TCU indicates that information is on the input lines and may be routed to the write heads for recording. The presence of a sprocket ready signal results in a "1" output from I021 which is applied as an input to the pulse delay card. This card produces a "1" output pulse equal to the amount of delay which partially enables the set and clear inputs to all stages of the Write register. The input data bits from the external control can now be placed in the Write register. The skew delay cards are individually adjustable so that each bit may be gated into the register at the time necessary to vertically align all bits on the tape.

A specific Write Register FF will change state each time a "1" is to be written on that particular track; the FF will remain unchanged if a "0" is to be recorded. The TCU, in other words, must supply NRZ1 input data to the 606.

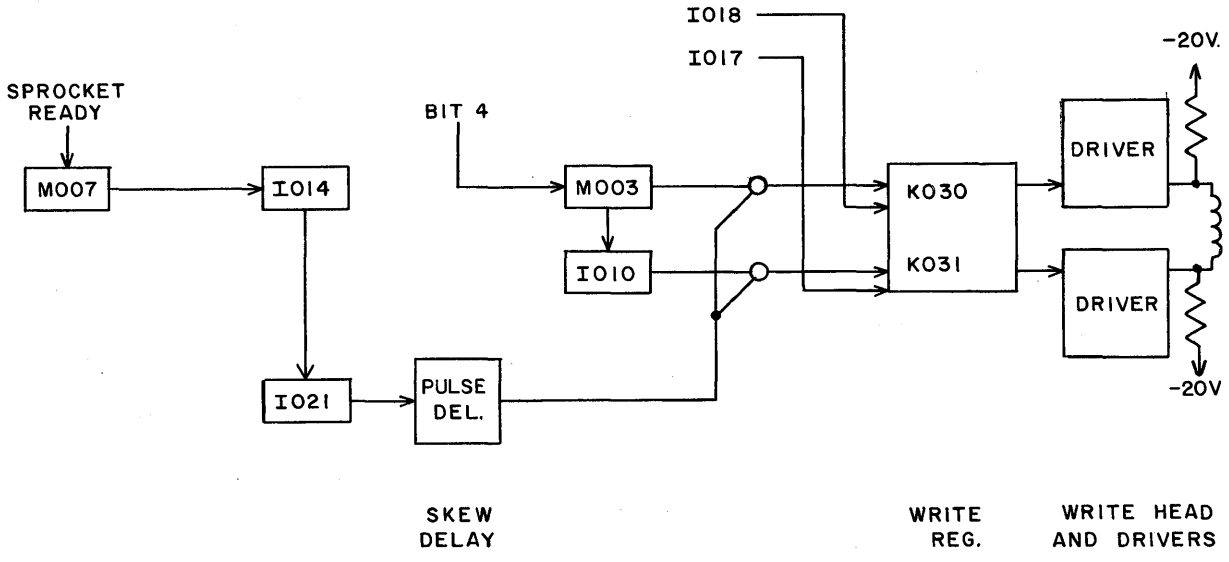


Figure 3-11. Typical Stage in Write Data Circuit

MOTION CONTROL CIRCUIT

The motion control circuit determines the direction tape is to be moved. After direction is selected, tape motion is controlled by the capstan drive and brake control circuit (appendix B) which applies pressure or vacuum to the capstans and pneumatic brake port. In the drive condition, vacuum is applied to the forward or reverse capstan while pressure is applied to the brake port. In this case, the tape is held away from the brake port but against the rotating capstan and is therefore moved across the read-write heads. In the clear or non-drive condition, vacuum instead of pressure is applied to the brake port while pressure is applied to both capstans. The tape is, in this case, held against the brake port but separated from both rotating capstans.

Tape direction is determined by the Forward and Reverse FFs. Because the forward and reverse circuits are similar in design and function, only the forward circuit (figure 3-12) is discussed.

The Forward FF is set when:

1) Forward operation is selected from external control, or
2) Forward operation is selected by pressing Forward switch on 606 control or maintenance panels, or
3) Forward operation is selected by local control logic (tape loaded and move-to-load-point operation selected, or tape not loaded and move-to-load-point operation selected).

The following actions occur when the Forward FF is set:

1) Forward indicator is turned on.
2) I407 produces a "1" output for 2 ms which is applied to Y402 in the forward capstan drive circuit. This allows two amp current to flow for 2 ms in the new direction to reduce actuation time of the pneumatic valve coil.
3) Set output from the Forward FF is sent to EF cards in the capstan drive circuit. The capstan drive circuit applies vacuum to the forward capstan. Tape is therefore moved in the forward direction.
4) A busy signal is returned to the external control indicating that a forward or reverse operation is in progress. This signal stays up approximately 4 ms after motion stops.

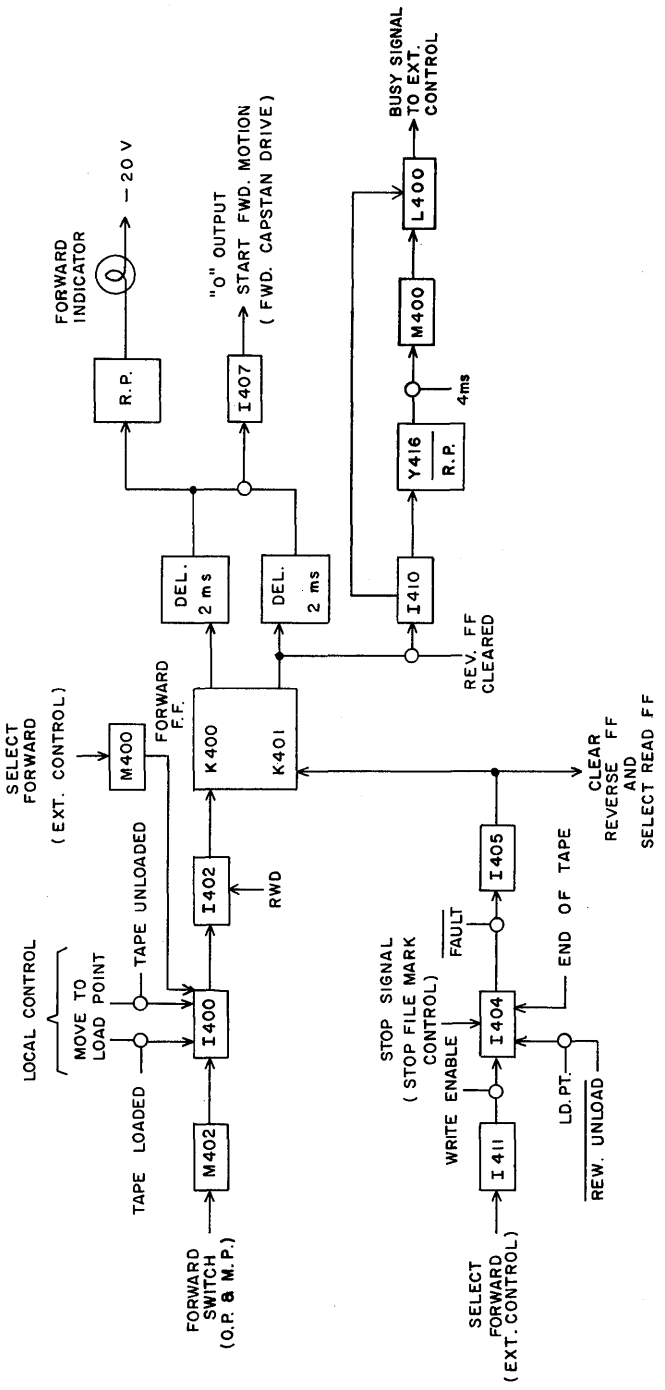


Figure 3-12. Motion Control Circuit

The Motion FFs will be cleared if any of the following conditions exist:

1) Forward command from external control is dropped while the write operation is still enabled.
2) Operation is under local control, and end of tape is detected.
3) Load point is sensed while rewind operation is in progress.
4) Fault detected.
5) Stop control circuit (figure 3-8) produces a stop signal.

When the Motion FF's are cleared, the Read Select FF is also cleared. Therefore, a new read select signal must precede every new motion select signal.

When cleared, the Motion FFs:

1) Turn off Motion indicators on the operator and maintenance panels.
2) Stop tape motion by removing vacuum to capstan and applying vacuum to brake port.
3) Drop busy signal to TCU after a 4 ms delay.

SERVO DRIVE CONTROL

The servo drive control monitors and controls the length of the tape loop in each of the vacuum storage columns. The output from this circuit is applied to the reel motor drive circuit (appendix B) which provides the output power necessary to operate the reel drive motors and brakes.

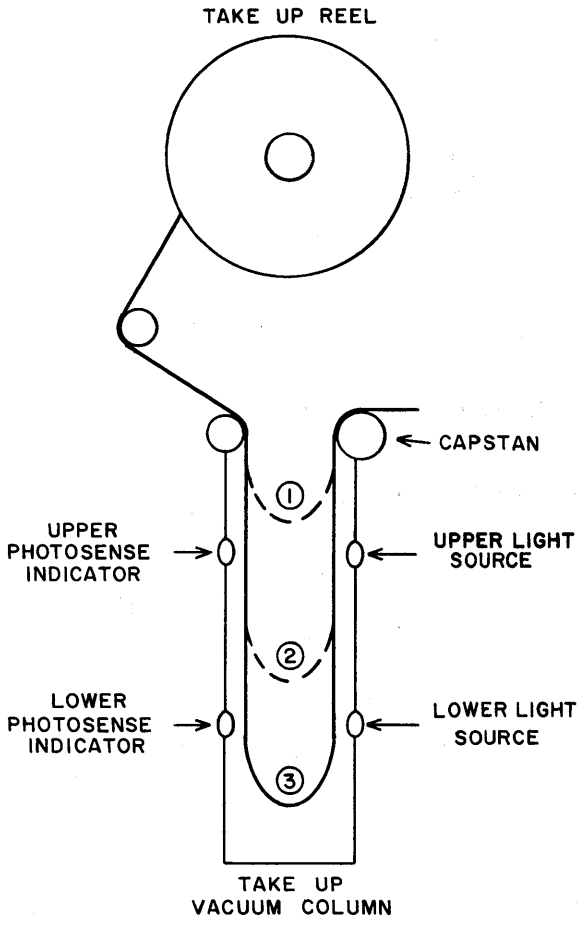
The servo drive control logic is divided into three sections:

Photosense circuits	Determine the position of tape in the vacuum storage columns and, based upon this information, specify which reel is to be braked or the direction in which it is to be driven.
Oscillator circuit	Specifies the repetition rate at which drive pulses from the photosense circuits can be applied to the reel motor drive circuit.
Tachometer circuits	Compare tape speed with a preset value. Enable drive pulses to be applied to the reel motor drive circuits only when reel speed is less than the preset value and photosense circuits specify drive direction.

The following paragraphs describe the operation of each of the sections of the servo drive control logic. Because the servo drive control logic is similar in design and function for both the take-up and supply reels, only the take-up circuits are discussed.

PHOTO SENSE CIRCUITS

Each vacuum column is equipped with an upper and lower photocell network. The photocells, when illuminated, indicate that the tape loop is above the respective photocell, i. e., tape has not been placed between the photocell and its light source (figure 3-13).



If the tape loop is in position 1, both the upper and lower photocells will be illuminated. This indicates that more tape must be supplied to the column by the take-up reel (drive reel CCW).

If the tape loop is in position 2, only the lower photocell will be illuminated. This indicates that the take-up reel must be braked to maintain the tape loop in this position.

If the tape loop is in position 3, both the upper and lower photocells will be off. This indicates that tape must be removed from the column by the take-up reel (drive reel CW).

Figure 3-13. Loop Sensing in Vacuum Columns

The outputs from the photocells are amplified and applied through the inverter circuits (figure 3-14) to the Brake, CW and CCW relay pullers. These elements, in response to the input from the photocell amplifiers, determine whether the take-up reel is to be braked or driven in the CW or CCW direction (table 3-3).

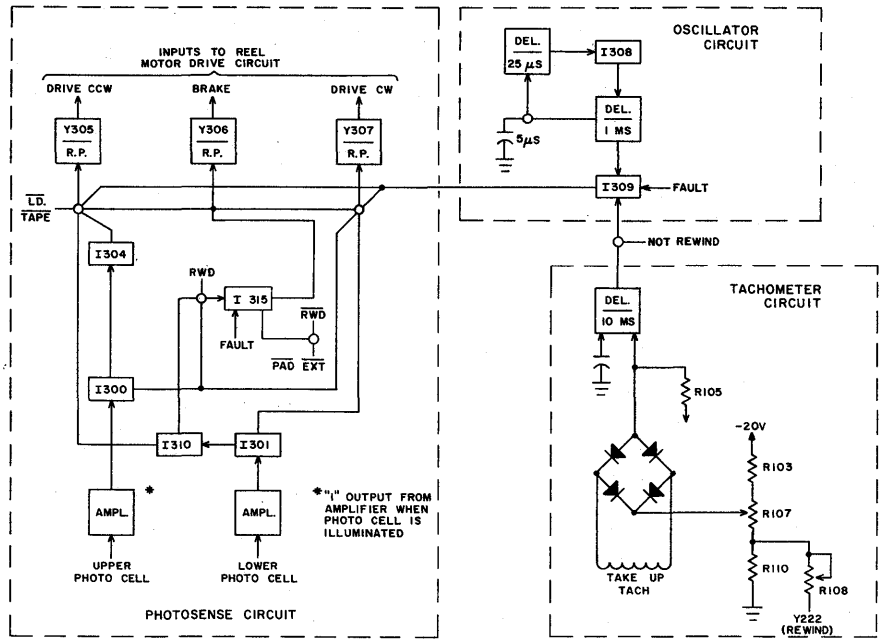


Figure 3-14. Servo Drive Control Circuits (Take-Up Reel)

TABLE 3-3. PHOTOSENSE CIRCUIT DESCRIPTION

CONDITION	ACTION	RESULT
Both photocells on	"1" input to brake relay puller (Y306) "1" input to CCW relay puller (Y305) "0" input to CW relay puller (Y307)	No brake take-up reel Drive take-up reel CCW No drive take-up reel CW
Upper photocell off Lower photocell on (Not Rewind)	"0" input to brake relay puller (Y306) "0" input to CCW relay puller (Y305) "0" input to CW relay puller (Y307)	Brake take-up reel No drive take-up reel CCW No drive take-up reel CW
Both photocells off	"1" input to brake relay puller (Y306) "0" input to CCW relay puller (Y305) "1" input to CW relay puller (Y307)	No brake take-up reel No drive take-up reel CCW Drive take-up reel CW

A fault condition causes an immediate "0" output from I315 and the take-up reel will immediately be braked. During a load tape operation, the AND input to the drive CCW relay puller will be disabled. Thus, the reel cannot be driven CCW until tape is loaded. This precaution eliminates the possibility of all tape being unwound from the take-up reel into the vacuum column during the load tape process.

During a rewind operation, the output from I315 is a steady "1" and the reel is not braked. When the load point marker is detected, however, the rewind selection is removed and the pressure pad which was previously retracted, is extended. During the period that the pad is moved from the not extended to the extended position, the reel is braked. Therefore, when the load point marker is sensed during a rewind operation, the tape is braked until the pressure pad is fully extended. This indicates that the next motion operation may be initiated.

OSCILLATOR CIRCUIT

The oscillator circuit (figure 3-14) specifies the repetition rate at which drive pulses from the photosense circuits may be applied to the reel motor drive control circuit. The oscillator applies a 25 usec "0" input to I309 every 1 ms. The 25 usec and 1 ms periods are specified by the delay cards in the circuit. Therefore, I309 produces a 25 usec "1" output as long as the tachometer input to I309 during the 25 usec period is also a "0".

A "1" output from I309 partially enables the AND inputs to the CW and CCW relay pullers in the photosense circuits. The inputs will be fully enabled, resulting in a drive pulse, when the photocells indicate the need for the pulse. If a fault exists, the output from I309 is a steady "0" and no enable pulses are sent to the relay pullers.

TACHOMETER CIRCUIT

The tachometer circuit (figure 3-14) disables the application of drive pulses to the reel motor circuit when tape speed into or out of the vacuum storage columns exceeds capstan speed by approximately 10 feet per second. The maximum speed of the reel motor is therefore limited in order to reduce the time required to stop the reel.

The tachometer is an AC generator whose output voltage is directly proportional to the tape speed into or out of the columns. As tape speed drops below the capstan speed of 150 ips, frequency and amplitude are both reduced accordingly. As tape speed is increased, amplitude and frequency increase proportionately.

The bridge circuit full wave rectifies the output signal from the tachometer allowing only negative signals to be applied as inputs to the delay card (Y314). The input circuit of the delay card is positively biased due to the resistor network composed of R105 and R107. If the tape speed into or out of the vacuum column is less than the speed of the capstan, the rectified output from the tachometer will be less than the established bias level. The delay card, therefore, will have a "0" input and output and the enable output from I309 will be solely dependent on the oscillator input. In this case, I309 will produce a 25 usec drive enable pulse every 1 ms.

If tape speed is greater than capstan speed, the delay card (Y313) will be recycled resulting in a "1" input to I309 from Y313. In this case, I309 will not produce a drive enable pulse for at least 9 ms.

The tachometers operate only during low speed (150 ips) forward and reverse operations. During a high speed rewind operation, the AND input to I309 from the tachometer circuit is disabled. Therefore, the tachometer does not affect the rate at which drive pulses are applied to the reel motors.

LOCAL CONTROL

This section of the logic consists of all sense circuits as well as those control circuits which are activated by manual switches and/or signals from the TCU. The circuits are discussed in the following order: sense, rewind, rewind unload, move to load point and load tape. Operational flow charts and tables which describe the load tape, rewind, and rewind unload procedures are included at the end of the circuit descriptions.

SENSE CIRCUITS

Ready

The Ready FF (K200/201), when set, indicates that the tape unit is under external control (ready). A not ready condition (Ready FF cleared) indicates that the tape unit is under manual control and cannot communicate with the external equipment.

The Ready FF (figure 3-15) is set by pressing the Ready key on the operator's panel. When set, the following actions occur:

1) Ready light on operator's panel and maintenance panel turns on.

2) A ready and no fault signal is sent to the external equipment indicating that the 606 is under external control.

The tape unit is returned to the not ready status (Ready FF cleared) when the unit is locally master cleared or placed in the tape unload mode. Note that a master clear from the computer will not clear the Ready FF.

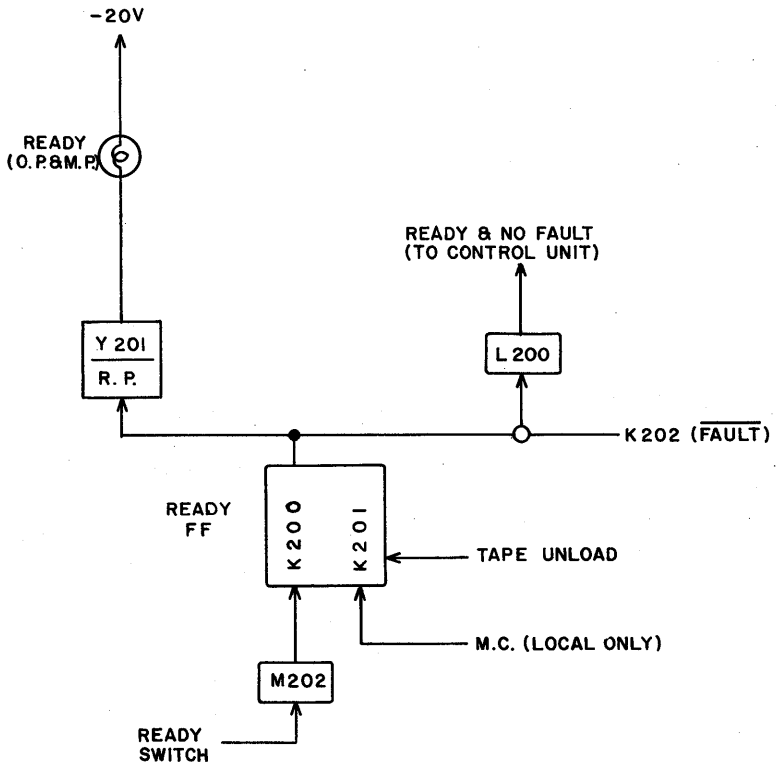


Figure 3-15. Ready Circuit

End of Tape (EOT)

Detecting the end of tape reflective marker when tape is moving forward sets the End of Tape FF (K204/205). The EOT FF (figure 3-16), when set, initiates the following:

1) Turns on the EOT light on the maintenance panel.
2) Returns an EOT signal to the external equipment indicating that the reflective marker has been located.
3) Stops tape motion by clearing the Motion FFs only if unit is under manual control (refer to motion control logic). If unit is under external control, motion continues until the forward command drops.

The FF will be cleared by detecting the EOT marker while tape is reversing, or when a load point marker is detected.

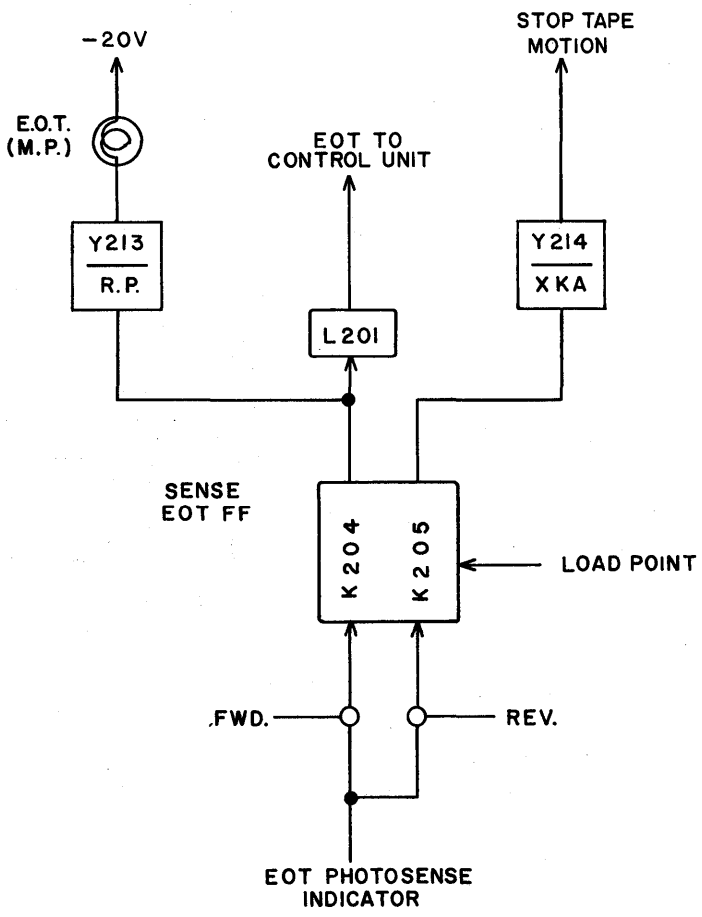


Figure 3-16. End of Tape Circuit

Search Load Point

The search load point circuit (figure 3-17) detects the load point marker and stops tape motion when the marker is positioned over the photocell. When searching load point, tape motion is stopped only when the marker has approached the photocell from the reverse direction at 150 ips. This procedure allows the same portion of the marker to be positioned over the photocell during the following operations:

1) During a forward operation, the marker is first moved forward past the photocell at 150 ips and then reversed at 150 ips.

2) During a reverse operation, because tape is already reversing at 150 ips, tape motion immediately stops when the marker is detected.

3) During a rewind operation, the marker is rewound past the photocell at 320 ips, moved forward past the photocell at 150 ips and then reversed at 150 ips.

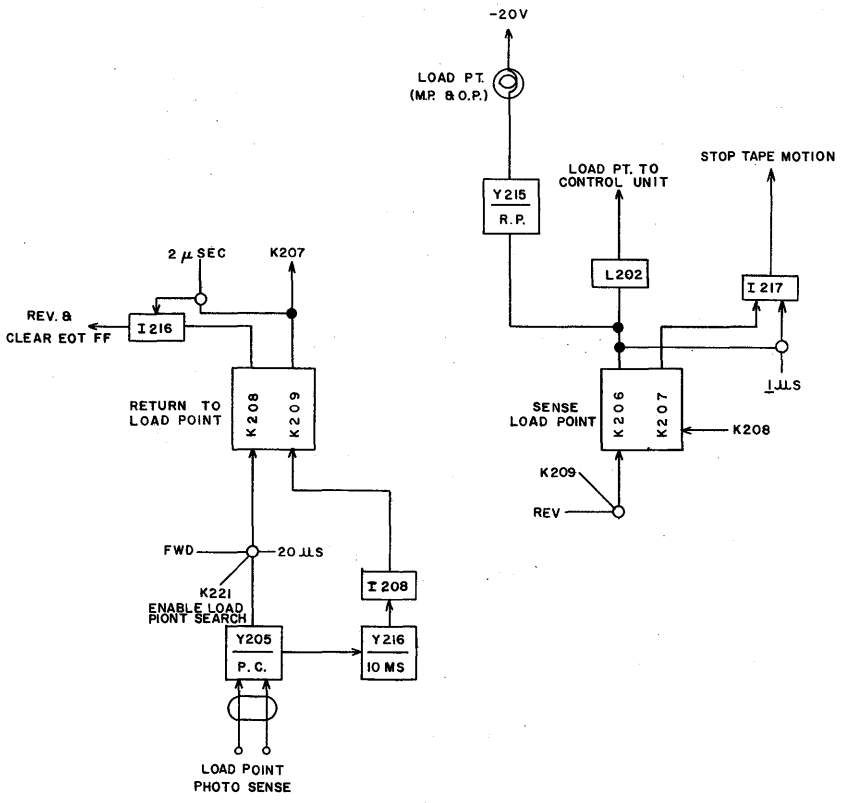


Figure 3-17. Search Load Point Circuit

The Return to Load Point FF (figure 3-17) is set when the load point marker is detected during the forward motion. After exhausting a 10 ms delay which allows tape to move completely past the load point marker, I208 produces a "1" output which clears the FF preparing it for the next search operation. The Return to Load Point FF, when cleared, allows a 2 usec output pulse from I216 which reverses tape motion (see motion control logic) and clears the Sense EOT FF. The EOT FF is cleared so that a load point or end of tape signal, but not both, is sent to the TCU.

When the load point marker is detected during the reverse operation, the Return to Load Point FF is again set. Because the tape is in the reverse mode, the Sense Load Point FF is also set.

The Sense Load Point FF, when set, performs the following:

1) Lights the Load Point indicators.
2) Returns a load point signal to the TCU.
3) Stops tape motion.
4) Clears the Move to Load Point FF (figure 3-21).
5) Initiates a move to load point sequence if a rewind operation was selected. This sequence allows the load point marker to be moved forward past the photocell at 150 ips, and then reversed at 150 ips until the photocell is again encountered. Tape motion is then stopped.

The Sense Load Point FF and the Return to Load Point FF will be cleared only when the load point marker is moved off the photocell.

Note that if tape is initially moving in the reverse direction when the load point is first sensed, the Sense Load Point FF will be immediately set and motion will stop.

Fault

The fault circuit (figure 3-18) stops operation when any one of a number of fault conditions is detected. The presence of a fault condition disables the AND input to I204 which sets the Fault FF (K202/203). The Fault FF will be set if:

1) The Pneumatic switch is open (indicates that tape has been removed from the vacuum column). The Loop Ready light on the maintenance panel will be turned off when the switch is opened.
2) Fault switch on maintenance panel is open (down) or temperature thermostat is open. An open temperature thermostat indicates that the normal operating temperature has been exceeded and the Temp Normal light on the maintenance panel will be turned off.
3) Relay K3 is de-energized (capstan motors off, vacuum motors off).
4) There is an external or local master clear.

The Fault FF, when set, initiates the following actions:

1) Lights the Fault switch on the maintenance panel and operator's panel.
2) Stops forward motion by clearing the Motion FF.
3) Stops reel servo drive and activates reel servo brakes.

The Fault FF remains set until cleared by a signal from the move to load point circuit or by an external or local master clear signal.

REWIND

The rewind circuit (figure 3-19) allows tape to be rewound from the take-up reel to the supply reel at a rate of 320 ips. Motion stops when a load point marker is sensed.

A rewind operation (refer to figure 3-24 and table 3-5) is initiated by setting the Rewind FF (K218/219). This FF is set by one of the following:

1) A select rewind signal from the TCU.
2) Pressing the Reverse key on the operator's panel.
3) Selecting a rewind unload operation. In this case, the rewind circuit merely initiates high speed rewind but does not control the operation. Motion stops not when the load point marker is sensed but rather when all tape has been placed on the supply reel (tape unloaded).

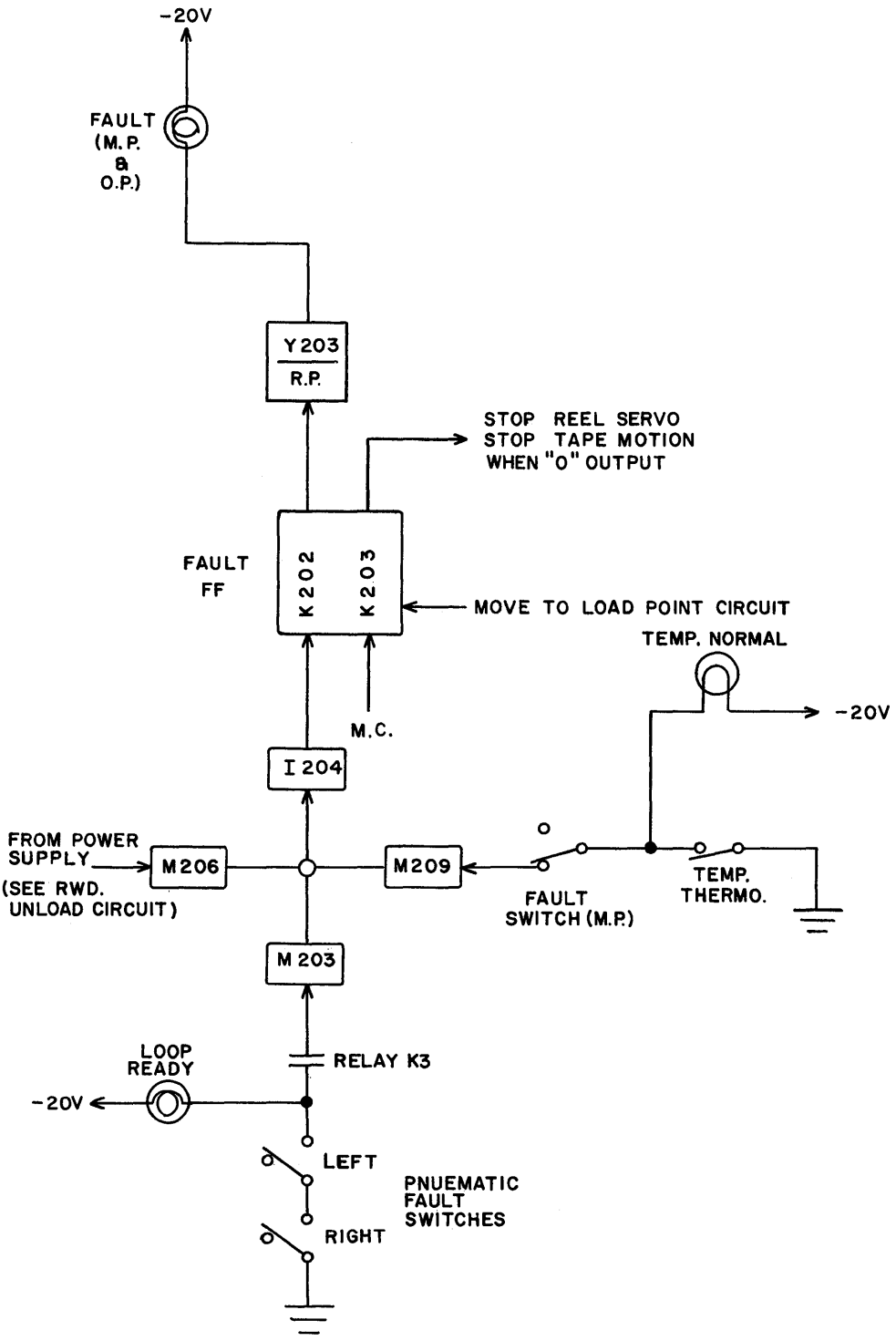


Figure 3-18. Fault Circuit

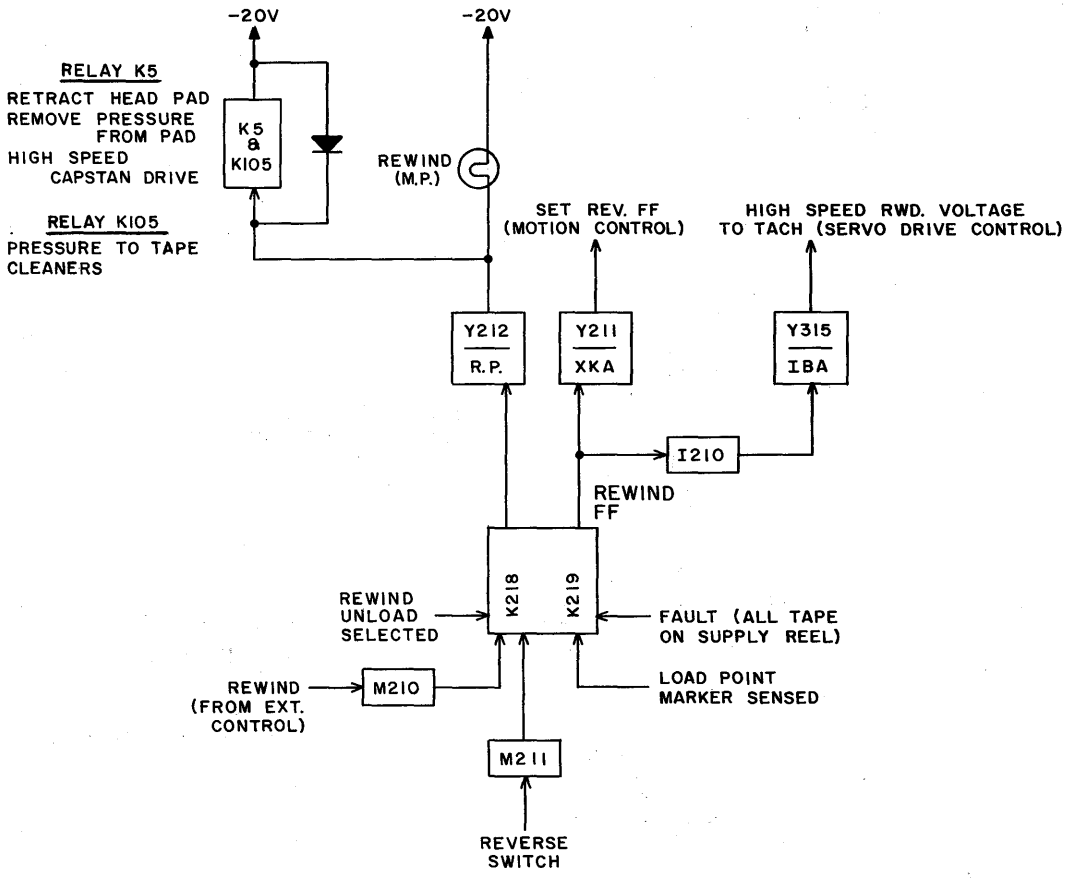


Figure 3-19. Rewind Circuit

Setting the Rewind FF results in a ground output from the relay puller (Y212), a "1" output pulse from the SKA card, and a "1" input to the IBA card.

The output from the relay puller lights the Rewind indicator on the maintenance panel and energizes relay K5 in the power supply. This relay allows voltage to be applied to the high speed windings of the capstan drive motors which enables a rewind speed of 320 ips. Energizing this relay also retracts the head pad and removes pressure from the head pad.

Relay K105 is also energized by the relay puller (Y212) when a rewind operation is selected. This relay (when energized) allows atmospheric pressure to be applied to the two tape cleaners located on either side of the head assembly. If a rewind or rewind

unload operation is not selected, K105 is not energized and vacuum is valved to the tape cleaners. Therefore, tape is cleaned only during forward and reverse operations but not during operations involving high speed rewind.

The output pulse from the XKA card sets the Reverse FF (see motion control) which initiates tape motion. The IBA card output removes ground from the tachometer positive bias circuit during high speed rewind operations. This reduces, to a safe level, the negative drive to the delay cards when the tachometer output is increased due to the high tape velocity.

The rewind FF is returned to its original clear state when a load point marker is sensed, or, in the case of a rewind unload operation, when a fault occurs indicating that all tape is on the supply reel. Clearing the Rewind FF does not stop tape motion but merely establishes the conditions necessary for the next operation. Motion is stopped by clearing the Reverse Motion FF (see motion control circuit).

REWIND UNLOAD

The rewind unload circuit reverses tape at 320 ips from take-up reel to supply reel. Tape motion stops when all tape has been rewound on the supply reel. Figure 3-25 and table 3-6 detail the rewind unload operation sequence.

The rewind unload circuit (figure 3-20) consists of the Rewind Unload FF (K214/215) and the Unload FF (K216/217). The Rewind Unload FF is set by a rewind unload signal from the external control or by pressing the Unload key on the operator's panel. The Rewind Unload FF, when set, initiates the following actions:

1) Turns on Rewind Unload indicator on the maintenance panel.
2) Sets the Rewind FF which allows tape to be reversed at 320 ips (see rewind circuit). Tape speed, however, is reduced from 320 ips to 150 ips when the load point marker is detected. This prevents tape wrap on the take-up reel when the unload condition is reached (see table 3-6).
3) Partially enables the set input to the Unload FF.

If the pneumatic switches are open, i. e., all tape has been rewound on the supply reel, the Fault FF and the Unload FF will be set. The Fault FF, when set, clears the Rewind FF and the Reverse Motion Control FF, terminating tape motion.

The Unload FF, when set, performs the following functions:

1) Turns on the Unload indicator on the operator's and maintenance panels.
2) Clears the Rewind Unload FF.
3) Clears the Ready FF. Thus, the 606, when in the unload condition, can only be operated from the operator's or maintenance panels.
4) De-energizes relay K3 (power supply) which removes vacuum from the tape storage columns and turns off the vacuum-pressure pump and capstan motors. Because K3 is in series with K4 in the fault circuit, power is also removed from the reels and brakes.

The Unload FF remains set until the tape load procedure is executed (chapter 2). Therefore, before any other operation can be executed, the tape unit must be placed in the load condition by pressing the Load Point key.

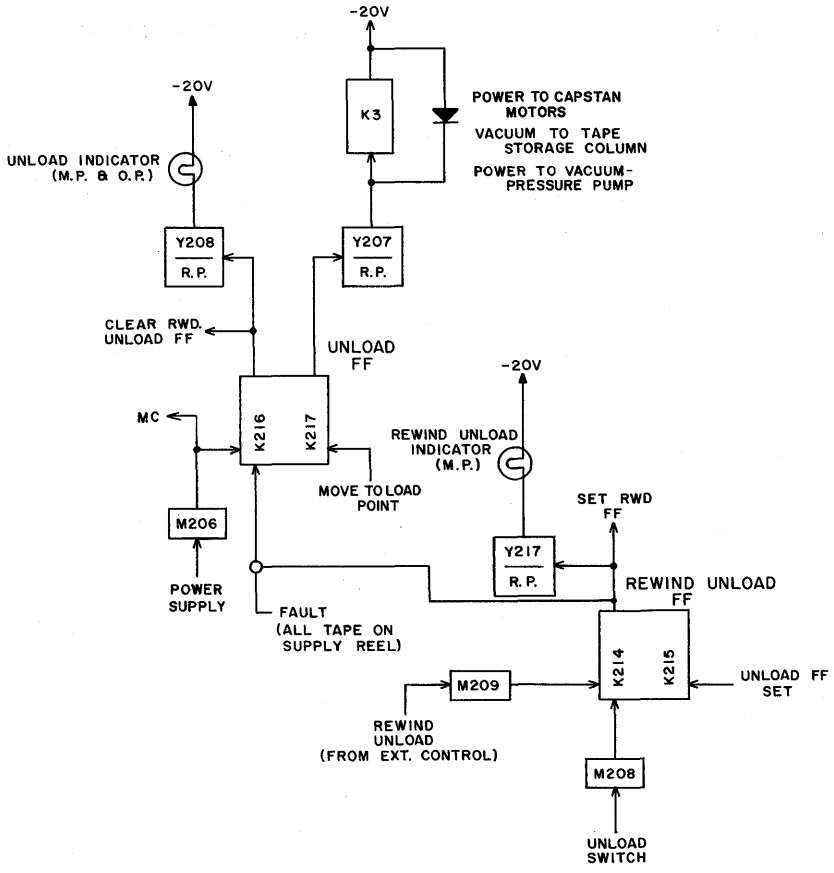


Figure 3-20. Rewind Unload Circuit

Note that an output pulse from M206 master clears the tape transport and also sets the Unload FF. This pulse occurs under the following conditions:

1) Power is switched from the off to the on status.
2) Loss of ac and/or dc operating voltages.

As before, the Unload FF must be cleared by moving tape to the load point before any other operation can be executed.

MOVE TO LOAD POINT CIRCUIT (MLP)

The MLP circuit (figure 3-21) is primarily responsible for determining when tape is to be moved forward during a move to load point operation. Two separate situations are discussed: tape initially unloaded, and tape initially loaded.

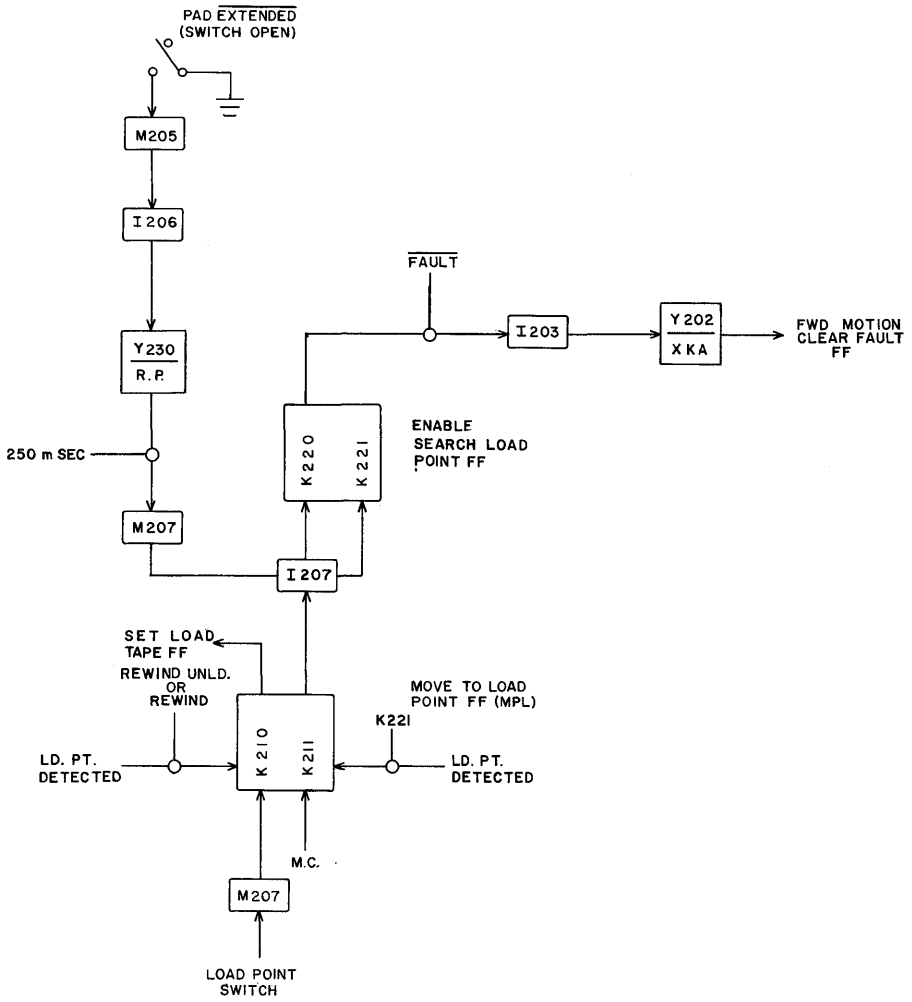


Figure 3-21. Move to Load Point Circuit

A move to load point operation is selected by pressing the Load Point key on the operator's panel. Pressing this key sets K210/211 which performs the following functions:

1) Clears the Unload FF (rewind unload circuit) which turns on the vacuum-pressure pump and capstan motors.
2) Clears the Rewind FF (rewind circuit) which allows the head pad to be extended.
3) Sets K220/221 after the head pad is fully extended (pad switch closed) and the 250 ms delay has been depleted. This delay insures that the head pad has been raised into position so that tape is touching the heads.
4) Partially enables the set input to the Load Tape FF (see load tape circuit). This FF is set and enables forward motion only if tape is to be moved from the unload status to the load point. If tape is already loaded, forward motion is enabled by the output from Y202.

Setting K220/221 results in a "1" output from Y202 which performs a double function. It first clears the Fault FF which was set during the load tape procedure when power was switched from the off to the on status. Secondly, it initiates forward tape motion if tape is not in an unload condition. Thus, if tape is initially loaded, forward motion will be selected by the "1" output from Y202. However, if the tape is initially unloaded, forward motion will be initiated by the Load Tape FF (refer to load tape circuit).

In either case, once motion is selected, tape moves forward until the load point marker is detected and referenced with respect to the heads (see sense load point circuit). Tape motion stops and K210/211 and K220/221 are cleared in preparation for the next move to load point operation.

Note that K210/211 is set when the load point marker is sensed if a rewind operation has been selected. In this case, the circuit allows the load point marker to be located with respect to the photocell even though a load point operation was not selected by pressing the load point key.

LOAD TAPE

The load tape circuit (figure 3-22) allows tape to be moved from an unload status to the load point. The Load Tape FF (K212/213) is set when:

1) Vacuum column photocells indicate that tape is not in the columns (upper photocells lighted) and
2) Load Point key on the operator's panel is pressed.

Ordinarily, no tape in the vacuum columns is sensed as a fault condition which stops tape motion. In this case, however, the Load Tape FF, when set, picks a relay (K104) which causes the upper ports of the pressure differential switches in the vacuum columns to be bypassed to atmospheric pressure. Under normal (no fault) conditions, the upper ports are at atmospheric pressure so this condition is not recognized as a fault. However, even though no fault condition is sensed, the tape is still positioned above the upper ports.

Pressing the Load Point key results in a "1" output from Y202 (move to load point circuit) which:

1) is prevented from initiating forward motion because the Load Tape FF is set. This is necessary since tape has not, as yet, been positioned in the brake region of the columns (between upper and lower photocells).
2) Clears the Fault FF which enables tape to be placed in the supply column (see servo drive control circuit).

When tape has been positioned in the brake region of the supply column, the servo drive control circuit generates a forward motion pulse which is enabled because the Load Tape FF is set. Tape is then moved from the supply column to the take-up column. The Load Tape FF is cleared when tape is placed in the brake region of the take-up column but forward motion continues until the load point marker is located.

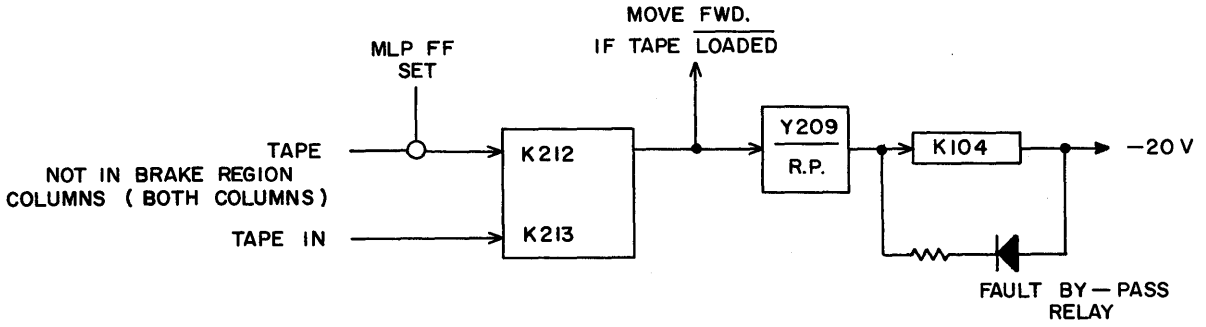


Figure 3-22. Load Tape Circuit

LOCAL CONTROL FLOW CHARTS AND TABLES

Load Tape Operation	Figure 3-23 Table 3-4
Rewind Operation	Figure 3-24 Table 3-5
Rewind Unload Operation	Figure 3-25 Table 3-6

TABLE 3-4. LOAD TAPE OPERATION

STEP	COMMENTS
1	Power, when switched from the off to the on condition, sets the Fault FF and the Unload FF. The Unload FF, when set, turns on the Unload indicators on both the operator's and maintenance panels. Operation then stops until the Load Point key is pressed.
2	Pressing the Load Point key causes the Move to Load Point FF to be set. This FF, when set, initiates the following actions: 1) Clears the Unload FF 2) Sets the Load Tape FF
3A	The Unload FF, when set, energizes relay K3 which performs the following: 1) Applies vacuum to the tape columns which pulls tape into columns. 2) Turns on pressure-vacuum pump and capstan motors (tape does not move at this time because pressure holds tape away from the capstans). 3) Starts to extend the head pad.
3B	The Load Tape FF, when set, indicates that tape has not been placed in the columns. Ordinarily this condition would be sensed as a fault. In this case, however, the upper pneumatic fault ports are bypassed because relay K104 is energized.
4	When the head pad is fully extended and in place, K220/221 is set. This FF, when set, enables tape motion by clearing the Fault FF.

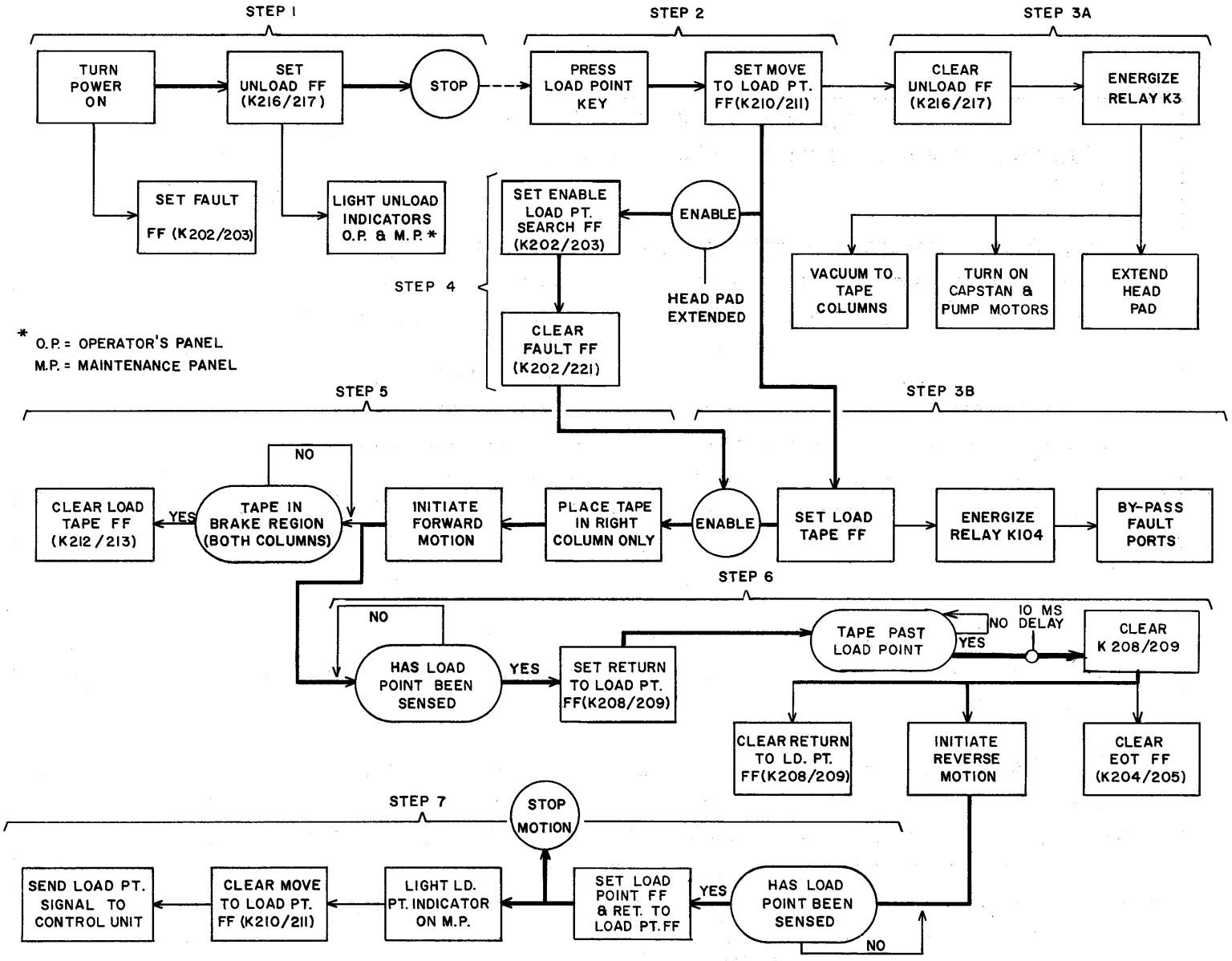


Figure 3-23. Load Tape Operation

TABLE 3-4. CONTINUED

STEP	COMMENTS
5	The Load Tape FF, when set, places tape in the right vacuum column and initiates forward motion by setting the Forward FF in the motion control circuit. Tape is therefore drawn from the right column and placed in the left column. When sufficient tape has been placed in both columns so that the top photocells are covered, the Load Tape FF is cleared. Motion continues, however, until the load point marker is detected.
6	Once motion is selected, tape moves forward until the load point marker is sensed. The Return to Load Point FF is set and tape continues past the load point marker. The Return to Load Point FF is cleared 10 ms later. This FF, when cleared, initiates the following actions: 1) Clears the EOT FF 2) Clears the Load Point FF 3) Stops forward motion and initiates reverse motion
7	Tape moves in the reverse direction until the load point marker is again sensed. The Return to Load Point FF is again set. The Load Point FF is also set and enables the following actions: 1) Stops tape motion 2) Lights the Load Point indicator on the maintenance panel 3) Clears the Move to Load Point FF 4) Returns a load point signal to the TCU indicating that the load point marker has been located.

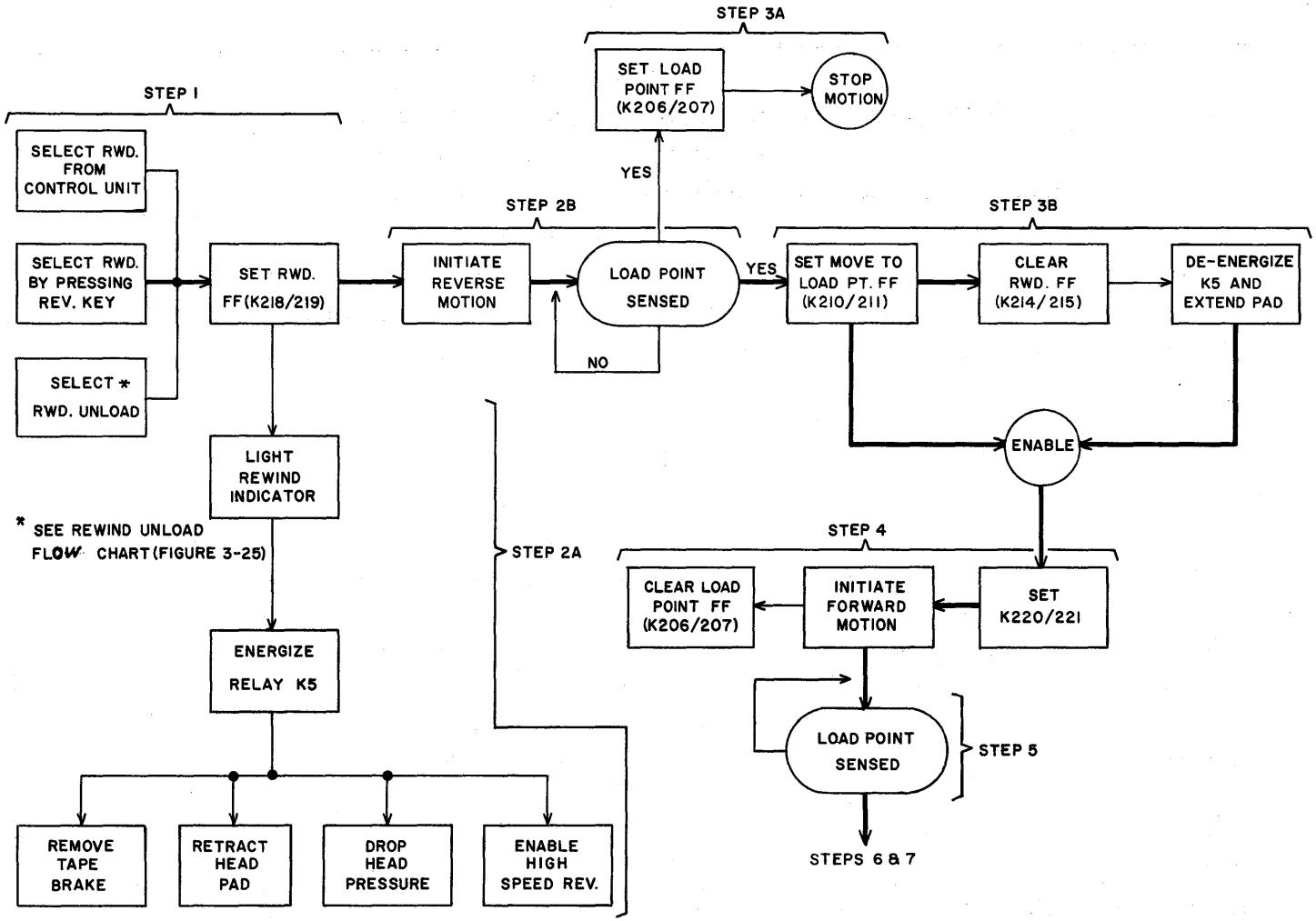


Figure 3-24. Rewind Operation

TABLE 3-5. REWIND OPERATION

STEP	COMMENTS
1	The Rewind FF is set when a rewind operation is selected by the TCU, when the reverse key on the operator's panel is pressed, or when a rewind unload operation is selected.
2A	When set, the Rewind FF lights the Rewind indicator on the maintenance panel and energizes relay K5. This relay performs a variety of functions which include retracting the head pad and enabling a high speed reverse operation.
2B	The Rewind FF, when set, also initiates reverse tape motion by setting the Reverse Motion FF in the motion control circuit. Motion continues until the load point marker is detected which performs the following:
3A	1) Sets the Load Point FF (K206/207) which stops motion by clearing the Motion FF.
3B	2) Sets the Move to Load Point FF which in turn clears the Rewind FF. Relay K5 is de-energized and the head pad is extended.
4	When the head pad is fully extended, K220/221 in the MLP circuit is set. This FF, when set, initiates forward motion and the Load Point FF is cleared 10 ms after the load point marker is moved from the photocell.
5	Forward motion continues until the load point marker is sensed.
6 & 7	Same as steps 6 and 7 in the load tape operation (table 3-4 and figure 3-23).

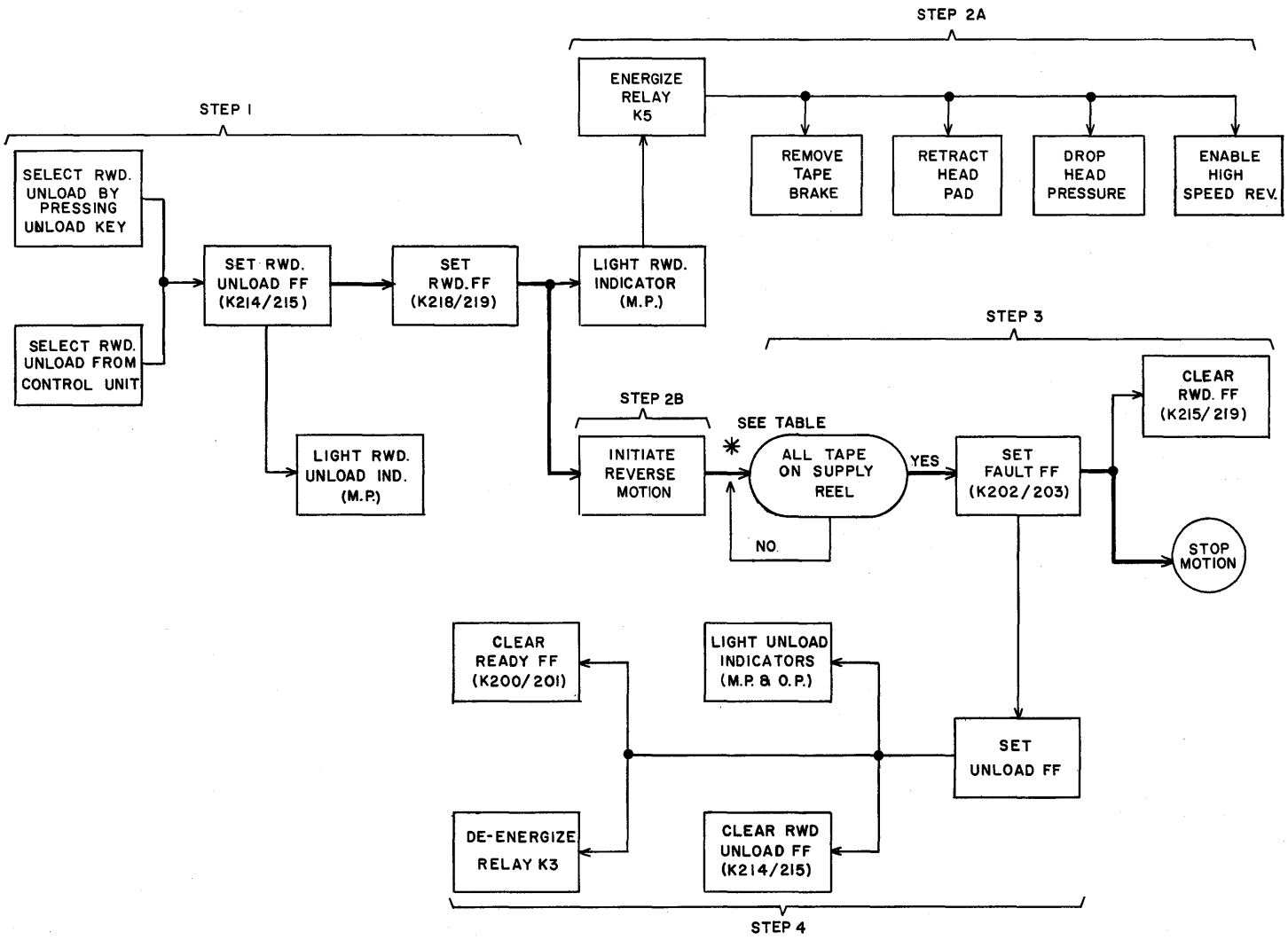


Figure 3-25. Rewind Unload Operation

TABLE 3-6. REWIND UNLOAD OPERATION

STEP	COMMENTS
1	A rewind unload operation is selected by pressing the Unload key on the operator's panel. The operation may also be externally selected by the control unit. In either case, the Rewind and Rewind Unload FFs are both set.
	Setting the Rewind FF results in the following:
2A	1) Lights the Rewind indicator on the maintenance panel and energizes relay K5. This relay retracts the head pad prior to reversing tape and enables a high speed operation.
2B	2) Initiates reverse tape motion by setting the Reverse FF in the motion control circuit. Motion then continues at reduced speed until all tape has been placed on the supply reel.* When the load point marker is detected, tape is stopped and the head pad is extended.
3	When all tape has been placed on the supply reel, the condition is recognized as a fault. The Fault FF is set which: 1) Stops tape motion by clearing the Motion FF 2) Clears the Rewind FF 3) Sets the Unload FF
4	The Unload FF, when set, performs the following functions: 1) Turns on the Unload indicator on the operator's and maintenance panel. 2) Clears the Rewind Unload FF. 3) Clears the Ready FF. Thus, the 606, when in the unload condition, can only be operated from the operator's panel or maintenance panel. 4) De-energizes relay K3 (power supply) which removes vacuum from the tape storage columns and turns off the capstan motors. Because K3 is in series with K4 in the fault circuit, power is also removed from the reels and brakes. The Unload FF remains set until the tape load procedure is executed. Therefore, the tape unit must be placed in the load condition before any other operation can be executed.

TABLE 3-6. CONTINUED

STEP	COMMENTS
*	When the load point marker is detected during a high speed rewind unload operation, the Load Point FF (K206/207) is set. The Move to Load Point FF (K210/211) is also set and applies a clear signal to the Rewind FF. Relay K5 in the rewind circuit is de-energized which disables the high speed operation and allows the head pad to be extended. Because the Rewind Unload FF remains set during this period, the Rewind FF is simultaneously set and cleared resulting in a "0" output from both sides of the FF. (The FF will be stabilized in the clear state when a fault is detected and the Rewind Unload FF is cleared.) While the head pad is being extended, the brake relay pullers in the servo drive control circuit both receive "0" inputs. Thus, both the supply and take-up tape reels are braked. The reverse capstan, however, continues to move tape until the tape is positioned above the left top photocell or below the right bottom photocell. When either condition is reached, tape is separated from the capstan by pressure and motion stops until the head pad is fully extended. The pad, when extended, removes the reel brakes and allows the servo drive circuit to position tape between the photocells. The reverse capstan (which is still selected) now moves tape to the unload condition. Because a high speed reverse was disabled by clearing the Rewind FF, tape speed from load point to unload is less than 150 ips.

Appendix Section

APPENDIX A
THEORY OF CONTROL DATA LOGIC

The basic logic building block is a single inverter transistor circuit, represented on logic diagrams by a rectangle. This circuit uses the 180° phase shift of a grounded emitter amplifier to produce an inversion between input and output. Two circuits may be connected to form a bi-stable flip-flop.

The voltage levels used in the logic are -3v and -0.5v, representing "1" and "0", respectively. The single inverter circuit inverts these signals; a -3v input becomes a -0.5v output, and vice versa.

Control Data logic circuits are mounted on 2 1/2 by 2 1/8 inch printed circuit cards (figure 1). Each card is equipped with a 15-pin male connector for plugging into the equipment chassis.

The logic cards used are Single Inverter, Double Inverter, and Flip-Flop, designated 10 series, 20 series, and 30 series, respectively. The second digit denotes the number of inputs to each circuit.

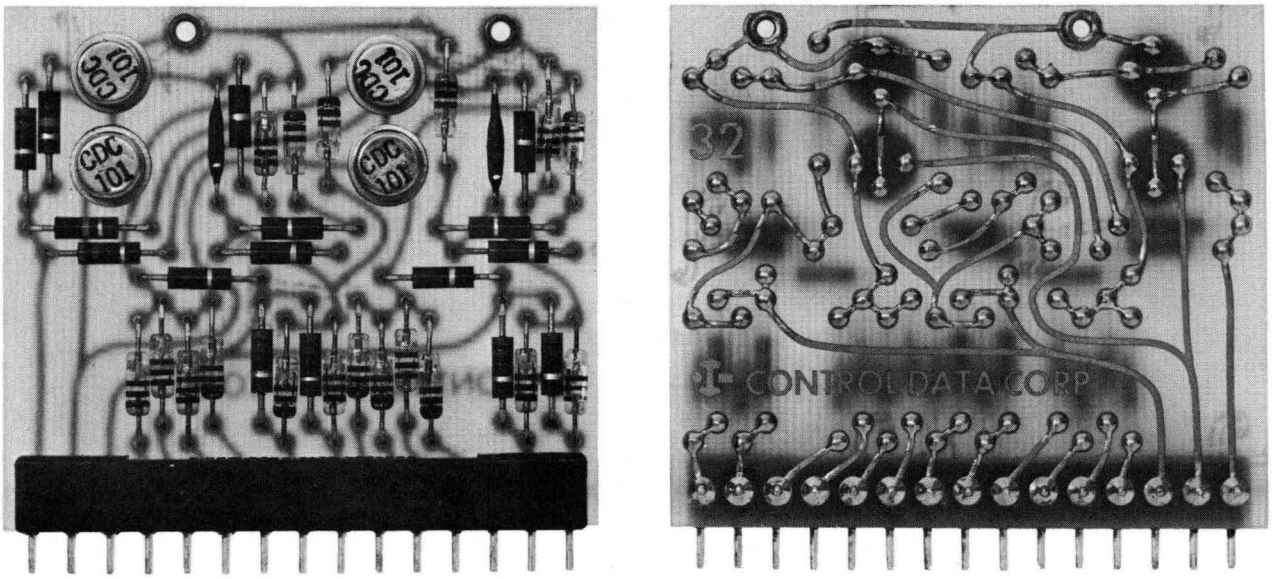


Figure 1. Control Data Printed Circuit Card

For example, a 14 card is a single inverter with 4 inputs. A 22 card contains two separate inverter circuits, each having two inputs. A 31 card contains two inverter circuits connected to form a flip-flop, each circuit having one input.

On a 20 or 30 series card, the circuits are designated Circuit A and Circuit C. In numbering components and designating circuit locations, a diode might be numbered CR12A or CR12C; a location might be written R76A or R76C, where R refers to the chassis row, 76 to the connector number, and A or C to the circuit.

ANALYSIS OF SINGLE INVERTER

In the standard inverter circuit shown in figure 2, transistor Q01 is connected as an emitter-follower; Q02, as an amplifier. The collector circuits of the transistors have two feedback loops which prevent the transistors from being driven to cutoff or saturation. Switching from one state to the other is accomplished in 50 to 100 nanoseconds.

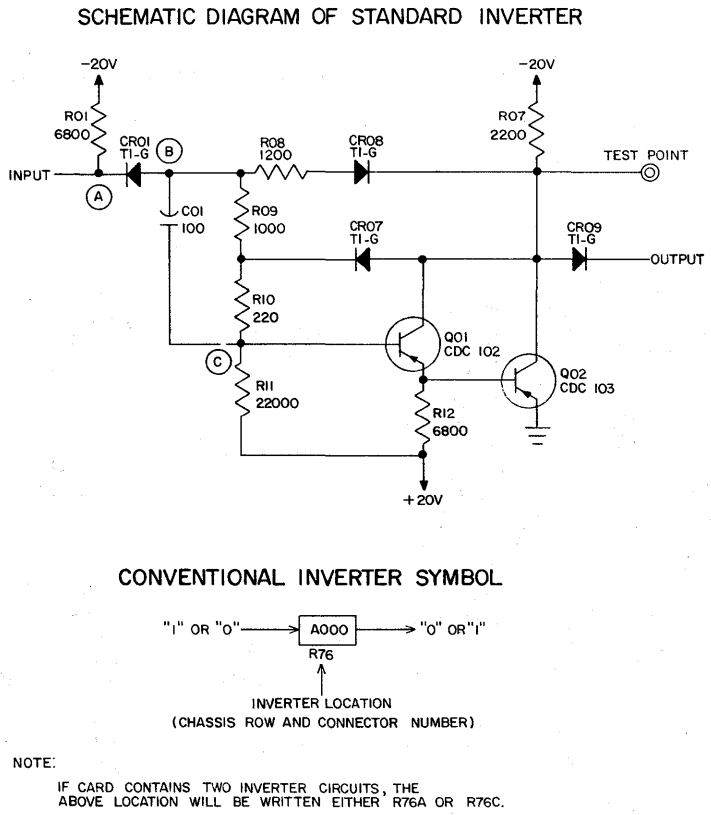


Figure 2. Standard Inverter Circuit

An input signal is applied through isolation diode CR01 to a voltage divider network composed of resistors R07, R08, R09, R10, and R11. An input signal of -0.5v (point A) results in -1.5v at point B and +0.8v at the base of Q01 (point C) so that Q01, and consequently Q02, do not conduct. CR01 is biased 1v in the backward direction to provide for noise suppression at the input of the inverter. Capacitor C01, between CR01 and the base of Q01, provides rapid coupling of input signal changes to Q01, improving the switching time of the circuit.

An open input circuit has the same effect as a -3v signal; point A is biased at -3v and CR01 conducts. Thus, a voltage of -1.1v appears at the base of Q01, causing both transistors to conduct.

Transistors Q01 and Q02 each provide beta* current gains of approximately 100; loop gain of the two transistors is on the order of 10^4. The collector current of Q01 and Q02 develops the output voltage across resistor R07. Output diode CR09 isolates the output line from the other output lines.

Diodes CR07 and CR08 form the feedback loops which prevent transistors Q01 and Q02 from being driven to cutoff or saturation. The positive-going limit allows a maximum transistor conduction that is less than saturation; the negative-going limit fixes a minimum conduction for the transistors.

When the transistors approach cut-off, their collectors approach -3.0v. The collector potential is coupled back to the base of Q01 through CR08, R08, R09, and R10. The base of Q01 is always held at a sufficiently negative voltage to permit some minimum conduction of Q01 and thus Q02.

When the transistors approach saturation, the collectors approach 0v. The collector potential is coupled back to the base of Q01 through CR07 and R10. The base of Q01 is thus prevented from becoming so negative that saturation occurs.

---

* The beta current gain is the ratio of collector current to base current.

FLIP-FLOP (FF)

A FF is two single inverter circuits interconnected as shown in figure 3. (each rectangle represents a single inverter). One of the inverters is the set side of the FF; the other, the clear side. The FF is placed in the "1" (set) state by a set input that is "1". It is placed in the "0" (cleared) state by a clear input that is "1". (Set and clear inputs are never "1" at the same time.)

The storage capability of a FF means that it remains in a state that is indicative of the last "1" input received. Specifically, if a "1" pulse is present at the set input, then the output of inverter K000 (figure 3) becomes "0". This output is applied as an input to K001 and the output becomes "1". The output of K001 is fed back to K000. When the set input returns to "0", the feedback connection between K000 and K001 permits the storage of the state to which the "1" pulse on the set input forced the FF. If the clear input later receives a "1" pulse, the output of K001 becomes "0", and the feedback input to K000 is "0". K000 furnishes a "1" output which is returned to K001 to replace the "1" pulse at the clear input.

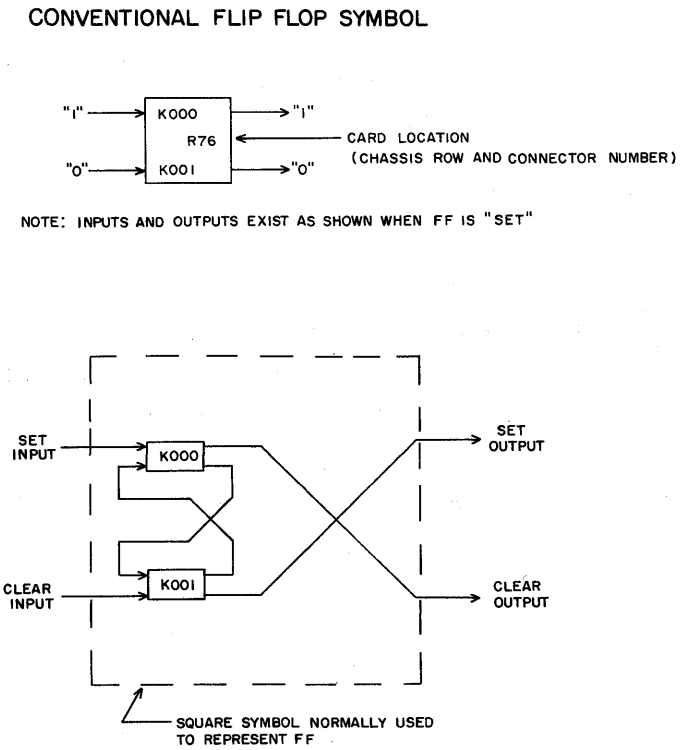


Figure 3. Interconnection of Inverters to Form a FF

When the FF is set, K001 has a "1" output, and K000 has a "0" output. When the FF is cleared, K001 has a "0" output, and K000 has a "1" output.

The conventional square symbol for a FF is used in figure 3 to show the relationship between it and the inverter configuration which forms the FF. The square which represents the FF encompasses the crossover of the outputs.

AND CIRCUIT

A three-input AND circuit is shown in figure 4. The AND gate requires all inputs to be "1". If any are "0", a "1" on another input will not be sensed.

If the transistors on cards A, B, and C are not conducting, their output diodes are biased in the reverse direction, and the resulting output signals are interpreted as being at the logical "1" level. The circuit on card D places a negative voltage on the base of the transistor so that it conducts.

If the transistor on card A, B, or C is conducting, its collector goes to approximately ground potential. Its output diode is biased in the forward direction from the -20v source on card D, and the transistor on card D is held in the non-conducting state.

OR CIRCUIT

A three-input OR circuit is shown in figure 5. An OR gate allows a "1" signal on any input to be sensed, although a "0" signal may simultaneously appear on another input. The input lines are separated by diodes; a -3v signal will not be nullified by a -0.5v signal on another input lines.

If the transistor on card A, B, or C is not conducting so that the card has a "1" output, the input circuit on card D will apply a negative voltage to the base of the transistor on card D, causing it to conduct.

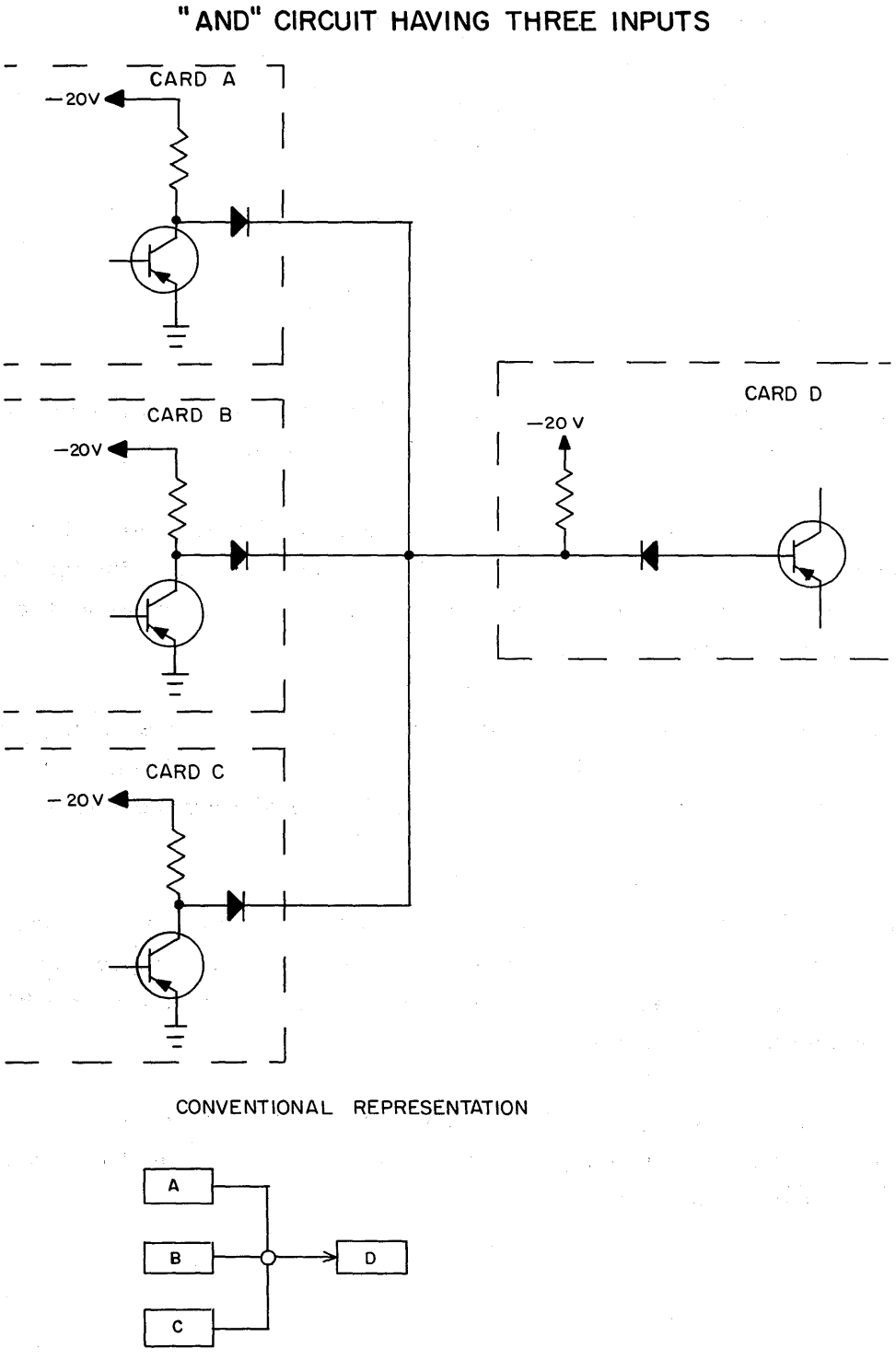


Figure 4. AND Circuit

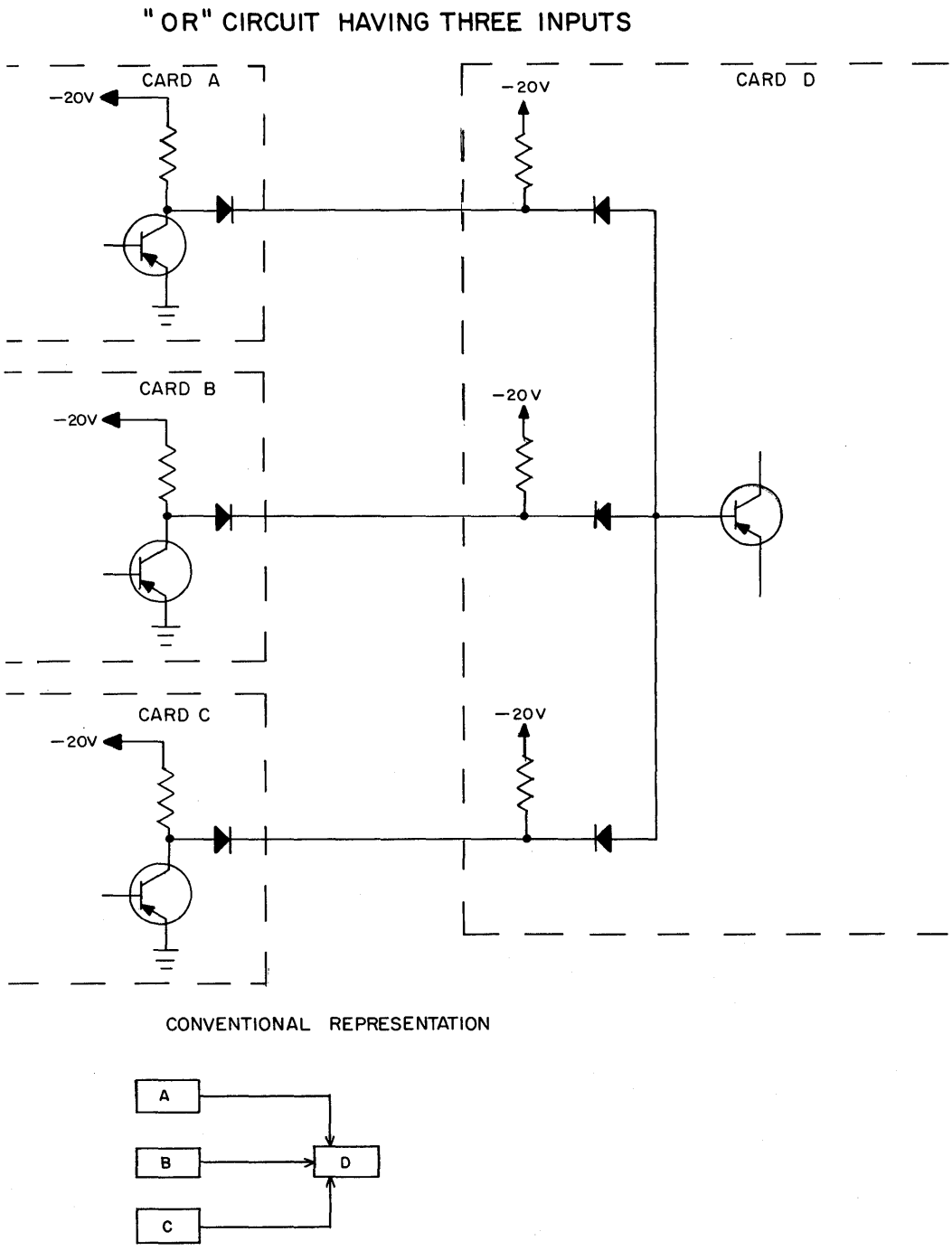


Figure 5. OR Circuit

BASIC THREE-STAGE COUNTER

A counter is essentially a double rank register which increases or decreases the quantity stored, an increment at a time. The three-stage counter circuit shown in figure 6 is additive from binary 000 through 111.

A count is stored in two steps:

1) A "1" input on the advance line consecutively sets a FF in rank 1. When all three are set, the next input clears them.

2) A "1" input on the transfer line causes the FFs in rank two to assume the same state as the corresponding FFs in rank 1.

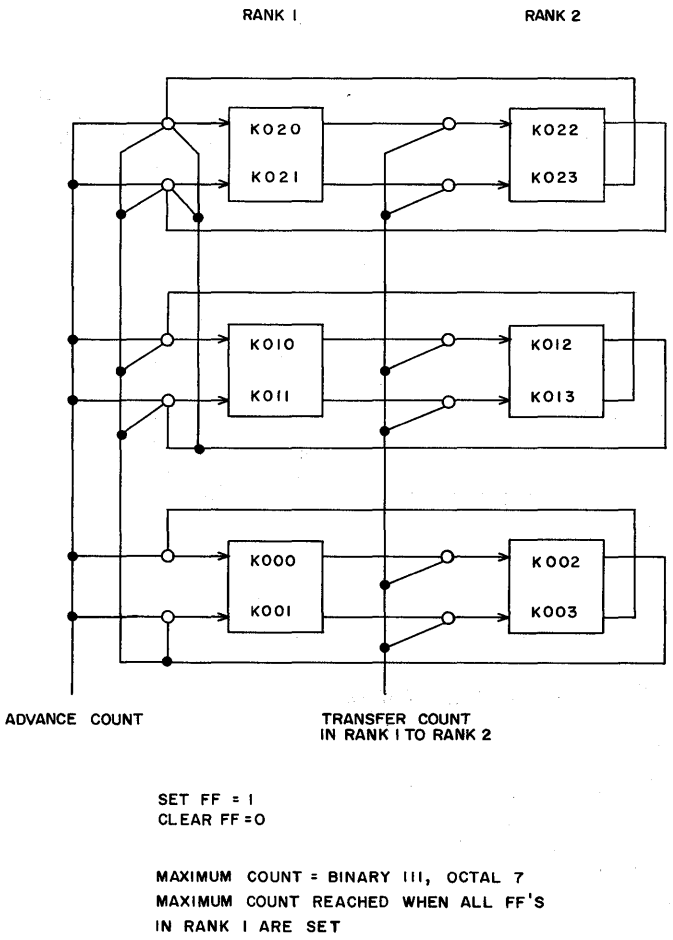


Figure 6. Three-Stage Counter

To analyze the operation of the counter, assume that both ranks are initially cleared; the count stored is zero. The first advance command finds the AND gate to K000 enabled and therefore enters the count 001 (octal 1) into rank 1. This partially enables the AND gate to K002. The transfer command enters the count 001 into rank 2. The next advance command finds the AND gate to K001 and K010 enabled and enters the count 010 (octal 2) into rank 1. The operation continues as shown in table 1, until the count reaches 111 (octal 7), which is the highest possible count in a three-stage counter. A command sequence returns both ranks to count 000.

TABLE 1. COUNTING SEQUENCE FOR THREE-STAGE COUNTER

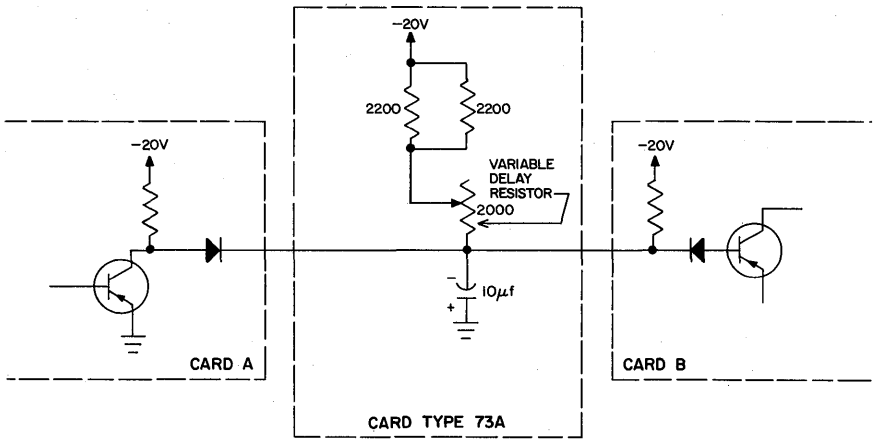
Command	Quantity Stored (Octal)	Rank 1			Rank 2		
		K02-	K01-	K00-	K02-	K01-	K00-
Initial conditions	0	0	0	0	0	0	0
Advance	1	0	0	1	0	0	0
Transfer		0	0	1	0	0	1
Advance	2	0	1	0	0	0	1
Transfer		0	1	0	0	1	0
Advance	3	0	1	1	0	1	0
Transfer		0	1	1	0	1	1
Advance	4	1	0	0	0	1	1
Transfer		1	0	0	1	0	0
Advance	5	1	0	1	1	0	0
Transfer		1	0	1	1	0	1
Advance	6	1	1	0	1	0	1
Transfer		1	1	0	1	1	0
Advance	7	1	1	1	1	1	0
Transfer		1	1	1	1	1	1
Advance	0 (or 8)	0	0	0	0	0	0
Transfer		0	0	0	0	0	0

DELAY CIRCUIT

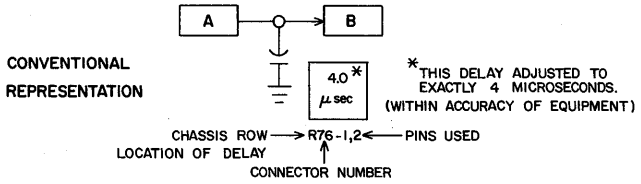
Placing a capacitor from the signal line to ground forms a delay circuit. The delay time is the time required to charge the capacitor when a -3v "1" signal appears on the line.

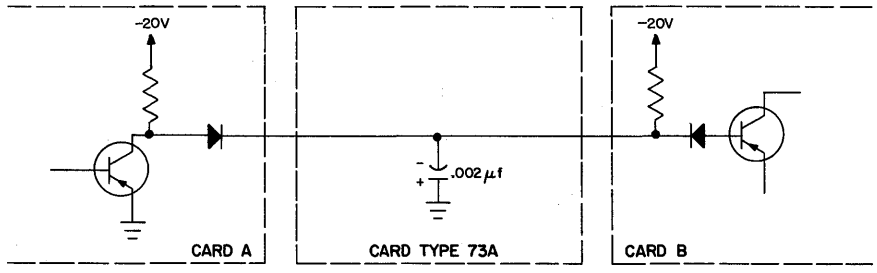
A delay is used to postpone the time at which a "1" signal is sensed by the input circuit of a card. It will have negligible effect on a "0" signal.

During the time that the transistor on card A is conducting, its collector will be at almost ground potential (figure 7). The voltage across the delay capacitor will not be more than 0.5v, and will contain very little charge.



TYPICAL ADJUSTABLE DELAY INSTALLATION





TYPICAL NON-CRITICAL DELAY INSTALLATION

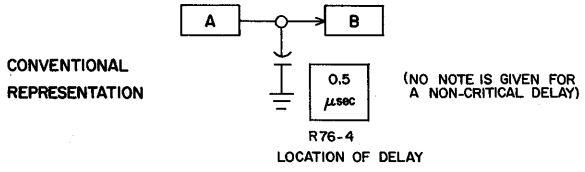
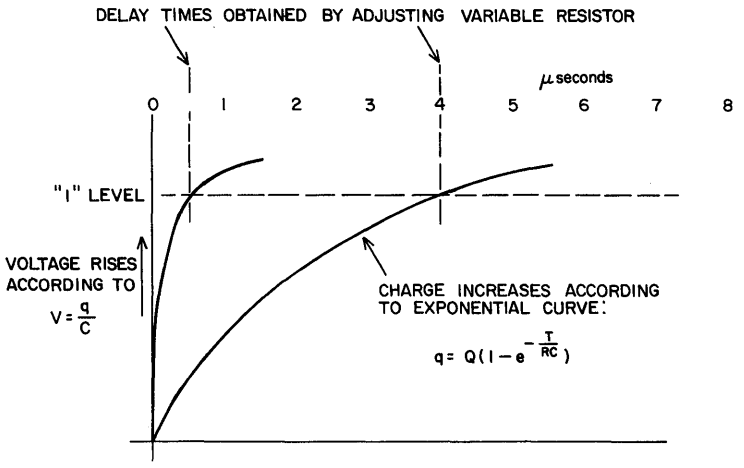


Figure 7. Typical Delay Circuits

When the output of card A switches to "1" and its transistor stops conducting, the input circuitry on card B attempts to bias the input line at the -3v level. Initially this voltage is absorbed by the uncharged delay capacitor, which gradually obtains a charge as shown in figure 8. In the case of an adjustable delay, the capacitor also receives charging current from the circuit on the 73A card.

The size of the capacitor and the rate at which it receives charging current govern the delay time. For a long delay, use a large capacitor. To increase or decrease the delay time, increase or decrease the series resistance between the capacitor and the source of charging current.



NOTE:

SYMBOL	REFERS TO:	UNITS
T	TIME	SECONDS
q	PARTIAL CAPACITOR CHARGE	COULOMBS
Q	FINAL CAPACITOR CHARGE	COULOMBS
R	SERIES RESISTANCE	OHMS
C	CAPACITANCE	FARADS
V	APPLIED POTENTIAL	VOLTS
e	NATURAL LOGARITHM BASE	PURE NUMBER 2.718, APPROX.

Figure 8. Relationship of Delay Time and Capacitor Charge Time

PULSE FORMING NETWORKS

Many circuits contain pulse forming networks, consisting of two inverters and a capacitive delay to reshape a steady "1" signal into a short "1" pulse. The leading edge network produces a pulse upon receipt of a "1" signal; the trailing edge network produces a pulse when the "1" signal ends (figure 9).

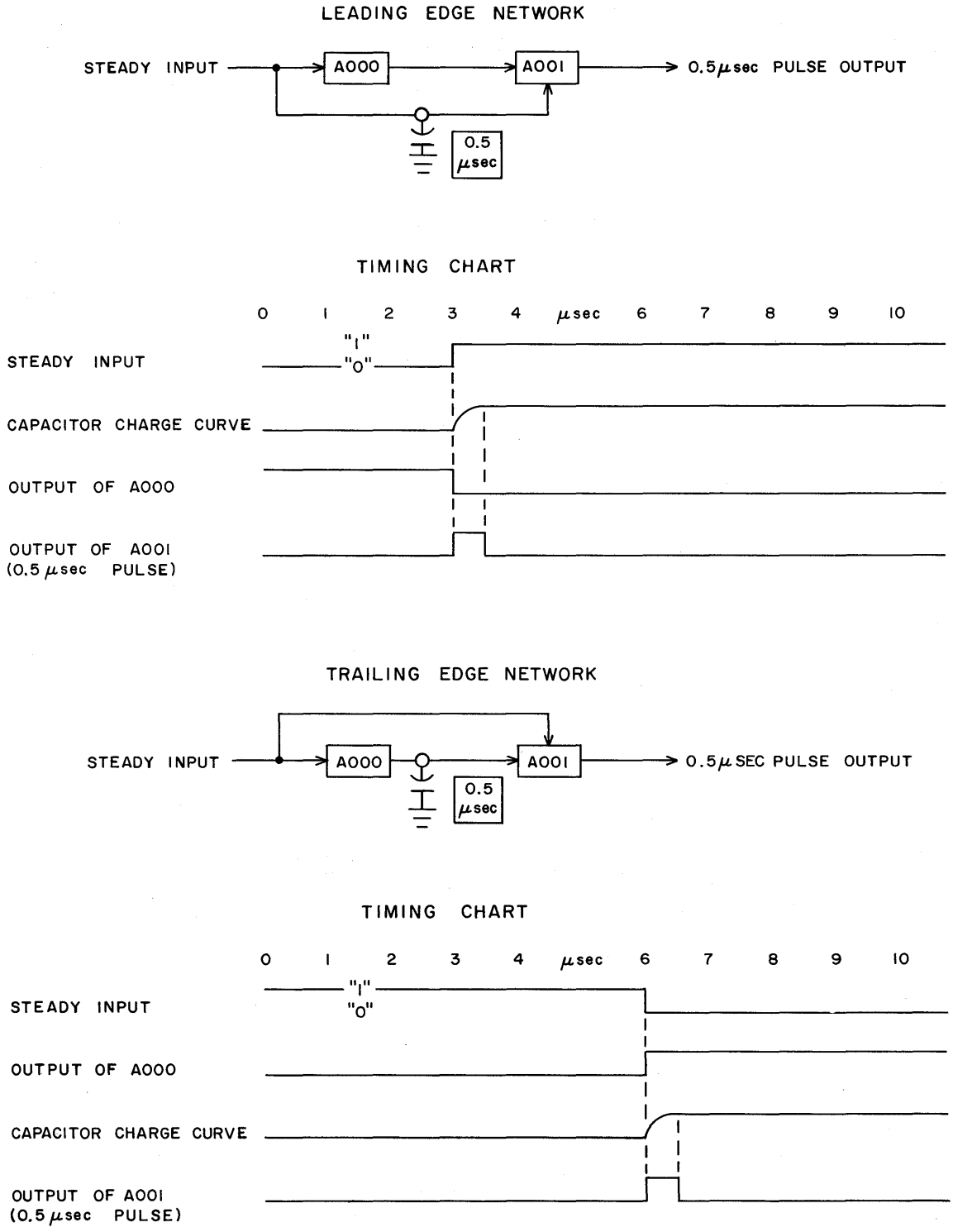


Figure 9. Pulse-Forming Networks

When a "1" input is received by a leading edge network, double inversion produces a "1" output. When the capacitor is sufficiently charged, a "1" is sent directly into A001 through an OR gate, and the output of inverter A001 switches to "0".

In the case of a trailing edge network, the steady input signal is fed directly into both inverters. When this signal goes to "0", the output of both inverters switches to "1". The "1" output of A000 does not reach A001 until the capacitor has charged sufficiently. The "1" enters A001 through an OR gate, and its output switches to "0".

TIMING CHAIN PULSE GENERATOR

A convenient method of obtaining a series of four sequential pulses using two FFs and three delays is shown in figure 10.

The two FFs exhibit four distinct sets of conditions at different time intervals. Initially both are in the clear state. A "1" pulse input to K000 sets K000/001, so that K001 has a "1" output. After a brief delay, this signal sets K002/003. K003 sends a "1" through a delay to K001; K000/001 is cleared. K000 sends a "1" through the third delay to K003; K002/003 is also cleared.

These four sets of conditions and the times at which they occur are:

	K000/001	K002/003
Time 0	Clear	Clear
Time 1	Set	Clear
Time 2	Set	Set
Time 3	Clear	Set
Time 0 (or 4)	Clear	Clear

The lengths of these time intervals are dependent upon the capacitive delays. In the example show, all of the times are 0.5 usec. These may be varied.

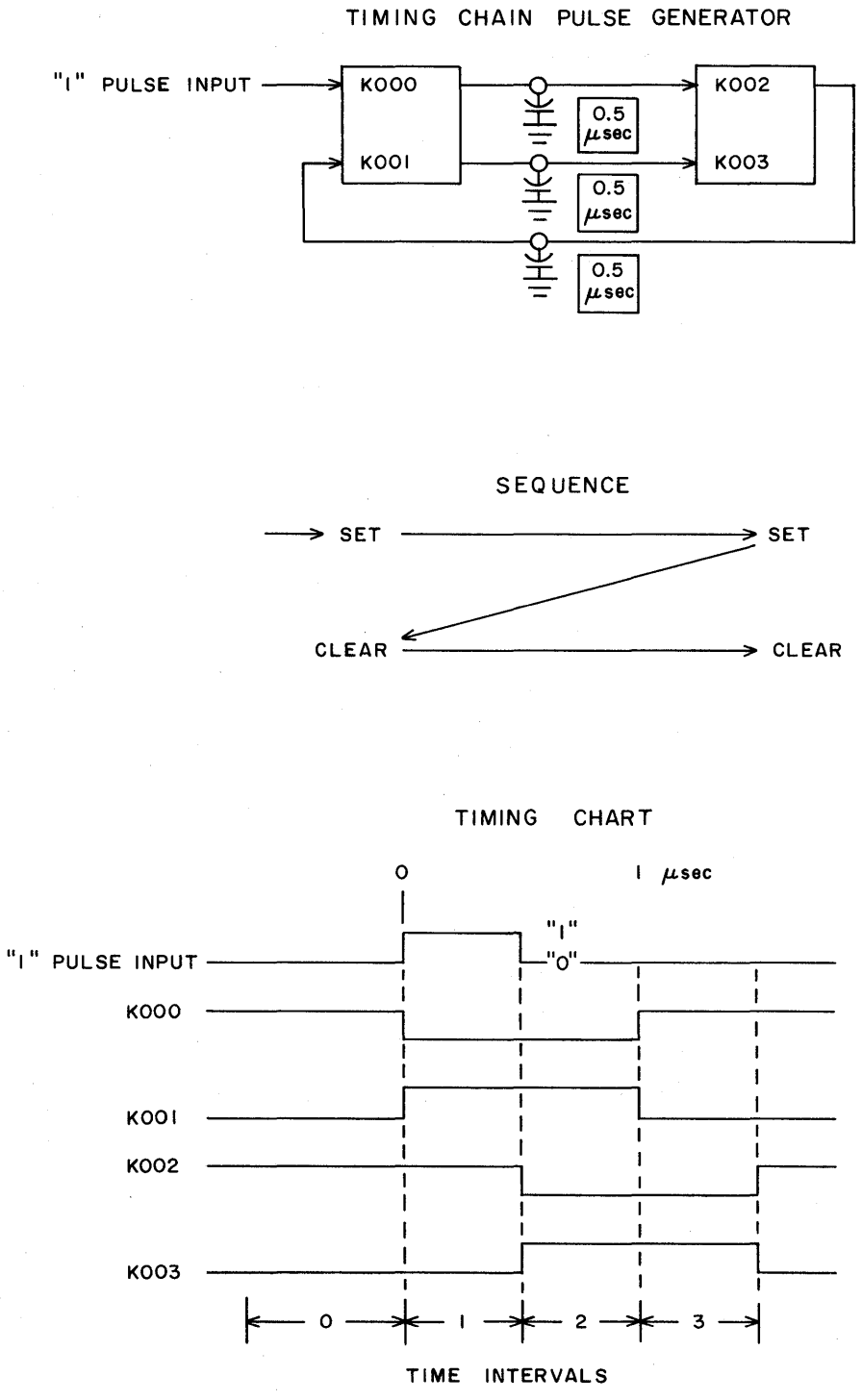


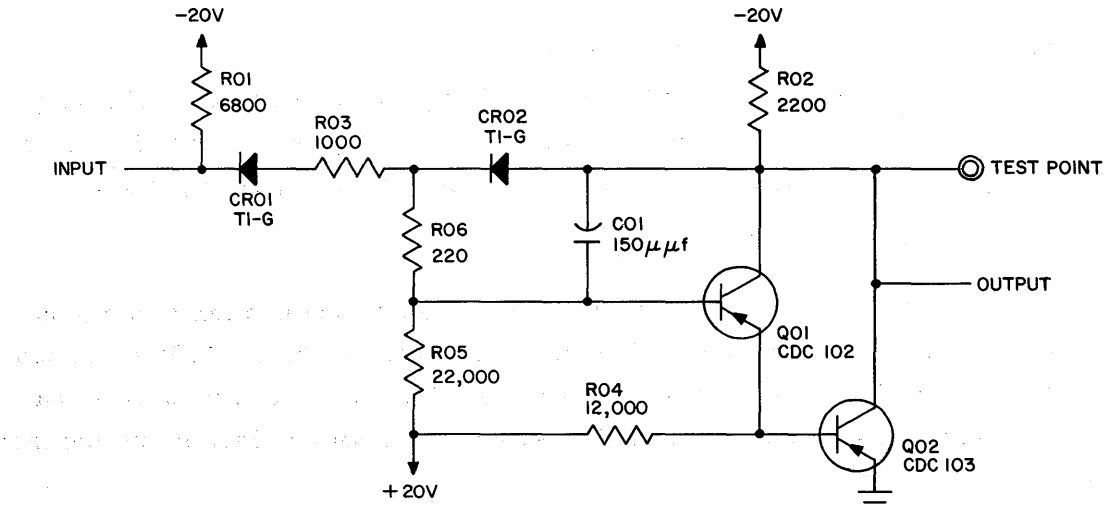
Figure 10. Pulse Generator Networks

OUTPUT/INPUT CARDS, L--- AND M--- SERIES

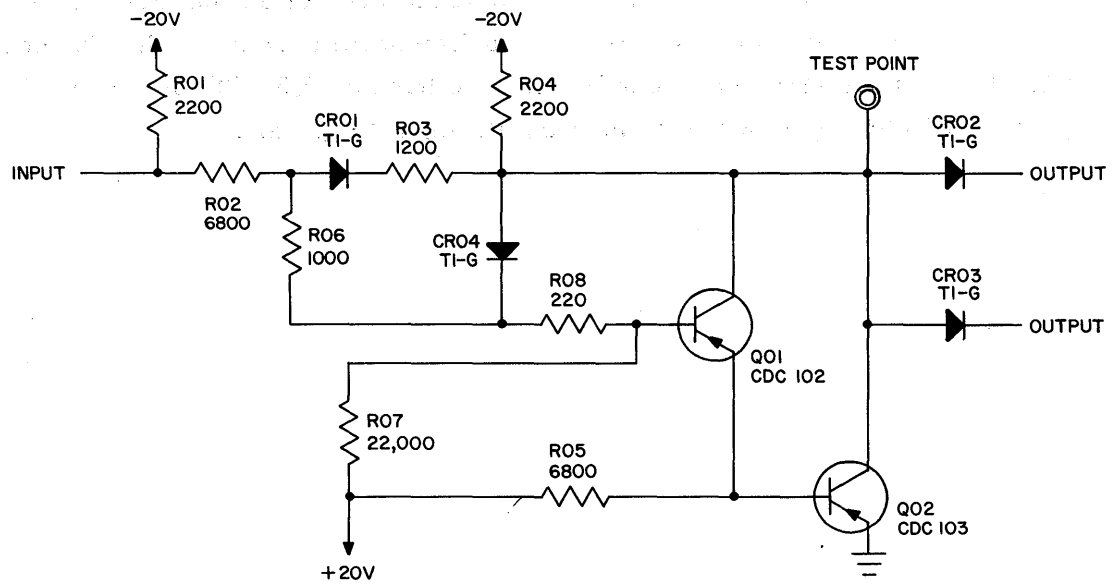
The output/input cards adapt the relatively low level logic voltages to the relatively high level voltages necessary for cable transmission. Card types 62 and 61, which perform this adaptation, contain three separate circuits per card, A, B, and C (figure 11).

These cards are similar to a standard inverter card in that they contain a common emitter transistor circuit. However, although these cards produce a 180° electrical phase shift, they do not function as logical inverters. Instead, they are used in pairs so that the total phase shift is 360° and the initial and final voltage levels are identical (figure 11).

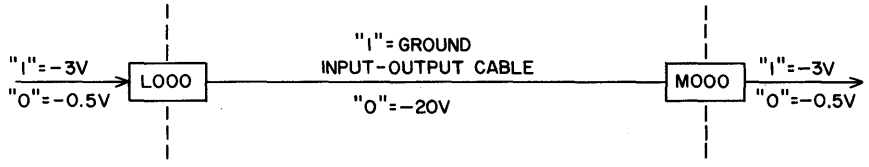
Another similarity between an M--- card and a standard inverter is the fact that the card circuitry biases the transistors in their conduction state if an open circuit occurs on the card input. Thus an M--- card can be made to have a -0.5v "0" or a -3v "1" output by opening and closing a switch connecting its input to ground.



L--- OUTPUT CARD TYPE 62



M--- INPUT CARD TYPE 61



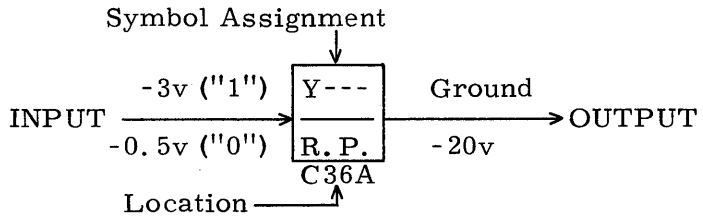
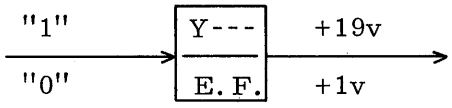
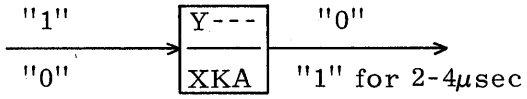
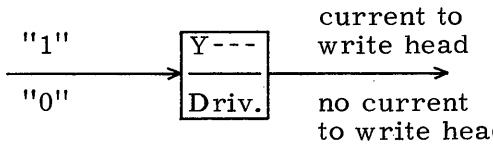
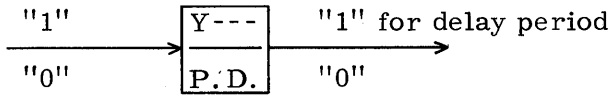
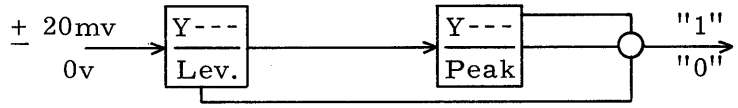
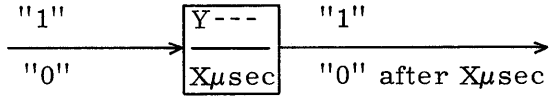
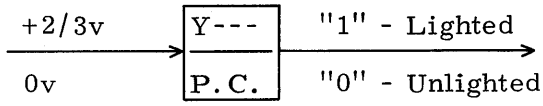
CONVENTIONAL REPRESENTATION

Figure 11. Input/Output Circuits

APPENDIX B

SPECIAL PURPOSE CIRCUITS

The special purpose logic circuits used in the 606 are mounted on standard 2 1/2 by 2 1/8 inch printed circuit cards equipped with 15-pin male connectors. Each special purpose card is given an alphabetic designation and is represented logically by a small square.

NAME	TYPE	LOGICAL REPRESENTATION
Relay Puller	IAA	
Power Emitter Follower	IBA	
Counter Differentiator	XKA	
Write Driver	IIA	
Adjustable Pulse Delay	UCB	
Level Detector	EDA	
Peak Detector	ODA	
Adjustable Delay	UAA	
Photocell Amp.	OAA	

RELAY PULLER (IAA)

This circuit drives the high current or inductive loads which operate relays or large capacitance or peak loads such as lamps. It is particularly useful in driving loads up to 0.6 amp which are terminated at negative voltages from -5v to -50v.

The relay puller circuit can also be used as an L--- card. The input-output voltage levels are the same for both cards.

"1" (-3v) → Y--- R.P. → "1" (Ground)
"0" (-0.5v) → "0" (-20v)

"1" (-3v) → L--- → "1" (Ground)
"0" (-0.5v) → "0" (-20v)

The input stage of the relay puller circuit (figure 1) has its transistor connected as an emitter follower with the collector returned to -20v through a limiting resistor, R03. The first stage emitter follower current does not flow through the load as it does in circuits such as the 55 card. The only current flowing to the load in the turn off condition is the leakage current of the output transistor. The circuit limits collection voltage on Q01 to -20v; Q02 may have excursions to -50v. Turn-on time is 5μsec maximum and turn-off switching is 25μsec maximum.

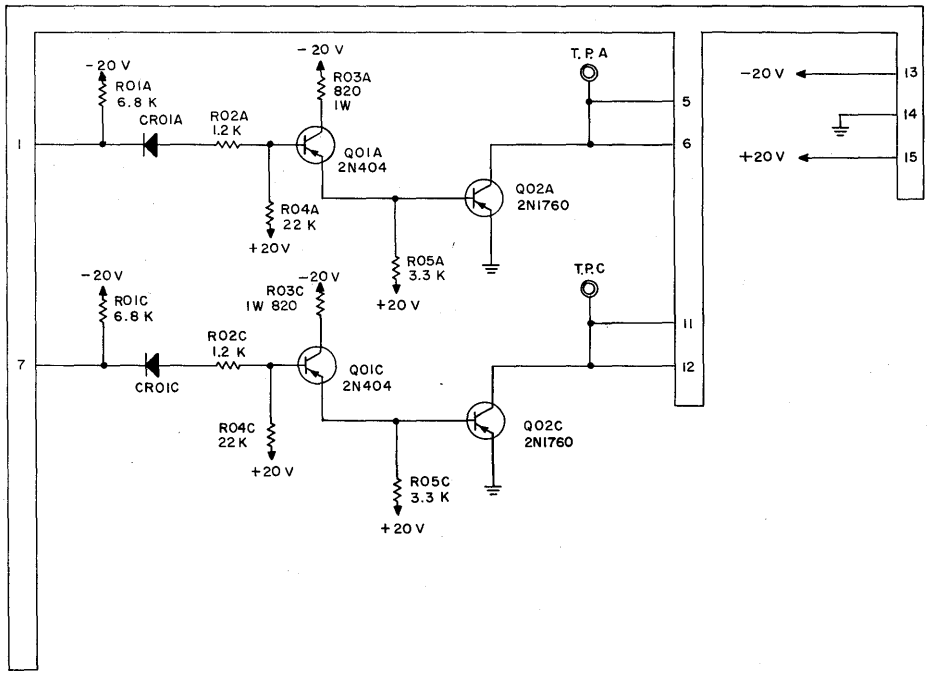


Figure 1. IAA - Relay Puller

POWER EMITTER FOLLOWER (IBA)

This circuit (figure 2), used with a solid-state H switch (capstan drive circuit), drives diagonally opposite legs of the switch. A separate card of this type drives a switching transistor which provides a 2 ms double magnitude current pulse to reduce actuation time.

The circuit differs from the regular inverter circuit in two ways:

1) The emitter follower is in the second stage instead of the first.
2) The output load is returned to +20v instead of -20v.

Turn on time varies from 1 to 20μsec with the current limiting resistor output connected to +20v. Turn off switching ranges from 5 to 50μsec.

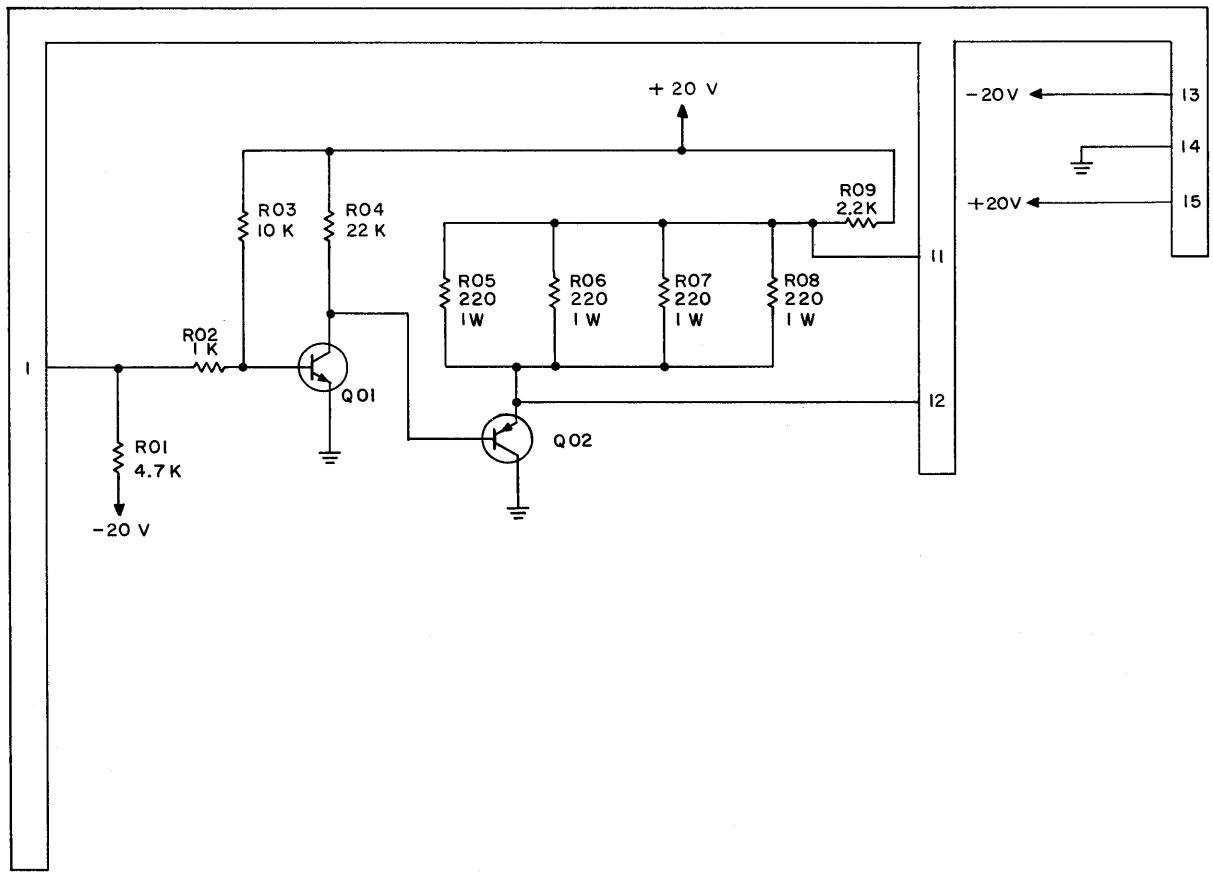


Figure 2. IBA, Power E.F. (+20V)

COUNTER DIFFERENTIATOR (XKA)

This card (figure 3) operates as a single pulse generator with a circuit normally switched to a "0" on the output. When one of the two inputs changes from "1" to "0" within 10μsec, the card provides a "1" output for 2 to 4μsec. If either input returns to a "1" while the output is a "1", the output will switch to a "0" within 0.5μsec.

The circuit consists of an inverter stage followed by a RC differentiating circuit and an emitter follower output.

The input stage is similar to a two input inverter without the speed up diode and emitter follower in the circuit. The negative excursion on the output of the first stage equals -6v instead of the usual -3v. This compensates for attenuation in the RC differentiator.

The variations in the emitter follower (Q02) or the number of loads connected to the output have only a second order effect on the RC time constant. The time constant depends almost entirely on the values of R07 and C01. R07 also limits the base drive and saturation.

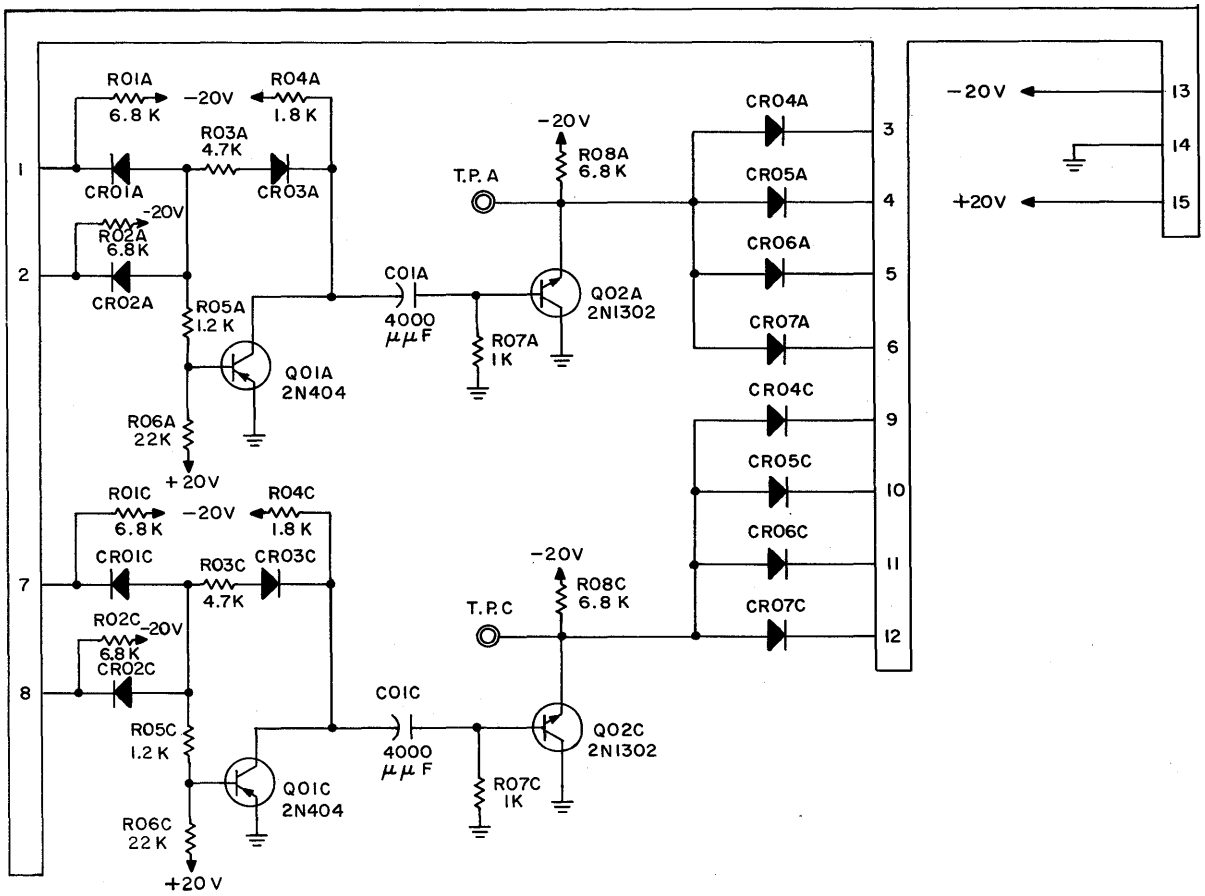


Figure 3. XKA, Counter Differentiator

WRITE DRIVER (IIA)

The write driver circuit (figure 4) develops the current applied to the write heads during a write operation. Each card contains two independent drive circuits whose outputs are connected to opposite ends of the windings of the write head.

The circuit consists of transistor Q01, connected as an emitter follower, and transistor Q02 and Q03, connected in parallel as amplifiers. A "0" input results in 0v at the base of Q01. The emitter of Q01 is clamped to ground by CR03; neither Q02 nor Q03 conduct. Consequently, no current flows to the output pin.

A "1" input signal causes Q01 to conduct; conduction is held below saturation by feedback diode CR01. The negative voltage applied to the bases of Q02 and Q03 causes these transistors to conduct. Current, therefore, flows through the emitter of Q02 and Q03 to the collector and then to the output pin.

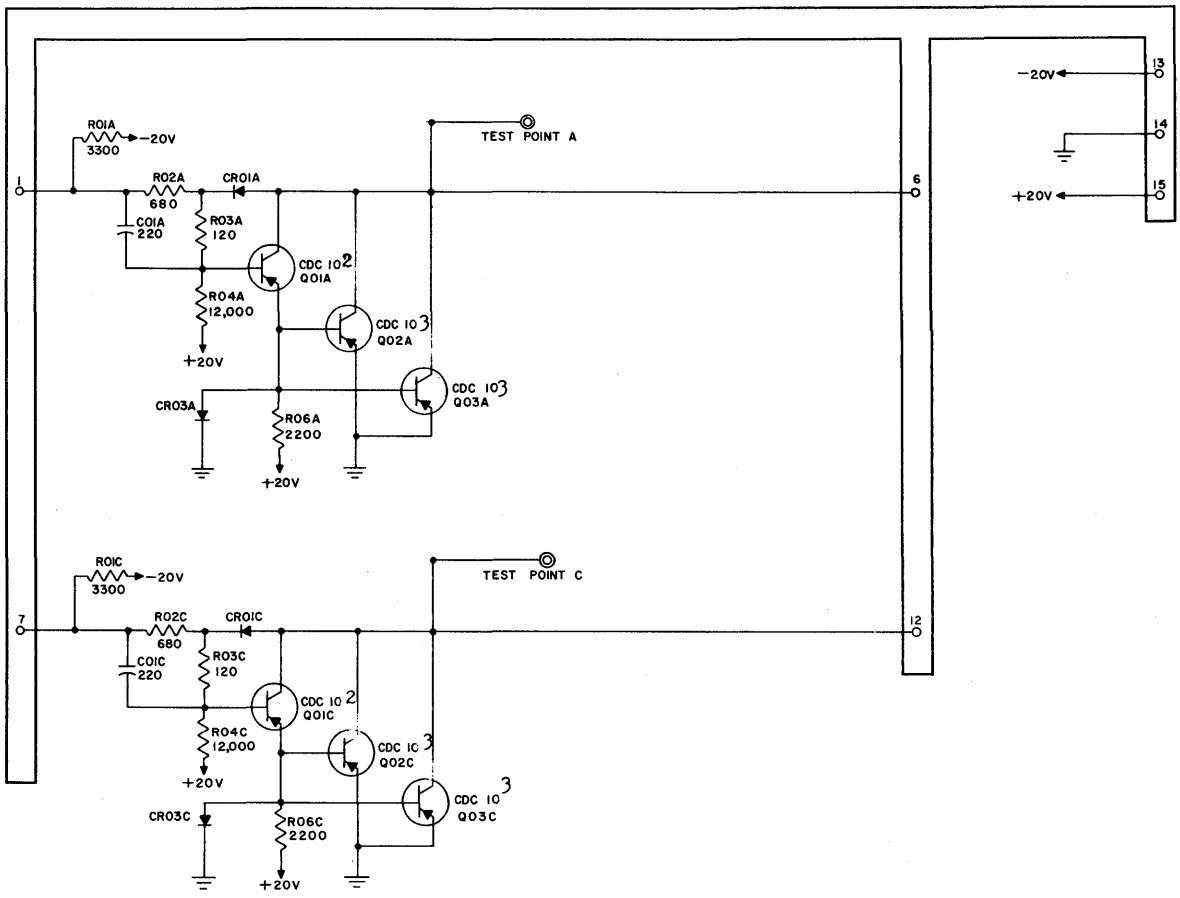


Figure 4. IIA, Write Driver

ADJUSTABLE PULSE DELAY (UCB)

The pulse delay card (figure 5) is used as a read and write skew adjustment which compensates for mechanical misalignment of head gaps and small switching delays or phase lags in the electronic amplifiers. The card produces a narrow output pulse after a short adjustable delay (1 3/4 - 5μsec). A recycle time of 5μsec is necessary for delays to equal 95% of the specified delay period.

The circuit is divided into three sections. Section A is a one shot multivibrator circuit composed of Q01A and Q02A. Themultivibrator is triggered by a negative input signal passing through a differentiating network to the base of Q01A. Conduction of Q01A couples a positive pulse to the base of Q02A and causes it to switch off. Multivibrator regeneration is completed by the common emitter resistor (R11A). The period of the multivibrator is determined by R08A, C02A, and voltage on the movable arm of R06A. Recycle time is determined by resistors R06A and R07A and capacitor C02A. Q02A is a high gain transistor which provides reserve output current for the limited base drive available in the circuit. Diode CR05A supplies the additional emitter current necessary for the collector load of Q02A, and references the emitter to near ground for this stable state of the multivibrator. During the multivibrator period, CR05A is reverse biased, permitting the gain of the two transistors to be utilized through a common emitter resistance (R11A) providing fast fall and rise times.

Circuits B and C are simplified inverter circuits which use a high frequency transistor to decrease switching time. Circuit C also uses a delay capacitor (C01C) which allows the positive output to be delayed permitting ANDing with the output of Circuit B for a 3/4μsec pulse output.

The three circuits are not connected internally and may be used as separate and complete elements. The circuits may also be connected through external jumpers as shown in figure 6 to provide a delay output pulse from a negative input.

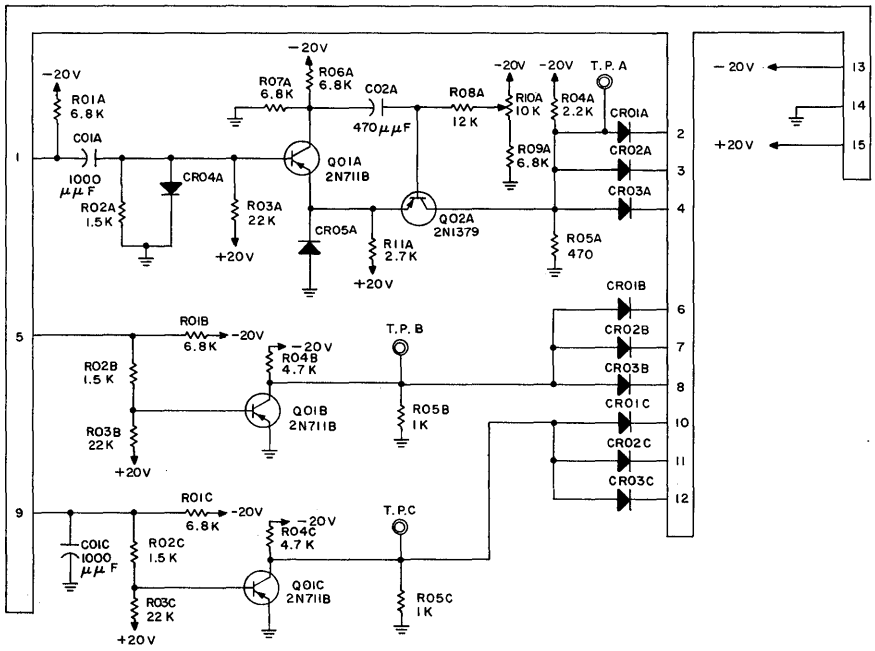


Figure 5. UCB, Adjustable Pulse Delay

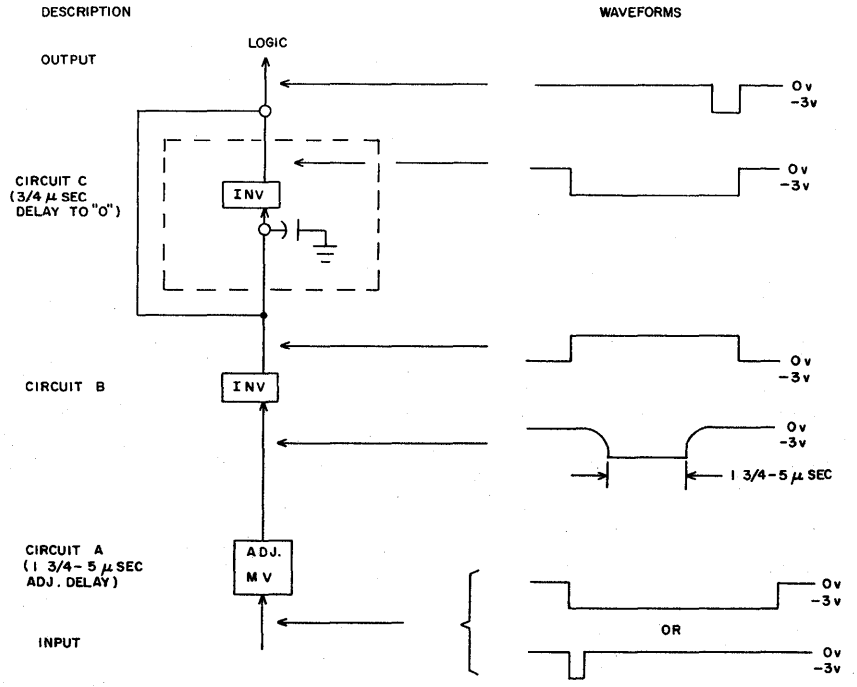


Figure 6. Adjustable Pulse Delay Waveforms

LEVEL DETECTOR (EDA)

The level detector (figure 7) is used in the read data circuit to preamplify, rectify, and detect NRZ1 information on magnetic tape. Three outputs are provided:

1) A class A low impedance output which provides a gain of 125. Gain may be increased to 190 by means of an external jumper from ground to pin 3.
2) A rectified signal derived from the class A signal which exceeds a threshold of 2 volts peak to peak. The rectified signal is increased by a factor of 2 from the class A signal for portions in excess of the threshold point. (The threshold may be reduced to 1.1v by means of an external jumper from ground to pin 7.)
3) A "1" output provided by a switching circuit operating from the threshold point when the peak to peak threshold is exceeded.

The class A preamplifier incorporates a transformer input to minimize common mode signal interference. The amplifier contains one stage of voltage gain (Q01) and two stages of current gain (Q02 and Q03). A positive feedback loop is provided within the amplifier by C02 and R07. This loop returns a signal to the junction of R06 and R07 which approaches, but never exceeds the signal at the collector of Q01. Thus, R06 presents a very high impedance in the collector load of Q01 and increases the a-c voltage gain of Q01 from a value of less than 100 to over 1000. Gain is stabilized by the negative feedback network composed of R04 and R03 which is used as a reference point for the input transformer secondary. Note that R02 may be connected externally in parallel with R03.

The rectifying circuit is composed of transformer T02 and diodes CR01 through CR04. The threshold at which detection takes place is determined by R15, R16, and R17 when the input to pin 7 is -12v. If pin 7 is jumpered to ground, R18 essentially parallels R15 and R16. R19 acts as a normal input load and CR05 provides isolation from other circuits operating in parallel.

The switching circuit is composed of Q04 which turns off when the rectifier circuit reaches the threshold point. This "1" output may be used directly as a level detection point or as part of an AND term with the peak detector output.

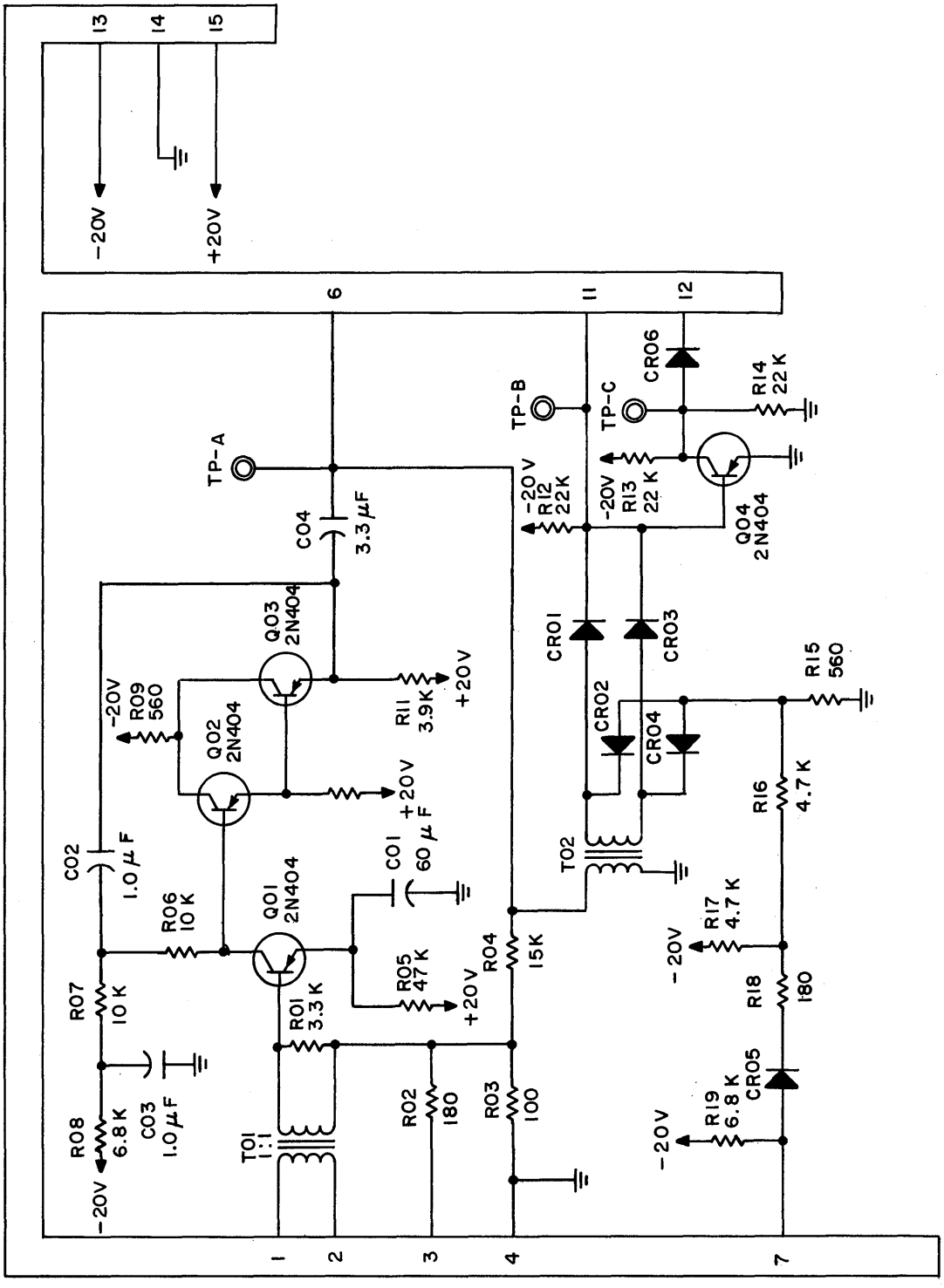


Figure 7. EDA, Real Level Detector

READ PEAK DETECTOR (ODA)

The read peak detector (figure 8) is used with the output of the level detector. The level detector full wave rectifies a class A signal into positive pulses, and passes the portion of the signal which exceeds a pre-determined level to the peak detector (figure 9).

Peak detection is accomplished by first differentiating the rectified class A signal, and then detecting the zero crossover point of this differentiated signal.

The first portion of the peak detector circuit consists of the differentiating amplifier (C01, R01, and R02). Because R02 is connected to the output of the high gain amplifier, the resistance presented to the differentiating capacitor is essentially R02/G where G equals the gain of the amplifier (approximately 1000).

The high gain amplifier uses three transistors in a single inverting circuit. Q01 is the voltage amplifier; Q02 and Q03 are emitter follower connected and provide current gain. A positive feedback loop (C02 and R04) returns a signal to the junction of R03 and R04. This signal approaches, but never exceeds, the signal at the collector of Q01. R03 presents a very high impedance in the collector load of Q01, and increases the a-c voltage gain of Q01 from 100 to 1000. Because the voltage returned to the junction of R03 and R04 is always slightly less than that at the output of Q01, the circuit is free of the usual oscillatory problems associated with positive feedback. The coupling capacitor C04 eliminates d-c positive feedback and thermal drift problems associated with high impedance loads. The d-c (8v) operating point at the output of the amplifier is made stable by the negative feedback divider (R01 and R02).

The differentiated output is coupled by C05 to the zero crossover switching circuit of Q04. R10 normally biases Q04 in the on state. When a signal appears, CR01 prevents Q04 from being overdriven by the differentiated signal which initially swings in the negative direction. When the differentiated signal swings positive and exceeds 0v, CR01 conducts and removes the drive from Q04 causing it to turn off. R09 acts as a load on C05, reducing the effect of non-linear loading by the switching circuit.

Q05 is used in the simplified version of the normal inverter logic circuit. A delay capacitor, C06, delays the "1" (negative) excursion at the input, and the "0" (positive) excursion on the output.

A narrow negative output pulse (1/4 to 1/2μsec) is produced when the output diodes of Q04 and Q05 are ANDed. The "1" (negative) output pulse corresponds to a point just following the positive peak on the input, or the zero crossover point in the positive direction of the differentiator output.

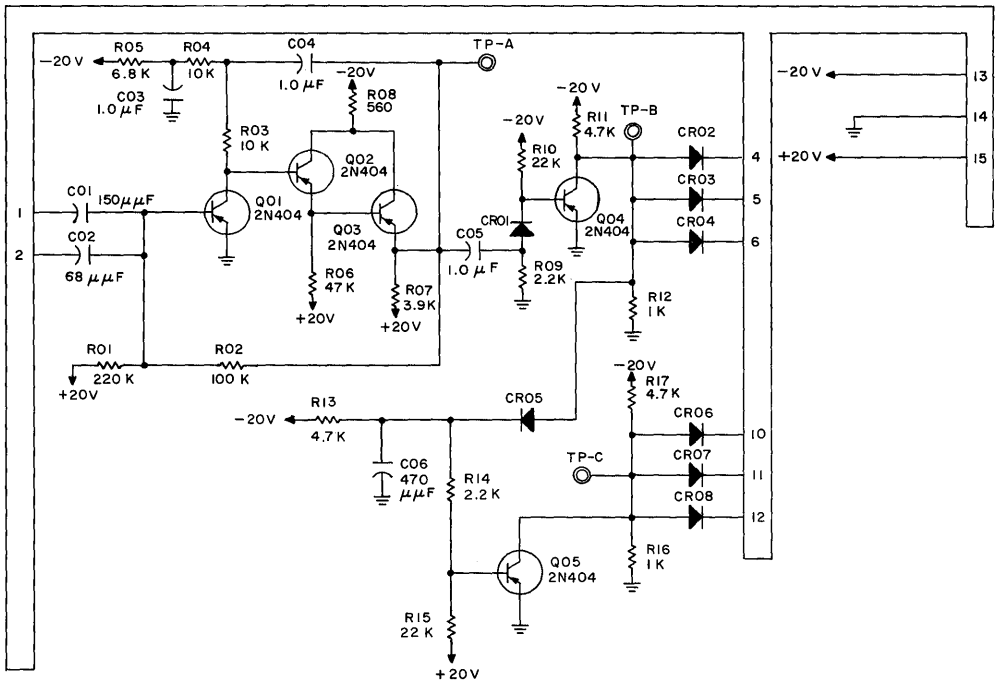


Figure 8. ODA, Read Peak Detector

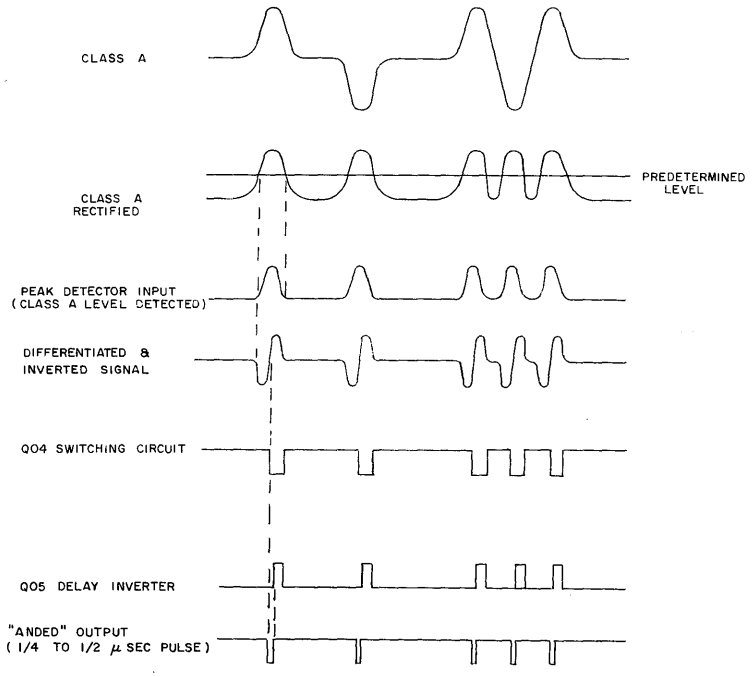


Figure 9. Read Peak Detector Waveforms

ADJUSTABLE DELAY (UAA)

The adjustable delay circuit (figure 10) is non-inverting in relation to the input but changes from "1" to "0" are delayed at the output of the delay.

The input stage of the circuit is an inverting circuit with a speed up diode (CR01) to reduce turn off time in Q01. The timing circuit is composed of C04, R07, R08 and potentiometer R06. Longer range delays are obtained by paralleling C04 with C01 and/or C02 with external jumpers. A limited delay adjustment may be obtained by paralleling R05 with the charge network (R07, R08 and R06). Some external adjustment may also be obtained by connecting a potentiometer between pins 3 and 7.

Discharge of C04 is accomplished by the emitter follower (Q02) in the second stage through diode CR02. Drive to Q02 is determined by the drop across R09 which also provides a small percentage of the current to discharge C04.

The third stage is emitter driven to obtain voltage gain and proper bias reference to switch the output stage. The base circuit reference is changed by connecting R06 as a voltage divider. As R06 inserts resistance to increase the RC time constant, it also removes resistance in the base divider of Q03. A greater portion of the RC time constant can be used for long delays. The normal adjustment range of 9 to 1 is extended to approximately 20 to 1.

The fourth and final stage, Q04, is an inverter circuit with a saturation limiting diode (CR07) which limits base drive. A divider circuit in the base allows considerable voltage swing to improve turn-on time. The output excursions are limited in the negative direction by a resistance divider.

PHOTOCELL AMPLIFIER (OAA)

The photocell amplifier (figure 11) receives inputs from silicon solar cells. The output from the amplifier is a "1" when the solar cell is illuminated and a "0" when unlighted. An adjustable potentiometer is provided because of the low level signals normally available from the solar cells. This allows optimum centering of the switching point of the amplifier to compensate for the over-all photocell excitation, sensitivity and amplifier tolerances.

The first stage of the amplifier consists of an inverting amplifier, Q01. This transistor is turned on by drive current flowing through R02A from potentiometer R01A. Normally

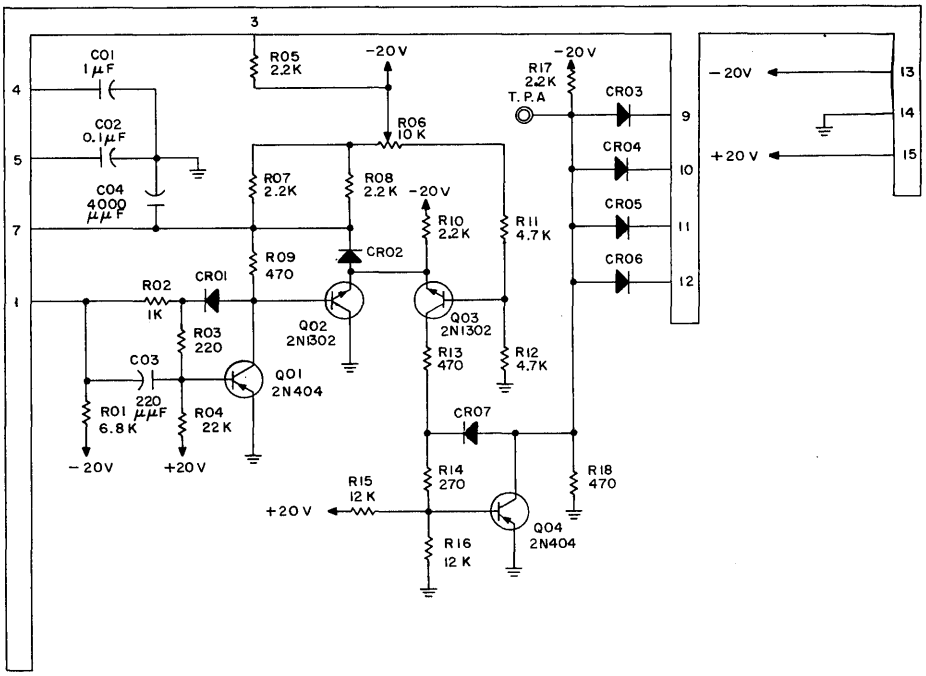


Figure 10. UAA, Adjustable Delay

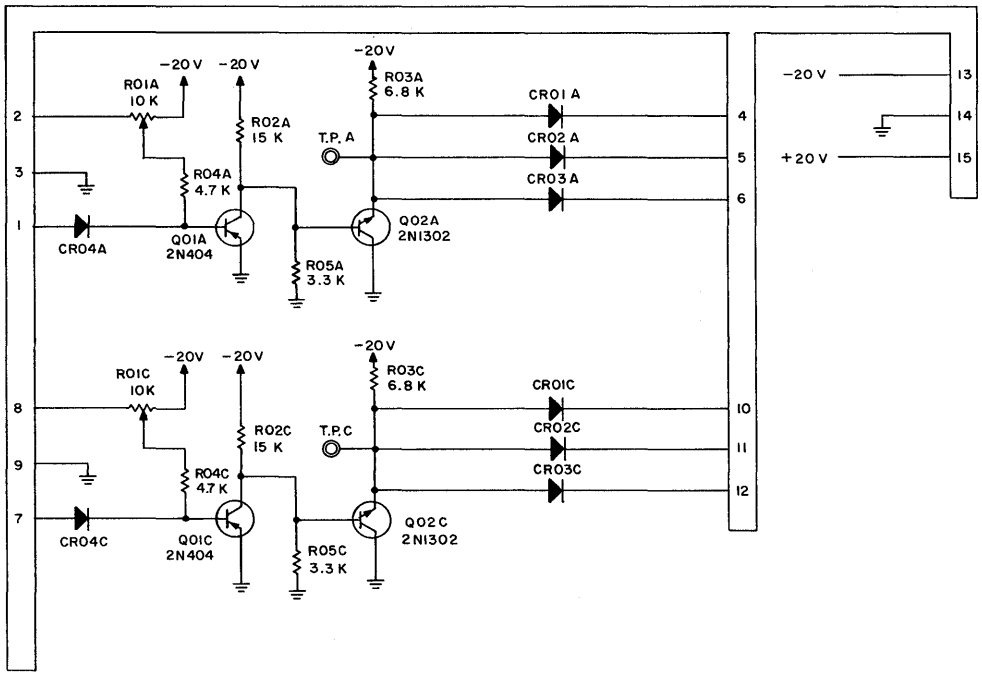


Figure 11. OAA, Photo Cell Amplifier

pin 2 is jumpered externally to pin 3 to provide R01 with the maximum range of adjustment. The positive terminal of the photocell is normally connected to pin 1. Thus, the output current of the photocell counteracts the turn-on current of R02A. Sufficient output from the photocell turns off Q01. CR01 compensates for the change in base to emitter potential of Q01A with changing temperature.

The output of Q01A is directly coupled to Q02 which acts as an emitter follower. The logical "1" excursion at the output is determined primarily by the divider composed of R03A and R04A since the gain of Q02A is sufficient to provide only minor loading of this divider regardless of the number of outputs actually used. Three diodes (CR02A, 3A, 4A) are provided for ANDing with other logical circuits.

REEL MOTOR DRIVE CIRCUITS

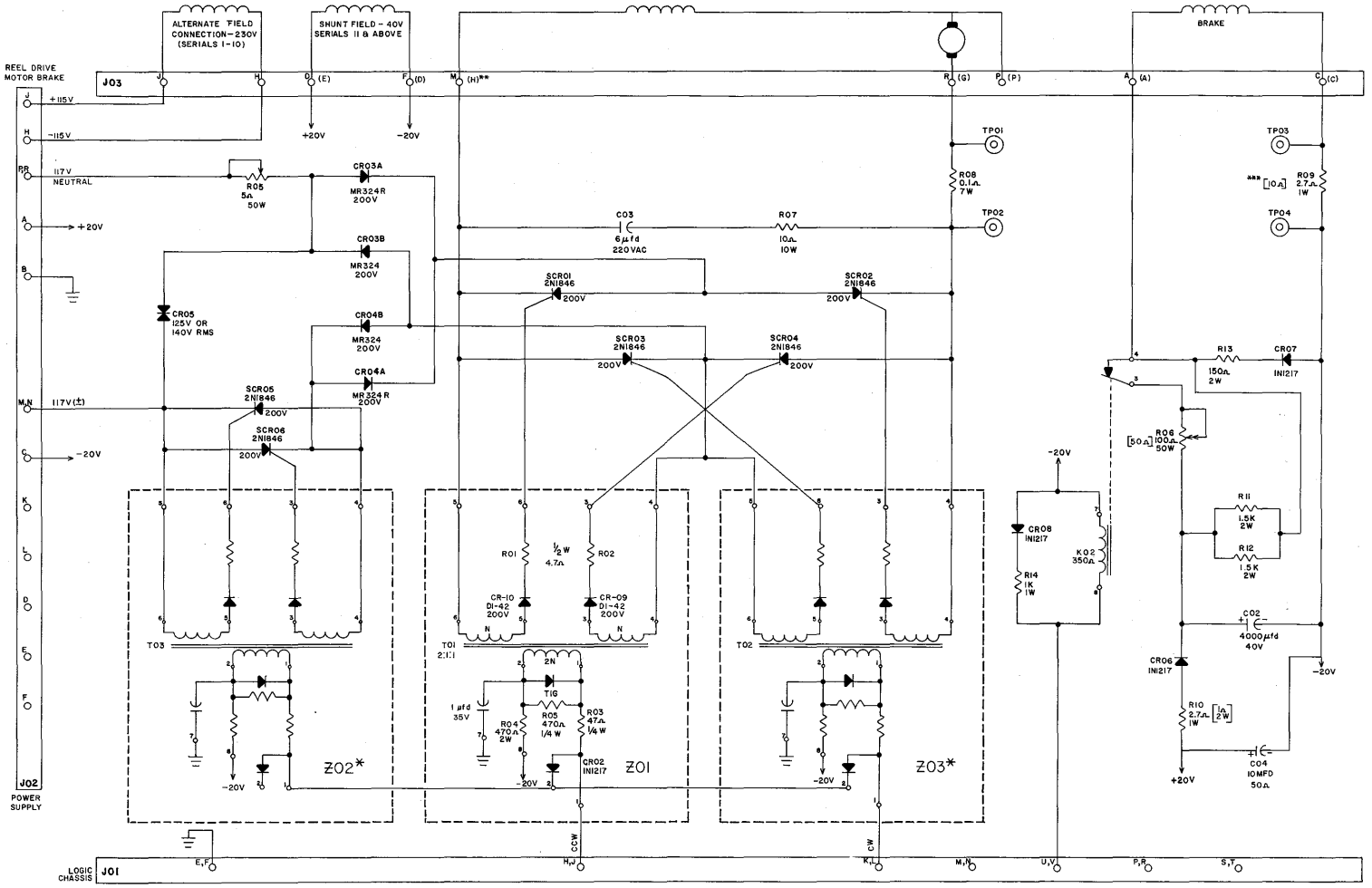
The reel motor drive circuits (figure 12) provide the output power necessary to operate motors and brakes associated with the take-up and supply reels. Each of the two reel motors has a motor drive circuit. Input to the drive circuits is from output drivers in the logic section (servo drive control). The power supply and power distribution unit furnish a-c and d-c power.

The drive circuits are on-off drivers, as contrasted to a proportional servo system. A solid-state drive circuit is used in armature control of the shunt field direct current motor and provides high speed switching of the 12 amp (maximum) currents required in the high performance servo. The drive circuit turns on the line voltage (SCR05, SCR06), rectifies it (CR03A, B and CR04A, B) and applies the proper polarity (SCR01, 2, 3, 4) to the motor armature for rotation in the selected direction. Transformers T01, T02, and T03 isolate the line voltage from the output drivers in the logic while coupling 25 usec pulses to the control elements of the silicon controlled rectifiers (SCR). Pulse repetition rate when the SCR's are turned on is approximately 1000 cycles per second until the reel speed equals the capstan speed. Pulses are then applied as required to maintain a reel speed slightly in excess of the capstan speed. When the tape loop returns to the center or brake region of the loop box, motor drive power is removed by interrupting the control pulses (refer to servo drive control logic).

Control pulses are applied to T01 and T03 for clockwise rotation, and to T02 and T03 for counter clockwise rotation. A pulse repetition rate of 1000 cps turns on the SCR's at an early point in each half-cycle of the supply power. This turn-on point varies with motor speed due to the back EMF of the armature.

The SCR's are turned off by reducing the current to approximately 0.05 amp. In SCR05, 6 this occurs during each half-cycle of the power input. The current in the remaining SCR's is reduced to the turn-off point shortly thereafter and readies the H switch (SCR01, 2, 3, 4) to select proper polarity the next time motor drive is required.

A high-speed mercury relay (K02) operates the multiple disc friction brakes. The relay circuit applies brake power when the relay is non-energized, providing some fail-safe protection. Sufficient energy is stored in C02 to bring the reel to a stop if power is inadvertently interrupted during operation.



* REFER TO Z01 FOR SYMBOL NUMBERS AND COMPONENT VALUES.

** 8 PIN CONNECTORS ARE SHOWN IN PARENTHESIS; ALL OTHERS REFER TO 14 PIN CONNECTORS.

*** COMPONENT VALUES FOR PARTICLE BRAKES ARE SHOWN IN BRACKETS; ALL OTHERS REFER TO FRICTION BRAKES.

Figure 12. Reel Motor Drive Circuit

CAPSTAN DRIVE AND BRAKE CIRCUITS

The motion control circuit determines the direction tape is to be moved. After direction is selected, tape motion is controlled by the capstan drive and brake control circuit which applies pressure or vacuum to the capstans and pneumatic brake port. In the drive condition, vacuum is applied to the forward or reverse capstan while pressure is applied to the brake port. In this case, the tape is held away from the brake port but abainst the rotating capstan and is therefore moved across the read-write heads. In the clear or non-drive condition, vacuum instead of pressure is applied to the brake port while pressure is applied to both capstans. The tape is, in this case, held against the brake port but separated from both rotating capstans.

The capstan drive and brake circuits energize a two-terminal valve coil which, in turn, allows vacuum or pressure to be valved to the brake port or appropriate capstan. The capstan and brake port coils are driven by an identical circuit. The pneumatic valve coil requires that the current direction be reversed to switch from pressure to vacuum or vice versa. To reduce actuation time, the pneumatic valve coil also requires 2-amp initial current in the new direction for 2 ms. One amp is sufficient to maintain the valve in the steady state position until the next change.

The circuit which controls the direction and magnitude of current in the pneumatic valve coil L01 is shown in figure 13. The switching circuit which selects the direction of current in L01 is called an H switch. The switches are composed of transistors with heat sinks (Q01 through Q04) and are located in the four legs of the H configuration. The load (L01) is at the crossbar of the H configuration. At any given instant, two of the four transistors are switched on while the remaining two transistors are switched off. The on transistors occupy diagonally opposite legs in the H configuration. Q01 and Q03 will be switched on for a forward operation, connecting vacuum to the rotating capstan causing it to drive tape. Q02 and Q04 will be switched on for a reverse or stop operation, connecting pressure to the rotating capstan and preventing contact with the tape.

If the EFs are removed from the circuit, resistors R1 through R5 provide bias for Q01 through Q05. One EF operates each pair of switches in the H configuration. Resistors R_x and R_y in the EF card prevent overdrive of Q03 and Q04. This allows the EF to

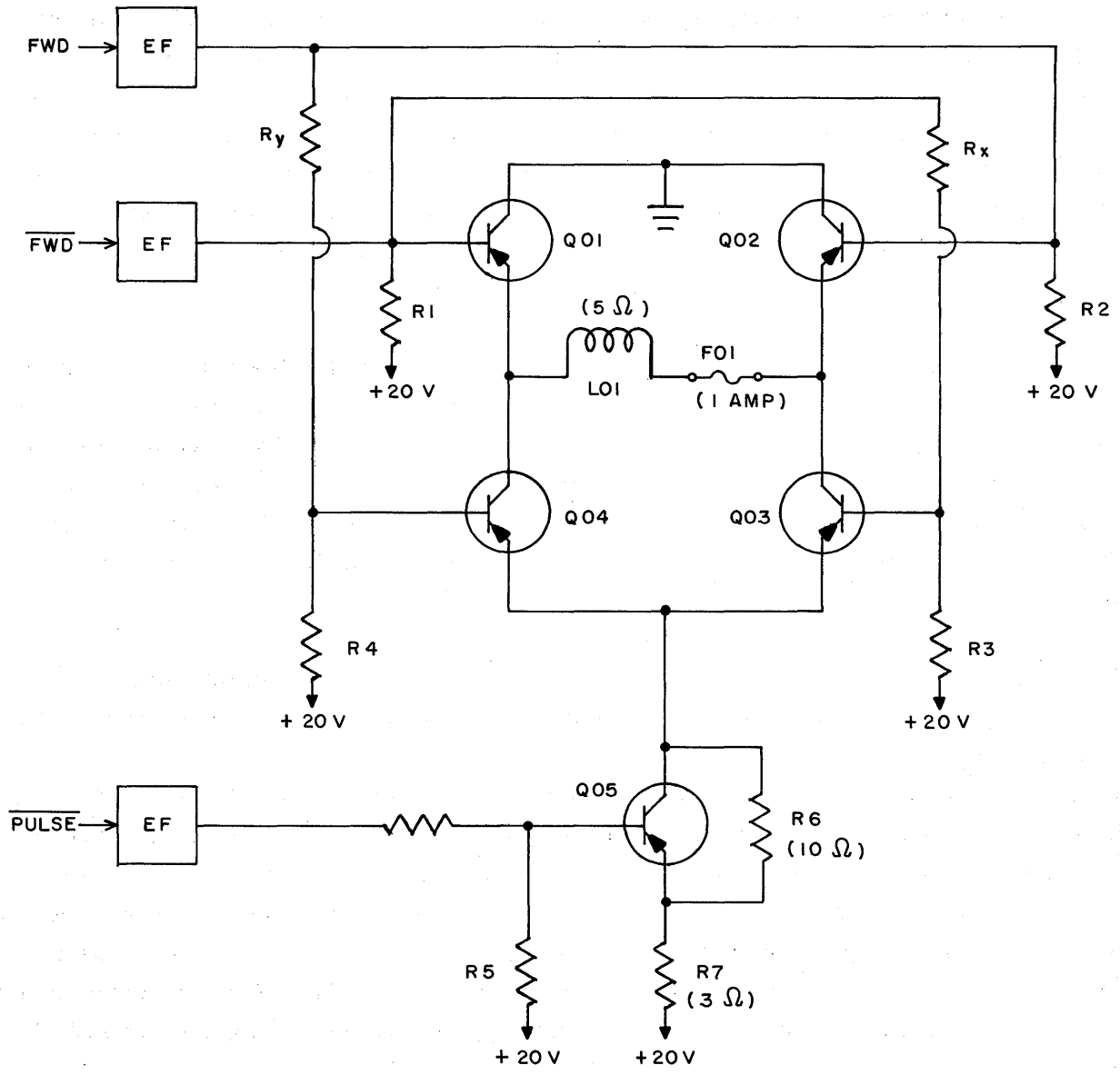


Figure 13. Typical Drive Circuit

drive both switching transistors in parallel even though the emitter reference voltages are different. The value of R_x and R_y is chosen to provide approximately equal drive to both switching transistors.

The magnitude of current in the pneumatic valve coil is determined by the power supply voltage and the total effective series resistance in the circuit. The power supply voltage is fixed at 20 v. Total circuit resistance during the initial high current pulse, excluding the saturation resistance of switching resistors, is about 8 ohms (L01 and R7). After the current is reduced, the total circuit resistance is about 18 ohms (L01, R6, and R7).

Effective resistance of the switching transistors is less than 1 ohm for either level of current. The EF driving Q05 drives only Q05. The emitter voltages of Q03, Q04 and Q05 are approximately the same during the high current level; each of the conducting transistors has approximately the same drive. The change in emitter voltages of Q03 and Q04 at the lower current level causes a corresponding decrease in the drive current of Q03 or Q04. Q05 is turned off at the lower current level.

The use of the series resistance (R6 and R7) in this circuit prevents excessive current flow and avalanche failure of several semiconductors due to small delays in turn-off of Q01 through Q04. Fuse F01 prevents a sustained high current level from damaging L01.

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Printed in U.S.A.