86816400

CONTROL DATA CORPORATION

CONTROL DATA®
66X EXERCISER
TB113

GENERAL DESCRIPTION
OPERATION
INSTALLATION AND CHECKOUT
THEORY OF OPERATION
DIAGRAMS
MAINTENANCE
MAINTENANCE AIDS
PARTS

HARDWARE MAINTENANCE MANUAL

REVISION RECORD

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PREFACE

This manual provides information pertaining to the CONTROL DATA® 66X Exerciser (TB113). It is intended for use by Customer Engineering and other personnel involved in maintaining the CONTROL DATA® 66X, 34XXX, and 92XXX Magnetic Tape Transports.

The manual contains the following sections of information.

Section 1	General Description
Section 2	Operation and Programming
Section 3	Installation and Checkout
Section 4	Theory of Operation
Section 5	Diagrams
Section 6	Maintenance
Section 7	Maintenance Aids
Section 8	Parts Data

Section 9, Wire Lists, is not included. Wiring information is included in Section 5, Diagrams. Section 10, Equation Summary, does not apply to this equipment.

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General Description

Section 1

General Description

1.0 Functional and Operational Description

The 66X Exerciser (hereinafter referred to as the exerciser) is a portable, hand-carried, tape transport maintenance aid. It is designed to provide maintenance capability for the Control Data® 66X, 92XXX, and 35XXX model Magnetic Tape Transports. The exerciser is approximately 6 inches high, 18 inches wide, and 13 inches deep and weighs approximately 25 pounds. It can easily be carried as on-board airline baggage as it fits under an airline seat, and can therefore be readily transported to wherever it is needed in support of tape transport maintenance.

The exerciser is housed in a light-weight aluminum carrying case. Medium-scale integrated circuits and miniature components have been incorporated into its design, thereby effecting a compact, light-weight, easy-to-carry, yet highly functional testing capability which can greatly simplify and reduce the time required to perform maintenance on the tape transport.

The exerciser receives status signals and read data from the tape transport and transmits control and write data signals to the tape transport. In this way, the tape transport may be operated while not connected to a computer or any other control device. The control signals and data are a simulation of the signals and data normally furnished by the controller, and provide a means of exercising the tape transport in order to isolate malfunctions and to perform routine preventive maintenance.

The exerciser is completely self-contained and includes the necessary cables to provide both operating power for the exerciser and interface to the tape transport. Ruggedness and reliability have been incorporated into the exerciser design.

The operator control panel contains the necessary switches, controls, and indicators to permit operator control of the unit. Exerciser logic is provided in a logic card rack under the operator panel. Program control is accomplished by a two-bit by eight-address memory. The operator stores the desired program in memory via the operator control panel switches.

2.0 Equipment Specifications

Refer to Table 1-1 for a detailed list of exerciser physical and electrical specifications.

CHARACTERISTICS	REQUIREMENT
PHYSICAL	
Height	6.0 inches (15.24 cm)
Width	18.0 inches (45.72 cm)
Depth	13.0 inches (33.02 cm)
Weight	25.0 pounds (11.34 kg)
ENVIRONMENTAL	
Temperature	Operating: 60° to 90° F (15.6° to 32.2° C) Non-operating: -30° to 150° F (-34.4° to 65.6° C)
Relative Humidity	Operating: 0% to 90% without condensation. Non-operating: 0% to 90% without condensation.
Altitude	Maximum operating: 15,000 feet (4,921 meters) Minimum operating: -1,000 feet (304.8 meters) Maximum non-operating: 40,000 feet (12,192 meters)
ELECTRICAL	
Power Source	120 volts AC at 50 to 60 Hertz, or 220 volts AC at 50 to 60 Hertz, 2 wire plus ground.
Line Current	0.9 amperes at 120 volts AC
LOGIC LEVELS (Interface)	
Logic "1"	+0.250 volts DC nominal when connected to the tape transport. +0.025 volts DC nominal when not connected to the tape transport.

Table 1-1 Equipment Specifications

CHARACTERISTICS	REQUIREMENT
LOGIC LEVELS (cont'd) (Interface)	
Logic "0"	-0.250 volts DC nominal when connected to the tape transport. -0.025 volts DC nominal when not connected to the tape transport.
LOGIC LEVELS (Internal)	
Logic "1" (DTL)	+5.0 volts DC nominal
Logic "0" (DTL)	+0.2 volts DC nominal
Logic "1" (TTL)	+3.3 volts DC nominal
Logic "0" (TTL)	+0.2 volts DC nominal

Table 1-1. Equipment Specifications (cont'd)

3.0 Interface Lines

Figure 1-1 shows the interface lines between the exerciser and the tape transport. Refer to Table 1-2 for a definition of the interface signals.

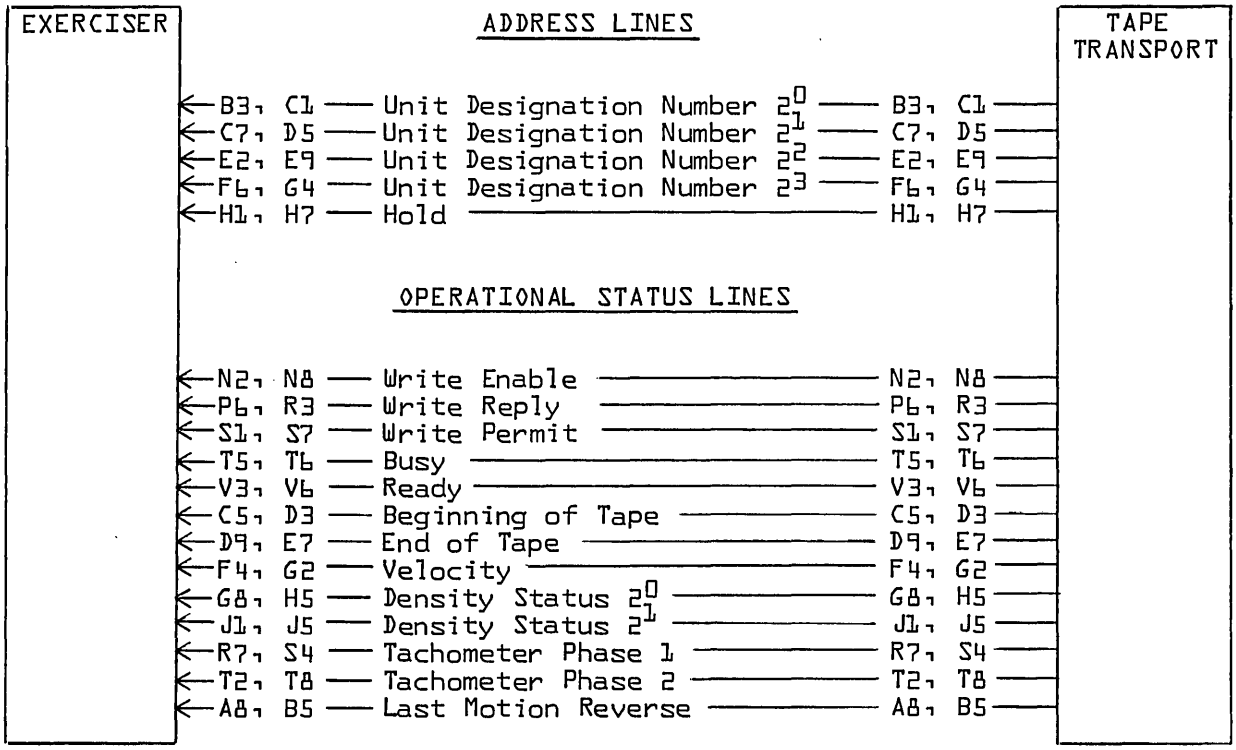


Figure 1-1 Interface Pin Assignments

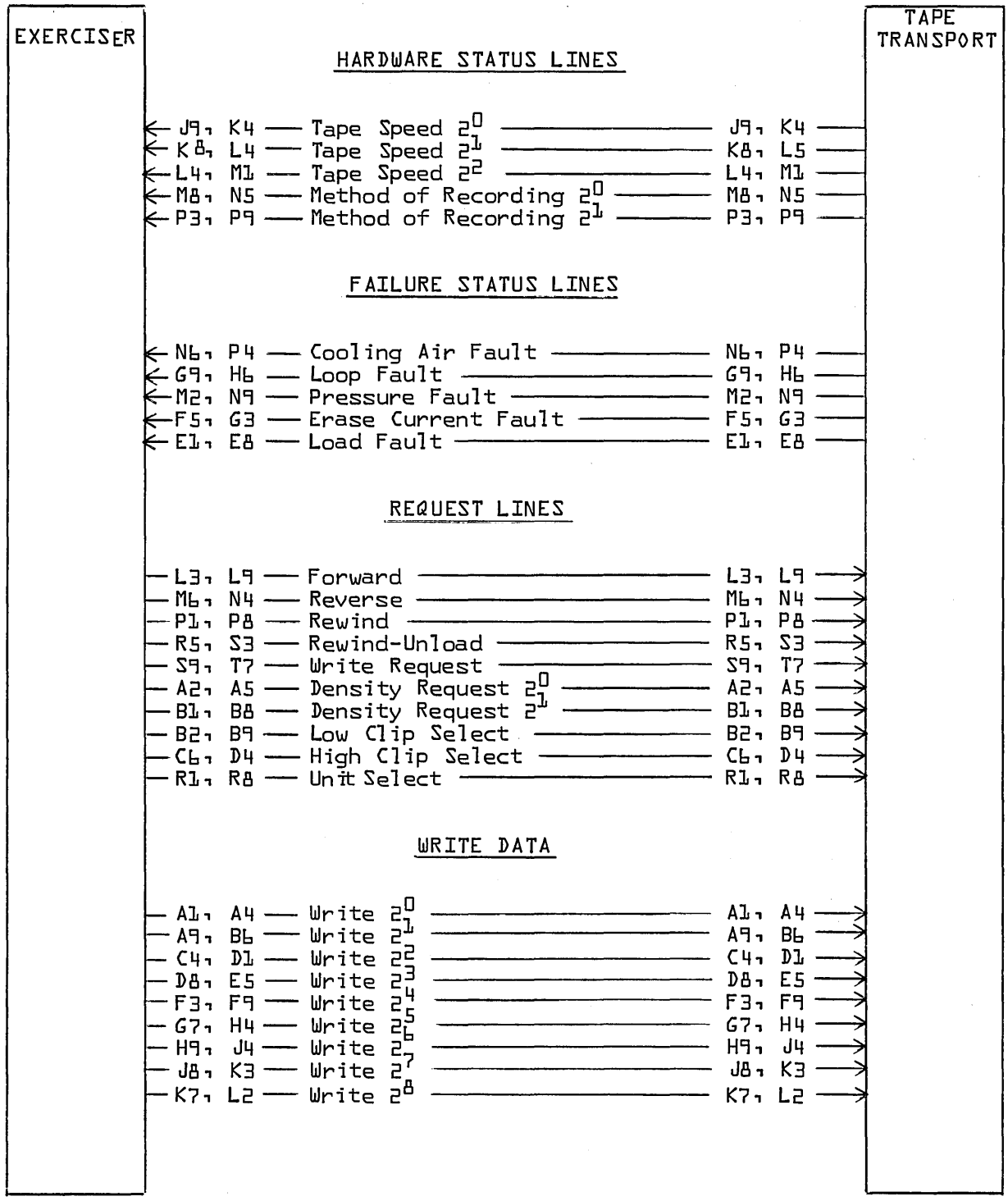


Figure 1-1 Interface Pin Assignments (cont'd)

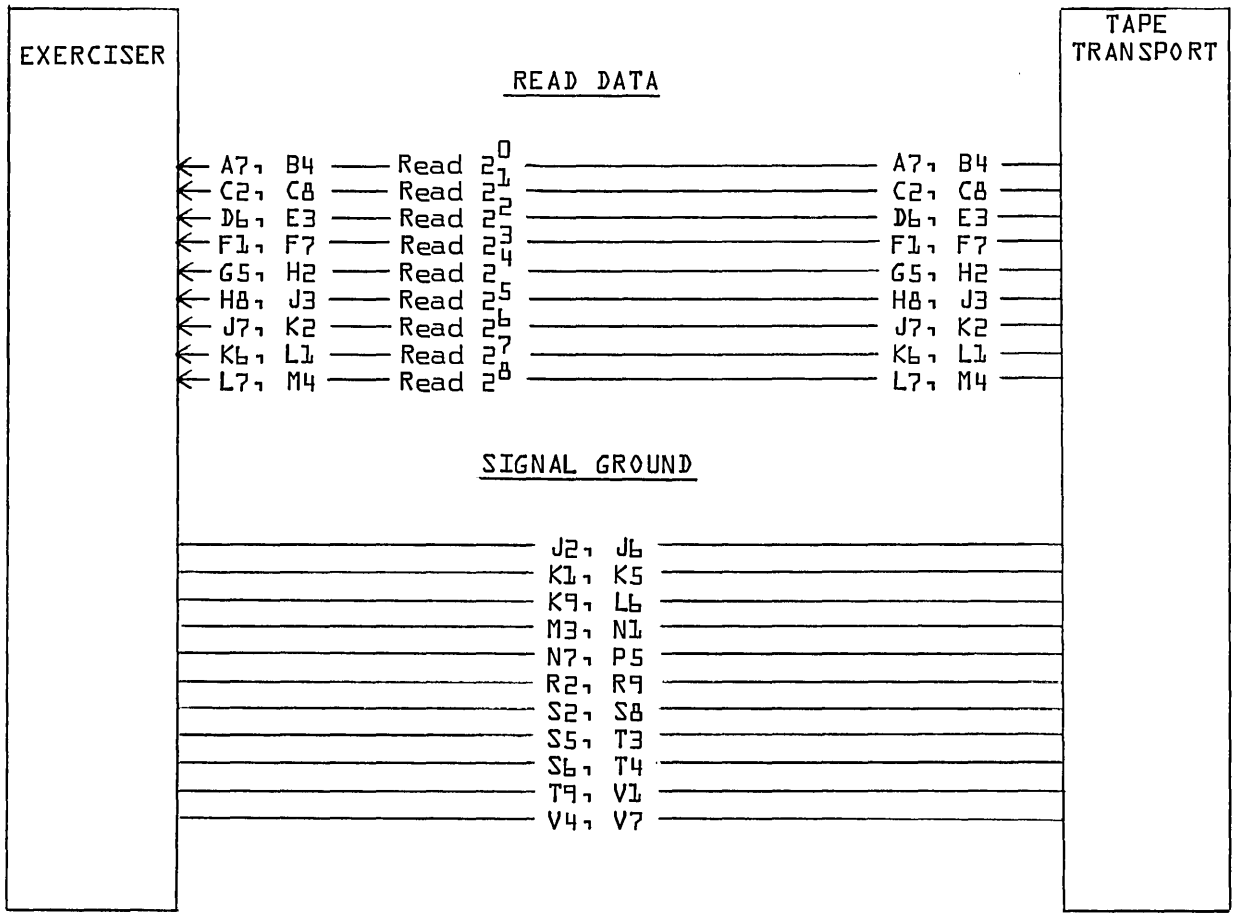


Figure 1-1 Interface Pin Assignments (cont'd)

SIGNAL	PINS	ACTIVE LEVEL	FUNCTION
TO THE EXERCISER			
Unit Designation Number 2^0 2^1 2^2 2^3	B3, C1 H8, H9 J3, J4 J5, J6	"1" or "0" "1" or "0" "1" or "0" "1" or "0"	The four binary coded octal Unit Designation Lines from the tape transport indicate one of the unit numbers between 0 and 17_8 that has been selected on the tape transport operator control panel.
Hold	J9, K1	"1"	Indicates the tape transport is in a stand-by condition, that is, none of the sixteen {0-17_8} Unit Designation Numbers have been selected.
Write Enable	N5, N6	"1"	Indicates that a write ring is present in the mounted reel of tape and permits the tape transport to accept and process a write request.
Write Reply	G7, G6	"1"	Indicates that write and erase current is on in the tape transport. It is turned on by a Write Request and off by a Reverse, Rewind, or Rewind-Unload request.
Write Permit	L3, L4	"1"	Permits write data to be accepted by the tape transport. Remains low long enough to maintain the inter-record gap.
Busy	L1, L2	"1"	Indicates that tape is in motion. The tape transport will not respond to a new motion command when busy is high, except that the unit will respond to a forward or reverse command that is re-instated within 300 microseconds after it is dropped, regardless of the state of the Busy line at that time.

Table 1-2. Interface Signal Description

SIGNAL	PINS	ACTIVE LEVEL	FUNCTION
		TO THE EXERCISER	
Ready	M2, M3	"1"	Indicates that the tape transport is under remote control and will respond to requests from the exerciser.
Beginning of Tape	L9, M1	"1"	Indicates that a beginning of tape marker is detected by the tape transport. It is high when the reflective marker is under the sensor.
End of Tape	G7, G8	"1"	Indicates that an end of tape marker is detected by the tape transport. It is high when the reflective marker is under the sensor.
Velocity	L7, L8	"1"	Indicates that tape is moving at full speed (±4 percent) in the forward or reverse direction.
Density Status 2^0 2^1	 N9, P1 P2, P3	 "1" or "0" "1" or "0"	The two lines indicate the density at which the tape transport is operating. The code is as follows: 2^1 2^0 0 0 556 BPI NRZI 0 1 800 BPI NRZI 1 0 1600 BPI Phase Encoded 1 1 NOT USED
Tachometer Phase 1 Tachometer, Phase 2	R7, S4 T2, T8	"1" or "0" "1" or "0"	The Phase 1 and Phase 2 outputs from the capstan electronics are pulse trains with repetition rates proportional to the capstan speed.
Last Motion Reverse	A8, B5	"1"	Indicates that the last commanded direction of the transport was reverse or rewind.

Table 1-2 Interface Signal Description (cont'd)

SIGNAL	PINS	ACTIVE LEVEL	FUNCTION
TO THE EXERCISER			
Tape Speed 2^0 2^1 2^2	 J9, K4 K8, L5 L4, M1	 "1" or "0" "1" or "0" "1" or "0"	The three lines indicate tape speed. The code is as follows: (No other codes are accepted by the exerciser). 2^2 2^1 2^0 0 0 1 100 IPS 0 1 0 150 IPS 1 0 0 200 IPS
Method of Recording 2^0 Method of Recording 2^1	M8, N5 P3, P9	"1" or "0" "1" or "0"	The two lines indicate the recording method of the tape transport. The code is as follows: 2^1 2^0 0 0 7 Track, 556 or 800 BPI NRZI 0 1 9 Track, 800 BPI NRZI 1 0 9 Track, 800 BPI NRZI or 1600 BPI Phase Encoded 1 1 9 Track, 1600 BPI Phase Encoded
Cooling Air Fault	N6, P4	"1"	Indicates that the transport cabinet temperature has reached a level such that an increase of 10 degrees will result in an automatic rewind unload.
Loop Fault	G9, H6	"1"	Indicates a loop has dropped, causing the tape transport to go not Ready.
Pressure Fault	M2, N9	"1"	Indicates that the air bearing pressure has reached a value of 2.25 to 2.50 psi.
Erase Current Fault	F5, G3	"1"	Indicates that the erase signal amplitude is less than 2% of standard while Write Reply is high.
Load Fault	E1, E8	"1"	Indicates that the tape transport has failed to load tape automatically.

Table 1-2. Interface Signal Description (cont'd)

SIGNAL	PINS	ACTIVE LEVEL	FUNCTION
TO THE TAPE TRANSPORT			
Read Data 2^0 2^1 2^2 2^3 2^4 2^5 2^6 2^7 2^8	 A7, B4 C2, C8 D6, E3 F1, F7 G5, H2 H8, J3 J7, K2 K6, L1 L7, M4	 "1" or "0" "1" or "0" "1" or "0" "1" or "0" "1" or "0" "1" or "0" "1" or "0" "1" or "0" "1" or "0"	In the NRZI format, the tape transport sends a "1" pulse to the exerciser any time there is a change in the direction of the write current. In the Phase Encoded format the tape transport sends a "1" voltage level to the exerciser whenever there is a change in write current in one direction and sends a "0" voltage level to the exerciser whenever there is a change in the write current in the opposite direction.
Forward	L3, L9	"1" or "0"	When Forward goes from a low to a high, tape moves in the forward direction. When Forward returns to a low, tape motion stops.
Reverse	M6, N4	"1"	When Reverse goes from a low to a high, tape moves in the reverse direction. When Reverse returns to a low, tape motion stops.
Rewind	P1, P8	"1"	The Rewind signal is a one microsecond pulse. The tape transport will execute a rewind operation provided Busy is not present.
Rewind-Unload	R5, S3	"1"	The Rewind-Unload signal is a one microsecond pulse. The tape transport executes an Unload operation. If the tape is not at load point, the unload operation is automatically preceded by a rewind operation.

Table 1-2. Interface Signal Description (cont'd)

SIGNAL	PINS	ACTIVE LEVEL	FUNCTION
TO THE TAPE TRANSPORT			
Density Request 2^0 2^1	 A2, A5 B1, B8	 "1" or "0" "1" or "0"	Two lines are used to request one of three conditions. A fourth condition, Local, permits the density to be selected at the operator control panel on the tape transport. The code is as follows: 2^1 2^0 0 0 556 BPI NRZI 0 1 800 BPI NRZI 1 0 1600 BPI Phase Enabled 1 1 Local
Low Clip Select	B2, B9	"1"	Over-rides the standard tape transport clipping level and commands a Low Read Threshold.
High Clip Select	C6, D4	"1"	Over rides the standard tape transport clipping level and commands a High Read Threshold.
Unit Select	R1, R8	"1"	When this line is held high the unit select light is lit on the tape transport.
Write Data 2^0 2^1 2^2 2^3 2^4 2^5 2^6 2^7 2^8	 A1, A4 A9, B6 C4, D1 D8, E5 F3, F9 G7, H4 H9, J4 J8, K3 K7, L2	 "1" or "0" "1" or "0" "1" or "0" "1" or "0" "1" or "0" "1" or "0" "1" or "0" "1" or "0" "1" or "0"	Seven or nine lines carry six or eight information bits and one parity bit. Odd parity is generated. In the NRZI format, the write current changes only when a "1" is written on the tape. If a zero is written there is no change in the write current. In the Phase Encoded format the write current changes for both zeros and ones.

Table 1-2. Interface Signal Description (cont'd)

Section 2

Operation

Section 2

Operation

1.0 General

The following section provides the procedures necessary to operate the exerciser. Instructions are given for programming the memory prior to placing the exerciser in a program mode.

Before operating the exerciser, insure that the procedures in Section 3, Installation and Checkout, have been performed to insure the exerciser is ready for operation.

2.0 Operator Controls and Indicators

The controls and indicators on the operator control panel provide manual operation of the exerciser. Refer to Figure 2-1 for the location of all operator controls and indicators and to Table 2-1 for a description of each control or indicator.

In Table 2-1, switch positions and control limits are indented under the component name. The index numbers on the illustration in Figure 2-1 correspond to the item numbers in the table. The reference designators in Table 2-1 correspond to the designators on the back side of the operator control panel. In the ID (Identification) column of Table 2-1, the following abbreviation definitions apply.

ABBREVIATION	DEFINITION
C	Control
CB	Circuit-Breaker
D	Display
ETI	Elapsed Time Indicator
F	Fuse
I	Indicator
J	Jack
PB	Pushbutton
PB-I	Pushbutton-Indicator
S	Switch

ITEM	COMPONENT NAME	ID	REF. DESIG.	FUNCTION
1	AC POWER	J	J2	A three prong, male, recessed connector that accepts the female end of the AC power cable. Input may be 120 or 220 volts. Normal operation is on 120 volts. If 220 volts is used, a wiring change must be made within the exerciser.
2	AC POWER FUSE	F	XF1	A 120 or 220 volt AC, one ampere, SLO-BLO fuse.
3	TIMER	T	XM1	A 0 to 2000 hour elapsed time indicator, measuring the time AC power has been applied to the exerciser.
4	AC POWER	S	S1	
	ON			Applies 120 or 220 volt AC power to exerciser AC components. Also Master Clears the exerciser, but not the tape transport.
	OFF			Removes AC power from exerciser components.
5	DISPLAY	D	DS1, DS2, DS3	A bank of three light-emitting-diode arrays which display octal digits from 000 through 777. Data to be displayed is selected by the DISPLAY SELECT switch (item 6).
6	DISPLAY SELECT	S	S2	The data to be routed to the DISPLAY (item 5) is selected by this switch.
	START			Displays the time the tape transport takes to get up to required velocity after a motion command is received. The time is in terms of the number of tachometer pulses from the raising of a motion line to the raising of the Velocity line.
	STOP APP			Displays the time the tape transport takes to stop after a motion command is terminated. The time is in terms of the number of tachometer pulses from the lowering of a motion line (Forward or Reverse) to the next raising of a motion line.

Table 2-1. Switches, Controls, Indicators, and Jacks (cont'd)

ITEM	COMPONENT NAME	ID	REF. DESIG.	FUNCTION
6 (cont'd)	DISPLAY SELECT			
	STOP ACT			Similar to STOP APP except that the time is from the lowering of the Velocity line to the next raising of a motion line.
	SKEW			Operates in conjunction with the SIGNAL MONITOR switch (item 31) to display the time in terms of 50 nano-second pulses from the detection of the first data bit to the detection of the data bit selected by the SIGNAL MONITOR switch. Data bits 2^0 through 2^7 and the parity bit (nine bits) are selected by positions 1 through 9 respectively on the SIGNAL MONITOR switch. The display is updated every one-half second.
	RECORD GAP			Displays the time between the last bit before a record gap and the first bit after a record gap. The time is in terms of the number of tachometer pulses between the End of Operation and the next data pulse.
	READ			Displays the octal value of the data on the Read lines. The right DISPLAY digit indicates the value of tracks 2^0, 2^1, and 2^2; the center digit indicates the value of 2^3, 2^4, and 2^5; and the left digit indicates the value of 2^6, 2^7, and P. The display changes directly as the data bits change.
	ADDRESS			Displays the status of the four Unit Designation Number lines and the Hold line from the tape transport. Unit Designation Numbers may be 000 through 017 depending upon the setting of the Unit Number switch on the tape transport. The hold line will be 020 when it is high, indicating none of the 16 Unit Designation Numbers have been selected.

Table 2-1. Switches, Controls, Indicators, and Jacks (cont'd)

ITEM	COMPONENT NAME	ID	REF. DESIG.	FUNCTION
6 cont'd	DISPLAY SELECT MODEL			Displays the status of the Tape Speed and Method of Recording lines from the tape transport. The first and second digits indicate tape speed, thus; 20 for 200 ips, 15 for 150 ips, and 10 for 100 ips. When the CDC-IBM switch is set to IBM, the first and second digits indicate 07 for 75 ips and 12 for 125 ips. The third digit indicates the method of recording, thus; 0 for 9 track phase encoded, 1 for 9 track dual mode, 2 for 9 track NRZI, and 3 for 7 track NRZI.
	FAULT			Displays the status of the five FAULT lines from the 66X, as follows: DISPLAY — FAULT 001 — LOAD 002 — ERASE CURRENT 004 — VACUUM 010 — LOOP 020 — COOLING AIR The status of two or more fault lines may be added together, thus a display other than those listed above would indicate more than one fault. As an example, 037 would indicate all five faults active.
7	I/O	J	J1	A 160-pin female connector which receives either male plug of the input/output cable to the tape transport.
8	READY (STATUS)	I	DS13	Indicates that the tape transport is ready to respond to requests from the exerciser.
9	BUSY (STATUS)	I	DS12	Indicates that the tape is in motion. The tape transport will not respond to a new motion command when busy.

Table 2-1. Switches, Controls, Indicators, and Jacks (cont'd)

ITEM	COMPONENT NAME	ID	REF. DESIG.	FUNCTION
10	BOT (STATUS)	I	DS11	Indicates that the tape transport detected a Beginning of Tape marker.
11	EOT (STATUS)	I	DS10	Indicates that the tape transport detected an End of Tape marker.
12	FWD (STATUS)	I	DS9	Indicates that the exerciser Forward motion signal is high.
13	REV (STATUS)	I	DS8	Indicates that the exerciser Reverse motion signal is high.
14	WRITE REPLY (STATUS)	I	DS7	Indicates that the tape transport write and erase current is on.
15	DENSITY REQUEST 2^1 and 2^0	S	S7, S6	The two switches are used to select one of three densities. 2^1 2^0 DENSITY 0 0 556 BPI 0 1 800 BPI 1 0 1600 BPI When both switches are set to 1 the density may be selected at the tape transport.
16	DENSITY STATUS 2^1 and 2^0	I	DS15, DS14	Indicates the density at which the tape transport is operating. The code is the same as for the Density Request above.
17	WRITE PERMIT (ERROR)	PB-I	S/DS8	Indicates that the tape transport raised the Write Permit line before the Velocity line. The error may be cleared by pressing the pushbutton.
18	FAULT (ERROR)	PB-I	S/DS7	Indicates that one or more of the tape transport Fault lines (Load, Erase Current, Vacuum, Loop, or Cooling Air) has been activated. The Fault line that has been activated may be displayed on the DISPLAY by setting the DISPLAY SELECT to FAULT. The error indication may be cleared by pressing the pushbutton.

Table 2-1. Switches, Controls, Indicators, and Jacks (cont'd)

ITEM	COMPONENT NAME	ID	REF. DESIG.	FUNCTION
19	VELOCITY (ERROR)	PB-I	S/DS6	Indicates that the tape transport dropped the Velocity signal during the time that a Motion Request (Forward, Reverse or Rewind) from the exerciser was active. The error indication may be cleared by pressing the pushbutton.
20	PARITY (ERROR)	PB-I	S/DS5	Indicates that incorrect (even) parity was detected on the Read Data lines. The error indication may be cleared by pressing the pushbutton.
21	PARITY ERROR RESPONSE	S	S13	
	BACKSPACE			When a parity error is detected, the PARITY (ERROR) indicator lights. The tape transport stops, backs over the word where the error occured, and then attempts to re-execute the original instruction without a parity error. If successful, the PARITY (ERROR) indicator goes out and the tape transport continues executing the instructions in memory. If not successful, the tape transport will continue to back up and re-execute until it is successful or until the parity error is cleared by pressing the PARITY (ERROR) pushbutton.
	OFF			When a parity error is detected, the PARITY (ERROR) indicator lights but the tape transport continues to execute the program without interruption. If the PARITY (ERROR) pushbutton is pressed, the indicator goes out and remains out unless another parity error is detected.

Table 2-1. Switches, Controls, Indicators, and Jacks (cont'd)

ITEM	COMPONENT NAME	ID	REF. DESIG.	FUNCTION
21 (cont'd)	PARITY ERROR RESPONSE			
	TRAP			When a parity error is detected, the PARITY (ERROR) indicator lights. The tape transport does not stop. The word containing the parity error is gated into a register. If the DISPLAY SELECT switch is set to READ, the octal value of the word is presented on the DISPLAY. Before parity can be checked again, the register must be cleared by either pressing the PARITY (ERROR) pushbutton or setting INT CONTROL switch to MC.
22	PATTERN	S	S12	
	TRUE			The data output in a write operation are all true values of the settings of the DATA switches (item 24).
	TRUE/COMP			The data output for the first frame in a write operation are all true values of the settings of the DATA switches. The data in each subsequent frame are alternating complement and true values of the settings of the data switch.
23	CLIPPING LEVEL	S	S11	
	HI			The high tape transport clipping level is commanded.
	NORMAL			The standard tape transport clipping level is commanded.
	LOW			The low tape transport clipping level is commanded.

Table 2-1. Switches, Controls, Indicators, and Jacks (cont'd)

ITEM	COMPONENT NAME	ID	REF. DESIG.	FUNCTION
24	DATA 2^0 through 2^7	S	S17 thru S24	
	I			A logic one is written on the respective track.
	E			The data on the respective track is erased, that is, no flux changes occur in the write head.
	0			A logic zero is written on the respective track.
25	P DATA	S	S27	
	ON			Automatic odd parity is generated for each word being written.
	OFF			Automatic parity generation is disabled. The output is a constant erase level.
26	PAUSE TIME	C	S/R1	
	OFF			The time between the execution of any two instructions is approximately 6 microseconds.
	INCREASE			As the control is rotated from the OFF position to the furthest clockwise position, the time between the execution of any two instructions is increased from approximately 1 to 100 milliseconds.
27	RECORD LENGTH	C	S/R2	
	ONE WORD			When the exerciser is connected to an NRZI tape transport, the true value of the DATA switch settings is written twice for each record, once as a one word record and then as a simulated Longitudinal Redundancy Check (LRC) word. When connected to a Phase Encoded tape transport, the true value of the DATA switch settings is written once for each record.

Table 2-1. Switches, Controls, Indicators, and Jacks (cont'd)

ITEM	COMPONENT NAME	ID	REF. DESIG.	FUNCTION
27 (cont'd)	RECORD LENGTH			
	INCREASE			As the control is rotated from the ONE WORD position to the furthest clockwise position, the writing time, and therefore the number of words per record, is increased. The writing time is increased from 1 to 100 milliseconds. When writing in the NRZI format, an even number of words is always written. In the Phase Encoded format, the number of words may be odd or even. The number of words is dependent upon the tape speed and density.
28	GND	J	J3	A test point common to signal ground only - not AC power ground.
29	SIGNAL MONITOR	J	J4	Signals selected by the SIGNAL MONITOR switch (item 31) are routed to this test point. The signals are not attenuated or delayed.
30	SIGNAL MONITOR	I	DS16	Signals selected by the SIGNAL MONITOR switch are displayed. The signals are extended by 25 milliseconds so they can be observed on the indicator.
31	SIGNAL MONITOR	S	S26	Signals selected by the switch are displayed on the SIGNAL MONITOR indicator and routed to the SIGNAL MONITOR jack.
	1 through 9 (Read Data 2^0 through 2^8)			Data bits 2^0 through 2^8, being read by the exerciser, are selected by positions 1 through 9, respectively. Bit 2^8 is the parity bit. For seven track transports, data at switch positions 7 and 8 are always zero.
	10 (Parity Error Pulse)			When a parity error is detected, a pulse sets the Parity Error flip flop. This pulse is available at this position. When the PARITY (ERROR) indicator is lit it remains on until cleared. A determination may be made as to whether or not more than one parity error is detected after the indicator is on by observing the signal at this switch position.

Table 2-1. Switches, Controls, Indicators, and Jacks (cont'd)

ITEM	COMPONENT NAME	ID	REF. DESIG.	FUNCTION
31 cont'd	SIGNAL MONITOR			
	11 (Write Enable)			Write Enable signal from the tape transport indicating that a write ring is present in the mounted reel of tape.
	12 (Velocity)			Velocity signal from the tape transport indicating that tape is moving within ±4 percent of full speed in either the forward or reverse direction.
	13 (Write Permit)			Write Permit signal from the tape transport indicating that the tape transport is ready to accept write data.
	14 and 15 (Tach I and Tach II)			The two outputs from the tape transport capstan tachometer electronics are pulse trains and may be selected at these two switch positions. The two signals should be 90 degrees out of phase with each other.
	16 (Busy)			The Busy signal from the tape transport indicating that tape is in motion.
	17 (End of Operation)			The End of Operation signal which is generated by the exerciser.
	18 (Forward I/O)			The Forward motion signal on the input/output lines.
	19 (Reverse I/O)			The Reverse motion signal on the input/output lines.
	20 (Time 1)			When the Busy signal goes from a "1" to a "0", a timing chain is initiated. Time 1 of this chain is selected at this position.
	21 (Last Motion Reverse)			The Last Motion Reverse signal from the tape transport.
	22 (Go)			An internally generated signal which occurs when either a Forward motion signal or a Reverse motion signal is output by the exerciser.

Table 2-1. Switches, Controls, Indicators, and Jacks (cont'd)

ITEM	COMPONENT NAME	ID	REF. DESIG.	FUNCTION
31 (cont'd)	SIGNAL MONITOR			
	23 (Write Terminate)			The set output of the Write Terminate flip-flop. The flip-flop is used to provide the Write Jog sequence.
	24 (Write Data)			A 200-nanosecond pulse which occurs when the Data flip-flop is set. The Data flip-flop sets when a Write instruction is commanded.
32	TAPE CONTROL	S	S14	A spring-loaded momentary-on switch that returns to the OFF position when released.
	UNLOAD			An Unload request pulse is transmitted to the tape transport. Once the unload operation has started it cannot be stopped by the exerciser.
	OFF			Normal position of the switch and has no effect on exerciser operation.
	REWIND			A Rewind request pulse is transmitted to the tape transport. Once the rewind operation has started it cannot be stopped by the exerciser.
33	INT CONTROL	S	S15	A spring-loaded momentary-on switch that returns to the OFF position when released.
	LAMP TEST			Applies power to all operator panel indicators for as long as the switch is held in this position. The lamp test may be performed while a program is executing without affecting exerciser operation.
	OFF			Normal position of the switch and has no affect on exerciser operation.
	MC			All input/output ceases and all exerciser functions are returned to initial conditions, including the program address counter which returns to 000.

Table 2-1. Switches, Controls, Indicators, and Jacks (cont'd)

ITEM	COMPONENT NAME	ID	REF. DESIG.	FUNCTION
34	START	PB	S16	A spring-loaded momentary-on pushbutton that returns to the OFF position when released. If the MODE switch (item 37) is set to RUN or STEP, pressing the pushbutton starts the execution of the instruction stored in memory at the address indicated by the ADDRESS indicator. If the MODE switch is set to LOAD, pressing the pushbutton increments the program address one count.
35	INT TEST	S	S8	
	ON			The responses from the tape transport which are necessary for successful completion of the instructions in memory are simulated in order that proper operation of the exerciser may be determined. The length of each instruction including Rewind is determined by the setting of the RECORD LENGTH control.
	S/S			The Ready, Busy, BOT, and EOT signals are accepted from the tape unit and are used in their ordinary contexts to control the Start/Stop (S/S) test; all other transport inputs are ignored.
	OFF			Normal position of the switch and does not affect exerciser operation.
36	OPERATION	S	S9	
	CONTINUOUS			Write or read operations continue (independent of the RECORD LENGTH control) without generating or recognizing record gaps until the End of Tape or Beginning of Tape marker is sensed, at which time the next instruction is executed. Two forward or two Reverse instructions in succession would stop the operation at End of Tape, or Beginning of Tape, respectively. The operation will also stop if the INT CONTROL switch is set to MC.

Table 2-1. Switches, Controls, Indicators, and Jacks (cont'd)

ITEM	COMPONENT NAME	ID	REF. DESIG.	FUNCTION
36 (cont'd)	OPERATION			
	CONT REC			Write or read operations are performed in record segments. The instruction changes at End of Tape or Beginning of Tape. The length of a write is determined by the RECORD LENGTH control; the length of a read by the length of the record on tape. Operation stops at End of Tape or Beginning of Tape if there are two forward or two reverse instructions in succession. Operation also stops if INT CONTROL is set to MC.
	RECORD			Write or read operations are performed in record segments. The instructions change after each record. The length of a write is controlled by the RECORD LENGTH control; the length of a read by the length of the record on tape. The operation stops if the INT CONTROL switch is set to MC.
37	MODE	S	S10	
	RUN			Storage of instructions in memory is inhibited. When the START pushbutton is pressed, program execution begins at the current memory location and continues to the breakpoint, cycles to zero, and then repeats. Repetition is halted by setting the switch to STEP or by setting INT CONTROL switch to MC.
	STEP			Storage of instructions in memory is inhibited. When the START pushbutton is pressed, the instruction, whose indicator was lit, is executed and the program address counter is incremented by one count.
	LOAD			Program execution is inhibited. When an INSTRUCTION pushbutton is pressed, the corresponding instruction is stored at the current memory location. The INSTRUCTION indicator lights.

Table 2-1. Switches, Controls, Indicators, and Jacks (cont'd)

ITEM	COMPONENT NAME	ID	REF. DESIG.	FUNCTION
38	REWIND (INSTRUCTION)	PB-I	S/DS1	Lights to indicate a Rewind instruction is to be executed or is currently being executed. When the pushbutton is pressed a Rewind instruction is stored at the current memory location, if the MODE switch is set to LOAD.
39	WRITE (INSTRUCTION)	PB-I	S/DS2	Lights to indicate a Write instruction is to be executed or is currently being executed. When the pushbutton is pressed a Write instruction is stored at the current memory location, if the MODE switch is set to LOAD.
40	REVERSE (INSTRUCTION)	PB-I	S/DS3	Lights to indicate a Reverse motion instruction is to be executed or is currently being executed. When the pushbutton is pressed a Reverse motion instruction is stored at the current memory location, if the MODE switch is set to LOAD.
41	FORWARD (INSTRUCTION)	PB-I	S/DS4	Lights to indicate a Forward motion instruction is to be executed or is currently being executed. When the pushbutton is pressed a Forward motion instruction is stored at the current memory location, if the MODE switch is set to LOAD.
42	BREAKPOINT 2^0 2^1, and 2^2	S	S3 thru S5	When the memory location represented by the binary configuration of these switches is reached, the instruction at that address is executed and the program address counter is returned to zero. The position of the switches does not affect memory storage capability.
	1			When set to this position the memory address represented by the binary configuration of the switches is enabled for execution.
	0			When set to this position the memory address represented by the binary configuration of the switches is disabled for execution.
43	ADDRESS 2^0, 2^1 and 2^2	I	DS4 thru DS6	Provide binary indication of the current memory address.

Table 2-1. Switches, Controls, Indicators, and Jacks (cont'd)

3.0 Operating Procedure

1. Insure that both the exerciser and the tape transport are in a power down condition.

2. Disconnect the connector on the cable from the controller to the tape transport, at the tape transport.

3. Open the exerciser and remove the input/output cable that is stored under the lid on the top cover.

4. Connect the input/output cable to the I/O connector on the exerciser and to the connector on the tape transport where the controller cable was connected.

5. Remove the AC power cable that is stored under the lid on the top cover of the exerciser.

6. Connect the female end of the AC power cable to the recessed, male, AC POWER connector on the operator panel.

7. Power up the tape transport.

CAUTION

Before applying power to the exerciser, insure that the exerciser is properly wired for the power source being used. Internal wiring changes are required to convert from 120 volt to 220 volt operation, or vice-versa. See Section 6, Maintenance, for input power change instructions.

8. Connect the AC power cable to the 120 or 220 volt AC outlet.

9. Set the exerciser AC POWER switch to ON.

10. Observe the exerciser ERROR indicators and if any are lit, press the appropriate ERROR pushbutton and observe that the indicator goes out.

11. Bring the tape transport up to a Ready condition.

12. Insure that the INT TEST switch on the exerciser is set to OFF.

13. Set the DENSITY REQUEST 2^0 and 2^1 switches to the following positions, depending upon the desired read or write density.

2^0	2^1	DENSITY
0	0	556 BPI
1	0	800 BPI
0	1	1600 BPI
1	1	Local-The density may be selected on the tape transport.

14. Observe that the DENSITY STATUS indicators light to indicate the density which has been selected either on the exerciser or at the tape transport.

15. Set the PARITY ERROR RESPONSE switch to either BACKSPACE, OFF, or TRAP. When set to OFF, the PARITY {ERROR} indicator lights but the program continues when a parity error is detected. When set to BACKSPACE, the exerciser will continue trying to reread or rewrite until the parity error no longer exists. When set to TRAP, the exerciser program continues but the word with the parity error is trapped in a register and may be displayed on the DISPLAY when the DISPLAY SELECT switch is set to READ.

16. Set the PATTERN switch to either TRUE or TRUE/COMP depending upon whether writing of the true value of the DATA switches or the true and alternating complement value of the DATA switches is desired.

17. Set the CLIPPING LEVEL switch to either HI, NORMAL, or LOW depending upon whether the high, normal, or low clip level of the read data from the tape transport is desired.

18. If a write operation is to be performed, set the 2^0 through 2^7 DATA switches to 1 if a "1" is to be written, to 0 if a "0" is to be written, or to E if it is desired to erase the track.

19. Set the P DATA switch to ON or OFF depending upon whether it is desired to generate automatic parity or to erase the parity track, respectively.

20. Set the RECORD LENGTH control to either ONE WORD or to a position from just off the ONE WORD position to the fully clockwise position, depending upon whether a one word record or a record from 2 to 100 milliseconds long is desired.

21. Set the PAUSE TIME control to either OFF or to a position from just off the OFF position to the fully clockwise position, depending upon whether a time between execution of program instructions from 6 microseconds in the OFF position to from 2 to 100 milliseconds is desired.

22. Set the MODE switch to LOAD.

23. Load the desired program into memory by pressing the START pushbutton to increment the program to the desired address, as indicated by the ADDRESS indicators, followed by pressing the appropriate INSTRUCTION pushbutton. Any of the four instructions (Forward, Reverse, Write, or Rewind) may be programmed at any of the eight addresses.

24. Set the 2^0, 2^1, and 2^2 BREAKPOINT switches to 1 or 0 depending upon the number of instructions to be executed. Refer to the following table.

2^2	2^1	2^0	INSTRUCTIONS
0	0	0	1
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	7
1	1	1	8

25. Set the MODE switch to STEP or RUN depending upon whether the program is to be executed one instruction per depression of the START pushbutton or continuously in sequence after one depression of the START pushbutton, respectively.

26. Set the OPERATION switch to CONTINUOUS, CONT REC, or RECORD. When set to CONTINUOUS, one instruction will be executed until either the Beginning of Tape or End of Tape is reached disregarding record gaps, then the program is incremented. When set to CONT REC one instruction will be executed until either the Beginning of Tape or End of Tape is reached, however record gaps will be written in the case of a Write operation or read in the case of a Read operation, then the program is incremented. When set to RECORD, an instruction is executed until a record gap is written or read, then the program is incremented.

27. Set the DISPLAY SELECT switch to the appropriate position to display the desired information on the DISPLAY. Refer to the DISPLAY SELECT position definitions printed on the lid on the top cover of the exerciser.

28. Set the IBM-CDC switch, located on logic card 1BEF at location B2, to either IBM or CDC depending upon whether the exerciser is connected to an IBM or CDC subsystem tape transport.

29. Press the START pushbutton to commence execution of the program instructions.

30. The program will halt any time that the INT CONTROL switch is set to MC.

31. When the TAPE CONTROL switch is set to REWIND or UNLOAD, the tape transport tape will rewind or unload as applicable.

32. Set the SIGNAL MONITOR switch to position 1 through 24 to display any of the applicable signals on the SIGNAL MONITOR indicator and made available for monitoring on the SIGNAL MONITOR test point. Refer to the names of the SIGNAL MONITOR signals printed on the lid on the cover of the exerciser.

33. Set the TAPE CONTROL switch to UNLOAD.

34. Remove tape from and power down the tape transport.

35. Set the AC POWER switch on the exerciser to OFF.

Section 3

Installation and Checkout

Section 3

Installation and Checkout

1.0 General

This section provides detailed information pertaining to crating and uncrating, site installation, and preparation for use.

2.0 Installation

2.1 Crating

Perform the following procedure. Refer to Figure 3-1.

1. Coil AC power cable and input/output cable and insert behind hinged center partition.
2. Insure six thumb screws holding exerciser main assembly in aluminum case are secure.
3. Insure AC POWER fuse and TIMER are secure in place in operator panel.
4. Close case cover and latch.
5. Insert exerciser in place in shipping carton, CDC Part Number 59322400, which may be ordered from Customer Engineering Materials. Refer to Figure 3-1.
6. Close carton covers and seal.

2.2 Uncrating

Perform crating procedure in reverse sequence. It is suggested that the cartons and packing be retained for future shipment.

2.3 Physical Limitations

When the cover case is opened completely, the exerciser requires an area approximately 18 inches high, 18 inches wide, and 18 inches deep. The exerciser weighs approximately 25 pounds. The input/output cable is ten feet long, therefore the exerciser must be placed on a workbench or other appropriate support which is within ten feet of the tape transport.

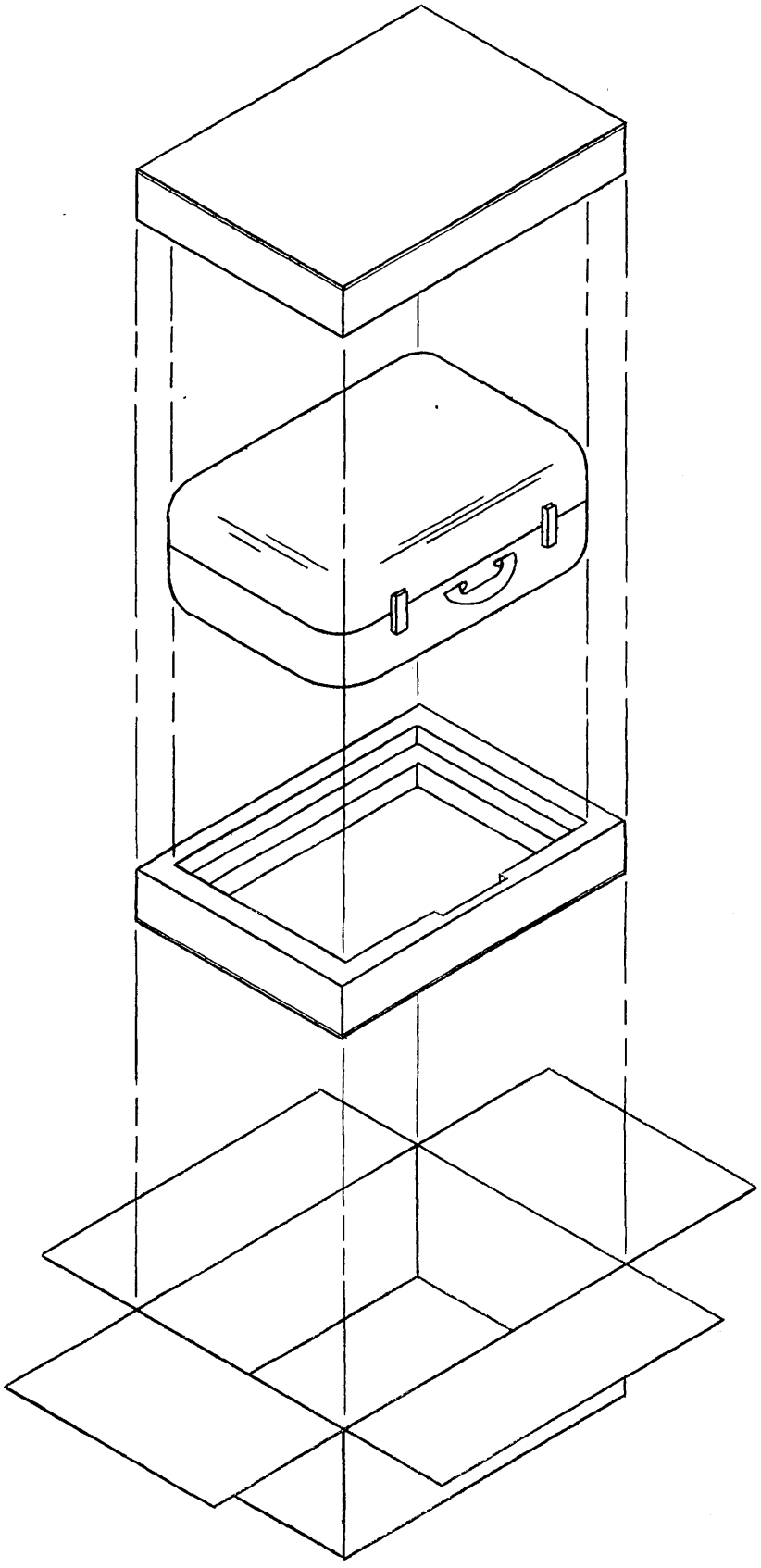


Figure 3-1. Recommended Packing Procedure Using Shipping Carton, CDC PN 59322400

2.4 Power Requirements

The exerciser requires either 120 volt AC, 60Hz, single phase, three wire power or 220 volt AC, 50Hz, single phase, two wire power. Normal operating power is 120 volt AC, 60Hz. If 220 volt AC, 50Hz is used, a wiring change must be made to the exerciser. Refer to Section 6, Maintenance, for procedures for wiring for either power source.

2.5 Cabling and Connectors

Two cables are supplied with the exerciser, an AC power cable and an input/output cable. The AC power cable is eight feet long and the input/output cable is ten feet long. The AC power cable has a female plug on one end to be inserted into the recessed male connector on the exerciser. The other end of the AC power cable has a two wire plus ground male plug to fit into a normal wall outlet. The AC power cable can be used for either 120 volts or 220 volts AC. The input/output cable has identical male 160-pin connectors on each end to mate with identical 160-pin female connectors on the exerciser and the tape transport.

2.6 Cooling Requirements

Operating temperature for the exerciser should be from 60°F (15.56C) to 90°F (32.22C). Recommended operating temperature is 75°F (23.89C). Maximum temperature gradient should be 5° per hour. Permissable non-operating temperature is -30°F (-34.44C) to 150°F (65.56C). Permissable operating and non-operating relative humidity is non-condensing 0 to 90 percent.

2.7 Preparation For Use

Perform the following before application of power.

1. Uncrate the exerciser.
2. Visually inspect the exterior of the case for dents or defects.
3. Open the case and check the operator panel for loose or broken components. Replacement procedures for site replaceable components are given in Section 6, Maintenance.
4. Remove the operator panel from the case by loosening the six knurled spring-loaded captive screws from the panel. Lift the panel straight up from the aluminum case.
5. Inspect the underside of the panel for broken wire, loose components, or bent connector pins.

6. Remove and inspect the two fuses on the DC power supply. Replace if necessary.

7. Insure that all the printed circuit cards are installed and are properly seated in the logic rack. Compare the logic card designator on the logic card with the card placement diagram printed on the bottom of the logic rack to insure that the cards are located properly.

8. Insure that there is an Equipment Identification Plate on the plate on the bottom of the card rack and that an FCO Log, form AA1870, is affixed to the inside bottom of the case.

9. Replace the panel in the case. If checkout procedure is to follow, the panel need not be replaced.

2.8 Checkout

1. Open the case cover.

2. Remove the operator panel from the case by loosening the six knurled spring-loaded captive screws and lifting the panel straight up from the case.

3. Remove and inspect the one ampere AC fuse. Replace if necessary.

4. Insure a 2000 hour cartridge is installed in the TIMER.

CAUTION

Do not connect the AC power cable until the exerciser has been inspected to insure it is wired properly for the power source to be used. Internal wiring changes are required to convert from 120 volt to 220 volt operation, or vice-versa.

5. Inspect terminal board TB1 under the operator control panel. Refer to Figure 6-5 for the location of TB1. If the exerciser is to be used for 120 volt operation one jumper should be connected between terminals 1 and 2 and one jumper should be connected between terminals 3 and 4. For purposes of identification, terminal 1 is closest to the underside of the operator panel. For 220 volt operation both jumpers should be connected between pins 2 and 3.

6. Remove the AC power cable from under the lid of the case cover.

7. Insure the AC POWER switch is set to OFF.

8. Insert the female plug on the AC power cable straight into the recessed, male AC POWER connection on the operator panel.

9. Set the INT TEST switch to ON.

10. Set the DENSITY REQUEST 2^0 and 2^1 switches to 0.

11. Set the DISPLAY SELECT switch to START.

12. Set the SIGNAL MONITOR switch to position 1.

13. Rotate the PAUSE TIME and RECORD LENGTH controls to the fully clockwise position.

14. Set the P DATA switch to ON.

15. Set the 2^0through 2^7DATA switches to 1.

16. Set the CLIPPING LEVEL switch to NORMAL.

17. Set the PATTERN switch to TRUE.

18. Set the PARITY ERROR RESPONSE switch to OFF.

19. Set the OPERATION switch to RECORD.

20. Set the MODE switch to LOAD.

21. Set the BREAKPOINT 2^0, 2^1, and 2^2 switches to 1.

22. Install the internal test plug connector onto the I/O connector.

23. Set the AC POWER switch to ON.

24. Observe the ERROR indicators. If any are lit, press the appropriate pushbutton and observe that the indicator goes out.

25. Observe that the READY {STATUS} indicator is lit, the DISPLAY indicates 000, and that one and only one of the INSTRUCTION indicators is lit.

26. Set the SIGNAL MONITOR switch to positions 1 through 24 and observe that the SIGNAL MONITOR indicator is lit at positions 1 through 9, 11 and 21.

27. Return the SIGNAL MONITOR switch to position 1.

28. Set the INT CONTROL switch to LAMP TEST.

29. Observe that all the indicators on the operator panel are lit and that the DISPLAY indicates 888.

30. Alternately press the START and appropriate INSTRUCTION pushbutton and load a Forward instruction at address 0, a Reverse instruction at address 1, a Write instruction at address 2, a Rewind instruction at address 3, a Forward instruction at address 4, a Reverse instruction at address 5, a Write instruction at address 6, and a Rewind instruction at address 7.

31. Set the INT CONTROL switch to MC.

32. Set the MODE switch to STEP. Observe that (INSTRUCTION) indicators toggle between WRITE and FORWARD in steps 33-36 when the START pushbutton is depressed.

33. Press the START pushbutton one time and observe that when it is pressed that the BUSY and FWD {STATUS} indicators blink. Also observe that the program address incremented to 2 as observed on the ADDRESS indicators.

34. Press the START pushbutton one time and observe that when it is pressed that the BUSY and REV {STATUS} indicators blink. Also observe that the program address incremented to 4.

35. Press the START pushbutton one time and observe that when it is pressed that the WRITE REPLY {STATUS} indicator lights and remains lit. Also observe that the program address incremented to 6.

36. Press the START pushbutton one time and observe that when it is pressed that the WRITE REPLY {STATUS} indicator remains lit. Also observe that the program address incremented to 0.

37. Set the MODE switch to RUN. PAUSE TIME and RECORD LENGTH controls to minimum CCW. Observe that BUSY, FWD and WRITE REPLY {STATUS} indicators and all ADDRESS and INSTRUCTION indicators are lit and running. (NOTE: The PARITY ERROR indicator may intermittently come on.)

38. Press the START pushbutton. Observe that the FORWARD, REVERSE, WRITE, and REWIND {INSTRUCTION} indicators are blinking in sequence. Also observe that the ADDRESS indicators are Lit, indicating the program is executing. Also observe that the BUSY, FWD, REV, and WRITE REPLY {STATUS} indicators are Lit and that the SIGNAL MONITOR indicator is Lit.

39. Observe the DISPLAY. It should indicate between 004 and 010.

40. Set the DISPLAY SELECT switch to RECORD GAP. Observe that the DISPLAY is changing values.

41. Set the DISPLAY SELECT switch to READ. Observe that the DISPLAY indicates 777.

42. Set the DISPLAY SELECT switch to ADDRESS. Observe that the DISPLAY indicates 020.

43. Set the DISPLAY SELECT switch to MODEL and observe that the DISPLAY indicates 200.

44. Set the DISPLAY SELECT switch to FAULT and observe that the DISPLAY indicates 000.

45. Set the DISPLAY SELECT switch to READ.

46. Set the P DATA switch to OFF.

47. Set RECORD LENGTH to maximum CW and observe the DISPLAY. It should alternate between 377 and 777.

48. Observe that the PARITY {ERROR} indicator is lit.

49. Set the PARITY {ERROR} RESPONSE switch to BACKSPACE.

50. Observe that the PARITY {ERROR} indicator is blinking and that the program is executing as observed on the ADDRESS indicators and that the INSTRUCTION indicator are sequencing. Also observe that the BUSY, FWD, REV, and WRITE REPLY {STATUS} indicators are blinking.

51. Set the PARITY ERROR RESPONSE switch to TRAP. Observe that the PARITY {ERROR} indicator is lit.

52. Set the P DATA switch to ON.

53. Set the 2^0 through 2^7 DATA switches to 0.

54. Observe the DISPLAY. It should alternate between 400 and 777.

55. Press the PARITY {ERROR} pushbutton and observe that the DISPLAY alternates between 400 and 777 and that the PARITY {ERROR} indicator blinks.

56. Set the PARITY ERROR RESPONSE switch to OFF.

57. Set the OPERATION switch to CONT REC. Observe that the program has stopped and that the WRITE {INSTRUCTION} indicator is lit. Also observe that the BUSY and FWD {STATUS} indicators are blinking and that the WRITE REPLY indicator is lit.

58. Set the INT CONTROL switch to MC. Observe that the RDY and WRITE REPLY {STATUS} indicators are lit. Also observe that the FWD {INSTRUCTION} indicator is lit.

59. Press the START pushbutton.

60. Set the OPERATION switch to CONTINUOUS. Observe that the BUSY, FWD and WRITE REPLY {STATUS} indicators are lit.

Section 4

Theory of Operation

Section 4

Theory of Operation

1.0 Introduction

The theory of operation for the exerciser is divided into four levels. They are as follows:

Level 1 General Description

This is a brief description of the operation of the major parts of the exerciser. The major parts are depicted in an overall exerciser block diagram. This description is intended for the person who needs only a brief understanding of the function and capabilities of the exerciser, therefore no detailed description of the exerciser operation is included. The general description is included in this section.

Level 2 Functional Description

This is a detailed description of the operation of the exerciser. It is supported by appropriate timing diagrams and is supplemented by information in Section 1 including interface pin assignments and interface signal descriptions. It is also supplemented by information in Section 2 including the complete description of all operator controls and indicators.

The functional description is intended for the person who needs to know in detail how the exerciser operates but who does not need to know how individual circuits and components work. The functional description is included in this section.

Level 3 Circuit Descriptions

The circuit descriptions are included in Section 5, Diagrams. They describe the operation of every logic circuit, power distribution diagram, and control panel schematic in the section and are located on the page facing the diagram. They are intended for use by the Customer Engineer in troubleshooting the exerciser.

Level 4 Circuit Element Description

The circuit element descriptions are included in Section 7, Maintenance Aids. They describe the operation of every integrated circuit and discrete component circuit in the exerciser. They are supported by truth tables, logic diagrams, and timing diagrams. They are intended to be used by the Customer Engineer primarily for isolating malfunctions down to the individual integrated circuit and discrete component circuit level.

2.0 General Description

The exerciser receives hardware status and address information from the tape transport. The hardware status indicates the speed of the tape transport and the method of recording, i.e., NRZI or Phase Encoded. The address indicates the unit number of the tape transport that is connected to the exerciser. The exerciser then transmits requests to the tape transport which have been programmed into the exerciser by the operator. The request may be motion commands, rewind or unload, write or read, density request, or read clip level. When the tape transport receives the requests it transmits back operation status, which includes such information as write status, busy, ready, beginning of tape, end of tape, velocity, density, and tachometer pulses. The exerciser then either transmits write data to the tape transport or receives read data from it depending upon the program instructions. Correct parity is either checked or generated depending upon whether the operation was read or write, respectively. During the read or write operation error checking of the operation is continually performed. In addition, faults which may occur within the tape transport are transmitted to and displayed by the exerciser.

All interface between the exerciser and the tape transport is through the input/output section of the exerciser, which consists of the input/output connector and cable and the transmitters and receivers. Refer to Figure 4-1 for a diagram depicting the relationships between the major sections of the exerciser and the tape transport.

Control of exerciser operations and storage of instructions is accomplished by the program control and memory section. The operator control panel ADDRESS indicators, BREAKPOINT switches, and INSTRUCTION pushbutton-indicators are used to store up to eight instructions in a two-bit by eight-address memory. Tape Transport density is selected by the DENSITY REQUEST switches. The MODE switch, OPERATION switch, and START pushbuttons control the operation sequence of the exerciser. The length of time between execution of instructions and the length of a record are controlled by the PAUSE TIME and RECORD LENGTH controls, respectively. A non-programmed unload or rewind operation can be initiated by the TAPE CONTROL switch. The exerciser can be master cleared or a lamp test may be performed by the INT CONTROL switch. To check for proper operation of the exerciser, an internal test may be made by the INT TEST switch.

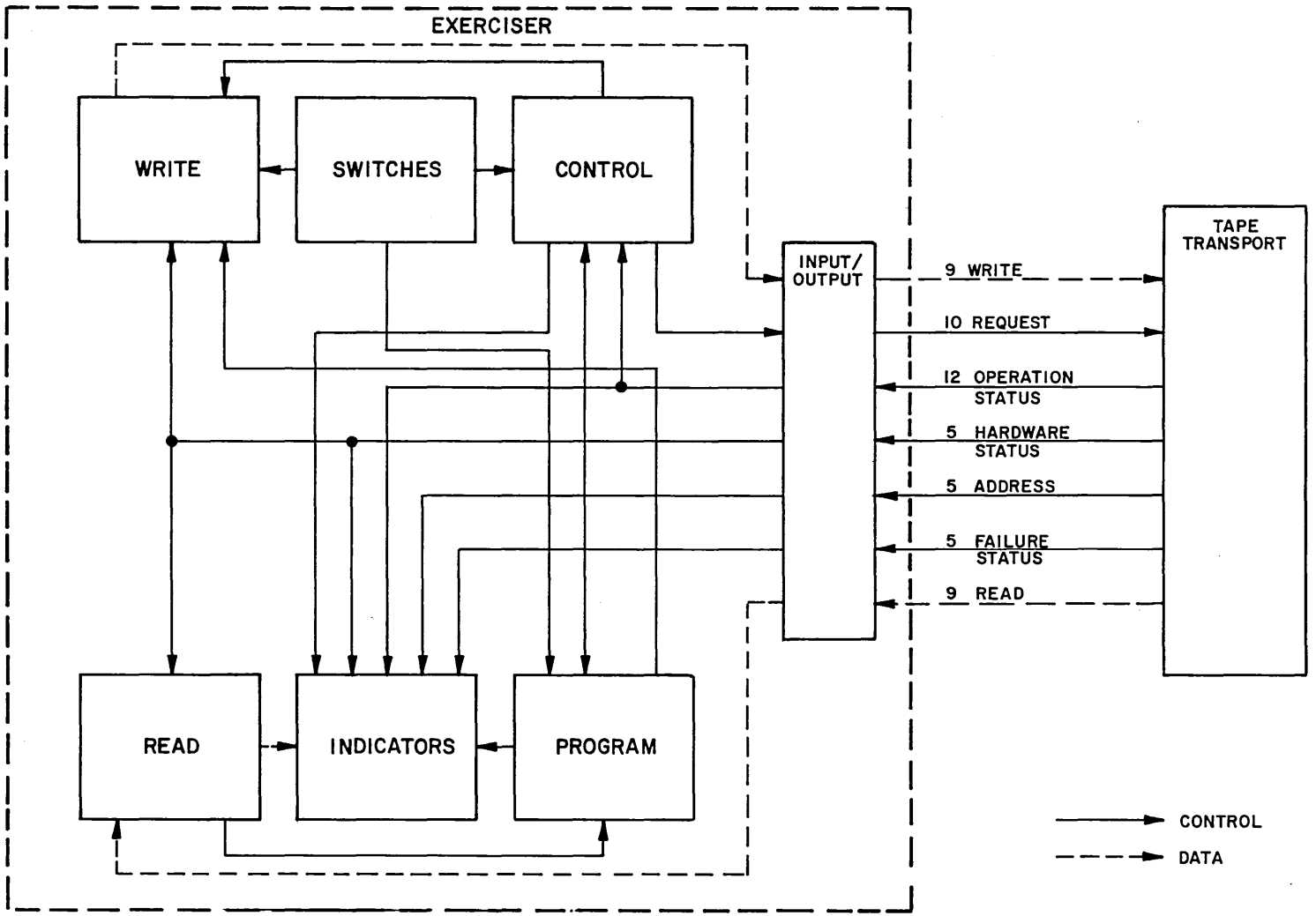


Figure 4-1. Exerciser Block Diagram

Writing data on the tape transport tape is accomplished by the write section. Ones or zeros may be written on any track by setting the DATA switches to the appropriate setting. The true or alternating true and complement output of the data switch settings can be selected by the PATTERN switch. Odd parity will be generated if enabled by the P DATA switch.

Whenever a forward or reverse motion is commanded without a write command, a read operation will be performed. Odd parity will be checked if enabled by the P Data switch. A high or low read clip level may be selected by the CLIPPING LEVEL switch.

When enabled by the P DATA switch, odd parity is generated by the exerciser during a write operation and checked during a read operation. When a parity error is detected the PARITY ERROR indicator lights. The exerciser will either backspace and attempt to re-execute without a parity error or will trap and display the word with the parity error, depending upon the setting of the PARITY ERROR RESPONSE switch. Errors in tape transport operation detected by the exerciser are displayed on the ERROR indicators. When the tape transport detects a fault or malfunction in its operation, an indication is transmitted to the exerciser and is displayed on the DISPLAY.

The display section of the exerciser provides a visual indication of operational and hardware status. The STATUS indicators light to indicate the operational status of both the exerciser and the tape transport. The DISPLAY indicators provide both the operational status and the hardware status of the tape transport. The desired status may be selected by the DISPLAY SELECT switch. The SIGNAL MONITOR switch provides the ability to select different signals for display on the SIGNAL MONITOR indicator and for observation on an oscilloscope at the SIGNAL MONITOR jack.

3.0 Functional Description

3.1 General Exerciser Operating Conditions

Pressing the START pushbutton initiates exerciser operation. A Forward, Reverse, Write, or Rewind command is transmitted to the tape transport when START is pressed. The tape transport returns a Busy signal when it receives the motion command, indicating that tape is in motion. Write data is then transmitted to the tape transport if a write operation is to be performed, or read data is received by the exerciser if a read operation is to be performed. When a write operation is performed, read data is transmitted back to the exerciser for parity checking. Since the tape transport does not generate an End of Operation signal, the exerciser must determine when an operation has ended and then generate its own signal. This is done by the exerciser when it detects that there has been read data followed by a period of 50 microseconds when there has been no read data. An internal exerciser End of Operation signal is then generated. The End of Operation signal removes the motion command. An End of Tape or Beginning of Tape

signal also generates an End of Operation signal and removes the rewind command. When the tape transport Busy signal goes low the exerciser timing chain is initiated. When the Time 6 pulse occurs, another motion command will be transmitted to the tape transport if the exerciser is in the RUN mode. If it is in the STEP mode another operation cannot be initiated until the START pushbutton is again pressed. Refer to the following timing diagram.

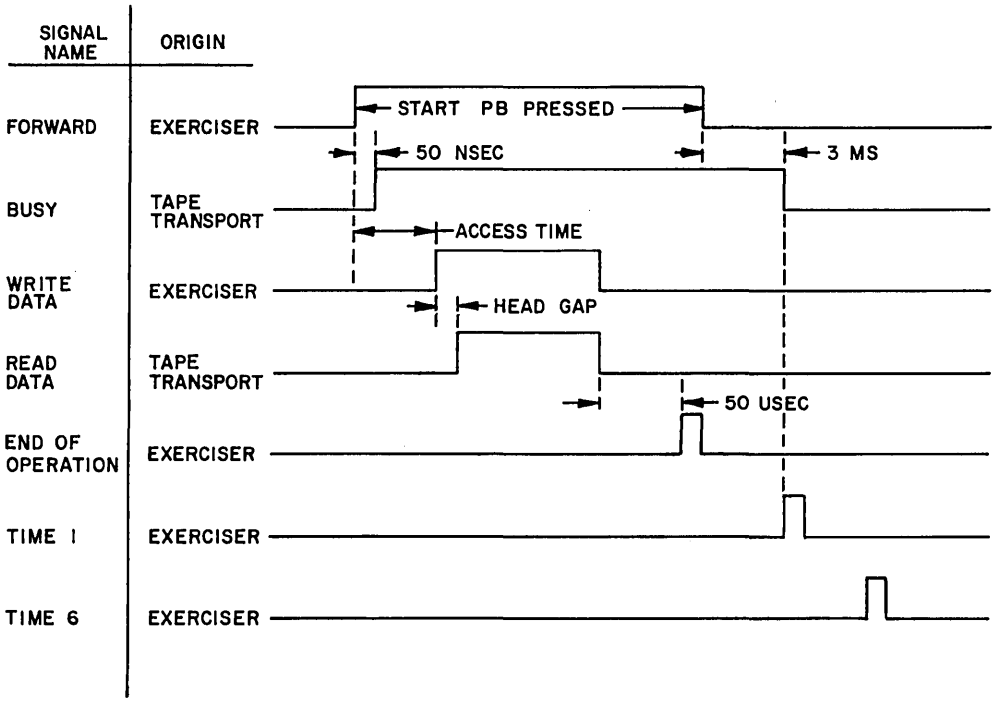


Figure 4-2. General Operation Timing Diagram

The exerciser read and write functions are conditioned by the recording mode (NRZI or PE), tape speed (100, 150 or 200 IPS), and number of tracks (7 or 9) information from the tape transport.

3.2 Write Operation

The exerciser initiates a Write operation by raising the Forward line, then raising Write Request no later than 200 nanoseconds after Forward. When a write operation is initiated, the tape transport returns a Busy within 50 nanoseconds after the Forward and Write Request signals are activated by the Exerciser, indicating that tape is in motion. Write reply is activated by the tape transport within 50 nanoseconds after Busy, indicating that the tape transport has turned on the write current and erase heads. The Velocity signal is sent to the exerciser when the tape is up to speed. The tape transport sends the Write Permit signal after a given period of time has elapsed for inter-record gap generation. When Write Permit is received the exerciser begins outputting data. The exerciser cannot output data unless Write Permit is active.

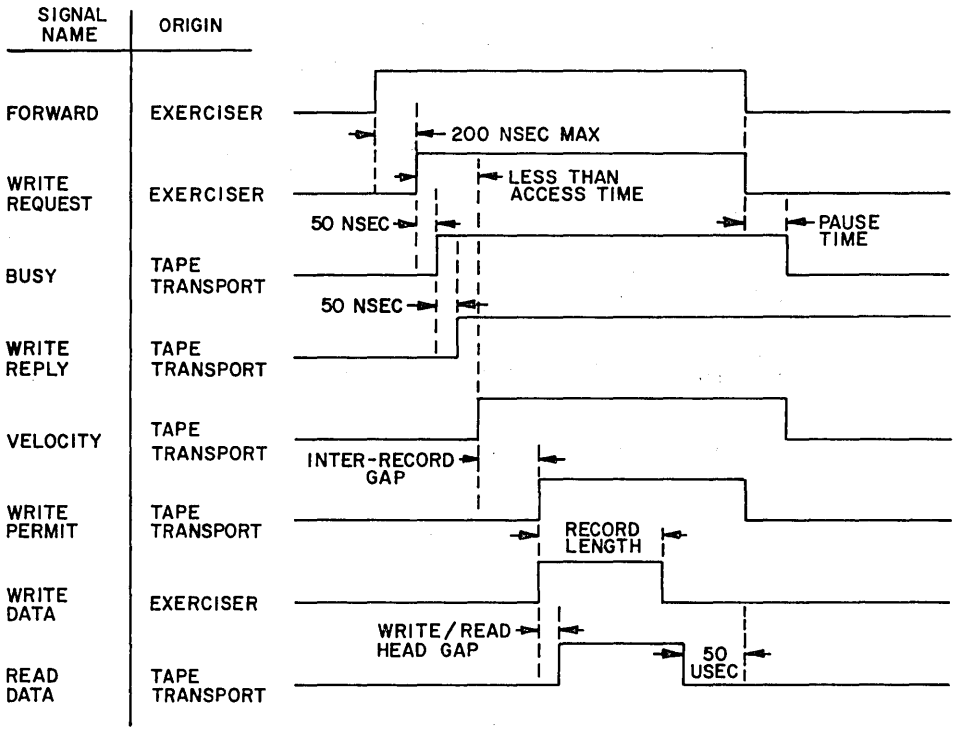


Figure 4-3. Write Timing Diagram

The PATTERN switch permits the value selected by the DATA switches to be output as a true value (TRUE position) or as alternating true and complement words (not alternating records), beginning with a true word output. If TRUE/COMP is selected, in conjunction with the ONE WORD position of the RECORD LENGTH control, all output words will be true (one word record, first word must be true). The method and rate of recording (NRZI or PE) depends on the Density Status of the tape transport.

The DATA switches for bits 2^6 or 2^7 are sampled or not sampled for automatic parity generation depending on the track information received from the tape transport. A seven-track tape unit does not require these bits, so the exerciser does not include these bits in automatic parity generation.

Parity generation is automatically generated as a correct odd value when the "P" DATA switch is in the ON position. With this switch in the OFF position, the parity output line is held at logical "0" (i.e., erase). This is not necessarily incorrect parity, since 2^0 through 2^7 may be set for an odd number of bits, thus not requiring the generation of a parity bit.

When data are being output, they are also simultaneously being returned to the exerciser via the read heads and the Read lines and are continually being checked for proper parity. If an error is detected during a write, the exerciser will command a backspace with an attempt to re-execute without a parity error or will trap and display the word, depending upon the setting of the PARITY ERROR RESPONSE switch.

The CLIPPING LEVEL switch is used by the exerciser to enable a higher (HI position) or lower (LOW position) Read Threshold at the tape transport. In the HI or LOW position, the High Clip Select or Low Clip Select line, respectively, is held at logical "1" by the exerciser, until the switch is moved to the NORMAL position, wherein both Clip Select lines are held at logical "0".

The length of a write operation is controlled by the RECORD LENGTH control if the OPERATION switch is in the RECORD position. The control provides the capability of varying the length of a record from 1 data word (in the detented position) or from 2 millisecond (nominal) to approximately 100 millisecond (nominal) under potentiometer control. When the control knob is rotated to its fully counter-clockwise limit (in the detented position), the switch is OFF and the potentiometer is disabled. This position is labeled ONE WORD. When a write is initiated in the NRZI recording mode with this selection, two words are actually output. The exerciser, in this case, is simulating the fact that a one-word write from the Tape Control Unit (TCU) also consists of two words: a data word and an LRC (Longitudinal Redundancy Check) word. The two corresponding words from the exerciser, however, are identical to each other and consist of the pattern selected by the PATTERN switch. In the Phase Encoded recording mode, only one word is output. This value is also the same as the settings of the DATA switches.

Rotating the RECORD LENGTH control clockwise turns the switch ON and enables the potentiometer. The exerciser outputs an even number of words in NRZI, regardless of the setting of the potentiometer. In the Phase Encoded mode, an odd or even number of words may be output, depending on the exerciser internal timing.

With the OPERATION switch in the CONTINUOUS position, the Write Operation is terminated automatically when the exerciser senses End of Tape or Beginning of Tape or by manual operator intervention, but is continuous until one of these actions occurs.

When the exerciser drops the Write Request and Forward lines, the tape transport should drop Write Permit within 50 nanoseconds. After a maximum of 1 millisecond, Velocity drops. Busy drops within the Stop time period, which varies depending upon the model tape transport.

The exerciser prepares, during a write operation, to perform a Write Jog sequence. However, this Write Jog sequence is not performed until reverse motion is requested under program control. Write Jog is not performed for a manual Rewind or Unload as initiated by the TAPE CONTROL switch. The tape transport keeps Write Reply active until the Exerciser requests reverse motion.

3.3 Read

A read operation is performed when the exerciser raises the Forward line or the Reverse line without raising the Write Request line. The inactive state of the Write Request line with the active state of a motion line is interpreted as a read by the tape transport.

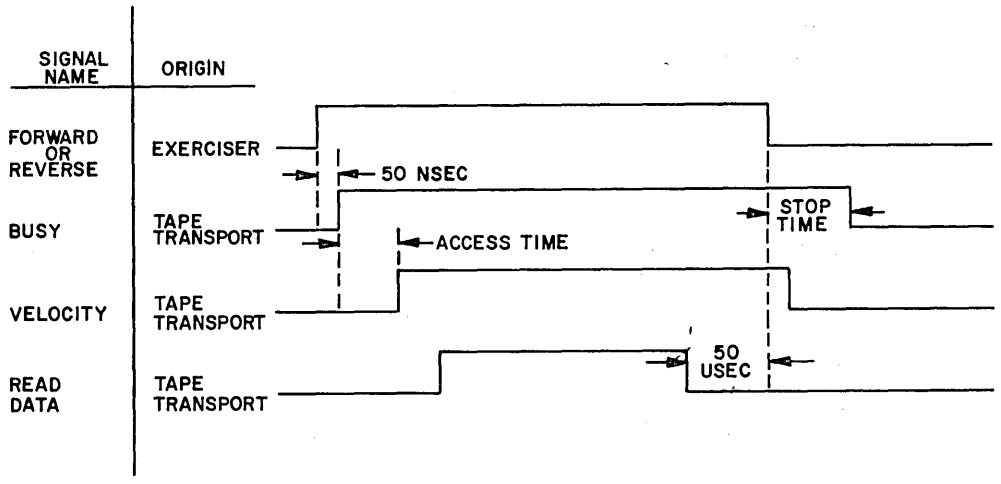


Figure 4-4. Forward or Reverse Read Timing Diagram

Data are returned on the Read lines and are displayed in octal by the DISPLAY indicators, if the DISPLAY SELECT switch is in the READ position. These data are continually being checked for odd parity. The absence of data for 50 microseconds is interpreted by the exerciser as the end of a record gap, and the exerciser generates its own internal End of Operation.

The Write Jog sequence is performed any time a Write operation is followed by either a Reverse Read operation or a Rewind operation while under program control. This sequence consists of a Forward signal which is 77_8 Tachometer pulses in duration. Although the absence of Write Request would normally mean a read operation, Write Reply is still active, signifying that the erase heads are still on. Thus, during the time that Busy is active for the Write Jog sequence, the erase heads are creating a one-inch record gap. The exerciser begins the reverse read by raising the Reverse line as soon as the tape transport drops Busy. The tape transport detection of the active state of the Reverse line drops Write Reply.

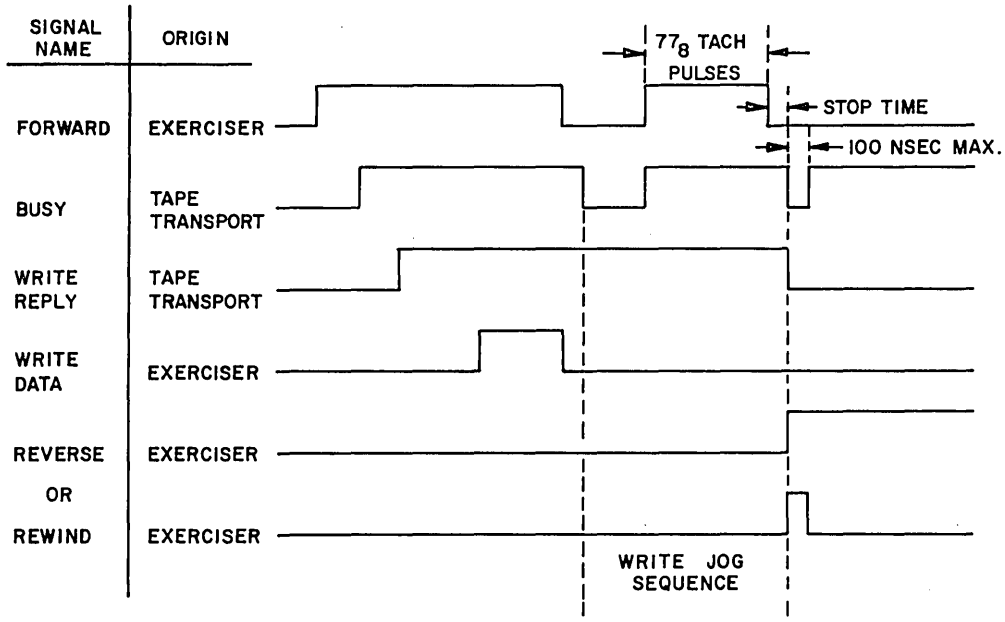


Figure 4-5. Write Jog Sequence Timing Diagram

3.4 Rewind

The rewind operation may be initiated by the exerciser under the control of the PROGRAM CONTROL section or by momentarily placing the TAPE CONTROL switch in the REWIND position. The Rewind signal is sent to the tape transport as a 1 microsecond pulse. Once this operation has been initiated, the exerciser cannot take further actions until the Beginning Of Tape (BOT) marker is sensed by the tape transport and returned to the exerciser via the BOT Status line.

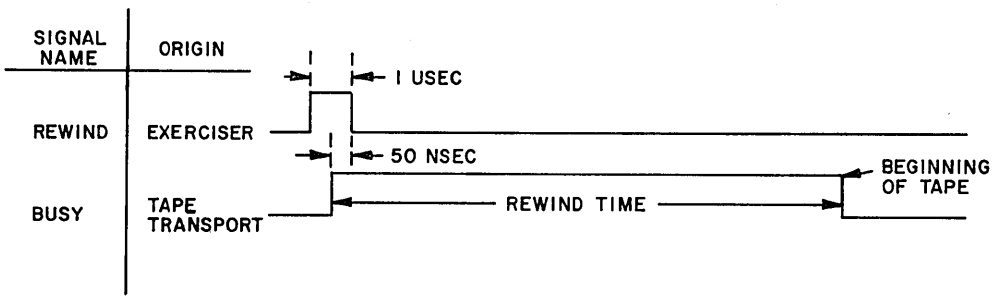


Figure 4-6. Rewind Timing Diagram

3.5 Unload

The unload operation is initiated by the exerciser only when the TAPE CONTROL switch is momentarily placed in the UNLOAD position. The Unload signal is a 1 microsecond pulse. Once this operation has been initiated, the exerciser cannot take further actions until the tape has been reloaded and brought to the BOT marker.

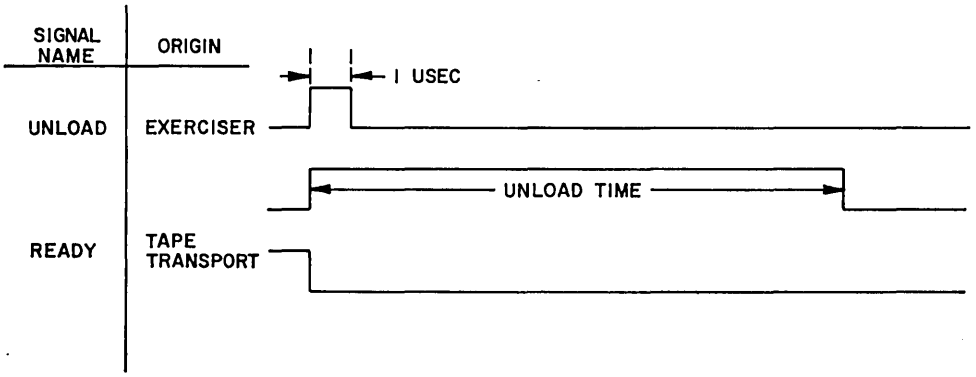


Figure 4-7. Unload Timing Diagram

3.6 Error Detection

Four errors are detected by the exerciser. They are Write Permit Error, Fault Error, Velocity Error, and Parity Error. These are defined below.

Write Permit Error:	The tape transport raised the Write Permit line before raising the Velocity signal.
Fault:	The tape transport has activated one of the five Fault lines.
Velocity:	The tape transport dropped the Velocity line for 100 nanoseconds minimum while a motion line was active.
Parity:	The exerciser has detected even {incorrect} parity during a Write or Read operation during the period when sampling is permitted. The sampling period which the Exerciser uses depends on the tape speed of the transport.

The ERROR section consists of the WRITE PERMIT, FAULT, VELOCITY, and PARITY pushbutton/indicators.

Write Permit, Fault, and Velocity Errors, once detected are retained until the associated pushbutton is pressed, provided the error is not steady state. An Error is cleared by pressing the associated pushbutton. Momentarily setting the INT CONTROL switch to the MC position will clear a Parity error only.

The first parity sampling period begins upon the first detection of any bit on the Read Data lines and ends after a period which depends on the tape speed as shown in the chart below.

Tape Speed	Sampling Period (nominal)
100ips (75ips for 34XXX)	3.0 microsecond
150ips (125ips for 34XXX)	2.0 microsecond
200ips	1.5 microsecond

At the end of the sampling period, parity is checked. Following the check, the next bits on the Read Data lines trigger another sampling period. Thus, the sampling period is the word time and establishes the maximum skew period within which the exerciser can accurately detect parity errors.

The PARITY ERROR RESPONSE switch determines how the exerciser will respond to a detected parity error. With the OFF position selected, no action, other than the indication, is taken by the exerciser. With TRAP selected, the exerciser halts parity detection on the word containing the error by retaining the erroneous word in an internal register. Motion signals continue to be generated. The value of a retained (trapped) word is displayed on the DISPLAY when the DISPLAY SELECT switch is set to READ. The operator's only indications that a word has been trapped are the illumination of the PARITY ERROR indicator, in conjunction with the fact that TRAP has been selected. Following a trapped parity error, pressing the PARITY pushbutton will clear the error indication and clear the trap register.

When the PARITY ERROR RESPONSE switch is in the BACKSPACE position and a parity error is detected, the PARITY ERROR indicator lights and then immediately goes out. Tape motion momentarily stops and then starts, with tape motion in the opposite direction that it was in when the parity error occurred. When the tape has backed over the word where the parity error occurred it will again momentarily stop. The program address counter does not advance. The instruction is re-executed in an attempt to write or read without a parity error. If the parity error re-occurs the exerciser will continue trying to backspace and re-execute until the parity error does not occur.

3.7 Restrictions

Certain restrictions are imposed on the operation of the Exerciser PROGRAM CONTROL section by design parameters of both the exerciser and the tape transport. These restrictions are discussed below.

A Rewind instruction in the memory must be immediately followed by a command involving forward motion. If a Rewind is followed by a Rewind, the exerciser will recognize the transition of Busy to logical "0", indicating the tape transport has reached Beginning of Tape following the first Rewind, and will output another Rewind pulse. However, the tape transport ignores Rewind commands while sensing BOT and will ignore the second Rewind command. Thus, the Exerciser will hang, waiting for the transition of Busy to logical "0". If a Rewind is followed by a Reverse command, the Exerciser will not attempt to activate the Reverse line and will halt. Both of the two conditions just discussed involve attempts to initiate reverse motion, other than Unload, while BOT is being sensed.

A write operation initiated by the exerciser while the BOT line from the tape transport is active does not begin outputting data until 377_8 Tachometer pulses from the tape transport have been counted by the Exerciser, following the tape transport de-activation of BOT.

A Write instruction in the memory must not be immediately followed by a Forward instruction. A reverse motion signal must be generated to allow the exerciser to generate a Write Jog sequence. The Forward instruction following a Write instruction would involve a read with Write Reply (erase heads on) still active, and is an undefined operation.

The exerciser will not attempt an operation involving forward motion while End of Tape (EOT) is being sensed. Thus, a Forward write or read must be followed by a Reverse or Rewind instruction, if the detection of EOT as a result of the forward operation is anticipated (OPERATION switch in the CONTINUOUS position).

The Exerciser is capable of detecting parity errors from Phase Encoded tapes only if the tape contains a pattern of all 1's.

Section 5

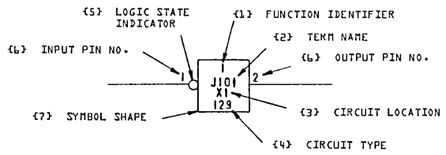
Diagrams

SYMBOL INDEX

The following is an alphanumeric listing of every logic symbol shown on the logic drawings, along with the manual page number on which that term is shown.

REVISIONS					
REV.	E.C.O.	DESCRIPTION	DATE	CHK'D	APP'D.
A		DRAWING RELEASE			

BASIC SYMBOL NOTATION



THIS SYMBOL IS TYPICAL OF THOSE USED IN THE DIAGRAMS SECTION. THE NUMBERS IN PARENTHESES CORRESPOND TO THOSE ASSOCIATED WITH THE PERTINENT DEFINITIONS BELOW.

DEFINITIONS

{1} FUNCTION IDENTIFIER

THIS LETTER (OR LETTERS) OR SYMBOL INDICATES THE OVERALL FUNCTION OF THE LOGIC SYMBOL. THE ABBREVIATED IDENTIFIERS ARE DEFINED BELOW.

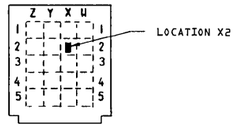
&	=	AND
1	=	OR
=1	=	EXCLUSIVE-OR
J-K	=	J-K FLIP-FLOP
REC	=	RECEIVER
XMT	=	TRANSMITTER
MUX	=	MULTIPLEXER
CNTR	=	COUNTER
SHREG	=	SHIFT REGISTER
⎍⎍	=	ONE SHOT
MODE	=	ODD PARITY GENERATOR/CHECKER
OD	=	EVEN PARITY GENERATOR/CHECKER
MEM	=	MEMORY

{2} TERM NAME

THIS ALPHA-NUMERIC DESIGNATOR IS USED TO IDENTIFY A PARTICULAR CIRCUIT ELEMENT, WHICH MAY BE ONE OF SEVERAL OF THE SAME TYPE. THIS DESIGNATOR IS UNIQUE FOR EACH SYMBOL WITHIN THE EXERCISER AND IS PROVIDED AS AN AID IN THE DISCUSSION OF THE THEORY OF OPERATION.

{3} CIRCUIT LOCATION

THE CIRCUIT LOCATION REFERS TO THE PHYSICAL LOCATION OF AN ELEMENT ON A PRINTED CIRCUIT CARD. THIS LOCATION IS DERIVED FROM THE GRID COORDINATES WHICH ARE USED ON EACH CARD. THERE ARE 20 (4 COLUMNS, 5 ROWS) ON A CARD. ONE CARD (A1AZF) HAS 5 COLUMNS AND 5 ROWS. COLUMN X HAS A CHIP AT ROW 2 ONLY. AS AN EXAMPLE OF THE USE OF THIS COORDINATE LOCATING SCHEME, SEE X2 BELOW.



COMPONENT SIDE

{4} CIRCUIT TYPE

THIS IS EITHER A NUMERIC OR ALPHA-NUMERIC IDENTIFIER WHICH REFERS TO THE TYPE OF CIRCUIT THE SYMBOL REPRESENTS. THE CIRCUIT TYPES USED IN THE EXERCISER ARE LISTED BELOW. REFER TO THE MAINTENANCE AIDS SECTION FOR DETAILED DESCRIPTIONS OF EACH TYPE.

INDUSTRIAL DTL	
TYPE	GENERAL FUNCTION
122	DUAL 4-INPUT GATE
126	QUAD 2-INPUT GATE
128	TRIPLE 3-INPUT GATE
129	HEX 1-INPUT INVERTER
150	DUAL J-K FLIP-FLOP
151	DUAL J-K FLIP-FLOP

TTL	
TYPE	GENERAL FUNCTION
140	QUAD 2-INPUT NAND GATE
146	HEX INVERTER
149	QUAD 2-INPUT EXCLUSIVE-OR GATE
170	DUAL 4-INPUT MULTIPLEXER
189	QUAD 2-INPUT MULTIPLEXER
195	DUAL MONOSTABLE MULTIVIBRATOR
240	DUAL J-K FLIP-FLOP
500	SYNCHRONOUS 4-BIT BINARY UP/DOWN COUNTER
502	8-BIT ODD/EVEN PARITY GENERATOR/CHECKER
514	16-BIT REGISTER FILE
515	5-BIT SHIFT REGISTER

DTL/TTL COMPATIBLE INTERFACE	
TYPE	GENERAL FUNCTION
162	DUAL DIFFERENTIAL RECEIVER
176	DUAL LINE DRIVER

{5} LOGIC STATE INDICATOR

THE LOGIC STATE INDICATOR IS A 0.125 INCH DIAMETER CIRCLE LOCATED ADJACENT TO THE LOGIC SYMBOL AND IN A LINE WITH THE INPUT OR OUTPUT.

LOGIC "0" OUTPUT - THE PRESENCE OF A CIRCLE ON AN OUTPUT LINE INDICATES THAT THE LOGIC FUNCTION HAS AN OUTPUT OF LOGIC "0" WHEN THE FUNCTION IS SATISFIED.

LOGIC "1" OUTPUT - THE ABSENCE OF A CIRCLE ON AN OUTPUT LINE INDICATES THAT THE LOGIC FUNCTION HAS AN OUTPUT OF LOGIC "1" WHEN THE FUNCTION IS SATISFIED.

WITH INVERTER LOGIC THE USE OF & TO DENOTE "AND" IS ACTUALLY THE ABBREVIATION FOR "NAND" AND "1" IS ACTUALLY THE ABBREVIATION FOR "NOR", WITH A LOGIC "1" INPUT TO A "NOR" DEFINED AS +0.2 VDC. THUS, THE CIRCLE ON THE INPUT TO A LOGIC "NOR" FUNCTION DENOTES A STATE WHICH IS OPPOSITE TO THE STANDARD -- I.E., A CIRCLE INDICATES THAT THE SIGNAL IS AT +0.2 VDC WHEN AT LOGIC "1".

THE CIRCLE ON THE INPUT OF A "NAND" DENOTES THE "INHIBIT" STATE -- I.E., IF THE INPUT BECOMES LOGIC "0", THE INDICATED FUNCTION OF THE "NAND" IS INHIBITED.

THE STANDARD LOGIC LEVELS ARE LISTED BELOW, AND ARE DEFINED FOR STRAIGHT-LINE INPUTS TO A "NAND".

INDUSTRIAL DTL LOGIC "1"	+5.0VDC (NOMINAL)
INDUSTRIAL DTL LOGIC "0"	+0.2VDC (NOMINAL)
TTL LOGIC "1"	+3.3VDC (NOMINAL)
TTL LOGIC "0"	+0.2VDC (NOMINAL)

{6} INPUT/OUTPUT PINS

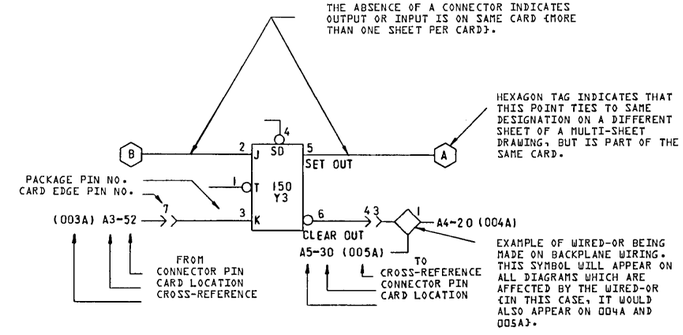
THE NUMBER OF AN INPUT OR OUTPUT PIN IS NORMALLY LOCATED ABOVE THE ASSOCIATED SIGNAL LINE AND ADJACENT TO THE SYMBOL OUTLINE.

{7} SYMBOL SHAPE

UNIFORM SHAPE (I.E., RECTANGULAR FORM) SYMBOLOGY IS USED FOR ALL INTEGRATED CIRCUIT ELEMENTS, INCLUDING MSI. THE SIZE OF THE SYMBOL IS DETERMINED BY THE NUMBER OF INPUT/OUTPUT PINS WHICH MUST BE USED.

LOGIC DIAGRAM TAGGING INFORMATION

1. A CARD MAY REQUIRE MORE THAN ONE SHEET.
2. INPUTS ARE SHOWN ON THE LEFT SIDE AND OUTPUTS ARE SHOWN ON THE RIGHT.



REFERENCE DRAWING			
COMPONENTS EXCEPT AS NOTED	TOL	VALUE	SIZE
RES.			
CAP.			

DRAFTSMAN	B. Peterson	2/15/72
CHECKER	M. Peterson	2/16/72
ENGINEER	J. O. Rued	17FEB72
APPROVAL	DSC	18FEB72
	J. A. Rued	18Feb72

CONTROL DATA CORPORATION
CUSTOMER ENGINEERING DIVISION

KEY TO LOGIC SYMBOLOGY

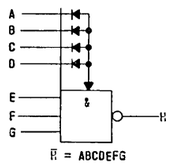
PRODUCT	SIZE	DRAWING NUMBER	REV.
TB111-A01	D	59340600	A
PAGE		SHEET 1 OF 2	

CODE IDENT 34011

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		DRAWING RELEASE	PC			

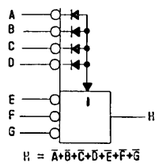
SYMBOLOGY EXAMPLES

AND GATE WITH EXTENDED INPUT



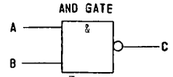
$\overline{H} = ABCDEFG$

OR GATE WITH EXTENDED INPUT



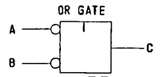
$H = \overline{A}+\overline{B}+\overline{C}+\overline{D}+\overline{E}+\overline{F}+\overline{G}$

AND GATE



$\overline{C} = AB$

OR GATE

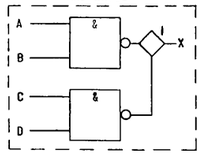


$C = \overline{A}+\overline{B}$

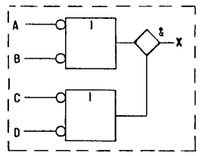
AND/OR GATE TRUTH TABLE

A	B	C
0	1	1
1	0	1
1	1	0

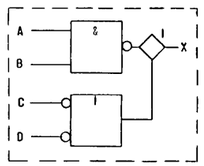
WIRED-OR FED BY TWO AND GATES



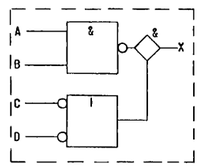
WIRED-AND FED BY TWO OR GATES



WIRED-OR FED BY AN AND GATE AND AN OR GATE



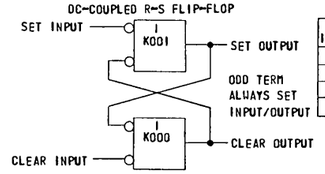
WIRED-AND FED BY AN AND GATE AND AN OR GATE



TRUTH TABLE FOR WIRED-AND/OR [APPLIES TO ENTIRE CIRCUIT (ENCLOSED BY DOTTED LINES) REPRESENTED BY TWO LOGIC ELEMENTS AND WIRED-AND/OR OUTPUT.]

A	B	C	D	AND/OR (X)
0	0	0	0	1
1	0	0	0	1
0	1	0	0	1
1	1	0	0	0
0	0	1	0	1
1	0	1	0	1
0	1	1	0	1
1	1	1	0	0
0	0	0	1	1
1	0	0	1	1
0	1	0	1	1
1	1	0	1	0
0	0	1	1	0
1	0	1	1	0
0	1	1	1	0
1	1	1	1	0

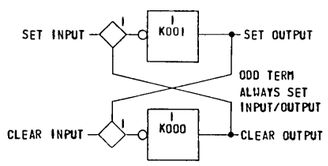
OR GATES INTERCONNECTED TO FORM A DC-COUPLED R-S FLIP-FLOP



LOGIC CHARACTERISTICS

SET INPUT	CLEAR INPUT	SET OUTPUT	CLEAR OUTPUT
1	1	NO CHANGE	
1	0	0	1
0	1	1	0
0	0	1	1

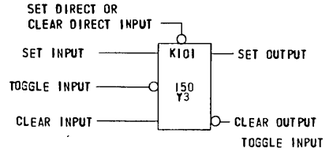
OR GATES INTERCONNECTED TO FORM A WIRED-OR FLIP-FLOP



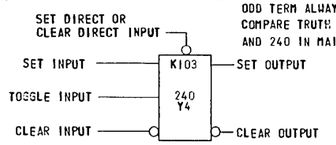
LOGIC CHARACTERISTICS

SET INPUT	CLEAR INPUT	SET OUTPUT	CLEAR OUTPUT
1	1	NO CHANGE	
1	0	0	1
0	1	1	0
0	0	0	0

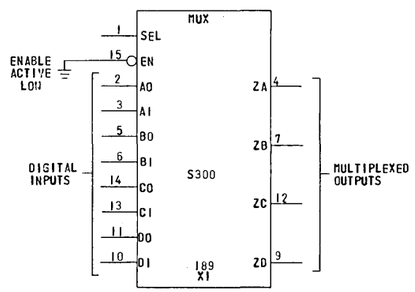
J-K FLIP-FLOP



TOGGLE INPUT UNDERSTOOD TO FEED BOTH SET AND CLEAR INPUT AND GATES. ODD TERM ALWAYS SET INPUT/OUTPUT. COMPARE TRUTH TABLES FOR TYPES 150 AND 240 IN MAINTENANCE AIDS SECTION.



TYPICAL MSI

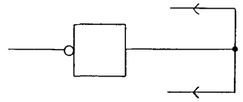


MISCELLANEOUS SCHEMATIC INFORMATION

1. ALL SWITCHES SHOWN IN OFF POSITION OR POSITION 1. SWITCHES WHICH HAVE ONLY 3 CONTACTS, BUT HAVE 3 POSITIONS ARE SHOWN IN THE CENTER, OFF POSITION.

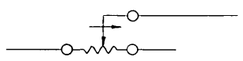
2. N.O./N.C. DESIGNATIONS, AS USED ON SWITCHES, APPLY TO PUSHBUTTONS ONLY; N.C. ON THE OPEN INPUT TO A LOGIC ELEMENT STANDS FOR "NO CONNECTIONS".

3. SIGNAL FLOW IS LEFT-TO-RIGHT UNLESS OTHERWISE INDICATED BY DIRECTION ARROWS.



4. THE SYMBOL BELOW IS USED TO REPRESENT A LIGHT-EMITTING DIODE (LED). THE TWO ARROWS AT 45° ANGLES TO THE DIODE SYMBOL INDICATE THAT THIS IS A PHOTO-EMISSIVE DEVICE. THIS DEVICE IS POLARIZED, AS INDICATED BY THE + AND - SIGNS.

5. THE ARROW ON THE WIPER OF A POTENTIOMETER POINTS IN THE CLOCKWISE DIRECTION.



6. ROTARY SWITCHES USED ON THE EXERCISER FRONT PANEL USE THE PIN NUMBERING EMBOSSED ON THE BACK PLATE OF THE SWITCH, EXCEPT FOR THE WIPER ASSOCIATED WITH A PARTICULAR DECK. SINCE THIS IS NOT EMBOSSED ON THE PLATE, IT IS ASSIGNED THE NEXT HIGHER NUMBER ABOVE THOSE WHICH ARE EMBOSSED.

CONTROL DATA CORPORATION — CUSTOMER ENGINEERING DIVISION	KEY TO LOGIC SYMBOLOGY	CODE IDENT 34011	D	DWG NO 59340600	REV A
				SHEET 2	

TRANSMITTERS & RECEIVERS 1BDF CARD
CR001A

The 1BDF logic board at location A2 contains: six, type 162, dual line receivers; six, type 176, dual line drivers; and an oscillator circuit. There are two receivers and two drivers, or transmitters, on each integrated circuit chip for a total of 12 receivers and 12 transmitters. One transmitter is not used. Each receiver and transmitter has two 56-ohm terminator resistors.

Nine receivers accept the nine Read bits (2^0 through 2^7 and Read Parity). When the differential voltage between the plus and minus receiver inputs is greater than +0.025 volt, the receiver outputs a logic "1". When the differential voltage is greater than -0.025 volt, the receiver outputs a logic "0".

The Read 2^6 and 2^7 receiver outputs each have two diodes with the cathodes wired together with a pull up resistor to +5 volts DC. The anode of one diode is connected to the output of the receiver; the anode of the other diode to the $\overline{\text{7 TRACK}}$ signal. The circuit is a positive AND gate. When the exerciser is connected to a nine track tape transport, the $\overline{\text{7 TRACK}}$ signal is a logic "1" enabling the AND gate. The output of the AND gate will be a "1" when the output of the receiver is a "1" and it will be a "0" when the output of the receiver is a "0". When the exerciser is connected to a seven track tape transport the $\overline{\text{7 TRACK}}$ signal is a logic "0" and the positive AND gate is disabled. The output of the AND gate is then a constant "0" regardless of the receiver output.

The Velocity signal from the tape transport is wired so the negative from the tape transport transmitter is connected to the exerciser receiver positive and the positive from the tape transport transmitter to the negative of the exerciser receiver. In this way, when the velocity input is a "1" the receiver output is a "0". This is done so that when the exerciser is in Internal Test, the Internal Test signal to inverter J104 will provide a logic "0" to pin 8 on the receiver. When the input to pin 8 is a logic "0" the ZB output ($\overline{\text{Velocity I/O}}$) will be a constant logic "1", thus permitting generation of the Velocity signal, which is done on another board.

The Tachometer Phase 1 and Tachometer Phase II signals from the tape transport are connected to receiver R103. They are connected positive to negative and negative to positive, the same as the Velocity signal. When the two tachometer pulses are logic "1", the output from the receiver is a logic "0". The logic "0" receiver output goes to inverters J105 and J106. The inverter outputs (Tachometer Phase 1 and 2) are a logic "1".

During Internal Test, when the Internal Test signal is a logic "1", the logic "1" will be applied through CR1 to pin 10 of AND gate J103. The Busy signal, which is also a logic "1" during internal test, is applied through CR2 to pin 10 of J103. Inverters J100, J101, and J102, in conjunction with C9, C10, and C11, constitute an oscillator. Capacitors C10 and C11 determine the oscillator frequency which is nominally 100 microseconds. Capacitor C9 serves to stabalize the oscillator output. The oscillator output, ANDed with Internal Test and Busy, provides the Tachometer Phase 1 and Phase 2 pulses through OR gates J105 and J106.

SHEET REVISION STATUS						REVISIONS					
				2	1	REV.	E.C.O.	DESCRIPTION	DATE	CHK'D	APP'D
				A	A	A		DRAWING RELEASE	1-7-72	GK	HS
				A	B	B	CE00 117	SEE ECO	10/24/72	[illegible]	

+5VDC
R39 1K
REC
SELA
SELB
A,B
R100
A+
A-
B+
B-
ZA
ZB
162 Y2
R40 56
R38 56
R41 56
R42 56
R45 1K
R101
162 Y4
R46 56
R44 56
R47 56
R48 56
R50 1K
R102
162 Y3
R51 56
R49 56
R52 56
R53 56

J1-B4 READ 2^0 (+) 51
J1-A7 READ 2^0 (-) 35
J1-M4 READ PARITY (+) 39
J1-L7 READ PARITY (-) 42
J1-E3 READ 2^2 (+) 47
J1-D6 READ 2^2 (-) 32
J1-C8 READ 2^1 (+) 48
J1-C2 READ 2^1 (-) 45
J1-H2 READ 2^4 (+) 53
J1-E5 READ 2^4 (-) 54
J1-F7 READ 2^3 (+) 46
J1-F1 READ 2^3 (-) 41

READ 2^0 57 → A5-23 004A, S26-1 009B
READ PARITY 35 → A5-25 004A, S26-9 009B
READ 2^2 43 → A5-26 004A, S26-3 009B
READ 2^1 49 → A5-24 004A, S26-2 009B
READ 2^4 58 → A5-33 004A, S26-5 009B
READ 2^3 44 → A5-28 004A, S26-4 009B

J100 129 Y1
J101 129 Y1
J102 129 Y1
J103 126 Z1
J104 129 Y1
C9 .01 100S
C10 .1 100OS
C11 .1 100OS
CR1
CR2
R67 1K
TP11

J105 126 Z1
J106 126 Z1
TACH I 75 → A4-66 009A, B5-46 008A, S26-14 009S
TACH II 76 → A4-72 009A, B5-48 008A, S26-15 009S

010A A3J2B 1, 79 → +5VDCI
010A A3J2A 2, 80
C1 .1, C2 .1, C3 .1, C4 .1
010A A3J2D 37, 40 → -5VDC
C5 .1, C6 .1, C7 .1, C8 .1
010A A3J2H 13, 31, 50, 68

R68 1K
R56 56, R55 56
R103
R57 56, R58 56
R69 1K
R104
R60 56, R59 56
R70 1K
CR3
CR4
READ 2^7 79 → A5-32 004A, S26-8 009S
VELOCITY 170 63 → B5-70 008A
R61 56, R62 56
R71 1K
R105
R64 56, R63 56
R72 1K
CR5
CR6
READ 2^5 55 → A5-30 004A, S26-6 009S
READ 2^6 77 → A5-27 004A, S26-7 009R

S8A-1 INTERNAL TEST 38
B4-57 BUSY 60
R54 1K TP12
J1-R7 TACH I (-) 74
J1-S4 TACH I (+) 73
J1-T2 TACH II (-) 62
J1-T6 TACH II (+) 61
J1-L1 READ 2^7 (+) 70
J1-K6 READ 2^7 (-) 69
J1-F4 VELOCITY (-) 66
J1-J2 VELOCITY (+) 65
DISABLE READ DATA 67
J1-J3 READ 2^5 (+) 72
J1-H8 READ 2^5 (-) 71
J1-K2 READ 2^6 (+) 64
J1-J7 READ 2^6 (-) 59
A3-29 7 TRACK 78

REFERENCE DRAWING	
ASSEMBLY	59331300
DETAIL	59331400

COMPONENTS EXCEPT AS NOTED			
	TOL	VALUE	SIZE
RES.	5%	OHMS	1/4 W
CAP.		UF	

		DATE
DRAFTSMAN	B. Gatano, Jr.	10/27/71
CHECKER	[illegible]	11-72
ENGINEER	G. Rust	11/6/72
APPROVAL	[illegible]	11/7/72
	G. Rust	11/7/72

CONTROL DATA CORPORATION
CUSTOMER ENGINEERING DIVISION

001A

LOGIC/SCHEMATIC DIAGRAM
IBDF-
TRANSMITTERS AND RECEIVERS
LOC A2

PRODUCT	SIZE	DRAWING NUMBER	REV.
TB111-A01	D	59331500	B
PAGE		SHEET 1 OF 2	

CODE IDENT 34011

TRANSMITTERS AND RECEIVERS 1BDF CARD

CR001B

The eight Write data bits (2^0 through 2^7) are input through inverters J107 through J115 to transmitters T100, T101, T102, T104 and T105. The Write Parity bit goes directly to transmitter T100 without first going through an inverter. The $\overline{\text{Rewind}}$ $\overline{\text{Unload}}$ signal goes through inverter J112 to transmitter T103. A +5 volts DC through R21 to A0 of transmitter T103 is transmitted as the Unit Select signal to the tape transport and lights the UNIT SELECT switch.

When the P DATA switch (CR009A) is set to OFF, the Write Parity signal to T100 is a logic "0" (ground). A steady state logic "0", which is a DC erase, is transmitted to the tape transport. When the P DATA switch is set to ON, odd Write Parity from the parity generator P500 (CR005B) to T100 is transmitted to the tape transport.

When a DATA switch (CR009A) is set to E, there will be no Write data signals to the appropriate inverter (J107 through J115). The +5 volts DC and the pull-up resistor supply a logic "1" to the input of the inverter. The resultant logic "0" output to the transmitter will provide a steady state logic "0" (DC erase) to the tape transport.

When a DATA switch is set to 1, $\overline{\text{1's DATA}}$ from CR005A will be input to the appropriate inverter. The output of the inverter will be 1's DATA to the transmitter, so 1's DATA will be transmitted to the tape transport. When the DATA switch is set to 0, $\overline{\text{0's DATA}}$ will be input to the inverter with 0's DATA going to the transmitter and thus, 0's DATA to the tape transport.

The $\overline{\text{Rewind Unload}}$ signal, from CR006B when the TAPE CONTROL switch (CR009A) is set to UNLOAD, is a one microsecond logic "0" pulse. The one microsecond pulse is provided by the one-shot circuit shown on CR006B. The logic "0" pulse to inverter J112 provides a logic "1" pulse to T103, thus a one microsecond logic "1" pulse is transmitted to the tape transport.

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		INITIAL RELEASE	RG	1-7.72		

009A S25-2 → 22 WRITE PARITY
009A S17A-2 → 4 WRITE 2^0
009A S18A-2 → 20 WRITE 2^1
009A S19A-2 → 17 WRITE 2^2
009A S20A-2 → 3 WRITE 2^3
009A S21A-2 → 19 WRITE 2^4
006B B3-45 → 36 REWIND UNLOAD
009A S24A-2 → 2 WRITE 2^7
009A S23A-2 → 25 WRITE 2^6
009A S22A-2 → 24 WRITE 2^5

+5VDC
TP6 TP1 TP4 TP3 TP2 TP5 TP10 TP8 TP9 TP7
R1 1K R2 56 R3 56 R4 56 R5 47K R6 56
R7 56 R8 1K R9 47K R10 56 R11 56 R12 47K R13 56
R14 47K R15 1K R16 56 R17 47K R18 56 R19 56 R20 56
R21 1K R22 1K R23 56 R24 56 R25 56 R26 56
R27 1K R28 56 R29 56 R30 1K R31 56 R32 56 R33 56 R34 56
R35 47K R36 47K R37 47K

J107 146 W1 (8→9)
J108 146 W1 (3→4)
J109 146 W1 (1→2)
J110 146 W1 (10→11)
J111 146 W1 (5→6)
J112 146 X1 (1→2)
J113 146 X1 (3→4)
J114 146 X1 (5→6)
J115 146 X1 (8→9)

XMT
SELA SELB A,B AO AI BO BI ZA+ ZA- ZB+ ZB-
T100 176 W2
T101 176 W4
T102 176 W3
T103 176 X2
T104 176 X3
T105 176 X4

WRITE PARITY (+) 6 → J1-L2 009C
WRITE PARITY (-) 5 → J1-K7 009C
WRITE 2^0 (+) 8 → J1-A4 009C
WRITE 2^0 (-) 7 → J1-A1 009C
WRITE 2^1 (+) 14 → J1-B6 009C
WRITE 2^1 (-) 16 → J1-A9 009C
WRITE 2^2 (+) 15 → J1-D1 009C
WRITE 2^2 (-) 18 → J1-C4 009C
WRITE 2^3 (+) 9 → J1-E5 009C
WRITE 2^3 (-) 10 → J1-D8 009C
WRITE 2^4 (+) 11 → J1-F9 009C
WRITE 2^4 (-) 12 → J1-F3 009C
UNIT SELECT (+) 21 → J1-R8 009C
UNIT SELECT (-) 26 → J1-R1 009C
REWIND UNLOAD (+) 28 → J1-S3 009C
REWIND UNLOAD (-) 23 → J1-R5 009C
WRITE 2^7 (+) 29 → J1-K3 009C
WRITE 2^7 (-) 30 → J1-J8 009C
WRITE 2^6 (+) 32 → J1-J4 009C
WRITE 2^6 (-) 27 → J1-H9 009C
WRITE 2^5 (+) 34 → J1-H4 009C
WRITE 2^5 (-) 35 → J1-G7 009C

0018

CONTROL DATA CORPORATION — CUSTOMER ENGINEERING DIVISION	LOGIC/SCHEMATIC DIAGRAM 180F- TRANSMITTERS AND RECEIVERS LOC A2	CODE IDENT 34011	D	DWG NO 59331500	REV A
				SHEET 2	

DISPLAY 1AZF

CR002A

Diagram CR002A contains eight receivers, the three static display logic gates (address, model, and fault), and an inhibit for the eight receivers during Internal Test.

When the INT TEST switch (CR009A) is set to ON, a logic "1" is present on the input of inverters J200 and J201. The logic "0" output inhibits the eight receivers, therefore the 16 receiver outputs all go to a logic "1".

The Method of Recording 2^0 and 2^1 signals, Tape Speed 2^2 signal, and Hold signal are connected to the receivers positve to positive and negative to negative. All the other signals are connected positive to negative and negative to positive. When the Method of Recording 2^0 and 2^1 signals, Tape Speed 2^2 signal, and Hold signal are high the output from the receivers are high, and vice-versa. When the other signals are high the output of the receivers are low. An inverter on the output inverts these opposite polarity signals back to the correct polarity. When the INT TEST switch is set to ON, a logic "0" is applied to the inhibit pin 6 of each receiver and so all the receivers output a logic "1". The signals from those receivers that have an inverter on the output will all be inverted during Internal Test. In this way, those signals which should be active during an Internal Test to simulate inputs from the tape transport will be high. They are; Method of Recording 2^0 and 2^1, Tape Speed 2^0, and Hold. All the other signals will be low during Internal Test.

The static display logic provides the signals to the multiplexers on CR002B to route the address, model, and fault information to the DISPLAY. When the DISPLAY SELECT switch is set to ADDRESS, MODEL, or FAULT, a logic "0" is present on pin 9 or 10 of J202. Any logic "0" into J202 will give a logic "1" out, providing the Address or Model or Fault signal.

When the switch S2 is set to ADDRESS or FAULT, a logic "0" is present on pin 13 or 12 of J205. When the switch is set to MODEL, diode CR2 prevents the logic "0" from being present on pin 13 of J205. Any logic "0" into J205 will give a logic "1" out, providing the Address or Fault signal.

When J202 is made by S2 being set to ADDRESS or MODEL or FAULT, a logic "1" is present on pin 1 of J203. When the switch is set to Fault, a logic "0" is present on pin 2 of J203. The logic "1" out is the $\overline{\text{Address or Model}}$ signal.

When switch S2 is set to ADDRESS, MODEL, or FAULT, a logic "0" is present on pin 9 or 10 of J202. Any logic "0" in to J202 will provide a logic "1" out to pin 4 of J204. When S2 is set to ADDRESS, a logic "0" is present on pin 5 of J204. The logic "0" in will provide a logic "1" out, which is the $\overline{\text{Model or Fault}}$ signal.

SHEET REVISION STATUS						REVISIONS				
				2	1	REV.	E.C.O.	DESCRIPTION	DATE	CHK'D	APP'D.
				A	A	A		DRAWING RELEASE	1-7-72		
				B	B	B	CE00 138	SEE ECO	11-00-72		

009C J1-N5 — 20 — M.O.R. 2⁰ (+)
009C J1-M8 — 7 — M.O.R. 2⁰ (−)
009C J1-M1 — 5 — TAPE SPEED 2² (+)
009C J1-L4 — 6 — TAPE SPEED 2² (−)
009C J1-K8 — 18 — TAPE SPEED 2¹ (−)
009C J1-L5 — 15 — TAPE SPEED 2¹ (+)
009C J1-J9 — 7 — TAPE SPEED 2⁰ (−)
009C J1-K4 — 8 — TAPE SPEED 2⁰ (+)
009C J1-C7 — 16 — ADDRESS 2¹ (−)
009C J1-D5 — 14 — ADDRESS 2¹ (+)
009C J1-B3 — 12 — ADDRESS 2⁰ (−)
009C J1-C1 — 11 — ADDRESS 2⁰ (+)
009C J1-H7 — 34 — HOLD (+)
009C J1-H1 — 32 — HOLD (−)
009C J1-P9 — 30 — M.O.R. 2¹ (+)
009C J1-P3 — 27 — M.O.R. 2¹ (−)
009C J1-F5 — 36 — ERASE CURRENT FAULT (−)
009C J1-G3 — 33 — ERASE CURRENT FAULT (+)
009C J1-E1 — 25 — LOAD FAULT (−)
009C J1-E8 — 28 — LOAD FAULT (+)
009C J1-F6 — 38 — ADDRESS 2³ (−)
009C J1-G4 — 35 — ADDRESS 2³ (+)
009C J1-E2 — 23 — ADDRESS 2² (−)
009C J1-E9 — 26 — ADDRESS 2² (+)
009C J1-S1 — 70 — WRITE PERMIT (−)
009C J1-S7 — 69 — WRITE PERMIT (+)
009C J1-N6 — 65 — COOLING AIR FAULT (−)
009C J1-P4 — 66 — COOLING AIR FAULT (+)
009C J1-G9 — 72 — LOOP FAULT (−)
009C J1-H6 — 71 — LOOP FAULT (+)
009C J1-M2 — 63 — VACUUM FAULT (−)
009C J1-M9 — 64 — VACUUM FAULT (+)
009A S8A-1 — 73 — INTERNAL TEST
009A S2-7 — 51 — ADDRESS
009A S2-8 — 54 — MODEL
009A S2-9 — 48 — FAULT

M.O.R. 2⁰ (A)
TAPE SPEED 2² (B)
TAPE SPEED 2¹ (C)
TAPE SPEED 2⁰ (D)
ADDRESS 2¹ (E)
ADDRESS 2⁰ (F)
HOLD (G)
M.O.R. 2¹ (H)
ERASE CURRENT FAULT (I)
LOAD FAULT (J)
ADDRESS 2³ (K)
ADDRESS 2² (L)
WRITE PERMIT I/O 67 → 85-66 008A
COOLING AIR FAULT (N)
LOOP FAULT (O)
VACUUM FAULT (P)
ADDRESS + MODEL + FAULT (Q)
ADDRESS + MODEL (R)
MODEL + FAULT (S)
ADDRESS + FAULT (T)

REFERENCE DRAWING					DRAFTSMAN	DATE			
ASSEMBLY 59329700					B. Peterson	11/30/71	CONTROL DATA CUSTOMER ENGINEERING DIVISION	LOGIC/SCHEMATIC DIAGRAM 1AZF- DISPLAY LOC A3	
DETAIL 59329800					CHECKER				
COMPONENTS EXCEPT AS NOTED					ENGINEER		PRODUCT TB1113-A01	SIZE D	DRAWING NUMBER 59329901 REV. B
	TOL	VALUE	SIZE		APPROVAL				
RES.	5%	OHMS	1/4W				PAGE		SHEET 1 OF 2
CAP.		UF							

002A

CODE IDENT 34011

DISPLAY 1AZF

CR002B

Diagram CR002B contains four multiplexers, D200 through D203. The outputs of the four multiplexers are the nine bits to light the three DISPLAY indicators. The output may be either the dynamic display information or the static display information.

Multiplexers D201, D202, and D203 output two display bits each, while D200 outputs three bits. The outputs of D200 are the three high order bits (2^8, 2^7, and 2^6) and the outputs of D201, D202, and D203 are the six lower order bits.

The D200 multiplexer has a select (SEL) and an enable (EN) control input. Data input is either dynamic or static. When the multiplexer is outputting either Fault or Address information, the left indicator is always a zero since none of the addresses or faults have three digits. Therefore, the D200 multiplexer has fewer data inputs than the other three multiplexers.

The outputs of the D200 multiplexer are either Fault, Address, Model, or Dynamic as indicated in the table below for each logic input on Q (Address or Fault or Model) and T (Address of Fault).

D200

INPUT		OUTPUT
Q (SEL)	T (EN)	
"0" or "1"	"1"	FAULT
"0" or "1"	"1"	ADDRESS
"1"	"0"	MODEL
"0"	"0"	DYNAMIC

On D201, D202, and D203 multiplexers, the A0 through A3 and B0 through B3 inputs are as follows:

INPUT	INFORMATION
A0, B0	MODEL
A1, B1	ADDRESS
A2, B2	FAULT
A3, B3	DYNAMIC

The outputs of D201, D202, and D203 multiplexers are either Model, Address, Fault, or Dynamic as indicated in the table below for each logic input on R (Address or Model) and S (Model or Fault).

INPUT		OUTPUT
R (SEL 2)	S (SEL 1)	
"1"	"0"	FAULT
"0"	"1"	ADDRESS
"0"	"0"	MODEL
"1"	"1"	DYNAMIC

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		INITIAL RELEASE				
B	CE00138	SEE ECO				

M.O.R. 2^0 (A)
M.O.R. 2^1 (H)
TAPE SPEED 2^2 (B)
ADDRESS + FAULT + MODEL (Q)
ADDRESS + FAULT (T)
0038 A4-46 → 78 28
TAPE SPEED 2^1 (C)
0038 A4-30 → 76 27
0038 A4-26 → 62 26
HOLD (G)
0038 A4-9 → 41 24
COOLING AIR FAULT (N)
TAPE SPEED 2^0 (D)
ADDRESS 2^3 (K)
0038 A4-5 → 55 25
LOOP FAULT (D)
0038 A4-19 → 46 22
ADDRESS 2^2 (L)
0038 A4-23 → 45 23
VACUUM FAULT (P)
0038 A4-24 → 60 21
ADDRESS 2^1 (E)
0038 A4-20 → 52 20
ERASE CURRENT FAULT (I)
ADDRESS + FAULT (R)
MODEL + FAULT (S)
ADDRESS 2^0 (F)
LOAD FAULT (J)
0054 B2-16 → 74 CDC

J206 129 V1
J207 126 X1
J208 126 X1
J209 129 W1
J210 126 X1
J211 126 X1
J212 129 V1
J213 129 V1
J214 126 Y2
J215 129 W1
J216 129 Z2
J217 126 Y2
J218 129 V1
J219 126 Y2
J220 126 Y2
J221 129 W1
J222 129 Z2
J223 129 W1
J224 129 Z2
J225 129 V1
J226 129 W1
J227 129 V1
J228 129 W1
J229 129 Z2

TP1 TP7

TP5

D200 MUX
SEL EN A0 A1 B0 B1 D0 D1 ZA ZB Z0 Z1 189

D201 MUX
SEL2 SEL1 A0 A1 A2 A3 B0 B1 B2 B3 ZA ZB 170 X2

D202 MUX
SEL2 SEL1 A0 A1 A2 A3 B0 B1 B2 B3 ZA ZB 170 X3

D203 MUX
SEL2 SEL1 A0 A1 A2 A3 B0 B1 B2 B3 ZA ZB 170 X4

TAPE SPEED 2^0 → A5-58 004A, B2-12 005A
7 TRACK → A2-78 001A, B2-74 005B, A5-60 004A, B2-4 005A
TAPE SPEED 2^2
TP12 DISPLAY 2^8 → DS3-4 009B
TP11 DISPLAY 2^7 → DS3-5 009B
TP10 DISPLAY 2^6 → DS3-2 009B
TAPE SPEED 2^1 → A5-57 004A, B2-14 005A
COOLING AIR FAULT → B5-30 008B
TP2 DISPLAY 2^4 → DS2-5 009B
TP4 DISPLAY 2^5 → DS2-4 009B
VACUUM FAULT → B5-38 008B
TP3 DISPLAY 2^2 → DS1-4 009B
TP6 DISPLAY 2^3 → DS2-2 009B
LOOP FAULT → B5-14 008B
TP9 DISPLAY 2^0 → DS1-2 009B
TP8 DISPLAY 2^1 → DS1-5 009B
ERASE CURRENT FAULT → B5-36 008B
LOAD FAULT → B5-34 008B

0028

CONTROL DATA CORPORATION — CUSTOMER ENGINEERING DIVISION

LOGIC/SCHEMATIC DIAGRAM
IAZF-
DISPLAY
LOC A3

CODE IDENT 34011 | D | DWG NO 59329901 | REV B | SHEET 2

SKEW AND TACHOMETER 1BCF CARD

CR003A

TACH FLIP FLOP

The Tach flip-flop (K306/K307) permits gating of the Tach I and Tach II pulses from the tape transport to the C300 and C301 counters (CR003B) and then to the operator panel DISPLAY.

The Tach flip-flop is set when: (1) the $\overline{\text{Skew}}$ signal from the DISPLAY SELECT switch (CR009A) is present on pin 2 of J325, and (2) the Clear Counter one microsecond pulse from K301 flip-flop and capacitor C6 is present on pin 1 of J325. The set output of the Tach flip-flop provides a logic "1" to pin 1 of J326. The Tach I and Tach II pulses are ANDed with the Tach flip-flop set output at J326 and provide the Gate Tachometer signal output to the counters and the DISPLAY.

The Tach flip-flop is cleared by the one microsecond Clear Tach signal from K303 flip-flop and capacitor C9. That one-shot pulse is available when K303 is toggled by one of the outputs of AND gates J312, J314, J316, and J318 through a wired-OR.

The J312 AND gate outputs a logic "0" to K303 when both a Velocity signal from B5(CR008A) is present and the Start Time signal from the DISPLAY SELECT switch (CR009A) through J311 is present.

The J314 AND gate outputs a logic "0" to K303 when both the Go Pulse from B5(CR008A) and either the Stop Act or Stop App signal from the DISPLAY SELECT switch (CR009A) through J313 is present. The J316 AND gate outputs a logic "0" to K303 when both the Record Gap signal from the DISPLAY SELECT switch (CR009A) and no data from A5(CR004A) through J317 are present.

The J318 AND gate outputs a logic "0" to K303 when the $\overline{\text{Skew}}$, $\overline{\text{Stop App}}$, $\overline{\text{Record Gap}}$, $\overline{\text{Start Time}}$, and $\overline{\text{Stop Act}}$ signals from the DISPLAY SELECT switch (CR009A) are present. In other words, when the switch is set between any two positions, the AND gate J318 is made and K303 flip-flop provides a Clear Tach pulse to the Tach flip-flop.

SKEW I, SKEW II, AND SKEW III FLIP FLOPS

Skew, as measured by the exerciser, is the time from the receipt of the first data bit to the time of the receipt of the data bit selected by the SIGNAL MONITOR switch, positions 1 through 9. The three Skew flip-flops are used to enable skew measurement during that period of time.

The Skew I flip-flop (K304/K305) is set when the skew signal from the DISPLAY SELECT switch (CR009A) is present at pin 13 of AND gate J323 and when there is an absence of data for at least one microsecond. When this occurs, a logic "1" is present on pin 12 of J323.

The purpose of the one microsecond delay, which is accomplished by capacitor C10, is so that the Skew I flip-flop will get set between frames of data; not between two data bits in the same frame. When there is an absence of data, the input to J317 is a logic "1" from A5 (CR004A). The logic "0" out of J317 to J322 provides a logic "1" out of J322. If the data is absent for at least one microsecond, a logic "1" will be input to AND gate J323. If the data is absent for less than one microsecond, capacitor C10 will not charge up and the input to J323 will remain a logic "0", therefore the Skew I flip-flop will not get set. The logic "1" out of the set side of the flip-flop through the wired-OR goes to the clear of the Skew III flip-flop, the clear of the Skew II flip-flop, and to pin 1 of AND-gate J310 and pin 2 of AND gate J309. When the first Data bit from A5 through J317 is present on pin 2 of AND gate J310, the AND gate is enabled and the Skew III flip-flop is set. The set output of the flip-flop goes to exclusive-OR gate J320. The Skew II flip-flop is cleared at this time so the set output to J320 is a logic "0". The logic "1" on pin 2 is output from J320 as the Gate Skew signal.

When the Signal Monitor signal, which is the signal present at whatever position the switch is set to, comes in, a logic "1" is applied to pin 1 of AND gate J309. Since skew is a measurement of the time from the first data bit to the data bit selected by the SIGNAL MONITOR switch, positions 1 through 9, the Signal Monitor signal will normally be one of the read data bits on positions 1 through 9.

The Skew I flip-flop, which is set, provides a logic "1" through the wired-OR to pin 10 of K308 and K310, removing the clear from the Skew II and Skew III flip-flops. The set output from the Skew I flip-flop also enables AND gates J309 and J310. The signal from the Signal Monitor is present on pin 1 of J309 so the Skew II flip-flop is set. When Data comes in from A5 (CR004A) through J317, J310 is made and sets the Skew III flip-flop. The J320 exclusive-OR gate, which had a logic "1" output when the set output of Skew II flip-flop was present on pin 1, now has a logic "0" output when a logic "1" is present on pin 2. In this way, the Gate Skew signal is present only when one of the two flip-flops (Skew II and Skew III) is set and one is clear. Skew III flip-flop is set when Data comes in from A5 and Skew II flip-flop sets when Data selected by the SIGNAL MONITOR switch is present.

When either Skew II or Skew III flip-flop sets, OR-gate J319 is made and the Q300 oscillator is started. Then, every one-half second, K301 flip-flop is toggled and the C300 and C301 counters are cleared to zero. Therefore, every one-half second the skew display is updated.

The Skew I, Skew II, and Skew III flip-flops are cleared when the Clear Counter signal from K301 flip-flop is available through inverter J308 to K304, K310, and K308.

CLEAR COUNTER SIGNAL

The Clear Counter signal is a one microsecond pulse formed by flip-flop K301 and capacitor C6. The K301 clear output clears C300 and C301 counters (CR003B) to zero. The Clear Counter pulse is provided any time one of the AND gates J301, J306, J304, and J305 is made.

The J301 AND gate is made when the DISPLAY SELECT switch (CR009A) is set to STOP ACT and when the Velocity signal goes low.

The J304 AND gate is made when the End of Operation signal is present and when the DISPLAY SELECT switch is set to either RECORD GAP or STOP APP.

The J305 AND gate is made when the Go Pulse is present and the DISPLAY SELECT switch is set to START TIME.

The J306 AND gate is made when the .5 second Q300 oscillator signal is present. The oscillator is enabled whenever the Skew II or Skew III flip-flop is set. Therefore, the counter is cleared and the skew is updated every one-half second. When the oscillator times out, after having been enabled by the clear output of the Skew II or Skew III flip-flop, the oscillator output pulse enables J306 and fires the K301 flip-flop. The one microsecond output pulse then clears the two counters, C300 and C301.

SHEET REVISION STATUS						REVISIONS					
					2	1	REV.	E.C.O.	DESCRIPTION	DATE	CHK'D	APP'D.
					A	A	A		DRAWING RELEASE	1-7-72		

0098 S26-25 → 63 SIGNAL MONITOR

009A S2-3 → 70 STOP ACT

008A B5-65 → 78 VELOCITY

009A S2-5 → 45 RECORD GAP

0048 A5-63 → E.O.T.

008A B5-78 → 74 GB PULSE

009A S2-1 → 73 START TIME

009A S2-2 → 64 STOP APP

004A A5-29 → 34 DATA

009A S2-4 → 43 SKEW

001A A2-76 → 72 TACH II

001A A2-75 → 66 TACH I

+5VDC R1 1K, R6 1K, R8 1K, R9 1K, R11 1K

J300 129 Z2, J301 126 Z3, J302 129 Z2, J303 126 Z3, J304 126 Z3, J305 126 Z3, J306 129 Z2, J307 129 Z2, J308 129 Z2, J309 140 Y5, J310 140 Y4, J311 129 Y2, J312 126 Z1, J313 126 Z1, J314 126 Z1, J315 129 Y2, J316 126 Z1, J317 146 W3, J318 128 Z5, J319 126 X3, J320 149 Y3, J321 129 Z2, J322 129 X2, J323 126 X3, J324 129 Y2, J325 126 Y1, J326 128 Z5

TP11, TP10, TP9, TP12

K301 150 Z4 (CLEAR COUNTER), K309 140 Y5, K308 140 Y5 (SKEW II), K311 140 Y4, K310 140 Y4 (SKEW III), K303 150 Z4 (CLEAR TACH), K305 129 Y2, K304 129 Y2 (SKEW I), K307 129 Y2, K306 126 Y1 (TACH)

CR1, CR2, CR3, CR4, CR5, CR6

C6 .001, C7 22, C9 .001, C10 .001, 1US

Q300 AA10: +5VDC, .5 SECONDS, R5 1K, R2 220K, R3 1.5K, C8 .01, R4 22K, Q1 IIS43, R7 33, 5USEC, Q2 DDI106

CLEAR COUNTER → A

GATE SKEW → B

GATE TACHOMETER → C

0010A A3J2B → +5VDC1 (C1 .1, C2 .1, C3 .1, C4 .1)

0010A A3J2A

0010A A3J2D → -5VDC (C5 .1, C6 .1, C7 .1, C8 .1)

0010A A3J2H

REFERENCE DRAWING	DRAFTSMAN	DATE
ASS'Y-59331000	J. REYES	10/20/71
DETAIL-59331100	CHECKED	1-6-72
	ENGINEER	1/6/72
	APPROVAL	1/6/72

COMPONENTS EXCEPT AS NOTED	TOL	VALUE	SIZE
RES.	5%	OHMS	1/4W
CAP.		UF	

CONTROL DATA CORPORATION — CUSTOMER ENGINEERING DIVISION

003A

LOGIC/SCHEMATIC DIAGRAM
18CF-
SKEW AND TACHOMETER
LOC A4

PRODUCT TB111-A01 | SIZE D | DRAWING NUMBER 59331200 | REV. A | SHEET 1 OF 2 | PAGE

CODE IDENT 34011

SKEW AND TACHOMETER 1BCF CARD

CR003B

COUNTING

The outputs from the D300 and D301 multiplexers and inverter J334 are the nine Data bits which go to the three DISPLAY segments on the operator panel. Bits 2^0, 2^1, and 2^2 go to segment DS1; bits 2^3, 2^4, and 2^5 go to segment DS2; and bits 2^6, 2^7 and 2^8 go to segment DS3. The Data bits go to the DISPLAY when any of the dynamic displays have been selected by the DISPLAY SELECT switch. They include; Start Time, Stop Act and Stop App, Record Gap, Skew, and Read Data.

The 2^8 Data Bit is displayed only when the Read Data is displayed. When the DISPLAY SELECT switch (CR009A) is set to READ, a logic "0" is present on the input of inverter J332. The logic "1" out of J332 enables AND gate J333 when the Data 2^8 signal is present. When not in the READ position, a constant logic "0" is forced out of J334.

In addition, when the DISPLAY SELECT switch is set to READ, a logic "0" is present on pins 1 of D300 and D301 multiplexers. The Data 2^0 through 2^7 bits are thus selected by the multiplexers and are output to the DISPLAY.

When the DISPLAY SELECT switch is not set to READ, a logic "1" is present on pin 1 of D300 and D301 multiplexers. The C300 and C301 counter outputs are then selected by the multiplexers. Counters C300 and C301 are both 4-bit counters. The CLR input to the counters is from either the MC (Master Clear) position of the INT CONTROL switch (CR009A) or the Clear Counter signal from CR003A. A logic "0" on either one to J330 will produce a logic "1" out and clear both counters. The two counters both function as up counters.

After C300 has counted to 17_8, the Z0, Z1, Z2, and Z3 outputs will all be logic "1". On the 20_8 count, the CAR output will be a logic "1". The C301 counter functions in the same way. When 17_8 CAR pulses from C300 have been input to pin 5 of C301, the Z0, Z1, Z2 and Z3 outputs of C301 will all be logic "1's".

The Gate Tachometer pulses, which are the AND of the Tach I and Tach II pulses, when present at pin 12 of OR gate J331, are gated through and are counted by C300 and then C301.

When the Gate Skew signal is a logic "1", AND gate J329 is enabled and 50 nanosecond pulses from Y1 (20 millihertz oscillator) are gated to J331 and are then counted by C300 and C301.

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		INITIAL RELEASE	JPR	1-7-72		KO

B GATE SKEW

C GATE TACHOMETER

R12 680 · R13 680 · R14 680 · C11 10PF · Y1 20MHZ

J327 146 W3 · J328 146 W3 · J329 140 Y4 · J331 140 Y5

SKEW/TACH COUNTER

CNTR C300 500 X5 — UP, DN, CLR, LD, CAR, Z0–Z3

+5VDC · R10 1K

TP1 TP2 TP8 TP7

MUX D300 189 W5 — SEL, EN, A0–A3, B0–B3, C0–C3, D0–D3, ZA–ZD

004A A5-41 → DATA 2^3 → 2^3 → A3-45 002B

004A A5-44 → DATA 2^2 → 2^2 → A3-46 002B

004A A5-43 → DATA 2^1 → 2^1 → A3-60 002B

004A A5-38 → DATA 2^0 → 2^0 → A3-52 002B

009A S15-1 → $\overline{MC}$

A $\overline{CLEAR\ COUNTER}$

J330 126 X3

CNTR C301 500 X4 — UP, DN, CLR, LD, Z0–Z3

TP3 TP4 TP6 TP5

MUX D301 189 W4 — SEL, EN, A0–A3, B0–B3, C0–C3, D0–D3, ZA–ZD

004A A5-45 → DATA 2^7 → 2^7 → A3-76 002B

004A A5-46 → DATA 2^6 → 2^6 → A3-62 002B

004A A5-39 → DATA 2^5 → 2^5 → A3-55 002B

004A A5-42 → DATA 2^4 → 2^4 → A3-41 002B

+5VDC · R15 1K

009A S2-6 → $\overline{READ}$

004A A5-35 → DATA 2^8 → 2^8 → A3-78 002B

J332 129 X2 · J333 126 X3 · J334 129 X2

003B

CONTROL DATA CORPORATION — CUSTOMER ENGINEERING DIVISION	LOGIC/SCHEMATIC DIAGRAM 1ECF- SKEW AND TACHOMETER LOC A4	CODE IDENT 34011	D	DWG NO 59331200	REV A
				SHEET 2	

READ AND END OF OPERATION LBAF CARD

CR004A

RUNNING TIME METER

A +5 volts DC is provided through resistor R9 to the 2000 hour timer, XM1 (CR009A).

READ

The Read Data from the tape transport is input to this logic board, where the Data is inserted into a register so it can be displayed. The data is also checked for proper parity (odd). The nine Read Data signals into inverters J410 through J418 are OR-ed together. If any Read Data signal is high, the output of the wired-OR will be low. The $\overline{\text{Data}}$ signal goes to logic board A4 (CR003A) for skew measurement and also to CR004B for generation of an End of Operation signal.

The $\overline{\text{Data}}$ signal goes to pin 5 of K411 one-shot and pin 11 of K413 one-shot. The time of the K411 one-shot is determined by the Tape Speed 2^0, 2^1, and 2^2 inputs. The time is 3 microseconds for Tape Speed 2^0 (100 IPS), 2 microseconds for Tape Speed 2^1 (150 IPS), and 1.5 microseconds for Tape Speed 2^2 (200 IPS).

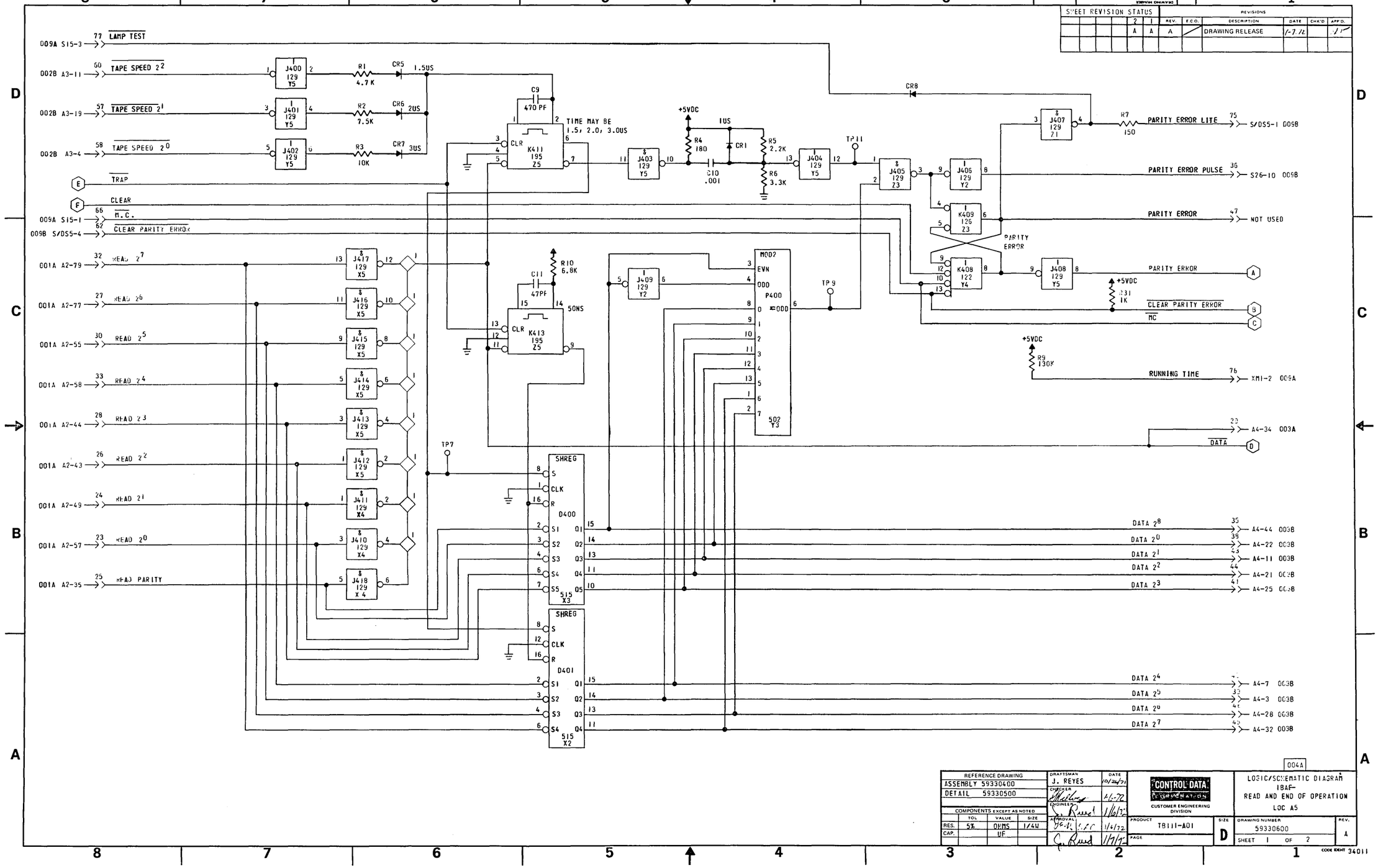
The pulse out on pin 6 of one-shot K411 permits Read Data to be gated into D400 and D401 shift registers during the time that the pulse is high. Therefore, the first time a data bit comes in, the shift registers gate in data for a certain period of time, and then the data is latched into the register. This is referred to as the skew sampling time and varies depending upon tape speed. If the skew is greater than the time selected, the word will be latched into the register with the one skewed bit missing, resulting in a parity error. The two shift registers are cleared, to accept the new Read Data, by the output on pin 9 of K413 one-shot which fires when the Read Data bit comes in on pin 11.

After the Read Data is latched into the register, it is output to logic board A4(CR003B), then to A3(CR007B) where it is subsequently sent to the DISPLAY when READ is selected on the DISPLAY SELECT switch.

The output of D400 and D401 also goes to parity checker P 400. If the data coming in is even parity, a logic "1" is output on pin 6. The logic "1" goes to AND gate J405. The trailing edge of the one-shot pulse out of K411 fires the one-shot circuit, composed of resistors R4 and R5 and capacitor C10, which provides a one microsecond pulse to AND gate J405. When AND gate J405 is made the pulse out sets the Parity Error flip-flop.

When the Parity Error flip-flop sets, the logic "1" out on the set side through inverter J407 lights the PARITY ERROR indicator. The pulse output of J405 through inverter J406 is the Parity Error pulse which goes to the SIGNAL MONITOR switch. The pulse output from J405, rather than the steady logic output of the Parity Error flip-flop, is supplied to the SIGNAL MONITOR so that if more than one parity error occurs the errors can be observed as pulses on the SIGNAL MONITOR indicator. If the output of the Parity Error flip-flop went to the SIGNAL MONITOR, there would be no way of telling if more than one parity error occured.

The Parity Error flip-flop is cleared by; (1) pressing the PARITY ERROR pushbutton (CR009B), or (2) setting the INT CONTROL switch to MC, and (3) a Clear signal which is generated by the Backspace flip-flop being set and an End of Operation signal being generated. The Backspace and End of Operation signals clear the Parity Error flip-flop so that parity errors are not detected during a backspace operation.


SHEET REVISION STATUS
REVISIONS
REV. A A A
F.C.O.
DESCRIPTION: DRAWING RELEASE
DATE 1-7-72
CHK'D
APP'D
009A S15-3 77 LAMP TEST
002B A3-11 60 TAPE SPEED 2^2
002B A3-19 57 TAPE SPEED 2^1
002B A3-4 58 TAPE SPEED 2^0
TRAP
CLEAR
009A S15-1 66 M.C.
009B S/DS5-4 62 CLEAR PARITY ERROR
J400 129 Y5
J401 129 Y5
J402 129 Y5
R1 4.7K
R2 7.5K
R3 10K
CR5 1.5US
CR6 2US
CR7 3US
C9 470 PF
K411 195 25
TIME MAY BE 1.5, 2.0, 3.0US
+5VDC
R4 180
R5 2.2K
R6 3.3K
C10 .001
CR1
1US
J403 129 Y5
J404 129 Y5
TP11
CR8
J405 129 Z3
J406 129 Y2
K409 126 Z3
K408 122 Y4
J407 129 Z1
J408 129 Y5
R7 150
PARITY ERROR LITE 75 S/DS5-1 009B
PARITY ERROR PULSE 36 S26-10 009B
PARITY ERROR 47 NOT USED
PARITY ERROR
PARITY ERROR A
CLEAR PARITY ERROR B
MC C
R31 1K
R9 130K
RUNNING TIME 76 XM1-2 009A
001A A2-79 32 READ 2^7
001A A2-77 27 READ 2^6
001A A2-55 30 READ 2^5
001A A2-58 33 READ 2^4
001A A2-44 28 READ 2^3
001A A2-43 26 READ 2^2
001A A2-49 24 READ 2^1
001A A2-57 23 READ 2^0
001A A2-35 25 READ PARITY
J417 129 X5
J416 129 X5
J415 129 X5
J414 129 X5
J413 129 X5
J412 129 X5
J411 129 X4
J410 129 X4
J418 129 X4
R10 6.8K
C11 47PF
K413 195 25
50NS
J409 129 Y2
MOD2
EVN
ODD
P400
=ODD
TP9
502 Y3
TP7
SHREG
S
CLK
R
D400
D401
S1 S2 S3 S4 S5
Q1 Q2 Q3 Q4 Q5
515 X3
515 X2
DATA 2^8 35 A4-44 003B
DATA 2^0 38 A4-22 003B
DATA 2^1 43 A4-11 003B
DATA 2^2 44 A4-21 003B
DATA 2^3 41 A4-25 003B
DATA 2^4 A4-7 003B
DATA 2^5 A4-3 003B
DATA 2^6 A4-28 003B
DATA 2^7 A4-32 003B
23 A4-34 003A
DATA D
004A
REFERENCE DRAWING
ASSEMBLY 59330400
DETAIL 59330500
COMPONENTS EXCEPT AS NOTED
RES. 5% OHMS 1/4W
CAP. UF
DRAFTSMAN J. REYES 10/24/71
CHECKER 11-72
ENGINEER 1/6/72
APPROVAL 1/4/72
1/7/72
CONTROL DATA CORPORATION
CUSTOMER ENGINEERING DIVISION
LOGIC/SCHEMATIC DIAGRAM
IBAF-
READ AND END OF OPERATION
LOC A5
PRODUCT TB111-A01
SIZE D
DRAWING NUMBER 59330600
REV. A
SHEET 1 OF 2
PAGE
CODE IDENT 34011

READ AND END OF OPERATION 1BAF CARD

CR0048

DENSITY REQUEST TRANSMITTER

The Density Request 2^0 and 2^1 signals are transmitted to the tape transport via T400 transmitter. The Density Request 2^0 and 2^1 lines are high or low depending upon the setting of switch S6 and S7 (CR0094), respectively. Resistors R21, R22, R23, and R24 serve as terminator resistors for the transmitter.

CLIPPING LEVEL TRANSMITTER

The High and Low Clipping Level signals are transmitted to the tape transport via T401 transmitter. The Clipping Level is selected by CLIPPING LEVEL switch S11. Resistors R25, R26, R27, and R28 serve as terminator resistors for the transmitter.

TRAP FLIP-FLOP

When the PARITY ERROR RESPONSE switch (CR0094) is set to TRAP and a Parity Error signal is present, AND gate J427 is made and the Trap flip-flop sets. When set, the clear output goes to CR004A and clears the two one-shots, K411 and K413. In this way, the two shift registers, D400 and D401, are disabled from gating any more Read Data in so that the registers will hold the previously detected parity error in order for it to be displayed.

The Trap flip-flop is cleared by either setting the INT CONTROL switch (CR0094) to MC or by pressing the PARITY ERROR pushbutton.

BACKSPACE FLIP-FLOP

The Backspace flip-flop is set when the PARITY ERROR RESPONSE switch is set to BACKSPACE, when a Parity Error signal is present, when Data is present, and when the OPERATION switch is not set to CONTINUOUS.

The Backspace flip-flop is cleared by: (1) setting the INT CONT switch to MC, or (2) by the set output of the Backspace Clear flip-flop which sets on Time 3 of the timing chain and when the Backspace set output is present. In other words, the Backspace Clear flip-flop is set on Time 3 after the Backspace flip-flop is set. Time 3 is the third pulse of the internal timing chain which is initiated after the Busy signal drops. The next time Busy drops the timing chain is again initiated and so Time 1 and the Backspace Clear flip-flop set output clear the Backspace flip-flop and on Time 2 the Backspace Clear flip-flop clears. This is so that when a Backspace operation is being performed that another Backspace operation cannot be commanded.

The set output of the Backspace flip-flop goes to logic board B3 (CR006B) where it is used to perform a backspace operation.

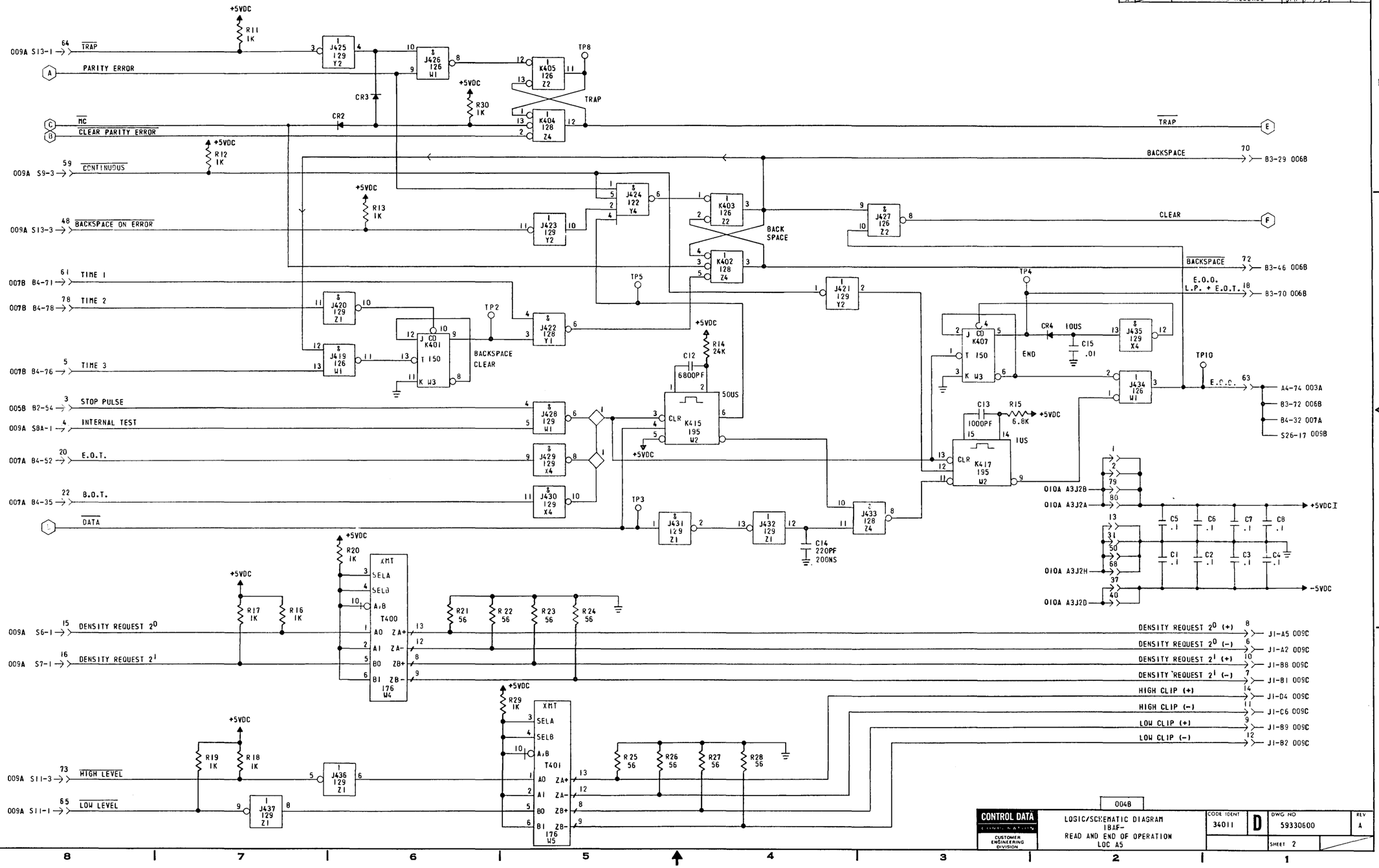
END OF OPERATION

The End of Operation signal is used to increment the program address counter and also to drop the Forward, Reverse, and Write signals. One-shot K415 is designed to fire when a transition from a logic "0" to a logic "1" input is present on pin 4. When it fires, a logic "1" is output on pin 6 for 50 microseconds, at which time the one-shot times out. If another transition is applied to input pin 4 before the one-shot times out, the one-shot will retrigger and the output will remain high as long as inputs are applied. When there has been no transition for 50 microseconds, the one-shot times out and the output on pin 6 goes to a logic "0".

When Read Data (logic "0") comes in to one-shot K415, the one-shot is enabled for firing when Read Data goes away (logic "1"). As soon as Read Data goes away, a logic "1" is applied to pin 4 of K415 and it fires. A logic "0" is then applied to AND gate J433, pin 10. When there has been an absence of data for 50 microseconds, K415 times out and a logic "1" is output on pin 7 to J433. A logic "1" will also be present on pin 11 of J433 200 nanoseconds after Read Data has gone away, therefore J433 will be made. When J433 is made, one-shot K417 provides a one microsecond logic "0" out to OR-gate J434, which outputs the End of Operation pulse.

The J434 OR-gate is also made when the 10 microsecond one-shot composed of flip-flop K407 and capacitor C15 fires. This occurs whenever the Beginning of Tape or End of Tape signal arrives. It also occurs when the INT TEST switch (CR0094) is set to ON or S/S and the Stop Pulse from B2 (CR005B) arrives.

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		INITIAL RELEASE	JPR	1-77		



0048

CONTROL DATA CUSTOMER ENGINEERING DIVISION	LOGIC/SCHEMATIC DIAGRAM IBAF- READ AND END OF OPERATION LOC A5	CODE IDENT 34011	D	DWG NO 59330600	REV A
				SHEET 2	

WRITE 2BAF CARD

CR005A

The primary purpose of the write logic is to produce phase enabled and NRZI ones and zeros data. Two oscillators, K517 and K519, are always running. Oscillator K517 produces a 3.0 microsecond waveform output and K519 produces a 515 nanosecond waveform output. Oscillator K517 is used to produce a 556 BPI NRZI data pattern and oscillator K519 is used to produce a 1600 BPI phase enabled and an 800 BPI NRZI data pattern.

The output of oscillator K517 is fed directly to multiplexer A500 on pins 4 and 7. The output of oscillator K519 is fed to pin 6 of A500 and to the 1600 BPI flip-flop. The output of the 1600 BPI flip-flop is fed to the 800 BPI flip-flop which is in turn fed to pin 5 of multiplexer A500.

Multiplexer A500 is used to select the appropriate density. The Density status 2^0 and 2^1 signals from the tape transport gate one of the four inputs out to counter C500. When Density status 2^0 and 2^1 are both low, 556 BPI is output from A500. When Density status 2^0 is high and 2^1 is low, 800 BPI is output from A500. If Density status 2^0 and 2^1 were both high, 556 BPI would be output, however this Density status is not used.

The output of A500 multiplexer, which is 556, 800, or 1600 BPI is input to C500 counter on pin 4. To obtain the correct write data clock rate, the C500 counter is loaded at the A0, A1, A2, and A3 inputs with a load factor which is dependent upon tape speed. The load factor is used to divide the count on pin 4. When switch S1 is set to CDC and when the Tape Speed 2^0 (100 IPS) signal is high, a factor of six (0110) is loaded into C500. When S1 is set to CDC and Tape Speed 2^1 (150 IPS) is high, a factor of four (0100) is loaded into C500. When S1 is set to CDC and Tape Speed 2^2 (200 IPS) is high, a factor of three (0011) is loaded into C500. When S1 is set to IBM and Tape Speed 2^0 is high (75 IPS), an eight (1000) is loaded into C500. When S1 is set to IBM and Tape Speed 2^1 is high (125 IPS), a 5 (0101) is loaded into C500. When Tape Speed 2^2 is high, a three (0011) is loaded into C500 regardless of whether S1 was set to CDC or IBM.

Counter C500 divides the input on pin 4 by a factor which is dependent upon what is loaded on A0, A1, A2, and A3. When the counter has counted to zero, a BOR output goes from pin 13 to Data flip-flop K505. The BOR output also goes back to the LD input on the counter. In this way, every time there is a BOR pulse the input at A0, A1, A2, and A3 is again loaded into the counter.

The BOR output toggles the Data flip-flop. The flip-flop output is a square wave representation of the BOR input. The clear output of the Data flip-flop is fed into the toggle input of the 1's Data True/Complement flip-flop, K507. The 1's Data True/Complement flip-flop divides the input in half for writing a true/complement pattern. The true/complement pattern is the same as the true pattern except the frequency is only one-half.

The clear output of K505 also goes to inverter J514 and then to the one-shot circuit composed of resistors R7 and R8 and capacitor C7. The output of J515 is Write Data which goes to the SIGNAL MONITOR switch and also to CR005B where it is used with the End of Tape signal or the set output of the Stop Enable flip-flop to clear the Write flip-flop. The set output of the Data flip-flop, after going through J511 and J512, also goes to the toggle input of the 0's Data True/Complement flip-flop, K509. Flip-flop K509 divides the frequency of the Data flip-flop in half for producing a true/complement pattern.

The set output of Data flip-flop K505 goes to AND gate J517 and AND gate J520. AND gate J517 is enabled when the TRUE position of the PATTERN switch (CR009A) is selected. The wired-OR on the output of AND gates J516 and J517 outputs 1's data when either 1's Data is on pin 1 of J516 and TRUE/COMPLEMENT from the PATTERN switch is on pin 2 of J516, or when the TRUE signal from the PATTERN switch is on pin 5 of J517 and the set output of the Data flip-flop is on pin 4 of J517.

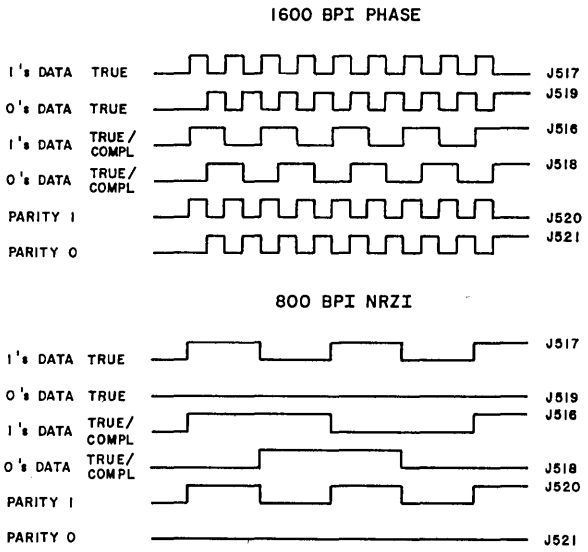
The wired-OR on the output of AND gates J518 and J519 outputs a 0's Data signal when the True/Complement signal is on pin 10 of J518 and 0's Data is on pin 9 of J518, or when the True signal is on pin 11 of J519 and the set output of the Data flip-flop is on pin 9 through inverters J511, J512, and J513. Capacitor C8 eliminates crossover. In addition, the set output of the Phase Enable flip-flop must be on pin 10 of J519.

The Parity signal is output to P DATA switch S25 (CR009A) from this logic card. The P500 parity generator (CR005B) receives the eight Write Data bits from the DATA switches (CR009A). The setting of the DATA switches determines whether 0's or 1's parity will be generated. 1's Parity out of P500 is input to AND gate J520 (CR005A) and 0's Parity from P500 is input to AND gate J521. AND gate J520 is made when the Data flip-flop is

set. AND gate J521 is made when the output of the set side of the Data flip-flop, fed through three inverters, is present on pin 1, when the Phase Enable flip-flop is set, and the Odd Parity signal is present. The output of J520 or J521 through inverter J522 is the Parity bit.

When the exerciser is connected to a seven track tape transport, the Write Data 2^6 and 2^7 signals into AND gate J523 and J524 (CR005B) are disabled by the 7 Track signal. In this way, only Write Data 2^0 through 2^5 signals are input to parity generator P500.

The Phase Enable flip-flop is set when Density status 2^1 is high, which indicates that the exerciser is connected to a phase enabled tape transport. When the Data flip-flop is set, the Data into J510 sets the Phase Enable flip-flop. The flip-flop set output enables either phase 0's Data or phase Parity bit. The Phase Enable flip-flop is cleared as soon as the Write Instruction goes low.



SHEET REVISION STATUS						REVISIONS				
						REV.	E.C.O.	DESCRIPTION	DATE	CHK'D	APP'D
				A	A	A		DRAWING RELEASE	1-7-72	GK	
				A	B	B	CE00 138	SEE ECO	4-21-72		

REFERENCE DRAWING	
ASS'Y-86817200	
DETAIL-86817300	

COMPONENTS EXCEPT AS NOTED			
	TOL	VALUE	SIZE
RES.	5%	OHMS	1/4W
CAP.		UF	

DRAFTSMAN	J. REYES	1/6/72
CHECKER		
ENGINEER		1/6/72
APPROVAL		1-7-72
		1/7/72

CONTROL DATA CORPORATION
CUSTOMER ENGINEERING DIVISION

LOGIC/SCHEMATIC DIAGRAM
28AF
WRITE
LOC B2

PRODUCT: TB113-A01
SIZE: D
DRAWING NUMBER: 86817400
REV: B
SHEET 1 OF 3
CODE IDENT 34011

* R31 IS SELECTABLE SET BETWEEN 1500 AND 330 TO SEQUENCE THE REQUIRED TIME.

** R32 IS SELECTABLE SET BETWEEN 4.7K AND 680 TO SEQUENCE THE REQUIRED TIME.

WRITE 2BAF CARD
CR005B

WRITE FLIP FLOP

The Write flip-flop is used to initiate sending of write data. When AND gate J525 is made, the logic "0" out to the Write flip-flop sets it. The one-shot circuit, composed of resistors R21 and R22 and capacitor C9, is used to provide a pulse to the set side of the Write flip-flop when J525 is made. This is done so that the flip-flop is set by a pulse and not a steady logic level so that when a clear signal comes back to the flip-flop it can be cleared. AND-gate J525 is made when a Write Permit signal, a Velocity signal, a Beginning of Tape and 377 count signal, and a Write Instruction are present. The Write Permit signal is high when the tape has moved far enough to insure generation of a record gap. The Velocity signal is high when the tape is moving at the proper speed. BOT and 377 is high when the tape has moved 377_8 counts from beginning of tape.

When the Write flip-flop is set, the set output goes to the clear of the Phase Enable flip-flop, to the Clear Direct of the Data flip-flop, and to the 1's Data flip-flop which removes the clear signal from those three flip-flops, permitting them to be set.

When the Write flip-flop is set, the clear output through OR-gate J528 starts the Q500 oscillator. This oscillator is used to vary the length of a record being written. The oscillator frequency is variable from 2 to 100 milliseconds by the RECORD LENGTH control (CR009A). Write data will be sent out until Q500 oscillator times out and then the Stop Enable flip-flop will get set. When the Stop Enable flip-flop is set, a logic "1" out on the set side goes to AND gate J535. When Write Data is present, J535 is made and the logic "0" output goes back and clears the Write flip-flop.

The Write flip-flop is cleared in three ways; (1) when the Stop Enable flip-flop is set and Write Data is present, (2) when the End of Tape signal and Write Data are present, so no writing will occur after the end of tape is reached, even though Q500 oscillator may not yet have timed out, and (3) by the Master Clear signal.

STOP ENABLE FLIP-FLOP

The Stop Enable flip-flop is set when the Q500 oscillator pulse is high. The oscillator starts when (1) the Write flip-flop is set, or (2) when Write is not selected and a Write Terminate is not being performed, but when the INT TEST switch is set to ON and the Go flip-flop is set.

The Stop Enable flip-flop is also set when a one-word write is performed and the OPERATION switch (CR009A) is not set to CONTINUOUS. In this case, when doing a One-Word Write, the Stop Enable flip-flop is set when the first Write Data comes in. The Stop Enable flip-flop set output then clears the Write flip-flop.

The Stop Enable flip-flop clears when a Go Pulse arrives. This is so that the Stop Enable flip-flop is initialized whenever the Go flip-flop sets.

The Stop Enable flip-flop is also cleared when the OPERATION switch is not set to RECORD. The flip-flop is thus held cleared. The Write flip-flop is cleared in this case when the End of Tape signal arrives.

When the Stop Enable flip-flop is set, the set output is ANDed at J535 with Write Data. The Write Data is present when the one-shot circuit, composed of resistors R7 and R8 and capacitor C3, has fired, which occurs every 200 nanoseconds or after every other flux change.

The output of AND gate J535 clears the Write flip-flop which disables the Write clock.

When the OPERATION switch is not set to RECORD, Q500 oscillator is disabled by the logic "0" through diode CR4. With Q500 disabled, the Stop Enable flip-flop cannot be set.

The Stop Pulse, when generated, provides an End of Operation signal when doing a Read or Rewind operation in Internal Test. When doing a Write operation in Internal Test, the End of Operation signal is generated from having data followed by an absence of data. The Stop Pulse is only generated during a Read operation.

The Stop Pulse is generated by the output from Q500 oscillator and also when a Write operation is not being performed and a Write Termination sequence is not being performed.

Q500 OSCILLATOR

The Q500 oscillator is initiated, (1) when the Write flip-flop is set, or (2) when a Write instruction is not selected, and when a Write Terminate sequence is not being performed, when INT TEST switch is ON, or in S/S and (3) after the Go flip-flop gets set.

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		INITIAL RELEASE	JPR	1-7-74	BK	
B	CE00117	SEE ECO	CE			

+5VDC
R14 1K
R15 1K
R16 1K
R17 1K
R20 1K
R12 1K
R13 1K
MOD200
EVN
ODD
P500
EVN
ODD
502 Z5
009A S19B-3 62 WRITE DATA 2^2
009A S20B-3 64 WRITE DATA 2^3
009A S21B-3 47 WRITE DATA 2^4
009A S22B-3 60 WRITE DATA 2^5
009A S17B-3 67 WRITE DATA 2^0
009A S18B-3 65 WRITE DATA 2^1
1'S PARITY
0'S PARITY
010A A3J2E
010A A3J2F
010A A3J2C
+5VDCII
C1 .1
C2 .1
C3 .1
C4 .1
+5VDC
R18 1K
009A S23B-3 72 WRITE DATA 2^6
0028 A3-29 74 7 TRACK
J523 126 Z3
+5VDC
R19 1K
009A S24B-3 73 WRITE DATA 2^7
J524 126 Z3
008A B5-56 75 WRITE PERMIT
008A B5-55 71 VELOCITY
008A B5-51 69 B.O.T.•377
006B B3-33 63 WRITE
J525 122 Z4
1US
R21 1K
CR2
C9 .001
+5VDC
R22 2.2
R23 3.3
K513 128 Z2
K512 126 Z3
WRITE
TP9
WRITE
CR5
009A S15-1 78 HC
1500
2M.S. TO 100M.S.
+5VDC
R25 2K
R26 22K
R27 1K
C11 470PF
5USEC
Q1 2N2647
Q2 2N3414
Q3 2N1106
R24 2K
C10 .68
R28 750
TP12
TP11
0068 B3-78 56 WRITE TERMINATE
CR6
+5VDC
R33 10K
009A S8A-1 41 INTERNAL TEST
007A B4-30 43 3D
009A R/S2-1 70 RECORD LENGTH
008A B5-78 77 3D PULSE
J526 129 Z1
J527 128 Y5
J528 126 Z3
CR3
CR4
J531 129 Z1
J532 129 Z1
J533 126 Y1
K515 129 Z1
K514 128 Z2
STOP ENABLE
J535 126 Y1
J534 126 Y1
+5VDC
R29 1K
009A R/S2-5 58 ONE WORD
009A S9-3 66 CONTINUOUS
TP10
J529 126 Y1
J530 129 Z1
STOP PULSE 54 A5-3 004B
WRITE DATA
007A B4-52 52 E.O.T.
J522 122 Z4
DISABLE READ DATA 48 A2-67 001A

005B

CONTROL DATA CORPORATION, CUSTOMER ENGINEERING DIVISION	LOGIC / SCHEMATIC DIAGRAM 2BAF WRITE LOC B2	CODE IDENT 34011	D	DWG NO 86817400	REV B
				SHEET	

PROGRAM CONTROL

CR006A

The exerciser PROGRAM CONTROL section permits Forward, Reverse, Write, and Rewind operations to be performed automatically, without requiring the operator to initiate each operation. The four instructions are loaded in memory and, depending upon the setting of the MODE switch, may be executed one per depression of the START pushbutton or in automatically repeated sequences after being initiated by pressing the START pushbutton.

The PROGRAM CONTROL consists primarily of M600 memory, I600 and O600 multiplexers, and the program address counter which is made up of Address 2^0, Address 2^1, and Address 2^2 (K603, K605 and K607) flip-flops. The program address counter and I600 multiplexer are used together to write instructions into memory. The program address counter and O600 multiplexer are used together to read instructions out of memory. The location at which the memory stores or reads out instructions is determined by the program address counter. The information that is stored in memory is determined by the INSTRUCTION pushbuttons (CR009B) and the I600 multiplexer. Information read from memory is determined by the program address counter and O600 multiplexer.

The M600 Memory is a 16-bit register file which is used as a 2-bit by 8-location memory. The memory is addressed on pins 14, 13, 4, and 5. The memory is enabled for writing by a logic "0" on pin 12. It is enabled for reading by a logic "0" on pin 11. Since pin 11 is always grounded (logic "0") the memory reads out at all times the information stored at the selected address. Data is input to the memory on pins 15, 1, 2, and 3 and is output on pins 10, 9, 7, and 6. The memory operates as a 2-bit by 8-location device by the addressing and accessing method used.

The output from Address 2^0 and Address 2^1 flip-flops determines the address in memory that the instruction will either be written into or read out from. The output from Address 2^2 flip-flop selects one of the two instructions that are being written into or read out of memory. Since the M600 memory was designed as a 4-bit by 4-location device, two instructions are always input to or output from it. The program address counter (Address 2^2 flip-flop output) and the I600 multiplexer select one of the two instructions to be input and the program address counter and O600 multiplexer select one of the two instructions to be output.

The program address counter, having three stages, has eight possible output states. Each time the counter goes through these eight states, which is one pass through the counter, the Address 2^0 and Address 2^1 flip-flops go through four states twice. That is, in one pass of the full counter from 000 through 111, the address 2^0 and address 2^1 flip-flops go from 00 through 11 twice. During the period the two flip-flops are going from 00 through 11 the first time, the Address 2^2 flip-flop is clear. During the second pass of Address 2^0 and 2^1 flip-flops from 00 through 11, the address 2^2 flip-flop is set. The output of the three flip-flops during one complete pass of the counter is as follows:

ADDRESS	2^0	0	1	0	1	0	1	0	1
ADDRESS	2^1	0	0	1	1	0	0	1	1
ADDRESS	2^2	0	0	0	0	1	1	1	1

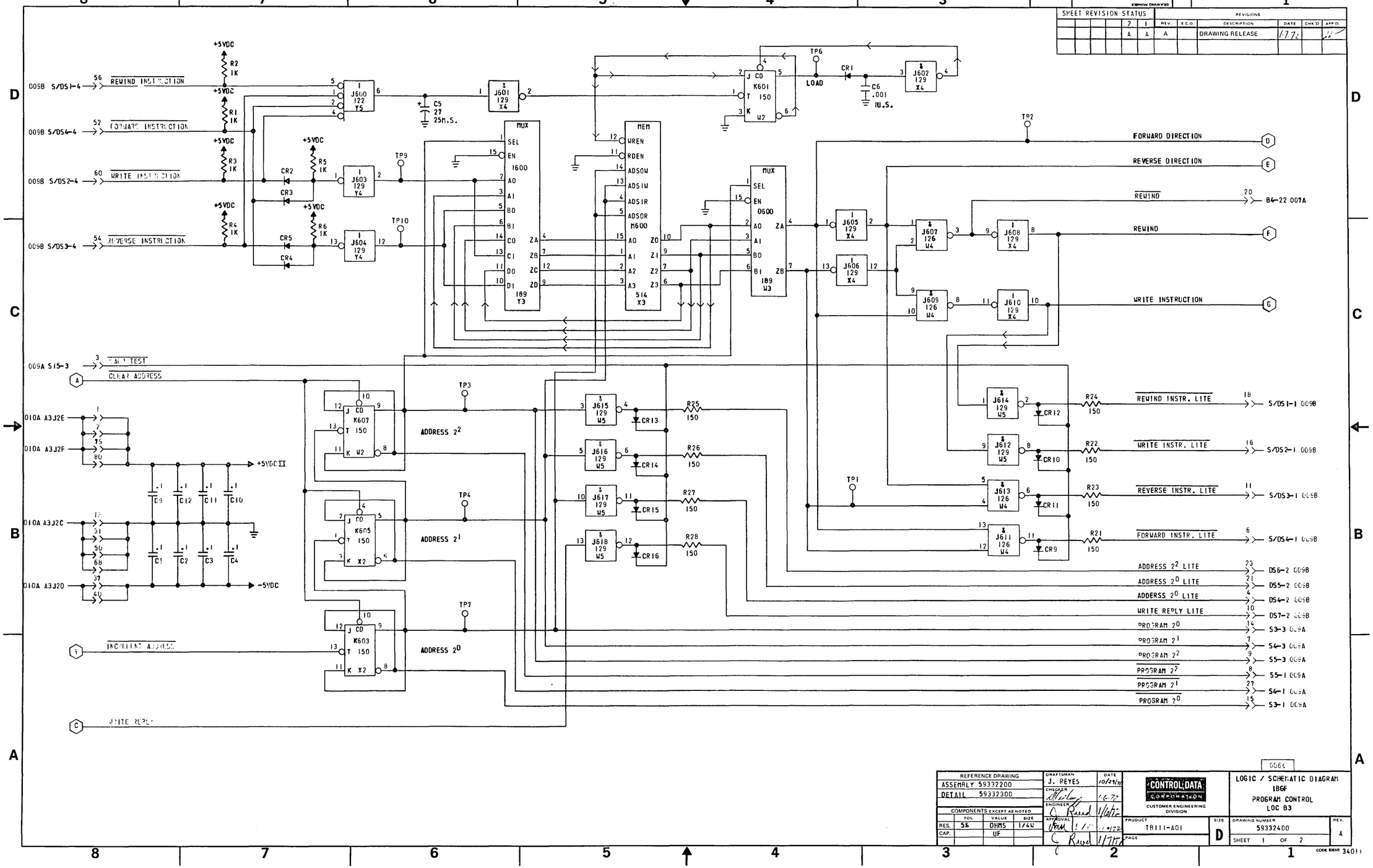
There are four possible instructions: Rewind, Forward, Write, and Reverse. The instructions have the following binary value when inverter J603 is assigned bit position 2^0 and J604 is assigned bit position 2^1.

	2^0 (J603)	2^1 (J604)
Rewind	0	0
Forward	1	1
Write	1	0
Reverse	0	1

Pressing one of the four INSTRUCTION pushbuttons, which have a ground to them when the MODE switch is set to LOAD, routs the ground to OR-gate J603 or J604, except REWIND which routs the ground only to J600. Since there is no input to J603 or J604 when REWIND is pushed, the +5 volts DC through R5 and R6 provides a logic "0" out of J603 and J604. The ground from any of the four pushbuttons into J600 provides a 25 millisecond delayed 1 microsecond Load pulse. The pulse is delayed 25 milliseconds by capacitor C5 to eliminate spikes on the output of the pushbutton. The 1 microsecond pulse is provided by Load flip-flop K601 and capacitor C6. The 1 microsecond logic "0" pulse into M600 memory at pin 12 permits writing the appropriate instruction during that 1 microsecond period.

When the set output from the Address 2^2 flip-flop is a logic "0", which it will be for the first four program address counter counts, the logic "0" into pin 1 of I600 multiplexer will gate through the information that is on inputs A0, B0, C0, and D0. The information on A0 and B0 will be the instruction from the INSTRUCTION pushbutton. The information that is on C0 and D0 is one of the two instructions being fed back from M600 memory. When the set output of Address 2^2 is a logic "1", which it is for the second four counts of the program address counter, the information on inputs C1, D1, A1, and B1 will be gated through. The information on C1 and D1 will be the instruction from the INSTRUCTION pushbutton and the information on A1 and B1 will be the other instructions fed back from memory.

For one complete pass through the program address counter (eight counts), eight instructions can be loaded in or read out. On the first count i.e., Address 2^0, 2^1, and 2^2 flip-flop set outputs are 000, the instruction from the INSTRUCTION pushbutton present on I600 input A0 and B0 and the instruction fed back from memory into C0 and D0 will be stored at the two addresses represented by logic "0's" into memory pins 14, 13, 4, and 5. On the second count, the instruction present on the same pins will be stored at the address represented by a logic "1" from Address 2^0 flip-flop into M600, pins 14 and 5, and the address represented by a logic "0" from Address 2^1 flip-flop into pins 13 and 4. Every time a Load pulse enables the memory, four bits (two instructions) are stored at one address. One of the instructions is from the INSTRUCTION pushbutton. The other instruction is the one fed back from the memory. During the first four program address counter counts, the first half of the memory locations are stored with new instructions from the INSTRUCTION pushbuttons and the second half are stored with instructions fed back. During the second four counts, new instructions from the pushbuttons are stored in the second half and the four instructions fed back are stored in the first half. This is done because two instructions are always stored at one time. One instruction is the new one; the other one is a previously stored instruction, restored.


SHEET REVISION STATUS
REVISIONS
REV. E.C.O. DESCRIPTION DATE CHK'D APP'D
A A DRAWING RELEASE 1-73
+5VDC
R2 1K
R1 1K
R3 1K
R5 1K
R4 1K
R6 1K
009B S/DS1-4
009B S/DS4-4
009B S/DS2-4
009B S/DS3-4
56 REWIND INSTRUCTION
52 FORWARD INSTRUCTION
60 WRITE INSTRUCTION
54 REVERSE INSTRUCTION
CR2
CR3
CR5
CR4
J600 122 Y5
J601 129 X4
J602 129 X4
J603 129 Y4
J604 129 Y4
J605 129 X4
J606 129 X4
J607 126 W4
J608 129 X4
J609 126 W4
J610 129 X4
C5 27 25M.S.
C6 .001 10U.S.
TP6
LOAD
CR1
TP9
TP10
TP2
MUX
SEL
EN
1600
A0
A1
B0
B1
C0
C1
D0
D1
189 Y3
MEM
WREN
RDEN
ADSOW
ADSIW
ADSIR
ADSOR
M600
514 X3
MUX
0600
M600
189 W3
FORWARD DIRECTION
REVERSE DIRECTION
REWIND
REWIND
WRITE INSTRUCTION
009A S15-3
MAN TEST
CLEAR ADDRESS
010A A3J2E
010A A3J2F
010A A3J2C
010A A3J2D
+5VDC II
-5VDC
C9 C12 C11 C10
C1 C2 C3 C4
J CD K607 T 150 K W2
J CD K605 T 150 K X2
J CD K603 T 150 K X2
ADDRESS 2^2
ADDRESS 2^1
ADDRESS 2^0
TP3
TP4
TP7
TP1
INCREMENT ADDRESS
WRITE REPLY
J615 129 W5
J616 129 W5
J617 129 W5
J618 129 W5
CR13
CR14
CR15
CR16
R25 150
R26 150
R27 150
R28 150
J614 129 W5
J612 129 W5
J613 126 W4
J611 126 W4
CR12
CR10
CR11
CR9
R24 150
R22 150
R23 150
R21 150
REWIND INSTR. LITE
WRITE INSTR. LITE
REVERSE INSTR. LITE
FORWARD INSTR. LITE
ADDRESS 2^2 LITE
ADDRESS 2^0 LITE
ADDERSS 2^0 LITE
WRITE REPLY LITE
PROGRAM 2^0
PROGRAM 2^1
PROGRAM 2^2
PROGRAM 2^2
PROGRAM 2^1
PROGRAM 2^0
B4-22 007A
S/DS1-1 009B
S/DS2-1 009B
S/DS3-1 009B
S/DS4-1 009B
DS6-2 009B
DS5-2 009B
DS4-2 009B
DS7-2 009B
S3-3 009A
S4-3 009A
S5-3 009A
S5-1 009A
S4-1 009A
S3-1 009A
REFERENCE DRAWING
ASSEMBLY 59332200
DETAIL 59332300
COMPONENTS EXCEPT AS NOTED
TOL VALUE SIZE
RES. 5% OHMS 1/4W
CAP. UF
DRAFTSMAN J. PEYES 10/24/72
CHECKER
ENGINEER C. Reed 11/6/72
APPROVAL 11/7/72
CONTROL DATA CORPORATION
CUSTOMER ENGINEERING DIVISION
LOGIC / SCHEMATIC DIAGRAM
186F
PROGRAM CONTROL
LOC 83
PRODUCT TB111-A01
SIZE D
DRAWING NUMBER 59332400
REV. A
SHEET 1 OF 2
CODE IDENT 34011

PROGRAM CONTROL 1BGF CARD

CR006B

INTERNAL WRITE REPLY FLIP-FLOP

The Internal Write Reply flip-flop (K612/K613) provides a simulated Write Reply signal when the exerciser is in the Internal Test Mode. The signal normally comes from the tape transport indicating that the write and erase current is on. When the flip-flop is set, the logic "0" clear output through J636 and J618 (CR006A) lights the WRITE REPLY light. The clear output also goes through J636 to AND gate J641 and, during Time 3 of the timing chain and also when the Direction flip-flop is cleared, sets the Write Terminate flip-flop.

The Internal Write Reply flip-flop is set by the Write signal when AND gate J644 is made. This occurs when the INT TEST switch is set to ON, when a Write instruction is present, when the Direction flip-flop is set indicating a forward direction, and when the Go pulse signal is present from logic card B4(CR007A).

The Internal Write Reply flip-flop is cleared, providing a logic "1" output on pin 6, when INT TEST is set to OFF, providing a ground on pin 5 of K612. When not in Internal Test, the flip-flop is held cleared. The Write Reply signal then comes from the tape transport through R600 receiver.

The flip-flop is also cleared when the Direction flip-flop is cleared, indicating a Reverse direction, and the Go pulse from B5(CR008A) is present.

FORWARD FLIP-FLOP

The Forward Flip-Flop (K611) provides a Forward or Reverse command to the tape transport. When the flip-flop is set the set output is a Forward command and when it is cleared the clear output is a Reverse command.

The flip-flop is set when the Forward Direction signal is received from memory through J638 and $\overline{\text{Backspace}}$ is present from the clear output of the Backspace flip-flop on logic card A5(CR004B)

The flip-flop clears when a Reverse Direction signal is received from memory through J640 and the $\overline{\text{Backspace}}$ is again present.

The flip-flop toggles when the Backspace signal is present from the Backspace flip-flop and Time 2 from the internal timing chain is present. When toggled by Backspace and Time 2, the flip-flop will provide a $\overline{\text{Forward}}$ signal out if it was Forward, and vice versa. During Backspace operations, the flip-flop is inhibited from being set or cleared.

BREAKPOINT FLIP FLOP

The Breakpoint flip-flop is used to increment or to clear to zero the program address counter (Address 2^0, 2^1, and 2^2 flip-flops) on logic card B3(CR006A). The clear output of the flip-flop, in conjunction with other signals, performs this function through gates J628 and J629 and gates J631 and J633.

The program address counter is incremented by a logic "0" out of AND gate J628 or AND gate J629. A logic "0" is output from J628 when: (1) the Breakpoint flip-flop is cleared indicating we are not at breakpoint, (2) an End of Operation signal is present either from Load Point or End of Tape when not in the Record mode, or from the internally generated End of Operation signal from logic card A5(CR004B) when in the Record mode, (3) the $\overline{\text{Backspace}}$ signal from A5(CR004B), indicating a backspace operation is not in progress, is present. During a backspace operation the address should not be changed.

A logic "0" is output from J629 when the START pushbutton is pressed and the MODE switch is set to LOAD.

The program address counter can be cleared to zero by a logic "0" out of AND gate J631 or AND gate J633. A logic "0" is output from J633 when a Master Clear is present from the INT CONTROL switch. A logic "0" is output from J631 when: (1) the Breakpoint flip-flop is set indicating the exerciser is at breakpoint, (2) an End of Operation is present as described above, and (3) the Backspace signal is present.

The Breakpoint flip-flop is set when the output of the Address 2^0, Address 2^1, and Address 2^2 flip-flops (CR006A), routed through the three BREAKPOINT switches (CR009A), coincides with the setting of the three switches. The output of the switches (BP 2^0, BP 2^1, and BP 2^2) goes to AND gate J619. When either Time 2 is present through J621 and J620 or when the START switch is pressed, the Breakpoint flip-flop sets.

The Breakpoint flip-flop is cleared when; (1) the Master Clear signal is present from the INT CONTROL switch, or (2) during Time 1, or (3) when the MODE switch is set to LOAD. The flip-flop is held cleared during a Load sequence so the program address counter is not cleared to zero during the load.

UNLOAD

When the TAPE CONTROL switch (CR009A) is set to UNLOAD, a ground is routed to the 1 microsecond one-shot circuit composed of R19, R20, and C8. The signal out is a 1 microsecond negative going $\overline{\text{Rewind Unload}}$ pulse through T103 Transmitter (CR001B) to the tape transport to unload tape.

REWIND

When the TAPE CONTROL switch is set to REWIND, a ground is routed to one-shot circuit composed of R17, R18, and C7. The signal out is a 1 microsecond negative going pulse through OR-gate J647, through T600 transmitter, to the tape transport to rewind tape.

A rewind signal also is transmitted to the tape transport through T600 when AND gate J646 is made. This occurs when a Rewind instruction from memory is present, when the Go flip-flop (CR008A) is set producing the Go Pulse, and when the Write Terminate flip-flop (K614/K615) is cleared. The tape transport is prevented from doing a Rewind during a write sequence until after a Write Jog sequence has been performed.

WRITE TERMINATE FLIP-FLOP

The Write Terminate flip-flop (K614/K615) is used to provide a record gap after a record has been written (Write Jog sequence). When the flip-flop is set, a forward is forced for approximately one inch of tape after a write operation before the first subsequent reverse operation.

The Write Terminate flip-flop is set when AND gate J641 is made. This occurs when: (1) a Reverse command is given, as indicated by a logic "1" out of the clear side of the Forward flip-flop (K611), and (2) Write Reply signal is active, and (3) Time 3 from the timing chain.

The Write Terminate flip-flop clears when the $\overline{\text{Busy}}$ pulse is received, indicating that tape motion has stopped.

WRITE

The Write signal is transmitted to the tape transport when AND gate J644 is made. This occurs when: (1) the direction is Forward as indicated by the Forward flip-flop being set, and (2) a Write instruction from memory is present, and (3) Write Enable is present from the tape transport indicating a write ring is installed, or from the INTERNAL TEST switch being in ON or S/S, and (4) GO from the Go flip-flop is present.

FORWARD

The Forward signal to the tape transport is present when either the Write Terminate flip-flop is set or the Forward flip-flop is set, either one providing a logic "0" into OR-gate J643.

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		INITIAL RELEASE		1-7-1-		JJ

009A S16B-2 66 START SWITCH
007B B4-78 58 TIME 2
009A S3-2 48 BP 2⁰
009A S4-2 43 BP 2¹
009A S5-2 49 BP 2²
007B B4-71 62 TIME 1
009A S10A-1 64 LOAD
004B A5-63 72 EOO
009A S9-1 59 CONTINUOUS
004B A5-18 70 LP'+ EOT EOO
009A S15-1 63 MC
004B A5-72 46 BACKSPACE
6 WRITE INSTRUCTION
007A B4-30 75 GO
D FORWARD DIRECTION
E REVERSE DIRECTION
004B A5-70 29 BACKSPACE
009A S14-1 77 MANUAL REWIND
F REWIND
008A B5-78 35 GO PULSE
007B B4-76 73 TIME 3
009A S8A-1 61 INTERNAL TEST
009C J1-N2 67 WRITE ENABLE (-)
009C J1-N8 65 WRITE ENABLE (+)
009C J1-P6 55 WRITE REPLY (-)
009C J1-R3 57 WRITE REPLY (+)
008A B5-74 69 BUSY PULSE
009A S14-3 53 UNLOAD

+5VDC R9 560
CR7
CR6
J620 129 Y4
J621 129 Y4
J619 122 Y5
K609 129 Y4
K608 128 Y2
BREAKPOINT
TP8
BREAKPOINT 44 NOT USED
J628 128 Y2
INCREMENT ADDRESS B
J627 129 Z4
J629 126 Z3
J630 129 Z4
J622 129 Y4
CR8
+5VDC R10 1K
J624 126 Z3
J625 129 Z4
J626 129 Z4
+5VDC R8 1K
J631 128 Y2
CLEAR ADDRESS A
J623 126 Z3
+5VDC R7 10K
J632 129 Z4
J633 129 Z4
FORWARD 71 B4-58 007A
+5VDC R29 1K
XMT T600 176 X5
SELA
SELB
AB
A0 ZA+
A1 ZA-
B0 ZB+
B1 ZB-
R32 56
R33 56
R30 56
R31 56
WRITE (+) 17 J1-T7 009C
WRITE (-) 19 J1-S9 009C
REWIND (+) 25 J1-P8 009C
REWIND (-) 24 J1-P1 009C
WRITE 33 B2-63 005B
WRITE ENABLE 74 S26-11 009B
WRITE REPLY C
J638 126 X1
J640 126 X1
J639 126 X1
K611 151
CD SO
J T
K WI
TP5
CR17
+5VDC R16
CR18
FORWARD
J644 128 Y1
J645 129 Z2
TP11
J647 126 Z1
J646 128 Y1
+5VDC R17 2.7M
1US C7 .01
R18 1K
J643 126 Z2
FORWARD 12 B4-42 007A
TP12
J634 129 Z2
J635 126 Z3
K613 126 Z1
INTERNAL WRITE REPLY
J637 126 Z1
K612 126 Z1
J641 128 Y1
K615 129 Z2
WRITE TERMINATE 76 B4-54 007A S26-23 009B
WRITE TERMINATE
J642 129 Z2
K614 129 Z2
WRITE TERMINATE 78 B2-56 005B
CR19
J636 129 Z2
+5VDC
1US R19 2.7M C8 .01
R20 1K
REWIND UNLOAD 45 A2-36 001B
REC R600 162 Z5
SELA
SELB
AB
A+ ZA
A-
B+ ZB
B-
R11 56
R12 56
R14 56
R15 56
R13 1K +5VDC

0068

CONTROL DATA CUSTOMER ENGINEERING DIVISION
LOGIC / SCHEMATIC DIAGRAM
18GF~
PROGRAM CONTROL
LOC B3
CODE IDENT 34011
D
DWG NO 59332400
REV A
SHEET 2

MOTION CONTROL I 2AZF CARD
CR0079A

REPEAT FLIP FLOP

Whenever the START pushbutton is pressed, a logic "0" pulse is applied to J700 with a logic "1" out to pin 5 of J701. Whenever the MODE switch (CR0079A) is set to LOAD, a logic "1" is applied to pin 4 of J701 (when set to LOAD the AND-gate J701 is inhibited). The two logic "1's" into J701 provide a logic "0" out and the Repeat flip-flop is set. The logic "0" out of J701 also sets the Go flip-flop. When Go is set, the clear output (logic "0") goes to J703. After a 1 microsecond delay caused by capacitor C11, a logic "1" is available on pin 10 of J704. If the MODE switch is set to STEP, J702 is enabled and a logic "1" is available at pin 9 of J704. With AND gate J704 being made, the Repeat flip-flop is cleared. In other words, when START is pressed with the MODE switch in STEP, the Repeat flip-flop is set and the Go flip-flop is set. One microsecond later the Repeat flip-flop is cleared, therefore only one operation will be performed.

When the MODE switch is set to RUN and the START pushbutton is pressed the Repeat and Go flip-flops are set, however AND gate J704 is not made because of the logic "1" on the input to J702 and so the Repeat flip-flop does not get cleared. The Repeat flip-flop can only be cleared then by setting the MODE switch to STEP or setting the INT CONTROL switch to MC.

GO FLIP FLOP

The Go flip-flop (K702/K703) is set whenever any instruction (Forward, Reverse, Write, or Rewind) is executed. No instruction can be executed until the flip-flop sets.

The Go flip-flop sets whenever the START pushbutton is pressed, when MODE is not set to LOAD, by the logic "0" from J701. The set output goes to J709 and J710. When a Forward instruction from memory is present on pin 10 of J710, a Forward signal is output from J712 to the tape transport and also to the FORWARD (STATUS) indicator on the operator panel.

When a Reverse instruction from memory is present on pin 1 of J709, and if a Write Terminate sequence is not in progress and a Rewind is not commanded, the Reverse signal is output from J711 to the tape transport and to the REVERSE (STATUS) indicator. The Rewind and Write Terminate inhibit a Reverse signal from being output.

The Go flip-flop is also set when the Write Terminate flip-flop (CR0068) is cleared. The set output (logic "0") to J705 provides a logic "1" to J706 with a logic "0" out of J706. The one-shot circuit composed of R2, R3, and C12 provide a one microsecond negative going pulse to the set side of the Go flip-flop. This is done so that after a Forward Jog, the Go flip-flop is set to permit a Reverse signal output.

The Go flip-flop is also set when AND-gate J708 is made. This occurs when the Repeat flip-flop is set and the Set Enable signal is present. The Set Enable signal may come from either J736 or J737 (CR0078). AND-gate J737 is made when the PAUSE TIME switch (CR0079A) is set to OFF and Time 6 from the timing chain is present. The timing chain is initiated after the Busy signal from the tape transport, indicating tape is in motion, rises and then falls. Time 6 is the sixth one microsecond pulse after the timing chain is initiated. In other words when PAUSE TIME is OFF and Time 6 comes up, the Go flip-flop sets. When PAUSE TIME is ON, J735 is made and a logic "1" is on pin 10 of J736. When a logic "1" pulse from oscillator circuit Q700 is available on pin 9 of J736, then that AND-gate is made and the Set Enable signal is output from J738. Oscillator Q700 is enabled when the Pause flip-flop is set. The Pause flip-flop is set when the Time 6 signal comes up and is cleared by the oscillator output signal. Oscillator Q700 may be adjusted by the PAUSE TIME control (CR0079A) from a two millisecond to a 100 millisecond output.

The Go flip-flop is cleared as follows.

1. When $\overline{\text{Ready}}$ is present. The Go flip-flop cannot be set when $\overline{\text{Ready}}$ is present.
2. When INT CONTROL is set to MC.
3. When an End of Operation signal is present which comes from Load Point, End of Tape, or generated internally after having received data followed by a period of at least 50 microseconds when no data is received.
4. When a Reverse instruction is present and the tape transport is at Beginning of Tape.
5. When a Forward instruction is present and the tape transport is at End of Tape and a Write Terminate is not present. This is to permit doing a Write Jog even though at end of tape.
6. When the Write Terminate signal and the End Write Terminate signal are both present. The End Write Terminate signal is present 77_8 tachometer pulses after Write Terminate starts. Therefore after 77_8 tachometer pulses after Write Terminate, the Go flip-flop is cleared.

SHEET REVISION STATUS						REVISIONS					
				2	1	REV.	E.C.O	DESCRIPTION	DATE	CHK'D	APP'D
				A	A	A		DRAWING RELEASE	4-7-72	BK	
				B	B	B	CE00 097	SEE ECO	7MAR72	RJC	

009A S15-3 → 24 LAMP TEST

(A) SET ENABLE

006A B3-20 → 22 REWIND

009A S16B-2 → 36 START SWITCH

009A S10A-1 → 46 LOAD

009A S15-1 → 48 MC

009A S10B-1 → 28 STEP

006B B3-76 → 54 WRITE TERMINATE

(H) READY

J700 129 X5 · J701 126 X4 · K701 126 X4 · TP5 · J708 126 X4 · REPEAT · K700 128 X3 · TP4 · R1 +5VDC 1K · J702 129 X5 · J704 126 X4 · J703 129 X5 · C11 .001 1US · +5VDC · R2 1K · C12 .001 · CR1 · R3 10K · J705 129 Y5 · J706 129 Y5 · J707 129 Y5 · J716 129 Y5 · J717 129 X5 · J718 126 Y4 · J719 128 X3 · J720 126 Y4 · J709 122 W3 · J711 129 W5 · J710 126 Y4 · J712 129 W5 · TP2 · K703 128 X3 · 90 · J715 129 X5 · K702 129 X5 · TP3 · J713 129 Y5 · J714 129 Y5

006B B3-20 → 32 EOD

006B B3-71 → 58 FORWARD

(C) B.O.T.

006B B3-12 → 42 FORWARD

(D) E.O.T.

006A B5-55 → 56 END WRITE TERMINATE

(E) READY

(F) BUSY

J721 129 W5 · CR2 · R5 150 · REVERSE LITE → 21 DS8-2 006B

J722 129 W5 · CR3 · R6 150 · FORWARD LITE → 19 DS9-2 006B

J723 129 W5 · CR4 · R7 150 · EOT LITE → 14 DS10-2 006B

J724 129 W5 · CR5 · R8 150 · BOT LITE → 12 DS11-2 006B

J725 129 W4 · CR6 · R9 150 · READY LITE → 9 DS13-2 006B

J726 129 W4 · CR7 · R10 150 · BUSY LITE → 4 DS12-2 006B

I/O REVERSE → 20 B5-24 006B · S26-19 009B

(G) 30 → S26-22 006B · B2-43 006B · B3-75 006B · B5-53 006A

I/O FORWARD → 16 B5-26 006B · S26-18 006B

EOT → 52 A5-20 006B · B2-52 006B

BOT → 35 A5-22 006B · B5-44 006A

WRITE TERMINATE (H)

READY → 10 NOT USED

BUSY → 57 A2-60 006A · B5-72 006A · S26-16 009B

REFERENCE DRAWING	
ASSEMBLY	86816900
DETAIL	86817000

COMPONENTS EXCEPT AS NOTED			
	TOL	VALUE	SIZE
RES.	5%	OHMS	1/4W
CAP.		UF	

DRAFTSMAN		DATE 1/24/72
CHECKER		1-6-72
ENGINEER		1/6/72
APPROVAL		1/6/72
		1/7/72

CONTROL DATA CORPORATION
CUSTOMER ENGINEERING DIVISION

LOGIC/SCHEMATIC DIAGRAM
2AZF
MOTION CONTROL I
LOC B4

PRODUCT T8113-A01 · SIZE D · DRAWING NUMBER 86817100 · REV. B · SHEET 1 OF 2 · PAGE

CODE IDENT 34011

MOTION CONTROL I 2AZF CARD

CR0078

TIMING CHAIN

The timing chain is developed by K707, K709, K711, K713, K715 and K717 flip-flops. The flip-flops are enabled when the Busy signal from the tape transport, through R701 receiver and J730, J732, and J733 gates, drops. During Write Terminate the timing chain is inhibited by a logic "1" on pin 10 of J732.

INTERNAL TEST

When the INTERNAL TEST switch is set to ON, a logic "1" through R26 to J727 provides a logic "0" to J728. The logic "1" out of J728 is the Ready signal. When INTERNAL TEST is not on, the Ready signal comes from the tape transport through R701 receiver. The logic "0" from J727 also goes to pin 6 of R700 and R701 receivers, which inhibits their operation. When R700 is inhibited, the output on pins 4 and 9 are the $\overline{\text{Beginning of Tape}}$ and $\overline{\text{End of Tape}}$ signals. When R701 is inhibited, the output on pins 4 and 9 are the $\overline{\text{Ready}}$ and $\overline{\text{Busy}}$ signals.

When INTERNAL TEST is set to ON, a Busy signal will be output from J730 as soon as the Go flip-flop sets. When the Go flip-flop is cleared, AND-gate J731 outputs a logic "1" which is delayed 100 microseconds by C18. This delay is so that Busy will not be dropped until 100 microseconds after motion (Go command) has been removed.

When the INT TEST switch is set to S/S (START/STOP), B4-38 is connected to ground, approximating a logic "0" input to J727. This forces a logic "1" output from J727 and provides a constant enable for receivers R700 and R701. The Ready, Busy, Bot, and EOT are thereby permitted to have the same effects as in normal operation; however, the remaining receivers are inhibited (see CR0001A, CR0002A, and CR0006B).

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		INITIAL RELEASE				
B	CE00097	SEE ECO				

009A R/SI-5 → 26 PAUSE TIME OFF
009A R/SI-1 → 5 PAUSE TIME

+5VDC
R11 1K
R13 56 R12 56
R19 56 R20 56
R21 1K
R23 56 R22 56
R24 56 R25 56
R26 1K → +5VDC

009C J1-C5 → 70 BOT (-)
009C J1-D3 → 69 BOT (+)
009C J1-D9 → 66 EOT (-)
009C J1-E7 → 64 EOT (+)
009C J1-V3 → 74 READY (-)
009C J1-V6 → 72 READY (+)
009C J1-T5 → 62 BUSY (-)
009C J1-T6 → 60 BUSY (+)

REC SELA SELB A↕B R700 A+ A- B+ B- ZA ZB 162 Z5
REC SELA SELB A↕B R701 A+ A- B+ B- ZA ZB 162 Z4

J727 129 X2 · J728 126 Y4 · J729 129 X2 · J730 126 Y3 · J731 126 Y3 · J732 126 Y3 · J733 126 Y3 · J734 129 X2 · J735 129 X2 · J736 126 Y1 · J737 126 Y1 · J738 129 X2 · J745 129 X2

K705 126 Y1 · K704 126 Y1 · PAUSE · TP6 · TP1

Q700 +5VDC 2MS TO 100MS
R14 2K · R15 2K · R16 22K · R17 1K
Q1 2N2647 · Q2 2N3414
C13 .68 · C14 470PF 50S
Q3 DD1106
CR8

TP11 · TP10 · TP9

TIME 6 → 77 NOT USED
TIME 4 → 73 NOT USED
TIME 5 → 75 NOT USED

B.O.T. → C
E.O.T. → D
BUSY → F
READY → E
READY → B
10 SET ENABLE → A

(S) GO
009A S8B-1 → 38 INTERNAL TEST
C18 .1UF 100US

J CD K713 T 150 K Z3 · TIME 4 · C15 .001 · CR9 · J742 129 Y2
J CD K715 T 150 K Z2 · TIME 5 · C16 .001 · CR10 · J743 129 Y2
J CD K717 T 150 K Z1 · TIME 6 · C17 .001 · CR11 · J744 129 X2
1US

(11) WRITE TERMINATE

TP7 · TP12 · TP8

J CD K707 T 150 K Z3 · TIME 1 · C19 .001 · CR12 · J739 129 Y2
J CD K709 T 150 K Z2 · TIME 2 · C20 .001 · CR13 · J740 129 Y2
J CD K711 T 150 K Z1 · TIME 3 · C21 .001 · CR14 · J741 129 Y2
1US

TIME 1 → 71 → S26-20 009B · A5-61 004B · B3-62 006B
TIME 2 → 78 → A5-78 004B · B3-58 006B
TIME 3 → 76 → A5-5 004B · B3-73 006B

LAST MOTION REVERSE → 45 → S26-21 009B

010A A3J2E → +5VDCII
010A A3J2F
010A A3J2C
010A A3J2D → -5VDC
C2 C3 C4 C5 C1 27
C7 C8 C9 C10 C6 27

+5VDC
REC SELA SELB A↕B R702 A+ A- ZA 162 X15

009C J1-B5 → 44 LAST MOTION REVERSE +
009C J1-A8 → 47 LAST MOTION REVERSE -
R27 56
R28 56

0078

CONTROL DATA CORPORATION — CUSTOMER ENGINEERING DIVISION	LOGIC/SCHEMATIC DIAGRAM 2AZF MOTION CONTROL 1 LOC B4	CODE IDENT 34011	D	DWG NO 86817100	REV B
				SHEET 2	

MOTION CONTROL II 1BFF CARD

CR008A

END WRITE TERMINATE FLIP FLOP

The End Write Terminate flip-flop (K804/K805) is used to terminate the Write Jog sequence after 100_8 tachometer pulses or 0.800 inch of tape has advanced since Write Jog sequence was initiated. The flip-flop is set when output Z2 of C801 counter goes to a logic "1". The Tachometer I and II pulses, together with a not Beginning of Tape condition, are ANDed at J801 and then counted at C800 counter. After 17_8 tachometer pulses, C800 outputs a logic "1" from pin 12 to C801 counter, pin 5. C801 counter outputs a logic "1" from Z2 on the 100_8 count. The logic "1" from C801 counter through J803 sets the flip-flop.

The End Write Terminate signal, which clears the Go flip-flop (CR007A), stops motion. When the Busy signal from the tape transport, indicating that tape motion has stopped, is received on pin 13 of K801 flip-flop, it sets and the clear output clears the End Write Terminate flip-flop. The $\overline{\text{Busy}}$ signal from the set output of K801 is a one microsecond pulse created by capacitor C9. The clear output of K801 also clears C800 and C801 counters to zero. Flip-flop K807 sets when the Go signal from logic board B4 (CR007A) is present on pin 1. A one microsecond pulse produced by capacitor C11 clears C800 and C801 counters to zero.

BOT AND 377 FLIP FLOP

The BOT and 377 flip-flop (K802/K803) is used to provide a 3.20 inch distance at the beginning of tape before any writing is enabled. The flip-flop is set at Beginning of Tape. It is cleared by a logic "1" from pin 12 of C801 counter which occurs on the 400_8 tachometer pulse. The clear output, available after BOT and after 377_8 tachometer pulses, enables writing on the tape.

INTERNAL VELOCITY FLIP FLOP

The Internal Velocity flip-flop (K808/K809) provides a Velocity signal when the INT TEST switch is set to ON.

When INT TEST is set to ON or S/S, a logic "1" is present at pin 2 of J807. When the GO flip-flop (CR007A) is set, a logic "1" is present at pin 1 of J807. The logic "0" out of J807 is delayed one millisecond by capacitor C10 and then sets the Internal Velocity flip-flop.

The clear output through J813 provides the Velocity signal in Internal Test. When not in Internal Test, the Velocity signal from the tape transport enables J813 and provides the Velocity signal out.

The clear output of the Internal Velocity flip-flop is delayed one microsecond by capacitor C12 and then goes to AND gate J811. When the Go signal from the Go flip-flop is on pin 12 of J811, the AND gate is made and the Write Permit signal is output. One millisecond after the Go signal is present the Velocity signal is output and one microsecond after that the Write Permit signal is output. When not in Internal Test, the Write Permit signal from the tape transport is present on pin 13 of J812 and the Write Permit signal is output.

The Internal Velocity flip-flop is cleared when the Go signal from the Go flip-flop goes to a logic "0". The logic "0" from the Go flip-flop also disables AND gate J811 and the Write Permit signal is removed.

SHEET REVISION STATUS						REVISIONS					
				2	1	REV.	E.C.O.	DESCRIPTION	DATE	CHK'D	APP'D.
				A	A	A		DRAWING RELEASE	1-7-72		

007A B4-35 B.O.T.
001A A2-75 TACH I
001A A2-76 TACH II
007A B4-57 BUSY
007A S8A-1 INTERNAL TEST
007A B4-30 SB
002A A3-67 WRITE PERMIT I/O
001A A2-65 VELOCITY I/O
010A A3J2E +5VDC II
010A A3J2F
010A A3J2C
010A A3J2D -5VDC

B.O.T.•377 → NOT USED
B.O.T.•377 → B2-69 005B
END WRITE TERMINATE → B4-56 007A
BUSY PULSE → B3-69 006B
WRITE PERMIT → B2-75 005B, S26-15 009B
GO → A
VELOCITY → A4-78 003A, B2-71 005B, S26-12 009B
GO PULSE → B3-35 006B, B2-77 005B, A4-76 003A

REFERENCE DRAWING			
ASS'Y-59331900			
DETAIL-59332000			
COMPONENTS EXCEPT AS NOTED			
	TOL	VALUE	SIZE
RES.	5%	OHMS	1/4W
CAP.		UF	

	NAME	DATE
DRAFTSMAN	J. REYES	10-25-71
CHECKER		11-6-72
ENGINEER		11/6/72
APPROVAL		11-6-72
		11/7/72

CONTROL DATA
CUSTOMER ENGINEERING DIVISION

008A

LOGIC / SCHEMATIC DIAGRAM
IBFF-
MOTION CONTROL II
LOC 35

PRODUCT	SIZE	DRAWING NUMBER	REV.
IB113-A01	D	59332101	A
PAGE		SHEET 1 OF 2	

CODE IDENT 34011

MOTION CONTROL II 1BFF CARD

CR008B

T800 TRANSMITTER

The I/O Forward and I/O Reverse signals from logic board B4 (CR007A) are output to the tape transport through T800 transmitter.

R800 RECEIVER

The four Density status lines from the tape transport are received on R800 receiver and the status is then output to the DENSITY STATUS indicators (CR009B) and to logic board B2.

SIGNAL MONITOR FLIP FLOP

The Signal Monitor flip-flop (K818/K819) is set whenever any signal is routed through the SIGNAL MONITOR switch (CR009B) to J822, with its resultant logic "0" out to pin 1 of the flip-flop. The set output lights the SIGNAL MONITOR indicator (CR009B). The clear output is delayed 25 milliseconds by capacitor C13 and then clears the flip-flop. In this manner, any pulse into the flip-flop will light the indicator for 25 milliseconds so it can be seen by the operator. If the signal that sets the flip-flop is a steady logic level, the indicator remains lit as long as the logic level is present. When the logic level is removed the flip-flop clears after 25 milliseconds and the indicator goes out.

FAULT FLIP FLOP

The Fault flip-flop (K816/K817) is set whenever one of the five fault lines from the tape transport is activated. The set output lights the FAULT indicator (CR009B). The flip-flop is cleared by a logic "0" (ground) from the FAULT pushbutton when it is pressed. If any of the Fault lines are active when the FAULT pushbutton is pressed, the flip-flop will set and the FAULT indicator will light again as soon as the push-button is released.

WRITE PERMIT ERROR FLIP FLOP

A Write Permit Error occurs when a Write Permit signal is received without a Velocity signal being received.

The Write Permit Error flip-flop (K814/K815) sets when the Write Permit signal from logic board B5 (CR008A) is received at AND gate J816 and the Velocity signal from B5 is not received at J816. When the Velocity signal is not present at inverter J814, a logic "1" is output from J814 to J816, the AND gate is made, and the logic "0" out sets the flip-flop. The set output lights the WRITE PERMIT ERROR indicator.

The Write Permit Error flip-flop is cleared when the WRITE PERMIT ERROR pushbutton is pressed. When the flip-flop is cleared the indicator goes out.

VELOCITY ERROR FLIP FLOP

A Velocity Error occurs if, after the Go signal and the Velocity signal are both high, the Velocity signal goes low while the Go signal remains high.

The Velocity Error flip-flop sets when the Go signal from B5(CR008A) is high at pin 1 of AND gate J815, the Velocity signal from B5 through inverter J814 is a logic "1" on pin 2 of J815, and the Velocity Resync flip-flop (K810/K811) is set and provides a logic "1" to pin 13 of J815. When the Velocity Error flip-flop is set, the VELOCITY ERROR indicator lights.

Whenever the Velocity signal is high and the Go signal is high, the Velocity Resync flip-flop is set. The set output provides a constant logic "1" to J815. As long as the Velocity signal remains high, the logic "0" from J814 prevents AND gate J815 from being made. If the Velocity signal goes low, while the Go signal remains high, a logic "1" from J814 enables AND gate J815 and the Velocity Error flip-flop gets set. The Velocity Resync flip-flop is cleared after the Go signal goes low and the Velocity signal again goes high.

The Velocity Error flip-flop may be cleared by pressing the VELOCITY ERROR pushbutton. The indicator then goes out.

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		INITIAL RELEASE	JPR	1/12		

007A B4-16 → 26 I/O FORWARD
007A B4-20 → 24 I/O REVERSE
009A S15-3 → 4 LAMP TEST
C WRITE PERMIT
009B S/DS8-4 → 42 CLEAR W.P. ERROR
A GO
B VELOCITY
009B S/DS6-4 → 32 CLEAR VELOCITY ERROR
009B S26-25 → 76 SIGNAL MONITOR
002B A3-42 → 30 COOLING AIR FAULT
002B A3-56 → 14 LOOP FAULT
002B A3-43 → 38 VACUUM FAULT
002B A3-39 → 36 ERASE CURRENT FAULT
002B A3-24 → 34 LOAD FAULT
009B S/DS7-4 → 28 CLEAR FAULT

+5VDC
R14 1K
R3 1K
R4 10K
R2 1K
R5 1K
R19 1K

XMT. T800 176 W5
3 SELA
4 SELB
10 A,B
1 AO ZA+ 13
2 AI ZA- 12
5 BO ZB+ 8
6 BI ZB- 9

R10 56
R11 56
R12 56
R13 56

FORWARD (+) → 22 J1-L9 009C
FORWARD (-) → 20 J1-L3 009C
REVERSE (+) → 16 J1-N4 009C
REVERSE (-) → 18 J1-M6 009C

J816 126 X4
J815 129 W2
J814 129 W2
J815 128 X5
J822 129 Z4
J817 129 W4
J818 129 W4
J819 129 W3
J820 129 W3
J821 129 W3

K815 129 W2
K814 129 W2
WRITE PERMIT ERROR
TP3
TP1
K813 129 W3
K812 129 W3
VELOCITY ERROR
K811 126 X4
K810 126 X4
VELOCITY RESYNC
K819 126 Z3
K818 126 Z3
SIGNAL MONITOR
J823 129 Z4
J824 129 Z4
C13 27 25M.S.
K817 129 W4
K816 129 W4
FAULT

J826 129 W2 → CR4 → R7 150 → WRITE PERMIT ERROR LITE → 8 S/DS8-1 009B
J825 129 W3 → CR3 → R6 150 → VELOCITY ERROR LITE → 12 S/DS6-1 009B
J828 129 W4 → CR6 → R9 150 → SIGNAL MONITOR LITE → 10 DS16-2 009B
J827 129 W4 → CR5 → R8 150 → FAULT LITE → 6 S/DS7-1 009B
J829 129 Y2 → CR7 → R20 150 → DENSITY STATUS 2¹ LITE → 58 DS15-2 009B
J830 129 Y2 → CR8 → R21 150 → DENSITY STATUS 2⁰ LITE → 57 DS14-2 009B

DENSITY STATUS 2¹ → 63 B2-6 005A
DENSITY STATUS 2⁰ → 64 B2-18 005A

R15 56
R16 56
R17 56
R18 56

009C J1-J5 → 60 DENSITY STATUS 2¹(+)
009C J1-J1 → 59 DENSITY STATUS 2¹(-)
009C J1-H5 → 62 DENSITY STATUS 2⁰(+)
009C J1-G8 → 61 DENSITY STATUS 2⁰(-)

REC R800 162 Z2
5 SELA
8 SELB
6 A,B
1 A+ ZA 4
2 A- 12 B+ ZB 9
11 B-

0088

CONTROL DATA CORPORATION — CUSTOMER ENGINEERING DIVISION	LOGIC / SCHEMATIC DIAGRAM IBFF MOTION CONTROL II LOC 85	CODE IDENT 34011	D	DWG NO 59332101	REV A
				SHEET 2	

CONTROL PANEL ASSEMBLY

CR0094

DISPLAY SELECT

A signal ground is input to the DISPLAY SELECT switch S2 on pin 10. When the switch is set to any of the nine positions, a ground is routed to the logic board and pin shown on the output line. Since a ground is actually a logic "0", the signal is the not representation of that which is labeled on the switch i.e., the signal to logic card A4, pin 73, is the $\overline{\text{START}}$ signal. The ground out of S2 causes the appropriate signal to be displayed at the DISPLAY on the operator control panel.

DENSITY REQUEST

When switch S6 (2^0 DENSITY REQUEST) is set to 0, a ground is routed to card A5, pin 15. There is no connection at the 1 position. Switch S7(2^1) is similar to S6.

INT TEST

When switch S8 is set to OFF, a ground is applied to several boards to prohibit the internal test. There is no connection at the ON position.

OPERATION

When switch S9 is set to RECORD, a ground is supplied to logic card B3, pin 59. When set to CONTINUOUS, a ground is supplied to logic cards at A5, pin 59, and at B2, pin 66. There is no connection at the CONT REC position.

MODE

When S10 is set to LOAD, a ground is supplied through pins 2 and 1 of section A to: B4, pin 46; B3, pin 64; and to S/DS 1 (A). When set to STEP, the ground is present through pins 2 and 3 of section A to pins 2 and 1 of section B to B4, pin 28. The RUN position has no connection.

BREAKPOINT

The inputs to S3, S4, and S5 (2^0, 2^1 and 2^2 BREAKPOINT) switches are from the Address 2^0, Address 2^1, and Address 2^2 flip-flops, respectively (CR0014). The set output of the flip-flops goes to pin 3 and the clear output to pins 1. When set to position 0, the set output of the flip-flops goes to AND gate J619 (CR0068); when set to 1 the clear output goes to J619. Switches S3, S4, and S5 serve to supply either the set or clear output of the three flip-flops to the AND gate.

START

The 2.7 megohm resistor and .01 microfared capacitor on section B of switch S16, in conjunction with 560 ohm resistor R9 on logic board B3 (CR0068), form a one-shot circuit and serve to eliminate noise when the pushbutton is pressed. When START is pressed, the .01 microfared capacitor charges up at a relatively fast rate through the small 560 ohm resistor, providing a +5 volt DC output to logic card B3 and B4. When the pushbutton is released, the .01 capacitor discharges through the 2.7 megohm resistor in approximately 27 milliseconds. Another one-shot through the 560 ohm resistor and the .01 microfared capacitor cannot be effected until the capacitor has discharged through the 2.7 megohm resistor. In this way, only one pulse per depression of the pushbutton is assured.

INT CONTROL

Switch S15 has two 27 microfared capacitors mounted on it. Capacitor C2 between pins 3 and 2 eliminates high frequency noise in the ground circuitry when in the LAMP TEST position. When the switch is set to MC, a Master Clear signal is output as long as the switch is held in the MC position. Capacitor C1 between pins 1 and 2, in conjunction with resistor R7 on logic card B3(CR0068), provides a 20 millisecond delay of the Master Clear signal after the switch is released.

TAPE CONTROL

When S14 is set to REWIND or UNLOAD, a ground is supplied to logic card B3 (CR0068). When set to REWIND, resistors R17 and R18 and capacitor C7 on B3 provide a one microsecond one-shot Rewind pulse. When set to UNLOAD, resistors R19 and R20 and capacitor C8 on B3 provide a one microsecond one-shot Unload pulse.

PARITY ERROR RESPONSE

When switch S13 is set to TRAP, a ground is output to logic card A5 (CR0048) to the input of inverter J425. When a Parity Error is present to inverter J427, the Trap flip-flop gets set. The parity error is ultimately displayed on the DISPLAY when the DISPLAY SELECT switch is set to READ.

When switch S13 is set to BACKSPACE, a ground is routed to card A5 (CR0048) to inverter J423. If a Parity Error is present and the exerciser is in the Record mode, the Backspace flip-flop gets set.

There is no connection to the OFF position of switch S13.

PATTERN

When switch S12 is set to TRUE/COMP, a ground is provided to logic card B2, pin 42 (CR0055). Since a ground is considered a logic "0", the signal name on logic diagram CR005A is called True, not True/Complement. There is no connection to the TRUE position of the switch.

CLIPPING LEVEL

When switch S11 is set to LOW or HI, a ground is supplied to logic card A5, pin 65 or 73, respectively (CR0048). There is no connection to the NORMAL position.

The $\overline{\text{0's Data}}$ and $\overline{\text{1's Data}}$, from logic card B2(CR005A), pins 24 and 34 respectively, is input to the eight data switches (S17 through S24) at pins 1 and 3, respectively. When any of the switches is set to 0, $\overline{\text{0's Data}}$ is output on pin 2 of that switch to the Write data transmitters on logic card A2 (CR001B). When any of the switches is set to 1, $\overline{\text{1's Data}}$ is output on pin 2 of that switch to the Write data transmitter.

There is no connection to the E (erase) position of the switches. Whenever a switch is set to E, a steady logic "0" (DC erase) is transmitted to the tape transport from the +5 volts DC and the pull-up resistor on the input to the inverter on the input to the transmitter on logic card A2(CR001B).

On the B section of the eight switches, when the switch is set to position 1, a ground is output on pin 3 to logic card B2(CR005B), Parity Generator P500, for generation of odd parity.

When P switch S25 is set to ON, the "0" or "1" Parity bit from the parity generator on logic card B2(CR005A and CR005B) is routed through the switch to the transmitter on logic card A2(CR001B). When the P switch is set to OFF, a ground is routed to the transmitter on logic board A2(CR001B), providing a constant logic "0" out to the tape transport. This is used to erase the parity track.

When the exerciser is connected to a seven track tape transport, Write data is still transmitted from the exerciser to the tape transport, however it is not used by the tape transport. When the 2^6 and 2^7 Data switches (S23 and S24) are set to 1 when connected to a seven track tape transport, a ground is routed through S23B, pin 3, and S24B, pin 3, to OR-gates J523 and J524 on logic card B2 (CR005B). However the $\overline{\text{7 Track}}$ signal which is a logic "0" when connected to a seven track unit provides a logic "1" out of J523 and J524 to parity generator P500. Since two "1's" (an even number) are input to P500, the output of P500 is not effected.

PAUSE TIME

When R/S1 is set to OFF, an open circuit (logic "0") exists between R/S1 and inverters J735 and J737 on logic card B4(CR0078). The oscillator circuit Q700 (CR0078) is by-passed and there will be no pause time between execution of program instructions. When R/S1 is moved from the OFF position, the ground to B4 is removed and the potentiometer becomes part of the Q700 oscillator circuit on card B5. The frequency determining elements of the oscillator circuit are the R14 potentiometer and C13 capacitor. As the control is rotated, the oscillator frequency varies from 2 milliseconds to 100 milliseconds.

RECORD LENGTH

This circuit is similar to the PAUSE TIME circuit described above. When set to ONE WORD, oscillator circuit Q500 on logic card B2(CR0058) is by-passed. As the control is rotated, the frequency of Q500 is varied from 2 milliseconds to 100 milliseconds.

RUNNING TIME

The timer XM1 is connected to +5 volts DC on logic card A5(CR004A). Any time the exerciser is on, +5 volts DC is available to operate XM1.

SHEET REVISION STATUS						REVISIONS				
			3	2	1	REV.	E.C.O.	DESCRIPTION	DATE	CHK'D	APP'D.
			A	A	A	A		DRAWING RELEASE	1-7-72	GK	
			A	B	B	B	CE00 138	SEE ECO	4-28-72		

003A A4-45 RECORD TAP
003A A4-43 SKEW
003A A4-70 STOP ACT
003A A4-64 STOP APP
003A A4-73 START
002A A3-48 FAULT
002A A3-54 MODEL
002A A3-51 ADDRESS
003B A4-27 READ

DISPLAY SELECT

S6: 2^0 → A5-15 004B; N.C.
S7: 2^1 → A5-16 004B; N.C.

DENSITY REQUEST

A2-38 001A
A3-73 002A
A5-4 004B
B2-41 005B
B3-61 006B
B5-54 008A

S8A: OFF; S/S ON → N.C.; S/S OFF → B4-38 007B
S8B: ON → N.C.

INT TEST

S9: RECORD → B3-59 006B; CONT REC → A5-59 004B; CONTINUOUS → B2-66 005B
LOAD → (A) 009B

OPERATION

S10A: LOAD → B3-64 006B; B4-46 007A
S10B: STEP/LOAD → B4-28 007A; RUN → N.C.

MODE

0068 B3-48 → S3: 2^0 → B3-15 006A; B3-14 006A
0068 B3-43 → S4: 2^1 → B3-27 006A; B3-7 006A
0068 B3-49 → S5: 2^2 → B3-8 006A; B3-9 006A

BREAKPOINT

010A A3J2-H GND
⚠1 +5VDCI
S16A: N.C. → N.C.; N.O.
S16B: N.C. → R1 2.7 MEG; C1 .5US .01; N.O. → B3-66 006B; B4-36 007A; A5-77 004A; B3-3 006A; B4-24 007A; B5-4 008B; (B) 009B

START

C2 27
S15: LAMP TEST; OFF; MC → C3 27 → A4-42 003B; A5-66 004A; B2-78 005B; B3-63 006B; B4-48 007A

INT CONTROL

S14: REWIND → B3-77 006B; OFF; UNLOAD → B3-53 006B

TAPE CONTROL

S13: TRAP → A5-64 004B; OFF; BACKSPACE → A5-48 004B

PARITY ERROR RESPONSE

S12: TRUE/COMP → B2-42 005A; TRUE → N.C.

PATTERN

S11: LOW → A5-65 004B; NORMAL; HI → A5-73 004B

CLIPPING LEVEL

GND J3
XM1 2K HOUR RUNNING TIME → A5-76 004A

DATA

001B A2-4 DATA 2^0 → S17A → B2-24 005A; S17B → B2-34 005A
001B A2-20 DATA 2^1 → S18A → N.C.; S18B → B2-67 005B
001B A2-17 DATA 2^2 → S19A → N.C.; S19B → B2-65 005B
001B A2-3 DATA 2^3 → S20A → N.C.; S20B → B2-62 005B
001B A2-19 DATA 2^4 → S21A → N.C.; S21B → B2-64 005B
001B A2-24 DATA 2^5 → S22A → N.C.; S22B → B2-47 005B
001B A2-25 DATA 2^6 → S23A → N.C.; S23B → B2-60 005B
001B A2-2 DATA 2^7 → S24A → N.C.; S24B → B2-72 005B
001B A2-22 P → S25: OFF; ON → B2-73 005B; B2-38 005A

⚠1 +5VDCI
R/S1
PAUSE TIME
007B B4-5 → 250K
OFF
INCREASE → B4-26 007B
PAUSE TIME
RECORD LENGTH
005A B2-70 → 250K
ONE WORD
INCREASE → B2-58 005B
R/S2
RECORD LENGTH

NOTES:
⚠1 COMMON +5VDCI.

* S8 & S10 PIN CONNECTIONS

S8	S10	SECTION A	SECTION B
OFF	LOAD	1-2	1-2
S/S	STEP	2-3	1-2
ON	RUN	2-3	2-3

REFERENCE DRAWING	DRAFTSMAN	DATE
ASSEMBLY 59333400	J. REYES	11/4/71
	CHECKED	1-6-72
	ENGINEER G. Reed	1/6/72
	APPROVAL DEM DLC	1/4/72
	G. Reed	1/7/72

COMPONENTS EXCEPT AS NOTED

	TOL	VALUE	SIZE
RES.	5%	OHMS	1/4W
CAP.		UF	

CONTROL DATA — CUSTOMER ENGINEERING DIVISION

SCHEMATIC DIAGRAM: CONTROL PANEL ASSEMBLY

PRODUCT TR13-A01 | SIZE D | DRAWING NUMBER 86817600 | REV. B | SHEET 1 OF 3 | PAGE

CODE IDENT 34011

CR009B

INSTRUCTION

The four INSTRUCTION indicators (S/DS1 through S/DS4) light when the appropriate instruction from memory M600 on logic card B3(CR006A), through multiplexer D600 and through inverters J611 through J614, is routed to the indicator. The indicators also light when the pushbutton is pressed. When the MODE switch S10 (CR009A) is set to LOAD, a ground (A) is present on pin 2 of the instruction pushbutton. The ground is routed through the pushbutton to load the instruction in M600 memory. The instruction is read out of memory, at the same time that the memory is loaded, and then returns to the INSTRUCTION indicator to light it. The indicators also light when the Lamp Test signal is received through diodes CR9 through CR12 on logic board B3.

ADDRESS

The three ADDRESS indicators (DS4, DS5, and DS6) light to indicate the status of the program address counter, which is composed of flip-flops K603, K605, and K607 on logic card B3(CR006A). The set output of the flip-flops is inverted by J615, J616, and J617 and provides a logic "0" to the indicators to light them. The indicators are also lit by the Lamp Test signal through diodes CR13, CR14, and CR15 on logic card B3.

ERROR

The four ERROR indicators (S/DS5 through S/DS8) light whenever the appropriate Error signal from logic card B5(CR008B) or A5(CR004A) is received. They also light whenever the Lamp Test signal is received from the same cards. The indicator goes out when the pushbutton is pressed, supplying a ground to logic card B5 or A5 which clears the flip-flop that provided the signal to light the indicator.

DENSITY STATUS

The two DENSITY STATUS indicators (DS14 and DS15) light when the appropriate Density Status signal from the tape transport is received at receiver R800 on logic card B5(CR008B) and is routed through inverters on B5 to the indicators. They also light when the Lamp Test signal is received through diodes CR7 and CR8 on B5.

STATUS

The seven STATUS indicators (DS7 through DS13) light whenever the appropriate status signal from the tape transport, which is received on logic board B4(CR007B) or B3(CR006B), is routed through inverters on B4(CR007A) or B3(CR006A) to the indicator. The Lamp Test signal, through diodes CR2 through CR7 on B4 and CR16 on B3, also lights the indicators.

DISPLAY

Whenever INT CONTROL switch S15(CR009A) is set to LAMP TEST, a ground is routed through pin 3 to pin E of DS1, DS2, and DS3. The ground in on pin E with +5 volts DC in on pin 7 lights the digit eight on each LED array. The data input to the three displays is from the multiplexers on logic card A3(CR002B). The data that is displayed is determined by the setting of the DISPLAY SELECT switch. The ground on pin 3 of each display prohibits the digit nine from lighting since the display is used only as an octal read out.

SIGNAL MONITOR

The data in on pins 1 through 24 of S26 is routed through pin 25 to the SIGNAL MONITOR test point J4 and to logic card B5(CR008B) and A4(CR003A). On logic card B5 the signal is extended by 25 milliseconds. Capacitor C13 delays the clearing of the Signal Monitor flip-flop for that period of time. The delayed signal is then routed to the SIGNAL MONITOR indicator DS16.

The data is also routed from S26 to the Skew II flip-flop on logic card A4(CR003A). In this way, the Read data bit selected by position 1 through 9 of S26 sets the flip-flop. The skew measurement, which is the time from the receipt of the first data bit to the data bit selected by the SIGNAL MONITOR switch positions 1 through 9, is thus effected.

GND

The ground jack J3 is signal, not AC power ground.

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		INITIAL RELEASE	JPR	1-7-76		
B	CE00138	SEE ECO	JPR	3-3-76		

INSTRUCTION

009A (A) LOAD → REWIND B3-56 006A

006A B3-18 REWIND

S/DS1 — REWIND

S/DS2 — WRITE B3-60 006A

006A B3-16 WRITE

S/DS3 — REVERSE B3-54 006A

006A B3-11 REVERSE

S/DS4 — FORWARD B3-52 006A

006A B3-6 FORWARD

FORWARD

ADDRESS

006A B3-4 ADDRESS 2^0 — DS4 — 2^0

006A B3-21 ADDRESS 2^1 — DS5 — 2^1

006A B3-23 ADDRESS 2^2 — DS6 — 2^2

ERROR

A3J2-H GND

S/DS5 — PARITY A5-62 004A

004A A5-75 PARITY

PARITY

S/DS6 — VELOCITY B5-32 008B

008B B5-12 VELOCITY

VELOCITY

S/DS7 — FAULT B5-28 008B

008B B5-6 FAULT

FAULT

S/DS8 — WRITE PERMIT B5-42 008B

008B B5-8 WRITE PERMIT

WRITE PERMIT

DENSITY STATUS

008B B5-57 DENSITY STATUS 2^0 — DS14 — 2^0

008B B5-58 DENSITY STATUS 2^1 — DS15 — 2^1

008B B5-10 SIGNAL MONITOR — DS16

SIGNAL MONITOR

STATUS

A3J2-B +5VDC

006A B3-10 WRITE REPLY — DS7

WRITE REPLY

007A B4-21 REVERSE — DS8

REV

007A B4-19 FORWARD — DS9

FWD

007A B4-14 E.O.T. — DS10

EOT

007A B4-12 B.O.T. — DS11

BOT

007A B4-4 BUSY — DS12

BUSY

007A B4-9 READY — DS13

READY

J4

003A A4-63

008B B5-76

SIGNAL MONITOR

A3J2-E +5VDC

009A (B) LAMP TEST

002B A3-44 D 2^2

002B A3-57 D 2^1

002B A3-58 D 2^0

DS1

002B A3-22 D 2^5

002B A3-21 D 2^4

002B A3-59 D 2^3

DS2

J3

A3J2-C GND

002B A3-77 D 2^8

002B A3-75 D 2^7

002B A3-61 D 2^6

DS3

DISPLAY

008A B5-65 VELOCITY

006B B3-74 WRITE ENABLE

004A A5-36 PARITY ERROR PULSE

001A A2-35 READ PARITY

001A A2-79 READ 2^7

001A A2-77 READ 2^6

001A A2-55 READ 2^5

001A A2-58 READ 2^4

001A A2-44 READ 2^3

001A A2-43 READ 2^2

001A A2-49 READ 2^1

001A A2-57 READ 2^0

S26

005A B2-45 WRITE DATA

006B B3-76 WRITE TERMINATE

007A B4-30 30

007B B4-45 LAST MOTION REV

007B B4-71 TIME 1

007A B4-20 REVERSE I/O

007A B4-16 FORWARD I/O

004B A5-63 E.O.B.

007A B4-57 BUSY

001A A2-76 TACH II

001A A2-75 TACH I

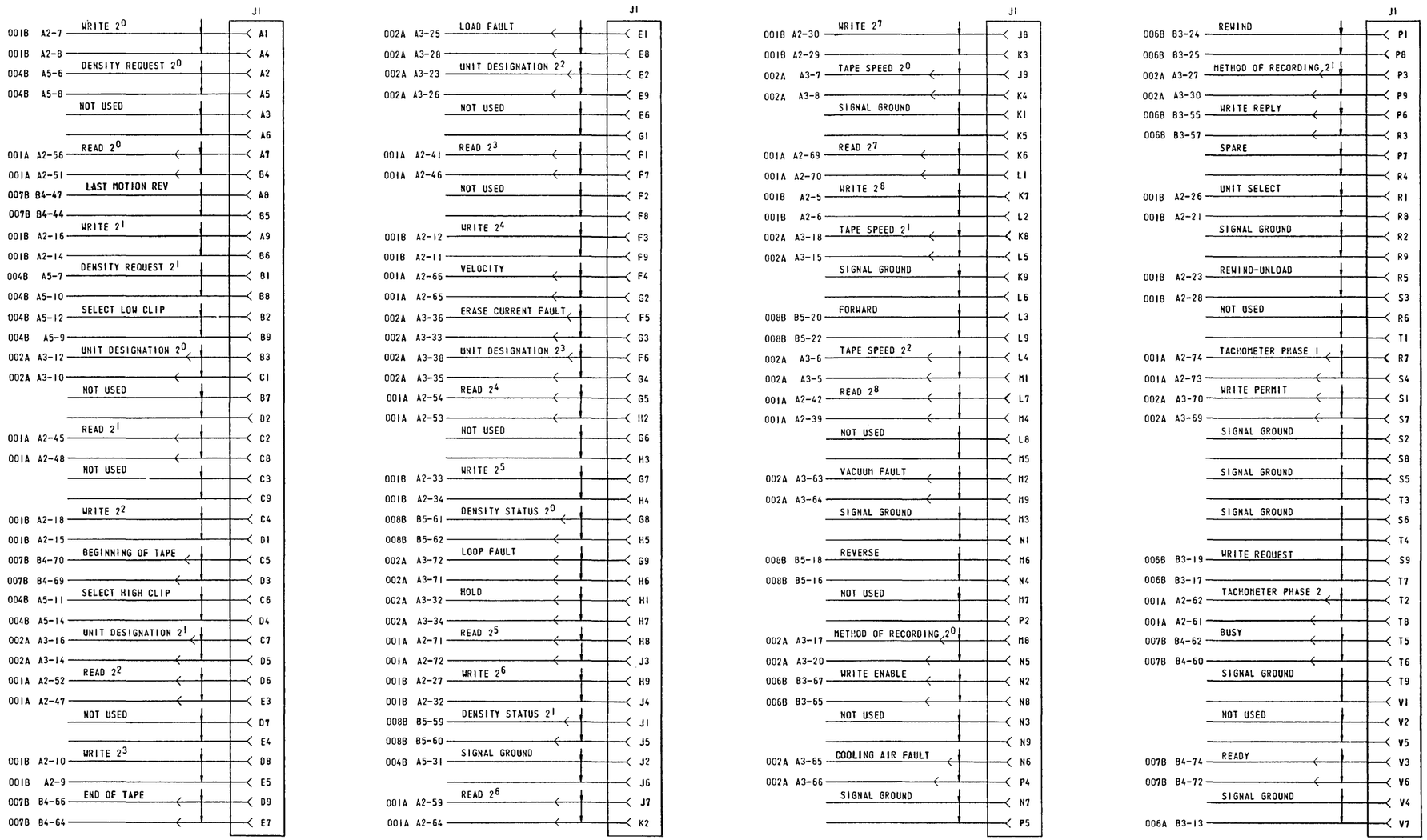
006A B5-56 WRITE PERMIT

SIGNAL MONITOR

009B

CONTROL DATA CUSTOMER ENGINEERING DIVISION	SCHEMATIC DIAGRAM, CONTROL PANEL ASSEMBLY	CODE IDENT 34011	D	DWG NO 86817600	REV B
				SHEET 2	

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A		INITIAL RELEASE	JPR	4-72		JLC



009C

CONTROL DATA CORPORATION, CUSTOMER ENGINEERING DIVISION	SCHEMATIC DIAGRAM, CONTROL PANEL ASSEMBLY	CODE IDENT 34011	D	DWG NO 86817600	REV A
				SHEET 3	

POWER DISTRIBUTION SCHEMATIC

CR 010A

Connector J2, which is mounted on the operator control panel, is a combination male, three pin, recessed, AC power jack and a radio frequency interference (RFI) filter. The AC power cable is connected between J2 and either 120 or 220 volts AC. The connector is grounded to the exerciser by the screws which hold the connector to the operator panel. The ground wire is also connected to pin 5 on terminal board TB1, which is mounted on the baffle plate assembly. The hot line from J2 goes through a one-ampere SLO-BLO fuse to pin 2 of deck A on the AC POWER switch, S1. The neutral line goes from J2 to pin 2 of deck B on S1. When the AC POWER switch is set to ON, 120 or 220 volts AC is supplied to pins 1 and 4 of TB1. When the exerciser is connected to 120 volts, there should be a jumper between pins 1 and 2 of TB1 and a jumper between pins 3 and 4. When connected to 220 volts, both jumpers should be connected between pins 2 and 3.

The output from TB1 will be 120 volts on each primary winding of transformer T1 regardless of whether the input is 120 or 220 volts. The two fans, B1 and B2, each operate on 120 volts.

The output of two of the secondary windings goes to bridge rectifiers BR1 and BR2. The output of the third winding is not used.

The negative output of BR1 is grounded. The positive output goes through three-ampere fuse F1 to two voltage regulators, VR1 and VR2. Each voltage regulator is capable of delivering approximately 1.5 amperes current. Since approximately three-amperes total current is required, two voltage regulators are needed. Capacitor C1 serves to filter the output of the bridge rectifier. The full-wave rectified output of the bridge rectifier normally goes from a low of zero volts to a high of approximately nine volts. Capacitor C1 changes the output to a low of approximately seven volts to a high of approximately nine volts. Voltage regulators VR1 and VR2 then regulate the seven to nine volt swing to a steady five volt DC output.

The positive output of BR1 goes through three-ampere fuse F1 to the two voltage regulators, VR1 and VR2. Each voltage regulator is capable of delivering approximately 1.5 amperes current output.

Capacitors C3 and C4 on the input to pin 3 of VR1 and VR2 eliminate high frequency noise on the regulator output. Without these capacitors the regulators would tend to oscillate with a resultant oscillation on the output.

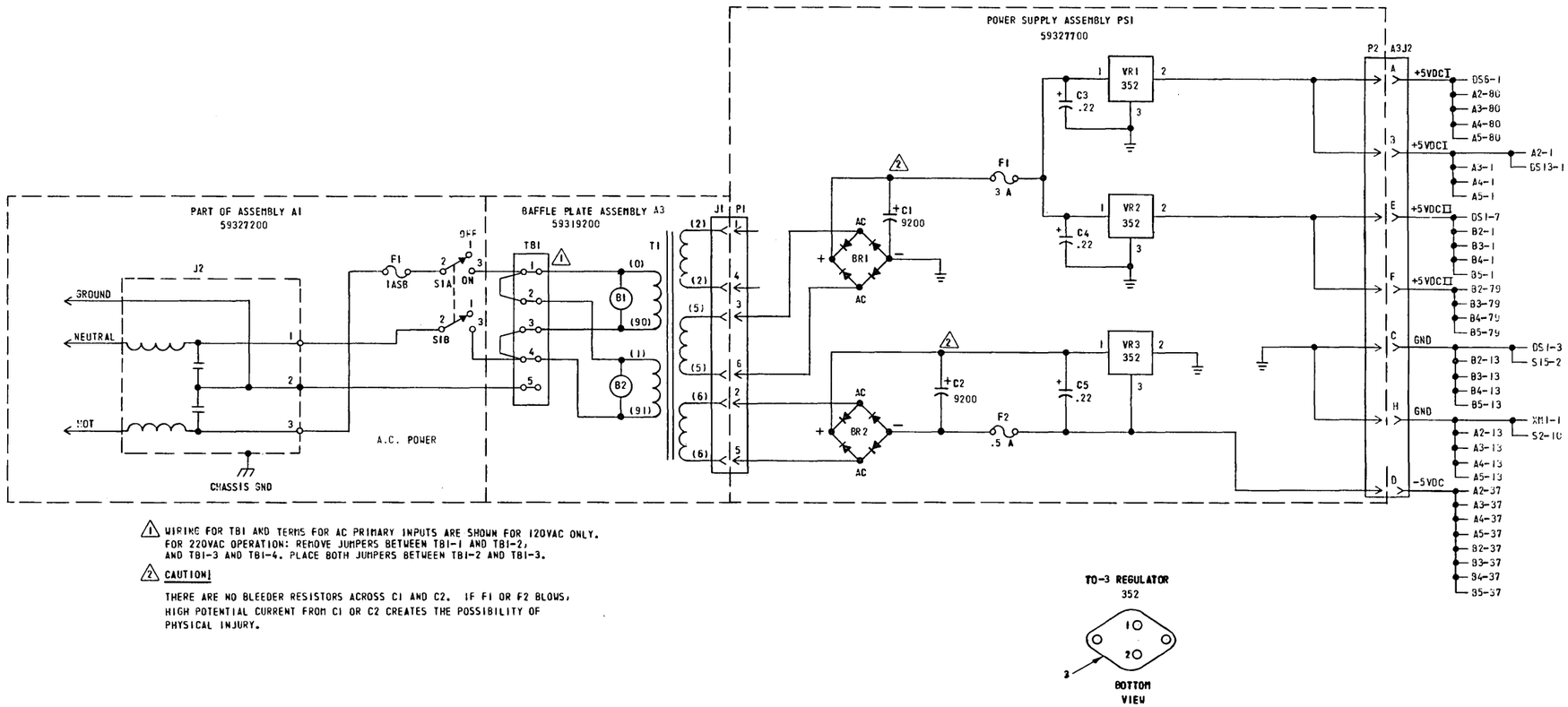
The +5 volts DC from VR1 goes to the logic cards at location A2 through A5 and also to the DISPLAY LEDs on the operator panel. The +5 volts DC from VR2 goes to the logic cards at locations B2 through B5 and also to the remaining LEDs on the operator panel.

To obtain the -5 volts DC, the positive output of BR2 goes to the input of VR3 at pin 1. The negative output of BR2 goes through 0.5 ampere fuse F2 to pin 3 of VR3 and to the power supply -5 volt DC output jack. The normal output on pin 2 is grounded. With the positive output of BR2 to pin 1 of VR3, the input to VR3 is positive with respect to ground. This relationship is necessary for the voltage regulator to operate. The output on pin 3, which is normally grounded is now a regulated -5 volts DC.

Capacitor C2 filters the output of BR2. Capacitor C5 eliminates high frequency noise on the regulator output.

The -5 volts DC goes to all cards that require the -5 volts DC.

REVISIONS					
REV.	E.C.O.	DESCRIPTION	DATE	CHK'D	APP'D
A		DRAWING RELEASE	1-7-72	GK	
B	CE00097	SEE ECO	6MAR73		



⚠1 WIRING FOR TB1 AND TERMS FOR AC PRIMARY INPUTS ARE SHOWN FOR 120VAC ONLY. FOR 220VAC OPERATION: REMOVE JUMPERS BETWEEN TB1-1 AND TB1-2, AND TB1-3 AND TB1-4. PLACE BOTH JUMPERS BETWEEN TB1-2 AND TB1-3.

⚠2 CAUTION!

THERE ARE NO BLEEDER RESISTORS ACROSS C1 AND C2. IF F1 OR F2 BLOWS, HIGH POTENTIAL CURRENT FROM C1 OR C2 CREATES THE POSSIBILITY OF PHYSICAL INJURY.

TO-3 REGULATOR
352

BOTTOM VIEW

REFERENCE DRAWING			

COMPONENTS EXCEPT AS NOTED			
	TOL	VALUE	SIZE
RES.	5%	OHMS	1/4W
CAP.		UF	

	DRAFTSMAN	DATE
	M. Leimann	11-4-71
CHECKER		
ENGINEER		
APPROVAL		11/6/72

CONTROL DATA
CUSTOMER ENGINEERING DIVISION

PRODUCT: T811-A01
PAGE:
SIZE: D

DRAWING NUMBER: 59338500
REV.: B
SHEET 1 OF 1

POWER DISTRIBUTION SCHEMATIC

CODE IDENT 34011

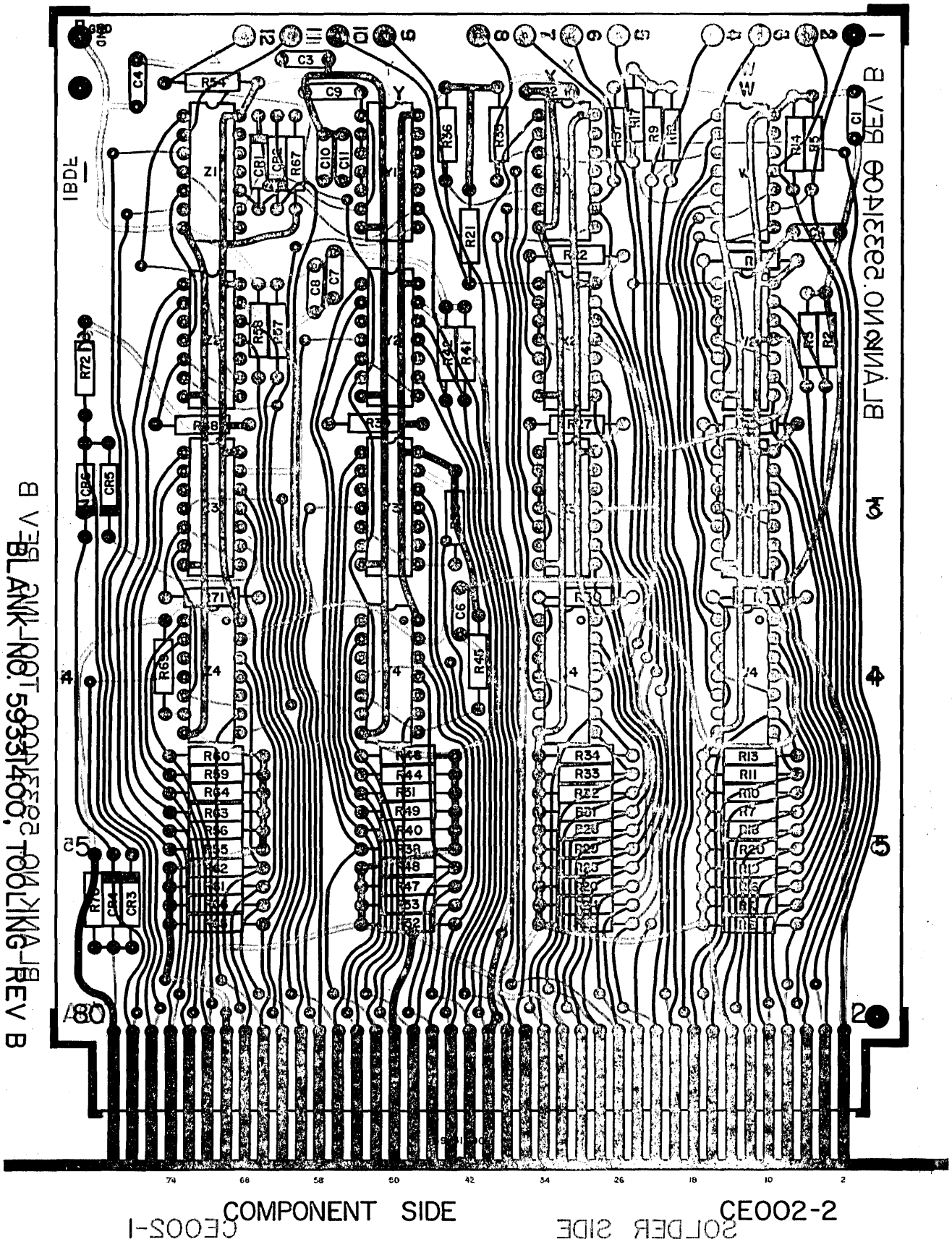


Figure 5-1 Card Composite, 1BDF

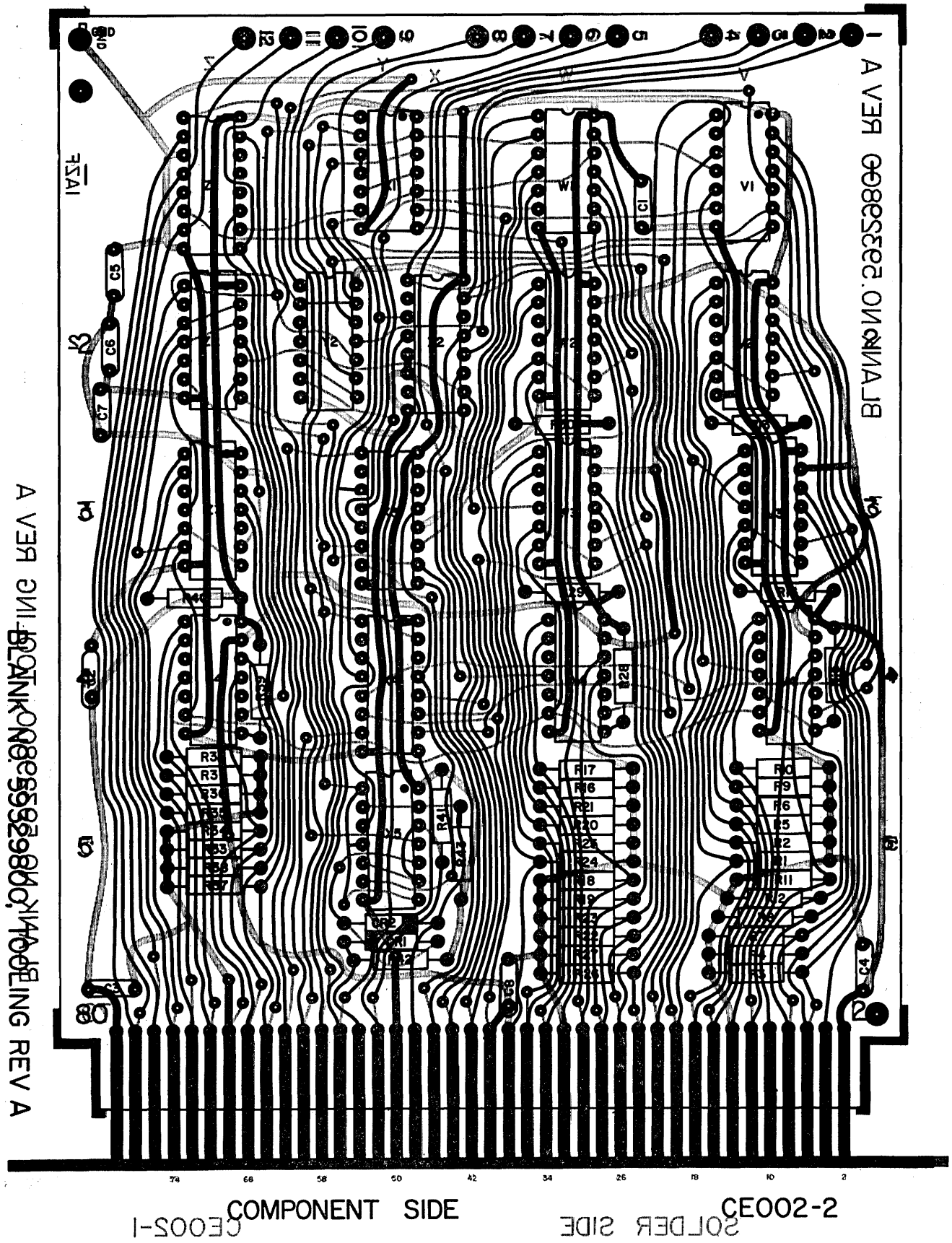


Figure 5-2 Card Composite, 1AZF

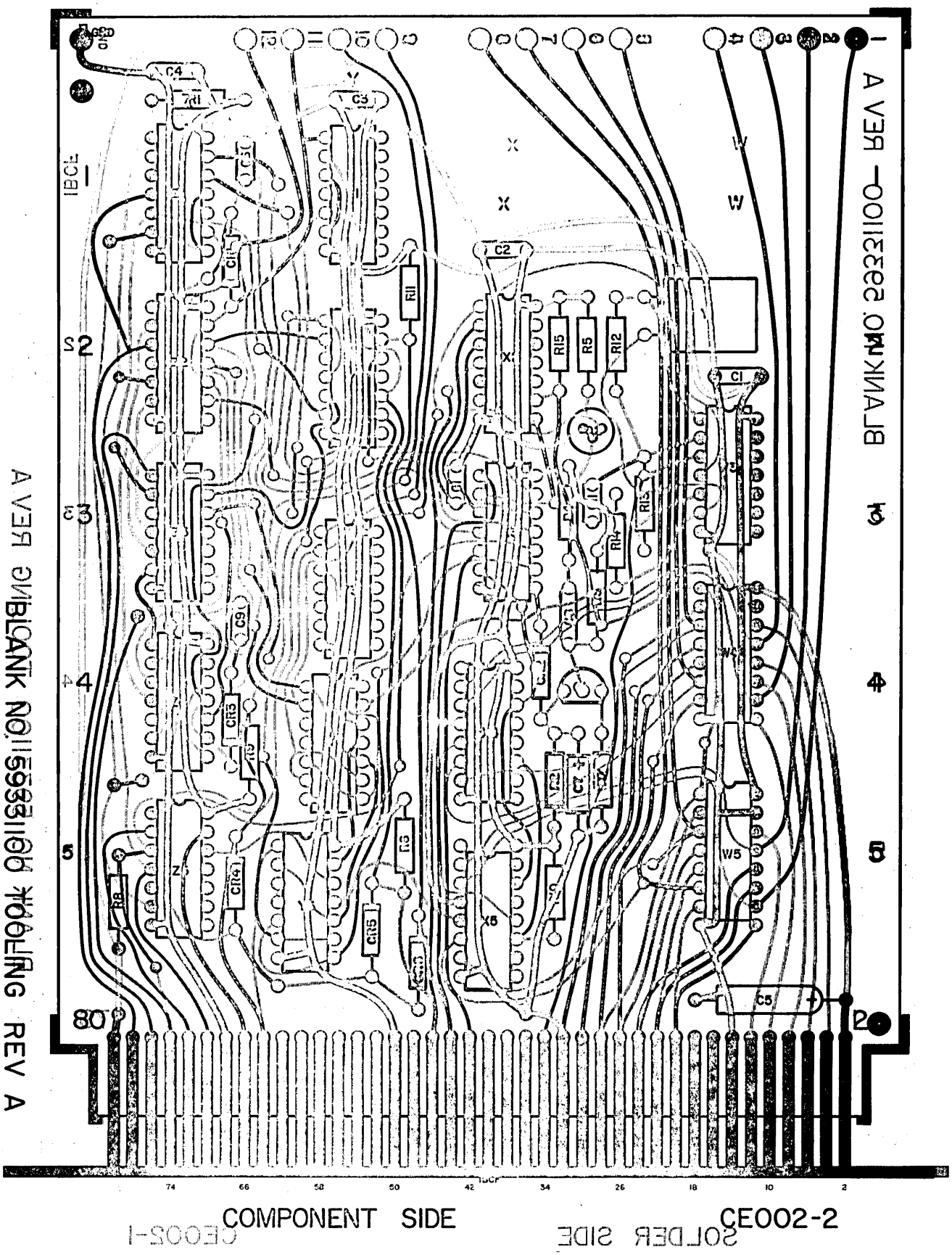


Figure 5-3 Card Composite, 1BCF

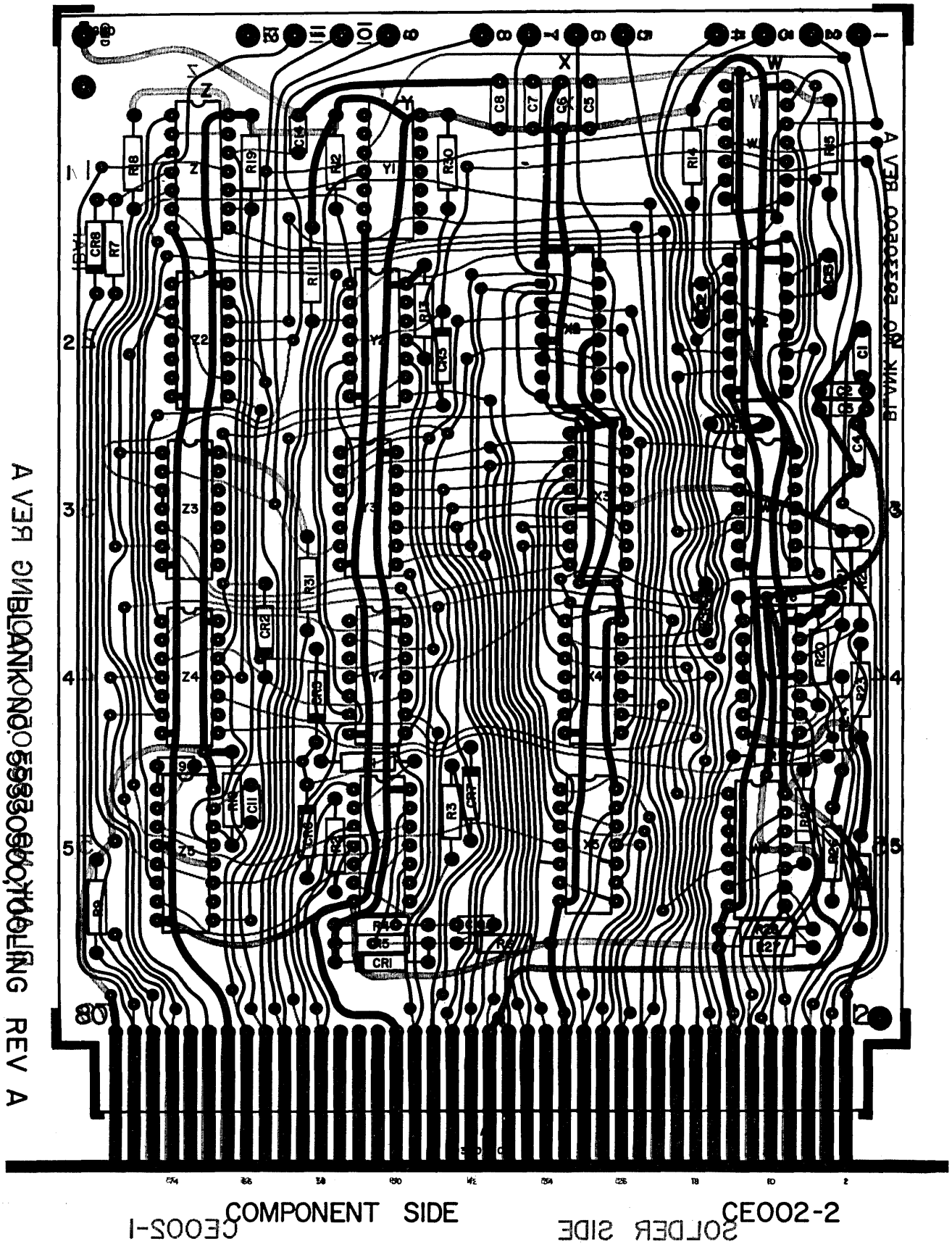


Figure 5-4 Card Composite, 1BAF

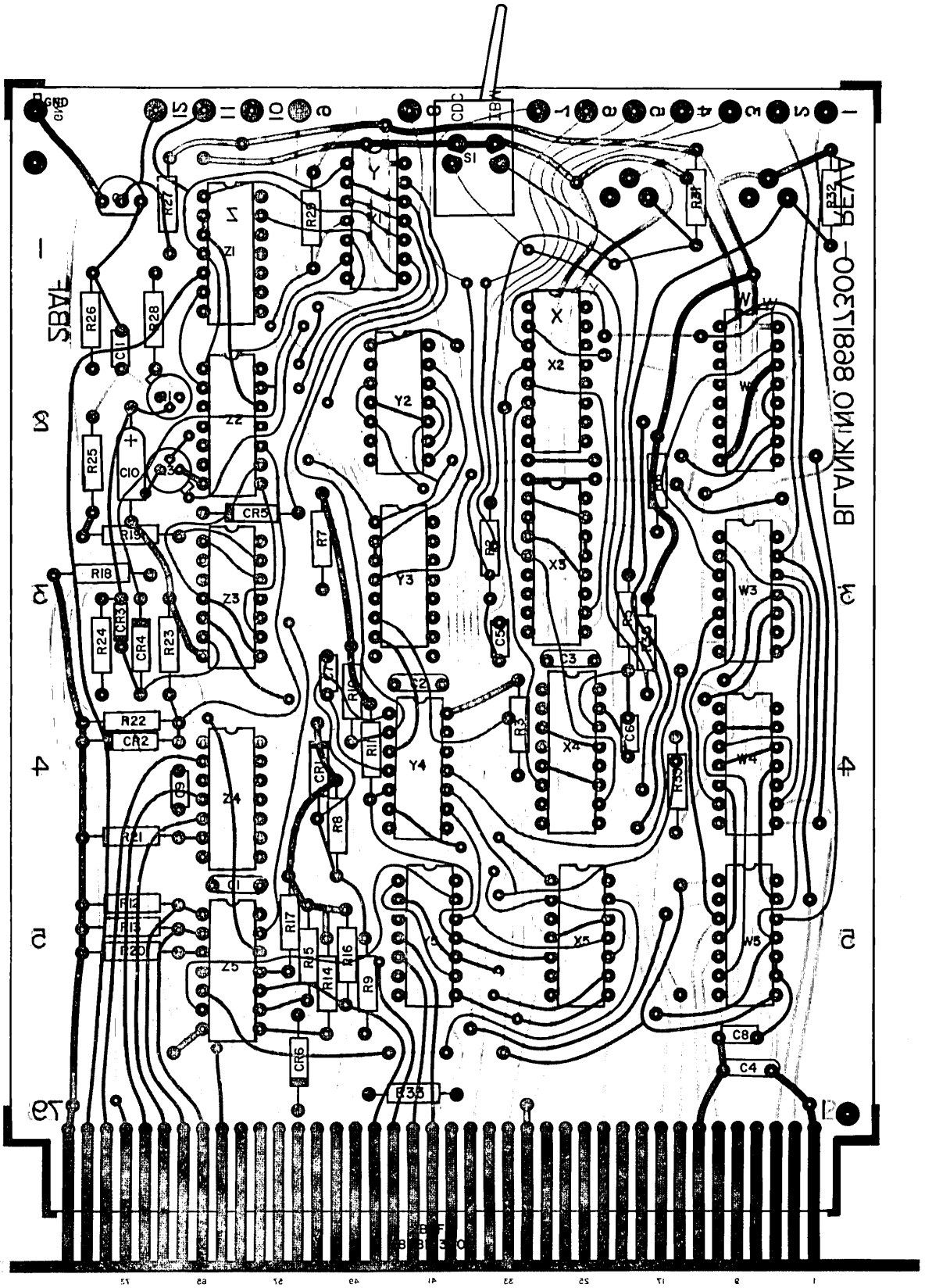


FIGURE 5: Card Composite, 2BAF

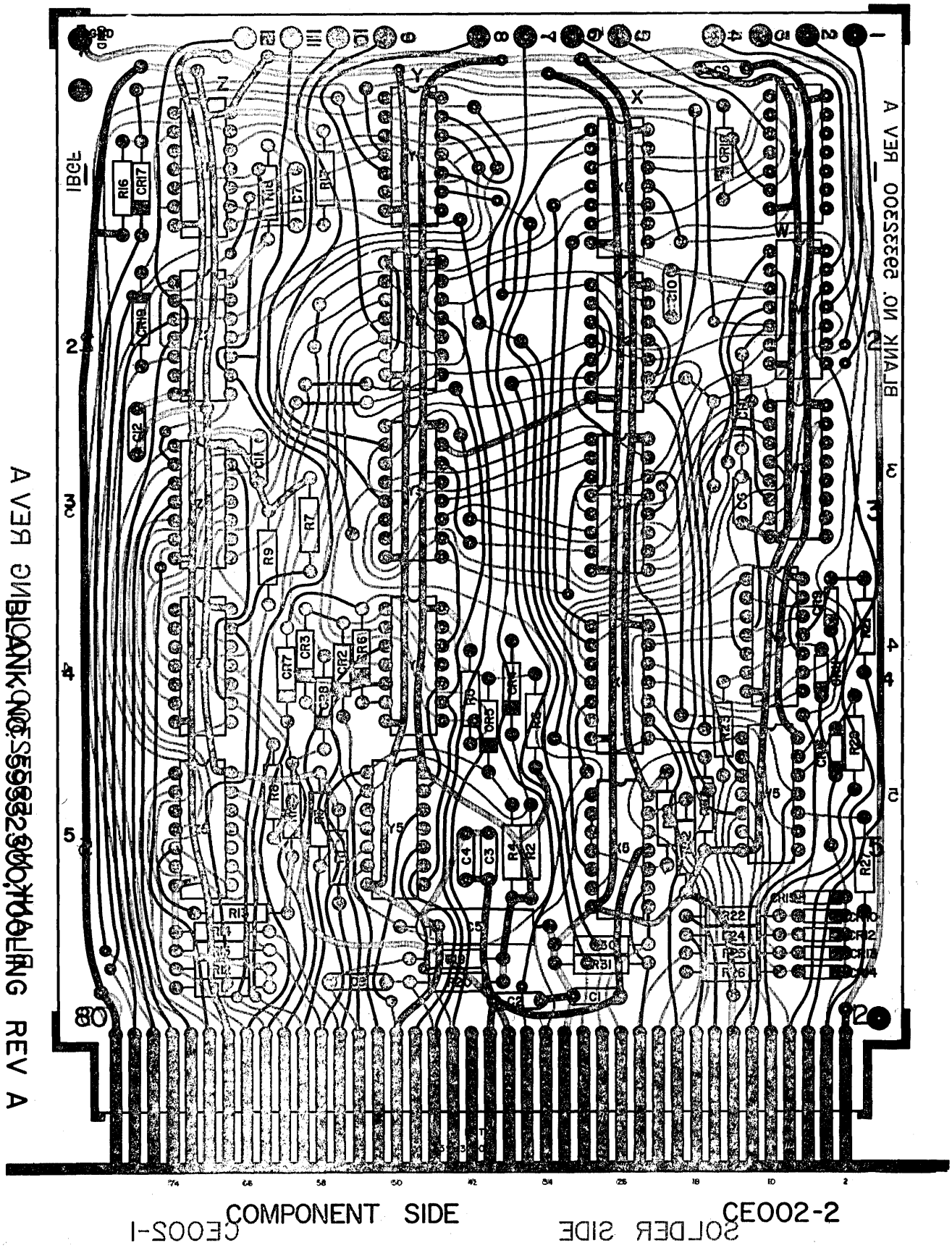


Figure 5-6. Card Composite, 1BGF

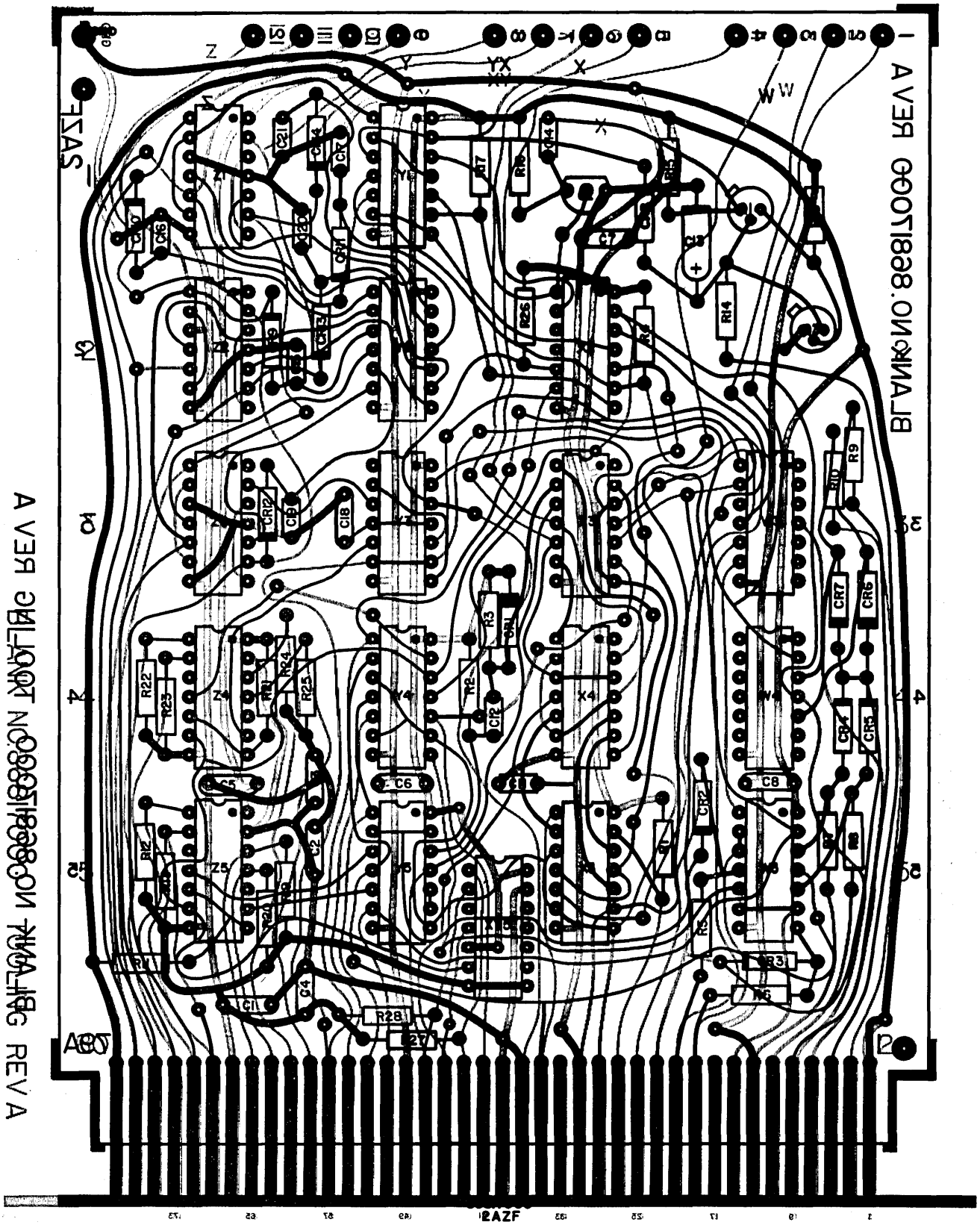


Figure 5-7 Card Composite, 2AZF

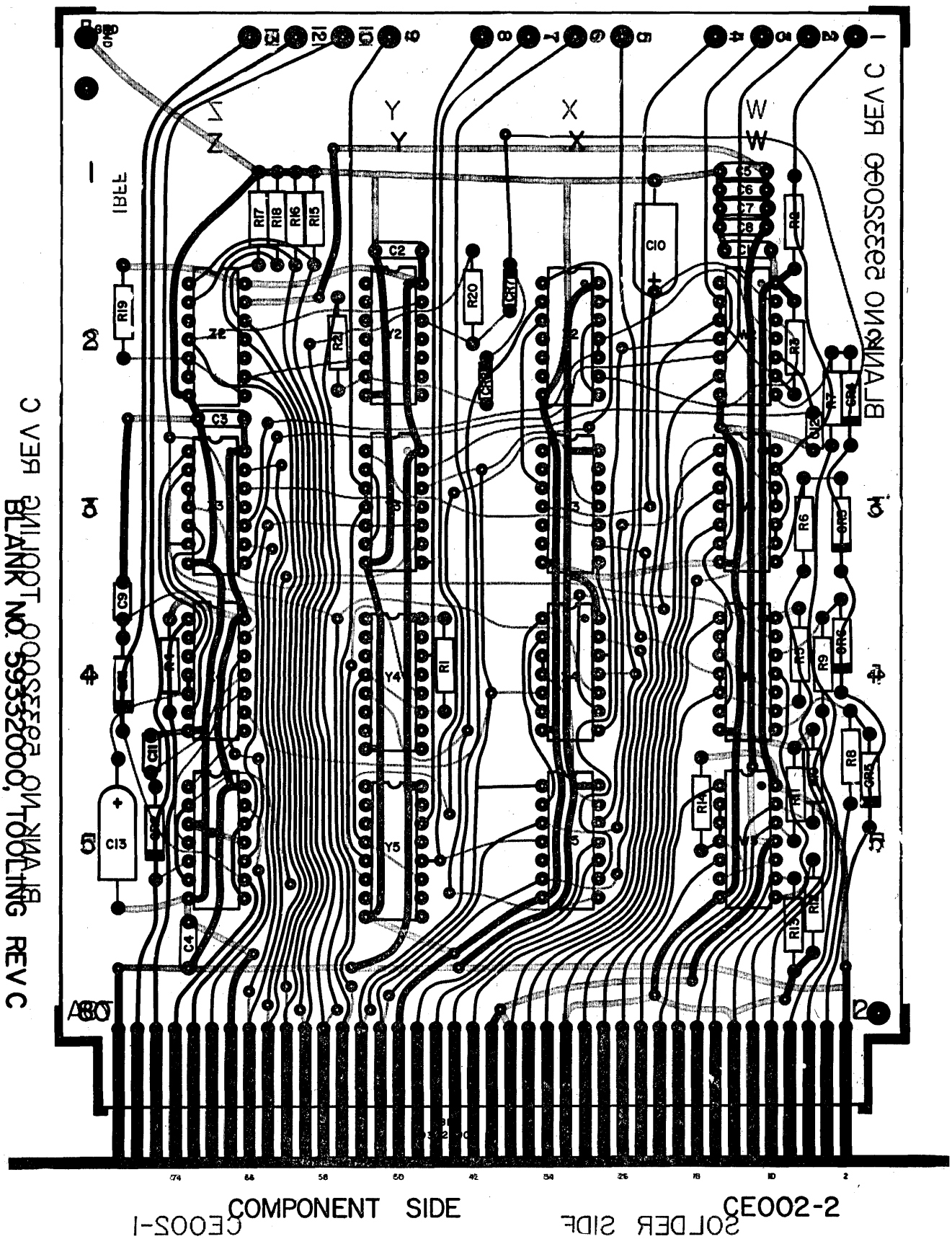


Figure 5-8 Card Composite, 1BFF

Section 6

Maintenance

Section 6

Maintenance

1.0 Introduction

This section contains procedures necessary for maintenance of the exerciser. The recommended serviceability level is limited to replacement of switches, indicators, printed circuit cards, transistors, diodes, capacitors, transformer, and fans. Procedures for removing integrated circuit packages are given but should be used only in emergencies.

2.0 Preventive Maintenance Index

This Preventive Maintenance Index is a chart reflecting preventive maintenance frequency and is cross-referenced to Preventive Maintenance Procedures.

PREVENTIVE MAINTENANCE INDEX

Equipment No. TB 113-A01

Level 1 Bimonthly or ---------- 300 hours
Level 2 Semi-annually or ----------1000 hours
Level 3 Annually or ---------- 2000 hours

Number	Level	Title or Procedure	Time Est. Mins.
1.1	1	515 Nanosecond Clock Check	5
1.2	1	3 Microsecond Clock Check	5
2.1	2	Elapsed Time Indicator Check	2
2.2	2	Power Supply Output	5
2.3	2	Clean	5
3.1	3	General Inspection	5

This PMI lists the recommended frequency of performing preventive maintenance on this equipment. Scheduling of this preventive maintenance is a site responsiblity. Scheduling may include variations in the recommended frequency due to individual site conditions (i.e., usage, environment, time, etc.).

3.0 Preventive Maintenance Procedures

The following procedures should be performed as specified in the Preventive Maintenance Index. Procedures for removal and replacement of parts are referenced in the action step RR-1, RR-2, etc.).

PREVENTIVE MAINTENANCE PROCEDURE

PM-1.1 515 Nanosecond Clock Check

CHECK/conditions	ACTION
1. Loosen 6 knurled spring-loaded captive screws and lift unit out from case.	
2. Connect female end of AC power cable to male recessed AC POWER connector on operator panel.	
CAUTION Insure Exerciser is properly wired for power source used. Refer to Changing Input Power Procedure in this section.	
3. Connect male end of AC power cable to 115 or 220 volt power source.	
4. Set AC POWER switch to on.	
5. Connect oscilloscope Channel A test probe to TP5 on 2BAF card at location B2. Connect probe ground to card ground.	
CHECK: Does the oscilloscope display a 515 nanosecond waveform?	
YES ↓ Check complete.	NO → 1. Troubleshoot and repair the 515 Nanosecond Clock circuitry.

PREVENTIVE MAINTENANCE PROCEDURE

PM-1.2 3 Microsecond Clock Check

CHECK/conditions	ACTION
1. Loosen six knurled spring-loaded captive screws on operator panel and lift unit out from case.	
2. Connect female end of AC power cable to male recessed AC POWER connector on operator panel.	
CAUTION Insure Exerciser is properly wired for power source used. Refer to Changing Input Power Procedure in this section.	
3. Connect male end of AC power cable to 115 or 220 volt power source.	
4. Set AC POWER switch to ON.	
5. Connect oscilloscope Channel A test probe to TP3 on 2BAF card at location B2. Connect probe ground to card ground.	
CHECK: Does the oscilloscope display a 3 microsecond waveform?	
YES ↓ Check complete.	NO → 1. Troubleshoot and repair 3 microsecond clock circuitry.

PREVENTIVE MAINTENANCE PROCEDURE

PM-2.1 Elapsed Time Indicator Check

CHECK/conditions	ACTION
1. Removed from operator control panel. CHECK: Does timer show fewer than 1900 hours?	
YES ↓ Reinstall indicator	
NO ——→	1. Order new timer, part number 58045205. Install new timer when 2000 hours has elapsed on old one.

PREVENTIVE MAINTENANCE PROCEDURE

PM-2.2 Power Supply Output

CHECK/conditions	ACTION
1. Loosen six knurled spring-loaded captive screws on operator panel and lift unit out from case.	
2. Connect female end of AC power cable to male recessed AC POWER connector on operator panel.	
CAUTION Insure exerciser is properly wired for power source used. Refer to Changing Input Power procedure in this section.	
3. Connect male end of AC power cable to 120 or 220 volt power source.	
4. Set the INT TEST switch to ON.	
5. Install the internal test plug connector on the I/O connector.	
6. Set AC POWER switch to ON.	
7. Connect oscilloscope Channel A probe to pin 1 on card at location A5. Refer to card location diagram on the bottom of the logic card rack for the location of pin 1. Connect ground to card ground.	

CHECK: Does oscilloscope indicate +5 (±0.25) volts DC with less than 50 millivolts peak-to-peak ripple?

YES

NO → 1. Repair or replace power supply (RR-1).

8. Connect oscilloscope Channel A probe to pin 1 on card at location B5. Connect ground to card ground.

CHECK: Does oscilloscope indicate +5 (±0.25) volts DC with less than 50 millivolts peak-to-peak ripple?

YES

NO → 1. Repair or replace power supply (RR-1).

9. Connect oscilloscope probe to pin 40 on bottom of the card connector at location B5. Refer to card location diagram on the bottom of the logic card rack for the location of pin 40. Connect oscilloscope ground to GND test point on operator panel.

CHECK: Does oscilloscope indicate -5 volts DC with less than 50 millivolts peak-to-peak ripple?

YES

NO → 1. Repair or replace power supply (RR-1).

Check complete

PREVENTIVE MAINTENANCE PROCEDURE

PM-2.3 Clean

CHECK/conditions	ACTIONS
1. Insure exerciser power is off.	
2. Loosen six knurled spring-loaded captive screws on operator control panel and remove unit from case.	
	1. Using a dry cloth or kimwipe, clean dust and other residue from bottom of case.
	2. Blow dust and other residue from card rack and other exerciser components.
	3. Replace unit in case and tighten six captive screws.

PREVENTIVE MAINTENANCE PROCEDURE

PM-3.1 General Inspection

CHECK/conditions	ACTION
1. Insure exerciser power is off.	
2. Loosen six knurled spring-loaded captive screws on operator control panel and remove unit from case.	
	1. Inspect entire unit for loose or broken components.
	2. Inspect all wiring for evidence of fraying.

4.0 Removal and Replacement Procedures

The following procedures describe removal and replacement of major exerciser Components.

NUMBER	PROCEDURE
RR-1	Power Supply
RR-2	Baffle Plate
RR-3	Fan
RR-4	Transformer
RR-5	Printed Circuit Cards
RR-6	Integrated Circuits
RR-7	Broken Card Rack Wires

REMOVAL/REPLACEMENT PROCEDURE

RR-1 Power Supply

Removal

1. Remove the round connector plug (see Figure 6-1) from the baffle plate.
2. Remove the four power supply mounting screws from the front side of the panel (see Figure 6-2).
3. Move the power supply to one side.
4. Disconnect the square connector from the baffle plate.

Replacement

1. Perform removal procedure in reverse order.

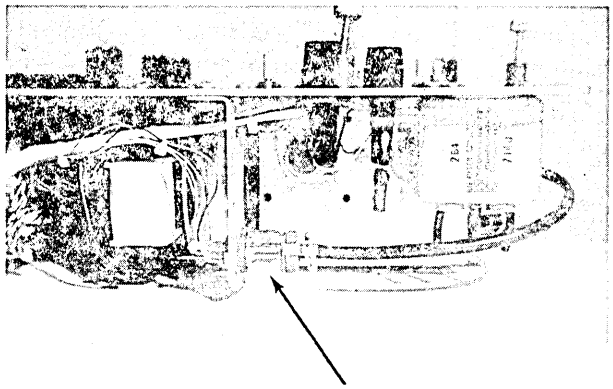


Figure 6-1. Plug P2 on Baffle Plate

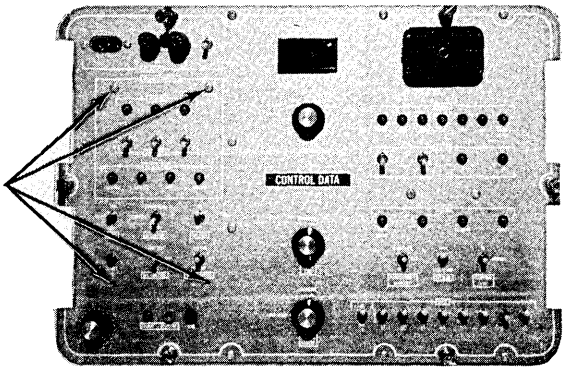


Figure 6-2. Power Supply Mounting Screws

REMOVAL/REPLACEMENT PROCEDURE

RR-2 Baffle Plate

Removal

1. Unsolder the wires from the round connector jack on the baffle plate (see Figure 6-1).
2. Disconnect terminal board leads.
3. Remove the four baffle plate mounting screws (see Figure 6-3).

Replacement

1. Perform removal procedure in reverse order.

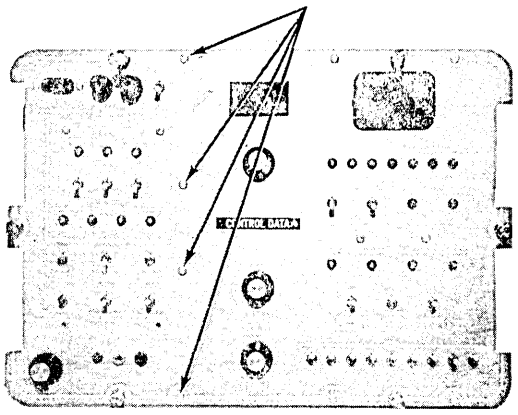


Figure 6-3. Baffle Plate Mounting Screws

REMOVAL/REPLACEMENT PROCEDURE

RR-3 Fan

Removal

1. Remove baffle plate assembly in accordance with procedure RR-2.
2. Unsolder and disconnect fan wires.
3. Remove four screws and nuts holding fan to baffle plate. Observe direction screws go through baffle plate to insure they are installed in the same direction in the replacement procedure.

Replacement

1. Perform removal procedure in reverse order. Refer to Power Distribution Schematic, 59338500, when connecting wires. The fans are labeled B1 and B2 on the schematic.

REMOVAL/REPLACEMENT PROCEDURE

RR-4 Transformer

Removal

1. Remove baffle plate assembly in accordance with procedure RR-2.
2. Unsolder and disconnect wires from transformer.
3. Remove four screws and nuts holding transformer to baffle plate. Observe direction screws go through baffle plate to insure they are installed in the same direction in the replacement procedure.

Replacement

1. Perform removal procedures in reverse order. Refer to Power Distribution Schematic, 59338500, when connecting wires.

REMOVAL/REPLACEMENT PROCEDURES

RR-5 Printed Circuit Card

Removal

1. Grasp the card to be removed and pull straight out. The connectors hold the board tightly and sometimes require the use of a long nose pliers in removal.

2. A card extender, PN 59314900, may be ordered from Customer Engineering Materials for use in trouble-shooting printed circuit cards.

Replacement

1. Insure logic card to be inserted is oriented with components facing away from front panel as per Figure 6-4.

2. Insert card into connector and push into place. Insure that card is well seated into the connector.

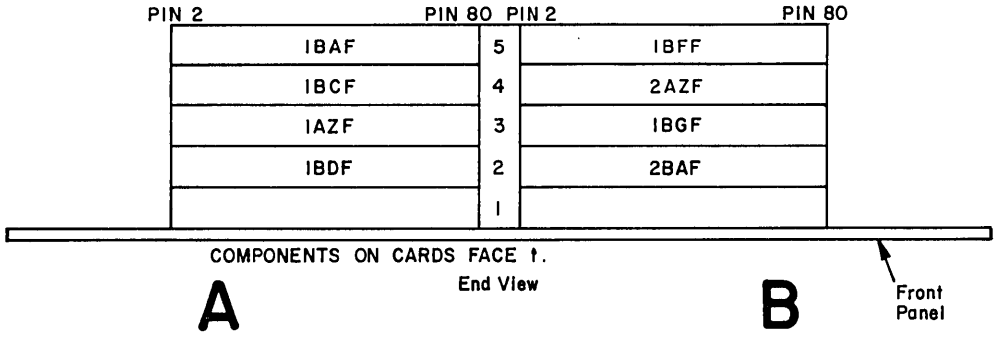


Figure 6-4. Printed Circuit Card Location

REMOVAL/REPLACEMENT PROCEDURE

RR-6 Integrated Circuits

Removal (14 and 16 pin dual in-line packages, Figure 6-5 and 6-6).

1. Cut each pin on the component side of the board.
2. When all pins have been cut, lift the integrated circuit off and throw it away.
3. Apply heat (25 watt iron) to the eyelets on the opposite (foil) side of the board. Heat each eyelet individually with the soldering iron, while pulling on the cut pin from the component side of the board.
4. When all the cut pins have been removed, use either a solder sucker (CDC part number 1221043G) or rapid movement of the soldering iron to open up the eyelets.

Replacement

1. Insert pins through holes in board. Insure that the integrated circuit is installed in the correct position.
2. Turn board over and insure that the integrated circuit is held in position up against the board.
3. Hold soldering iron in contact with one pin, the foil, and the solder until solder melts and flows around pin.
4. When the solder has melted, first remove the solder, then the soldering iron.
5. Continue by soldering all pins.

REMOVAL/REPLACEMENT PROCEDURES

RR-7 Broken Card Rack Wires

Removal

1. If wires are inadvertently broken on the card rack, it is advisable to replace the entire wire since there will not be enough left to provide the proper wrap on the connector. Remove broken wire. Use of long nose pliers may be helpful. The card rack is hinged and may be raised up for ease of maintenance. Remove two screws on end opposite hinge and two screws in center of rack.

Replacement

1. Strip the wire back approximately 1 inch.
2. Insert the wire into the wire wrap tube all the way up to the insulation. The Gardner Denver model 14X142 wire wrap gun with size 24-26 gauge insert is recommended for this work.
3. With the wire threaded in the wire wrap tube, place the insert down over the wire wrap pin.
4. Energize the gun to the point at which the wire is firmly wrapped around the post.
5. In emergencies only, solder the wire to the pin.

5.0 Miscellaneous Maintenance Procedures

5.1 Changing Input Power

NOTE

The terminal board at which input power changes are made is TB1 and is mounted on the baffle plate assembly. It is located near J3 which is the GND jack. Refer to Figure 6-5.

5.1.1 220 Volt Operation (Convert from 120 volt)

1. Disconnect jumper between terminals 1 and 2.
2. Disconnect jumper between terminals 3 and 4.
3. Connect both jumpers between terminals 2 and 3.

5.1.2 120 Volt Operation (Convert from 220 Volt)

1. Disconnect the two jumpers between terminals 2 and 3.
2. Connect one of the jumpers removed in step 1 between terminals 3 and 4.
3. Connect one of the jumpers removed in step 1 between terminals 1 and 2.

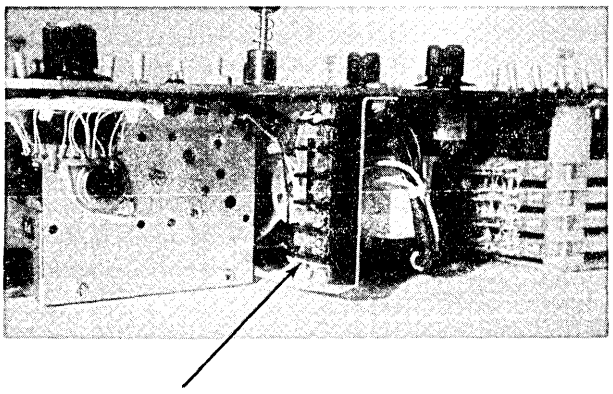


Figure 6-5. Terminal Board TB1 Location

Section 7

Maintenance Aids

Section 7

Maintenance Aids

1.0 Introduction

This section contains information concerning the operation of individual circuit elements which are used in the exerciser.

2.0 Circuit Elements

2.1 Integrated Circuits

2.1.1 General

There are three types of integrated circuit elements used in the exerciser. These are the common industrial Diode-Transistor Logic (DTL), the Transistor-Transistor Logic (TTL), and the DTL/TTL compatible interface circuits. The three types are described in this section and include the following circuits.

INDUSTRIAL DTL

Type 122 Dual 4-input gate
Type 126 Quad 2-input gate
Type 128 Triple 3-input gate
Type 129 Hex 1-input inverter
Type 150 Dual J-K flip-flop
Type 151 Dual J-K flip-flop

TTL

Type 140 Quad 2-input NAND gate
Type 146 Hex 1-input inverter
Type 149 Quad 2-input exclusive-OR gate
Type 170 Dual 4-bit digital multiplexer
Type 189 Quad 2-input multiplexer
Type 195 Dual monostable multivibrator
Type 240 Dual J-K flip-flop
Type 500 Synchronous 4-bit binary up/down counter
Type 502 8-bit odd/even parity generator/checker
Type 514 16-bit register file
Type 515 5-bit shift register

DTL/TTL COMPATIBLE INTERFACE

Type 162 Dual Line Receiver
Type 176 Dual Line Driver

This section also includes a description of a typical DTL inverter, wired-OR and wired-AND gates, an inverter flip-flop, and a wired-OR flip-flop.

2.1.2 Logic Levels

2.1.2.1 Integrated Circuits

Logic levels are as follows:

Industrial DTL Logic "1"	+5.0VDC (nominal)
TTL Logic "1"	+3.3VDC (nominal)
DTL/TTL Compatible Interface Logic "1"	Differential voltage greater than +.025VDC
Industrial DTL Logic "0"	+0.2VDC (nominal)
TTL Logic "0"	+0.2VDC (nominal)
DTL/TTL Compatible Interface Logic "0"	Differential voltage greater than -.025VDC

2.1.3 Common Industrial DTL Circuts

2.1.3.1 Typical DTL Inverter

An integrated circuit common industrial DTL inverter is shown in Figure 7-1. This circuit is the basic building block for the exerciser logic functions. This diagram shows an extender input which most package types do not have. However, since this input merely expands a positive AND gate by allowing more diodes to be added, it is unimportant from a circuit operation viewpoint. Consider the input gate a positive AND gate. This can also be classed as a negative OR gate. Thus, the same inverter package can be assigned an AND or an OR function. The primary difference is in the output polarity which is considered active at any point in time. Assume a logic "0" input to any input pin. This forward-biases the respective input diode and places +0.8VDC on the base of Q1. Q1 cuts off and since it is an emitter-follower, feeds a voltage of less than 0.8VDC to the base of Q2. Q2 cuts off and its collector approaches +5VDC. Thus, any logic "0" input yields a logic "1" output to provide the OR function. Next assume all inputs at logic "1". All input diodes are reverse-biased and the base of Q1 approaches +1.75VDC. Q1 conducts and provides base current for Q2. Q2 conducts and its collector approaches ground. Thus, all logic "1" inputs yield a logic "0" output for the AND function. The maximum voltage which is observable with an

oscilloscope on the extender input pin is approximately +1.75VDC. This voltage is present only when all inputs (including diode-extended inputs) are at logic "1".

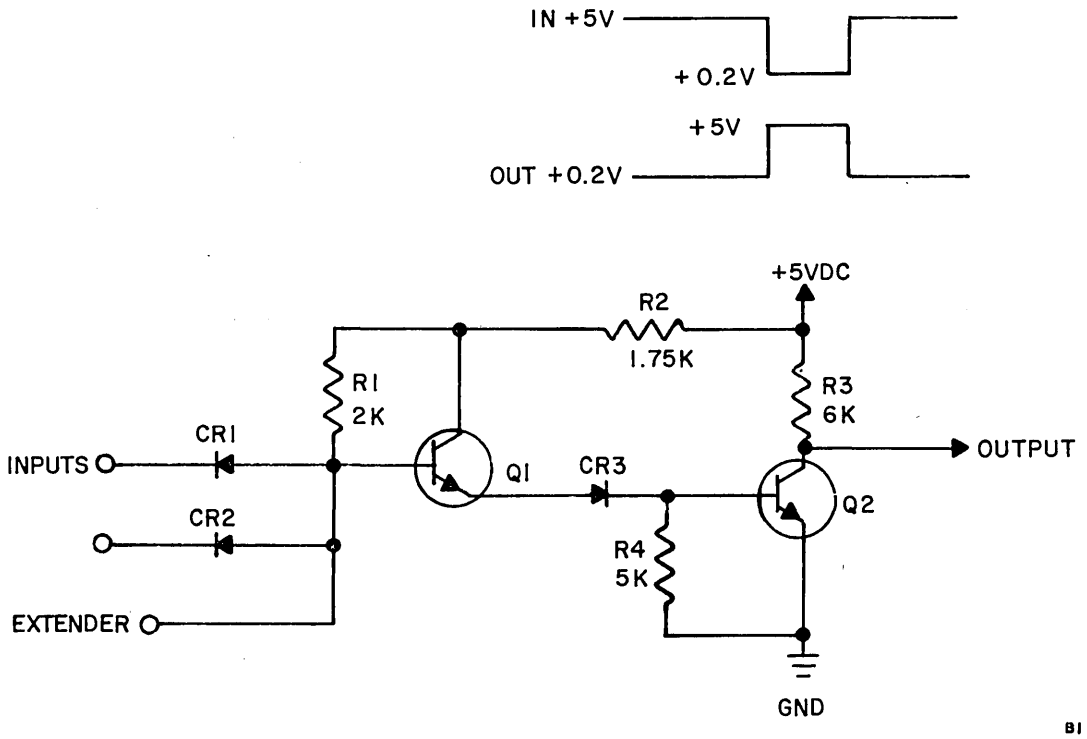


Figure 7-1. Typical DTL Inverter

2.1.3.2 Wired-OR and Wired-AND Gates

The wired-OR and wired-AND functions are identical except that the polarity when the gate is considered active determines the name of the logic function. Since an inverter OR gate is enabled by logic "0" (with DTL elements), wiring the outputs of two or more inverters together as a gate and using the output signal of that gate when at logical "0" makes up the wired-OR function. In Figure 7-2, assume the A, B, and C inputs to be logic "1" and input D at logical "0". The AND gate on the input to JWWW will be made and the AND gate on the input to JXXX will be broken. If the outputs of these two inverters were isolated from each other, JXXX would output logical "0" and JYYY would output logical "1". However, when these outputs are tied together, the logic "0" takes precedence and both outputs go to logic "0". The wired-AND function requires that both JYYY and JZZZ have at least one logic "0" input each. This causes the

wired-AND to go to logic "1", which is the desired active polarity into IYYY.

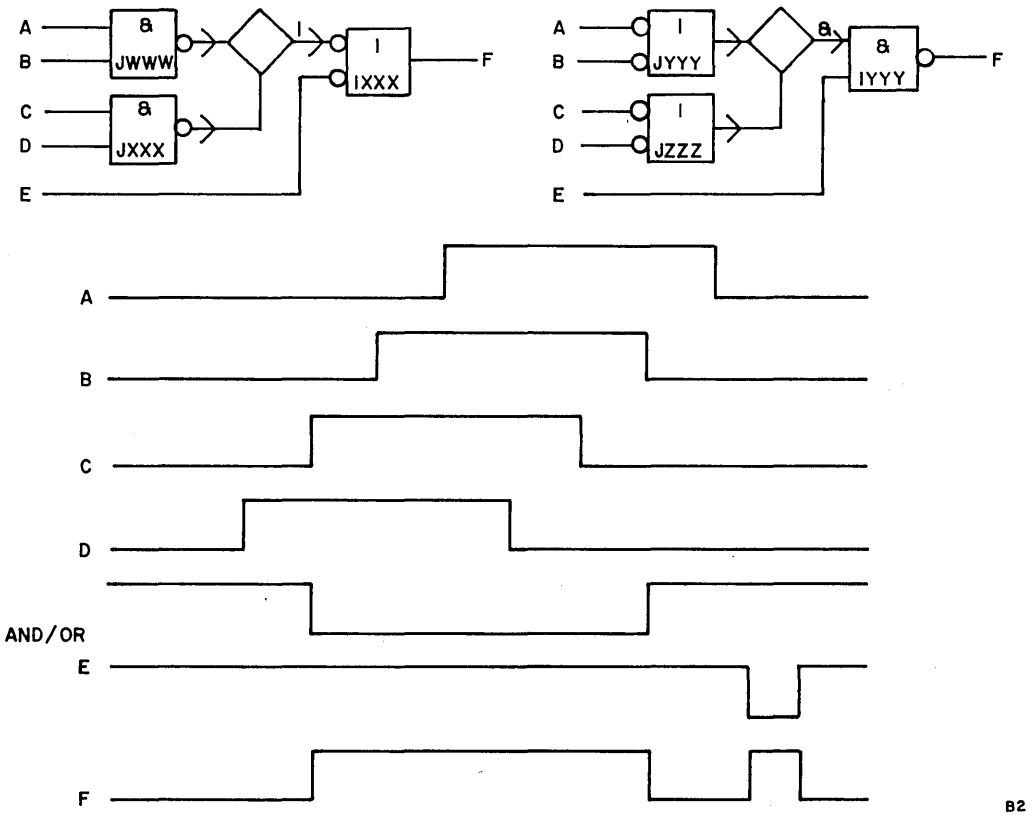


Figure 7-2. Wired-OR and Wired-AND Gates

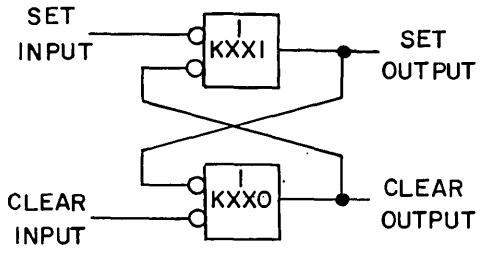
2.1.3.3 Inverter Flip-Flops

2.1.3.3.1 Normal Inverter Flip-Flop

This flip-flop circuit is made up of two normal inverters. Refer to Figure 7-3. The set and clear inputs, when active, are logical "0". The outputs when active, are logical "1". Assume logical "0" in the input to KXX1 and logic "1" on the input to KXX0. Since KXX1 is an OR, the set output goes to logic "1".

The set output may feed some other logic function but also serves as a feedback path for the set state. With both the clear input and the feedback path at logic "1", KXX0 outputs logic "0". This logic "0" is fed back to KXX1 and serves as a latch, holding KXX1 at logic "1" after the set input logic "0" has been removed. The clear of the flip-flop is similar.

With both set and clear inputs at logic "0" simultaneously, both outputs go to logic "1" because of the OR function of each inverter. With both inputs at logic "1", the flip-flop will remain in its previous state.



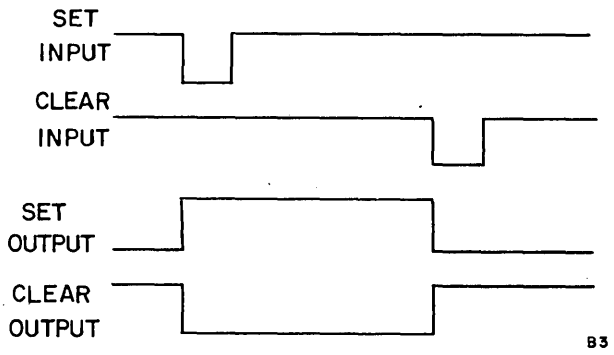


Figure 7-3. Normal Inverter Flip-Flop

2.1.3.3.2 Wired-OR Flip-Flops

This flip-flop circuit is made up of two single input inverters. Refer to Figure 7-4. The set input is combined with the clear output in a wired-OR configuration. The clear input is combined with the set output in a wired-OR configuration. Assume a logic "1" into both inputs A & B. If JXXX were not tied to the wired-OR on the set input of KXX1, its output would be at logic "0" and its duration would be the same as the B input (shown by dotted lines). But because of the set input wired-OR, the pulse output from JXXX will not appear as a duplicate of the B ANDed input. It will appear only as an inversion of the set output.

KXX1 outputs logic "1" on the "1" to "0" transisitions of JXXX output. JYYY is not made on its input and cannot output logic "0". The flip-flop latches with KXX0 logic "0" output because of the wired-OR configuration. The output of KXX0 is as shown in the diagram.

This flip-flop has the advantages of speed and space saving. When the logic "0" output from KXX0 is used to perform some function, there is none of the normal inverter delay. The clear output goes to logic "0" at the same instant as the set input. This arrangement also saves input pins. The normal inverter flip-flop requires at least 4 input pins. Since the number of inputs determines packaging density, fewer packages are necessary for a given number of wired-OR 2-input flip-flops.

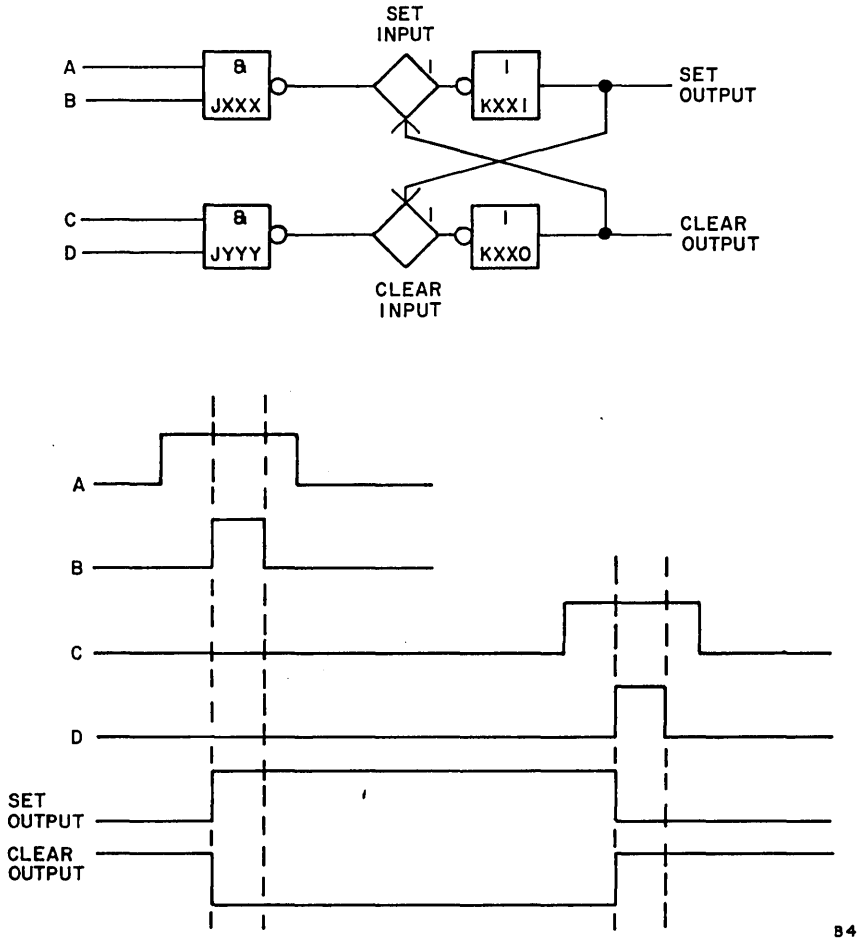


Figure 7-4. Wired-OR Flip-Flop

2.1.3.4 Type 122, Dual 4-Input Gate

The type 122 consists of two expandable 4-input gate circuits. Figures 7-5 and 7-6 show pin assignments and a logic diagram. The gate is shown on logic diagrams with the circles on the output of AND gates and on the input of OR gates. The circle is drawn according to its logic function, however, the same basic inverter circuit is used on both applications. Each gate has an extended input.

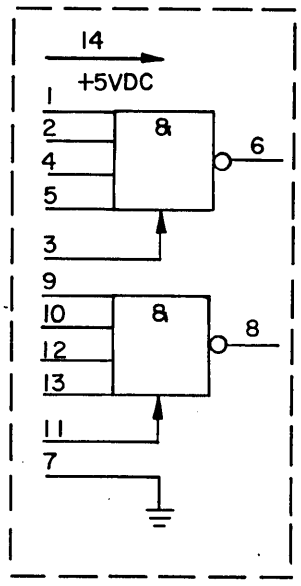


Figure 7-5. Type 122, Pin Assignments

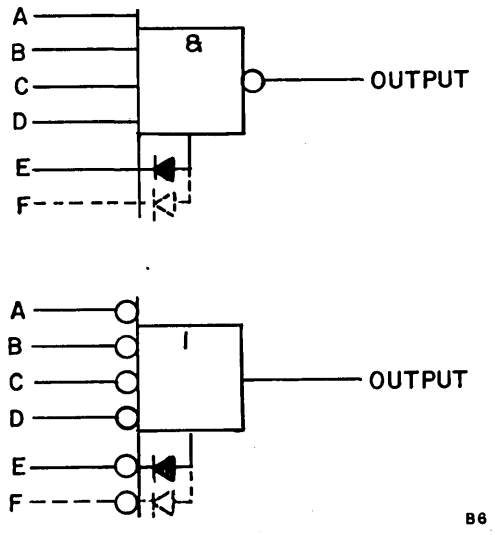


Figure 7-6. Type 122, Logic Diagram

The output of either the AND or the OR gate is high for all input combinations except when all the inputs are high, then the output is low. Refer to Truth Table 7-1.

A	B	C	D	E, etc.	OUTPUT
L	L	L	L	L	H
L	L	L	L	H	H
L	L	L	H	H	H
L	L	H	H	H	H
L	H	H	H	H	H
H	H	H	H	H	L

Table 7-1. Type 122, Truth Table

2.1.3.5 Type 126, Quad 2-Input Gate

Figure 7-7 shows a quad 2-input package. Its function is the same as a 122, except for the number of inputs and the fact that it has no diode extender.

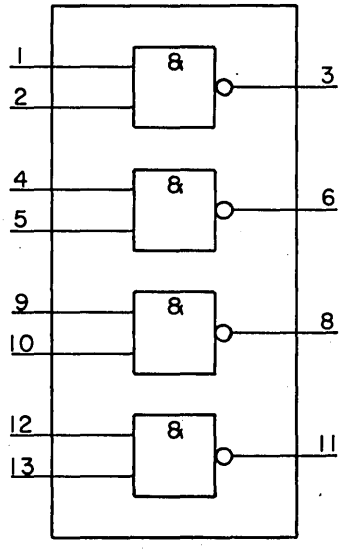


Figure 7-7. Type 126, Logic Diagram and Pin Assignments

2.1.3.6 Type 128, Triple 3-Input Gate

Figure 7-8 shows a triple 3-input gate package. Its function is the same as a 122, except for the number of inputs and the fact that it has no diode extender.

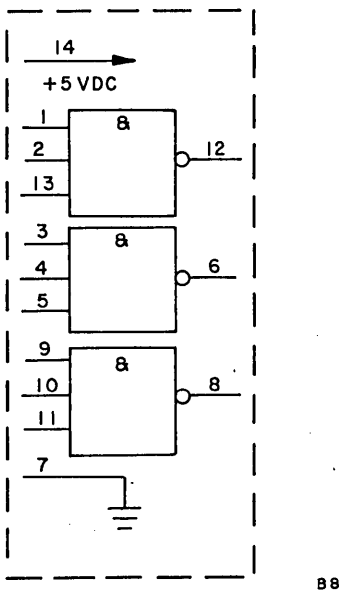


Figure 7-8. Type 128, Logic Diagram and Pin Assignment

2.1.3.7 Type 129, Hex 1-Input Inverter

Figure 7-9 shows a hex one-input inverter package. Each circuit performs the function of inversion only. The circular logic level indicator on the input or the output denotes the state, when active, of the signal feeding the 129 or the signal being output by the 129, respectively.

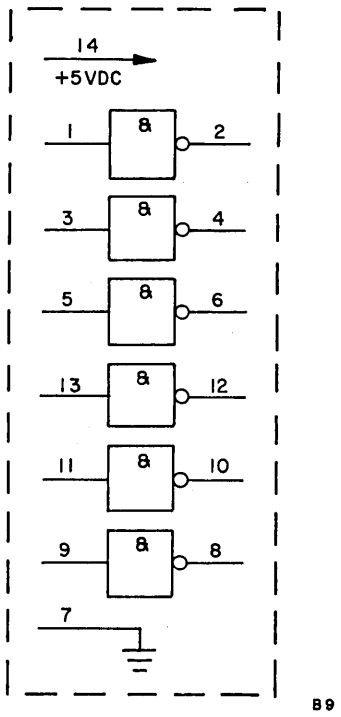


Figure 7-9. Type 129, Logic Diagram and Pin Assignments

2.1.3.8 Type 150, Dual J-K Flip-Flop

The type 150 is a dual J-K flip-flop consisting of two separate flip-flops, each one incorporating a master slave design. Pin assignments and a logic diagram are shown in Figures 7-10 and 7-11.

Data is accepted by the master flip-flop while the clock is high. Transfer of data from the master flip-flop to the slave flip-flop occurs on the high to low transition of the clock. When the clock is low, the J and K inputs are inhibited. The SD input provides a means of presetting the flip-flop.

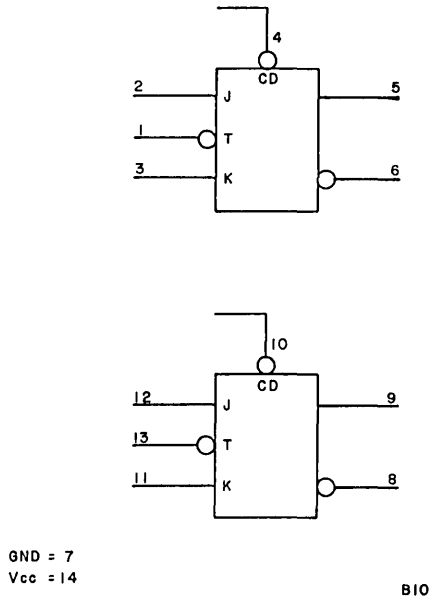


Figure 7-10. Type 150, Pin Assignments

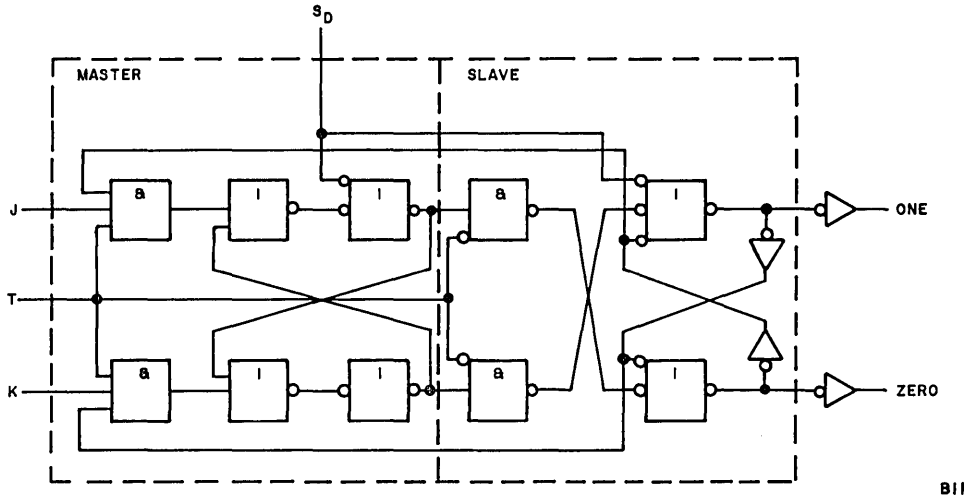


Figure 7-11. Type 150, Logic Diagram

Truth Table 7-2 defines the next state of the flip-flop after a high to low transition of the clock pulse. The output of the flip-flop is a function of the previous state of the flip-flop and the conditions of the inputs prior to a high to low transition of the clock.

INPUTS		OUTPUT BEFORE CLOCK GOES HIGH TO LOW		OUTPUT AFTER CLOCK GOES HIGH TO LOW	
J	K	ONE	ZERO	ONE	ZERO
L⋈	X	L	H	L	H
H⋈	X	L	H	H	L
X	L⋈	H	L	H	L
X	H⋈	H	L	L	H

L⋈ = defined as a low input that does not go high at any time while the clock is high.

L = steady state low voltage output.

H⋈ = defined as an input that is high at some time while the clock is high.

H = steady state high voltage output.

X = the condition of the input or output has no effect on the next state of the flip-flop.

Table 7-2. Type 150, Truth Table

2.1.3.9 Type 151, Dual J-K Flip-Flop

The type 151 is a dual J-K flip-flop. Refer to Figure 7-12 for pin assignments and to Figure 7-13 for a functional logic diagram.

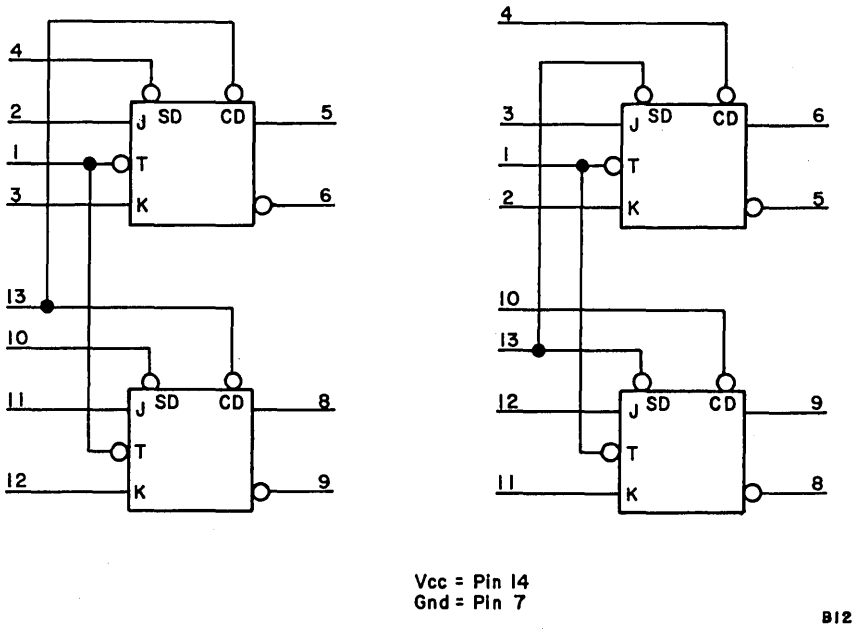


Figure 7-12. Type 151, Pin Assignments

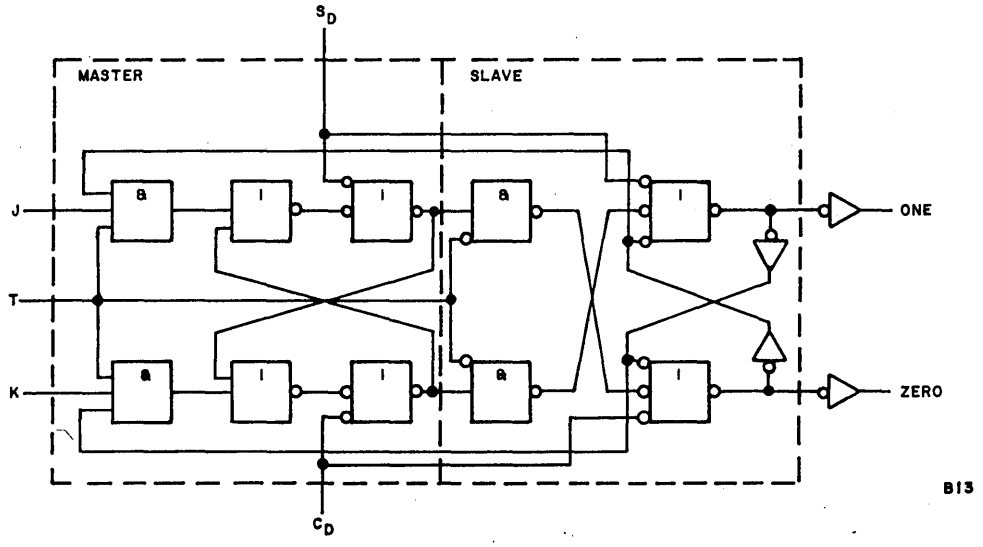


Figure 7-13. Type 151, Functional Logic Diagram

The type 151 is similar to the type 150 dual J-K flip-flop, however the type 151 has a clear direct input which the type 150 does not. The asynchronous set and clear inputs provide the ability to control the state of the flip-flop independent of static conditions on the clock and synchronous inputs.

Synchronous operation of the type 151 is the same as synchronous operation of the type 150. Refer to Table 7-2 for a truth table on synchronous operation of the type 150 and type 151. Refer to Table 7-3 for a truth table on asynchronous operation of the type 151.

INPUTS		OUTPUTS	
SD	CD	ONE	ZERO
L	L	H	H
L	H	H	L
H	L	L	H
H	H	STATE DETERMINED BY SYNCHRONOUS INPUTS AND CLOCK INPUT	

Table 7-3. Type 151, Asynchronous Operation Truth Table

2.1.4 Transistor-Transistor Logic

2.1.4.1 Type 140, Quad 2-Input NAND Gate

The type 140 is a quad 2-input NAND gate. The function of the TTL type 140 is the same as the DTL type 126 quad 2-input NAND gate, however it operates at a higher speed. Refer to Figure 7-14 for a logic diagram and pin configuration.

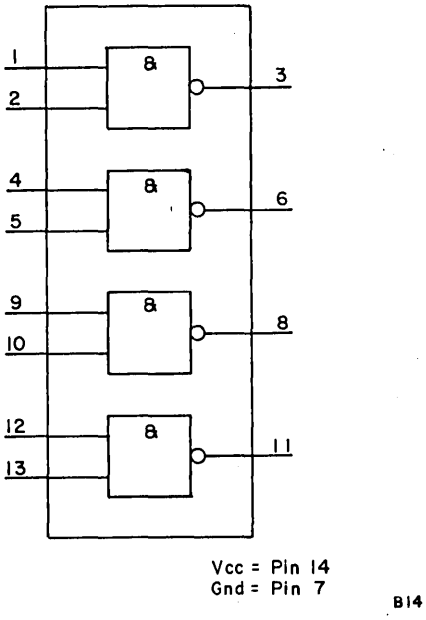


Figure 7-14. Type 140, Logic Diagram and Pin Assignments

2.1.4.2 Type 146, Hex Inverter

The type 146 is a hex inverter. It is similar to the DTL type 129, however it operates at a higher speed. Refer to Figure 7-15 for a logic diagram and pin assignments.

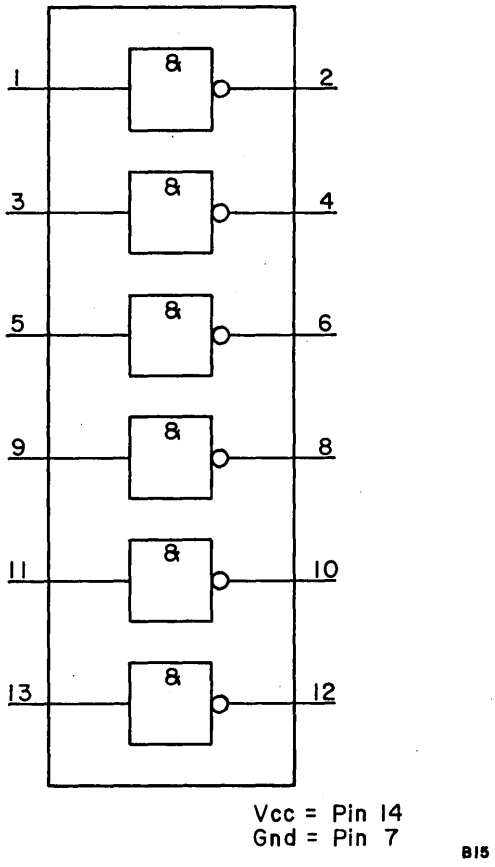


Figure 7-15. Type 146, Logic Diagram and Pin Assignments

2.1.4.3 Type 149, Quad 2-Input Exclusive-OR Gate

The type 149 is a quad 2-input exclusive-OR gate. Each circuit performs the function $Y = \overline{A}B + A\overline{B}$ When the input states are complementary, the output goes to a logic "1". Refer to Table 7-4, Truth Table.

INPUTS		OUTPUTS
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

Table 7-4. Type 149, Truth Table

Refer to Figure 7-16 for a logic diagram and pin assignments.

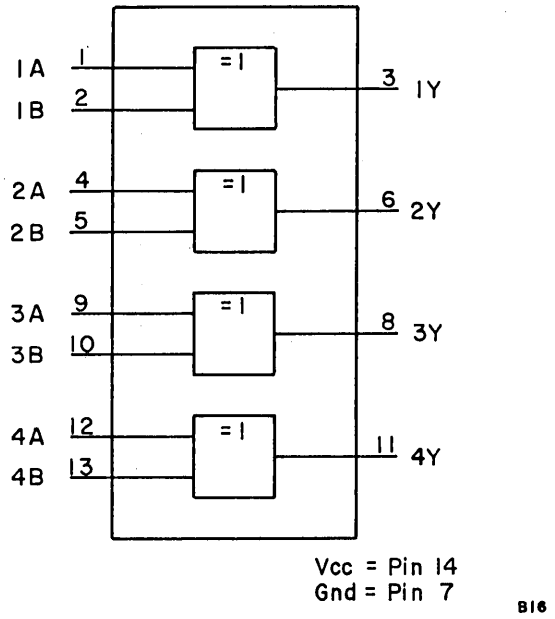


Figure 7-16. Type 149, Logic Diagram and Pin Assignments

2.1.4.4 Type 170, Dual 4-Input Multiplexer

The 170 is a dual 4-input digital multiplexer. It consists of two multiplexing circuits with common input select logic (S0 and S1). Each circuit contains four inputs and two fully buffered complementary outputs. The 170 allows two bits of data to be switched in parallel to either the high or low outputs from four 2-bit data sources. Both polarities of outputs are available.

The 170 is used to move data from up to four sources to a common output. The movement of the data is enabled by the select input. Refer to Figure 7-17 for pin assignments and to Figure 7-18 for a logic diagram of the 170. A truth table is shown in Table 7-5.

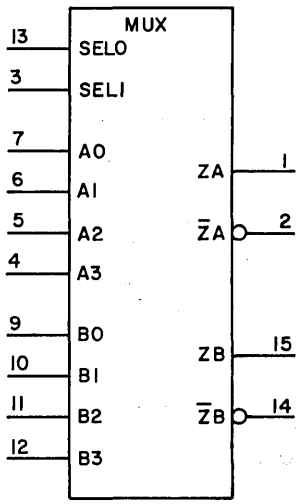


Figure 7-17. Type 170, Pin Assignments

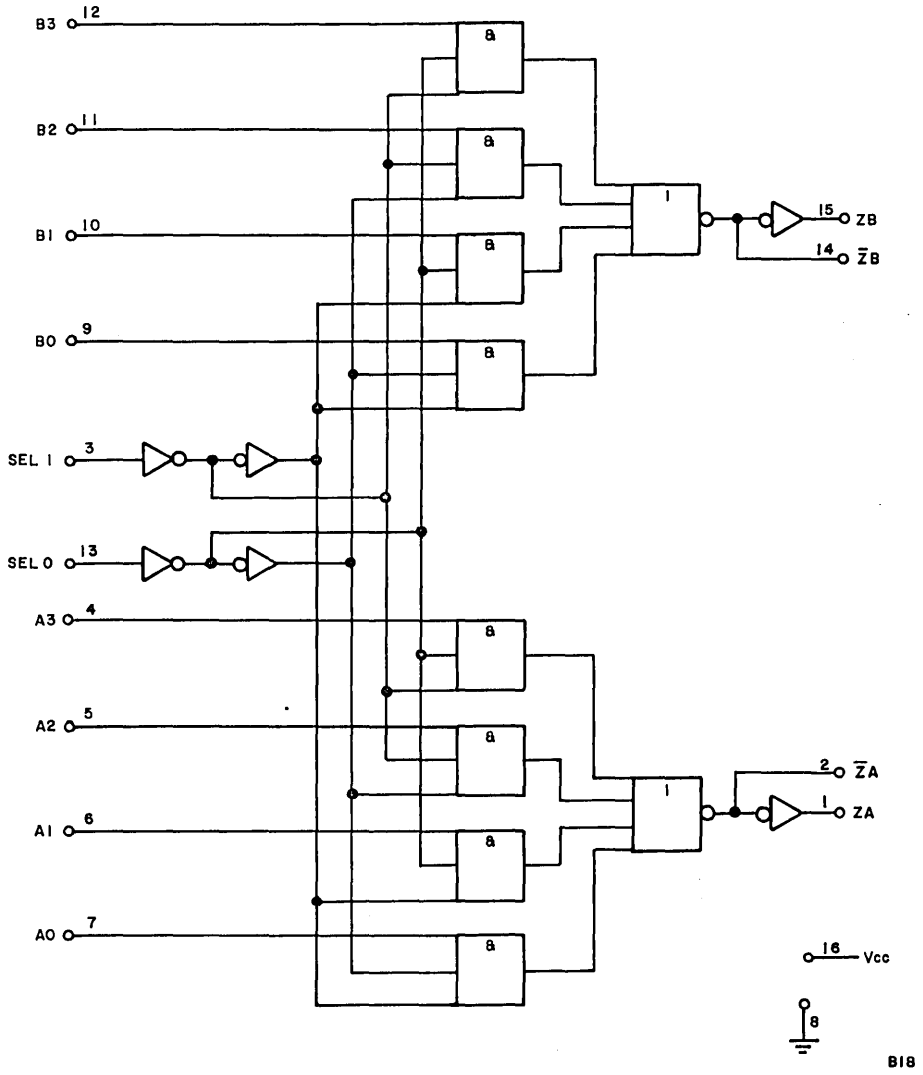


Figure 7-18. Type 170, Logic Diagram

SELECT INPUTS		INPUTS				OUTPUTS	
SEL0	SEL1	A3	A2	A1	A0	ZA	ZA
L	L	L	X	X	X	L	H
L	L	H	X	X	X	H	L
H	L	X	L	X	X	L	H
H	L	X	H	X	X	H	L
L	H	X	X	L	X	L	H
L	H	X	X	H	X	H	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	H	L
SEL0	SEL1	B3	B2	B1	B0	ZB	ZB
L	L	L	X	X	X	L	H
L	L	H	X	X	X	H	L
H	L	X	L	X	X	L	H
H	L	X	H	X	X	H	L
L	H	X	X	L	X	L	H
L	H	X	X	H	X	H	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	H	L

L = low voltage level

H = high voltage level

X = either high or low logic level

Table 7-5. Type 170, Truth Table

2.1.4.5 Type 189, Quad 2-Input Multiplexer

The type 189 is a quad 2-input multiplexer. It has a common enable (active low) input (EN), a common select input (SEL), and active high outputs (ZA, ZB, ZC, and ZD). Refer to Figure 7-19. It allows four bits of data to be switched in parallel to the appropriate outputs from two 4-bit data sources (A0 and A1, B0 and B1, C0 and C1, and D0 and D1). When the enable is not active (low), all the outputs are held low. Refer to Table 7-6, Truth Table.

$\overline{EN}$	SEL	A0 thru D0	A1 thru D1	ZA thru ZD
H	X	X	X	L
L	L	H	X	H
L	L	L	X	L
L	H	X	H	H
L	H	X	L	L

H = high voltage level

L = low voltage level

X = either high or low voltage level

Table 7-6. Type 189, Truth Table

2.1.4.6 Type 195, Dual Monostable Multivibrator

The type 195 is a dual, retriggerable monostable multivibrator (one-shot). The 195 provides an output pulse whose duration and accuracy is a function of external timing components. An active low reset input (CLR) allows the one shot to be reset. The inputs are DC coupled making triggering independent of input transition times. If the input signal is applied to an active high input, triggering will occur on the rising edge of the waveform. By applying the input signal to an active low input, triggering will occur on the falling edge of the waveform. The input conditions to be satisfied for triggering are indicated by external logic symbols in Figure 7-20.

Each time the input conditions for triggering are met, the external capacitor is discharged and a new cycle is started. Successive inputs with a period shorter than the delay time retrigger the monostable resulting in a continuous true output. Refer to Figure 7-20.

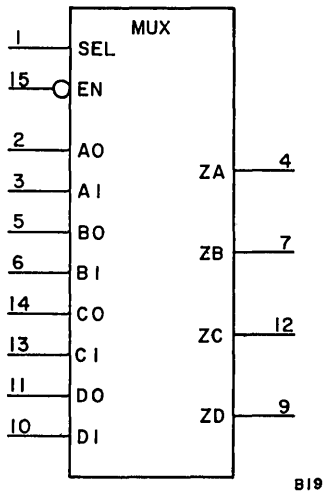


Figure 7-19. Type 189, Logic Diagram and Pin Assignments

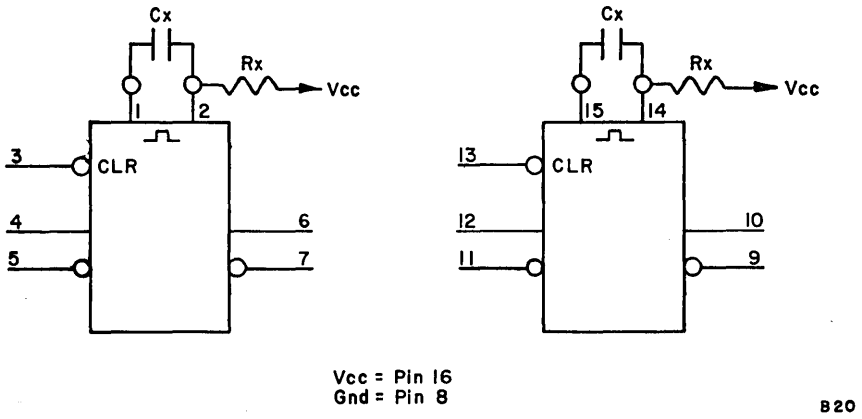


Figure 7-20. Type 195, Logic Diagram and Pin Assignments

2.1.4.7 Type 240, Dual J-K Flip-Flop

The type 240 is a dual J-K flip-flop. It is of the master-slave design.

The 240 is a dual edge triggered flip-flop which allows the inputs to change while the clock is low, and changes state according to the input conditions present a short set up period before the clock transition from low to high. This information is transferred to the outputs after the clock transition from low to high. The clocking operation is independent of the rise and fall times of the clock waveform. When the clock is high, the J and K inputs are inhibited. Refer to Figure 7-21 for pin assignments and a logic diagram of the 240.

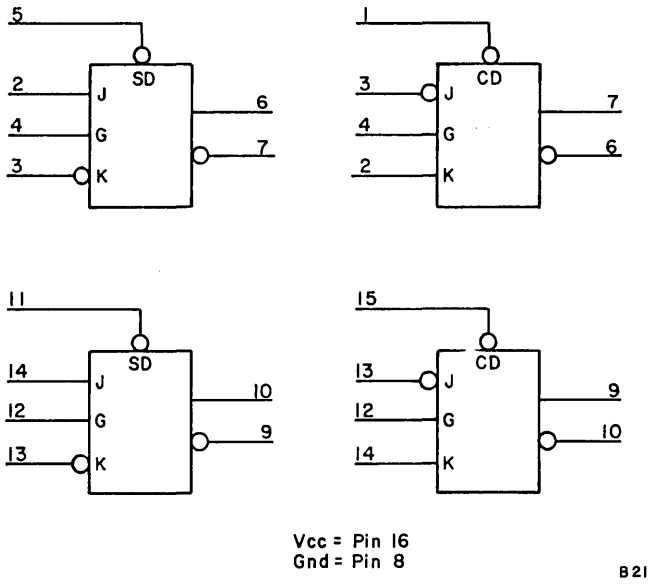


Figure 7-21. Type 240, Logic Diagram and Pin Assignments

The 240 has asynchronous inputs (SD and CD) which provide the ability to control the state of the flip-flop independent of static conditions of the clock and synchronous inputs. Refer to Table 7-7 for an asynchronous operation truth table.

INPUTS		OUTPUTS	
SD	CD	Q	$\overline{Q}$
L	L	H	H
L	H	H	L
H	L	L	H
H	H	Synchronous Inputs Control	

Table 7-7. Type 240, Asynchronous Operation Truth Table

Truth Table 7-8 defines the next state of the flip-flop after a low to high transition of the clock pulse during synchronous operation. The next state is a function of the J and K inputs.

INPUTS		OUTPUTS	
J	K	Q	$\overline{Q}$
L	H	NO CHANGE	
L	L	L	H
H	H	H	L
H	L	TOGGLE	

Table 7-8. Type 240, Synchronous Operation Truth Table

2.1.4.8 Type 500, Synchronous 4-Bit Binary Up/Down Counter

The type 500 is a synchronous 4-bit binary up/down counter. The direction of counting is selected by the input on pins 4 and 5. Refer to Figure 7-22. Synchronous operation is provided by having the four flip-flops clocked simultaneously so that the outputs change coincidentally with each other.

The outputs of the four master-slave flip-flops are triggered by a low-to-high transition of either the count down or count up input. Direction of counting is determined by which count input is pulsed while the other count input is high.

The counter is programmable. That is, the outputs may be preset to any state by entering the desired data at the data inputs while the load input (pin 11) is low. The output will change to agree with the data inputs independently of the count pulses.

The clear input forces all outputs to the low level when a high level is applied. The clear function is independent of the count and load inputs.

The counter has look ahead borrow and carry pulses. The borrow output produces a pulse at the same time and equal in width to the count-down input when the counter underflows. The carry output produces a pulse equal in width to the count up input when an overflow condition exists.

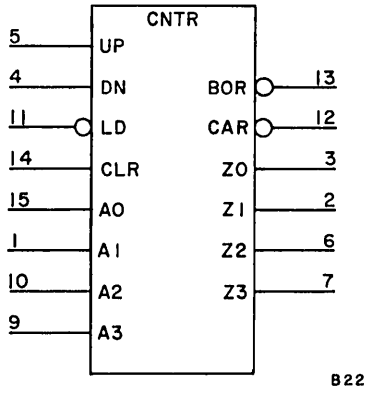


Figure 7-22. Type 500, Pin Assignments

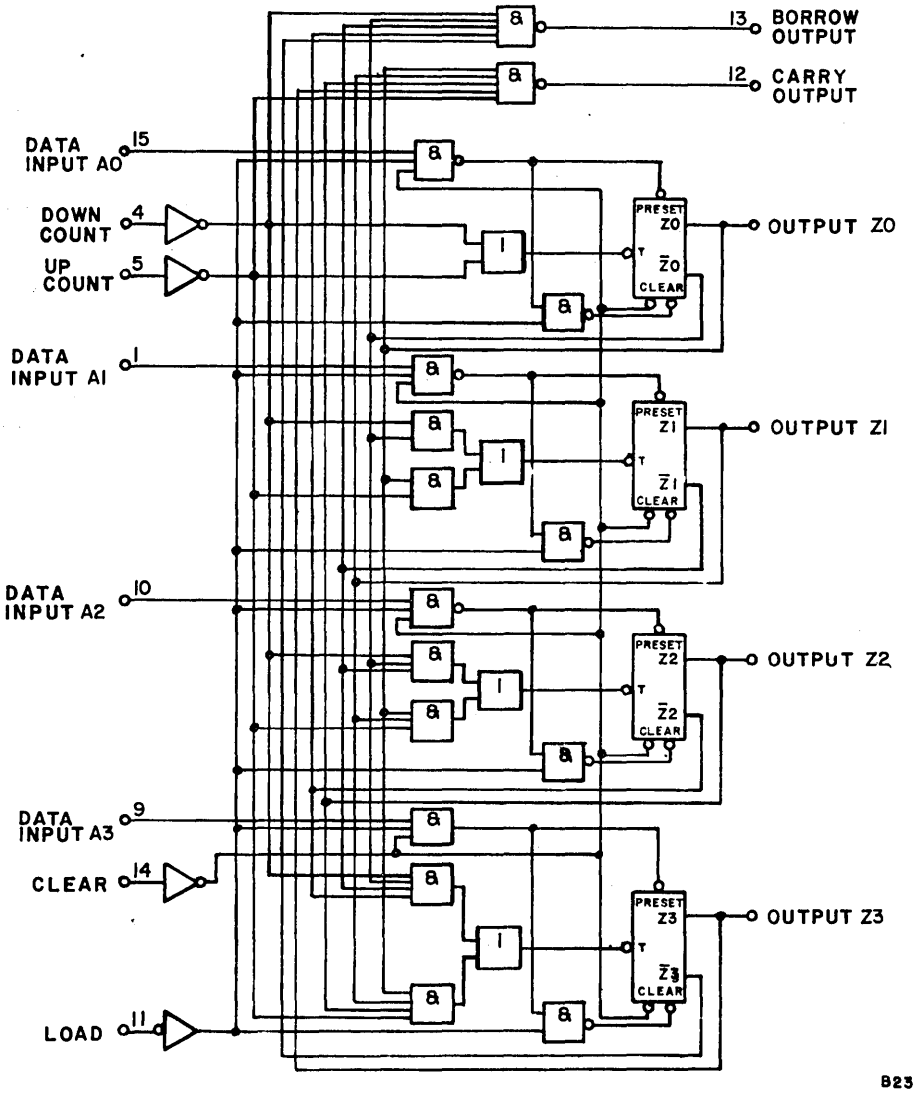
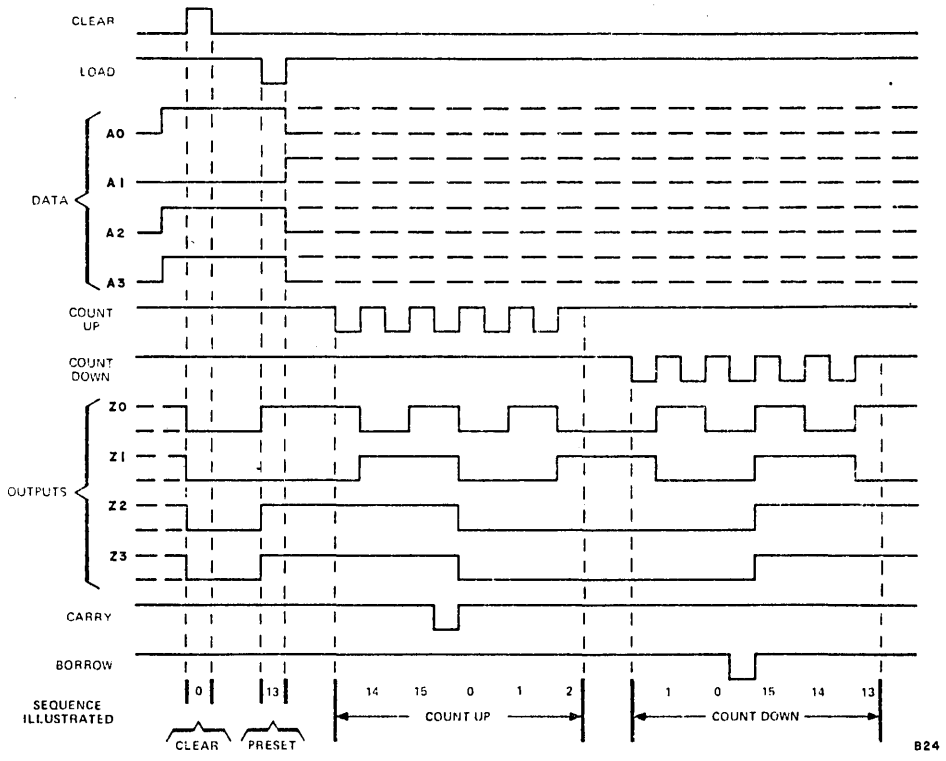


Figure 7-23. Type 500, Logic Diagram

typical clear, load, and count sequences

Illustrated below is the following sequence:

1. Clear outputs to zero.
2. Load (preset) to BCD thirteen.
3. Count up to fourteen, fifteen, carry, zero, one, and two.
4. Count down to one, zero, borrow, fifteen, fourteen, and thirteen.



NOTES: A. Clear overrides load, data, and count inputs.
B. When counting up, count-down input must be high, when counting down, count up input must be high.

Figure 7-24. Type 5001 Timing Diagram

2.1.4.9 Type 502, 8-Bit Odd/Even Parity Generator/Checker

The type 502 is a 8-Bit odd/even parity generator/checker. The eight data bits are input on pins 8 through 13, 1 and 2. To function as an even parity generator/checker, the input to pin 3 must be a "1" and to pin 4 a "0". To function as an odd parity generator/checker, the input to pin 4 must be a "1" and to pin 3 a "0". An even parity generator/checker will output a "1" on pin 5 and a "0" on pin 6 when the sum of the data inputs is even. An odd parity generator/checker will output a "1" on pin 5 and a "0" on pin 6 when the sum of the data inputs is odd. When the inputs to pins 3 and 4 are both "1" the outputs on pins 5 and 6 will be "0" regardless of data inputs. When the inputs to pins 3 and 4 are both "0" the output on pins 5 and 6 will be "1" regardless of data inputs. Refer to Figures 7-25 and 7-26. Refer to Table 7-9 for a truth table for the type 502.

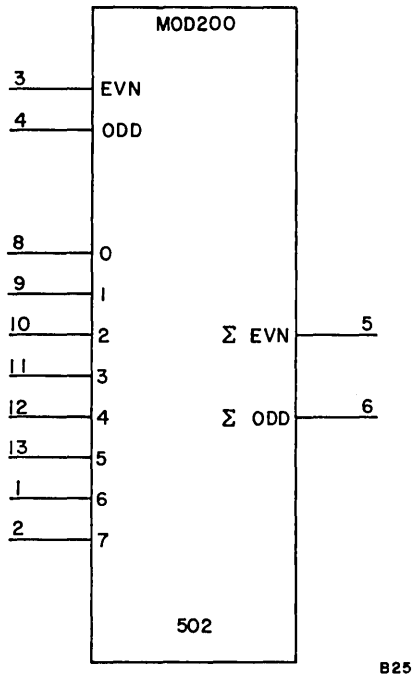


Figure 7-25. Type 502, Pin Assignments

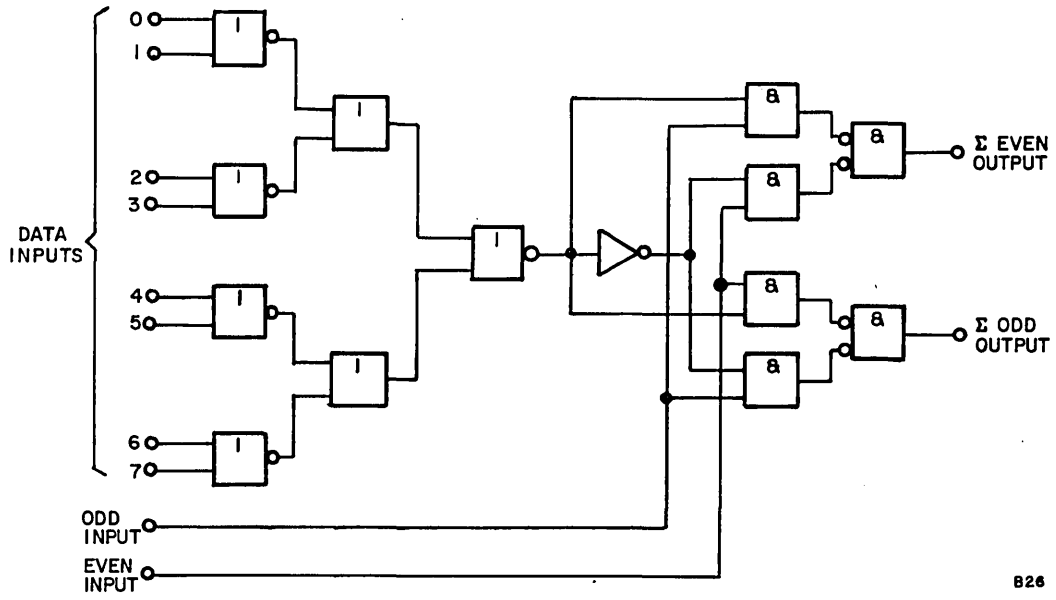


Figure 7-26. Type 502, Logic Diagram

INPUTS			OUTPUTS	
Σ of 1's AT 0 thru 7	EVEN	ODD	Σ EVEN	Σ ODD
EVEN	1	0	1	0
ODD	1	0	0	1
EVEN	0	1	0	1
ODD	0	1	1	0
X	1	1	0	0
X	0	0	1	1

X = irrelevant

Table 7-9. Type 502, Truth Table

2.1.4.10 Type 514, 16-Bit Register File (Memory)

The type 514 is a 16-Bit register file (memory). It is designed for four words, four bits each operation. Separate on-chip decoding is provided for addressing the word locations for either writing in or retrieving data. This permits simultaneous writing into one location and reading from another word location. The data inputs supply the word to be stored. Location of the word is determined by the write address inputs A and B in conjunction with the write enable signal. Data applied to the inputs will be the same as the data output for a particular location. That is, if a high level signal is desired at the output, a high level signal should be applied at the input. Refer to Figures 7-27 and 7-28. Refer to Table 7-10 for a truth table for the type 514.

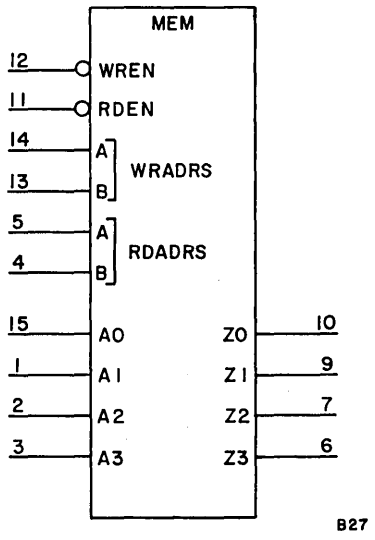


Figure 7-27. Type 514, Pin Assignments

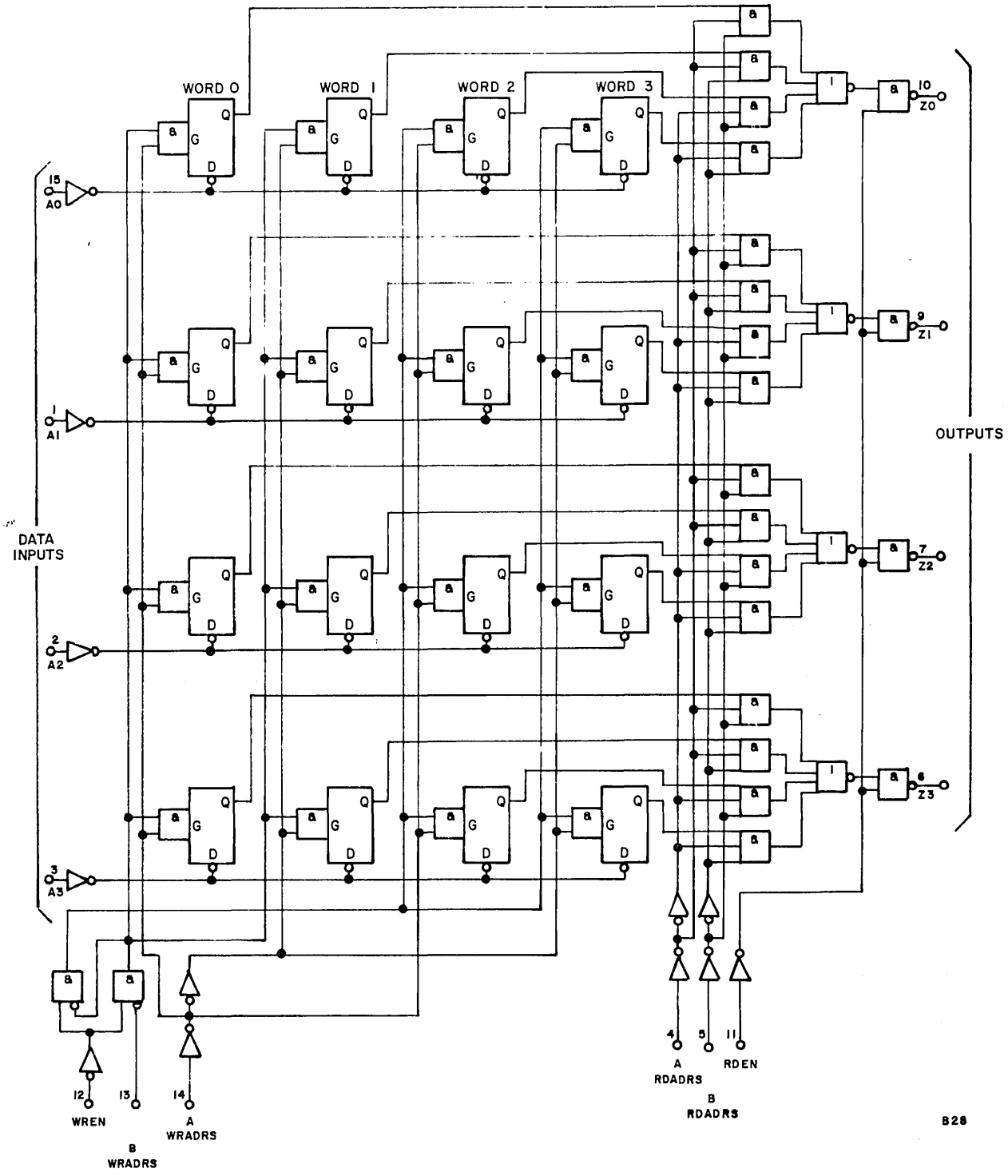


Figure 7-28. Type 514, Logic Diagram

WRITE FUNCTION TABLE (See Notes A, B, and C)

WRITE INPUTS			WORD			
B WRADRS	A WRADRS	WREN	0	1	2	3
L	L	L	Q=D	Q_n	Q_n	Q_n
L	H	L	Q_n	Q=D	Q_n	Q_n
H	L	L	Q_n	Q_n	Q=D	Q_n
H	H	L	Q_n	Q_n	Q_n	Q=D
X	X	H	Q_n	Q_n	Q_n	Q_n

READ FUNCTION TABLE (See Notes A and D)

READ INPUTS			OUTPUTS			
B RDADRS	A RDADRS	RDEN	Z0	Z1	Z2	Z3
L	L	L	W0B1	W0B2	W0B3	W0B4
L	H	L	W1B1	W1B2	W1B3	W1B4
H	L	L	W2B1	W2B2	W2B3	W2B4
H	H	L	W3B1	W3B2	W3B3	W3B4
X	X	H	H	H	H	H

Table 7-10. Type 514, Truth Table

NOTES: A. H = high level
L = low level
X = irrelevant

B. (Q=D) = The four selected internal flip-flop outputs will assume the states applied to the four external data inputs.

C. Q_n = No change.

D. WOB1 = The first bit of word 0, etc.

2.1.4.11 Type 515, 5-Bit Shift Register

The 515 is a 5-bit shift register. It consists of five R-S master-slave flip-flops connected to form parallel-to-serial or serial-to-parallel conversion of binary data. Since both inputs and outputs to all flip-flops are accessible, parallel-in/parallel-out or serial-in/serial-out operation may be performed. The five flip-flops are simultaneously set to the logical "0" state by applying a logical "0" voltage to the clear input. This condition may be applied independent of the state of the clock input.

The flip-flop may be independently set to the logic "1" state by applying a logic "1" to both the preset input of the specific flip-flop and the common preset input. The common preset input is provided to permit setting each flip-flop independently or setting two or more flip-flops simultaneously. Preset is also independent of the state of the clock input or clear input.

Transfer of information to the output pins occurs when the clock input goes from a logic "0" to a logic "1". Since the flip-flops are R-S master-slave circuits, the proper information must appear at the R-S inputs of each flip-flop prior to the rising edge of the clock input voltage waveform. The serial input provides this information to the first flip-flop while the outputs of the subsequent flip-flop provide information for the remaining R-S inputs. The clear input must be at a logic "1" and the preset input must be at a logic "0" when clocking occurs. Refer to Figure 7-29 for the logic symbol and to Figure 7-30 for pin assignments and a logic diagram.

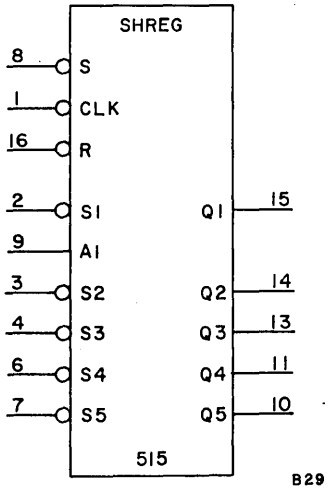


Figure 7-29. Type 515 Logic Symbol

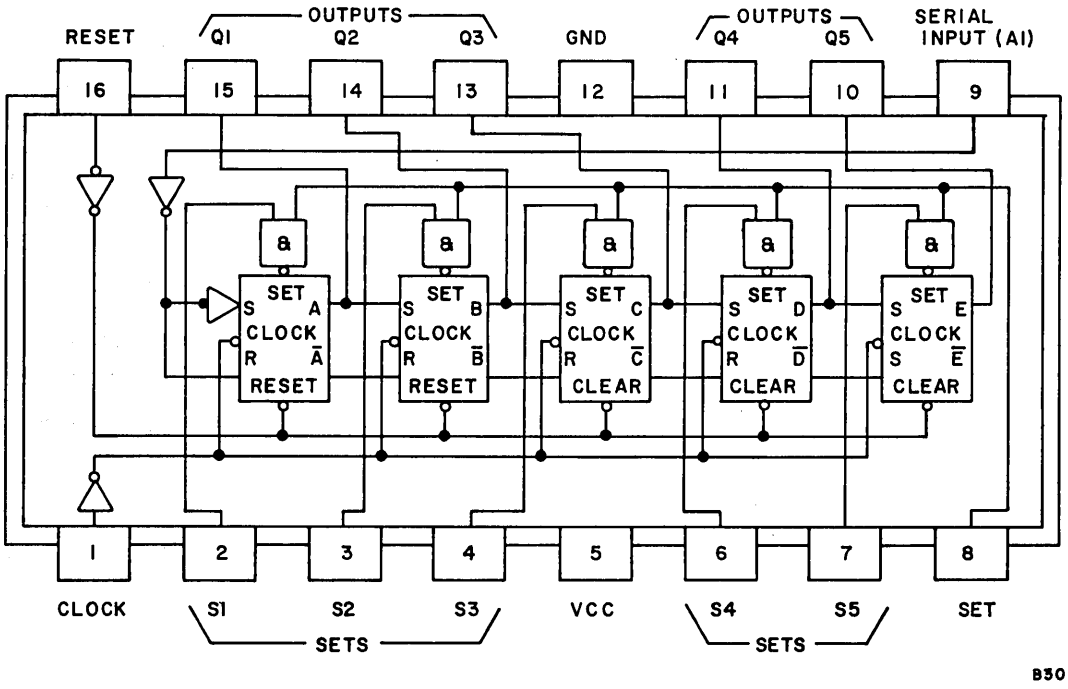


Figure 7-30. Type 515, Logic Diagram and Pin Assignments

2.1.5 DTL/TTL Compatible Interface Circuits

2.1.5.1 Type 162, Dual Line Receiver

The type 162 is a DTL/TTL compatible high speed dual line receiver. The receiver has two independent channels with common voltage supply and ground. The 162 is designed to detect low-level differential signals (25 millivolts or greater) and convert the polarity of the signal into appropriate TTL compatible output logic levels. Refer to Figure 7-31 for a logic symbol.

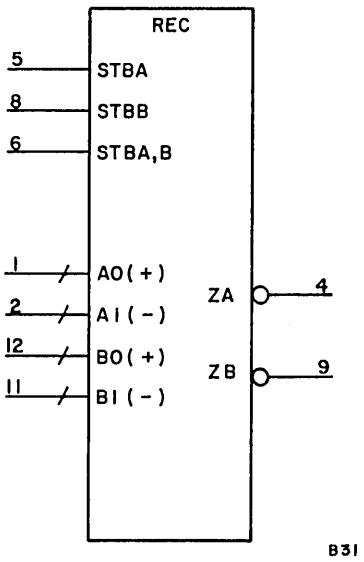


Figure 7-31. Type 162, Logic Symbol

The receiver has a Strobe input to each channel (STBA and STBB) and a common Strobe (STBA,B) to both channels.

Refer to Table 7-11, Truth Table. When the voltage differential between pins A and B (ID) is equal to or greater than ±25 millivolts, output Y will be high regardless of the Strobe inputs. If the differential input voltage (ID) is greater than -25 millivolts but less than +25 millivolts the output Y will be high for any Strobe input except when the Strobes are both high, then the output is indeterminate. If the differential input voltage is equal to or less than -25 millivolts, the output will be high for any Strobe input except when both the inputs are high, then the output is low. Refer to Figure 7-32 for a logic diagram and pin assignments.

DIFFERENTIAL INPUTS (ID) A-B	STBA or STBB	STBA,B	OUTPUT Y
$V_{ID} \geq 25$ mV	L or H	L or H	H
-25 mV < V_{ID} < 25mV	L or H	L	H
	L	L or H	H
	H	H	INDETERMINATE
$V_{ID} \leq -25$ mV	L or H	L	H
	L	L or H	H
	H	H	L

Table 7-11. Type 162, Truth Table

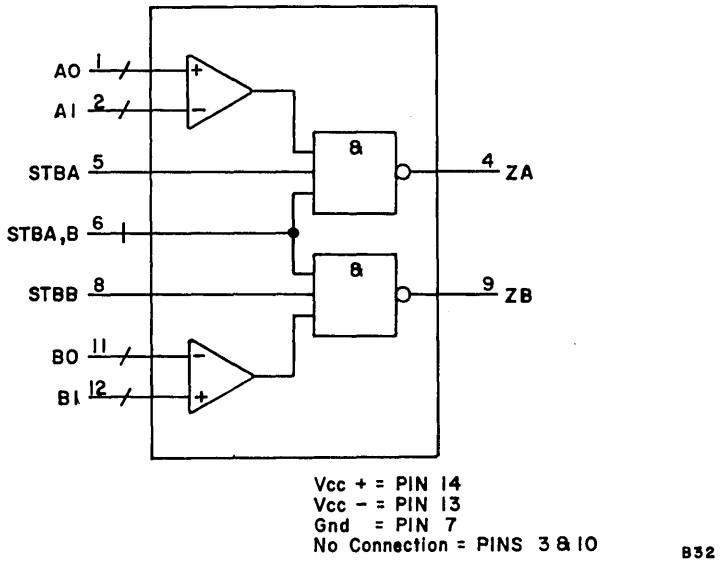


Figure 7-32. Type 162, Logic Diagram and Pin Assignments

2.1.5.2 Type 176, Dual Line Driver

The type 176 is a DTL/TTL compatible high speed dual line driver. The driver has two independent channels with common voltage supply and ground terminals. The 176 provides a constant output that is switched to either of the two output terminals, depending upon the logic level at the two input terminals. The output can be switched off (inhibited) by appropriate logic levels on the inhibited inputs. Refer to Table 7-12, Truth Table. If either the INHA or INHB or INHA,B are low, the output will be high (off state) regardless of the inputs. If an INHA or INHB and INHA,B are high, the ZA(+) and ZB(+) outputs will be low (on state) and the ZA(-) and ZB(-) outputs high if either or both input are low. If both an INHA or INHB and INHA,B are high and both the inputs are high, the ZA(+) and ZB(+) outputs will be high and the ZA(-) and ZB(-) output low. Refer to Figure 7-33 for a logic symbol. Refer to Figure 7-34 for a logic diagram and pin assignments.

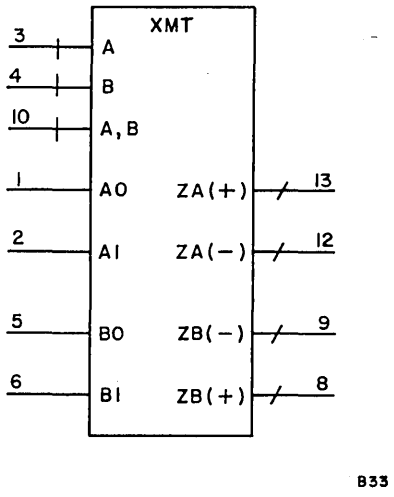


Figure 7-33. Type 176 Logic Symbol

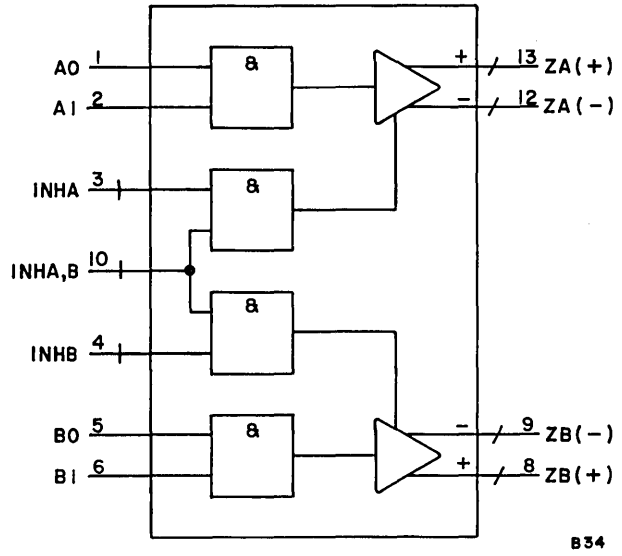


Figure 7-34. Type 176, Logic Diagram and Pin Assignments

LOGIC INPUTS		INHA or INHB	INHA,B	OUTPUTS	
A	B			ZA{+},ZB{+}	ZA{-},ZB{-}
L or H	L or H	L	L or H	H	H
L or H	L or H	L or H	L	H	H
L	L or H	H	H	L	H
L or H	L	H	H	L	H
H	H	H	H	H	L
Low output represents the on state. High output represents the off state.					

Table 7-12. Type 176, Truth Table

2.2 Discrete Component Circuits

2.2.1 Type AA10 Oscillator

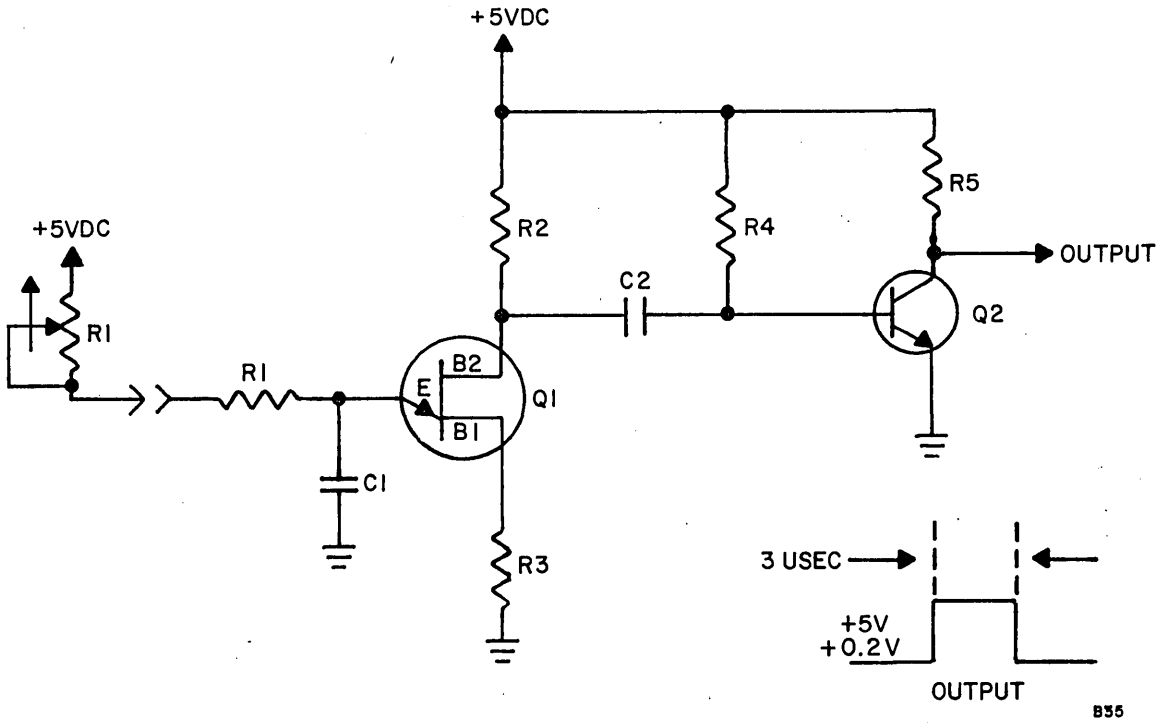


Figure 7-35. Type AA10, Schematic

This circuit consists of a unijunction relaxation oscillator, a differentiator, and a pulse-shaping amplifier. The quiescent state of the circuit is with Q1 cut off and Q2 conducting. Refer to Figure 7-35. This causes the collector of Q2 to be clamped at a voltage close to ground. The RC circuit composed of R1 (front panel), R1 (logic board), and C1 is the frequency determining element of the oscillator.

As C1 charges, a voltage is reached on the emitter of Q1 which will fire Q1. When Q1 fires, C1 discharges back through the Base 1 Emitter junction. While this discharge is occurring, a negative-going pulse of approximately 0.5 volts is formed on Base 2. C2 and R4 differentiate the Base 2 pulse. The negative portion of the differentiated waveform cuts off Q2. The collector of Q2 goes to +5VDC for nominally three microseconds.

Section 8

Parts

Section 8

Parts

The following parts are replaceable by the Customer Engineer and are available from Customer Engineering Materials.

DESCRIPTION	CDC PART NUMBER	REFERENCE DESIGNATOR
Capacitor, .22 ufd,	72407205	C3, C4
Capacitor 9200 ufd,	58018802	C1, C2
Diode, Gernianium	51001277	
Diode, Silicon	51007385	
Display Unit, 3 Digit	59327300	DS1, DS2, DS3
Fan	58007101	B1, B2
Indicator, Light Emitting Diode, (LED)	59315704	DS4, DS5, DS6, DS7, DS8, DS9, DS10, DS11, DS12, DS13, DS14, DS15, DS16
Integrated Circuit, CDC Type 122 Motorola MC830P Fairchild SL4669 ITT NC 2520	51577500	
Integrated Circuit, CDC Type 126 Motorola MC 846 Fairchild SL 946	51577900	
Integrated Circuit, CDC Type 128 Motorola MC 862P Fairchild SL 4675 ITT NC 2526	51578100	

DESCRIPTION	CDC PART NUMBER	REFERENCE DESIGNATOR
Integrated Circuit, CDC Type 129	51654400	
ITT MIC-9936-5D		
Integrated Circuit, CDC Type 140	50250600	
Texas Instruments 7400 Fairchild 9002		
Integrated Circuit, CDC Type 146	51701800	
Texas Instruments 7404 Fairchild 9016		
Integrated Circuit, CDC Type 149	36188200	
Texas Instruments 7486		
Integrated Circuit, CDC Type 150/154	51717000	
Fairchild 9094		
Integrated Circuit, CDC Type 151/155	51717100	
Fairchild 9097		
Integrated Circuit, CDC Type 162	50252900	
Texas Instruments 75107		
Integrated Circuit, CDC Type 170	51761700	
Fairchild 9309		
Integrated Circuit, CDC Type 176	50252800	
Texas Instruments 751100		

DESCRIPTION	CDC PART NUMBER	REFERENCE DESIGNATOR
Integrated Circuit, CDC Type 189 Texas Instruments 74157 Fairchild 9322	51784000	
Integrated Circuit, CDC Type 195 Fairchild 9602	59319800	
Integrated Circuit, CDC Type 240 Fairchild 9024	51786700	
Integrated Circuit, CDC Type 500 Texas Instruments 74193 Fairchild 9366	17184200	
Integrated Circuit, CDC Type 502 Texas Instruments 74180	15105400	
Integrated Circuit, CDC Type 514 Texas Instruments 74170	15104000	
Integrated Circuit, CDC Type 515 Texas Instruments 7496 Fairchild 9396	15104100	
Potentiometer, with Power Switch, 0 to 250 ohms	58045010	R/S1/ R/S2
Power Supply Assembly	59327700	PS1
Printed Circuit Card, 1AZF	59329700	

DESCRIPTION	CDC PART NUMBER	REFERENCE DESIGNATOR
Printed Circuit, Card 1BAF	59330400	
Printed Circuit, Card 2 AZF	86816900	
Printed Circuit, Card, 1 BCF	59331000	
Printed Circuit Card, 1 BDF	59331300	
Printed Circuit Card, 2 BAF	86817200	
Printed Circuit Card, 1 BFF	59331900	
Printed Circuit Card 1 BGF	59332200	
Switch-Indicator, Light Emitting Diode (LED)	59315604	S/DS1 thru S/DS8
Switch, Pushbutton, DPDT	58046151	S16
Switch, Rotary, 1 Deck 9 position	58006815	S26
Switch, Rotary, 1 Deck 24 position	59327500	S16
Switch, Toggle, SPDT, ON-ON	58008503	S3 thru S7 S12, S25
Switch, Toggle, SP3T ON-NONE-ON	58008504	S9, S11, S13
Switch, Toggle, SP3T ON-ON-ON	58008509	S8, S10
Switch, Toggle, SP3T ON (mom.)--OFF-ON-(mom.)	58008505	S14, S15
Switch, Toggle, DPDT ON-ON	58008502	S1
Timer, 200 Hour	58045205	XM1
Transistor, CDC DDI 106	51003059	Q2 (1BCF) Q3 (2BAF, 2AZF)
Transistor, T1S43	51569300	Q1 (1BCF)
Transistor, 2N3414	38906100	Q2 (2BAF, 2AZF)
Transistor, Unijunction, 2N2647	51569300	Q1 (2BAF, 2AZF)
Transformer, Step Down	58007006	T1

DESCRIPTION	CDC PART NUMBER	REFERENCE DESIGNATOR
Rectifier, Bridge 25A	59319700	BR1, BR2
Regulator, Voltage Type 352, LM309K	15105300	VR1 - VR3
Switch, Toggle, DP3T, ON-OFF-ON	58008500	S17-S24

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