83324850

CONTROL DATA CORPORATION

CDC® EXPANDED MODULE DRIVE

PA1A2

PA1A3

THEORY OF OPERATION

GENERAL MAINTENANCE INFORMATION

TROUBLE ANALYSIS

ELECTRICAL CHECKS AND ADJUSTMENTS

REPAIR AND REPLACEMENT

Volume 2

HARDWARE MAINTENANCE MANUAL

REVISION RECORD

REVISION	DESCRIPTION
01 (06-14-83)	Preliminary release
02 (01-19-84)	Technical and editorial corrections.
A (06-01-84)	Original release. This edition obsoletes all previous editions.

REVISION LETTERS I, O, Q AND X ARE NOT USED.

Address comments concerning this manual to:

Control Data Corporation
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Customer Documentation Dept.
5950 Clearwater Drive
Minnetonka, MN 55343

or use Comment Sheet in the back of this manual.

LIST OF EFFECTIVE PAGES

Sheet 1 of 5

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PREFACE

This manual contains maintenance information for the CONTROL DATA® PA1A2 and PA1A3 Expanded Module Drive (XMD). It is prepared for customer engineers and other technical personnel directly involved with maintaining the XMD.

The information in this manual is presented as follows:

Section 1 - Theory of Operation. Describes power functions, electromechanical functions, interface, unit selection, servo surface decoding, sector detection, seek functions, head selection, read/write functions, and fault detection.

Section 2 - General Maintenance Information. Contains information on warnings and precautions, maintenance tools and materials, testing the drive, and accessing the drive for maintenance.

Section 3 - Trouble Analysis. Contains procedures and information to assist in troubleshooting the drive.

Section 4 - Electrical Checks and Adjustments. Provides electrical test procedures.

Section 5 - Repair and Replacement. Contains procedures and information on the replacement and adjustment of drive assemblies.

The following manuals apply to the XMD and are available from Control Data Corporation, Literature Distribution Services, 308 North Dale Street, St. Paul, MN 55103:

Publication No.	Title
83324840	PA1A2 and PA1A3 Hardware Maintenance Manual, Volume 1 (contains general description, operation, installation and checkout information, and parts data)

(Continued on Next Page)

Publication No.	Title
83324850	PA1A2 and PA1A3 Hardware Maintenance Manual, Volume 2 (contains theory of operation and maintenance)
83324860	PA1A2 and PA1A3 Hardware Maintenance Manual, Volume 3 (contains diagrams)
83322440	CDC Microcircuits, Volume 1 (provides functional descriptions for integrated circuits)
83324440	CDC Microcircuits, Volume 2 (provides functional descriptions for integrated circuits)

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ABBREVIATIONS

A	Ampere
ABR	Absolute Reserve
ABV	Above
ac	Alternating Current
ADD	Address
ADDR	Address
ADJ	Adjust
ADRS	Address
AGC	Automatic Gain Control
ALT	Alternate
AM	Address Mark
AME	Address Mark Enable
AMP	Amplifier, Ampere
ASSY	Assembly
BLW	Below
C	Celsius
CB	Circuit Breaker
CDA	Complete Drive Assembly
CDC	Control Data Corporation
CH	Channel
CHK	Check
CLK	Clock
CLR	Clear
cm	Centimeter
CNTR	Counter
COMP	Comparator
CONT	Control
CONTD	Continued
CT	Center Tap
CYL	Cylinder
D/A	Digital to Analog
dc	Direct Current
DET	Detect
DIFF	Differential
DIV	Division
DLY	Delay
DRVR	Driver
ECL	Emitter Coupled Logic
ECO	Engineering Change Order
EMI	Electromagnetic Interference

ABBREVIATIONS (Contd)

EN	Enable
ENBL	Enable
EXT	External
F	Fahrenheit, Fuse
FCO	Field Change Order
FDBK	Feedback
FIG	Figure
FLT	Fault
ft	Foot
FTU	Field Test Unit
FWD	Forward
GND	Ground
HD	Head
HDA	Head and Disk Assembly
HEX	Hexagon
Hg	Mercury
HR	High Resolution
HYST	Hysteresis
Hz	Hertz
IC	Integrated Circuit
IDENT	Identification
in	Inch
IND	Index
INTRPT	Interrupt
I/O	Input/Output
IPB	Illustrated Parts Breakdown
IPS	Inches per Second
kg	Kilogram
kPa	Kilopascal
kW	Kilowatt
lb	Pound
LED	Light Emitting Diode
LSI	Large Scale Integration
LTD	Lock to Data
m	Meter
MAX	Maximum
MB	Megabyte

ABBREVIATIONS (Contd)

MEM	Memory
MHz	Megahertz
mm	Millimeter
MPI	Magnetic Peripherals, Inc.
MPU	Microprocessor Unit
MRK	Mark
ms	Millisecond
MTR	Motor
mV	Millivolt
NC	No Connection
NORM	Normal
NRZ	Non Return to Zero
ns	Nanosecond
OC	On Cylinder
OS	One-Shot
OSC	Oscillator
P	Plug
PD	Peak Detect
pF	Picofarad
PG	Page
PHH	Phillips Head
PLO	Phase Lock Oscillator
PROC	Procedure
PROG	Programmable
PS	Power Supply
PWR	Power Supply
RCVR	Receiver
RD	Read
RDY	Ready
REF	Reference
REQ	Request
RES	Reserved
REV	Reverse, Revision
RGTR	Register
r/min	Revolutions Per Minute
RTM	Reserve Timeout Mode
RTZ	Return to Zero

ABBREVIATIONS (Contd)

R/W	Read/Write
s	Second
S/C	Series Code
SEC	Second
SEL	Select
SEQ	Sequence
SPD	Speed
SS	Sector Switch
T	Tracks to go
TF	Thread Forming
TIM	Timer
TP	Test Point
TSP	Troubleshooting Procedure
TTL	Transistor-Transistor Logic
V	Volts, Voltage
Vbb	Bias Voltage
VCC	Bias Voltage
VCO	Voltage Controlled Oscillator
W	Watts
W/	With
W/O	Without
W PROT	Write Protect
W+R	Write or Read
W·R	Write and Read
WRT	Write
XFR	Transfer
XMD	Expanded Module Drive
Ω	Ohms
$	Hexadecimal Address
uF	Microfarad
us	Microsecond

SECTION 1

THEORY OF OPERATION

THEORY OF OPERATION 1

INTRODUCTION

The theory of operation section describes drive operations and the hardware used in performing them. It is divided into the following major areas (refer to figure 1-1):

- Power Functions - Describes how the drive provides the voltages necessary for drive operation.
- Electromechanical Functions - Provides a physical and functional description of the mechanical and electromechanical portions of the drive disk rotation, head positioning, and air flow systems.

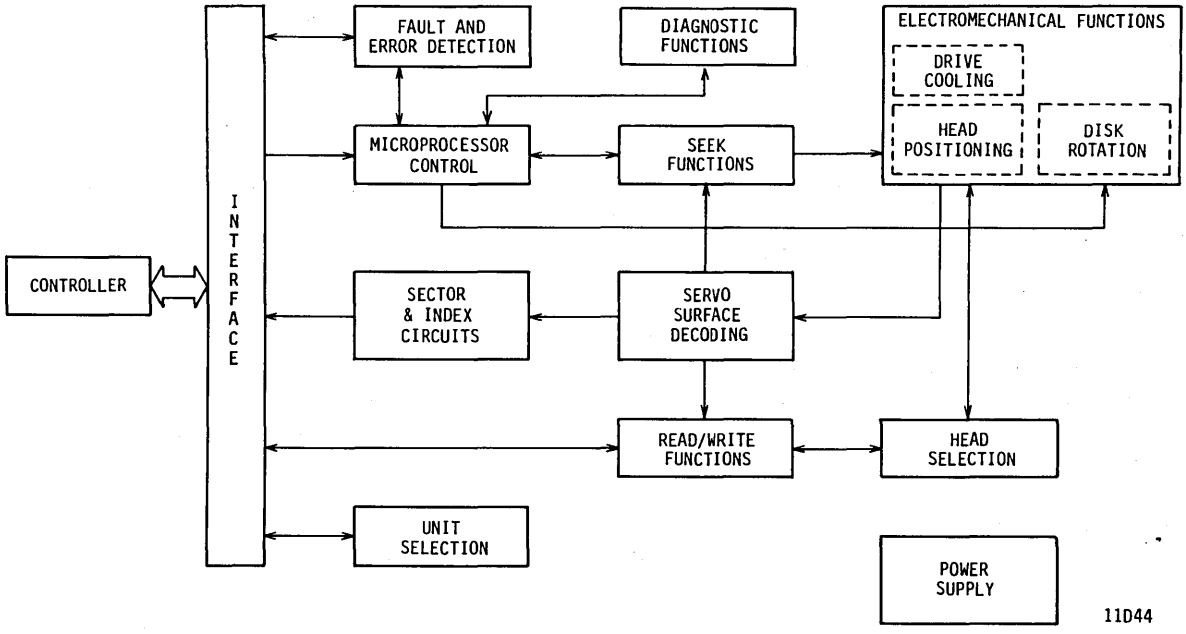


Figure 1-1. Drive Functional Block Diagram

- Interface - Describes the signal lines connecting the drive and controller. It also describes the I/O signals carried by these lines and how they are processed by the drive logic.

- Unit Selection - Explains how the controller logically selects the drive, so the drive will respond to controller commands.

- Servo Surface Decoding - Explains how the decoding of the data read from the servo surface by the servo head is used to locate the radial position of the heads during a seek movement, the rotational position of the disks (indicated by the Index signal) when the heads are on track, and the exact speed of the disks (indicated by the 2.41 MHz clock signal).

- Sector Detection - Explains how the drive derives the sector pulses that are used to determine the angular position, with respect to index, of the read/write heads.

- Seek Functions - Explains how the servo logic controls the movements of the head positioning mechanism in positioning the heads over the disks.

- Head Selection - Explains the head selection process.

- Read/Write Functions - Describes how the drive processes the data that it reads from and writes on the disk.

- Fault Detection - Describes the conditions that the drive interprets as faults.

The descriptions in this section are limited to drive operations only. In addition, they explain typical operations and do not list variations or unusual conditions resulting from unique system hardware or software.

Functional descriptions are frequently accompanied by simplified logic and timing diagrams. These are useful both for instructional purposes and as an aid in troubleshooting. However, they have been simplified to illustrate the principles of operation. Therefore, the diagrams (and timing generated from them) in volume 3 of the hardware maintenance manual should take precedence over those in this section if there is a conflict between the two.

POWER FUNCTIONS

GENERAL

Power functions are processes that take place within the power supply and the drive when the drive is initialized, loaded, or stopped. The load operation is conditioned by whether the drive is set up for local or remote operation. In all cases, the load and stop sequences are controlled through MPU programming that monitors whether start conditions are present and whether certain interlock and operating conditions are satisfactory. The following areas of the power functions will be discussed in detail:

- Power Distribution -- Describes how power is distributed to the drive circuitry.
- Power On Initialization -- Describes how the drive circuitry is initialized when power is applied and how the drive is prepared for normal operation.
- Local/Remote Power Sequencing -- Explains how the spindle may be powered up either at the drive or by the controller.
- Retract Sequence -- Describes how the drive is powered down, including retracting the heads and stopping the disk rotation.

POWER DISTRIBUTION

The power supply provides the drive with basic dc supply voltages when circuit breaker CB1 is placed in the ON position. All drive circuitry, except the cooling fan and drive motor, is operated with the dc supply voltages. The ac power cable connects the power supply (through CB1) to site ac power. The power supply can be conditioned for operation with any standard ac input voltage, as described in the Installation and Checkout section of Hardware Maintenance Manual, Volume 1.

The dc power supply provides four basic dc supply voltages to the drive electronics. These voltages are +5 V, -5 V, +24 V, and -24 V. The dc power supplies are protected against overload by circuit breaker CB1 on the power supply. In addition, the $\pm$5 V dc regulators are separately protected against over voltage and over current conditions. Overvoltage causes circuit breaker CB1 to open when the voltage exceeds 6.2 $\pm$ 0.5. The overcurrent foldback circuitry limits the +5 volt supply to 15 amperes, and the -5 volt supply to 7 amperes. The $\pm$24 volt dc voltages are separately protected against an overload by CB2.

There are secondary regulators on the drive's Control Board that develop additional bias voltages for certain integrated circuits. One regulator steps down the +24 V input and develops a regulated +15 V source. Another regulator steps down the -24 V input and develops a regulated -15 V source. A third regulator steps down the -15 V regulated dc power to develop a regulated bias of -8.3 V for the servo preamp chip.

The drive has circuitry that monitors the various supply voltages and disables write and/or servo functions when dc power is unreliable. For more information about voltage faults, refer to the Fault and Error Conditions discussion.

POWER ON INITIALIZATION

Power on initialization occurs when ac power is applied to the drive. Following successful initialization, a load operation occurs each time that start conditions become available. Figure 1-2 is a simplified diagram of the power on circuitry, and figure 1-3 is a flowchart of the sequence. The following paragraphs describe power on initialization in detail and summarize the load operation. More information about load operations is given under Seek Functions.

Placing power supply circuit breaker CB1 ON enables dc power to the drive. A level detector on the Control Board monitors the +5 Vdc input from the power supply and drives the -Low Vcc line high when the +5 Vdc increases to +4.9 V. Until this time, the DC Master Clear latch is set, and its output, the -DC Master Clear signal, remains low. In the Sector Counter Gate Array, the -DC Master Clear signal resets the sector counter. In addi- tion, the -DC Master Clear signal disables the interface by blocking unit selection, and the remote power sequencing cir- cuitry. In dual channel drives, the -DC Master Clear signal blocks unit selection by either controller.

The -MPU Reset line to the MPU goes low when -DC Master Clear goes low, and it is held low by a one-shot for about 3 ms after the -Low Vcc line goes high. When -MPU Reset goes high, the MPU performs three self-test operations to initialize itself. These tests are as follows:

- The MPU performs a checksum calculation on the ROM contents. This test validates that the MPU's firmware instructions are readable.
- The MPU tests its internal RAM by writing information into it and reading it back.
- The MPU initializes its PIAs by sending data to them and reading it back.

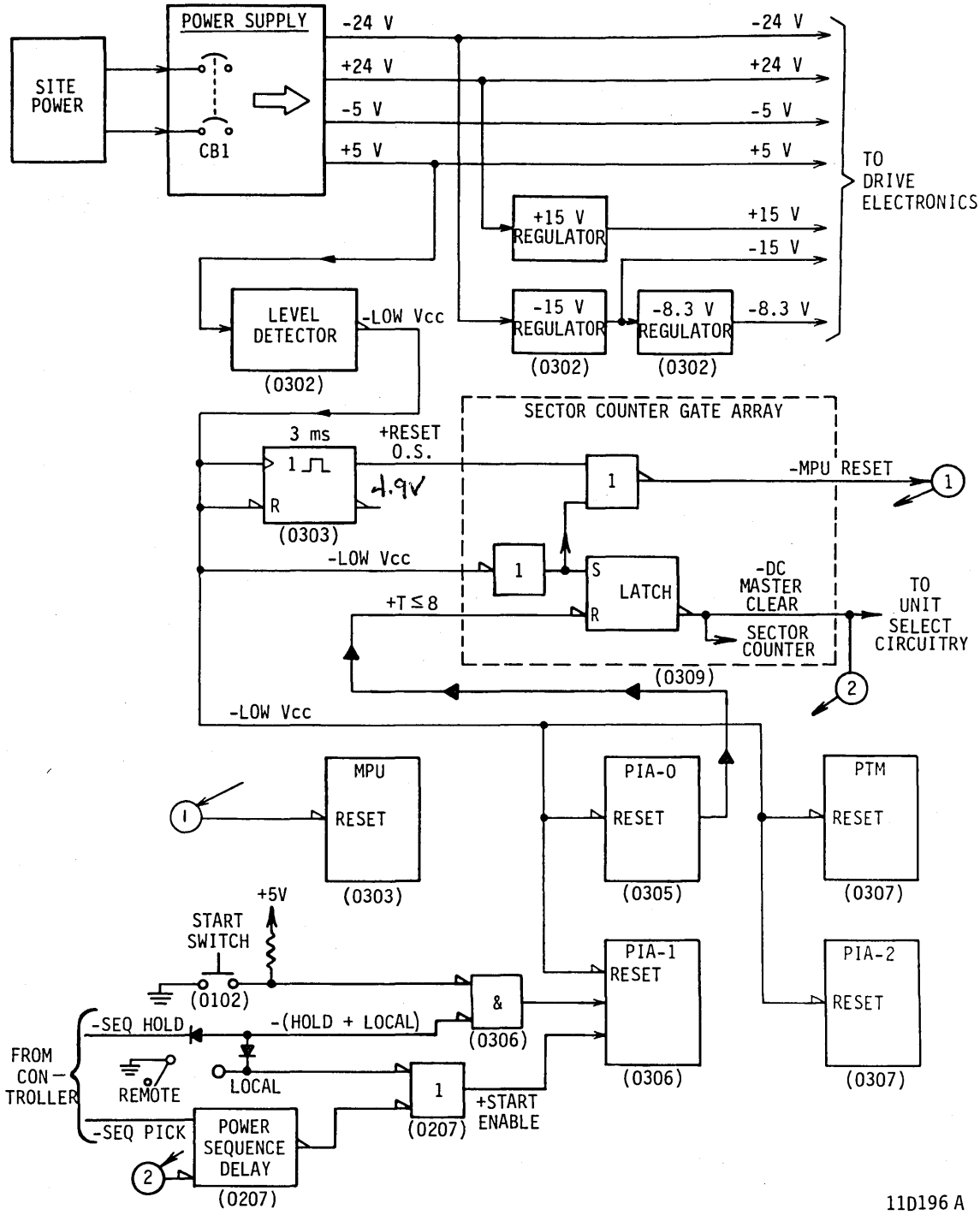


Figure 1-2. Power On Circuitry

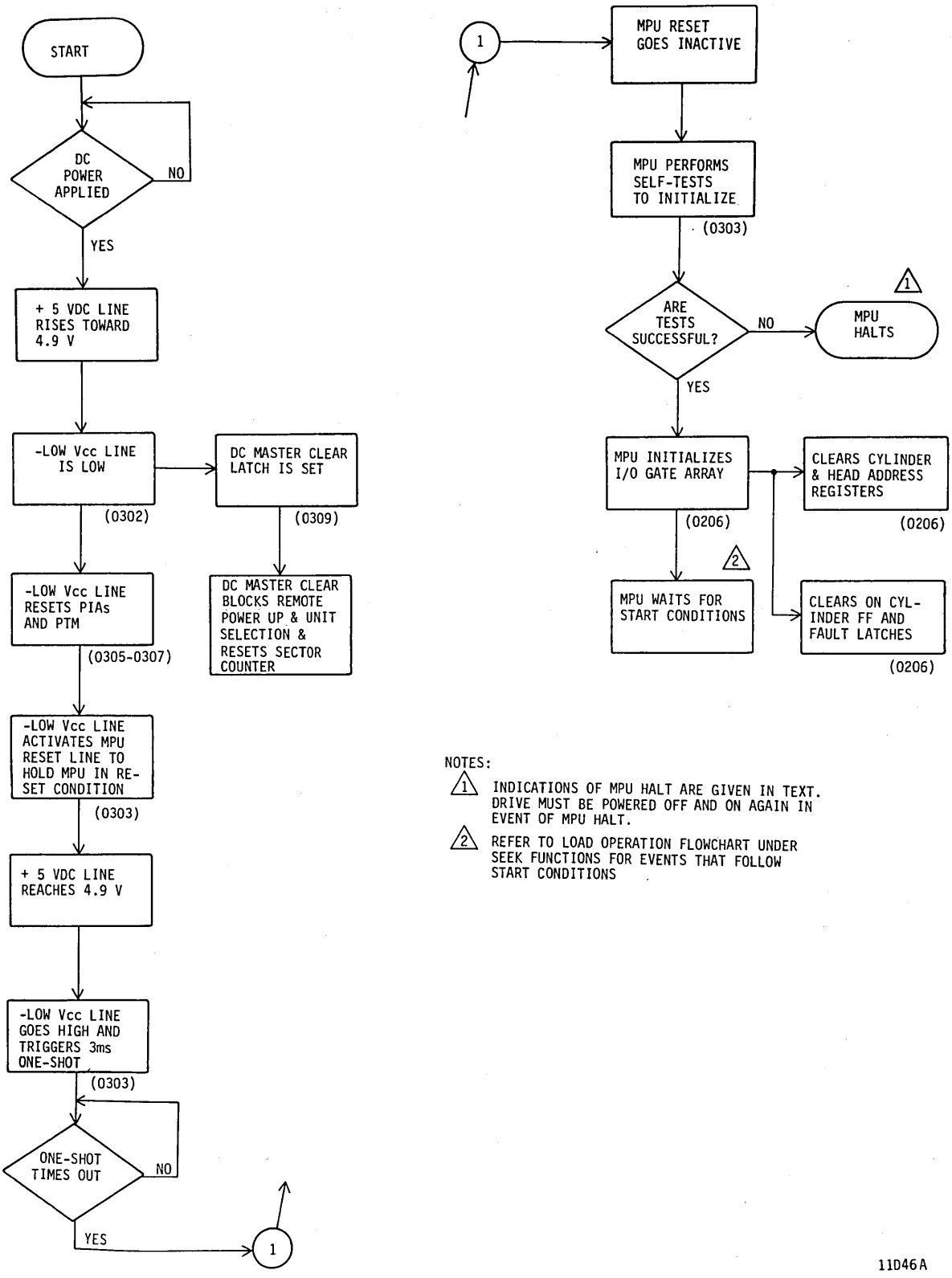


Figure 1-3. Power On Initialization Flowchart

If the first two tests fail, the MPU halts and all the individual fault LEDs on the Fault Display Board remain lit. If the third test fails, the MPU tries to light the First Seek LED and halts. None of these tests can produce an operator panel FAULT indication, and there is no way to clear these faults except by turning CB1 OFF.

With the self-tests complete, the MPU initializes the circuitry within the I/O Gate Array. The MPU communicates with the I/O Gate Array via I/O Control lines 1, 2, and 3. The MPU pulses I/O Control lines 1 and 2 with a serial code that clears the Cylinder Address register (CAR), the Head Address register (HAR), the On Cylinder FF, and the Fault latches.

At this point, power on initialization is complete. This process will not be repeated until dc power is removed and reapplied to the drive. The MPU waits for start conditions by monitoring the START switch and (in remote operation) the Sequence Hold and Sequence Pick signals from the controller.

When start conditions are present, the MPU directs the load operation. The load operation energizes the drive motor to bring the disks up to speed and loads the heads to position them over the disks at track 0. Details of the load operation are given under Seek Functions. When the load operation is complete, the drive waits for commands from the controller.

LOCAL/REMOTE POWER SEQUENCING

The local/remote feature selects whether or not the controller can control starting and stopping the drive motor. Part of drive installation is setting the LOCAL/REMOTE switch (on the drive I/O Board) for either local or remote operation. The LOCAL/REMOTE switch setting determines start conditions for the drive motor during a load operation. With the LOCAL/REMOTE switch in LOCAL, start conditions require only that the START switch is in the On position. With the LOCAL/REMOTE switch in REMOTE, start conditions require that the START switch is in the On position and that the controller has activated the Sequence Hold and Sequence Pick signals.

In a system of several drives set up for remote operation, all drives receive Sequence Hold and Sequence Pick at the same time. Once Sequence Pick is received, a delay circuit in the I/O circuitry activates +Start Enable after an interval equal to five seconds multiplied by the drive address. Thus, each drive in the system has a unique start-up interval. However, when Sequence Hold goes inactive, it causes all drives to stop their drive motors at the same time.

RETRACT AND STOP SEQUENCE

The retract and stop sequence retracts the heads and stops the drive motor. There are two conditions that initiate a retract and stop sequence. One is a loss of start conditions, and the other is a loss of ac power to the drive. Both conditions produce retract operations: the first, a normal retract; and the second, an emergency retract. These retract operations are discussed in detail under Seek Functions. The drive motor comes to a stop after the retract is completed.

A loss of start conditions occurs when the START switch is pressed to release it from the Start position or (in remote operation) when the controller deactivates Sequence Hold. The MPU monitors the start conditions and commands a retract when they are removed. The retract operation (discussed under Seek Functions) uses servo control to move the heads completely outward over the landing zone. The heads are held in this position by a retract command until the actuator unlocking solenoid is released, locking the heads in the retracted position. The MPU then drops the Motor Run command to disable the Motor Relay, and friction braking stops the drive motor. The drive remains in this condition until start conditions reappear.

A loss of ac power results when power supply circuit breaker CB1 is switched OFF or when there is a loss of site ac power. When the dc voltages drop, an emergency retract takes place. The emergency retract operation requires no MPU intervention, and it uses the voltage generated by the Retract Capacitor to drive the heads outward to the landing zone. The actuator unlocking solenoid assists the Retract Capacitor in retracting the carriage, and then holding the carriage in the retracted position. With a loss of ac power, the drive motor is stopped by the friction brake.

ELECTROMECHANICAL FUNCTIONS

GENERAL

Certain drive functions are performed by electromechanical components. These functions include disk rotation, head positioning, and drive cooling and ventilation. Disk rotation and head positioning are controlled by the drive logic circuitry. Drive cooling and ventilation is controlled by power supply circuitry.

DISK ROTATION

General

Disk rotation is accomplished by an electromechanical system that accelerates the disks to 2160 r/min during a load operation and stops disk rotation with friction braking during a retract and stop operation. The mechanical and electrical aspects of this system are discussed in the following paragraphs.

Mechanical Description

The electromechanical components used to perform disk rotation and control are the spindle, the drive motor and belt, and the friction brake.

Spindle

The disks are mounted on the spindle assembly. The spindle like the disks, is part of the module. When the spindle is rotated by the drive motor, the disks rotate with the spindle.

Drive Motor and Belt

The drive motor rotates the disks in the module using a belt and pulley arrangement. Spring tension is used to maintain uniform belt pressure between the motor mounting plate and the pulley mounted on the module spindle. Refer to figure 1-4.

Friction Brake

The brake mounts on the top of the motor. Its purpose is to stop the motor within 6.5 seconds of the start of the retract and stop sequence.

The brake consists of an electromagnet and a clutch mechanism as shown in figure 1-4. The motor shaft passes through the center of the electromagnet and couples to the friction part of the clutch.

The electromagnet is energized at the start of a load sequence. Energizing the electromagnet pulls the top clutch plate away from the hexagonal collar mounted on the motor shaft, allowing the friction disk to rotate freely.

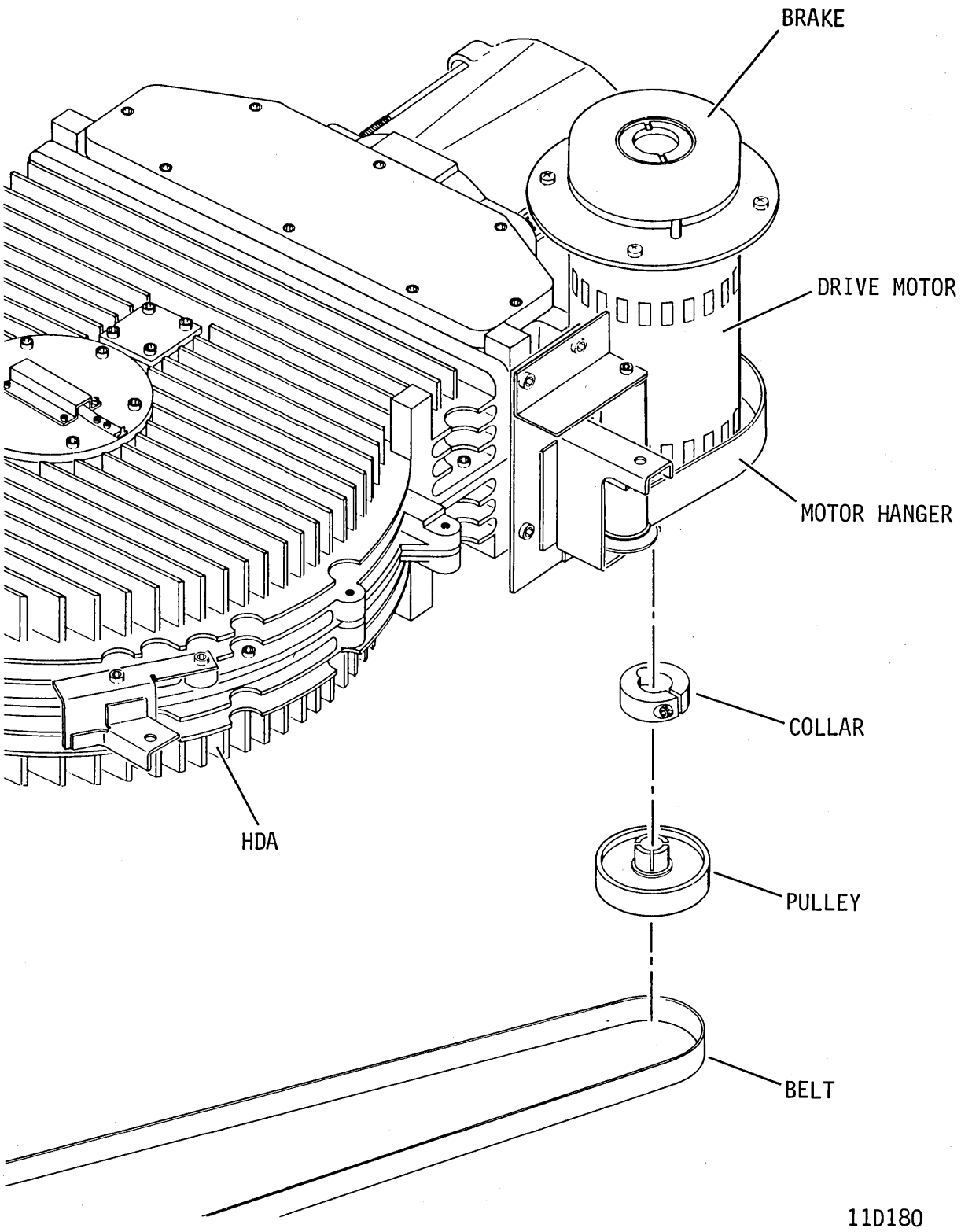


Figure 1-4. Module Assembly

During the retract and stop sequence, the microprogram deenergizes the electromagnet at the same time as the motor. With the electromagnet deenergized, the braking springs push the upper clutch plate downward, squeezing the friction disk between the clutch plates. Because the friction disk couples directly to the motor shaft, the resulting drag on the friction plate causes the motor to decelerate. The motor speed detection circuitry activates the -Motor Sensor line to indicate that braking is complete. The flasher circuit then causes the Ready indicator to flash for 30 seconds and the MPU inhibits restart of the spindle motor for this period.

HEAD POSITIONING

General

Data is written on and read from the disk by the heads. The drive must position the heads over a specific data track before a read or write operation can be performed. Head positioning is performed by the actuator mechanism. The actuator is controlled by inputs received from the servo circuits (refer to the discussion on Seek Functions).

Actuator and Magnet Physical Description

The actuator (shown in figure 1-5) consists of the actuator housing, the carriage, the voice coil assembly, and the headarm assemblies. A single head-arm assembly consists of the arm, four read/write heads (or one servo head), and a preamp chip. The carriage assembly fits within and is provided with horizontal movement into/out of the permanent magnet by bearings riding along a carriage track. During head positioning, the carriage rides the track toward or away from the magnet and out over the disk surfaces.

Whenever the drive is in the stopped condition, the actuator is latched in the retracted position with the heads over the landing zone. The actuator remains locked until the next load sequence when the MPU activates the actuator unlocking solenoid. The automatic actuator locking feature eliminates the need to manually lock the actuator when transporting the drive.

Actuator and Magnet Functional Description

The voice coil is mounted on the carriage assembly and moves in and out of the magnet as the servo signals change. The magnet is mounted on the housing in a position which allows the voice coil to move as the field in the coil changes. This small in and out motion of the voice coil in the magnet provides the

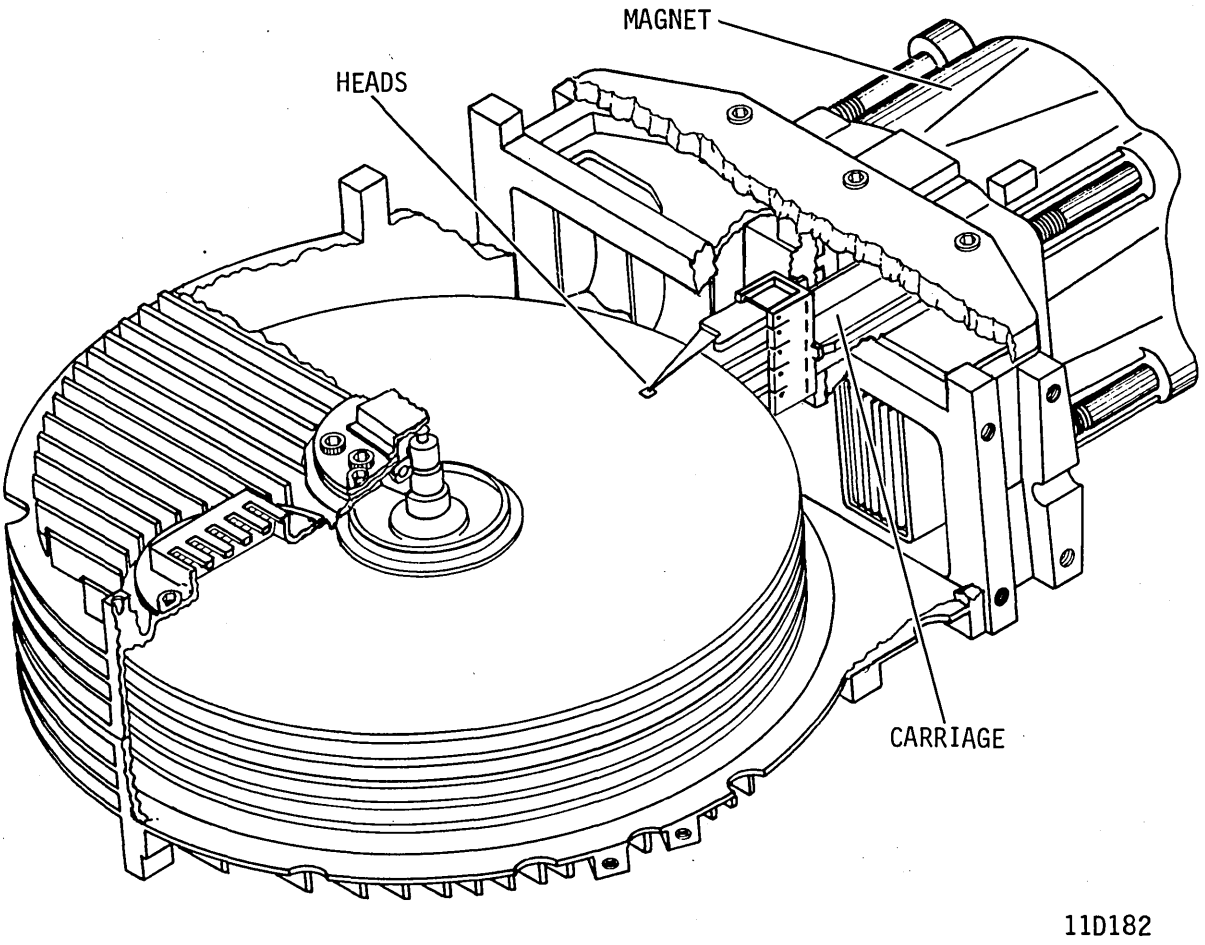


Figure 1-5. Actuator and Magnet Assembly

motion for the heads over the disk surface. The movement of the carriage (and therefore the heads) is controlled by positioning signals from the servo logic. The positioning signals are derived in the analog servo system and processed by the power amplifier. The output of the power amplifier is a current signal which is applied to the voice coil.

The current from the power amplifier causes a magnetic field in the voice coil which either aids or opposes the field around the permanent magnet. This reaction either draws the voice coil into the magnet or forces it away, depending on the polarity of the current through the voice coil. The acceleration of the voice coil is dependent on the amplitude of the voice coil current.

HEADS

General

The heads are magnetic devices that record data on, and read data from, the disk surface (the servo head, however, reads prerecorded data but cannot write). Each head is mounted at the end of a supporting arm. The head and arm together with the pre amp chip are called a head-arm assembly. The head-arm assemblies are attached to the front of the actuator assembly (figure 1-6).

The drive has 16 movable data heads and one servo head. The data (or read/write) heads are used to record data on and read data from the disk data surfaces. The servo head is used to read prerecorded data from the servo disk surface for use by the drive analog servo circuits.

The following paragraphs describe the physical characteristics of the movable head-arm assemblies and how they function during head load and retract sequences. Further information about the heads is found in the discussions on seek and read/write functions.

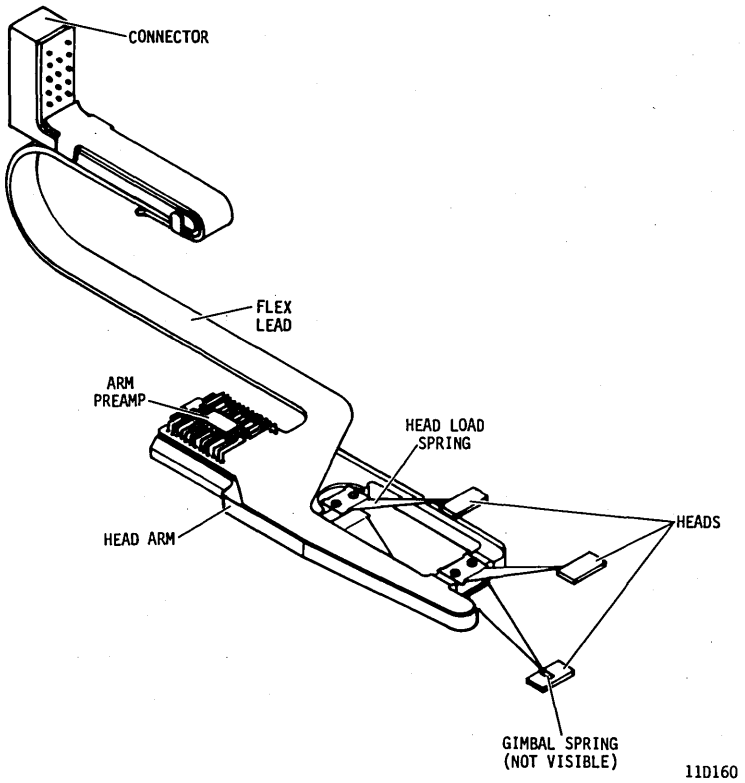


Figure 1-6. Data Heads

Head-Arm Assembly

Each read/write head-arm assembly consists of a rigid arm, supporting four heads on load springs and gimbal springs, and a preamp chip (figure 1-6). The servo head-arm supports a single head on load springs and gimbal springs, and a preamp chip. The head-arm assemblies are mounted at the front of the actuator carriage and follow the in/out motion of the carriage created by the reaction of the voice coil magnetic field to the field permanent magnet. The rigid arm by itself does not provide the action necessary for the heads to load or unload. The head load spring forces its associated head toward the disk surface; the gimbal spring allows the head free axial movement along its vertical and horizontal axes independent from the rigid arm.

Read/write information is transferred to and from the heads through cables connected to a preamp mounted on the arm. The read/write information is interfaced to the HDA interface board (__TSX card) mounted underneath the HDA. The HDA interface board, in turn, is interfaced to the Bulkhead board located inside the sealed module.

Head Loading

In the retract (non-operating) condition, the head load springs are forcing their respective heads against the disk surface in the landing zone. There are two landing zones on each data surface -- one for each head. At the extreme outward travel, the heads are located over their respective landing zones. When a load operation is per- formed, the program turns on the drive motor and actuates the carriage unlocking solenoid. When the drive motor is rotating the disks at acceptable speed, the heads move away from the disk surfaces and fly on the cushion of air created by disk ro- tation. At this point in the load sequence, the heads are moved inward to track zero. The heads continue to fly on the cushion of air until the spindle stops rotating.

The head load spring forces the head toward the disk surface, while the cushion of air pushes against the head to resist its closer approach. The air cushion pressure varies directly with disk speed, so that at proper speed the force of the head load spring pressing the head towards the disk surface and the opposing force of the air cushion resisting the closer approach of the head are balanced such that the heads fly at the correct height above the disk.

If the disk drops below speed, the air cushion pressure decreases and the head load springs force the heads closer to the disk surface. Sufficient loss of speed would cause the heads to stop flying and contact the disk. This is called head landing. Because insufficient disk speed causes head landing, heads are not moved into the data areas until the disks have come up to speed. For the same reason, the heads are retracted from the data surfaces when the speed drops below a safe operating level.

AIR FLOW SYSTEM

The air flow system is divided into two parts, one for the drive unit and the other for the sealed data pack.

The drive air flow system (figure 1-7) provides continuous air replacement and circulation to dissipate the heat generated by drive operation. The main component of the drive air flow system is the fan that is mounted on the rear panel of the power supply. The fan motor is driven by power from the ac section of the power supply. The fan pulls ambient air through the input and primary filter of the front panel. The air circulation travels over the electronics, cooling these assemblies before leaving the drive through the back panel. The system intake port is located on the front panel. This port is covered by the primary filter which keeps large particles from being drawn into the system.

The air flow system for the HDA is a self-contained closed loop system (figure 1-8). The rotation of the disks creates air circulation patterns within the HDA. The module contains two filters; an absolute filter located inside the module, and an external breather filter located on the top of the module.

If the pressure within the module becomes less than the surrounding atmosphere, make up air enters through the breather filter to equalize the pressure. Likewise, if the module pressure exceeds atmospheric pressure, air leaves the module through the breather filter.

INTERFACE

General

All communications between drive and controller must pass through the interface. This communication includes all commands, status, control signals, and read/write data transfers. The interface consists of the I/O cables and the logic required to process the signals sent between drive and controller.

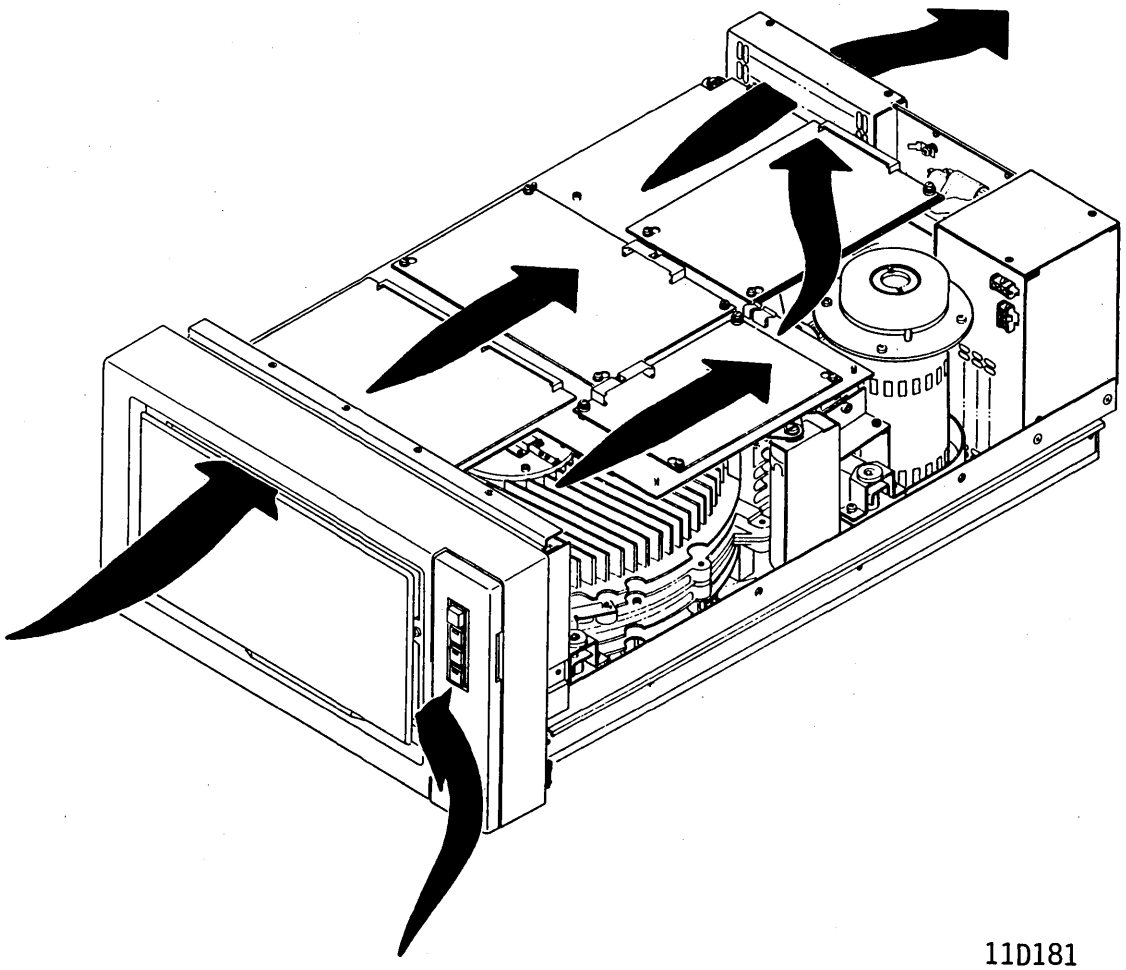


Figure 1-7. Drive Air Flow System

The following discussion describes both the I/O cables and I/O signal processing.

I/O CABLES

The drive has two I/O cables per channel, consisting of an A cable and a B cable. These cables contain all the lines going between the drive and controller.

The A cable carries commands and control information to the drive and status information to the controller.

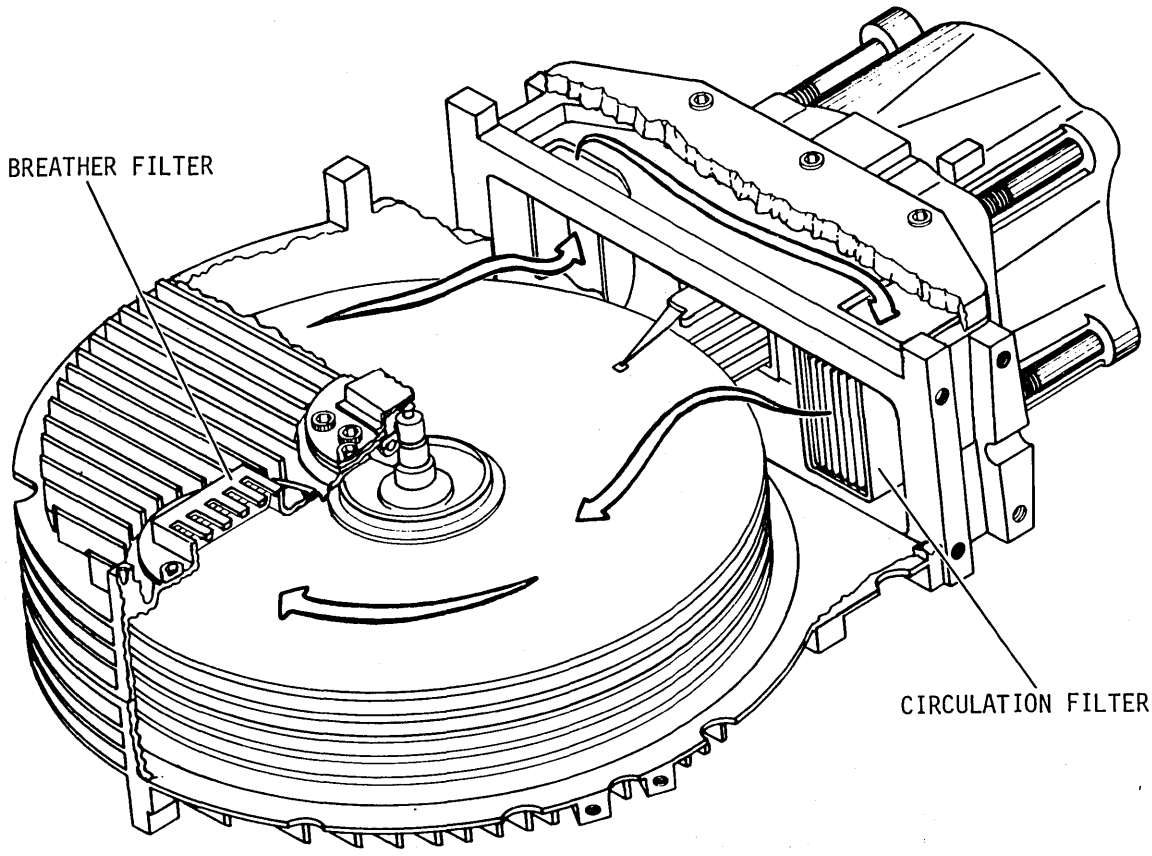


Figure 1-8. Module Component and Air Flow

The B cable carries read/write data, clock, and status information between drive and controller. Figure 1-9 shows all lines (except those not used) in the A and B cables. The functions of each of these lines is explained in table 1-1.

I/O SIGNAL PROCESSING

I/O signals from the controller initiate and control all drive operations except local power on. The I/O signals are sent to receivers in the drive and are routed from the receivers to the appropriate drive logic. The drive in turn sends information concerning the operation back to the controller via the drivers. Figure 1-10 shows the basic logic involved in the routing of the I/O signals.

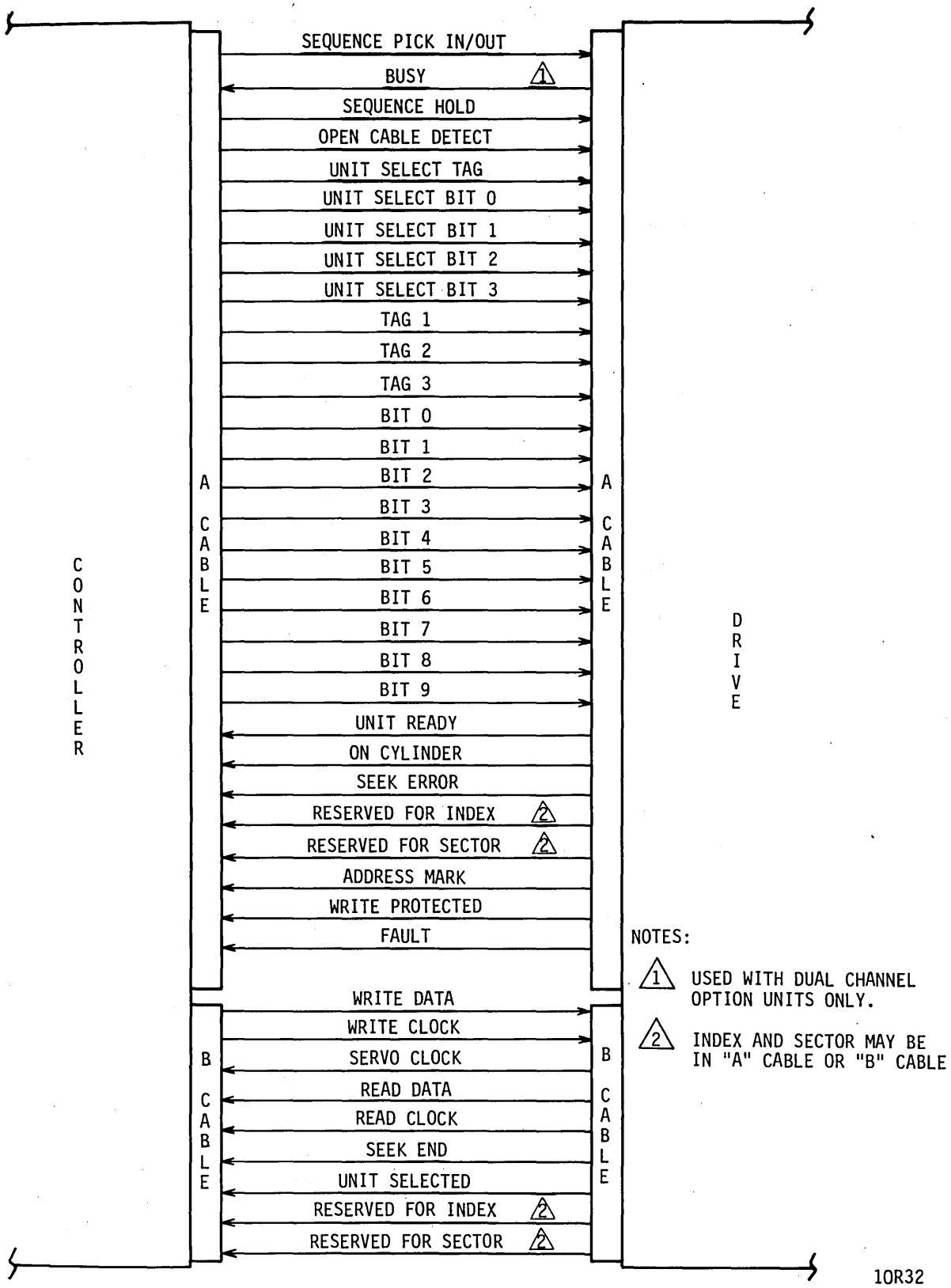


Figure 1-9. Interface Lines

Certain I/O signals cannot be transmitted or received unless the drive is selected. These signals include the tag and bus bit signals from the controller and the status bits to the controller.

All commands (except unit select) are sent to the drive via the tag and bus bit lines. The tag lines define the basic operation to be performed and the bus bits further define and modify the basic operation. Table 1-1 explains the functions of all tag and bus lines.

TABLE 1-1. INTERFACE LINES

Signal	Meaning
Function: Power Up Sequencing	
Sequence Pick	A ground from the controller on this line and the Sequence Hold line starts the power on cycle when the drive's LOCAL/REMOTE switch is in the REMOTE (REM) position, provided that the START switch has been pressed and the Sequence Hold line is active from the controller. Sequence Pick triggers a delay circuit that delays the power on sequence for an interval based on the drive address.
Sequence Hold	A ground from the controller on this line holds the drives in a power on condition provided the START switch is on when operating the drive in the Remote mode (LOCAL/REMOTE switch in the REMOTE position). Removing the ground from this line powers down all operating drives in the system.
Table Continued on Next Page	

TABLE 1-1. INTERFACE LINES (Contd)

Signal	Meaning
Function: Controller Selecting Drive	
Unit Select Tag	This signal gates Unit Select lines into the logical number compare circuit. Unit is selected after 600 ns (maximum) internal time lapse. Drive will not process commands until selected. When the Unit Select Tag is accompanied by the proper logical address and Bus Bit 9 active, this indicates a priority select status in dual channel systems. The drive is unconditionally selected and reserved by the channel issuing this command provided that this channel has not been disabled.
Unit Select Bits 0, 1, 2, and 3	A binary code is placed on these four lines to select a drive. The binary code must match the logical address of the drive determined by the logical address plug inserted in the operator panel. Drives can be numbered 0 through 7. Bit 3 must be inactive for a unit selection to occur.
Unit Selected	This signal indicates the drive has accepted a Unit Select request. This line must be active before the drive will respond to any command from the controller.
Open Cable Detect	A voltage is supplied by the controller to override the bias voltage at the drive receiver. If the A cable is disconnected or if controller power is lost, unit selection and/or controller commands are inhibited.
Table Continued on Next Page	

TABLE 1-1. INTERFACE LINES (Contd)

Signal	Meaning
Function: Drive Indicates Operational Status	
Unit Ready	Unit Ready indicates that the drive is up to speed, that the first seek was successful, and that no fault condition exists.
Index	This signal is derived from the servo tracks. It occurs once per revolution of the disk, and its leading edge is the leading edge of sector zero.
Sector	This signal is derived from the servo tracks. The number of sector signals that occur for each revolution of the disk is selected by switches on the Control board.
Busy	Used only in dual channel drives, this signal is generated when a controller attempts to select a drive that has already been selected and/or reserved by the other controller. This signal is sent to the controller attempting the selection.
Write Protected	This signal indicates that the drive write circuits are disabled. The write protect mode is enabled by a jumper on the Control board or by a switch on the operator panel, by a fault condition, or by a loss of motor speed. Attempting to write while the write protect mode is active results in a fault condition.

Table Continued on Next Page

TABLE 1-1. INTERFACE LINES (Contd)

Signal	Meaning
On Cylinder	This signal indicates that the servo head is positioned at a track. This line goes inactive if the positioner drifts off cylinder. The status is cleared with any seek instruction causing carriage movement, or a zero-track seek. A carriage offset command causes a loss of on cylinder for a period of 2.75 milliseconds nominal. A zero-track seek causes On Cylinder to drop for 30 microseconds nominal.
Seek End	This signal indicates either an on cylinder status or seek error status resulting from a seek operation that has terminated.
Seek Error	This signal indicates that the drive was unable to complete a seek within 500 ms or that the positioner has moved outside the recording field. The seek error can be cleared by an RTZ command or by a power up operation.
Fault	When this line is active, it indicates that one or more of the following faults exist: • First Seek fault • DC voltage fault • Write fault • Write or read attempted while off cylinder

Table Continued on Next Page

TABLE 1-1. INTERFACE LINES (Contd)

Signal	Meaning
Fault (Contd)	• Write gate during a read operation or Read Gate during a write operation • Head Select fault
Address Mark Found	When an address mark has been found, this line goes high.
Function: Controller Sends Commands to Drive	
Bits 0 through 9 (Bus Lines)	These ten lines carry data to the drive. The meaning of the data is a function of the active tag line.
Tag 1 (Cylinder Select)	This tag line gates the data on the bus lines to the drive Cylinder Address register. The bus bits have the significance listed below. Bus bits 0-9, with the value shown below, encode the cylinder address for the seek operation. Bus Bit — Function 0 — Cylinder Address 2^0 1 — Cylinder Address 2^1 2 — Cylinder Address 2^2 3 — Cylinder Address 2^3 4 — Cylinder Address 2^4 5 — Cylinder Address 2^5 6 — Cylinder Address 2^6 7 — Cylinder Address 2^7 8 — Cylinder Address 2^8 9 — Cylinder Address 2^9
Table Continued on Next Page	

TABLE 1-1. INTERFACE LINES (Contd)

Signal	Meaning
Tag 2 (Head Select)	This tag line gates the data on the bus lines to the drive Head Address register. The bus bits have the significance listed below. Bus Bit — Function 0 — Head Address 2^0 1 — Head Address 2^1 2 — Head Address 2^2 3 — Head Address 2^3
Tag 3 (Control Select)	This tag line gates the data on the bus lines to the logic circuits of the drive for commanding various operations. The operation performed is dependent upon which of the bus lines is active. The significance of the bus bits is as follows: Bus Bit — Name — Function Performed 0 — Write Gate — Enables write driver. Not accepted if there is a seek error or fault status. 1 — Read Gate — Enables read circuitry. Leading edge triggers the read chain circuit to synchronize on an all zeros pattern. Not accepted if there is a seek error or fault status.
Table Continued on Next Page	

TABLE 1-1. INTERFACE LINES (Contd)

Signal	Meaning
Tag 3 (Contd)	Bus Bit / Name / Function Performed 2 Servo Offset Plus — Offsets the positioner 75 microinches toward the spindle from the on cylinder position. Disables On Cylinder for 2.75 ms. 3 Servo Offset Minus — Offsets the positioner 75 microinches away from the spindle from the on cylinder position. Disables On Cylinder for 2.75 ms. 4 Fault Clear — A pulse sent to the drive that clears the Fault flip-flop provided that the fault condition no longer exists. 5 Address Mark Enable — When this signal occurs with a Write Gate, an address mark is written. When this signal occurs with a Read gate, an address mark search is initiated.

Table Continued on Next Page

TABLE 1-1. INTERFACE LINES (Contd)

Signal	Meaning
Tag 3 (Contd)	Bus Bit / Name / Function Performed 6 RTZ — A pulse sent to the drive to move the positioner to track zero. It also resets the Head Address register, Cylinder Address register, and Seek Error flip-flop. 7 Data Strobe Early — Enables the read comparator to strobe the data at a time earlier than nominal. 8 Data Strobe Late — Enables the read comparator to strobe the data at a time later than nominal. 9 Release — Used with dual channel option only, it clears channel reserved and channel priority select reserve status. (Refer to Unit Selection discussion).
Functions: Read, Write, and Clocks	
Read Data	This line transmits data recovered from the disk. This data is transmitted in NRZ form to the controller.
Table Continued on Next Page	

TABLE 1-1. INTERFACE LINES (Contd)

Signal	Meaning
Read Clock	This clock is derived from, and is synchronous with, the detected data. Read Clock defines the beginning of a data cell and is transmitted continuously.
Write Data	This line transmits NRZ data from the controller to the drive for recording on the disk surface with 2-7 encoding.
Write Clock	This clock is the Servo Clock retransmitted to the drive during a write operation. Write Clock must be synchronized to the NRZ data and must be transmitted 250 ns prior to Write Enable.
Servo Clock	Servo Clock is a phase-locked 14.52 MHz signal generated from the servo track tribits. Servo Clock is continuously transmitted.

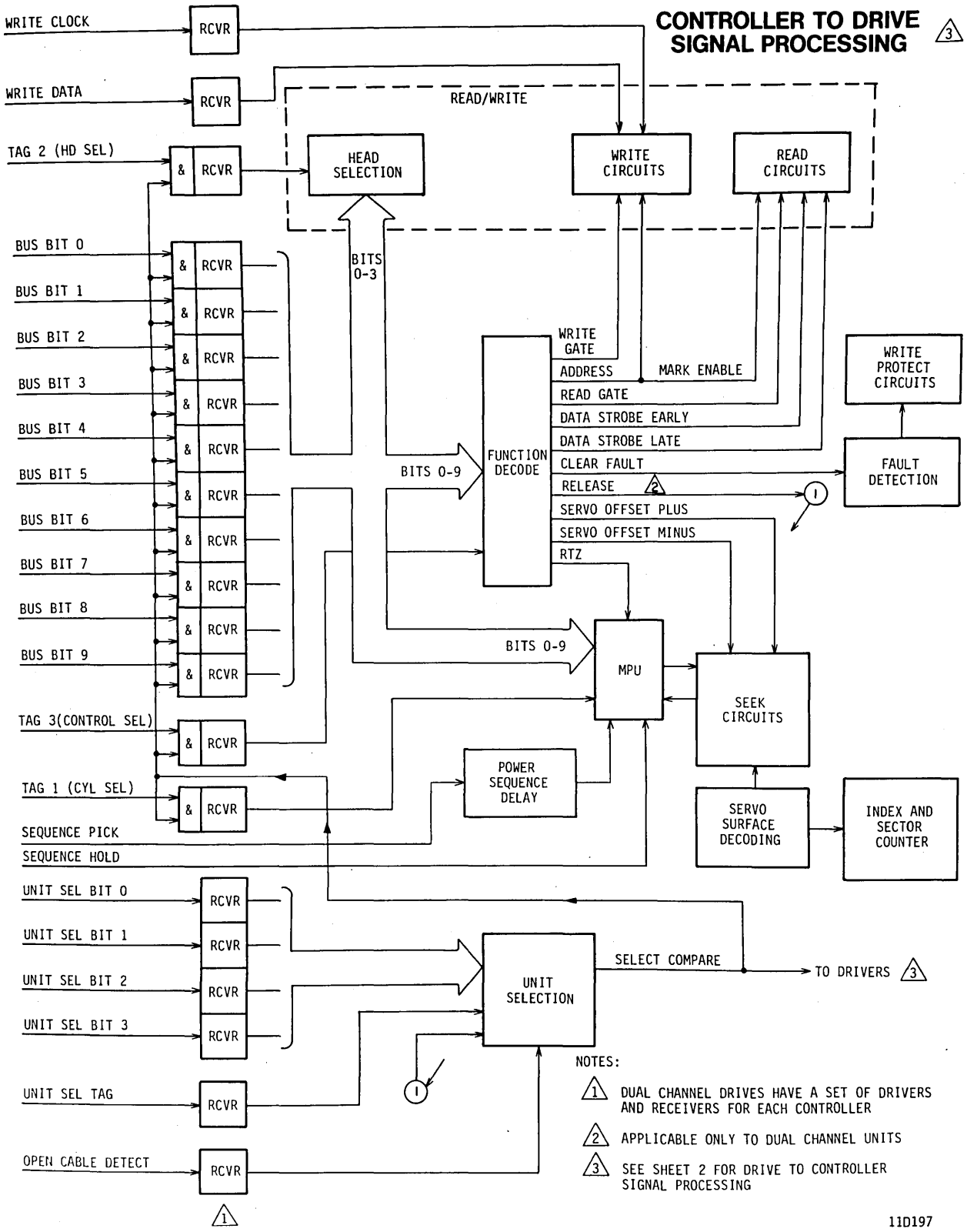
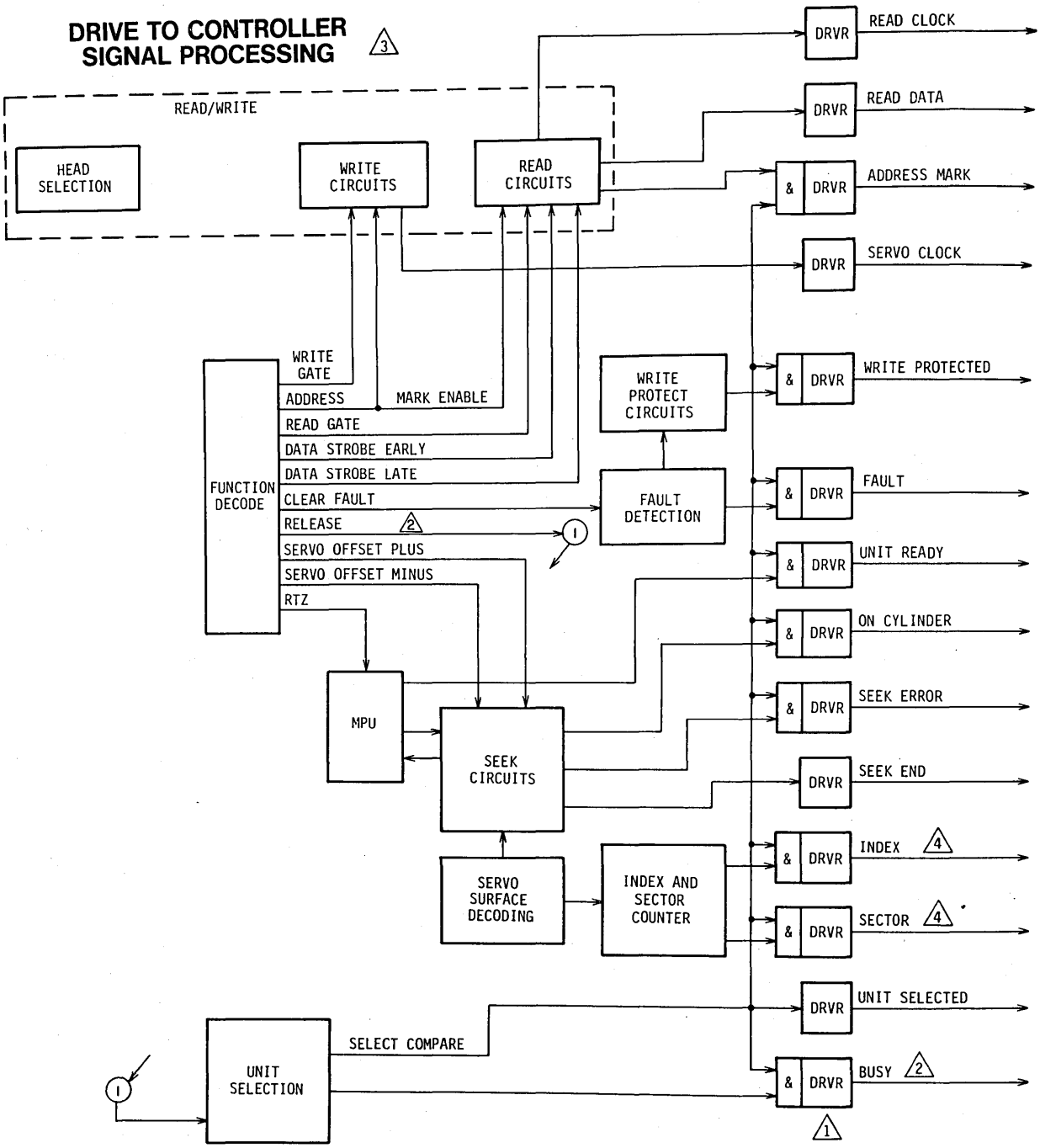


Figure 1-10. I/O Signal Processing (Sheet 1 of 2)



NOTES:

1. DUAL CHANNEL DRIVES HAVE A SET OF DRIVERS AND RECEIVERS FOR EACH CONTROLLER
2. APPLICABLE ONLY TO DUAL CHANNEL UNITS
3. SEE SHEET 1 FOR CONTROLLER TO DRIVE SIGNAL PROCESSING
4. INDEX AND SECTOR SIGNALS ARE SENT CONTINUOUSLY WHEN INDEX/SECTOR JUMPER PLUG IS IN "B" POSITION

11D53-2

Figure 1-10. I/O Signal Processing (Sheet 2)

UNIT SELECTION

GENERAL

The drive must be selected before it will respond to any commands from the controller. This is the case because the tag and bus bit receivers, as well as certain drivers, are not enabled until the drive is selected.

In both single and dual channel units, the select sequence is initiated by a Unit Select Tag signal from the controller. However, the sequence performed is different depending on whether a single or dual channel is being considered. Since only one controller can communicate with the drive at a time, dual channel logic must solve the problem of priority when more than one controller wants to select the drive at the same time. The following paragraphs describe both single and dual channel selection.

SINGLE CHANNEL UNIT SELECTION

The single channel unit select sequence (see figure 1-11) starts when the controller sends the Unit Select Tag accompanied by a logical address on the four unit select lines.

When the drive recognizes the Unit Select Tag, it compares its own logical address (as indicated by the logical address plug) to the address sent by the controller. The drive's logical address is determined by the logical address plug which fits into the operator panel. Depending on the plug used, this address can be any number from 0 to 7. If no plug is used, the number is 7.

If the address sent by the controller is the same as that of the drive and the Open Cable Detect signal is active (indicating the A cable is connected and controller has power), the drive enables its Select Compare signal.

The Select Compare signal enables the receivers and drivers to the controller and also enables the Unit Selected signal. The drive is now ready to respond to further commands from the controller.

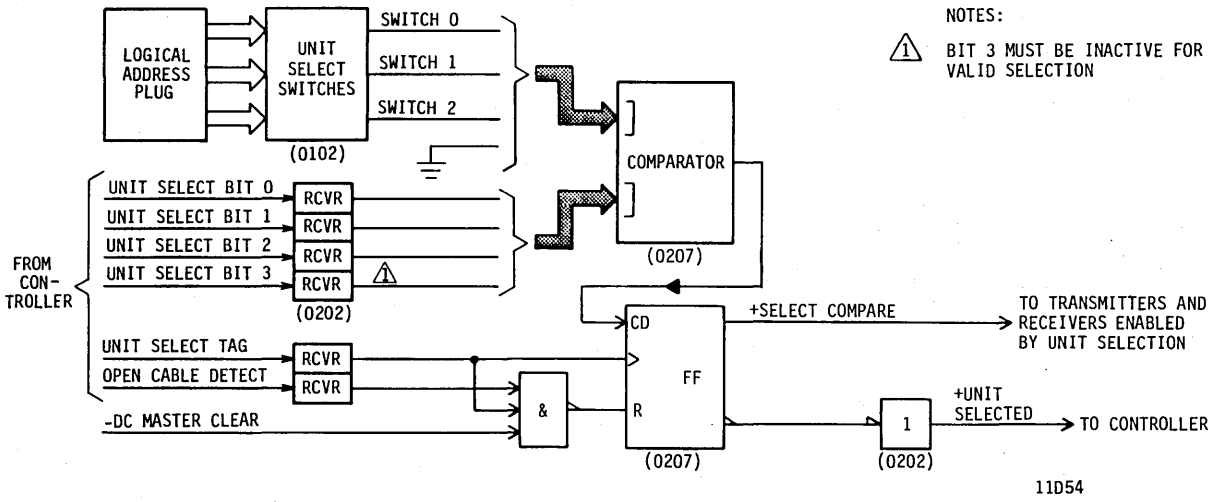


Figure 1-11. Unit Select Logic (Single Channel)

DUAL CHANNEL UNIT SELECTION

General

Dual channel drives are connected to, and can be selected by, either of two controllers. However, because the drive is capable of responding to only one controller at a time, the controllers must compete for use of the drive. For this reason, there are functions associated with dual channel selection that are not necessary when selecting single channel units.

The functions controlling dual channel selection are as follows:

- Select - Logically connects the drive to the controller, thus enabling it to respond to commands from the selecting controller.
- Reserve - Reserves the drive so it can be selected at any time by the reserving controller, but prevents it from being selected by the other controller.

- Release - Releases drive from reserved condition.

- Priority Select - Allows controller to force select the drive by disabling the interface to the controller having the drive selected or reserved.

- Maintenance Disable - Allows disabling either channel interface during maintenance.

The following discussions describe each of these functions. It should be noted that because these functions are basically the same regardless of which channel is involved, they are described only as they relate to Channel I. Figure 1-12 shows the select logic associated with channel I selection and table 1-2 describes the major elements on this figure. Figure 1-13 is a flowchart of the dual channel unit select and reserve functions.

Select and Reserve Function

The drive is both selected and reserved during the same sequence and this sequence is initiated by a Unit Select Tag accompanied by a logical address. However, the drive can be successfully selected and reserved only if none of the following conditions exist:

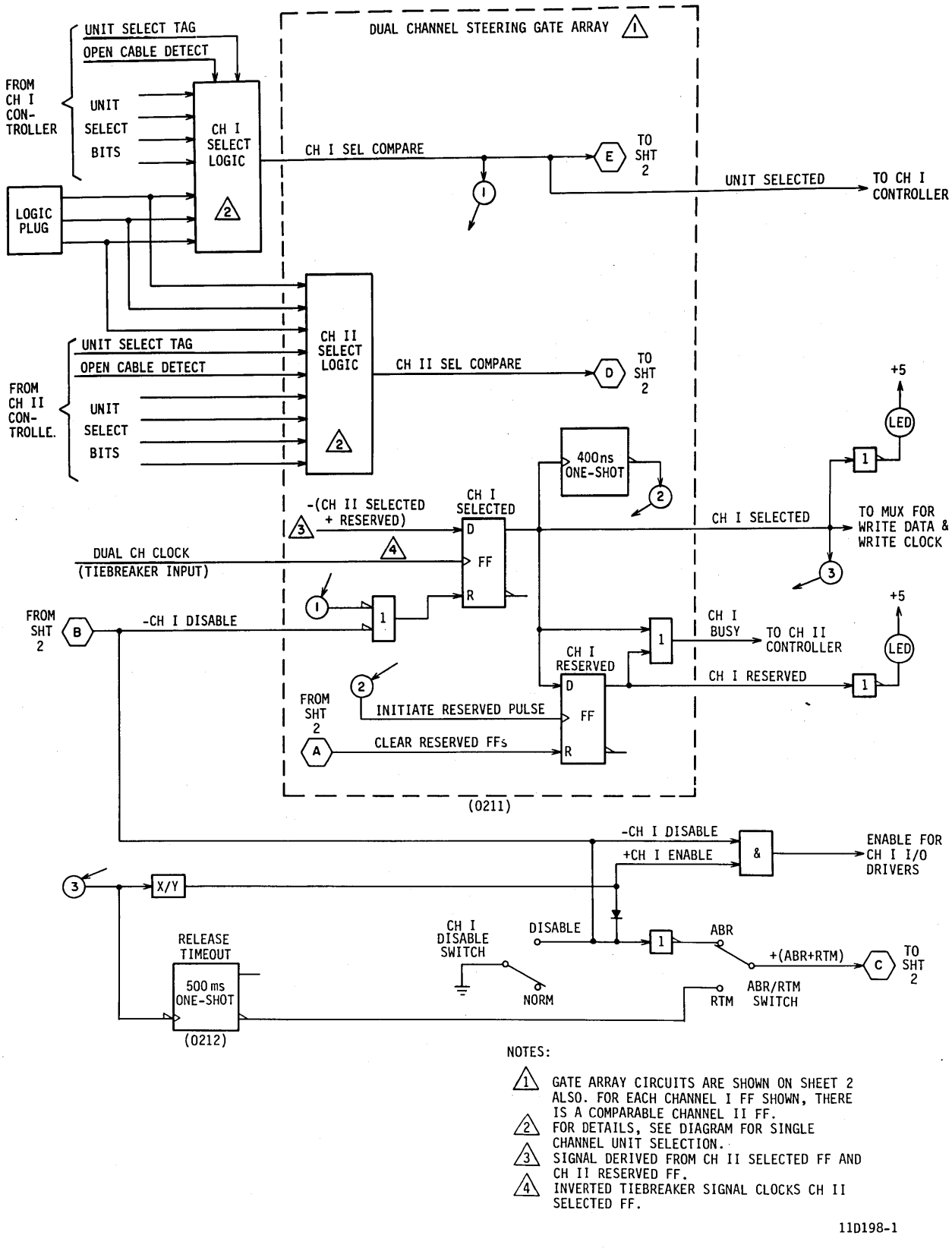
- Drive is already selected and reserved by other controller.

- Drive is not selected but is reserved by other controller.

- Channel to drive attempting selection has been disabled by either a priority or maintenance disable function.

The following paragraphs describe how the drive is initially selected and also how it responds to a Unit Select Tag when it is selected, reserved, or disabled.

Assuming the drive is available (not selected, reserved, or disabled) and it receives a Unit Select Tag and logical address from the controller on channel I, it compares the address received with that indicated by its logical address plug. If the two addresses are the same, the drive enables the Channel I Select Compare signal. The logic used to generate this signal is identical to that used in the single channel units (refer to figure 1-11).

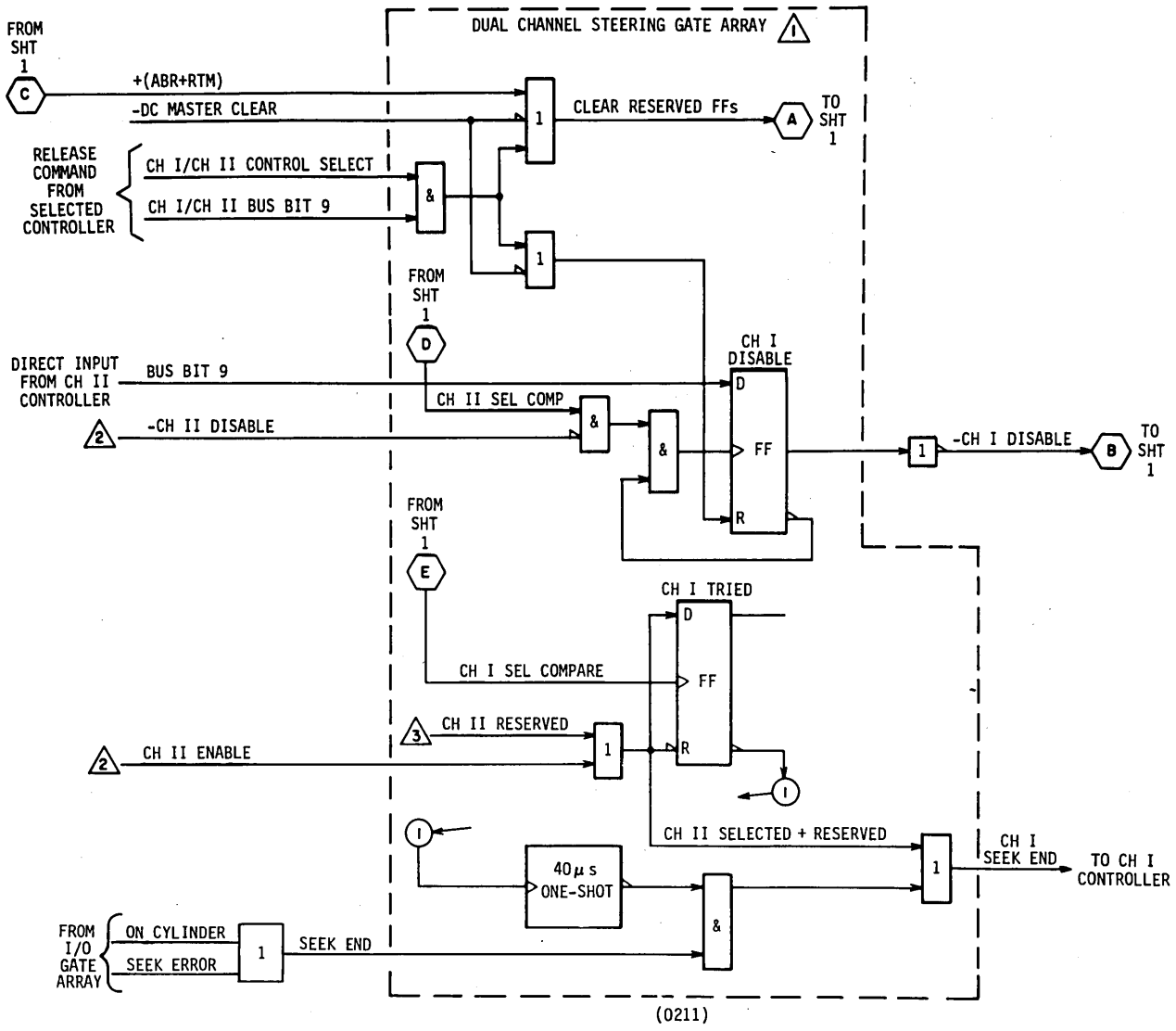


NOTES:

1. GATE ARRAY CIRCUITS ARE SHOWN ON SHEET 2 ALSO. FOR EACH CHANNEL I FF SHOWN, THERE IS A COMPARABLE CHANNEL II FF.
2. FOR DETAILS, SEE DIAGRAM FOR SINGLE CHANNEL UNIT SELECTION.
3. SIGNAL DERIVED FROM CH II SELECTED FF AND CH II RESERVED FF.
4. INVERTED TIEBREAKER SIGNAL CLOCKS CH II SELECTED FF.

11D198-1

Figure 1-12. Channel I Dual Channel Logic (Sheet 1 of 2)



NOTES:

1. GATE ARRAY CIRCUITS ARE SHOWN SHEET 1 ALSO. FOR EACH CHANNEL I FF SHOWN, THERE IS A COMPARABLE CHANNEL II FF.
2. SIGNALS DERIVED FROM CHANNEL II OUTPUTS OF GATE ARRAY.
3. SIGNAL DERIVED FROM CH II RESERVED FF.

11D198-2

Figure 1-12. Channel I Dual Channel Logic (Sheet 2)

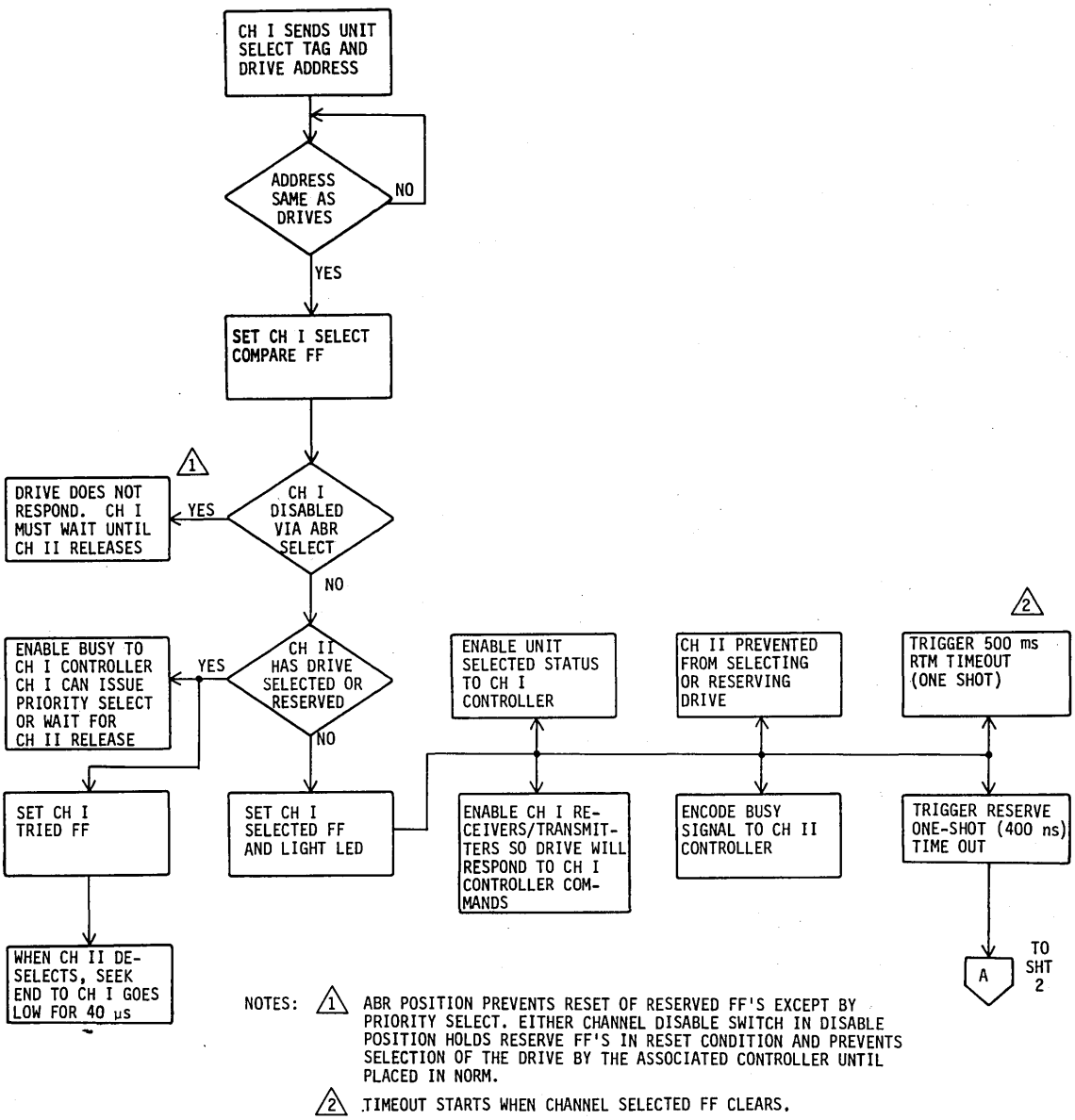


Figure 1-13. Dual Channel Selection Flowchart (Sheet 1 of 2)

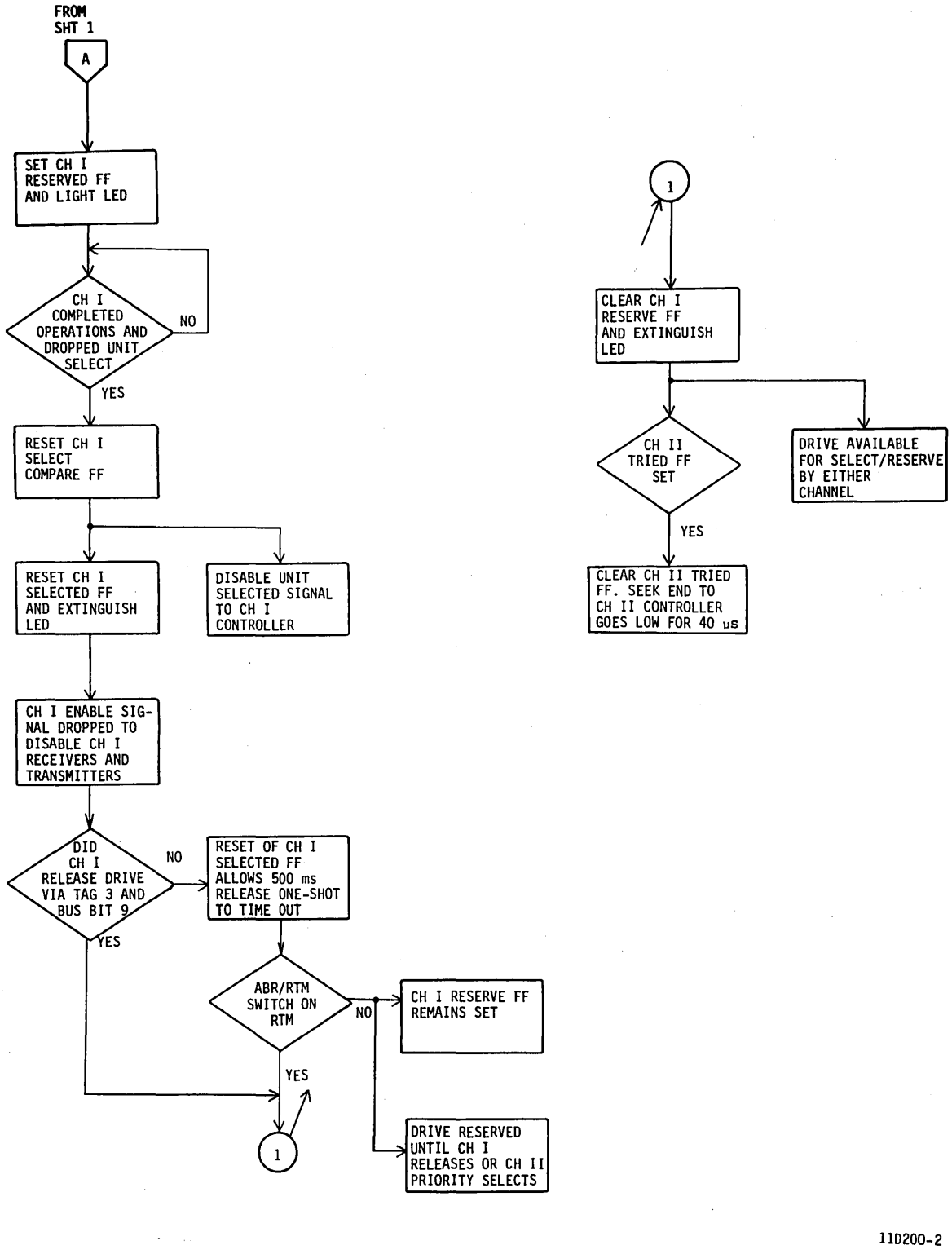


Figure 1-13. Dual Channel Selection Flowchart (Sheet 2)

TABLE 1-2. DUAL CHANNEL UNIT SELECT CIRCUIT FUNCTIONS

Element*	Function
ABR/RTM Switch	Determines whether the drive will be in ABR (absolute reserve) or RTM (reserve timeout) mode. If switch is in RTM position, drive is released from reserved condition 500 ms (nominal) after being deselected. If switch is in ABR position, drive remains reserved until it receives either a release or priority select command.
Release Timeout One Shot	Times out 500 ms after drive is deselected. If drive is in RTM mode, the reserved FF is cleared when timeout occurs.
Channel I Disable FF	Sets if drive receives Priority Select command. This causes drive to be selected and reserved for controller and disables channel to other controller.
Channel I Disable Switch	Disables channel I whenever it is set to disable position. It must be in NORM position during normal operations.
Channel I Reserved FF	Sets during select and reserve sequence. When set it keeps drive reserved to channel I until channel I releases or channel II issues a Priority Select command.
Channel I Selected FF**	Sets during select and reserve sequence and enables drivers and receivers to channel I controller.
Channel I Select and Compare Logic	Compares logical address of drive with that sent by controller (see Single Channel Unit Selection).

Table Continued on Next Page

TABLE 1-2. DUAL CHANNEL UNIT SELECT CIRCUIT FUNCTIONS (Contd)

Element*	Function
Initiate Reserved Pulse	Generates 400 ns pulse whenever Select Compare signal goes true. Leading edge of this pulse clocks Channel I and Channel II Reserve FF.
Channel I Select Tried FF	Sets if channel I tries to select and reserve drive while it is already selected and/or reserved by channel II. When drive is deselected and released by Channel II, this FF clears and thereby triggers the Select Tried one shot.
Select Tried One Shot	Generates 40 microsecond pulse whenever either Tried FF clears. This pulse is sent to controller (associated with the Channel Tried FF that triggered the one shot) via the Seek End line.

* Includes only those elements directly concerning channel I and shown in figure 1-12.

**The Channel Selected FF's are alternately clocked by the 14.52 MHz clock signal to prevent simultaneous selection.

The Select Compare signal causes the Channel I Selected FF to set, thereby enabling the receivers and drivers to the Channel I controller and triggering the Reserve one-shot. The output pulse from this one-shot clocks and sets the Channel I Reserved FF. With these FFs set, the drive sends Unit Selected to the channel I controller indicating that it is ready to accept further commands.

Providing channel II does not issue a priority select command (see Priority Select Function discussion), the drive remains selected to channel I until the controller on channel I drops its Unit Select Tag or changes the logical address to another drive. At this time, the drive's Channel I Selected FF clears, thus disabling the drive drivers and receivers for that channel. This also disables the Unit Selected signal thus informing the controller that the drive will no longer respond to

commands. However, the drive remains reserved to channel I (allowing channel I to reselect while preventing channel II from selecting) until the Channel I Reserve FF is also Clear. This is cleared by either a release or priority select function (refer to these discussions).

If channel I attempts to select and reserve the drive while it is selected and reserved by channel II, the Channel I Select Compare signal is still generated as during the initial select and reserve sequence. However, the Channel I Select and Reserve FFs do not set, and therefore the attempt is unsuccessful. The drive still sends the Channel I Unit Selected signal to the controller, but, in this case, it is accompanied by the Channel I Busy signal. The Busy signal indicates that the drive is being used by channel II.

The drive also sets its Channel I Tried FF, thus recording the unsuccessful attempt. When the drive is no longer selected or reserved by channel II, this FF clears, causing Seek End to the channel I controller to go low for 40 microseconds. This informs the controller that the drive is no longer selected or reserved.

If the channel I controller tries to select the drive while channel I is disabled (either by a priority select or maintenance disable function), the attempt is unsuccessful and no response is sent back to the channel I controller.

Release Function

The release function will release the drive from either a reserved or priority selected condition. There are two types of release functions:

- Timeout release pulse
- Release command

The timeout release pulse is capable of releasing the drive from the reserved condition only. This pulse is generated by the 500 ms Timeout Release one-shot and releases the drive by clearing the Reserve FF. The pulse is triggered when the drive is selected (Select FF sets) and times out 500 ms after the drive is deselected (Select FF clears).

Whether or not the one shot has any effect on the Release FF depends on the position of the ABR/RTM switch. If this switch is in the RTM (reserve timeout) position, the FF clears when the one-shot times out, thus making the drive available to the other channel. However, if this switch is in ABR (absolute reserve) position, the one-shot has no effect on the FF and the drive remains reserved.

A Release command will release the drive from both the reserved and priority selected conditions. This command is initiated by the reserving and/or priority selecting controller when it issues a Tag 3 (Control Select) with Bus Bit 9 active. This clears the Reserve and Disable FFs and allows the other controller to select the drive.

Priority Select Function

If the drive is selected and reserved, the other controller can force selection by issuing a Priority Select command (Unit Select Tag accompanied by drive logical address and Bus Bit 9). This command will disable the channel to the controller presently using the drive and also select and reserve the drive to the controller issuing the Priority Select command.

For example if channel I has the drive and channel II wants to select, channel II issues a Priority Select command. In this case, the command sets the Channel I Disable FF which in turn results in clearing the Channel I Selected and Reserved FFs. It also sets the Channel II Selected and Reserved FFs, thereby selecting and reserving the drive for channel II.

Once the Disable FF is set, that channel (in this case channel I) is disabled until the other controller (in this case channel II) issues a command to clear it.

Maintenance Disable Function

It is also possible to disable either channel by setting the Disable switch for that channel (refer to figure 1-12) to the disable position.

DRIVE SERVO SYSTEM

The drive writes data on and reads data from the disk data recording areas under the direction of the controller. These operations cannot be done randomly, however, for when the controller wishes to retrieve data, it must be able to find the exact location where that data has been stored. This problem is resolved by mapping the disks into discrete sections called "Tracks" which are narrow concentric bands that cover the entire circumference of the circle. The tracks are then further subdivided into equal areas called "Sectors".

After the controller has selected the unit with which it wishes to perform an operation, it must then direct the drive to the specific location on the data recording surface where it wants the operation to be performed. The operation of positioning the heads over the desired track is called a Seek operation. The drive servo system under the direction of the microprocessor unit (MPU) performs the Seek operation to position the heads by using information read from the servo surface by the servo head.

The eight recording surfaces on the disks are divided into two data bands each containing 1024 tracks sequentially numbered from zero on the outer edge of the band to 1023 on the inner edge of the band. The controller selects a track and a recording surface.

Each track is subdivided into equal segments called sectors. This division is accomplished by setting a number into the sector switches (see the discussion called Sector Detection). When the controller has selected the unit, the track, and the head, then it waits for the particular sector(s) where it wishes to write (store) or retrieve (read) data. Another option for locating an area on a track to be operated upon is by writing an Address Mark at a specific location on the track, and then looking for the mark at the beginning of a read operation.

When the controller commands the drive to go to a track/head/sector where it wishes to perform a read or write operation, the drive servo system under the direction of the MPU performs the positioning (Seek) operation. The MPU program uses information read from the servo surface by the servo head to do the Seek operation. The following discussion will describe servo surface decoding and then describe seek functions.

SERVO SURFACE DECODING

GENERAL

The servo surface is a prerecorded disk surface in the module that provides three basic types of information to the drive electronics. Information from the servo surface is read by the servo head. The servo head is mounted on the same positioner as the data heads; thus, movements of the servo head across the servo surface correspond exactly to movements of the data heads across the data surfaces.

The three types of information available from the servo surface are as follows:

- Radial movement of the heads, indicated by the Position signal
- Rotational position of the disks, indicated by the Index signal
- Exact speed of the disks, indicated by the 2.41 MHz Clock signal.

The significance of each type of information for drive operation and the development of the basic feedback signals from the servo signal are presented under the following topics:

- Tribit Recording Scheme
- Servo Surface Format
- Tribit Decoder Circuit Operation

TRIBIT RECORDING SCHEME

Servo information consists of tribit coding on a series of concentric tracks located on the servo surface. The pattern of flux reversals alternates from track to track. Each track has 128 segments, consisting of a special nine-byte resync code followed by 341 normal servo bytes.

Unless the servo head is positioned directly over one servo track, the signal it detects is a composite of signals from the two tracks nearest the head. Figure 1-14 shows servo information recorded on two adjacent tracks and the signal detected when the servo head is halfway between the tracks.

In figure 1-14, two normal bytes are followed by an index byte. Each normal byte contains three bits -- a sync bit and two position bits. The sync bits have negative polarity and are recorded on all tracks. The position bits have positive polarity and are staggered from track to track so that they make separate contributions to the composite servo signal.

The resync nine-byte codes appearing 128 times per disk rotation contain different combinations of sync bits and position bits, depending on what the code designates on the disk surface. The different codes and their relation to the disk format are explained under the next topic. Each nine-byte code is followed by 341 normal bytes. Thus, for each disk rotation, the servo head detects 128 X 350 or 44 800 servo bytes.

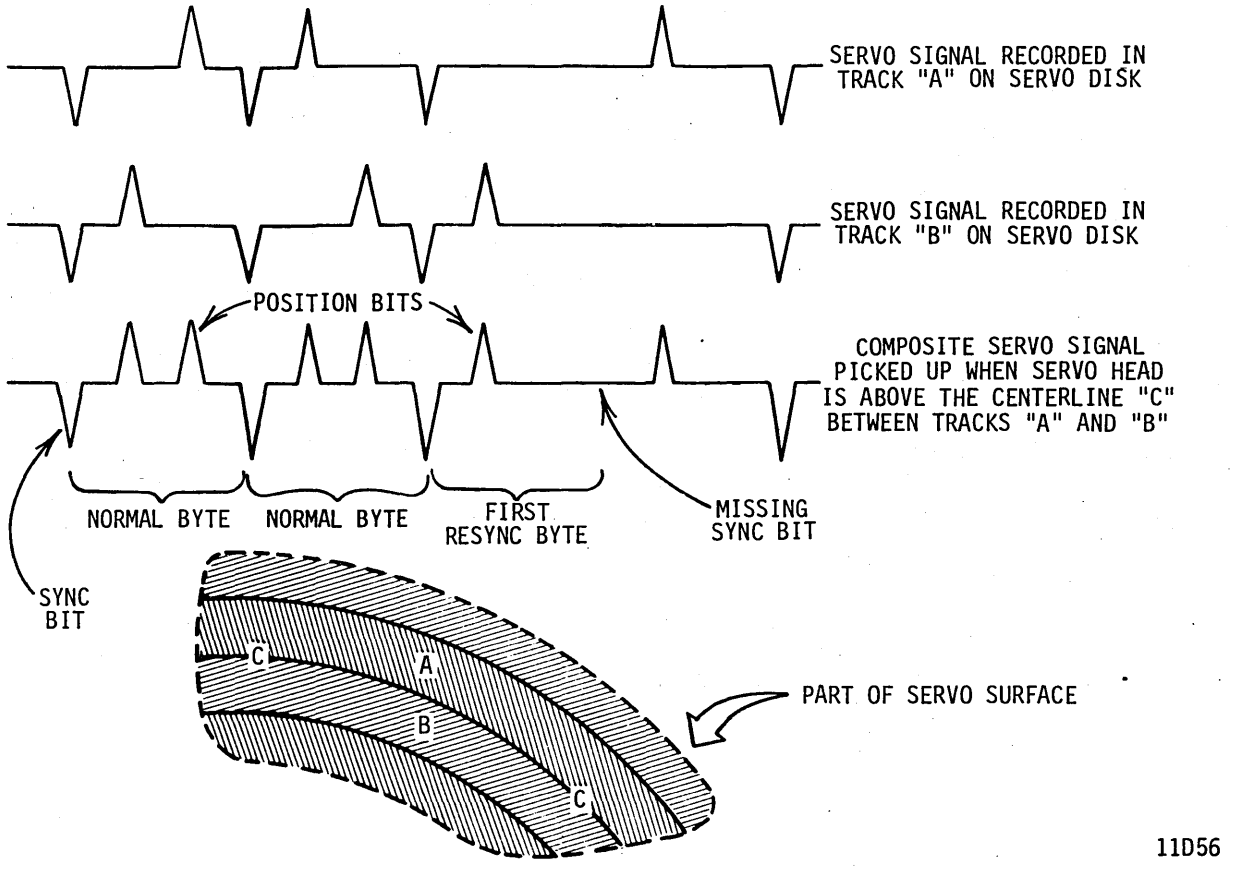


Figure 1-14. Tribit Pattern

The relative amplitude of the position bits within each servo byte is used to indicate the precise position of the servo head and, therefore, the data heads. When the data heads are located at the centerline of a data track, the servo head is actually centered between two of the prerecorded servo tracks and is reading an edge of each. The detected signal is a mixture of the two adjacent tribit signals. The amplitude of each position bit within a servo byte is proportional to the read coil overlap of the recorded servo tracks. With the head centered, each adjacent servo track contributes equal position bit amplitudes. As the head moves away from its centered position toward one servo track, the track being approached makes a greater contribution to the detected position bits than the one being left. The tribit demodulator converts this variation into the position signal used by the seek circuitry (see Position Demodulation).

Figure 1-15 shows the detected servo signal for three different servo head positions. In one of the three cases, the servo head is located on the centerline between two servo tracks, and the position bits have equal amplitudes. In the other two cases, the servo head is located on either side of the centerline, and the position bits have different amplitudes.

SERVO SURFACE FORMAT

The servo surface, through its encoding format, establishes the format of the disk data surfaces. The servo surface format divides the disk surfaces into four zones, a 1024-track data zone, two guardbands, and a buffer zone. The guardbands indicate areas of the disk that cannot be used for recording of data. The outer guardband consists of 10 tracks on the outer portion of the disk, and the inner guardband consists of 330 tracks on the inner portion of the disk. The buffer zone consists of 2 tracks located between the outer guard band and the data zone. In addition, all four zones contain an encoded "reference line" which establishes the logical beginning of each track. When this reference is decoded, the drive sends the Index signal to the controller via the interface.

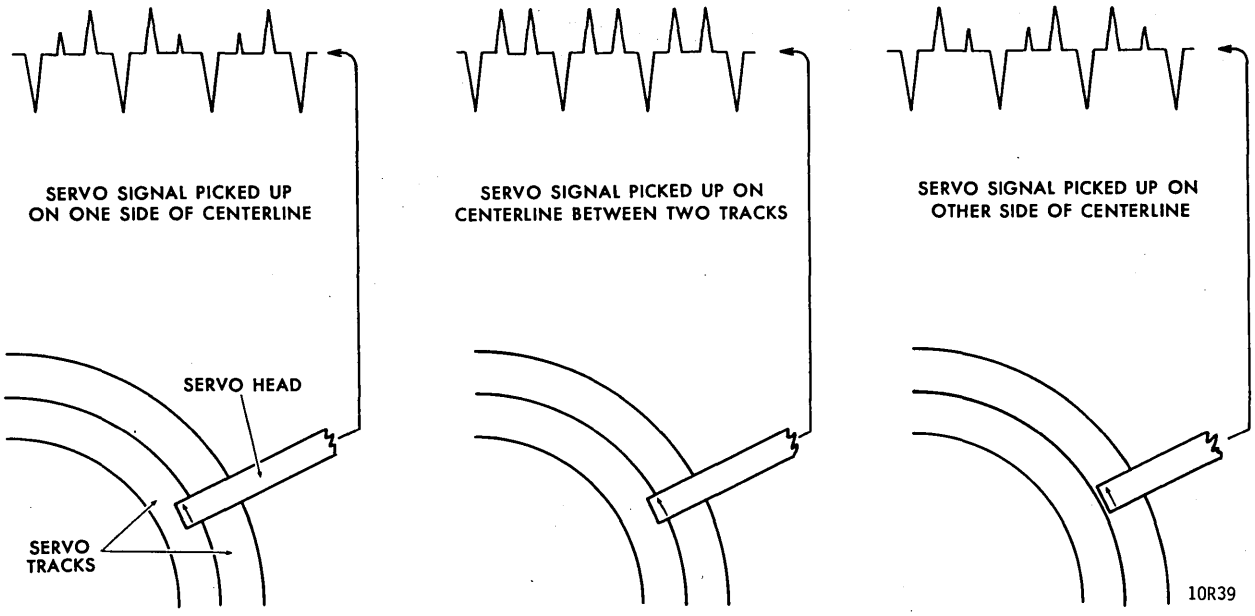


Figure 1-15. Tribit Signal Variations

Figure 1-16 shows the positioning of heads on the data pack disk surfaces and explains, in the exploded portion of the drawing, how formatting information is encoded on the disk. As described in the Tribit Recording Scheme discussion, nine-byte resync codes are used as format indicators. The index pattern (101000101) marks the logical beginning of each servo track. The remaining 127 coded patterns spaced around each servo track depend on the zone for that track. The outer guardband is encoded with pattern 100010101, the data zone and buffer zone with pattern 100010001, and the inner guardband with pattern 101010001.

Refer to the Index and Guardband Decoding discussion for a description of the circuitry that performs this decoding.

TRIBIT DECODER CIRCUIT OPERATION

General

Operation of the tribit decoder circuitry is discussed first in terms of its relation to other systems within the drive. This is followed by explanations of the individual functions performed by the decoder.

System Overview

Decoding the information present in the servo signal is essential for other functional areas of drive operation. Figure 1-17 is a functional block diagram showing signal flow between the tribit decoder and these other functional areas.

Inputs to the decoder come from the servo preamp and the MPU. The servo preamp amplifies the signal detected by the servo head. The +Slope signal, supplied by the MPU, sets up the phase of the decoded Position signal so that it can be used by the seek circuits.

The MPU monitors three output signals from the decoder. During normal seek operations, the servo head remains over the data zone. Thus, when the Inner or Outer Guard Band Pulses go active, the MPU reacts by altering the seek protocol. Improper decoder operation can affect seek reliability. For this reason, the MPU monitors the -Demodulator Active line.

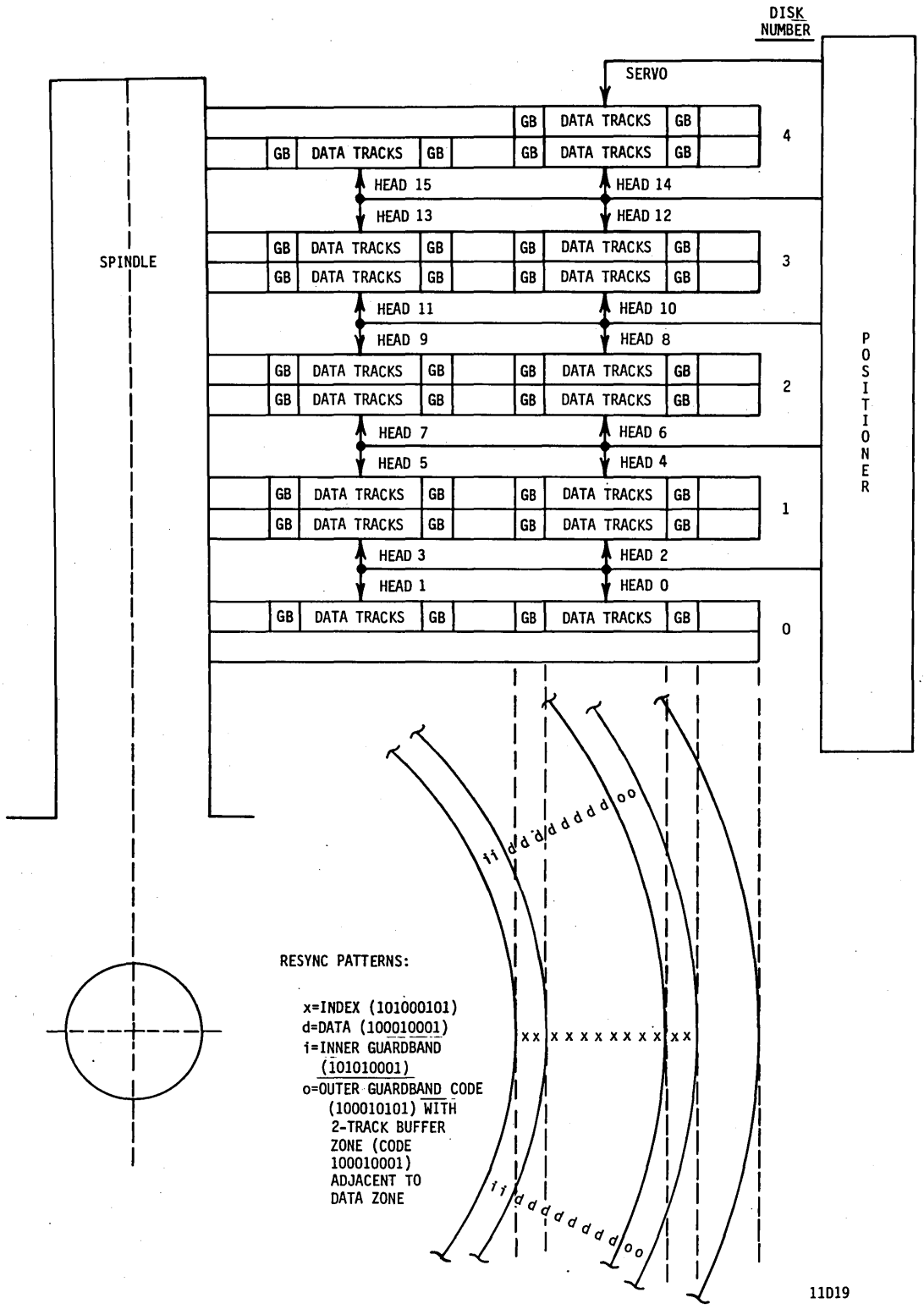


Figure 1-16. Servo Disk Format

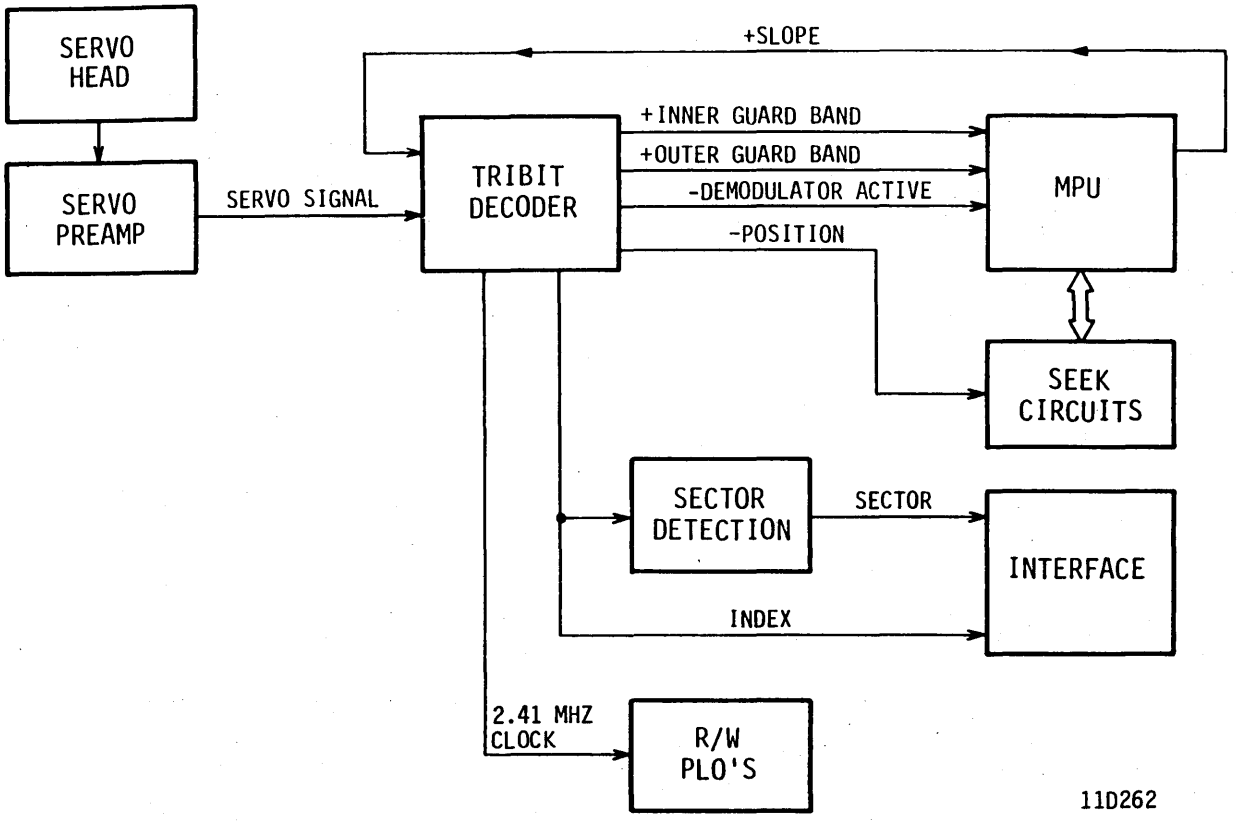


Figure 1-17. Tribit Decoder System Diagram

Data transfers to and from the disk must be coordinated with respect to the rotational position of the disk. The Index signal is decoded and is input to the Sector Detection circuitry which, in turn, generates a given number of Sector pulses per disk rotation. The controller coordinates data transfers based upon the Index and Sector pulses transmitted to it via the interface.

The 2.41 MHz Clock from the decoder is used by the R/W PLO circuitry to form a 14.5 MHz Servo Clock. The Servo Clock operates at exactly six times the frequency of the 2.41 MHz Clock, and it tracks the rotational velocity of the disk. The controller transfers data to the disk in sync with the Servo Clock. This compensation in the rate of data transfers to the disk makes the written data pattern independent of disk speed.

The remaining topics within this discussion cover the operation of circuits within the tribit decoder. Figure 1-18 is a block diagram showing these circuits and their interconnections.

Sync Bit Detector

The Sync Bit Detector monitors the Tribits signal from the Servo Preamp and generates a pulse on the -Sync Detect line each time a sync bit occurs in the Tribits signal. Sync bit detection is essential for all other tribit decoder functions because sync bits are the primary input to the Servo PLO circuit which in turn controls the timing of the Position Demodulator and the Index and Guard Band Decoder. In addition, the -Sync Detect signal reflects the encoding used to indicate Index, Data, and Guardband regions on the servo surface. Figure 1-19 is a block diagram of the Sync Bit Detector.

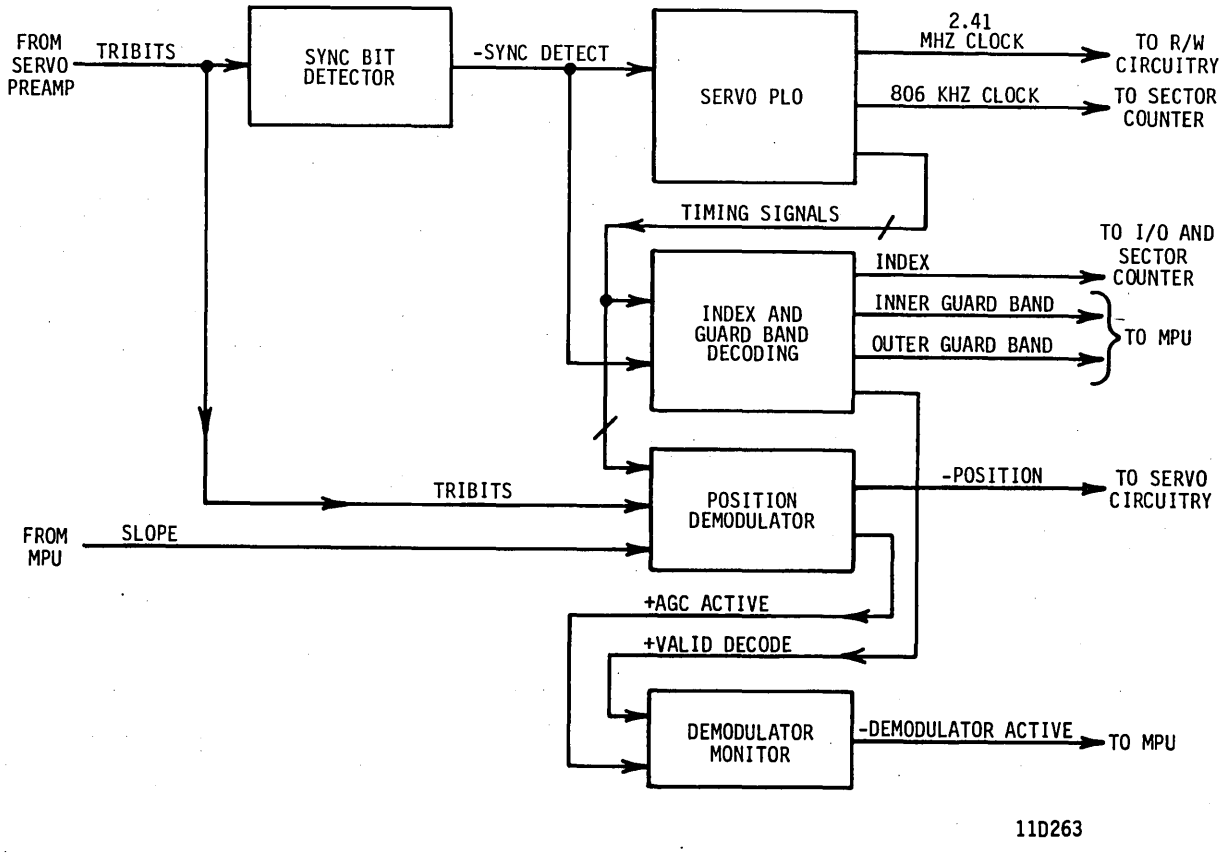


Figure 1-18. Tribit Decoder Block Diagram

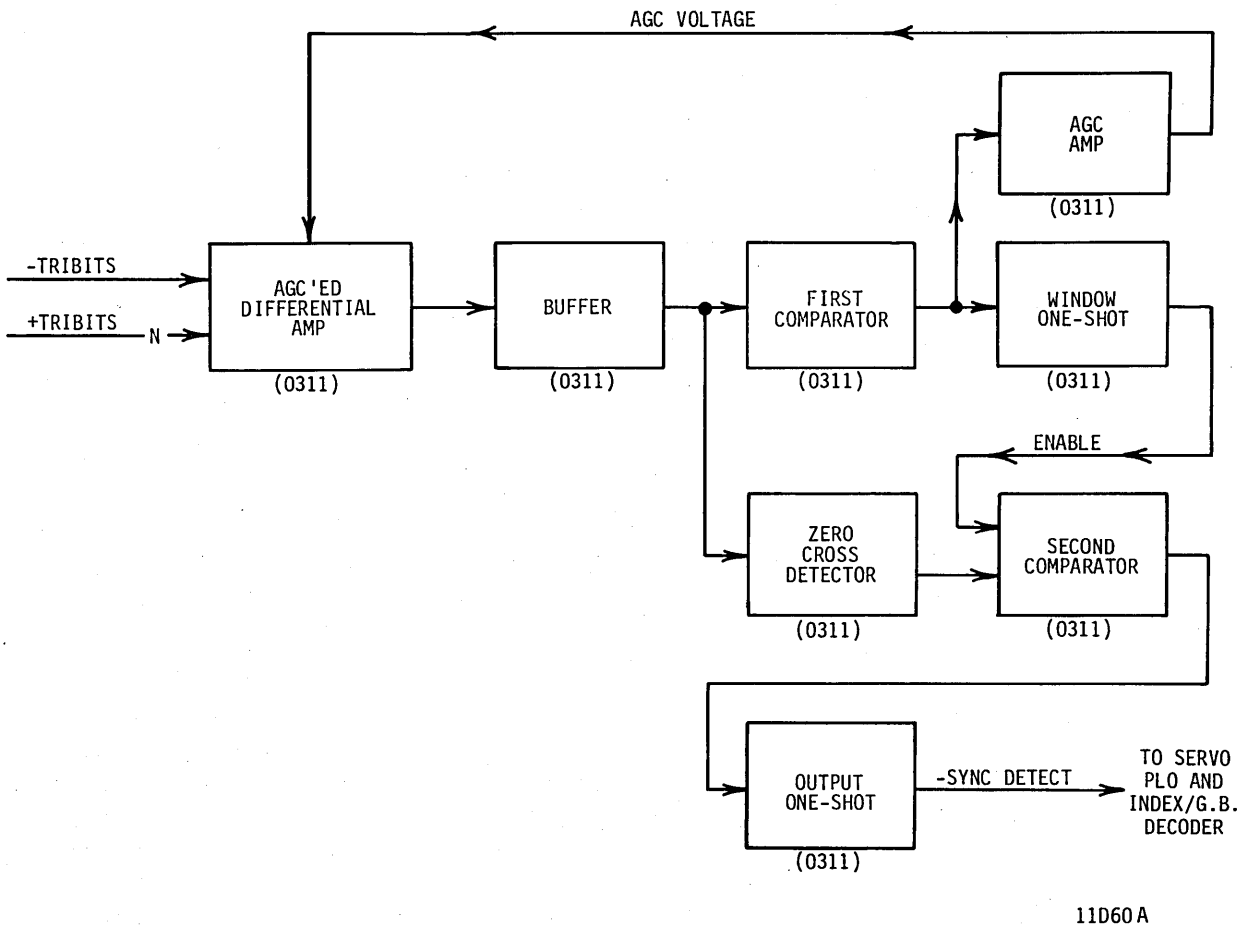


Figure 1-19. Sync Bit Detector

The Tribits signal is applied to an AGC-controlled differential amplifier. The amplifier output passes through a buffer stage and is ac-coupled to the input of the first comparator. A dc offset at the comparator input allows the comparator to be enabled only by the most negative portion of each sync bit.

Output pulses from the first comparator perform two functions. The AGC amp looks at these pulses and develops an AGC voltage to control the gain of the differential amplifier at the input. This AGC loop operates to ensure that the pulses coming from the first comparator have a constant duty cycle.

In addition to controlling AGC, the output pulses trigger a one-shot to develop a window during which sync bit detection is enabled. The gate from the window one-shot enables a second comparator. The input to the second comparator is the Tribits signal, differentiated by a zero-cross detector. The second comparator reacts only to zero-crossings produced when sync bits are expected because it is disabled at other times. Seeing an acceptable zero crossing, the second comparator triggers the output one-shot to generate a negative pulse on the -Sync Detect line.

Servo PLO

The Servo PLO uses a phase-locked loop to keep the timing in the tribit decoder synchronized to the detection of the sync bits in the Tribit signal. As shown in figure 1-20, a portion of the Servo PLO circuitry is located in the Demodulator Logic Chip. Circuitry external to the chip includes a charge pump, the 9.67 MHz Voltage-Controlled Oscillator (VCO) and logic that compensates for missing sync bits.

The Sync Bit Detector supplies -Sync Detect pulses to the phase comparator in the Demodulator Logic Chip. As described under Servo Surface Format, each servo track has patterns encoded by missing sync bits to locate index on the disk and to indicate whether the track is in an inner or outer guard band or in the data zone. However, the phase comparator latch must be reset at regular intervals of about 620 ns. Because the encoded patterns never contain two consecutive missing sync bits, it is possible to develop a "dummy" trigger pulse whenever a sync bit is missed. To do this, -Sync Detect pulses clock a retriggerable one-shot. Each missing bit allows the one-shot to time out and trigger the missing bit one-shot. In this way, the phase comparator latch is reset periodically either by pulses on the -Sync Detect line or on the +Missing Bit line.

The Set input to the phase comparator latch is derived from a Divide-by-Six counter in the Demodulator Logic Chip. This counter is clocked by the 9.67 MHz signal from the VCO, which oscillates at six times the repetition rate of -Sync Detect pulses. The counter subdivides the interval between -Sync Detect pulses into six equal parts. Through various logical combinations of the outputs of the counter stages, the synchronizing logic develops gates needed for the different decoding operations. Because the PLO keeps the Divide-by-Six counter phase-locked to the detected sync bits, these timing gates stay synchronous with the tribit pattern. One of these gates, the Set input to the phase comparator latch, goes active when three VCO oscillations have occurred following reset of the latch.

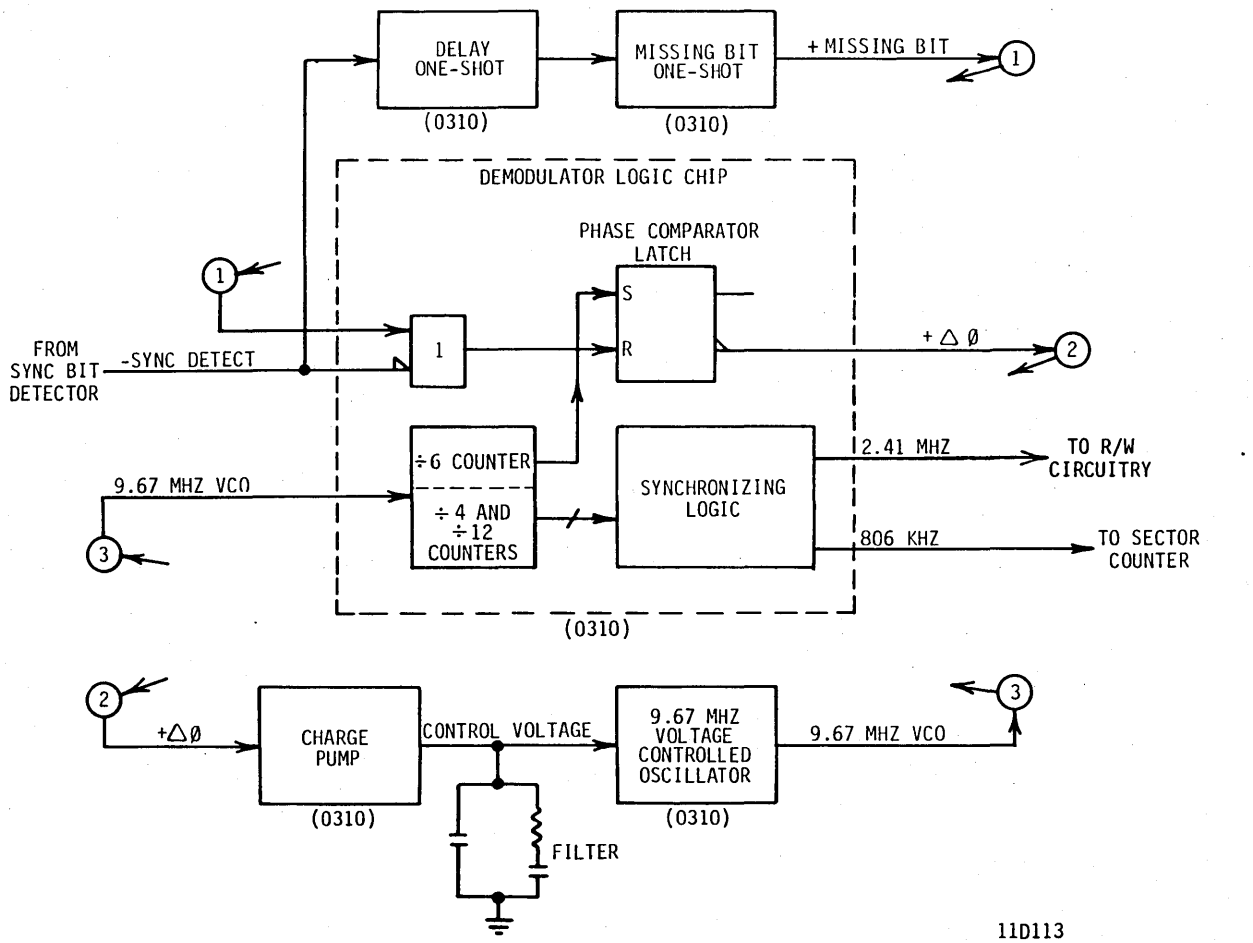


Figure 1-20. Servo PLO Block Diagram

Thus, the +Delta Ø signal generated by the latch is active for three VCO oscillations and is then inactive until the next Reset input occurs (approximately three VCO oscillations later).

The phase comparator latch causes the VCO to shift in frequency when the active interval and the inactive interval of the +Delta Ø signal are not equal. This frequency shift is governed by a charge pump that supplies the control voltage to the VCO. When the +Delta Ø signal is inactive, the charge pump supplies current to the capacitors filtering the control voltage to the VCO (making the control voltage more negative). When the +Delta Ø signal is active, the charge pump draws current from these capacitors (making the control voltage more positive). Thus, any imbalance in the set and cleared intervals of +Delta Ø produces a net change in the control voltage.

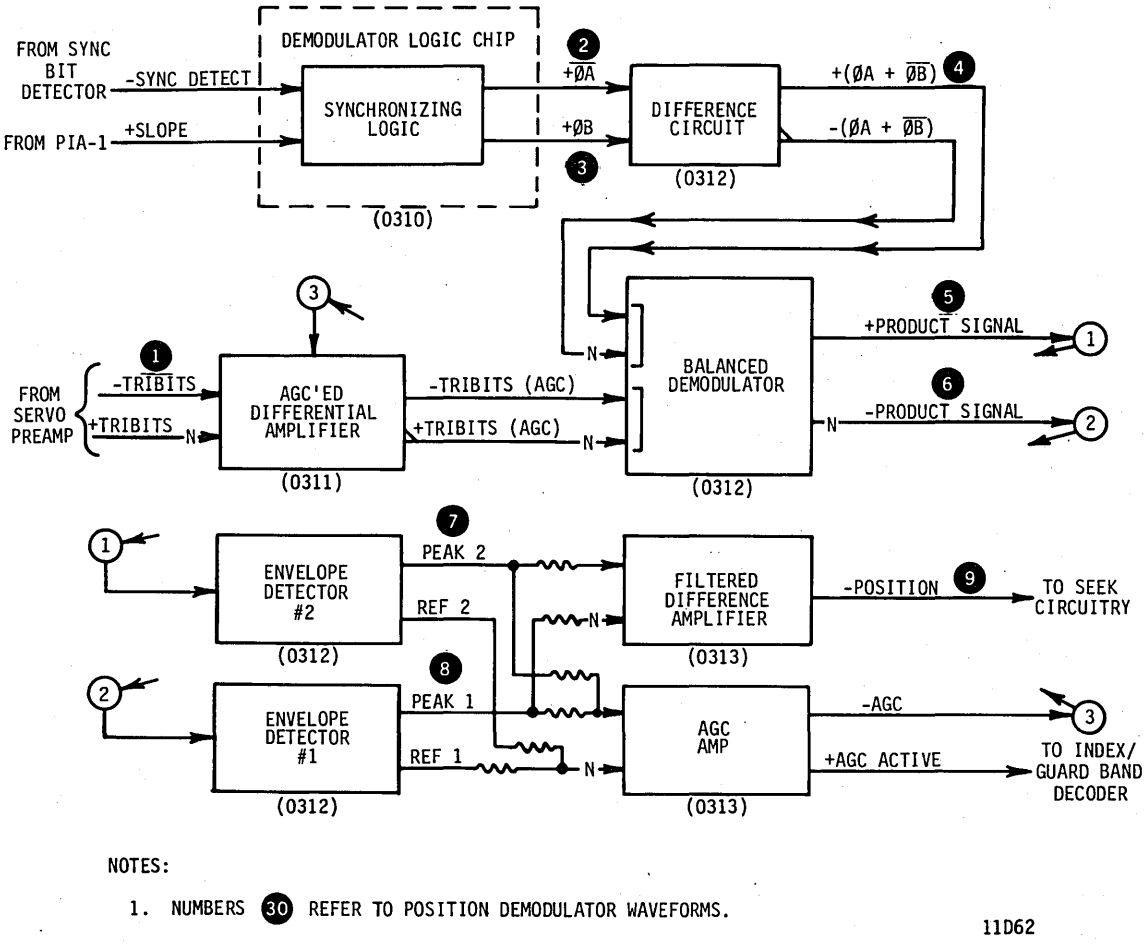
Consider three situations of changing disk speed and its effect on the Servo PLO. When the disks are rotating at constant speed and the VCO is phase-locked, the set and cleared intervals of the phase comparator latch are equal, the control voltage is normal, and the VCO frequency remains the same. During a decrease in disk speed, the VCO frequency must decrease. In this case, the Set input to the latch is early, and +Delta Ø is inactive longer than it is active. This makes the control voltage more negative which in turn reduces the VCO frequency. During an increase in disk speed, the VCO frequency must increase. In this case, the Set input to the latch is late, and +Delta Ø is active longer than it is inactive. This makes the control voltage more positive which in turn increases the VCO frequency.

The Divide-by-Six counter develops timing signals used by the Position Demodulator and by the Index and Guard Band Decoder. In addition, the following clocks are derived from the VCO signal:

- 806 kHz -- derived by dividing the VCO signal by twelve and supplied to the Sector Counter Gate Array.
- 2.41 MHz -- derived by dividing the VCO signal by four and supplied to the Write PLO.

Position Demodulator

The Position Demodulator consists of the circuitry in the Tribit Decoder that develops the -Position signal. It derives this signal from the position bits in the Tribit pattern while depending on timing information developed from the sync bits in the Tribit pattern. The timing information is consistent on all servo tracks while the position information changes from track to track. Consistent timing information keeps the demodulator synchronized (regardless of the position or velocity of the servo head) and allows the demodulator to detect the changes in position information from which the -Position signal is derived. Figure 1-21 is a block diagram of the Position Demodulator, and figure 1-22 provides typical waveforms for the circuit. The following paragraphs review how position is encoded on the servo surface, discuss signal flow through the demodulator, and describe briefly how the Position signal is used by the servo circuitry.



NOTES:

1. NUMBERS (30) REFER TO POSITION DEMODULATOR WAVEFORMS.

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Figure 1-21. Position Demodulator Circuitry

As described earlier under Tribit Recording Scheme, any given tribit pattern contains two position bits. One bit is supplied by each of the two servo tracks closest to the servo head, and the two bits are staggered so they appear in sequence in the Tribit signal. If the position bits available from one set of alternate servo tracks are designated as #1 bits and the position bits from the remaining tracks are designated as #2 bits, then the -Position signal is positive when the #2 bit amplitudes exceed the #1 bit amplitudes and is negative when the #1 bit amplitudes exceed the #2 bit amplitudes. The synchronizing logic in the Demodulator Logic Chip develops gating signals (+ØA and +ØB) that discriminate between the #1 bits and #2

bits. This logic is initialized when an Index pattern (resync pattern) occurs in the Tribit signal (see Index and Guard Band Decoding). Through the resync process, gating signals internal to the Demodulator Logic Chip are forced to match the format of the tribits as they were recorded on the servo surface.

These internal gating signals are output from the Demodulator Logic Chip as the +ØA and +ØB signals. However, the MPU controls which internal gate becomes +ØA and which gate becomes +ØB via the +Slope signal issued by PIA-1. At the start of a new seek, the MPU sets the level of the +Slope signal, thereby choosing whether or not to interchange the +ØA and +ØB signals. Interchanging them inverts the Position signal and allows the MPU to ensure that the +Position signal will have the required slope as the seek circuits position the heads at their new destination. This slope requirement is discussed further under Seek Functions.

As shown in figure 1-21, the balanced demodulator uses the +ØA and +ØB signals to develop, from the Tribits signal, input signals for the two channels of envelope detection. The balanced demodulator has two differential inputs: a three-step gating signal and an Amplified Tribits signal. The Amplified Tribits signal is produced from the Tribits signal by an AGC-controlled differential amplifier. A difference circuit develops the +(ØA + not ØB) signal and its inverse from the +ØA and +ØB gates.

Figure 1-22 shows typical input and output waveforms for the balanced demodulator. The balanced demodulator multiplies the two input signals to create complementary product signals. Because the three-step gating signal is zero when sync bits appear, the product signals contain only position peaks. In the +Product signal, the #2 bits are positive and the #1 bits are negative. In the -Product signal, the opposite is true.

Although each envelope detector input contains both positive and negative peaks, the detector is sensitive only to changes in the positive peaks. Each detector uses two transistors to update the voltage on a capacitor. In intervals where the envelope amplitude is increasing (successive peaks are more positive), one transistor pulls the capacitor voltage up. In intervals where the envelope amplitude is decreasing, the other transistor pulls the capacitor voltage down. Because this adjustment occurs at the instant of peak detection, the output signal from the detector steps to a new level, holding that level until the next peak. Additional transistors in each detector circuit act as current sources and provide temperature compensation.

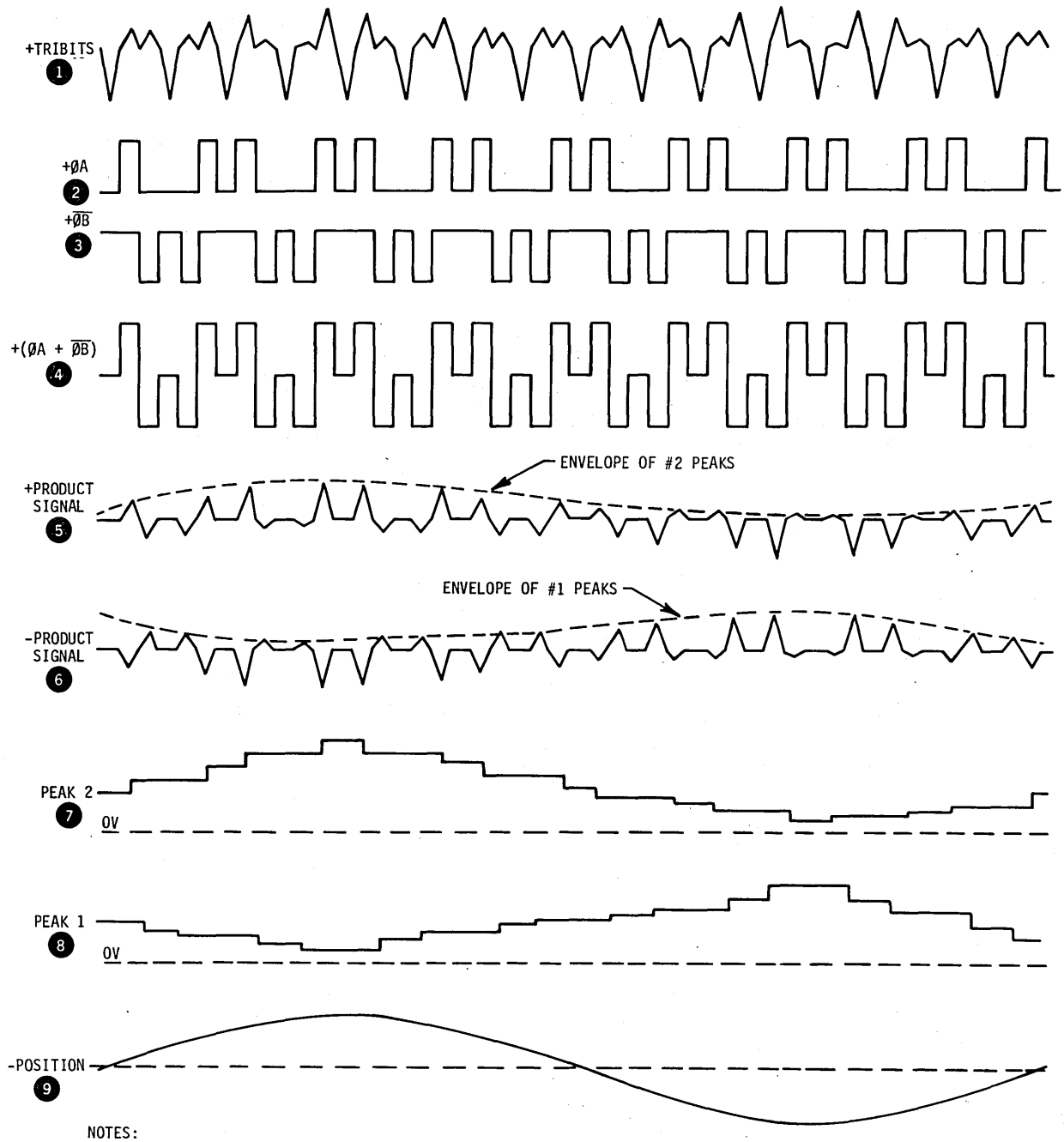


Figure 1-22. Position Demodulator Waveforms

The envelope detector outputs, the Peak 1 and Peak 2 signals, are differential inputs to a filtered difference amplifier. This stage develops the -Position signal by subtracting Peak 1 from Peak 2. It uses a low-pass filter to remove from the -Position signal any high frequency noise, resulting from the steps in the Peak 1 and Peak 2 inputs. The -Position signal is zero when the servo head is centered between two servo tracks. At this time, the data heads are positioned directly over a data track. The -Position signal varies either positive or negative depending on displacement of the servo head from that centerline.

The AGC Amp monitors the sum of the Peak 1 and Peak 2 signals, relative to the sum of two bias voltages (Ref 1 and Ref 2) from the envelope detectors, to produce an AGC voltage for the differential input amplifier. AGC action keeps the peak-to-peak amplitude of the -Position signal independent of servo signal variations. A level detector, connected to the AGC voltage, issues the +AGC Active signal to indicate that position demodulation is satisfactory. If the +AGC Active signal goes low or if valid decoding ceases (see the next topic), the -Demodulator Active line goes high, warning the MPU that the tribit decoder is not functioning properly.

With one exception, movement of the servo head from one track to an adjacent track reverses the polarity of the Position signal. This is true when the servo head crosses tracks in the guard bands and the data zone. However, the buffer zone, located between the outer guard band and data zone, has two consecutive tracks that are recorded with identical (not alternating) position information. Thus, as the servo head moves across these tracks, the Position signal stays negative and does not cross zero as it does in the other zones. This characteristic of the Position signal is needed for Return to Zero seeks (see Seek Functions).

Index and Guard Band Decoding

The index and guard band decoding circuitry produces output pulses each time the servo head detects certain codes in the pattern of sync bits on the servo surface. This circuitry also originates the +Valid Decode signal which is used to indicate reliable decoder operation. Refer to Servo Surface Format for a description of the sync bit codes and their location on the servo disk.

Figure 1-23 is a block diagram of the index and guard band decoding circuitry. This circuitry is located in the Demodulator Logic Chip.

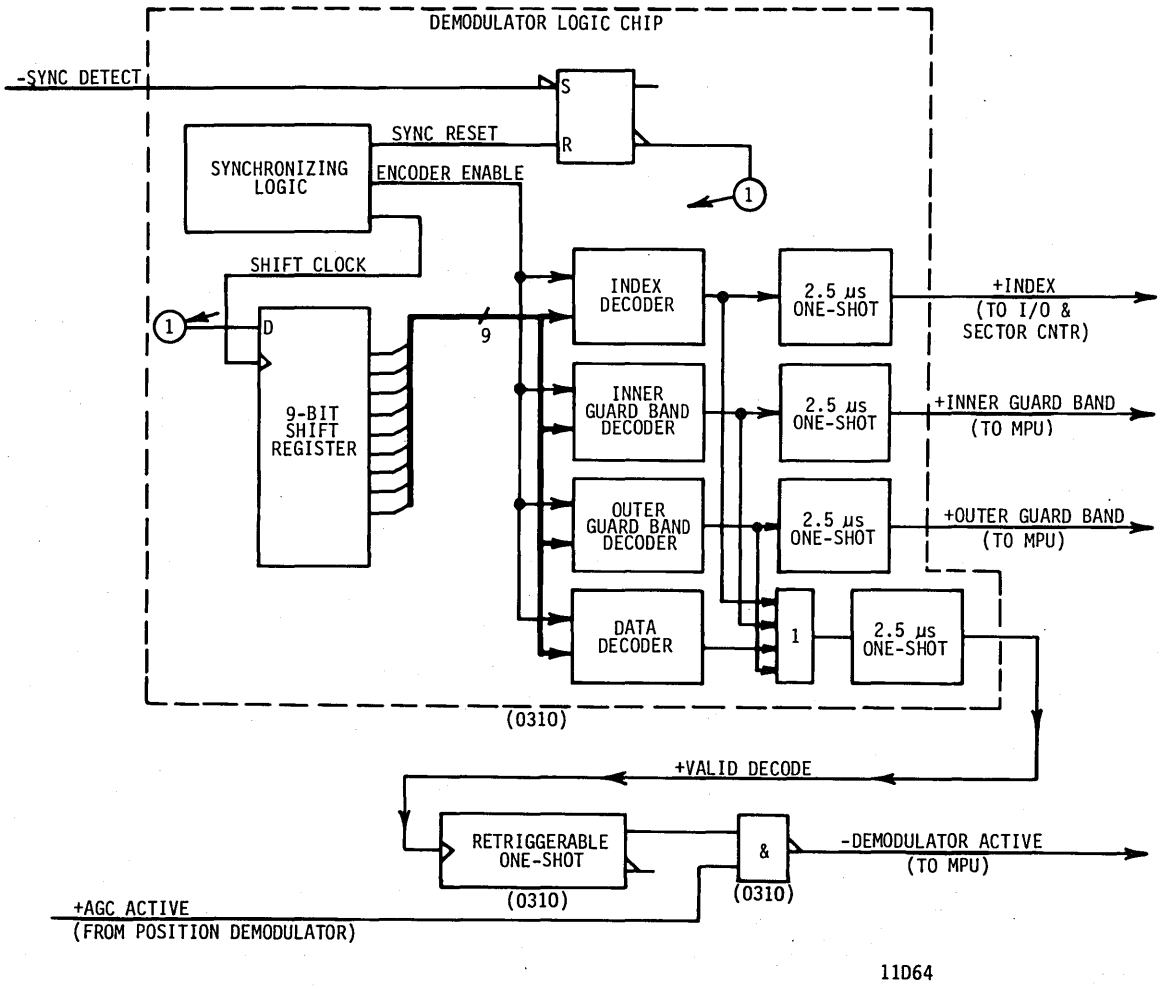


Figure 1-23. Index and Guard Band Decoder

The decoding circuit responds to three timing signals that repeat in sequence for each tribit pattern detected. The synchronizing logic, controlled by the Servo PLO, issues the Sync Reset signal prior to the detection of each sync bit. If a sync bit is detected, a low pulse on the -Sync Detect line sets a FF. If no sync bit was detected, however, the FF remains reset. The next timing signal, Shift Clock, clocks the output of the FF into the first stage of a 9-bit shift register and produces a shift in the register.

The shift register contains information about whether a sync bit was present in each of the nine preceding tribit patterns. After clocking the shift register, the synchronizing logic activates a gate (Decoder Enable) that enables each of the decoder circuits shown in figure 1-23. Each decoder looks for a particular pattern of ones and zeros in the shift register's outputs corresponding to a code of missing sync bits on the servo track. The codes detected are as follows:

- When the register contains 101000101, the Index Decoder triggers two one-shots to activate the +Index and +Valid Decode lines for 2.5 microseconds.

- When the register contains 100010101, the Outer Guard Band Decoder triggers two one-shots to activate the +Outer Guard Band and +Valid Decode lines for 2.5 microseconds.

- When the register contains 101010001, the Inner Guard Band Decoder triggers two one-shots to activate the +Inner Guard Band and +Valid Decode lines for 2.5 microseconds.

- When the register contains 100010001, the Data Decoder triggers a one-shot to activate the +Valid Decode line for 2.5 microseconds. The Demodulator Logic Chip has no output corresponding to the code for the data zone.

The Inner and Outer Guard Band signals are supplied as interrupts to the microprocessor at PIA-1. These interrupts inform the microprocessor that the heads are not located over the data zone. The Index signal is used by the Sector Counter as described in the next topic, and is also sent to the controller.

Pulses on the Valid Decode line are supplied as triggers to a retriggerable one-shot. During normal decoder operation, this one-shot stays set. If the one-shot times out, the -Demodulator Active line to the MPU goes high to indicate improper decoding.

Sector Detection

The sector detection circuit (figure 1-24) generates signals which are used by the drive to determine the angular position of the heads with respect to index. These signals are called Sector pulses and a specific number of them are generated during each revolution of the disks. The Sector pulses logically divide the disk into areas called sectors.

The Sector pulses are generated by the Sector counter which generates a pulse each time it reaches its maximum count (4095). The counter is incremented by 806 kHz clock pulses. These clock pulses are derived by dividing the 9.67 MHz Servo Clock by 12 and represent the beginning of each data byte. The Index pulse resets the counter allowing 22 400 clock pulses per revolution of the disk.

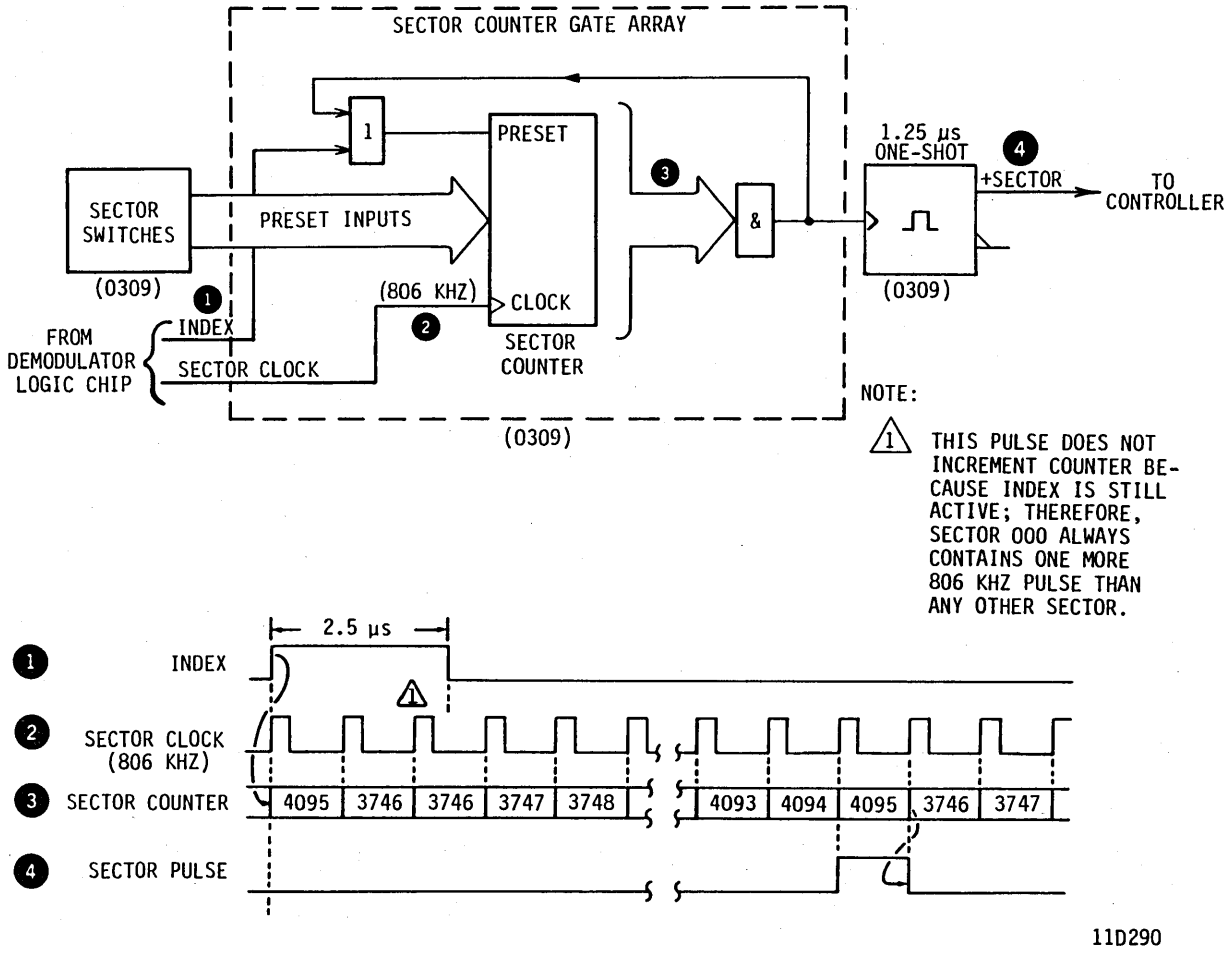


Figure 1-24. Sector Detection - Logic and Timing

The fact that the same number of 806 kHz clock pulses occur during each revolution makes it possible to program the counter to reach the maximum count (thus generating a Sector pulse) any desired number of times per revolution. This is done by presetting the counter to the proper value at the beginning of each sector. For example, if it is desired to have 64 sectors, the counter would have to count 350 clock pulses in each sector (22 400 divided by 64) and the counter would be preset to 3746. In this case, the counter starts at 3746 and increments each clock time until it reaches the maximum count (4095). Reaching the maximum count causes the Sector pulse to be generated. The next clock pulse (350) presets the counter back to 3746 (thus disabling the Sector pulse) and the counter begins the next sector.

The sector length is varied by presetting the sector switches located on the control board. Refer to volume 1 of the maintenance manual for details regarding the setting of the sector switches.

SEEK FUNCTIONS

GENERAL

During seek operations, the drive positions the heads over the desired cylinder on the disk. The drive servo circuits, under the direction of a microprocessor unit (MPU), control this function. The drive servo circuits translate MPU instructions into electromechanical motion to position the read/write heads accurately and to allow the transfer of magnetic pulses to and from a disk storage surface. The two main topics of this section describe servo circuit operation and the sequencing of events in different types of seeks. Since these subjects are interrelated, they are preceded by an overview of system operation that explains the roles played by the interface and the MPU, and that describes the servo functions in general terms.

SYSTEM OVERVIEW

Each seek operation can be described in terms of four basic drive activities. These activities are shown in terms of general information flow between major drive functional elements in figure 1-25. These activities occur in the following sequence:

- Command -- The interface processes the command from the controller that instructs the drive to seek to a different cylinder on the disks.

- Control -- The MPU interprets the seek command, then translates the command into a sequence of controls sent to the servo circuitry. These controls dictate the direction of the seek, specify actuator velocity throughout the seek, and step the servo through its operating modes.

- Execution -- The servo circuitry executes the seek in response to control information received from the MPU. This execution is accomplished in three modes: the coarse mode, during which the actuator is moved at a controlled velocity toward its destination; the settle-in mode, in which the actuator locks in to its final position; and the track-following mode, in which the actuator position is maintained until another seek is commanded. The servo controls current to the voice coil to

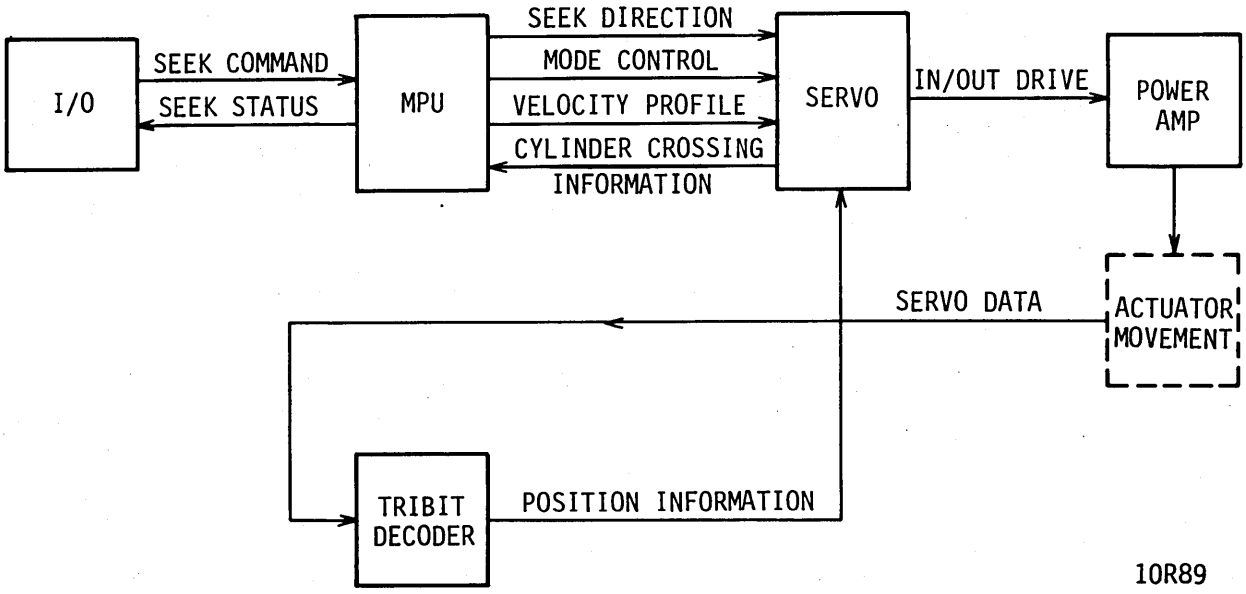


Figure 1-25. Seek Functions Block Diagram

move the actuator/heads via in and out drive signals to the power amp. Position information from the tribit decoder serves as a feedback source to the servo loop and is converted into cylinder crossing information for the MPU.

- Status -- The MPU informs the controller via the interface whether or not the seek was accomplished successfully. This indicates whether or not a reliable data transfer can be performed on the selected cylinder.

The concept of a closed loop is essential to understanding the operation of the servo system. Figure 1-26 shows a generalized servo loop that illustrates several principles governing the servo loops in the drive. The inputs to the summing amp are added, and any departure of the sum away from zero indicates that the system is unbalanced. To compensate for the imbalance, the summing amp issues a correction signal to the mechanical system. The response of the mechanical system is converted into an electrical signal which is an input to the summing amp. Mechanical movement continues until the system balance is restored, corresponding to a null in the summing amp inputs.

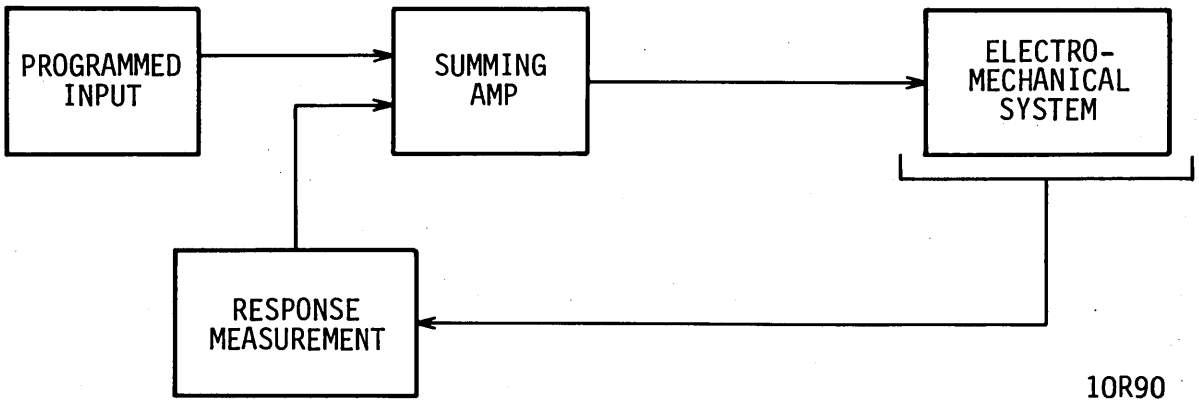


Figure 1-26. Generalized Servo Loop

The drive employs two basic servo loops, a coarse loop used in the coarse mode and a fine loop used in the settle-in and track-following modes. Figure 1-27 breaks out the block diagram of figure 1-26 to show the coarse servo loop in simplified form. In the coarse loop, the actuator moves at a prescribed velocity from the original cylinder address to the final cylinder address. The summing amp receives two inputs -- one signal represents the prescribed (desired) velocity of the actuator and the other represents the measured velocity of the actuator.

When the desired velocity exceeds the measured velocity, desired current is produced to accelerate the actuator. When the measured velocity exceeds the desired velocity, desired current is produced to decelerate the actuator. The actuator is allowed to coast when the two inputs are equal.

Figure 1-28 breaks out the block diagram of figure 1-26 to show the fine servo loop in simplified form. In the fine loop, the heads settle-in to their destination position and then maintain their position on track. The summing amp has no programmed input. Its only input is the Position signal, which is nulled at track center and varies positive or negative depending on how far the heads are displaced from track center. Any displacement of the heads from track center is adjusted by the fine loop until the summing amp input is nulled.

The following paragraphs discuss the circuit operation of these loops in more detail and then go on to describe the sequence of events in typical seeks.

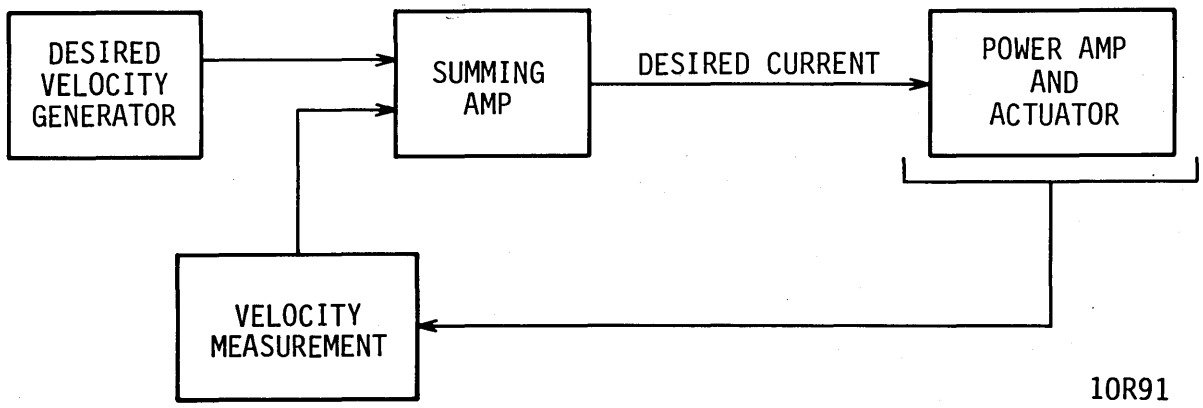


Figure 1-27. Simplified Coarse Servo Loop

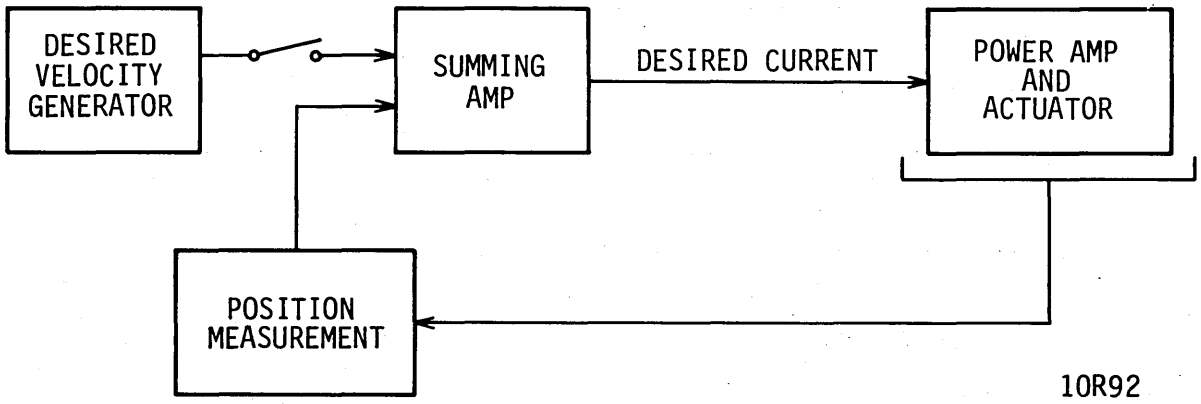


Figure 1-28. Simplified Fine Servo Loop

SERVO CIRCUIT FUNCTIONS

General

Servo circuit functions are discussed in terms of the three basic loops within the servo circuitry (coarse, fine, and load/retract loops). The coarse loop and the fine loop have some circuit elements in common. These common circuit elements are described in detail under Coarse Loop Operation and are mentioned briefly under Fine Loop Operation. Seek operations follow defined sequences in which the MPU exercises control over the servo circuitry. These sequences are described under the next topic, Types of Seeks.

Coarse Loop Operation

General

The servo system, operating in the coarse loop, moves the heads from the existing cylinder address to within one half track of the new address. Figure 1-29 is an overall block diagram of the coarse loop circuitry. Discussion of the coarse loop is presented in the following topics:

- Microprocessor Control System
- Desired Velocity Generation
- Cylinder Pulse Detection
- Velocity Measurement
- Summing Amp
- Power Amp Driver
- Power Amplifier

Microprocessor Control System

The microprocessor control system monitors various functions of the drive and executes most of the control sequences required for seek functions. The following paragraphs provide a general description of the components and signal paths in the microprocessor system, and describe the role of the microprocessor system pertaining to seek functions. Figure 1-30 is a block diagram of the microprocessor system. Readers interested in internal operation of the microprocessor and its peripheral chips may refer to the CDC Microcircuits Manual for more information.

The microprocessor control system consists of a 6802 microprocessor unit (MPU), an 8K-byte read-only memory (ROM), three peripheral interface adapter (PIA) chips, and a programmable timing module (PTM). The MPU communicates with its peripheral chips via an 8-bit bidirectional data bus, a 16-bit address bus, and several control lines. A decoder chip monitors Address lines 13 through 15 and develops chip select signals for each peripheral chip whenever the Valid Memory Address line is active. The MPU sets the Read line to read data from a peripheral or clears the line to write data into a peripheral. The Phase 2 Clock, developed by a crystal-controlled oscillator feeding the MPU, provides a timing reference for the system.

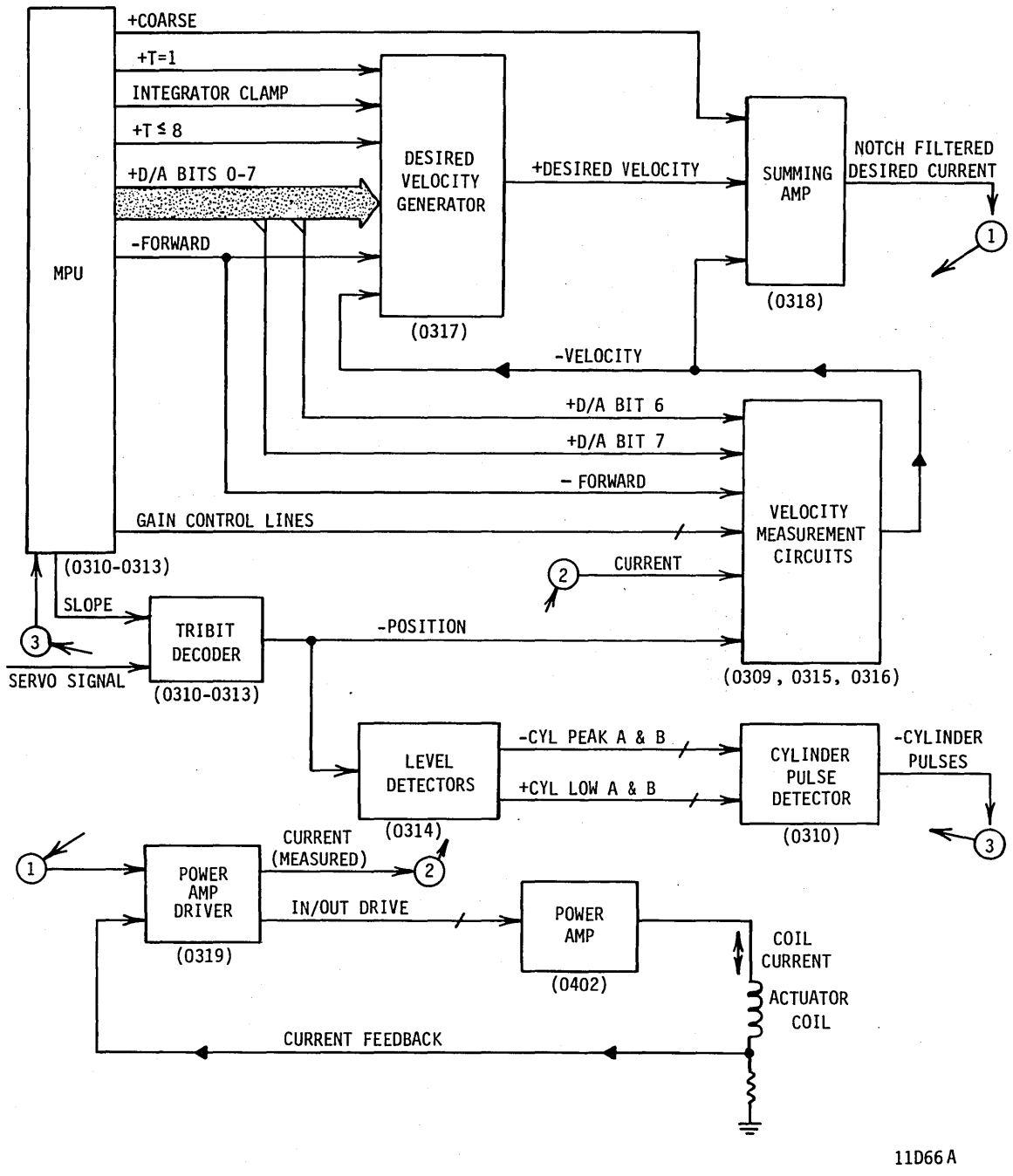


Figure 1-29. Coarse Loop Block Diagram

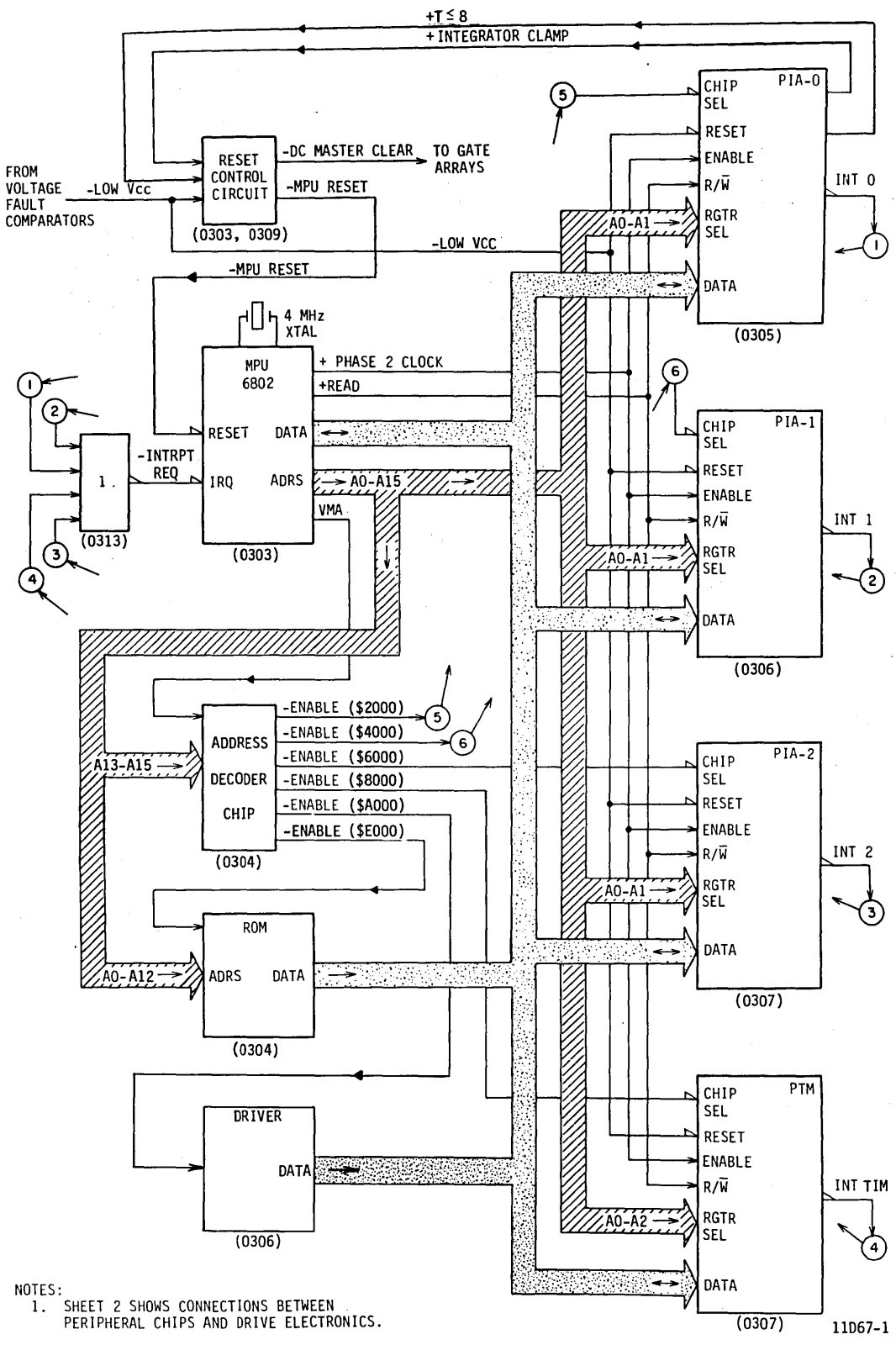


Figure 1-30. Microprocessor Control System (Sheet 1 of 2)

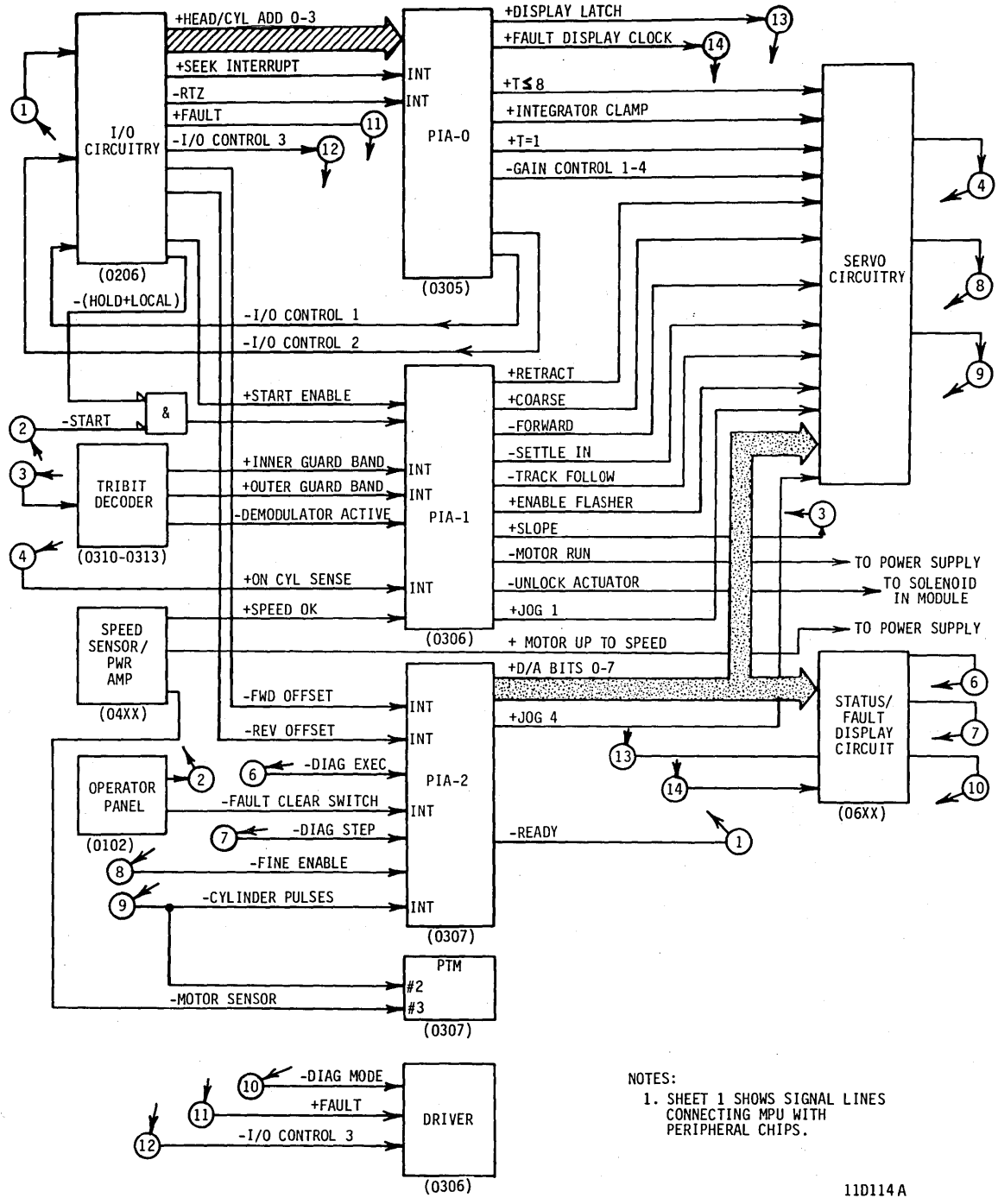


Figure 1-30. Microprocessor Control System (Sheet 2)

The firmware instructions for the MPU reside in the ROM. Detailed information about the MPU programming is beyond the scope of this manual. However, the various sequences which the MPU performs are outlined under Power Functions and Types of Seeks. The ROM also contains a table that specifies a velocity profile for normal seeks.

A driver chip and three PIAs allow the MPU to monitor the digital levels of certain signals developed in hardware external to the microprocessor system. In addition, the MPU can output various command signals via the PIAs. Certain PIA input signals form maskable interrupts to the MPU. When unmasked, these interrupts inform the MPU of status changes that require switching to a different routine within its firmware. The specific PIA inputs and outputs are listed in figure 1-30 and are referenced in the applicable circuit descriptions. A set of PIA lines requiring additional explanation includes I/O Control lines 1, 2, and 3. I/O Control lines 1 and 2 go from PIA-0 to the I/O Gate Array. These lines allow the MPU to perform various operations inside the gate array, such as setting the On Cylinder and Seek Error FFs, multiplexing cylinder and head addresses out of the array, and reading various fault statuses via the I/O Control 3 line.

Within the PTM, counter #2 allows the MPU to count tracks-to-go in a seek. This counter is decremented during seeks by cylinder pulses. Counter #3 is used by the MPU to generate timeouts for various operations.

The MPU system performs the following basic functions during drive operation:

- It monitors start conditions to initiate load and retract operations.
- It starts and stops the drive motor.
- It monitors the Seek Interrupt line and executes normal seeks.
- It specifies the desired actuator velocity during coarse seeks.
- It monitors the RTZ Interrupt line and executes RTZ seeks.
- It controls the On Cylinder and Seek Error FFs in the I/O Gate Array.
- It performs diagnostic functions in response to inputs entered on the Fault Display board.

These functions are described in detail in the remainder of Seek Functions. In addition, the MPU exchanges fault status with the I/O Gate Array. This activity is discussed under Fault and Error Conditions.

Desired Velocity Generation

The desired velocity circuit generates the +Desired Velocity signal, a changing analog voltage that indicates the desired velocity of the actuator throughout the coarse mode of the seek. Throughout the seek, the MPU refers to a table in the ROM that specifies desired velocity in binary form as a function of the number of tracks to go (T), which is the number of track crossings remaining until the heads reach their destination.

The velocity table is organized in a manner that allows one table of values to be used for all normal seeks. The maximum velocity of the table is for 255 tracks, and as the values decrease, a velocity profile is developed whereby velocity is proportional to the square root of the distance remaining. This profile produces constant deceleration of the heads in order to minimize seek times while controlling the approach of the heads to their final position. The organization of tabulated velocity in terms of tracks to go makes it possible to use one table for all seeks. Different seek lengths start at different points within the table. For example, the velocity specified when T=30 is the same regardless of the total seek length.

The desired velocity circuit provides a ramp signal from the D/A (Digital to Analog) Converter based upon the eight D/A Bits it receives from the ROM table via PIA-2 (see figure 1-31). When $T \leq 8$, the two uppermost D/A bits are masked out at the D/A and are used elsewhere, and the Integrator Clamp signal is input via PIA-0 to provide a sawtooth signal from the Velocity Integrator to add fill-in current to the ramp as the heads approach the selected track. At each cylinder crossing, the MPU refers to a count of tracks to go in PTM Counter #2 and outputs the current value of tabulated velocity using the D/A Bits. Each change in the D/A Bits results in a stepped change in the D/A ramp. Typical waveforms for the desired velocity circuit are given in figure 1-32.

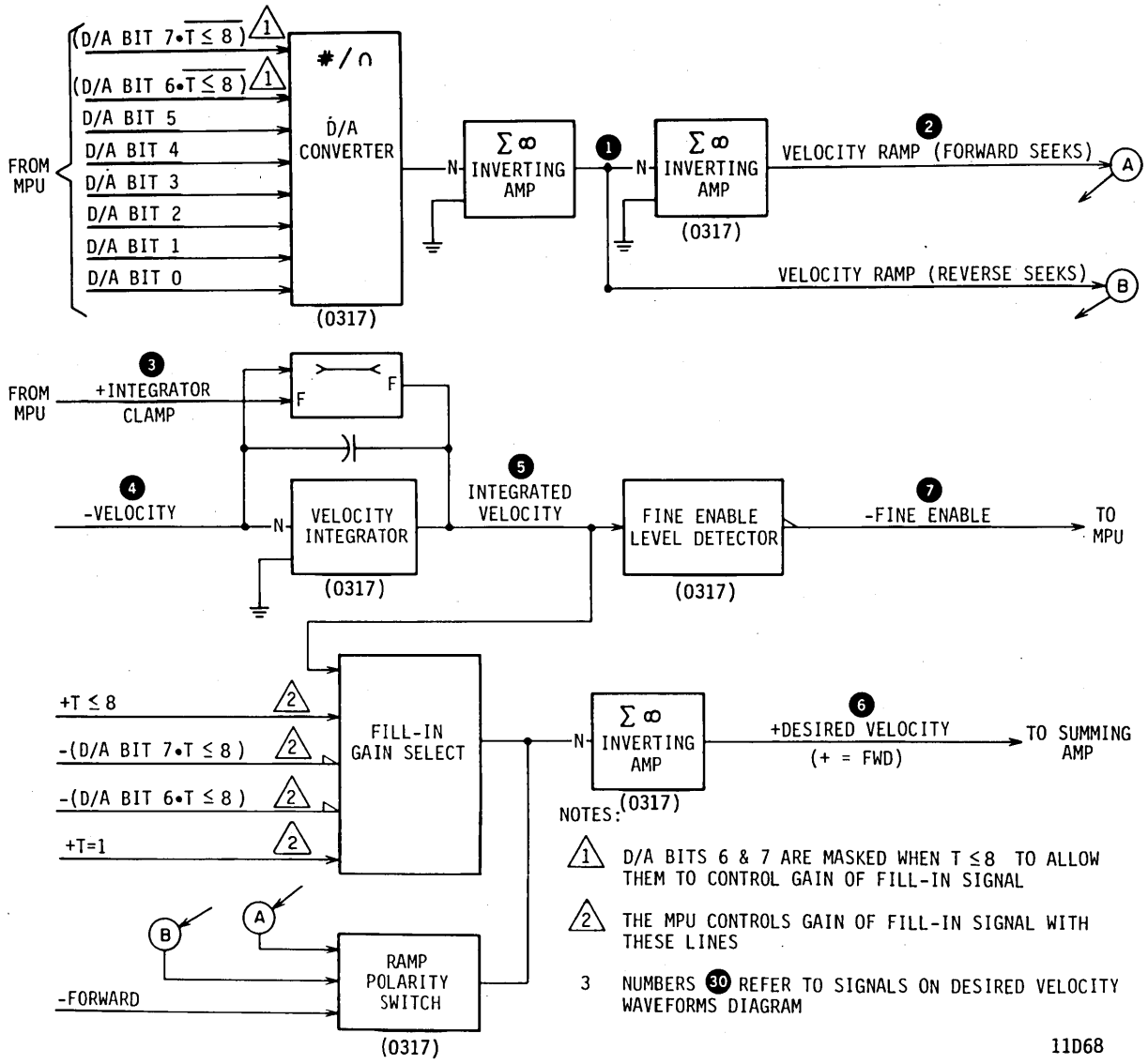
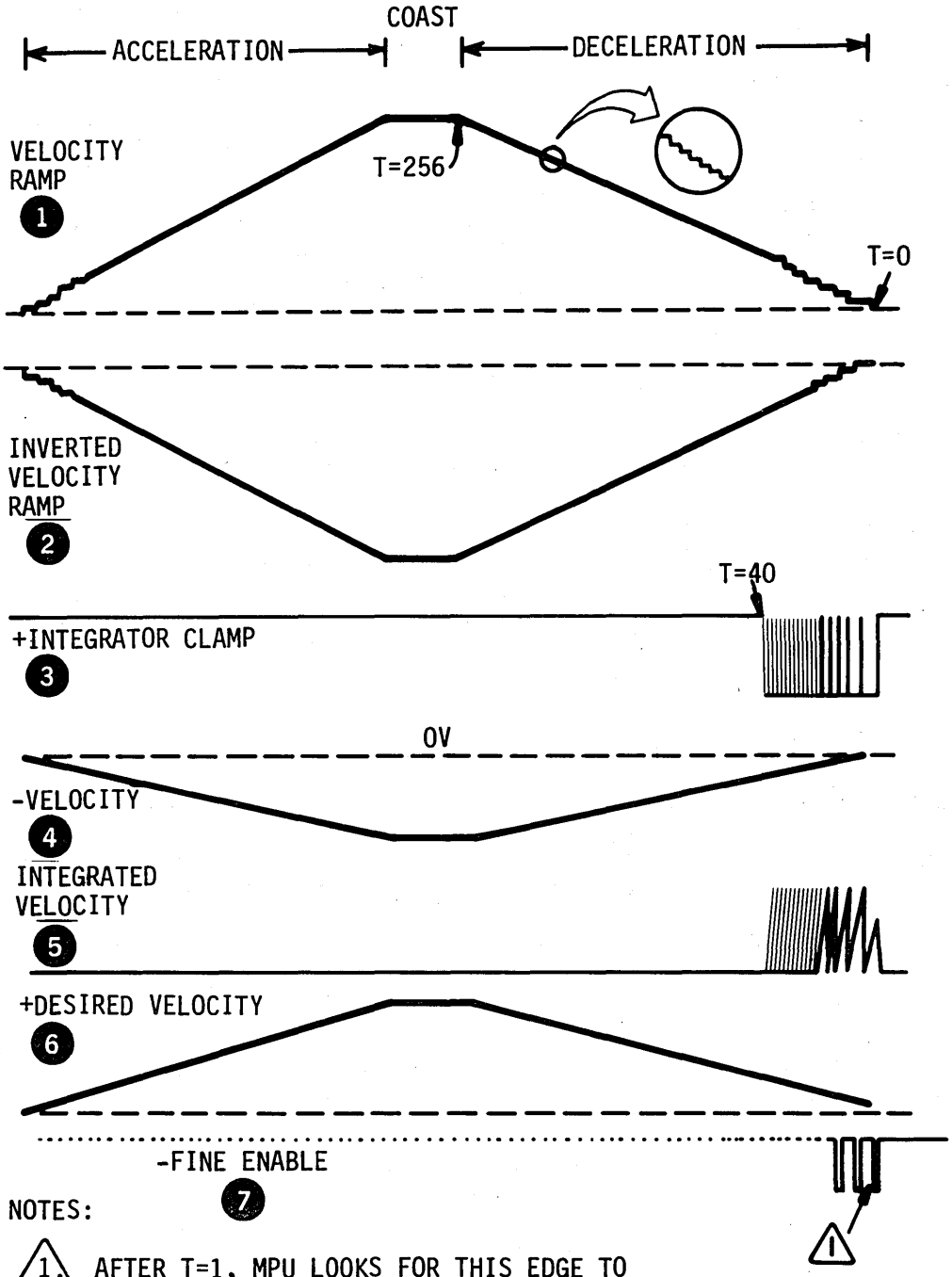


Figure 1-31. Desired Velocity Circuit



NOTES:

1. AFTER T=1, MPU LOOKS FOR THIS EDGE TO SWITCH SERVO TO FINE LOOP OPERATION.
2. NUMBERS (30) REFER TO SIGNALS ON DESIRED VELOCITY CIRCUIT DIAGRAM.
3. THESE WAVEFORMS APPLY TO LONG FORWARD SEEK.

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Figure 1-32. Desired Velocity Waveforms

The sawtooth from the Velocity Integrator compensates for the stepped nature of the D/A ramp by filling in the sudden changes in the ramp. When T<40, the sawtooth output is obtained by integrating the -Velocity signal from the velocity circuit. This output is clamped to zero each time a cylinder crossing occurs. D/A Bits 6 and 7 are reserved for controlling the degree of filling provided by the sawtooth in the final portion of the seek (when T≤8). These bits are set or cleared according to the ROM velocity table, but they are masked out of the D/A Converter input when T≤8. In the final tracks of the seek, when the velocity signal being integrated is reduced, the portion of the sawtooth applied to the +Desired Velocity signal is increased accordingly.

The sawtooth from the Velocity Integrator serves an additional purpose in the final track of coarse mode. Integrating velocity gives an indication of displacement. Each time the sawtooth reaches a specified value corresponding to a 1/2 track displacement from the last cylinder crossing, a level detector which monitors the sawtooth issues the -Fine Enable signal. With T≤1, the MPU looks for this signal and reacts by switching servo operation from the coarse mode to the settle-in mode.

Cylinder Pulse Detection

A Cylinder Pulse is generated each time the heads cross a servo track during the coarse seek operation. Cylinder pulses serve two purposes. First, they decrement Counter #2 in the PTM, keeping its difference count equal to the number of tracks to go in the seek; this points the MPU to the correct tabulated velocity value which is stored in ROM. Second, for T<40 the +Integrator Clamp line goes active during cylinder pulses to clamp the sawtooth output of the Velocity Integrator to zero. Thus, the sawtooth waveform returns to zero each time that the D/A Converter gets a revised input (see Desired Velocity Generation discussion).

During a seek, the Position signal from the Tribit Decoder alternates between positive and negative values (see Servo Surface Decoding discussion). Each zero-crossing of the Position signal corresponds to a cylinder crossing. Figure 1-33 provides a simplified logic diagram and waveforms for this circuit. The cylinder pulse detector uses four level detectors in conjunction with switching logic located in the Demodulator Logic Chip. The two level detectors, designated "A", monitor the +Position signal, and the two level detectors, designated "B", monitor the -Position signal. Each level detector switches its output signal at unique levels, based on its thresholds

and hysteresis. The "A" level detectors recognize zero-crossings and position peaks of one polarity by activating the +Cylinder Low A and the -Cylinder Peak A lines respectively. Similarly, the "B" level detectors recognize zero-crossings and position peaks of the other polarity by activating the +Cylinder Low B and the -Cylinder Peak B lines.

The four level detector outputs supply control signals to switching logic in the Demodulator Logic Chip. In developing the -Cylinder Pulses signal, this logic must sense a position peak prior to responding to a position zero-crossing. Figure 1-33 shows how transitions in the four input signals produce the changes in the -Cylinder Pulses signal. This design ensures that only one Cylinder Pulse is generated for each zero-crossing of the Position signal.

Velocity Measurement

A continuous indication of actuator velocity is needed during the coarse seek mode. The -Velocity signal is developed and introduced to the coarse loop so that the servo loop can force actual velocity to match desired velocity. The -Velocity signal is negative during a forward movement (positive during a reverse movement), and its amplitude is proportional to velocity.

As part of the First Load operation, the MPU does a calibration procedure (a series of 128-track seeks) where it adjusts the gain of the velocity measurement circuit in order to compensate for gain variations in the servo disk. The gain is adjustable in steps depending on which combination of the four gain control lines is set. Upon finding the optimum combination of settings, the MPU maintains that combination (output from PIA-0) until another First Load operation is necessary.

Figure 1-34 is a simplified block diagram of the velocity measurement circuits. Velocity measurement is a sequenced operation in which the switching control circuit selects different signal inputs for the Velocity Signal Generator and determines the operating mode of the Velocity Signal Generator.

The sequencing pattern repeats itself with every complete oscillation of the -Position signal. Each oscillation of the -Position signal has four distinct regions, as shown in figure 1-35. The positive peak region is followed by a linear region with constant falling slope. Then there is a negative peak region followed by a linear region with constant rising slope. The switching control circuit monitors the -Position signal with two level detectors, one that senses the positive peak region and another that senses the negative peak region. The

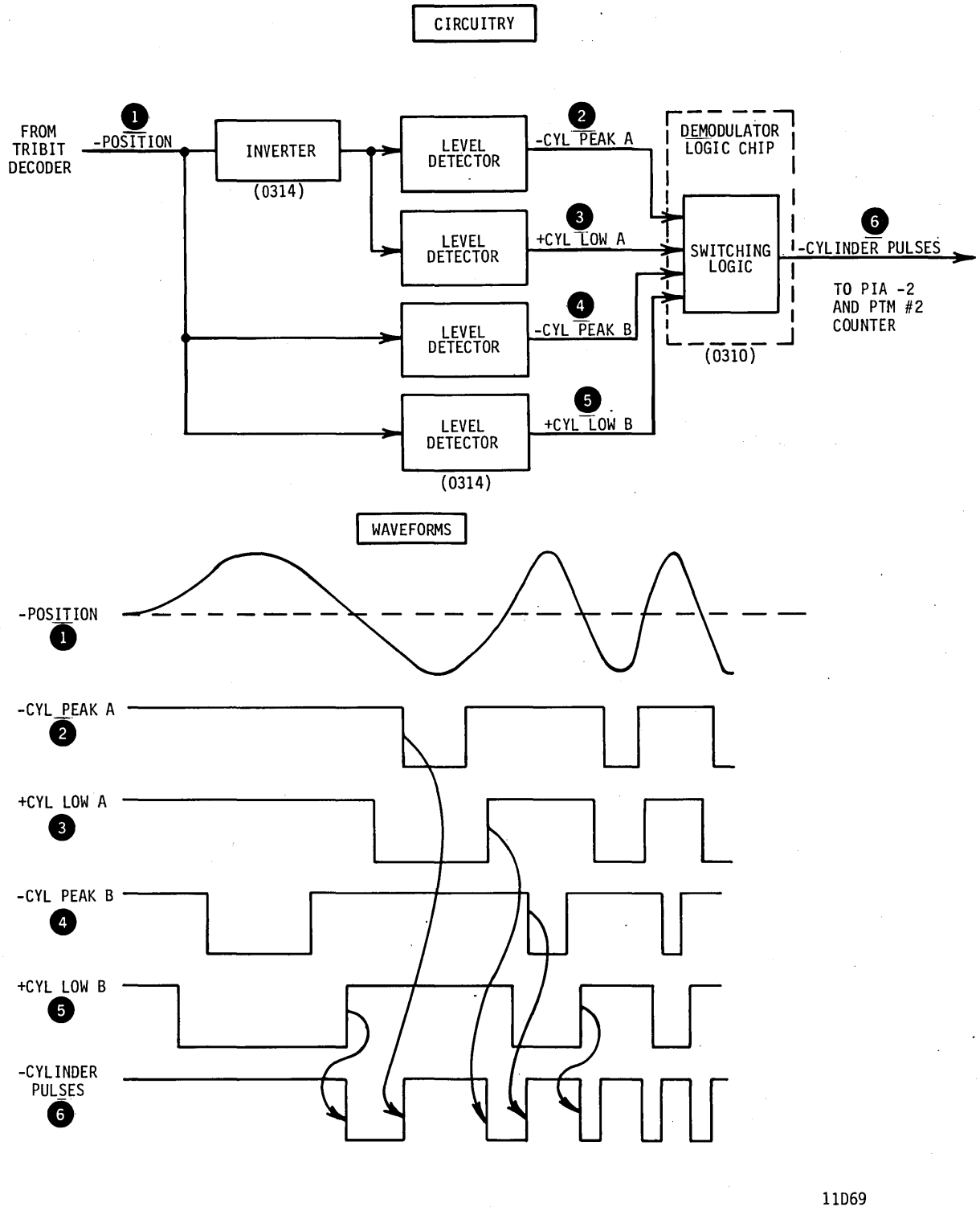


Figure 1-33. Cylinder Pulse Circuitry and Waveforms

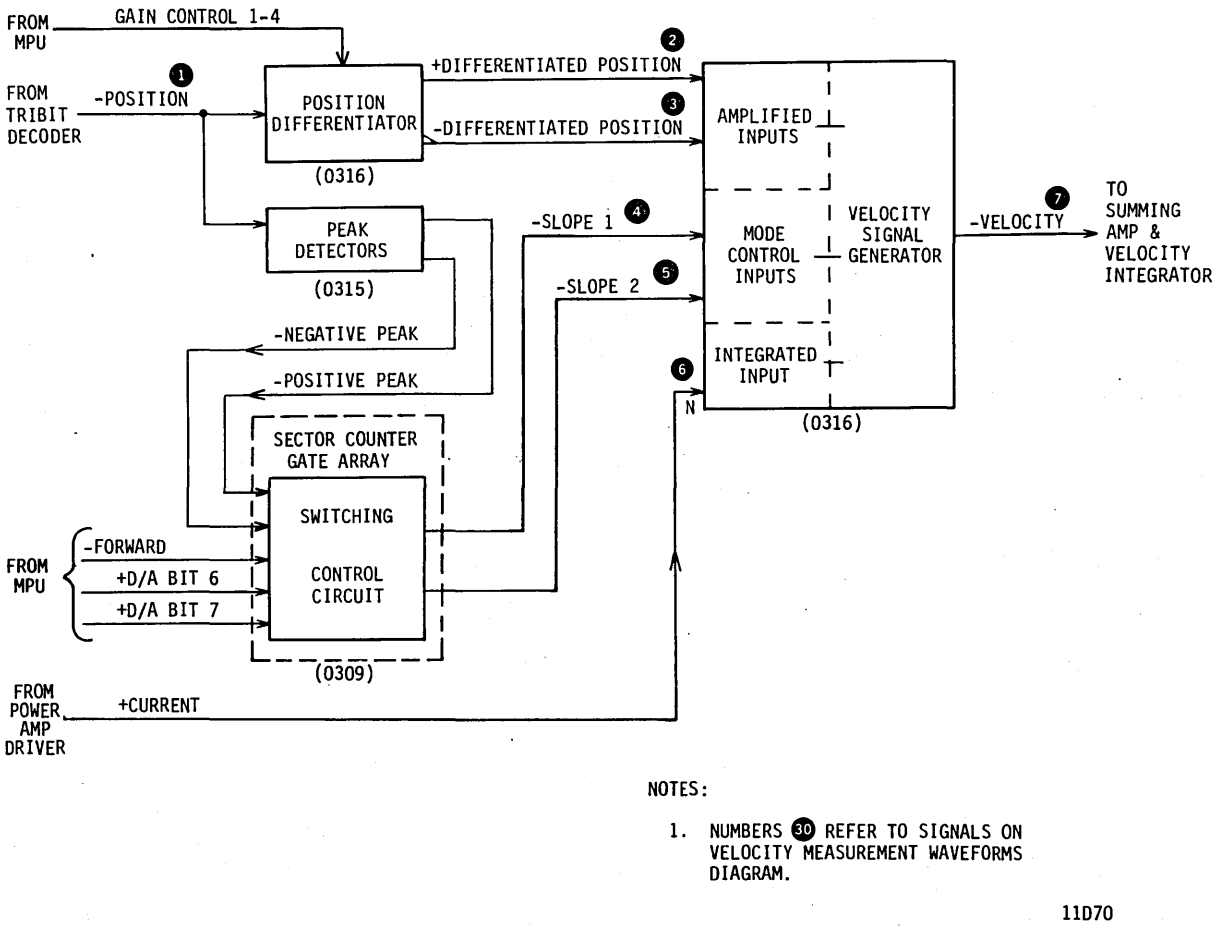


Figure 1-34. Velocity Measurement Circuits

-Negative/Positive Peak signals are used by the switching control circuit (in the Sector Counter Gate Array) to define the regions of the -Position signal. Through control lines -Slope 1 and -Slope 2, the switching control circuit regulates the Velocity Signal Generator.

In each sequence pattern, the switching control circuit activates one control line during one linear region and the other control line during the other linear region. During the linear regions, the differentiated position outputs are proportional to velocity because velocity is the time rate of position change. So during linear regions, the switching control circuit places the Velocity Signal Generator in the amplifying mode and selects the differentiated input of the proper polarity in each region. In the first linear region of the coarse

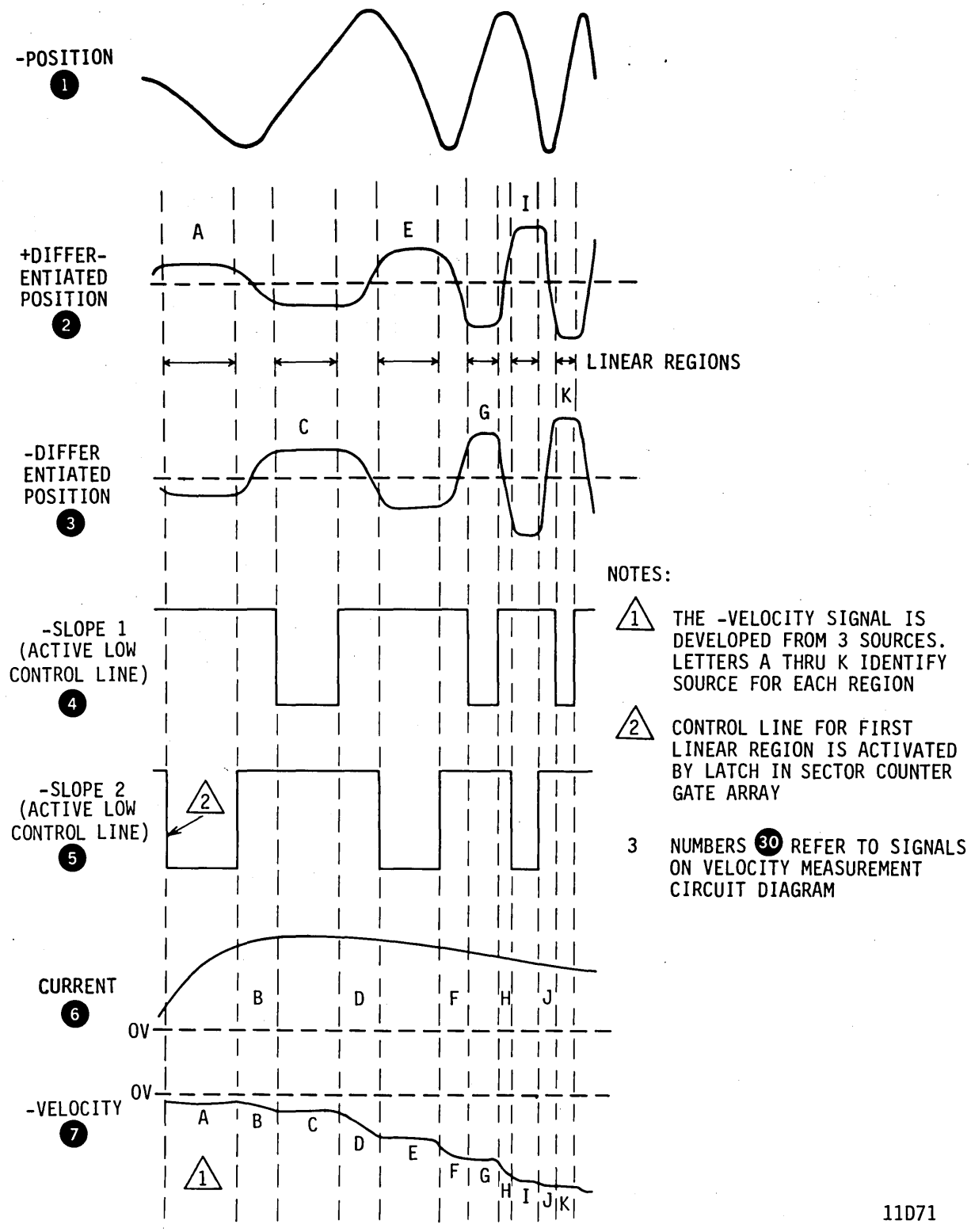


Figure 1-35. Velocity Measurement Waveforms

seek (the first 1/2 track), the MPU presets a latch in the switching control logic with signals on the +D/A Bit 6, +D/A Bit 7, and -Forward lines. Through the rest of the seek, the circuit is self-running. The detected position signal peaks alternately set and clear the latch, and the latch alternately activates the two control lines in successive linear regions. The proper input polarity to the Velocity Signal Generator is a function of the latch state and the level of the -Forward line; this makes the -Velocity signal polarity match the seek direction.

When the -Position signal is in the peak regions and thus neither control line is active, the switching control circuit allows the Velocity Signal Generator to integrate its Current input. This fills in the gaps in the -Velocity signal at times when no differentiated position signal is available.

The +Current signal is derived in the Power Amp Driver by amplifying the -Current Sense signal sampled by the voice coil. Any acceleration or deceleration of the actuator produced by the servo loop is proportional to this current. Velocity is the integral of acceleration; therefore, when the Velocity Signal Generator integrates the Current signal, it is deriving a velocity signal during Position signal peaks.

Summing Amp

The servo system operates, in each mode, to null the input to the summing amp. The MPU selects the signal input to the summing amp via PIA-1 by enabling one of two analog gates. In coarse loop operation, the +Coarse line is active, and velocity information is input to the Summing Amp. In fine loop operation, the -Settle In line is active and position information is input to the Summing Amp (see discussion of Fine Loop Operation).

The Summing Amp input in coarse loop operation is the sum of the +Desired Velocity and -Velocity signals. When measured velocity is equal to desired velocity, these signal inputs add to zero, and -Notch Filtered Desired Current, the output of the Summing Amp, is zero. With unmatched inputs, the -Notch Filtered Desired Current line has a voltage level that indicates both the magnitude and the polarity of actuator current that will bring the servo system into balance. Zener diodes in the feedback path of the Summing Amp prevent amplifier saturation by keeping the output amplitude between -10 volts and +10 volts. When -Notch Filtered Desired Current is negative, the resulting actuator current will accelerate the heads in a forward seek or decelerate the heads in a reverse seek.

Power Amp Driver

The Power Amp Driver generates In Drive or Out Drive currents as inputs to the Power Amp in response to the voltage level on the -Notch Filtered Desired Current line from the Summing Amp. Together, the Power Amp Driver and the Power Amp make up a current feedback amplifier. Through a feedback loop that monitors actuator current, the Power Amp Driver adjusts the current in the In Drive line or the Out Drive line as necessary to produce the actuator current specified by the -Notch Filtered Desired Current signal. Figure 1-36 shows the Power Amp Driver in simplified form, and the following paragraphs provide a detailed description of its circuit operation.

The Current Sense signal, an analog voltage proportional to actuator current, is applied to an op amp which amplifies it to produce the +Current signal. The +Current signal is a positive voltage when the actuator exerts inward force and a negative voltage when the actuator exerts outward force. At a second op amp, the +Current and -Notch Filtered Desired Current signals are added, inverted and amplified to produce the +Current Error signal. The +Current Error signal is zero when the actuator current matches the desired current specified by the servo loop. A mismatch makes the +Current Error signal go positive or negative as required to bring the actuator current to the desired value. In this manner, the Power Amp Driver and Power Amp are a closed loop current amplifier.

The +Current Error signal is input to an analog gate which is enabled by the -Enable Power Amp signal. The -Enable Power Amp signal is latched in the Sector Counter Gate Array. Prior to starting the drive motor or loading the heads, the MPU pulses the +T≤8 and -Forward lines to reset the latch and activate the enable. The latch is set to remove the enable either by the MPU (after a head retract) or by a voltage fault. In the case of a voltage fault, the servo remains disabled until the fault condition is cleared. With the analog gate enabled, the +Current Error signal is fed to the inputs of the In and Out Driver transistors.

When the error voltage is positive, it cuts off the Out Driver transistor and regulates the current in the In Drive output line. When the error voltage is negative, it cuts off the In Driver transistor and regulates the current in the Out Drive output line. When the error voltage changes sign, it reverses the direction of actuator current, thereby reversing the force applied to the actuator.

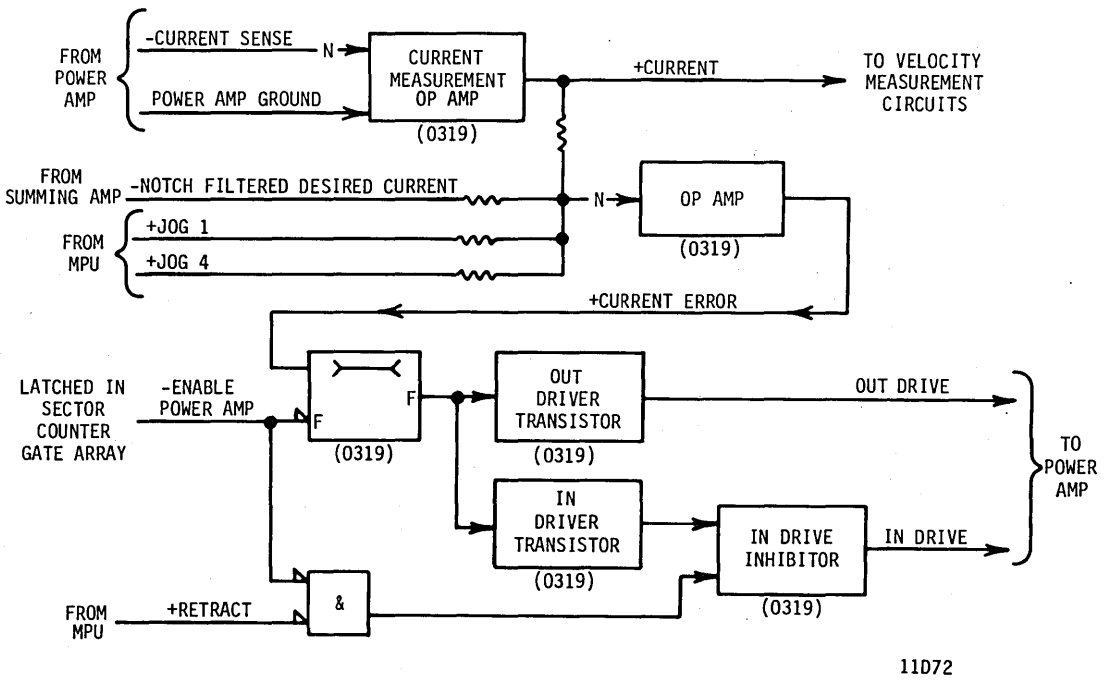


Figure 1-36. Power Amp Driver Circuitry

The +Jog 1 and +Jog 4 inputs allow the MPU to move the heads slightly while the drive motor is being started. They supply a negative offset to the +Current Error signal, and the actuator is forced outward against its crash stop. In this way, contact between the heads and the landing zone portion of the disk is broken before the disks begin to rotate. During normal servo operation, the MPU keeps the jog inputs inactive.

Power Amp

The Power Amp, acting on inputs from the Power Amp Driver, produces the actuator current required by the servo loop. Figure 1-37 is a simplified drawing of the Power Amp circuitry.

When positive actuator current is required, the Power Amp Driver generates current in the In Drive line. The In Direction Amplifier amplifies this input current and regulates (positive) current flow from ground through the sampling resistor and the actuator coil to -24 V. The negative voltage on the Current Sense line is supplied to the Power Amp Drive to complete the loop regulating the amplifier (see discussion of Power Amp Driver). In direction actuator current forces the actuator to accelerate during a forward move and to decelerate during a reverse move.

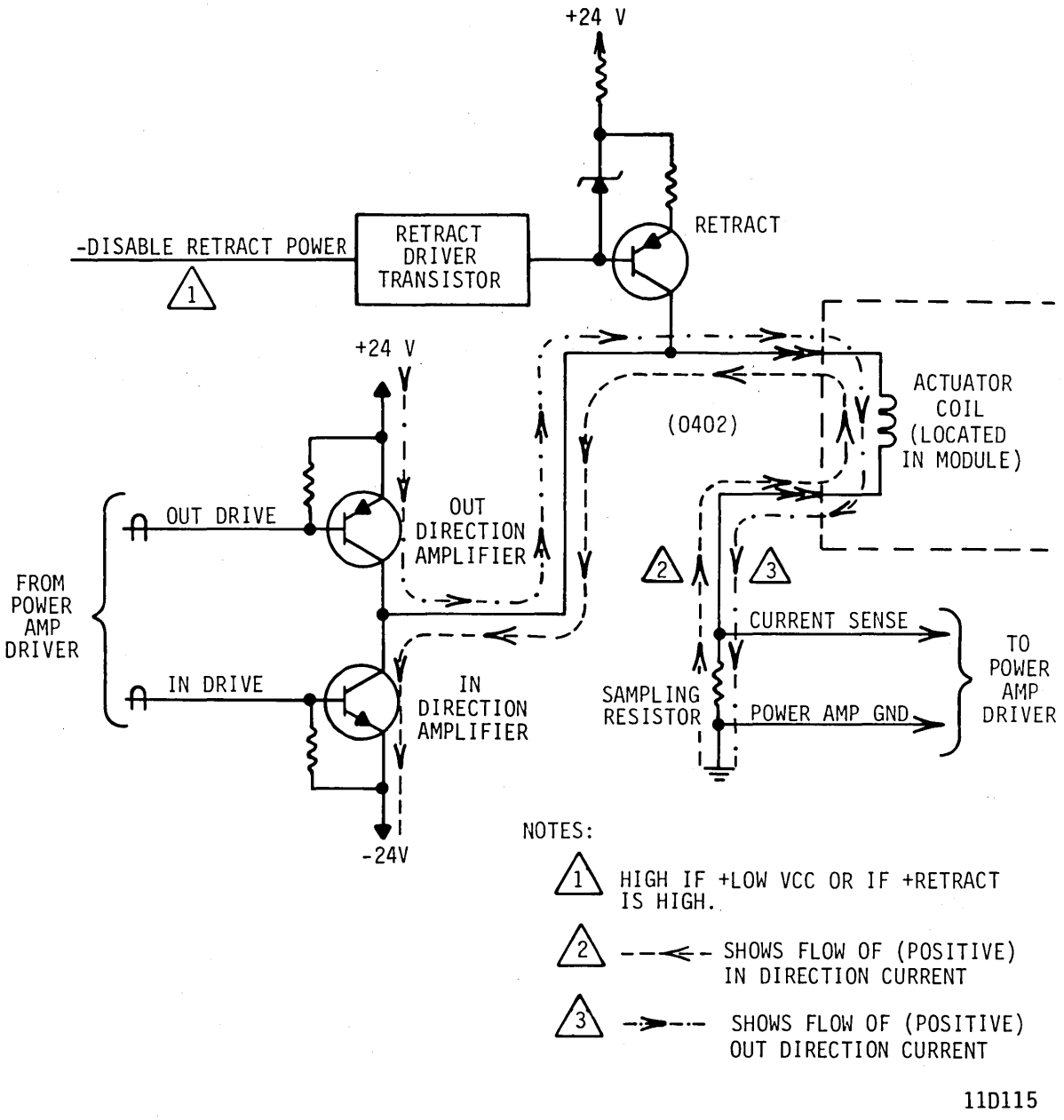


Figure 1-37. Power Amp Circuitry

When negative actuator current is required, the Power Amp Driver generates current in the Out Drive line. The Out Direction Amplifier amplifies this input current and regulates (positive) current flow from +24 V through the actuator coil and the sampling resistor to ground. In this case, the voltage on the Current Sense line is positive. Out Direction actuator current forces the actuator to accelerate during a reverse move and to decelerate during a forward move.

During retract operations, the Retract Power Amplifier regulates actuator current. This operation is discussed under Retract Control Circuitry.

Fine Loop Operation

General

The servo system shifts from the coarse loop to the fine loop when there is 1/2 track remaining in the seek. Fine loop operation continues until the beginning of the following seek. Figure 1-38 is a simplified block diagram of the fine loop circuitry. Discussion of the fine loop is presented in the following topics:

- Position Error Generation
- Fine Loop Actuator Movement

Position Error Generation

In fine loop operation, the servo system adjusts the position of the actuator to null the input signal to the Summing Amp. The Summing Amp input developed for fine loop operation is different for settle in and for track-following modes. However, both of these error signals basically derive from the +Position signal from the Tribit Decoder.

At the start of a seek, the MPU sets or clears the +Slope input to the Tribit Decoder to ensure that +Position goes positive as the heads move inward and negative as the heads move outward from their destination track. The +Position signal is zero with the heads exactly on track. This relationship is true for every destination track on the disk. Thus, with some modification, +Position is a suitable error signal for the Summing Amp in the fine loop. The modification takes into account the following considerations:

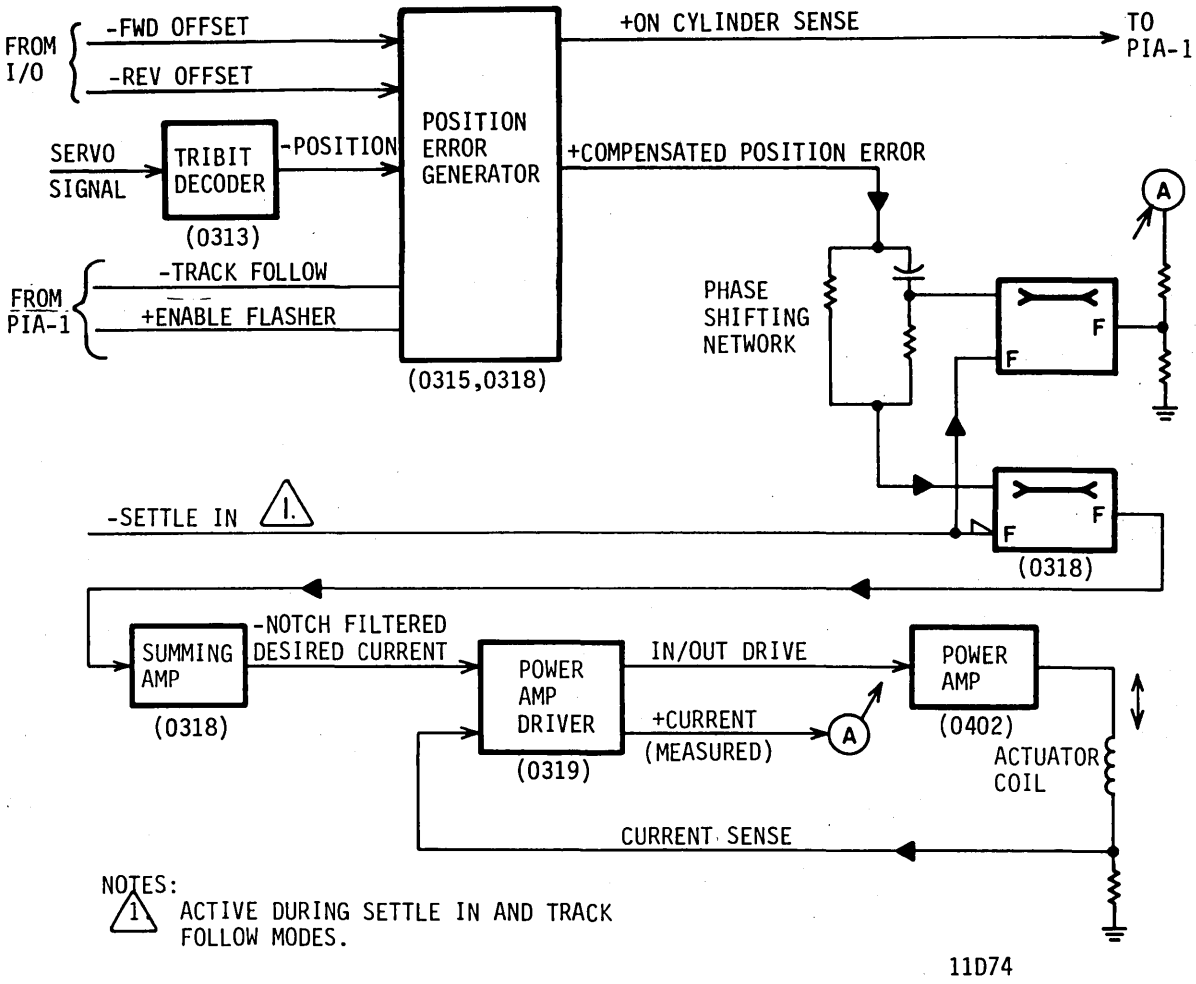


Figure 1-38. Fine Loop Block Diagram

- Stability of fine servo loop -- requires the addition of a differentiated correction to the error signal.
- Servo offsets -- allow the controller to reposition the heads to either side of track center to recover read errors.
- Increased gain in track-following mode -- gives the servo more responsive control when keeping the heads on track.

Figure 1-39 shows the position error circuitry in simplified form.

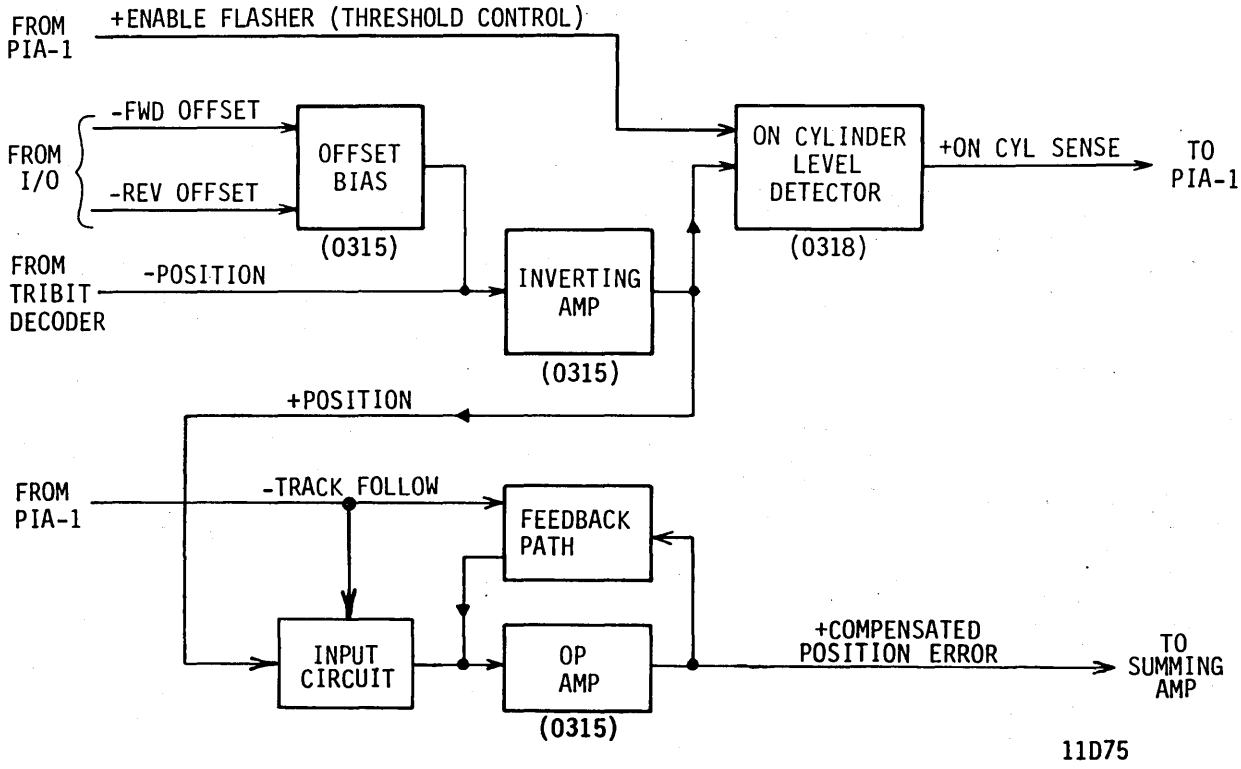


Figure 1-39. Position Error Circuitry

The position error circuitry consists of two op amps and a level detector. The first op amp inverts -Position and applies it with an optional offset to the second inverting op amp and the level detector. An offset, a dc shift of the position signal, results when the controller issues a Servo Offset command in order to recover marginal read data. When the I/O Gate Array decodes Servo Offset Plus (Tag 3 and Bus bit 2), it activates -FWD Offset, and the Offset Bias circuit shifts the position signal about 0.75 V negative. When the I/O Gate Array decodes Servo Offset Minus (Tag 3 and Bus bit 3), it activates -REV Offset, and the Offset Bias circuit shifts the position signal about 0.75 V positive. Servo Offset Plus displaces the heads inward from track center.

The +Position signal from the first op amp inputs both the On Cylinder level detector and the second op amp. The second op amp develops the +Compensated Position Error signal which is used as an error signal for both the settle-in and track-following modes. This op amp has an analog gate in its feedback path that makes its operation different in settle-in mode than it is in track-following mode.

For both settle-in and track-following, the +Compensated Position Error signal passes through a phase-shifting network before being applied to the Summing Amp input. This network, shown in figure 1-38, consists of a resistor which is in parallel with a series-RC differentiator. Adding a differentiated component to the error signal improves the stability of the fine servo loop. Prior to settle-in (T>1/2 track), an analog gate presets the capacitor charge by sampling the +Current signal to permit a smooth transition from the coarse to the settle-in mode. When -Settle-In goes active, it disables that analog gate, allowing the phase-shifting network to operate. A second analog gate is switched on to pass the error signal on to the Summing Amp input.

The MPU allows 0.8 ms for settle-in before switching to the track-following mode. In the track-following mode, the servo maintains the heads on cylinder until a new seek command appears. When -Track Follow goes active, an analog gate modifies the input circuit and feedback path for the second op amp in the position error circuitry. This change increases the low-frequency gain of that amplifier to provide tighter servo control in track-following.

The On Cylinder Sense level detector informs the MPU when to set the On Cylinder FF (in the track-following mode). The detector has two thresholds, controlled by the +Enable Flasher line from PIA-1. Prior to settle-in, the MPU activates the +Enable Flasher line, making the detector circuit sensitive to any settle-in problems. When the position signal drops to the threshold level of the detector, the detector activates the +On Cylinder Sense signal to generate an interrupt via PIA-1. Once the +On Cylinder Sense signal is steadily active, the MPU responds to this interrupt by issuing On Cylinder status to the I/O Gate Array. With the heads on cylinder, the MPU drops the +Enable Flasher signal to make the On Cylinder Sense level detector less sensitive to changes in the position signal.

Thus, the Summing Amp receives a different input in each seek mode. Response of the servo circuitry to the Summing Amp input is summarized in the next topic.

Fine Loop Actuator Movement

In the fine loop, as in the coarse loop, the Summing Amp develops the -Notch Filtered Desired Current signal in response to its input error signal. The Power Amp Driver and Power Amp, acting as a current feedback amplifier, develop current in the voice coil to match the -Notch Filtered Desired Current input signal. This voice coil current moves the heads toward track center. As the heads move toward track center, the position

error signal goes to zero. The loop is balanced when the heads are at track center and the Summing Amp input is nulled. With a positive Summing Amp input, -Notch Filtered Desired Current is negative; this results in positive voice coil current and an inward force on the heads.

For details about this circuit operation, refer to the following topics presented under Coarse Loop Operation:

- Summing Amp
- Power Amp Driver
- Power Amp

Retract Control Circuitry

The retract control circuitry moves the actuator outward until the heads are located in the landing zone. As shown in figure 1-40, the -Disable Retract Power signal determines whether the retract control circuitry is operating. When the signal is low, the retract amplifier is cut off. When the signal is high, the retract amplifier acts as a source of out direction current. The amplifier is connected to +24 Vdc from the power supply, and the voltage provided by the retract capacitor. The amplifier develops voice coil current from the source with the highest potential.

The retract amplifier is biased into operation either when the MPU issues the Retract command or when the +5 Vdc supply voltage drops enough to activate the +Low Vcc signal. The MPU uses the Retract command for normal head retraction before powering down the spindle or if it detects low spindle speed.

Conditions that enable the retract amplifier also inhibit the In Drive current from the Power Amp Driver. The In Drive Inhibitor is activated if either the +Retract line or the -Enable Power Amp line goes high. The second signal automatically goes high if a voltage fault occurs. Cutting off the In Direction Amplifier ensures that the retract actuator current will be unopposed by in direction current in the power amplifier.

Load Control Circuitry

Loading the heads consists of moving them inward from the landing zone to the data zone. In this process, the MPU controls the force exerted by the actuator. The force is produced by current pulses, generated by the load control circuitry. As

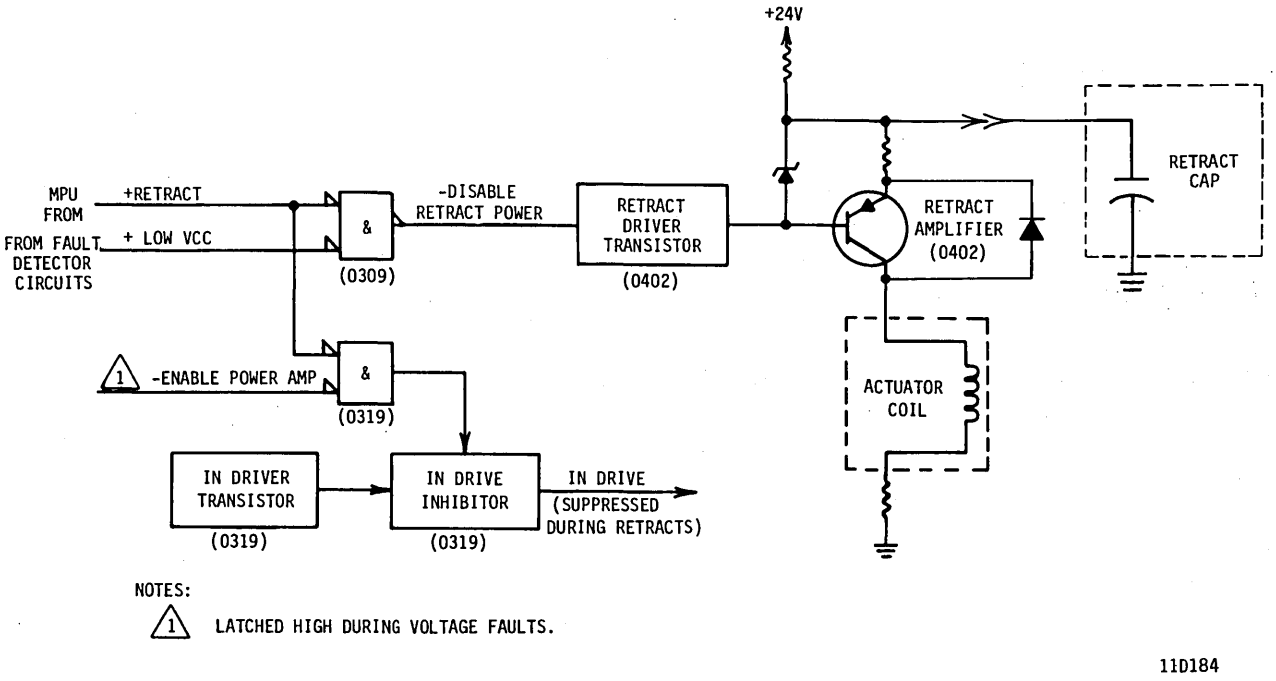


Figure 1-40. Retract Circuitry Block Diagram

shown in figure 1-41, the load control circuitry uses portions of the coarse servo loop. Unlike coarse servo control, which feeds back measured velocity in the servo loop, load control is accomplished without servo feedback.

Figure 1-41 shows the MPU inputs to the load control circuitry. Throughout the process, the MPU holds +D/A Bits 0-7 active to establish the amplitude of the current pulses, and, except for the final current pulse, it holds the -Forward line active. The desired velocity generator supplies a constant bias on the +Desired Velocity line. By switching the +Coarse signal on and off, the MPU causes the bias on the +Desired Velocity line to be applied as pulses to the summing amp. The power amp driver and power amp develop pulses of coil current in response.

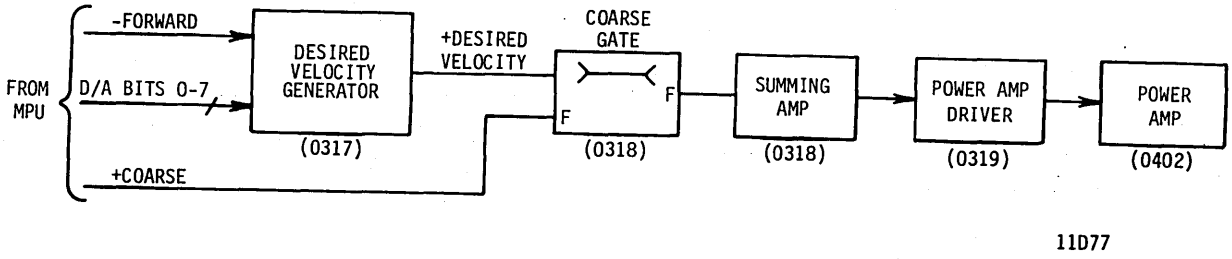


Figure 1-41. Load Circuitry Block Diagram

Following its program, the MPU begins the load with a long pulse to start the actuator moving, followed by a series of shorter pulses to sustain that motion. While generating the shorter pulses, the MPU monitors the -Demodulator Active line. As the heads move out of the landing zone, the Tribit signal is detected. When the tribit decoder becomes synchronized, it issues the -Demodulator Active signal. The MPU allows a 40 ms delay and then counts 5 cylinder pulses to verify that the tribit decoder is reliable. At this point, the MPU switches the -Forward line high and creates a long pulse of out direction current to stop the actuator motion.

TYPES OF SEEKS

General

The drive has four basic types of seeks: the load operation, normal seek, return to zero (RTZ) seek, and retract operation. The load and RTZ operations use both the outward and inward movements to move the actuator to track 0. The retract operation is an outward movement that moves the heads to the landing zone beyond the outer guard band. Normal seek operations can be either inward or outward movements, depending upon where the new address is located, relative to the present address. The four basic seek operations are discussed in the following text.

Load Operation

The load operation is an MPU-controlled sequence that starts the drive motor, moves the heads from the retracted position to track 0, and calibrates the velocity measurement circuitry. A load operation cannot take place until power on initialization is successfully completed. Refer to the Power Functions discussion for details about power on initialization. The load operation is described in the following paragraphs and is flowcharted in figure 1-42.

When power on initialization is complete, the MPU waits for start conditions before initiating the load operation. The MPU requires that the START switch is placed in the Start position and (in remote operation) that Sequence Pick and Sequence Hold are available from the controller. Once Sequence Pick is received, a delay circuit in the I/O circuitry activates +Start Enable after an interval equal to five seconds multiplied by the drive address.

With start conditions present, the MPU starts the drive motor. During the first three seconds of motor acceleration, the MPU causes the actuator to move outward against the soft carriage stop. During this motion, called a jog, the heads begin flying over the landing zone. Prior to the jog, the MPU pulses the -Forward and +T≤8 lines to latch the +Enable Power Amp signal coming from the Sector Counter Gate Array. In addition, the MPU issues the Unlock Actuator command via PIA-1 which in turn activates the solenoid allowing the actuator to move forward. The MPU controls the jog current by activating the +Jog 1 and +Jog 4 lines to the power amp driver.

The MPU starts the drive motor by issuing the Motor Run command to the power supply (via PIA-1) and requires that the -Speed OK line from the motor speed detection circuit goes low after a delay from 3 to 7 seconds. With Speed OK, the MPU doublechecks motor speed by counting -Motor Sensor pulses entering the programmable timer (PTM #3). The MPU continues to check motor speed until the speed is between 1950 and 2050 r/min.

Prior to loading the heads, the MPU initializes the Gain Control lines for the velocity measurement circuitry. (These lines are calibrated later in the load operation). Also, the MPU ensures that the +Fault line is inactive and that -Demodulator Active line is high. Because the landing zone is located beyond the outer guard band, the heads must move forward before a servo signal is detected.

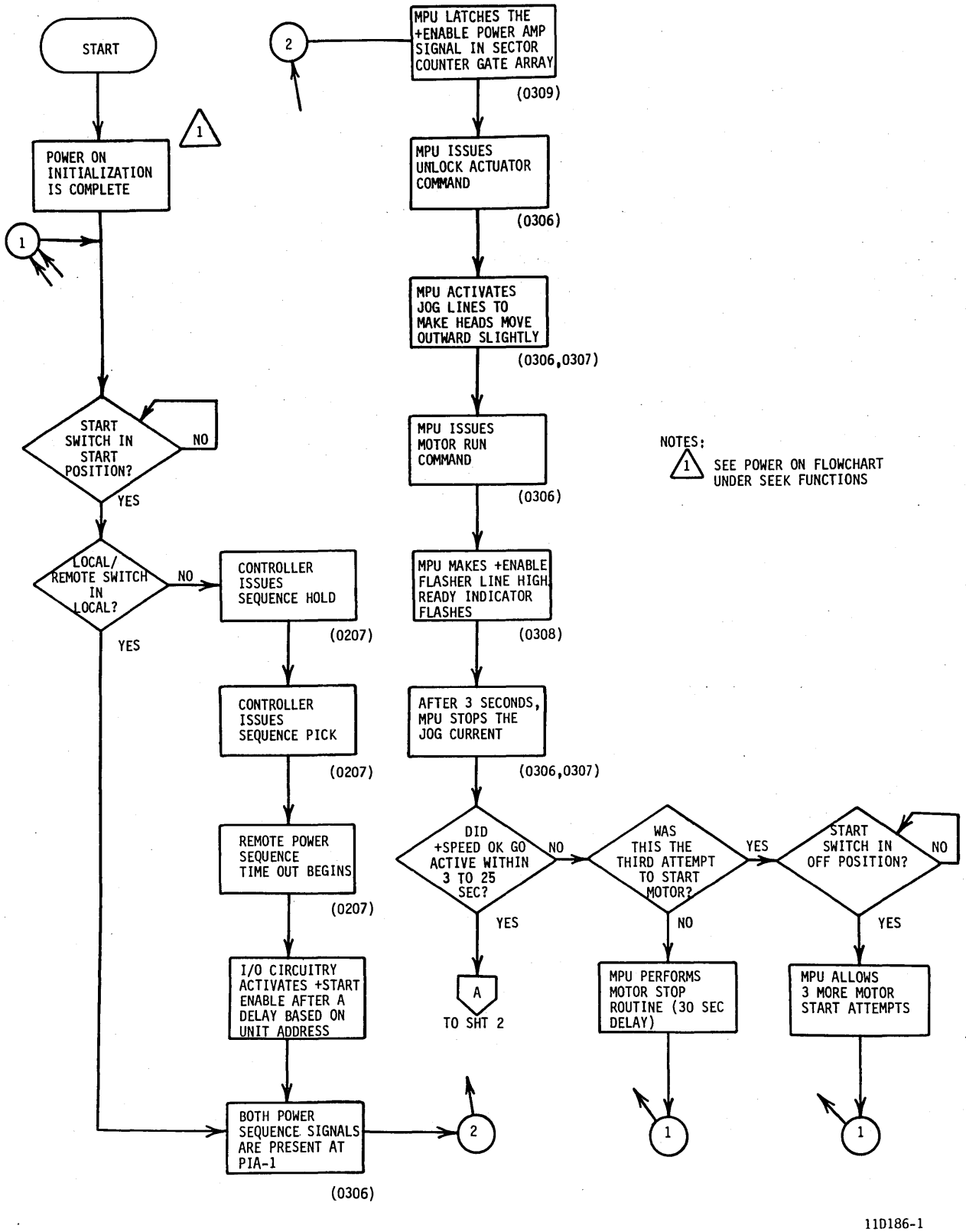


Figure 1-42. Load Operation Flowchart (Sheet 1 of 4)

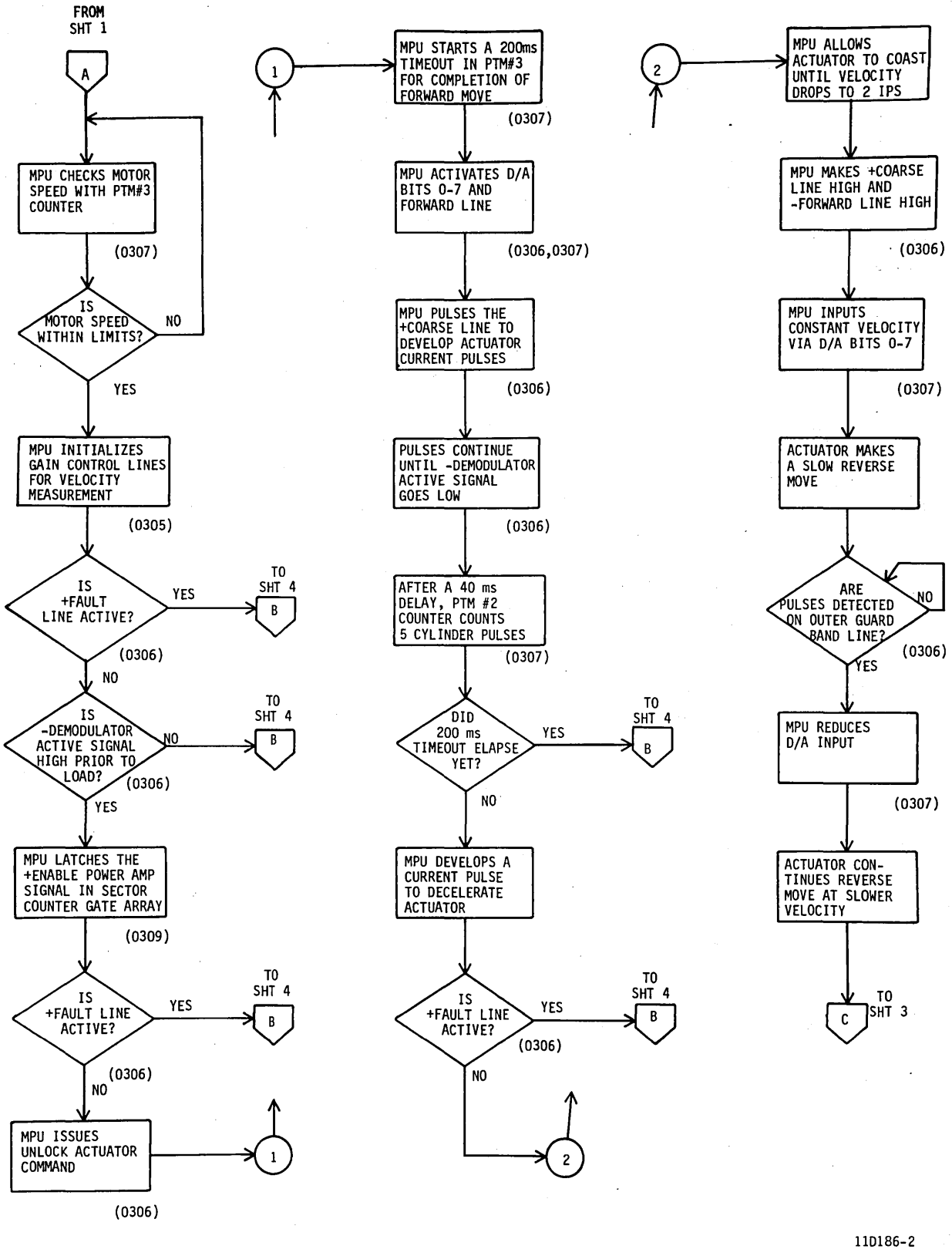


Figure 1-42. Load Operation Flowchart (Sheet 2)

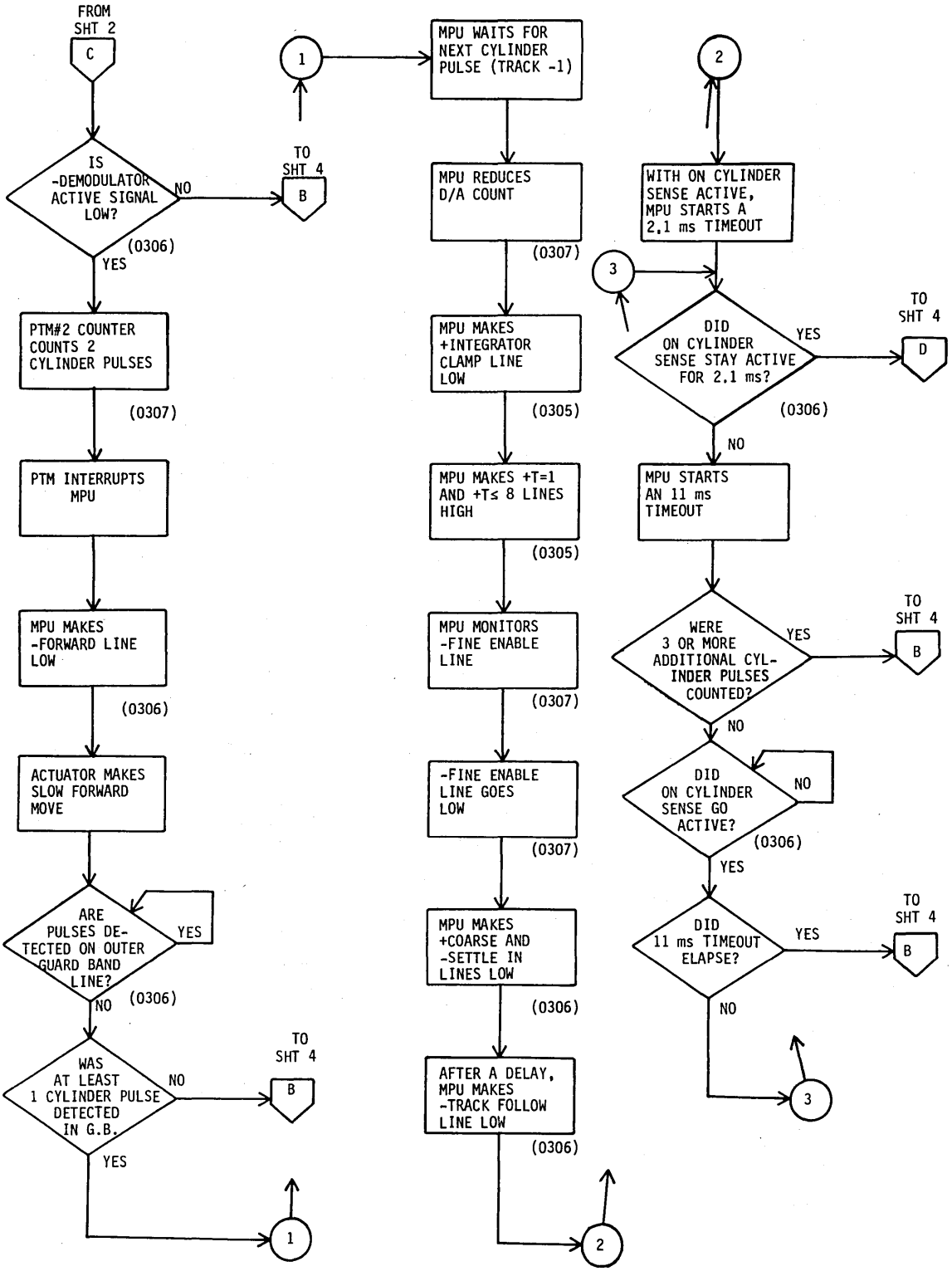


Figure 1-42. Load Operation Flowchart (Sheet 3)

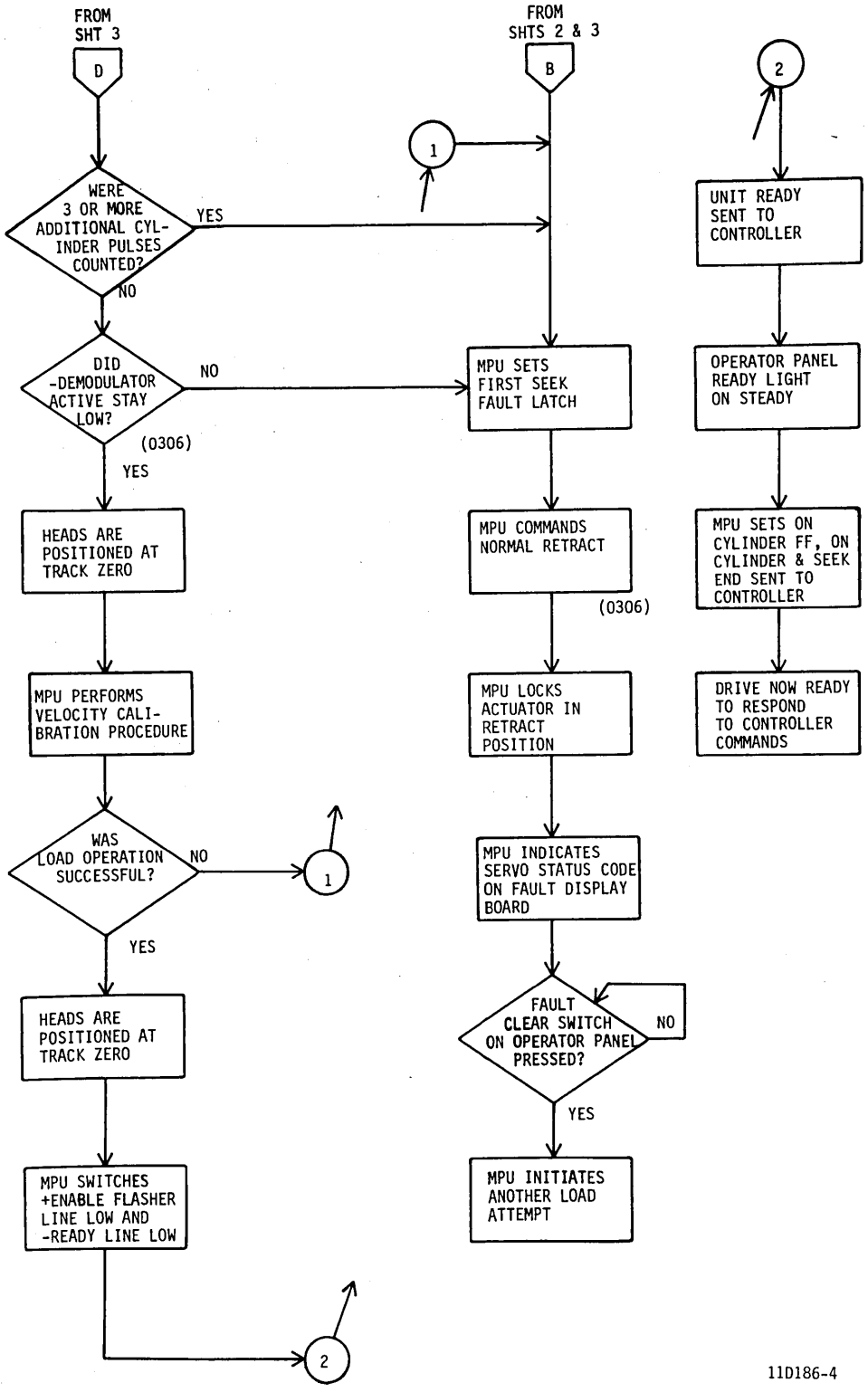


Figure 1-42. Load Operation Flowchart (Sheet 4)

To start the heads moving inward, the MPU latches the +Enable Power Amp signal in the Sector Counter Gate Array and unlocks the actuator. As discussed under Load Control Circuitry, the MPU develops current pulses that force the actuator to move forward from the landing zone. Figure 1-43 shows the carriage trajectory during the load seek. Once the -Demodulator Active signal goes low, indicating that the tribit decoder has locked in the servo signal, the MPU stops issuing current pulses, delays 40 ms, and begins counting cylinder pulses using the programmable timer (PTM #2). After counting 5 cylinder pulses, the MPU uses the load control circuitry to develop a decelerating current pulse.

At this point, the actuator is floating freely over the data zone. Throughout the forward move, the MPU uses a timer to ensure that the move is complete within 200 ms. If the timeout occurred or if the +Fault line went active during the move, the MPU sets the First Seek latch in the I/O Gate Array and lights the front panel FAULT indicator.

After waiting for the actuator velocity to drop to two inches per second, the MPU uses the coarse servo loop to move the heads outward into the outer guard band. To do this, the MPU switches the +Coarse line high and the -Forward line high. The MPU inputs the D/A converter with a constant desired velocity via D/A bits 0-7 from PIA-2.

Once the heads reach the outer guard band, the MPU reduces the D/A input, and the actuator continues to move outward at reduced velocity. The MPU verifies that the -Demodulator Active signal remains low, and it uses the programmable timer (PTM #2) to monitor cylinder pulses.

When PTM #2 has counted the two cylinder pulses for this move, it interrupts the MPU. The MPU reacts by issuing the Forward command to make the heads seek inward. The MPU requires that one cylinder pulse appears before the Outer Guard Band signal goes inactive (or it sets the First Seek fault latch). After the Outer Guard Band signal goes inactive, the MPU waits for one additional cylinder pulse representing the last track crossing before track 0.

When this cylinder pulse interrupts the MPU, the MPU reduces the D/A Converter velocity signal further (via D/A bits 0-7) and activates the Velocity Integrator by clearing the +Integrator Clamp line. The MPU also sets the +T=1 and the +T$\leq$8 lines to control the level of Integrated Velocity contributing to the Desired Velocity signal. With a constant D/A input from the MPU and the Velocity Integrator ramping up, the Desired Velocity signal approaches zero as the Integrated Velocity signal subtracts more and more from the D/A Converter velocity signal.

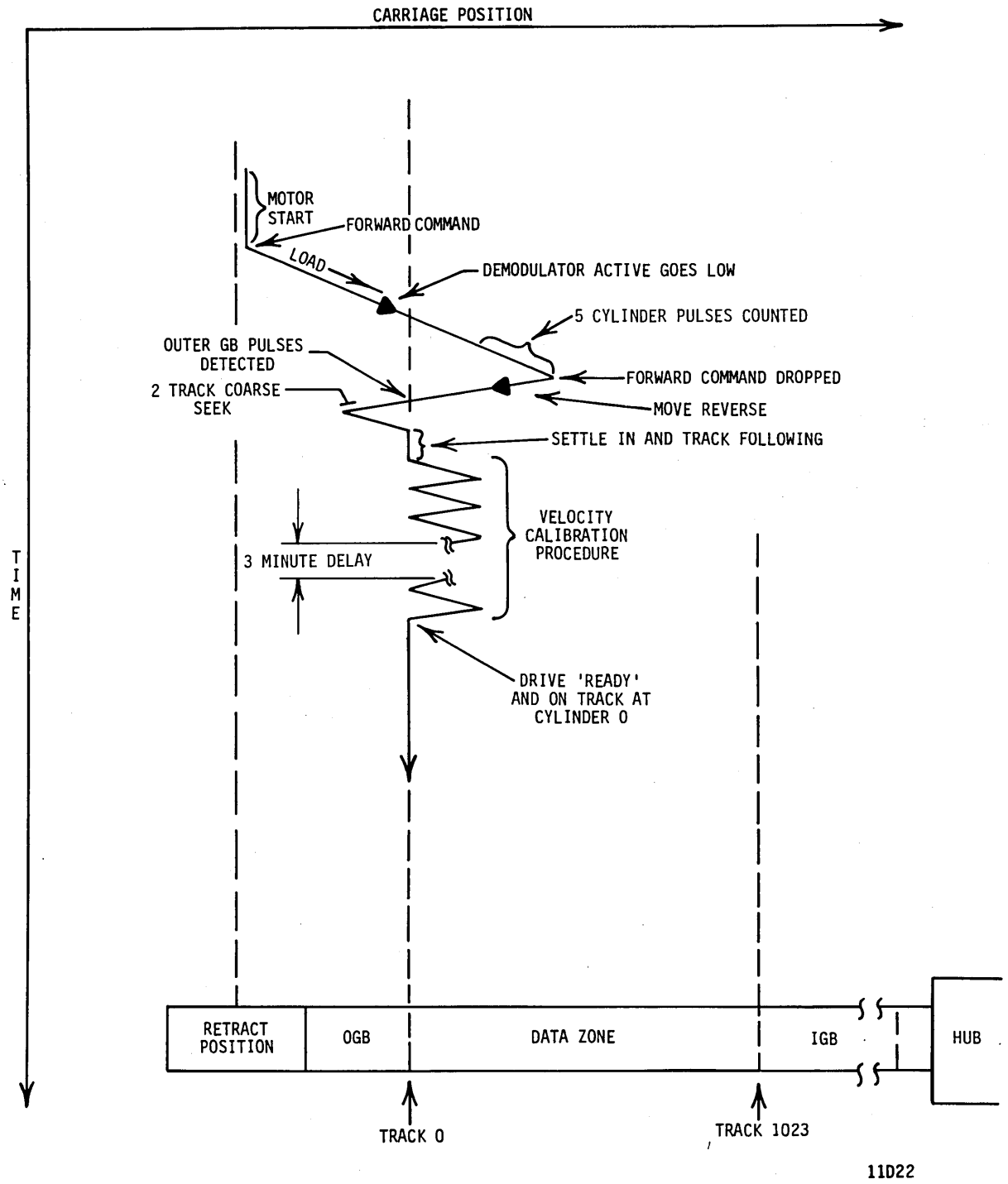


Figure 1-43. Load Seek Trajectory

The MPU monitors the -Fine Enable signal. This signal goes low with approximately 1/3 of a track to go. The MPU reacts by switching the +Coarse and -Settle In signals low via PIA-1. This places the servo in the first (track-capture) phase of the fine servo loop.

After a 0.8 millisecond delay, the MPU issues the Track Follow command via PIA-1. The Track Follow signal adds a low frequency gain boost to the positioning loop. Once the On Cylinder Sense signal goes active, the MPU allows a 2.1 millisecond timeout to ensure that the actuator has settled on track. During this interval, the MPU monitors the On Cylinder Sense signal. If that signal goes inactive, the MPU allows 11 milliseconds for it to go active again. In this case, the 2.1 millisecond interval repeats to ensure that On Cylinder Sense remains active. In either interval, if three or more cylinder pulses are counted, this indicates excessive overshoot, and the MPU sets the First Seek fault latch and terminates the load operation.

When On Cylinder Sense has stayed active for 2.1 milliseconds, the MPU ensures that -Demodulator Active is still low (indicating a reliable servo signal) prior to starting the velocity calibration procedure. In the velocity calibration procedure, the MPU commands a series of 128-track repeat seeks where it adjusts the gain of the velocity measurement circuit in order to compensate for gain variations in the servo disk. The gain is adjustable in steps depending on which combination of the four gain control lines is set. Upon finding the optimum combination of settings, the MPU maintains that combination (output from PIA-0) until the load operation is repeated.

After a 3 minute delay following the velocity calibration procedure, the heads are positioned at track 0. If the load operation was successful, the MPU issues the -Ready signal at PIA-2 and clears the +Enable Flasher signal at PIA-1. With -Ready signal low, the front panel Ready indicator lights, and Unit Ready status appears on the interface. Also, by inactivating the +Enable Flasher line, the MPU reduces the sensitivity of the On Cylinder Sense level detector while the heads are on cylinder. The MPU sets the On Cylinder FF in the I/O Gate Array, causing On Cylinder and Seek End status to appear on the interface. The MPU then waits for further instructions from the controller.

If the load operation was unsuccessful, the MPU performs a normal retract, provides a servo status code on the fault display board, sets the First Seek fault latch, and lights the front panel FAULT indicator. This fault can be cleared only by operation of the Fault Clear switch. Pressing the Fault Clear switch initiates another load attempt with a maximum of three tries allowed by the MPU.

Normal Seek

Normal seeks are initiated by controller command and implemented by the drive servo circuitry. The normal seek is the operation used to move the heads from one location to another on the disk surface. The same track can also be selected, but a zero track seek requires no actuator movement and the operation is handled by the I/O Gate Array.

The normal seek occurs in two directions, reverse (from the center towards the outer edge) and forward (from the outer edge towards the center). Going from a higher-numbered track to a lower-numbered one involves an out direction movement of the actuator, while going from a lower-numbered track to a higher-numbered one involves an in movement. Figure 1-44 is a detailed flowchart showing the normal seek operation.

With the drive in the unit ready and on cylinder conditions, the controller initiates a normal seek by raising the Tag 1 (Cylinder Select) signal and placing the desired cylinder address on the Bus bits 0 through 9. The address is gated into the Cylinder Address register (in the I/O Gate Array) by the Cylinder Select Tag.

Inside the I/O Gate Array several processes take place. If a new seek command leaves the Cylinder Address register contents unchanged (a zero-track seek), the On Cylinder line remains set and no Seek Interrupt is enabled to PIA-0. If a new seek command requires a seek to a different seek address, however, the Cylinder Select tag clears the On Cylinder FF and triggers a one-shot that sends Seek Interrupt to PIA-0. The MPU responds to this interrupt by initiating a seek routine.

The MPU transfers the destination cylinder address from the I/O Gate Array into its internal RAM via PIA-0 by pulsing the I/O Control 1 and 2 lines. These control lines operate a multiplexer in the gate array to place the address, four bits at a time, on Head/Cylinder Address lines 0-3. After reading the cylinder address, the MPU pulses the control lines to cause the Head Address to be multiplexed onto Head/Cylinder Address lines 0-3.

The seek operation from this point until the on cylinder condition is achieved is under the control of the MPU programming. The program compares the new address with the present address (stored in RAM memory) to calculate the difference between the two (T=tracks to go) and the direction of the move (in or out).

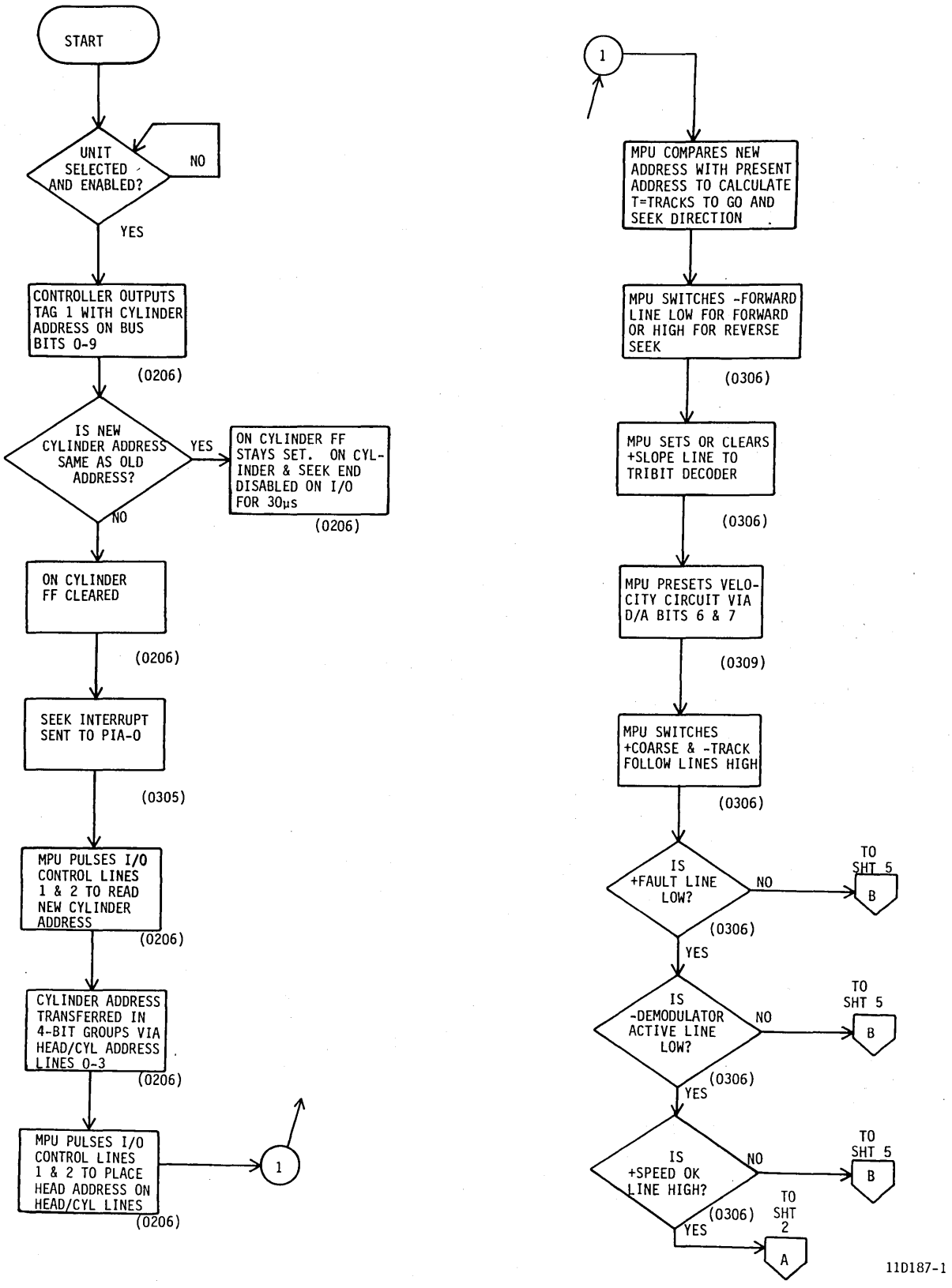


Figure 1-44. Normal Seek Flowchart (Sheet 1 of 5)

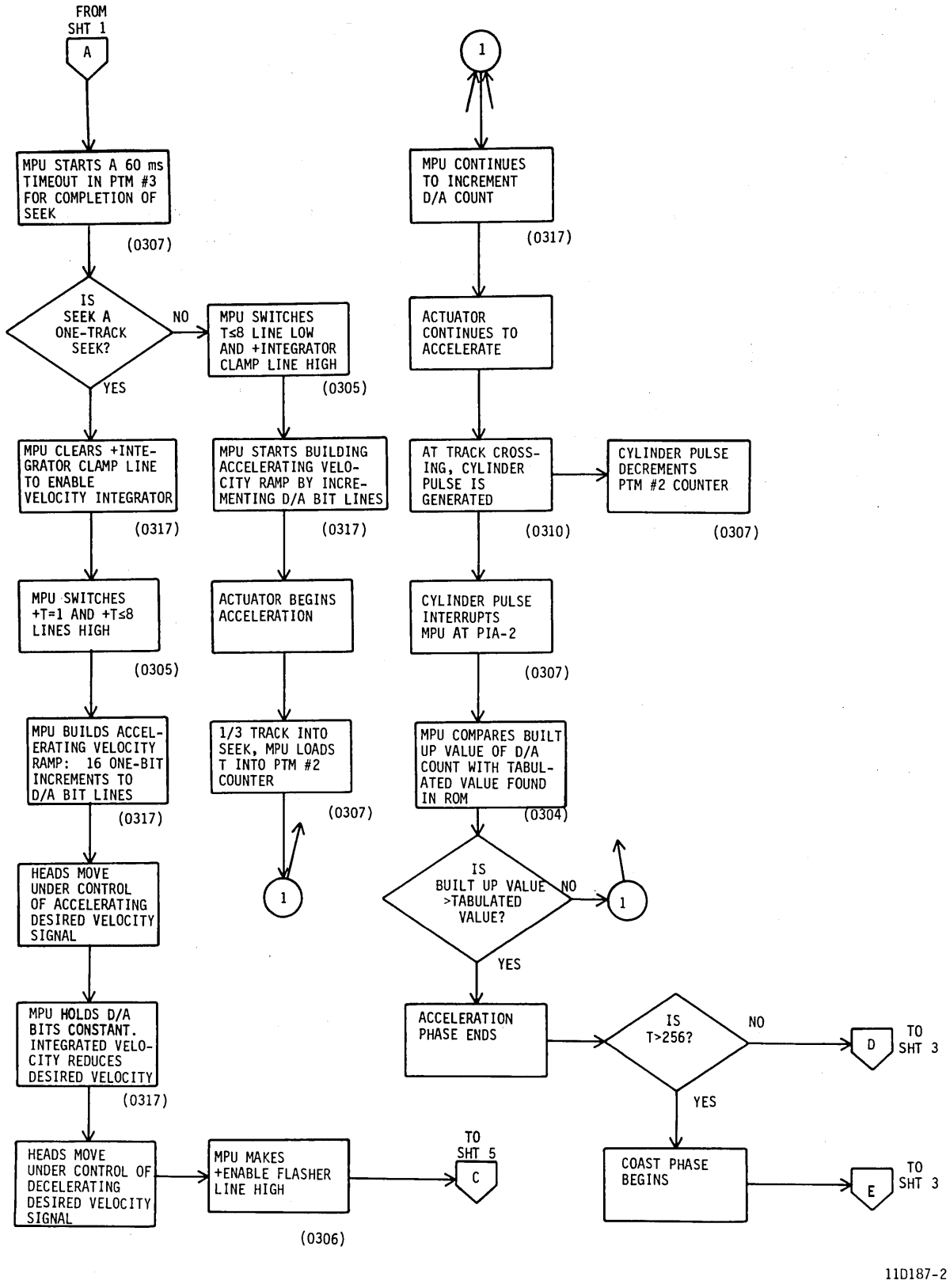


Figure 1-44. Normal Seek Flowchart (Sheet 2)

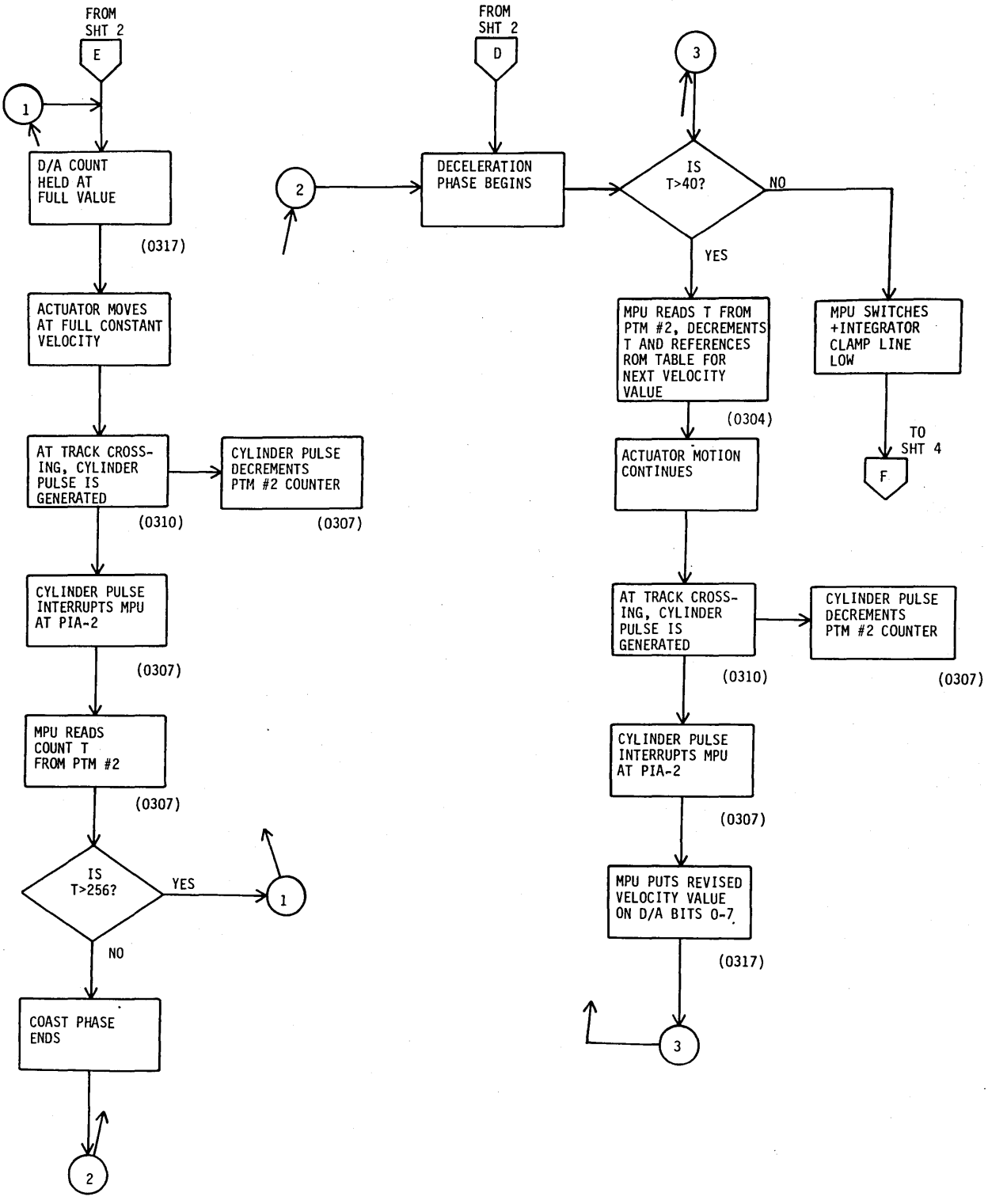
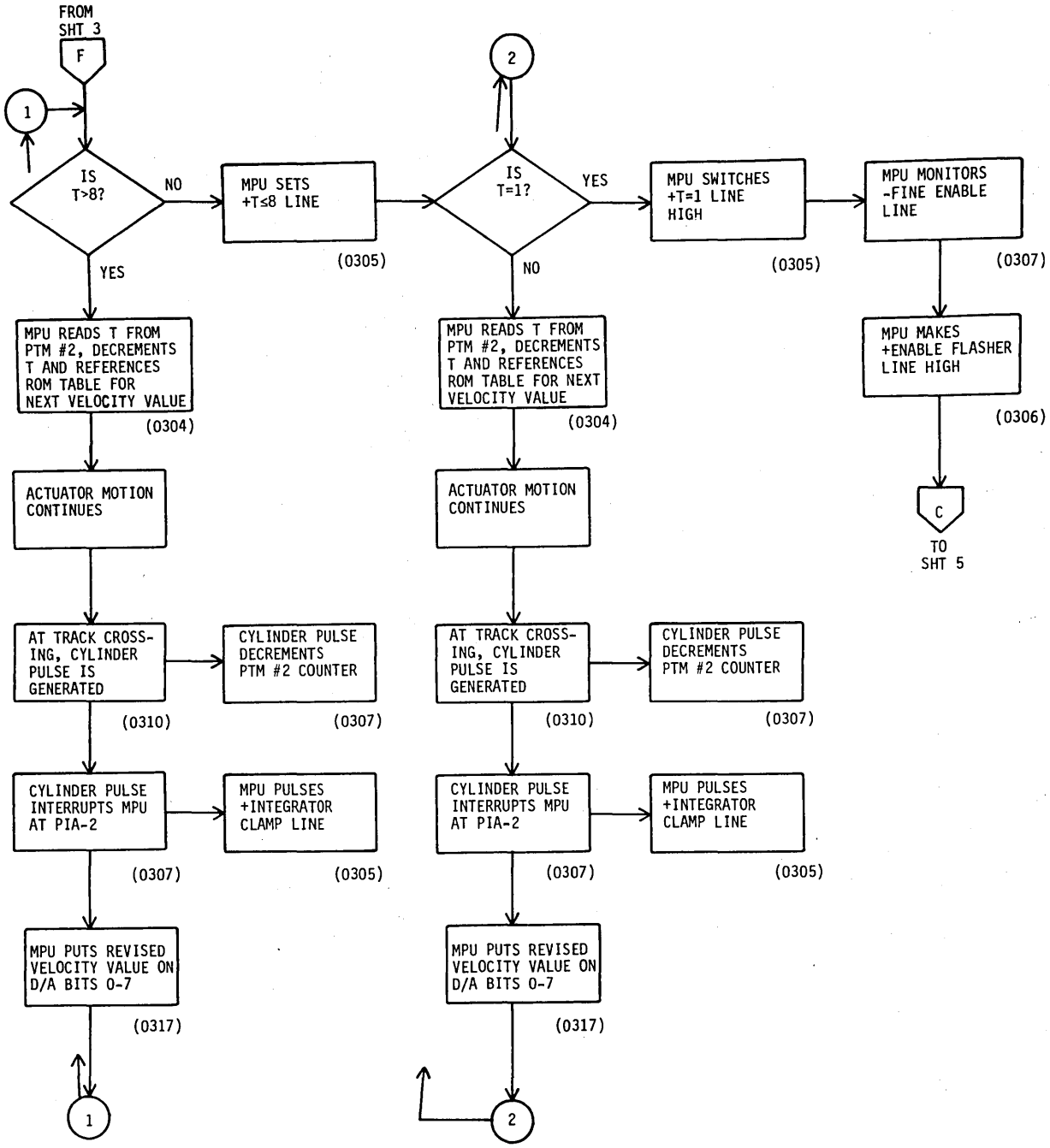
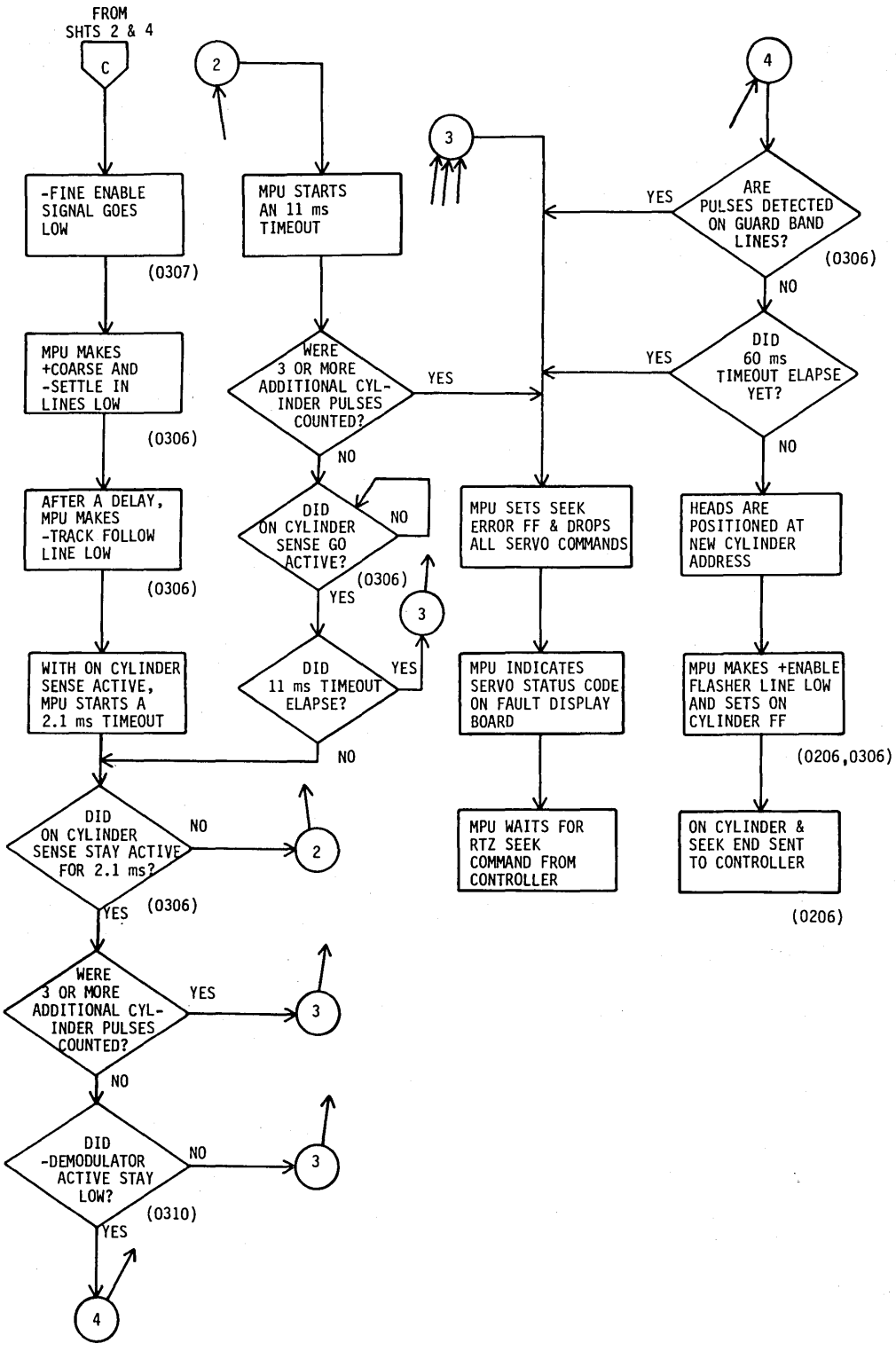


Figure 1-44. Normal Seek Flowchart (Sheet 3)



11D187-4

Figure 1-44. Normal Seek Flowchart (Sheet 4)



11D187-5

Figure 1-44. Normal Seek Flowchart (Sheet 5)

In all seeks, the MPU presets certain signal lines to condition the coarse servo loop. The -Forward line is switched low for in direction seeks or high for out direction seeks. The MPU initializes the velocity measurement circuit by setting or clearing a latch in the Sector Counter Gate Array. To do this, the MPU supplies inputs via the D/A Bit 6, D/A Bit 7, and -Forward signals. The MPU checks to make sure that there is no fault condition and that the Demodulator Active and Speed OK signals are active.

If these conditions are met, the MPU loads the programmable timer (PTM #3) with a 60 millisecond timeout count (so that a Seek Error will be indicated if the seek is not completed at the end of the timeout). The MPU sets or clears the +Slope line to the tribit decoder circuit to ensure that the decoded position signal has the proper phase at the destination track. The MPU then starts the seek by making the -Track Follow and the +Coarse lines high and by introducing an accelerating velocity profile to the Desired Velocity circuit.

The remaining coarse seek is different for one-track seeks than it is for longer seeks. For one-track seeks, the MPU clears the +Integrator Clamp line, allowing the Velocity Integrator to generate the Integrated Velocity signal. The MPU also sets the T=1 and the $T \leq 8$ lines to control the level of Integrated Velocity contributing to the Desired Velocity signal, and it builds an accelerating velocity profile by incrementing the D/A bits input to the D/A Converter one bit at a time.

After 16 increments, the MPU holds the D/A input constant, and a decelerating velocity profile results as the Integrated Velocity signal ramps up. The Integrated Velocity signal subtracts more and more from the D/A Converter velocity signal to bring the Desired Velocity signal toward zero. The MPU monitors the -Fine Enable line, as it switches from coarse to fine loop operation when -Fine Enable goes low.

For seeks greater than one track, a different coarse seek sequence is managed by the MPU. The MPU builds an accelerating velocity ramp by incrementing the D/A bits entering the D/A Converter every 43 microseconds. At approximately 1/3 of a track into the seek, the MPU loads T, the number of tracks to go, into the programmable timer (PTM #2). (A cylinder pulse, generated as the heads cross each track, decrements PTM #2 directly to keep the count T current).

The MPU continues to increment the D/A bit count, building up the velocity profile, until deceleration conditions are reached. This happens when the D/A count reaches the value specified in the velocity table for the current value of T. For the remainder of the coarse seek, the MPU controls the D/A count based upon the velocity table. For long seeks, the D/A count stays at maximum (all bits set) and the carriage coasts at full velocity prior to actual deceleration.

Throughout the deceleration portion of the coarse seek, the MPU updates the D/A count at each cylinder crossing and activates the velocity integrator circuit once T<40. The MPU clamps integrated velocity to zero by pulsing the +Integrator Clamp line at each cylinder crossing and adjusts the level of the Integrated Velocity signal by means of four control lines to the circuit: $T \leq 8$, T=1, D/A bit 6, and D/A bit 7.

When T=1, the MPU monitors the -Fine Enable signal. This signal goes low with approximately 1/3 of a track to go. The MPU reacts by switching the +Coarse and -Settle In signals low via PIA-1. This places the servo in the first (track-capture) phase of the fine servo loop.

After a 0.8 millisecond delay, the MPU issues the Track Follow command via PIA-1. The Track Follow signal adds a low frequency gain boost to the positioning loop. Once the On Cylinder Sense signal goes active, the MPU allows a 2.1 millisecond timeout to ensure that the actuator has settled on track. During this interval, the MPU monitors the On Cylinder Sense signal. If that signal goes inactive, the MPU allows 11 milliseconds for it to go active again. In this case, the 2.1 millisecond interval repeats to ensure that On Cylinder Sense remains active. In either interval, if three or more cylinder pulses are counted, this indicates excessive overshoot, and the MPU sets the Seek Error FF.

At the end of the timeout, the MPU ensures that -Demodulator Active is low and that there are no pulses on the Inner or Outer Guard Band lines. If the seek operation was successful, the MPU switches the +Enable Flasher line low. This reduces the sensitivity of the On Cylinder Sense level detector while the heads are on cylinder. The MPU sets the On Cylinder FF in the I/O Gate Array using I/O Control lines 1 and 2. With this FF set, On Cylinder and Seek End status appear on the interface.

If the seek operation was unsuccessful, the MPU sets the Seek Error FF in the I/O Gate Array by using Control lines 1 and 2. With this FF set, Seek Error and Seek End status appear on the interface. As a maintenance aid, the MPU displays a servo status code on the fault display board. These codes, discussed in Section 3, indicate where the seek operation failed.

After providing Seek End status, the MPU waits for further commands from the controller.

Return to Zero Seek

The Return to Zero (RTZ) seek is the operation that moves the heads from any location on the disk to track 0. Although the MPU uses an RTZ seek as part of the load operation, the controller can command RTZ seeks also. Both types of RTZ seeks are identical, except for the status presented if they fail. If the RTZ seek in a load operation is unsuccessful, the MPU lights the First Seek fault indicator, and a reattempt occurs only if the Fault Clear switch is pressed. If a controller-initiated RTZ seek is unsuccessful, the MPU sets the Seek Error FF, and Seek Error is active on the I/O. In this case, the drive waits for another RTZ command from the controller.

This discussion pertains specifically to the controller-initiated RTZ seek. This seek is flow-charted in figure 1-45. Refer to the Load Operation discussion for details about the RTZ portion of the load operation.

The controller initiates an RTZ operation by outputting Tag 3 (Control Select) along with Bus bit 6. The RTZ Seek command is decoded on the I/O Gate Array where it clears the Cylinder and Head Address registers, the On Cylinder FF, and Seek Error FF (all in the I/O Gate Array). In addition, the I/O Gate Array sends the RTZ interrupt to PIA-0 on the Control Board to generate an interrupt to the MPU.

The MPU reads the RTZ interrupt and initiates the RTZ. At this point, the actuator is floating freely over the data zone. Prior to moving the actuator, the MPU checks the -Demodulator Active and the +Fault lines. If either line is high, the MPU sets the Seek Error FF.

After waiting for the actuator velocity to drop to two inches per second, the MPU uses the coarse servo loop to move the heads outward into the outer guard band. To do this, the MPU switches the +Coarse line high and the -Forward line high. The MPU inputs the D/A converter with a constant desired velocity via D/A bits 0-7 from PIA-2.

Once the heads reach the outer guard band, the MPU reduces the D/A input, and the actuator continues to move outward at reduced velocity. The MPU verifies that the -Demodulator Active signal remains low, and it uses the programmable timer (PTM #2) to monitor cylinder pulses.

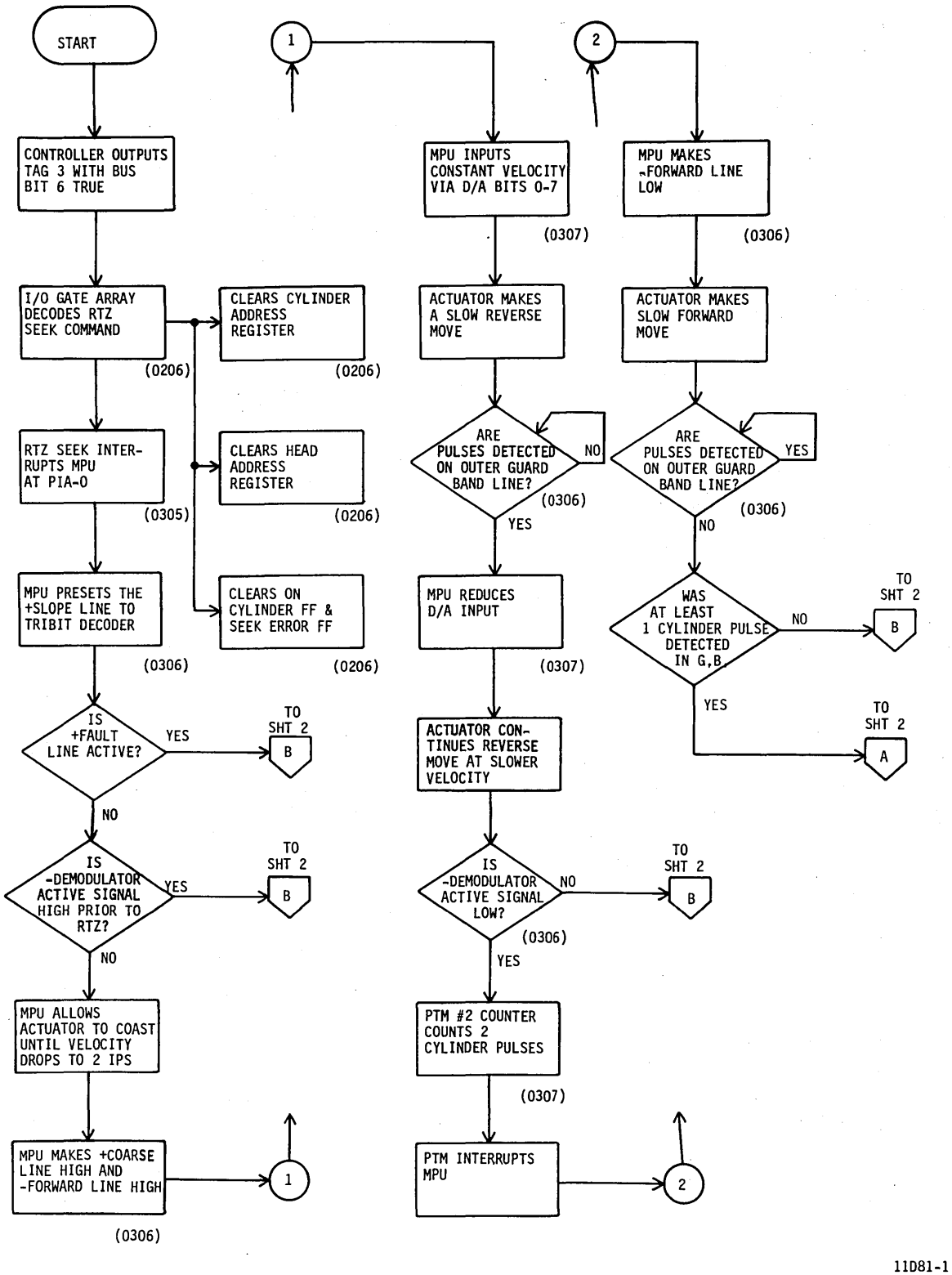


Figure 1-45. Return to Zero (RTZ) Seek (Sheet 1 of 2)

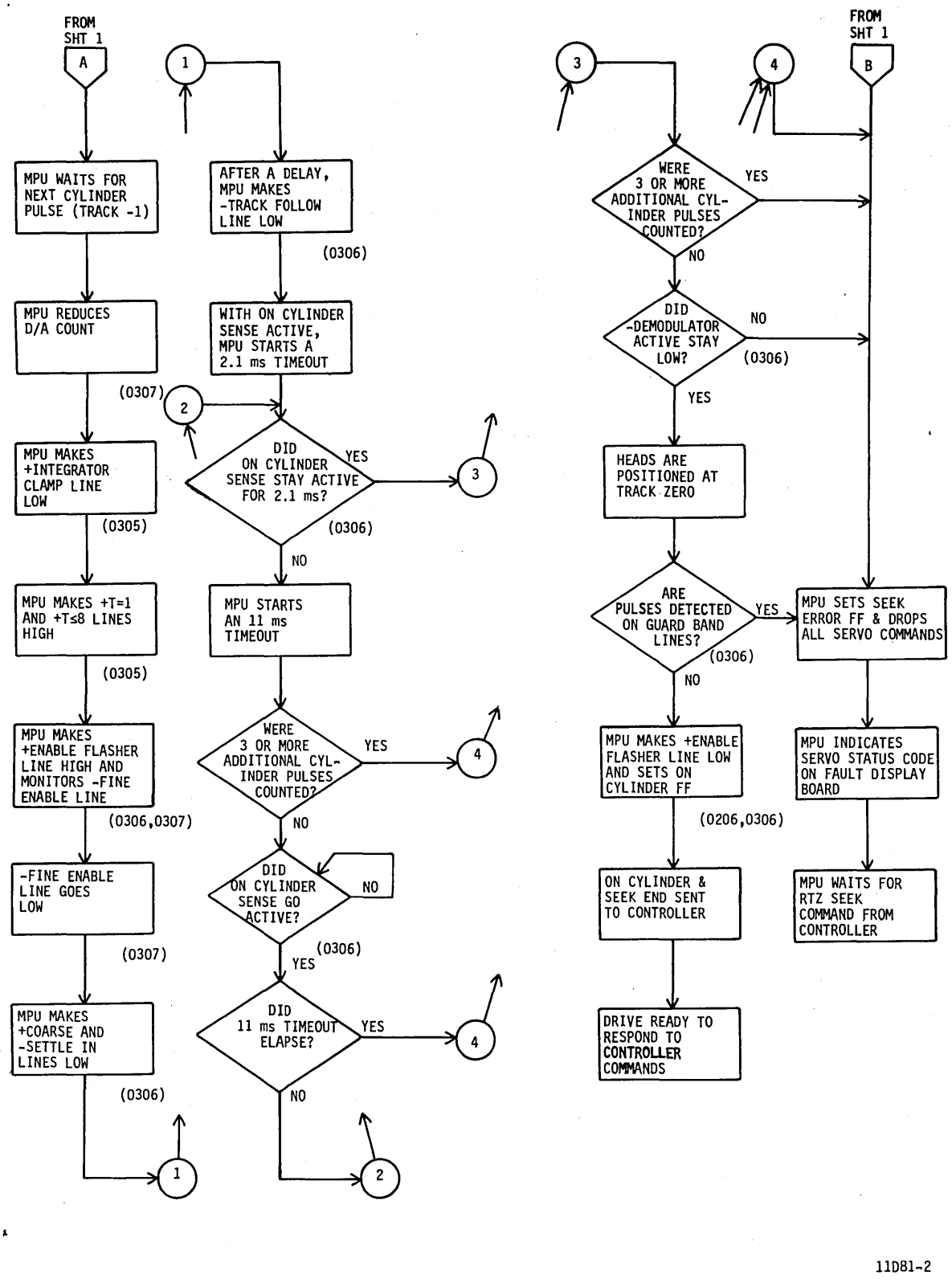


Figure 1-45. Return to Zero (RTZ) Seek (Sheet 2)

When PTM #2 has counted the two cylinder pulses for this move, it interrupts the MPU. The MPU reacts by issuing the Forward command to make the heads seek inward. The MPU requires that one cylinder pulse appears before the Outer Guard Band signal goes inactive (or it sets the Seek Error FF). After the Outer Guard Band signal goes inactive, the MPU waits for one additional cylinder pulse representing the last track crossing before track 0.

When this cylinder pulse interrupts the MPU, the MPU reduces the D/A Converter velocity signal further (via D/A bits 0-7) and activates the Velocity Integrator by clearing the +Integrator Clamp line. The MPU also sets the +T=1 and the +T≤8 lines to control the level of Integrated Velocity contributing to the Desired Velocity signal. With a constant D/A input from the MPU and the Velocity Integrator ramping up, the Desired Velocity signal approaches zero as the Integrated Velocity signal subtracts more and more from the D/A Converter velocity signal.

The MPU monitors the -Fine Enable signal. This signal goes low with approximately 1/3 of a track to go. The MPU reacts by switching the +Coarse and -Settle In signals low via PIA-1. This places the servo in the first (track-capture) phase of the fine servo loop.

After a 0.8 millisecond delay, the MPU issues the Track Follow command via PIA-1. The Track Follow signal adds a low frequency gain boost to the positioning loop. Once the On Cylinder Sense signal goes active, the MPU allows a 2.1 millisecond timeout to ensure that the actuator has settled on track. During this interval, the MPU monitors the On Cylinder Sense signal. If that signal goes inactive, the MPU allows 11 milliseconds for it to go active again. In this case, the 2.1 millisecond interval repeats to ensure that On Cylinder Sense remains active. In either interval, if three or more cylinder pulses are counted, this indicates excessive overshoot, and the MPU sets the Seek Error FF.

At the end of the timeout, the MPU ensures that -Demodulator Active is low and that there are no pulses on the Inner or Outer Guard Band lines. If the RTZ operation was successful, the MPU switches the +Enable Flasher line low. This reduces the sensitivity of the On Cylinder Sense level detector while the heads are on cylinder. The MPU sets the On Cylinder FF in the I/O Gate Array using I/O Control lines 1 and 2. With this FF set, On Cylinder and Seek End status appear on the interface.

If the RTZ operation was unsuccessful, the MPU sets the Seek Error FF in the I/O Gate Array by using Control lines 1 and 2. With this FF set, Seek Error and Seek End status appear on the interface. As a maintenance aid, the MPU displays a servo status code on the fault display board. These codes, discussed in Section 3, indicate where the seek operation failed.

After providing Seek End status, the MPU waits for further commands from the controller.

Retract and Stop Operation

The MPU uses the retract operation during the stop sequence to move the heads completely outward until they are located over the landing zone. The MPU initiates the retract sequence when it detects a loss of start conditions. A loss of start conditions occurs when the START switch is pressed to release it from the the Start position or (in remote operation) when the controller deactivates Sequence Hold.

Seeing a loss of start conditions, the MPU deactivates the Ready signal, drops all commands to the servo circuitry, and then issues the Retract command. The retract moves the heads slowly outward into the landing zone and holds them in contact with the soft actuator stop. After a delay, the MPU drops the Unlock Actuator command to lock the actuator in this position.

The MPU then drops the Motor Run command. The MPU monitors Motor Sensor pulses with the programmable timer (PTM#3); when the motor has stopped rotating, the MPU waits two seconds and drops the Retract command. The MPU allows a 30 second delay (during which the Ready indicator flashes) before it can recognize new start conditions and initiate another load operation.

HEAD OPERATION AND SELECTION

GENERAL

Information is recorded on and read from the disk by the read/write heads (refer to figure 1-46). The drive has two read/write heads for each data recording surface in the disk module as shown. The drive has 8 recording surfaces and 16 read/write heads. For this reason, before a read or write can be performed, the controller must command the drive to select the head located over the disk surface where the data is to be read or written.

The following discusses how the heads read and write the data and also how the desired head is selected.

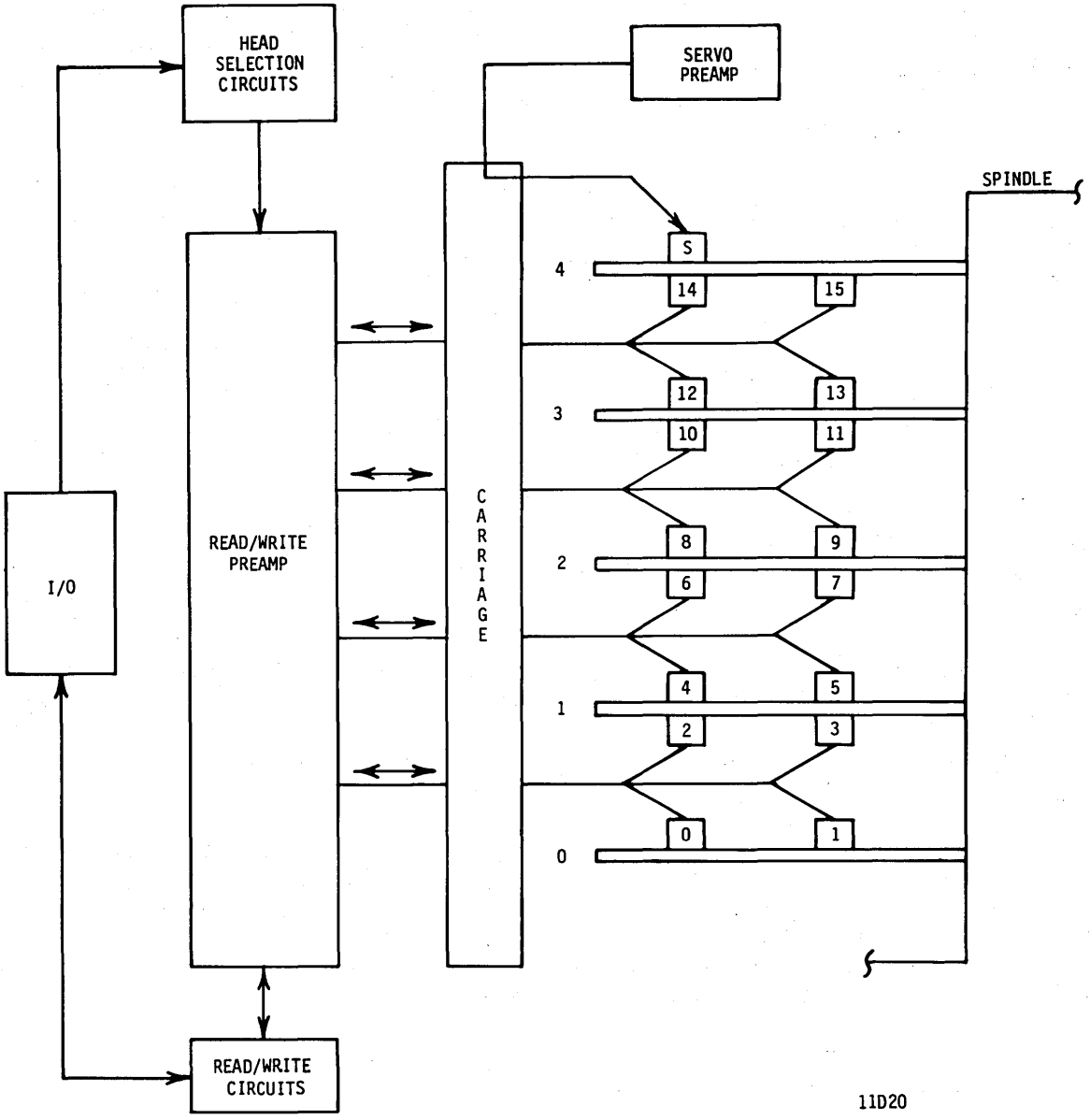


Figure 1-46. Read/Write Heads

HEAD FUNCTIONAL DESCRIPTION

Each read/write head has two opposing coils wound on the same core. The coils interface to the read/write circuitry via a preamp mounted on the head-arm. Selecting a head requires selecting an arm preamp and supplying selection signals to that preamp indicating which head on that arm is desired. In response to the signal inputs, the enabled arm preamp selects one of four heads, and either provides current switching for the head in write operations or amplification of voltage induced in the head in read operations. Refer to Read/Write Functions for details about the Arm Preamp.

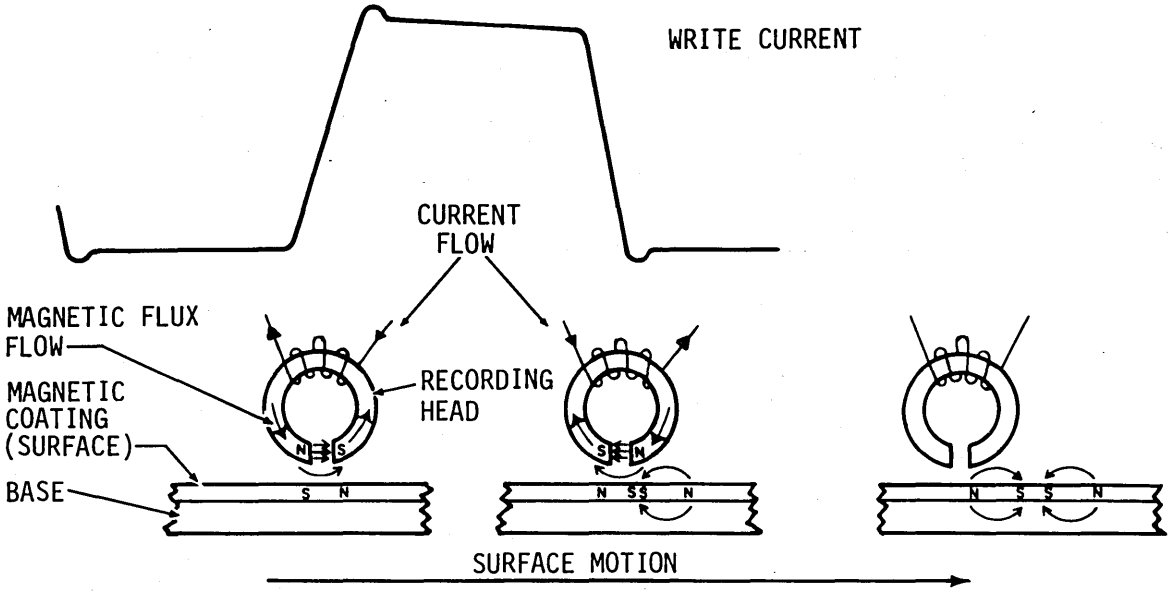
During write operations, the read/write head develops a changing flux pattern on the disk surface passing beneath it. The Arm Preamp supplies the selected head with a source of write current. At each transition of the write data signal, the preamp reverses the current in the head coil. This switching reverses the flux across the gap in the head (see figure 1-47). The flux field magnetizes the iron oxide particles bound to the disk surface. Each particle is then the equivalent of a miniature bar magnet with a north pole and a south pole. The writing process orients the poles to store the direction of the flux field as the oxide passes beneath the head. The direction of the flux field is a function of write current switching while its amplitude depends on the amount of current (the greater the current, the more oxide particles that are affected).

Information (data) is written by switching the current through the head. Switching between the two head coils reverses the direction of the flux field across the gap. The flux change defines a data bit. New data is written simply by writing over any data which may already be on the disk.

During a read operation, disk motion beneath the head causes the stored flux to induce a voltage in the heads (refer to figure 1-48). This voltage is analyzed by the Read circuit to define the data recorded on the disk. Each flux reversal (produced while writing) generates a readback voltage pulse. Each pulse, in turn, represents a data bit.

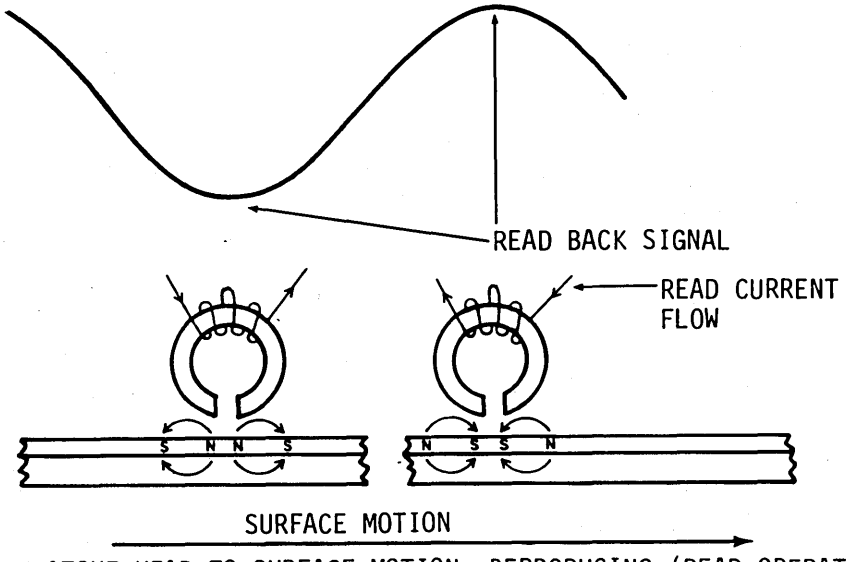
HEAD SELECTION

A head must be selected before a read or write operation can be performed. Prior to head selection, the controller issues a cylinder select command. Under MPU control, the servo system moves the heads to the cylinder specified by the controller. By selecting a head, the controller specifies a particular track within that cylinder. Head selection starts when the controller sends the drive a Head Select (Tag 2) command and a head address. The head address is sent on Bus bits 0 through 3.



NOTE: RELATIVE HEAD TO SURFACE MOTION, RECORDING (WRITE OPERATION) 11D189

Figure 1-47. Writing Data



NOTE: RELATIVE HEAD TO SURFACE MOTION, REPRODUCING (READ OPERATION)

11D190

Figure 1-48. Reading Data

The Head Select tag gates the address into the Head Address register (HAR) in the I/O Gate Array. Figure 1-49 shows the head selection circuits. The cylinder address and the head address are multiplexed out of the gate array on +Head/Cylinder Address lines 0-4. The MPU controls this multiplexing with I/O Control lines 1 and 2. In the initial phase of a seek, the Head/Cylinder Address lines transfer the new cylinder address to the MPU. With this transfer complete, the lines carry head address information. Thus, whenever the heads are on cylinder, +Head Address line 0 reflects HAR bit 0, and so forth.

The Head/Cylinder Address lines go from the I/O board to the Read/Write board via the Control board. The Read/Write board contains a ROM, addressed by Head/Cylinder Address lines 0-4. Depending on its addressing, the ROM activates one of its output lines, -Arm Select 1-4, to enable one arm preamp. The enabled arm preamp in turn selects one of the heads on its head-arm in response to the +Head Select 1 and 2 lines. These lines are activated by Head/Cylinder Address lines 0 and 1 respectively. The Arm Select, Head Select, and common control lines for the preamps are routed through the HDA Interface Board (_TSX) to the Bulkhead board (inside the module) and then to the individual arm preamps.

If an illegal head address (greater than 15) is received, no head is selected. A Write Fault occurs if the drive attempts to write data with no head selected. Table 1-3 shows the combination of address lines that selects each head.

READ/WRITE FUNCTIONS

GENERAL

When the drive is on cylinder and has a head selected, it is ready to perform a read or write operation. The controller initiates a read or write operation by sending a Control Select (Tag 3) along with the proper bus bit (Bit 0 for Write Gate and Bit 1 for Read Gate). During a write operation, the drive receives data from the controller and writes it on the disk. During a read operation, the drive recovers data from the disk and transfers it to the controller.

Figure 1-50 is a block diagram of the read/write circuits. The remainder of the discussion describes the read/write circuits and is divided into the following areas:

- Basic Read/Write Principles -- Explains the principles of recording and recovering data from a magnetic disk.
- Write Circuits -- Describes the circuits used by the drive to record data on the disk.

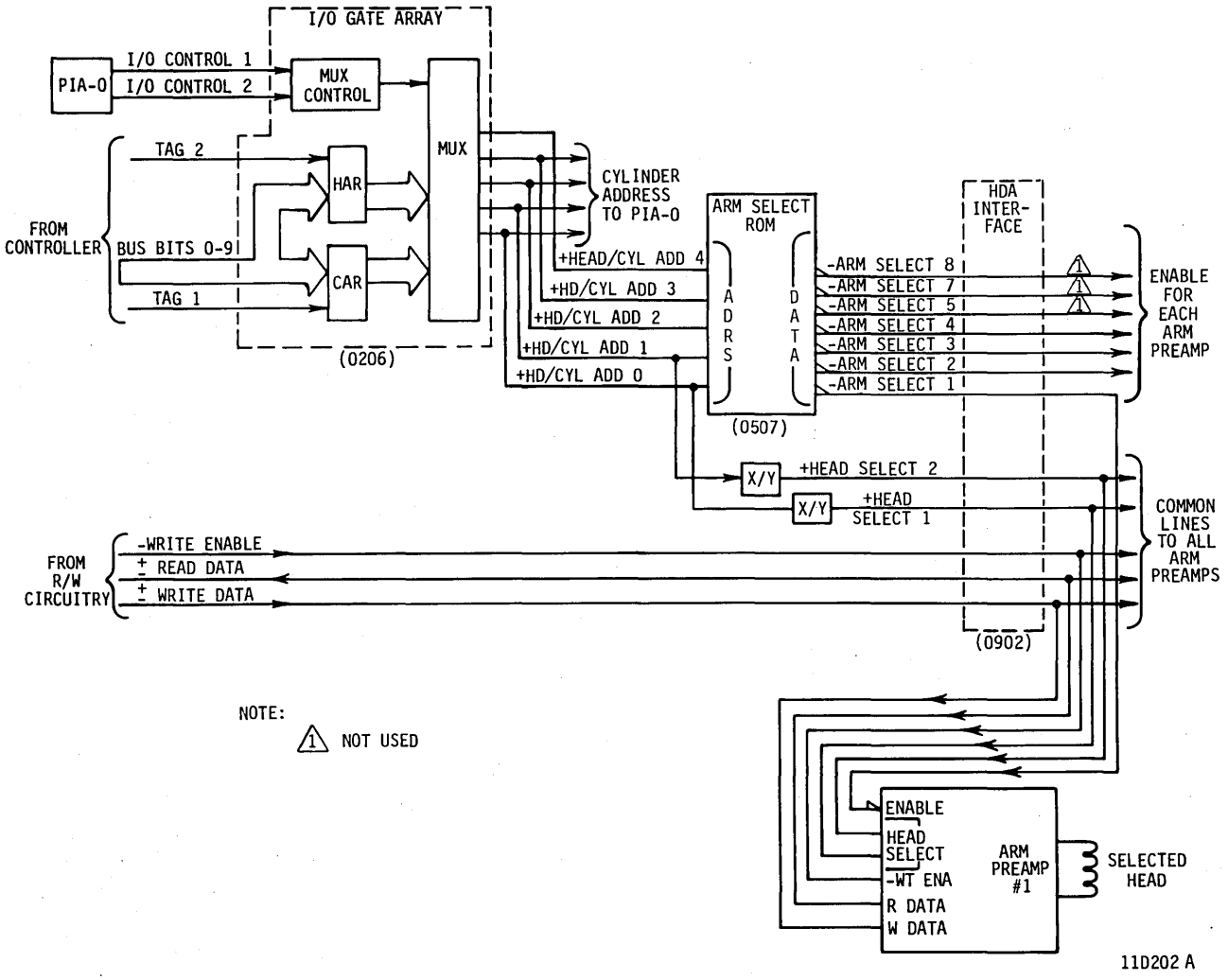


Figure 1-49. Head Selection Circuits

- Read Circuits -- Describes the circuits used by the drive to recover data from the disk.

BASIC READ/WRITE PRINCIPLES

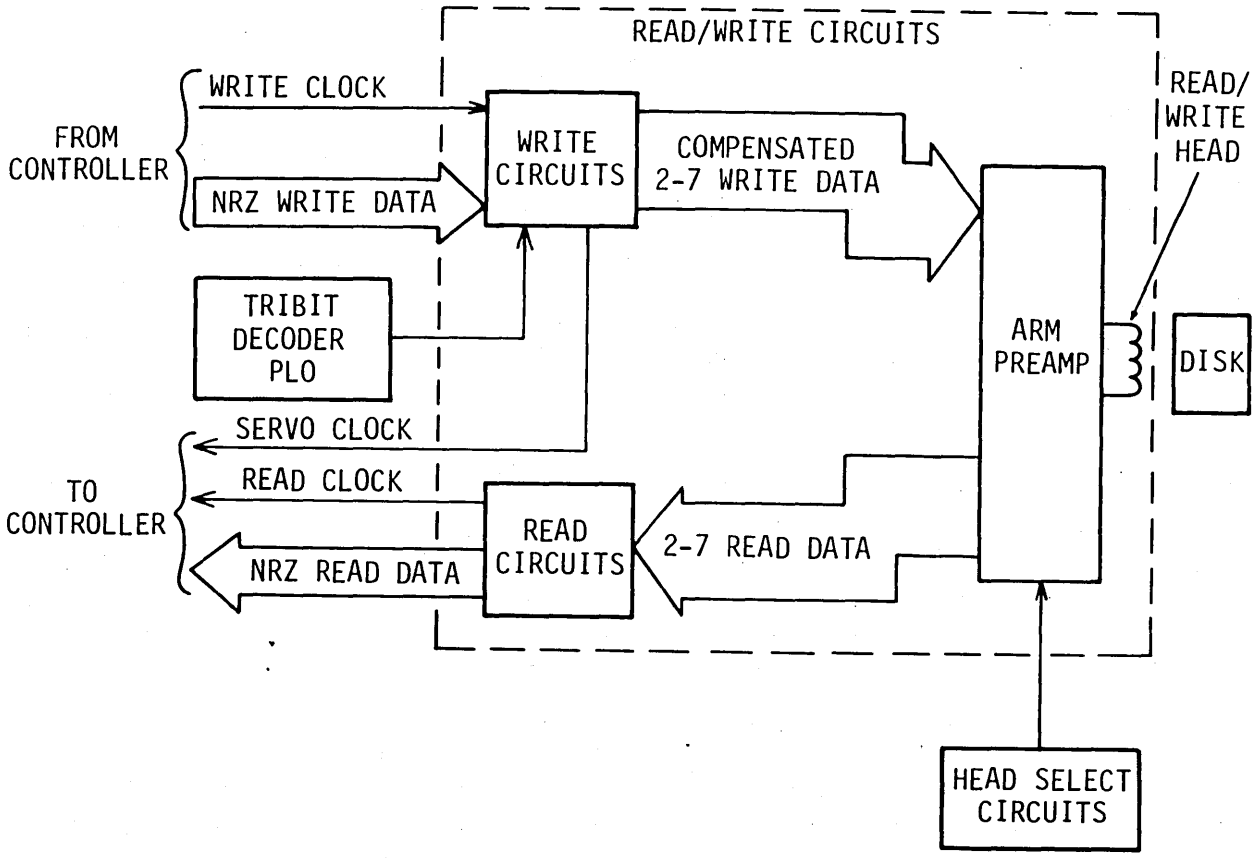
Principles of 2-7 Recording

The drive employs two modulation schemes for read/write data transfers. The controller transfers data on the interface with Non Return to Zero (NRZ) modulation in a write operation. Write circuitry in the drive encodes the incoming data by changing it to 2-7 modulation. Transfers between the read/write circuitry and the disk use 2-7 modulation. Therefore, in a read operation, read circuitry in the drive must decode the 2-7 read data to create NRZ data which is suitable for the controller. The following paragraphs define both modulation schemes and the explain why 2-7 modulation is used in the drive.

TABLE 1-3. HEAD SELECT ADDRESSING

Head Selected	Arm Selected	+Head/Cylinder Address Lines				
		0	1	2	3	4
0	1	0	0	0	0	0
1	1	1	0	0	0	0
2	1	0	1	0	0	0
3	1	1	1	0	0	0
4	2	0	0	1	0	0
5	2	1	0	1	0	0
6	2	0	1	1	0	0
7	2	1	1	1	0	0
8	3	0	0	0	1	0
9	3	1	0	0	1	0
10	3	0	1	0	1	0
11	3	1	1	0	1	0
12	4	0	0	1	1	0
13	4	1	0	1	1	0
14	4	0	1	1	1	0
15	4	1	1	1	1	0

NRZ data is transferred at a nominal rate of 14.5 MHz. Each data bit is defined throughout an interval called a bit cell, and the nominal duration of each bit cell is 68.9 ns. For consecutive cells indicating binary 1, the read or write data interface line is driven at the active level. For consecutive cells indicating binary 0, the read or write data interface line is driven at the inactive level. Thus, NRZ data lines return to zero only when the transferred data changes from binary 1 to binary 0.



11D84

Figure 1-50. Read/Write Circuits

For disk transfers, the 2-7 scheme is superior to the NRZ scheme in two ways. First, it reduces the maximum rate of flux reversals on the disk; this permits greater recording density on the disk. Second, the recording bandwidth, or range from the minimum to maximum flux reversal rate, is limited; with narrowed bandwidth, the read/write circuitry has fewer noise problems.

The translation between NRZ modulation and 2-7 modulation is a translation of seven basic code words, as shown in table 1-4. Any string of NRZ data can be expressed as a series of these individual code words. The corresponding 2-7 data string is a series of translated code words where each 2-7 code word has replaced its corresponding NRZ word. So, the write circuitry encodes the NRZ data as 2-7 data, and the read circuitry decodes the 2-7 data as NRZ data.

TABLE 1-4. TRANSLATION BETWEEN NRZ AND 2-7 CODES

NRZ Code Words	2-7 Code Words
00	1000
01	0100
100	001000
101	100100
111	000100
1100	00001000
1101	00100100

Each 2-7 code word has twice as many bits as its related NRZ code word. Therefore, the 2-7 bit cell is half the NRZ bit cell or 34.45 ns, nominal. As the 2-7 data is written on the disk, the head changes its flux each time the code contains a binary 1. Although 2-7 uses twice the bit rate of NRZ, binary ones appear in 2-7 code less frequently than level changes occur in the corresponding NRZ code. Therefore, use of 2-7 code allows data to be written more densely on the disk.

The name 2-7 derives from the fact that preceding and following each occurrence of a binary 1 in the code, there are at least two zeros and as many as seven zeros.

Peak Shift

Peak shift is a predictable effect that would complicate decoding of the 2-7 read signal if it were not compensated for in the write circuitry. The following paragraphs explain why peak shift occurs and how write compensation reduces the effects of peak shift.

Figure 1-51 shows selected write and read signals that are relevant to the description of peak shift. The write data line toggles each time a binary 1 appears in the 2-7 data string. Each toggle of write data reverses the magnetic flux on the data head to produce a region of changing recorded flux in the disk surface. The flux reversal on the disk has a finite length on the disk because of the shape of the flux pattern from the head gap and the inability of the head to reverse its magnetic flux instantaneously.

In read operations, the data head develops a composite readback voltage as it intercepts changing flux from the disk surface. Each flux reversal creates a readback voltage peak, as shown in figure 1-51. The composite readback voltage, developed by the head passing over a flux reversal, is a superposition of the peak caused by that flux reversal and by the leading and trailing edges of the peaks caused by the adjacent flux reversals. Any difference in the contributions of the two adjacent peaks will shift the central peak away from the closer adjacent peak.

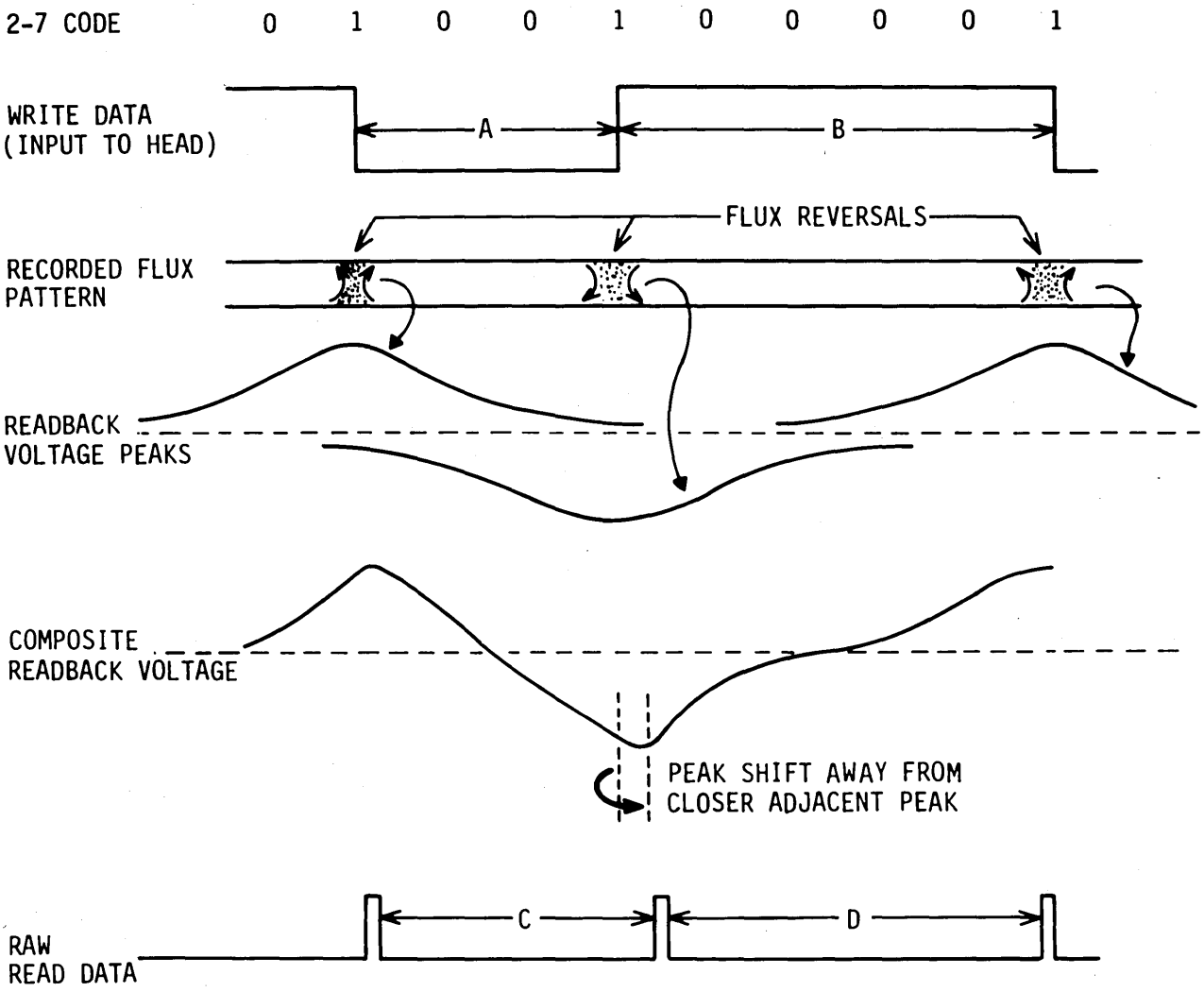
Accurate decoding in read operations requires that the raw read data signal has timing intervals identical to those in the write data signal. Peak shift lengthens certain intervals and shortens other intervals in a manner that is predictable from the spacing of adjacent peaks. Write compensation anticipates this problem by advancing or delaying each write transition by an amount that depends on the number of binary 0s leading and trailing the binary 1 producing that transition. When the number leading exceeds the number trailing, write compensation delays the write transition. When the number trailing exceeds the number leading, write compensation advances the write transition. When the two numbers are equal, the transition occurs without compensation. Thus, compensated write data drives the heads, and the raw read data contains the same timing as the uncompensated write data.

The discussion of Write Compensation under Write Circuits includes a table that defines the compensation shift for each possible data pattern.

WRITE CIRCUITS

General

The write circuit operation is initiated by Tag 3 (Control Select) with Bus Bit 0 true. This allows the drive to start processing serial NRZ data received from the controller. NRZ data is synchronized to the 14.5 MHz Write Clock derived from the Servo Clock sent to the controller. The Write Data is



WITHOUT WRITE COMPENSATION, C > A AND D < B,
AND INACCURATE READ DECODING WOULD BE POSSIBLE

10R72A

Figure 1-51. Peak Shift Waveforms

received via the Write Data line and is first sent to the 2-7 encoder circuit. This circuit converts the data to 2-7 modulation and sends it to the write compensation circuit. Write compensation modifies the data timing to compensate it for peak shift (refer to discussion on basic read/write principles for more information concerning peak shift). The compensated data is then processed by the write toggle FF. The write toggle FF provides the data signal that controls current switching in the selected arm preamp.

Figure 1-52 shows the write circuits and table 1-5 briefly explains their function.

Write PLO

The Write PLO circuitry uses a phase-locked loop to generate the 29.01 MHz (2F) Write Clock. As shown in figure 1-53, this circuitry consists of frequency dividers, a coincidence comparator, a charge pump, and a voltage-controlled oscillator (VCO). The frequency dividers and coincidence comparator are located in the Write Compensation and PLO ECL Logic Array.

TABLE 1-5. WRITE CIRCUIT FUNCTIONS

Circuit	Function
Write PLO	Generates the 29.01 MHz Write Clock which is divided by two to develop the 14.5 MHz Servo Clock.
2-7 Encoder	Converts the NRZ data from the controller to 2-7 data.
Write Compensation Circuit	Compensates the data for problems caused by peak shift.
Write Toggle FF	Produces a write signal that changes polarity each time the compensated 2-7 data goes to a binary 1.
Arm Preamp	Switches the write current in the head coil as the signal from the Write Toggle FF changes polarity.

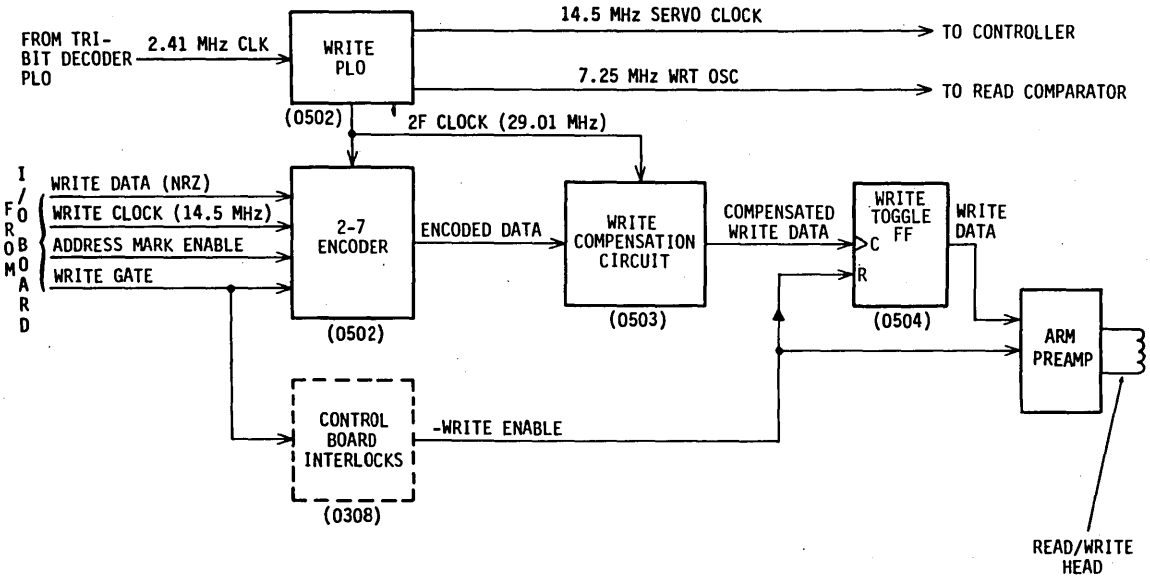


Figure 1-52. Write Circuits Block Diagram

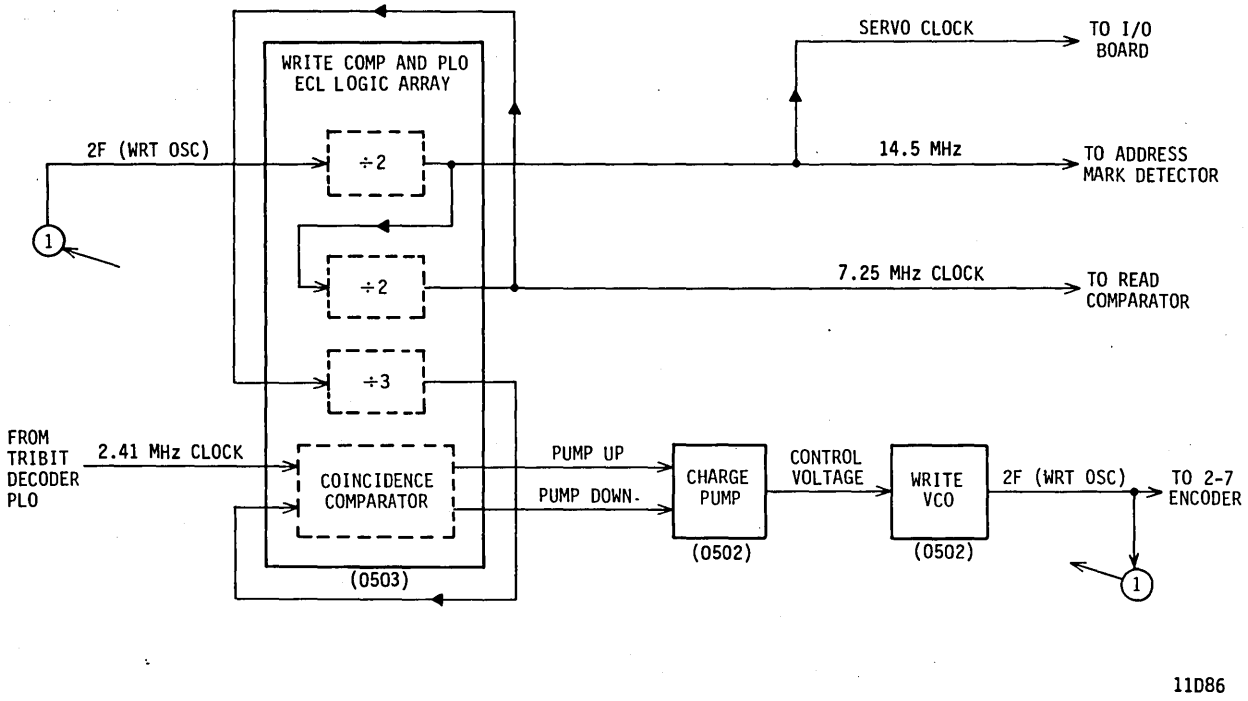


Figure 1-53. Write PLO BLock Diagram

The phase-locked loop uses the 2.41 MHz Clock from the Tribit Decoder PLO as a frequency reference (refer to the Servo Surface Decoding discussion). The Write VCO operates under loop control to generate the 29.01 MHz (2F) Write Clock, at twelve times the frequency of the reference clock. Two divisions by two and one division by three of the VCO output develop a 2.41 MHz feedback signal that can be compared to the reference clock to adjust the loop operation.

The loop reaches phase lock by comparing the coincidence of the leading edges of the reference and feedback clocks. Each time the feedback clock leads the reference clock, the coincidence comparator pulses the Pump Down line. Pump Down pulses cause the charge pump to vary the Control Voltage signal as necessary to reduce the Write VCO frequency until the reference and feedback clocks are coincident (phase-locked). Each time the feedback clock lags the reference clock, the coincidence comparator pulses the Pump Up line. Pump Up pulses cause the charge pump to vary the Control Voltage signal as necessary to increase the Write VCO frequency until phase lock occurs.

The Write PLO circuit operates continuously whenever the servo signal is being decoded. The PLO provides the following outputs to other circuits:

- 2F (WRT OSC) signal to the 2-7 Encoder circuit.
- 14.5 MHz Servo Clock to the controller (via the interface). This is returned to the drive as Write Clock.
- 7.25 MHz clock to the Read Comparator circuit.

2-7 Encoder

The 2-7 Encoder converts NRZ data into 2-7 data. As described under Basic Read/Write Principles, there is a one-to-one correspondence between seven NRZ code words and seven 2-7 code words. The encoder recognizes the coding in the write data string as a succession of the seven NRZ words, and outputs a series of 2-7 code words, each one translated from its NRZ equivalent. Table 1-4, presented under Basic Read/Write Principles, shows the translation used between the two groups of seven code words. The 2-7 encoding function takes place within a single ECL Logic Array, the 2-7 Encode/Decode chip.

The encoder uses synchronous timing circuitry controlled by two clock inputs, the 14.5 MHz Write Clock from the controller and the 29.01 MHz 2F Clock from the Write PLO (see figure 1-54). The encoder has a synchronizer that develops two clocks in phase with the 2F Clock -- the 2-7 Data Clock and a 14.5 MHz internal clock. The 2-7 Data Clock is supplied to the write compensation circuit. The internal clock shifts NRZ data into a pattern recognition circuit. Each time this circuit recognizes one of the seven NRZ code words, it parallel-loads an output shift register and starts looking for the following word.

The output shift register shifts its contents on each rising edge of the 2F Clock. The active low serial output of the register is -Encoded Data. This line is active for binary ones and inactive for binary zeros in the 2-7 data unless an address mark is being written. During an address mark, there are no transitions in the written flux, and a segment of the data track is erased. To command an address mark, the controller issues Tag 3 along with Bus bit 0 (Write Gate) and Bus bit 5 (Address Mark Enable). When Bus bit 5 goes inactive, the encoder resumes normal operation.

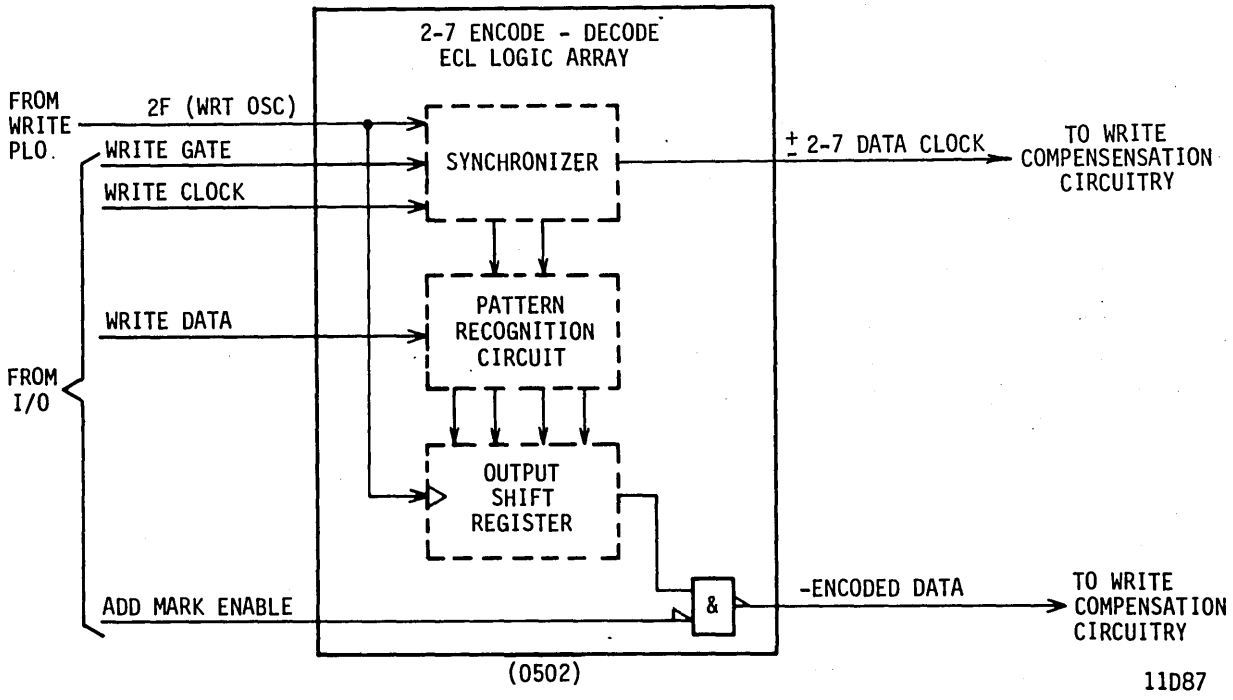


Figure 1-54. 2-7 Encoder Block Diagram

The encoder begins translating NRZ code words with the first binary zero in the NRZ data occurring on or after the second rising edge of Write Clock. Encoder operation proceeds continuously, processing all NRZ data input to it until Write Gate goes inactive.

Write Compensation Circuit

The write compensation circuit modifies the timing of transitions in the encoded 2-7 data in a manner that compensates for peak shift (refer to discussion on basic read/write principles).

Encoded 2-7 data contains isolated bit cells at binary one preceded and followed by from two to seven bit cells at binary zero. Each time the data changes from binary zero to binary one, the head reverses its flux direction. Write compensation shifts this positive-going edge away from its nominal timing, and this timing change is related to the number of zeros preceding and trailing a binary one in the data pattern.

The write compensation function takes place in the Write Compensation and PLO ECL Logic Array (see figure 1-55). This chip is capable of following four different compensation schemes as dictated by its "A" and "B" inputs. Input "A" is pulled low and input "B" is tied high. This combination, and the delays with which the 2-7 Data Clock enters chip inputs P1 through P9, produce specified time shifts for each possible data pattern. Table 1-6 specifies the delay for each data pattern relative to the nominal delay present in the circuitry. In the table, negative delays represent earlier timing and positive delays represent later timing.

Uncompensated data enters the circuit via the -Encoded Data line. This data is clocked into a 13-bit shift register. The delay line develops the clock input by delaying the 2-7 Data Clock. When the center bit of the shift register contains a binary one, the circuit looks at the number of register bits which are zero on each side of the center bit. Depending on the number of leading zeros and trailing zeros, one of the delayed clocks P1 through P9 is applied to an AND gate along with the center bit of the register. Thus, the AND gate sees the center register bit go active, followed by the applied clock going active; with both inputs active, the gate outputs a compensated write data pulse. The positive edge of the compensated data pulse is timed by the clock selected.

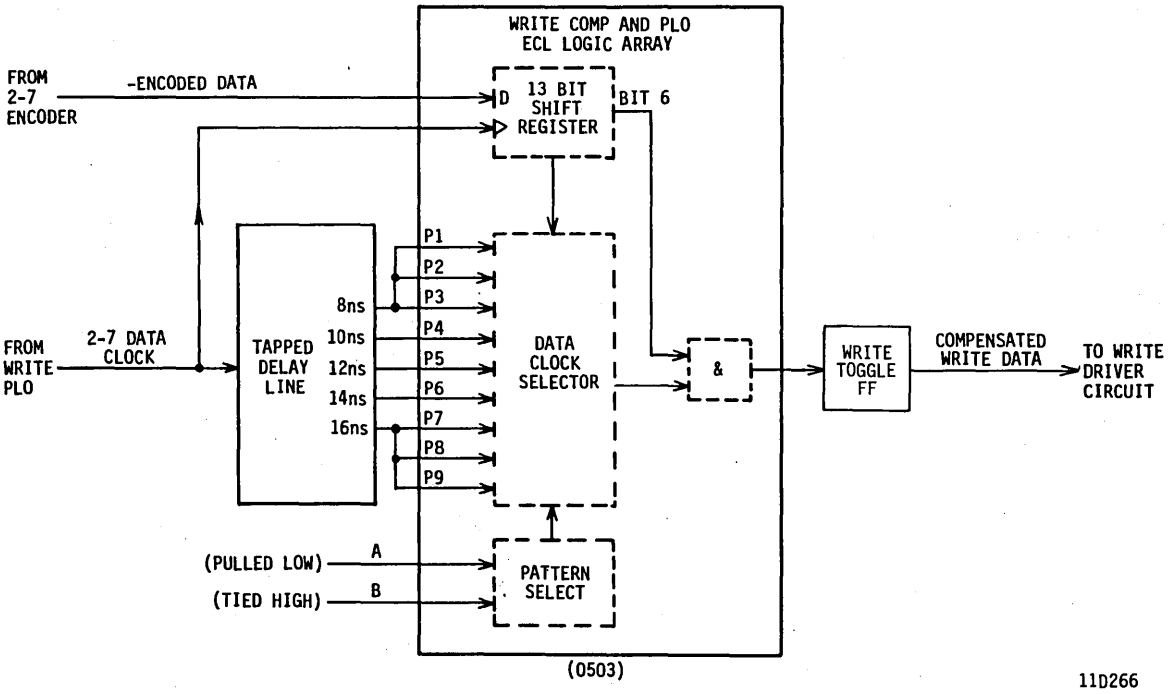


Figure 1-55. Write Compensation Block Diagram

Table 1-6 specifies the clock input gated out of the write compensation circuit for each possible data pattern. Note that a majority of the data patterns use the P5 clock and have the nominal delay.

After being write compensated, the data is transmitted to the write toggle FF.

Write Toggle FF

The compensated write data is applied as the clock input to a latch. This latch changes state with each positive edge at its clock input. The write toggle FF operates only when the -Write Enable line is active (low). With -Write Enable inactive, the latch remains cleared, and the Write Data lines to the Arm Preamps remain inactive. The -Write Enable line comes from the Control board and is active only when all the following are true:

- Write Gate is active

TABLE 1-6. WRITE COMPENSATION FOR EACH DATA PATTERN

		Number of Trailing Zeros					
		2	3	4	5	6	7
Number of Leading Zeros	2	0 ns* P5**	-2 ns P4	-4 ns P3	-4 ns P2	-4 ns P1	-4 ns P1
	3	+2 ns P6	0 ns P5	0 ns P5	-2 ns P4	-2 ns P4	-2 ns P4
	4	+4 ns P7	0 ns P5	0 ns P5	0 ns P5	0 ns P5	0 ns P5
	5	+4 ns P8	+2 ns P6	0 ns P5	0 ns P5	0 ns P5	0 ns P5
	6	+4 ns P9	+2 ns P6	0 ns P5	0 ns P5	0 ns P5	0 ns P5
	7	+4 ns P9	+2 ns P6	0 ns P5	0 ns P5	0 ns P5	0 ns P5

*Top entry gives delay relative to nominal timing where negative numbers show early timing and positive numbers show late timing.

**Bottom entry indicates which delayed clock enables a compensated output pulse.

- Write Protect is not active
- No faults exist
- Speed OK is active
- Enable Power Amp signal is active

Arm Preamp

Each head arm contains an LSI chip that serves as a preamp for the heads attached to that arm. The LSI chip selects a data head and either switches write current through the head or amplifies the read signal detected by the head (see figure 1-56). These paragraphs concentrate on the preamp's write function and assume that head selection has occurred.

The LSI chip functions as a write driver when the -Write Enable line goes active (low). The chip develops regulated current for the selected head coil and reverses the current in that coil to produce flux reversals on the disk.

Throughout a write operation, write current is always flowing through one of the head coils. The Write Toggle FF inputs two Write Data lines to the selected Arm Preamp. When a transition occurs on the input lines, the LSI chip switches the write current directions through the head coil. This switching action produces a recorded flux reversal on the disk surface.

While an address mark is being written, there is no switching action, and an unchanging flux is recorded on the disk. Thus, writing an address mark erases a segment of the data track.

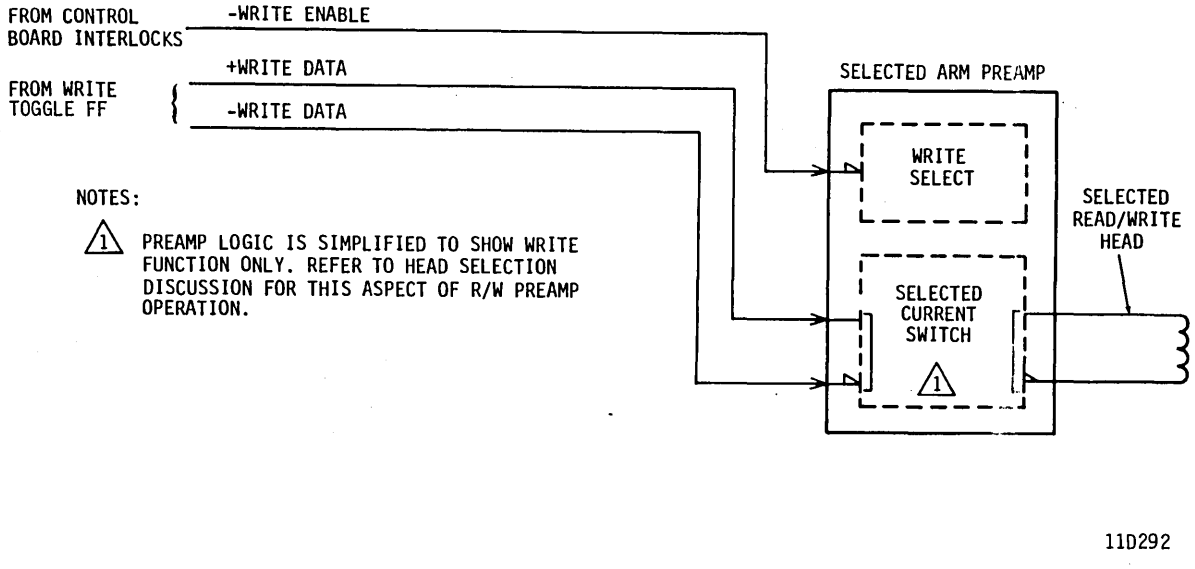


Figure 1-56. Arm Preamp

READ CIRCUITS

General

Read operations are initiated by a Control Select (Tag 3) with Bus bit 1 true. This enables the preamp circuits, which sense the data written on the disk and generate analog read data signals.

The analog data goes to the Data Latch circuit which changes it into digital 2-7 data.

The Read Comparator and PLO circuit generates a 29.01 MHz Read Clock signal that is phase-locked to the 2-7 read data. The 2-7 Decoder changes the 2-7 data to NRZ data synchronized to a 14.5 MHz Read Clock. Both data and clock are then sent to the controller.

Figure 1-57 shows the main elements in the read circuits and table 1-7 briefly describes each of these elements. The following paragraphs further describe the read circuits.

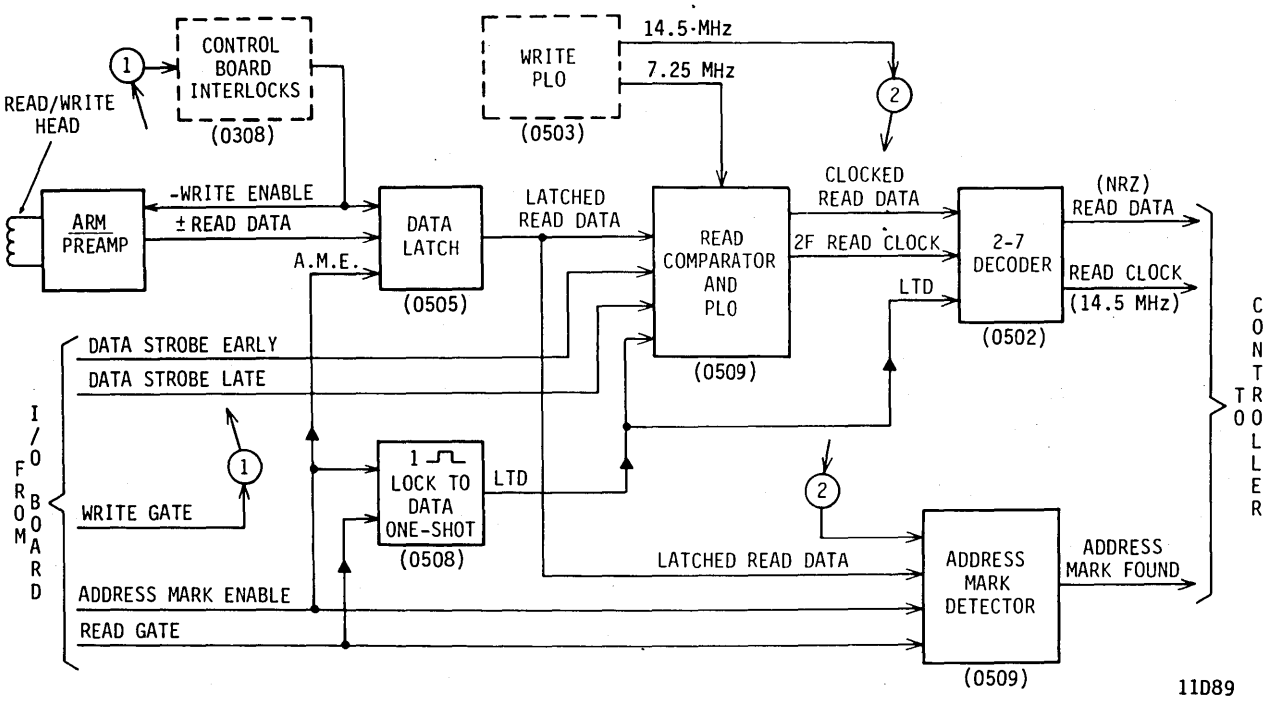


Figure 1-57. Read Circuits Block Diagram

TABLE 1-7. READ CIRCUIT FUNCTIONS

Circuit	Function
Arm Preamp	Processes the analog signal from the data head so that it can be used by the Data Latch circuit.
Data Latch Circuit	Changes the analog 2-7 data into digital 2-7 data. This data is sent to the Read Comparator circuit.
Read Comparator and PLO Circuit	Develops a 29.01 MHz Read Clock that is synchronized to 2-7 read data.
2-7 Decoder	Translates data coding from 2-7 to NRZ modulation and generates 14.5 MHz Read Clock synchronized to NRZ data. NRZ data is sent to the controller with the 14.5 MHz Read Clock.
Address Mark Detector	Detects the address mark and transmits an Address Mark Found to the controller.

Arm Preamp

The Arm Preamp is an LSI chip that selects a data head on its head arm and either switches write current through the head or amplifies the read signal detected by the head. These paragraphs concentrate on the preamp's read function and assume that head selection has occurred.

The LSI chip functions as a read preamp when the -Write Enable line is inactive (high). The chip contains a separate differential amplifier for each head, and head selection enables the differential amplifier associated with the desired head. In read operations, both coils in the selected head develop a readback pulse when the head passes over a written flux reversal on the disk. The head coil centertap is not used, and the other two coil leads provide a differential input to the preamp.

The differential amplifier selected in the chip amplifies the read signal and sends it on the Read Data lines to read circuitry on the Read/Write board.

Data Latch Circuit

The Data Latch circuit receives analog read data from the selected Arm Preamp and converts it into digital data. As shown in figure 1-58, some portions of the Data Latch circuit are located inside the Data Latch Analog Master Chip, and other portions are outside the chip.

The input signal is amplified by the Buffer Amp, provided that -Write Enable is inactive (high). The +HCA 0 line establishes the gain of the Buffer Amp -- lower for outer heads or higher for inner heads. After further amplification (inside the master chip), the signal is split into three signal paths -- the high resolution channel, the low resolution channel, and the hysteresis channel. The high and low resolution channels contain independent wave-shaping circuitry, and they provide separate inputs to the Data Latch FF. The high resolution channel supplies delayed clock pulses to the Data Latch FF, and the low resolution channel supplies a D-input to the Data Latch FF. Successive clock pulses toggle the FF when the D-input has changed. Each transition of the Data Latch FF triggers a 28 ns one-shot that pulses the $\pm$Latched Data output lines once for each written flux transition sensed by the data head. These pulses are gated by a multiplexer to the Read Comparator.

Splitting the analog data signal into two paths and combining the high and low resolution channels in the Data Latch FF is a system that discriminates against high frequency noise components in the Analog Data but maintains the timing of the data transitions. The low resolution channel uses a band-pass filter (with a 5 MHz bandwidth) followed by a zero-cross detector to develop a digital waveform similar to the Write Data waveform used in recording. However, filtering out the high frequency components of the input signal lowers the timing resolution of the channel's output signal. The high resolution channel uses a band-pass filter (with a 13 MHz bandwidth) followed by a zero-cross detector and a delayed pulse-forming circuit. With its wider bandwidth, this channel closely follows the timing present at its input. Each change in the low resolution signal is clocked into the Data Latch FF by a delayed clock pulse from the high resolution channel. Erroneous clock pulses from the high resolution channel do not toggle the Data Latch FF because they do not follow a change in the FF's D-input.

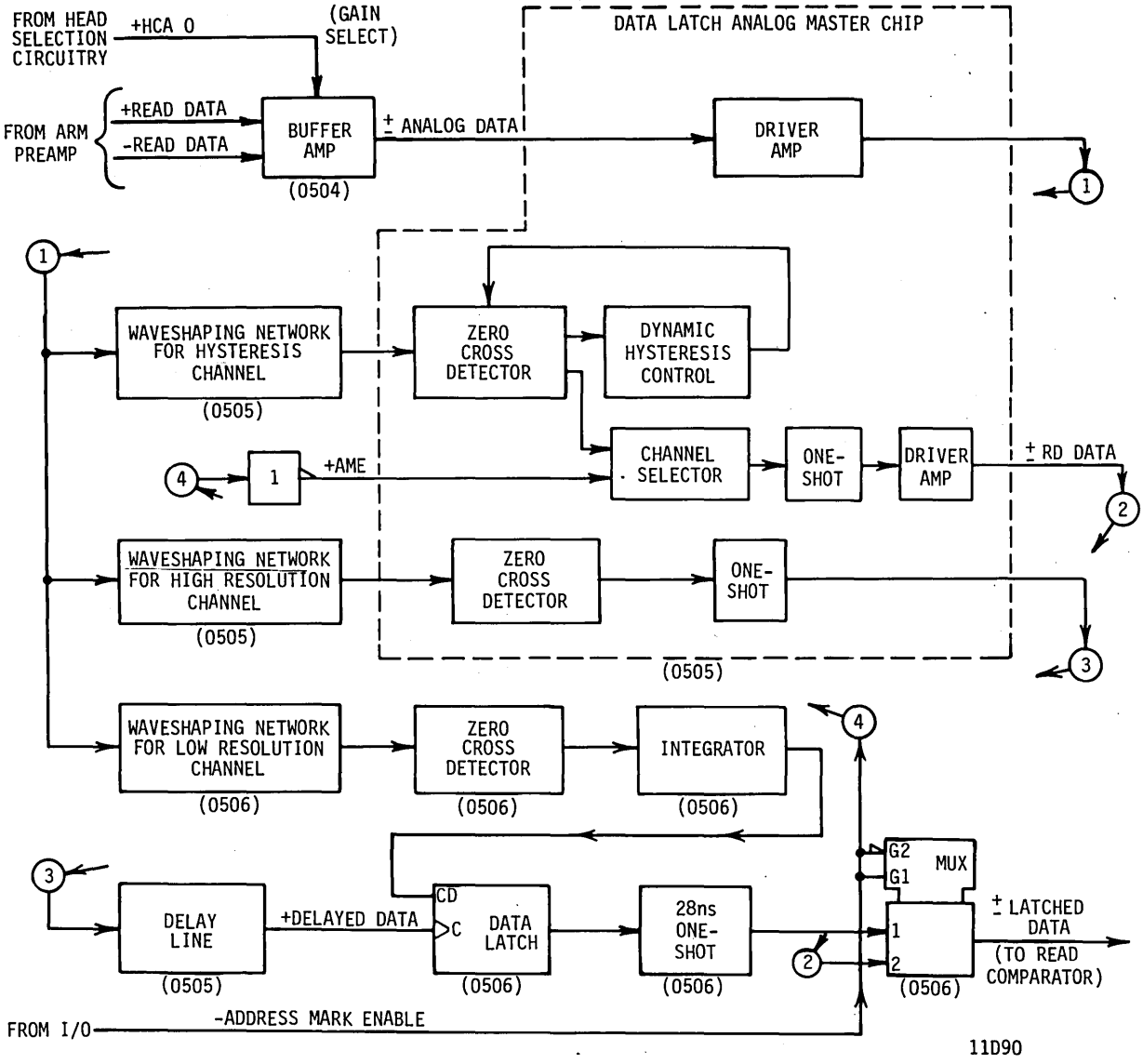


Figure 1-58. Data Latch Block Diagram

The Data Latch circuitry switches into a different operating mode during an address mark search. In an address mark search, the pulses on the ±Read Data output lines cease when the head is passing over an address mark, which is a previously erased segment of the track. An address mark search is initiated when Address Mark Enable goes active, which happens when the controller issues Control Select (Tag 3) with Bus bits 1 and 5 active. With Address Mark Enable active, the multiplexer selects the output of the hysteresis channel for the ± Latched Data signal. Inside the master chip, the hysteresis channel contains a zero-cross detector and a dynamic hysteresis control circuit. To regulate operation of this zero-cross detector and to prevent unwanted output pulses during an address mark, the dynamic hysteresis control circuit adjusts the switching thresholds of the zero-cross detector. In this way, noise pulses arising during the address mark are prevented from producing transitions in the output signal.

The ±Latched Data from the Data Latch circuitry is sent to the Read Comparator - Address Mark ECL Logic Array.

Read Comparator and PLO

The Read Comparator and PLO circuitry uses a phase-locked loop to generate the 29.01 MHz Read Clock, and processes latched read data from the Data Latch to develop clocked read data. Data Strobe commands from the controller condition the timing of clocked read data relative to the read clock to provide a means of error recovery to the read circuitry.

Figure 1-59 is a simplified block diagram of the Read Comparator and PLO circuitry. The phase-locked loop uses the Read Oscillator Control portion of the Read Comparator - Address Mark ECL Logic Array to regulate operation of the Current Pump and to provide stop/start control of the Voltage-Controlled Oscillator (VCO). The Current Pump supplies a Control Voltage signal to the VCO that determines the frequency of the 2F RD OSC signal output from the VCO. The 2F RD OSC signal is fed back to the Read Oscillator Control to complete the loop.

The phase-locked loop locks the VCO frequency to one of two reference signals. When the drive is reading data (-Read Gate low), the phase-locked loop uses the pulse train on the Latched Data line as a timing reference. In this case, the Read Oscillator Control uses a quadrature comparator to drive the Pump Up and Pump Down lines as necessary to keep the rising edges of the 2F RD OSC signal coincident with the rising edges of +Latched Data pulses. For each Latched Data pulse, the quadrature comparator outputs a variable-length pulse on the Pump Up line, followed by a fixed-length pulse on the Pump Down line.

When the Pump Up and Pump Down pulses differ in length, the Control Voltage to the VCO varies accordingly to phase shift the VCO and bring it into phase lock.

When the drive is not reading data (-Read Gate high), the phase-locked loop maintains the VCO frequency close to the value it has during read operations. In this mode, a coincidence comparator in the ECL Logic Array monitors the phase difference between the 7.25 MHz WRT OSC signal (derived from the Write PLO) and the 2F RD OSC signal fed back from the VCO. When the rising edge of the 7.25 MHz signal leads the rising edge of the 2F signal, this comparator pulses the Pump Up line to increase the Read VCO frequency. Conversely, when the rising edge of the 7.25 MHz signal lags the rising edge of the 2F signal, this comparator pulses the Pump Down line to decrease the Read VCO frequency.

The Read Oscillator Control circuitry uses the Stop/Start VCO line to control VCO operation while switching between the quadrature and coincidence comparators. The Stop/Start VCO line goes active for approximately 200 ns after the Latched Data pulse following a change in the Read Gate signal. While the Stop/Start VCO line is active, the VCO is inhibited, and its control voltage is held constant. This enables the Read PLO to phase lock within 2 microseconds during the switching transitions.

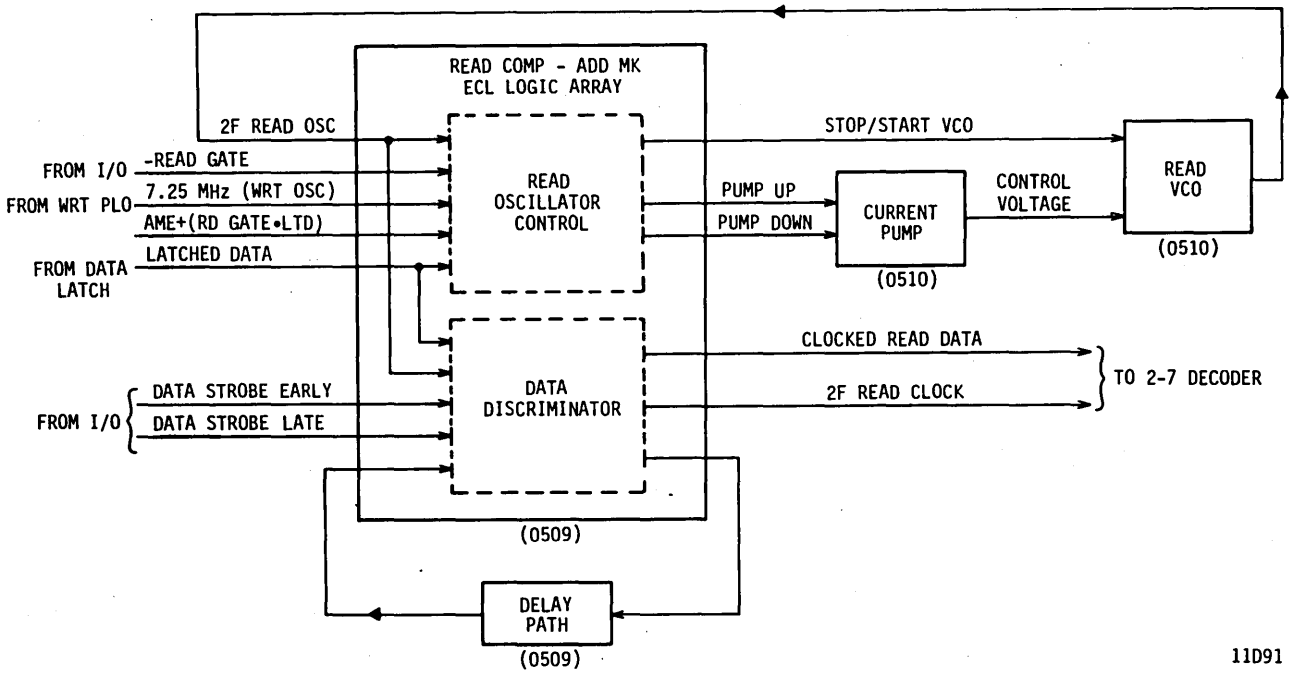


Figure 1-59. Read Comparator and PLO Block Diagram

The Data Discriminator portion of the Read Comparator - Address Mark ECL Logic Array conditions the 2F Read Clock and Clocked Read Data signals for use in the 2-7 Decoder (see figure 1-59). With nominal timing, pulses on the Clocked Read Data line are active for one 2F bit cell (34.45 ns), and positive transitions of the 2F Read Clock coincide with the center of Clocked Read Data pulses. For error recovery, the controller can issue a Data Strobe Early or a Data Strobe Late command (data early or late relative to clock) to shift this timing either way from its nominal value. The controller commands Data Strobe Early by issuing Tag 3 (Control Select) with Bus bit 7 active. The Data Discriminator responds by routing the clock signal through a 2.9 ns delay path. This process delays the 2F Read Clock relative to the Clocked Read Data pulses. The controller commands Data Strobe Late by issuing Tag 3 with Bus bit 8 active. The Data Discriminator responds by routing the data signal through a 2.9 ns delay path. This process delays the Clocked Read Data pulses relative to the 2F Read Clock.

The Clocked Read Data and 2F Read Clock signal are input to the 2-7 Decoder, which converts the read data from 2-7 code into NRZ form and generates the 14.5 MHz Read Clock.

2-7 Decoder

The 2-7 Decoder converts 2-7 data into NRZ data and generates the 14.5 MHz Read Clock from the 29.01 MHz Read Clock. Both inputs, the 2-7 data and the 29.01 MHz Read Clock, come from the Read Comparator and PLO circuitry.

As described under Basic Read/Write Principles, there is a one-to-one correspondence between seven 2-7 code words and seven NRZ code words. The decoder recognizes the coding in the 2-7 read data input as a succession of the seven 2-7 words, and outputs a series of NRZ code words, each one translated from its 2-7 equivalent. Table 1-4, presented under Basic Read/ Write Principles, shows the translation used between the two groups of seven code words. The 2-7 decoding function takes place within a single ECL Logic Array, the 2-7 Encode/Decode chip.

Figure 1-60 is a simplified block diagram of the 2-7 Decoder. The decoder synchronizes after the +Lock to Data input goes inactive (low). This occurs 3 microseconds after Read Gate goes active unless an address mark search is in progress. If an address mark search is in progress, +Lock to Data goes inactive 3 microseconds after Address Mark Enable goes inactive, provided

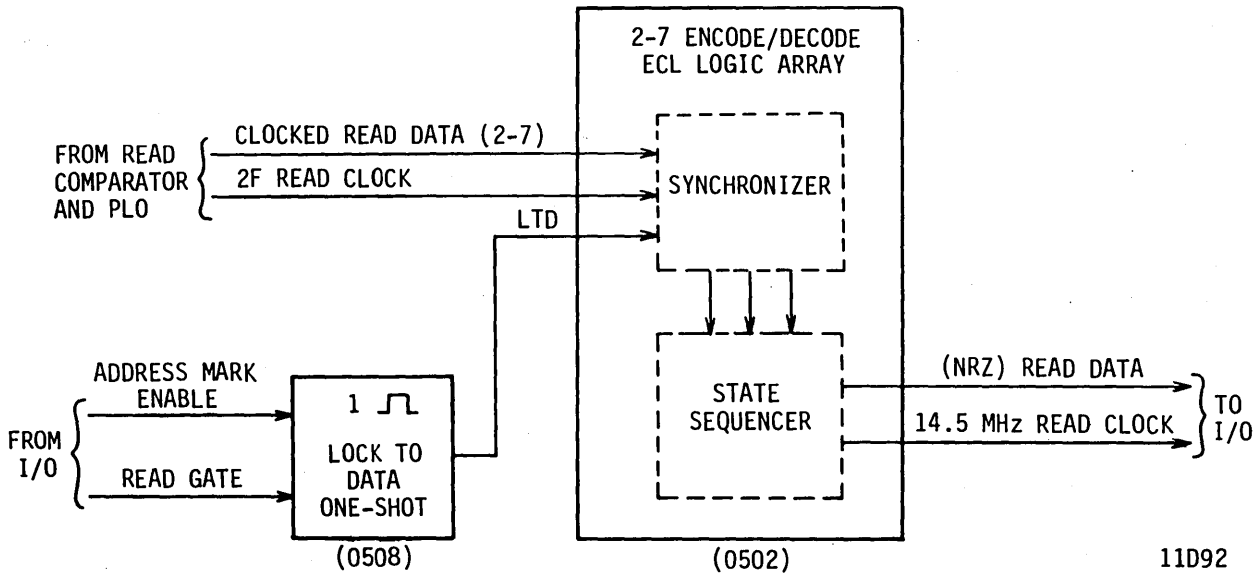


Figure 1-60. 2-7 Decoder Block Diagram

that Read Gate stays active. Once +Lock to Data goes inactive, synchronization occurs when the 2-7 input data contains three or more binary zeros followed by a binary one. This binary one sets up the proper phase of the 14.5 MHz Read Clock relative to the NRZ Data output line and initiates the decoding process. The clock and decoding operations are discussed in the following paragraphs.

The 14.5 MHz Read Clock is generated from the 29.01 MHz Read Clock as this signal clocks a divide-by-two FF. The set output of the FF is inverted and supplied to the D-input through a gate that is enabled as a result of synchronization. Synchronization selects which positive edge of the 29.01 MHz Read Clock determines the positive edge of the 14.5 MHz Clock.

The decoding function is performed by a state sequencer. The state sequencer has eight FFs, and each of the eight states corresponds to one of the FFs being set. It operates by shifting states on each falling edge of the 14.5 MHz Read Clock. Thus, the interval for each state is one NRZ bit cell (68.9 ns). Two factors determine the current state of the sequencer. These are the previous state and the binary values of the last two 2-7 data bits input to the circuit. Therefore, at any time the state of the sequencer reflects the recent decoder

inputs. The binary level decoded on the NRZ Data lines is state-dependent. During two of the states (NRZ bit cells), the output is binary zero, and during the other states, the output is binary one. In summary, the way the sequencer maps one state into the next state implements the specified translation from 2-7 data words into NRZ data words.

The decoder output stays low until synchronization occurs, and there is a processing delay of four 2-7 bit cells within the decoder.

The decoder sends the ±NRZ Read Data and ±Read Clock outputs to the I/O board to be transmitted on the interface to the controller.

Address Mark Detection

The Address Mark Detector, which is part of the Read Comparator/Address Mark ECL Logic Array, monitors the Latched Read Data signal from the Data Latch during an address mark search. If a gap of 1.38 to 2.48 microseconds is detected between incoming read pulses, the detector sets the Address Mark Found line, and the I/O circuitry sets the Address Mark line on the interface.

Figure 1-61 shows the input and output signals for the Address Mark Detector. An address mark search occurs when the controller issues Tag 3 (Control Select) with Bus bits 1 and 5 active. In this situation, the -Read Gate line is low and the AME line is high. Together, these two signal inputs enable the Address Mark Detector.

The detector contains a counter circuit which is driven by the 14.5 MHz Clock signal from the Write PLO until it is reset by incoming read pulses. If incoming read pulses are detected during the interval from 20 to 36 clock periods, the Address Mark Found line is set. This line remains set until the lock-to-data interval ends (3 microseconds after Address Mark Enable is cleared) or until -Read Gate goes high.

The detector also contains a discriminator that distinguishes between read data gaps, caused by media defects, and gaps indicating address marks. If a defect is crossed, the discriminator inhibits the Address Mark Found output.

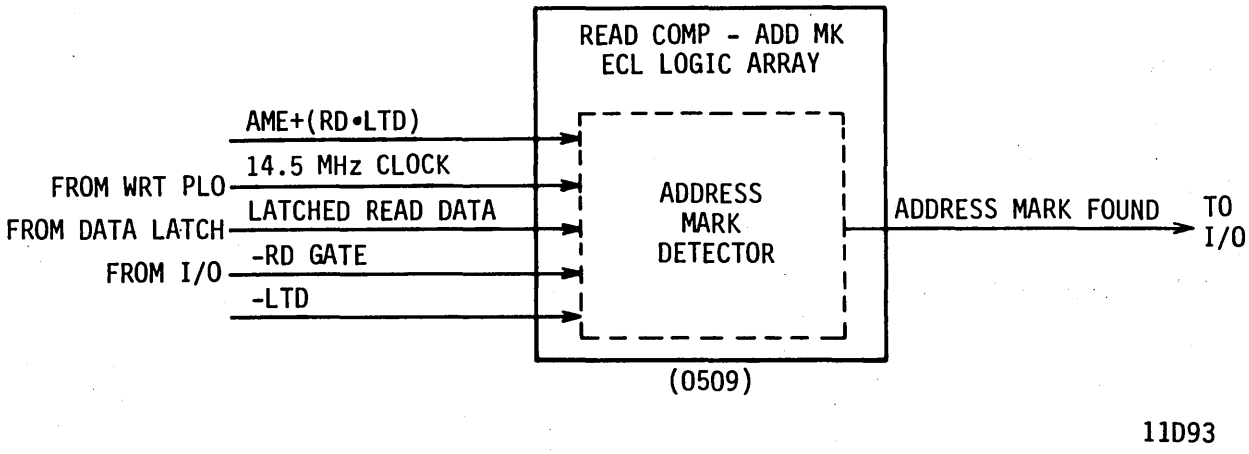


Figure 1-61. Address Mark Detector Block Diagram

FAULT AND ERROR CONDITIONS

GENERAL

The following paragraphs describe those conditions which are interpreted by the drive as errors. These errors are divided into two categories: (1) those that generate the Fault signal and (2) those that do not generate the Fault signal. Included in the following descriptions are a list of conditions that produce each error status, the effect of that status on drive operation, and actions that clear the status indication to return the drive to normal operation.

ERRORS INDICATED BY FAULT SIGNAL

General

The drive has monitoring circuitry that recognizes six types of error conditions. When any of these error conditions occurs, it sets the respective latch in the I/O Gate Array. An OR circuit in the gate array receives inputs from the six latches; if one or more of the latches is set, the OR circuit activates the Fault line. The Fault line remains active until the latches are cleared.

When the Fault line goes active, it lights the FAULT indicator on the operator panel, disables write operations, and issues Fault and Write Protected status to the controller. The active Fault line interrupts the MPU at PIA-0 (see figure 1-62). The MPU responds by dropping the Ready signal and by communicating with the I/O Gate Array to identify the fault. The Unit Ready line to the controller goes inactive, and the READY indicator on the operator panel flashes until the fault is cleared.

Provided the error condition or conditions no longer exist, the Fault signal is cleared by the following:

- Controller Fault Clear command (Tag 3 with Bus bit 4)
- Fault Clear switch on operator panel
- Removing power from the drive by means of CB1

The controller Fault Clear command is decoded inside the I/O Gate Array to develop a reset input for the latches. When the Fault Clear switch is pressed, it interrupts the MPU at PIA-2. The MPU responds by pulsing the I/O Control 1 and 2 lines with a code that develops a reset input for the latches. In either case, the reset input will clear a latch only if it is no longer being set by the error condition. In the process of removing and reapplying power to the drive, the fault circuitry is initialized as part of the power initialization, and any pre-existing fault status is lost.

The following paragraphs describe the individual fault conditions which set each of the latches in the I/O Gate Array and thus activate the Fault signal.

Voltage Fault

This fault is generated whenever either the $\pm$15 or $\pm$5 voltages are detected to be below satisfactory operating levels. Threshold detectors on the Control board activate the Voltage Fault line if any of the following voltages drop:

- The +15 V supply drops to 14.35 V.
- The +5 V supply drops to 4.83 V.
- The -5 V supply drops to -4.90 V.
- The -15 V supply drops to -14.46 V.

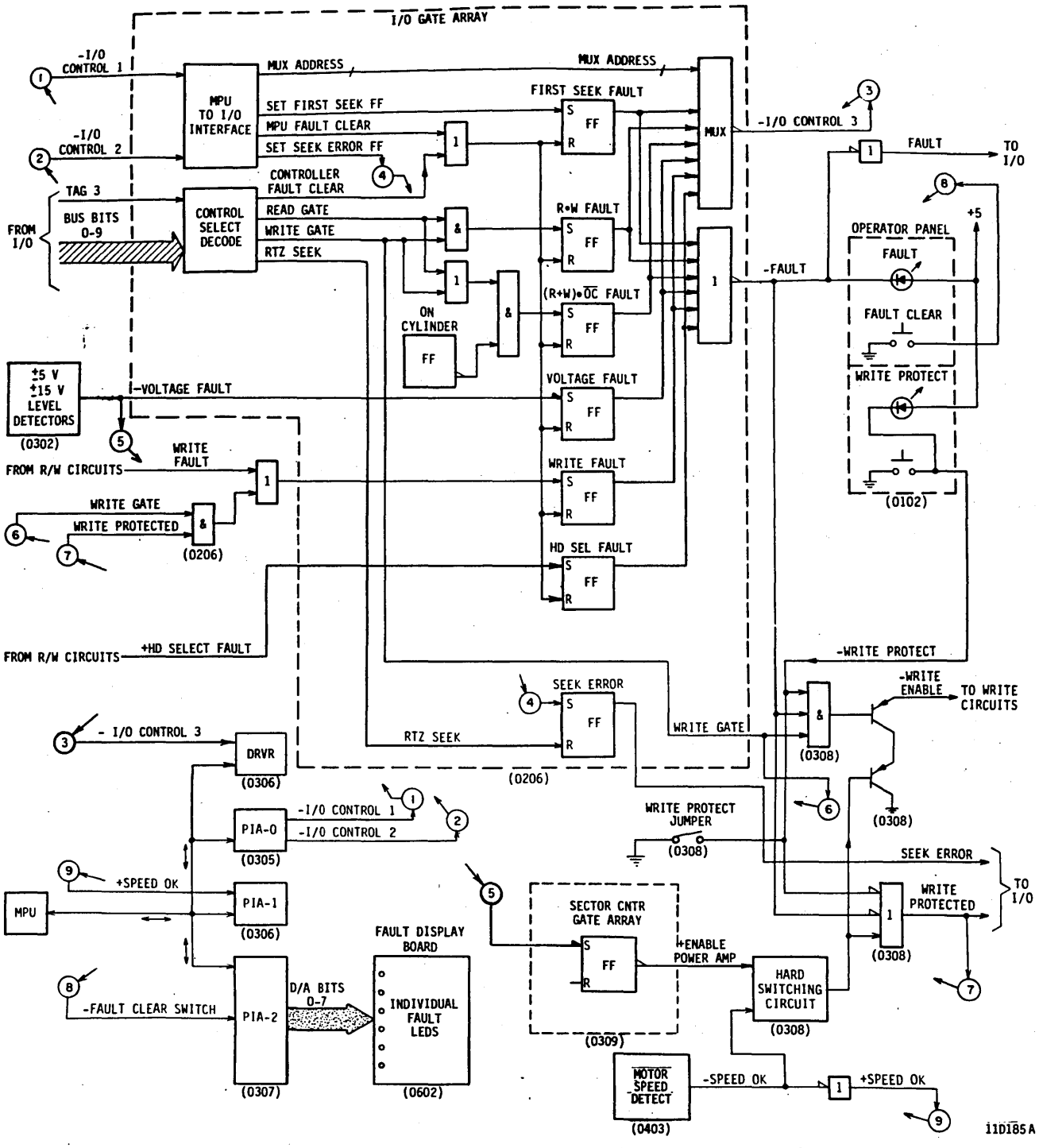


Figure 1-62. Fault and Error Detection Circuitry

When the -Voltage Fault signal goes low, it sets the individual fault latch in the I/O Gate Array and latches the Enable Power Amp signal inactive in the Sector Counter Gate Array. When the Enable Power Amp signal is inactive, it adds an additional degree of write protection, needed to safeguard existing data on the disks by inhibiting the write circuitry while a voltage problem exists. A hard switching circuit deactivates the -Write Enable line when the +Enable Power Amp line is low and keeps it inactive for about 1/2 second after that line is reactivated. This supplements the write protection normally invoked when the Fault line is active or when the drive is placed in the Write Protect mode.

An additional voltage detector circuit detects when the +5 V supply drops to 4.73 V, making MPU operation unreliable. This condition generates a -Low Vcc signal to produce the Reset signal for the MPU chips and the DC Master Clear signal for the gate arrays. Also, when the -Low Vcc signal goes active, the -Disable Retract Power line goes high to retract the actuator.

Read or Write and Off Cylinder

This fault is generated if the drive is in an off cylinder condition and it receives a Read or Write gate from the controller. The I/O Gate Array decodes both gates from Tag 3 commands and contains the On Cylinder FF. When the On Cylinder FF is cleared and either gate goes active, logic in the gate array sets the associated fault latch.

Write Fault

A write fault is encoded if any of the following conditions exist:

- Write Gate received while drive is in Write Protected mode
- Write Clock not present when Write Gate is active
- No write data transitions when the Write Gate is active (except when the Address Mark Enable signal is active)
- Head open (bad head detected)
- No Arm Enable signal is active when Write Enable is active.

All conditions except the first one activate the Write Fault line coming from the Read/Write board. Gating circuitry on the Read/Write board develops the Write Fault signal when individual fault conditions are detected, provided that Write Enable is active and Address Mark Enable is inactive. The gating circuitry keeps the Write Fault line inactive during transitions between read and write operation. The Write Fault line or the combination of Write Protect and Write Gate lines active sets the associated latch in the I/O Gate Array.

Head Select Fault

This fault is generated when more than one head is selected during a write operation. When this condition is detected, it sets the associated latch in the I/O Gate Array.

Read and Write Fault

This fault is generated whenever the drive receives a Read Gate and a Write Gate simultaneously. This condition is detected internally in the I/O Gate Array to set the associated latch.

First Seek Fault

First Seek fault, as opposed to Seek Error, results from error conditions that occur during the load operation. Seek Error, on the other hand, indicates error conditions that occur during normal seeks and RTZ seeks. First Seek faults generate an active Fault signal while Seek Errors activate the Seek Error and Seek End lines to the controller. Seek Errors are discussed in the next topic, and the error conditions that cause a First Seek fault are described in the following paragraphs.

Unlike the other individual fault latches, the latch for First Seek fault is set by the MPU. To set the latch, the MPU inputs the I/O Gate Array with a specific pulse code on I/O Control lines 1 and 2. The error conditions resulting in a First Seek fault are monitored by the MPU during the power on initialization and load operation. Assuming that the MPU is operational, it sets the associated latch in the I/O Gate Array if any of the following tests fail:

- Demodulator Active is inactive at the start of the load, but goes active after the heads move inward from the landing zone. Demodulator Active must remain stable throughout the rest of the load.

- The Fault line stays inactive during the load.
- The MPU moves the heads out of the landing zone and detects 100 cylinder pulses before a timeout occurs.
- At least one cylinder pulse is detected in the outer guard band as the heads approach track zero.
- During the first 2.1 ms of track-following, less than three cylinder pulses are detected.
- In the 11 ms interval allowed during track-following if On Cylinder Sense goes inactive, this signal returns to the active level, and less than three cylinder pulses are detected.
- No seek error occurs during the velocity calibration procedure.

The MPU aborts the load operation when a First Seek fault is indicated. Although a controller Fault Clear command will reset the Fault signal, the MPU waits until the operator panel Fault Clear switch is pressed before attempting another load.

ERRORS NOT INDICATED BY FAULT SIGNAL

General

Two types of errors do not generate the Fault status -- seek errors and the motor speed error. The seek error has an associated status FF, while the motor speed error does not.

Motor Speed Error

The -Speed OK signal is developed by circuitry on the Linear Power Amplifier board. When the spindle speed falls below 1275 r/min, the -Speed OK signal goes high. The -Speed OK signal is used by several circuits on the Control board (see figure 1-62), and these uses are outlined in the following paragraphs.

An interlocks circuit monitors the -Speed OK line to provide write protection if the line goes low. Write protection is needed to safeguard existing data on the disk by inhibiting the write circuitry while a motor speed error exists. A hard switching circuit deactivates the -Write Enable line when -Speed OK goes high and keeps it inactive for about 1/2 second after -Speed OK goes low again.

The MPU monitors the +Speed OK signal at PIA-1. If the +Speed OK signal goes low, the MPU drops the Ready signal, retracts and locks the actuator, and stops the spindle motor. The MPU then initiates a sequence to restart the motor, perform a load seek, and bring the drive to the ready condition.

Seek Error

Seek Error is a status signal sent to the controller indicating error conditions that occur during normal seeks and RTZ seeks. The Seek Error signal is active when the Seek Error FF, located in the I/O Gate Array, is set.

During normal seeks and RTZ seeks, the MPU tests certain error conditions. If any tests fail, the MPU sets the Seek Error FF in the I/O Gate Array. These tests include the following:

- The Demodulator Active signal is active at the start and end of normal seeks, and it is active throughout RTZ seeks.
- Fault stays inactive throughout seeks.
- The time required for a normal seek is less than the 60 ms timeout allowed by the MPU.
- During the first 2.1 ms of track-following, less than three cylinder pulses are detected (normal or RTZ seeks).
- In the 11 ms interval allowed during track-following if On Cylinder Sense goes inactive, this signal returns to the active level, and less than three cylinder pulses are detected.
- Less than three guard band pulses are detected at PIA-1 during one seek. Inner and outer guard band pulses are counted in normal seeks. Only inner guard band pulses are counted during RTZ seeks.
- The MPU gets a reset input to force it out of a hang condition.

If any of these tests fails, the MPU sets the Seek Error FF using I/O Control lines 1 and 2 (see figure 1-62). This causes both the Seek Error and Seek End status signals to be sent to the controller via the I/O transmitters.

In the event of a Seek Error, the MPU drops all servo commands, allowing the heads to remain in their current position over the disks. The seek error condition cannot be cleared except by a controller RTZ command. An attempt by the controller to perform a read or write operation while the seek error condition exists will result in the generation of a Read or Write and Off Cylinder fault.

SECTION 2

GENERAL MAINTENANCE INFORMATION

GENERAL MAINTENANCE INFORMATION 2

INTRODUCTION

This section contains general information relating to maintenance of the drive. A person performing maintenance should be familiar with the information in this section in addition to being thoroughly familiar with drive operation. Information is divided into the following areas:

- Warnings and Precautions - Lists warnings and precautions that must be observed when working on the drive.
- Electrostatic Discharge Protection - Provides instructions for the proper handling of electrostatically sensitive devices.
- Maintenance Tools and Materials - Lists the tools and materials required to perform maintenance on the drive.
- Testing the Drive - Provides information concerning the electrical testing of the drive.
- Accessing Assemblies for Maintenance - Identifies the various parts of the drive and describes how to access these parts for maintenance.

WARNINGS AND PRECAUTIONS

Observe the following warnings and precautions at all times. Failure to do so may cause equipment damage and/or personal injury.

- Use care while working on the drive when fully extended on slides. Ensure that the rack or cabinet, in which the drive is mounted, is adequately supported or counterbalanced to prevent the drive from falling forward when extended.
- Use care while working with the power supply because line voltages are present.
- Do not attempt to disassemble the module. It is not field repairable. Replace the entire module assembly if it is found to be defective.

- Do not operate the drive over an extended period of time without the top cover installed.

- Always deenergize drive before removing or installing circuit boards, cables, or any other electrical components.

- Observe the precautions listed under Electrostatic Discharge Protection.

ELECTROSTATIC DISCHARGE PROTECTION

All drive electronic assemblies are sensitive to static electricity, due to the electrostatically sensitive devices used within the drive circuitry. Although some of these devices such as metal-oxide semiconductors are extremely sensitive, all semiconductors as well as some resistors and capacitors may be damaged or degraded by exposure to static electricity.

Electrostatic damage to electronic devices may be caused by a direct discharge of a charged conductor, or by exposure to the static fields which surround charged objects. To avoid damage to drive electronic assemblies, service personnel must observe the following precautions when servicing the drive:

- Ground yourself to the drive - whenever the drive electronics are or will be exposed, connect yourself to ground with a wrist strap (see table 2-1). Connection may be made to any metal assembly or to the ground jack on the _TRX mother board in front of the _UCX power amp. board. As a general rule, remember that you, the drive, and the circuit cards must all be at ground potential to avoid potentially damaging static discharges.

- Keep boards in conductive bags - when circuit boards are not installed in the drive, keep them in conductive static shielding bags (see table 2-1). These bags provide absolute protection from direct static discharge and from static fields surrounding charged objects. Remember that these bags are conductive and should not be placed where they might cause an electrical short circuit.

- Remove boards from bags only when you are grounded - all boards received from the factory are in static shielding bags, and should not be removed unless you are grounded.

- Turn off power to drive before removing or installing any circuit boards.

- Never use an ohmmeter on any circuit board.

MAINTENANCE TOOLS AND MATERIALS

The maintenance procedures described in this manual require the use of certain special tools, test equipment, and materials. These are listed in table 2-1 along with the appropriate CDC part number. Note that the list includes only special tools. It is assumed that the service person has normal maintenance tools.

Use of the items listed in table 2-1 is described in the procedures in which they are required. Additional information is provided on the programmable field test unit (see Testing the Drive).

TABLE 2-1. MAINTENANCE TOOLS AND MATERIALS

Description	Part Number
Front Panel Lock Tool	CDC 94391301
Gauge Plate (.115 Inch for brake adjustment)	CDC 77425250
Oscilloscope, Dual Trace	Tektronix 475A or equivalent
Programmable Field Test Unit (TB2A3A)	CDC 95614711
Scope Probe Tip (Hatchet type)	CDC 12212885
Static Shielding Bags and Ground Wrist Straps	See Accessories in Parts Data (Section 4 of Hardware Maintenance, Volume 1)
Volt/ohmmeter	Ballantine 345 or equivalent digital voltmeter

TESTING THE DRIVE

GENERAL

During testing and troubleshooting the drive is normally required to perform various operations such as reading and writing test data. Self-contained diagnostics or a programmable field test unit (PFTU) can be used to control the drive during these operations.

SELF-CONTAINED DIAGNOSTICS

Diagnostic tests are available at the fault/status display board (_UQX) located behind the operator panel cover. Setting the diagnostic mode switch to the on position causes the Ready signal to drop and places the unit in diagnostic mode. This allows the drive to be operated and controlled independent of the rest of the system. See section 3 Trouble Analysis for operating instructions.

PROGRAMMABLE FIELD TEST UNIT

The TB2A3A is the PFTU recommended for use with the drive (see table 2-1 for part numbers). The TB2A3A allows the drive to be operated and controlled independent of the rest of the system. The following outlines the procedure for connecting the PFTU to the drive. For specific instructions on connecting and operating the PFTU, see the PFTU manual.

CAUTION

To avoid possible damage to interface circuitry, always deenergize drive, controller, and PFTU before removing or installing I/O cables.

During testing, the PFTU I/O cables must be connected to the drive in place of the system I/O cables. Before disconnecting the system I/O cables, disable the controller and set drive circuit breaker CB1 to the OFF position. In a daisy chain system, power off all the drives.

When the drive is powered down, remove the system I/O cables from the drive to be tested. Connect the PFTU A cable to drive connector J4 and the PFTU B cable to drive connector J2. Connect a terminator to drive connector J3. See the installation section of hardware maintenance volume 1 for the terminator and

its part number. In a daisy chain system, make whatever connections are necessary to ensure that the other drives remain under system control, and restore power to the other drives. At the completion of testing, restore the drive to normal operation by reversing the process outlined above.

IDENTIFYING TEST POINTS

The drive circuit boards have test points to aid in signal tracing during maintenance and troubleshooting. These test points appear, physically, as shown on figure 2-1 and may be located anywhere on the component side of the circuit boards. The logic diagrams show the test points schematically.

The diagrams and maintenance procedures identify a test point by referring to the coordinate locator code and in some cases letter designator. TP-G620 (B) is an example of a test point reference. Here, G620 is the component locator and "B" is the letter designator. The coordinate locator code indicates where the test point is located on the board. The introduction to diagrams section explains how to use the coordinate locators. The test point designators are letters, etched or silkscreened onto the board, that progress in alphabetical order from left to right and top to bottom (see figure 2-2). Not all test points have letter designators. In the procedures, the letter designator is always in parenthesis, following the locator code.

ACCESSING ASSEMBLIES FOR MAINTENANCE

The major drive assemblies and components are shown on figure 2-3. These parts are accessed by extending the drive on its slides and removing the top cover.

Extend the drive by using the Front Panel Lock Tool to release the cabinet latch located behind the front panel insert (see figure 2-3), and pulling the drive forward. When extending the drive, exercise caution to ensure that the equipment rack remains stable. Also, take care that the system cabling is not damaged when sliding the drive in and out of the rack.

If it is necesary to remove the drive from the slides, see entire drive removal procedure in section 5 of this manual. Section 5 also contains a top cover removal procedure and procedures for removing most of the other field replaceable parts, including the circuit boards.

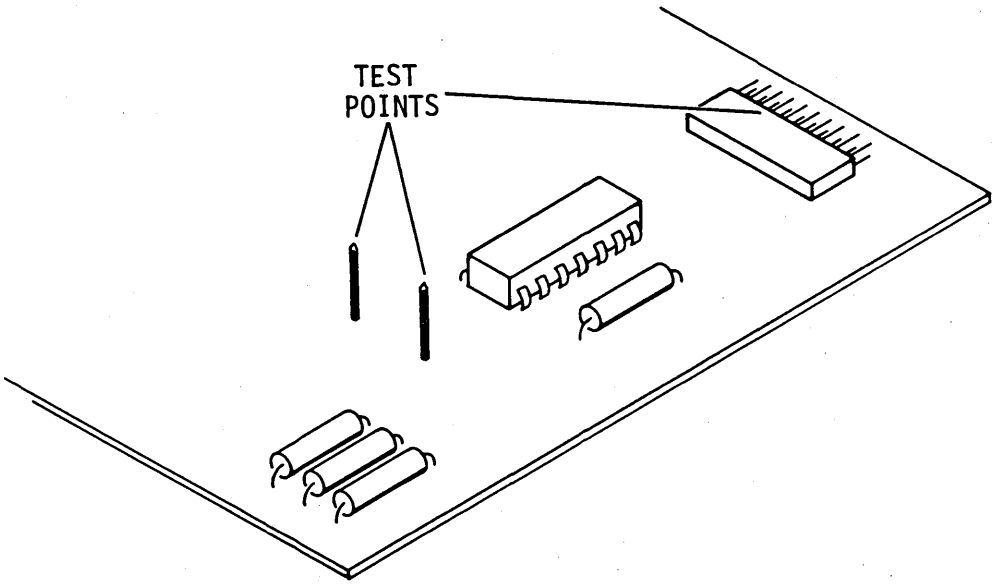


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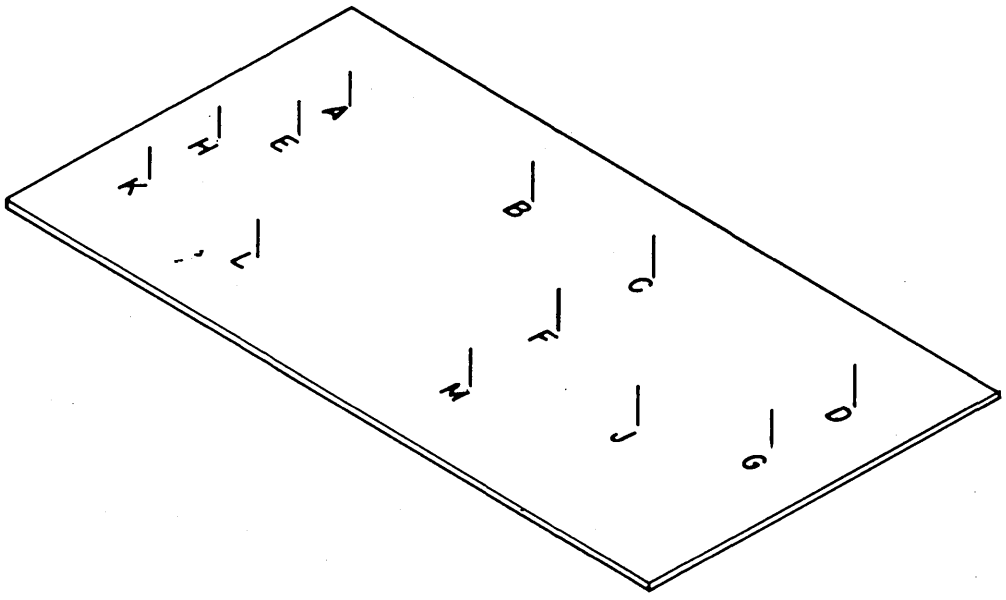
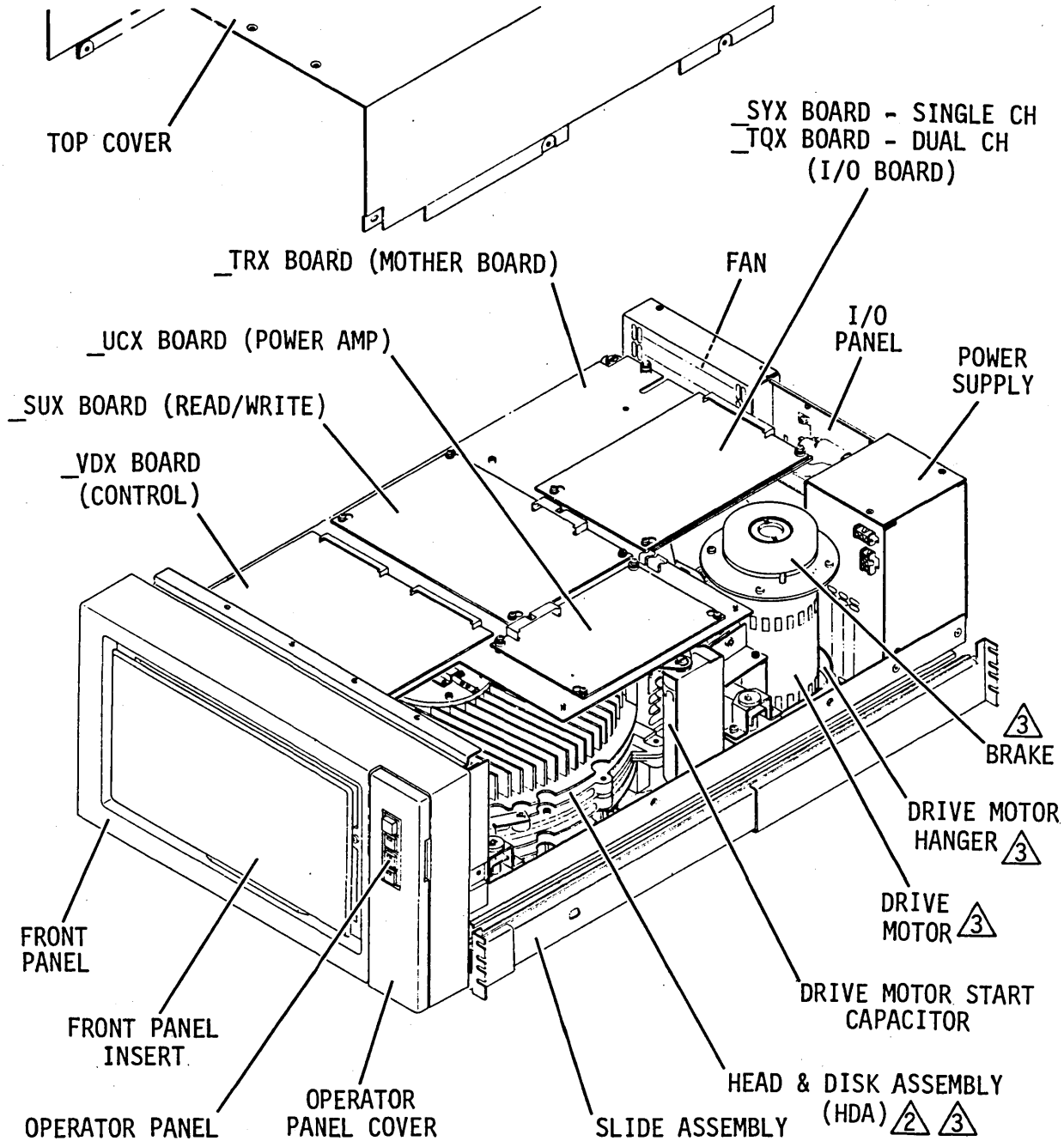
Figure 2-1. Test Points



10R110

Figure 2-2. Test Point Letter Designators

Extending the drive and removing the top cover allows access to most circuit board test points. As shown on figure 2-3 the _SUX, _SYX, _TQX, _UCX, and _VDX boards are mounted on the _TRX mother board on top of the drive and are readily accessible. The _TSX board is mounted to the underside of the HDA, and the spindle access cover must be removed from the base pan to gain access to it. The _WFV and the _RTX boards are located within the power supply assembly and require removal of power supply top covers to gain access.



NOTES:

1. FRONT PANEL LATCH AND FILTER ARE BEHIND INSERT.
2. _TSX (HDA INTERFACE) BOARD AND ACTUATOR UNLOCKING SOLENOID COIL ARE LOCATED ON UNDERSIDE OF HDA (SEE SHEET 4)
3. PART OF MODULE ASSEMBLY. THESE PARTS ARE ATTACHED TO HDA AND ARE REMOVED FROM DRIVE WHEN HDA IS REMOVED.

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Figure 2-3. Component Locator (Sheet 1 of 7)

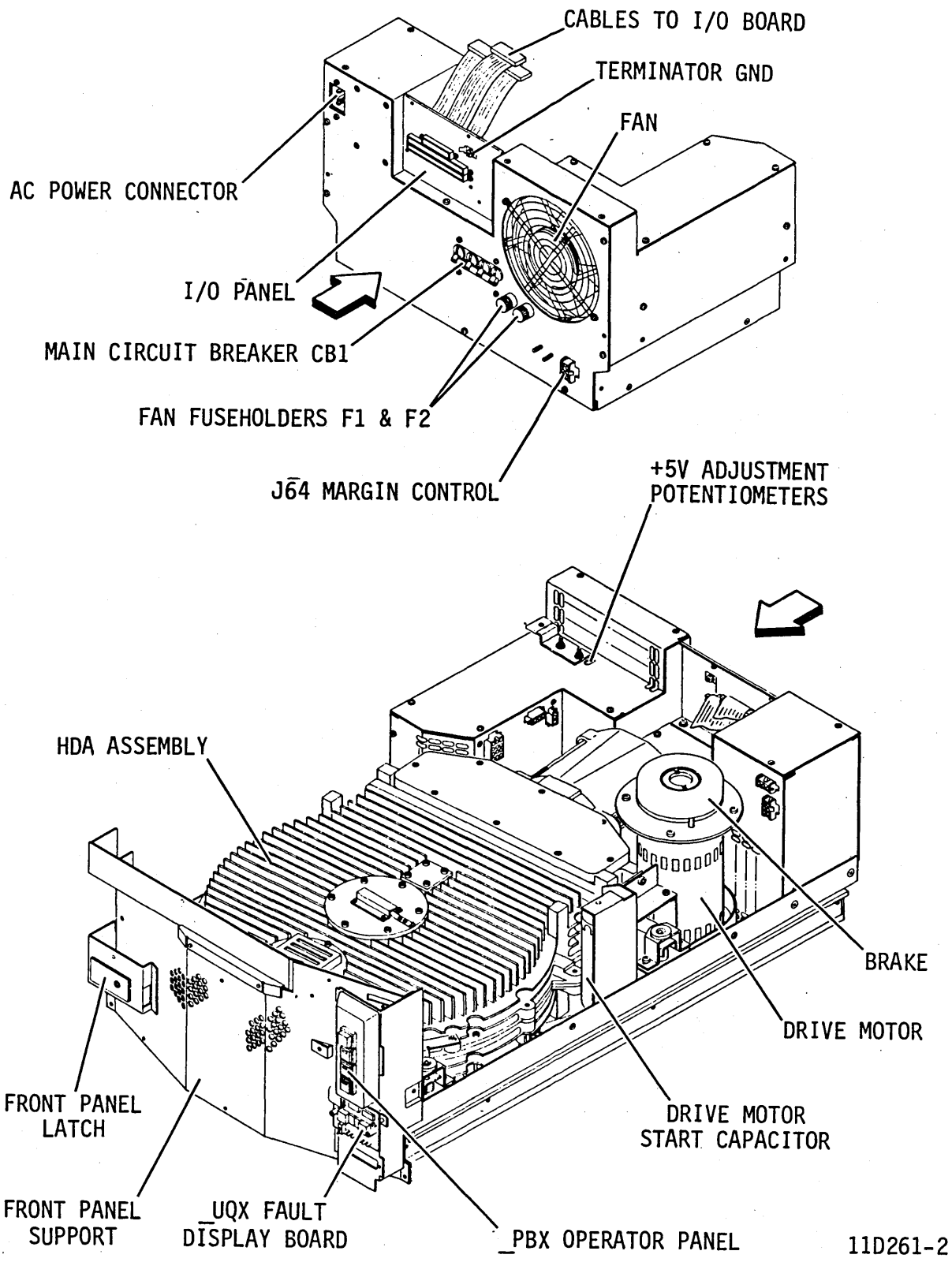


Figure 2-3. Component Locator (Sheet 2)

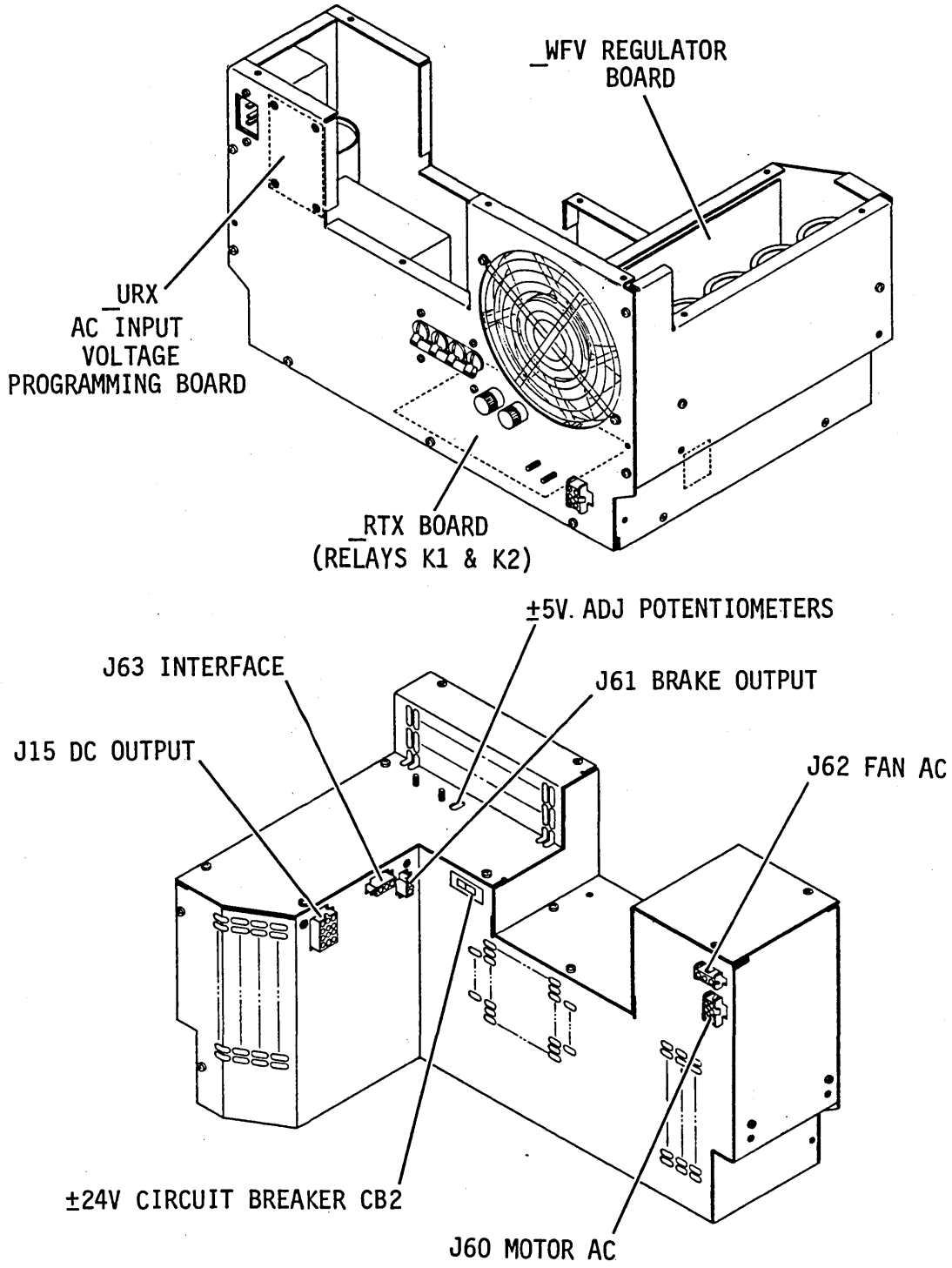
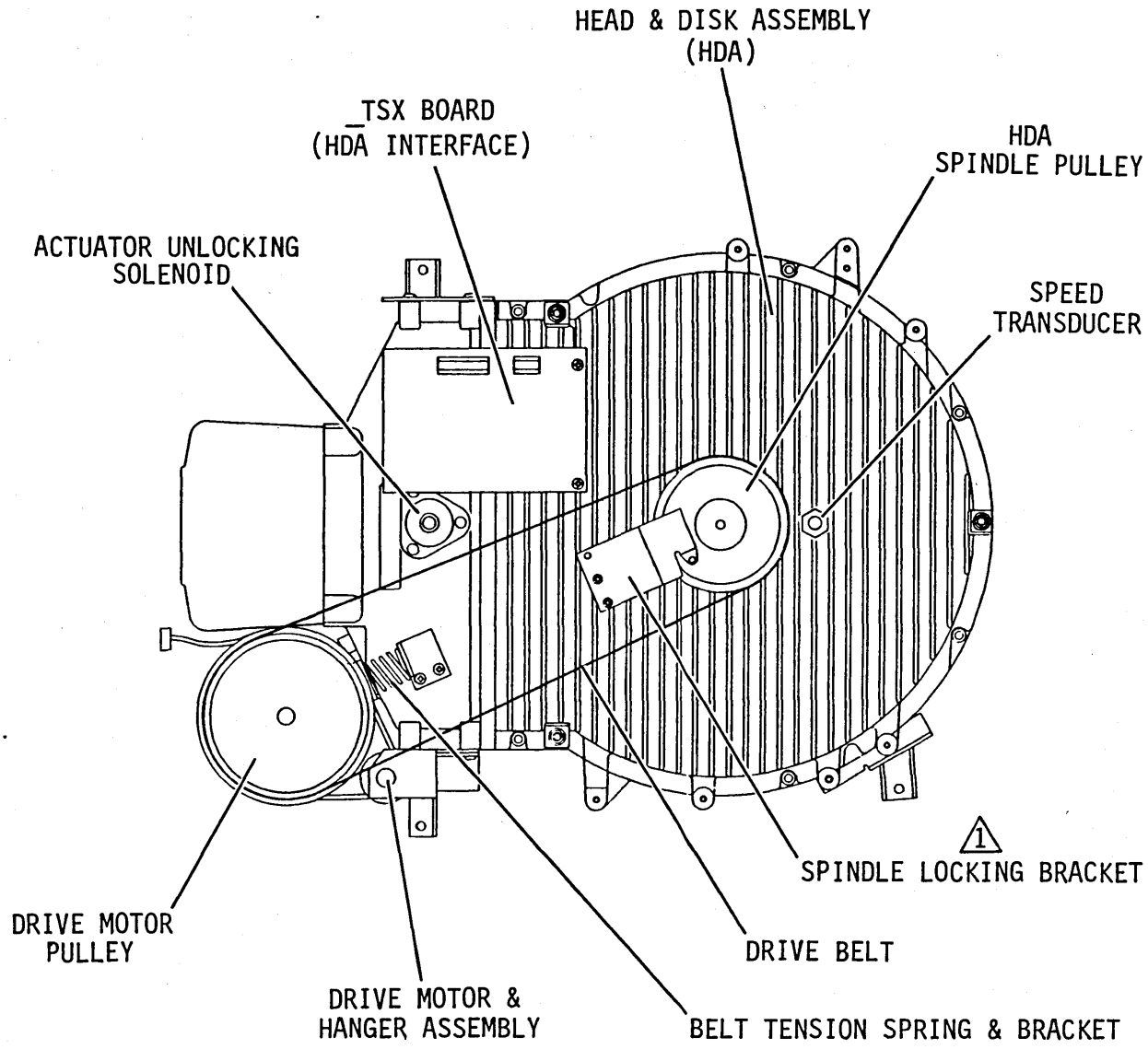


Figure 2-3. Component Locator (Sheet 3)

MODULE ASSEMBLY
BOTTOM VIEW

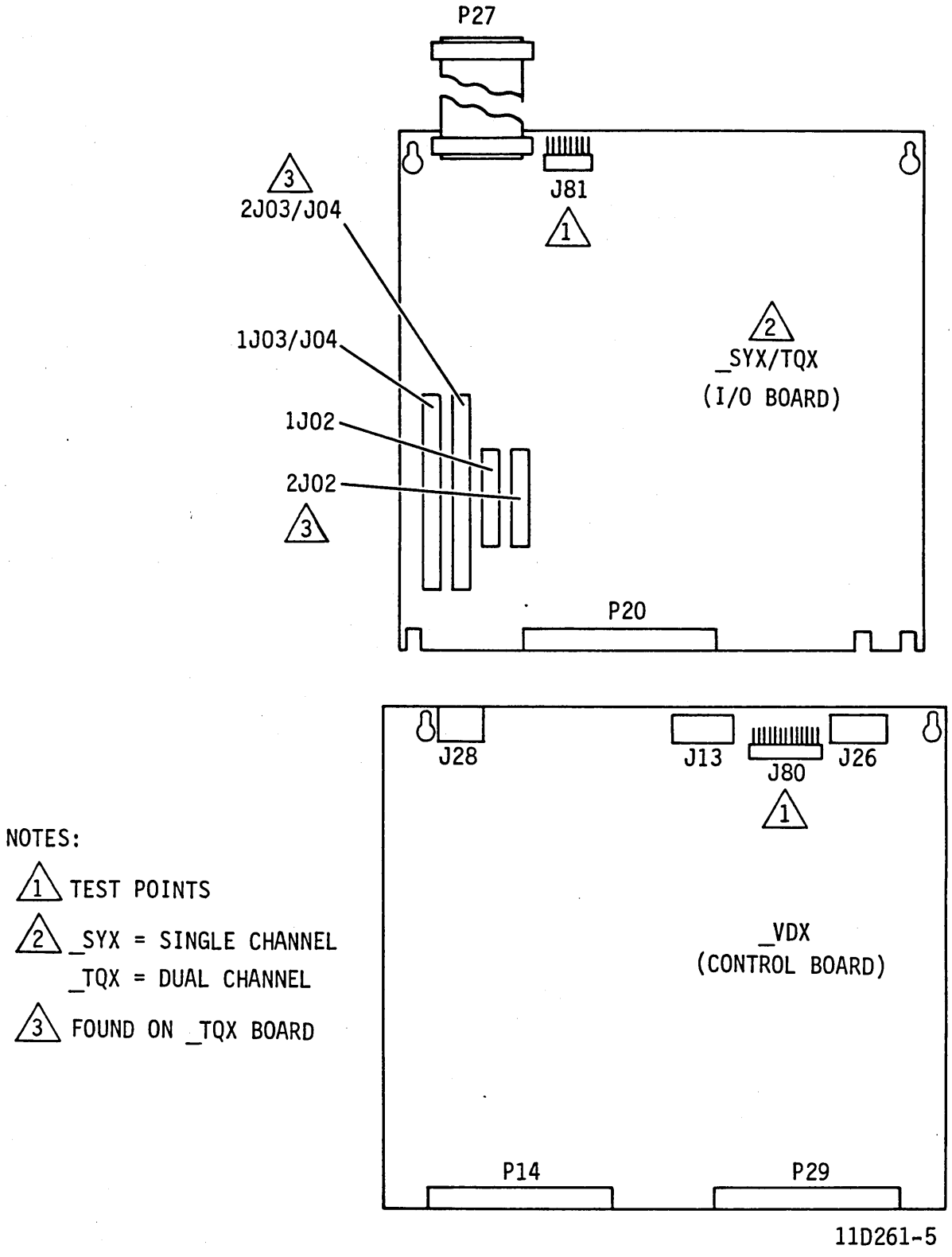


NOTES:

1. SHOWN IN LOCKED POSITION.

11D261-4

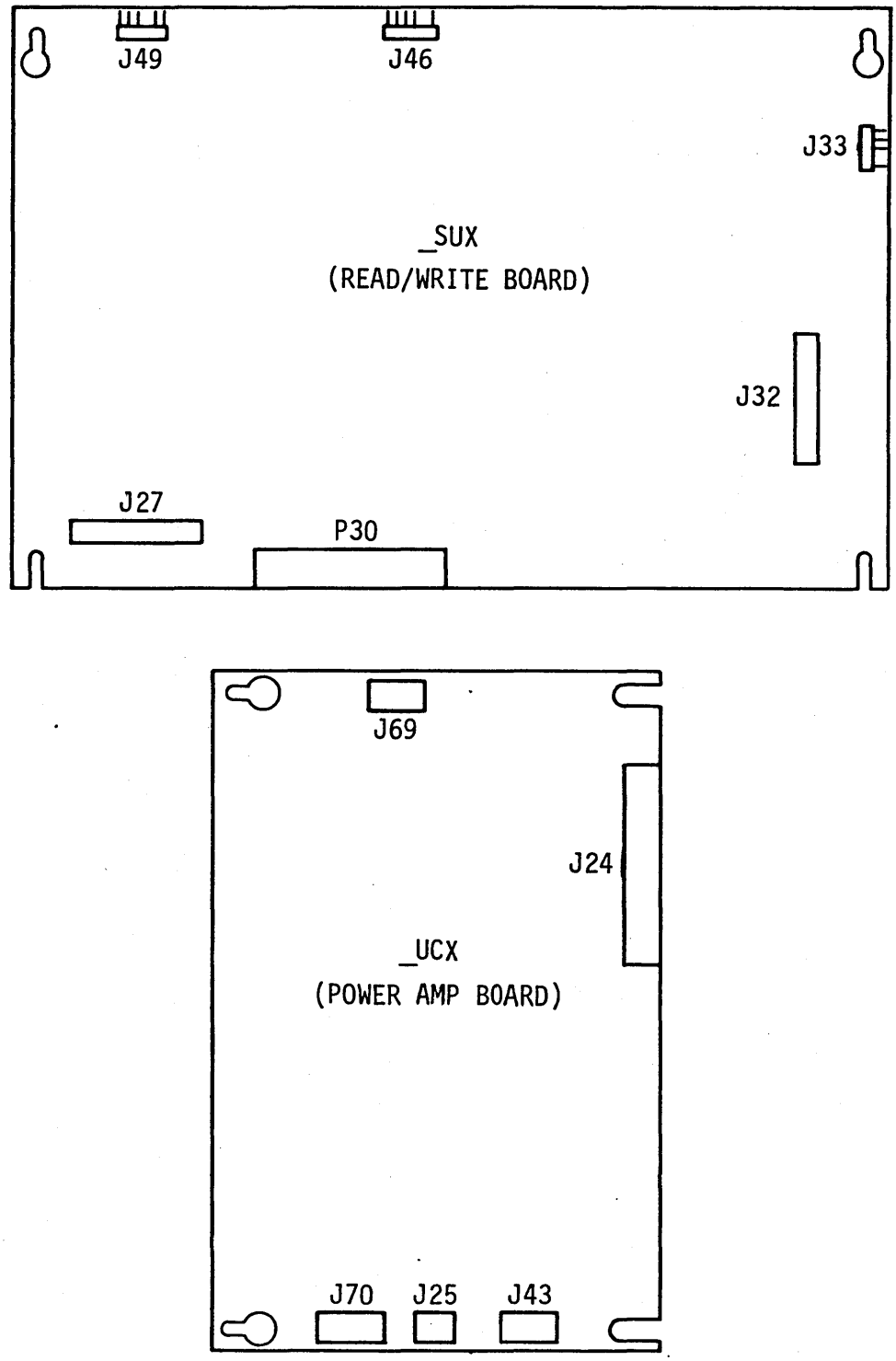
Figure 2-3. Component Locator (Sheet 4)



NOTES:

1. TEST POINTS
2. _SYX = SINGLE CHANNEL
   _TQX = DUAL CHANNEL
3. FOUND ON _TQX BOARD

Figure 2-3. Component Locator (Sheet 5)



11D261-6

Figure 2-3. Component Locator (Sheet 6)

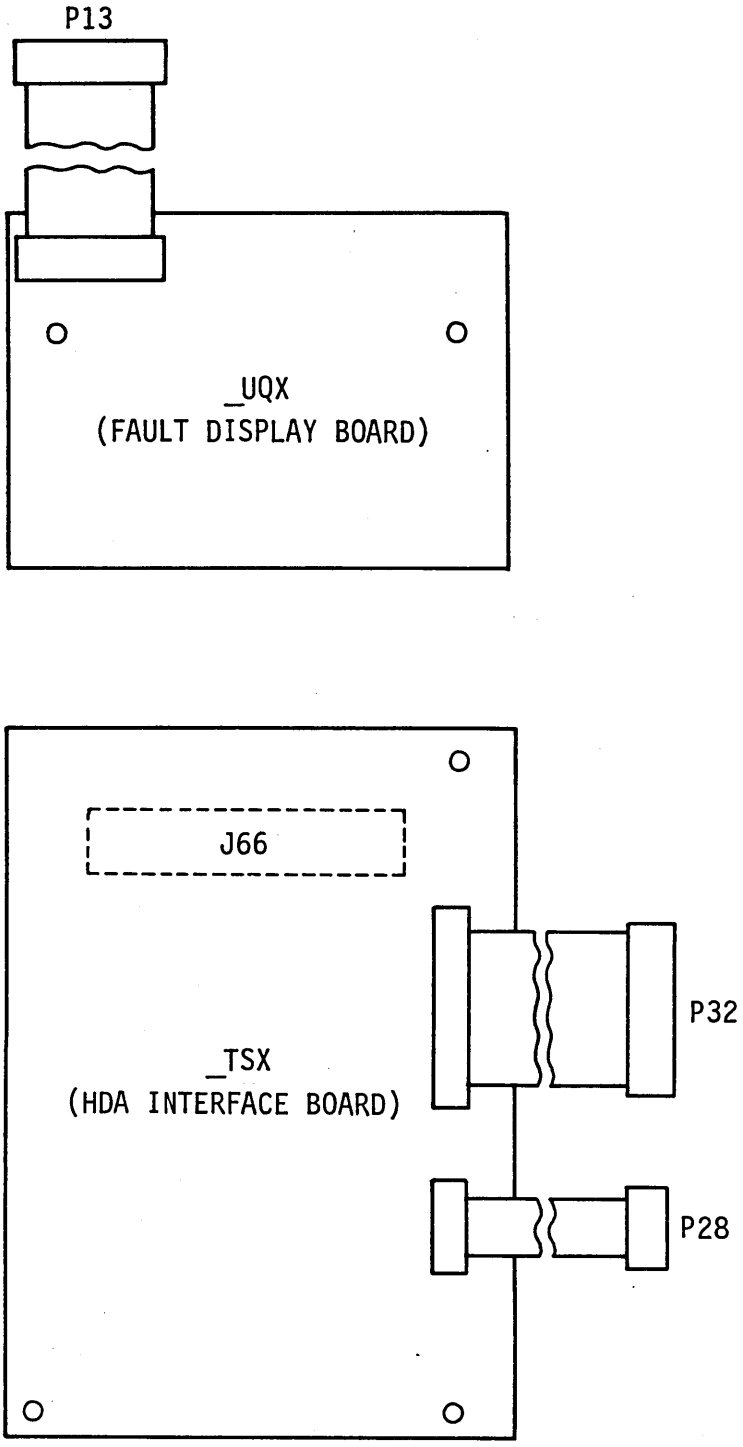


Figure 2-3 Component Locator (Sheet 7)

SECTION 3

TROUBLE ANALYSIS

CAUTION

When servicing the drive, observe all precautions listed under Electrostatic Discharge Protection in section 2 of this manual. Failure to observe these precautions can result in serious damage to electronic assemblies.

INTRODUCTION

The trouble analysis section contains information on isolating and correcting problems causing improper drive operation. Persons performing troubleshooting should be thoroughly familiar with drive operation and with all information in the general maintenance section of this manual (particularly the warnings and precautions).

Because of the many types of malfunctions that may occur, the information in this section will not provide a solution to every problem. The intention, therefore, is to solve common problems and to provide a starting point for the rest. The final recommendation in all cases is to call field support.

Trouble analysis information is divided into two parts:

- Troubleshooting procedures
- Diagnostic/Servo Status Codes

The troubleshooting procedures describe how to isolate and correct common drive problems. The procedures cover all the major areas of drive operation: power, servo, read and write. Diagnostic testing is used to determine which major drive assembly has failed. The servo status codes apply specifically to the servo system and describe the status codes presented by the MPU during servo operation. Probable causes and corrective actions are also included with the servo status code definitions.

Many of the corrective actions in this section refer to procedures given in Section 4, Electrical Checks and Section 5, Repair and Replacement. All procedures are referred to by number. For example, a reference to procedure 4201 refers to 4201 - Tribit Check in section 4. The first digit always indicates the section (4 or 5) where the procedure is found.

TROUBLESHOOTING PROCEDURES

The troubleshooting procedures describe how to isolate and correct common drive problems. Figure 3-1 is an example of a troubleshooting procedure and explains the format. The following paragraphs explain how to use the troubleshooting procedures.

Before starting a procedure, ensure that all assumptions have been satisfied. The assumptions along with other advisory information is given in the introductory paragraph to the procedure and describe conditions that must exist for the procedure to be valid.

When the assumptions are satisfied, proceed to the first step of the procedure. After performing the action or answering the question, follow the line down to the next step. For a question, follow the line beneath the appropriate Y (yes) or N (no) response. Continue until a corrective action is reached.

After taking the first recommended action, retest the unit. If the test results do not change, try recommended action 2, and so on, being sure to retest after each action. The corrective actions which are easier to perform (checking a signal or changing a circuit board, for example) are listed before the more difficult tasks such as replacing the HDA. If the corrective actions do not solve the problem, call field support.

The procedures appear in the following order:

- TSP1 - Power Check: Provides an overall check of drive power.
- TSP2 - ±5 Volt Check: Shows how to isolate problems in the ±5 volt loads.
- TSP3 - ±24 Volt Load Check: Shows how to isolate problems in the ±24 volt loads.
- TSP4 - First Seek Check: Provides possible causes for the drive failing to successfully complete a first seek.

- TSP5 - Direct or RTZ Seek Check: Provides possible causes for the drive failing to successfully complete a direct or RTZ seek.

- TSP6 - Write Check: Provides information for isolating cause of write errors.

- TSP7 - Read Check: Provides information for isolating cause of read errors.

- TSP8 - Address Mark Check: Provides possible causes for read or write address mark problems.

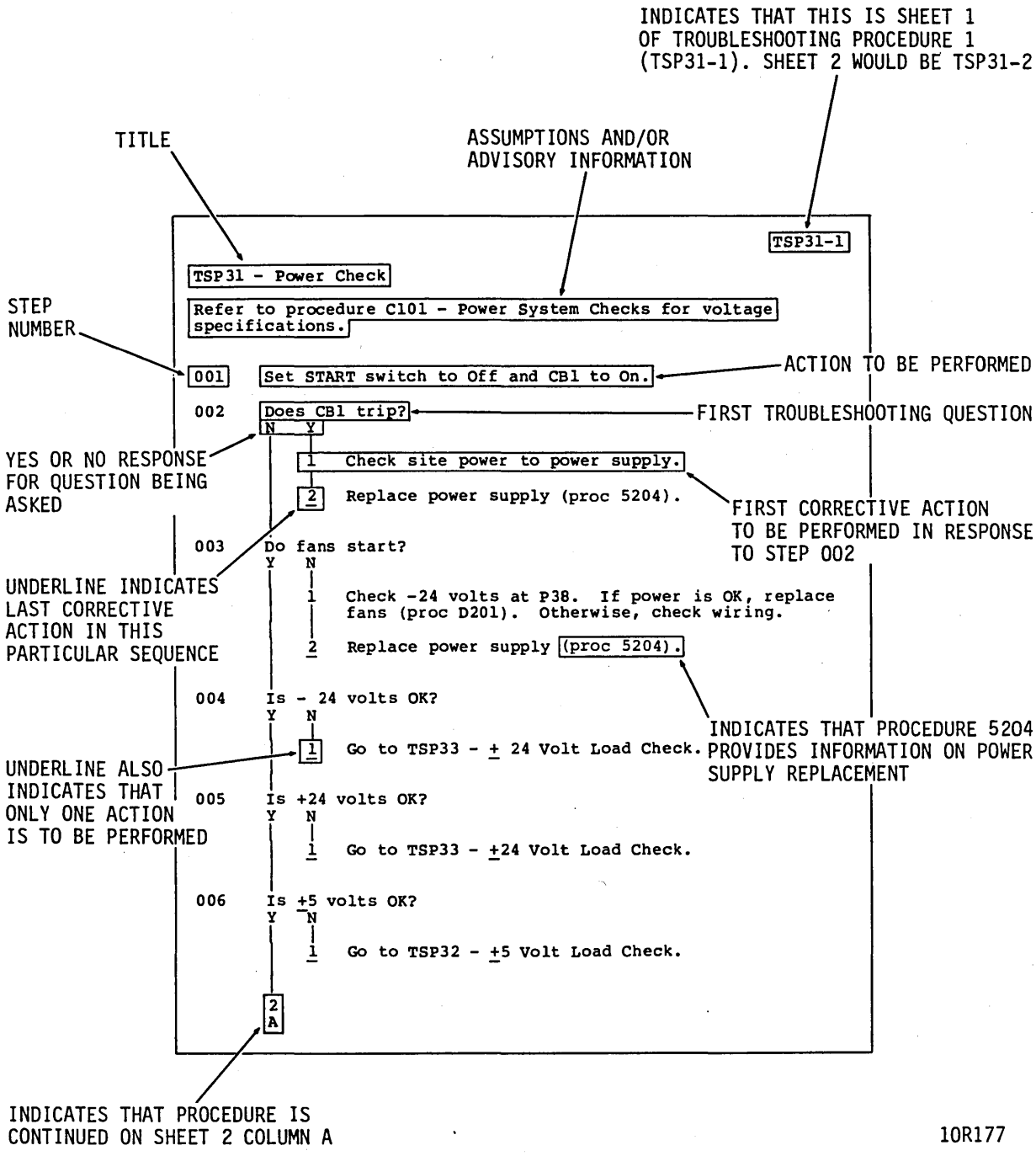
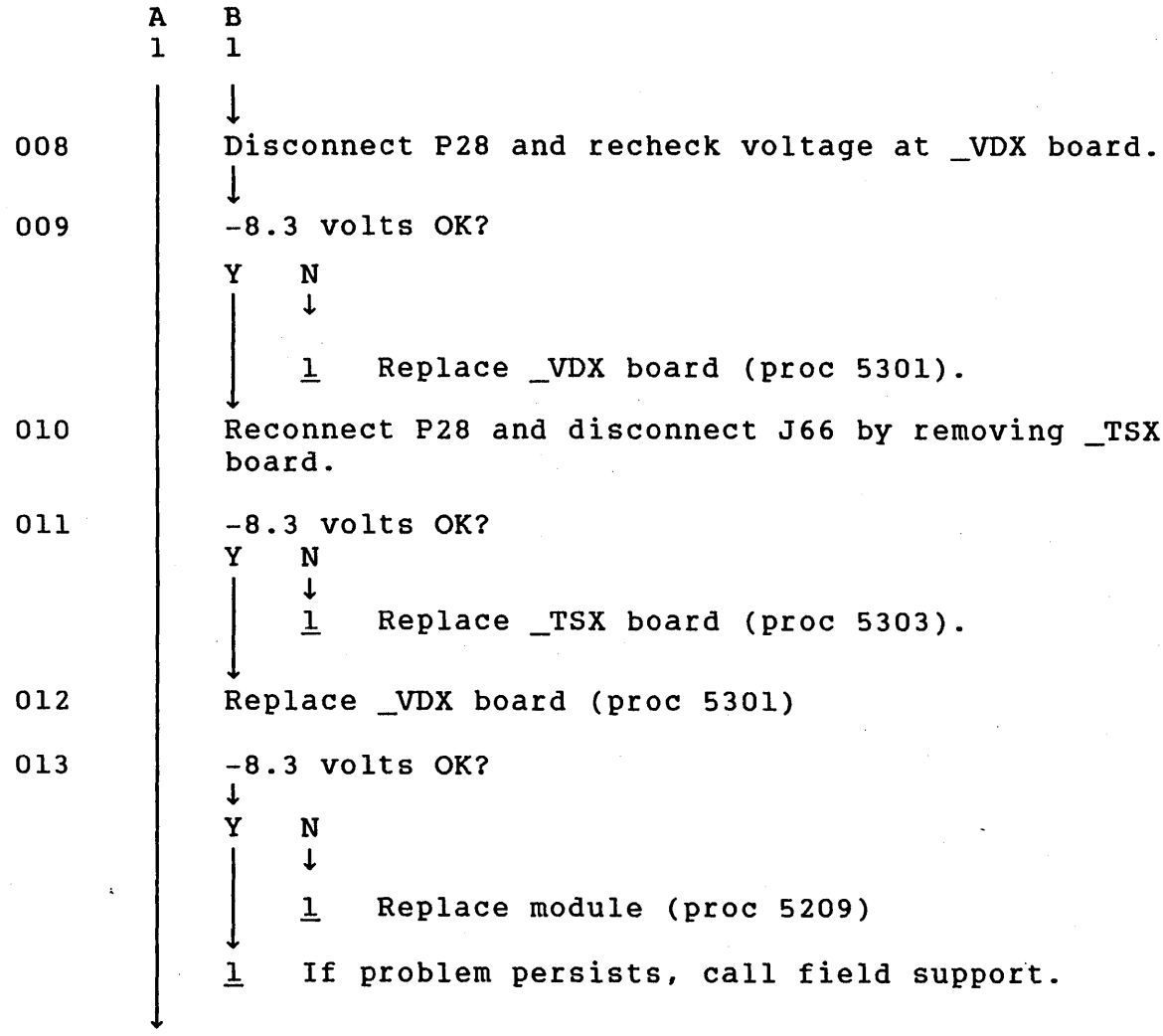


Figure 3-1. Example of Troubleshooting Procedure

TSP1 - Power Check

Refer to procedure 4101 - Power Checks for voltage specifications.

001 Set START switch to Off and CB1 to On.
↓
002 Does CB1 trip?
N Y
| ↓
| 1 Ensure power supply is set at proper voltage.
| ↓
| 2 Check site power to power supply.
| ↓
| 3 Replace power supply (proc 5207).
↓
003 Does fan start?
Y N
| ↓
| 1 Check ac voltage at J19 pins 1 and 2 of power
| | supply. If power is OK, replace fan (proc 5201).
| | Otherwise, check wiring.
| ↓
| 2 Replace power supply (proc 5207).
↓
004 Is -24 volts OK?
Y N
| ↓
| 1 Go to TSP3 - ± 24 Volt Load Check.
↓
005 Is +24 volts OK?
Y N
| ↓
| 1 Go to TSP3 - ±24 Volt Load Check.
↓
006 Are ±5 volts OK?
Y N
| ↓
| 1 Perform ±5 volt adjustment (proc 4102).
| ↓
| 2 Go to TSP2 - ±5 Volt Load Check.
↓
007 Is -8.3 volts OK?
Y N
↓ ↓
2 2
A B


A
1
B
1
008
Disconnect P28 and recheck voltage at _VDX board.
009
-8.3 volts OK?
Y
N
1
Replace _VDX board (proc 5301).
010
Reconnect P28 and disconnect J66 by removing _TSX board.
011
-8.3 volts OK?
Y
N
1
Replace _TSX board (proc 5303).
012
Replace _VDX board (proc 5301)
013
-8.3 volts OK?
Y
N
1
Replace module (proc 5209)
1
If problem persists, call field support.
014
Power check OK.

TSP2 - ±5 V Load Check

This check isolates problems with ±5 volts. Refer to procedure 4101 - Power Checks for voltage specifications.

001 Deenergize drive and check for short circuits between:
- +5 volts or -5 volts and ground.
- +5 volts and -5 volts.
- ±5 volts and ±24 volts.

↓

002 Do any short circuits exist?

N Y

↓

1 Remove loads (one at a time) to isolate short.

↓

2 Inspect wiring and boards.

003 Remove all loads, except (_VDX) from ±5 volts by disconnecting P24 (_UCX), P20 (_SYX/_TQX) and P30 (_SUX) from __TRX (mother board), P32 (_SUX to __TSX) and P13 (_UQX) and P26 (_PBX) from (_VDX) board, P28 from _TSX to _VDX, _TSX to module, then recheck voltages.

↓

004 Are ±5 volts OK?

Y N

↓

1 Check wiring and power supply.

↓

2 Replace _VDX (proc 5301).

005 Deenergize drive, add _UCX to ±5 volt load by connecting P24 to J24 _TRX (mother board), then recheck voltages.

↓

006 Is ±5 volts OK?

Y N

↓

1 Replace _UCX (proc 5304).

007 Deenergize drive, add _SYX/_TQX to ±5 volt load by connecting P20 to J20 _TRX (mother board), then recheck voltages.

↓

2

A

A
1
|
↓

008 Is ±5 volts OK?
Y N
| ↓
| 1 Replace _SYX/_TQX (proc 5305).
↓

009 Deenergize drive, add _SUX to ±5 volt load by connecting P30 to J30 _TRX (mother board), then recheck voltages.
↓

010 Are ±5 volts OK?
Y N
| ↓
| 1 Replace _SUX (proc 5302).
↓

011 Deenergize drive, add _TSX to ±5 volt load by connecting P32 to J32 (_SUX), then recheck voltages.
↓

012 Are ±5 volts OK?
Y N
| ↓
| 1 Replace _TSX (proc 5306).
↓

013 Deenergize drive, add _UQX to ±5 volt load by connecting P13 to J13 (_VDX), then recheck voltages.
↓

014 Are ±5 volts OK?
Y N
| ↓
| 1 Replace _UQX (proc 5203).
↓

015 Deenergize drive, add _PBX to ±5 volt load by connecting P26 to J26 (_VDX), then recheck voltages.
↓

016 Are ±5 volts OK?
Y N
| ↓
| 1 Replace _PBX (proc 5202).
| ↓
| 2 Replace power supply (proc 5207).
↓

1 If problem persists, call field support.

TSP3 - ±24 Volt Load Check

This check isolates problems with ±24 volts. Refer to procedure 4101 - Power Checks for voltage specifications.

001 Deenergize drive and check for short circuits between:
- +24 volts and -24 volts and ground.
- +24 volts and -24 volts.
- ±24 volts and ±5 volts.

↓

002 Do any short circuits exist?

N | Y

↓

1 Remove loads (one at a time) to isolate short.

↓

2 Inspect wiring and boards.

003 Remove all loads, except (_VDX) and (_SYX/_TQX) from ±24 volts by disconnecting P24 (__UCX) from __TRX (mother board), then recheck voltages.

↓

004 Are ±24 volts OK?

Y | N

↓

1 Check wiring and power supply.

↓

2 Replace _VDX (proc 5301).

005 Deenergize drive, add _UCX to ±24 volt load by connecting P24 to J24 _TRX (mother board), then recheck voltages.

↓

006 Is ±24 volts OK?

Y | N

↓

1 Replace _UCX (proc 5304).

↓

1 Replace power supply (proc 5207). If problem persists call field support.

001 Initiate first seek as follows:
- a. Set LOCAL/REMOTE switch to local.
- b. Set CB1 & START switch to ON.

002 Does READY indicator light?

N → 003 Drive has successfully completed first seek.

Y → 004 Do all fault LEDs light?

N → 005 Are ±5 volts OK?

N → 1 Check ±5 volts. See TSP2.

Y → 1 Replace _VDX (proc 5301).

Y → 006 Is operator panel fault light on?

N → 1 Check P43 (_UCX) to voice coil.

2 Replace _UCX (proc 5304).

Y → 007 Does Volt Fault LED light?

N → 1 Check LED's on fault status display board (located behind front panel insert) for error code and table 3-2 for error code definition.

2 Check all power harness connections.

Y → 008 If problem persists, call field support.

TSP5 - Direct or RTZ Seek Check

This test assumes that the following conditions exist: (1) drive is operating under control of TB2A3A and (2) first seek was successfully completed.

001 Does FAULT indicator light or is Seek Error active?
Y N

002 Direct or RTZ seek is OK.

003 Does Volt Fault LED light?
N Y

1 Power problem. See TSP 1.

004 Does On Cylinder go active?
Y N

005 Does error always occur at or near the same cylinder?
Y N

1 Check _TSX to J28 (_VDX) and P43 to _UCX board.

2 Replace _UCX board (proc 5304).

3 Replace _VDX (5301).

4 Replace module (proc 5209).

1 Replace module (proc 5209).

2
A

A
1
↓

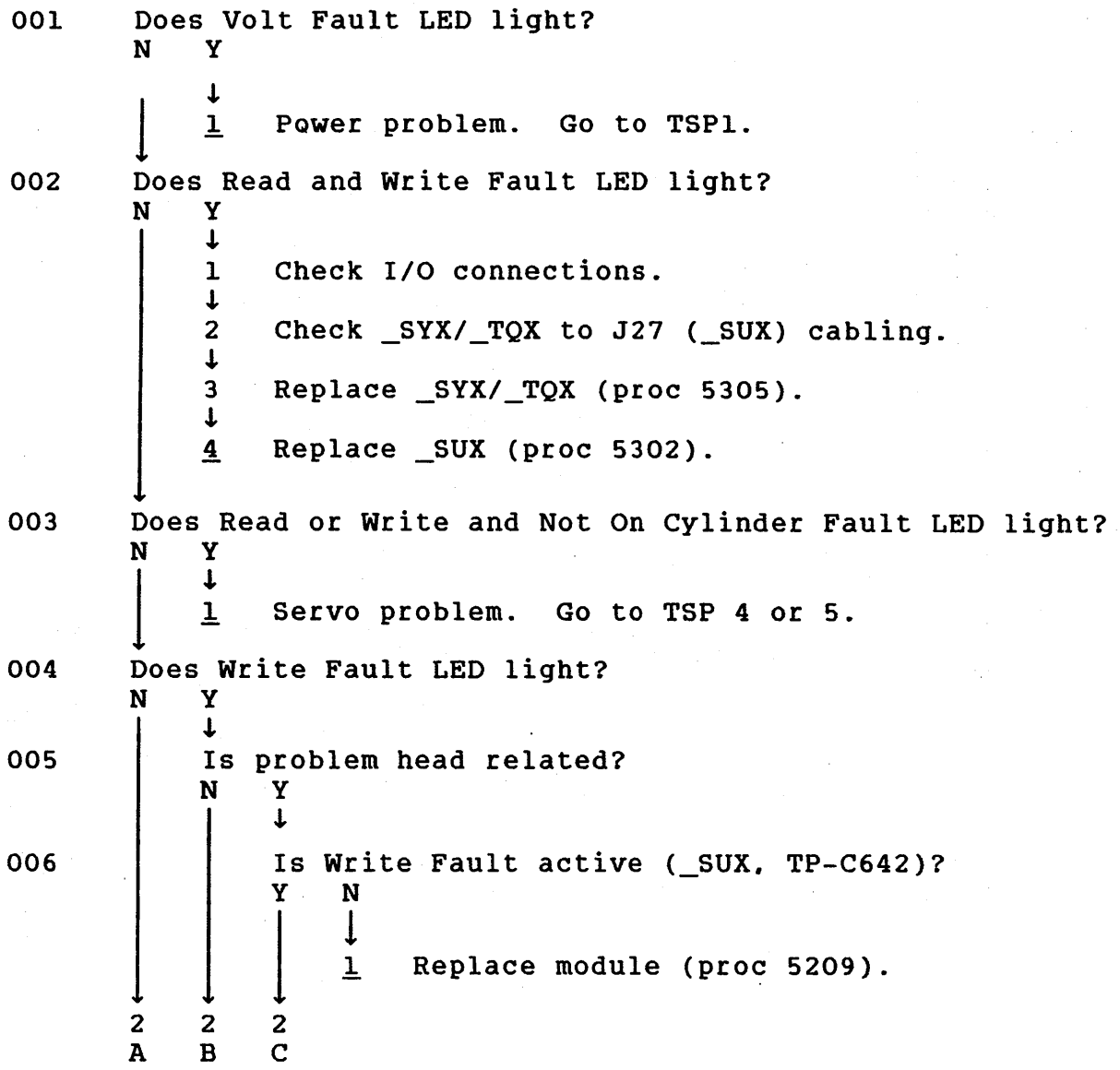
006 Does error always occur when seeking to or near the same cylinder?

N Y

```
|   1  Replace _SYX/_TQX (proc 5305).
|   ↓
|   2  Replace _VDX (proc 5301).
|   ↓
|   3  Replace module (proc 5209).
↓
1  Check cabling connection from _TSX to J28 (_VDX)
↓
2  Replace _SYX/_TQX (proc 5305).
↓
3  Replace _VDX (proc 5301).
↓
4  Replace module (proc 5209).
```

TSP6 - Write Check

This check assumes that the drive is performing write or write format operations under control of the TB2A3A.



```
A   B   C
1   1   1
|   |   ↓
|   |   1   Check head/cylinder address bits on _SUX.
|   |   |   If bits are OK, replace module (5209).
|   |   |   Otherwise, proceed to next action.
|   |   ↓
|   |   2   Check I/O connections.
|   |   ↓
|   |   3   Check P27 connector at _SUX.
|   |   ↓
|   |   4   Check P32 to _TSX cabling.
|   |   ↓
|   |   5   Check _TSX to module connection.
|   |   ↓
|   |   6   Replace _SYX/_TQX (proc 5305).
|   |   ↓
|   |   7   Replace _SUX (proc 5302).
|   |   ↓
|   |   8   Replace _TSX (proc 5303).
|   |   ↓
|   |   9   Replace module (proc 5209).
|   ↓
007 |   Is Write Fault active (_SUX, TP-C642)?
|   Y   N
|   |   ↓
|   |   1   Check for data at output of _SUX.  If data
|   |   |   is absent, perform 4303 - Write Data Check.
|   |   ↓
|   |   2   Check head/cylinder address bits on _SUX.
|   |       If bits are OK, replace module (proc 5209).
|   ↓
|   1   Perform procedure 4303 - Write Data Check.
|   ↓
|   2   Replace _SUX (proc 5302).
|   ↓
|   3   Replace _VDX (proc 5301).
|   ↓
|   4   Replace _TSX (proc 5306).
|   ↓
|   5   Replace module (proc 5209).
↓
3
D
```

```
        D
        2
        ↓
008     Perform procedure 4303 - Write Data Check.
        ↓
009     Is the 2.41 (_SUX) MHz clock OK?
        Y   N
        |   ↓
        |   1   Servo problem.  See TSP 4 or 5.
        ↓
010     Is the 2F clock OK?
        Y   N
        |   ↓
        |   1   Replace _SUX (proc 5302).
        ↓
011     Is the 14.5 MHz clock OK?
        Y   N
        |   ↓
        |   1   Replace _SUX (proc 5302).
        |   ↓
        |   2   Replace _SYX/_TQX (proc 5305).
        ↓
012     Are Write Gate, Write Clock, and Write Data present?
        Y   N
        |   ↓
        |   1   Check I/O connections.
        |   ↓
        |   2   Check _SYX/_TQX to J27 (_SUX) cabling.
        |   ↓
        |   3   Replace _SYX/_TQX (proc 5305).
        |   ↓
        |   4   Replace _SUX (proc 5302).
        ↓
013     Is Write Data Compensated present?
        Y   N
        |   ↓
        |   1   Replace _SUX (proc 5302).
        ↓
014     Is Read/Write Data to preamplifier present?
        N   Y
        |   ↓
015     |   Write Data Check OK. If problems persist, call field
        ↓   support.
        4
        D
```

D
3
↓

016 Is Write Enable OK?

Y | N

| ↓
| 1 Replace _VDX (proc 5301).
| ↓
| 2 Replace _SUX (proc 5302).
↓

1 Replace _SUX (proc 5302).
↓
2 Replace module (proc 5209).

TSP7 - Read Check

This check assumes that the drive is performing read operations under control of the TB2A3A.

001 Does Volt Fault LED light?
N Y

002 1 Power problem. See TSP1.

003 Does Read and Write Fault LED light?
N Y
1 Check I/O connections.
2 Check _SYX/_TQX to J27 (_SUX) cabling.
3 Replace _SYX/_TQX (proc 5305).
4 Replace _SUX (proc 5302).

004 Does Read or Write and Not On Cylinder Fault LED light?
N Y
1 Servo problem. See TSP 4 or 5.

005 Is address mark detected?
Y N
1 Perform procedure 4403 - Read AM Check and go to TSP8.

006 Is there a data error?
Y N

007 Read operation is OK.

2
A

```
        A
        1
        ↓
008     Are errors head related?
        N   Y
        |   ↓
        |   1   Check head/cylinder address bits on _SUX.
        |   |   If bits are bad, suspect:
        |   |   a.  cabling problem.
        |   ↓   b.  _SYX/_TQX, _VDX, _TSX or _SUX.
        |   2   Replace module (proc 5209).
        ↓
009     Perform procedure 4402 - Read Data Check.
        ↓
010     Is Read Gate active?
        Y   N
        |   ↓
        |   1   Check I/O connections.
        |   ↓
        |   2   Check _SYX/_TQX to J27 (_SUX) cabling.
        |   ↓
        |   3   Replace _SYX/_TQX (proc 5305).
        |   ↓
        |   4   Replace _SUX (proc 5302).
        |   ↓
        |   5   Replace _TSX (proc 5303).
        ↓
011     Is 2.41 (_SUX) MHz Clock present?
        |
        Y   N
        |   ↓
        |   1   Servo problem.  See TSP 4 or 5.
        ↓
012     Is Read Clock and 2F Read Oscillator OK?
        Y   N
        |   ↓
        |   1   Replace _SUX (proc 5302).
        ↓
        3
        B
```

```
        B
        2
        ↓
013     Is head and preamplifier output present?
        Y   N
        |   ↓
        |   1   Check J32 (_SUX) to _TSX cabling.
        |   ↓
        |   2   Replace _SUX (proc 5302).
        |   ↓
        |   3   Replace _TSX (proc 5303).
        |   ↓
        |   4   Replace module (proc 5209).
        ↓
014     Is Latched or NRZ Read Data present?
        Y   N
        |   ↓
        |   1   Replace _SUX (proc 5302).
        ↓
015     Is Read Gate and Lock to Data timing present?
        Y   N
        |   ↓
        |   1   Replace _SUX (proc 5302).
        ↓
        1   Replace _SUX (proc 5302).
        ↓
        2   Replace _VDX (proc 5303).
        ↓
        3   Replace module (proc 5209).
```

TSP8 - Address Mark Check

The following check assumes that the drive is under control of the TB2A3A.

001 Perform procedure 4403 - Read AM Check.

002 Is AM Enable active?

Y: ↓

N: ↓

1 Check I/O connections.

↓

2 Check _SYX/_TQX to J27 (_SUX) cabling.

↓

3 Replace _SUX (proc 5302).

003 Is AM Found active?

Y: ↓

N: ↓

1 Replace _SUX (proc 5302).

↓

2 Replace _SYX/_TQX (proc 5305).

004 Is AM proper length?

Y: ↓

N: ↓

005 Perform procedure 4304 - Write AM Check.

↓

006 Is AM Enable active?

Y: ↓

N: ↓

1 Check I/O connections.

↓

2 Check _SYX/_TQX to J27 (_SUX) cabling.

↓

3 Replace _SYX/_TQX (proc 5305).

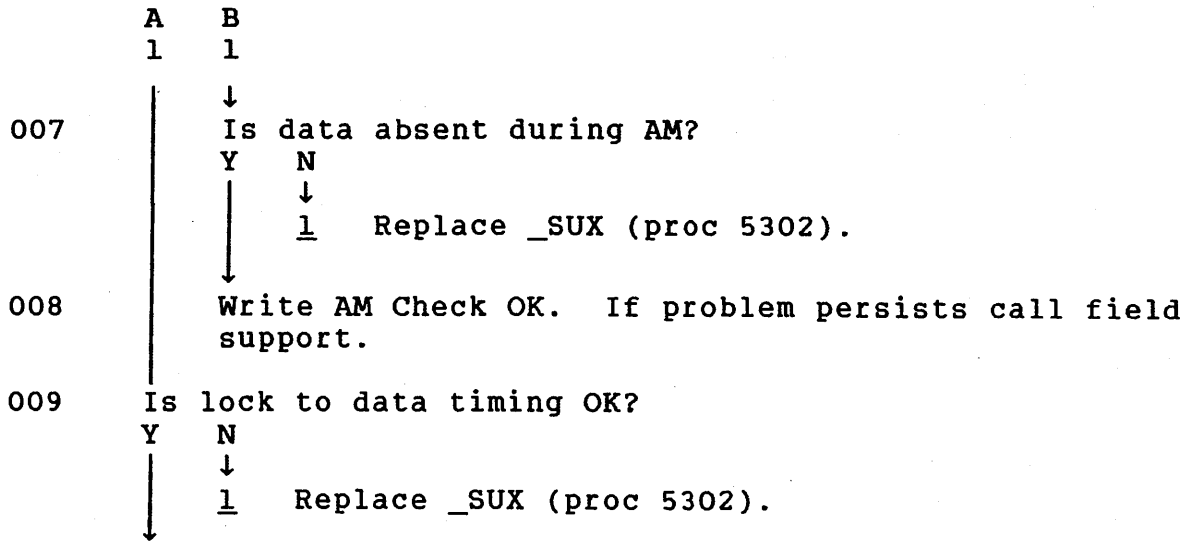
|

4 Replace _SUX (5302).

↓ ↓

2 2

A B


A
1
B
1
007
Is data absent during AM?
Y
N
1
Replace _SUX (proc 5302).
008
Write AM Check OK. If problem persists call field support.
009
Is lock to data timing OK?
Y
N
1
Replace _SUX (proc 5302).
010
Read AM Check OK. If problem persists, call field support.

DIAGNOSTIC/SERVO STATUS CODES

GENERAL

The diagnostic and servo status codes are two digit hexadecimal codes, generated by the MPU, that indicate either the diagnostic tests being initiated or operational status of the drive servo system. The following discussions explain how to perform diagnostic tests and defines various servo status codes.

DIAGNOSTIC TESTING

To be supplied.

SERVO STATUS CODE DEFINITIONS

Whenever the drive is in a power on condition (dc power active), the MPU is periodically checking the operation of the servo status system and generating appropriate status codes. The codes can be visually monitored by removing the drive front panel insert. Table 3-1 is a summary of all the status codes and table 3-2 provides definitions of each code. Each status code definition is divided into three parts:

1. Description: Basic definition of what type of problem the code indicates, during what operations the code appears, what additional error indications are present with the code, and how to initiate a retry or recovery from the error.

2. Probable Causes: What general areas could cause the problem. The purpose here is to provide a general idea of what functional areas could be causing the problem.

3. Actions: What specific things to check to correct the problem. Perform each action and retest the drive before proceeding to the next action. If all actions have been performed and the problem persists, call field support.

When interpreting the status codes it is important to know that not all codes appearing on the display indicate errors. Some indicate that the operation is still in progress, others that the operation has been successfully completed.

When an operation is in progress, the status is continually changing. Most codes flash on and off very rapidly and are not recognizable. Others will remain for several seconds.

If an error occurs, the status indicates the type of error and where in the sequence the error occurred. The error code will remain active until the proper action is taken to reset it (depends on nature of error).

TABLE 3-1. STATUS CODE SUMMARY

Status Code	Description
	Normal On Cylinder
00	Normal On Cylinder
	Normal Motor Stop
01	Retracting Heads To Landing Zone
02	Stopping Motor
03	Motor Stopped OK
	Normal Motor Start
07	Motor Start In Progress (No Jog)
08	Motor Start In Progress (Including Jog)
09	Speed OK Too Soon
0A	Too Long To Get Up To Speed (Retry)
0C	Too Many Startup Failures (No Retry)
0E	Motor Speed Too High
0F	Motor Speed Too Low
10	Speed Loss Recovery With Seek Error
	Motor Stop During Recovery From Speed Drop
11	Unloading Heads
12	Stopping Motor

Table Continued on Next Page

TABLE 3-1. STATUS CODE SUMMARY (Contd)

Status Code	Description
	Motor Start During Recovery From Speed Drop
18	Motor Start In Progress (Including Jog)
19	Speed OK Too Soon
1A	Too Long To Get Up To Speed (Retry)
1C	Too Many Startup Failures (No Retry)
1E	Motor Speed Too High
1F	Motor Speed Too Low
	Normal Load
21	Heads Loaded Before Load Begins
22	Fault After Power Amplifier Driver Enabled
25	Demodulator Active Timeout
26	Cylinder Pulse Timeout
27	Fault After Load Complete
28	Code 22 And Too Many Retries
2B	Code 25 And Too Many Retries
2C	Code 26 And Too Many Retries
2D	Code 27 And Too Many Retries

Table Continued on Next Page

TABLE 3-1. STATUS CODE SUMMARY (Contd)

Status Code	Description
	Normal RTZ
30	Can't Move In From Outer Guard Band
31	Lost Demodulator Active Before Turnaround
33	Timeout During RTZ
34	Backup Into Outer Guard Band
35	Turnaround
36	Out Of Guard Band Too Soon
37	Can't Find Cylinder Pulse At Track -1
38	Find Fine Enable
39	Settle In On Track 0
	Normal Guard Bands
40	Inner Guard Band Detected During Normal Seek
41	Inner Guard Band Detected During On Cylinder Routine
42	Inner Guard Band Detected While On Cylinder
43	Outer Guard Band Detected During Normal Seek
44	Outer Guard Band Detected During On Cylinder Routine
45	Outer Guard Band Detected While On Cylinder

Table Continued on Next Page

TABLE 3-1. STATUS CODE SUMMARY (Contd)

Status Code	Description
	Normal Seek Timeout
46	Seek Timeout
	(Normal) Can't Stop On Track During On Cylinder Routine
47	Too Long To Get On Cylinder Sense
48	Demodulator Active Lost During On Cylinder Routine
49	Too Many Cylinder Pulses During Settle In
4A	Too Many On Cylinder Dropouts
	Normal On Track
4B	Off Cylinder
4C	Lost Demodulator Active While On Cylinder
4E	Voltage Fault While On Cylinder
	Reset Dummy RTZ Mode Canceled
50	Recovery From Low Vcc Reset
51	Recovery From MPU Hang Reset
52	Recovered From Low Vcc Reset And Subsequent Speed Loss
53	Recovered From MPU Hang And Subsequent Speed Loss
58	Non Maskable Interrupt

Table Continued on Next Page

TABLE 3-1. STATUS CODE SUMMARY (Contd)

Status Code	Description
	Reset Dummy RTZ Mode Canceled (Contd)
59	Software Interrupt
5F	PIA Test Failure
80	Fault Before Seek Begins
90	Recovered From Speed Loss
	Servo Test Diagnostics
60	Servo Test Failure During RTZ
61	Servo Test Failure During Recalibrate
62	Servo Test Failure During 1 Track Seek
63	Servo Test Failure During Maximum Length Seek
64	Failed Recalibrate Test
65	1 Track Seek Too Short
66	1 Track Seek Too Long
67	Maximum Length Seek Too Long
68	Maximum Length Seek Too Short
69	Bad Preseek Status
70	Self Test Complete
71	Fan On
72	Execute Switch Does Not Release

Table Continued on Next Page

TABLE 3-1. STATUS CODE SUMMARY (Contd)

Status Code	Description
	Load And Fault Detected Before Seek Error Was Set
A1	Heads Loaded Before Load Begins
A2	Fault After Power Amplifier Driver Enabled
A5	Demodulator Active Too Late
A6	Cylinder Pulse Timeout
A7	Fault After Load Complete
A8	Code 22 And Too Many Retries
AB	Code 25 And Too Many Retries
AC	Code 26 And Too Many Retries
AD	Code 27 And Too Many Retries
	RTZ And Fault Detected Before Seek Error Was Set
B0	Can't Move In From Outer Guard Band
B1	Lost Demodulator Active Before Turnaround
B3	Timeout During RTZ
B4	Backup Into Outer Guard Band
B5	Turnaround
B6	Out Of Guard Band Too Soon
B7	Can't Find Cylinder Pulse At Track -1
B8	Find Fine Enable
B9	Settle In On Track 0

Table Continued on Next Page

TABLE 3-1. STATUS CODE SUMMARY (Contd)

Status Code	Description
	Guard Bands And Fault Detected Before Seek Error Was Set
C0	Inner Guard Band Detected During Normal Seek
C1	Inner Guard Band Detected During On Cylinder Routine
C2	Inner Guard Band Detected While On Cylinder
C3	Outer Guard Band Detected During Normal Seek
C4	Outer Guard Band Detected During On Cylinder Routine
C5	Outer Guard Band Detected While On Cylinder
	Seek Timeout And Fault Detected Before Seek Error Was Set
C6	Seek Timeout
	Can't Stop On Track During On Cylinder Routine And Fault Detected Before Seek Error Was Set
C7	Too Long To Get On Cylinder Sense
C8	Demodulator Active Lost During On Cylinder Routine
C9	Too Many Cylinder Pulses During Settle In
CA	Too Many On Cylinder Dropouts

Table Continued on Next Page

TABLE 3-1. STATUS CODE SUMMARY (Contd)

Status Code	Description
	On Track And Fault Detected Before Seek Error Was Set
CB	Off Cylinder
CC	Lost Demodulator Active While On Cylinder
CE	Voltage Fault While On Cylinder
	Reset Dummy RTZ Mode Active
D0	Recovery From Low Vcc Reset
D1	Recovery From MPU Hang Reset
	MPU Power On Test
FF	MPU Failed Power On Test

TABLE 3-2. STATUS CODE DEFINITIONS

Code	Description
00	Title: Normal On Cylinder DESCRIPTION: The MPU sets code 00 following a successful seek. This status indicates normal operation and lasts until the MPU receives a new seek interrupt or retracts the heads.
01	Title: Retracting Heads To Landing Zone DESCRIPTION: The MPU sets code 01 while it is retracting the heads. This status lasts approximately 0.2 second under normal conditions. If the heads retract, the motor stop sequence begins and the status changes to 02. If the MPU does not detect a demodulator inactive condition, the status remains at 01 and the motor continues to run. PROBABLE CAUSES: Drive continues to detect Demodulator Active pulses due to noise, control circuit failure or power amp failure. ACTIONS 1. Replace _VDX board (proc 5301). 2. Replace _UCX board (proc 5304). 3. Replace module (proc 5209).
02	Title: Stopping Motor DESCRIPTION: The MPU sets this status during the braking period. After MPU timeout (normally 30 seconds) the status changes to 03. PROBABLE CAUSES: N.A. ACTIONS: N.A.
Table Continued on Next Page	

TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
03	Title: Motor Stopped OK DESCRIPTION: The MPU sets code 02 when it detects that the motor is stopped. This code will be displayed following a normal stop sequence. Code will remain at 03 until microprocessor sees START switch turned on and sequence hold or Local from I/O board. PROBABLE CAUSES: N.A. ACTIONS: N.A.
07	Title: Motor Start In Progress (No Jog) DESCRIPTION: Status 07 is displayed, if a voltage fault is present at beginning of start sequence. PROBABLE CAUSES: Power supply defective or voltage out of adjustment. ACTIONS 1. Check for loose cables at P15 and P40. 2. Perform power checks (proc 4101). 3. Perform voltage adjustment (proc 4102).
08	Title: Motor Start In Progress (Including Jog) DESCRIPTION: Before starting the motor, the MPU causes the heads to move backwards, in jog. Code 08 is displayed until motor reaches full speed and speed OK is set by motor control circuit.

Table Continued on Next Page

TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
	PROBABLE CAUSES: N.A. ACTIONS: N.A.
09	Title: Speed OK Too Soon DESCRIPTION: Indicates that, during the power on sequence, it took less than 3 seconds for the motor to get up to speed. This condition stops the power on sequence. PROBABLE CAUSES: Faulty speed detection circuits. ACTIONS 1. Replace _UCX board (proc 5304). 2. Replace _VDX board (proc 5301).
0A	Title: Too Long To Get Up To Speed (Retry) DESCRIPTION: 0A is displayed during the stop routine if motor did not come up to speed within 25 seconds of starting. Display changes back to 08 during the start routine. If after three tries the motor does not come up to speed, the motor stops and display changes to 0C. PROBABLE CAUSES: See code 0C. ACTIONS: See code 0C

Table Continued on Next Page

TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
OC	Title: Too Many Startup Failures (No Retry) DESCRIPTION: Indicates that the drive has failed three times to bring the motor up to speed (see code OA). Setting START Switch to Off and back to On causes three more attempts. PROBABLE CAUSES: Power supply, motor control circuits, or motor. ACTIONS 1. Check J40 to J15 and J60 to motor wiring. 2. Check +24 volts from power supply. 3. Ensure brake is not energized constantly. If so replace brake (proc 5205). 4. Replace _UCX board (proc 5304). 5. Replace drive motor (proc 5206).
OE OF	Title: Motor Speed Too High Title: Motor Speed Too Low DESCRIPTION: Indicates that the motor speed is too high (OE) or too low (OF). The MPU performs this check after it receives the Speed OK from the _UCX board. When this condition exists, the drive keeps the motor running while continuing, indefinitely, to check motor speed. The heads do not load.
Table Continued on Next Page	

TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
	PROBABLE CAUSES: Problem with motor speed detection circuits. ACTIONS 1. Replace _UCX board (proc 5304). 2. Replace drive motor (proc 5206).
10	Title: Speed Loss Recovery With Seek Error DESCRIPTION: Indicates that drive has recovered from a speed loss and that seek error occurred during the recovery sequence. The heads are floating and Seek Error is active. On Cylinder and Ready signals will go active when the drive receives an RTZ command. PROBABLE CAUSES: Motor failure, motor cable or connector, motor speed detection circuitry, or power supply. ACTIONS If more failures occur: 1. Replace power supply (proc 5207). 2. Replace drive motor (proc 5206). 3. Replace _UCX board (proc 5304).
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TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
11 thru 1F	Title: Motor Start During Recovery From Speed Drop. DESCRIPTION: Same as codes 01 through 0F but occur during recovery from a loss of speed. The codes covered in this discussion are listed below with the corresponding code (without speed drop) given in parentheses. 11 (01) 12 (02) 18 (08) 19 (09) 1A (0A) 1C (0C) 1E (0E) 1F (0F) PROBABLE CAUSES: See codes 01 through 0F. ACTIONS: See Codes 01 through 0F.
21	Title: Heads Loaded Before Load Begins DESCRIPTION: Indicates a heads loaded condition before the heads moved forward from the retracted position. This error is detected during a load sequence. When the drive displays code 21, the following error indications also appear. • First Seek LED lights (first seek only). • FAULT indicator lights and Fault line goes active (first seek only). • Seek Error and Seek End lines go active (except during first seek). • Motor continues to run. If the error occurred during a first seek, pressing the Fault Clear switch clears the fault and initiates another load. If it occurred during an RTZ error recovery attempt, commanding another RTZ clears the seek error and initiates another load.
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TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
	ACTIONS 1. Replace _VDX board (proc 5301).
22	Title: Fault After Power Amplifier Driver Enabled DESCRIPTION: Indicates that the drive detected a fault condition after the power amplifier was enabled. The purpose of a check at this time is to detect a voltage fault before enabling current pulses to move the heads forward. When the drive displays code 22, the following error indications also appear. • First Seek LED lights (first seek only). • FAULT indicator lights and Fault line goes active. • Seek Error and Seek End lines go active (except during first seek). • Motor continues to run. If the error occurred during a first seek, pressing the Fault Clear switch clears the fault and initiates another load. If it occurred during an RTZ error recovery attempt, a controller Fault Clear followed by another RTZ clears the seek error and initiates another load. After five unsuccessful RTZ error recovery attempts, the drive displays code 28 and the Fault Clear switch must be pressed to continue. PROBABLE CAUSES: Voltage fault as a result of enabling power amplifier inputs. Extraneous fault, such as Read and Write, caused by I/O problem.
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TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
	ACTIONS Check LEDs for cause of fault condition. 1. If voltage fault exists: a. Check ±24 volts (proc 4101). If voltages are abnormal, go to ±24 Volt Load Check (TSP3). b. Replace _UCX board (proc 5304). 2. If a fault other than voltage exists: a. Check I/O cabling. b. Replace _UCX board (proc 5304).
25	Title: Demodulator Active Timeout DESCRIPTION: Indicates that, during a load sequence, Demodulator Active did not go active within 200 ms after the heads started moving forward. When the drive displays code 25, the following error indications also appear. • First Seek LED lights (first seek only). • FAULT indicator lights and Fault line goes active (first seek only). • Seek Error and Seek End lines go active (except during first seek). • Motor continues to run. If the error occurred during a first seek, pressing the Fault Clear switch clears the fault and initiates another load. If it occurred during an RTZ error recov-

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TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
	ery attempt, commanding another RTZ clears the seek error and initiates another load. After five unsuccessful RTZ error recovery attempts, the drive displays code 29 and the Fault Clear switch must be pressed to continue. PROBABLE CAUSES: Bad tribit detection circuit or bad servo disk. ACTIONS 1. Check cabling from _TSX board at J28 on _VDX board. 2. Replace _TSX board (proc 5303). 3. Replace _VDX board (proc 5301). 4. Replace module (proc 5209).
26	Title: Cylinder Pulse Timeout DESCRIPTION: Indicates that, during a load sequence, the MPU did not detect 5 cylinder pulses within approximately 350 milliseconds after Demodulator Active went active. When the drive displays code 26, the following error indications also appear. • First Seek LED lights (first seek only). • FAULT indicator lights and Fault line goes active (first seek only). • Seek Error and Seek End lines go active (except during first seek). • Motor continues to run.
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TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
	If the error occurred during a first seek, pressing the Fault Clear switch clears the fault and initiates another load. If it occurred during an RTZ error recovery attempt, commanding another RTZ clears the seek error and initiates another load. After five unsuccessful RTZ error recovery attempts, the drive displays code 2C and the Fault Clear switch must be pressed to continue. PROBABLE CAUSES: Demodulator failure, bad servo disk or cylinder pulse detection circuits. ACTIONS 1. Check cabling from _TSX board at J28 on _VDX board. 2. Replace _TSX board (proc 5303). 3. Replace _VDX board (proc 5301). 4. Replace module (proc 5209).
27	Title: Fault After Load Complete DESCRIPTION: Indicates that, during a load sequence, the MPU detected a fault just prior to the time that the heads turn around and move back into the guardband. When the drive displays code 27, the following error indications also appear. • First Seek LED lights (first seek only). • FAULT indicator lights and Fault line goes active (first seek only). • Seek Error and Seek End lines go active (except during first seek). • Motor continues to run.
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TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
	If the error occurred during a first seek, pressing the Fault Clear switch clears the fault and initiates another load. If it occurred during an RTZ error recovery attempt, commanding another RTZ clears the seek error and initiates another load. After five unsuccessful RTZ error recovery attempts, the drive displays code 2D and the Fault Clear switch must be pressed to continue. PROBABLE CAUSES: Voltage fault due to defective voltage regulator, power supply, power amplifier, or voice coil. Extraneous fault, such as Read and Write, caused by I/O problem. ACTIONS Check LEDs for cause of fault condition. 1. If voltage fault exists: a. Check ±24 volts (proc 4101). If voltages are abnormal, go to (TSP3) ±24 Volt Load Check. b. Replace _UCX board (proc 5304). c. Replace _VDX board (proc 5301). d. Replace module (proc 5209). 2. If a fault other than voltage exists: a. Check I/O cabling. b. Replace _SYX/_TQX board (proc 5305).
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TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
28 thru 2D	Title: Error Conditions With Too Many Retries. DESCRIPTION: Indicates that more than five RTZ error recovery attempts were made following the associated error (codes 22 through 27). After five attempts, the MPU sets one of the codes 28 through 2D and prevents further retries. Pressing the Fault Clear switch clears the error and allows five more retries. The codes covered in this discussion are listed below with the corresponding code (without too many retries) given in parentheses. PROBABLE CAUSES: See codes 22 through 27. ACTIONS: See codes 22 through 27. 28 (22) 2B (25) 2C (26) 2D (27)
30	Title: Can't Move In From Outer Guardband DESCRIPTION: Indicates, during a load or RTZ, that heads were moving in too fast to allow a turnaround in the data zone. Attempting a turnaround could result in the heads moving completely through the data zone, resulting in loss of servo control. When the drive displays code 30, the following error indications also appear. • First Seek LED lights (first seek only). • FAULT indicator lights and Fault line goes active (first seek only). • Seek Error and Seek End lines go active (except during first seek). • Motor continues to run.

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TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
	If the error occurs during a first seek, pressing the Fault Clear switch clears the fault and initiates another load. If it occurs during an RTZ, the drive automatically performs one retry. If the retry fails it is necessary to command another RTZ to clear the seek error and initiate another attempt. PROBABLE CAUSES: Problem with velocity circuits. ACTIONS 1. Initiate RTZ, if error repeats, replace _VDX board (proc 5301).
31	Title: Lost Demodulator Active Before Turnaround DESCRIPTION: Indicates that during backup portion of RTZ, Demodulator Active went inactive. This indicates that the heads may have moved back through the outer guardband to the outer surface of the disk, without generating outer guardband pulses. When the drive displays code 31, the following error indications also appear. • First Seek LED lights (first seek only). • FAULT indicator lights and Fault line goes active (first seek only). • Seek Error and Seek End lines go active (except during first seek). • Motor continues to run.
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TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
	If the error occurs during a first seek, pressing the Fault Clear switch clears the fault and initiates another load. If it occurs during an RTZ, the drive automatically performs one retry. If the retry fails it is necessary to command another RTZ to clear the seek error and initiate another attempt. PROBABLE CAUSES: Bad servo disk, loose connection or failure that causes loss of velocity control. ACTIONS 1. Check cabling at J28 on _VDX board. 2. Replace _VDX board (proc 5301). 3. Replace module (proc 5209).
33	Title: Timeout During RTZ DESCRIPTION: Indicates that during the backup portion of a load or RTZ, too much time elapsed before the heads reached the outer guardband. When the drive displays code 33, the following error indications also appear. • First Seek LED lights (first seek only). • FAULT indicator lights and Fault line goes active (first seek only). • Seek Error and Seek End lines go active (except during first seek). • Motor continues to run.
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TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
	If the error occurs during a first seek, pressing the Fault Clear switch clears the fault and initiates another load. If it occurs during an RTZ, the drive automatically performs one retry. If the retry fails it is necessary to command another RTZ to clear the seek error and initiate another load. PROBABLE CAUSES: Failure in velocity circuits, bad power amplifier or power amplifier driver circuits. ACTIONS 1. Replace _UCX board (proc 5304). 2. Replace _VDX board (proc 5301). 3. Replace module (proc 5209).
34	Title: Backup Into Outer Guardband DESCRIPTION: Code 34 is set when the outer guardband is detected during the backup phase of a load or RTZ seek. It normally remains set only until turnaround, when the code changes to 35. If the display stays at 34, it indicates either a timeout (too long to count 2 cylinder pulses) or Demodulator Active inactive error. The following error indications appear in addition to code 34. If the error occurs during a first seek: • First Seek LED lights. • FAULT indicator lights and Fault line goes active (first seeks only). • Motor continues to run.
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TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
	If the error occurs during an RTZ: • Seek Error and Seek End lines go active. • Motor continues to run but the servo system is disabled and the heads, although loaded, float freely over the disk surfaces. If the error occurs during a first seek, pressing the Fault Clear switch clears the fault and initiates another load. If it occurs during an RTZ, commanding another RTZ clears the seek error and initiates another seek to cylinder 0. PROBABLE CAUSES: Bad tribit decoder circuit or servo disk. ACTIONS 1. Check for loose cable at J28 on _VDX board. 2. Replace _VDX board (proc 5301). 3. Replace module (proc 5209).
35	Title: Turnaround DESCRIPTION: Code 35 is set at the turnaround point following the backup phase of a load or RTZ seek. This is the point where two cylinder pulses have been counted, reverse is cleared, and forward is set. Code 35 normally remains set only until the heads move forward four tracks thus bringing the heads to track -1 (preceding cylinder 0) and changing the code to 37. If the

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TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
	display stays at 35, it indicates either a timeout (too long to count 1 cylinder pulse) or Demodulator Active inactive error. The following error indications appear in addition to code 35. If the error occurs during a first seek: • First Seek LED lights. • FAULT indicator lights and Fault line goes active (first seeks only). • Motor continues to run. If the error occurs during an RTZ: • Seek Error and Seek End lines go active. • Motor continues to run but the servo system is disabled and the heads, although loaded, float freely over the disk surfaces. If the error occurs during a first seek, pressing the Fault Clear switch clears the fault and initiates another load. If it occurs during an RTZ, commanding another RTZ clears the seek error and initiates another seek to cylinder 0. PROBABLE CAUSES: Bad tribit decoder circuit or servo disk. ACTIONS 1. Check for loose cable at J28 on _VDX board. 2. Replace _VDX board (proc 5301). 3. Replace module (proc 5209).
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TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
36	Title: Out Of Guardband Too Soon DESCRIPTION: Indicates, during a load or RTZ, that the the drive detected less than one cylinder pulse before the heads moved out of the outer guardband. When the drive displays code 36, the following error indications also appear. If the error occurs during a first seek: • First Seek LED lights. • FAULT indicator lights and Fault line goes active (first seeks only). • Motor continues to run. If the error occurs during an RTZ: • Seek Error and Seek End lines go active. • Motor continues to run but the servo system is disabled and the heads, although loaded, float freely over the disk surfaces. If the error occurs during a first seek, pressing the Fault Clear switch clears the fault and initiates another load. If it occurs during an RTZ, commanding another RTZ clears the seek error and initiates another seek to cylinder 0. PROBABLE CAUSES: Bad tribit decoder circuit, cylinder pulse detection circuit, or servo disk.

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TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
	ACTIONS 1. Check for loose cable at J28 on _VDX board. 2. Replace _VDX board (proc 5301). 3. Replace module (proc 5209).
37	Title: Can't Find Cylinder Pulse At Track -1 DESCRIPTION: Indicates that, during a load or RTZ, either Demodulator Active went inactive or too much time elapsed while the drive was looking for track -1 (track preceding cylinder 0). When the drive displays code 37, the following error indications also appear. If the error occurs during a first seek: • First Seek LED lights. • FAULT indicator lights and Fault line goes active (first seeks only). • Motor continues to run. If the error occurs during an RTZ: • Seek Error and Seek End lines go active. • Motor continues to run. • The servo system is disabled and the heads, although loaded, float freely over the disk surfaces.

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TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
	If the error occurs during a first seek, pressing the Fault Clear switch clears the fault and initiates another load. If it occurs during an RTZ, commanding another RTZ clears the seek error and initiates another seek to cylinder 0. PROBABLE CAUSES: Bad tribit decoder circuit, cylinder pulse detection circuit, or servo disk. ACTIONS 1. Check for loose cable at J28 on _VDX board. 2. Replace _VDX board (proc 5301). 3. Replace module (proc 5209).
38	Title: Find Fine Enable DESCRIPTION: Indicates that, during a load or RTZ, either Demodulator Active went inactive or too much time elapsed while the drive was waiting for Fine Enable to go active. When the drive displays code 38, the following error indications also appear. If the error occurs during a first seek: • First Seek LED lights. • FAULT indicator lights and Fault line goes active (first seeks only). • Motor continues to run. If the error occurs during an RTZ:
Table Continued on Next Page	

TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
	• Seek Error and Seek End lines go active. • Motor continues to run. • The servo system is disabled and the heads, although loaded, float freely over the disk surfaces. If the error occurs during a first seek, pressing the Fault Clear switch clears the fault and initiates another load. If it occurs during an RTZ, commanding another RTZ clears the seek error and initiates another seek to cylinder 0. • The servo system is disabled and the heads, although loaded, float freely over the disk surfaces. If the error occurs during a first seek, pressing the Fault Clear switch clears the fault and initiates another load. If it occurs during an RTZ, commanding another RTZ clears the seek error and initiates another seek to cylinder 0. PROBABLE CAUSES: Bad tribit decoder circuit, cylinder pulse detection circuit, or servo disk. ACTIONS 1. Check for loose cable at J28 on _VDX board. 2. Replace _VDX board (proc 5301). 3. Replace module (proc 5209).
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TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
40	Title: Inner Guardband Detected During Normal Seek DESCRIPTION: Indicates that guardband pulses were detected while the heads were moving over the data zone. When the drive displays code 40, the following error indications also appear: • Motor continues to run but the servo system is disabled and the heads, although loaded, float freely over the disk surfaces. • Seek Error and Seek End lines go active. An RTZ command clears the seek error and initiates a seek to cylinder 0. PROBABLE CAUSES: Cylinder pulses missed or miscounted during seek. Could be caused by bad cylinder pulse detection circuits, defective servo surface, bad tribit decoder circuits, or electrical noise generated by nearby equipment. ACTIONS 1. Ensure that drive is not located near source of extreme electrical noise. 2. Check for loose cable at J28 on _VDX board. 3. Replace _VDX board (proc 5301). 4. Replace module (proc 5209).

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TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
41	Title: Inner Guardband Detected During On Cylinder Routine DESCRIPTION: Indicates guardband pulses were detected while the heads were settling into the on cylinder position. When the drive displays code 41, the following error indications also appear: If the error occurs during a first seek: • First Seek LED lights • FAULT indicator lights and Fault line goes active (first seeks only). • Motor continues to run. If the error occurs during an RTZ or normal seek: • Seek Error and Seek End lines go active. • Motor continues to run but the servo system is disabled and the heads, although loaded, float freely over the disk surfaces. If the error occurs during a first seek, pressing the Fault Clear switch clears the fault and initiates another load. If it occurs during an RTZ, commanding another RTZ clears the seek error and initiates a seek to cylinder 0. PROBABLE CAUSES: Bad servo track, bad tribit decoder circuits, electrical noise generated by nearby equipment.

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TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
	ACTIONS 1. Ensure that drive is not located near source of extreme electrical noise. 2. Replace _VDX board (proc 5301). 3. Replace module (proc 5209).
42	Title: Inner Guardband Detected While On Cylinder DESCRIPTION: Indicates that inner guardband pulses were detected while the heads were on cylinder. When the drive displays code 42, the following error indications also appear: • Motor continues to run but the servo system is disabled and the heads, although loaded, float freely over the disk surfaces. • Seek Error and Seek End lines go active. An RTZ command clears the seek error and initiates a seek to cylinder 0. PROBABLE CAUSES: Bad servo track, bad tribit decoder circuits, electrical noise generated by nearby equipment. ACTIONS 1. Ensure drive is not located near source of extreme electrical noise. 2. Replace _VDX board (proc 5301). 3. Replace module (proc 5209).
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TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
43	Title: Outer Guardband Detected During Normal Seek DESCRIPTION: Indicates that guardband pulses were detected while the heads were moving over the data zone. When the drive displays code 43, the following error indications also appear: • Motor continues to run but the servo system is disabled and the heads, although loaded, float freely over the disk surfaces. • Seek Error and Seek End lines go active. An RTZ command clears the seek error and initiates a seek to cylinder 0. PROBABLE CAUSES: Cylinder pulses missed or miscounted during seek. Could be caused by bad cylinder pulse detection circuits or by electrical noise generated by nearby equipment. ACTIONS 1. Ensure drive is not located near source of extreme electrical noise. 2. Replace _VDX board (proc 5301). 3. Replace module (proc 5209).
44	Title: Outer Guardband Detected During On Cylinder Routine DESCRIPTION: Indicates guardband pulses were detected while the heads were settling into the on cylinder position. When the drive displays code 44, the following error indications also appear:

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TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
	If the error occurs during a first seek: • First Seek LED lights. • FAULT indicator lights and Fault line goes active (first seeks only). • Motor continues to run. If the error occurs during an RTZ or normal seek: • Seek Error and Seek End lines go active. • Motor continues to run but the servo system is disabled and the heads, although loaded, float freely over the disk surfaces. If the error occurs during a first seek, pressing the Fault Clear switch clears the fault and initiates another load. If it occurs during an RTZ, commanding another RTZ clears the seek error and initiates a seek to cylinder 0. PROBABLE CAUSES: Bad servo track, bad tribit decoder circuits, electrical noise generated by nearby equipment. ACTIONS 1. Ensure drive is not located near source of extreme electrical noise. 2. Replace _VDX board (proc 5301). 3. Replace module (proc 5209).

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TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
45	Title: Outer Guardband Detected While On Cylinder DESCRIPTION: Indicates that outer guardband pulses were detected while the heads were on cylinder. When the drive displays code 45, the following error indications also appear: • Motor continues to run but the servo system is disabled and the heads, although loaded, float freely over the disk surfaces. • Seek Error goes active. An RTZ command clears the seek error and initiates a seek to cylinder 0. PROBABLE CAUSES: Bad servo track, bad tribit decoder circuits, electrical noise generated by nearby equipment. ACTIONS 1. Ensure drive is not located near source of extreme electrical noise. 2. Replace _VDX board (proc 5301). 3. Replace module (proc 5209).
46	Title: Seek Timeout DESCRIPTION: Indicates that during a normal seek the drive took longer than 60 milliseconds to reach on cylinder. When the drive displays code 46, the following error indications also appear.
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TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
	• Seek error and Seek End lines go active. • Motor continues to run but servo system is disabled and the heads, although loaded, drift freely over the disk surfaces. An RTZ clears the seek error and initiates a seek to cylinder 0. PROBABLE CAUSES: Problem with voice coil or velocity circuits. ACTIONS 1. Replace _VDX board (proc 5301). 2. Replace _UCX board (proc 5304).
47	Title: Too Long to Get On Cylinder Sense DESCRIPTION: Indicates that too much time elapsed from Fine Enable going active to On cylinder going active. When the drive displays code 47, the following error indications also appear: If the error occurs during a first seek: • First Seek LED lights. • FAULT indicator lights and Fault line goes active (first seeks only). • Motor continues to run. If the error occurs during an RTZ or normal seek:
	Table Continued on Next Page

TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
	• Seek Error and Seek End lines go active. • Motor continues to run but the servo system is disabled and the heads, although loaded, float freely over the disk surfaces. If the error occurs during a first seek, pressing the Fault Clear switch clears the fault and initiates another load. If it occurs during an RTZ, commanding another RTZ clears the seek error and initiates a seek to cylinder 0. PROBABLE CAUSES: On cylinder sense circuits not functioning. ACTIONS 1. Replace _VDX board (proc 5301). 2. Replace module (proc 5209).
48	Title: Demodulator Active Lost During On Cylinder Routine DESCRIPTION: Indicates that Demodulator Active went inactive as the heads approached on cylinder. When the drive displays code 48, the following error indications also appear. If the error occurs during a first seek: • First Seek LED lights. • FAULT indicator lights and Fault line goes active. • Motor continues to run.
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TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
	If the error occurs during an RTZ or normal seek: • Seek Error and Seek End lines go active. • Motor continues to run, but the servo system is disabled and the heads, although loaded, float freely over the disk surfaces. If the error occurs during a first seek, pressing the Fault Clear switch clears the fault and initiates another load. If it occurs during an RTZ, commanding another RTZ clears the seek error and initiates another load and seek to cylinder 0. PROBABLE CAUSES: Bad servo disk, bad tribit decoder circuits, loose cabling in feedback loop. ACTIONS Perform sequential forward seeks with read. 1. If error occurs at same cylinder each time, replace module. 2. If error occurs at random locations, check for loose cable at J28 on _VDX board. 3. If problem still exists, replace __VDX board (proc 5301).

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TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
49	Title: Too Many Cylinder Pulses During Settle In DESCRIPTION: Indicates that three or more cylinder pulses were detected during settle in thus, indicating excessive overshoot. Excessive overshoot can result in the heads settling on the wrong cylinder. When the drive displays code 49, the following error indications also appear: If the error occurs during a first seek: • First Seek LED lights. • FAULT indicator lights and Fault line goes active (first seeks only). • Motor continues to run. If the error occurs during an RTZ or normal seek: • Seek Error and Seek End lines go active. • Motor continues to run but the servo system is disabled and the heads, although loaded, float freely over the disk surfaces. If the error occurs during a first seek, pressing the Fault Clear switch clears the fault and initiates another load. If it occurs during an RTZ, commanding another RTZ clears the seek error and initiates another seek to cylinder 0. PROBABLE CAUSES: Velocity or cylinder pulse detection circuits.

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TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
	ACTIONS 1. Check for loose cable at J28 on _VDX board. 2. Replace _VDX board (proc 5301).
4A	Title: Too Many On Cylinder Dropouts DESCRIPTION: Indicates that On Cylinder Sense took too long to stabilize during the settle in phase. When the drive displays code 4A, the following error indications also appear: If the error occurs during a first seek: • First Seek LED lights. • FAULT indicator lights and Fault line goes active (first seeks only). • Motor continues to run. If the error occurs during an RTZ or normal seek: • Seek Error and Seek End lines go active. • Motor continues to run but the servo system is disabled and the heads, although loaded, float freely over the disk surfaces. If the error occurs during a first seek, pressing the Fault Clear switch clears the fault and initiates another load. If it occurs during an RTZ, commanding another RTZ clears the seek error and initiates another seek to cylinder 0.
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TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
	PROBABLE CAUSES: Cylinder pulses missed or miscounted during seek. Could be caused by bad cylinder pulse detection circuits, defective module, bad tribit decoder circuits, or electrical noise generated by nearby equipment. ACTIONS 1. Ensure drive is not located near source of extreme electrical noise. 2. Replace _VDX board (proc 5301). 3. Replace module (proc 5209).
4B	Title: Off Cylinder DESCRIPTION: Indicates that either On Cylinder Sense went inactive or cylinder pulses were detected while On Cylinder was active. When the drive displays code 4B, the following error indications also appear. • On Cylinder goes inactive. • Seek Error goes active. • Motor continues to run but the servo system is disabled and the heads, although loaded, float freely over the disk. An RTZ command clears the seek error and initiates a seek to cylinder 0. PROBABLE CAUSES: Bad servo disk, loose cabling in feedback loop, or poor tracking due to mechanical or electrical noise problems.
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TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
	ACTIONS 1. Ensure that malfunction was not caused by excessive vibration levels (for example, from nearby construction activities or nearby electrical noise (for example, line printers). 2. If error occurs at same cylinder each time, replace module (proc 5209). 3. If error occurs at random locations: a. Check for loose cable at J28 on _VDX board. b. Replace _VDX board (proc 5301). c. Replace module (proc 5209).
4C	Title: Lost Demodulator Active While On Cylinder DESCRIPTION: Indicates that Demodulator Active went inactive while the heads were on cylinder. When the drive displays code 4C, the following error indications also appear. • On Cylinder goes inactive • Seek Error goes active. • Motor continues to run. An RTZ command clears the seek error and initiates a load and seek to cylinder 0. PROBABLE CAUSES: Bad servo disk, bad tribit decoder circuits, loose cabling in feedback loop.
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TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
	ACTIONS Perform sequential forward seeks with read. 1. If error occurs at same cylinder each time, replace module. 2. If error occurs at random locations: a. Check for loose cable at J28 on _VDX board. b. If problem still exists, replace _VDX board (proc 5301).
4E	Title: Voltage Fault While On Cylinder DESCRIPTION: Indicates that the MPU detected a voltage fault while On Cylinder was active. When the drive displays code 4E, the following error indications also appear. • READY indicator goes out and Ready line goes inactive. • Seek Error goes active. • FAULT indicator lights and Fault line goes active. • Motor continues to run. If the fault is no longer present, a Controller Fault Clear followed by an RTZ or pressing Fault Clear switch clears the fault and initiates a load and seek to cylinder 0. PROBABLE CAUSES: Power failure within drive, power supply or site power.
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TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
	ACTIONS Check LEDs for cause of fault condition. 1. If voltage fault exists go to Power Check (TSP1 or proc 4101).
50	Title: Recovering From Low Vcc Reset DESCRIPTION: Indicates that recovery from low Vcc reset has taken place. At the start of the sequence, all I/O signals go inactive and remain so at least until the end of the MPU initialization phase. When MPU initialization is complete, Seek Error and Seek End go active. The Fault line also goes active and the FAULT indicator lights. The drive proceeds to bring the motor up to speed but will not load the heads until the fault condition is cleared (via controller Fault Clear signal or pressing Fault Clear switch). If the fault is cleared and load is successful, Ready goes active when the MPU is ready to perform normal servo actions. Seek error stays set until an RTZ is received. PROBABLE CAUSES: Momentary power supply or site power failure. ACTIONS 1. If more resets occur check site power, power supply, and drive power wiring.

Table Continued on Next Page

TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
51	Title: Recovering From MPU Hang Reset DESCRIPTION: Indicates that the drive is re-executing the power on sequence routine in an attempt to recover from an MPU hang condition. At the start of the sequence, all I/O signals go inactive and remain so at least until the end of the MPU initialization phase. When MPU initialization is complete, Seek Error and Seek End go active. If the recovery is successful, Ready goes active but the servo system is disabled and the heads, although loaded, float freely over the disk surfaces. An RTZ clears the seek error and initiates a seek to cylinder 0. PROBABLE CAUSES: Chip failure in MPU system causing instruction to be read incorrectly from EPROM. ACTIONS 1. Replace _VDX board (proc 5301).
52	Title: Recovered From Low Vcc Reset and Subsequent Speed Loss DESCRIPTION: Indicates that the heads are floating after recovery from a low Vcc reset followed by a loss of speed error. Seek Error is active. Ready remains active. On Cylinder remains inactive until the drive receives an RTZ. PROBABLE CAUSES: Momentary power supply or site power failure.
Table Continued on Next Page	

TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
	ACTIONS 1. If more resets occur check site power, power supply, and drive power wiring.
53	Title: Recovered From MPU Hang And Subsequent Speed Loss DESCRIPTION: Indicates that the heads are floating after recovery from an MPU hang followed by a loss of speed error. Seek Error is active. Ready remains active. On Cylinder remains inactive until the drive receives an RTZ. PROBABLE CAUSES: Microprocessor failed or conditions existed that caused it to hang in an illegal mode. ACTIONS 1. Replace _VDX board (proc 5301).
58	Title: Non-Maskable Interrupt DESCRIPTION: A non-maskable interrupt was detected by the microprocessor even though this type of interrupt should never occur. PROBABLE CAUSES: Microprocessor failed or problem with logic on control board. ACTION 1. Replace _VDX board (proc 5301).

Table Continued on Next Page

TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
59	Title: Software Interrupt DESCRIPTION: A software interrupt was detected by the microprocessor even though this type of interrupt should never occur. PROBABLE CAUSES: Microprocessor failed or problem with logic on control board. ACTION 1. Replace _VDX board (proc 5301).
5F	Title: PIA Test Failure DESCRIPTION: Indicates that, during power on initialization, the MPU detected a PIA failure. When this occurs the drive stops the power on sequence and keeps all fault LEDs lighted. To clear the error and initiate a retry, set CB1 to Off and then back to On. PROBABLE CAUSES: Bad PIA or defective chip in MPU system. ACTIONS 1. Replace _VDX board (proc 5301).
80	Title: Fault Before Seek Begins DESCRIPTION: Indicates that a fault condition existed when a normal or RTZ seek was commanded. When the drive displays code 80, the following error indications also appear. • Seek Error and Seek End go active.

Table Continued on Next Page

TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
	• Ready goes inactive. • FAULT indicator lights and Fault line goes active. • For a voltage fault, the motor continues to run but heads are retracted via emergency retract. • For other than a voltage fault, the motor continues to run but the servo system is disabled and the heads, although loaded, float freely over the disk surfaces. If the fault is no longer present, a Controller Fault Clear followed by an RTZ or pressing Fault Clear switch clears the fault and initiates a load and seek to cylinder 0. PROBABLE CAUSES: Any of the possible fault conditions. ACTIONS 1. Check fault LEDs on Status/Fault Display board.
90	Title: Recovered From Speed Loss DESCRIPTION: Indicates that drive has recovered from a speed loss. The heads are loaded but floating and Seek Error is active. On Cylinder and Ready will go active when the drive receives an RTZ. PROBABLE CAUSES: Motor speed detection circuit, motor failure or power supply failure. ACTIONS If more failures occur: 1. Replace _UCX board (proc 5304).
Table Continued on Next Page	

TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
	2. Replace power supply (proc 5207). 3. Replace drive motor (proc 5206).
A1 thru CE	Title: Error conditions with FAULT present. DESCRIPTION: The following codes correspond to codes previously listed, except that the FAULT line is active when they are observed. The codes covered in this discussion are listed below with the corresponding (NO FAULT) code given in parentheses. A1 (21) A2 (22) A5 (25) A6 (26) A7 (27) A8 (28) AB (2B) AC (2C) AD (2D) BO (30) B1 (31) B3 (33) B4 (34) B5 (35) B6 (36) B7 (37) B8 (38) B9 (39) C0 (40) C1 (41) C2 (42) C3 (43) C4 (44) C5 (45) C6 (46) C7 (47) C8 (48) C9 (49) CA (4A) CB (4B) CC (4C) CE (4E) When the drive displays one of the A1 through CE codes the following error indications also appear. • First Seek LED lights (first seek only). • FAULT indicator lights and Fault line goes active. • Seek Error and Seek End lines go active (not during first seek). • Motor continues to run. If the fault condition no longer exists, a Controller Fault Clear followed by an RTZ or pressing the Fault Clear switch clears the fault and initiates another load.

Table Continued on Next Page

TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
	PROBABLE CAUSES: Voltage fault caused by failure within drive, site power, or power supply. Extraneous fault, such as read and write, caused by I/O problem. ACTIONS Check LEDs for cause of fault condition. 1. If voltage fault exists: a. Check ±24 volts (TSP1). If voltages are abnormal, go to ±24 Volt Load Check (TSP3). b. Replace power supply (proc 5207). 2. If a fault other than voltage exists: a. Check I/O cabling. b. Replace _SYX/_TQX board (proc 5305).
60	Title: Servo Test Failure During RTZ DESCRIPTION: Indicates that the drive failed to complete an RTZ operation. The test is initiated with the heads at cylinder zero and requires that the carriage move two cylinders into the outer guardband and then return to cylinder zero. PROBABLE CAUSES: MPU failure, break in the cabling between the control board and the HDA, HDA failure, or power supply failure. ACTIONS 1. Replace _VDX board (proc 5301).
Table Continued on Next Page	

TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
	2. Check cabling between _UCX board and module (proc 5304). 3. Replace module (proc 5209). 4. Replace power supply (proc 5207).
61	Title: Servo Failure During Recalibrate DESCRIPTION: Indicates that the drive failed to complete six 128-track seeks repeated three times. All seeks start at cylinder zero with a destination of cylinder 127. PROBABLE CAUSES: MPU failure, break in the cabling between the control board and the HDA, HDA failure, or power supply failure. ACTIONS 1. Replace _VDX board (proc 5301). 2. Check cabling between _UCX board and module. 3. Replace module (proc 5209). 4. Replace power supply (proc 5207).
62	Title: Servo Test Failure During 1 Track Seek DESCRIPTION: Indicates that the drive failed to complete a series of 16 1-track seeks. All seeks originate at cylinder zero and terminate at cylinder one.

Table Continued on Next Page

TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
	PROBABLE CAUSES: MPU failure, break in the cabling between the control board and the HDA, HDA failure, or power supply failure. ACTIONS 1. Replace _VDX board (proc 5301). 2. Check cabling between _UCX board and module. 3. Replace module (proc 5209). 4. Replace power supply (proc 5207).
63	Title: Servo Test Failure During Maximum Length Seek DESCRIPTION: Indicates that the drive failed to complete a series of sixteen 1064-track seeks. All seeks originate at cylinder zero and terminate at cylinder 1063. PROBABLE CAUSES: MPU failure, break in the cabling between the control board and the HDA, HDA failure, or power supply failure. ACTIONS 1. Replace _VDX board (proc 5301). 2. Check cabling between _UCX board and module. 3. Replace module (proc 5209). 4. Replace power supply (proc 5207).

Table Continued on Next Page

TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
64	Title: Failed Recalibrate Test DESCRIPTION: Indicates that the servo logic failed to complete the same servo gain number three consecutive times while executing test 61. PROBABLE CAUSES: MPU failure or power supply failure. ACTIONS 1. Replace _VDX board (proc 5301). 2. Replace power supply (proc 5207).
65	Title: 1 Track Seek Too Short DESCRIPTION: Indicates that the drive executed the series of 16 one-track seeks in test 62 too fast. PROBABLE CAUSES: MPU failure. ACTION 1. Replace _VDX board (proc 5301).
66	Title: 1 Track Seek Too Long DESCRIPTION: Indicates that the drive executed the series of 16 one-track seeks in test 62 too slowly. PROBABLE CAUSES: MPU failure. ACTION 1. Replace _VDX board (proc 5301).
Table Continued on Next Page	

TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
67	Title: Maximum Length Seek Too Fast DESCRIPTION: Indicates that the drive executed the series of sixteen 1064-track seeks in test 63 too fast. PROBABLE CAUSES: MPU failure. ACTION 1. Replace _VDX board (proc 5301).
68	Title: Maximum Length Seek Too Slow DESCRIPTION: Indicates that the drive executed the series of sixteen 1064-track seeks in test 63 too slow. PROBABLE CAUSES: MPU failure. ACTION 1. Replace _VDX board (proc 5301).
69	Title: Bad Preseek Status DESCRIPTION: Indicates that drive was not ready at the time a seek operation was initiated. PROBABLE CAUSES: Fault detection circuitry not functioning. ACTION 1. Replace _SYX/_TQX board (proc 5305).

Table Continued on Next Page

TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
70	Title: Self Test Complete DESCRIPTION: Indicates that the drive successfully completed the power up tests. PROBABLE CAUSES: N.A. ACTION N.A.
71	Title: Fan On DESCRIPTION: Not functional on this drive. Status forced to on condition during power up.
72	Title: Execute Switch Does Not Release DESCRIPTION: Execute switch does not go to inactive state after a timeout following release. This prevents any use of the Fault Display panel. PROBABLE CAUSES: 1. Faulty Execute switch. 2. Short to ground in switch wiring. ACTIONS 1. Replace _UQX Fault Display panel (proc 5203). 2. Troubleshoot switch wiring.
Table Continued on Next Page	

TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
D0	Title: Recovering From Low Vcc Reset DESCRIPTION: Indicates that recovery from low Vcc has taken place. At the start of the sequence, all I/O signals go inactive and remain so at least until the end of the MPU initialization phase. When MPU initialization is complete, Seek Error and Seek End go active. The Fault line also goes active and the FAULT indicator lights. Code D0 remains set until the Fault line goes inactive. The drive proceeds to bring the motor up to speed but will not load the heads until the fault condition is cleared (via controller Fault Clear signal or pressing Fault Clear switch). If the fault is cleared and load is successful, Ready goes active when the MPU is ready to perform normal servo actions. Seek error stays set until an RTZ is received. PROBABLE CAUSES: Momentary power failure. ACTIONS 1. If more resets occur, check site power, power supply and drive power wiring.
D1	Title: Recovering From MPU Hang Reset DESCRIPTION: Indicates that the drive is re-executing the power on sequence routine in an attempt to recover from an MPU hang condition. At the start of the sequence, all I/O signals go inactive and remain so at least until the end of the MPU initialization phase. When MPU initialization is complete, Seek Error and Seek End go active. Code D1 remains set until the Fault line goes inactive.
Table Continued on Next Page	

TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
	If the recovery is successful, Ready goes active but the servo system is disabled and the heads, although loaded, float freely over the disk surfaces. An RTZ clears the seek error and initiates a seek to cylinder 0. PROBABLE CAUSES: Chip failure in MPU system causing instruction mode to be read incorrectly from EPROM. ACTION 1. Replace _VDX board (proc 5301).
FF	Title: MPU Failed Power On Test DESCRIPTION: Indicates that MPU failed power on initialization test. When this occurs, the drive stops the power on sequence and keeps all fault LEDs lighted. To clear the error and initiate a retry, set CB1 to OFF and then back to ON. PROBABLE CAUSES: Bad MPU, RAM, or other failure preventing MPU from operating. ACTIONS 1. Check for a failure in the ±5 volts and ±24 volts power supply (proc 4101). 2. Replace _VDX board (proc 5301).

SECTION 4

ELECTRICAL CHECKS AND ADJUSTMENTS

ELECTRICAL CHECKS AND ADJUSTMENTS 4

CAUTION

When servicing the drive, observe all precautions listed under Electrostatic Discharge Protection in Section 2 of this manual. Failure to observe these precautions can result in serious damage to electronic assemblies.

INTRODUCTION

This section contains electrical checks and adjustments intended for use in isolating problems causing improper drive operation. These procedures should be used in conjunction with the troubleshooting information in section 3.

If the drive appears to be operating properly, failure to meet a specification given here does not in itself indicate improper drive operation. The person performing these procedures should be thoroughly familiar with drive operation and with all information in the general maintenance section of this manual (particularly the warnings and precautions).

Each electrical check procedure is assigned a unique number. The numbers are used elsewhere in the manual to reference the procedures. The procedure numbers are organized into five categories: 41XX - power checks and adjustments, 42XX - servo checks, 43XX - write checks, 44XX - read checks, and 45XX - miscellaneous.

The procedures appear in the following order.

- 4101 - Power Checks
- 4102 - Voltage adjustment
- 4201 - Tribit Check
- 4202 - Position Signal Check
- 4203 - Servo Offset Check
- 4204 - On Cylinder Check
- 4301 - Write Fault Grounding
- 4302 - Write PLO Check

- 4303 - Write Data Check
- 4304 - Write Address Mark Check
- 4401 - Read PLO Check
- 4402 - Read Data Check
- 4403 - Read Address Mark Check
- 4501 - Index Check
- 4502 - Sector Check

POWER CHECKS AND ADJUSTMENTS

4101 - POWER CHECKS

The following procedure provides an overall check of the dc voltages used by the drive. Table 4-1, shows the voltages required by each drive component. See the diagrams section of hardware maintenance manual volume 3 for specific information concerning voltage test points.

CAUTION

Because some voltage measurements are on pins adjacent to each other, it is possible to touch both pins simultaneously, thus causing a short circuit. A short circuit will cause serious damage to drive electronic assemblies. Therefore, use extreme caution when performing the following steps.

1. Command continuous seeks between cylinder 0 and 512.
2. Connect voltmeter ground lead to a voltage return connection point listed below.
3. Measure between the return point and its respective voltage connection points to check the following voltages:

Voltage	Connection	Specification
+5 volts	TP-2 G201 (_UCX)	+4.85 to +5.25 volts
-5 volts	TP-1 F901 (_UCX)	-4.85 to -5.35 volts
±5 volt ret.	TP-3 G401 (_UCX)	±5 volt return
-8.3 volts *	J28-6 (_VDX)	-8.1 to -8.5 volts
+24 volts	TP-4 G701 (_UCX)	+21.6 to +26.4 volts
-24 volts	TP-6 H201 (_UCX)	-21.6 to -26.4 volts
±24 volt ret.	TP-5 G901 (_UCX)	±24 volt return
+15 volts *	J29-54 (_VDX)	N/A
-15 volts *	J29-56 (_VDX)	N/A

The voltages indicated by an asterisk are developed on the _VDX board from ±24 V input. Use ±24 volt ret. for voltmeter ground lead to measure these voltages.

4. Proceed to next test or return drive to system operation.

TABLE 4-1. DC VOLTAGE DISTRIBUTION

Component	Voltage					
	+5 V	-5 V	-8.3 V*	+24 V	-24 V	±15 V*
_VDX	X	X	X	X	X	X
_SUX	X	X				X
_SYX/_TQX	X	X				
_UCX	X	X		X	X	
Mother Bd (_TRX)	X	X		X	X	
_TSX	X	X	X			
_UQX	X					
_WFV	X	X		X	X	
_RTX				X		
Op Pnl (_PBX)	X					

*Voltages developed on the _VDX board from ±24 V input.

4102 - VOLTAGE ADJUSTMENT

Only the output voltages of the +5 V and the -5 V supplies are adjustable. The adjustment potentiometers are located within the dc section of the power supply. They are accessible through a slotted opening cut through the power supply top cover and the _TRX mother board as shown in figure 4-1.

+5 V Adjustment

1. Connect voltmeter to TP-2 at location G201 (+5 V) and TP3 at location G401 (±5 V return) on the _UCX power amp. board.

2. Adjust +5 V potentiometer (see figure 4-1) for an output reading of +5.1 ±.05 volts.

-5 V Adjustment

1. Connect voltmeter to TP-1 at location F901 (-5 V) and TP3 at location G401 (±5 V return) on the _UCX power amp. board.

2. Adjust -5 V potentiometer (see figure 4-1) for an output reading of -5.1 ±.05 volts.

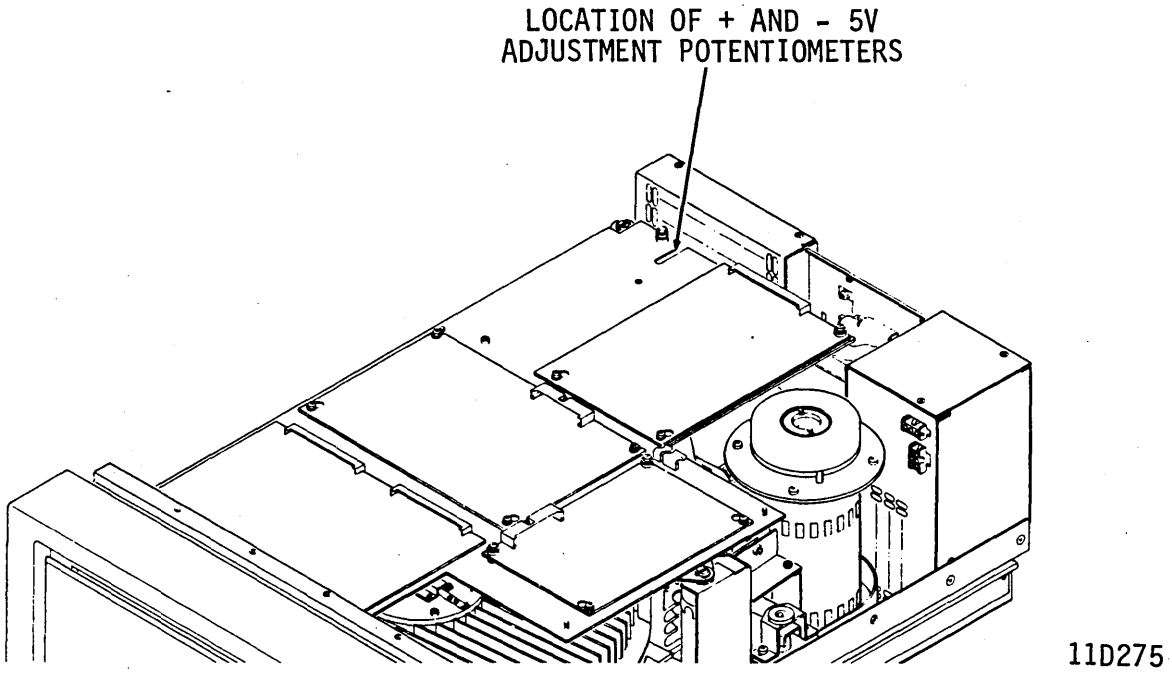

Figure 4-1. ±5 V Adjustment Potentiometers

SERVO CHECKS

4201 - TRIBIT CHECK

1. Connect oscilloscope as shown on figure 4-2.
2. Command a return to zero seek.
3. Observe that the relationship between +Tribit and -Tribit servo signals is similar to that on figure 4-2.
4. Connect oscilloscope as shown on figure 4-3.
5. Observe that the ±Tribit signals are similar to those on figure 4-3.
6. Proceed to next test or return drive to system operation.

4202 - POSITION SIGNAL CHECK

1. Connect oscilloscope as shown on figure 4-4.
2. Command continuous seeks between cylinders 0 and 512.

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	50 MV/CM	B507 ON _VDX (1)	-TRIBITS
CH 2	50 MV/CM	B407 ON _VDX (1)	+TRIBITS

TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
+ INT CH 1		

SCOPE GND TO GND ON LOGIC CARD.
USE X10 PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: .2 µs/CM MODE: ALT.

NOTES: (1) CONNECT SCOPE PROBE TO COMPONENT LEAD FARTHEST FROM THE BOARD EDGE..

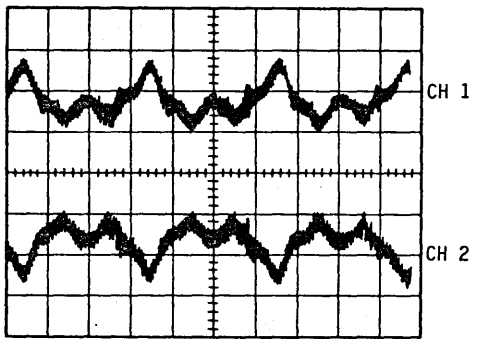

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Figure 4-2. Servo Signal Waveform

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	.2/CM	B519 ON _VDX (1)	-TRIBIT (AGC'D)
CH 2	.2/CM	C117 ON _VDX (1)	+TRIBIT (AGC'D)

TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
-INT. CH 1		

SCOPE GND TO GND ON LOGIC CARD.
USE XIO PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: .2 µs/CM MODE: ALT

NOTES: (1) CONNECT SCOPE PROBE TO COMPONENT LEAD CLOSEST TO THE BOARD EDGE.

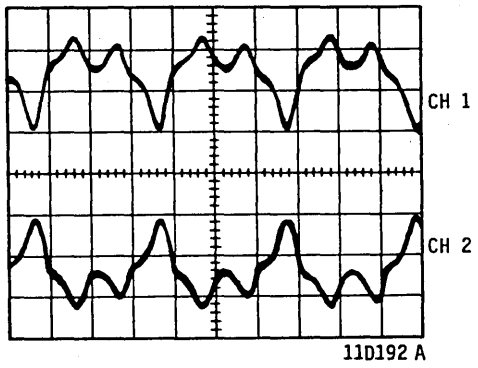


Figure 4-3. Tribits Waveform

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	2/CM	J80-7 ON _VDX	-POSITION
CH 2			

TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
+ EXT.	J80-4 ON _VDX	-FORWARD

SCOPE GND TO GND ON LOGIC CARD.
USE XIO PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 5 MS/CM MODE: CH 1

NOTES:

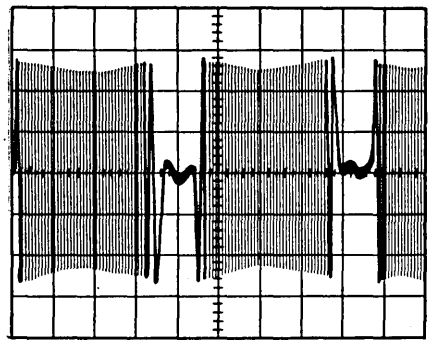


Figure 4-4. Position Signal (Tracks 0-512)

3. Observe that the peak to peak value of -Position signal remains between 9.5 and 11.5 volts over the period of a complete seek.

4. Command continuous seeks between cylinders 0 and 1023 and observe that -Position is as described in step 3 (see figure 4-5).

5. Proceed to next test or return drive to system operation.

4203 - SERVO OFFSET CHECK

This procedure checks the amount of head offset caused by a servo offset command. The measurement is made on the Position signal. The Position signal has an average dc level of zero, when there is no offset and the heads are on cylinder.

1. Set oscilloscope to measure 0.5 V/cm and connect it between J80-07 and ground (mother board ground jack).

2. Command return to zero seek and observe that scope indicates 0 $\pm$ 500 millivolts.

3. Command a read operation with positive (forward) offset and observe that scope indicates a dc offset between -0.60 and -0.90 volts.

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	2/CM	J80-7 ON _VDX	-POSITION
CH 2			

TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
+ EXT.	J8-4 ON _VDX	-FORWARD

SCOPE GND TO GND ON LOGIC CARD.
USE X10 PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 5 MS/CM MODE:

NOTES:

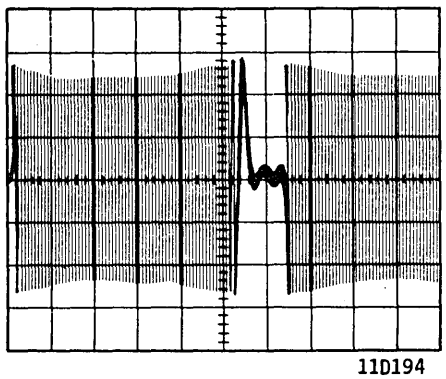


Figure 4-5. Position Signal (Tracks 0 to 1023)

4. Command a read operation with negative (reverse) offset and observe that scope indicates a dc offset between +0.60 and +0.90 volts.

5. Proceed to next test or return drive to system operation.

4204 - ON CYLINDER CHECK

This procedure verifies that On Cylinder goes active.

1. Connect oscilloscope as follows:

   a. Connect channel 1 to J81-9 (+On Cylinder) on _SYX or _TQX board.

   b. Trigger + Internal on channel 1.

   c. Set other controls as appropriate to make measurement in step 3.

2. Command continuous seeks between cylinders 0 and 1.

3. Observe that +On Cylinder goes active.

4. Proceed to next test or return drive to system operation.

WRITE CHECKS

The following procedures, 4301 through 4304, check various aspects of drive write circuit operation. Figure 4-6 is a block diagram showing the major components in the write circuits and the test points used in the procedures.

4301 - WRITE FAULT GROUNDING

If a write fault condition exists, the drive write circuits are disabled. This makes it difficult to test the write circuits and isolate the problem. Grounding the Write Fault signal at the point where it leaves the _SUX board disables the write fault function thus allowing the drive to perform write operations even though fault conditions exist. The following procedure describes the proper method for grounding the Write Fault signal.

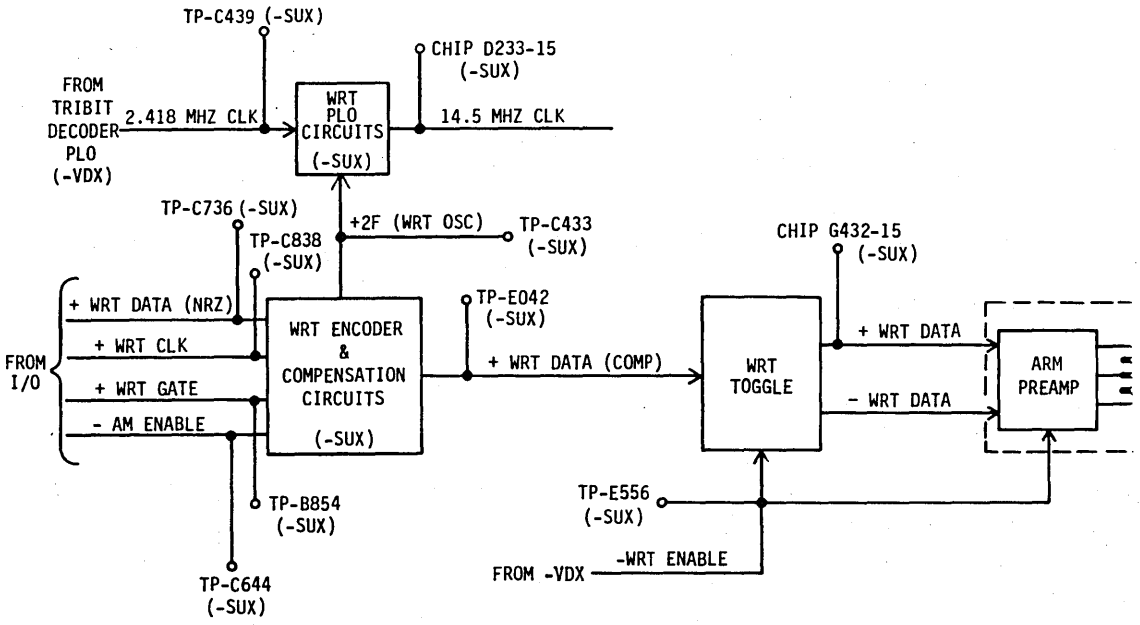


Figure 4-6. Write Circuits Test Points

CAUTION

Perform this procedure only during trouble-shooting when a write fault condition interferes with isolating the problem.

1. Remove power from drive as follows:

   a. Press START switch to stop motor and retract heads.

   b. Set CB1 to off.

CAUTION

Be certain to remove jumper wire when testing is complete. Failure to remove wire can result in loss of customer data.

2. Connect jumper wire between TP-C642 (Write Fault) and TP-A244 (ground) on _SUX board.

3. Power up drive and perform tests. Monitor TP-B645 (+Fault) on _SUX board to determine if write fault condition persists. When testing is complete, remove jumper wire.

4302 - WRITE PLO CHECK

This procedure checks the operation of the write PLO. The PLO provides timing signals used, during write operations by both the drive and controller.

1. Connect oscilloscope and observe that 2.418 Mhz Clock frequency is approximately as shown on figure 4-7.

2. Connect oscilloscope and observe that 14.5 Mhz Clock frequency is approximately as shown on figure 4-8.

3. Connect oscilloscope and observe that 2F (Write Oscillator) timing is approximately 29.01 MHz (see figure 4-9).

4. Proceed to next test or return drive to system operation.

4303 - WRITE DATA CHECK

This procedure checks for the presence of write data at various points in the write circuits (see figure 4-6). If the signals at these points are correct, it indicates the circuits are performing their basic functions. This procedure will normally be performed because of a write problem. In that case, a write fault condition may exist and it will be necessary to perform procedure 4301 - Write Fault Grounding to perform a write operation.

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	0.5 V/CM	TP-C439 ON _SUX	2.418 MHZ CLOCK
CH 2			

TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
- INT CH 1		

SCOPE GND TO GND ON LOGIC CARD.
USE XIO PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 0.2 µS/CM MODE:

NOTES:

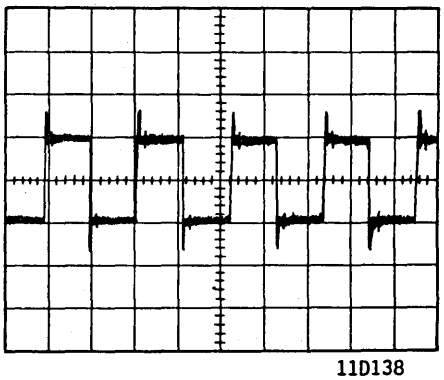


Figure 4-7. 2.418 MHz Clock Timing

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	0.5 V/CM	CHIP D233-15 ON _SUX	+ 14.5 MHZ CLOCK
CH 2			

TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
-INT CH 1		

SCOPE GND TO GND ON LOGIC CARD.
USE XIO PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 0.05 µS/CM MODE:

NOTES:

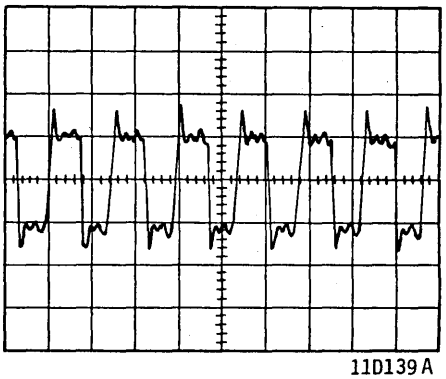


Figure 4-8. 14.5 MHz Servo Clock Timing

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	0.5 V/CM	TP-C433 ON _SUX	+ 2F (WRT OSC)
CH 2			

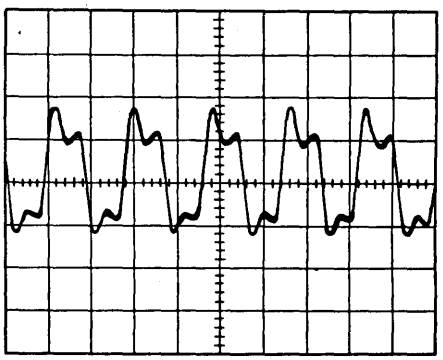
TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
- INT CH 1		

SCOPE GND TO GND ON LOGIC CARD.
USE X10 PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 0.02 µS/CM MODE:

NOTES:



11D140

Figure 4-9. 2F (Write Oscillator) Timing

CAUTION

To avoid possible loss of customer data, select a cylinder and head that will result in data being written on an unused track.

1. Command drive to seek to desired cylinder and select desired head and sector.

2. Command drive to write a 1010... pattern.

3. Connect oscilloscope and observe that +Write Gate and -Write Enable change state simultaneously as shown on figure 4-10.

4. Check inputs to write encoder and compensation circuits. Timing relationships between these signals, NRZ write data and write clock, must be correct before encoding and write compensation can be properly performed.

   a. Connect oscilloscope as shown on figure 4-11 and observe that Write Clock frequency is approximately 14.5 MHz.

b. Observe that timing relationship between Write Data (NRZ) and Write Clock is similar to that on figure 4-11. Write Clock should go positive at approximately the center of the data "1" pulses.

5. Check write data (compensated) control circuits as follows:

   a. Connect oscilloscope as shown on figure 4-12.

   b. Observe that timing relationship between Write Data (Compensated) and 2F (Write Oscillator) is similar to that on figure 4-12.

6. Check output of write toggle circuits as follows:.

   a. Move oscilloscope channel 2 probe to I/C G432-15 on _SUX board (see figure 4-13).

   b. Observe that signals are approximately as shown on figure 4-13.

7. Proceed to next test or return drive to system operation.

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	2.0 V/CM	TP-B854 ON _SUX	+ WRT GATE
CH 2	2.0 V/CM	TP-E556 ON _SUX	- WRT ENABLE

TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
+ INT CH 1		

SCOPE GND TO GND ON LOGIC CARD.
USE XIO PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 0.1 MS/CM MODE: ALT

NOTES:

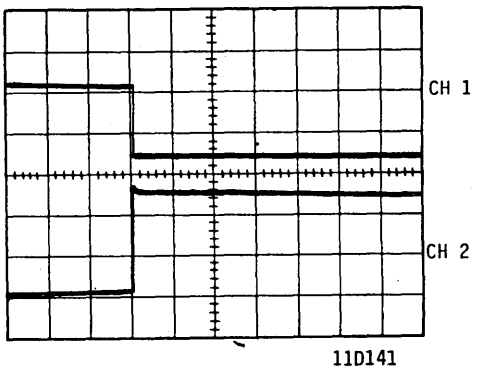


Figure 4-10. Write Gate Timing

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	0.5 V/CM	TP-C736 ON _SUX	+ WRT DATA (NRZ)
CH 2	0.5 V/CM	TP-C838 ON _SUX	+ WRT CLK

TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
-EXT	TP-E556	-WRT ENABLE

SCOPE GND TO GND ON LOGIC CARD.
USE XIO PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 50 NS/CM **MODE:** ALT

NOTES:

1. DISREGARD ANY GHOST IMAGES.

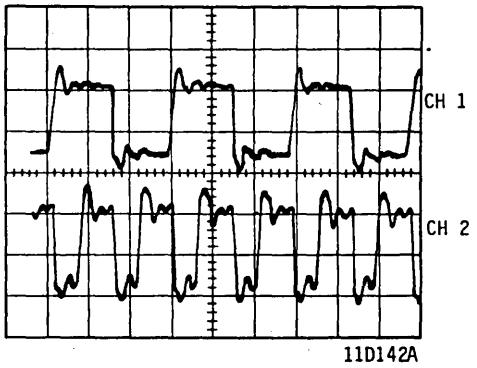


Figure 4-11. Write Data to Clock Timing

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	0.5 V/CM	TP-E042 ON _SUX	+ WRT DATA COMP
CH 2	0.5 V/CM	TP-C433 ON _SUX	+ 2F (WRT OSC)

TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
+ INT CH 1		

SCOPE GND TO GND ON LOGIC CARD.
USE XIO PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 0.05 µS/CM **MODE:** ALT

NOTES:

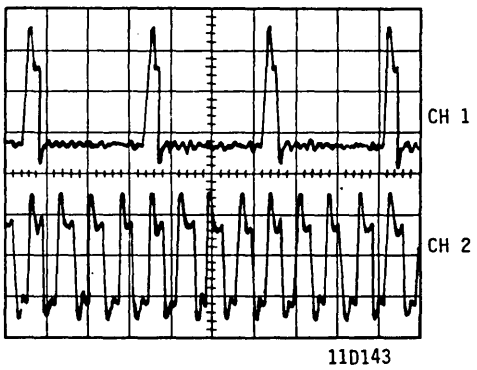


Figure 4-12. Compensated Write Data Timing

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	0.5 V/CM	TP-E042 ON _SUX	+ WRT DATA (COMP)
CH 2	0.5 V/CM	CHIP G432-15 ON _SUX	+ WRT DATA

TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
+ INT CH 1		

SCOPE GND TO GND ON LOGIC CARD.
USE XIO PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: .05 µS/CM MODE: ALT

NOTES:

1. DISREGARD ANY GHOST IMAGES.

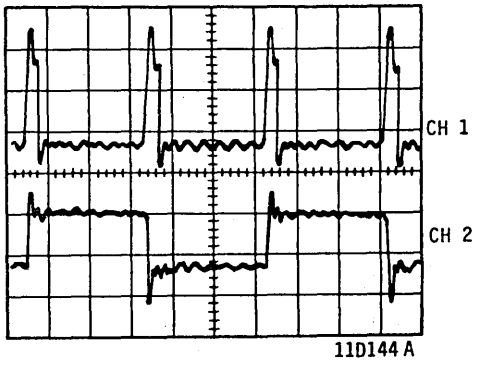


Figure 4-13. Write Toggle Output

4304 - WRITE ADDRESS MARK CHECK

This procedure verifies that the drive is not writing data during the time that Address Mark Enable is active.

CAUTION

To avoid possible loss of customer data, select a cylinder and head that will result in data being written on an unused track.

1. Command continuous write format with address mark operations using a 1010... data pattern.
2. Connect oscilloscope as shown on figure 4-14.
3. Observe that there are no data "1" pulses during the time that Address Mark Enable is Active.
4. Proceed to next test or return drive to system operation.

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	2.0 V/CM	TP-C644 ON _SUX	- AM ENABLE
CH 2	0.5 V/CM	TP-E042 ON _SUX	+ WRT DATA (COMP)

TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
+INT CH 1		

SCOPE GND TO GND ON LOGIC CARD.
USE X10 PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 0.5 µS/CM MODE: ALT

NOTES:

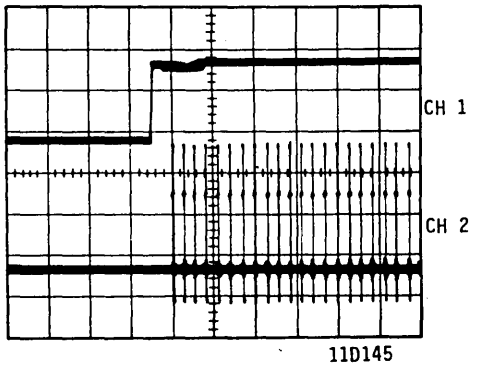


Figure 4-14. Write Address Mark Timing

READ CHECKS

The following procedures, 4401 through 4404, check various aspects of drive read circuit operation. Figure 4-15 is a block diagram showing the major components in the read circuits and the test points used in the procedures.

4401 - READ PLO CHECK

This procedure checks the operation of the read PLO circuits (see figure 4-15). The read PLO provides timing signals used during read operations.

1. Connect oscilloscope as shown on figure 4-16 and observe that 2F (Read Oscillator) frequency is approximately 29.01 MHz.

2. Connect oscilloscope as shown on figure 4-17 and observe that the + Pump Up and + Pump Down signals are coincident.

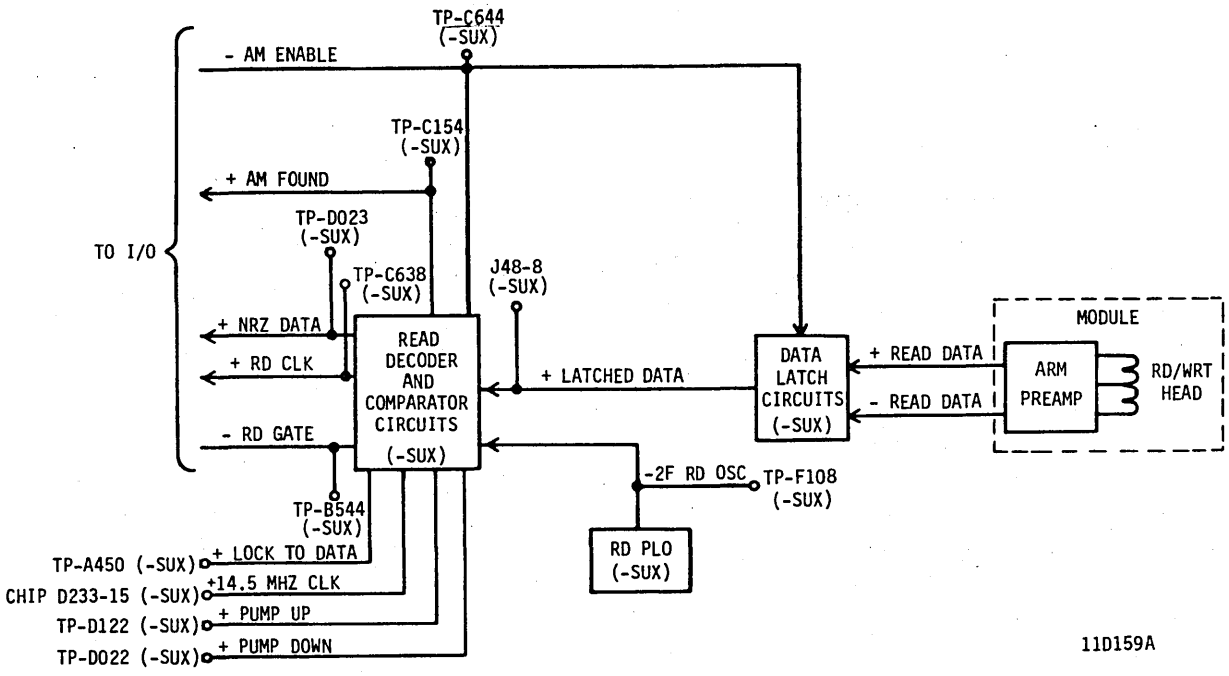


Figure 4-15. Read Circuits Test Points

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	0.5 V/CM	TP-F108 ON _SUX	- 2F RD OSC
CH 2			

TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
- INT CH 1		

SCOPE GND TO GND ON LOGIC CARD.
USE XIO PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 20 NS/CM **MODE:**

NOTES:

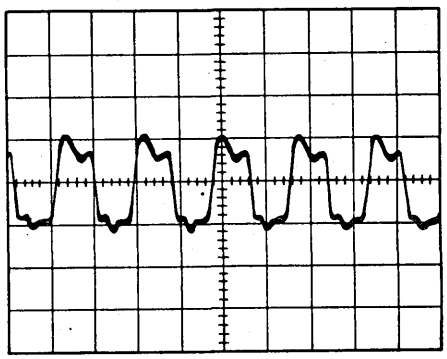


Figure 4-16. 2F (Read Oscillator) Timing

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	0.5 V/CM	TP-D122 ON _SUX	+ PUMP UP
CH 2	0.5 V/CM	TP-D022 ON _SUX	+ PUMP DOWN

TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
+ INT CH 1		

SCOPE GND TO GND ON LOGIC CARD.
USE X10 PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 50 NS/CM MODE: ALT

NOTES:

1. MEASUREMENT IS ONLY VALID IF DRIVE IS NOT READING.
2. OBSERVE THAT CH 1 AND CH 2 SIGNALS ARE COINCIDENT.

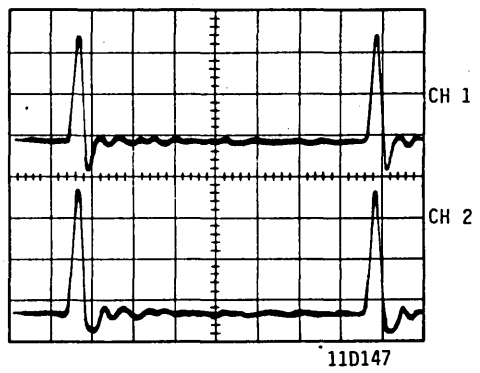


Figure 4-17. Pump Up/Down Timing (Not Reading)

CAUTION

To avoid possible loss of customer data, select a cylinder and head that will result in data being written on an unused track.

3. Command drive to write a 1010... pattern using desired head.
4. Command drive to perform continuous read operations.
5. Observe that + Pump Up and + Pump Down signals have the same timing relationship shown on figure 4-18.
6. Proceed to next test or return drive to system operation.

4402 - READ DATA CHECK

This procedure checks the operation of the heads, preamplifier, data latch, read comparator, and 2-7 decoder circuits.

1. Perform Write Data Check (proc 4303).
2. Perform Read PLO Check (proc 4401).

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	0.5 V/CM	TP-D122 ON _SUX	+ PUMP UP
CH 2	0.5 V/CM	TP-D022 ON _SUX	+ PUMP DOWN

TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
+ INT CH 1		

SCOPE GND TO GND ON LOGIC CARD.
USE X10 PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 50 NS/CM MODE: ALT

NOTES:

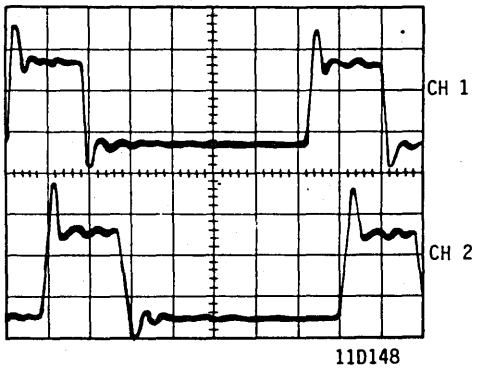


Figure 4-18. Pump Up/Down Timing (Reading)

CAUTION

To avoid possible loss of customer data, select a cylinder and head that will result in data being written on an unused track.

3. Command drive to seek to desired cylinder and select desired head.

4. Command drive to write a 1010... pattern and then to perform continuous read operations.

5. Check the Latched Read Data signal and its timing relationship with the 2F (Read Oscillator) signal.

   a. Connect and set up oscilloscope as shown on figure 4-19.

   b. Observe that 2F (Read Oscillator) pulses occur approximately in center of latched Read Data pulses.

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	0.5 V/CM	TP-J48-08 ON _SUX	+ LATCHED READ DATA
CH 2	0.5 V/CM	TP-F108 ON _SUX	- 2F READ OSC

TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
+INT CH 1		

SCOPE GND TO GND ON LOGIC CARD.
USE X10 PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 20 NS/CM MODE: ALT

NOTES:

1. DISREGARD ANY GHOST IMAGES.

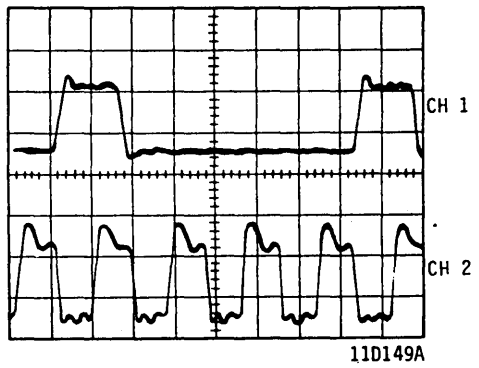


Figure 4-19. Latched Read Data Timing

6. Check Read Data to Read Clock timing.

   a. Connect oscilloscope as shown on figure 4-20 and observe that Read Clock frequency is approximately 14.5 MHz.

   b. Observe that Read Data to Read Clock timing is approximately as shown. Read Clock should go positive approximately at the center of the data "1" pulses.

   c. Observe that the NRZ data has a 1010... pattern.

7. Check Read Gate to Lock to Data timing.

   a. Connect oscilloscope as shown as shown on figure 4-21.

   b. Observe that +Lock to Data goes low at the proper time (see figure 4-21).

8. Proceed to next test or return drive to system operation.

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	0.5 V/CM	TP-D023 ON _SUX	+ NRZ READ DATA
CH 2	0.5 V/CM	TP-C638 ON _SUX	+ READ CLOCK

TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
+ INT CH 1		

SCOPE GND TO GND ON LOGIC CARD.
USE XIO PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 50 NS/CM MODE: ALT

NOTES:

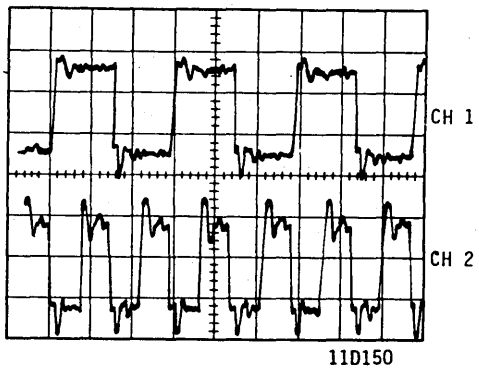


Figure 4-20. NRZ Read Data Timing

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	2.0 V/CM	TP-B544 ON _SUX	- READ GATE
CH 2	2.0 V/CM	TP-A450 ON _SUX	+ LOCK TO DATA

TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
- INT CH 1		

SCOPE GND TO GND ON LOGIC CARD.
USE XIO PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 1 µS/CM MODE: ALT

NOTES:

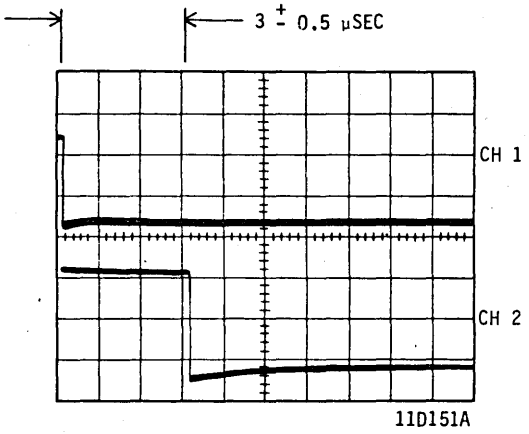


Figure 4-21. Read Gate to Lock to Data Timing

4403 - READ ADDRESS MARK CHECK

This procedure checks for the presence of address marks and verifies that the timing is correct.

CAUTION

To avoid possible loss of customer data, select a head and cylinder that will result in data being written on an unused track.

1. Command a write format in address mark mode using a 1010.. pattern. Then command a continuous read address mark operation.

2. Connect oscilloscope as shown on figure 4-22.

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	0.5 V/CM	TP-J48-8 ON _SUX	+ LATCHED READ DATA
CH 2	2.0 V/CM	TP-C154 ON _SUX	+ ADDRESS MARK FOUND

TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
+ EXT	TP-J81-2 ON _SYX/_TQX	+ INDEX

SCOPE GND TO GND ON LOGIC CARD.
USE X10 PROBES UNLESS OTHERWISE NOTED.

A TIME/DIV: 5 MS/CM MODE: ALT

B TIME/DIV: 0.5 μS/CM

NOTES:

1. SET HORIZONTAL DISPLAY TO "A" INTENSIFIED AND ADJUST DELAY TIME MULTIPLIER TO MOVE MARKER TO ADDRESS MARK.

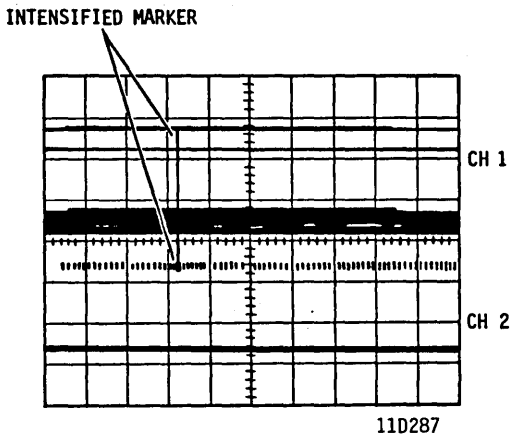


Figure 4-22. Scope Setup for AM Found Timing

NOTE

In "A Intensified" horizontal mode, the brightened marker highlights the segment of the sweep that is displayed later in "B Delayed" horizontal mode.

3. Adjust DELAY TIME MULTIPLIER on oscilloscope to move intensified marker into data pattern (see figure 4-22). To minimize display instability, use first address mark area following index.

4. Referring to figure 4-23 position oscilloscope HORIZ DISPLAY switch to B DELAYED and TRIGGERING to +EXT.

5. Check that the length of the address mark area is within the limits shown on figure 4-23. If it is outside these limits the address mark detection circuits may not function properly.

6. Observe that Address Mark Found goes active immediately following the address mark area.

7. Connect oscilloscope as shown on figure 4-24.

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	0.5 V/CM	TP-J48-8 ON _SUX	+ LATCHED READ DATA
CH 2	2.0 V/CM	TP-C154 ON _SUX	+ ADDRESS MARK FOUND

TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
+ EXT	TP-J81-2 ON _SYX/_TQX	+ INDEX

SCOPE GND TO GND ON LOGIC CARD.
USE X10 PROBES UNLESS OTHERWISE NOTED.

A TIME/DIV: 2 MS/CM MODE: ALT.
B TIME/DIV: 0.5 µS/CM

NOTES:

1. SET HORIZONTAL DISPLAY TO "B" (DELAYED) AND ADJUST DELAY MULTIPLIER AS REQUIRED.

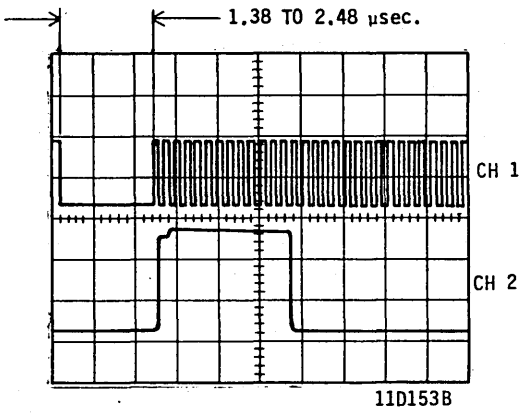


Figure 4-23. AM Found Timing

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	2.0 V/CM	TP-C644 ON _SUX	- AM ENABLE
CH 2	2.0 V/CM	TP-A450 ON _SUX	+ LOCK TO DATA

TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
- INT CH 1		

SCOPE GND TO GND ON LOGIC CARD.
USE X10 PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 1 µS/CM MODE: ALT

NOTES:

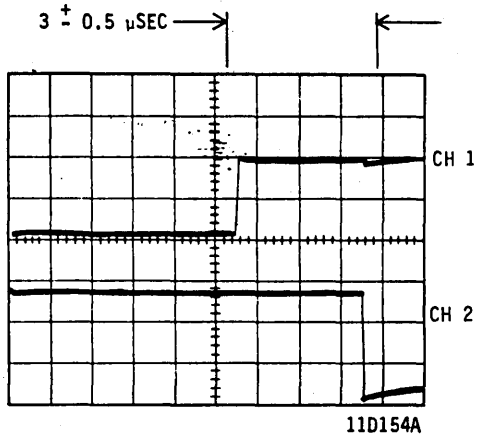


Figure 4-24. AM to Lock To Data Timing

8. Observe that +Lock to Data goes active at the proper time (see figure 4-24).

9. Proceed to next test or return drive to system operation.

MISCELLANEOUS LOGIC CHECKS

4501 - INDEX CHECK

This procedure checks that Index is present and has the proper pulse width. It also checks the time between successive Index pulses which is an indication of disk rotational speed.

1. Connect oscilloscope as shown on figure 4-25.

2. Observe that the Index pulse width is between 2.2 and 2.8 microseconds.

3. Connect oscilloscope as shown on figure 4-26.

4. Observe that the time between Index pulses is between 27.4 and 28.4 milliseconds.

5. Proceed to next test or return drive to system operation.

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	2.0 V/CM	TP-J81-2 ON _SYX/_TQX	+ INDEX
CH 2			

TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
+ INT CH 1		

SCOPE GND TO GND ON LOGIC CARD.
USE XIO PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 0.5 µS/CM. MODE:

NOTES:

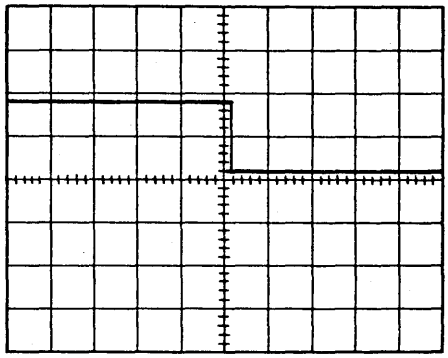


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Figure 4-25. Index Pulse Timing

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	2.0 V/CM	TP-J81-2 ON _SYX/_TQX	+INDEX
CH 2			

TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
+ INT CH 1		

SCOPE GND TO GND ON LOGIC CARD.
USE XIO PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 5 MS/CM MODE:

NOTES:

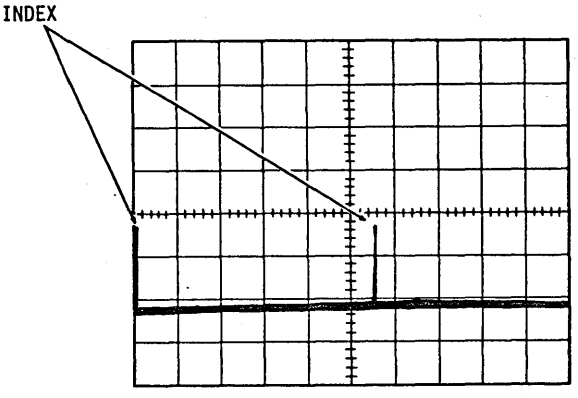

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Figure 4-26. Index to Index Timing

4502 - SECTOR CHECK

This procedure checks for the presence of sector pulses and that they have the proper width.

1. Connect oscilloscope as shown on figure 4-27.
2. Observe that the Sector pulse width is between 1.05 and 1.45 microseconds.
3. Proceed to next test or return drive to system operation.

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	2.0 V/CM	TP-J80-5 ON _VDX	+ SECTOR
CH 2			

TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
+INT CH 1		

SCOPE GND TO GND ON LOGIC CARD.
USE XIO PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 0.5 µS/CM **MODE:** CHAN. 1

NOTES:

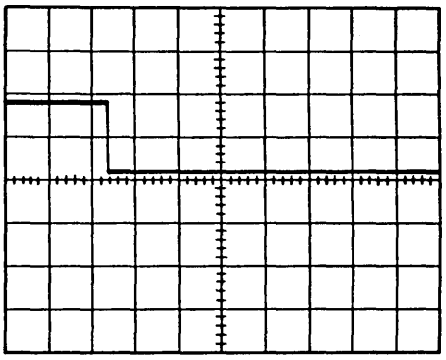


Figure 4-27. Sector Pulse Timing

SECTION 5

REPAIR AND REPLACEMENT

CAUTION

When servicing the drive, observe all precautions listed under Electrostatic Discharge Protection in section 2 of this manual. Failure to observe these precautions can result in serious damage to electronic assemblies.

INTRODUCTION

Repair of the drive is limited to replacement of defective parts and assemblies. This section describes removal and replacement and, where applicable, adjustment of all major field replaceable parts and assemblies. The information here should be used in conjunction with that in the parts data section of hardware maintenance volume 1.

If adjustments are required as a result of replacing a part, it is specified in the replacement procedure. If an adjustment is included, and there is some doubt as to the need for replacement, perform the adjustment prior to replacing the part.

The procedures in this section assume that the drive is mounted on slides in an equipment rack or cabinet. But unless otherwise specified, it is not necessary to remove the drive from the slides to perform maintenance. All procedures require that power be removed from the drive. The person performing the maintenance should be thoroughly familiar with the operation of the drive and with all information in the general maintenance section of this manual (particularly warnings and precautions).

Each procedure is assigned a unique number. The numbers are used elsewhere in the manual to reference the procedures. The procedures and numbers are organized into three categories: 51XX - mechanical, 52XX - electromechanical, and 53XX - electronic (circuit boards).

- 5101 - Entire Drive Removal & Replacement
- 5102 - Top Cover Removal & Replacement
- 5103 - Front Panel Removal & Replacement
- 5104 - Slide Removal & Replacement

- 5105 - Drive Belt Removal & Replacement
- 5201 - Fan Removal & Replacement
- 5202 - Operator Panel (_PBX) Removal & Replacement
- 5203 - Fault Display (_UQX) Removal & Replacement
- 5204 - Motor and Brake Assembly Removal & Replacement
- 5205 - Brake Removal, Replacement & Adjustment
- 5206 - Drive Motor Removal & Replacement
- 5207 - Power Supply Removal & Replacement
- 5208 - Unlocking Solenoid Coil Removal & Replacement
- 5209 - Module Removal & Replacement
- 5210 - Cable Replacement
- 5301 - _VDX Board Removal & Replacement
- 5302 - _SUX Board Removal & Replacement
- 5303 - _TSX Board Removal & Replacement
- 5304 - _UCX Board Removal & Replacement
- 5305 - _SYX/_TQX I/O Board Removal & Replacement
- 5306 - _TRX Mother Board Removal & Replacement
- 5307 - Drive Electronics Assembly Removal & Replacement
- 5308 - _RTX Relay Board Removal & Replacement
- 5309 - _WFV Regulator Board Removal & Replacement

5101 - ENTIRE DRIVE REMOVAL & REPLACEMENT

The following procedure provides instructions for removing and replacing the entire drive and assumes that the drive is mounted on slides in an equipment rack. Because of the weight involved, three or more persons should work together to lift the drive on and off the slide assemblies.

When removing a drive and replacing it with another drive from the factory, refer to section 3 in maintenance manual, volume 1, for information about packaging, unpackaging, and installation.

REMOVAL

1. Gain access to rear of drive, and disconnect power cord, I/O cables, ground cables and terminators from drive.

2. Remove front panel insert, release front panel latch, and pull drive forward until it locks in the fully extended position.

3. Remove mounting screws that secure drive to slides. Some screws must be removed through openings in intermediate slides. It is necessary to unlock the fully extended slides and push drive partially into rack to gain access to some of these screws.

4. Lift drive off slides.

5. Move drive to desired location.

REPLACEMENT

1. At the equipment rack, pull both slide assemblies to their fully extended position, making certain that each slide locks in position.

2. Place drive onto slide assemblies and ensure that the J bracket is engaged with the inner slide along its full length on both sides before releasing external support.

3. Carefully slide drive towards rack until front mounting holes in slide assemblies are aligned with front mounting holes in J brackets on drive.

4. Secure inner slides to drive by installing mounting screws into the eight holes provided (four holes on each side). Begin by installing screws into front mounting holes aligned during step 3. Tighten these screws securely. Three additional mounting holes on each side are accessible through openings in intermediate slides. It is necessary to unlock the fully extended slides and push drive partially into rack to gain access to some mounting holes through these openings. Install screws into all remaining mounting holes and tighten securely.

5. Unlock slide assemblies and push drive back to closed position in rack.

6. Gain access to rear of drive, and connect power cable, I/O cables, ground cables, and terminators to drive connectors. See hardware maintenance manual volume 1 for desired system cabling.

5102 - TOP COVER REMOVAL & REPLACEMENT

REMOVAL

CAUTION

With the top cover removed, electrostatic sensitive components are exposed and may be seriously damaged by static electricity. To avoid possible damage, observe all precautions listed under Electrostatic Discharge Protection in section 2 of this manual.

1. Remove power from drive as follows:

   a. Press START switch to release it from start position.

   b. Wait for READY indicator to stop flashing, and then gain access to rear of drive and set CB1 to OFF.

2. Gain access to rear of drive and remove screws securing cover to rear panel.

3. Remove front panel insert, release front panel latch, and pull drive forward until it locks in the fully extended position.

4. Remove all remaining screws securing cover to drive.

CAUTION

Cover must be carefully lifted off the drive to avoid possible damage to internal components adjacent to the cover.

5. Lift off cover.

REPLACEMENT

CAUTION

When replacing cover, use care to avoid damaging logic boards or other components.

1. Place cover on drive.

2. Install screws that fasten cover to top of drive (and on older units, to side of drive). Tighten screws securely.

3. Unlock slide assemblies and push drive back to closed position in rack.

4. Gain access to rear of drive and install screws that fasten cover to rear panel. Tighten screws securely.

5103 - FRONT PANEL ASSEMBLY REMOVAL & REPLACEMENT

REMOVAL

1. Remove power from drive as follows:

   a. Press START switch to release it from start position.

   b. Wait for READY indicator to stop flashing, then set CB1 to OFF.

2. Remove front panel insert (see figure 5-1) by pulling forward to disengage catches that hold insert in front panel.

3. Release front panel latch and slide drive out of rack far enough to permit access to mounting screws at rear of front panel.

4. Remove all screws securing front panel to front panel support and lift panel off drive.

REPLACEMENT

1. Place front panel on front panel support.

2. Align mounting holes in front panel with holes in front panel support, insert screws into holes at both the front and rear of front panel, and tighten securely.

3. Push drive back to closed position within rack.

4. Replace front panel insert by aligning catches to slots in front panel and pushing on insert until catches snap into place.

5104 - SLIDE REMOVAL & REPLACEMENT

The following procedure describes how to remove and replace slide assemblies. This procedure is used to replace a defective slide assembly or, if slide assemblies must be moved from one rack to another.

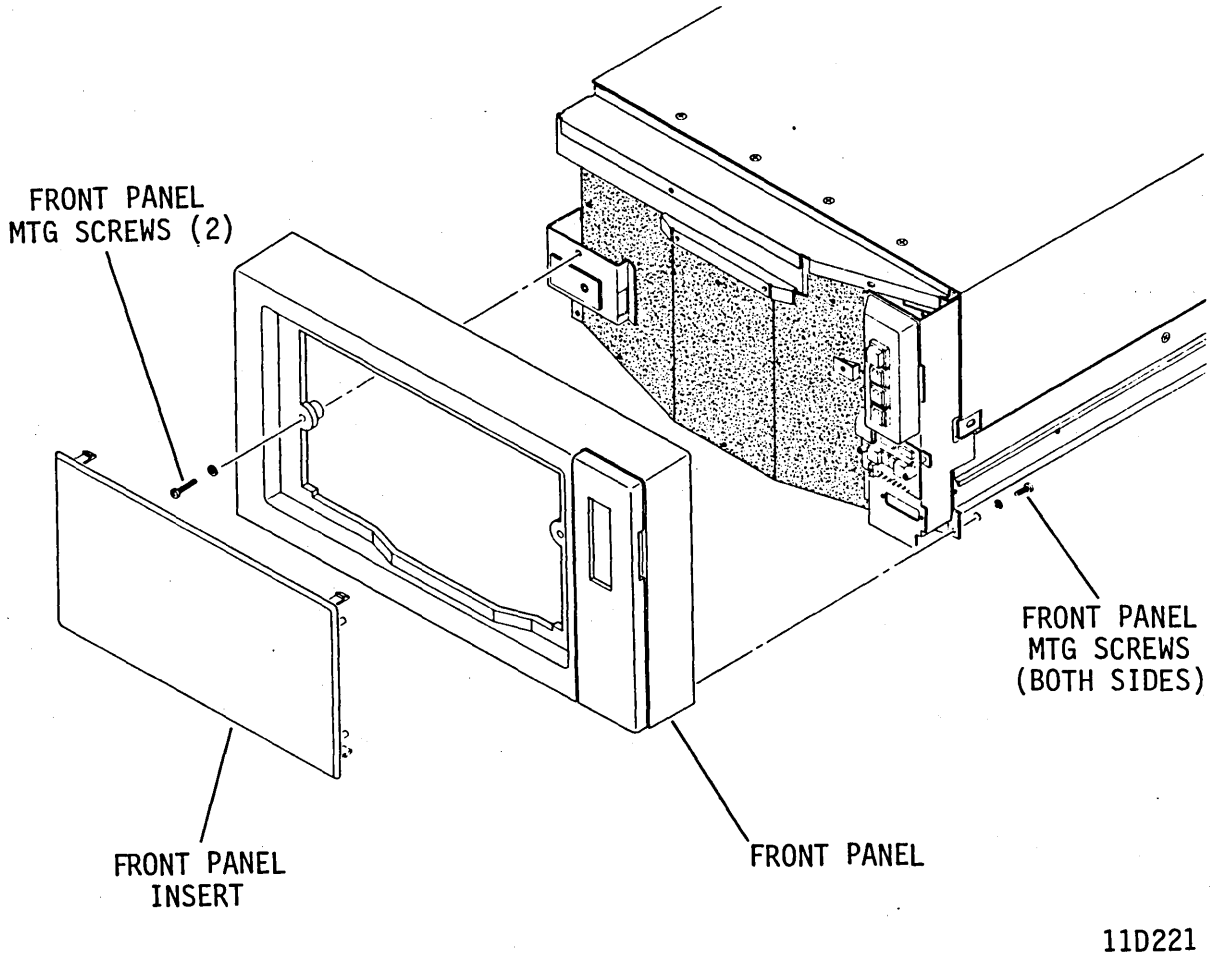
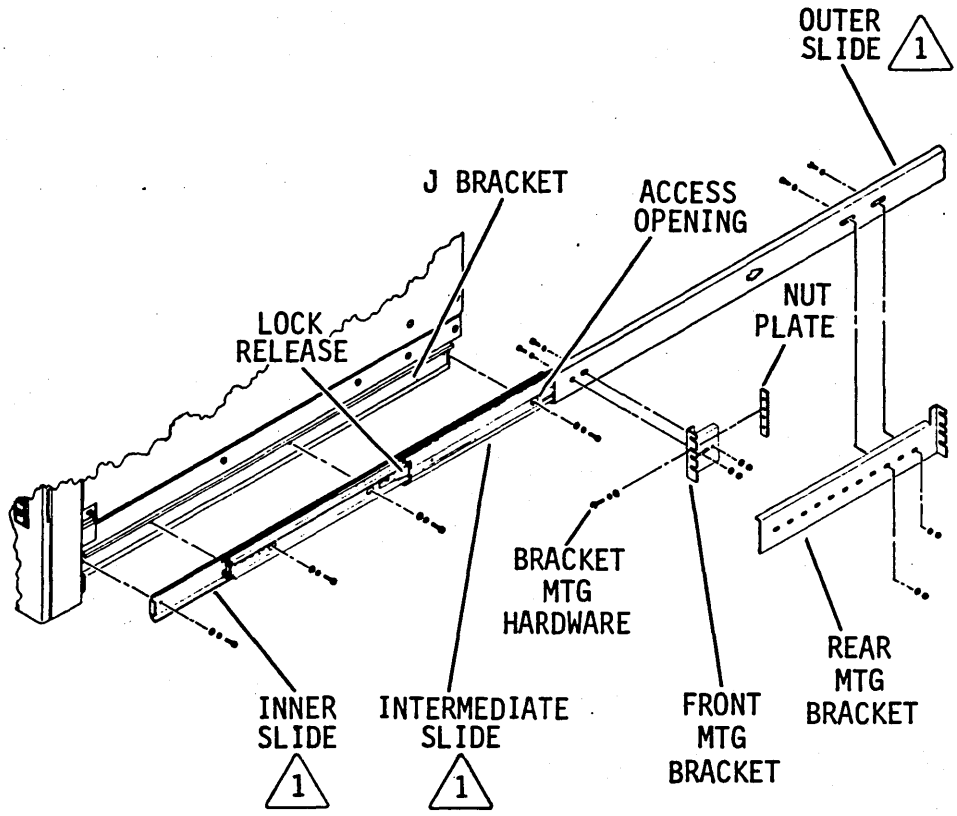


Figure 5-1. Front Panel Removal & Replacement

REMOVAL

1. Perform entire drive removal procedure (5101).
2. Unlock slide assemblies and push them into rack to their fully retracted position.
3. Remove screws securing slide assembly mounting brackets to rack and remove mounting brackets (with slide assemblies attached) from rack (see figure 5-2).



NOTES:

1. USE THESE PARTS LOCATIONS TO DIFFERENTIATE BETWEEN RIGHT HAND AND LEFT HAND SLIDES.

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Figure 5-2. Slide Removal & Replacement

REPLACEMENT

1. Loosely attach screws, lockwashers, and nut plates to appropriate holes in rack.

2. Loosely attach, or loosen already attached, screws that fasten front and rear mounting brackets to slide assemblies and adjust spacing between brackets to allow installation in rack.

3. Position slide assemblies in rack and tighten hardware securing them to rack. Figure 5-2 defines which slide assembly is used on right-hand side of rack.

4. Tighten screws that fasten mounting brackets to slide assemblies.

5. Perform entire drive replacement procedure (5101).

5105 - DRIVE BELT REMOVAL & REPLACEMENT

CAUTION

Damage to the disks and/or heads may occur if the disks within the module are allowed to rotate in either direction during drive belt removal and replacement. For this reason, install the spindle shipping lock prior to removing the drive belt.

REMOVAL

1. Perform top cover removal procedure (5102).

2. Remove spindle access cover and install spindle shipping lock (refer to installation section of maintenance manual volume 1).

3. Push on side of drive motor to compress belt tension spring and slide drive belt off motor and module pulleys.

REPLACEMENT

1. Push on side of drive motor to compress belt tension spring and slide drive belt onto motor and module pulleys.

2. Remove spindle shipping lock (refer to installation section of maintenance manual volume 1) and install spindle access cover.

3. Perform top cover replacement procedure (5102).

5201 - FAN REMOVAL & REPLACEMENT

REMOVAL

1. Perform top cover removal procedure (5102).

2. Remove screws securing rear panel to power supply enclosure along top edge.

3. Unlock slide assemblies and push drive back to closed position in rack.

4. Gain access to rear of drive and remove remaining screws securing rear panel to power supply enclosure. Tilt panel downward to permit fan removal.

5. Remove power wiring from slide-on terminals on fan.

6. Remove screws securing finger guard and fan to drive. Remove guard and fan.

REPLACEMENT

CAUTION

Installing fan backwards will result in improper airflow, which will cause overheating and premature component failure.

1. Orient replacement fan so power terminals are on lower right when facing rear of drive (see figure 5-3). Power terminals will extend upwards when the fan is positioned correctly.

2. Align fan to inside and finger guard to outside of rear panel. Attach with screws and tighten securely.

3. Connect two wires coming from fuseholders F1 and F2 to slide-on terminals on fan. On some units these wires may be terminated in a one piece connector that must be connected to fan terminals.

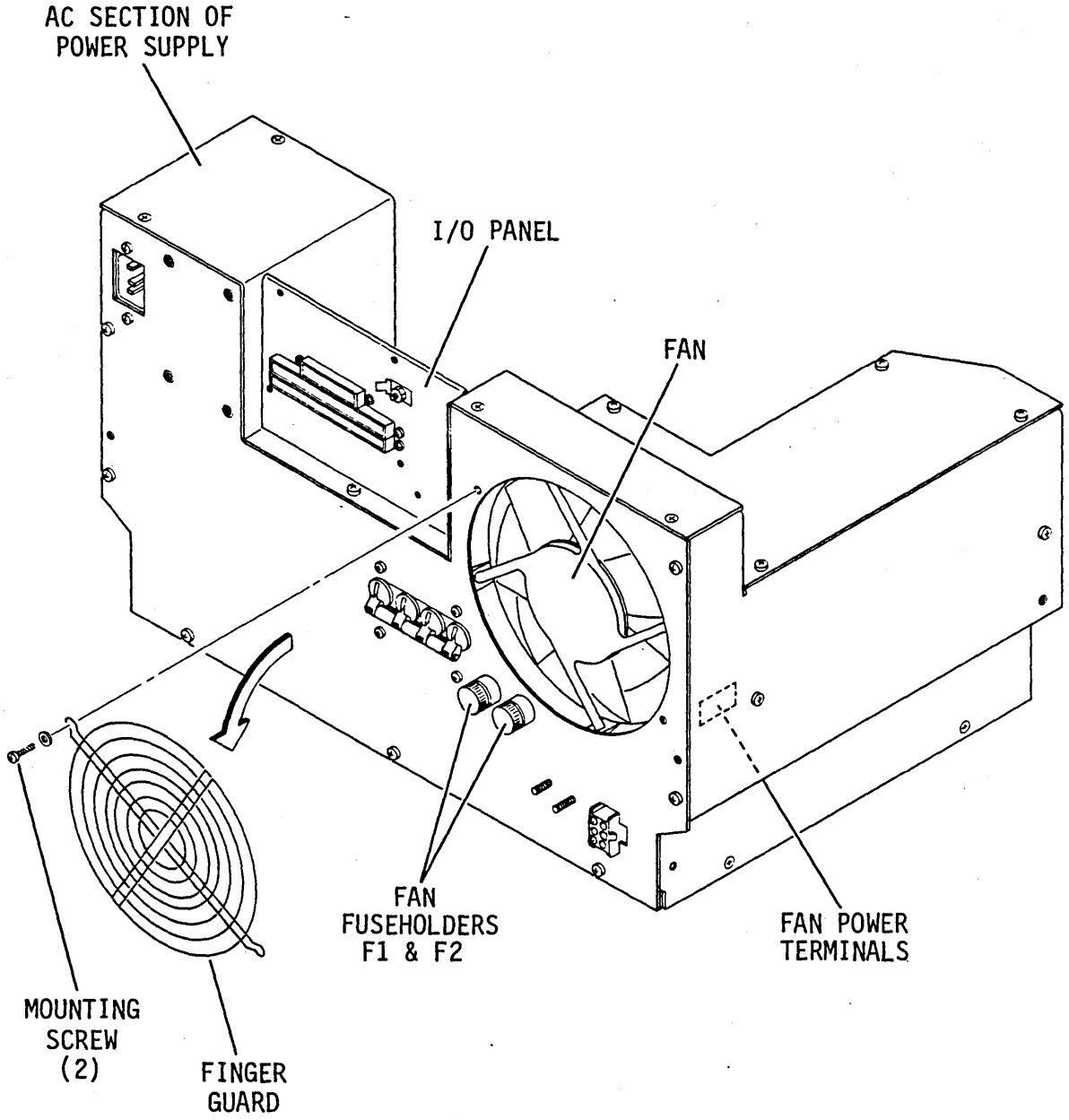


Figure 5-3. Fan Removal & Replacement

4. Lift rear panel back into place, install mounting hardware, and tighten securely.

5. Perform top cover replacement procedure (5102).

5202 - OPERATOR PANEL (-PBX) REMOVAL & REPLACEMENT

The operator panel (see figure 5-4) cannot be repaired and, except for the lenses, must be replaced as an assembly. The lenses can be replaced separately and are removed by carefully prying them from the switches (see figure 5-4). The following procedure describes removal and replacement of the operator panel.

REMOVAL

1. Perform top cover and front panel removal procedures (proc 5102, 5103).

2. Remove top cover from front panel support.

3. Disconnect P26 from J26 (on _VDX board) and remove cable from cable clips along top edge of front panel support.

4. Remove screws securing switch bracket to front panel support and lift bracket, with operator panel and cable attached, from drive.

5. Depress retainer springs on operator panel and snap it out of bracket.

REPLACEMENT

1. Thread P26 and cable through bracket and holes in front panel support.

2. Snap operator panel into place in switch bracket.

3. Loosely attach switch bracket to drive with screws and push downward on bracket while tightening screws.

4. Connect P26 to J26 (on _VDX board) and secure cable in cable clips along top edge of front panel support.

5. Install top cover on front panel support.

6. Perform top cover and front panel replacement procedures (proc. 5102, 5103).

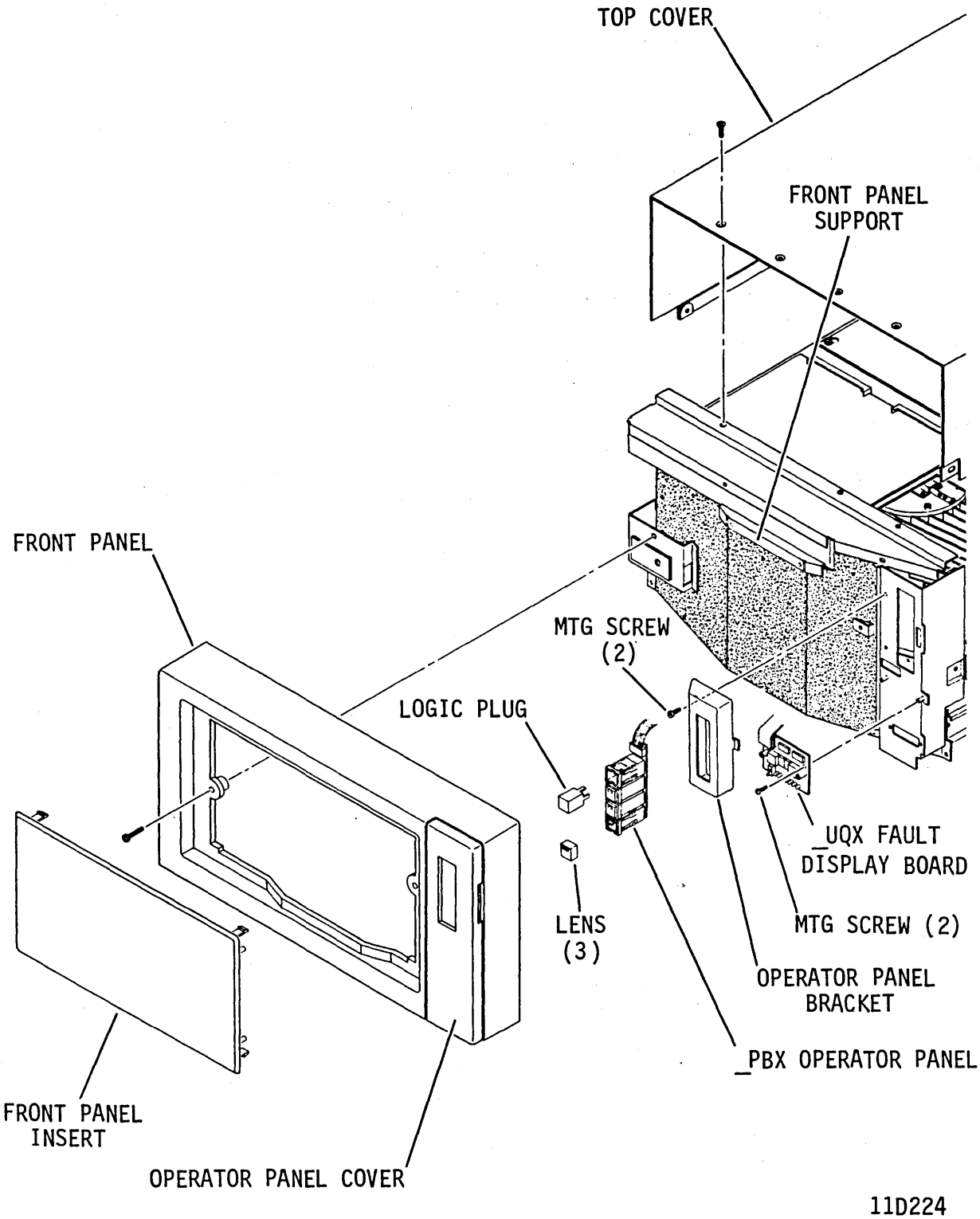


Figure 5-4. _PBX Operator Panel and _UQX Fault Display Removal & Replacement

5203 - FAULT DISPLAY (—UQX) REMOVAL & REPLACEMENT

The following procedure describes removal and replacement of the fault display board (see figure 5-4).

REMOVAL

1. Perform top cover and front panel removal procedures (proc. 5102, 5103).
2. Remove top cover from front panel support.
3. Disconnect P13 from J13 (on _VDX board) and remove cable from cable clips.
4. Remove screws securing fault display board (_UQX) to chassis and lift board, with cable attached, from drive.

REPLACEMENT

1. Thread P13 and cable through holes in front panel support.
3. Secure fault display board (_UQX) to drive with screws.
4. Connect P13 to J13 (on _VDX board) and secure cable in cable clips.
5. Install top cover on front panel support.
6. Perform top cover and front panel replacement procedures (proc. 5102, 5103).

5204 - MOTOR AND BRAKE ASSEMBLY REMOVAL & REPLACEMENT

This procedure describes how to replace the drive motor and brake as an assembly including the pulley and hanger (refer to figure 5-5). To remove & replace brake or drive motor separately, refer to procedures 5205 or 5206.

REMOVAL

1. Perform top cover removal procedure (5102).
2. Perform drive electronics assembly removal procedure (5307).

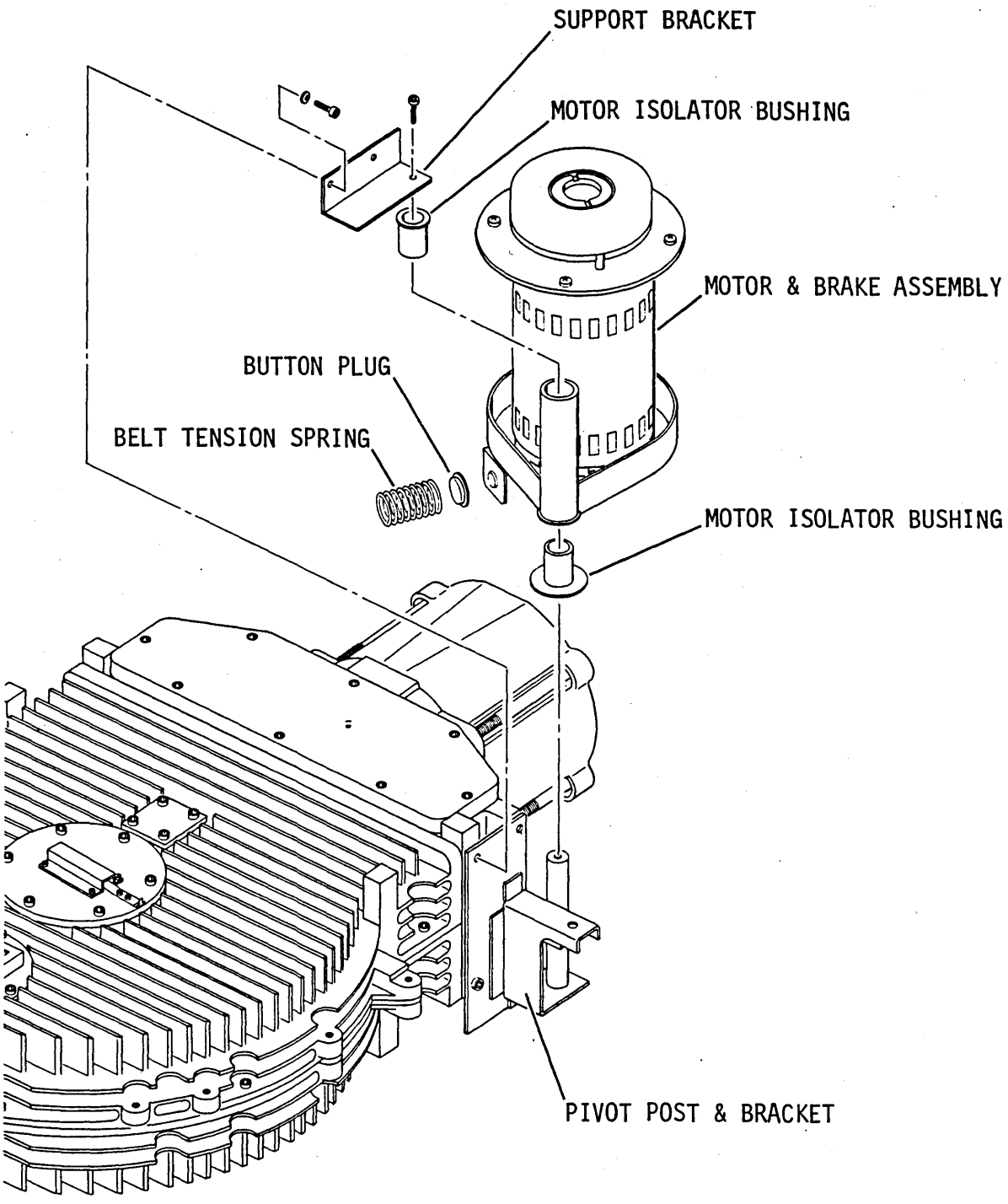


Figure 5-5. Motor and Brake Assembly Removal & Replacement

3. Disconnect drive motor cable from J60 and brake cable from J61 on power supply.

4. Remove start capacitor from clamp on side of drive. Remove end cap from capacitor, and disconnect wires from terminals. Cut tie wraps as necessary and pull wires free to allow removal from drive with motor.

5. Perform drive belt removal procedure (5105).

WARNING

Injury may result if the belt tension spring is not gripped securely during the following compression and removal procedure.

6. Remove belt tension spring by compressing it and sliding it out from between brackets.

7. Remove screws securing drive motor support bracket to module and to top of drive motor hanger pivot post. Remove the support bracket.

8. Lift drive motor and brake assembly out of drive. If motor isolator bushing remains on motor hanger pivot post, lift off and insert into bottom opening on motor hanger.

REPLACEMENT

1. Ensure motor isolator bushings are in place at top and bottom openings on motor hanger. Place drive motor and brake assembly onto pivot post.

2. Place the support bracket between the module and the top of the motor hanger pivot post. Insert mounting screws and tighten securely.

WARNING

Injury may result if the belt tension spring is not gripped securely during the following compression and replacement procedure.

3. Replace belt tension spring by compressing and sliding it into place between brackets.

4. Perform drive belt replacement procedure (5105).

5. Route drive motor wires with slide-on connectors to motor start capacitor clamp and replace cable ties removed during motor removal. Install wires onto capacitor terminals, replace capacitor end cap, and insert capacitor into clamp.

6. Connect drive motor cable to J60 and brake cable to J61 on power supply.

7. Perform drive electronics assembly replacement procedure (5307).

8. Perform top cover replacement procedure (5102).

5205 - BRAKE REMOVAL, REPLACEMENT & ADJUSTMENT

The hexagonal brake hub on the drive motor shaft (see figure 5-6) must be replaced and adjusted when the brake is replaced. Spacing between the brake hub and adaptor plate on the upper end of the motor must be adjusted as described in the adjustment procedure.

CAUTION

Damage to the disks and/or heads may occur if the disks within the module are allowed to rotate in either direction during brake removal, replacement, and adjustment. For this reason, install the spindle shipping lock prior to removing the drive belt (refer to drive belt removal and replacement procedure 5105).

REMOVAL

1. Perform top cover removal procedure (5102).

2. Perform drive belt removal procedure (5105).

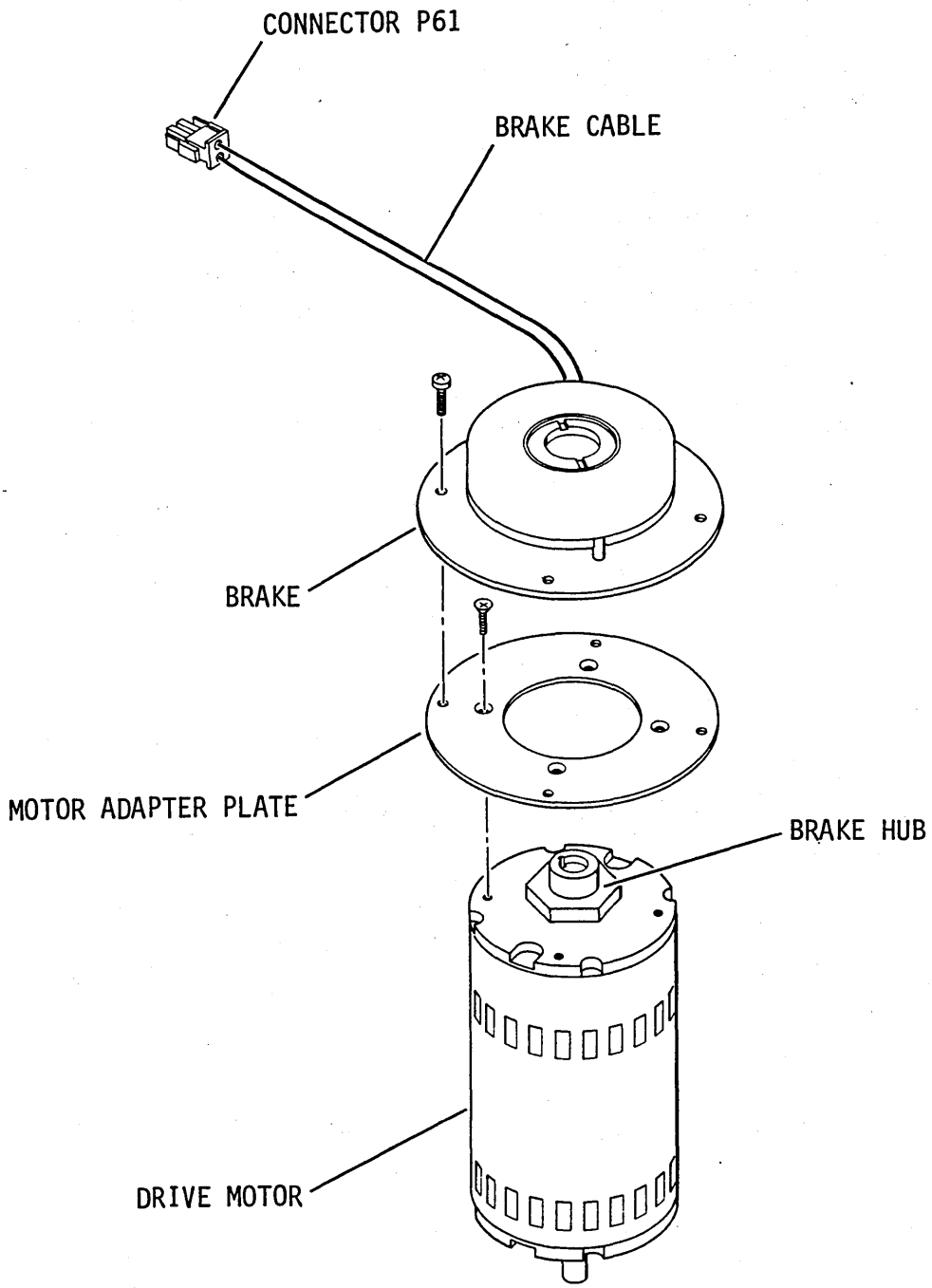


Figure 5-6. Brake Removal & Replacement

3. Perform drive electronics assembly removal procedure (5307).

4. Disconnect cable from J61 on power supply.

5. Remove screws attaching brake to adaptor plate on top of drive motor and lift off brake.

CAUTION

When set screws are loose and the brake hub is being removed, the key between the brake hub and the motor shaft can fall into the drive motor. Use care to prevent this from happening.

6. Loosen set screws securing hexagonal brake hub to drive motor shaft and slide brake hub and key off shaft.

REPLACEMENT

1. Slide hexagonal brake hub onto drive motor shaft and perform hub adjustment procedure described below, starting with step 4.

2. Place brake assembly over drive motor shaft and onto adaptor plate.

3. Rotate brake assembly to align mounting holes with those in adaptor plate, then install and tighten mounting screws.

4. Connect brake cable to J61 on power supply.

5. Perform drive electronics assembly replacement procedure (5307)

6. Perform drive belt replacement procedure (5105).

7. Perform top cover replacement procedure (5102).

ADJUSTMENT

1. Perform top cover removal procedure (5102).

2. Perform brake removal procedure described above.

3. Loosen set screws securing hexagonal brake hub to drive motor shaft.

CAUTION

When set screws are loose, it is possible for the key between the brake hub and the motor shaft to fall down far enough to contact top of drive motor. Make certain the key does not extend beyond the bottom surface of brake hub when the following adjustment is complete.

4. Place brake hub gauge plate (see general maintenance section for part number) between drive motor adaptor plate and hexagonal brake hub on drive motor shaft as shown in figure 5-7.

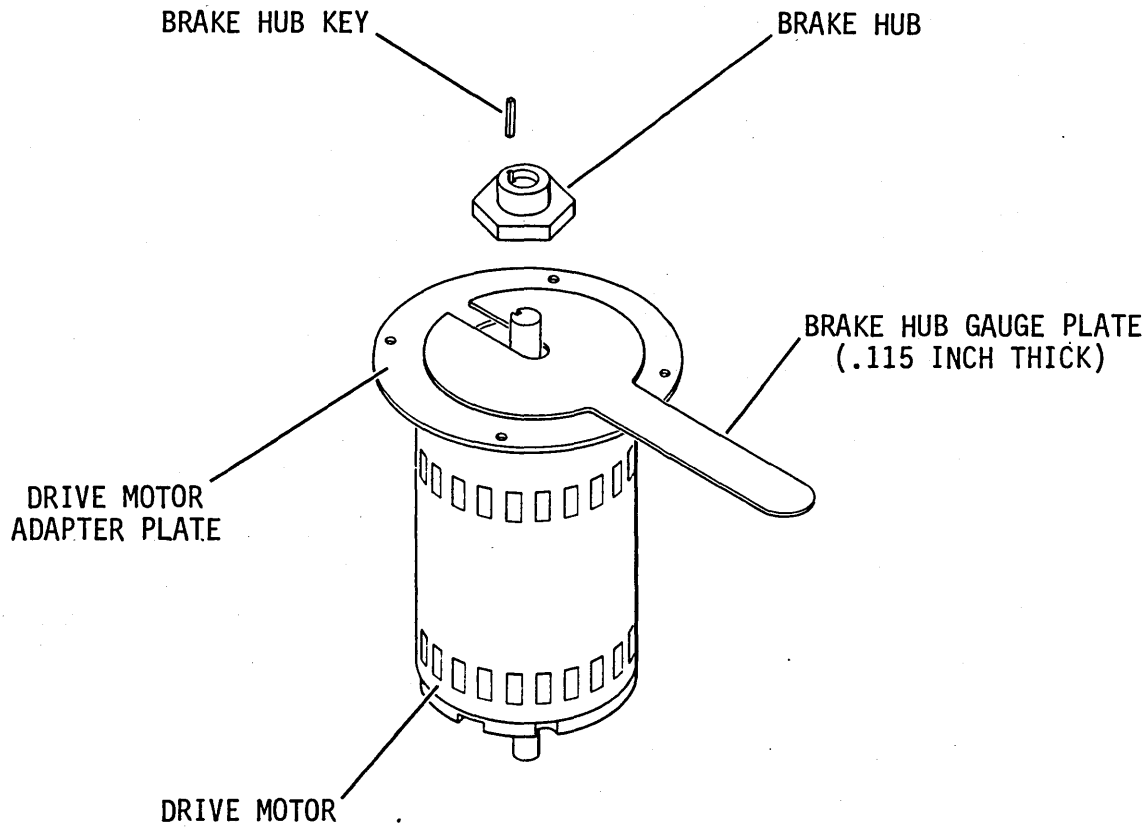


Figure 5-7. Brake Hub Adjustment

5. Adjust gap to thickness of gauge plate by pushing brake hub toward motor until it contacts plate.

6. Tighten set screws to 1.2 N·m (10.8 lbf·in) and remove gauge plate. Check adjustment.

7. Perform brake replacement procedure described above starting at step 2.

8. Perform top cover replacement procedure (5102).

5206 - DRIVE MOTOR REMOVAL & REPLACEMENT

This procedure describes how to replace the drive motor (see figure 5-8).

REMOVAL

1. Perform top cover removal procedure (5102).

2. Perform drive belt removal procedure (5105).

3. Loosen the collar securing pulley on drive motor shaft and slide pulley and collar off the shaft.

4. Remove screws securing brake to drive motor adaptor plate, lift off brake and temporarily set aside on top of power supply.

5. Perform the hexagonal brake hub removal part of brake removal procedure (5205).

6. Remove screws securing adaptor plate to top of drive motor. Lift adaptor plate off motor and set aside.

7. Disconnect motor cable from J60 on power supply.

8. Remove start capacitor from clamp on side of drive, remove end cap from capacitor, and disconnect wires from capacitor terminals. Cut tie wraps as necessary and pull wires free to allow removal from drive with motor.

9. Remove screws securing drive motor to hanger and lift drive motor out of drive.

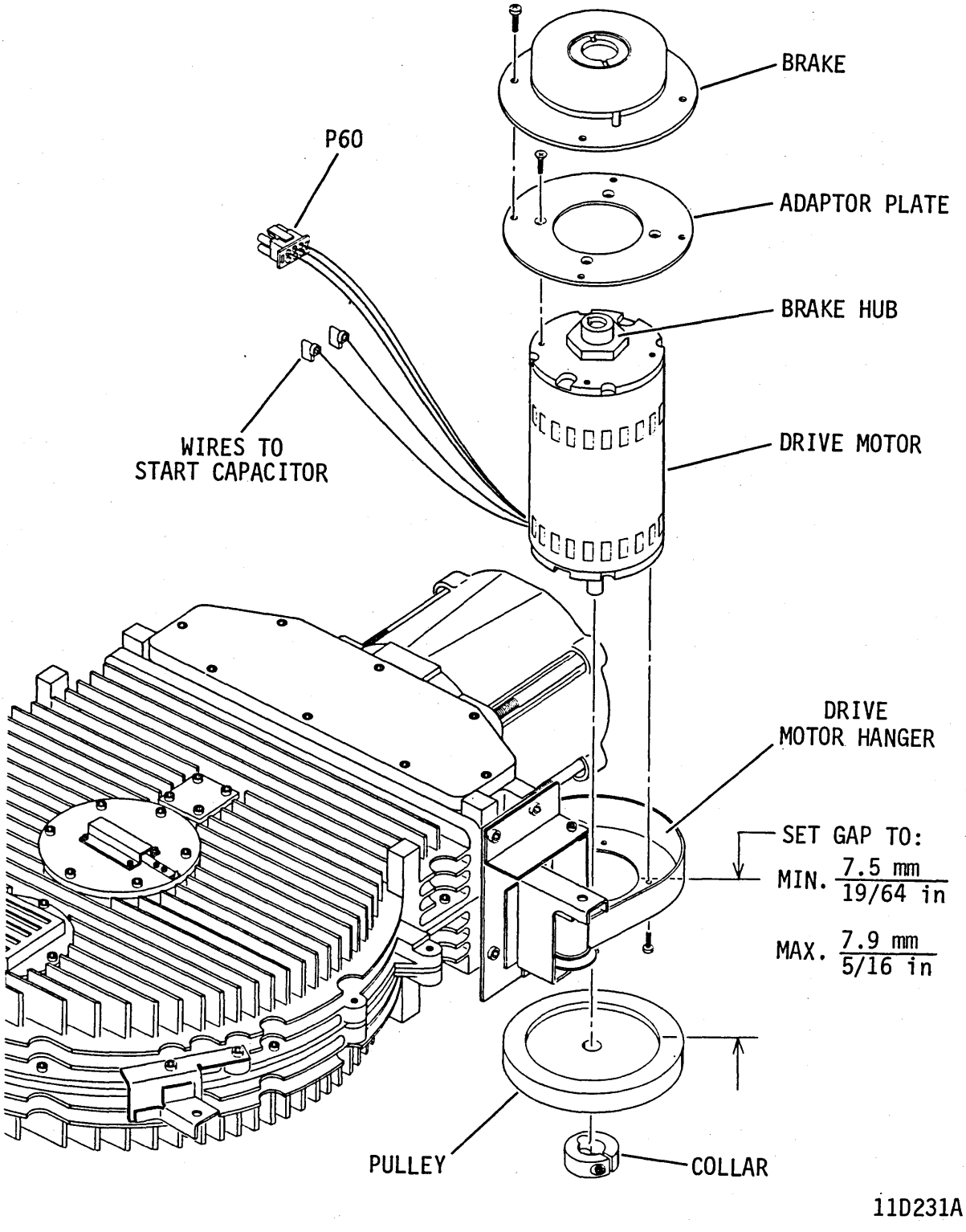


Figure 5-8. Drive Motor Removal & Replacement

REPLACEMENT

1. Set drive motor in place on drive motor hanger, install mounting screws and tighten securely.

2. Route drive motor wires with slide-on connectors to motor start capacitor clamp and replace cable ties removed during motor removal. Install wires onto capacitor terminals, replace capacitor end cap, and insert capacitor into clamp.

3. Place adaptor plate onto top of drive motor and install mounting screws. Tighten screws securely.

4. Perform the hexagonal brake hub replacement and adjustment part of brake replacement procedure (5205).

5. Place brake assembly over drive motor shaft and onto adaptor plate.

6. Rotate brake assembly to align mounting holes with those in adaptor plate, then install and tighten mounting screws.

7. Slide pulley and collar onto drive motor shaft, with collar facing away from motor, and slide towards motor until a distance of from 7.5 mm (19/64 inch) to 7.9 mm (5/16 inch) is measured between of drive motor hanger and pulley (refer to figure 5-8).

8. Tighten set screw on pulley collar to 19.8 N·m (175 lbf·in). Check distance between pulley and drive motor hanger.

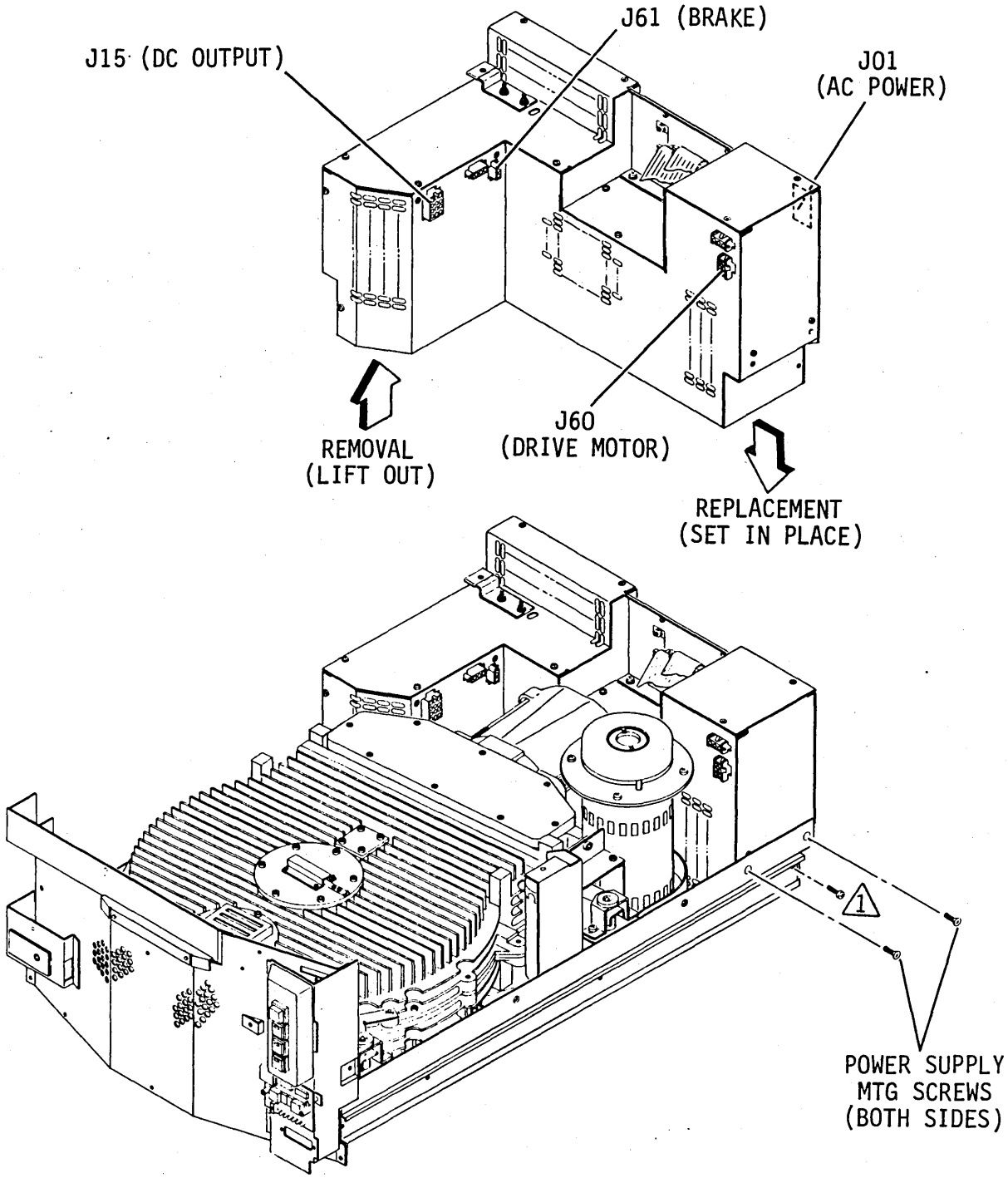
9. Connect motor cable to J60 on power supply.

10. Perform drive belt replacement procedure (5105).

11. Perform top cover replacement procedure (5102).

5207 - POWER SUPPLY REMOVAL & REPLACEMENT

The following procedure provides instructions for removing and replacing the power supply (see figure 5-9). A second person may be needed to provide assistance while the power supply is being removed and installed.



NOTES:

1. THESE SCREWS SECURE THE SLIDE ASSEMBLIES TO THE DRIVE AT THE REAR AND MUST BE REMOVED TO REMOVE POWER SUPPLY. (BOTH SIDES)

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Figure 5-9. Power Supply Removal & Replacement

REMOVAL

1. Remove power from drive as follows:

   a. Press START switch to release it from start position.

   b. Wait for READY indicator to stop flashing, and then gain access to rear of drive and set CB1 to OFF.

   c. Disconnect ac power cable from AC INPUT connector J1 on power supply.

2. Gain access to rear of drive and disconnect external I/O cables from I/O panel connectors.

3. Remove front panel insert, release front panel latch, and pull drive forward until it locks in the fully extended position.

4. Perform top cover removal procedure (5102).

5. Perform drive electronics assembly removal procedure (5307).

6. Disconnect cables from J15, J60, J61, and J63 on power supply.

7. Remove screws securing power supply to base pan at locations shown in figure 5-9.

8. Carefully lift power supply out of drive.

REPLACEMENT

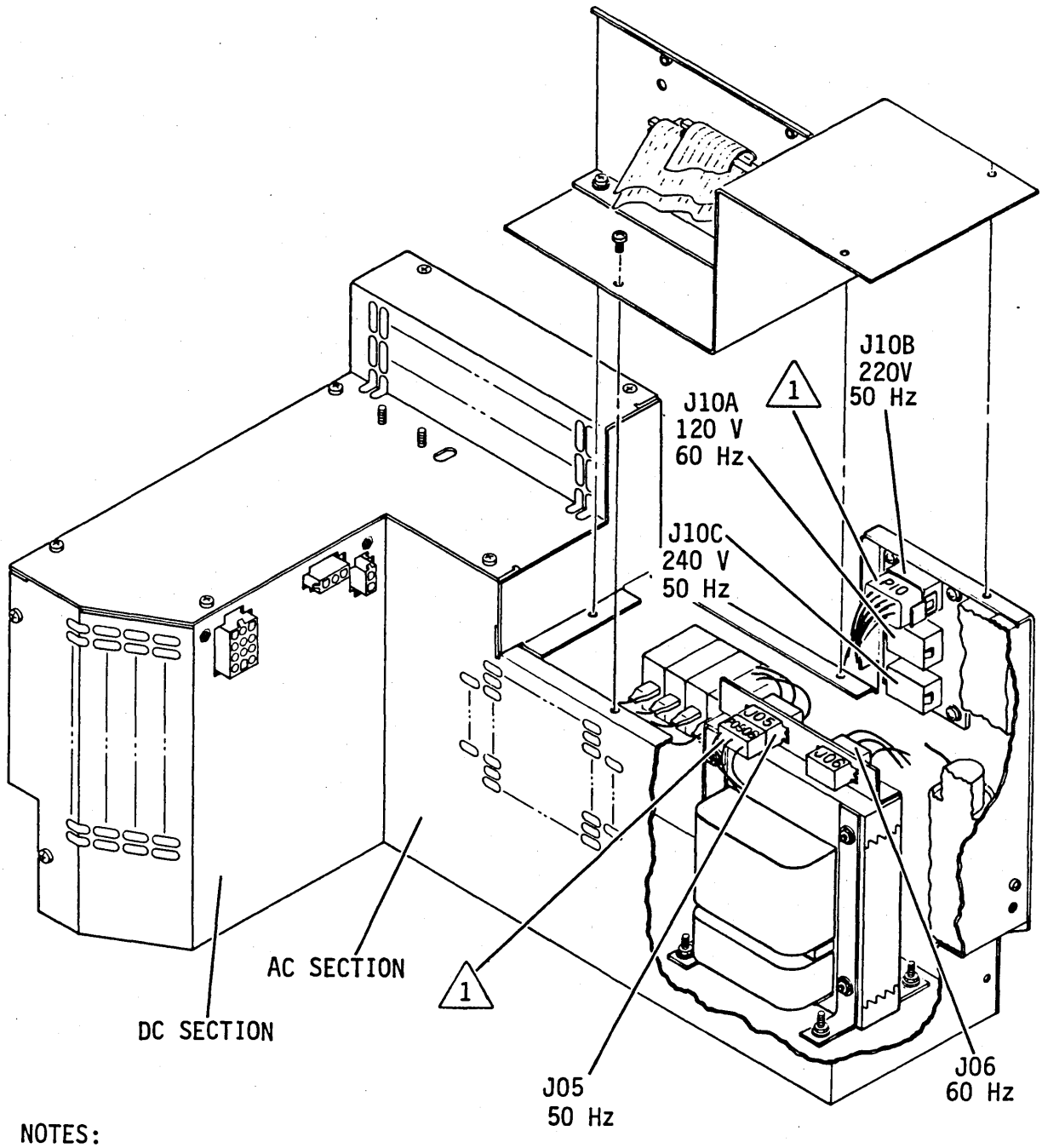
1. Check that the replacement power supply is programmed for proper voltage and frequency as follows:

   a. Remove top cover from ac section.

   NOTE

   An explanation of the P10 and P05/06 options is given on the chart called INTERNAL CONNECTIONS. This chart is displayed on the rear panel of the power supply.

   b. Examine the position of voltage select connector P10 and frequency select connector P05/06 (see figure 5-10). Determine if this position corresponds to the input voltage/frequency listed on the equipment identification label for the drive.



NOTES:

1. POWER SUPPLY IS SHOWN PROGRAMMED FOR 220 V 50 Hz OPERATION.
2. VOLTAGE AND FREQUENCY PROGRAMMING MUST BE SELECTED TO MATCH POWER REQUIREMENTS LISTED ON THE EQUIPMENT IDENTIFICATION LABEL FOR THE DRIVE IN WHICH THE POWER SUPPLY IS BEING INSTALLED.

11D228

Figure 5-10. Power Supply Voltage/Frequency Conversion

c. If the replacement power supply is wired correctly, disregard the remaining operations in step 1 and proceed to step 2. If changes are necessary, complete the remaining operations in step 1.

d. Locate component board with connectors labeled J10A, J10B, and J10C. One of these connectors has wiring harness connector P10 mated to it at time of shipment.

e. Squeeze retaining tabs and remove wiring harness connector P10. Install P10 onto connector programmed for the desired voltage range (J10A - 120 V, J10B - 220 V, or J10C - 240 V).

f. Locate harness connector P06/05 at the top of transformer T1. This connector will mate with bracket mounted connector J06 for 60 Hz operation or J05 for 50 Hz operation. Mate the harness connector P05/P06 with the appropriate bracket mounted connector (J05 or J06) for operation at the desired line frequency.

g. Place top cover on ac section of power supply, install mounting screws and tighten securely.

2. Carefully set power supply in place at rear of drive. Install mounting screws and tighten securely.

3. Connect cable to J15 on power supply.

NOTE

Leave connector P40 on opposite end of cable from J15 disconnected from _TRX mother board until the following voltage check is completed.

4. Temporarily connect ac power to power supply and perform the following voltage check.

a. Connect voltmeter ground lead to P40-7 and remaining lead to P40-6.

b. Set circuit breaker CB1 to ON.

c. Check for a voltage reading of +5.1 $\pm$.05 volts and, if necessary, adjust +5 V potentiometer to get this reading.

d. Move the voltmeter lead from P40-6 to P40-2.

e. Check for a voltage reading of -5.1 ±.05 volts and, if necessary, adjust -5 V potentiometer to get this reading.

f. Set circuit breaker CB1 to OFF and disconnect ac power from power supply.

5. Connect cables to J60, J61, and J63 on power supply.

6. Perform drive electronics assembly replacement procedure (5307)

7. Connect ac power cable to power supply, return power to the drive and perform power checks procedure (4101).

8. Perform top cover replacement procedure (5102).

9. Release slide assembly locks and push drive into rack.

10. Gain access to rear of drive and connect external I/O cables to I/O panel connectors.

5208 - UNLOCKING SOLENOID COIL REMOVAL & REPLACEMENT

This procedure describes how to replace the actuator unlocking solenoid coil. The coil is contained in a metal cannister that mounts on the bottom of the module (see figure 5-11).

REMOVAL

1. Perform top cover removal procedure (5102).

2. Remove spindle access cover from bottom of drive.

3. Clip tie wraps and disconnect cable from J25 on _UCX board.

CAUTION

Do not attempt to remove solenoid shaft and armature assembly from module. Only the solenoid coil is replaceable.

4. Remove screws that fasten solenoid coil to bottom of module and lower solenoid coil away from drive.

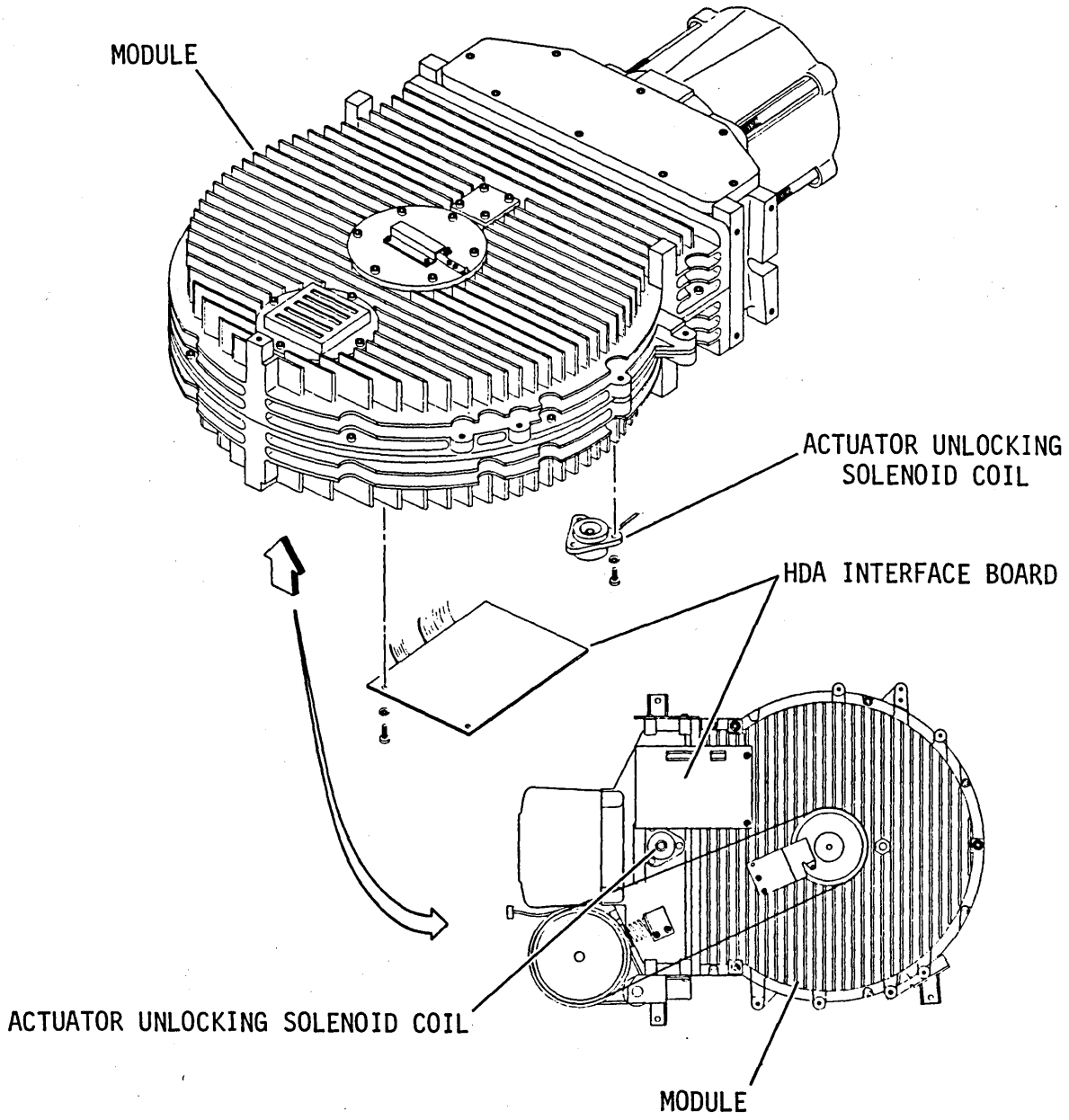


Figure 5-11. Unlocking Solenoid Coil Removal & Replacement

REPLACEMENT

1. Clean the area surrounding the solenoid shaft and armature assembly using a clean, line-free, cloth.

CAUTION

Do not attempt to replace solenoid shaft and armature assembly. Discard solenoid shaft and armature assembly supplied with replacement solenoid.

2. Place solenoid coil over solenoid shaft and armature assembly and onto module with leads facing towards magnet end of module. Install mounting screws and tighten securely.

3. Connect cable to J25 on _UCX board and reinstall tie wraps at original locations.

4. Install spindle access cover onto bottom of drive. Tighten mounting screws securely.

5. Perform top cover replacement procedure (5102).

6. Release slide assembly locks and push drive into rack.

5209 - MODULE REMOVAL & REPLACEMENT

REMOVAL

1. Perform top cover removal procedure (5102).

2. Perform front panel removal procedure (5103).

3. Perform drive electronics assembly removal procedure (5307).

4. Perform power supply removal procedure (5207).

5. Remove mounting screws securing front panel support to base pan and lift off front panel support (with operator panel and fault display board attached).

6. Remove start capacitor from clamp on side of drive, remove end cap from capacitor, and disconnect wires from capacitor terminals. Cut tie wraps as necessary and pull wires free to allow removal from drive with module.

7. Slide the cables going to the _TSX HDA interface board out of cable clamps located along side member of base pan.

8. Remove mounting screws securing shipping stops onto each module shock mount assembly and remove shipping stops.

WARNING

The module (HDA) assembly weighs more than 36.3 kg (80 lbs). To avoid injury, two persons should work together to lift the module out of the drive. Be certain to have a firm grip on the module before attempting to lift it from drive. Also, take care not to damage cables when removing module.

CAUTION

Do not place the module on any flat surface with the pulleys facing down. When removing the module from the drive, turn it over so the pulleys face up before setting it down. This reduces the chance of damaging the spindle shipping lock, the pulleys, or the _TSX HDA interface board.

9. Remove nuts securing module to shock mount studs and carefully lift module clear of drive.

REPLACEMENT

WARNING

The module (HDA) assembly weighs more than 36.3 kg (80 lbs). To avoid personal injury, two persons should work together to lift the module onto the drive. Be certain to have a firm grip on the module before attempting to lift it into its mounting position. Also, take care not to damage cables when installing module.

1. Orient module as shown in figure 5-12, lift it over drive and carefully lower it onto shock mount studs.

2. Install a nut onto each shock mount stud and tighten securely.

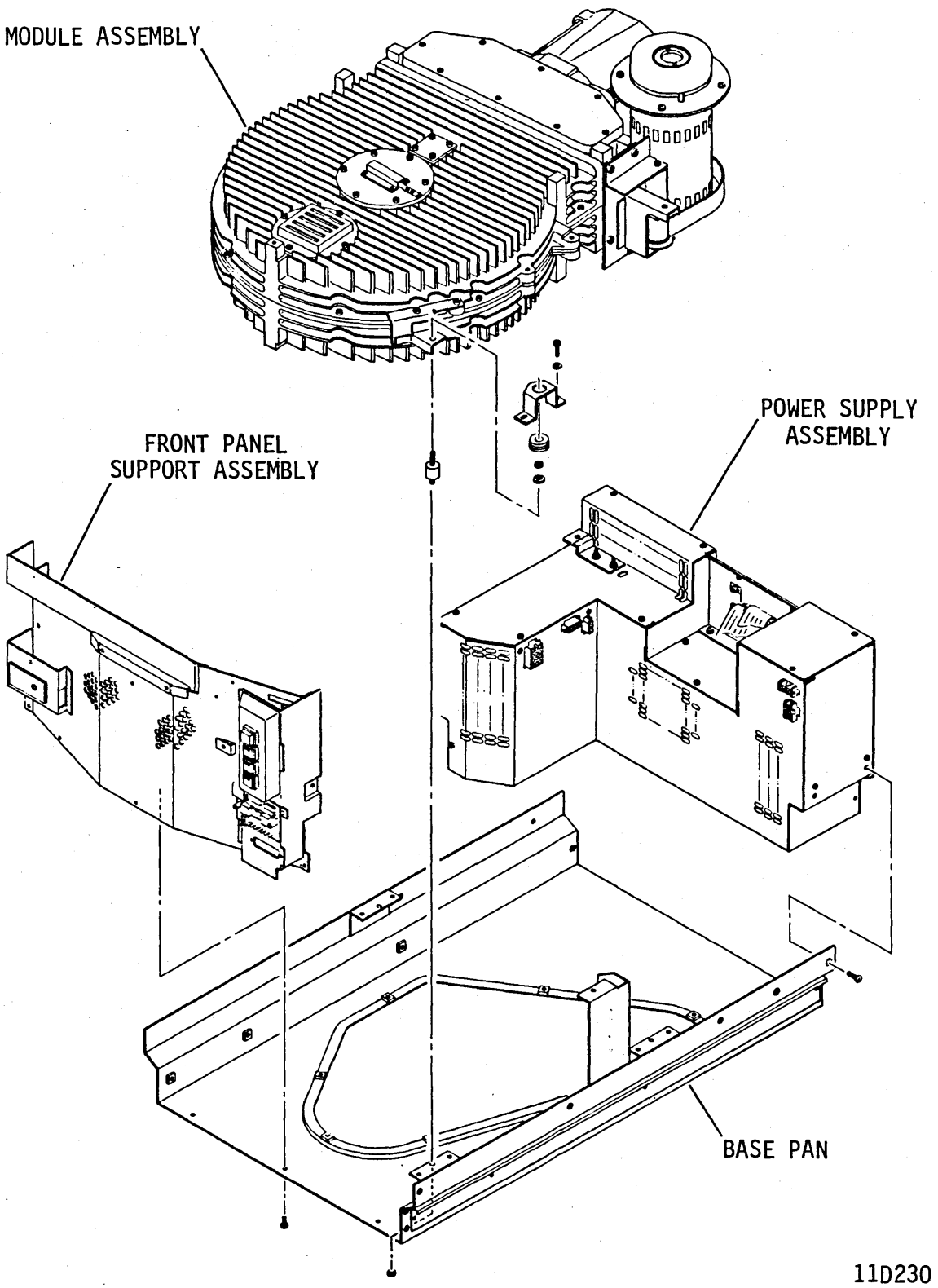


Figure 5-12. Module Removal & Replacement

3. Place shipping stops on each module shock mount assembly, then install mounting screws and tighten securely.

4. Slide the cables going to the _TSX HDA interface board into cable clamps located along side member of base pan.

5. Route wires from drive motor with slide-on connectors to motor start capacitor clamp and replace cable ties removed during module removal (if any). Install wires onto capacitor terminals, replace capacitor end cap, and insert capacitor into clamp.

6. Position front panel bracket (with operator panel and fault display board attached) on base pan. Install mounting screws and tighten securely.

7. Perform power supply replacement procedure (5207).

8. Perform drive electronics assembly replacement procedure (5307).

9. Perform a final check of all cable routing and connections.

10. Perform front panel replacement procedure (5103).

11. Perform top cover replacement procedure (5102).

5210 - CABLE REPLACEMENT

All interassembly cables are of the flat ribbon type with the exception of the dc power cable. The dc power cable is made up of individual wires tied together.

All of the flat ribbon cables have one end permanently attached to an assembly and are referred to as trailing cables. When a trailing cable is defective, the cable and the attached assembly must be replaced. However, the dc power cable can be replaced as a separate item.

5301 - —VDX BOARD REMOVAL & REPLACEMENT

REMOVAL

1. Perform top cover and front panel removal procedures (proc 5102, 5103).

2. Remove top cover from front panel support and disconnect cables from J13, J26, and J28.

3. Loosen or remove screws attaching _VDX board to _TRX mother board (see figure 5-13).

4. Slide board out of edge connectors J14 and J29 and lift it away from drive.

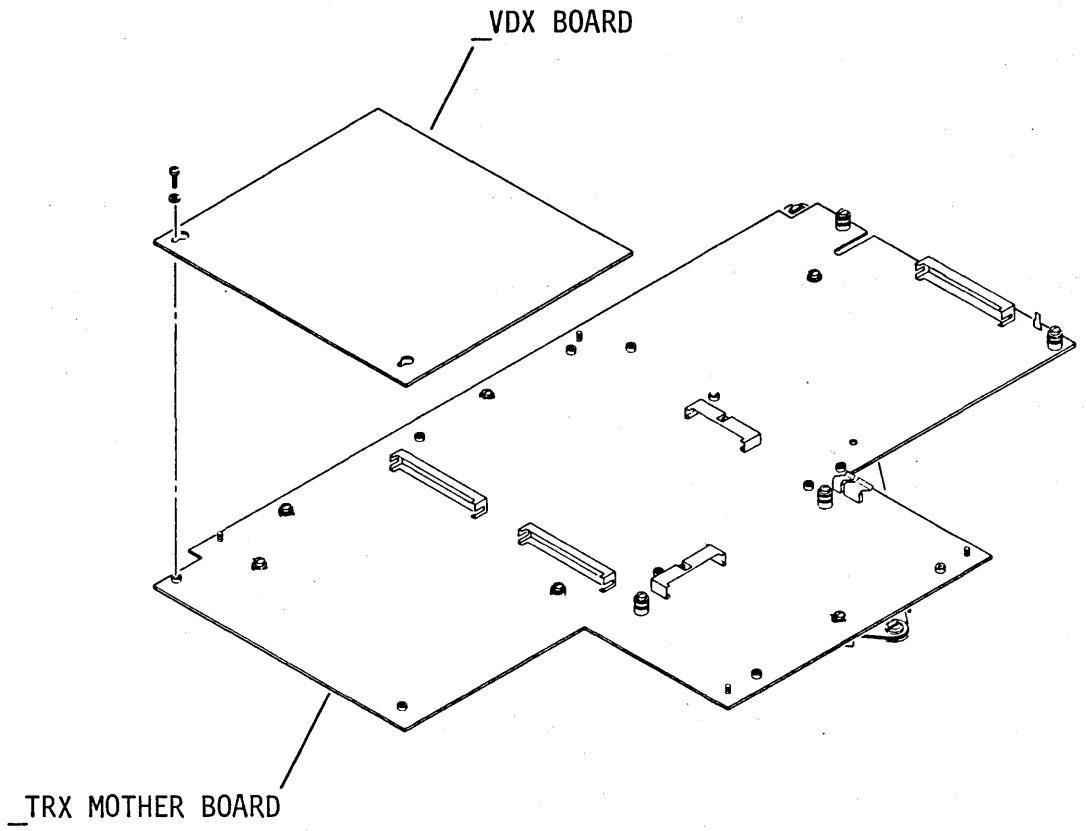


Figure 5-13. _VDX Board Removal & Replacement

REPLACEMENT

1. Slide board into edge connectors J14 and J29. Install and/or tighten mounting screws.

2. Connect cables to J13, J26, and J28. Replace top cover on front panel support.

3. Ensure that all sector select switches are set as indicated in the installation section of hardware maintenance volume 1.

4. Perform top cover and front panel replacement procedures (proc 5102, 5103).

5302 - _SUX (READ/WRITE) BOARD REMOVAL & REPLACEMENT

REMOVAL

1. Perform top cover removal procedure (5102).

2. Disconnect cables from connectors J27 and J32.

3. Loosen or remove screws securing _SUX board to _TRX mother board (see figure 5-14).

4. Slide board out of edge connector J30 and lift away from drive.

REPLACEMENT

1. Slide board into edge connector J30. Install and/or tighten mounting screws.

2. Connect cables to J27 and J32.

3. Perform top cover replacement procedure (5102).

5303 - _TSX (HDA INTERFACE) BOARD REMOVAL & REPLACEMENT

This procedure describes how to replace the _TSX board which is located on the bottom of the module (see figure 5-15).

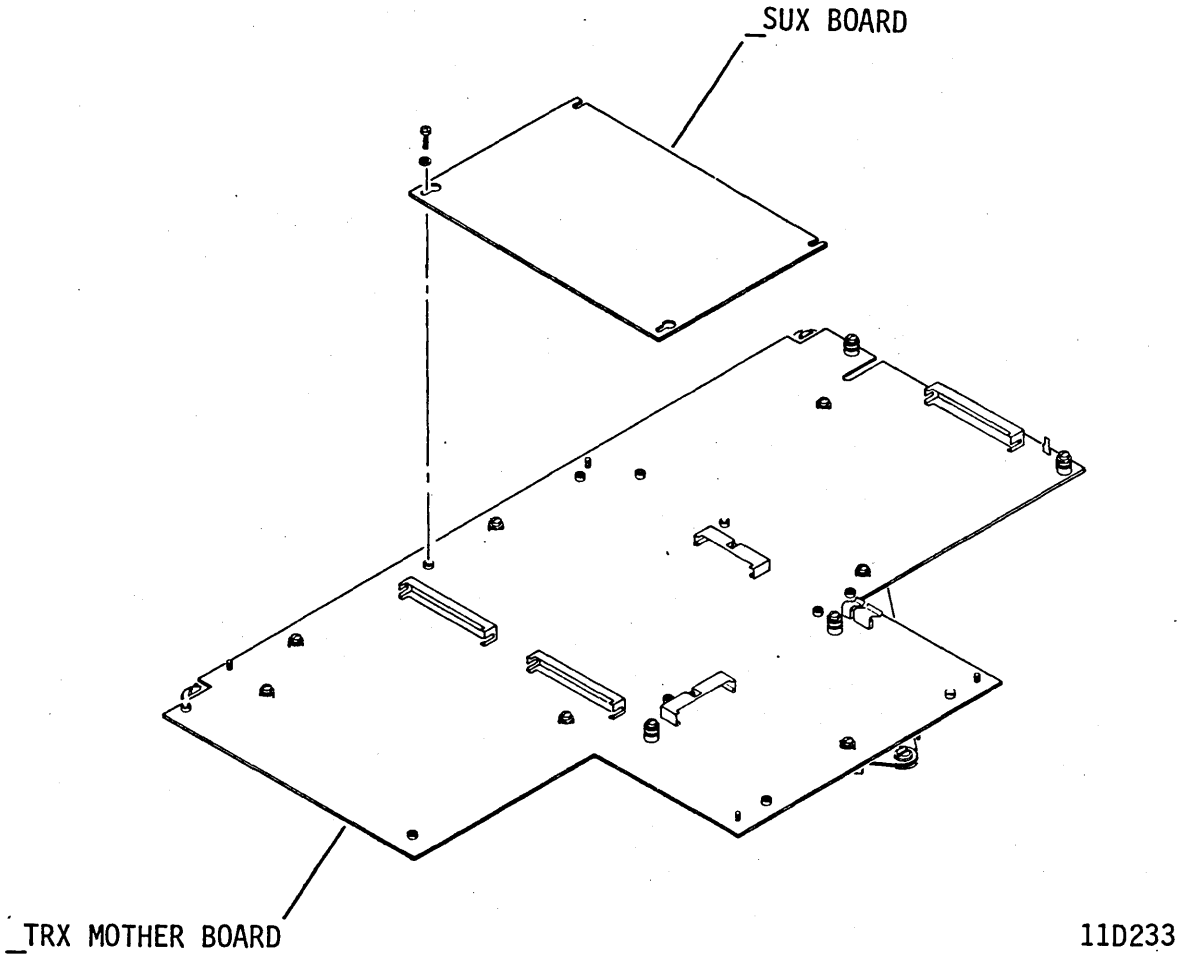


Figure 5-14. _SUX Board Removal & Replacement

CAUTION

The _TSX board contains a connector that plugs directly onto pins within module connector P66. Use care when removing or installing the board to avoid bending or damaging these pins.

REMOVAL

1. Perform top cover and front panel removal procedures (proc 5102, 5103).

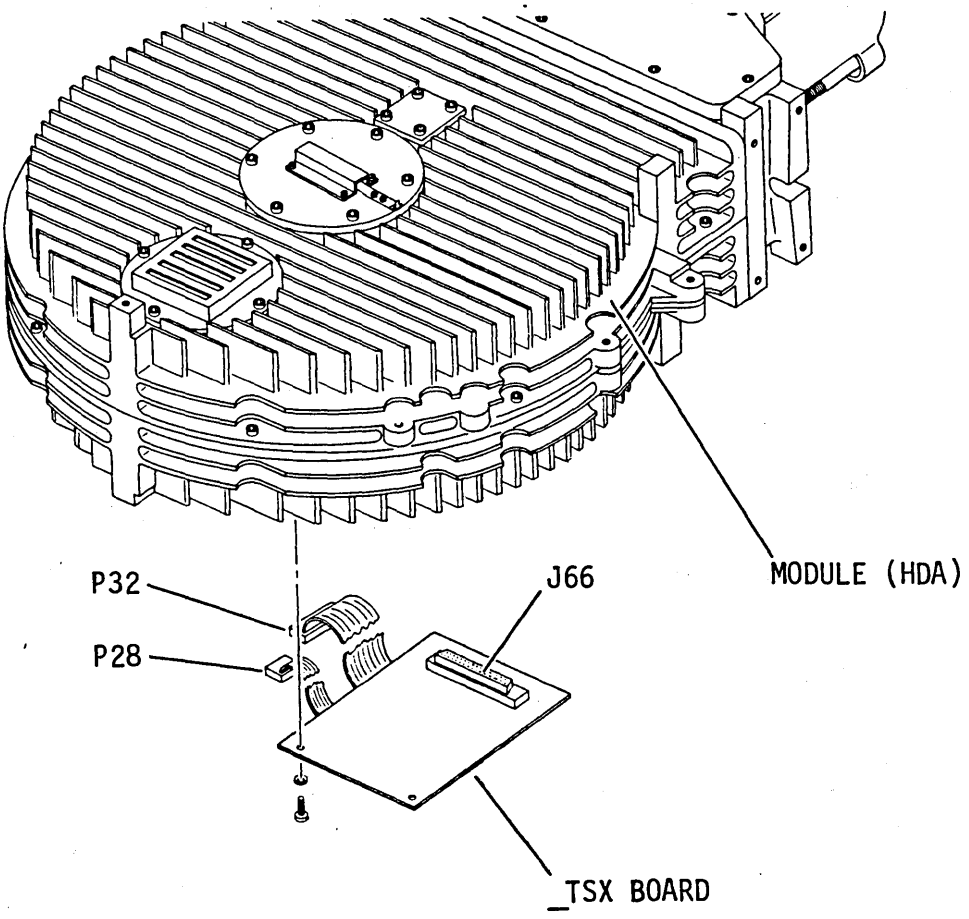


Figure 5-15. _TSX (HDA interface) Board Removal & Replacement

2. Remove top cover from front panel support, then disconnect cables from J28 on _VDX board and J32 on _SUX board.

3. Slide cables out of cable clamps located along side member of base pan.

4. Remove spindle access cover from bottom of drive.

5. Remove attaching hardware and pull off board (see figure 5-15).

REPLACEMENT

1. Align connector J66 on _TSX board with P66 on module and carefully push board into place.

2. Install attaching hardware and tighten securely.

3. Connect cables to J28 on _VDX board and J32 on _SUX board. Replace top cover on front panel support.

4. Slide cables into cable clamps located along side member of base pan.

5. Install spindle access cover onto bottom of drive and tighten mounting screws securely.

6. Perform top cover and front panel replacement procedures (proc 5102, 5103).

5304 - —UCX (POWER AMP.) BOARD REMOVAL & REPLACEMENT

REMOVAL

1. Perform top cover removal procedure (5102).

2. Disconnect cables from J69, J43, J70, and J25.

3. Loosen or remove screws securing _UCX board to _TRX mother board (see figure 5-16).

4. Slide board out of edge connector J24 and lift away from drive.

REPLACEMENT

1. Slide board into edge connector J24. Install and/or tighten mounting screws.

2. Connect cables to J69, J43, J70, and J25.

3. Perform top cover replacement procedure (5102).

5305 - —SYX/—TQX (I/O) BOARD REMOVAL & REPLACEMENT

REMOVAL

1. Perform top cover removal procedure (5102).

2. Disconnect cable from J27 on _SUX board.

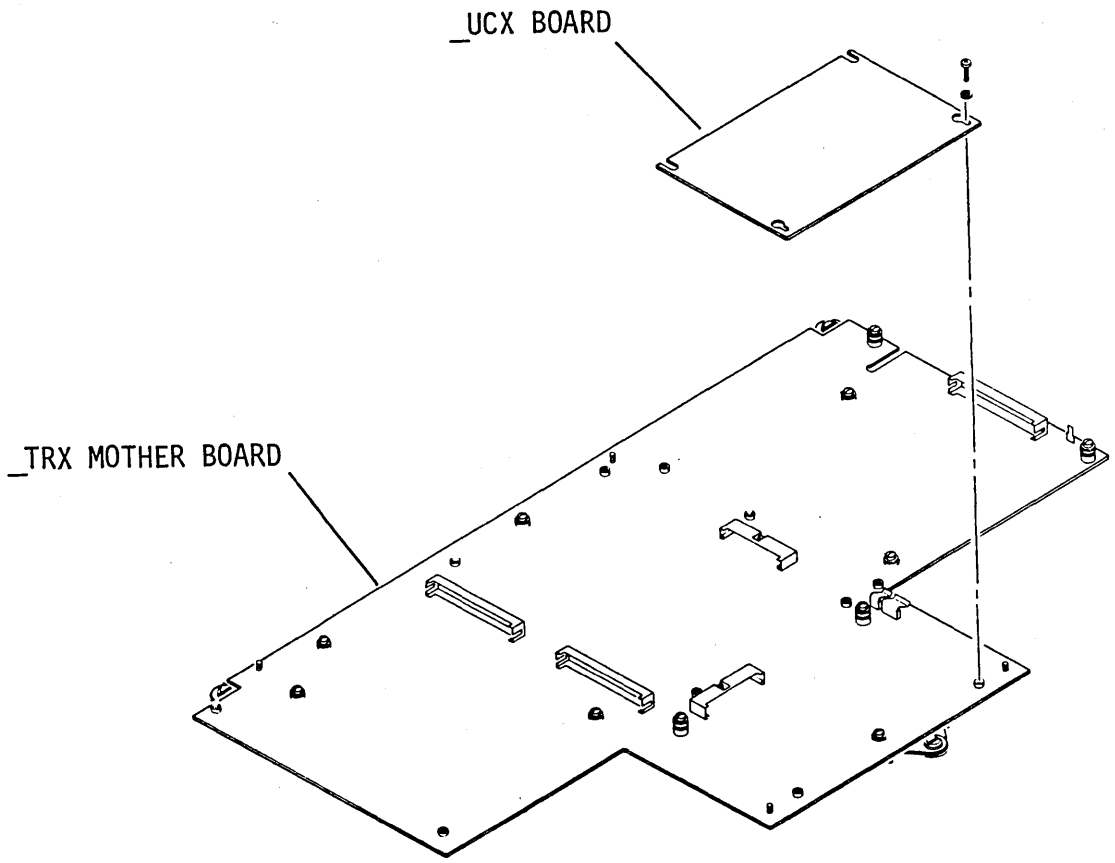


Figure 5-16. _UCX Board Removal & Replacement

3. Disconnect all I/O panel cables from connectors on _SYX or _TQX I/O board.

4. Loosen or remove screws attaching _SYX or _TQX board to _TRX mother board (see figure 5-17).

5. Slide board out of edge connector J20 and lift away from drive.

REPLACEMENT

1. Slide board into edge connector J20. Install and/or tighten mounting screws.

2. Connect cable to J27 on _SUX board.

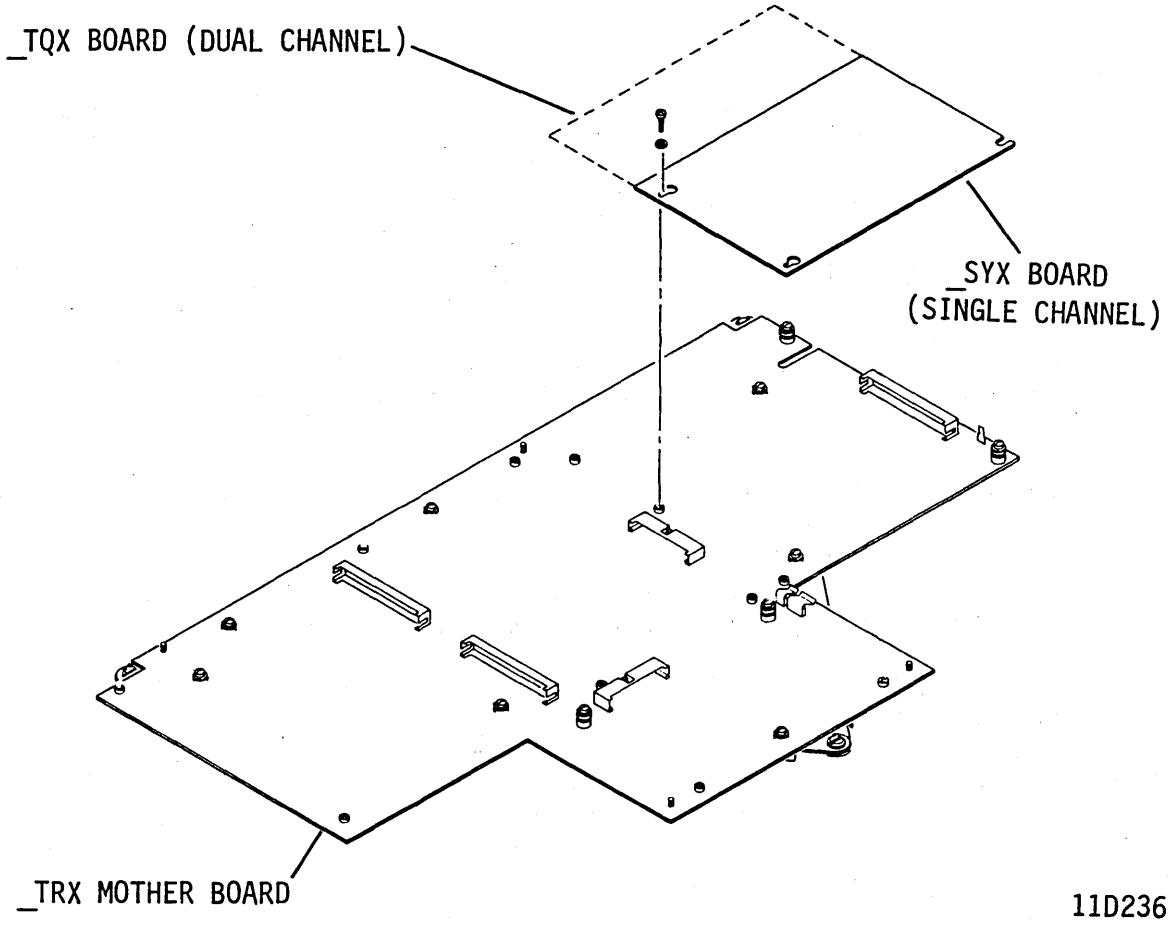


Figure 5-17. _SYX/_TQX I/O Board Removal & Replacement

3. Connect all I/O panel cables to connectors on _SYX or _TQX I/O board.

4. Ensure that all jumpers and switches are set either to match removed board or as indicated in the installation section of hardware maintenance manual volume 1.

5. Perform top cover replacement procedure (5102).

5306 - —TRX MOTHER BOARD REMOVAL & REPLACEMENT

REMOVAL

1. Perform removal procedures for top cover (5102) and front panel (5103).

2. Perform removal procedures for _VDX board (5301), _SUX board (5302), _UCX board (5304), and _SYX/_TQX I/O board (5305).

3. Disconnect I/O terminator ground wire from J67 at rear of mother board.

4. Disconnect cable from connector J65 on mother board.

5. Disconnect all ground straps between module and mother board.

6. Loosen three captive screws securing the mounting bracket and mother board to the drive and carefully lift up one side.

7. Disconnect dc power cable from J40 on underside of mother board.

8. Clip tie wraps and slide cables out of cable clamps mounted on underside of mother board.

9. Lift bracket with mother board attached off drive (see figure 5-18).

10. Remove screws securing mother board to bracket and separate board from the bracket.

REPLACEMENT

1. Align mother board to mounting holes in mounting bracket. Install screws and tighten securely.

2. Place bracket with mother board attached in its mounting position on drive. Do not tighten captive mounting screws at this time.

3. Lift up one side of the mother board and connect dc power cable to J40 on underside of mother board. Replace tie wraps and slide cables into cable clamp on underside of mother board.

4. Align captive screws on bracket with mounting holes and tighten securely.

5. Connect all ground straps between module and mother board.

6. Connect cable to J65 on mother board.

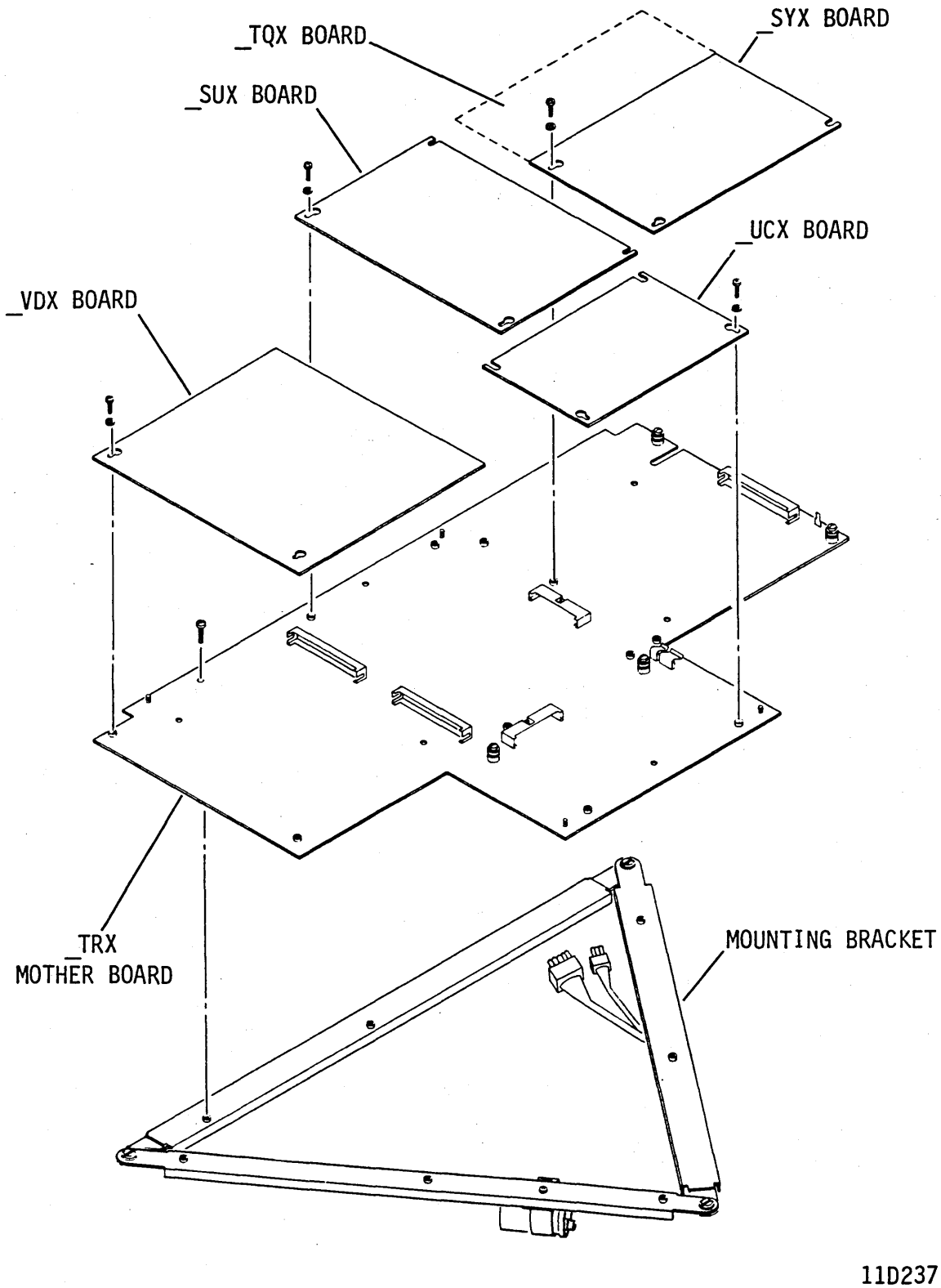


Figure 5-18. _TRX Mother Board Removal & Replacement

7. Connect I/O terminator ground wire to J67 on mother board at rear of unit.

8. Perform replacement procedures for _SYX/_TQX I/O board (5305), UCX board (5304), _SUX board (5302), and _VDX board (5301).

9. Perform replacement procedures for front panel (5103) and top cover (5102).

5307 - DRIVE ELECTRONICS ASSEMBLY REMOVAL & REPLACEMENT

The _VDX board, _SUX board, _UCX board, and _SYX or _TQX (I/O) board are mounted on the _TRX mother board as a single removable electronics assembly. It is necessary to remove this assembly to gain access to other components and assemblies within the drive. This procedure describes how to remove and replace the drive electronics assembly (see figure 5-19).

REMOVAL

1. Perform removal procedures for top cover (5102) and front panel (5103).

2. Disconnect I/O terminator ground wire from J67 on the _TRX mother board at rear of unit.

3. Disconnect cable from connector J65 on the _TRX mother board near the _UCX board.

4. Remove top cover from front panel support and disconnect cables from J13, J26, and J28 on _VDX board.

5. Disconnect cables from J69, J25, and J43 on _UCX board.

6. Disconnect cable from connector J32 on _SUX board.

7. Disconnect all I/O panel cables from connectors on _SYX or _TQX I/O board.

8. Disconnect all ground straps between module and _TRX mother board.

9. Loosen three captive screws securing the drive electronics assembly to the drive and carefully lift up one side.

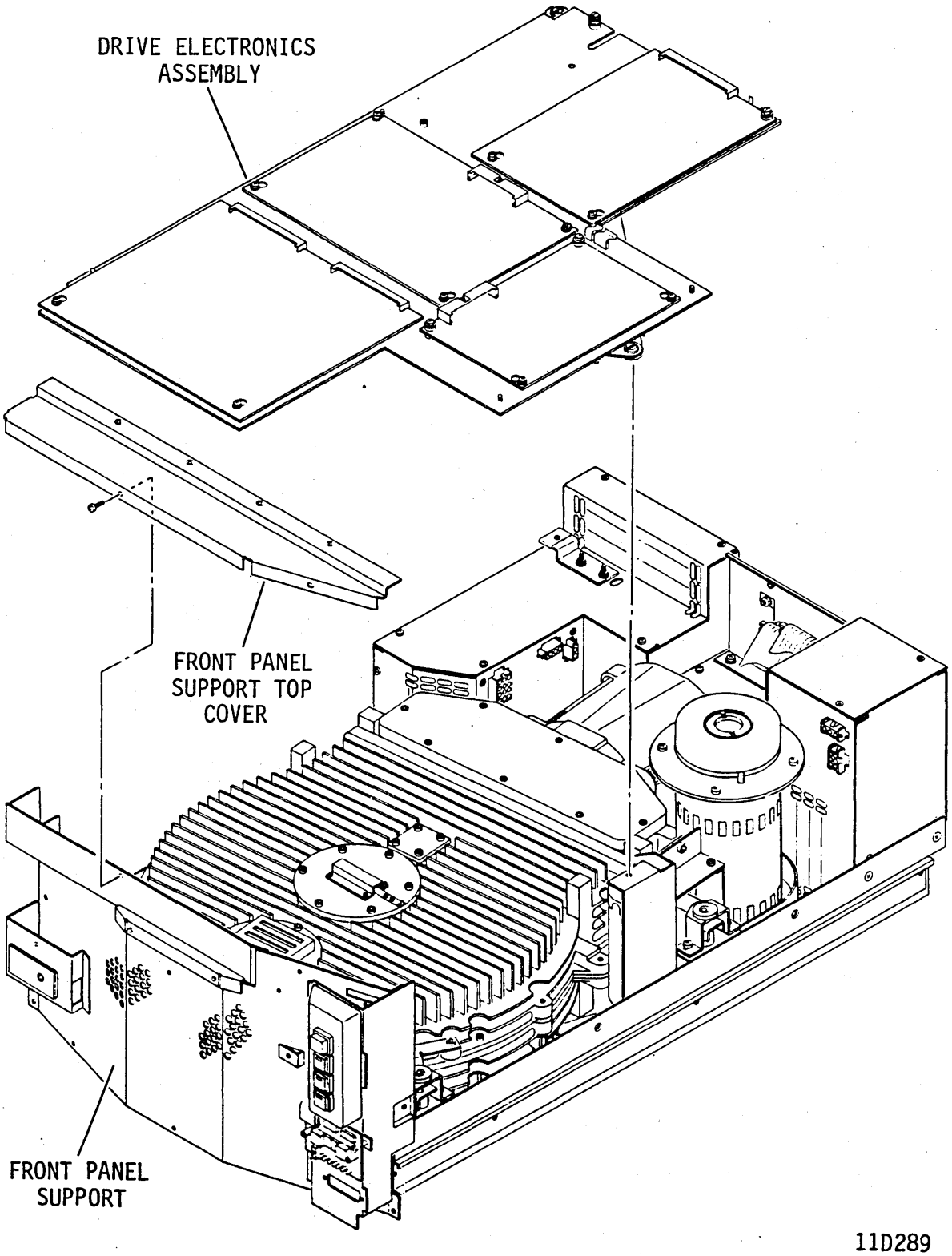


Figure 5-19. Drive Electronics Assembly Removal & Replacement

10. Disconnect dc power cable from J40 on underside of _TRX mother board.

11. Clip tie wraps and slide cables out of cable clamps mounted on underside of _TRX mother board.

12. Lift the drive electronics assembly off drive and set aside.

REPLACEMENT

1. Place drive electronics assembly in its mounting position on drive. Do not tighten captive mounting screws at this time.

2. Lift up one side of the drive electronics assembly and connect dc power cable to J40 on underside of _TRX mother board. Replace tie wraps and slide cables into cable clamp on underside of _TRX mother board.

3. Align captive screws with their respective mounting holes and tighten securely.

4. Connect all ground straps between module and _TRX mother board.

5. Connect all I/O panel cables to connectors on _SYX or _TQX I/O board.

6. Connect cable to connector J32 on _SUX board.

7. Connect cables to J69, J25, and J43 on _UCX board.

8. Connect cables to J13, J26, and J28 on _VDX board and replace top cover on front panel support.

9. Connect cable to J65 on the _TRX mother board near the _UCX board.

10. Connect I/O terminator ground wire to J67 at rear of unit.

11. Perform replacement procedures for top cover (5102) and front panel (5103).

5308 - —RTX RELAY BOARD REMOVAL & REPLACEMENT

This procedure describes how to replace the _RTX relay board which is located within the ac section of the power supply assembly (see figure 5-20).

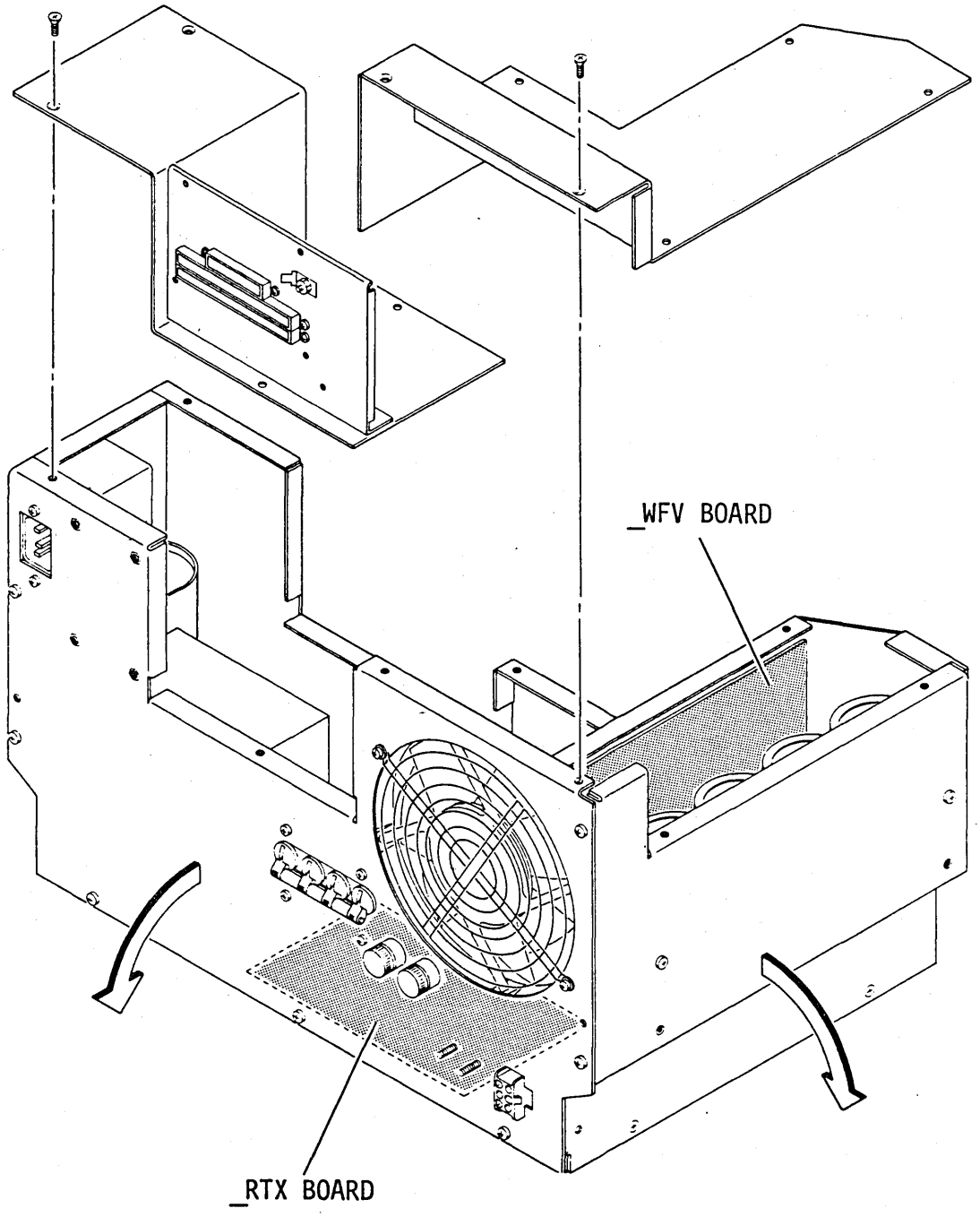


Figure 5-20. Power Supply Circuit Board Removal & Replacement

REMOVAL

1. Remove power from drive as follows:

   a. Press START switch to release it from start position.

   b. Wait for READY indicator to stop flashing and then set CB1 to OFF.

   c. Disconnect ac power cable from site power source.

2. Perform power supply removal procedure (5207).

3. Remove both top covers from power supply.

NOTE

It may be necessary to remove cable ties to permit tilting the rear panel far enough to gain access to _RTX board.

4. Remove hardware securing rear panel to power supply enclosure and tilt panel downward to allow access to _RTX wiring and mounting hardware.

5. Disconnect cables from J1, J2, and J3.

6. Remove screws securing _RTX board to bottom of power supply and lift it out of drive.

REPLACEMENT

1. Position _RTX board onto spacers at bottom of power supply, then install mounting screws and tighten securely.

2. Connect cables to J1, J2, and J3.

3. Replace removed cable ties. Lift rear panel upward to its mounting position, install screws and tighten securely.

4. Position both top covers on top of power supply, install mounting screws and tighten securely.

5. Perform power supply replacement procedure (5207).

6. Connect ac power cable to site power source.

5309 - —WFV REGULATOR BOARD REMOVAL & REPLACEMENT

This procedure describes how to replace the _WFV regulator board which is located within the dc section of the power supply assembly (see figure 5-20).

REMOVAL

1. Perform power supply removal procedure (5207).
2. Remove both top covers from power supply.
3. Remove hardware securing side panel to dc section of the power supply enclosure.
4. Disconnect cables from J1, J2, and J3 along top of _WFV board.
5. Tilt the side panel downward to allow access to _WFV wiring and mounting hardware.
6. Disconnect cable from J4.
7. Disconnect __WFV board ground strap from capacitor bank buss bar.
8. Remove screws along top edge of _WFV board and lift board out of drive.

REPLACEMENT

1. Align the bottom edge of the _WFV board with slot in bottom of power supply and insert board into its mounting position.
2. Install screws along top edge of _WFV board and tighten securely.
3. Connect cable to J4.
4. Connect __WFV board ground strap to capacitor bank buss bar.

5. Lift side panel upward to its mounting position.

6. Connect cables to J1, J2, and J3 along top of _WFV board.

7. Install side panel mounting screws and tighten securely.

8. Place both top covers onto power supply, install mounting hardware and tighten securely.

9. Perform power supply replacement procedure (5207).

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