77738036

CONTROL DATA CORPORATION

CONTROL DATA®
WREN II™ DISK DRIVE
MODEL 94155/94156

GENERAL DESCRIPTION
OPERATION
INSTALLATION AND CHECKOUT
THEORY
DIAGRAMS
MAINTENANCE

MAGNETIC PERIPHERALS, INC.
a Control Data Company

HARDWARE MAINTENANCE MANUAL

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REVISION RECORD

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Address all comments concerning this publication to the distributor or use the enclosed user comment sheet located in the back of this publication.

PREFACE

This manual provides the information needed to install, operate, maintain, troubleshoot, and refurbish the WREN II DISK DRIVES Model 94155 and Model 94156.

The total content of the Manual is comprised of six (6) sections, and is contained in one volume. The manual's publication number should be used when making reference to the WREN II Maintenance Manual.

The following table identifies the contents of this manual:

1 GENERAL DESCRIPTION
2 OPERATION
3 INSTALLATION AND CHECKOUT
4 THEORY
5 DIAGRAMS
6 MAINTENANCE

EMI NOTICE

WARNING: This equipment generates, uses and can radiate radio frequency energy, and if not installed and used in accordance with the instructions manual, may cause interference to radio communications. It has been tested and found to comply with the limits for a Class A computing device pursuant to Subpart J of Part 15 of the FCC rules, which are designed to provide reasonable protection against such interference when operated in a commercial environment. Operation of this equipment in a residential area is likely to cause interference in which case the user, at his own expense, will be required to take whatever measures may be required to correct the interference.

SAFETY INSTRUCTIONS

1. The WREN is to be installed in a customer supplied cabinet where the surrounding air does not exceed 46° C.
2. 6-32 UNC-2A screws are required for installation.
3. The power requirements are:
   +5 VDC ±5% 0.9A
   +12 VDC ±5% 2.4A (4.5Amps for 30 seconds at ±10%)
4. The power supply must satisfy the low voltage safety requirements.
5. Service is to be provided only by trained service personnel.
6. The incorporation of the WREN into a customer-supplied cabinet must meet the appropriate safety requirements of the country in which it is to be used.

SICHEREHITSANLEITUNG

1. Das Gerat ist ein Einbaugerat, vorgesehen fur eine maximale Umgebungstemperatur von 46° C.
2. Zur Befestigung des Wren-Drives werden 4 Schrauben 6-32 UNC-2A benotigt.
3. Als Versorgungsspannungen werden benotigt:
   +5 VDC ±5% 0.9 A
   +12 VDC ±5% 2.4 A (4.5 Amps Fur Ca. Sek fur ±10%)
4. Die Versorgungsspannung muss SELV entsprechen.
5. Alle Arbeiten durfen nur von ausgebildetem Servicepersonal durchgefuhrt werden.
6. Der Einbau des Drives muss den Anforderungen gemass DIN IEC 380/VDE 0806/8.81 entsprechen.

WARNING

This product is an electromechanical device which could present hazards if improperly handled. The device should be maintained only by qualified personnel in accordance with instructions contained in this manual and sound safety practices. Careless disassembly or maintenance procedures may result in damage to the device or injury to personnel. Observe all CAUTIONS or WARNINGS attached to the device or contained in this manual.

These WARNINGS and or CAUTIONS are not exhaustive. The manufacturer cannot know in advance all possible maintenance procedures, or tools, which may be devised by persons who choose not to follow the instructions in this manual. Any deviation from the prescribed procedures may entail risks which have not been evaluated by the manufacturer.

Any persons who use a non-approved procedure or tool must satisfy themselves that no injury to personnel, no damage to the device, and no deterioration of device performance will result."

TABLE OF CONTENTS

1.1 INTRODUCTION

The CDC Models 94155 and 94156 WREN II Disk Drives are small, low-cost, medium performance, random-access rotating-disk, mass-memory devices designed to record and recover data on up to five rigid 5 1/4 inch non-removable fixed disk media. The WREN uses low-mass flying read/write heads attached to a precisely controlled rotary positioner.

1.2 GENERAL DESCRIPTION

1.2.1 STANDARD FEATURES

The following are standard features of the WREN II Disk Drives:

- Industry Standard Interface
- Multiple Capacity Configurations
- Sealed head, disk, and actuator chamber
- No preventive maintenance required
- LSI circuitry for high reliability
- Low audible noise for office environments
- Vertical (side) or horizontal (bottom) mounting
- Low power consumption
- Balanced low mass rotary voice coil actuator
- OEM Manual
- Automatic shipping lock
- Terminators
- Shock mounts
- Dedicated head landing zone

1.2.2 MODEL CONFIGURATIONS

The model configurations are as follows:

MODEL NUMBER	MEGABYTES	NUMBER OF CYLINDERS	NUMBER OF DATA HEADS
94156-86 94155-86	86	925	9
94156-67 94155-67	67	925	7
94156-48 94155-48	48	925	5

1.2.3 ACCESSORIES

The following accessories are available for the WREN and must be ordered and shipped separately:

- Front panel kit, 77771280.
- Power supply - includes five-foot power cable.
- Maintenance Manual, 77738036.

1.2.4 MAJOR COMPONENTS

The major components of the WREN are shown in Figure 1-1.

CAUTION

NEVER remove the top cover of the WREN. This exploded view is for information only. Servicing items in the upper sealed environmental enclosure (heads, media, actuator, etc.) requires special facilities. Only the printed circuit boards external to the sealed area can be replaced without special facilities.

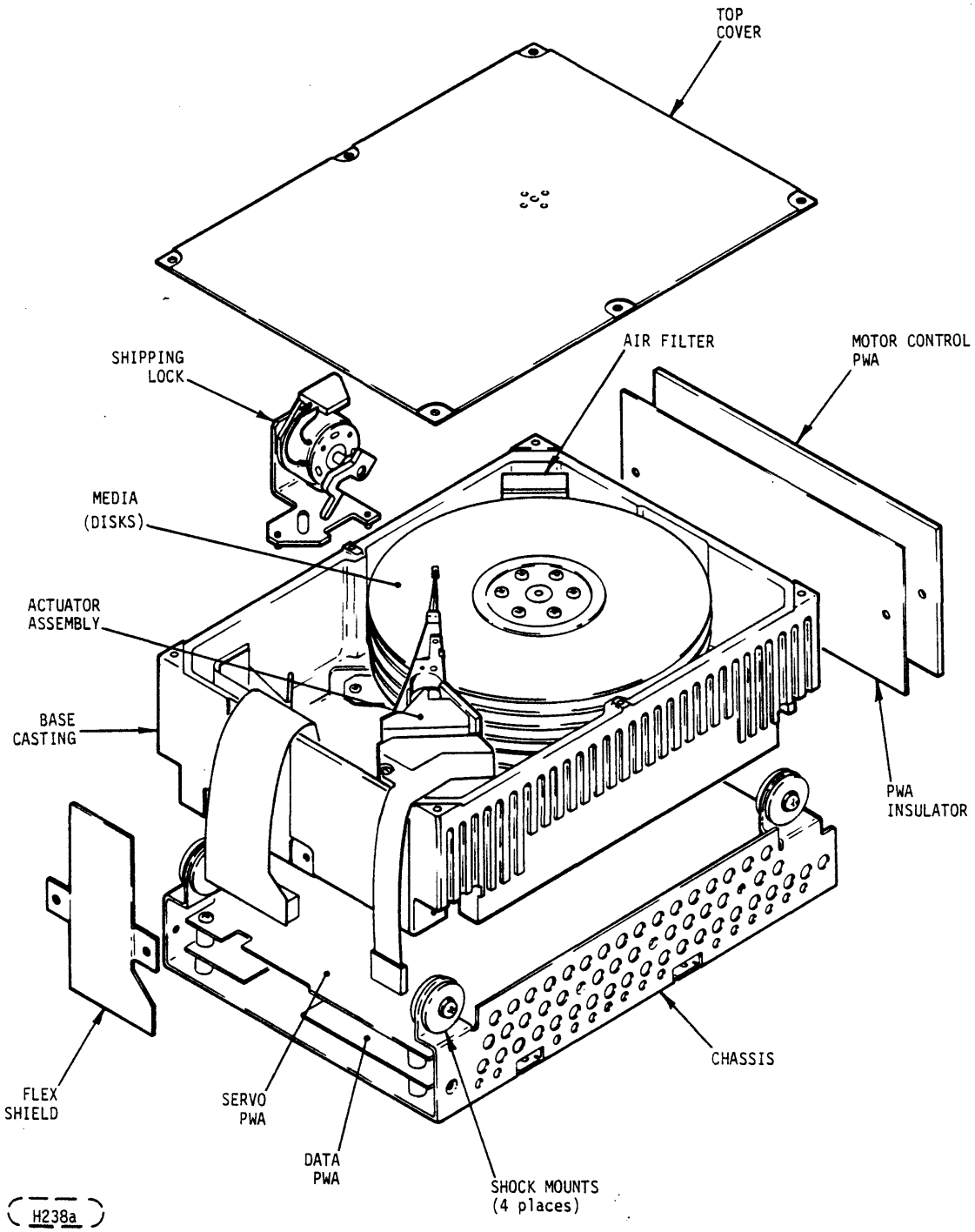


FIGURE 1-1. WREN II EXPLODED VIEW

2.1 INTRODUCTION

There is only one mechanical function required of the operator: to ensure that power is applied. During routine computer operations, the operator should, of course, note any malfunctions or problems and report them.

2.2 OPERATING AND PRELIMINARY DIAGNOSIS PROCEDURE

Due to the sophisticated design and special equipment required to repair the WREN, most repairs may only be effected at a properly equipped and staffed depot service and repair facility. These repair facilities will be capable of performing all warranty and routine repair activities.

Because the front panel indicator provides limited failure conditions (see paragraph 2.2.2) and no operator/drive interaction is required, operating systems must contain sufficient error reporting information to allow the operator to make preliminary diagnosis of problems. In other words, software must adequately inform the operator if any technical difficulties arise. In multi-unit installations, logical and physical identification are necessary for the operator to identify a defective unit.

2.2.1 OPERATING INSTRUCTIONS

1. The following conditions must be met to initiate operation of the disk drive.

   a. The DC power cable from the power supply must be connected.

2. The operating temperature of the drive is 50° to 115° F (10° to 46° C) with a maximum temperature change of 18° F (10° C) per hour. Relative humidity of 20% to 80%.

3. In case of a malfunction, the unit is to be serviced only by trained personnel.

2.2.2 FRONT PANEL INDICATOR (AVAILABLE ONLY WITH FRONT PANEL KIT)

The front panel indicator under normal operation will serve as a Drive Selected indicator. It will also flash to indicate a drive failure when one of the following conditions exist.

1. Rotor is locked.
2. Spindle speed exceeds $\pm$5% tolerance for more than 30 seconds.
3. The WREN cannot load heads after 6 attempts (i.e., PLO does not lock, automatic arm restraint fails to release, etc.).

3.1 INTRODUCTION

This section provides the information and procedures necessary to install and checkout the WREN II Disk Drive. The WREN is designed, manufactured, and tested with a "Plug-in and Play" installation philosophy. Basically, this philosophy minimizes the requirements for a highly trained person to integrate a WREN into their system.

3.2 UNPACKING

Visually inspect the shipping container for any obvious damage. During unpacking, exercise care so that any tools being used do not cause damage to the unit. As the drive is unpacked, inspect it for possible shipping damage. All claims of this type should be filed promptly with the transporter involved. If a claim is filed for damages, save the original packing materials.

After the drive is unpacked, inspect the drive for any visual damage. Compare all parts listed on the shipping bill with the received equipment. Discrepancies or damage should be reported to the Sales Representative. Save the packing materials; they can be used for reshipment.

3.3 OPERATING ENVIRONMENT

The environmental conditions required for optimum performance of the disk drive are, in general, the same as those in an office environment with minimum or no environmental control. These conditions are:

Temperature	50° to 115° F (10° to 46° C)
Humidity	20% to 80%
Altitude	-983 to +6,562 feet (-300 to +2,000 meters)

The room temperature should not change more than 18° F (10° C) per hour. Relative humidity should be kept between 20% and 80%. Avoid high relative humidity as much as possible since it can cause condensation in the drive. Very low relative humidity should also be avoided because it can lead to particle attraction and accumulation by static electricity.

3.4 SPACE ALLOCATION AND MOUNTING REQUIREMENTS

Figure 3-1 shows overall dimensions of the drive for determining space allocation and mounting requirements.

The WREN is designed for multiple unit installation in a standard 19-inch rack. Since the WREN is a fixed drive, slides are not provided, but tapped holes are placed at various locations, on the chassis for mounting in the enclosure.

The WREN provides internal cooling for the PWA's and mechanical components. The WREN design also uses the outer transistor heat sinks to dissipate heat. Direct contract to the WREN heat sinks should not be made.

Consideration should also be given to minimizing restriction of airflow through cooling holes in the drive and near these heat sinks.

A sometimes overlooked consideration when mounting several drives in the same enclosure is heat dissipation. Because power supplies, for example, are typically heavy, they are usually mounted in the bottom of an enclosure. They also produce large amounts of heat. This heat rises to the top of the cabinet or enclosure and the temperature can increase drastically. Cabinet ventilation, either by natural convection or forced cooling, must be provided to keep the internal air temperature around the disk drive within the limits specified in paragraph 3.3.

3.4.1 EMI CONSIDERATIONS

The WREN II, as delivered, is designed for system integration and installation into a suitable enclosure prior to use by an end user. As such the WREN is supplied as a component and is not subject to Subpart 3 of Part 15 of the FCC rules. However, the unit has been tested using proper shielding and grounding and found to be compliant with Class A limits of Subpart 3 of Part 15 of the FCC rules. The physical design characteristics of the WREN serve to minimize radiation when packaged in an enclosure that provides reasonable shielding and will meet or exceed the Class A limits of subpart 3 of Part 15 of the FCC rules.

If the enclosure does not provide adequate shielding, the use of shielded I/O cables is required. If I/O cables are installed external to the enclosure, shielded cables should be used, with the shields grounded to the enclosure and to the host controller.

3.5 MOUNTING ORIENTATIONS

There are only two mounting orientations: disk in a horizontal plane and disks in a vertical plane. In either the horizontal or vertical mounting, the uppermost casting surface should be in a level position or drive performance may be affected.

3.5.1 VERTICAL ORIENTATION MOUNTING

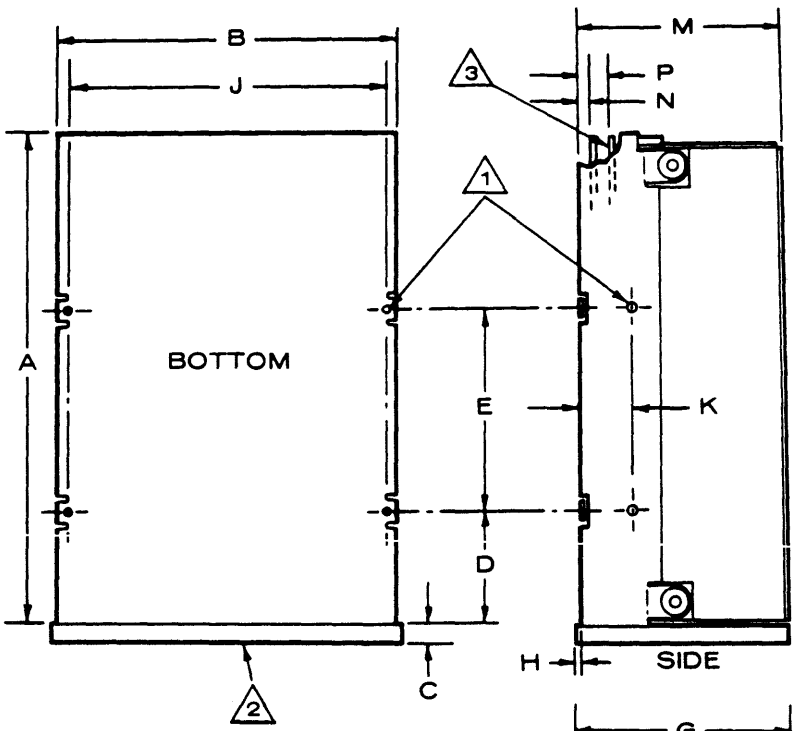
In the vertical orientations, the WREN II disk drives can be mounted with either side up.

The drive must be mounted using four bottom screws for horizontal mount or four side screws for vertical mount.

Two tapped holes are provided on each side of the drive for securing the drive to the enclosure (cabinet). The drive may be bolted to an overhead member in a suspended mount and/or bolted from below in a supportive mount. Screws with 6-32 threads and sufficient length to allow several threads of engagement in the casting after passing through the cabinet mounting member should be used. Maximum screw penetration into WREN chassis should not exceed 0.31 inch.

3.5.2 HORIZONTAL ORIENTATION MOUNTING

As shown in Figure 3-1, four 6-32 tapped holes are provided in the base of the chassis to facilitate mounting in the horizontal position.



NOTES:

1. MOUNTING HOLES: FOUR ON BOTTOM, TWO ON EACH SIDE. 6-32 UNC. MAX SCREW LENGTH INTO CHASSIS 0.31 IN. (7.87 MM). USE ALL FOUR BOTTOM HOLES FOR HORIZONTAL MOUNTING OR ALL FOUR SIDE HOLES FOR VERTICAL MOUNTING. (BOTTOM HOLES PREFERRED).
2. FRONT PANEL ACCESSORY.
3. DRIVE INTERFACE CONNECTIONS..
4. WEIGHT IS APPROX 7.50 LBS (3.4 Kg)

	IN	CM
A	8.0 MAX	20.32
B	5.75 $^{+0.00}_{-0.02}$	14.6
C	0.29 ± 0.02	.74
D	1.87 ± 0.02	4.75
E	3.12 ± 0.01	7.92
F	5.88 ± 0.01	14.9
G	3.38 ± 0.02	8.58
H	0.065 ± 0.02	.165
J	5.50 ± 0.02	13.97
K	0.86 ± 0.02	2.18
M	3.25 ± 0.02	8.25
N	0.37 REF	.94 REF
P	0.63 REF	1.60 REF

H251a

FIGURE 3-1. OUTLINE AND MOUNTING DIMENSIONS

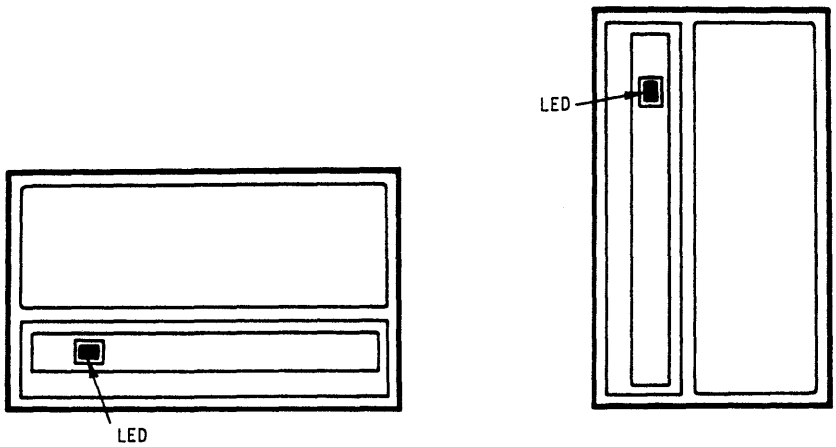


FIGURE 3-2. HORIZONTAL AND VERTICAL (EITHER SIDE DOWN) MOUNTING ORIENTATION

The WREN may be mounted directly to the rack using size 6-32 screws. Place the drive in the rack or cabinet and secure it with screws with sufficient length to ensure adequate thread engagement and such that screw penetration into the WREN chassis does not exceed 0.31 inch.

3.6 DRIVE CABLING

The required connections to the drive are power and signal cables. All input/output cables exit at the rear of the disk drive. The signal cables consist of a command interface cable and a data interface cable. Figures 3-3 and 3-4 show the orientation of the command, DC power and data connectors.

Figure 3-5 shows the intercabling and terminator placement for the various drive connection arrangements. Shown are radial and daisychained system configurations. A single drive would be connected as shown for the radial configuration.

Terminator resistor packs are included in each drive. The terminator consist of a DIP resistor module which is plugged into a DIP socket in each drive. (See Figure 3-3 and 3-4 for location.) An equivalent terminator must be provided in the controller on each input signal line from the WREN to the controller.

3.6.1 RADIAL CONFIGURATION

View A of Figure 3-5 shows each drive interfaced to its own Command cable, which in turn, allows interfacing of more than four drives and a variety of system operational techniques. Each drive has its Data cable and Command cable radially connected to the host controller. The length of each individual cable must not exceed 20 feet (6.1 meters) for Disk Drives with CDC506 interfaces and 10 feet (3.0 meters) for Disk Drives with ESDI. Each Command and Data cable must be terminated at each end in its characteristic impedance. The termination of these cables is accomplished in the drive by the terminating resistor pack for the Command Cables and by resistors on the Data PWA for the Data Cables. These same resistor values must be installed in the host controller.

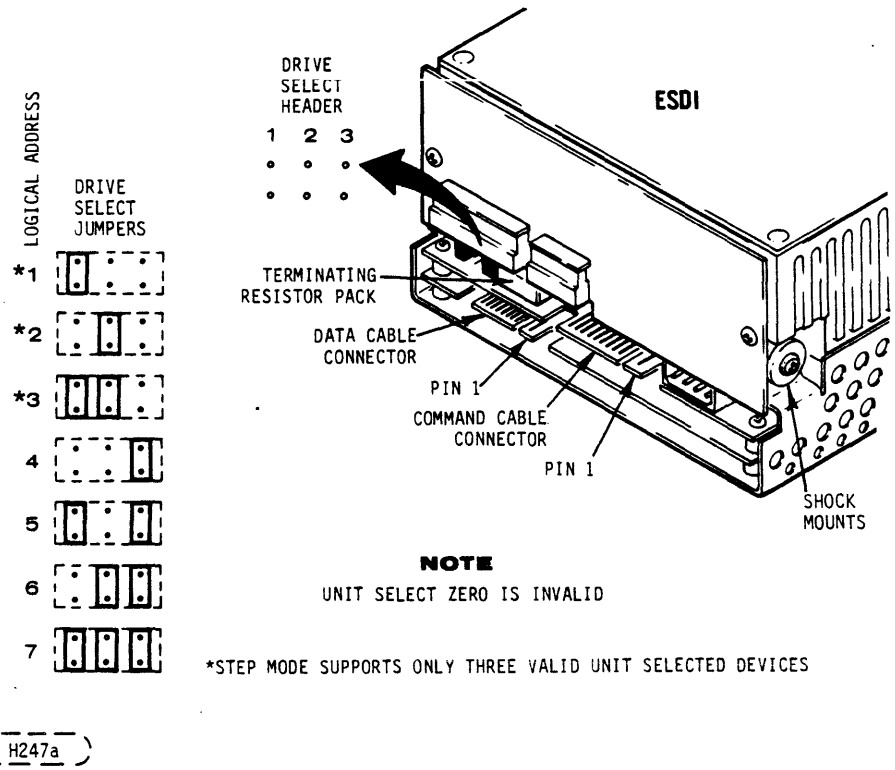


FIGURE 3-3. WREN II I/O CONNECTIONS (ESDI)

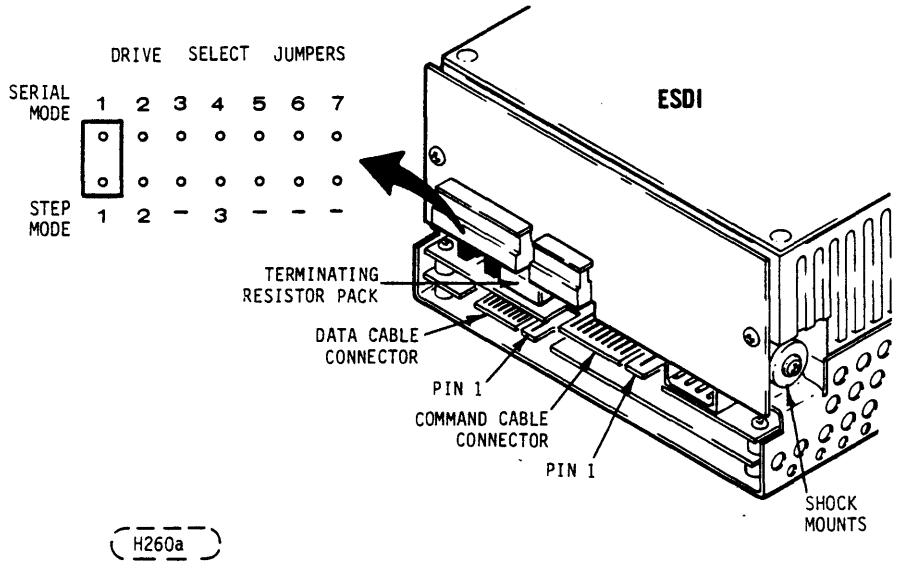


FIGURE 3-3A. OPTIONAL DRIVE SELECT JUMPERS (ESDI)

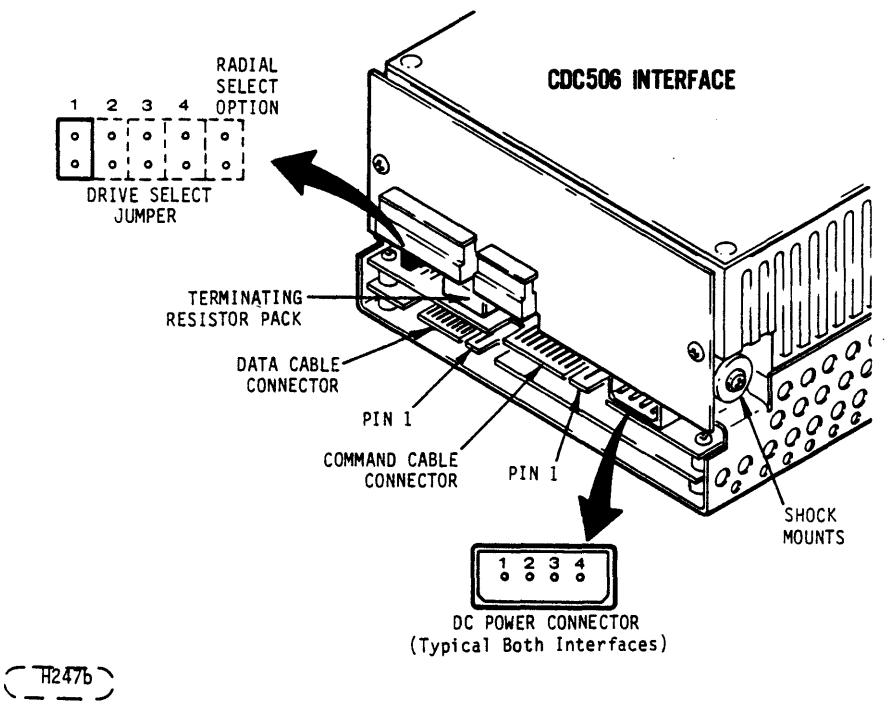
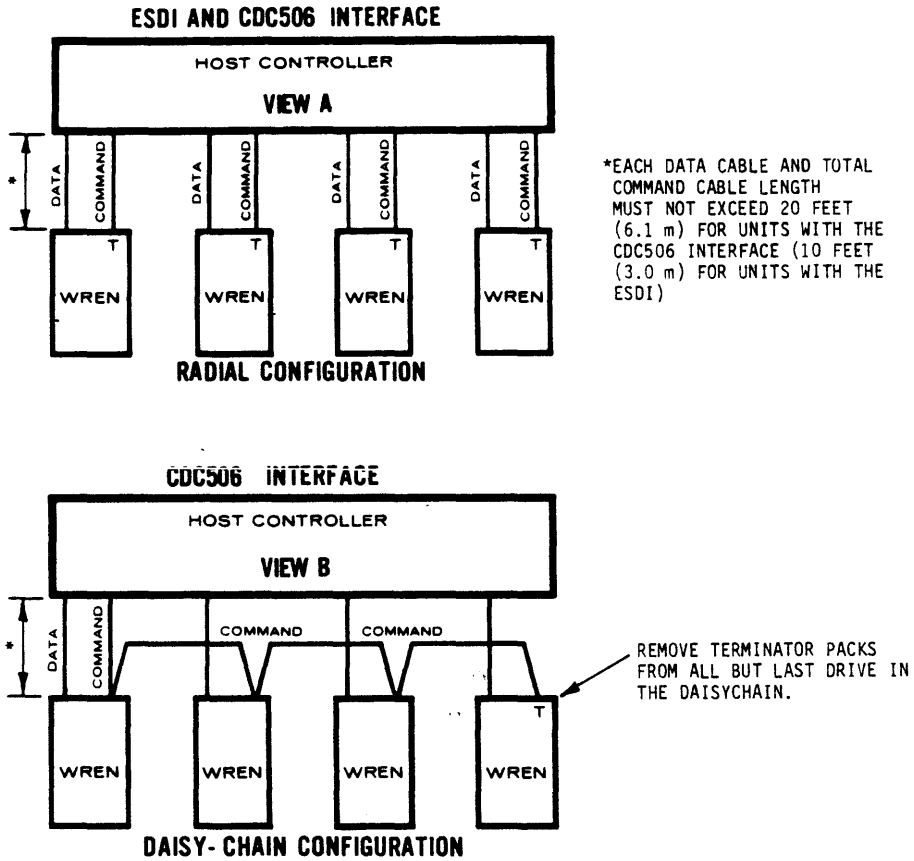


FIGURE 3-4. WREN II I/O CONNECTIONS (CDC 506)

Each Command cable is terminated in the drive by installing the terminating resistor pack. Each Data cable is terminated in the drive by resistors mounted on the Servo PWA.



NOTE 1: 'T' INDICATES TERMINATING RESISTOR PACK. WREN DATA CABLES ARE PERMANENTLY TERMINATED.

MAXIMUM NUMBER OF DRIVES PER CHAIN IS: CDC506 (4 DRIVES), SERIAL MODE ESDI (7 DRIVES), STEP MODE ESDI (3 DRIVES).

H246b

FIGURE 3-5. CABLING CONFIGURATIONS

3.6.2 DAISYCHAINED CONFIGURATION

In a daisychain configuration, the data cables are connected in a radial configuration and the drives are connected in daisychain on the command cable. The total length of all Command cables used shall be less than or equal to 20 feet (6.1 meters) for drives with the CDC506 interface and 10 feet (3.0 meters) for drives with ESDI. The logical address of each drive in the daisychain is determined by the "DRIVE SELECT" plug on the servo PWA. Each data and command cable must be terminated in the Host Controller.

3.7 DRIVE SELECTION

The logical address of the WREN Disk Drive is selected by installing a jumper into the appropriate location on the DRIVE SELECT header which is available from the back of the drive and located on the SERVO PWA. (See Figure 3-6.) This selection is done at the time of installation.

The drives with ESDI have three locations in the header for drive selection. In the serial mode, the binary address of the drive is determined by the location of the jumper and seven drives can be connected in a daisychain. In the step mode, only three drives can be connected in the daisychain. The locations of the jumper are shown in Figure 3-3. One, two, or three jumpers are required. The logical addresses are as follows:

LOCATION OF JUMPERS	LOGICAL ADDRESS
1	1
2	2
1 and 2	3
3	4
1 and 3	5
2 and 3	6
1, 2 and 3	7

An optional DRIVE SELECT header is also available on the WREN II with ESDI. This header is for logical addressing of the drives in the daisychain. This header has only seven sets of pins and is shown in Figure 3-3A.

The drives with the CDC506 Interface have five locations in the header for drive selection. If the drive is to be operated in a radial configuration, the jumper should be in location five. For a daisychain configuration, the jumper should be in position 1, 2, 3 or 4, depending on the location of the drive in the daisychain.

3.8 AUTO VELOCITY ADJUST

After power has been applied and spindle speed is in tolerance, the WREN actuator will perform several seeks (approximately 15) to fine tune the actuator for optimum performance. After all seeks are complete, the heads will be loaded over cylinder 00.

3.9 SELF SEEK TEST

The WREN II has the capability to perform full stroke seeks. The full stroke seeks are initiated as indicated in paragraphs 3.9.1 (Model 94156) and 3.9.2 (Model 94155). The full stroke seeks are initiated after power-up and will continue until SW1-1 (Model 94156) is switched to the OFF position or the jumper (Model 94155 and Model 94156 Optional Configuration) shown in Figures 3.6A, B, and D is removed.

3.9.1 UNITS WITH ESDI (MODEL 94156)

Units with this Interface will perform full stroke seeks if SW1-1 (Figure 3.6A) is in the ON position or if a jumper is installed (Figure 3.6D). The operations of all switches of SW1 are defined in Table 1.

3.9.2 UNITS WITH CDC506 INTERFACE(MODEL 94155)

Units with this Interface will perform full stroke seeks if a jumper is installed in the location shown in Figure 3.6B.

3.10 FRONT PANEL INDICATOR (OPTIONAL)

The front panel indicator under normal operation will serve as a Drive Selected indicator. It will also flash to indicate a drive failure when one of the following conditions exist.

1. Rotor is locked.
2. Spindle speed exceeds $\pm$5% tolerance for more than 30 seconds.
3. The WREN cannot load heads after 6 attempts (i.e., PLO does not lock, automatic arm restraint fails to release).

3.11 INITIAL CHECKOUT AND STARTUP PROCEDURE

1. Mount the drives either horizontally or vertically in the enclosure using standard hardware.
2. Connect the cables for either radial or daisychained configuration. Terminate as required.
3. Connect the Command cable, a 34-conductor ribbon cable, between the Controller and the Drive.
4. Connect the Data cable, a 20-conductor ribbon cable, between the Controller and the Drive.
5. Attach DC power cable from power supply to connector on the rear of the WREN.
6. Apply power to the drive.
7. Run system diagnostic to ensure the operability of the disk subsystem.

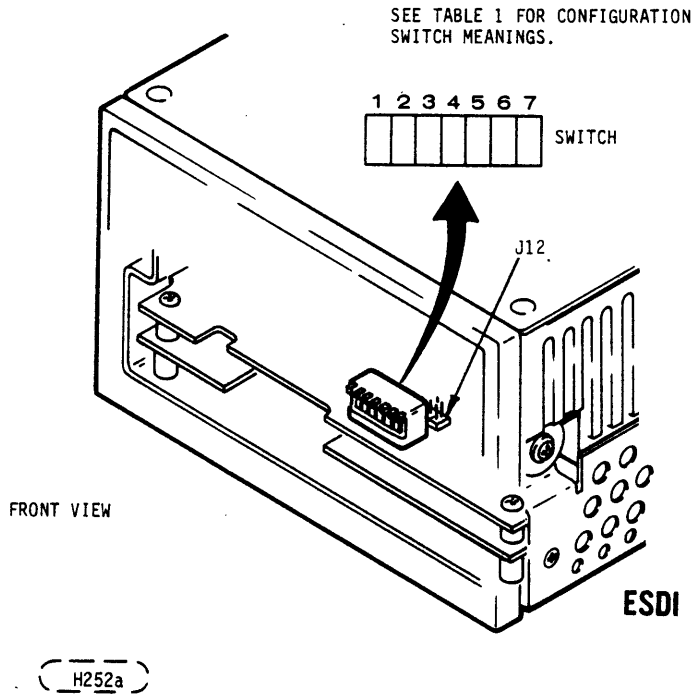


FIGURE 3-6A. CONFIGURATION SWITCH LOCATION (ESDI ONLY)

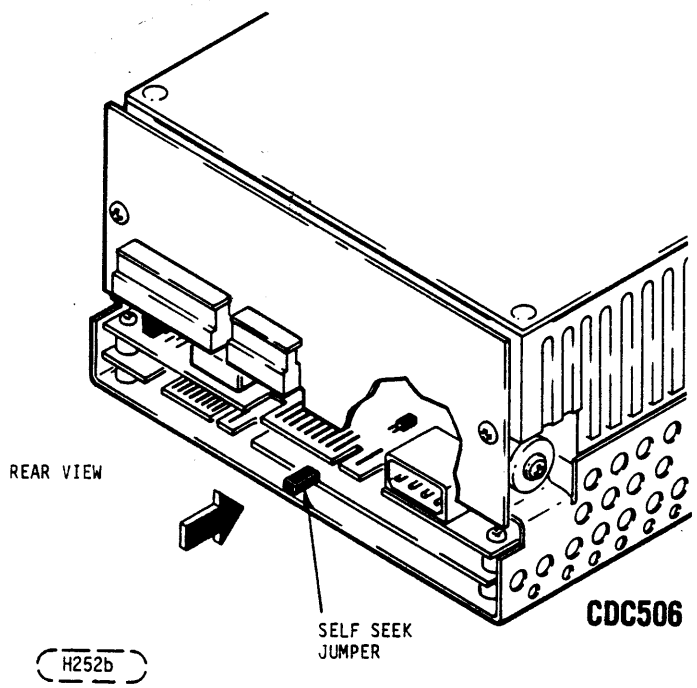


FIGURE 3-6B. SELF SEEK JUMPER (CDC506 ONLY)

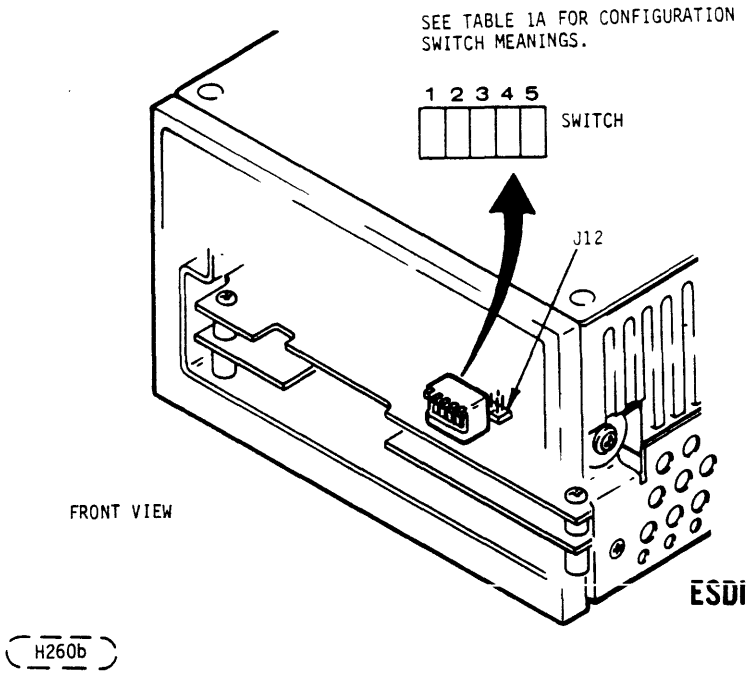


FIGURE 3-6C. OPTIONAL CONFIGURATION SWITCH LOCATION (ESDI ONLY)

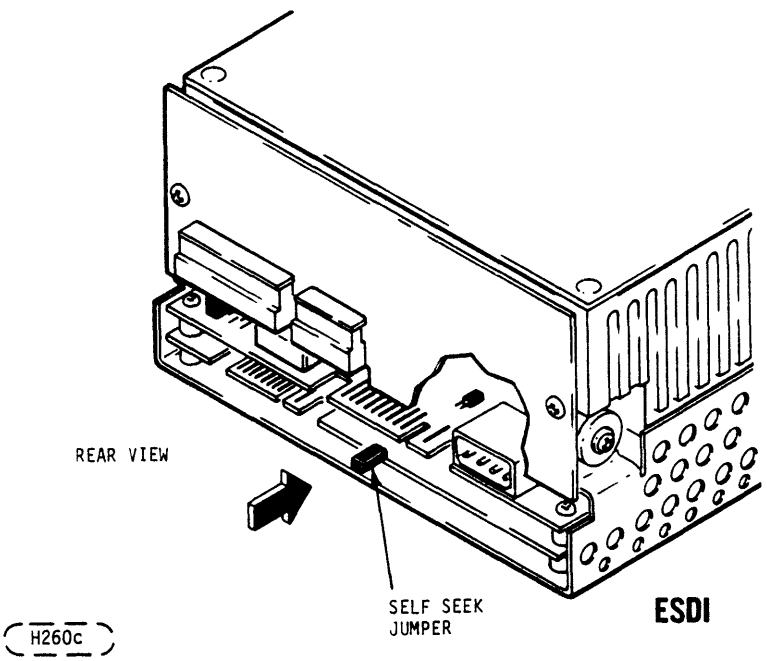


FIGURE 3-6D. OPTIONAL SELF SEEK JUMPER (ESDI ONLY)

TABLE 3-1. CONFIGURATION SWITCH SETTINGS (ESDI ONLY)

SWITCH NO.	ON	OFF
SW1-1	Self-Seek	Normal
SW1-2	Motor Control Implemented (1)	Motor Control Not Implemented
SW1-7	Serial Mode	Step Mode

	SWITCH NO.	
SECTORS/TRACK	SW1-3	SW1-4
17	ON	ON
16	OFF	ON
34	ON	OFF
32	OFF	OFF

	SWITCH NO.	
FORMAT MODE	SW1-5	SW1-6
Address Mark	ON	ON
Byte Clock	OFF	ON
Sector Pulse	OFF	OFF
Sector Pulse	ON	OFF

(1) When the SW1-2 switch is ON, a MOTOR ON command is required from the controller to start the spindle motor. When power is applied to the drive, the drive will generate an ATTENTION signal and activate Standard Status Bits 8 and 9 signifying "Power On Reset Conditions Exist" and "Spindle Motor Stopped". The controller must then respond with a command to Reset the Interface ATTENTION line and also the Start Motor Command in order to start the spindle motor.

NOTE: This procedure is required anytime that the "Power On Reset Condition Exists" status bit is received by the controller if the "Motor Control Implemented" switch is ON.

TABLE 3-1A. OPTIONAL CONFIGURATION SWITCH SETTINGS (ESDI ONLY)

SWITCH NO.	ON	OFF
SW1-1	Motor Control Implemented (1)	Motor Control Not Implemented

	SWITCH NO.	
SECTORS/TRACK	SW1-2	SW1-3
17	ON	ON
16	OFF	ON
34	ON	OFF
32	OFF	OFF

	SWITCH NO.	
FORMAT MODE	SW1-4	SW1-5
Address Mark	ON	ON
Byte Clock	OFF	ON
Sector Pulse	OFF	OFF
Sector Pulse	ON	OFF

(1) When the SW1-1 switch is ON, a MOTOR ON command is required from the controller to start the spindle motor. When power is applied to the drive, the drive will generate an ATTENTION signal and activate Standard Status Bits 8 and 9 signifying "Power On Reset Conditions Exist" and "Spindle Motor Stopped". The controller must then respond with a command to Reset the Interface ATTENTION line and also the Start Motor Command in order to start the spindle motor.

NOTE: This procedure is required anytime that the "Power On Reset Condition Exists" status bit is received by the controller if the "Motor Control Implemented" switch is ON.

4.1 INTRODUCTION

The general block diagram of the WREN II is shown in Figure 4-1. Other block diagrams will be used to aid in the description of the drives.

Logic signal names may be followed by the symbol "+L" or "-L". Active high (+4 volts for TTL or -0.8 volts for ECL) have "+L" while active low (+0.8 volts for TTL or -1.7 volts for ECL) have "-L". ECL signals may also indicate active high with "-P" and active low with "-N" suffix.

Integrated circuit pins will be identified by IC location and pin number. For example, "U25-12" is pin 12 of IC at location U25.

4.2 ASSEMBLIES

Figure 4-2 illustrates the physical placement of the major assemblies of the WREN II Disk Drive. The following paragraphs describe the operation of these assemblies.

4.2.1 MECHANICAL ASSEMBLIES

There are just two major subassemblies which make up a WREN II Disk Drive (Figure 4-2). The base assembly contains the media, filtration system and spindle motor. The base is built and tested as a unit and then mated with the actuator assembly. The actuator assembly contains the bobbin, coil, magnets, rotary arm and heads. After the actuator is mated to the base the information needed to position the heads is written on the bottom surface of the bottom disk. This operation is called servo track writing (STW). After STW the stop is installed and adjusted. The stop keeps the servo head over the servo data and will be adjusted only in connection with STW. The cover assembly is then installed with six screws. These operations are performed in special clean rooms to keep the media contamination free. For this reason the top cover of a WREN should not be removed. The assemblies nad components described in the following paragraphs are in an environmentally sealed area and shall be serviced at factory level depot ONLY.

See Maintenance Section 6 for the items of General Maintenance.

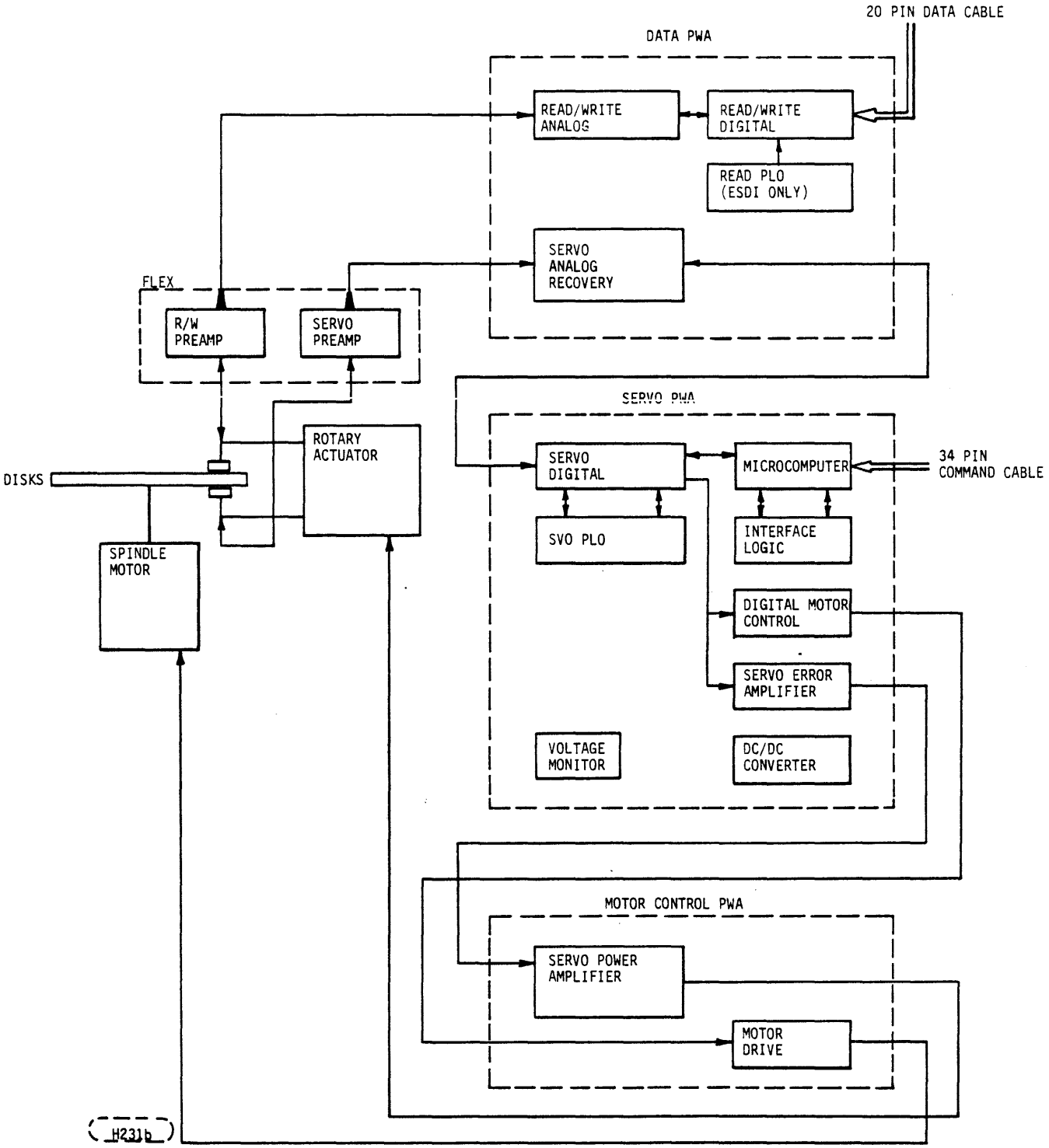


FIGURE 4-1. WREN II GENERAL BLOCK DIAGRAM

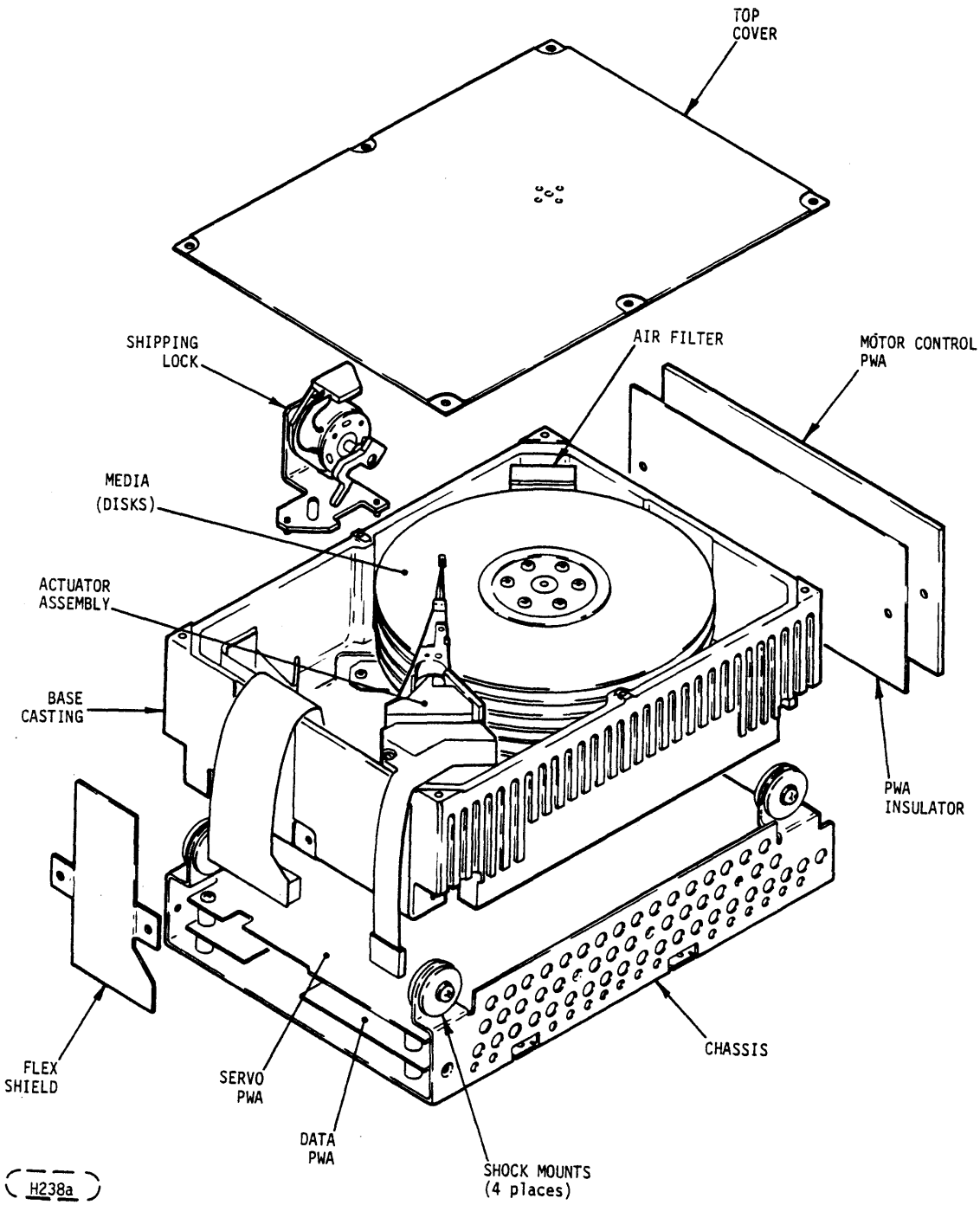


FIGURE 4-2. WREN II MAJOR ASSEMBLIES

4.2.1.1 ACTUATOR ASSEMBLY

The WREN II actuator is a rotary voice coil positioner. The voice coil can be thought of as a motor that moves through only a small angle. The motor stator consists of two permanent magnets, one upper and one lower, and a core bar (Figure 4-3). The motor rotor is a coil on a bobbin which fits around the stator core. By controlling the magnitude and direction of the rotor current, the rotor can be positioned any where in its range. The bobbin is attached to the rotary arm which provides the head mounting.

There are two bearings mounted in a bore thru the area. A shaft runs thru these bearings. This shaft is held in two V shape grooves on the housing which holds the magnets. The housing is later mounted to the base deck. Connection is made to the bobbin thru a three conductor flex cable.

The heads are mounted by screwing them into slots at the end of the actuator arm. Each head has a short flex cable on it which must be soldered to a flex cable on the actuator arm.

The flex cable on the actuator arm has two SSI115 integrated circuits on it. The signals to and from the nine data heads pass thru this circuit. The signal from the servo head passes through a preamp before being passed to the Data PWA.

Removal and replacement of the actuator is a depot level maintenance procedure ONLY.

4.2.1.2 BASE ASSEMBLY

The base assembly consists of the base casting, spindle assembly, head actuator assembly and filtration systems as shown in Figure 4-4.

The base casting is the frame of the drive and all assemblies mount to it. The base casting also divides the drive into sealed and unsealed compartments. The area above the base casting and under the cover is sealed and provides a clean environment. The heads in the WREN fly at only 10 to 14 microinches, therefore the air in the sealed compartment must be kept very clean.

The spindle to which the disks are attached is an integral part of the spindle motor. The disks are the recording media for the drive. The recording surface of each disk is coated with a layer of magnetic iron oxide and related binders. The WREN Disks also have a lubricant over the oxide. This reduces the friction when the heads are landing. The drive can have up to five disks, each separated by a spacer. The whole assembly is held together by a clamp plate which bolts to the top of the spindle hub. The assembly then is bolted to the base casting with the spindle shaft protruding through the base.

The spindle motor is a three phase brushless DC motor. The motor rotor mounted on the opposite end from the spindle has fan blades which provides some air flow to cool the electronics. A grounding spring rests on the center of the rotor and bolts to the base casting, this provides a path for any static electricity generated by the head-disk interface to flow to the ground.

The arm lock solenoid holds the arm and heads over the landing zone next to the spindle when power is not applied.

The first of the filtration systems is a breather filter. It is bolted over a hole in the top cover and provides clean air to equalize the pressure between the sealed compartment and the outside world. The second system is a recirculating absolute filter. It removes any foreign material that may be present in the sealed compartment. Air is pulled out of the filter by the low pressure created near the spindle. Air then can circulate thru open areas in the spindle and flow out across all the disks. Some of the air will flow through this filter whenever the disk is spun. Over the life of the drive all the air in the sealed compartment will be cleaned many times.

Any servicing of the spindle assembly, spindle motor and filters is a depot level procedure ONLY.

4.3 FUNCTIONAL DESCRIPTION

4.3.1 GENERAL

This description is organized into the following major headings:

- Overall Drive Control System
- Head Positioning System
- Read/Write System
- Auxiliary Systems

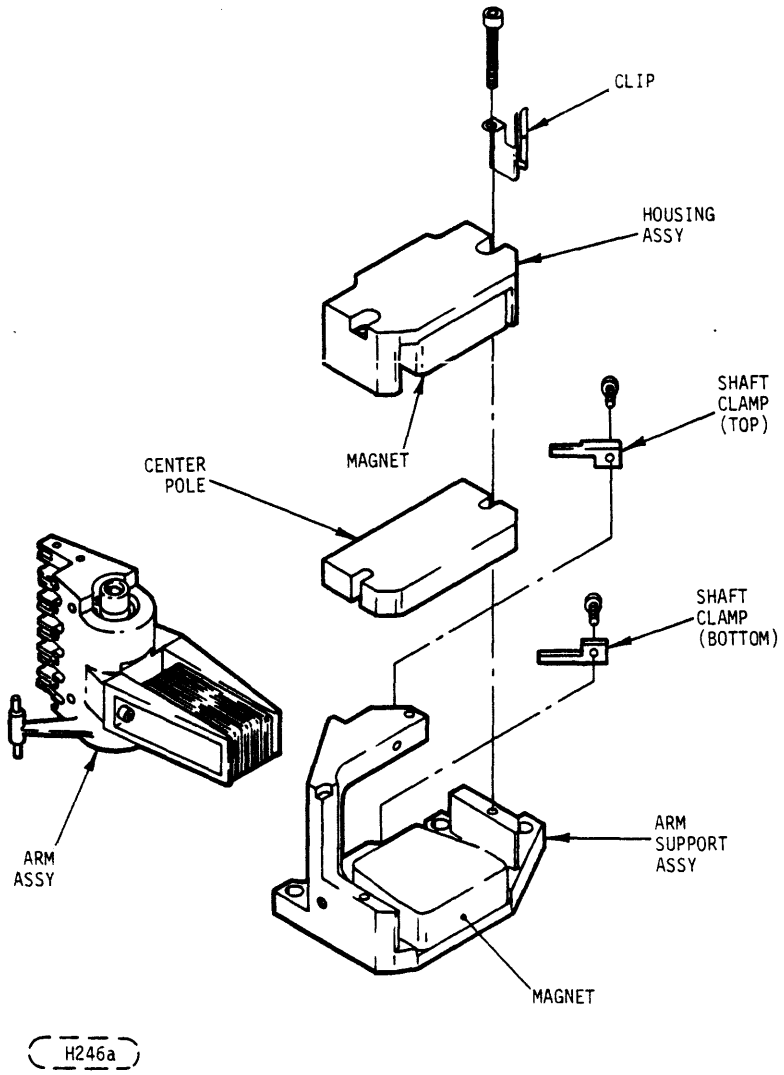


FIGURE 4-3. WREN II ACTUATOR ASSEMBLY

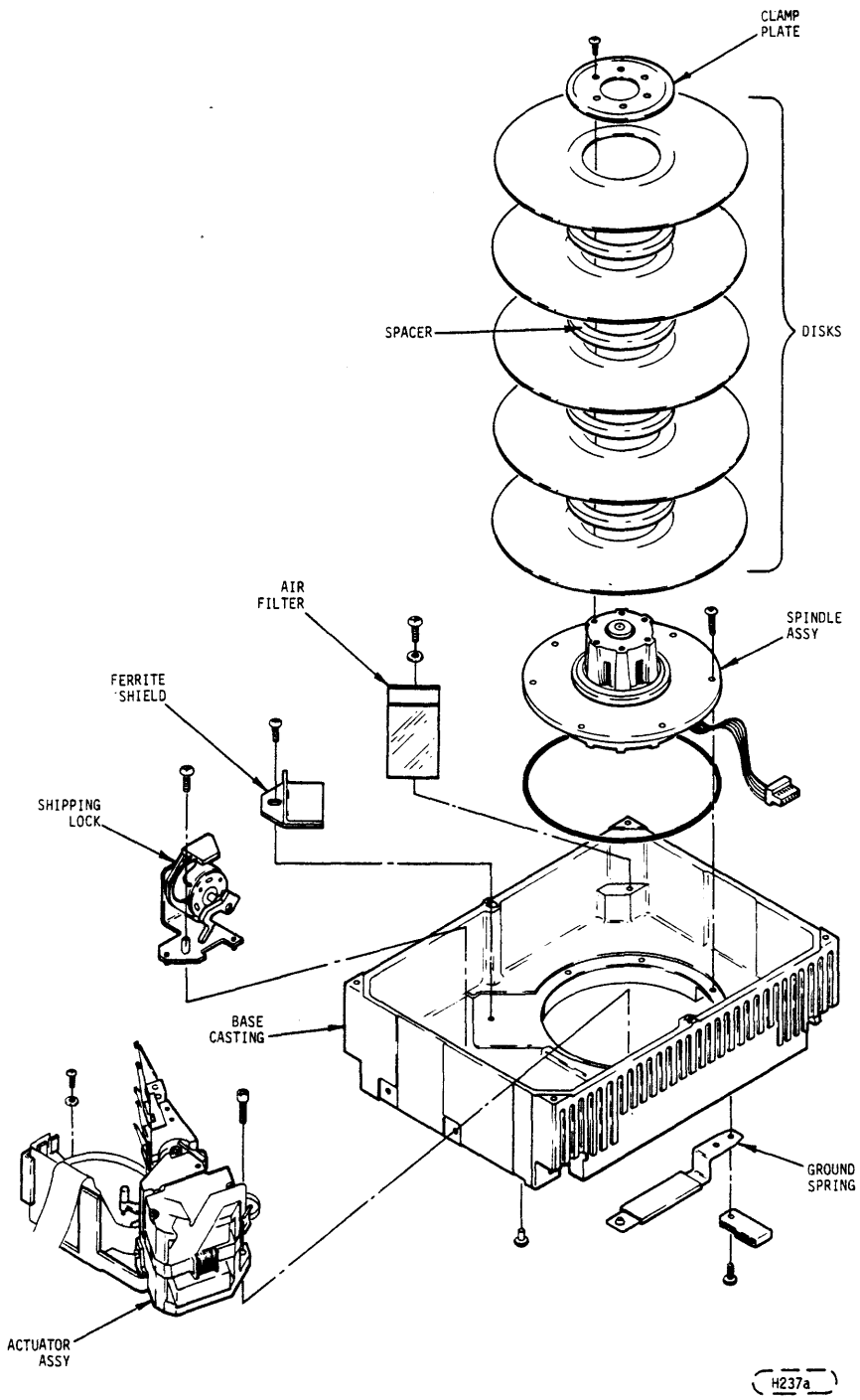


FIGURE 4-4. WREN II BASE ASSEMBLY

4.3.2 OVERALL DRIVE CONTROL SYSTEM

The WREN is under the control (excluding any control exerted by the controller via the interface lines) of the Microcomputer on the Servo PWA. The Microcomputer system is described in the following paragraphs. Any further details of the Microcomputer Theory must be taken from vendor publications for the various chips in the Microcomputer System.

4.3.2.1 MICROCOMPUTER OVERVIEW (CDC506 INTERFACE)

Figure 4-5 shows a simplified block diagram of the microcomputer. The microcomputer is an 8749 with two kilobytes of internal program memory. The microcomputer has no control of the read/write section with the exception of the write current magnitude.

When a step is received from the command cable interface, it is synchronized with the microcomputer clock and applied to the input of the 8749. This causes a counter to be incremented with each step pulse. The interface direction line is latched with the step pulse and applied to one of the Bus Port inputs. These two lines have all the information needed to cause a seek operation.

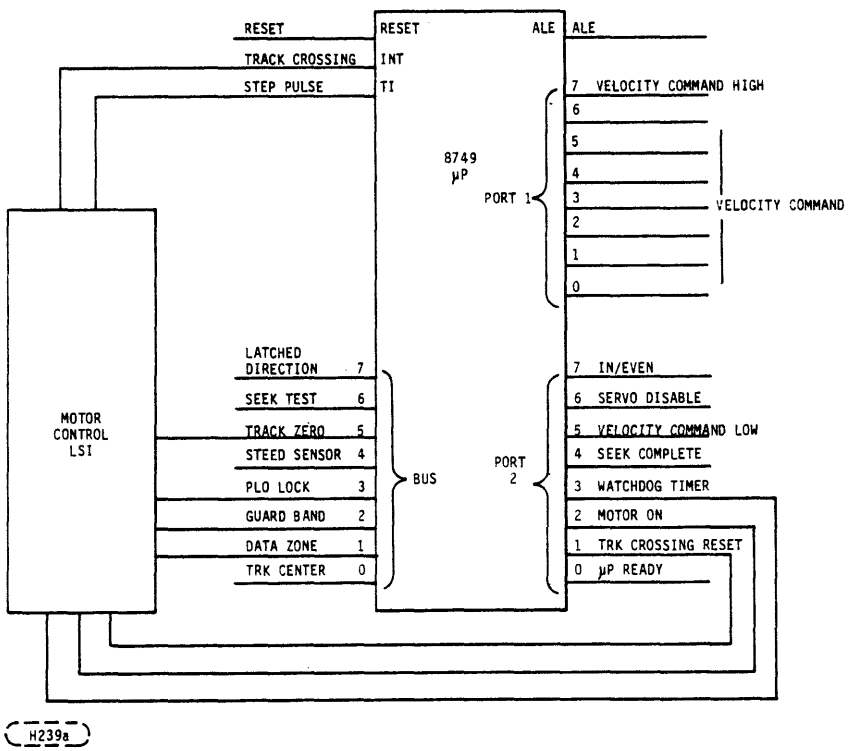


FIGURE 4-5. WREN II MICROCOMPUTER BLOCK DIAGRAM

When a seek is in progress, track-crossing pulses are generated in the servo LSI logic; these are applied to the 8749's Interrupt input. This input remains active until the Interrupt is serviced and a track-crossing reset is sent to the servo LSI on a Port 2 line. In this manner, the microcomputer keeps track of all incoming step pulses and track crossings that occur. The address latch enable (ALE) signal is sent to the spindle motor control as a clock for the speed regulator. During a seek, a seven-bit velocity command is output on Port 1 and goes to a D/A converter in the servo amplifier. The eighth bit on Port 1 is active for a high velocity command, and inactive for a low velocity command. A line from Port 2 titled "VCLO" (Velocity Command Low) is active for a low velocity command, and inactive for a high velocity command. The FINE signal puts the servo system into either the fine or coarse mode of operation. This signal is used in conjunction with the IN/EVEN lines. In refers to a seek from a lower to a higher numbered cylinder. In the coarse mode, this line is active during a forward seek and inactive during a reverse seek. When the drive switches to the fine mode this line is active when the target track is even and inactive when the target track is odd.

The Power On Reset signal originates from port 2 by setting even and servo disable. This enables the current regulator in the spindle motor control. When it is inactive, it enables the speed regulator. It is also used to provide appropriate resets to sequential logic contained in the drive electronics. During start-up, motor speed is monitored on the Bus Port from the speed sensor line. The phase lock oscillator (PLO) lock line is continuously monitored. Also during start-up, the servo is disabled via the Servo Disable line.

When the servo PLO is locked and the spindle motor is up to speed, head loading can commence. This is accomplished by the microcomputer issuing a velocity command, detecting guard band, performing a seek to track zero and switching back to fine mode on cylinder zero. The data zone latch is set by Index. Index code is written only in the data zone. This enables the microcomputer to distinguish between the data zone and the start zone.

There is a guard band latch external to the microcomputer that will disable the servo if guard band is encountered after the initial head load.

There is one other input to the Bus Port, called seek test. This input can be grounded with a jumper shunt to cause the drive to execute a continuous seek test following head load and the calibrate operation.

With the completion of head load, the microcomputer puts the drive through an automatic calibration procedure. During the calibrate sequence, a test seek is performed and timed by the microcomputer. When the microcomputer detects that the test seek is too slow, a short pulse is output on the Velocity adjust line. This pulse causes the automatic gain control (AGC) amplifier gain to decrease one step. This sequence is then repeated until the test seek is performed in the required time. The drive then returns to cylinder zero and sets the ready line. The ready line serves to indicate that the drive is on cylinder and ready to read or write. It will be false whenever the heads are outside the data zone. The SEEK COMP line issues a pulse at the end of a seek to set the seek complete latch.

A servo will be disabled and the ready line made false at any time that loss of servo PLO lock is detected. A timing diagram for the step-pulse synchronizer is shown in Figure 4-9.

4.3.2.2 MICROCOMPUTER FIRMWARE ROUTINES (CDC506 INTERFACE)

The flow charts that follow illustrate the manner in which the microcomputer controls servo operation in the WREN. Figure 4-10 shows a chart of the primary modules that make up the WREN firmware. On power-up, the program starts and always returns to the Main Idle module. During start-up, the program exits the Main Idle module and goes to the System Initialize module. Following System Initialize, it then goes to the Head Load module. Upon completion of Head Load, the program branches back to the Main Idle Loop.

A. Main Idle Module

When the drive is powered up, the SINIT module is called to perform the system initialization. Upon return from SINIT, a drive status check is done. The status check looks for PLO Lock, Data Zone, and Proper Spindle Speed. If PLO Lock or Data Zone is lost, if guard band is detected, or if spindle speed is not within tolerance an error counter is incremented. If the count overflows, the servo is disable and the main routine starts over.

If the drives' status is good the step register is checked. If no step pulses have been received the routine loops back to the status check. Execution continues in this loop until steps are received. When steps are detected the SEEK Module is called to move the heads. After returning from SEEK, if the error flag is not set, control loops back to the status check. However, if the error flag is set, the drive will attempt a short recovery. Failing this, SINIT is called and execution starts over.

This action is shown in the flow chart of Figure 4-6.

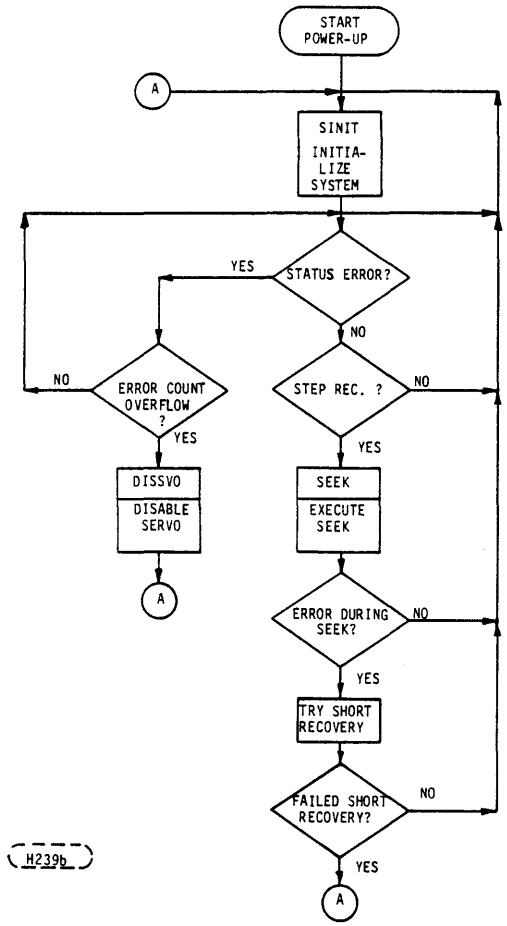
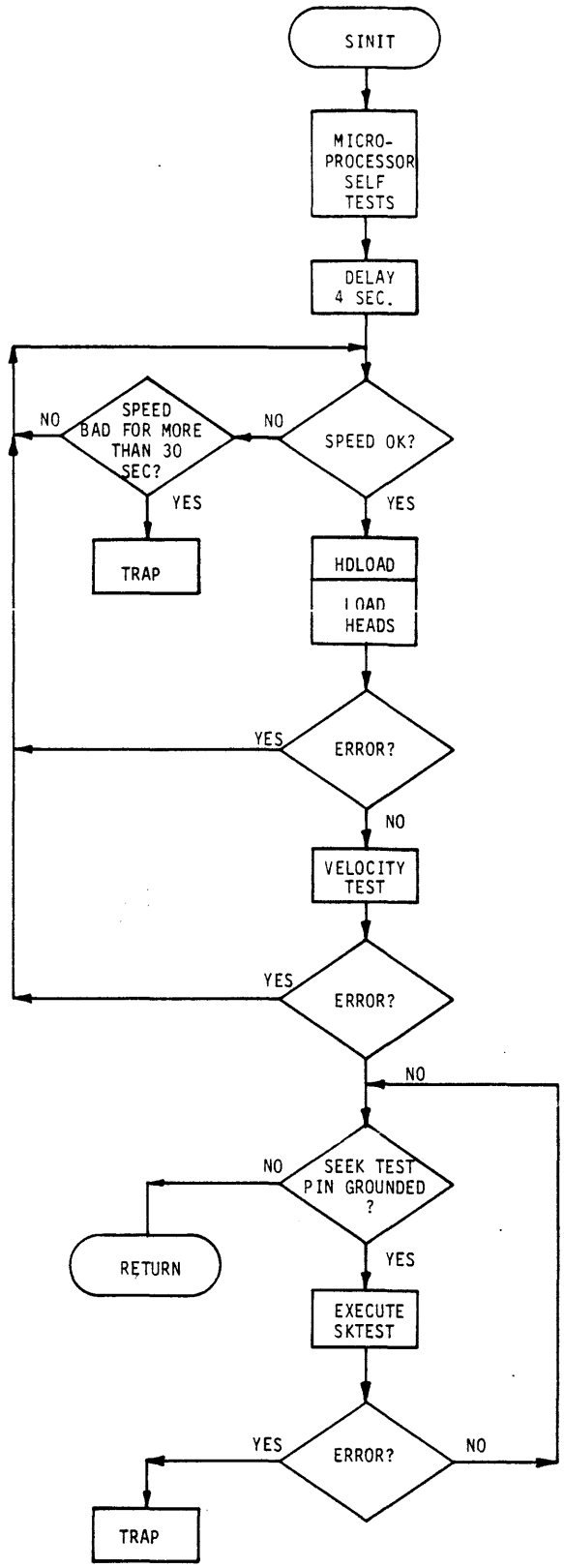


FIGURE 4-6. MAIN IDLE MODULE

B. SINIT - System Initialize Module

This module begins with microprocessor tests, then delays 4 seconds to allow spindle speed to come up and stabilize. The speed is then checked; if the speed is not correct within 30 sec. execution will go to the trap loop. The only way to get out of the trap loop is to cycle the drives power off and on. If the speed is within tolerance, the HD LOAD Module is called to load the heads. If an error occurred during head load, control loops back to the speed check. If no errors, a velocity test is conducted.

The velocity test is a series of seeks with the velocity being incremented each seek. This is repeated until the test passes. If the test is not passed after 64 seeks, the test fails and control goes back to the speed check. After passing the velocity test the microprocessor tests for the presence of the seek test jumper. If the jumper is present, the seek test is performed until the jumper is removed or an error occurs. Should an error occur during seek test, execution goes to the trap loop. When the microprocessor tests the seek test line and the jumper is not present, control returns to the main module. This action is shown in the flow chart of Figure 4-7.



H229a

FIGURE 4-7. SYSTEM INITIALIZE

C. HDLOAD-Head Load Module

The Head Load procedure begins with the microprocessor insuring that the arm is against the inner arm restraint. Next a flag is checked indicating whether or not the heads have been loaded since power-up. If the flag is not set, a guard band check is made. Should the flag be set from a previous head load, then a check is made for data zone and guard band. Detection of either data zone or guard band will result in the servo being disabled, and control will return to the SINIT module.

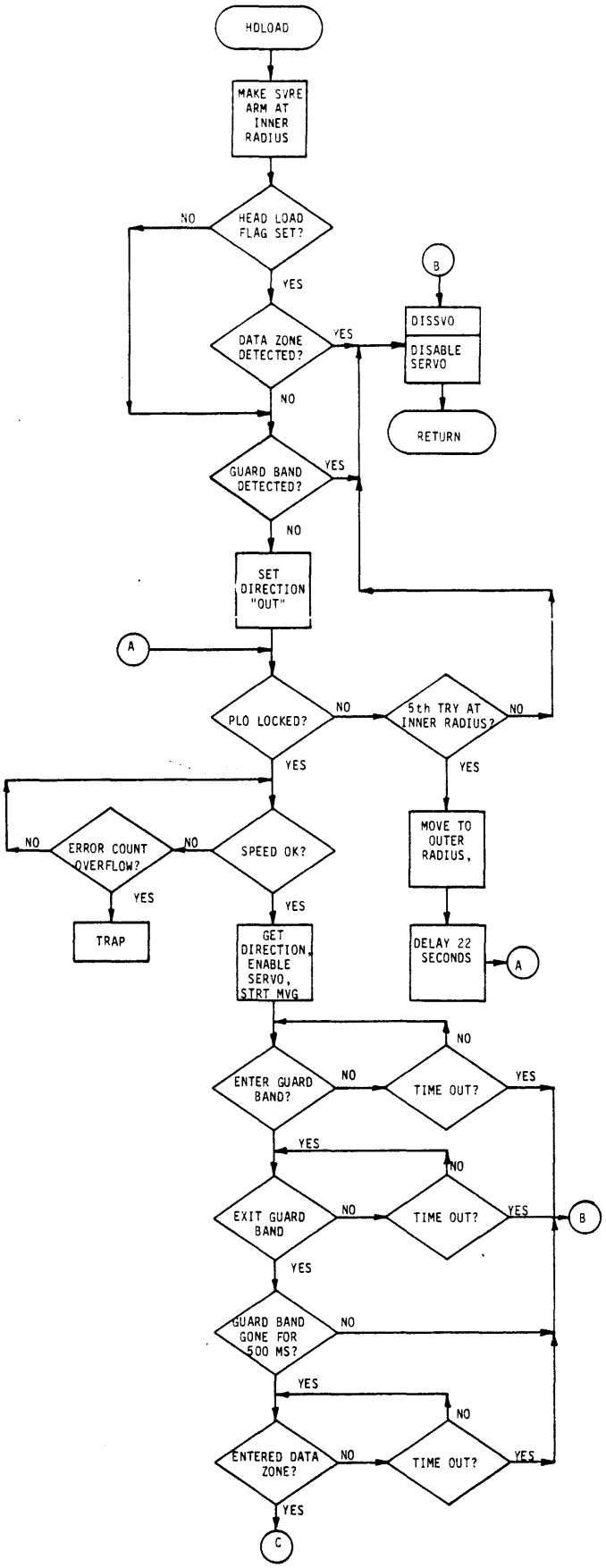
After passing the previous check(s), arm direction is set "out" and PLO Lock is checked. If PLO is not locked and if less than 5 head load attempts have been made, the servo will be disabled and control will return to SINIT. After the 5th attempt, the microprocessor will try to move the arm to the outer restraint and load heads from there.

With the PLO Locked, the spindle speed is checked. If the speed is not correct an error count is incremented and the speed is checked again. This is repeated until the speed is correct or the error count overflows. Error count overflow will cause control to go to the trap loop.

After speed check the servo is enabled and the heads are slowly moved across the disk. The heads should enter guard band then exit guard band. The microprocessor will check to make sure guard band is gone for 500 ms, then data zone should be detected. These four events are time dependent. If a timeout should occur on any of the four previous events, the servo will be disabled and control returned to SINIT.

At this time the heads should be loaded on max track. The microprocessor next will set a "home" velocity and start a 3 second timer. If a drive status error occurs, or if track 0 is not seen before timeout, the servo will be disabled. When track 0 is detected the cylinder address register is set to 0 and the SKTERM module is called to wrap up the seek. Completing this, control returns to SINIT.

This action is shown in the flow charts of Figures 4-8A and 4-8B.



H229b

FIGURE 4-8A. HEAD LOAD (SHEET 1)

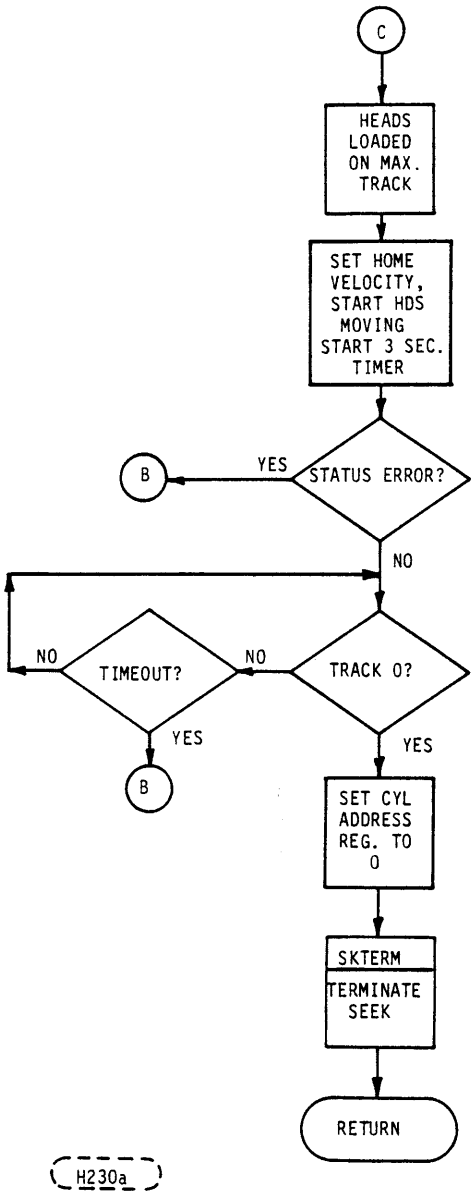


FIGURE 4-8B. HEAD LOAD (SHEET 2)

D. SEEK - Seek Module

The seek module is called by the Main module when the drive starts receiving step pulses. First, the SKINIT module is called to initialize the seek. Next, a check is made to see if step pulse are still coming in. If so, SKEX is called to execute the seek, if not, this call is skipped. On return from SKEX the error flag is checked. If the flag is set the servo is disabled and control returns to main. Next SKTERM is called to terminate the seek. Returning from SKTERM, the error flag is handled the same way as described above. Lastly, if more step pulses are received control loops to the top of the routine. If no more step pulses have been received control returns to main.

E. SKINIT - Seek Initialize Module

In the Seek Initialize module the direction input is read and stored. Next all initial conditions are saved and the step limit, or the maximum number of steps that can be made without exiting data zone, is calculated. Control then returns to the seek module.

F. TCINIT - Track Crossing Interrupt

During a seek, as a cylinder is crossed, a track crossing interrupt will be received. The interrupt service routine will update a track crossing register. The track crossing flag is set and interrupt logic cleared before returning.

The actions of D, E, and F are shown in the flow chart of Figure 4-9.

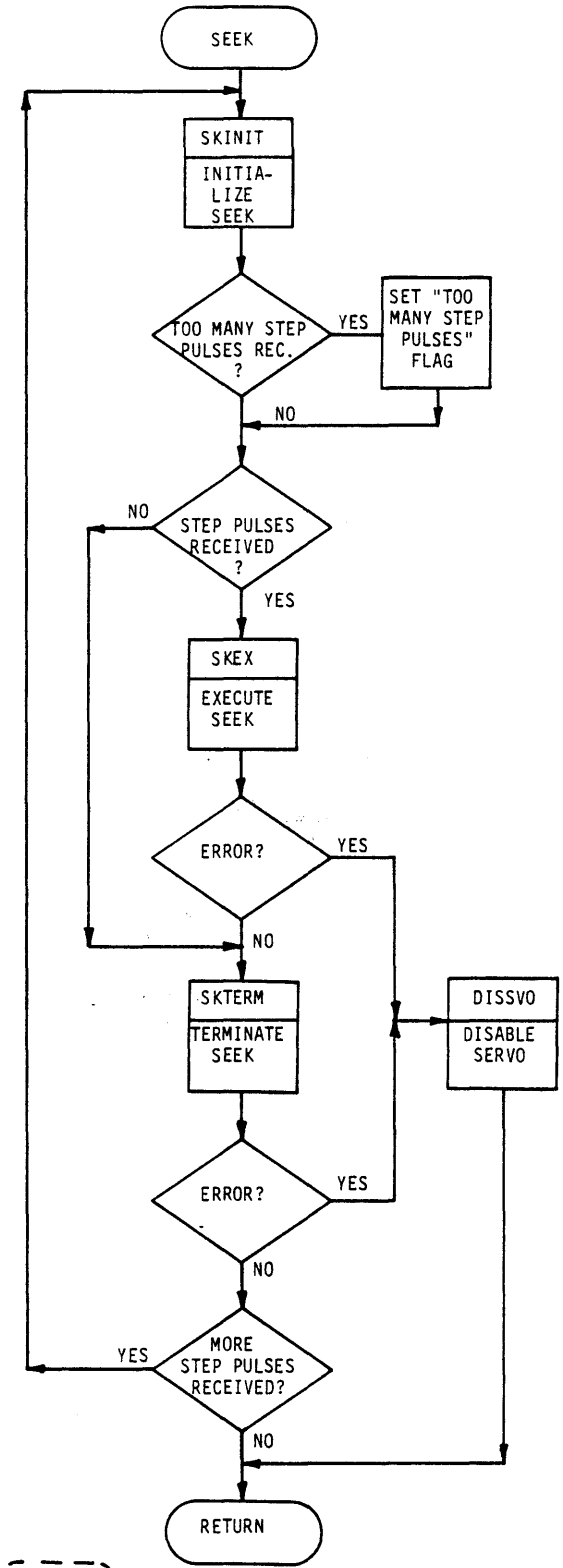


FIGURE 4-9. SEEK MODULE

G. SKEX - Seek Execute Module

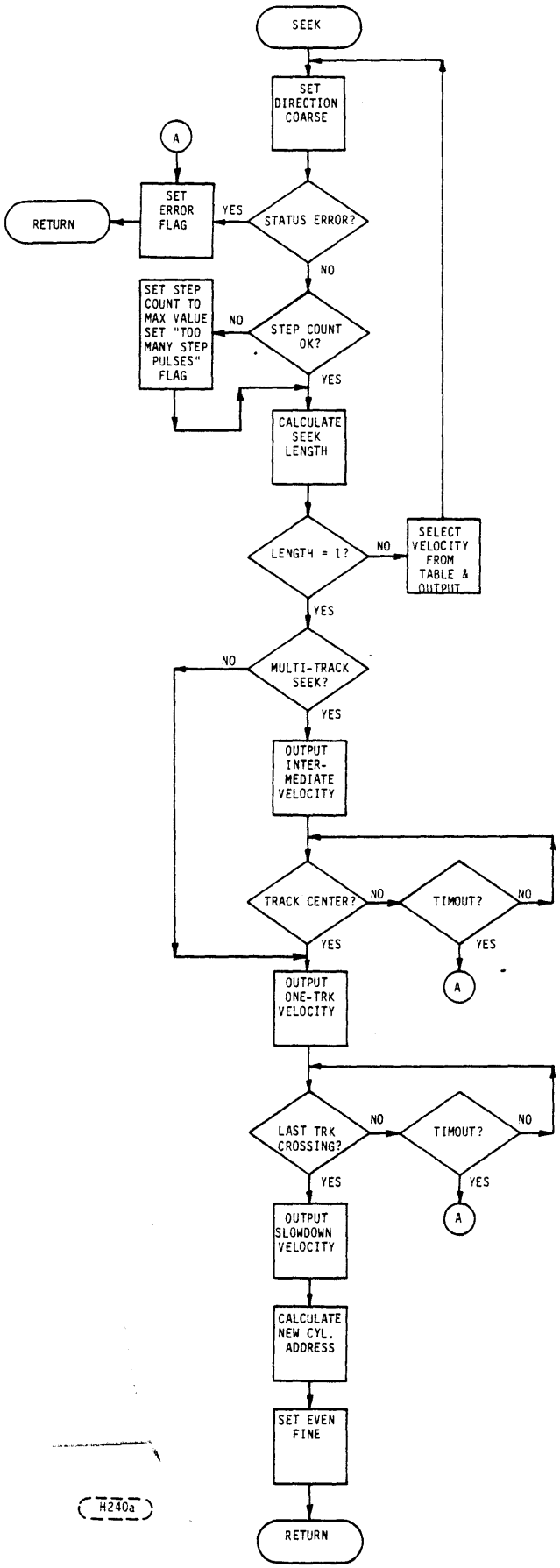
First the microprocessor sets the direction and coarse mode, then checks the drive's status. The number of step pulses received is compared to the limit calculated in SKINIT. If the limit is exceeded the step register is set to max cyl. or Track 0, depending on the direction set, and a "too many step pulses" flag is set. After the step pulse check, the seek length or number of tracks to go is calculated. If this distance is greater than 1 the corresponding velocity will be output. When the seek length is determined to be 1 the microprocessor will decide if the seek was originally a one-track seek or not. On a one track seek the one track velocity is output. On multi-track seeks an intermediate velocity is output, followed by a timed check for the center. If the timeout occurs before track center is detected an error flag is set and a return to SEEK follows. After track center is found, the one track velocity is output. At this point the last track crossing should be seen before timeout or the error flag will be set and control returned to SEEK. After the last track crossing, a slowdown velocity is output and the new cylinder address is calculated. Last, the microprocessor is even and fine, and control returns to SEEK.

This action is shown in the flow chart of Figure 4-10.

H. SKTERM-Seek Terminate Module

This module sets the write current first, then looks for track center. After track center is found the heads are allowed to settle. If more step pulses are being received or the "too many step pulses" flag is not set, control is returned to the SEEK module. When the flag is set the microprocessor will check to see if Step pulses are still being received and if so, will wait until the pulses stop. At this time the "too many step pulses" flag will be cleared and the step register restored to the step limit. Thus, when too many step pulses are received, the heads will seek to max track or track zero, depending on the direction. Lastly, if the direction is "out" a check for track zero is made. If track zero is not found the error flag is set before returning to SEEK, otherwise a normal return occurs.

This action is shown in the flow chart of Figure 4-11.



77738036-A FIGURE 4-10. SEEK EXECUTE MODULE 4-19

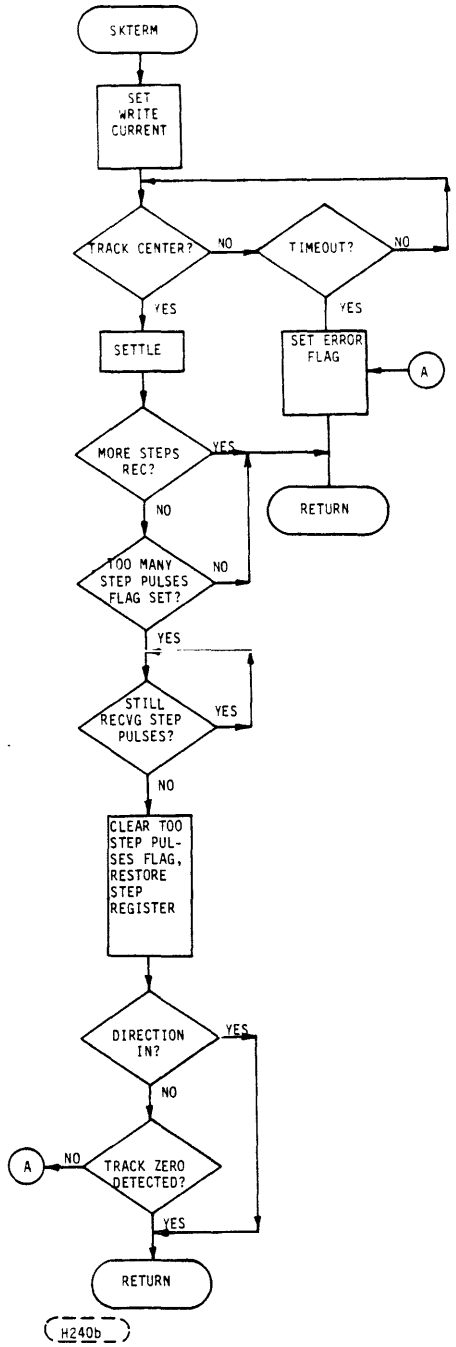


FIGURE 4-11. SEEK TERMINATE MODULE

I. DISSVO - Disable Servo Module

This disable servo routine first disables track crossing interrupts. Next the track crossing register/counter is turned off and cleared, as is the "too many step pulses" flag. The direction is set "in", servo disabled, and coarse mode set. Then the retry count is incremented and tested to see if this is the sixth retry. If so, control goes to the trap loop; if not, control is returned to the calling module. This action is shown in the flow chart of Figure 4-12.

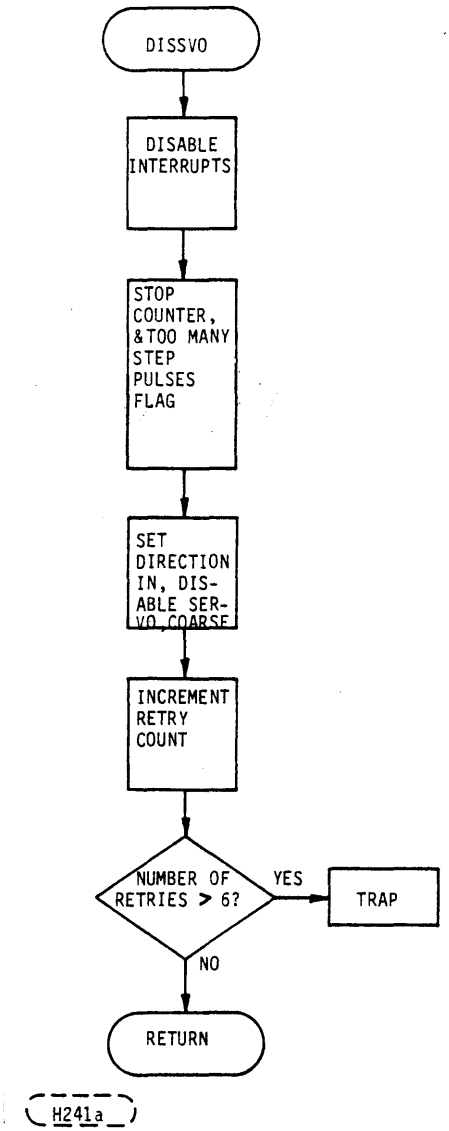


FIGURE 4-12. DISABLE SERVO MODULE

4.3.2.3 MICROPROCESSOR OVERVIEW (ESDI)

Figure 4-13 shows a simplified block diagram of the microcomputer. The microcomputer is an 8751 with four kilobytes of internal program memory. It also uses hardware memory mapping to increase the number of input and output signals. The microcomputer has no control of the read/write section with the exception of the write current magnitude.

When a step pulse is received, a counter is incremented. The interface direction line is latched with the step pulse and applied to one of the Bus Port inputs. These two lines have all the information needed to cause a seek operation.

The address latch enable (ALE) signal is sent to the spindle motor control as a clock for the speed regulator. During a seek, a seven-bit velocity command is output through Port 1 and goes to a D/A converter in the servo amplifier. The eighth bit is active for a high velocity command, and inactive for a low velocity command. A line from the port expander, titled "VCLO" (Velocity Command Low) is active for a low velocity command, and inactive for a high velocity command. The FINE signal puts the servo system into either the fine or coarse mode of operation. This signal is used in conjunction with the IN/EVEN lines. "In" refers to a seek from a lower to a higher numbered cylinder. In the coarse mode, this line is active during a forward seek and inactive during a reverse seek. When the drive switches to the fine mode, this line is active when the target track is even and inactive when the target track is odd.

During start-up, Power-On Reset is active for approximately 2 seconds. This enables the current regulator in the spindle motor control. When it is inactive, it enables the speed regulator. It is also used to provide appropriate resets to sequential logic contained in the drive electronics. During start-up, motor speed is monitored on the Bus Port from the Motor Speed line. The phase lock oscillator (PLO) lock line is continuously monitored. Also during start-up, the servo is disabled via the Servo Disable line.

When the servo PLO is locked and the spindle motor is up to speed, head loading can commence. This is accomplished by the microcomputer issuing a velocity command, detecting guard band, performing an RTZ, and switching back to fine mode on cylinder zero. The data zone latch is set by Index. Index code is written only in the data zone. This enables the microcomputer to distinguish between the data zone and the start zone.

There is one other input to Port 3, called Test Seek. This input can be grounded with a jumper shunt and causes the drive to go into a continuous test seek following head load and the calibrate operation.

With the completion of head load, the microcomputer puts the drive through an automatic calibration procedure. During the calibrate sequence, a test seek is performed and timed by the microcomputer. When the microcomputer detects that the test seek is too slow, a short pulse is output on the Velocity adjust line. This pulse causes the automatic gain control (AGC) amplifier gain to decrease one step. This sequence is then repeated until the test seek is performed in the required time. The drive then returns to cylinder zero and sets the ready line. The ready line serves to indicate that the drive is on cylinder and ready to read or write. It will be false whenever the heads are outside the data zone. THe SEEK COMP line issues a pulse at the end of a seek to set the seek complete latch.

A servo will be disabled and the ready line made false at any time that loss of servo PLO lock is detected.

4.3.2.4 MICROCOMPUTER FIRMWARE ROUTINES (ESDI)

The flow charts that follow illustrate the manner in which the microcomputer controls servo operation in the WREN II. Figure 4-14 shows a chart of the primary modules that make up the WREN II firmware. On power-up, the program enters and always returns to the Main Idle Module. During start-up, the program goes to the System Initialize module. Following System Initialize, it then goes to the Head Load module. Upon completion of Head Load, the program branches to the Main Idle Loop.

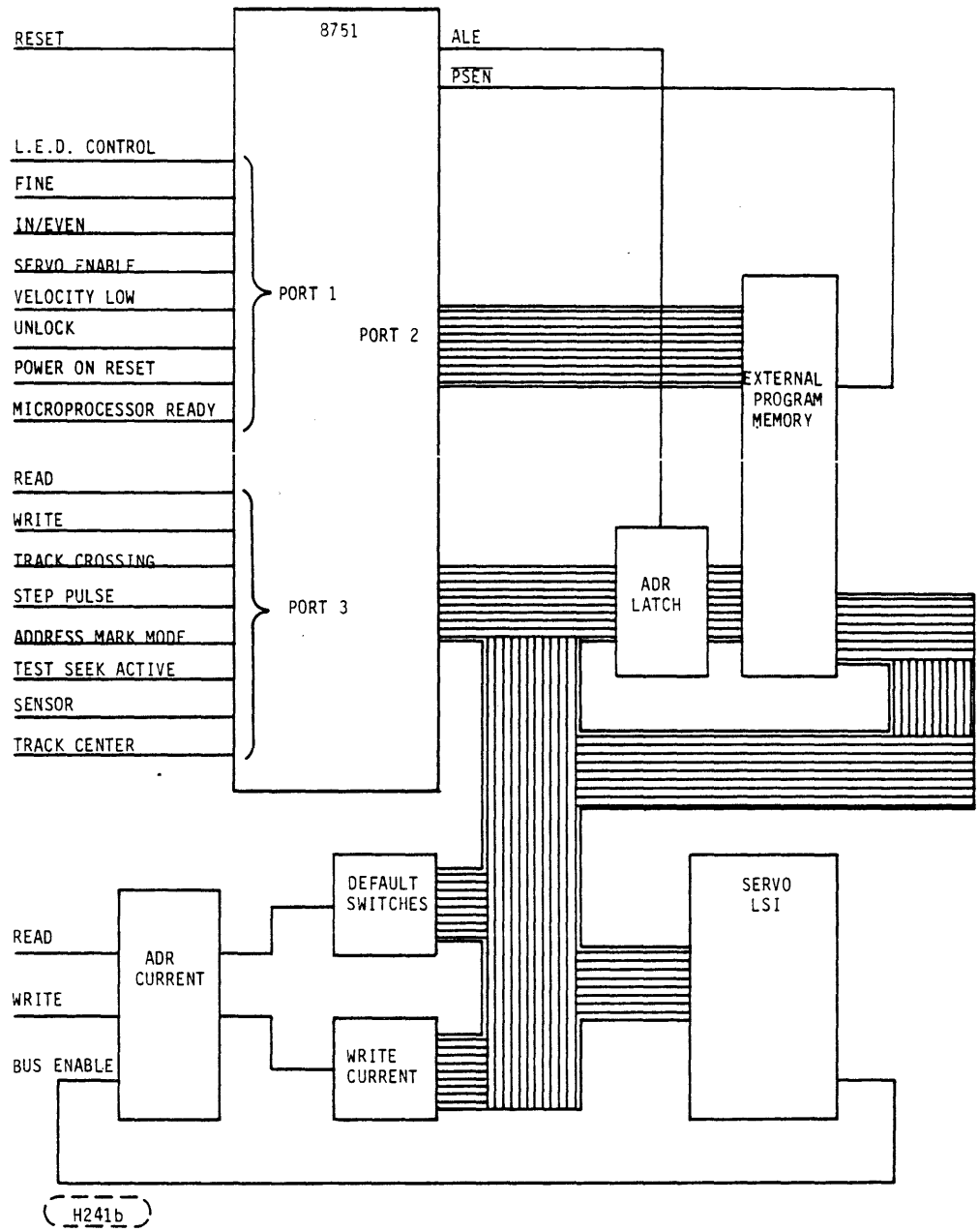


FIGURE 4-13. MICROCOMPUTER BLOCK DIAGRAM (ESDI)

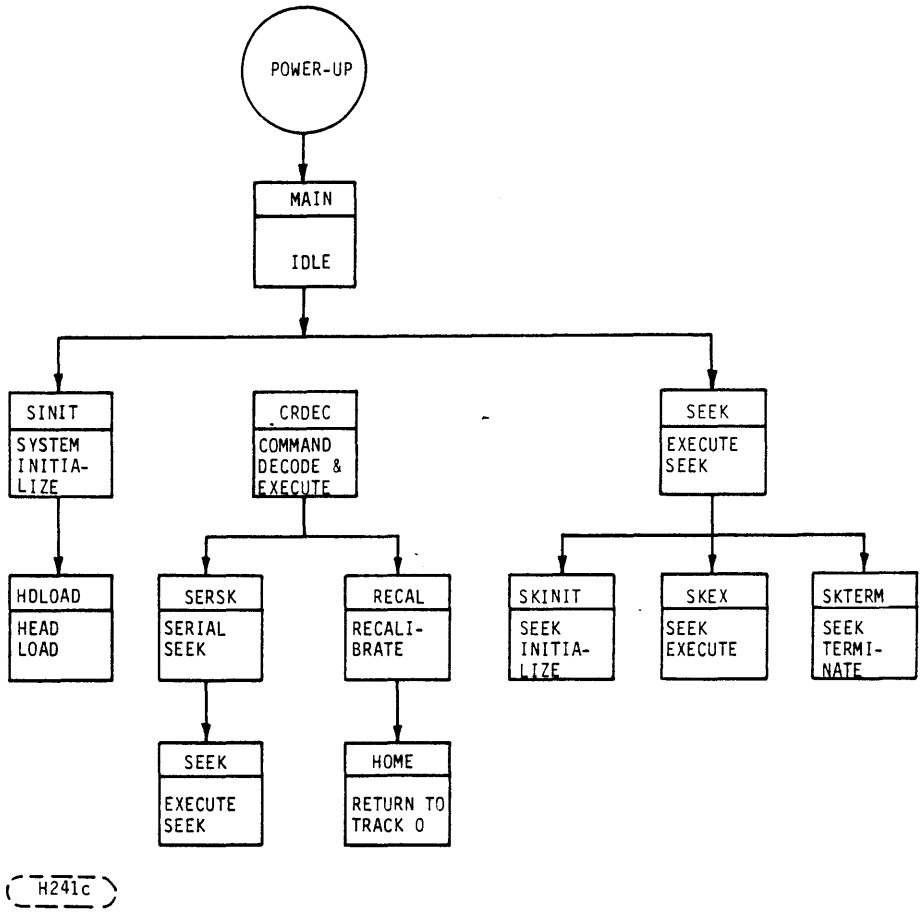


FIGURE 4-14. FIRMWARE MODULE CHART (ESDI)

A. "MAIN" Module

The "MAIN" module is entered from "SINIT", the initialization module. "Ready" and "Seek/Command Complete" are set, then a loop is entered which is only broken if a command is received (serial mode) or step pulses are detected (step mode). This loop consists of a status check, a speed check, and a step or command check. The status check is a check to make sure that "PLO lock" is true, and "Guard Band" and "Data Zone" are false. A bad status results in a call to "DISVO" to disable the servo. If the speed is not within tolerance, a filter register is incremented, as execution returns to the loop. If this filter runs down, then it is treated as an error. If step mode is in effect, and no step pulses have been received, nothing more is done, and execution loops back to check status again. Likewise, if in serial mode, and "Command Available" is false.

If "Command Available" is true, the "CRDEC" routine is called to read, decode, and execute the command. If step pulses are observed in step mode, the direction is saved, and "SEEK" is called.

In either case, if no errors occur, the "MAIN" routine is executed from the beginning. If there are errors, "Power-On Reset" is pulsed and "SBLOCK" is called to reinitialize before "MAIN" can be executed again.

This action is shown in the flow chart of Figure 4-15.

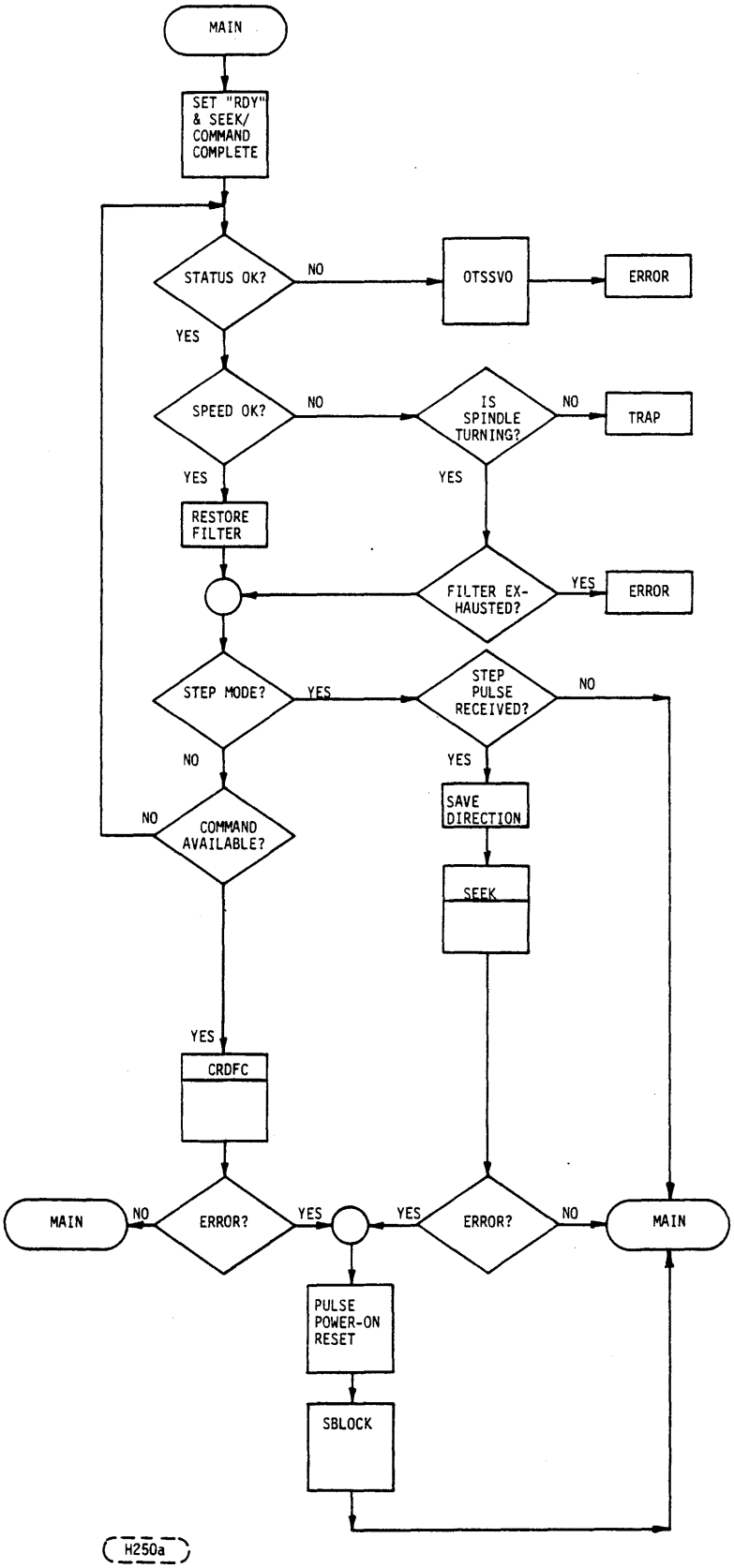


FIGURE 4-15. "MAIN" MODULE

B. "SINIT" Module

In System Initialization, it must be determined whether to set up for step mode or serial mode.

Serial mode can be set up to power up automatically, or a "motor on option" can be applied. If the latter is the case, nothing will happen until a "Motor On" command is received.

The motor is turned on, and after a delay, the subroutine "SBLOCK" executes the remainder of initialization. The flow chart for the "SINIT" module is shown in Figure 4-16.

C. "SBLOCK" Module

In "SBLOCK", the spindle is allowed to come up to speed, the arm is unlocked, and a retry counter is set to six, allowing for six retries if the system fails to power up properly.

Following a two second delay allowing the spindle speed to settle, the Head Load routine is called, followed by the Velocity Test and Seek Test routines. The flow chart for the "SBLOCK" module is shown in Figure 4-17.

D. "HDLOAD" Module

In the Head Load routine, the servo should be disabled and be in fine mode. If a Data Zone or Guard Band error is detected, a thirty second timeout is entered to wait for the error to disappear. If the error remains after thirty seconds, the trap state is entered. The flow chart for the "HDLOAD" Module is shown in Figure 4-18.

E. "LOADER" Module

After it has been verified that no Data Zone or Guard Band error exists, the Loader routine is called with an actual direction parameter. If an error is returned from this routine, the servo is disabled and another attempt is made to load the heads.

If this sequence is performed five times and the loader routine still fails, a slow move of the arm towards the outer radius is initiated. After a twenty-two second delay, the loader routine is called again with an inward direction parameter. If an error is returned, the servo is disabled and the trap state is entered.

The loader routine, first checks for a solid "PLO LOCK" signal, then verifies that the spindle speed is within acceptable limits. If the speed is unacceptable the TRAP routine is called immediately.

Load velocity is set in the direction indicated by the parameter. The servo is expected to enter and then leave guard band. Timeouts are set for both the entering and leaving of guard band. Expiration of either results in an error being returned.

After passing the guard band, the direction is reversed (invalid) until the guard band is detected once again. If it is not detected in time, an error is signaled.

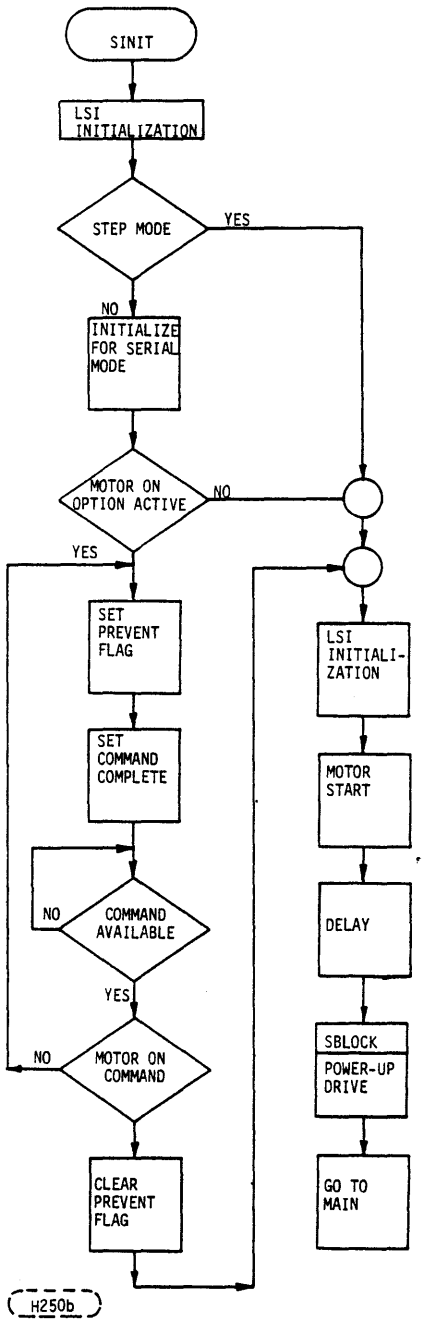


FIGURE 4-16. "SINIT" MODULE

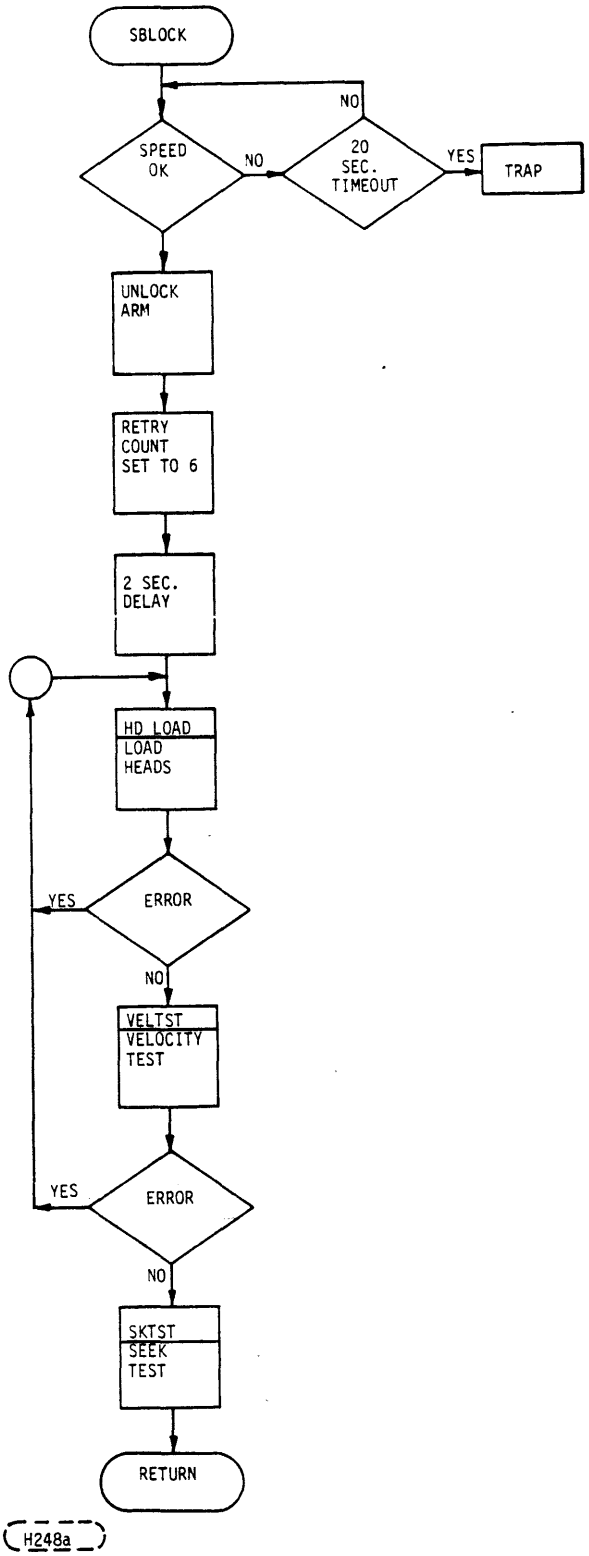


FIGURE 4-17. SBLOCK MODULE

When Guard Band is detected, Fine Mode is set and even track is set. A timeout is entered to wait for Data Zone. When it is detected, a return is executed.The flow chart for the "Loader" module is shown in Figure 4-19.

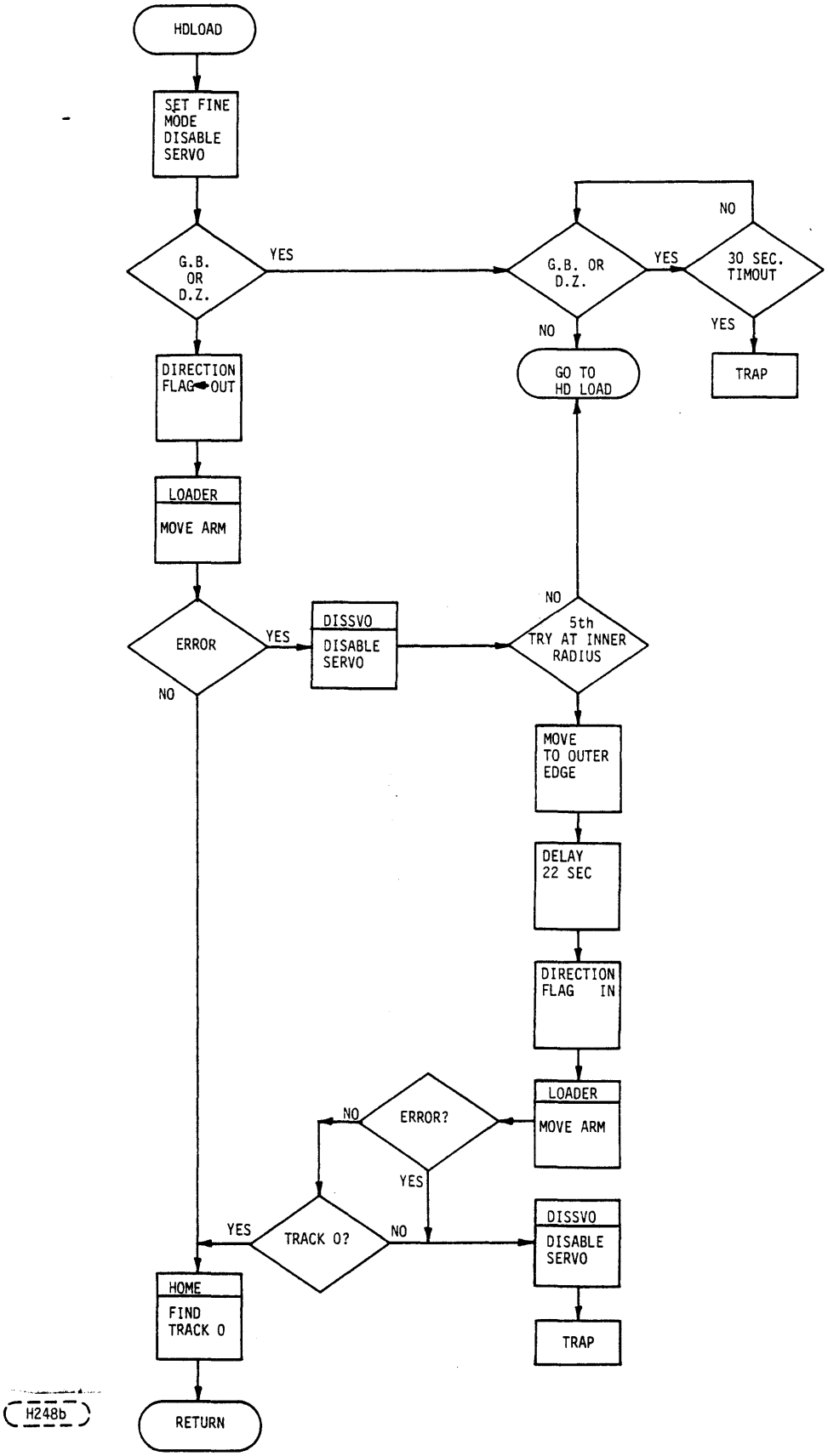


FIGURE 4-18. HD LOAD MODULE

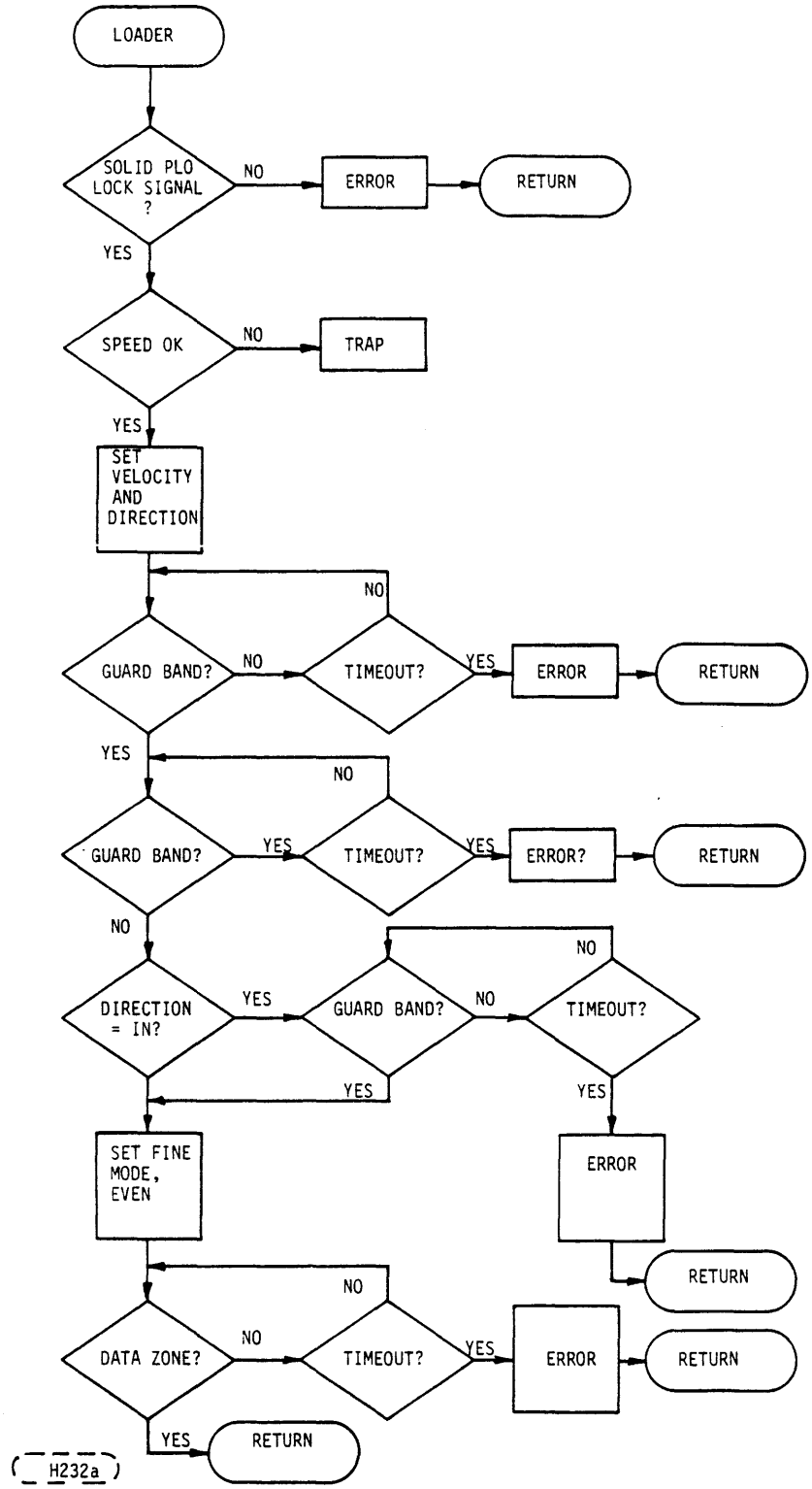


FIGURE 4-19. LOADER MODULE

F. "HOME" MODULE

Subroutine "HOME" first checks for Track 0. If this signal is true, the following paragraph is skipped. If the signal is false:

The cylinder address is compared with 4. If the cylinder address is greater than 4, a seek to cylinder 4 is performed. Then, from cylinder 4, or from a cylinder closer to 0, the RTZ velocity is set, along with coarse mode. Four seconds is allowed to find Track 0. A timeout is an error. When Track 0 is found, Fine Mode is set.

At this point, whether Track 0 was true upon entry, or recently detected, 50 milliseconds is allowed to find the "Data Zone" signal. A timeout results in an error. When "Data Zone" is detected, there is a 10 millisecond delay, after which the step register is checked for more step pulses. If more have been received, another 10 millisecond delay is executed. Then continues until 10 milliseconds go by without step pulses. At that time, the Track 0 signal is checked again. If true, a return is executed. If false, an error results.

The flow chart for the "HOME" module is shown in Figure 4-20.

G. "SEEK" Module

The seek routine, first calls the seek initialization subroutine, "SKINIT". If an error is returned, it is passed on to the caller. If there is no error, the seek execution subroutine, "SKEX" is called. If an error is returned, the servo is disabled by calling "DISSVO". Then a return is executed.

If "SKEX" returns no error, the seek termination subroutine is called. If more step pulses have been detected, the entire seek procedure is repeated. If no more step pulses have been detected, the address register is checked. If it is not zero, a return is executed. If it is zero, the Track 0 signal is checked. If it agrees, the return is executed. If it does not agree "HOME" is called before the return is executed.

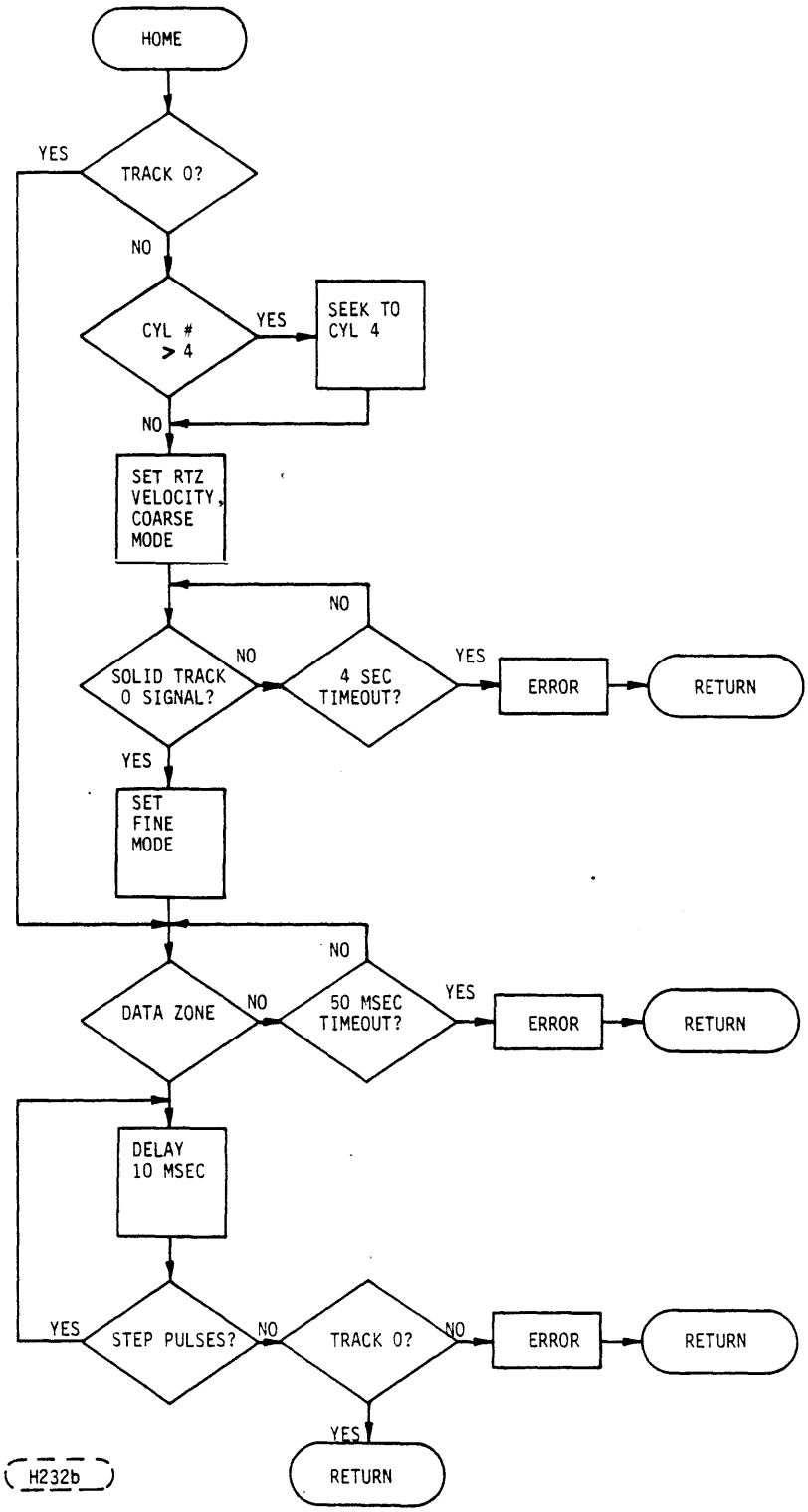


FIGURE 4-20. "HOME" MODULE

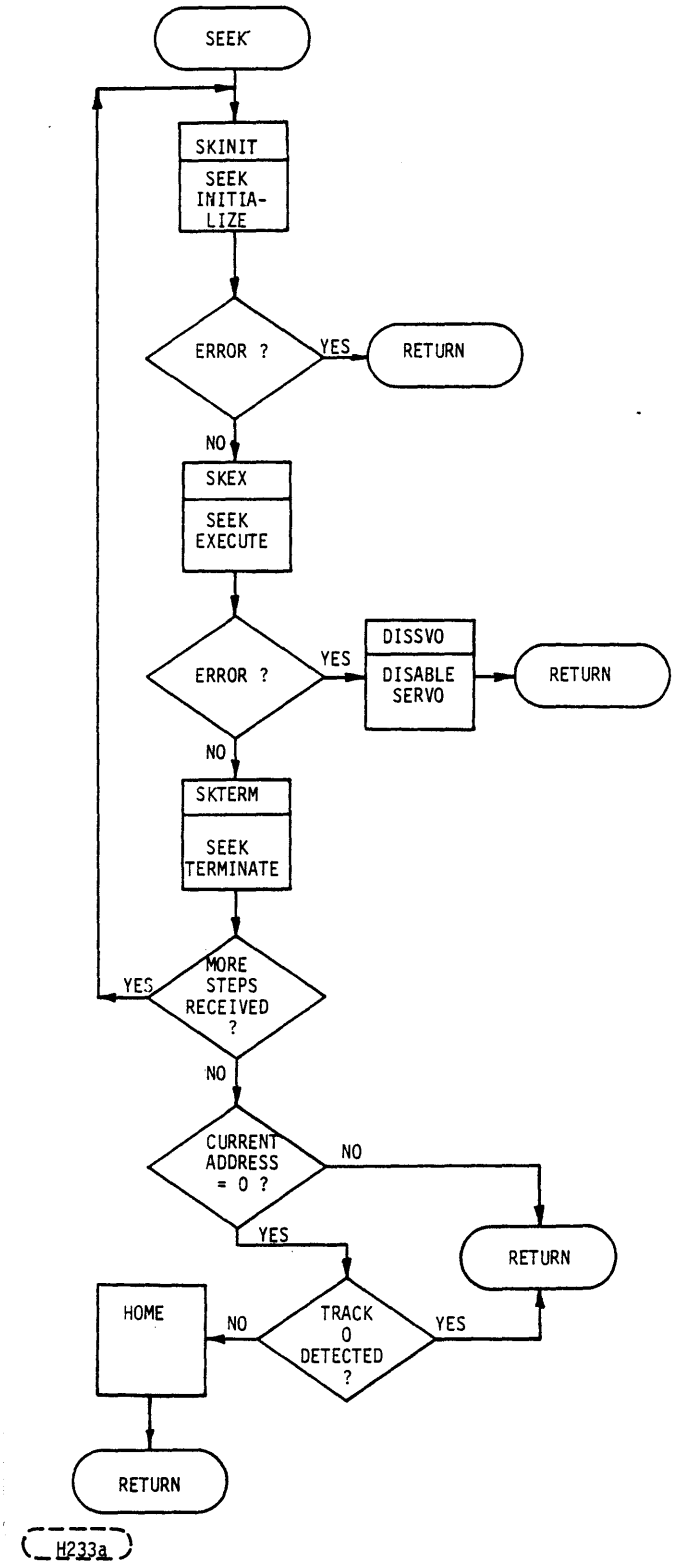


FIGURE 4-21. "SEEK" MOUDLE

H. "SKINIT" Module

Seek initialization "SKINIT", begins by calculating how many steps can be received without leaving the Data Zone. If there is an error in this calculation, it is returned to the caller. If no error is detected, a one-track seek velocity is set, along with direction and coarse mode. A return is then executed. The flow chart for the "SKINIT" module is shown in Figure 4-22.

I. "SKEX" Module

Seek execution, "SKEX", first enters a loop waiting for an indication that there is only one track to go in the seek. If there is a status error, or if it is discovered that the servo has moved too far, an error is returned. If no error, the velocity is updated each time the seek distance to go is determined. The seek continues until there is only one track to go.

When it has been determined that there is only one track to go is a multi-track seek, an intermediate velocity (between the one and two track seek velocities) is set. A five millisecond timeout is allowed to see "Track Center" become true. A timeout results in an error. When "Track Center" is detected, the one track seek velocity is set.

Regardless of the length of the original seek, the last track crossing is executed. If a ten millisecond timer runs down, it is an error. When the track crossing is detected, a slowdown velocity is set and the cylinder address is updated. Even or Odd is set, along with fine mode. After the write current is set, a return is executed. The flow chart for the "SKEX" module is shown in Figure 4-23.

J. "SKTERM" Module

Seek termination, SKTERM", sets write current, then waits for "Track Center". If it is not detected after 27 milliseconds, an error is returned. Otherwise the arm is allowed to settle before the return. The flow chart for the "SKTERM" module is shown in Figure 4-24.

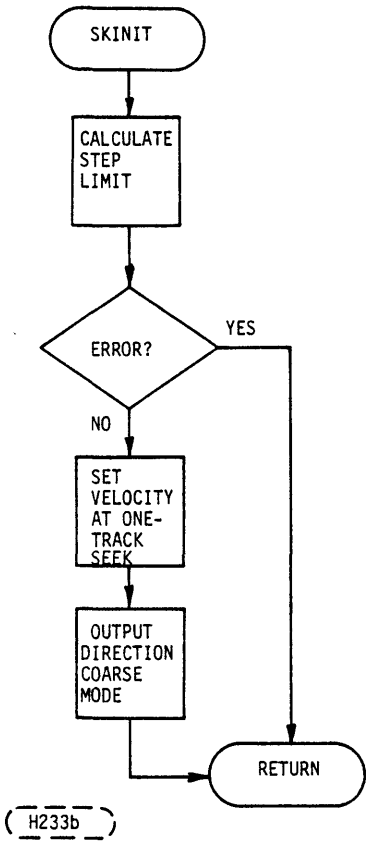


FIGURE 4-22. "SKINIT" MODULE

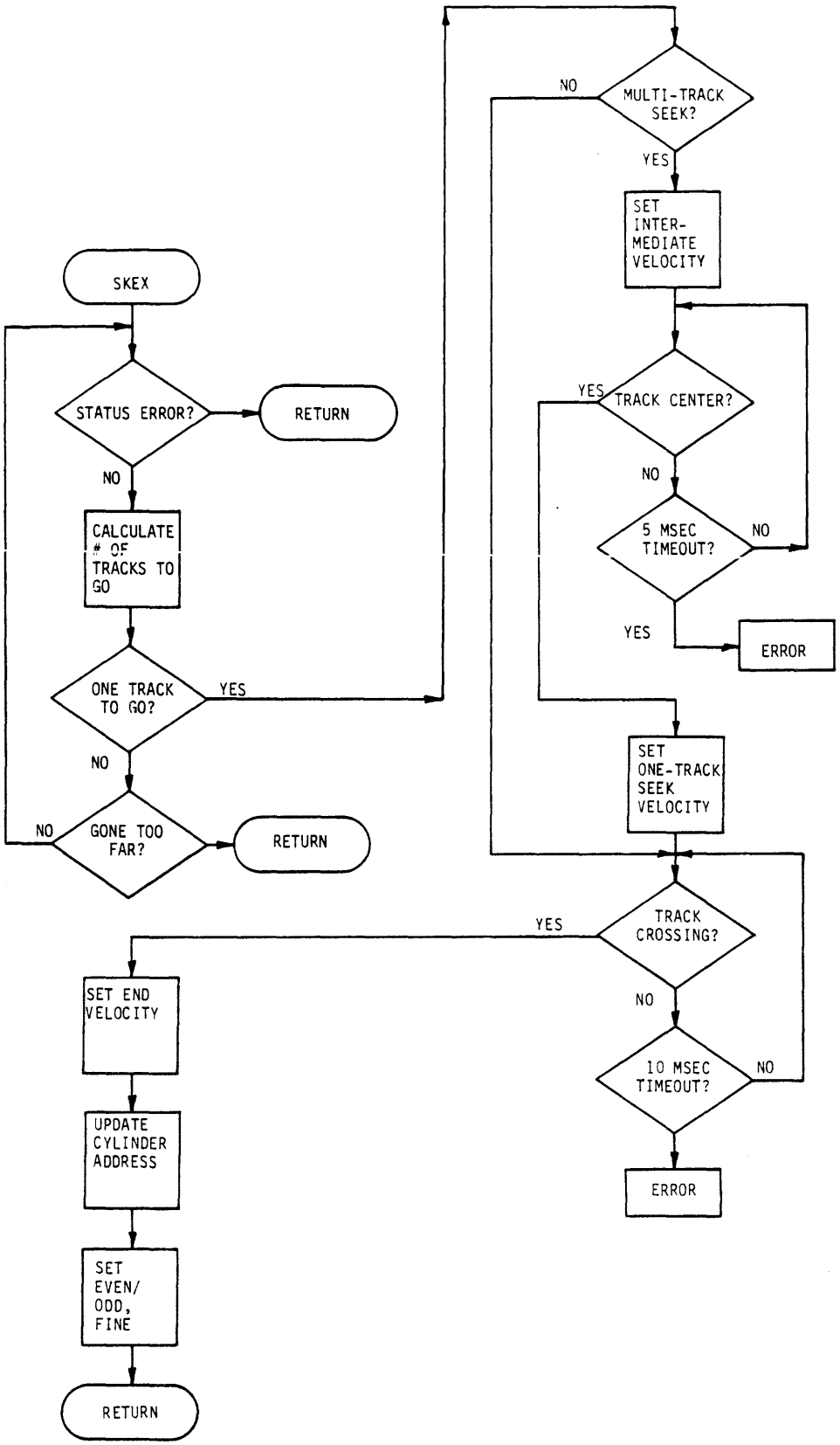


FIGURE 4-23. "SKEX" MODULE

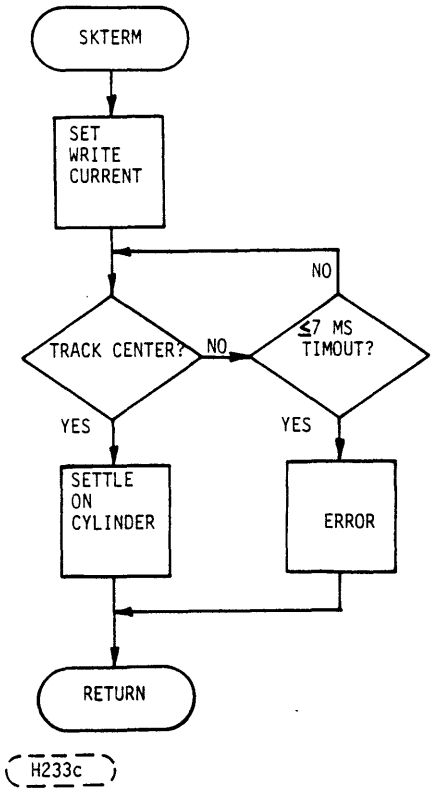


FIGURE 4-24. "SKTERM" MODULE

K. "CRDEC" Module

When "CRDEC" is entered, a "Command Available" has just been received, indicating a command. So "Command Complete" is cleared, then the command is read bit by bit. When all 17 bits (16 command bits and 1 parity bit) has been received, the parity bit is checked. If good, the appropriate command is executed. If the parity bit is not good, an error is returned. The flow chart for the "CRDEC" Module is shown in Figure 4-25.

L. "SERSK" Module

A serial seek command, "SERSK", checks the seek address (the lowest 3 nibbles of the command) to make sure it does not exceed the maximum cylinder. If the seek address exceeds the max cylinder, the "Invalid Command" bit is set and an error is returned. If a load seek address is read, the distance from the current address is determined. If the seek address and the cylinder address are equal, the seek distance is zero, and a return is executed. If the addresses differ, the direction is set, the step register is adjusted, and the seek performed by calling "SEEK", a step mode based routine. After the seek, execution is returned to the caller of "CRDEC". The flow chart for the "SERSK" Module is shown in Figure 4-26.

M. "RECAL" Module

A recalibration, "RECAL", is simply a call to the "HOME" Module. The flow chart for the "RECAL" Module is shown in Figure 4-27.

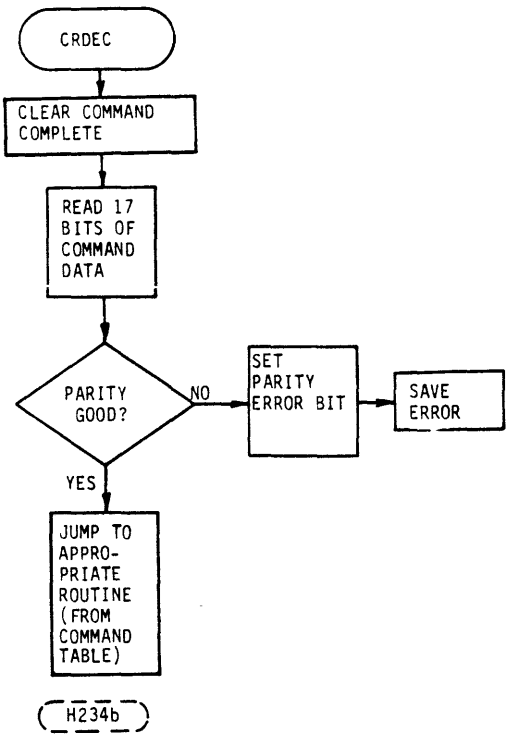


FIGURE 4-25. "CRDEC" MODULE

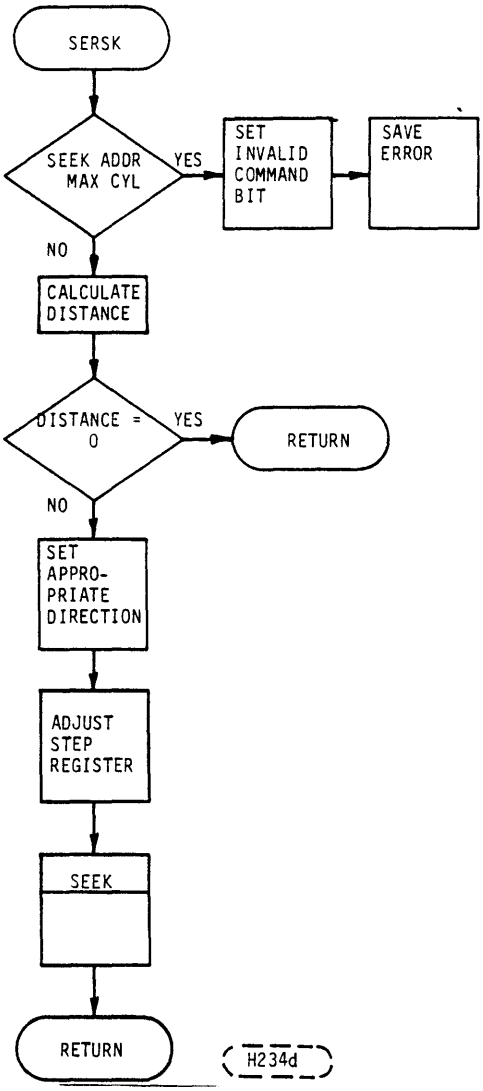


FIGURE 4-26. "SERSK" MODULE

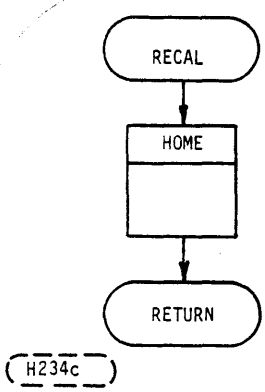


FIGURE 4-27. "RECAL" MODULE

4.3.3 HEAD POSITIONING SYSTEM

4.3.3.1 GENERAL

The data heads are positioned on the disk by a closed loop servo system (Figure 4-28). Mounted on the same actuator as the data head is a servo head which reads the specially formatted information on the servo surface (lower surface of the bottom disk). This information is decoded and amplified for the error signal needed to keep the actuator on track. The microcomputer provides a command signal to move from track to track.

The servo system contains a position loop, a veloctiy loop and a current loop. Figure 4-28 is a simplified block diagram of the servo system. The current loop is analog while the velocity and position loops are a combination of digital and analog circuitry. The compensation loops are not shown for simplicity. The positioning servo system utilizes velocity information that is obtained by differentiation of position signals.

The positioning operation begins when the system controller sends a step and direction command. The microcomputer then initiates and controls the seek. There are times when the microcomputer initiates a seek without a system controller command. Initial head-load and recovery from faults are two of these times.

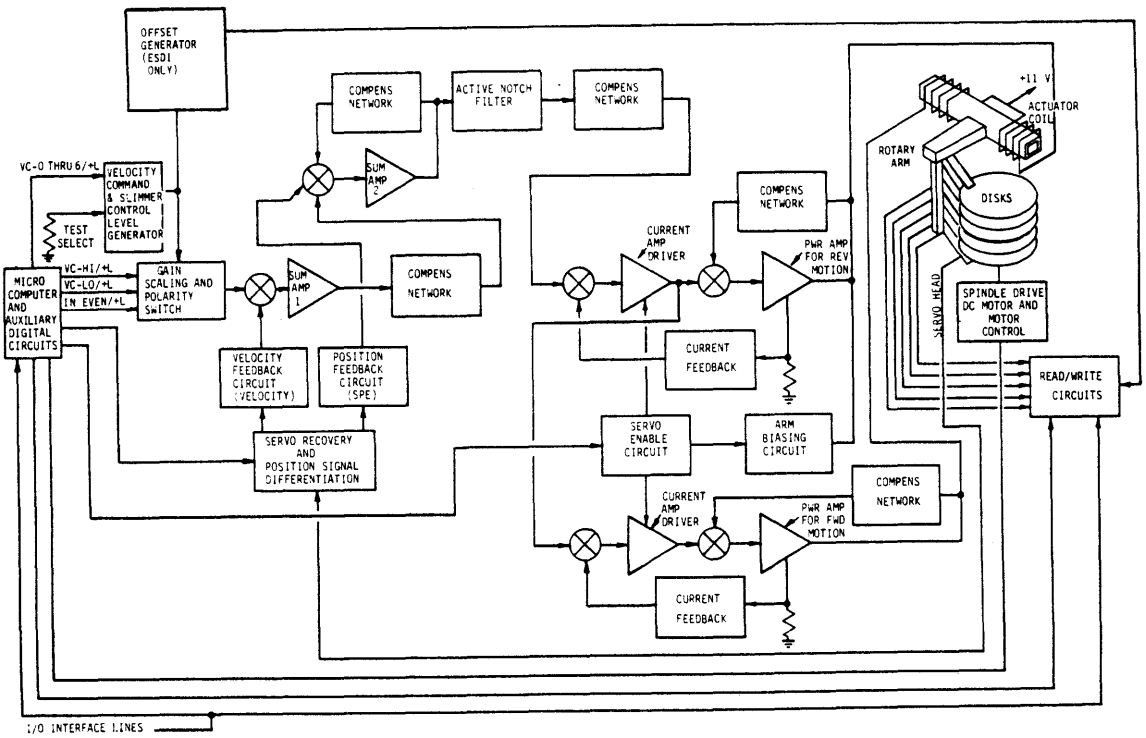


FIGURE 4-28. SERVO GENERAL BLOCK DIAGRAM

The microcomputer counts the number of tracks to be traversed and searches a velocity profile table for the correct velocity command code. The microcomputer outputs a digital number representing the initial velocity taken from the velocity profile table. A digital to analog converter generates an analog voltage which is amplified and applied to the actuator voice coil. The microcomputer also switches the servo circuit into the velocity mode. This begins the move to the destination track and causes information on the servo surface to be decoded into a velocity feedback signal. Each time the center of a track is crossed, the servo circuitry detects it and informs the microcomputer. The target track distance is then recalculated. As the heads approach the target track the microcomputer reduces the velocity. When the heads are within less than one-half track of their destination the microcomputer switches the servo to the fine mode.

In the fine mode the information on the servo surface is decoded into positional feedback. The microcomputer also decides if the target track is odd or even and sets a line to tell the servo circuit which track to center on.

4.3.3.2 SERVO SURFACE FORMAT

The Servo surface is divided into four zones as shown in Figure 4-29. The data zone defines the read/write area on the other surfaces (Track 00 to 924). The guard bands have coded information to tell the drive when the heads are outside the data zone. The WREN uses a landing zone because the heads are over media at all times. Flying and landing the heads in this zone prevents damage to customer data when cycling power. The landing zone also has data to enable the servo timing circuits to synchronize during start-up.

The servo format used in the WREN is composed of a five-dibit pattern. There are 2688 servo fields per track. The individual dibits within the servo field are called:

- Sync
- Code
- Even
- Odd
- Quadrature

The sync bits are used to lock the PLO which then provides the basic timing to decode the rest of the dibits. The code bit is used to mark the index, Track 00, and to differentiate the data zone from the guard band. The even, odd and quadrature bits are used to drive the position and velocity feedback signals.

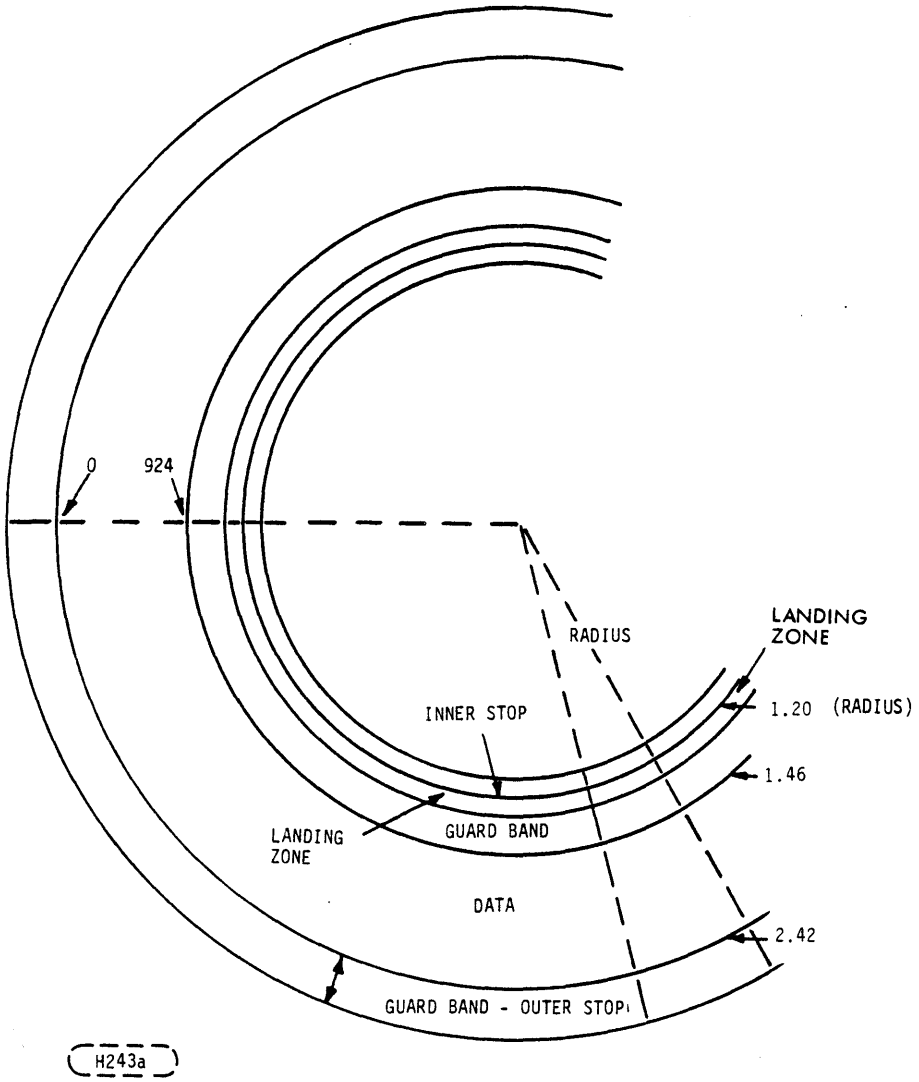


FIGURE 4-29. WREN II SERVO TRACK LOCATIONS

Servo tracks come in two varieties, even and odd. All tracks have sync bits. The code bit is present in the Track 00, but only in every other field. The code bit is also present for four fields at the beginning of each data track to mark the index and is also present in the guard band. Only even tracks have even bits and only odd tracks have odd bits. The quadrature bit is written half on the outside of the even track and half on the inside of the odd track as shown in Figure 4-30.

Data tracks on the other surfaces are offset one-half track from servo tracks, this means that when the servo head is halfway between and odd and even track the data head is on track center. Dibit pattern B in Figure 4-30 shows what the servo information will look like when the data head is on track center. NOTE: That the odd and even bits are of equal amplitude and the quadrature bit is a maximum amplitude. The servo circuits find the center of data tracks by subtracting the peak values of the odd dibits from the peak values of even dibits (see Figure 4-31). When this value is zero the data heads are centered. If the peak values of the quadrature dibit are also zero the track is odd. On the other hand if the quadrature dibits are at their maximum value the track is even.

When the servo is in the velocity mode the absolute value of the slope of the position signal is used as the velocity feedback. However, this slope has a discontinuity between tracks due to a change in sign. Therefore, when the position signal is over a set threshold the absolute value of the quadrature slope is used as the velocity feedback.

4.3.3.3 DETAILED POSITIONING SYSTEM DESCRIPTION (CDC506)

A block diagram of the WREN Servo System is shown in Figure 4-28. Two signals derived by the Servo Analog Data Recovery circuits are position and velocity signals. A block diagram of the analog circuits used to provide these signals is shown in Figure 4-32. These signals are used by the closed loop servo system to control the seeking and positioning of the heads. The analog circuits are controlled by the digital LSI circuit. which provides the proper gating signals, and by the microcomputer.

A detailed description of the functions of the circuits shown in Figure 4-32 is as follows:

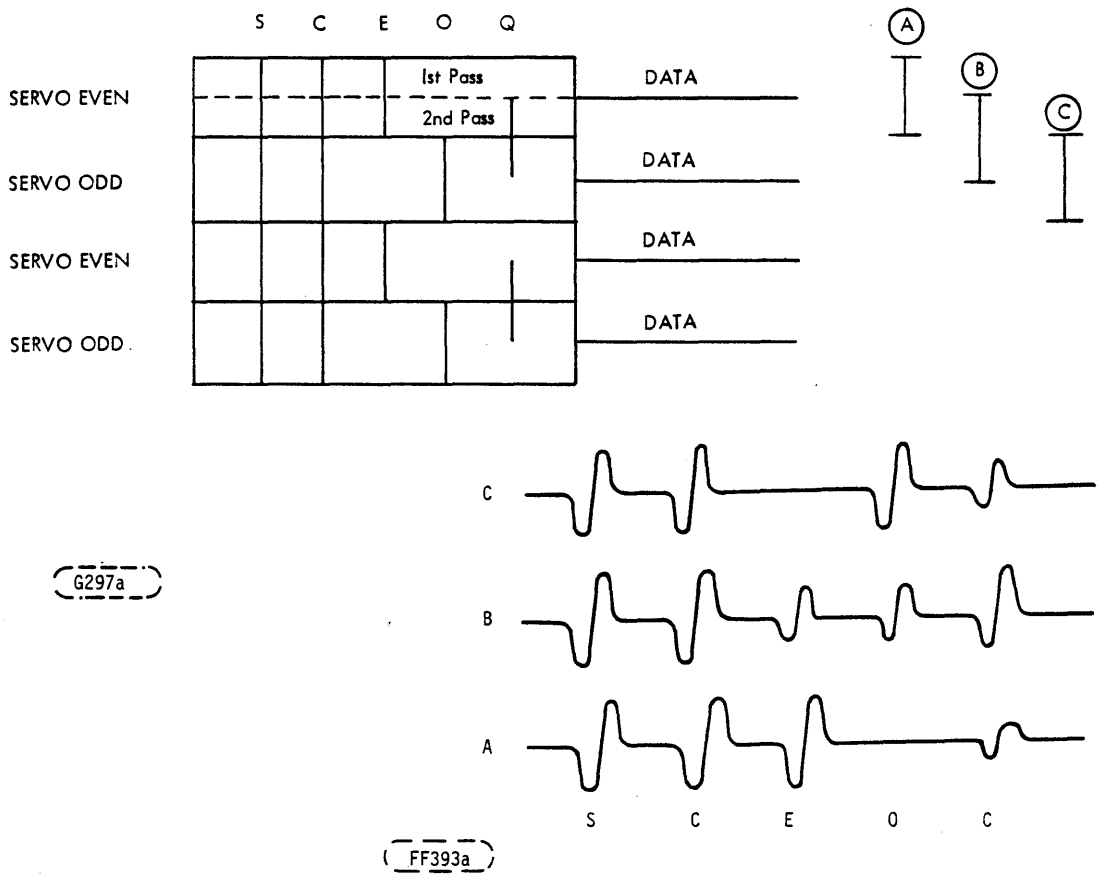


FIGURE 4-30. DIBIT PATTERNS

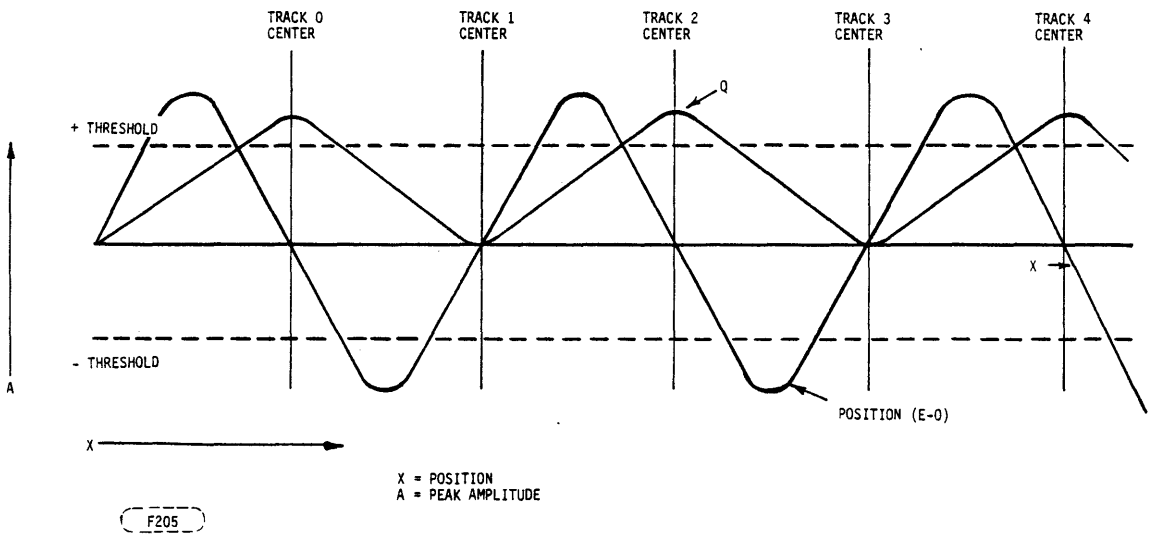


FIGURE 4-31. DERIVED POSITION AND QUADRATURE SIGNALS

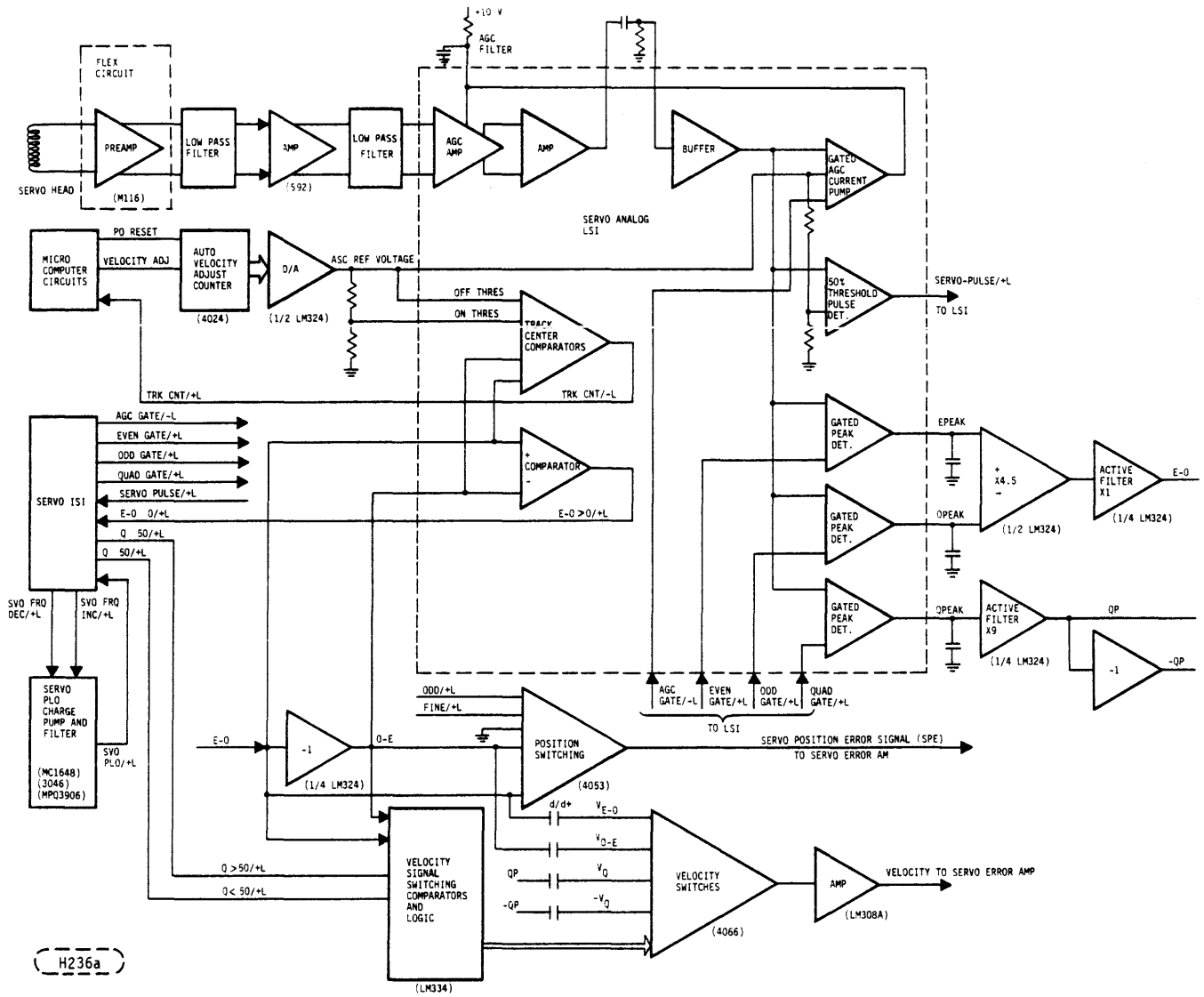


FIGURE 4-32. WREN II SERVO ANALOG DATA RECOVERY CIRCUITS

The signal from the servo disk is amplified by a low noise preamp (M116). This preamp is located on the flex circuit inside the sealed area. The output is sent to the Data PWA where it is filtered, amplified (592) and again filtered and applied to the Servo Analog LSI chip. The Analog LSI chip contains an automatic gain control (AGC) amp which is the controlling element in an AGC loop contained within the chip. Also in the chip is a high speed comparator with a threshold set at 50% of the peak dibit level which outputs a pulse when any dibits amplitude exceed 50% of the peak AGC level. The input signal from the 592 amp is applied to the AGC amp in the analog LSI. It is then amplified again and coupled to a buffer amp. The buffer amp drives a gated AGC current pump detector. The detector is gated such that only the sync dibit is used for AGC. The combined action of the AGC system is to produce a constant amplitude sync dibit at the output of the buffer amp. The AGC reference voltage controls the peak amplitude of the output of the buffer. This voltage is supplied externally to the LSI chip by a D/A converter circuit. The reference voltage is set up during a calibration cycle when power is applied to the drive.

The internal buffer output is also applied to three gated peak detectors which peak detect the three position dibits, even, odd and quad. The even and odd peak detectors are applied to difference amps with a gain of 4.5. The output of the difference amp is filtered by a two-pole active filter. This signal is E-O (even-odd) and is inverted to produce O-E (odd-even). These signals are shown in Figure 4-33. During seeks no position feedback is used and the position switching circuit grounds the SPE signal (servo position error). During track following mode (FINE) the position switching circuit selects either the E-O or O-E signal depending upon what polarity track (even or odd) is to be followed.

The velocity signal is developed from the position signal by taking the derivative of the E-O and O-E signals. These two velocity signals, (i.e., Ve-o and Vo-e) are applied to the velocity switches. These signals are of opposite polarity and the proper one is selected depending upon the position of the head over an even or odd track. The position of the head is determined by the servo digital LSI which detects the presence or absence of a Q dibit pulse. This signal is outputted by the LSI as Q <50 and Q >50. These two signals control what velocity feedback signal is used. As the head moves between tracks, the E-O and O-E signals become non-linear and their velocity signals are not accurate. To overcome this a quadrature dibit is written on the servo surface which is offset by 1/2 track from the even and odd dibits. This dibit is peak detected by the Q peak detector and amplified and filtered to generate the Qp signal.

This is inverted and becomes -Qp. Qp and -Qp are also differentiated to produce two other velocity signals V_Q and $-V_Q$. One of these signals is selected by comparing the amplitudes of the E-O and O-E signals. If either of these go too positive and enter their non-linear region the velocity feedback signal is switched to the V_Q or $-V_Q$ signal. The output from the velocity switches is buffered by an amplifier (LM308A) and this output is applied to the servo error amp as the velocity feedback.

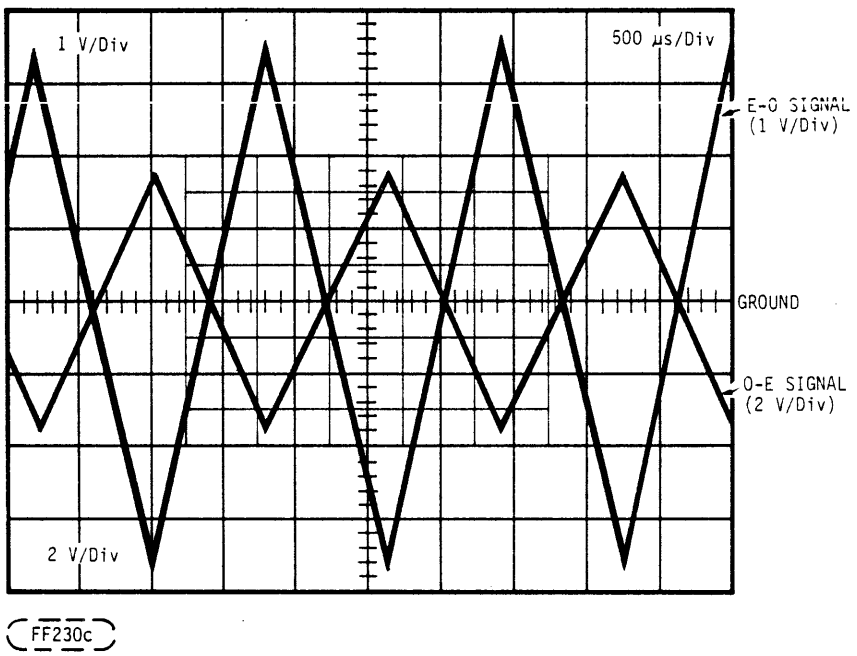


FIGURE 4-33. E-O AND O-E SIGNALS

The gain of the position and velocity feedback signals is controlled by the amplitude of dibits that are peak detected. The amplitude of the dibits is set by the AGC system which is referenced to an external voltage (AGC REF VOLTAGE). By changing the reference voltage the amount of feedback to the servo loop may be changed. This fact is used to adjust the velocity feedback signal to the exact amount required independent of component tolerances, etc. This is done upon power up sequence under control of the microcomputer circuits. The microcomputer does test seeks during which it measures the velocity of the arm. If the velocity is incorrect, it will increment the auto velocity adjust counter which changes the AGC REF VOLTAGE. Another test seek is performed and the process repeats until the correct velocity is achieved. This adjusts for errors associated with normal component tolerances.

Also located in the Servo Analog LSI are several comparator circuits. One of these is the Track Center Comparators which tells the microcomputer circuit that the head has reached the center of the track. This is used in the settle routine and also will indicate if the head has gone off track for some reason. Another comparator simply senses if the E-O signal is positive (E-O> O). This signal is used by the servo digital LSI in the track crossing generator circuit.

In addition to the position and velocity signals, the analog circuits of the servo system provides the following functional groups. (See Figure 4-32).

- Velocity and slimmer control level generator
- Actuator drive circuits:
  1. Gain scaling and polarity switch
  2. Summing amplifiers
  3. Power amplifier
- Servo system velocity feedback circuit
- Servo system position feedback circuit
- Active notch filter and compensation networks
- Servo enable and rotary arm biasing circuit

The velocity and slimmer control level generator is located on the Servo PWA. The microcomputer outputs a seven bit digital command by proper activation of the VC-0/+L through VC-6/+L lines to the digital to analog converter (DAC) U17. The DAC output is connected to current to voltage converter, U7-1. Scaling of the DAC output is accomplished at the factory by selecting the value of the test select resistor, R73. The two velocity ranges are chosen by the microcomputer by activating the VC-LO/+L or VC-HI/+L lines. The gain scaling of the amplifier U7-7 is provided thru analog switches U30-14 and U30-4. The IN-EVEN/+L line controls the direction of the seek by determining the inverting or noninverting configuration of the polarity switching amplifier, U7-7. When IN-EVEN/+L line is set "HIGH" the actuator drive circuits provide "REVERSE" motion of the rotary arm (from lower numbered tracks towards higher numbered tracks). When seek is complete and both lines VC-HI/+L, VC-LO/+L are set "LOW", R39 and R53 are disconnected from U7-7. This allows slimmer control levels to be set at U7-1 without affecting the servo system. Summing amplifier U7 in the seek mode subtracts the velocity feedback signal from the velocity command signal to generate the velocity error signal.

The velocity error signal drives the power amplifier through amplifier U3 and active notch filter U4-7. During the seek mode the line FINE/+L is "LOW" and position feedback signal is removed. When the rotary arm is positioned on track (FINE/+L is "HIGH"), the position signal will be active.

The power amplifier drives the head actuator coil. Q2 emitter resistor R24 on the motor control of PWA feeds back a voltage proportional to the current in the actuator coil for "FORWARD" motion. The feedback voltage is summed with the actuator drive signal at pin 9 of U4 on the Servo PWA.

The compensation networks on the motor control PWA (R7, C2 and R6, C1) control the gain and band width of the output stages of the Power Amp in order to insure high frequency stability. The compensation networks on the servo PWA (R7, R8, C6) control the bandwidth of the current loop. The U3 compensation feedback network (R33, R42, C12) together with the active 2.6 kHz notch filter provides high frequency compensation in the velocity loops and attenuates frequencies that may cause mechanical resonances.

The U3 compensation feedback network (R33, R41, C4) provides low frequency compensation for the position loop.

The network (R26, R5, C3) provides low frequency compensation in the velocity loop. The noise in velocity feedback is attenuated by compensation networks (R4, R2, C1 and R38, R23, R21, C11).

Servo disable and actuator retract are controlled by DISABLE/+L line and provided by CR3, CR4, Q2, U5 (12, 13, 14), and U6-13. The actuator retract procedure energizes the reverse winding with a controlled current to pull the arm into the landing zone. The DISABLE/+L line can be activated by both the microcomputer (SERVO EN/-L_ and the voltage fault monitor. Voltage fault monitor sets the DISABLE/+L line "HIGH" anytime either of the external power supplies (+12 V or +5 V) or internally generated -5 V is lost. In this case RESET/-L line is set "LOW". That resets the microcomputer. Anytime the DISABLE/+L line is active, WRT INHIBIT/-L is set "LOW" and disables the write function.

4.3.3.4 DETAILED POSITIONING SYSTEM DESCRIPTION (ESDI)

A block diagram of the WREN Servo System is shown in Figure 4-28. Two signals derived by the Servo Analog Data Recovery circuits are position and velocity signals. A block diagram of the analog circuits used to provide these signals is shown in Figure 4-32. These signals are used by the closed loop servo system to control the seeking and positioning of the heads. The analog circuits are controlled by the digital LSI circuit. which provides the proper gating signals, and by the microcomputer.

A detailed description of the functions of the circuits shown in Figure 4-32 is as follows:

The signal from the servo disk is amplified by a low noise preamp (M116). This preamp is located on the flex circuit inside the sealed area. The output is sent to the Data PWA where it is filtered amplified (592) and again filtered and applied to the Servo Analog LSI chip. The Analog LSI chip contains an automatic gain control (AGC) amp which is the controlling element in an AGC loop contained within the chip. Also in the chip is a high speed comparator with a threshold set at 50% of the peak dibit level which outputs a pulse when any dibits amplitude exceed 50% of the peak AGC level. The input signal from the 592 amp is applied to the AGC amp in the analog LSI. It is then amplified again and coupled to a buffer amp. The buffer amp drives a gated AGC current pump detector. The detector is gated such that only the sync dibit is used for AGC. The combined action of the AGC system is to produce a constant amplitude sync dibit at the output of the buffer amp. The AGC reference voltage controls the peak amplitude of the output of the buffer. This voltage is supplied externally to the LSI chip by a D/A converter circuit. The reference voltage is set up during a calibration cycle when power is applied to the drive.

The internal buffer output is also applied to three gated peak detectors which peak detect the three position dibits, even, odd and quad. The even and odd peak detectors are applied to difference amps with a gain of 4.5. The output of the difference amp is filtered by a two-pole active filter. This signal is E-O (even-odd) and is inverted to produce O-E (odd-even). These signals are shown in Figure 4-33. During seeks no position feedback is used and the position switching circuit grounds the SPE signal (servo position error). During track following mode (FINE) the position switching circuit selects either the E-O or O-E signal depending upon which polarity track (even or odd) is to be followed.

The velocity signal is developed from the position signal by taking the derivative of the E-O and O-E signals. These two velocity signals, (i.e., Ve-o and Vo-e) are applied to the velocity switches. These signals are of opposite polarity and the proper one is selected depending upon the position of the head over an even or odd track. The position of the head is determined by the servo digital LSI which detects the presence or absence of a Q dibit pulse. This signal is outputted by the LSI as Q <50 and Q >50. These two signals control what velocity feedback signal is used. As the head moves between tracks, the E-O and O-E signals become non-linear and their velocity signals are not accurate. To overcome this a quadrature dibit is written on the servo surface which is offset by 1/2 track from the even and odd dibits. This dibit is peak detected by the Q peak detector and amplified and filtered to generate the Qp signal.

This is inverted and becomes -Qp, Qp and -Qp are also differentiated to produce two other velocity signals V_Q and $-V_Q$. One of these signals is selected by comparing the amplitudes of the E-O and O-E signals. If either of these go too positive and enter their non-linear region the velocity feedback signal is switched to the V_Q or $-V_Q$ signal. The output from the velocity switches is buffered by an amplifier (LM308A) and this output is applied to the servo error amp as the velocity feedback.

The gain of the position and velocity feedback signals is controlled by the amplitude of dibits that are peak detected. the amplitude of the dibits is set by the AGC system which is referenced to an external voltage (AGC REF VOLTAGE). By changing the reference voltage, the amount of feedback to the servo loop may be changed. This fact is used to adjust the velocity feedback signal to the exact amount required independent of component tolerances, etc. This is done upon power up sequence under control of the microcomputer circuits. The microcomputer does test seeks during which it measures the velocity of the arm. If the velocity is incorrect it will increment the auto velocity adjust counter which changes the AGC REF VOLTAGE. Another test seek is performed and the process repeats until the correct velocity is achieved. This adjusts for errors associated with normal component tolerances.

Also located in the Servo Analog LSI are several comparator circuits. One of these is the Track Center Comparators which tells the microcomputer circuit that the head has reached the center of the track. This is used in the settle routine and also will indicate if the head has gone off track for some reason. Another comparator simply senses if the E-O signal is positive (E-O> O). This signal is used by the servo digital LSI in the track crossing generator circuit.

In addition to the position and velocity signals, the analog circuits of the servo system provides the following functional groups. (See Figure 4-32).

- Velocity and slimmer control level generator
- Actuator drive circuits:
  1. Gain scaling and polarity switch
  2. Summing amplifiers
  3. Power amplifier
- Servo system veloctiy feedback circuit
- Servo system position feedback circuit
- Active notch filter and compensation networks
- Servo enable and rotary arm biasing circuit

The velocity and slimmer control level generator is located on the Servo PWA. The microcomputer outputs a seven bit digital command by proper activation of the Data 0/+L through Data 7/+L lines to the digital to analog converter (DAC) U15. The DAC output is connected to current to voltage converter U16-1. Scaling of the DAC output is accomplished at the factory by selecting the value of the test select resistor, R61. The two velocity ranges are chosen by the microcomputer by activating the VC-LO/+L or Data 7/+L lines. The gain scaling of the amplifier U16-7 is provided thru analog switches U13-14 and U13-4. The IN-EVEN/+L line controls the direction of the seek by determining the inverting or noninverting configuration of the polarity switching amplifier U16-7. When IN-EVEN/+L line is set "HIGH" the actuator drive circuits provide "REVERSE" motion of the rotary arm (from lower numbered tracks towards higher numbered tracks). When seek is complete and both lines VC-HI/+L, VC-LO/+L are set "LOW", R40 and R42 are disconnected from U16-7. This allows slimmer control levels to be set at U16-1 without affecting the servo system. Summing amplifier U5 in the seek mode subtracts the velocity feedback signal from the velocity command signal to generate the velocity error signals.

The velocity error signal drives the power amplifier through amplifier U6 and active notch filter U10-14. During the seek mode the line FINE/+L is "LOW" and position feedback signal is removed. When the rotary arm is positioned on track (FINE/+L is "HIGH") the position signal will be active.

The power amplifier drives the head actuator coil. Q2 emitter resistor R24 on the motor control PWA feeds back a voltage proportional to the current in the actuator coil for "FORWARD" motion. The feedback voltage is summed with the actuator drive signal at pin 9 of U10 on the servo PWA. Q1 emitter resistor R23 feeds back a voltage proportional to the current in the actuator coil for "REVERSE" motion. The feedback voltage is summed with the actuator drive signal at pin 2 of U10 on the servo PWA.

The compensation networks on the motor control PWA (R7, C2 and R6, C1) control the gain and band width of the output stages of the Power Amp in order to insure high frequency stability. The compensation networks on the servo PWA (R28, R29, C9) control the bandwidth of the current loop. The U6 compensation feedback network (R48, R74, C17) together with the active 2.6 kHz notch filter provides high frequency compensation in the velocity loops and attenuates frequencies that may cause mechanical resonances.

The U3 compensation feedback network (R33, R11, C4) provides low frequency compensation for the position loop.

The network (R24, R47, C4) provides low frequency compensation in the velocity loop. The noise in velocity feedback is attenuated by compensation networks (R72, R70, C16 and R20, R21, R22, C1).

Servo disable and actuator retract are controlled by the DISABLE/+L line which is provided by CR8, CR9, Q3, U28 (6, 7, 8) and U38-1. The actuator retract procedure energizes the reverse winding with a controlled current to pull the arm into the landing zone. The DISABLE/+L line can be activated by both the microcomputer (SERVO EN/-L) and the voltage fault monitor. Voltage fault monitor sets the DISABLE/+L line "HIGH" anytime either of the external power supplies (+12 V or +5 V) or internally generated -5 V is lost. In this case RESET/-L line is set "LOW". That resets the microcomputer. Anytime the DISABLE/+L line is active, WRT INHIBIT/-L is set "LOW" and disables the write function.

4.3.4 READ/WRITE SYSTEM

4.3.4.1 GENERAL

To maximize the amount of data stored on the disk, the frequency of the flux reversals must be carefully controlled. Several recording methods are available and each has its advantages and disadvantages. The WREN uses the MFM recording method.

The time required to define one bit of information is called a cell. Each cell is nominally 200 ns in width. The data transfer rate is therefore, nominally 5.0 mega data bits/sec.

MFM defines a 1 by writing a flux transition at mid cell time. It defines a 0 by writing a flux transition at the end of cell time except when the cell is followed by a 1 in which case no flux transition is written in that cell.

The advantages and disadvantages of MFM recording are listed below:

- Fewer flux reversals are needed to represent a given binary number because there are no compulsory flux reversals at cell boundaries. Therefore, higher recording densities of data are achieved without increasing the number of flux reversals per inch. The number of flux reversals varies from a maximum of one reversal per bit (all "1's" or all "0's") to a minimum of one reversal for every two bits (alternating "1's" and "0's").

- Signal-to-noise ratio, amplitude resolution, read chain operation, and operation of the heads are improved by the lower recording frequency achieved because of fewer flux reversals required for a given binary number.

- Transition polarities have no relation to the value of a bit without defining the cell time along with cell polarity. This requires additional read/write logic which include a PLO and high quality recording media.

4.3.4.2 HEAD SELECT CIRCUIT (CDC506 INTERFACE)

The head select function is located on the data PWA and the flux circuit. The portion that is contained on the data PWA is shown in Figure 4-34B. There are four head select signals on the command cable interface, which is located on the servo PWA. Line receivers and buffers are also located on the Servo PWA. These signals are connected to the Data PWA by way of connector "J1" the signals are identified as "HD SEL 0/+L", "HD SEL 1/+L", "HD SEL 2/+L", and "HD SEL 3/+L".

Table 1 provides the correlation between the head select signals, head number selected and associated circuits:

TABLE 1

HEAD NO.	0	1	2	3	4	5	6	7	8
HD SEL 0/+L	L	H	L	H	L	H	L	H	L
HD SEL 1/+L	L	L	H	H	L	L	H	H	L
HD SEL 2/+L	L	L	L	L	H	H	H	H	L
HD SEL 3/+L	L	L	L	L	L	L	L	L	H
ACTIVE WRITE CURRENT GENERATOR	1	1	1	1	2	2	2	2	2
ACTIVE CHIP SELECT	1	1	1	1	2	2	2	2	2
PRE-AMP-1	X	X	X	X					
PRE-AMP-2					X	X	X	X	X

"HD SEL 0/+L" and "HD SEL 1/+L" signals go directly to the flex circuit, by way of connector "J2". The Pre-Amp integrated circuits do the decoding. "HD SEL 2/+L" signal goes to the "CHIP SELECT CONTROL" circuit only, however, the "HD SEL 3/+L" signal goes to both the flex circuit and the "CHIP SELECT CONTROL" circuit. The "CHIP SELECT CONTROL" circuit has three outputs:

"CHIP SEL 1/-L", "CHIP SEL 2/-L" and an or-tied output "UNSAFE/-L" which is also an output from the flex circuit.

"CHIP SEL 1/-L" goes active low only when heads #0 through #3 are selected. The low level goes to the flex circuit to "CHIP ENABLE PREAMP-" and also enables "WRITE CURRENT, GEN #1" for write operations. "CHIP SEL 2/-L" goes active low only when heads #4 through #11 are selected. The low level goes to the flex circuit to "CHIP ENABLE PREAMP-" and also enables "WRITE CURRENT, GEN #2" for write operations. If heads #9 through #11 are selected, which are invalid, PREAMP- detects that the heads are invalid and absent, when writing. It also pulls the "UNSAFE/-L" signal active low. If heads #12 through #15 are selected, the or-tied "UNSAFE/-L" output is pulled active low by the "CHIP SELECT CONTROL" circuit. This halts all writing functions and prevents false data from being written by valid heads.

4.3.4.3 READ CIRCUITS (CDC506 INTERFACE)

When the "WRT GATE/-L" signal is inactive high, the circuits are in the read mode. In this mode, the "WRT SELECT/-L" signal is inactive high which goes to the flex circuit and causes the preamp IC to amplify the read signal from the data head. Its differential output "RD DATA P" and "RD DATA N" goes to the data PWA. These signals pass through the "THREE POLE FILTER" to reduce preliminary front end noise. They then go into differential amplifier "AMP-A". The output of "AMP-A" goes through resistor "Zo" for proper source impedance and termination of "DELAY LINE-A". This delay line has a total delay time of 100 nanoseconds. At the output of "Zo", the read signal splits two ways. One split goes through "DELAY LINE-A" to one side of the input to "AMP-B" and the other split goes through the "SLIMMING CIRCUIT" to the opposite input of"AMP-B".

This circuit configuration provides a means for compensation of the read signal in order to minimize peak shift. This function is called "SLIMMING". For optimum performance, the amount of slimming increases as the resolution of the read head decreases. Because resolution is maximum at outer cylinders and minimum at inner cylinders, slimming must be adjusted to match. This function is performed by the "SLIMMER CONTROL" circuit. It measures the amplitude of the "SLIMMER LEVEL" signal and switches the "SLIMMING CIRCUIT" for one of three levels of slimming as follows:

1. Low slimming for outer cylinder
2. Medium slimming for intermediate cylinder
3. High slimming for inner cylinders

"AMP-B" provides two functions. It amplifies and differentiates the read signal. Its outputs go into the "ATTENUATOR" for the automatic gain control, where the read signal amplitude is adjusted to the proper level for input to the differential amplifier "AMP-C". This amplifier drives both the high resolution "5 POLE FILTER" and the low resolution "3 POLE FILTER" in parallel.

Here the read signal is split into two channels, high resolution channel and low resolution channel. The high resolution channel has a higher bandwidth and is used for accurate detection of the peak of the read signal. The low resolution channel has a lower bandwidth and provides a reliable qualification of the peak detection and eliminates false pulses due to noise in the high resolution channel.

The output from the high resolution "5 POLE FILTER" goes to the input of the differential amplifier "AMP-D" whose output goes to both the "BUFFER" for "DELAY LINE-B" and "AGC DETECTION AND CONTROL" circuit. The "AGC DETECTION AND CONTROL" circuit controls the "ATTENUATOR" in order to provide feedback for automatic gain control. The "WRITE SELECT/-L" signal controls two functions in the write circuits. In the write mode, it adjusts the "ATTENUATOR" to maximum attenuation in order to keep the read circuits from saturating due to the high amplitude write signals. Also, it causes the "AGC DETECTION AND CONTROL" circuit to clamp and hold its last value just before the write mode started. Therefore, when the write mode is over and the read mode resumes, the AGC value has been saved and resumes with very little change (ie quick write to read recovery).

In the low resolution channel, the output from the low resolution "3 POLE FILTER" goes to a "ZERO CROSS DETECTOR" and its output goes to the "QUALIFY AND PULSE CIRCUIT" for low resolution qualification of the read signal peak detection.

In the high resolution channel, "DELAY LINE B" output goes to a "ZERO CROSS DETECTOR" which outputs to the high resolution input of the "QUALIFY AND PULSE CIRCUIT". The high resolution signal has to be delayed 100 nanoseconds in order to provide setup time for the low resolution input to be able to qualify the high resolution read signal peak detection. The "QUALIFY AND PULSE CIRCUIT" generates an accurately timed read pulse output that goes to the input of the "ONE SHOT" which provides a pulse, of proper width, to the "DATA LINE DRIVER". The differential output of the "DATA LINE DRIVER" sends read pulse signals to the data cable interface on "+MFM READ DATA" and "-MFM READ DATA" lines.

4.3.4.4 WRITE CIRCUITS (CDC506 INTERFACE)

The characteristics of heads and media change with respect to the position on the media surface. Linear velocity and flying height are only two examples of these characteristics. Both examples increase as the radial position on the media increases. Likewise, there are electrical parameters that change but there are some controllable factors that can be implemented, in electrical circuits, which provide an optimum compromise for the desired performance. Such an example is the control of the magnitude of the write current used in the data head when writing data. The magnitude of the write current is adjusted as a function of cylinder number. the microcomputer uses the same digital to analog converter (D/A) that is used for the velocity command, during a seek operation. The D/A output is the "SLIMMER LEVEL" signal. This signal is set to zero for inner radius, where write current is minimum. For outer radius, where write current is maximum, the D/A is set to provide approximately 4.0 volts. The D/A provides equal increments every eight cylinders from inner to outer cylinders, thus providing a gradual increase in write current across the surface, from the inner radius (maximum cylinder) to the outer radius (cylinder zero).

Figure 4-34B is a block diagram of the data PWA Read/Write analog functions. In order to write data, "WRT GATE/-L" must be active low and "+MFM WRITE DATA" and "-MFM WRITE DATA" must provide the proper MFM encoded differential signals for writing data.

When the "WRT GATE/-L" signal, from the servo PWA, goes active low, the "WRITE CONTROL" circuit enables the "WRITE CURRENT DIRECTION" circuit, sets the "WRT SELECT/-L" active low to the flux circuit, and enables one of the write current generators, either "WRITE CURRENT GEN #1" or "WRITE CURRENT GEN #2". Also, the "WRT INHIBIT/-L" signal must be inactive high in order to enable the write flip flop "WRITE F/F" and the write current generators. If "WRT INHIBIT/-L" signal is active low, all write functions are over ridden and disabled by disabling "WRITE F/F", disabling both write current generators, and setting "WRT SELECT/-L" to an inactive high.

When the "SET WRT FLT/+L" signal is active high, it forces the "WRT INHIBIT/-L" signal to go active low. In the inactive low state, the "SET WRT FLT/+L" signal has no effect on the write circuits.

With "WRT GATE/-L" signal active low and "WRT INHIBIT/-L" signal inactive high, the selected data head is provided the proper write current direction per the write data inputs from the data cable signals "+MFM WRITE DATA" and "-MFM WRITE DATA". These differential signals are detected and buffered with the "DATA LINE RECEIVER". This signal pulses the "WRITE F/F" and toggles it with each pulse. The "WRITE F/F" complementary output controls the "WRITE CURRENT DIRECTION" circuit to provide proper differential signals on "RD DATA P" And "RD DATA N" to the flex circuit, which controls the direction of write current through the data head.

Under special conditions, the "FAULT/+L" signal will provide an active high which indicates that a write fault problem is present. The origin of such a problem is one or more of the following:

A. "UNSAFE/-L" signal active low
   1. Open data head
   2. Shorted data head
   3. Invalid data head selected
   4. Absence of write data signals

B. "CHIP SELECT CONTROL" circuit detects invalid data head selection.

The "FAULT/+L" signal goes to the servo PWA. It is normally inactive low but when it changes to an active high, a fault flip flop on the servo PWA is set which in turn sets the "SET WRT FLT/+L" signal to an active high and stops all write functions. The fault flip flop, on the servo PWA, is reset when the write enable cable signal goes inactive.

In the write mode, if the servo circuit detects a condition where the actuator is off track center, the fault flip flop, on the servo PWA, will be set. This halts all write functions and prevents data destruction on adjacent cylinders.

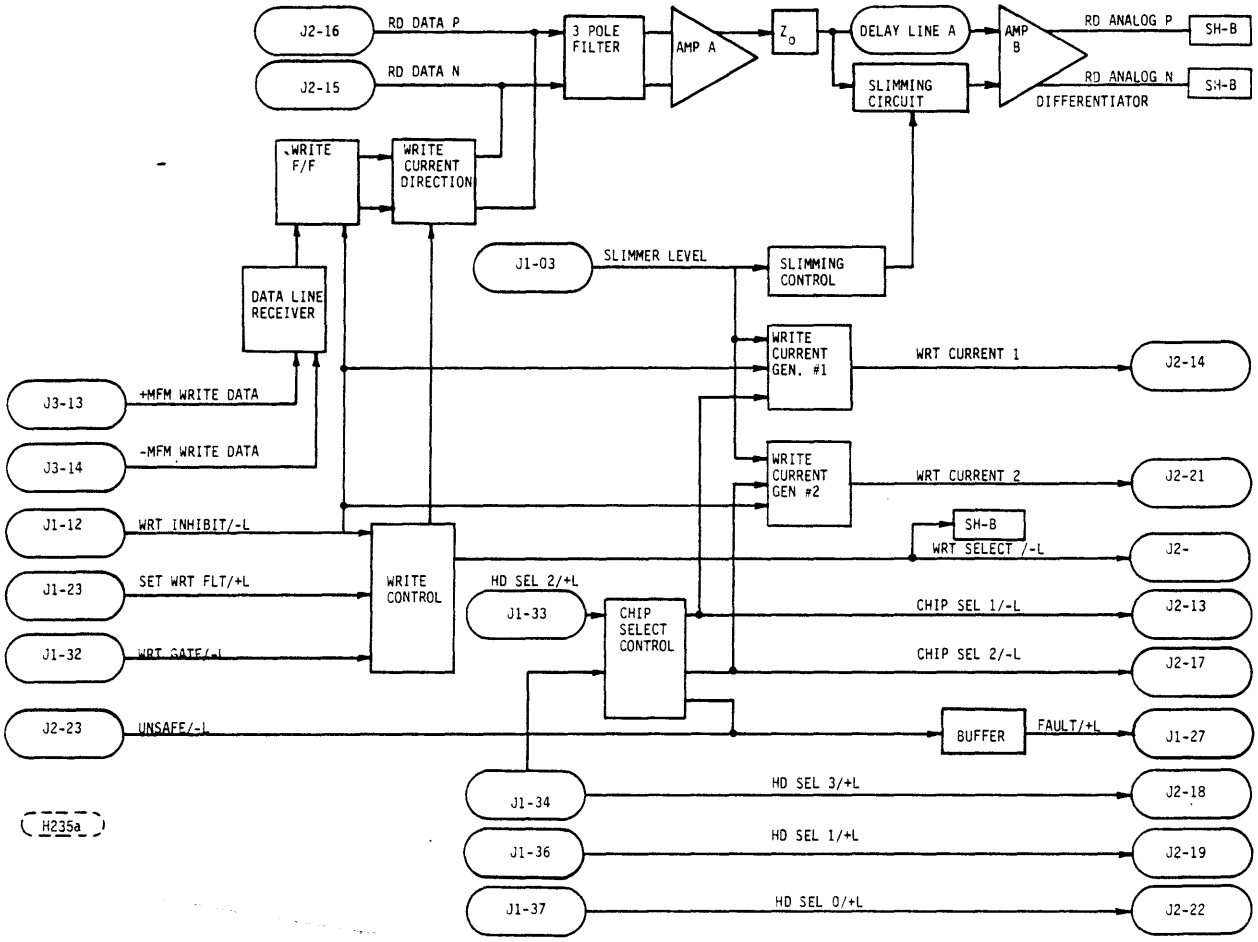


FIGURE 4-34A. HEAD SELECT, READ, AND WRITE BLOCK DIAGRAMS (CDC506 INTERFACE)

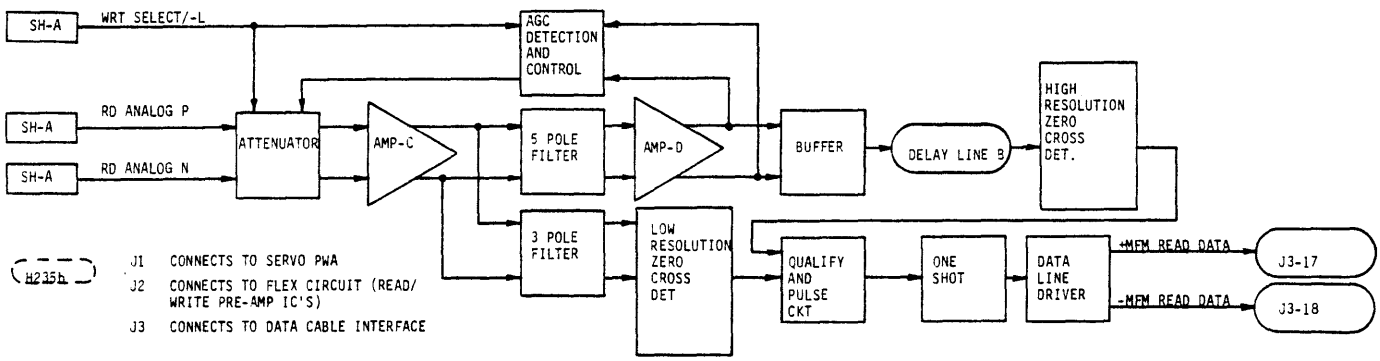


FIGURE 4-34B. HEAD SELECT, READ, AND WRITE BLOCK DIAGRAMS (CDC506 INTERFACE)

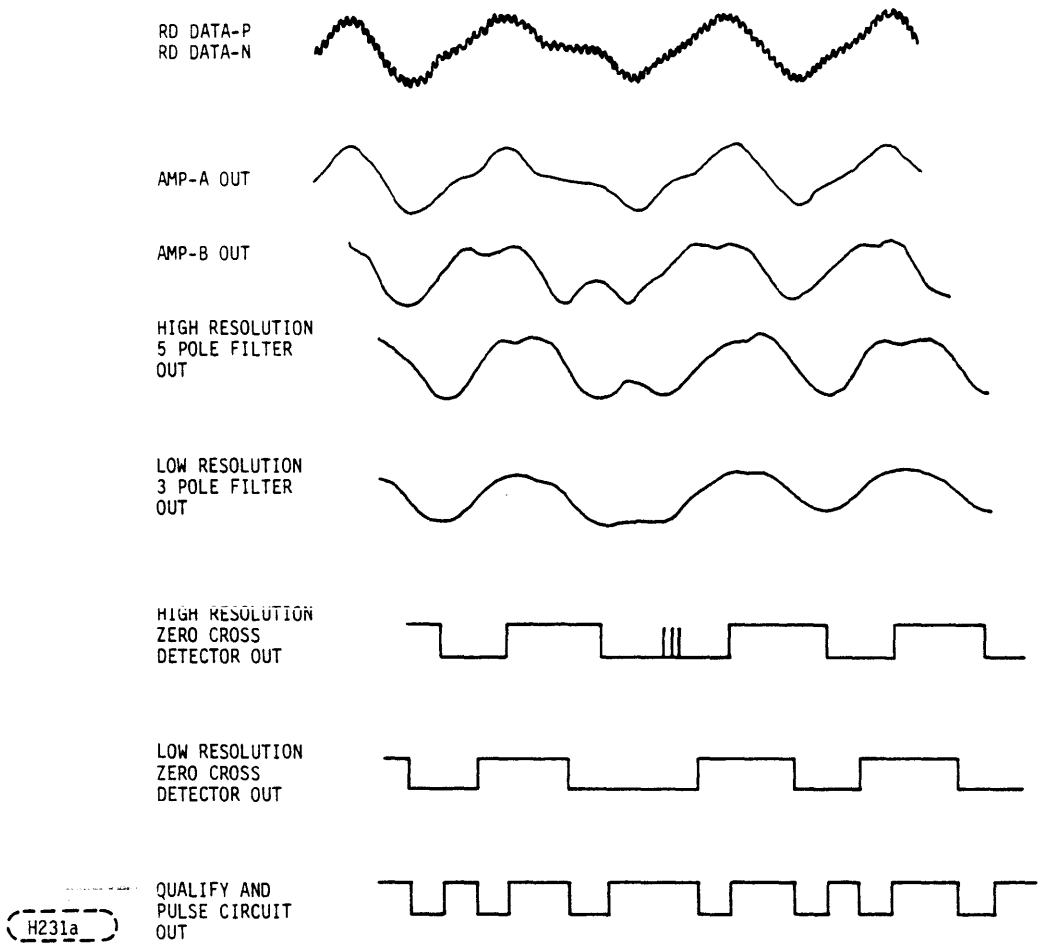


FIGURE 4-35. READ ANALOG TIMING DIAGRAM

4.3.4.5 HEAD SELECT CIRCUIT (ESDI)

The head select function is located on both the Servo and Data PWAs and on the flex circuit. There are four head select signals on the command cable interface, which is located on the Servo PWA. The signals are received by 74LS14 receivers and decoded to select the appropriate chip on the Read/Write Preamps on the flex lead. Table 2 lists correlation between head select signals, head number selected, and associated circuits.

TABLE 2

HEAD NO.	0	1	2	3	4	5	6	7	8
HD SEL 0/-L	H	L	H	L	H	L	H	L	H
HD SEL 1/-L	H	H	L	L	H	H	L	L	H
HD SEL 2/-L	H	H	H	H	L	L	L	L	H
HD SEL 3/-L	H	H	H	H	H	H	H	H	L
WRITE CURRENT GENERATOR	1	1	1	1	2	2	2	2	2
PRE-AMP-1	X	X	X	X					
PRE-AMP-2					X	X	X	X	X

Chip Sel 0/-L is active when heads 0-3 are selected. This select also turns on write current operator #1 and selects preamp #1. Chip Sel 1/-L is active for head 8 while Chip Sel 2/-L is active for heads 4-7. Chip Sel 1 and 2/-L are used to turn on write current generator #2 and select preamp #2.

If heads 9-11 are selected when writing, preamp #2 will detect that these are invalid heads and pull the "Unsafe/-L" signal low. If heads 12-15 are selected when writing, the chip select encoder will detect this and cause a write fault to be issued, which will stop all writing and prevent valid heads from writing false data.

4.3.4.6 READ CIRCUIT (ESDI)

When the "WRT GATE/-L" signal is inactive high, the circuits are in the read mode. In this mode, the "WRT SELECT/-L" signal is inactive high. This high level goes to the flex circuit and causes the preamp IC to amplify the read signal from the data head. The preamp IC differential output goes to the data PWA as signals "RD DATA P" and "RD DATA N". These signals are filtered by the "THREE POLE FILTER" to reduce preliminary front end noise. The filter output goes into differential amplifier "AMP-A". The output of "AMP-A" goes through resistor "Zo" for proper source impedance and termination of "DELAY LINE-A". This delay line has a total delay time of 100 nanoseconds. At the output of "Zo" the read signal is split. One split goes through "DELAY LINE-A" to one side of the input to "AMP-B" and the other split goes through the "SLIMMING CIRCUIT" to the opposite input of "AMP-B".

This circuit configuration provides a means for compensation of the read signal in order to minimize peak shift. This function is called "SLIMMING". For optimum performance, the amount of slimming increases as the resolution of the read head decreases. Since resolution is maximum at outer cylinders and minimum at inner cylinders, slimming must be adjusted to match. This function is performed by the "SLIMMER CONTROL" circuit. It measures the amplitude of the "SLIMMER LEVEL" signal and switches the "SLIMMING CIRCUIT" for one of three levels of slimming as follows:

1. Low slimming for outer cylinder
2. Medium slimming for intermediate cylinder
3. High slimming for inner cylinders

"AMP-B" performs two functions. It amplifies and differentiates the read signal. Its outputs go into the "ATTENUATOR" for the automatic gain control where the read signal amplitude is adjusted to the proper level for input to the differential amplifier, "AMP-C". The output of "AMP-C" drives both the high resolution "5 POLE FILTER" and the low resolution "3 POLE FILTER" in parallel.

At this point the read signal is split into two channels, high resolution channel and low resolution channel. The high resolution channel has the higher bandwidth and is used for accurate detection of the peak of the read signal. The low resolution channel has the lower bandwidth and provides a reliable qualification of the peak detection. It also eliminates false pulses due to noise in the high resolution channel.

The output from the high resolution "5 POLE FILTER" goes to the input of the differential amplifier "AMP-D" whose output goes to both the "BUFFER" For "DELAY LINE-B" and "AGC DETECTION AND CONTROL" circuit. The "AGC DETECTION AND CONTROL" circuit controls the "ATTENUATOR" in order to provide feedback for automatic gain control. The "WRITE SELECT/-L" signal controls two functions in the write circuits. In the write mode, it adjusts the "ATTENUATOR" to maximum attenuation in order to keep the read circuits from saturating due to the high amplitude write signals. It also causes the "AGC DETECTION AND CONTROL" circuit to clamp and hold its last value just before the write mode started. Therefore, when the write mode is over and the read mode resumes, the AGC value has been saved and resumes with very little change (ie., quick write to read recovery).

In the low resolution channel, the output from the low resolution "3 POLE FILTER" goes to a "ZERO CROSS DETECTOR" and its output goes to the "QUALIFY AND PULSE CIRCUIT" for low resolution qualification of the read signal peak detection.

In the high resolution channel, "DELAY LINE B" output goes to a "ZERO CROSS DETECTOR" which outputs to the high resolution input of the "QUALIFY AND PULSE CIRCUIT". The high resolution signal has to be delayed 100 nanoseconds in order to provide setup time for the low resolution input to be able to qualify the high resolution read signal peak detection. The "QUALIFY AND PULSE CIRCUIT" generates an accurately timed read pulse output that goes to the Data Recovery LSI. This Recovery LSI controls the Read PLO and retimes the Pulse Data (MFM) and sends it to the R/W LSI. The R/W LSI converts the MFM data to NRZ data. The NRZ data, together with a "Read Clock" is then sent to the data cable interface through a differential line driver.

4.3.4.7 WRITE CIRCUIT (ESDI)

The characteristics of heads and media change with respect to the position on the media surface. Linear velocity and flying height are two examples of these characteristics. Both examples increase as the radial position on the media increases. There are also electrical parameters that change but there are some controllable factors that can be implemented, in electrical circuits, which provide an optimum compromise for the desired performance. An example is the control of the magnitude of the write current used in the data head when writing data. The magnitude of the write current is adjusted as a function of cylinder number. The microcomputer uses the same digital to analog converter (D/A) that is used for the velocity command, during a seek operation. The D/A output is the "SLIMMER LEVEL" signal. This signal is set to zero for inner radius, where write current is minimum. for outer radius, where write current is maximum, the D/A is set to provide approximately 4 volts. The D/A provides equal increments every eight cylinders from inner to outer cylinders, thereby providing a gradual increase in write current across the surface from the inner radius (maximum cylinder) to the outer radius (cylinder zero).

Figures 4-36A and 4-36B are block diagrams of the ESDI Read/Write circuits. In order to write data, the write gate must be active and proper NRZ data with write clock must be present.

When the write gate goes active, the write control circuits enable one of the write current generators and sets one of the flex preamps into the write mode. The selected data head is provided the proper write current direction per the MFM write data output of the R/W LSI. The MFM write data pulses the write flip-flop and toggles it with each pulse. The write flip-flop's complementary output controls the write current direction circuit to provide proper differential signals to the flex R/W preamps.

Under certain conditions, the UNSAFE/-L signal will go active. This indicates the existance of some kind of problem. The fault may be caused by one or more of the following:

1. Open data head
2. Shorted data head
3. Invalid data head selected
4. No write data signals

The UNSAFE/+L signal is sent to the servo PWA where it is then sent to the interface. When the UNSAFE/+L signal is active, it causes the drive to stop writing. The WRITE INHIBIT/-L signal will also stop a write operation when active. This signal is active under the following conditions:

1. Voltage monitor fault
2. Offtrack servo error

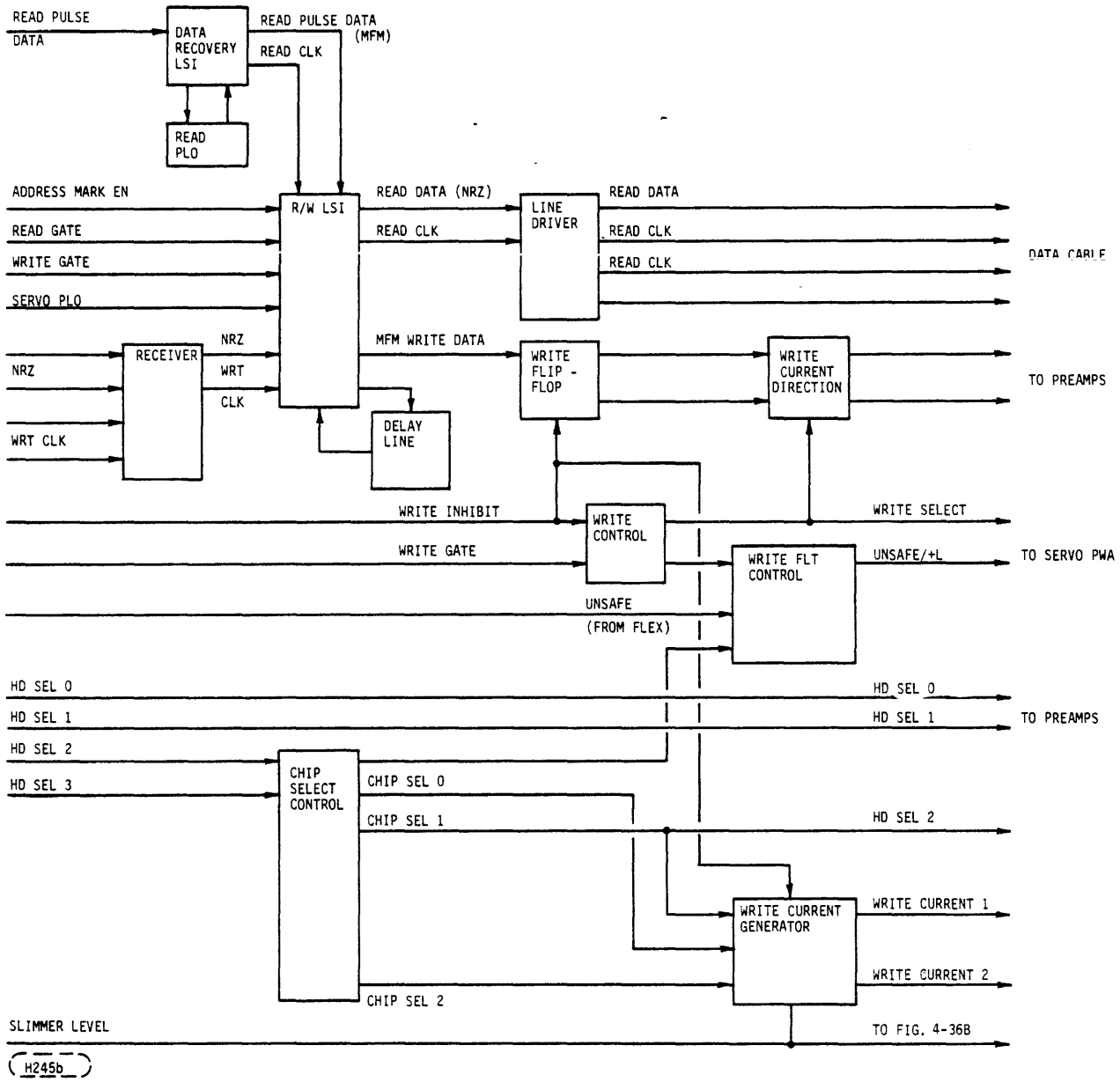


FIGURE 4-36A. READ/WRITE CIRCUIT BLOCK DIAGRAM

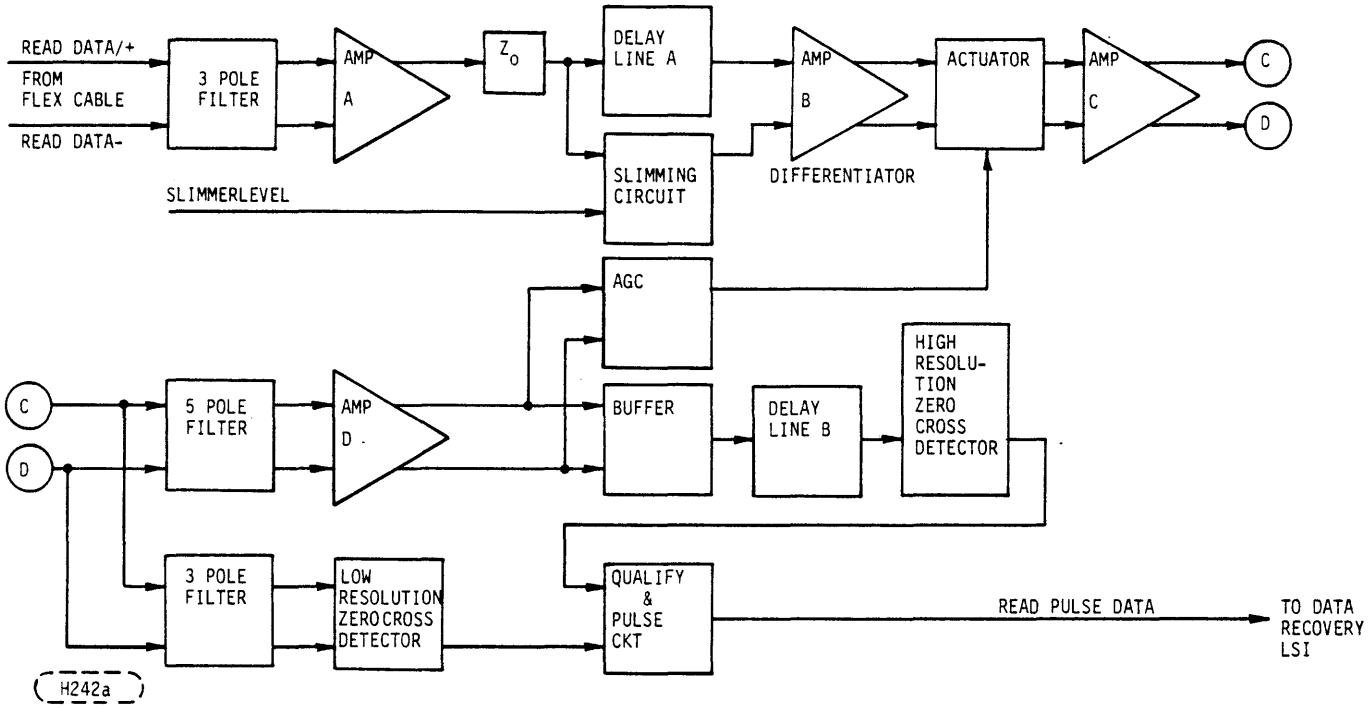


FIGURE 4-36B. READ/WRITE CIRCUIT BLOCK DIAGRAM

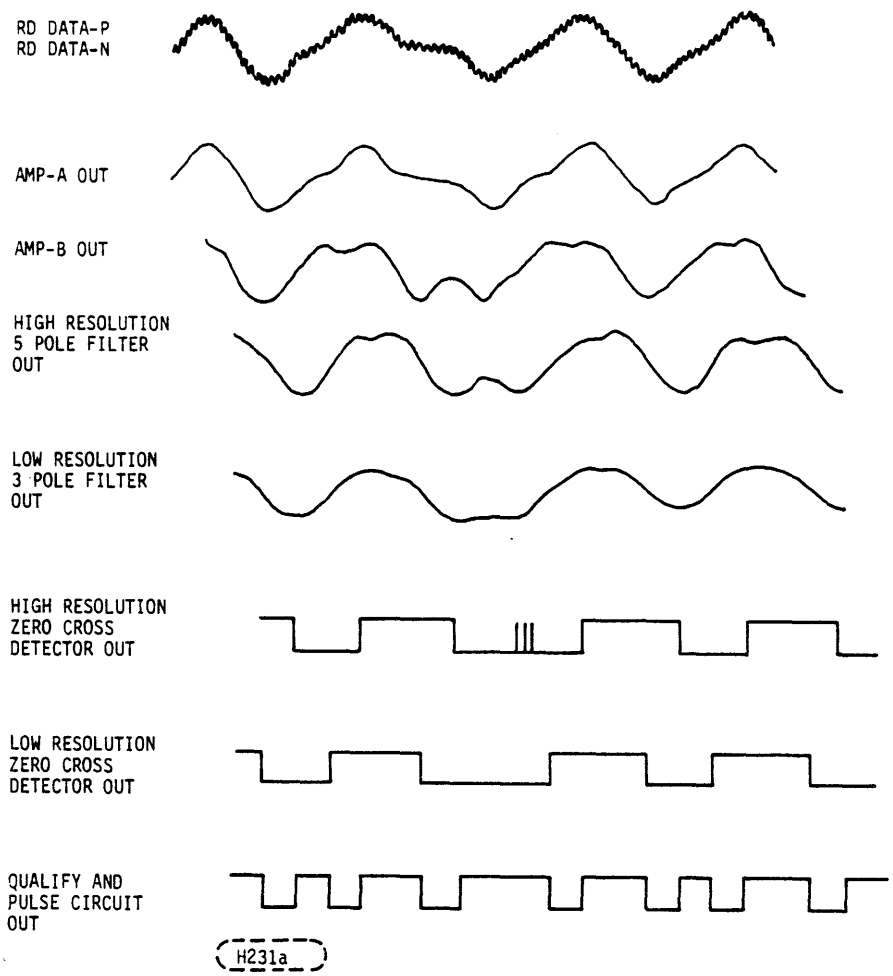


FIGURE 4-37. READ ANALOG TIMING DIAGRAM

4.3.5 DATA HEAD PREAMP CHIPS ON THE FLEX CABLE (ESDI AND CDC506 INTERFACES)

There are two Read/Write preamps on the flex cable. Each preamp is activated whenever its chip select line is switched to low TTL level. The preamps perform the following four functions:

1. The preamp selects the correct head.
2. The preamp diverts the write current to selected head.
3. The preamp generates an unsafe signal for the following conditions:
   a. Shorted heads
   b. Open heads
   c. Write current in the read mode
   d. No write data in the write mode
4. The preamp amplifies the read data from the selected head.

The head select encoding is shown in Figure 4-38. It should be noted that the preamps operates on +5 and -5 volts. When one or both of the preamps are in the read mode the data is presented on the READ-DATA-N and READ-DATA-P lines. The preamps are switched to the write modes if the WRITE SELECT lines are switched to low TTL levels. The proper value of write current must then be sinked from each write current (WC) line. If an unsafe condition is present the preamp(s) will switch the unsafe line from TTL high to TTL low. This will cause the digital circuitry to set the fault latch. The preamps will perform read and write operations on the head selected at the time; therefore, the head selection must be made before write is enabled.

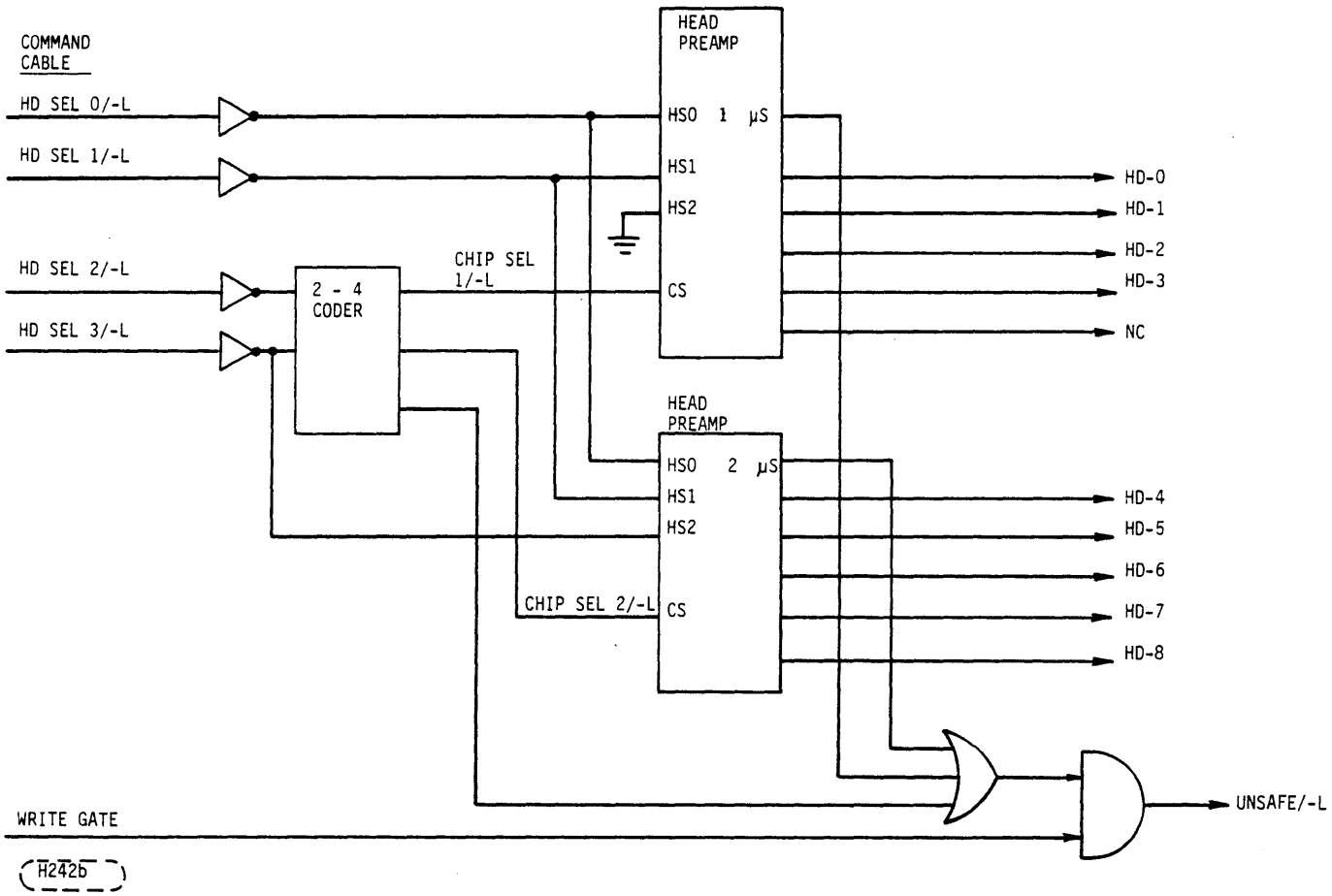


FIGURE 4-38. WREN II HEAD-SELECT LOGIC DIAGRAM

4.3.6 SERVO HEAD PREAMP ON THE FLEX CABLE (ESDI AND CDC506 INTERFACE)

A block diagram of the servo head preamp is shown in Figure 4-39. The preamp operates on +8.2 Volts and it amplifies the servo data from the servo head. The amplified signals are presented on the SERVO-N and SERVO-P lines. The servo head is connected to the preamp via two jumpers (J4's). These jumpers are removed during servo surface formatting.

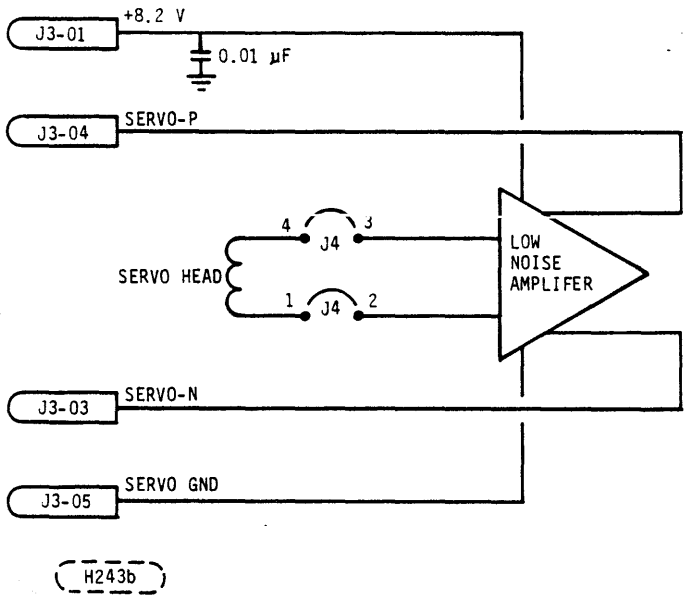


FIGURE 4-39. SERVO HEAD PREAMP (ON THE FLEX CABLE)

4.3.7 AUXILIARY SYSTEMS

4.3.7.1 WREN POWER SUPPLY CIRCUITS

The WREN requires only two external voltages, +12 volts and +5 volts but some circuits in the WREN require a negative voltage. This negative voltage is provided by a DC-DC converter circuit. In addition to this converter, voltage regulators provide +10 volts and +5 volts for critical read/write and servo circuits. Figure 4-40 is a block diagram of the power supply circuits internal to the WREN.

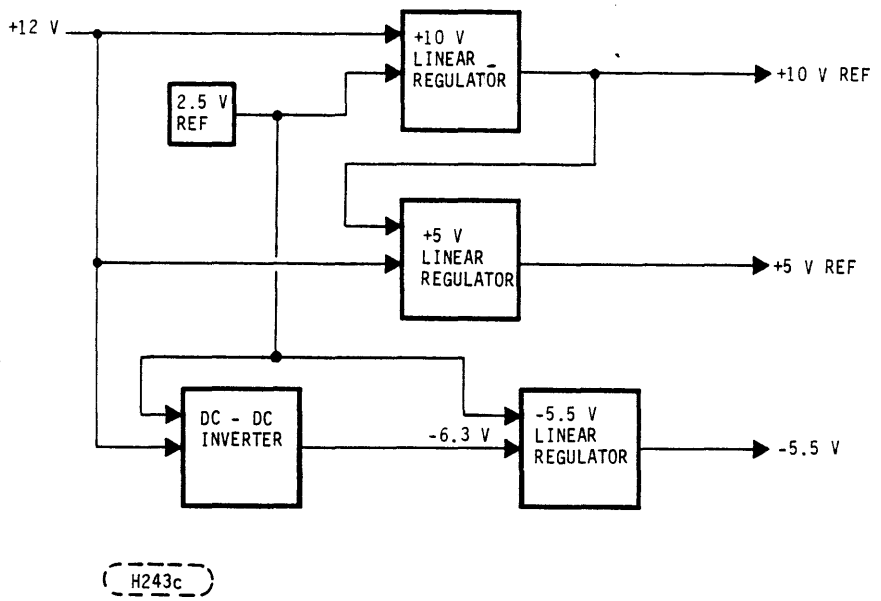


FIGURE 4-40. WREN II POWER SUPPLY CIRCUITS

Figure 4-41 shows the schematic of the DC-DC converter and linear regulator. Two comparators (LM393) control the operation of the switcher. If the output voltage at point C is too low then the bottom comparator will turn off and allow the switch transistor (3762) to apply +12 volts to point A of the 100 μH coil. This causes the current through the coil to increase linearly. This current is sensed by a 0.51 ohm resistor and when the current reaches ≈ 1 amp the upper comparator will turn on which turns off the switch transistor. The voltage at point A will then go negative until the latch diode (1N5818) turns on. This clamps the voltage across the inductor to ≈ 6.7 volts and the current in the inductor decreases linearly to zero. This current charges the 39 μF output capacitor which increases the output voltage. This increase in output voltage causes the lower comparator to switch on which will inhibit the switch transistor from turning on. The load current will discharge the 39 μf capacitor until the lower comparator switches states and starts the cycle over. Figure 4-42 gives typical waveforms for a load current of 200 mA. The output of C is well regulated but has high ripple (ie ≈ 200 mV). This voltage is then regulated by a linear regulator to remove ripple and decrease output impedance. The output of the linear regulator is -5.525 volts. This output is referenced to the +2.5 VR voltage and is sensed by an op-amp (LM324) which drives a NPN pass transistor (MPQ2222) via a PNP current source (MPQ3762). The use of a NPN pass transistor allows the regulator to function to very low voltage across the pass transistor (typically ≈ 0.3 volts).

+10 VOLT AND +5 VOLT REGULATORS

Figure 4-43 is a schematic of the +10 volt and +5 volt regulators. The +10 volt regulator is a conventional series pass design referenced to a 2.5 volt reference (MC 1403). The +10 volt regulator is similar to the -5.525 volt design except the transistors are of opposite polarity (ie. NPN vs PNP). Two pass transistors are used with current balancing resistors (4.7 ohm) to insure adequate power dissipation.

The +5 volts level from the divider is used as the reference for +5 VR regulator.

4.3.7.2 VOLTAGE MONITORING

The WREN II monitors the internal and external power supplies. This is done to assure data on the disk is not destroyed when power is shut off or interrupted. The circuits for doing this are on the SERVO-PWA. These circuits monitor the +5 and +12 volt external sources and the +10 and -5.5 volt supplies internal to the drive. These circuits also provide a delay of approximately 0.3 seconds after the +5 volt supply is turned on to allow the logic and microprocessor to be reset.

The outputs of the voltage monitoring circuits are used to directly inhibit any write current and to signal the microprocessor of voltage loss.

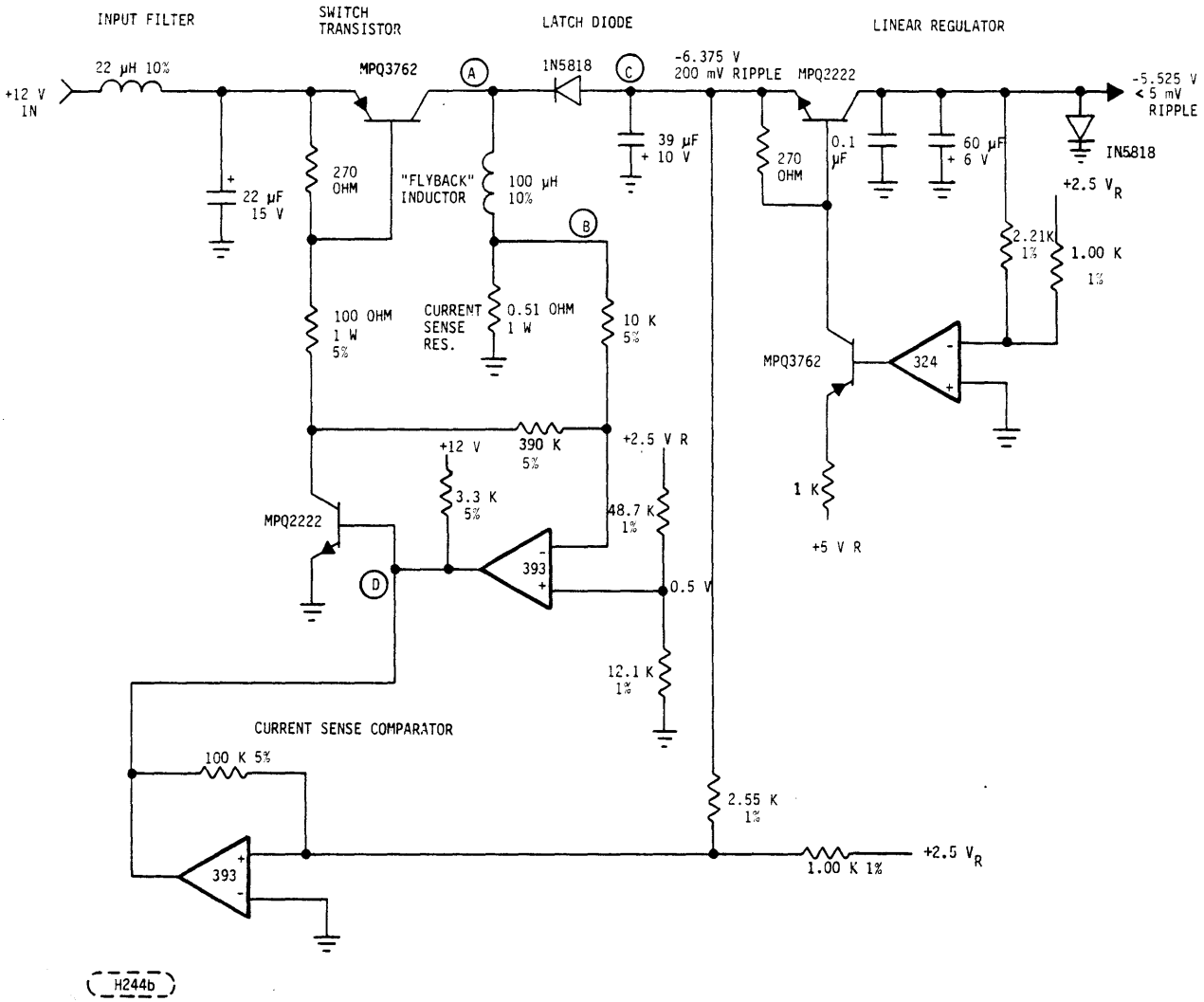


FIGURE 4-41. WREN II DC-DC CONVERTER

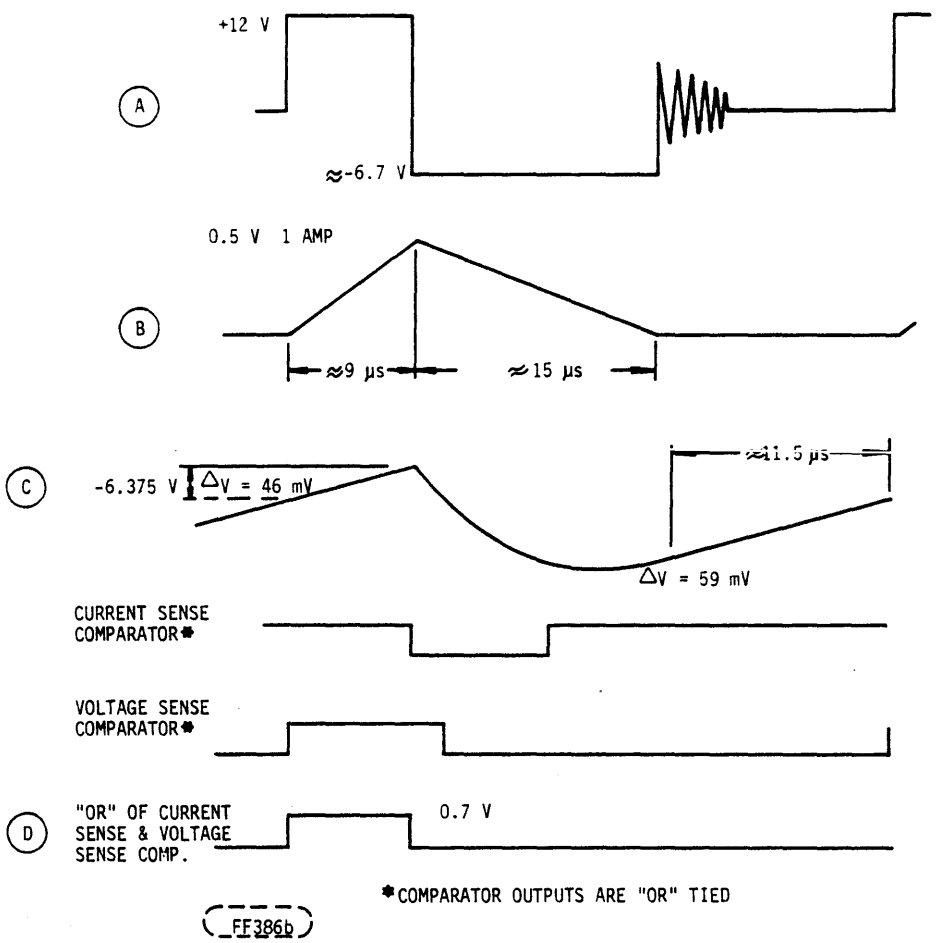


FIGURE 4-42. DC-DC CONVERTER WAVEFORMS

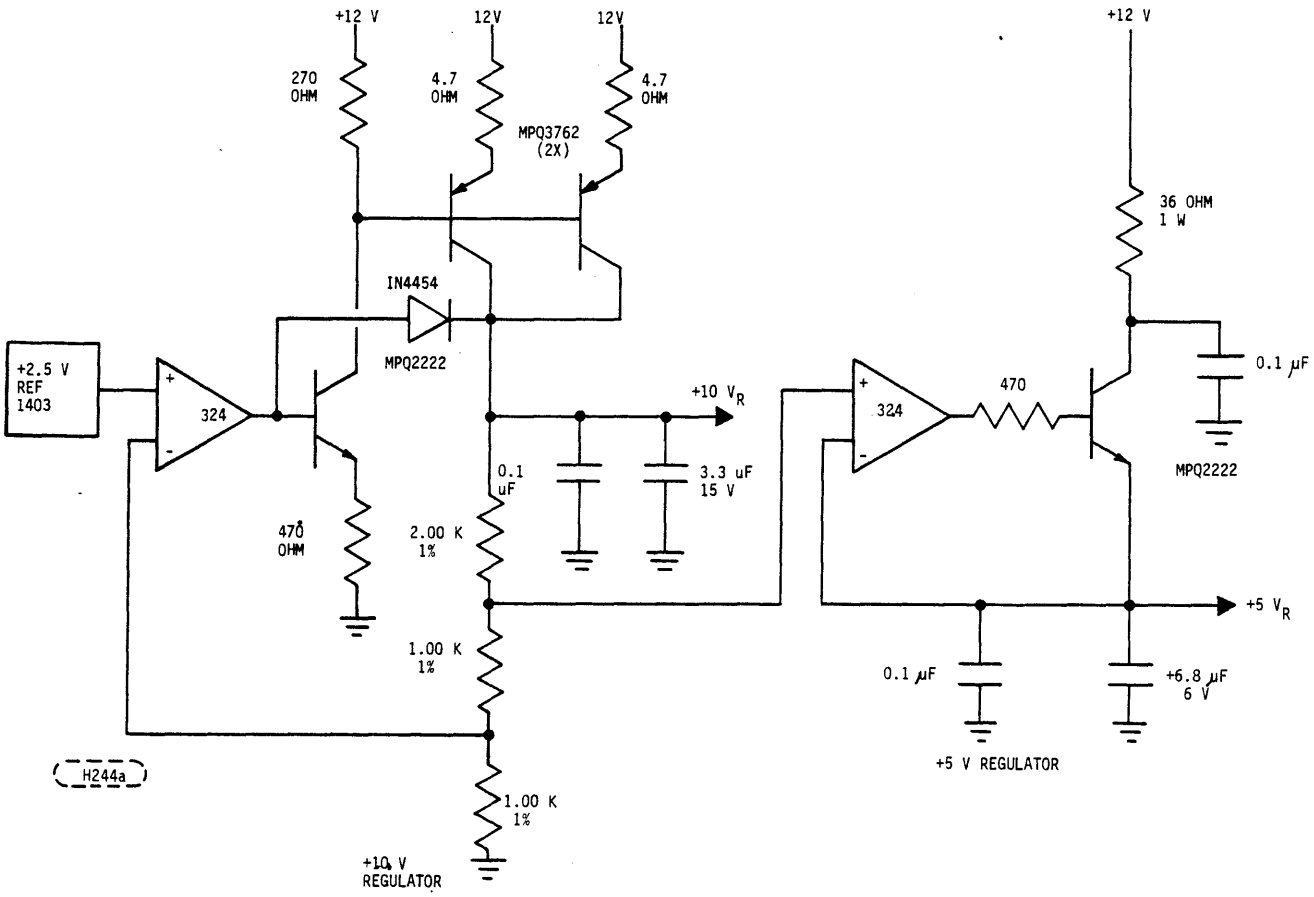


FIGURE 4-43. +10 VOLT AND +5 VOLT REGULATORS

4.3.7.3 VOLTAGE MONITORING (ESDI AND CDC506 INTERFACES)

The WREN II monitors the internal and external power supplies. This is done to assure data on the disk is not destroyed when power is shut off or interrupted. The circuits for doing this are on the SERVO-PWA. These circuits monitor the +5 and +12 volt external sources and the +10 and -5.5 volt supplies internal to the drive. These circuits also provide a delay of approximately 0.3 seconds after the +5 volt supply is turned on to allow the logic and microprocessor to be reset.

The outputs of the voltage monitoring circuits are used to directly inhibit any write current and to signal the microprocessor of voltage loss.

4.3.7.4 SPINDLE MOTOR CONTROL

A three phase brushless DC motorized spindle is driven by a current controlled power amplifier. Commutation is controlled by sensor devices inside the spindle motor. The motor current is set by the amplitude of a filtered pulse width modulated signal generated by the Servo LSI. (See Figure 4-44).

The motor control logic in the servo LSI chip uses the microprocessor clock as a reference to determine the motor speed error. the servo LSI generates a pulse width modulated output based on cumulative error to command motor current for the desired speed. The duty cycle of this signal is divided into 8 steps between 0% (minimum error) and 100% (maximum error). The 100% duty cycle is used while starting. Discrete circuits command a 3.25 Amp current for a 50 ms stiction breaking torque when power is applied. At power loss, the back EMF derived from the stored energy in the disk is used to hold the actuator solenoid in an unlocked position while the head actuator moves into the landing zone, after the heads are moved to the landing zone, the spindle speed will drop causing the back EMF to drop. When low back EMF is sensed, the dynamic braking relay will disconnect the motor from the power amps and short its windings. This rapidly decreases motor speed toward zero. This is done before the speed gets below 1600 Rev/min to reduce head/media wear while head flying heights are reduced at lower spindle speeds.

The motor connections are as below:

CONNECTOR PIN	LEAD COLOR*	LEAD CONNECTION (WIRE FUNCTION)
1	BROWN	SENSOR GROUND
2	RED	SENSOR SUPPLY (+12 V)
3	ORANGE	SENSOR C OUTPUT
4	YELLOW	SENSOR A OUTPUT
5	GREEN	SENSOR B OUTPUT
6	BLUE	PHASE C WINDING
7	PURPLE	PHASE A WINDING
8	GREY	PHASE B WINDING

* ALTERNATE LEAD COLORS: GREY WITH RED TRACER AT PIN 1 AND GREY AT ALL OTHER PINS.

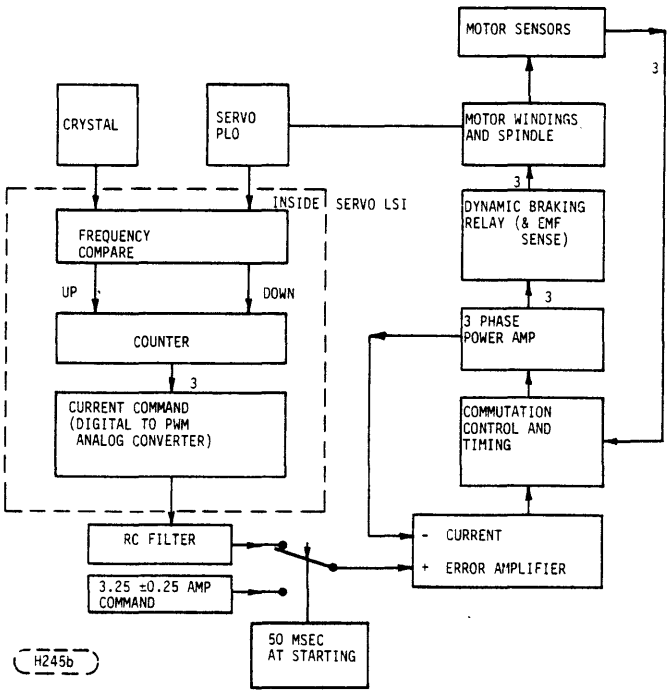


FIGURE 4-44. MOTORIZED SPINDLE DRIVE

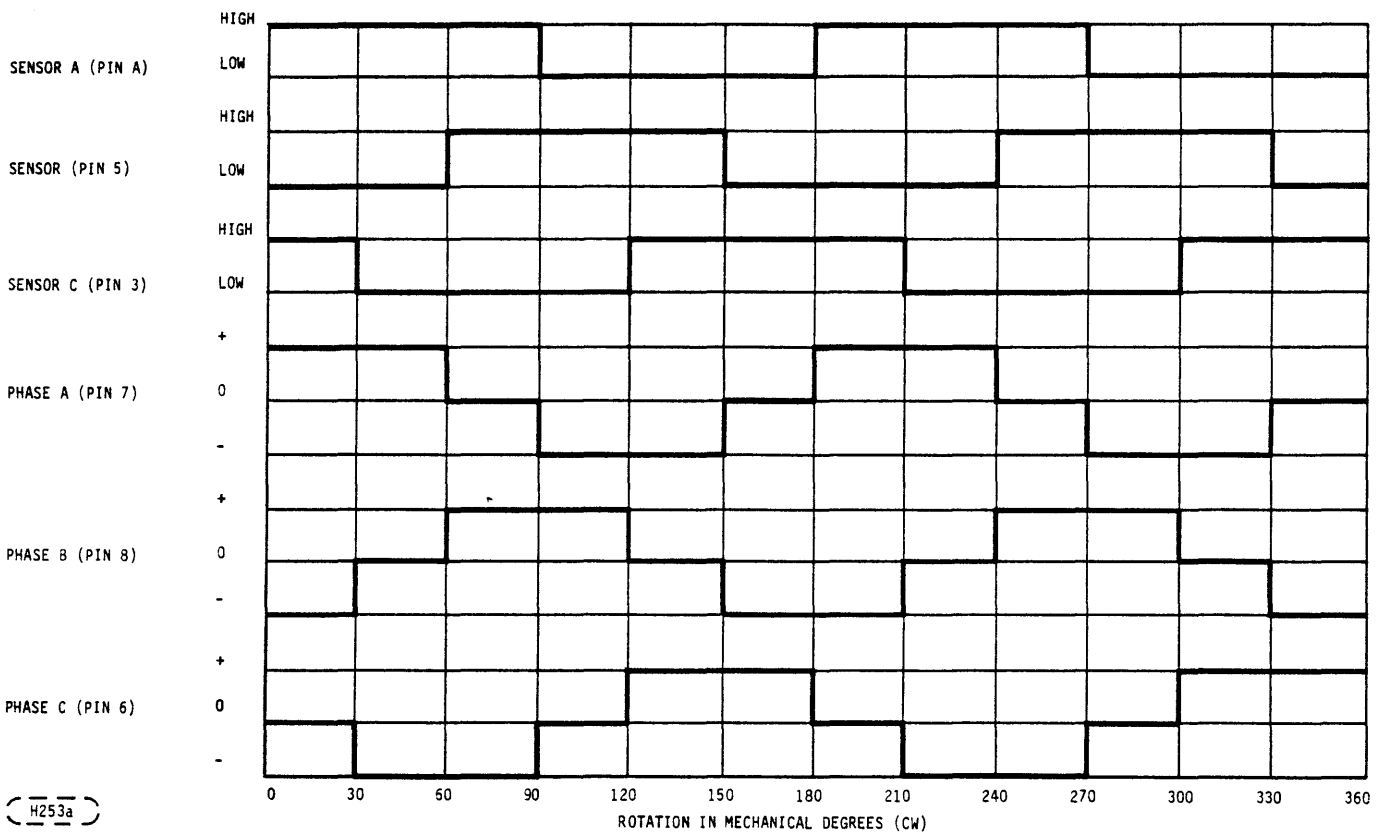


FIGURE 4-45. MOTOR TIMING DIAGRAM

5.1 INTRODUCTION

Most of the electronic functions of the WREN are included in three PWAs which are external to the sealed enclosure and one PWA (Flex Circuit) which is internal to the sealed enclosure. A block diagram of the function included in each board is as shown in Figure 5-1. Interface diagrams are shown in Figures 5-2A and 5-2B.

5.2 SCHEMATIC/PWA ORDERING

Schematic Diagrams and/or Printed Wire Assembly layouts can be ordered by contacting the CDC OEM Sales Office. Information needed will be the part number and the serial number from the label (Figure 5-3) located on the back of the unit. The Printed Wire Assembly number will also be needed. This number is stamped on the PWA (example shown in Figure 5-4).

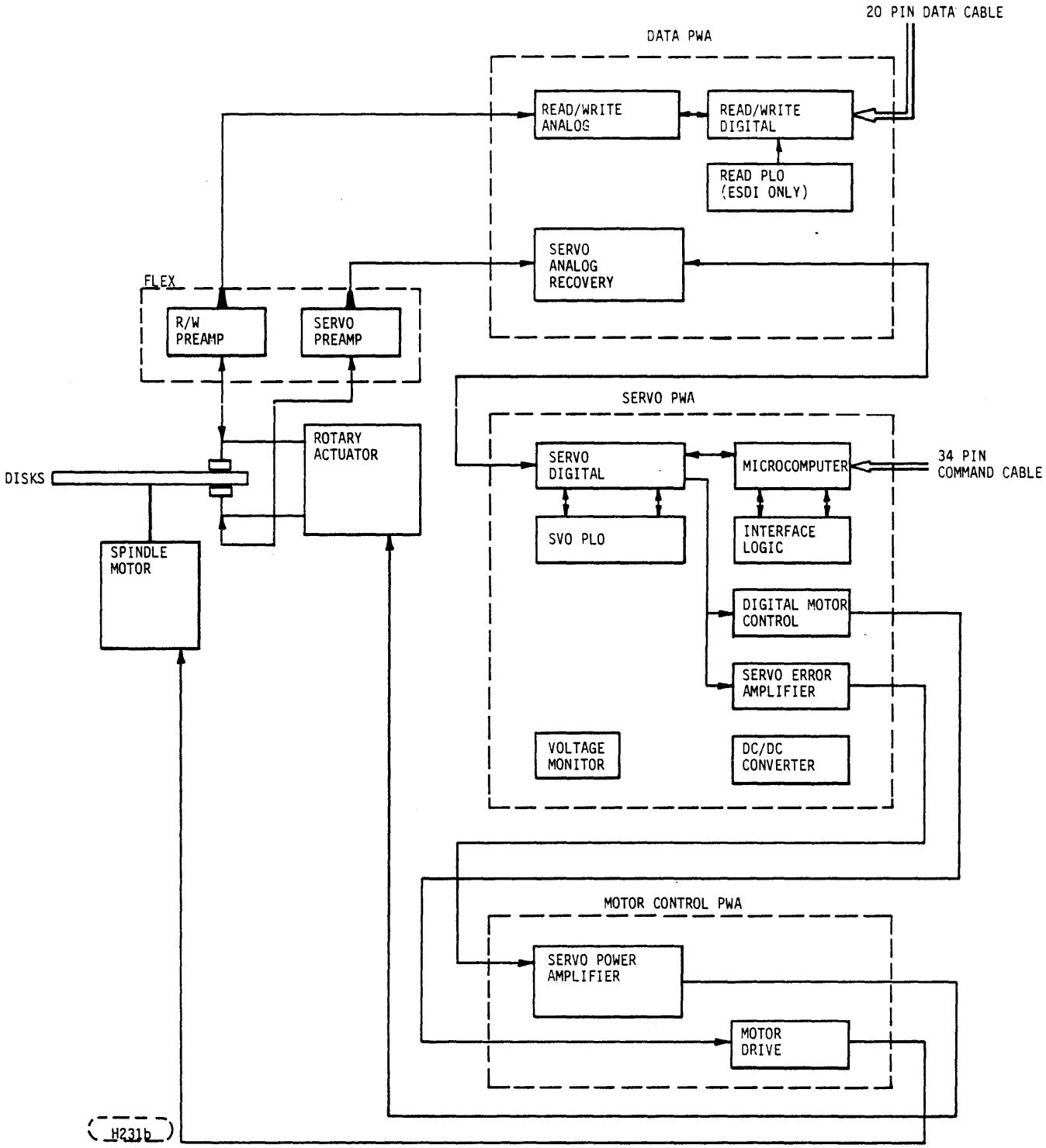


FIGURE 5-1. WREN II GENERAL BLOCK DIAGRAM

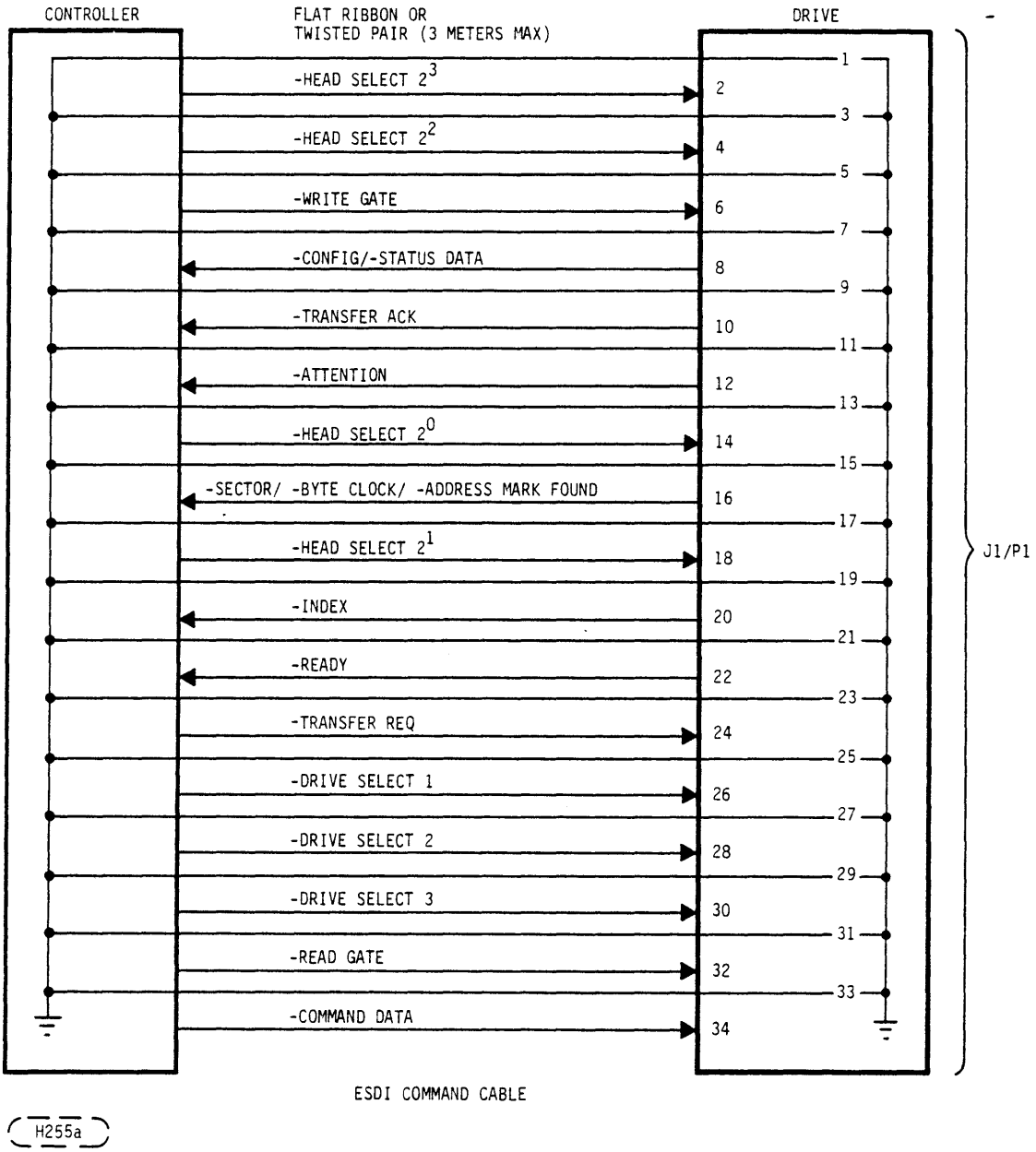
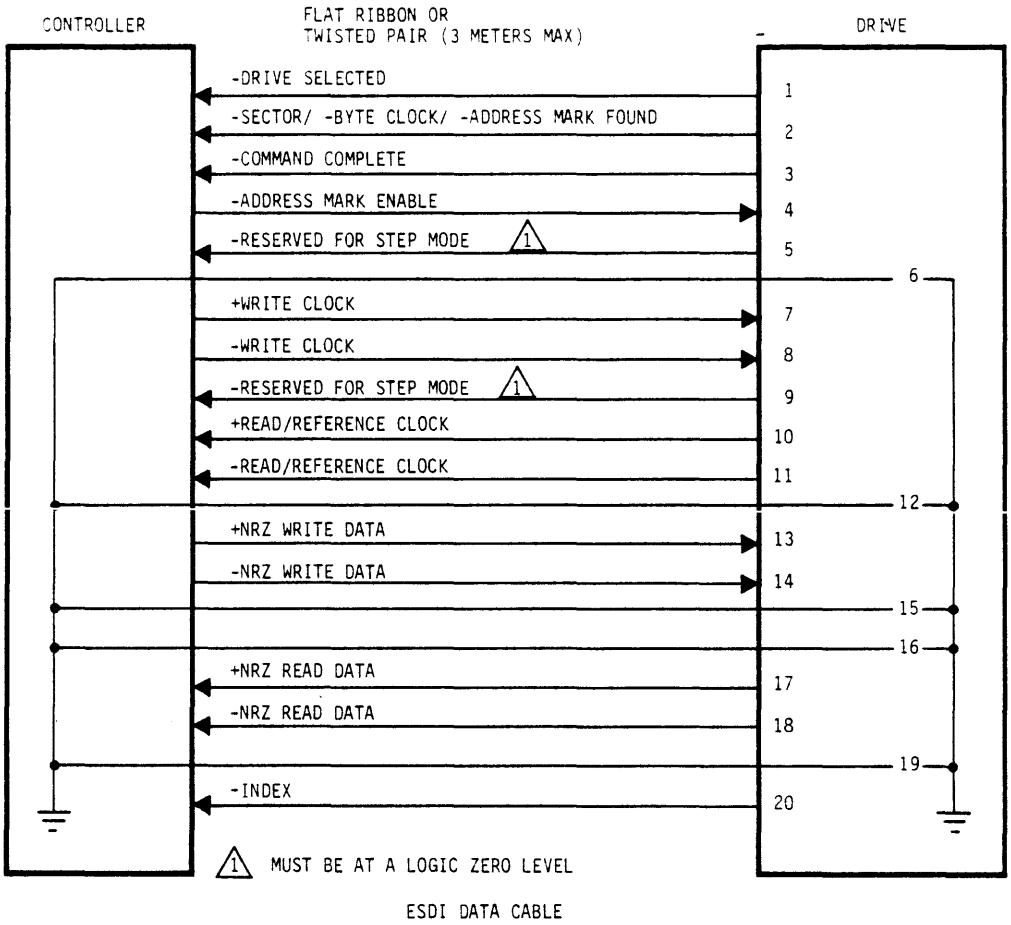
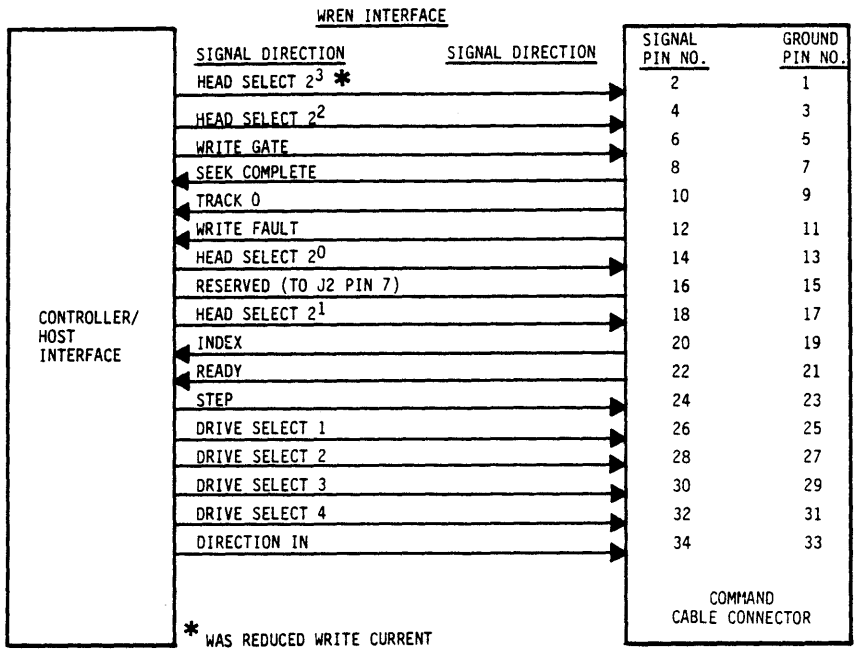


FIGURE 5-2A. ESDI (SHEET 1 OF 2)



H256a

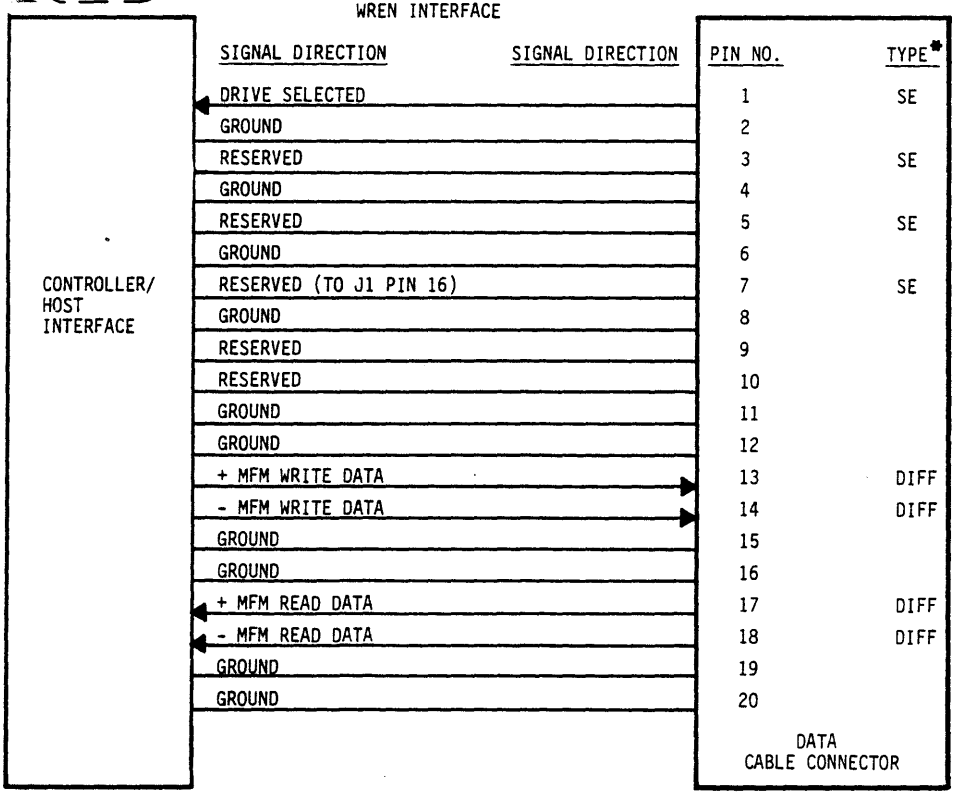
FIGURE 5-2A. ESDI (SHEET 2 OF 2)



NOTE: ALL SIGNALS IN THE COMMAND CABLE ARE SINGLE ENDED SIGNALS.

CDC 506 COMMAND CABLE

H254a



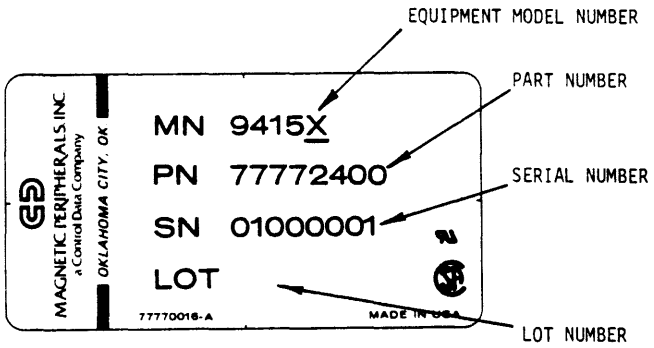
*SE = SINGLE-ENDED SIGNAL

DIFF = DIFFERENTIAL SIGNAL

FF141a

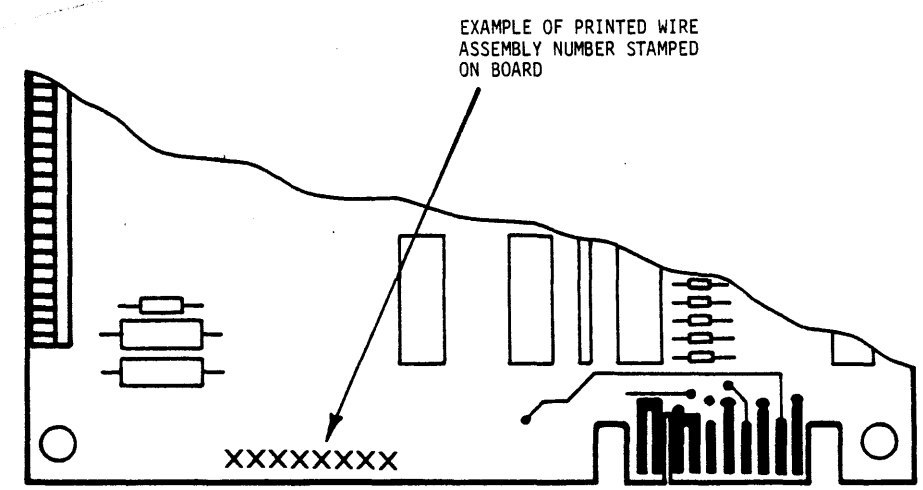
CDC 506 DATA CABLE

FIGURE 5-2B. CDC506 INTERFACE



H254b

FIGURE 5-3. SAMPLE LABEL OF WREN II DISK DRIVE



H104b

FIGURE 5-4. PWA IDENTIFICATION

MAINTENANCE 6

6.1 INTRODUCTION

This section contains the instructions required to maintain the CDC Model 94155 and 94156 WREN II Disk Drives. The information presented is provided for corrective maintenance as no preventative maintenance is required. All maintenance should be performed by qualified and trained service personnel.

The maintenance procedures detailed below should be performed only after power to the WREN drive has been turned off and data-signal cable connectors removed. The drive should then be placed with the chassis on a sponge rubber or foam mat on a flat surface.

The maintenance procedures provided in this section assume that the proper test equipment is available to troubleshoot and replace selected malfunctioning parts. Parts replacement is performed OUTSIDE THE SEALED AREA OF THE DRIVE, ONLY. ENCROACHMENT OF THE SEALED AREA VOIDS THE UNIT WARRANTY.

6.2 SAFETY AND SPECIAL MAINTENANCE PRECAUTIONS

- Avoid overtightening hardware (screws, nuts, etc.) when replacing assemblies and components. All screws and nuts are of the low carbon variety.
- Do not connect or disconnect cables without first removing all power form the drive.

CAUTION

The circuit assemblies contained in this equipment can be degraded or destroyed by ELECTRO-STATIC DISCHARGE (ESD).

Static electrical charges can accumulate quickly on personnel, clothing, and synthetic materials. When brought in close proximity to or, in contact with delicate components, ELECTRO-STATIC DISCHARGE OR FIELDS can cause damage to these parts. This damage may result in degraded reliability or immediate failure of the affected component or assembly.

To insure optimum/reliable equipment operation, it is required that technical support personnel discharge themselves by periodically touching the chassis ground prior to and during the handling of ESD susceptable assemblies. This procedure is very important when handling Printed Circuit Boards.

CAUTION

NEVER remove the cover of the WREN. Servicing items in the upper sealed environmental enclosure (heads, media, actuator, etc.) requires special facilities. Encroachment of the sealed enclosure voids the unit warranty. Only the printed-circuit boards, LED/grommet and ground spring external to the sealed area can be replaced without special facilities.

SPECIAL TOOLS	APPLICATION
TORX TX-15	6-32 Six Spline Socket Drive Machine
TORX TX-09	4-40 Screws

6.3 LED/MOUNT REMOVAL AND REPLACEMENT

1. Remove power from WREN Disk Drive.
2. Disconnect DC power, interface, and data-signal cables.
3. Place the WREN on a sponge rubber or foam pad on a flat surface with the chassis down.
4. Remove front panel by removing the two mounting screws.
5. Remove the section of the LED mount by prying it up with a small flat blade screwdriver.
6. Slide the LED out the front of the front panel.
7. Remove LED from mount section.

Replace LED by reversing the procedure.

NOTE

The shorter lead of the LED is nearest to the outside edge of the front panel.

6.4 MOTOR CONTROL PWA REMOVAL AND REPLACEMENT

1. Remove power from WREN drive.
2. Remove two mounting screws and spacers.
3. Disconnect two cables to PWA.

Replace Control PWA by reversing the procedure.

6.5 SERVO PWA REMOVAL AND REPLACEMENT

1. Follow instructions 1 thru 4 in paragraph 6.3 describing LED REMOVAL AND REPLACEMENT.
2. Remove the two shield mount screws behind the front panel.
3. Remove the four shock mount screws at each corner of the chassis.
4. Disconnect the three cables to the Servo and Data PWA.

CAUTION

Be sure to support the drive so it does not fall onto the PWA boards. Note the orientation of all cables, screws, and spacers for later re-assembly.

5. Lift the sealed enclosure of the drive carefully.
6. Place the sealed enclosure on its cover (upside down) on the sponge rubber or foam pad.
7. Remove the 4 screws holding the PWA assembly located on the bottom side of the chassis.
8. Remove the 4 screws holding the PWA assembly together.
9. Separate the two PWA boards, being careful not to lose the four spacers.

The Servo PWA is installed by reversing these instructions.

6.6 DATA PWA REMOVAL AND REPLACEMENT

1. Follow instructions 1 thru 9 in paragraph 6.5 describing SERVO PWA REMOVE AND REPLACEMENT.
2. Remove the four spacers, being careful not to lose them.

The Data PWA is installed by reversing these instructions.

6.7 GROUND SPRING REMOVAL AND REPLACEMENT

1. Follow instructions 1 thru 6 in paragraph 6.5 describing SERVO PWA REMOVAL AND REPLACEMENT.
2. Remove the two screws holding the ground spring down.
3. Remove ground spring.

Install ground spring by reversing the instructions.

NOTE

Center the ground spring over the center of the motor as much possible.

6.8 PARTS DATA

Recommended spare parts for the WREN external to the sealed enclosure, are shown in Figure 6-1. Only these parts can be replaced without special facilities. Encroachment of the sealed enclosure voids the unit warranty.

When ordering replacement parts for the WREN, describe the part and include the part number and serial number from the label (Figure 5-3) located on the back of the unit.

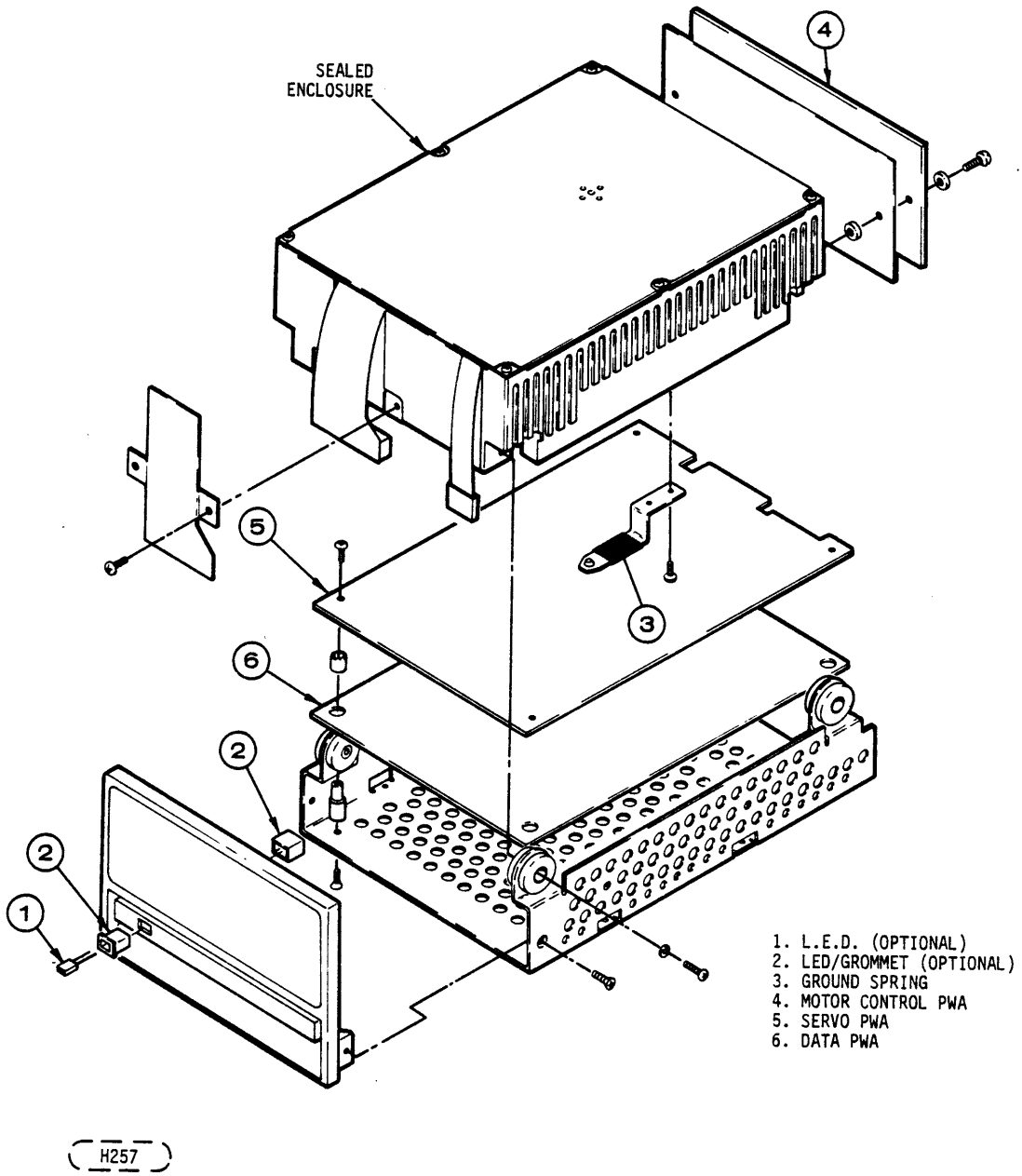


FIGURE 6-1. WREN II RECOMMENDED SPARES

USER COMMENTS

FILE REFERENCE

FROM:

Date _____

Name _____

Address _____

City _____

State _____ Zip Code _____

Area Code _____ Phone _____

NOTE:

This form is not intended to be used as an order blank. Control Data Corporation welcomes your evaluation of this publication. Please indicate any errors, suggested additions or deletions, or general comments below.

Business-related questions are to be directed to your Local Sales Office.

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Document: (Title/Number/Revision) _____

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Customer Training
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Phone: (405) 324-3001

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P.O. BOX 12313
Oklahoma City, Oklahoma
73157

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- ☐ COURSE DESCRIPTION
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