83322200

CONTROL DATA CORPORATION

CDC® STORAGE MODULE DRIVE

BK4XX

BK5XX

GENERAL DESCRIPTION
OPERATION
THEORY OF OPERATION
DISCRETE COMPONENT CIRCUITS

HARDWARE REFERENCE MANUAL

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or use Comment Sheet in the back of this manual.

LIST OF EFFECTIVE PAGES

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PREFACE

This manual contains information applicable to all the Storage Module Drives (SMDs) listed in the configuration charts (found following the table of contents). The configuration charts define each of the equipments covered by this manual in terms of cabinet mounting styles, cabinet colors, and the various electronic features provided. Since this manual covers all the various configurations available on the SMD, it is necessary to understand exactly which configuration you have, in order to know which procedures in this manual are applicable to your drive.

This manual has been prepared for customer engineers and other technical personnel directly involved with maintaining the SMD.

Reference information is provided in four sections in this manual:

- Section 1 - General Description
- Section 2 - Operation
- Section 3 - Theory of Operation
- Section 4 - Discrete Component Circuits

Other manuals, also applicable to the SMD's covered in this manual, are as follows:

Publication No.	Title
83322150	Hardware Maintenance Manual Volume 1; Installation and Checkout, Maintenance, Parts Data
83322250	Hardware Maintenance Manual Volume 2; Diagrams and Wire Lists. Applicable to BK4XX
83322240	Hardware Maintenance Manual Volume 2; Diagrams and Wire Lists. Applicable to BK5XX
83322440	Normandale Circuits Manual; General Theory, Logic Symbology, Data Sheets.

A guide for the Disk Drive Operator, publication number 83323770, is also available. The guide may be ordered through Literature Distribution Services at the following address:

Control Data Corporation
Literature Distribution Services
308 North Dale St.
St. Paul, MN 55103

CONTENTS

FIGURES

TABLES

ABBREVIATIONS

ABR	Absolute Reserve
ABV	Above
ADDR	Address
ADRS	Address
AGC	Automatic Gain Control
AM	Address Mark
AMPL	Amplifier
BLK	Black
BLW	Below
CAR	Cylinder Address Register
CH	Channel
CHAN	Channel
CNTLGL	Centrifugal
CNTR	Counter
COMP	Compensation
COMPTR	Comparitor
CONFIG	Configuration
CONT	Continued
CR REF	Cross Reference
CYL	Cylinder
D/A	Digital To Analog
DCDR	Decoder
DIFF	Difference
DLY	Delay
DRVR	Driver
DSBL	Disable
ECL	Emitter Coupled Logic
ECO	Engineering Change Order
EMER	Emergency
EN	Enable
EOT	End Of Travel
EQUIP	Equipment
EQUIV	Equivalent
FCO	Field Change Order
FF	Flip Flop
FIG	Figure
FLT	Fault
FREQ	Frequency
FTU	Field Test Unit
FWD	Forward
GND	Ground
HD	Head
I/O	Input-Output
INTLK	Interlock
LAP	Logical Address Plug
LD	Load
MAINT	Maintenance
MAX	Maximum
MB	Megabyte
MFM	Modified Frequency Modulation
MK	Mark
MULT	Multiple
NC	No Connection
NEG	Negative
NFR	Not Field Replaceable
NO	Number
NOM	Nominal
NORM	Normal
NRM	Normal
NRZ	Nonreturn To Zero
PC PT	Piece Part
PLO	Phase Lock Oscillator
PN	Part Number
POS	Positive
PWR	Power
RCVRS	Receivers
RD	Read
RDY	Ready
REC	Receiver
REF	Reference
REG	Register
REV	Reverse
RGTR	Register
RTM	Reserve Timer
RTZ	Return To Zero
S&IOABC	Sector and Index On A and B Cable
S&IOBC	Sector and Index On B Cable
S/C	Series Code
SEC	Second
SEL	Select
SEQ	Sequence
SER	Servo
SH	Sheet
SOL	Solenoid
SR	Servo
SW	Switch
T	Track
TBS	To Be Supplied
TLA	Top Level Assembly
TP	Test Point
TRK	Track
TTL	Transistor Transistor Logic
UNREG	Unregulated
VCO	Voltage Controlled Oscillator
W+R	Write Or Read
W·R	Write and Read
W/	With
W/O	Without
WRT	Write
WT	White
XDUCER	Transducer
XMTR	Transmitter

SECTION 1

GENERAL DESCRIPTION

INTRODUCTION

The Control Data BK4XX and BK5XX Storage Module Drives (SMD's) are high speed, random access digital data storage devices that connect to a central processor through a controller. The major difference between the drives is their storage capacity. The total data storage capacity of the BK4XX is 40 megabytes, and the BK5XX is 80 megabytes. All the equipment specifications for each drive are listed in table 1-1.

The remainder of this section provides a general description of the drives and is divided into the following areas:

- Data Storage Medium - Describes the disk pack which is the medium used to store the data.
- Drive Functional Description - Explains the basic function of the drive.
- Drive Physical Description - Provides a basic description of the drives physical characteristics.
- Equipment Configuration - Describes the various drive configurations and how to identify them.

TABLE 1-1. EQUIPMENT SPECIFICATIONS

Specification	Value
Size	Refer to Space and Clearance paragraph in Installation and Checkout section of maintenance manual volume 1.
Weight Pedestal Cabinet Acoustic Cabinet Acoustic Cabinet With Drawer Rack Mount (both 30 and 36 in) Basic Nude	 243 lbs. (110 kg) 340 lbs. (155 kg) 567 lbs. (258 kg) 160 lbs. (73 kg) 135 lbs. (61 kg) 140 lbs. (62 kg)
Temperature Operating Operating Change/Hr Transit (packed for shipment) Non-Operating Change/Hr	 59° F (15.5° C) to 90° F (32.2°C) 12° F (6.6° C) per hr -40° F (-40.4° C) to 158° F (70.0° C) 36° F (20° C) per hr
Relative Humidity Operating Transit (packed for shipment)	 20% to 80% 5% to 95% } No Condensation
Altitude Operating Transit (packed for shipment)	 -1000 ft (305 m) to 6500 ft (2000 m) -1000 ft (305 m) to 15,000 ft (4572 m)
Disk Pack Type Disks/Pack Data Surfaces Servo Surfaces Usable Tracks/Surface Tracks/Inch Track Spacing (center to center) Coating	 40 MB - 876 80 MB - 877 3 (Top and bottom disks are for protection only.) 5 1 40 MB - 411 80 MB - 823 40 MB - 192 80 MB - 384 40 MB - .0052 (.13 mm) 80 MB - .0026 (.66 mm) Magnetic Oxide

Table continued on next page

TABLE 1-1. EQUIPMENT SPECIFICATIONS (Contd)

Specification	Value
Data Capacity*	40 MB / 80 MB
Bytes/Track	20 160 / 20 160
Bytes/Cylinder	100 800 / 100 800
Bytes/Spindle	41 428 800 / 82 958 400
Cylinders/Spindle	411 / 823
Recording Characteristics	
Mode	Modified Frequency Modulation (MFM)
Density (nominal)	
Outer Track	4038 bits/in (1590 bits/cm)
Inner Track	6038 bits/in (2377 bits/cm)
Rate (nominal)	9.67 MHz (1 209 600 bytes/sec)
Heads	
Read/Write	5
Servo	1
Read/Write Width	40 MB - 0.004 in (0.102 mm) 80 MB - 0.002 in (0.051 mm)
Seek Characteristics	
Mechanism	Voice Coil, Driven By Servo Loop
Max Seek Time (411 or 823 Tracks)	55 ms
Max Track Seek Time	6 ms
Average Seek Time	30 ms
Latency**	
Average	8.33 ms (at 3600 r/min)
Maximum	17.3 ms (at 3474 r/min)
Spindle Speed	3600 r/min
Controllers Per Drive	1 or 2 - Refer to channel access column on configuration chart in front matter of manual.
Drives Per Controller	16 maximum
Power Requirements	Refer to configuration chart in front matter of manual. Also, refer to Installation and Checkout section of maintenance manual volume 1.

* Based on 8 bit bytes and not allowing for sectoring tolerance gaps.
** Latency is time required to reach specific track location after drive is on cylinder.

DATA STORAGE MEDIUM

The data storage medium for the drive is a disk pack, consisting of five 14-inch disks, center mounted on a hub (see figure 1-1). The disk pack is portable and interchangeable between equivalent drives. The packs are not interchangeable, however, between the 40 and 80 megabyte drives.

The disk pack has a total of six usable surfaces, each coated with a layer of magnetic oxide and related binders and adhesives. One of these surfaces, referred to as the servo surface, contains information prerecorded at the factory. This surface is used by the drive to generate position information and various timing signals. The remaining five surfaces can be used by the system for data storage and are referred to as data surfaces.

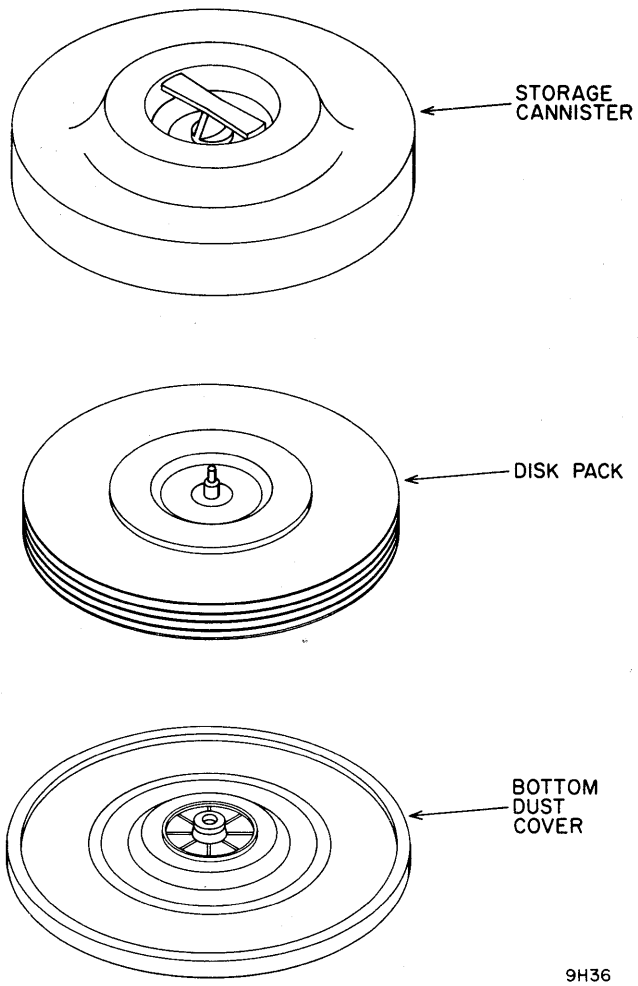


Figure 1-1. Disk Pack

DRIVE FUNCTIONAL DESCRIPTION

The drive contains all the circuits and mechanical devices necessary to record data on and recover it from the disk pack (see figure 1-2). The necessary power for this is provided by the drives power supply, which receives its input power from the site main power source.

All functions performed by the drive are done under direction of the controller. The controller communicates with the drive via the interface which consists of a number of I/O lines carrying the necessary signals to and from the drive.

Some interface lines, including those that carry commands to the drive, are not enabled unless the drive is selected by the controller. Unit selection allows the controller, which can be connected to more than one drive, to initiate and direct an operation on a specific unit.

All operations performed by the drive are related to data storage and recovery (normally referred to as writing and reading). The actual reading and writing is performed by electromagnetic devices called heads that are positioned over the recording surfaces of the rotating disk pack. There is a separate head for each surface in the pack and the heads are positioned in such a way that data is written in concentric tracks around the disk surfaces (see figure 1-2).

Before any read or write operation can be performed the controller must instruct the drive to position the heads over the desired track (called seeking) and also to use the head located over the surface (head selection) where the operation is to be performed.

After selecting a head and arriving at the data track, the controller still must locate that portion of the track on which the data is to be written or read. This is called track orientation and is done by using the Index and Sector signals generated by the drive. The Index signal indicates the logical beginning of each track and the Sector signals are used by the controller to determine the position of the head on the track with respect to Index.

When the desired location is reached the controller commands the drive to actually read or write the data. During a read operation the drive recovers data from the pack, and transmits it to the controller. During a write operation, the drive receives data from the controller, processes it and writes it on the disk pack.

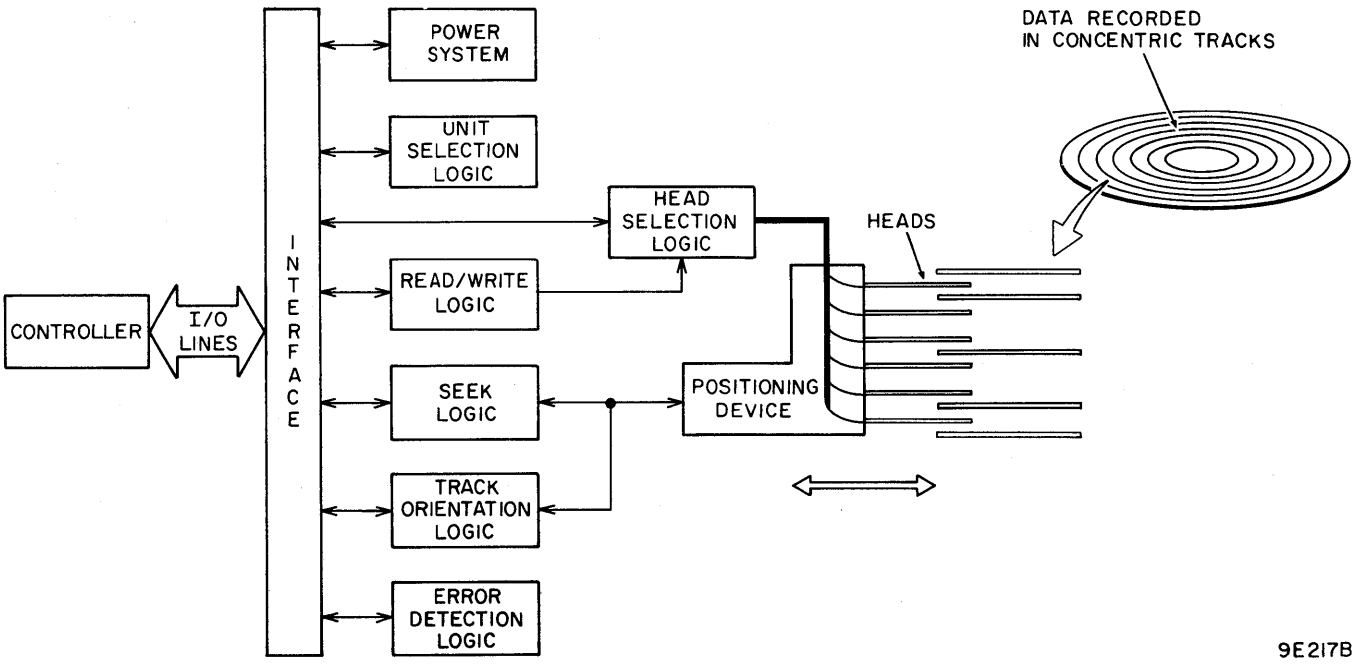


Figure 1-2. Drive Functional Blocks

The drive is also capable of recognizing certain errors that may occur during its operation. When an error is detected, it is indicated either by a signal to the controller or by a maintenance indicator on the drive itself.

DRIVE PHYSICAL DESCRIPTION

GENERAL

The physical description of the drive is divided into two areas: 1) Mounting Configuration Description, and 2) Drive Electronics Package Description. The mounting configuration description deals with the various cabinet styles in which the SMD is available. The drive electronics package description deals with the functional electronics of the SMD.

MOUNTING CONFIGURATION DESCRIPTION

The SMD is available in a number of mounting configurations (see figure 1-3). The mounting configurations provides a means of enclosing the drive electronics package and preventing dust and dirt from entering the pack area. In addition, some of the mounting configurations provide acoustic isolation. Some units (rack and drawer mounted) are mounted on slide rails, others are mounted in cabinets, and the naked unit is available as a desk top unit or can be mounted in a user supplied cabinet. Table 1-2 lists the names of the various mounting configuration assemblies.

TABLE 1-2. MOUNTING CONFIGURATION ASSEMBLIES

Index Number	Assembly Name
1	Pack Access Cover
2	Case Assembly
3	Top Panel
4	Rear Door Assembly
5	Side Panel Assembly
6	Front Door Assembly
7	Top Filler Panel
8	Bottom Filler Panel

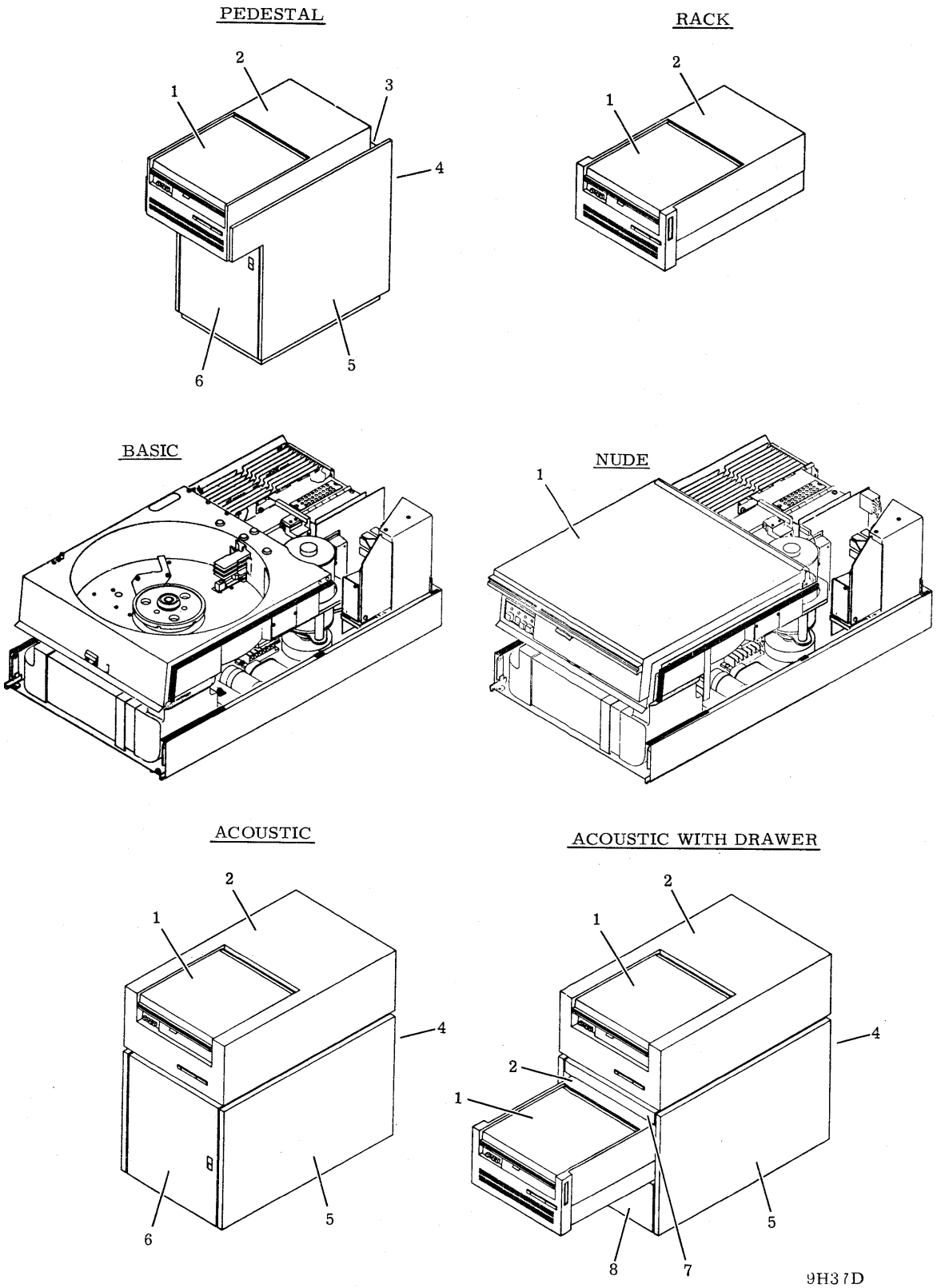


Figure 1-3. Drive Mounting Configurations

DRIVE ELECTRONICS PACKAGE DESCRIPTION

The drive electronics package contains three major assemblies: 1) the base assembly, 2) the logic chassis assembly, and 3) the deck assembly. Figure 1-4 illustrates these major assemblies as well as the subassemblies contained within each of them. Table 1-3 defines each of the subassemblies. The base assembly provides a means of mounting the drive electronics package to the mounting configuration used. It also contains the hinge plate to which the deck is attached. The deck can then be raised and lowered to provide maintenance access to the various elements contained within the base or on the underside of the deck. The logic chassis is attached to the deck by a hinged bracket on the top of the magnet assembly. In this way, the logic chassis can be raised or lowered to provide access to the wirewrap panel for maintenance purposes.

TABLE 1-3. DRIVE ELECTRONICS PACKAGE ASSEMBLIES

Assembly	Subassembly	Purpose
Base	Absolute Filter	Removes contaminants from air before it is forced into pack area.
	AC Power Supply	Filters and controls ac power and provides power to drive and blower motors and to dc power supply.
	Blower Motor	Blows clean air into pack area and cooling air into logic chassis.
	DC Power Supply	Rectifies ac power and provides seven dc output voltages as well as emergency retrack control.
	Power Control	Controls application of ac and dc power. Panel contains an elapsed time meter and circuit breakers.
Logic Chassis	I/O Cards	Interfaces I/O cable with backpanel.
	Logic Cards	Contain the majority of the integrated and discrete circuitry which makeup functional logic on machine.
	Terminator Cards	(Used only on last drive in a daisy chain string and on all star configuration drives.) Contain termination resistors for receivers and transmitters.
	Wirewrap Panel	Contains all wiring which interconnects logic cards, I/O cards, Terminator cards, and miscellaneous cables attached to logic chassis.
Deck	Actuator	Used to position servo and read/write heads. Made up of rail bracket, rails, carriage and coil assembly, magnet assembly, and also contains velocity transducer.
	Control Panel	Used by operator to control operation of drive. Contains three switches and indicators and the logical address plug.

Table continued on next page

TABLE 1-3. DRIVE ELECTRONICS PACKAGE ASSEMBLIES (Contd)

Assembly	Subassembly	Purpose
Deck (Contd)	Drive Motor and Brake	Drive motor drives spindle which in turn drives disk pack. Brake is used to decelerate pack after drive motor is turned off.
	Heads	Servo head reads data from disk pack servo surface to control actuator positioning. Read/write heads used to record and read back data on disk pack data surfaces.
	Pack Cover Solenoid	This optional feature locks pack access cover closed whenever disks are turning or power is removed from drive.
	Pack Cover Switch	Prevents drive motor start sequence from being initiated when pack access cover is opened.
	Parking Brake	Prevents spindle from turning while pack is being installed or removed.
	Power Amplifier	Provides final amplification of servo positioning signal before it is applied to voice coil.
	Read/Write Logic	Contains the logic associated with head selection, read amplification, and write data signal shaping.
	Shroud	Provides protection and ventilation for disk pack.
	Speed Transducer	Magnetic pickup which provides information to logic on relative speed of disk pack.
	Spindle	Provides surface to secure disk pack and means of transmitting drive motor rotational motion to pack.
	Track Servo Preamplifier	Provides first stage of amplification for track servo signal which is read from disk pack by servo head.

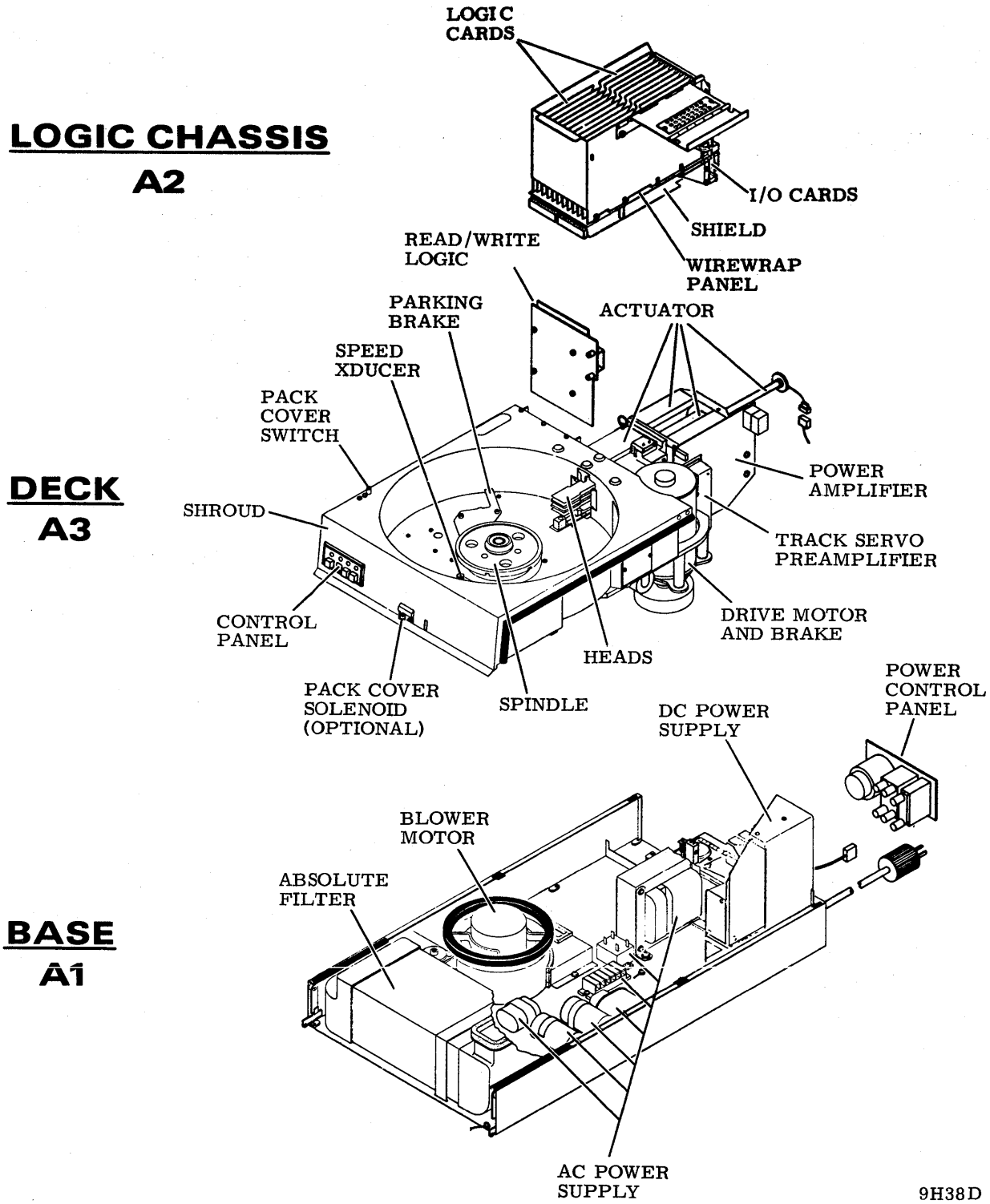


Figure 1-4. Drive Electronics Package

EQUIPMENT CONFIGURATION

GENERAL

The equipment configuration is identified by the equipment identification plate and by the FCO log. It is necessary to identify the equipment configuration to determine if the manuals being used are applicable to the equipment. The following describes the cabinet identification plate, FCO log and manual to equipment correlation.

EQUIPMENT IDENTIFICATION PLATE

General

This plate is attached to the front of the shroud on the drive (refer to figure 1-5). This plate identifies the drives basic mechanical and logical configuration at the time it leaves the factory. The information contained on this plate is defined in the following.

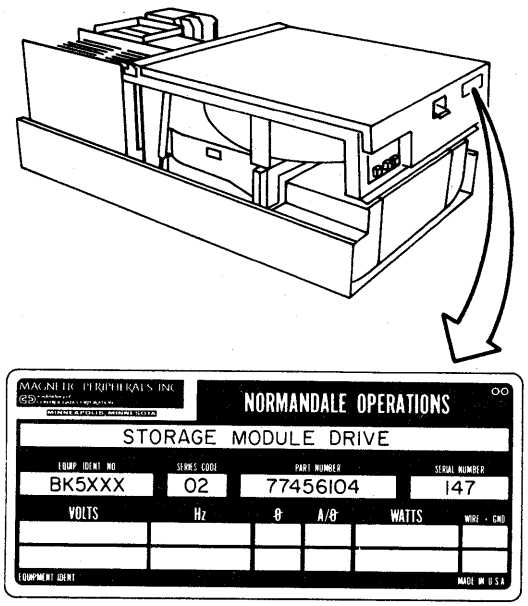


Figure 1-5. Equipment Identification Plate

Equipment Identification Number

This number is divided into the two parts shown in the example:

EXAMPLE: BK5 A2A

Equipment Identifier — BK5

Type Identifier — A2A

The equipment identifier indicates the basic functional capabilities of the drive. This number will be either BK4 or BK5. The differences between these units can be determined by referring to the configuration chart in front matter of this manual.

The type identifier indicates differences between drives that have the same equipment number. These differences are necessary to adapt a drive to specific system requirements. However, they do not change the overall capabilities of the drive as defined in the configuration chart.

Different type identifiers are assigned to define differences in input power, data capacity, channel access capabilities, A cable configurations, pack interlock solenoid (presence or absence), equipment colors, and equipment mounting styles. The configuration chart defines each of these catagories for every equipment identification number. Most of the catagories are self-explanatory. The following provides a further explanation of some of the areas.

- Channel Access - The drives are available in either single channel access (capable of being connected to one controller) or dual channel access (capable of being connected to two controllers at the same time).

- A Cable Configuration - The numerous A Cable configurations fall into three basic categories.

  60-Pin Configurations

  The standard configuration uses a 60-pin, flat cable and includes the Sector and Index signals. The configuration chart notation for these units is "60-pin". This same cable may be used with a B Cable that also includes Sector and Index signals. These units are designated by the abbreviation S&IOABC. A third possibility is a 60-pin, flat cable with the Sector and Index signals moved to the B Cable. The abbreviation for these units is S&IOBC.

50-Pin Configuration

The standard configuration uses a 50-pin, flat cable and includes the Sector and Index signals. The configuration chart notation for these units is "50-pin".

75-Pin Configuraiton

Some unique units have a flat-to-round, 60-75 pin A Cable configuration. These units are covered in separate manual supplements and are noted in the configuration chart as "75-pin".

Series Code

The series code represents a time period within which a unit is built. While all units are interchangeable at the system level, regardless of series code; parts differences may exist within units built in different series codes. When a parts difference exists, that difference is noted in the parts data section of maintenance manual volume 1.

Part Number

This number indicates the top level assembly number of the equipment and is for factory use only.

Serial Number

Each drive has a unique serial number assigned to it. Serial numbers are assigned sequentially within a family of drives. Therefore, no two equipments will have the same serial number.

FCO LOG

Field Change Orders (FCOs) are generated whenever a condition exists which requires that a machine(s) in the field be changed. It is important that FCOs be installed in the units in a timely manner because, once the FCO is released, the related manuals are changed to show only the post FCO condition. It is also important that the FCO log located on side of logic chassis be kept up to date. Without an accurate record of the changes which have been installed in the unit it would be impossible to relate the machine configuration to the manual.

MANUAL TO EQUIPMENT CORRELATION

Throughout the life cycle of a machine, changes are made, either in the factory build (a series code change) or by FCOs installed in the field. All of these changes are also reflected in changes to the manual package. In order to assure that the manual correlates with the machine, refer to the Manual To Equipment Level Correlation sheet located in the front matter of maintenance manual volume 1. This sheet records all the FCOs which are reflected in the manual. It should correlate with the machine FCO log if all the FCOs have been installed in the machine.

SECTION 2

OPERATION

INTRODUCTION

This section provides the information and instructions necessary for operating the drive and is divided into the following areas:

- Controls and Indicators - Locates and describes various controls and indicators related to operation of the drive.
- Operating Instructions - Describes procedures for operating the drive.

CONTROLS AND INDICATORS

GENERAL

The drive has two basic types of operator controls and indicators. These are (1) Operator control panel (2) power control panel. These are shown on figure 2-1 and explained in the following.

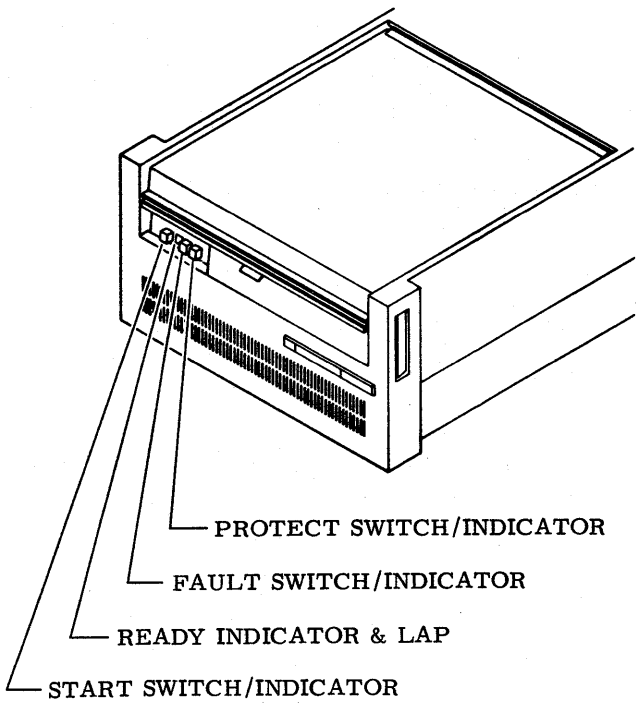


Figure 2-1. Control Panel Switches and Indicators

NOTE

Additional controls and indicators contained on cards in Logic Chassis, and used for maintenance purposes, are described in hardware maintenance manual.

CONTROL PANEL

The control panel is located on the front of the shroud, just below the edge of the pack access cover. The panel contains the switches and indicators required to control and monitor the basic operation of the drive. Figure 2-1 shows these controls and indicators and table 2-1 explains their functions.

POWER CONTROL PANEL

The power control panel is located at the rear of the base assembly. Depending on the mounting configuration of the drive, it may be necessary to open cabinetry in order to gain access to the panel. The panel contains an elapsed time meter and the power control circuit breakers. Figure 2-2 shows the power control panel components and table 2-2 explains their functions.

OPERATING INSTRUCTIONS

GENERAL

This discussion describes the procedures that are performed during normal operation of the drive. These procedures concern the disk pack and power application.

DISK PACK

General

There are two different types of disk packs applicable to the 40 and 80 megabyte drives. These packs are constructed so that they cannot be released from their storage cannister unless they are being installed on the correct drive. Be certain that the disk pack being installed is the proper type for the drive on which it is being installed.

Disk pack information is divided into storage and handling procedures and installation and removal procedures. Be thoroughly familiar with these procedures before attempting them on a drive.

TABLE 2-1. CONTROL PANEL FUNCTIONS

Switch Indicator	Function
START Switch/Indicator	Pressing switch when drive is in power off condition (disk pack not spinning) lights indicator and starts power on sequence, provided following conditions are met. • Disk pack is installed • Pack access cover is closed • All power supply circuit breakers are on
READY Indicator	Lights when unit is up to speed, heads are loaded, and no fault condition exists.
Logical Address Plug	Determines logical address of drive. Address can be set to any number from 0 to 15 by installing proper plug. If no plug is installed, address is 15.
FAULT Switch/Indicator	Lights if a fault condition exists within drive. It is extinguished by any of the following: • Pressing FAULT switch on operator control panel • Fault Clear signal from controller • Maintenance Fault Clear switch on fault card in logic chassis location A04. Conditions causing fault are described in discussion on Fault Detection in section 3 of this manual.
WRITE (Protect) Switch/Indicator	Pressing switch to light indicator, disables drives write circuits and prevents it from writing data on pack. Pressing switch to extinguish indicator, removes disable from write circuits.

TABLE 2-2. POWER CONTROL PANEL FUNCTIONS

Control/Indicator	Function
POWER SUPPLY Circuit Breaker	Applies ac power to transformer which in turn enables dc power supplied.
AC POWER Circuit Breaker	Applies ac power to POWER SUPPLY circuit breaker, blower motor, and to rear door fans used on acoustic mounting configuration only). Also provides power for drive motor; however, control panel START switch must be pressed to enable start sequence for motor.
Elapsed Time Meter	Records accumulated ac power-on time. Meter starts when AC POWER circuit breaker is set to ON.

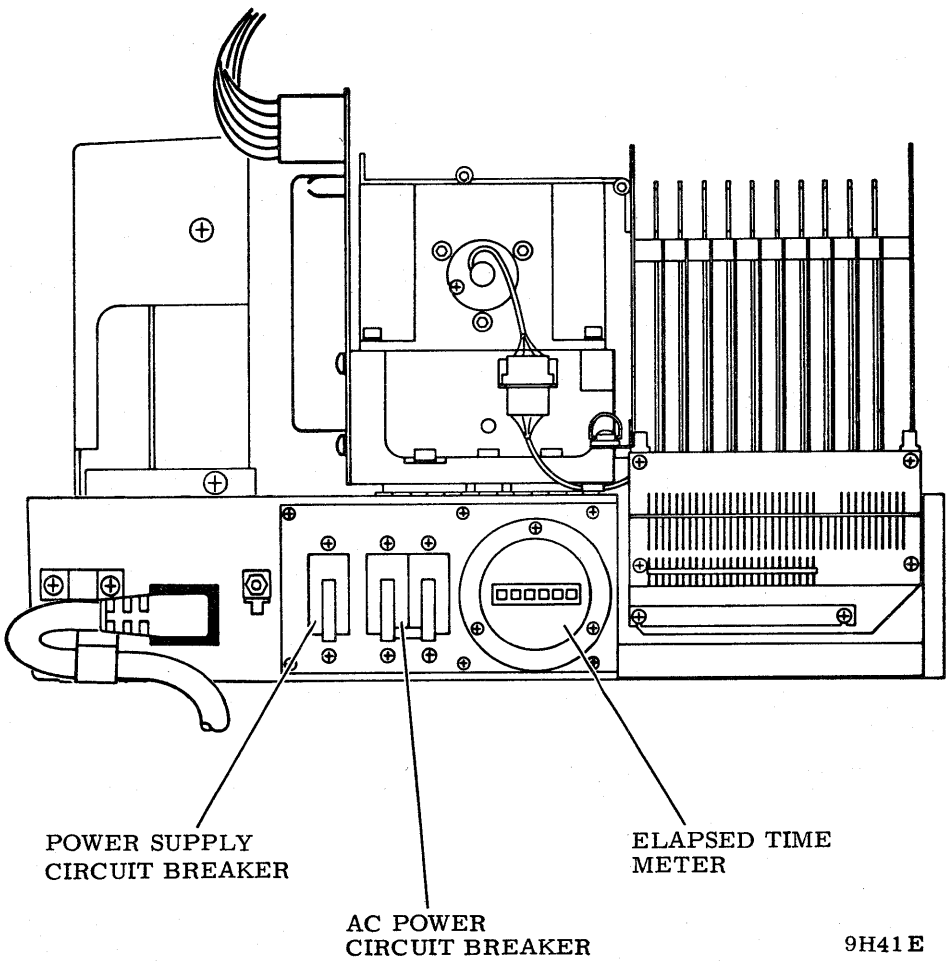


Figure 2-2. Power Control Panel Switches and Indicators

Disk Pack Storage

To ensure maximum disk pack life and reliability, observe the following precautions:

- Store disk packs in machine-room atmosphere (refer to environmental specifications table in maintenance manual volume 1).
- If disk pack must be stored in different environment, allow two hours for adjustment to computer environment before use.
- Never store disk pack in direct sunlight or in dirty environment.
- Store disk packs flat, not on edge. They may be stacked with similar packs when stored.
- Always be sure that both top and bottom of storage cannister are on disk pack and locked together whenever it is not actually installed in a drive.
- When marking packs, use pen or felt tip marker that does not produce loose residue. Never use a lead pencil. Write label before it is applied to disk pack canister.
- Do not attach any label to the disk pack itself. Labels will not remain attached when the pack is spinning and catastrophic head crashes may result. All labels should be placed on the pack canister if required.
- Cleaning of disk surfaces is not recommended. If disks must be cleaned, the cleaning must be done by trained service personnel.

Disk Pack Handling

Because it is possible for a damaged disk pack to cause damage to the heads of a drive, or to have damaged heads cause damage to a disk pack, it is important that the following be observed.

- Be aware of a sudden increase in error rate related to a specific drive or pack.
- Be aware of any unusual noise such as screeching or pinging while heads are loaded on a pack.
- Be aware of a burning odor coming from a drive.
- Be alert to the possibility of contamination such as dust, dirt, grease, oil, or smoke which could accumulate on the pack or heads.

If any of these conditions exist, or there is any doubt about the pack or drive's functional condition, call in trained service personnel.

CAUTION

Do not attempt to operate a suspect disk pack on another drive or operate a new disk pack on a drive with suspect heads. To do so may cause further damage.

Disk Pack Installation

The disk pack must be installed prior to performing any drive operation. Disk pack installation consists of setting the pack on the drive's spindle and locking the pack in place. The following describes the procedure.

CAUTION

Failure to ensure cleanliness of pack or shroud area, or failure to purge blower system may cause damage to pack or heads.

1. Set AC POWER circuit breaker to ON and allow blower to operate for two minutes minimum (to purge blower and shroud) before installing pack.
2. Disengage bottom dust cover from pack canister by holding bottom cover and turning canister handle counterclockwise.

CAUTION

Non-fully retracted heads indicate a problem in the drive's servo, and may result in damage to the pack or heads during pack installation or removal. If heads are not fully retracted, contact maintenance personnel. DO NOT push on heads.

3. Raise pack access cover and ensure that heads are fully retracted.
4. Carefully set disk pack on spindle, avoiding abusive contact between pack and spindle. Rotate storage canister handle clockwise until it stops turning. Then, give gentle snugging twist to handle and lift storage canister off pack.
5. Set storage canister into bottom dust cover and set aside for later use.
6. Close pack access cover to prevent entry of dust and contamination.

Disk Pack Removal

Disk pack removal consists of replacing the storage canister and lifting pack off spindle. The following describes the procedure.

1. Press START switch to stop drive motor and unload heads.

CAUTION

Non-fully retracted heads indicate a problem in the drive's servo, and may result in damage to the pack or heads during pack installation or removal. If heads are not fully retracted, contact maintenance personnel. DO NOT push on heads.

2. When disk pack has stopped turning, open pack access cover and ensure that heads are fully retracted.

3. Place storage canister over disk pack so post protruding from center of disk pack is received into storage canister handle.

4. Rotate storage canister handle counterclockwise until pack is free of spindle.

CAUTION

Avoid abusive contact between disk pack and spindle or one or the other may be damaged.

5. Lift disk pack out of drive by canister handle and close pack access cover.

CAUTION

Excessive force in tightening bottom dust cover will damage cover.

6. Install bottom dust cover on pack canister by holding dust cover and turning pack canister handle clockwise.

POWER APPLICATION

General

Power application is divided into two areas: Power On Procedure, and Power Off Procedure. These procedures assume that the drive is connected to an ac power source as defined in the installation section of the maintenance manual. They also assume that the LOCAL/REMOTE switch and MAINT UNIT DISABLE switch(es), located on cards in the logic chassis, are set to REMOTE and NORM respectively.

Power On Procedure

The following procedure describes applying power to the drive:

1. Gain access to power control panel and set AC POWER and POWER SUPPLY circuit breakers to ON. Ensure that blower starts to operate. Allow blower to operate for two minutes minimum before proceeding.

CAUTION

Failure to allow blower to operate for two minute period before installing disk pack will not allow sufficient purge time and may cause damage to disk pack or heads.

2. Install disk pack in accordance with Disk Pack Installation procedure.

3. Press START switch on control panel and ensure that START indicator lights. Drive starts as soon as Sequence Pick and Sequence Hold signals are available from controller. Within 30 seconds of the time the sequence signals are available, the READY indicator should light. Drive is then ready for operation.

Power Off Procedure

The following procedure describes removing power from the drive:

1. Press START switch on control panel to turn off START indicator. Ensure that heads unload and that drive motor stops.

2. Remove disk pack in accordance with Disk Pack Removal procedure.

3. Gain access to power control panel and set AC POWER and POWER SUPPLY circuit breakers to OFF.

SECTION 3

THEORY OF OPERATION

INTRODUCTION

The theory of operation section describes drive functions and the hardware used in performing them. It is divided into the following major areas (refer to figure 3-1):

- Power System Functions - Describes how the drive provides the voltages necessary for drive operation.
- Electromechanical Functions - Provides a physical and functional description of the mechanical and electromechanical systems (disk pack rotation, head positioning, and air flow).
- Interface Functions - Describes the signal lines connecting the drive and controller. It also describes the I/O signals carried by these lines and how they are processed by the drive logic.
- Unit Selection - Explains how the controller logically selects the drive so the drive will respond to controller commands.
- Seek Functions - Explains how the servo logic controls the movements of the head positioning mechanism in positioning the heads over the disk pack.
- Machine Clock Functions - Explains how this circuit uses signals derived from the disk pack to generate timing pulses for the index, sector and read/write circuits.
- Head Operation and Selection - Explains the head selection process.
- Track Orientation - Describes how the drive detects the index pattern which is used to indicate the logical beginning of each track and also explains how the drive derives the sector pulses, which are used to determine the angular position of the read/write heads with respect to Index.
- Read/Write Functions - Describes how the drive processes the data that it reads from and writes on the disk pack.
- Fault Detection - Describes the conditions that the drive interprets as faults.

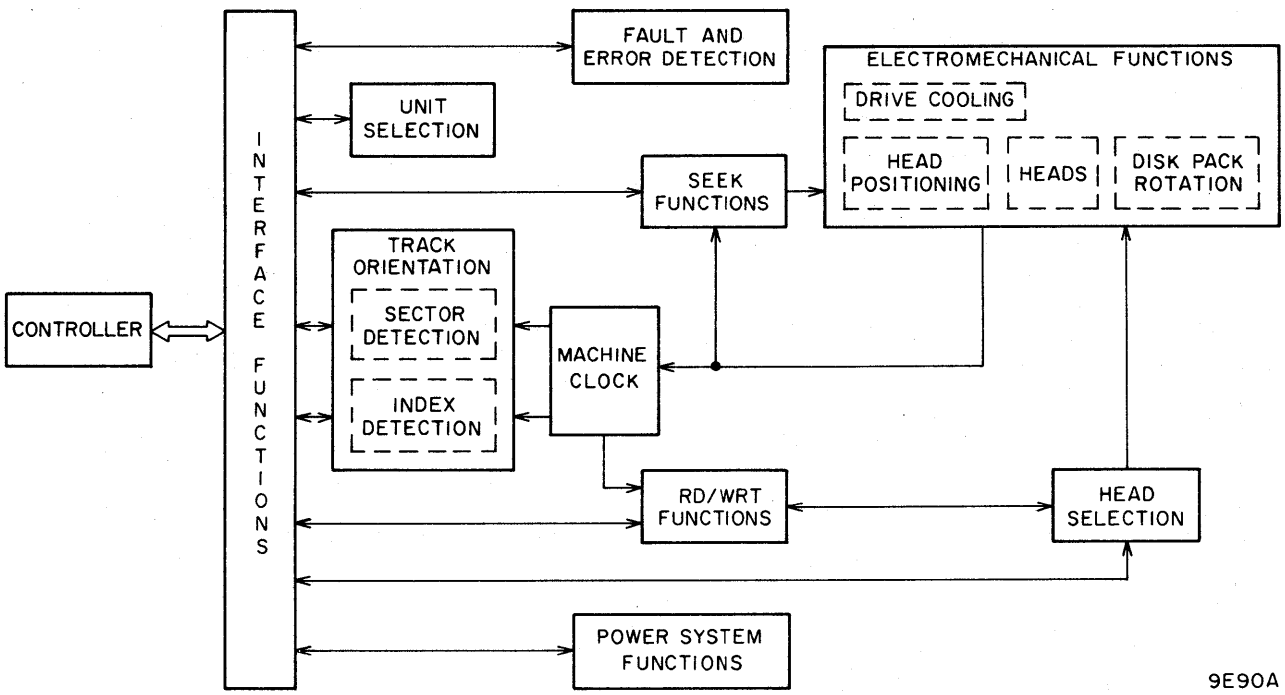


Figure 3-1. Drive Functional Block Diagram

The descriptions in this section are limited to drive operations only. In addition, they explain typical operations and do not list variations or unusual conditions resulting from unique system hardware or software environments.

Functional descriptions are frequently accompanied by simplified logic and timing diagrams. These are useful both for instructional purposes and as an aid in troubleshooting. However, they have been simplified to illustrate the principles of operation. Therefore, the diagrams (and timing generated from them) in the hardware maintenance manual should take precedence over those in this manual if there is a conflict between the two.

POWER SYSTEM FUNCTIONS

GENERAL

The major element in the drives power system is the power supply. The power supply receives its input from the site ac power source and uses it to produce the ac and dc voltages necessary for drive operation. These voltages are distributed to the drive circuitry via circuit breakers.

The drive motor is started and heads load function initiated during the power on sequence. The power off sequence unloads the heads and stops the drive motor. The drives LOCAL/REMOTE switch permits these sequences to be initiated either at the drive (local) or the controller (remote).

The remainder of this discussion provides further description of the power system and is divided into the following areas:

- Power Distribution - Describes how the power is distributed to the drive circuitry.
- Power Sequencing - Explains how the drive is powered up either at the drive or by the controller.
- Power On Sequence - Describes how power is applied to the drive motor and the heads load sequence initiated.
- Power Off Sequence - Describes how the heads are unloaded and the drive motor stopped.
- Emergency Retract - Explains sequence performed when conditions exist requiring the heads be unloaded immediately.

POWER DISTRIBUTION

Power distribution consists of routing power to the various elements in the power supply and rest of the drive so that the power on sequence can be performed. The distribution is controlled by circuit breakers located on the control panel. These circuit breakers also provide overload protection. The power distribution circuits are shown on figure 3-2 and basic operation is explained in the following.

The drive is connected to the main site power by the drive power plug P1. When the AC POWER circuit breaker (A1CB1) is closed, ac power is distributed to the elapsed time meter (M1), rear door fans (acoustic top mount drives only), and drive motor (DM1). The drive motor does not start, however, until the power on sequence is enabled.

When the POWER SUPPLY circuit breaker (A1CB2) is closed, ac power is supplied to transformer (T1). The transformer is a ferroresonant step-down transformer which supplies three output voltages to the dc power supply cards. The dc power supply cards rectify the stepped down ac voltages and regulate them to the required levels needed by the remainder of the drives logic.

In addition to the protection of the circuit breakers, the 42-volt, 20-volt, and 5-volt power supplies are protected by fuses located on the cards. The 12-volt power supply uses a current limiting resistor to provide similar protection.

When the drive is connected to the ac power source, and the two circuit breakers are closed, the power on sequence can begin.

POWER SEQUENCING

Power sequencing refers to the controllers ability to power up the drives. When the sequence is initiated, the drives are powered up one at a time beginning with the drive nearest the controller in the daisy chain string. As each drive reaches the up-to-speed condition, it passes the signal to the next drive in the string. The sequence is initiated when the controller grounds the Sequence Pick and Hold lines in the A cable.

In order for the drive to respond to the power sequencing signals the LOCAL/REMOTE switch must be set to REMOTE and the power on procedure must have been performed. This means that the circuit breakers and the START switch are set to ON. Once these con-

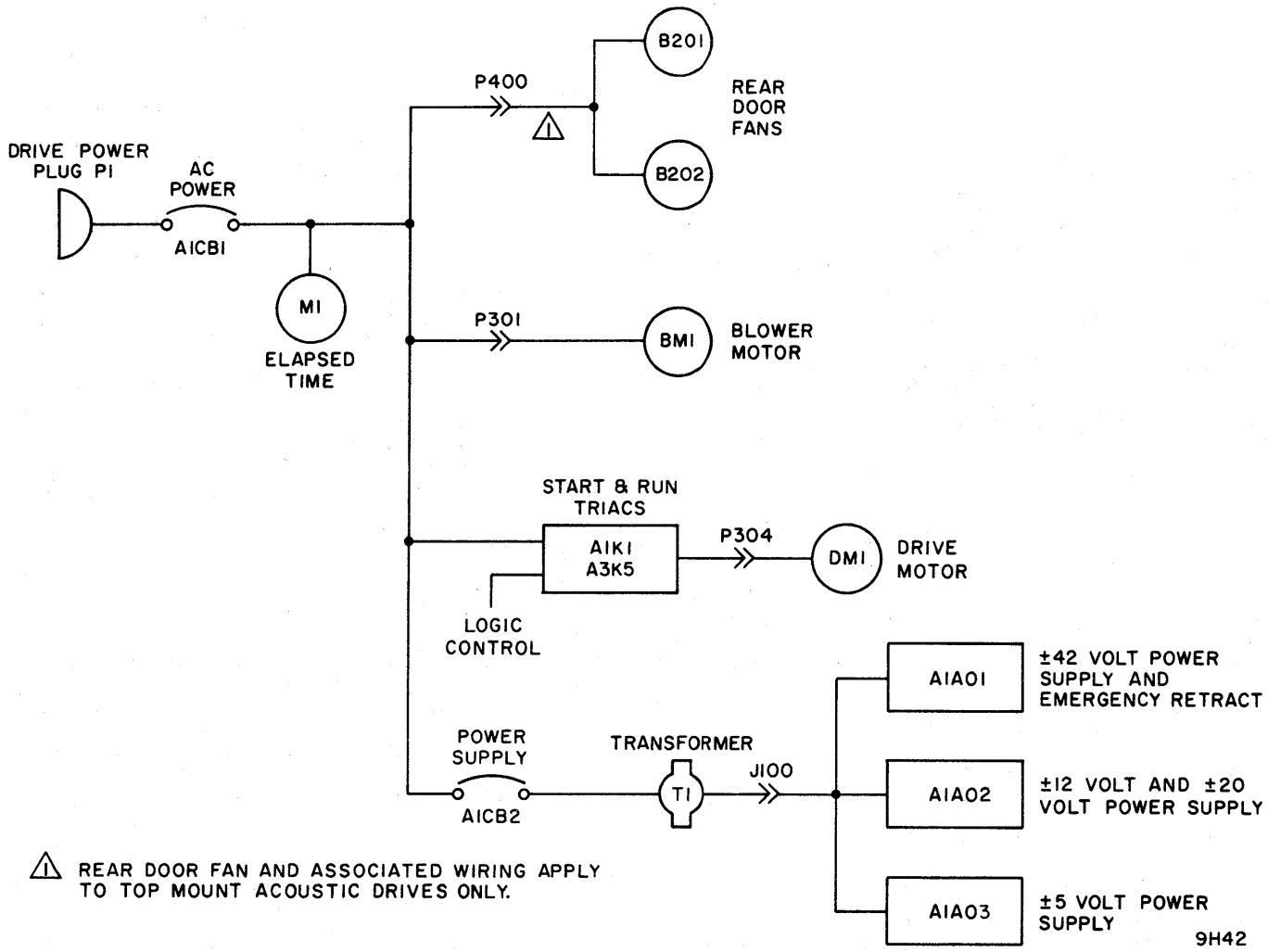


Figure 3-2. Power Distribution Diagram

ditions have been met, the drive will begin the power on sequence as soon as the Sequence Pin In and Hold signals are received.

NOTE

Sequence Pick is the signal received from the controller. Because the signal is interrupted before it is passed to the next drive, it is retitled Sequence Pick In and Pick Out as it is passed from drive to drive. This is not true for the Hold signal.

Figure 3-3 show the power sequencing circuitry contained in each drive. With the drive set to respond to the power sequencing signals, the start relay has transferred (refer to power on sequence) and Sequence Pick In signal cannot pass through the normally closed contacts to generate the Sequence Pick Out signal. Instead, the signal passes through the normally closed contacts of the speed relay (drive is not up to speed, so relay has not transferred) and initiated the drives power on sequence. When the drive reaches up-to-speed, the speed relay transfers. At this point the Sequence Pick In signal has a path through the normally open contacts of both the speed and start relays and the Sequence Pick Out signal is generated. This sequence is continued in each drive in the string.

Whenever a drive is not set to respond to the power sequencing signals, or when a drive is stopped after the power sequencing has taken place, the Sequence Pick signal is passed through the normally closed contacts of the start relay. In this way, the power sequencing is not interrupted when a drive is not being used or when a single drive is powered down. It should also be noted that changing the state of the LOCAL/REMOTE switch does

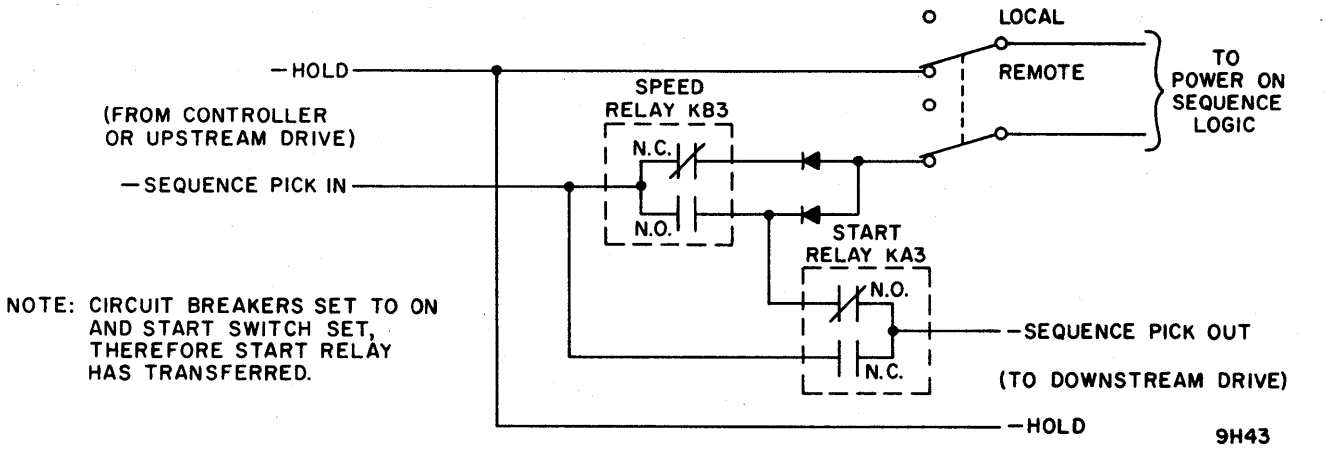


Figure 3-3. Power Sequencing Circuits

not effect the power sequencing of the other drive.

In the power off sequence, the controller removes the ground from the Sequence Pick and Hold lines and all drives are powered off at the same time (refer to power off sequence).

POWER ON SEQUENCE

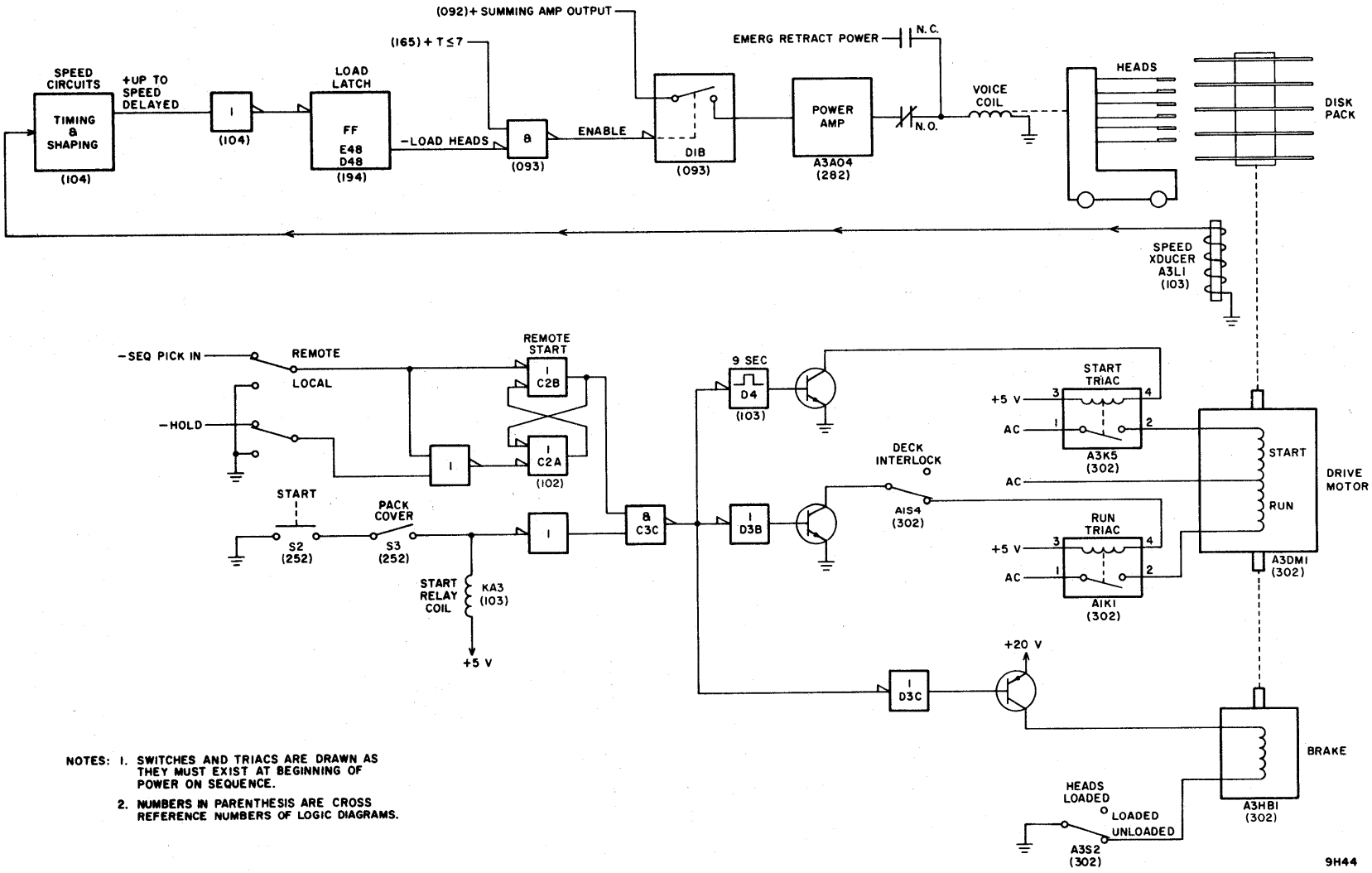
The power on sequence is the chain of events that allow the drive motor to start and the heads to load. In order for the power on sequence to begin, power distribution must be complete. Three functions are accomplished during the sequence: (1) brake power is disabled, (2) ac power is applied to the drive motor and the motor comes up to speed, (3) the heads are loaded onto the pack. Figure 3-4 is a simplified logic diagram of the power on sequence.

The power on sequence begins when the operator presses the START switch. Assuming the pack access cover is closed, the start relay is picked in order to enable power sequencing (refer to power sequencing discussion). Depending on the position of the LOCAL/REMOTE switch, the power on sequence begins immediately (Local) or when the sequence power signals are received from the controller (Remote). In either case the Remote Start latch is set and the sequence enabled.

In order for the drive motor to start the braking power must be disabled. This occurs when transistor Q10 is turned off and disconnects the plus 20 volt braking power. At this point there is still a ground path for the braking power through the closed contacts of the heads loaded switch. Once the heads have loaded, braking power cannot be reapplied until the heads have been unloaded.

At the same time that the braking power is disabled, the ac power is applied to the Start and Run windings of the drive motor. The ac power is controlled by the Start and Run triacs which are enabled when plus 5 volts is applied at pin 3 and ground is available at pin 4. The logical ANDing of the Start and Remote Start signals turns on transistors Q4 and Q7 which then provide the ground paths for the Start and Run triacs. With the ac power applied to the drive motor windings, it starts to turn. After 9 seconds the one shot, in the base current path of transistor Q7, times out. This turns off transistor Q7 and disables the Start triac. The drive motor continues to turn under the power of the run winding. It takes approximately 20 seconds for the drive motor to get sufficiently up to speed (approximately 3000 r/min) to pick the Speed Relay. At this point the Sequence Pick Out signal is sent to the next drive.

At the same time that the Up to Speed signal is generated, the 10 second delay circuit is started. When this circuit times out, the Up To Speed Delayed signal is generated and initiates the load heads function assuming there are no voltage faults (refer to emergency retract discussion). The heads load function causes the heads to move, from their retracted (unloaded) position, over the disk surface. The discussions on electromechanical functions and seek functions provide a more detailed description of what happens during this function. The heads load function is enabled when the output of the summing amplifier is connected to the power amplifier. This causes a current to flow in the voice coil and the carriage and coil assembly are driven forward, loading the heads on the disk surface. The enable which allows this function to happen, occurs when the load latch is set and the Tracks Equal To Or Less Than 7 signal is present.



NOTES: 1. SWITCHES AND TRIACS ARE DRAWN AS THEY MUST EXIST AT BEGINNING OF POWER ON SEQUENCE.

2. NUMBERS IN PARENTHESIS ARE CROSS REFERENCE NUMBERS OF LOGIC DIAGRAMS.

Figure 3-4. Power On Sequence - Simplified Logic

POWER OFF SEQUENCE

The power off sequence is that chain of events which unloads the heads and stops the drive motor. The power off sequence is essentially the reverse of the power on sequence. Refer to figure 3-4.

The sequence begins when either the START switch is pressed or the controller disables the power sequencing signals. In either case the Start signal is no longer present and the Load latch is reset. This also sets the Return To Zero latch and causes the heads to start to retract. The carriage performs a normal Return To Zero seek, except that the logic that normally stops the carriage at cylinder 000 is inhibited so that the heads retract completely.

With the heads unloaded there is no longer a signal available to keep transistor Q4 on, therefore the Run triac is disabled. This removes the ac power to the drive motor and causes the disks to start slowing down.

At the same time transistor Q10 is turned on, connecting the plus 20 volts to the hystersis brake coil. Since the heads have unloaded, there is once again a ground path through the heads loaded switch. With the brake thusly enabled, the disks stop in approximately 30 seconds.

EMERGENCY RETRACT

The emergency retract function provides a means of retracting the heads from the pack area whenever an unsafe condition exists. Emergency retract power is applied to the voice coil through the normally closed contacts or the retract relay A1K2. This relay is picked during the power on sequence in order to enable the voice coil drive to the voice coil. Figure 3-5 shows the emergency retract circuits.

During the normal functioning of the drive, relay A1K2 is picked. This happens when transistor A2A10Q9 is turned on allowing a path to ground. The transistor is turned on when the following signals are true: (1) Not Voltage Fault, (2) Up To Speed, and (3) Not Power Up Master Clear. Therefore, during the initial power on sequence, the transistor is turned off until the drive gets Up To Speed. At this time, assuming there are no voltage faults, the transistor turns on, connecting the relay coil to ground and the relay picks. This transfers the relay contacts and the voice coil drive enables the heads load sequence.

The emergency retract relay stays in the picked condition until the logic senses a voltage fault or a not up to speed condition. Either of these conditions turns off tran-

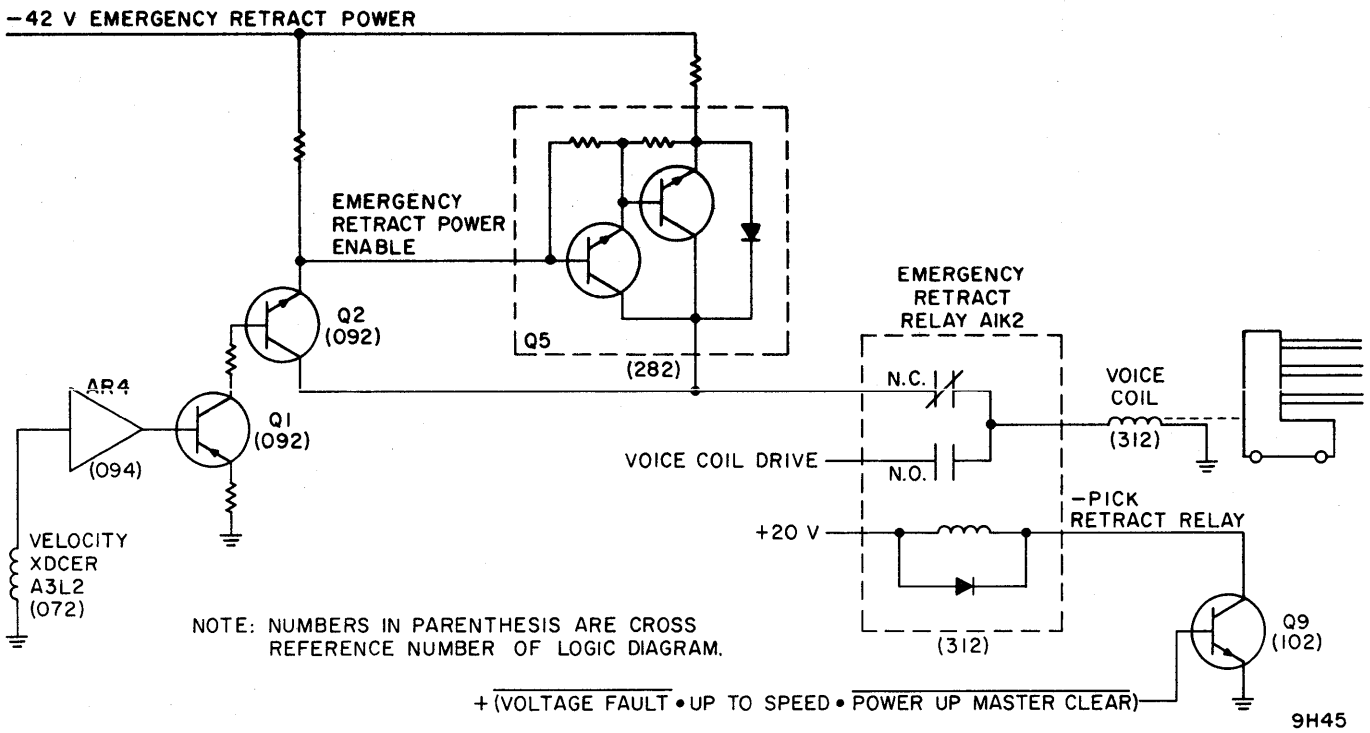


Figure 3-5. Emergency Retract Circuits

sistor A2A10Q9 and the emergency retract relay returns to its normally closed position. This connects the minus 42 volt emergency retract power to the voice coil and the heads retract.

The darlington power transistors A3A04Q5 is forward biased and therefore turned on at the beginning of the emergency retract sequence. However, in order to control the velocity of the emergency retract, the velocity transducer signal is amplified and used to turn off the transistor as the velocity increases. This prevents the carriage from slamming into the reverse stop during an emergency retract situation.

ELECTROMECHANICAL FUNCTIONS

GENERAL

Certain drive functions are a result of the electromechanical devices working under the control of logical circuitry. These functions include disk pack rotation, head positioning, and drive cooling and ventilation.

Disk pack rotation is performed by the disk pack rotation mechanism, which is controlled by the power system. The purpose of disk pack rotation is to create a cushion of air on the disk surfaces. The cushion of air allows the heads (which read and write the data) to move over the disk surfaces without actually contacting them.

The heads are positioned over specific data tracks on the disk surface by the head positioning mechanism. The mechanism is controlled by the servo circuits (refer to discussion of Seek Operations) and the power system.

Drive cooling and ventilation is provided by the air flow system. The main element in this system is the blower motor which receives its power from the power system.

Figure 3-6 is a block diagram showing each of the previously discussed mechanisms. A more detailed physical and functional description of each is provided in the following discussions.

DISK PACK ROTATION

General

The disk pack must be rotating fast enough to allow the heads to fly before any drive operation can be performed. The following mechanisms work in conjunction with the power system to control disk pack rotation (refer to figure 3-7):

- Drive Motor - Provides rotating motion for the spindle and disk pack.
- Spindle - Provides rotating mounting surface for disk pack.

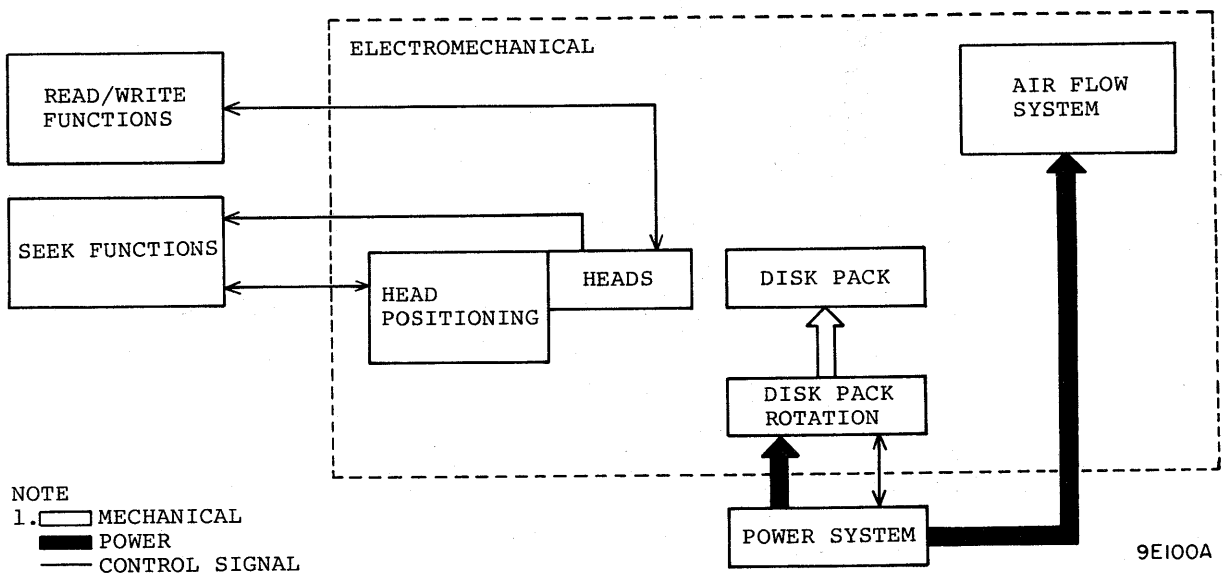


Figure 3-6. Electromechanical Functions - Diagram Block

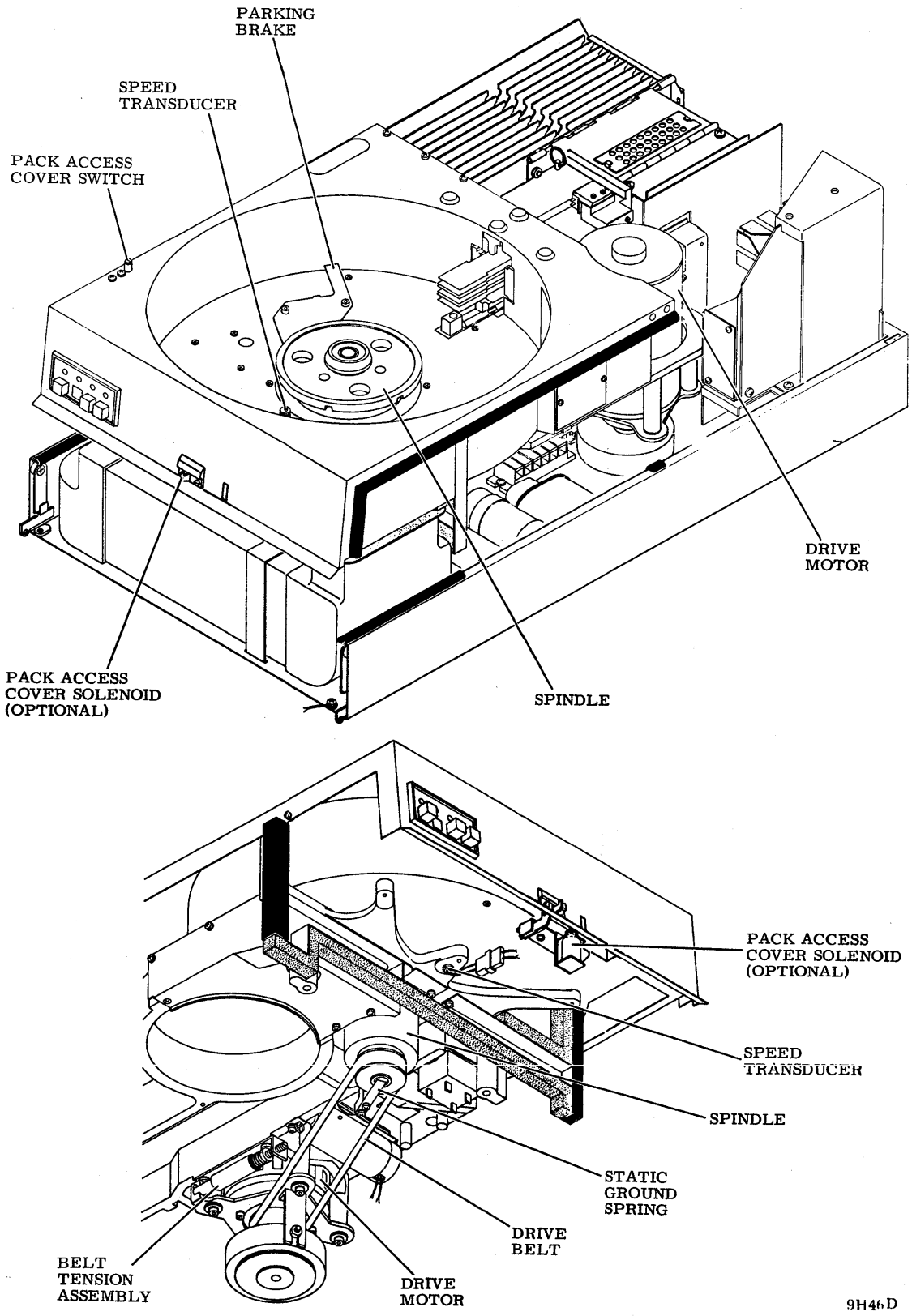


Figure 3-7. Disk Pack Rotation Mechanisms

- Parking Brake - Holds spindle while pack is being installed.
- Speed Transducer - Generates pulses that are used to determine speed of spindle.
- Pack Access Cover Switch - Ensures that pack access cover is closed before disk pack rotation begins.
- Pack Access Cover Solenoid - (Optional) Prevents pack access cover from being opened while pack is rotating.

These mechanisms are further described in the following paragraphs.

Drive Motor

The drive motor provides the rotational energy required to rotate the spindle and disk pack. The motor is mounted on the under side of the deck casting.

Motion is transferred from motor to spindle via the drive belt. This belt connects the pulley on the shaft of the drive motor to the pulley on the lower end of the spindle.

The spring in the belt tension assembly maintains enough tension on the plate to keep the drive belt tight. The spring tension is adjustable so tension on the belt can be adjusted to provide the best coupling between drive motor and spindle pulleys.

The motor starts during the power on sequence when power is applied to its start and run windings (refer to Power On Sequence discussion). The start winding helps the run winding start the motor in motion and get it up to speed. After nine seconds the start winding is no longer needed, and is disabled by the logic. The motor continues to accelerate, using only its run winding, until it reaches it maximum speed (approximately 3600 r/min). This speed is maintained until power is removed from the motors run winding.

The temperature of the drive motor is monitored by its internal thermal switch. If the motor overheats, this switch opens (pops up) resulting in loss of power to the drive motor. The motor slows down causing an emergency retract and power off sequence. The drive motor cannot be restarted until it cools off and the thermal switch is reset (by pressing it in).

Spindle

The spindle provides the means of mounting the disk pack within the drive and also of rotating the pack when the drive motor is energized.

When the pack is mounted, its lower guard disk rests on the pack mounting plate. This plate connects to a shaft which in turn connects to the pulley on the lower end of the spindle. When the drive motor starts, it transfers motion to this pulley via the drive belt and causes the pack mounting plate and disk pack to rotate.

The disk pack must be secured to the mounting plate with enough force so the two of them will rotate together. This force is provided by the lockshaft, which is a spring loaded shaft located within the spindle. When the pack is installed, the mounting screw on the bottom of the pack is threaded into the internal threads in the upper end of the lockshaft. As the pack is tightened down against the mounting plate, the springs holding the lockshaft exert a downward force on the pack. When this force is sufficient, a release mechanism (in the handle of the disk pack storage cannister) releases the cannister from the pack. The pack is now installed and will rotate whenever the drive motor is energized.

The ground spring bleeds off any static electricity accumlating on the spindle.

Parking Brake

The parking brake holds the spindle stationary whenever a disk pack is installed or removed. It is actuated by the disk pack storage cannister which contacts the spindle brake lock arm. This causes the brake tooth to move up and engage a slot in the bottom of the spindle thus preventing the spindle from rotating. When the cannister is removed, the arm is released, the brake tooth disengages, and the spindle is free to turn.

Speed Transducer

The speed transducer is a device that generates signals used to determine if spindle speed is sufficient to allow the heads to fly. The transducer is mounted beneath the spindle and consists of a small coil and core assembly. The transducer acts as a magnetic pick up, generating a pulse each time it senses a magnetic flux change. Since there are two magnetic slugs imbedded in the bottom plate assembly of the disk pack (at 180 intervals), two pulses are generated for each revolution of the pack.

The speed logic monitors these signals and uses them to determine if spindle speed is at least 3000 r/min. When this speed is reached, the Speed Pulse Interval Detector can no longer time out and the Up To Speed signal is generated. It is this signal which allows the Emergency Retract Relay to

pick and the heads to load. As long as the drive remains up to speed, the Emergency Retract Relay remains picked allowing the power amplifier to control the carriage position.

Pack Access Cover Switch

The pack access cover switch must be closed for the drive motor to start. The switch is in series with the START switch, and therefore only allows the Start signal through when the pack access cover is closed.

Pack Access Cover Solenoid (Optional)

If the drive is equipped with a pack access cover solenoid, the pack cover can be opened only if the dc power is on and the disk pack is not rotating. The solenoid controls the operation of the pack access cover as follows:

When the drive is in a power on condition and the Start and Speed Pulses Present signals are not true, the solenoid is energized. With the solenoid energized the interlock latch is pulled down and the pack access cover can be opened.

If dc power is removed from the drive, or if the Start or Speed Pulses Present signals are true, the solenoid is deenergized. The interlock latch is then in the up position which prevents the pack access cover from being opened.

HEAD POSITIONING

General

Data is read from and written on the disk by the heads. However, the drive must position the heads over a specific track on the disk pack before a read or write operation can be performed. Head positioning is performed by the actuator, under control of the signals received from the servo circuits (refer to discussion on Seek Functions).

The actuator is mounted at the rear of the deck assembly in a position so that the heads (when extended) are driven into the pack area within the shroud and out over the disk pack. The actuator (see figure 3-8) is made up of the rail bracket, carriage and coil, and magnet assemblies.

Actuator Physical Description

The carriage is the moveable portion of the assembly. It has the heads mounted on the front portion and the coil is attached to the rear. The carriage bearings ride on the upper and lower rails. The upper rail is attached to the rail bracket which is in turn attached to the deck casting. The lower rail is attached directly to the deck casting. In order to achieve accurate positioning, a precise alignment exists between the rails, rail bracket and deck castings.

Two cam towers, mounted on the front of the rail bracket, support the heads when they are in their retracted position. As the carriage moves forward during the heads load sequence, the heads ride down the ramps on the cam towers and are loaded onto the disk surface.

In addition to the upper rail and cam towers, the rail bracket also provides mounting for the upper stop block, heads loaded switch, and the flex lead assembly. The upper stop block, in conjunction with the lower stop block which is mounted on the deck, provide an absolute stop to prevent the carriage from being driven too far forward. The heads loaded switch provides a signal to the logic to indicate when the heads are loaded. The switch opens when the heads are extended (loaded). The flex lead assembly provides a means of applying voice coil drive power to the moving voice coil. The flex lead assembly consists of two flat flexible conductors and their associated insulating strips.

The magnet assembly provides a cutout area which allows the coil to move in and out of the magnet in response to the servo signals. The magnet also houses the velocity transducer. The transducer consists of a coil and a core. The transducer coil extends through the center of the magnet assembly and remains in a fixed position. The core is attached to the rear of the carriage, inside the voice coil, and moves with the carriage. The velocity transducer provides an output signal which has amplitude and polarity directly proportional to the rate and direction of the carriage movement.

Actuator Functional Description

The movement of the carriage and voice coil (and therefore the heads) is controlled by the positioning signals from the servo logic. The positioning signals are derived in the seek logic and processed by the power amplifier. The output of the power amplifier is a current signal which is applied to the voice coil through the flex lead assembly.

The current from the power amplifier causes a magnetic field around the voice coil which reacts with the permanent magnetic field around the magnet. This reaction either draws the voice coil into the magnetic field or forces it away, depending on the polarity of the current through the voice coil. The acceleration of the voice coil is dependent on the amplitude of the voice coil current.

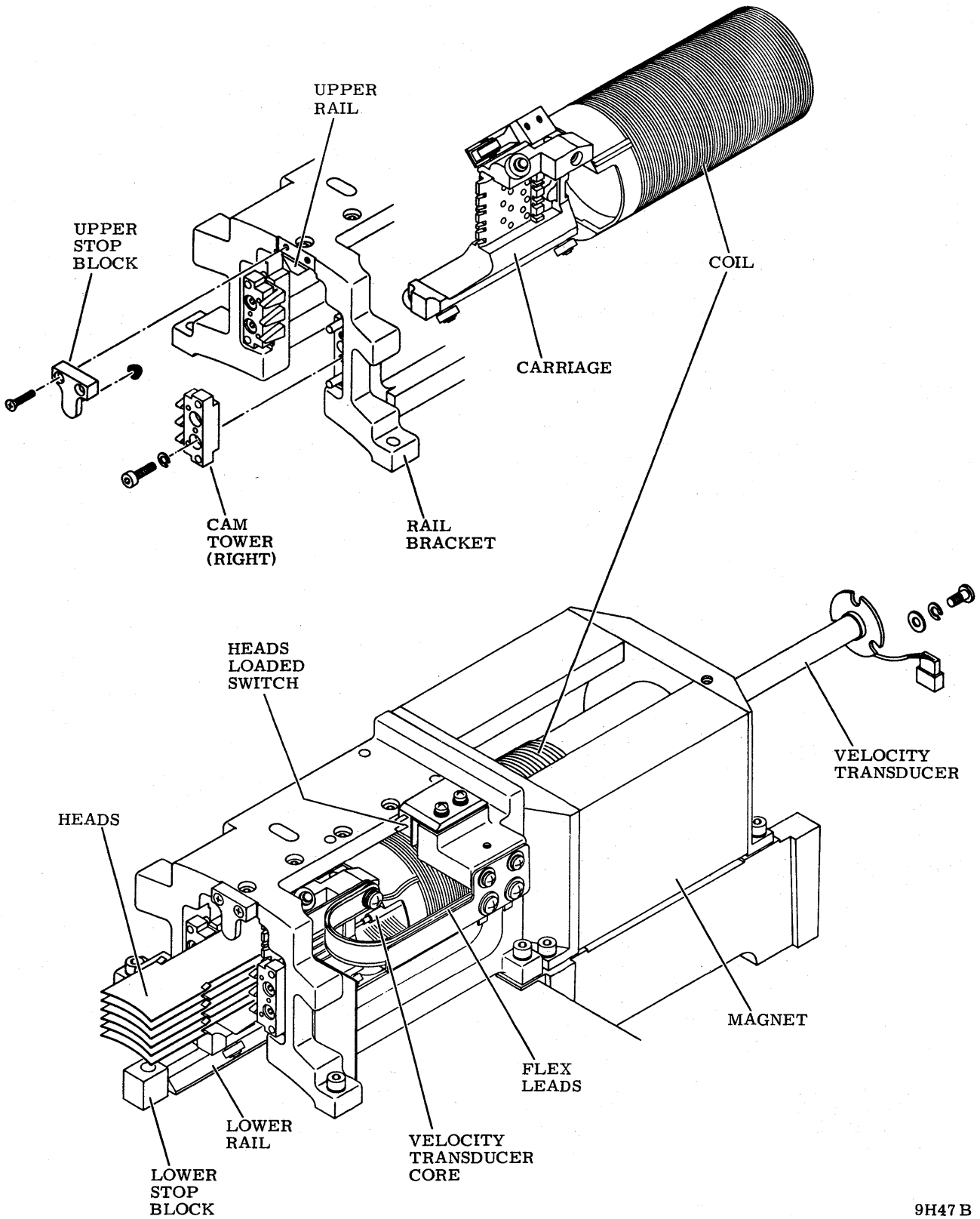


Figure 3-8. Actuator Components

Head Description

General

The heads are electromagnetic devices that record data on and read it from the disk pack. They are mounted in the end of a supporting arm; the head and arm together are called a head-arm assembly. The head-arm assemblies attach to the carriage.

The drive has 6 heads, one for each disk surface. There are two types of heads (1) read/write and (2) servo. There are 5 read/write heads which are used to record data on and read it from the data surface. There is one servo head which is used to read position information from the servo surface. This information is used by the drives servo circuits.

The following describes the physical characteristics of the head-arm assemblies and also how they function during head load and unload sequences. Further information concerning the heads is found in the discussions on head positioning, read/write, and seek functions.

Head-Arm Assemblies

Each head-arm assembly consists of a rigid arm, heads load spring, gimbal spring, and the head (refer to figure 3-9).

The rigid arm is mounted on the carriage and causes carriage motion to be transmitted to the head. However, the arm does not provide the action necessary for the head to load, unload and follow the disk surface. This action is provided by the head load and gimbal springs.

The head load spring attaches to the rigid arm and is the mounting point for the gimbal spring. The head in turn attaches to the gimbal spring.

During head loading and unloading, the head load springs ride on the cam tower ramps and keep the heads from contacting one another. When the heads are loaded, the head load and gimbal springs work together and allow the heads to move independently of the rigid arms in the direction shown in figure 3-9. Such motion is necessary because when the heads are over the disk surfaces they do not

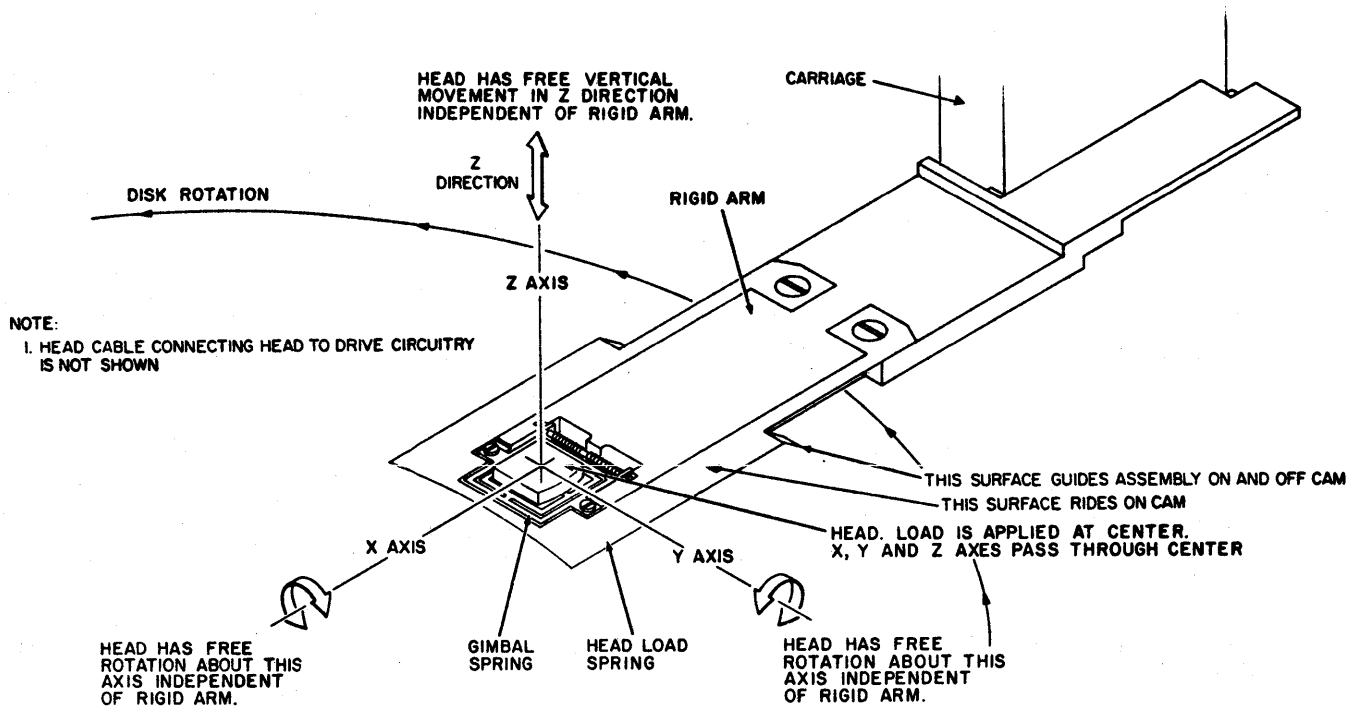


Figure 3-9. Head-Arm Assembly

contact the disk but actually fly on a cushion of air created by the spinning of the disk pack.

Information is sent to and from the heads via the head-arm cables. One end of each cable connects to a head and the other end has a plug which connects to the head select/read amplifier card.

Head Loading

The heads must be loaded before the heads can be positioned to a data track for the recording and reading of data. Loading the heads consists of moving them forward from their retracted (unloaded) positions until they are over the disk surfaces. All heads are loaded simultaneously.

The load sequence is initiated during the power up sequence when the disk pack has reached 3000 r/min. At this speed the spinning disk creates a sufficient cushion of air to allow the heads to fly.

When the pack is upt to speed and the load logic is enabled, the heads move forward with the head load springs riding on the cam tower ramps. As the heads move out over the disk surfaces, the head load springs ride off the surfaces of the cam tower ramps (refer to figure 3-10).

The load springs, while riding off the ramps, unflex and force the heads toward the air cushions on the spinning disk surfaces. When the cushions of air are encountered, they resist any further approach by the heads. However, the head load springs continue to force the heads down until the opposing air and spring pressures are equal.

The air cushion pressure varies directly with disk speed and if the disk pack is rotating at the proper speed, the air and spring pressures should be equal when the heads are flying at the correct height above the disks.

If the disk pack drops below this speed, air cushion pressure decreases and the head load springs force the heads closer to the disks. Sufficient loss of speed causes the heads to stop flying and contact the disk surfaces. This is called head crash and can cause damage to both the head and disk surfaces.

Because insufficient disk speed causes head crash, loading occurs only after the disk pack is up to speed. For the same reason, the heads unload automatically if disk pack speed drops below a safe operating level (refer to discussion on emergency retract).

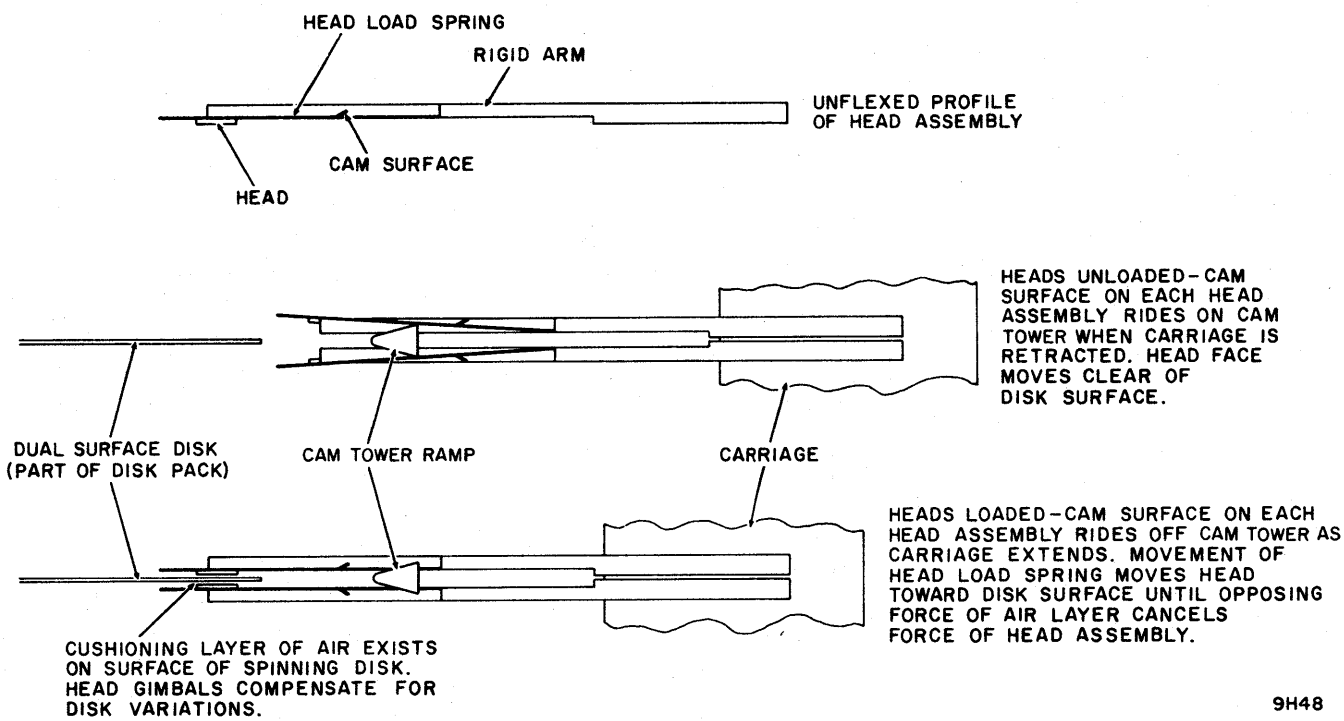


Figure 3-10. Head Loading

Head Unloading

The heads must be unloaded whenever the pack is stopped or if it is spinning too slowly to fly the heads. Unloading consists of retracting the heads until they are no longer over the disk surfaces.

The unload sequence is initiated either during a normal power off sequence, or during an emergency retract function. In both cases current is applied to the voice coil that causes the carriage to move back towards the retracted stop.

As the carriage retracts, the head load springs encounter the cam tower ramps and the heads are pulled away from the disk surfaces. The carriage continues to move back until it is fully retracted.

AIR FLOW SYSTEM

The air flow system provides cooling for the electronic components in the drive and a supply of clean air into the pack area to ensure cleanliness. The air flow system includes the blower assembly, primary filter, and absolute filter.

Air is initially drawn in through the primary filter which removes most of the particles from the air. The primary filter is located in the front of the case assembly on all mounting configurations except the acoustic. The primary filter in the acoustic cabinet is located in the front of the cabinet base, facing the floor.

On all drives, the air is drawn into the machine by the blower assembly. The blower motor provides the force to pull the air in and then push it through the machine. A port in the rear of the blower housing vents air into the read/write cards on the back of the shroud and through the logic chassis.

The other outlet from the blower housing vents air through the absolute filter, which removes all particles which might cause damage to the heads or disks. The air is then blown into the pack area, across the turning disks, and out through the heads and actuator mechanism. Since the air is forces into the pack area, a positive pressure is created which prevents contaminated air from entering around the pack access cover. Air coming out of the pack area through the actuator also vents across the power amplifier and power supply.

INTERFACE FUNCTIONS

GENERAL

All communications between drive and controller must pass through the interface. This communication includes all commands, status, control signals and read/write data transmitted and received by the drive.

The drive comes from the factory as either a single or dual channel unit (refer to discussion on equipment configuration in section 1 of this manual). The single channel units can connect to and communicate with one controller. The dual channel units can connect to and communicate with two controllers.

The interface, in both cases, consists of the I/O cables and the logic required to carry and process the signals sent between drive and controller (or controllers).

The following describes both the I/O cables and I/O signal processing.

I/O CABLES

All the signal lines between the drive and controller are contained in two flat ribbon type I/O cables. They are referred to as the A and B cables. In the case of dual channel units the drive has separate cables to each controller.

The A cable contains lines connected in twisted pairs, which carry commands and control information to the drive and status information to the controller. Maximum number of pins and signals depends on unit type (refer to discussion on equipment configuration in section 1 of this manual).

Figure 3-11 shows all lines in the A and B cables. The functions of each of these lines is explained in tables 3-1 and 3-2.

I/O SIGNAL PROCESSING

I/O signals from the controller initiate and control all drive operations except power on. The I/O signals are sent to receivers in the drive and are routed from the receivers to the appropriate drive logic. The drive in turn sends information, concerning the operation back to the controller via the transmitters. Dual channel units have separate receivers and transmitters for each controller. Figure 3-12 shows the basic logic involved in the routing of I/O signals.

Certain I/O signals cannot be transmitted or received unless the drive is selected. These signals are shown in figure 3-12 and include the tag and bus bit signals

All commands (except unit select) are sent to the drive via the tag and bus bit lines. These lines work in conjunction with the tags defining the basic operation to be performed and the bus bits further defining the basic operation. Table 3-1 explains the function off all tag and bus lines.

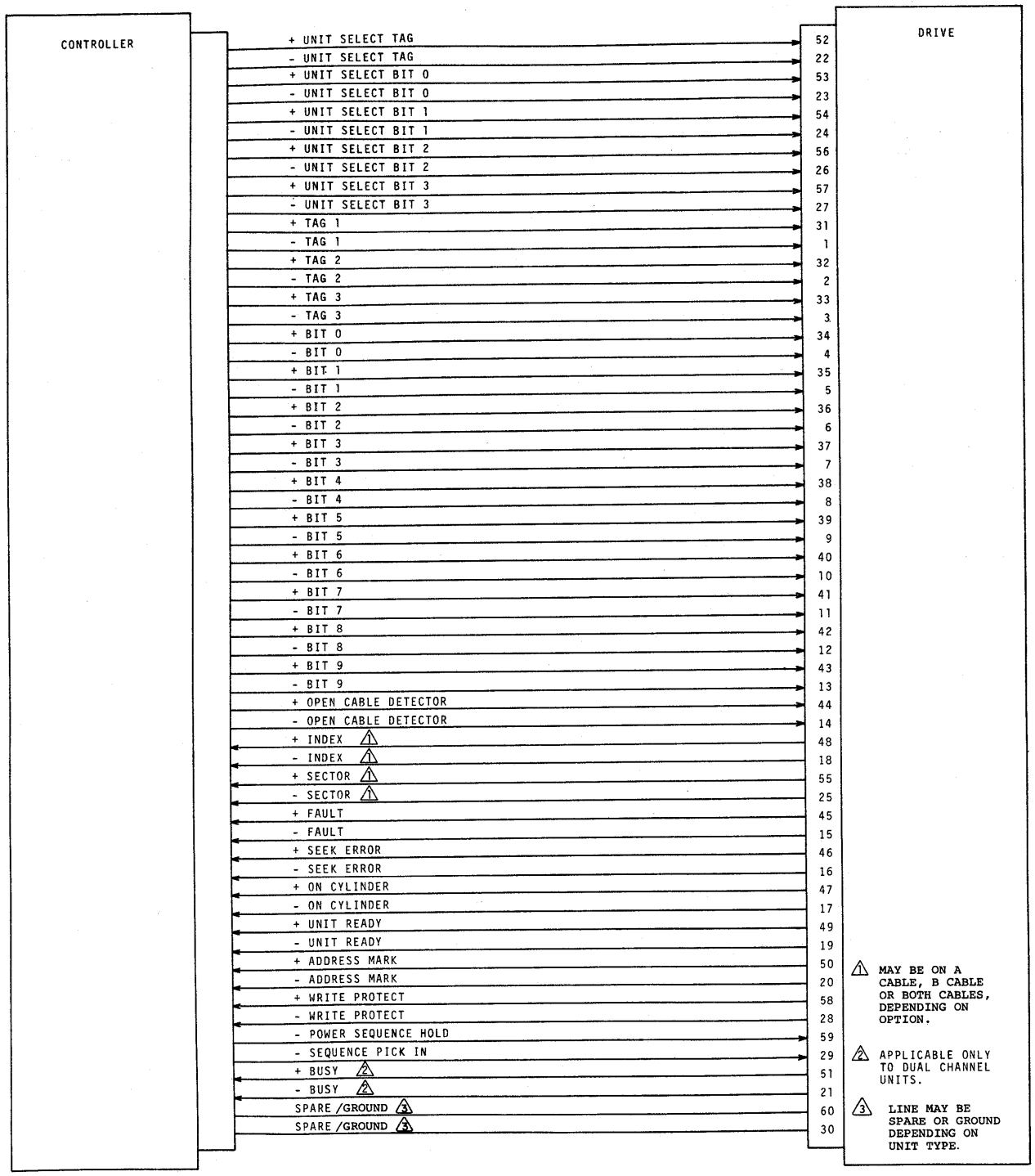


Figure 3-11. I/O Cables (Sheet 1 of 3)

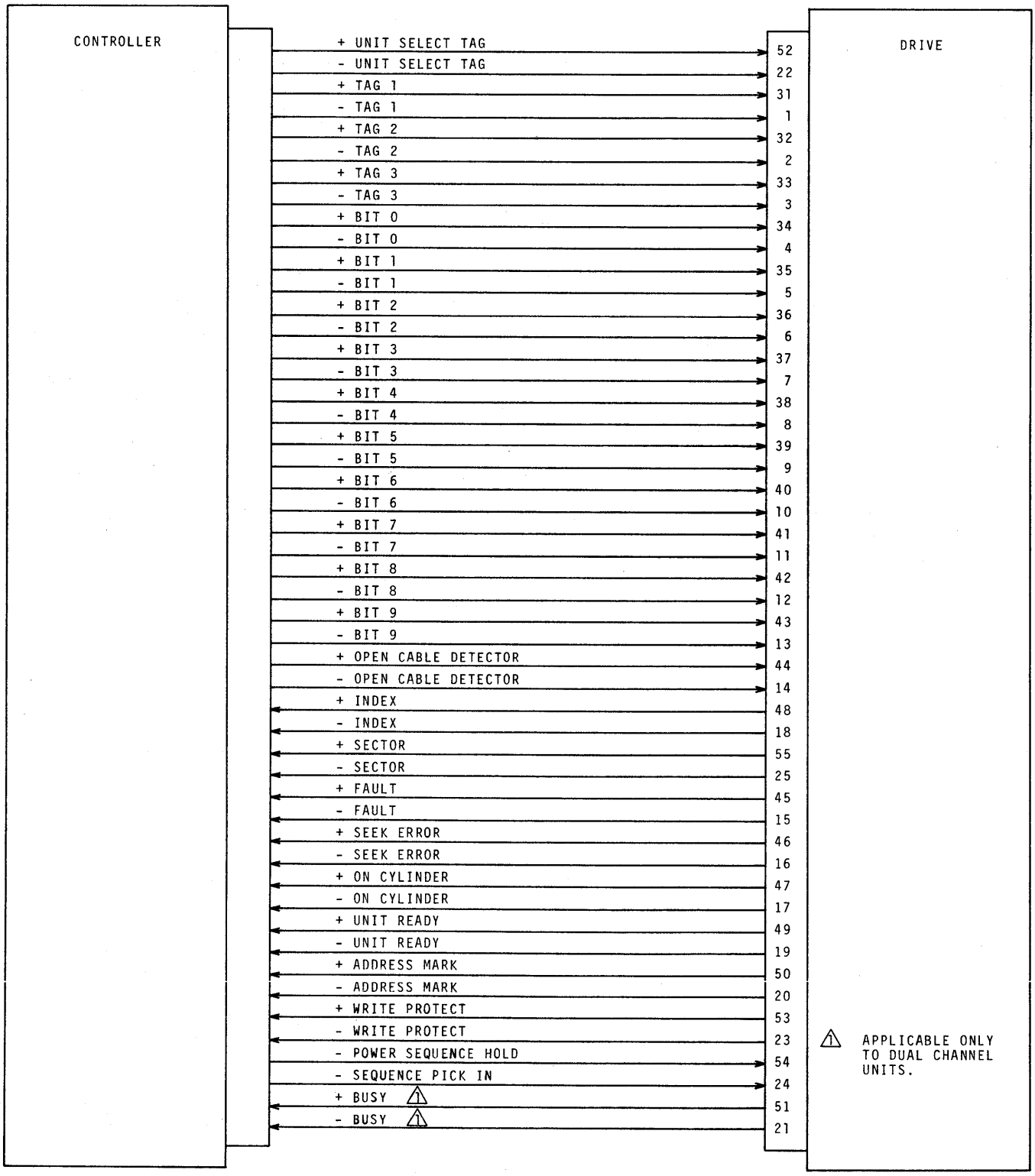


Figure 3-11. I/O Cables (Sheet 2 of 3)

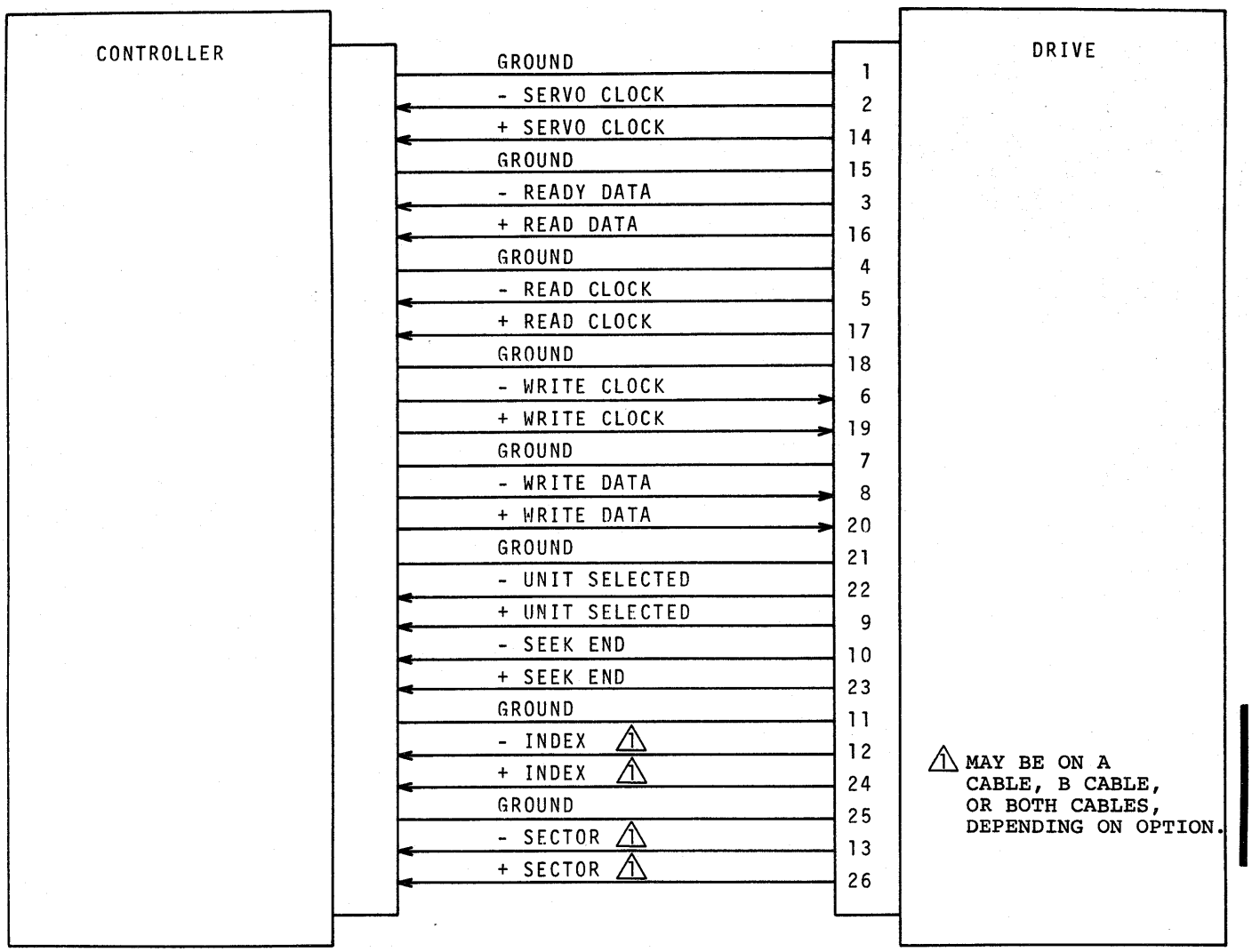


Figure 3-11. I/O Cables (Sheet 3 of 3)

TABLE 3-1. CONTROLLER TO DRIVE SIGNAL LINE FUNCTIONS

<table>
<tr><th>Signal</th><th>Function</th></tr>
<tr><td>Sequence Pick In</td><td>Used for power sequencing. A ground on this line powers up drive if LOCAL/REMOTE switch is in REMOTE and START switch is on (refer to discussion on Power Sequencing).</td></tr>
<tr><td>Power Sequence Hold</td><td>Used for power sequencing. This line must be grounded at controller for drive to complete and hold remote power up sequence (refer to discussion on Power Sequencing).</td></tr>
<tr><td>Open Cable Detect</td><td>Inhibits Unit Selection and any unwanted command such as Write Gate when "A" cable is disconnected or controller power is lost.</td></tr>
<tr><td>Unit Select Tag</td><td>Works in conjunction with either the Unit Select Bits (60 pin I/O) or the Bus Bits (50 pin I/O) to initiate a unit select sequence. In dual channel drives, a Unit Select Tag also reserves drive to the issuing controller, provided unit selection is successful. On both 50 and 60 pin I/O, dual channel drives, the Unit Select Tag in conjunction with Bus Bit 9 initiates a Priority Select function. Refer to Unit Selection discussion for greater detail.</td></tr>
<tr><td>Unit Select
Bits 0 thru 3
(Not applicable to units with 50 pin I/O)</td><td>Used to select the drive. The binary code on these lines must match the code of the drives logical address plug for the drive to be selected. These lines are used in conjunction with the Unit Select Tag (refer to discussion on Unit Selection).</td></tr>
<tr><td>Tag 1 (Cylinder Select)</td><td>Used in conjunction with Bus Bit lines to initiate seek function. This tag strobes the cylinder address, contained in Bus Bit lines, into drive logic. Drive must be on cylinder before this tag is sent. Bus Bits are interpreted as follows:
<table>
<tr><th>Bus Bit</th><th>Function</th><th>Bus Bit</th><th>Function</th></tr>
<tr><td>0</td><td>Cyl Adrs Bit 0</td><td>5</td><td>Cyl Adrs Bit 5</td></tr>
<tr><td>1</td><td>Cyl Adrs Bit 1</td><td>6</td><td>Cyl Adrs Bit 6</td></tr>
<tr><td>2</td><td>Cyl Adrs Bit 2</td><td>7</td><td>Cyl Adrs Bit 7</td></tr>
<tr><td>3</td><td>Cyl Adrs Bit 3</td><td>8</td><td>Cyl Adrs Bit 8</td></tr>
<tr><td>4</td><td>Cyl Adrs Bit 4</td><td>9</td><td>Cyl Adrs Bit 9</td></tr>
</table></td></tr>
<tr><td>Tag 2 (Head Select)</td><td>Used in conjunction with Bus Bit lines to initiate head select function. This tag strobes the head address, contained on Bus Bit lines, into drive logic. Bus Bits are interpreted as follows:
<table>
<tr><th>Bus Bit</th><th>Function</th></tr>
<tr><td>0</td><td>Head Adrs Bit 0</td></tr>
<tr><td>1</td><td>Head Adrs Bit 1</td></tr>
<tr><td>2</td><td>Head Adrs Bit 2</td></tr>
<tr><td>3 - 9</td><td>Not Used</td></tr>
</table></td></tr>
</table>

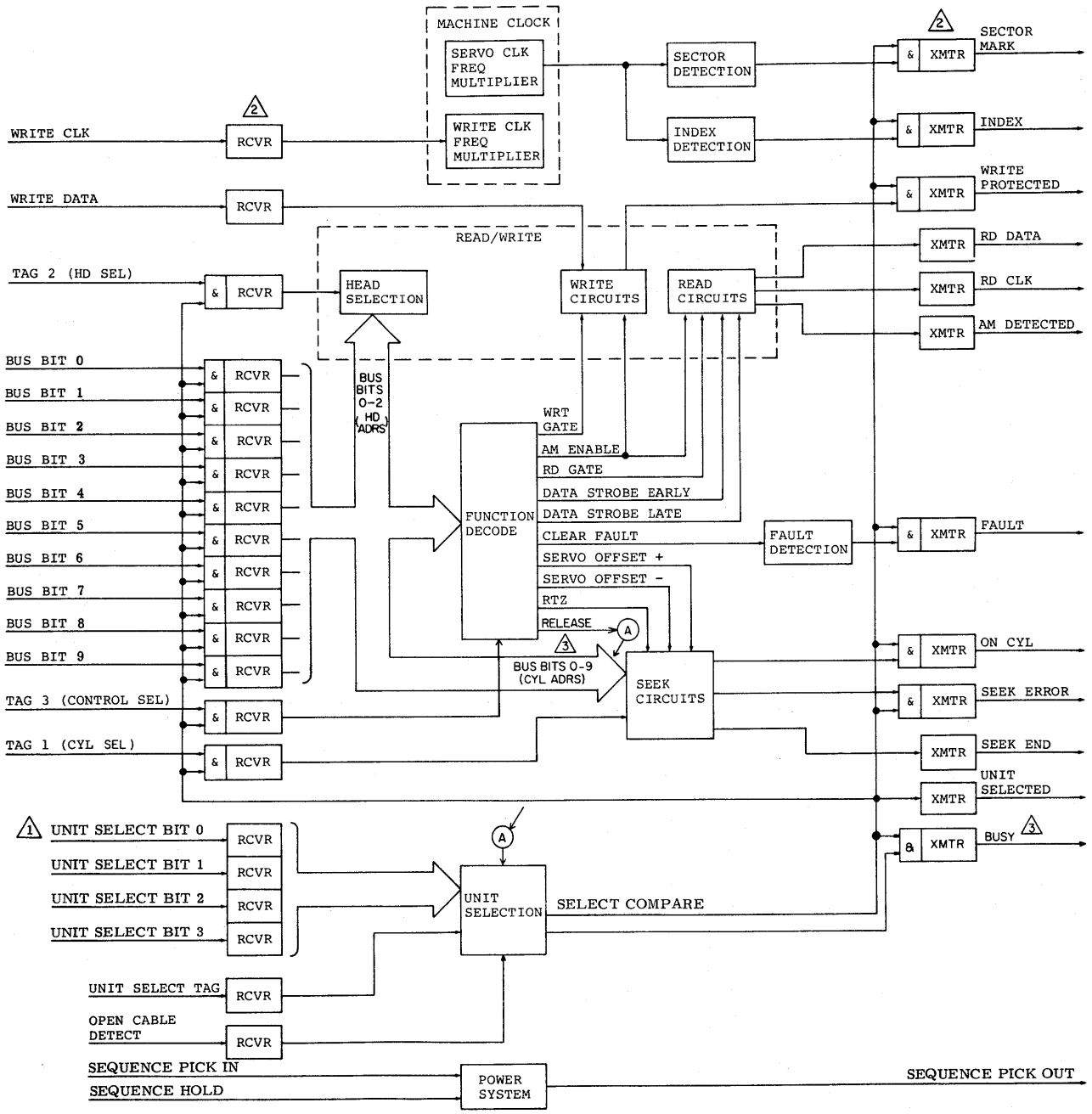
Table continued on next page

TABLE 3-1. CONTROLLER TO DRIVE SIGNAL LINE FUNCTIONS (Contd)

Signal	Function
Tag 3 (Control Select)	Initiates various operations to be performed by the drive. Used in conjunction with Bus Bit lines, which operation is initiated depends on content of these lines which are defined as follows: Bus Bit — Function 0 — Write Gate - Enables write drivers. 1 — Read Gate - Enables the digital read data lines. Leading edge triggers read chain to sync on all-zeros pattern. 2 — Servo Offset Positive - Offsets the actuator from the nominal on cylinder position toward the spindle. 3 — Servo Offset Negative - Offsets the actuator from the nominal on cylinder position away from the spindle. 4 — Controller Fault Clear - A 100 ns (minimum) pulse sent to drive. Clears the Fault Latch if fault condition no longer exists. 5 — Address Mark Enable - When combined with a Write Gate, Address Mark is written. When combined with a Read Gate, an Address Mark search is initiated. 6 — RTZ Seek - A pulse (250 ns to 1.0 µs wide) sent to drive to cause actuator to seek to track zero, clear head address register, and clear seek error latch. 7 — Data Strobe Early - Enables the PLO data separator to strobe the data at a time earlier than optimum. 8 — Data Strobe Late - Enables the PLO data separator to strobe the data at a time later than optimum. 9 — Release - Applicable only to dual channel units, this line resets the Reserved and Disable flip-flops for both channels thereby releasing both the Reserve and Priority Select commands.
Bus Bits (0 - 9)	Used in conjunction with Unit Select Tag and Tags 1, 2 and 3 to define commands to the drive.
Write Data	Carries NRZ data to be recorded on disk pack.
Write Clock	Synchronized to NRZ Write Data, it is a return of the Servo Clock. This signal is transmitted continuously.

TABLE 3-2. DRIVE TO CONTROLLER SIGNAL LINE FUNCTIONS

Signal Line	Function
Unit Ready	Indicates that drive is selected, up to speed, heads are loaded and no fault exists.
Busy (applicable only to dual channel units.)	Enabled when a unit selection is attempted but the drive is already reserved by the other controller. This signal is returned, to the controller attempting selection, along with the unit selected signal (refer to discussion on Unit Selection).
On Cylinder	Indicates drive has positioned the heads over a track (refer to discussion on Seek Functions).
Seek Error	Indicates that the unit was unable to complete a move within 500 ms, or that carriage has moved to a position outside recording field. A seek error interrupt also occurs if an address greater than track 410 (40 MB) or 822 (80 MB) has been selected. Refer to discussion on Seek Functions for more information.
Index	Occurs once per revolution of disk pack and its leading edge is considered leading edge of sector zero (refer to discussion on Index Detection).
Sector	Derived from servo surface of disk pack, this signal can occur any number of times per revolution of disk pack. Number of sector pulses occurring depends on setting of switches on card in position B08 in logic chassis (refer to discussion on Sector Detection).
Address Mark Found	Indicates that an Address Mark has been found. Enabled by a combination of Read Gate and Address Mark Enable (refer to discussion on Lock to Data and Address Mark Detect Circuits).
Write Protect	Indicates that drives write circuits are disabled. Is true under following conditions: • Head alignment is being performed • Fault condition exists • Write Protect switch on operator panel is activated
Fault	Indicates that one or more of these faults exist: DC power fault, head select fault, write fault, write or read while off cylinder, and Write Gate during a Read operation (refer to discussion on Fault and Error Detection).
Servo Clock	9.677 MHz clock signals derived from servo track dibits (refer to discussion on Machine Clock).
Read Data	Carries NRZ data recovered from disk pack (refer to discussions on Read/Write functions).
Read Clock	Clock signals derived from NRZ Read Data (refer to discussions on Read/Write functions).
Seek End	Seek End is a combination of ON CYL or SEEK ERROR indicating that a seek operation has terminated. If an address greater than cylinder 410 (40 MB) or 822 (80 MB) has been selected there will be no change in Seek End status (refer to discussions on Seek Functions). On dual channel units this line also carries a 27 µs pulse indicating one drive is available for selection (see discussion on Unit Selection).
Unit Selected	Indicates that the drive is selected. This line must be active before drive will respond to any commands from controller. However, on dual channel units, if Busy is returned in conjunction with Unit Selected, it indicates the drive is reversed to the other controller and selection was unsuccessful (refer to discussion on Unit Selection).



NOTES:

1. DRIVES WITH 50 PIN A CABLE I/O DO NOT HAVE UNIT SELECT LINES, THEY USE BUS BITS 0 THROUGH 3. FOR UNIT SELECTION
2. DUAL CHANNEL DRIVES HAVE A SET OF XMTRS AND RCVRS FOR EACH CONTROLLER
3. APPLICABLE ONLY TO DUAL CHANNEL UNITS

9H50A

Figure 3-12. I/O Signal Processing

UNIT SELECTION

GENERAL

The drive must be selected before it will respond to any commands from the controller. This is the case because the tag and bus bit receivers as well as certain transmitters are not enabled until the drive is selected (this is shown in figure 3-12).

In both single and dual channel units, the select sequence is initiated by a Unit Select Tag signal from the controller. However, the sequence performed is different depending on whether a single or dual channel is being considered. The reason for this is that the dual channel units must solve the problem of two controllers trying to select the drive when only one may have it selected at a time.

The following paragraphs describe both single and dual channel selection.

SINGLE CHANNEL UNIT SELECTION

The single channel unit select sequence (see figure 3-13) starts when the controller sends a Unit Select tag accompanied by a logical address either on the four Unit Select lines (in the case of drives with 60 pin I/O) or Bus Bits 0 through 4 (in the case of drives with 50 pin I/O).

When the drive recognizes the Unit Select tag it compares its own logical address (as indicated by the logical address plug) to the address sent by the controller. The drives logical address is determined by the logical address plug which fits into the control panel. Depending on the plug used, this address can be any number from 0 to 15. If no plug is used the number is 15.

If the address sent by the controller is the same as that of the drive, and the Open Cable Detect signal is active (indicating the A cable is connected and controller has power) the drive enables its Select Compare signal.

The Select Compare signal in turn enables the receivers and transmitters to the controller and also enables the Unit Selected signal. The drive is now ready to respond to further commands from the controller.

DUAL CHANNEL UNIT SELECTION

General

Dual channel drives are connected to, and can be selected by, either of two controllers. However, because the drive is capable of responding to only one controller at a time, the controller must compete for use of the drive. For this reason, there are functions associated with dual channel selection that are not necessary when selecting single channel units.

The functions controlling dual channel selection are as follows:

- Select - Logically connects the drive to the controller thus enabling it to respond to commands from the selecting controller.
- Reserve - Reserves the drive so it can be selected at any time by the reserving controller, but prevents it from being selected by the other controller.
- Release - Releases drive from reserved condition.
- Priority Select - Allows controller to force select the drive by disabling the interface to the controller having the drive selected or reserved.
- Maintenance Disable - Allows disabling either channel interface during maintenance.

The following discussions describe each of these functions. It should be noted that because these functions are basically the same regardless of which channel is involved, they are described only as they relate to channel I. Figure 3-14 shows the select logic associated with channel I selection and table 3-3 describes the major elements on this figure. Figure 3-15 is a flow chart of the dual channel unit select functions.

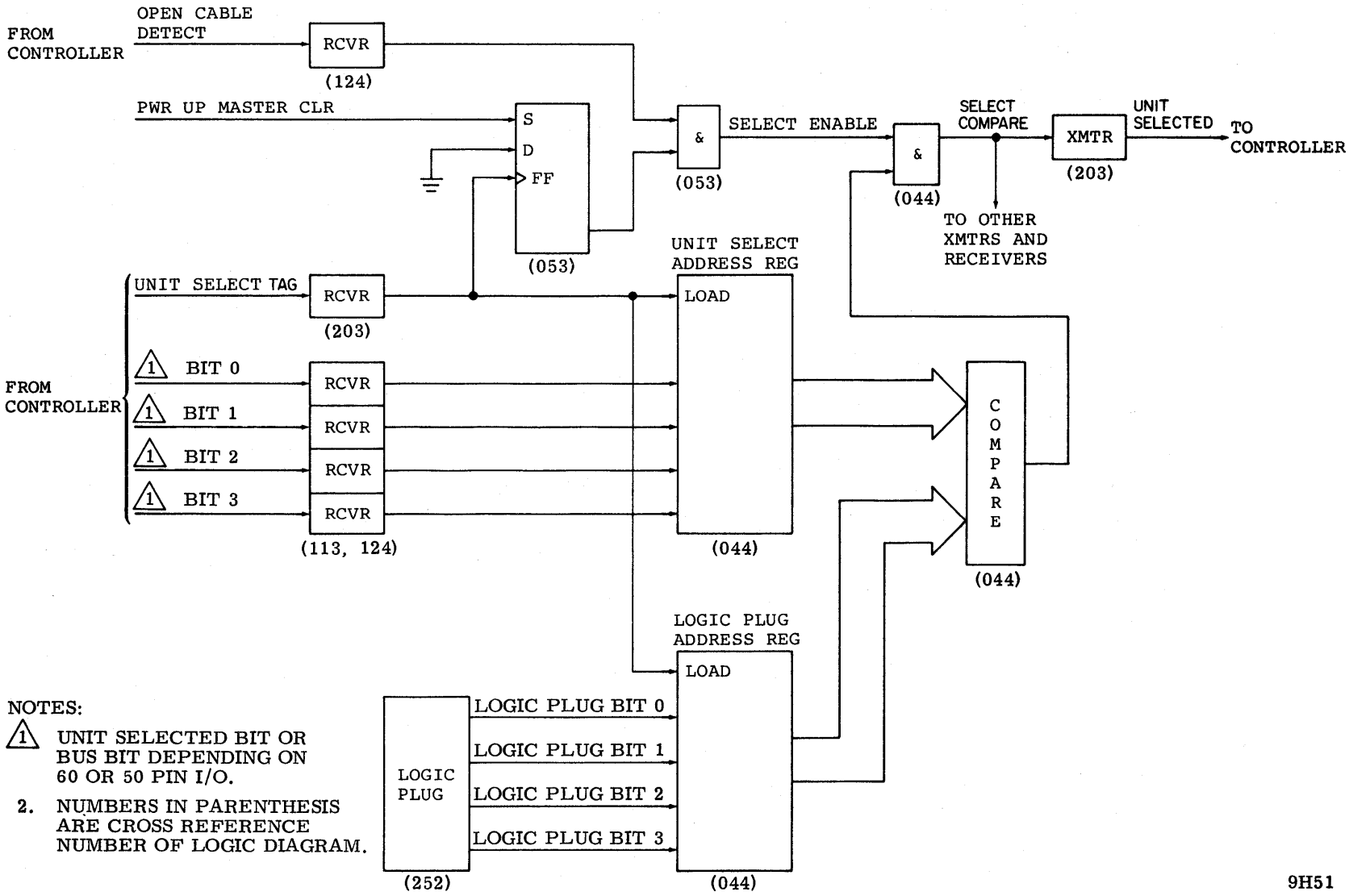
Select and Reserve Function

The drive is both selected and reserved during the same sequence and this sequence is initiated by a Unit Select Tag accompanied by a logical address. However, the drive can be successfully selected and reserved only if none of the following conditions exist:

- Drive is already selected and reserved by other controller.
- Drive is not selected but is reserved by other controller.
- Channel to drive attempting selection has been disabled by either a priority or maintenance disable function.

The following paragraphs describe how the drive is initially selected and also how it responds to a Unit Select Tag when it is selected, reserved, or disabled.

Assuming the drive is available (not selected, reserved or disabled) and it receives a Unit



NOTES:

1. UNIT SELECTED BIT OR BUS BIT DEPENDING ON 60 OR 50 PIN I/O.
2. NUMBERS IN PARENTHESIS ARE CROSS REFERENCE NUMBER OF LOGIC DIAGRAM.

Figure 3-13. Single Channel Unit Select Logic

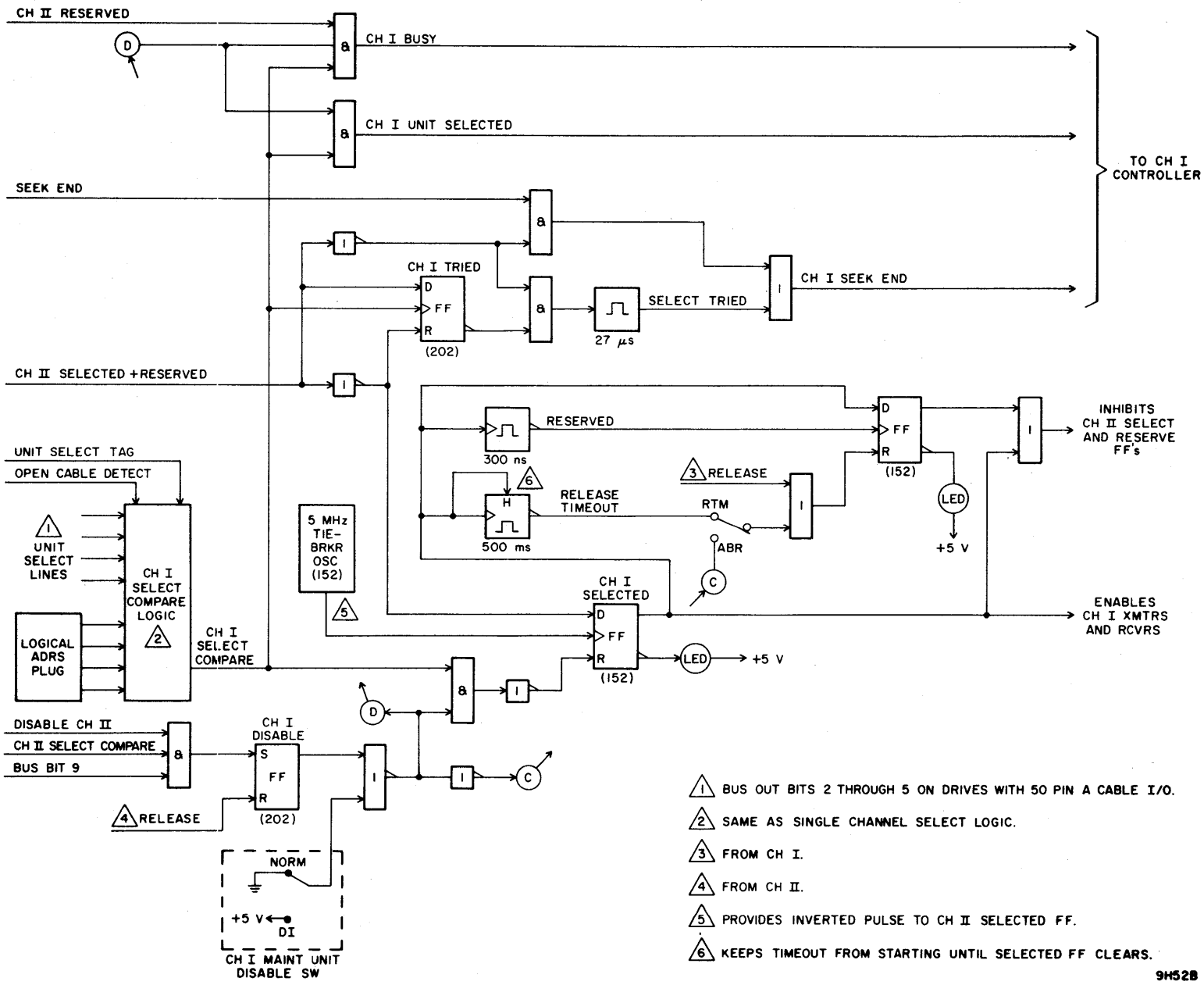


Figure 3-14. Channel I Dual Channel Select Logic

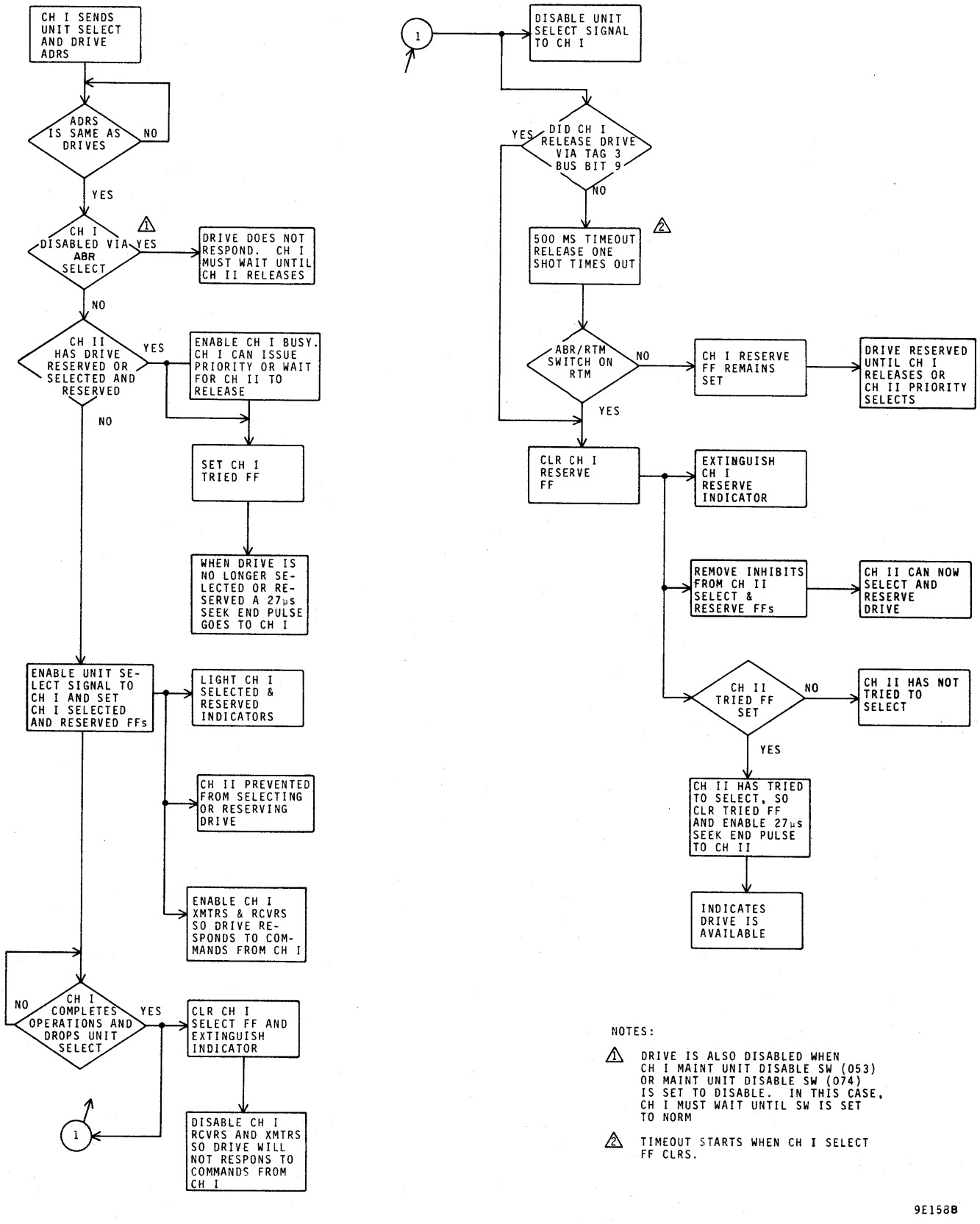


Figure 3-15. Dual Channel Select and Reserve Flow Chart

TABLE 3-3. DUAL CHANNEL UNIT SELECT CIRCUIT FUNCTIONS

Element *	Function
ABR/RTM Switch	Determines whether the drive will be in ABR (absolute reserve) or RTM (reserve timeout) mode. If switch is in RTM position, drive is released from reserved condition 500 ms (nominal) after being deselected. If switch is in ABR position, drive remains reserved until it receives either a release or Priority Select command.
Release Timeout One Shot	Deselecting drive causes this one shot to generate a 500 ms (nominal pulse). If drive is in RTM mode the trailing edge of this pulse clears the reserved FF.
Channel I Disable FF	Sets if drive receives Priority Select command. This causes drive to be selected and reserved drive for controller issuing command and disables channel to other controller.
Channel I Maintenance Unit Disable Switch	Disables channel I whenever it is set to disable position. It must be in NORM position during normal operations.
Channel I Reserved FF	Sets during select and reserve sequence. When set it keeps drive reserved to channel I until channel I releases or channel II issues a Priority Select command.
Channel I Selected FF	Sets during select and reserve sequence and enables transmitters and receivers to channel I controller.
Channel I Select and Compare Logic	Compares logical address of drive with that sent by controller (see single channel Unit Selection).
Reserved Pulse One Shot	Generates 300 ns pulse whenever either selected FF sets. Leading edge of this pulse clocks Channel I Reserve FF and trailing edge clocks Channel II Reserve FF.
Tiebreaker Oscillator	Provides 5MHz clock pulses for the channel I and channel II Selected FFs. Channel I selected is clocked by leading edge of each pulse thereby giving priority to channel I in cases where both controller attempt selection simultaneously.
Channel I Select Tried FF	Sets if channel I tries to select and reserve drive while it is already selected and/or reserved by channel II. When drive is deselected and released by channel II, this FF clears and thereby triggers the Select Tried One shot.
Select Tried One Shot	Generates 27 μs pulse whenever either Tried FF clears. This pulse is sent to controller (associated with the Tried FF that triggered the one shot) via the Seek End line.

* Includes only those elements directly concerning channel I and shown on figure 3-14.

Select Tag and logical address from channel I, it compares the address received with that indicated by its logical address plug. If the two addresses are the same, the drive enables the Channel I Select Compare signal. The logic used to generate this signal is identical to that used in the single channel units (refer to figure 3-13).

Enabling Channel I Select Compare causes Channel I Unit Selected to go active and also remove the clear from the Channel I Selected FF. The next 5 MHz tiebreaker clock pulse sets the Channel I Selected FF.

Setting the Channel I Unit Selected FF enables the channel I receivers and transmitters as well as triggering the 300 nanosecond Reserve one shot. The resulting one shot pulse clocks and sets the Channel I Reserved FF. With the select and reserve FFs set, the sequence is complete and the drive responds to further commands from channel I.

Provided channel II does not issue a priority select (see Priority Select Function discussion), the drive remains selected and reserved to channel I until this controller

either disables its Unit Selected Tag or changes the logical address. At this time, the drives Channel I Selected FF clears thus disabling the transmitters and receivers to that channel. This also disables the Unit Selected signal thus informing the controller that the drive will no longer respond to commands. However, the drive remains reserved to channel I (thus allowing channel I to reselect while preventing channel II from selecting) until the Channel I Reserve FF is also clear. This is cleared by either a release, priority select, or maintenance disable function (refer to these discussions).

If Channel I attempts to select and reserve the drive while it is selected and reserved by channel II, the channel I Select Compare signal is still generated as during the Initial Select and Reserve sequence. However, the Channel I Select and Reserve FFs do not set, and therefore the attempt is unsuccessful. The drive still sends the Channel I Unit Selected signal to the controller; but, in this case, it is accompanied by the Channel I Busy signal. The Busy signal indicated that the drive is being used by channel II.

The drive also sets its Channel I Tried FF, thus recording the unsuccessful attempt. When the drive is no longer selected or reserved by channel II, this FF clears thereby generating a 27 μs Seek End Pulse to the channel I controller. This informs the controller that the drive is no longer selected or reserved.

If the channel I controller tries to select the drive while channel I is disabled (either by a priority select or maintenance disable function), the attempt is unsuccessful and no response is sent back to the channel I controller.

Release Function

The release function will release the drive from either a reserved or priority selected condition. There are two types of release functions: (1) timeout release pulse and (2) Release command.

The timeout release pulse is capable of releasing the drive from only the reserved condition. This pulse is generated by the 500 ms Timeout Release one shot and releases the drive by clearing the Reserve FF. The pulse is triggered when the drive is selected (Select FF sets), and times out 500 ms after the drive is deselected (Select FF clears).

Whether or not the one shot has any effect on the Release FF, depends on the position of the ABR/RTM switch. If this switch is in the RTM (reserve timeout) position, the FF clears when the one shot times out thus making the drive available to the other channel. However, if this switch is in ABR (absolute reserve) position, the one shot has no effect on the FF and the drive remains reserved.

A Release command releases the drive from both the absolute reserved and priority selected conditions. This command is initiated by the reserving and/or priority selecting controller when it issues a Tag 3 (Control Select with Bus Bit 9 active. This clears the Reserve and Disable FFs and allows the other controller to select the drive.

Priority Select Function

If the drive is selected and reserved, the other controller can force selection by issuing a Priority Select command (Unit Select Tag accompanied by drive logical address and Bus Bit 9). This command disables the channel to the controller presently using the drive and also select and reserve the drive to the controller issuing the priority select.

For example if channel I has the drive and channel II wants to select, channel II issues a Priority Select command. In this case, the command sets the Channel I Disable FF which in turn clears the Channel I Selected and Reserved FFs. It also sets the Channel II Selected and Reserved FFs thereby selecting and reserving the drive for channel II.

Once the Disable FF is set, that channel (in this case channel II) is disabled until the other controller (in this case channel II) issues a command to clear it.

Maintenance Disable Function

It is also possible to disable either channel by setting Maintenance Unit Disable switch for that channel (refer to figure 3-14) to the disable (DI or DII) position.

SEEK FUNCTIONS

GENERAL

The drive must move the heads to the desired position over the disk pack before any read or write operation can be performed. This is done during seek functions and is performed by the drives servo circuits.

The servo circuits form a closed loop servo system that controls movement by comparing the present position of the heads to the desired future position and generating a position control signal proportional to the difference between them.

The major elements in the servo loop are shown on figure 3-16. The servo circuit functions are described in table 3-31.

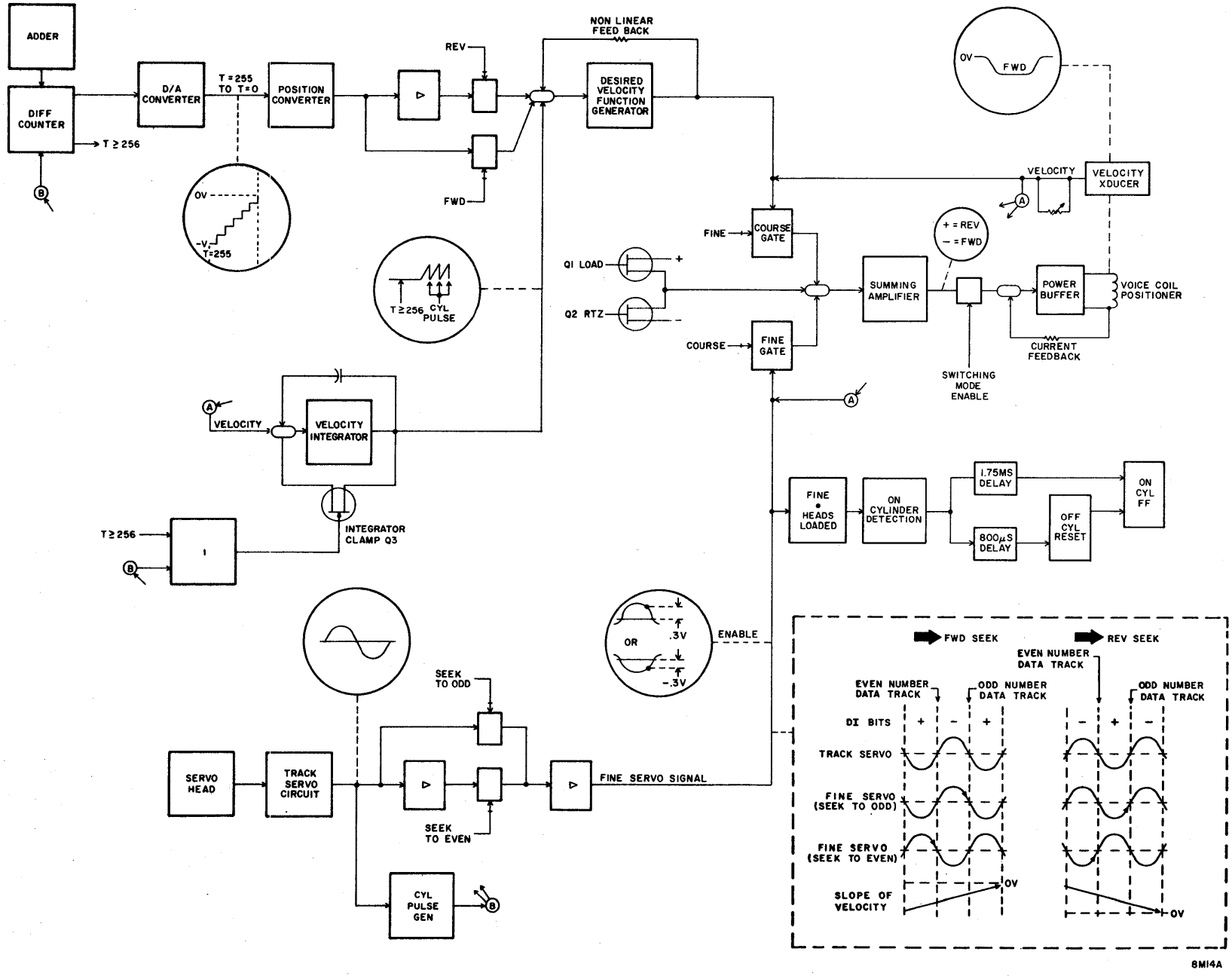


Figure 3-16. Servo System Functional Block Diagram

TABLE 3-3.1. SERVO CIRCUIT FUNCTIONS

Circuit Element	Function
Cylinder Address Register	Holds the present cylinder address. It is updated to the new cylinder address when a seek is initiated.
Cylinder Address Adder	Combines the present cylinder address with the new cylinder address complement to arrive at the difference.
Difference Counter	Holds the number of tracks yet to be crossed before reaching the desired track or cylinder. Counter value is zero when on cylinder.
Digital-to-Analog Converter	Monitors the seven lowest order bits of difference counter to provide an analog indication of Position Error during the last 256 tracks (except last track) of all Seek operations.
Position Converter	Provides coarse Position Error signal, the amplitude of which is proportional to the number of tracks to go. Amplitude is clamped at negative saturation while tracks remaining are equal to, or greater than 256. Amplitude decreases in discrete steps (controlled by D/A converter) as last 256 tracks of a seek are crossed. Signal is inverted for reverse seeks.
Desired Velocity Function Generator	Processes Position Error signal at gain levels that vary as Position Error decreases. The resulting output is the analog representation of the desired velocity curve to achieve maximum control to deceleration. The parallel non-linear feedback circuit maintains tight loop control by increasing gain as the Position Error signal approaches zero. This gain control prevents loss of control during the critical deceleration portion of the seek and is essential to minimize overshoot and settle out problems. It also minimizes drift about null.
Summing Amplifier	Generates a control signal to drive the power amplifier. When Position Error exceeds Velocity Amplifier signal, control signal causes power amplifier to accelerate carriage. When Velocity signal exceeds Position Error, carriage decelerates.
Switching Mode Control	Decelerates carriage from tracks equal 256 to tracks equal 7 by supplying pulses of maximum reverse current to the voice coil to follow Position Error deceleration curve.
Load Gate	Provides a constant positive input to the summing amplifier. This causes forward velocity 7 in/s (178 mm/s).
RTZ Gate	Provides a constant negative input to the summing amplifier. This causes reverse velocity 7 in/s (178 mm/s).
Power Amplifier	Responds to summing amplifier derived control signal to drive carriage mounted voice coil positioner. Current feedback is used to stabilize the gain of the power amplifier.

Table continued on next page

TABLE 3-3.1. SERVO CIRCUIT FUNCTIONS (Cont'd)

Circuit Element	Function
Velocity Amplifier	Amplifies signal of carriage mounted linear velocity transducer to provide an indication of velocity to the servo circuit. Also receives a negative feedback from positioner which acts to cancel current coupling that occurs from the velocity transducer location within the magnetic field created when current is applied to the voice coil positioner. The associated amplifier disable forces amplifier gain to zero during a Power Off sequence (unload heads). This is required so that coupling between the positioner field and the velocity transducer does not cause oscillation during movement to the retraction position.
Velocity Integrator	Provides an integrated representation of velocity between each of the last 256 track pulses of a seek. Integrator is clamped off to gain of zero at all other times. Integrator output is a sawtooth waveform applied to input of desired velocity function generator between each track pulse to fill in or smooth out the stepped signal of the D/A converter (received via the position converter).
Fine Servo and Fine Latch	Fine servo monitors integrated velocity. When difference counter is 1 (T=1) and integrated velocity exceeds 1.4 V, it indicates that there is one-half track to go. Fine latch sets to enable fine gate and disable coarse gate. This switches Position Error input to summing amplifier from desired velocity (coarse gate) to fine position (fine gate). Fine also has the following effects: a. Turns on integrator clamp to switch off velocity integrator. b. Enables on cylinder detection. During load or RTZ sequences, both outputs of Fine Latch are high. This disables both the fine and coarse gates so that motion is under control of load gate or RTZ gate.
Bit 0 Address Register and Slope FF	Used to select proper track servo signal phase for use as Fine Position Analog signal (signal controlling servo loop as last track is approached and carriage is stopped). If bit 0 is not set, the seek destination is an even numbered track and the track servo signal will not be inverted for use in stopping the carriage. If bit 0 is set, an odd track is identified and track servo is inverted. Register bit content is placed in Slope FF which performs actual gating.
On Cylinder Detector	Monitors fine position signal when T<1. When signal is less than about 0.98 V, heads are close enough to track centerline to be assumed to be on cylinder. After 1.75 ms delay, On Cylinder is returned to controller and to drive logic. If heads overshoot at end of seek so that voltage exceeds 1.61 V, delay is reinitiated. Delay permits carriage to settle out before controller may attempt any read/write operations.

SERVO DISK INFORMATION

General

The servo disk surface (refer to figure 3-17) contains servo positioning information that is recorded on the disk at the time of manufacture.

This information is read by the servo head and processed by the position feedback circuits. These circuits generate position feedback signals that are used by the positioning circuits to control the positioning of the heads. The servo disk information is also used to generate clock signals used by the Index and Machine clock circuits.

The following describes the information recorded on the servo surface.

Dibits

The servo positioning information is recorded on the disk as specific patterns of flux reversals referred to as dibits. There are two types of dibits: positive and negative.

The positive and negative dibits are classified according to the type of waveform produced when they are read by the servo head (the waveform actually appears at the output of the track servo preamp). The positive dibits produce a waveform with the leading pulse positive and the trailing pulse negative. The negative dibits produce a waveform with the leading pulse negative and the trailing pulse positive. The dibit patterns and their associated waveforms are shown on figure 3-18.

Dibit Tracks

The dibits are recorded in track patterns around the disk. The servo surface has 441 (833) dibit tracks each recorded exclusively with either positive or negative dibits. These

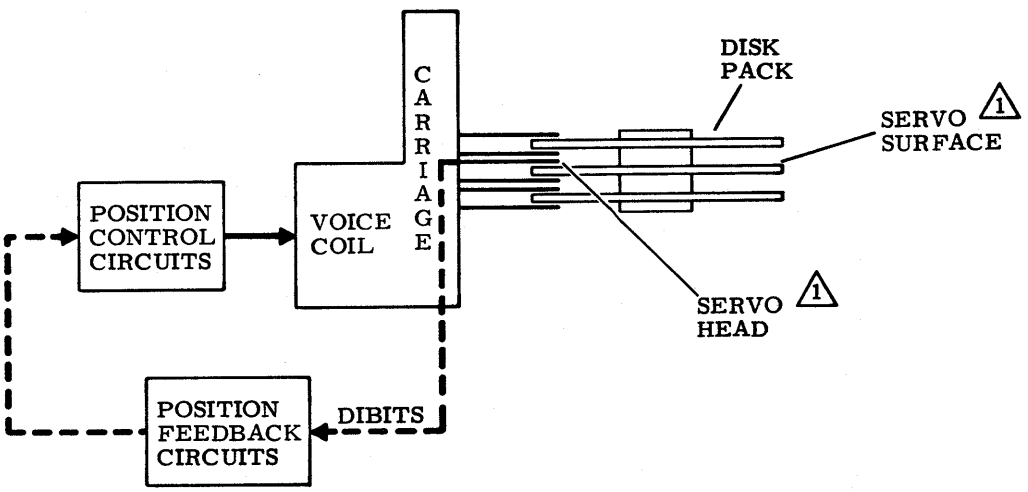


Figure 3-17. Servo Head and Surface

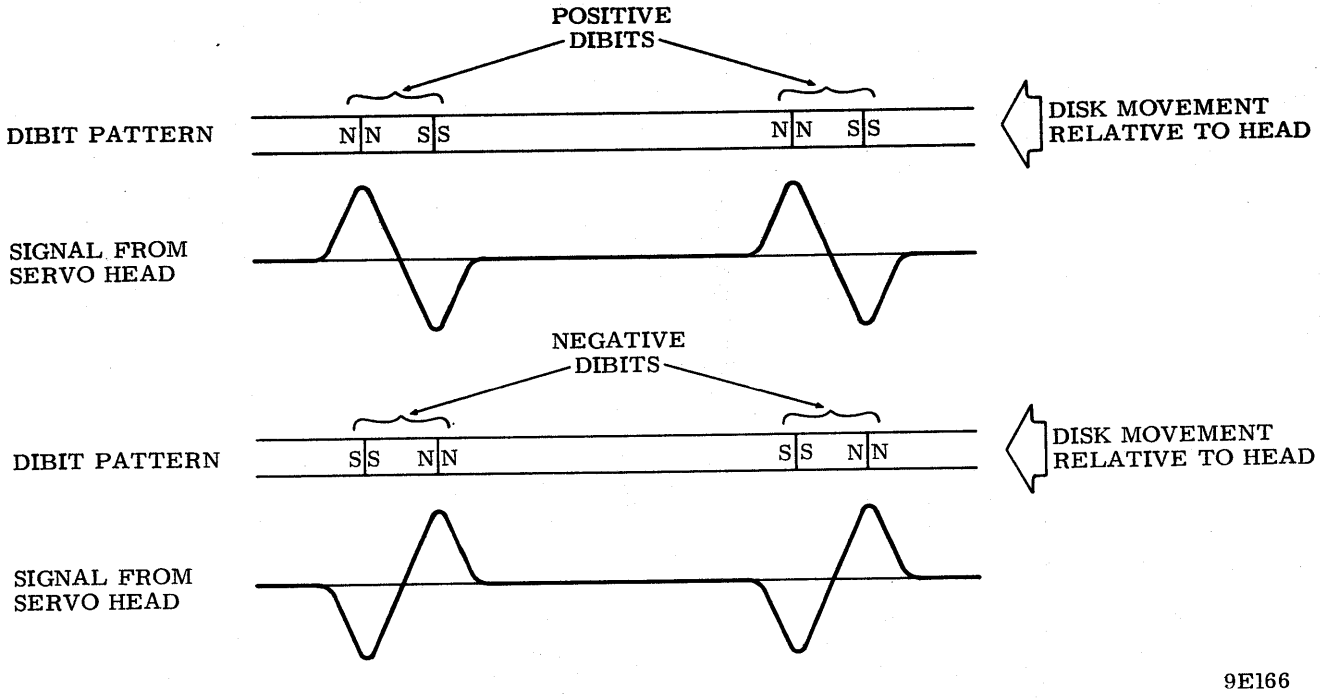


Figure 3-18. Positive and Negative Dibit Pattern

tracks are recorded adjacent to one another with no void area between them. Those tracks containing only positive dibits are known as positive-odd dibit tracks and those tracks containing only negative dibits are known as negative-even dibit tracks.

Outer and Inner Guard Bands

The outer 12 (24) tracks are positive-odd dibit tracks and contain only positive dibits. This area is known as either the outer guard band or the reverse end of travel (EOT).

The inner 18 (36) tracks are negative-even dibit tracks and are known as either the inner guard band or the forward end of travel (forward EOT).

Both the outer and inner guard bands are shown on figure 3-19.

Servo Zones

In between the inner and outer guard bands is an area called the servo zone.

The servo zone consists of 412 (824) alternately spaced positive-odd and negative-even dibit tracks. Because the dibit tracks are adjacent to one another, junctions are formed between the positive and negative tracks. These junctions are referred to as servo tracks. The servo zone contains 411 (823) servo tracks, numbered from 000 to 410 (822).

Cylinder Concept

The data recording zones on the data surfaces are aligned vertically with the servo track zone on the servo surface. For this reason, all head movement and positioning is referenced to the position of the servo head over the servo surface.

Therefore, when the servo head is positioned over a specific servo track on the servo surface, all other heads are positioned over the corresponding data tracks on their respective data surfaces. For example, if the servo head is over track 10, all other heads are also over track 10. The vertical alignment of these tracks create an imaginary cylinder as shown on figure 3-20.

POSITION FEEDBACK GENERATION

General

All position feedback information is generated by the position feedback circuits. These circuits use the dibit data read from the servo disk to generate the feedback signals required by the position control circuits.

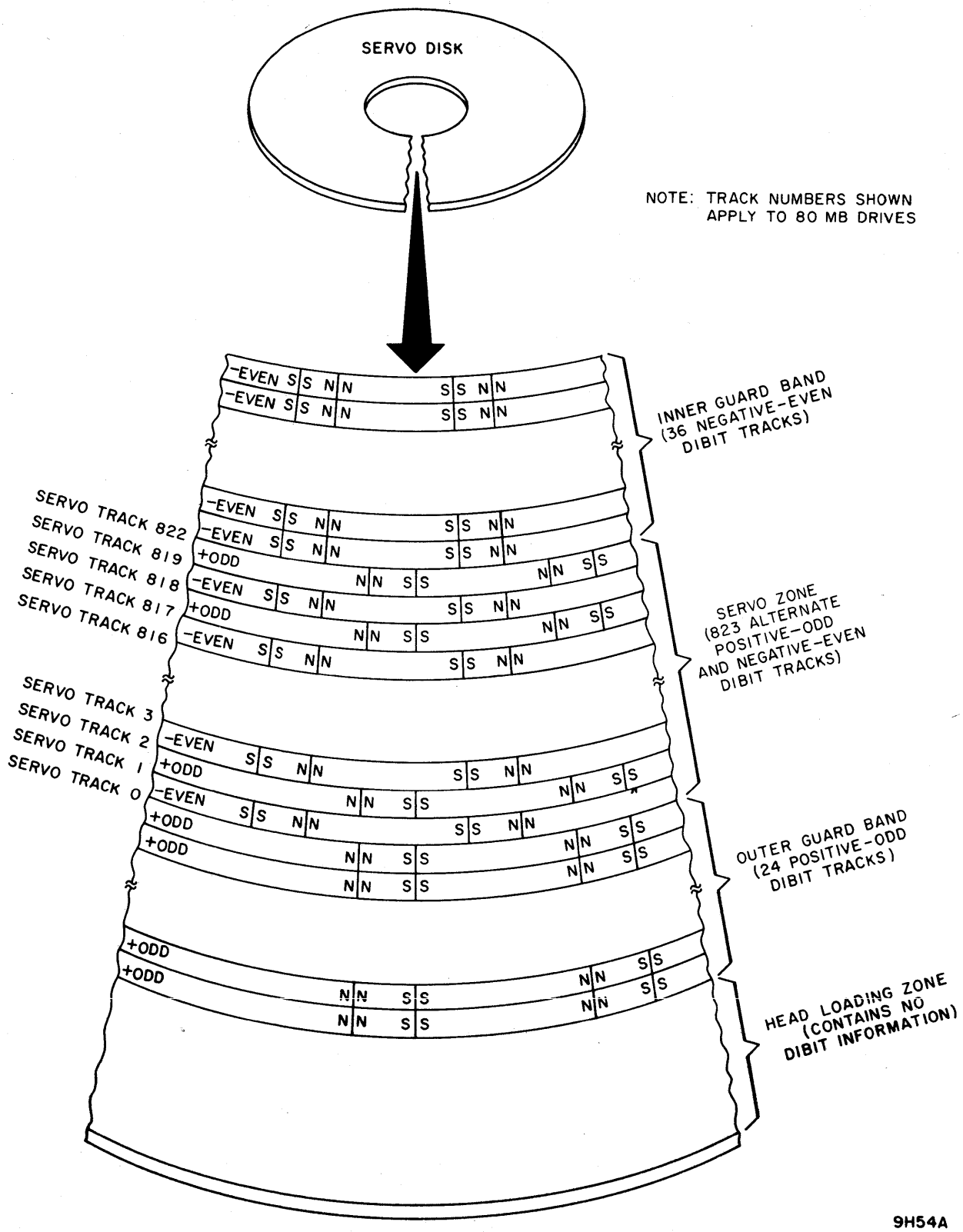


Figure 3-19. Servo Disk Format

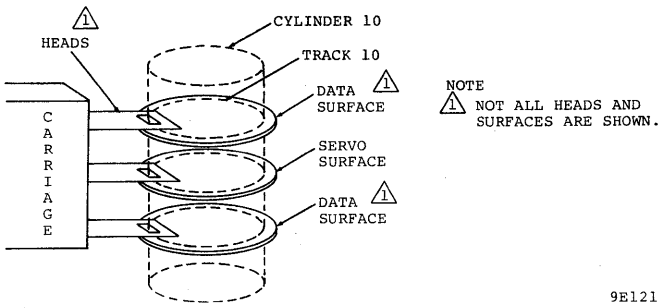


Figure 3-20. Cylinder Concept

The feedback signals generated and their basic functions are as follows:

- Track Servo signal - Used by the fine position control circuits to control positioner movement during the last half track of a seek.
- Cylinder Pulses - Pulses that occur each time the servo head crosses a servo track. These pulses are used by the coarse position control to determine the distance to the desired cylinder.
- Reverse EOT Pulse - Provides feedback to the RTZ coarse position control circuits during a return to zero seek (RTZS).
- Forward EOT Enable and Odd Dibits - Provides feedback during RTZ, Load, and Unload seeks that cause positioning control to be switched from the RTZ, Load, and Unload coarse position control circuits to the fine position control circuits.

In addition to providing these signals, the position control feedback circuits also produce the Odd/Even dibit signals used by the Machine Clock and Index Detection circuits.

A basic block diagram of the position feedback circuits is shown on figure 3-21 and each of the elements on the diagram are explained in the following discussion.

Track Servo Preamp

This signal from the servo head must be processed by the track servo preamplifier before the servo track information can be used by the rest of the position feedback circuits.

The signal received from the servo head depends on the type of servo dibit track it is reading. When the head is over the outer or inner guard bands, it reads from tracks that have either all positive or all negative dibits. In this case, the preamp produces either all positive or all negative dibit waveforms (refer to figure 3-18).

When the head is over the servo zone, it passes over both types of dibit tracks and the preamp produces a waveform that is a mixture of both types of dibit signals.

The amplitude of each dibit component in the waveform is proportional to how much the servo head is overlapping the tracks. If the head is centered over a servo track the signal has equal positive and negative dibit components. However, when the head is away from the centerline, the amplitude of one dibit component is greater than the other (this is shown on figure 3-22).

If the servo head is moving through the servo zone, each component alternately increases and decreases as the servo tracks are passed. This is also shown on figure 3-22.

The output of the track servo preamp is sent to the AGC and dibits detect circuit.

Dibit Sensing

The dibits sense circuit (refer to figure 3-21) detects the presence of dibits data. The output from this circuit is the Dibits Sense signal and it must be active (indicating dibits are present) for the position feedback circuits to function. This prevents them from generating false signals when no dibits are present (as for example, during a heads load or when heads are unloaded).

The Dibits Sense signal is first enabled during the heads load sequence when the heads loaded switch transfers. The signal goes active when dibits with an amplitude of at least 145 mv peak to peak have been present for 3 ms. if the Dibits Signal should drop below this level for more than 50 µs, the Dibits Sense signal goes inactive thus disabling the cylinder crossing, odd/even dibits clock and track servo amplifier circuits.

Therefore, losing dibits results in totally disabling the position feedback circuits.

Automatic Gain Control (AGC)

The purpose of the AGC circuits (refer to figure 3-21) is to provide gain control for the dibits signals before applying them to the track servo amplifier and odd/even dibits clock circuits. This gain control is necessary for proper servo system operation. The outputs from the AGC circuits are the AGC'ED Servo signals.

Gain control is obtained by feeding back a signal from the track servo circuit to the AGC circuits. This feedback signal, referred to as AGC, is derived from the AGC'ED Servo signals and the amplitude of the AGC and AGC'ED Servo signals are directly proportional. Therefore, when the AGC'ED Servo signals increase it causes an increase in the AGC signal and vice versa.

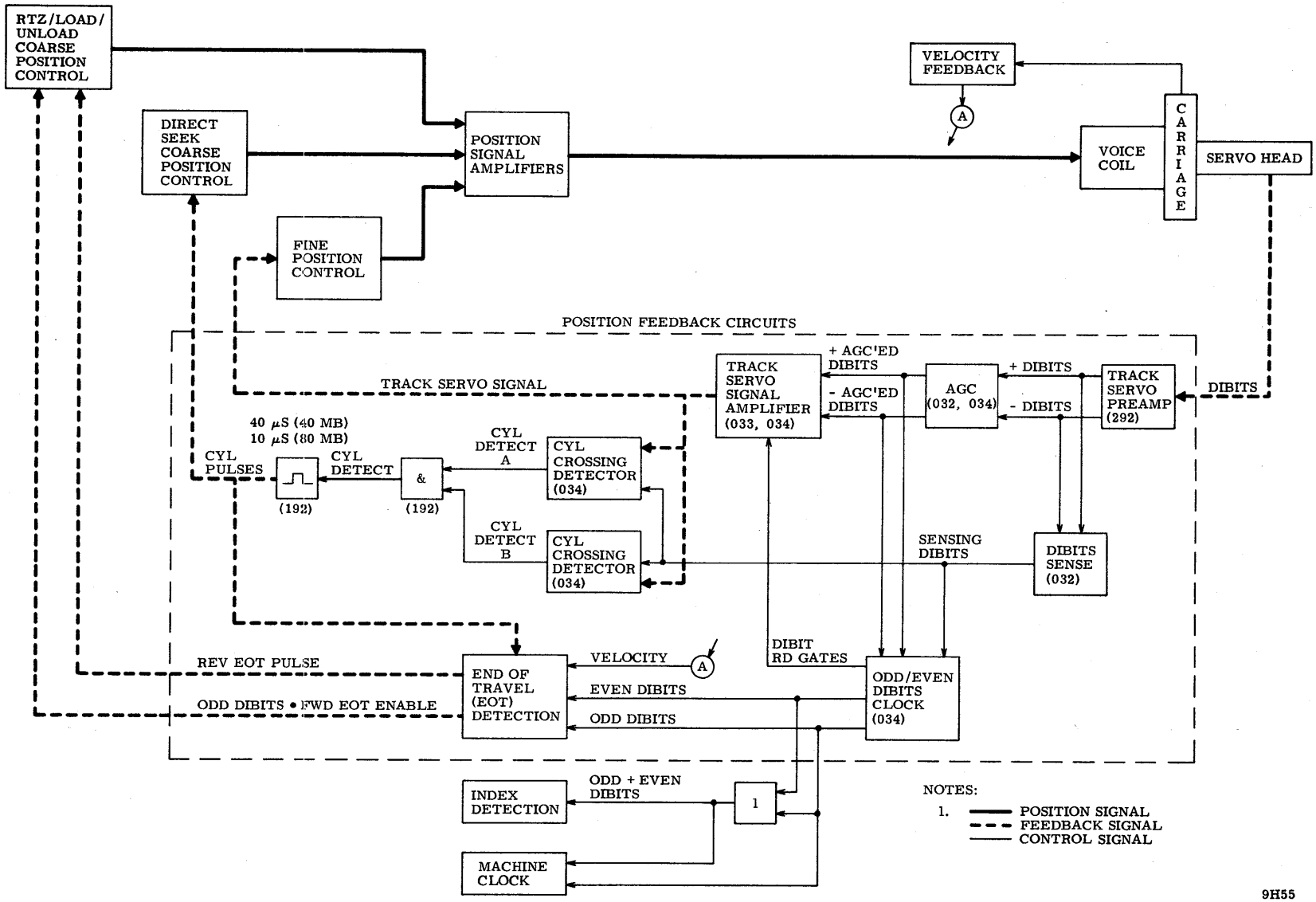


Figure 3-21. Position Feedback Circuit - Block Diagram

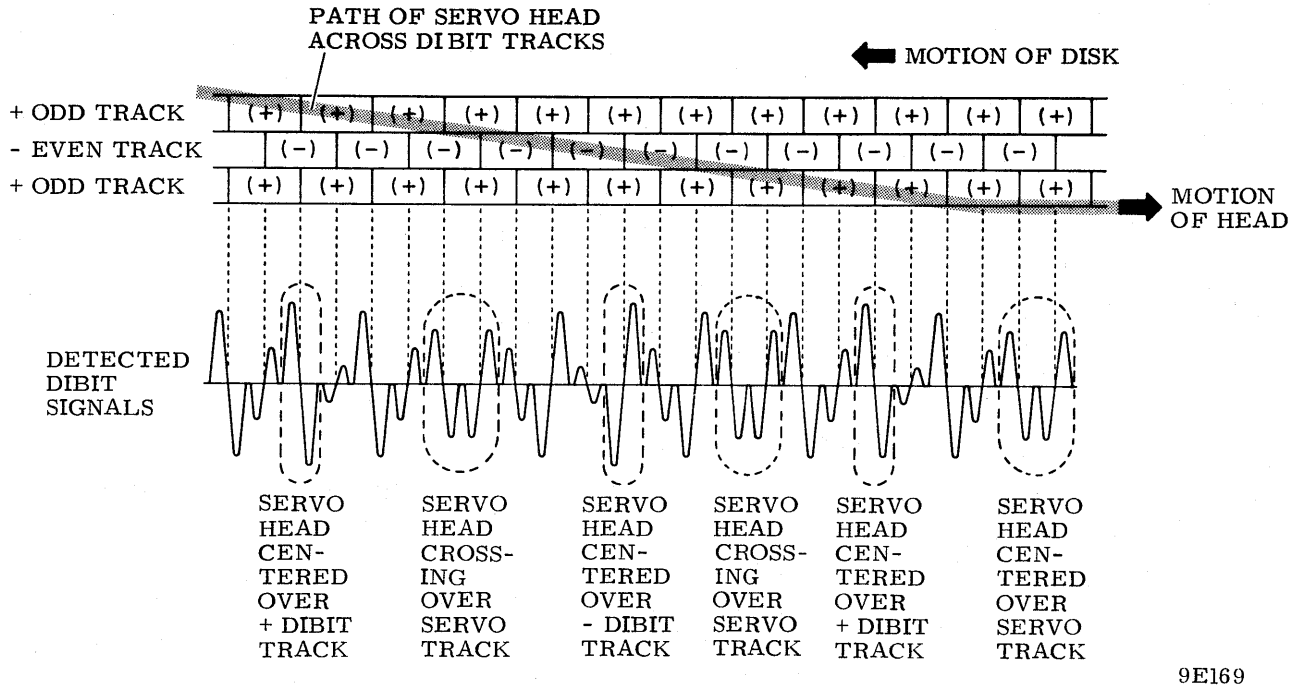


Figure 3-22. Servo Preamp Output

When the AGC signal increases, it causes a decrease in the gain of the AGC circuits. This results in reducing the amplitude of the AGC'ED Servo signal.

When the AGC signal decreases, the gain of the AGC circuits increases and the AGC'ED Servo signal becomes larger.

The net result is that the overall gain of the AGC Circuit remains constant.

Track Servo Signal Amplification

The track servo amplifier circuits (refer to figure 3-23) used the AGC'ED Servo signal from the AGC circuit and the Dibit read gate signals from the odd/even dibit clock circuits to produce a signal that varies as the position of the servo head changes with respect to the dibit tracks. This signal is referred to as the track Servo signal.

The main elements in the track servo circuits are the peak detectors, peak detector buffers, AGC control amplifier and differential amplifier (refer to figure 3-23).

The peak detectors monitor the AGC'ED Dibits signals and are enabled by the Positive-Odd and Negative-Even Dibit Read Gate signals.

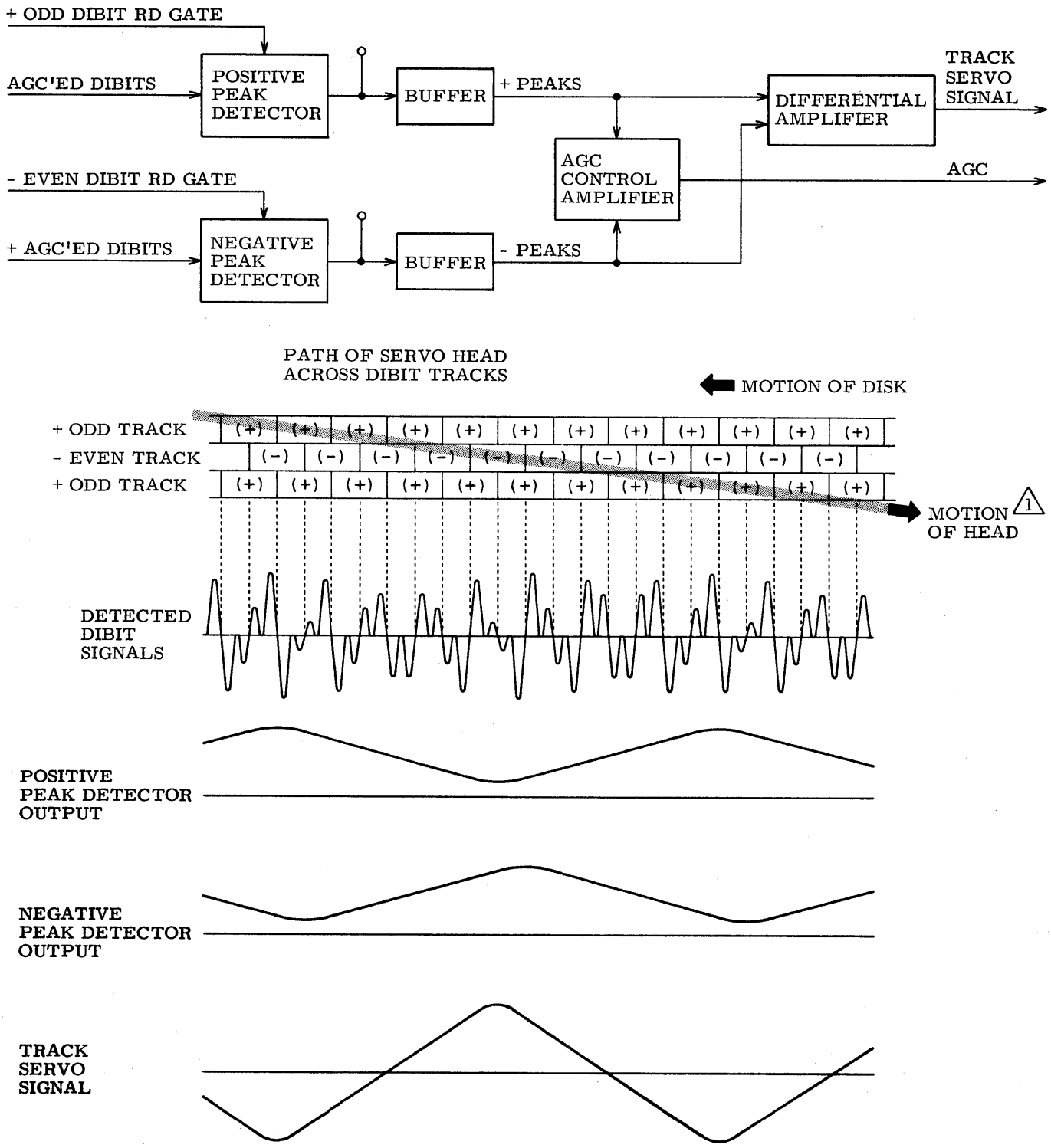
The positive peak detector is enabled by the Positive-Odd Dibit Read Gate signal and is active during the positive portion of the positive-odd dibit cycle. The negative peak detector is enabled by the Negative-Even Dibit Read Gate signal and is active during the negative portion of the negative-even dibit cycle. The peak detectors are inactive at all other times.

This results in peak detector outputs that are proportional to the amplitude of the dibit signals they are monitoring. Therefore, the positive peak detector output is maximum when the servo head is over a positive-odd dibit track the negative peak detector output is maximum when the head is over a negative-odd dibit track (refer to figure 3-23).

The outputs of the peak detectors are processed by the peak detector buffers to provide signals of the proper amplitude and polarity for the AGC and differential amplifiers.

The AGC control amplifier uses the buffer outputs to generate the AGC voltage that is used by the AGC circuits.

The differential amplifier uses the two buffer outputs to produce a voltage with a polarity and magnitude directly proportional to the difference between them. This is the Track Servo signal.



NOTES:

1. MOTION OF HEAD EXAGGERATED.
2. ALL WAVEFORMS IDEALLIZED FOR PURPOSES OF ILLUSTRATION.

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Figure 3-23. Track Servo Amplifier Circuit and Signals

The Track Servo signal is at its maximum positive value when the servo head is over negative-even dibit tracks and maximum negative when the servo head is over positive-odd dibit tracks.

If the servo head is centered over a servo track (between positive-odd and negative-even dibit tracks) the signal is zero. Therefore when the servo head moves through the servo zone, the Track Servo signal passes through zero each time the head crosses a servo track (refer to figure 3-23).

The Track Servo signal is applied to the Fine Position control and Cylinder crossing detection circuits. The Fine Position control circuits use the signal to generate the positioning signal that controls movement during the last one half track of a seek (and during forward EOT conditions). The Cylinder crossing detect circuits use the signal to generate cylinder pulses as each servo track is crossed.

Odd/Even Dibits Clock Generation

The odd/even dibits clock circuits (refer to figure 3-24) generate the Odd Dibits, Even Dibits and also the Odd and Even Dibits Read Clock signals. These signals are derived from the AGC'ED Dibits signals which are applied to the level detectors.

The level detectors create digital pulses from the AGC'ED Dibits signals by switching to their low state whenever they sense their respective dibit signals. The level detectors are enabled by the Sensing Dibits signal which is active only when dibits are being read from the disk.

The outputs from the level detectors are used to produce both the dibits read gate and odd/even dibits signals.

The Odd and Even dibits Read Gate signals are generated when their respective one shots are triggered by the negative going edge of the level detector outputs. The dibit read gate signals are used to enable the track servo amplifier circuits.

The Odd Dibits and Even Dibits signals are produced by the outputs of the level detectors working in conjunction with the output of the dibits read gate one shots. The logic and timing for this is shown on figure 3-24.

The Odd Dibits and Even Dibits signals have a nominal frequency of 403 Khz. However, becuase they are derived from dibits which are in turn derived from the rotating disk, this frequency will vary with disk speed.

The Odd or Even Dibits signal is generated by ORing the Odd Dibits and Even Dibits signals. This produces an 806 Khz (nominal) signal which also varies with disk speed.

The Odd Dibits, Even Dibits and Odd or Even Dibits signals are used by the machine clock, index detection and End of travel detection circuits (refer to discussion on these circuits for more information).

Cylinder Crossing Detection

The cylinder crossing detection circuits (refer to figure 3-21) use the Track Servo signal to generate a pulse as each servo track is crossed.

When the servo head crosses a servo track the heads are crossing a cylinder (refer to discussion on Cylinder Concept); therefore, these pulses are called Cylinder Pulses.

The cylinder crossings are detected by cylinder crossing detectors A and B. Cylinder crossing detector A produces an output pulse from the time the Track Servo signal goes through zero in a positive direction until it goes through -0.4 V in a negative direction (see figure 3-25). Cylinder crossing detector B produces an output pulse from the time the Track Servo signal gies through zero in a negative direction until it goes through +0.4 V in a positive direction.

This results in an overlapping of the two pulses after each zero crossing and combining them produces a pulse to trigger the 40 µsec (10 µsec) Cylinder Pulse one shot.

The Cylinder Pulses from the one shot are used by the direct seek coarse control circuits to count the number of cylinders crossed during a seek. They are also used by the End of Travel Detection circuits. Refer to the discussions on these circuits for further descriptions of how they are used.

It should be noted that the cylinder crossing detection circuits are operative only when the heads are loaded and dibits are being read from the disk. At all other times, the Sensing Dibits signal is inactive thus disabling the cylinder crossing detectors. This prevents false Cylinder Pulses from being generated.

End of Travel Detection

The end of travel (EOT) detection logic (refer to figure 3-26) is used to sense when the heads are outside of the data area and over one of the guard bands. Depending on the type of seek being performed, the output from this circuit will be interpreted as either an error indication or a feedback signal.

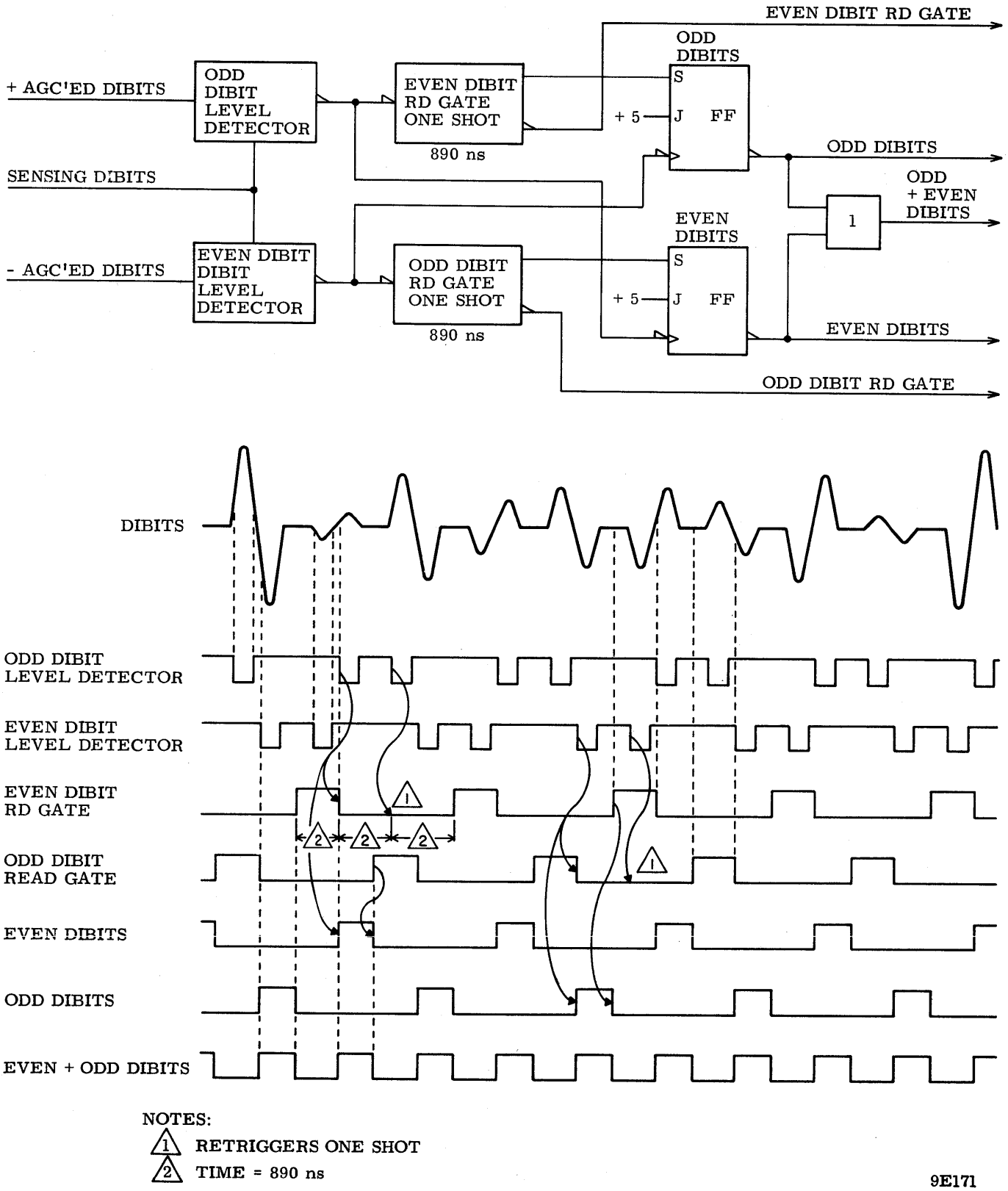


Figure 3-24. Odd/Even Dibit Clock - Logic and Timing

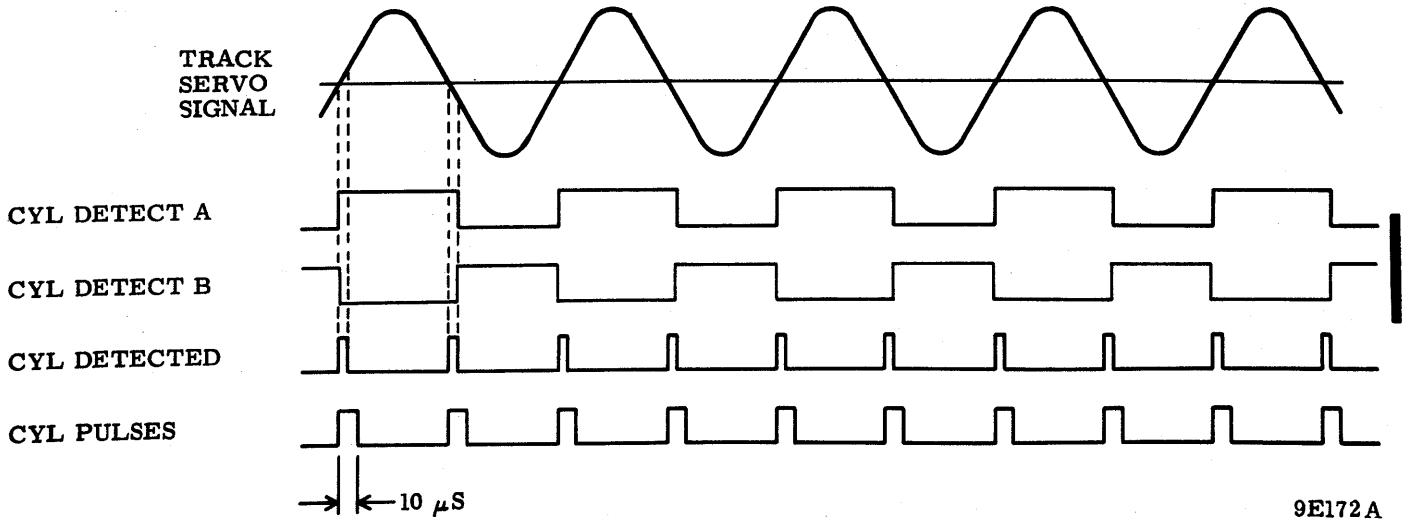


Figure 3-25. Cylinder Crossing Detection

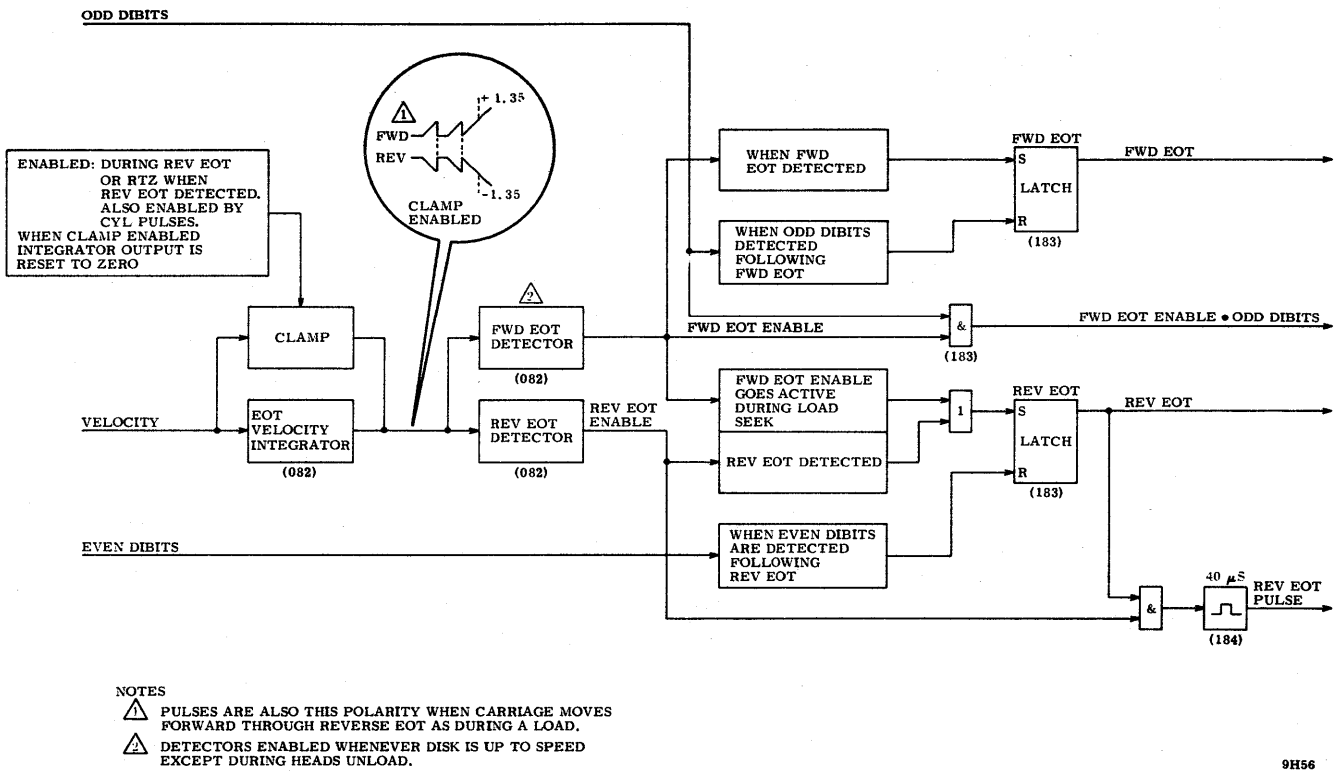


Figure 3-26. End of Travel Detection Circuits

If the drive is performing a direct seek to one of the tracks in the data area, an EOT is interpreted as a positioning error and the proper error sequence is initiated. However if an RTZ, Load or Unload seek is being performed, the EOT signals are used as feedback for the RTZ/Load/Unload coarse position control circuits.

The main elements in the EOT detection circuits are the EOT Integrator, EOT detectors and the Forward and Reverse EOT FFs.

The EOT Velocity Integrator works similar to the Desired Velocity Integrator in the direct seek coarse position control circuits. It monitors the Velocity signal and generates a sawtooth output waveform that rises from zero until reset by either a Cylinder pulse (when moving through data area) or by the Reverse EOT Pulse (during an RTZ when it detects the reverse EOT). If neither of these are present (as when moving over the outer or inner guard band) the output continues to rise.

The output from the EOT Velocity Integrator is monitored by the Forward and Reverse EOT detectors. The Forward EOT Detector is enabled whenever the integrator output exceeds +1.35 volts. This occurs either during a load when the heads are moving forward through the inner guard band or whenever the heads move into the outer guard band. In both of these cases the Velocity signal is of the proper polarity and there are no pulses to reset the integrator.

The Reverse EOT Detector is enabled whenever the Integrator output exceeds -1.35 volts. This occurs when the heads are moving in reverse over the inner guard band.

The Forward and Reverse EOT Enables are applied to the Forward and Reverse EOT FFs. The conditions causing these FFs to set and clear are shown on figure 3-26.

VELOCITY FEEDBACK GENERATION

The velocity of the carriage must be controlled to have the shortest seek time without having the heads overshooting or oscillating around the desired cylinder. The signal used to provide this control is generated by the velocity feedback circuits (refer to figure 3-27).

The velocity of the carriage is sensed by the velocity transducer. This is mounted within the magnet and consists of a stationary coil and movable magnetic core (refer to figure 3-28).

When the carriage moves, the core moves thus inducing in EMB in the coil. This EMF is converted by the velocity amplifier into the velocity signal.

The amplitude of this signal varies with the speed of the carriage and the polarity depends on the direction of movement. If the seek is in a forward direction, the polarity is negative and if it is in a reverse direction the polarity is positive.

Refer to the discussion on Electromechanical Functions for further description of the velocity transducer.

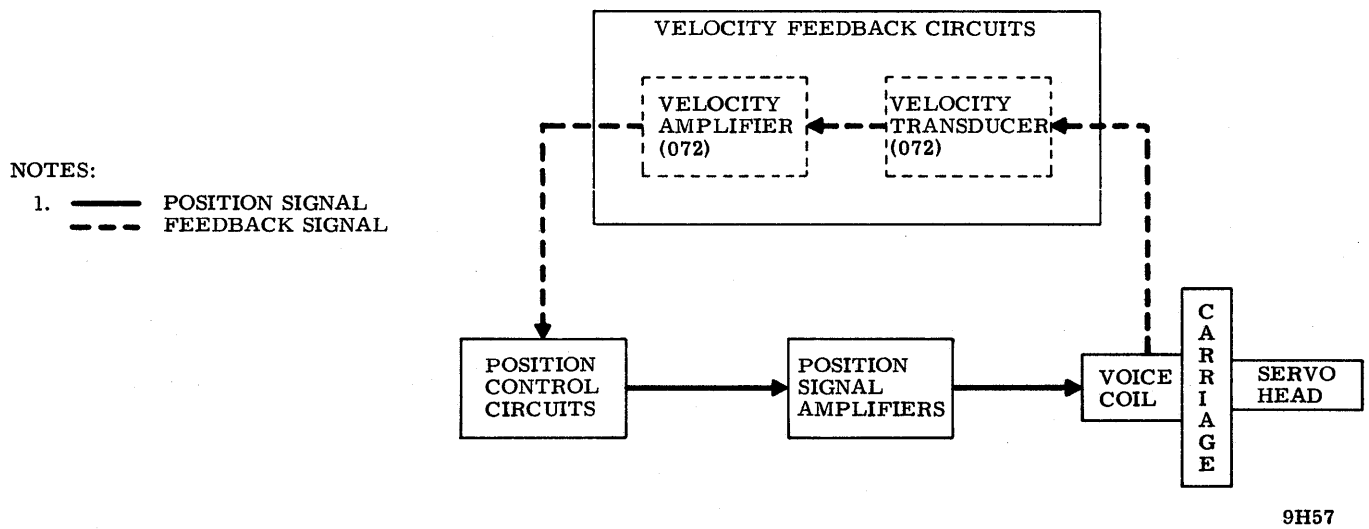


Figure 3-27. Velocity Feedback Circuits

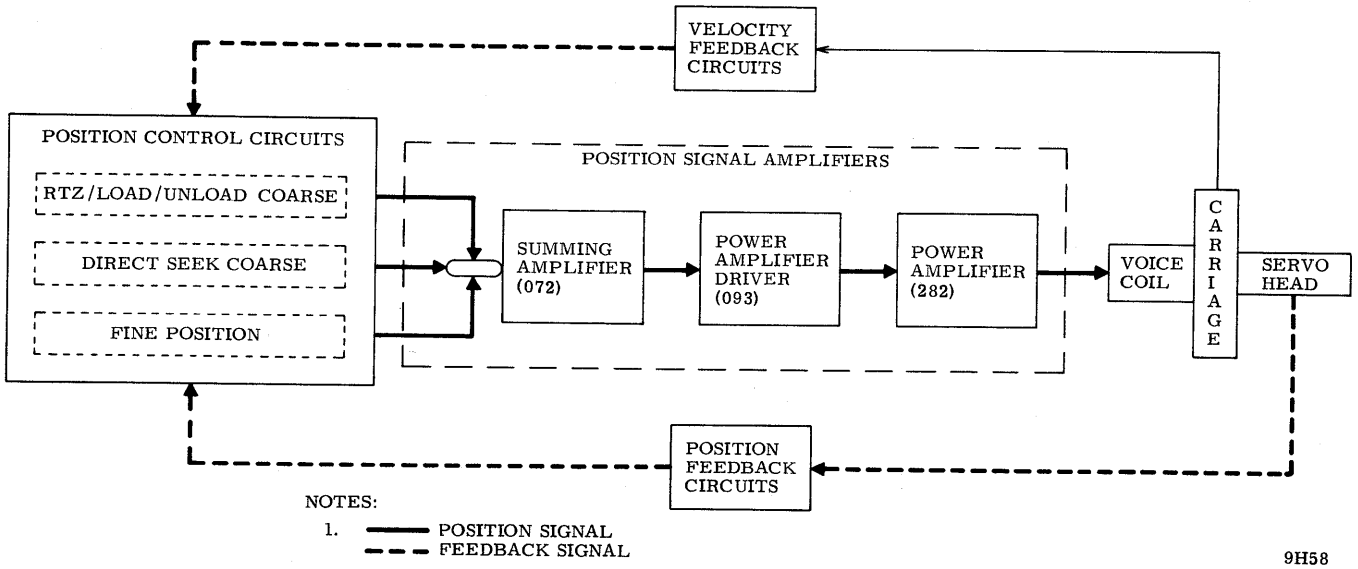


Figure 3-28. Position Signal Amplifier Circuits

POSITION SIGNAL AMPLIFICATION

The signals from the position control circuits are processed by the position amplifier circuits (refer to figure 3-28) to provide the current for the voice coil.

Any one of the three position signals may provide the input to these circuits depending on the type of seek being performed and how close the heads are to the destination. This input signal is applied to the summing amplifier.

The output from the summing amplifier is then applied to the power amplifier driver which uses it to generate the Forward and Reverse Current signals. These signals are sent to the power amplifier.

The power amplifier uses the Forward and Reverse Current signals to produce a voice coil current with the proper polarity and amplitude to move the voice coil and carriage thereby positioning the heads.

DIRECT SEEK POSITION CONTROL

General

A direct seek is one in which the drive is commanded by the controller to move the heads from their current logical cylinder location to another, specified by the controller. The controller initiates the direct seek by placing the new cylinder address on the Bus Lines and strobing the lines with a Cylinder Select command (Tag 1).

The direct seek function is divided into two modes: (1) coarse and (2) fine. The coarse mode consists of all but the last half track of the seek. The servo system is in fine mode during the last half track and while the heads are tracking over the desired cylinder. The following discussions describe both the coarse and fine modes.

Direct Seek Coarse Control

General

The direct seek is controlled by the direct seek coarse control circuits for all but the last half track of the seek. Figure 3-29 shows these circuits and the signals they generate.

The three main inputs to these circuits are the address of the destination cylinder (received from the controller in conjunction with the Cylinder Select tag), the Cylinder pulses (received from the position feedback circuits), and the Velocity signal (received from the velocity feedback circuits). These signals are used to produce a coarse positioning signal that varies with distance and also controls the speed of the carriage as it moves toward the destination.

How the coarse positioning signal is generated and also how the loop operates under coarse control is explained in the following paragraphs.

Coarse Position Signal Generation

At the start of the seek, the distance to the destination cylinder is determined by the comparator. It does this by comparing the address sent by the controller with the

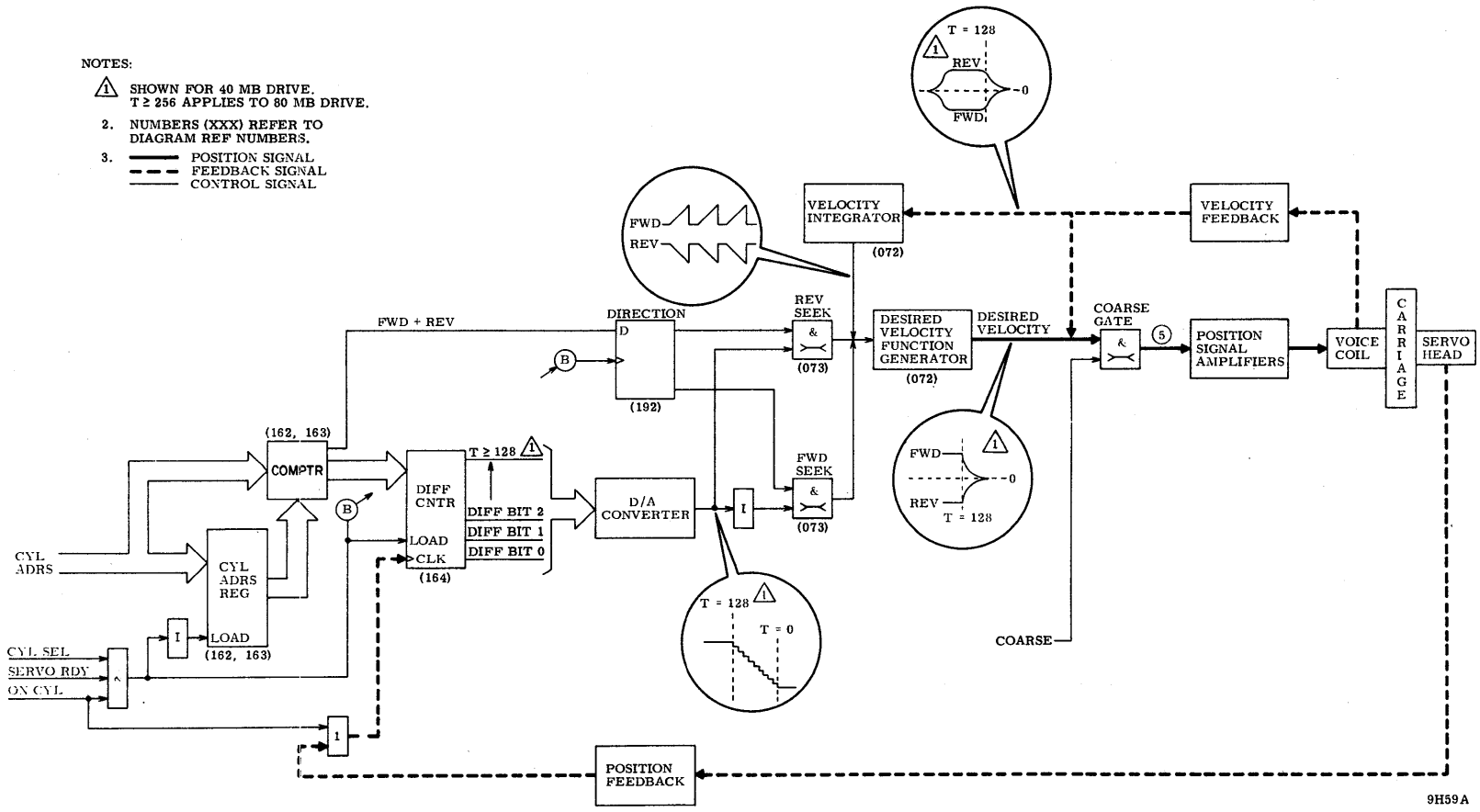


Figure 3-29. Direct Seek Coarse Position Control Circuits

address presently contained in the cylinder address register (this is the address at which the heads are presently located) and then generating a difference count indicating how many cylinders the heads will have to cross in reaching the new address.

The difference count is loaded into the Difference counter. After the difference counter is loaded, the new address (received from the controller) is loaded into the Cylinder Address register and will be the present address at the start of the next seek.

The Difference counter is decremented by the cylinder pulses as each logical cylinder is crossed thus keeping track of the number of logical cylinders left in the seek.

The output of the D/A converter is determined by the value of the input bits from the Difference counter. When these bits are all active, the D/A Converter output is maximum. This is the case where the number of logical cylinders to go exceeds 128 (256). However, when logical cylinders to go are less than 128 (256), the D/A Converter output steps down (with the counter output) as each logical cylinder is crossed.

The D/A Converter output signal is gated via either the Forward or Reverse gate to the Desired Velocity Function Generator. The output of the Desired Velocity Function Generator (Desired Velocity) varies in amplitude with the D/A Converter output (and therefore with distance to the destination) and in polarity with direction of the seek.

The seek direction is determined at the start of the seek by the adder which generates the Forward or Reverse signal. This signal is used to either set or clear the Direction FF and thereby enable either the Forward or Reverse Gate.

If the seek is in a forward direction (towards the spindle), the FF is cleared thus enabling the Forward gate. This causes a Desired Velocity signal that varies from a negative voltage to zero.

If the seek is in a reverse direction (away from the spindle), the FF is set thus enabling the Reverse gate. In this case, the Desired Velocity signal varies from a positive voltage to zero.

In either case the output from the D/A Converter must be smoothed out during the last 128 (256) logical cylinders of a seek to prevent steps from appearing in the Desired Velocity output. This function is performed by the Velocity Integrator.

The Velocity Integrator is enabled when logical cylinders to go reaches 128 (256) and at this point starts generating sawtooth pulses. These pulses start from zero at the time the Cylinder pulse goes false (which occurs after the cylinder crossing) and rises until by the next cylinder pulse (which occurs at the next cylinder crossing).

When the sawtooth pulses are summed with the D/A Converter output, the resulting Desired Velocity signal is a smooth curve that decreases in amplitude with distance to the destination cylinder.

The Desired Velocity signal is then summed with the Velocity signal which is received from the velocity feedback circuits. The Velocity signal varies in amplitude with carriage speed and is opposite in polarity to the Desired Velocity signal. It is necessary to sum Desired Velocity with Velocity in order to control carriage speed and thus ensuring minimum seek time without overshootint the destination cylinder.

The resultant signal, Desired Velocity summed with Velocity, is the final output of the coarse position circuits and is applied to the position signal amplifiers via the coarse gate.

Loop Operation During Coarse Control

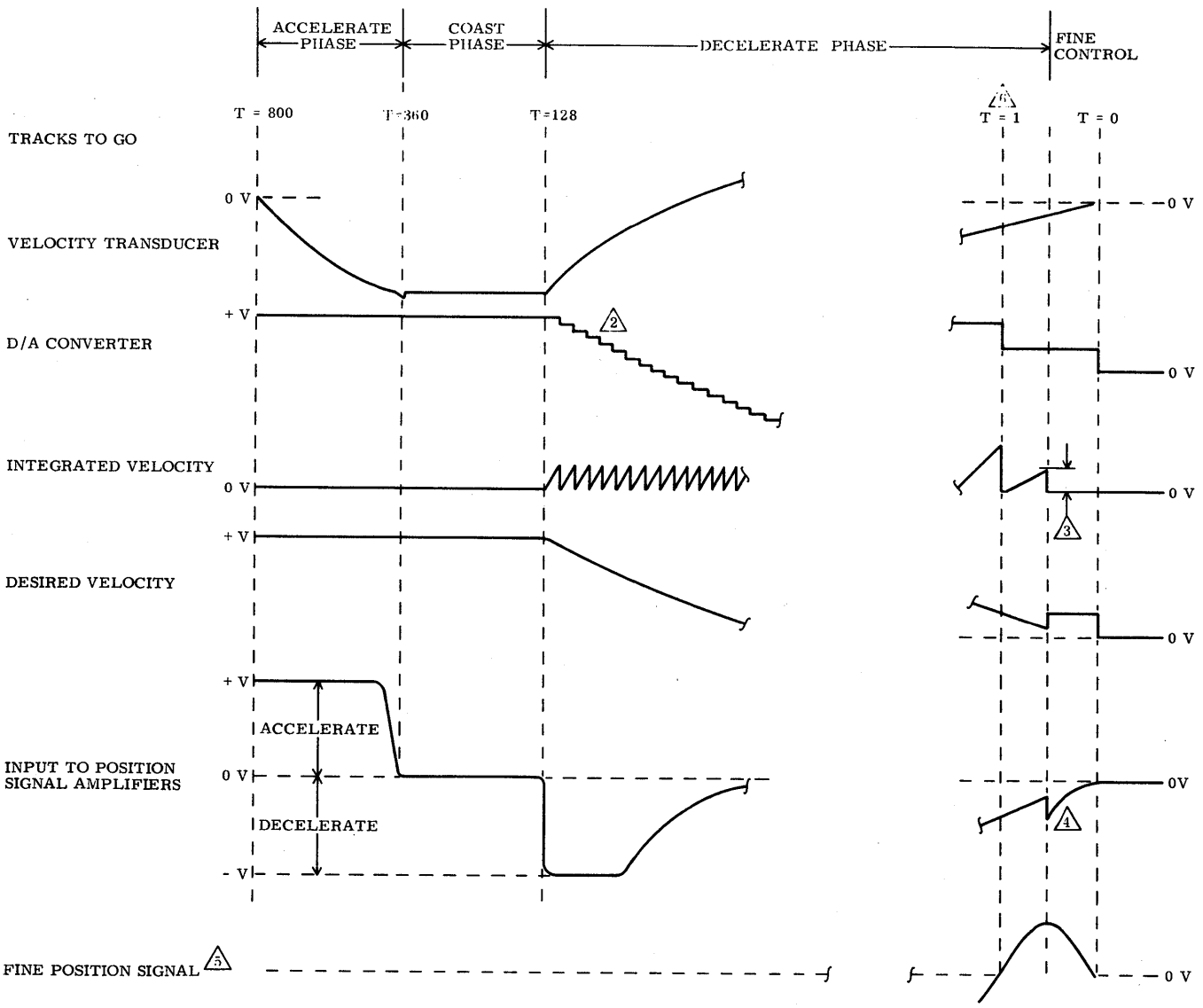
The position signal amplifiers use the output from the coarse position amplifier circuits to produce current for the voice coil. This current controls carriage motion.

The Coarse control portion of a typical direct seek can be divided into three phases:

- Accelerate Phase - Voice coil receives maximum current and carriage accelerates from zero to maximum velocity.
- Coast Phase - Carriage is at maximum velocity and coasts along under its own inertia.
- Deceleration Phase - Carriage approaches destination and must slow down to avoid overshoot.

It should be noted that it takes about 60 cylinders for the carriage to reach maximum velocity (about 55 in/sec). During shorter seeks, particularly those less than 128 (256) logical cylinders, maximum velocity will not be obtained. In cases where maximum velocity is not reached the primary functions remain the same but the coast phase will not occur (or be very short) and the carriage begins to decelerate sooner.

The following describes how the servo loop operates during a typical direct seek long enough for the drive to obtain maximum velocity. The signals generated are shown in figure 3-30.



NOTES:

1. SIGNALS SHOWN APPLY TO FWD SEEK ABOUT 800 CYL IN LENGTH. ALL POLARITIES EXCEPT D/A CONVERTER ARE OPPOSITE FOR REV SEEKS. TIMING AND AMPLITUDE ARE NOT TO SCALE.
2. OUTPUT DECREASES WITH EACH CYLINDER PULSE.
3. SERVO SYSTEM SWITCHES TO FINE CONTROL WHEN INTEGRATED VELOCITY EXCEEDS 0.9 V.
4. GAIN CHANGE CAUSED BY SWITCH FROM COARSE TO FINE CONTROL. SIGNAL FOR LAST HALF TRACK IS DUE TO FINE POSITION INPUT AND IS SHOWN HERE FOR REFERENCE ONLY.
5. FROM FINE POSITION CONTROL CIRCUITS AND IS SHOWN FOR REFERENCE ONLY.
6. SCALE EXPANDED FOR CLARITY BEYOND T = 1.

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Figure 3-30. Direct Seek Coarse Position Control Signals

The acceleration phase occurs during the first part of the seek. At this time, the carriage is stationary and the output from the coarse gate is due entirely to the Desired Velocity signal with no opposing Velocity signal. Therefore, voice coil current is maximum in the direction necessary to cause maximum carriage acceleration.

As the carriage accelerates a Velocity signal is generated by the velocity feedback circuits. Because this signal opposes the Desired Velocity signal, the resultant signal to the position signal amplifiers is reduced thereby reducing voice coil current. However, Desired Velocity signal is still greater and the carriage continues to accelerate.

Eventually carriage speed increases to the point where the Velocity signal equals the Desired Velocity signal and the two signals cancel one another. This causes the positioning signal from the coarse gate, and therefore the voice coil current, to drop to zero. The carriage now coasts along at maximum velocity of about 55 in/sec.

As the carriage coasts, friction losses and back EMF of the moving voice coil tend to slow it down. However, when this occurs the velocity signal becomes less than the Desired Velocity signal (which is still maximum) thus causing enough voice coil current to speed up the carriage until the two signals cancel again.

This continues as long as the Desired Velocity signal remains at its maximum value, which is until less than 128 (256) cylinders remain in the seek. Beyond this point, the carriage starts to decelerate.

When less than 128 (256) cylinders remain, the D/A Converter starts to step down thus causing the Desired Velocity signal to decrease. When Desired Velocity is less than Velocity, current is applied to the voice coil in the reverse direction causing the carriage to slow down until the Velocity signal is again equal to Desired Velocity. The carriage now coasts under its own inertia until the D/A Converter steps down again.

This process continues and the carriage slows down as the destination cylinder is approached. When the heads are within one half track of the destination, the servo system switches to fine control.

Direct Seek Fine Control

General

The last half track of a direct seek is controlled by the fine position control circuits (refer to figure 3-31). These circuits generate the signal used to bring the drive over the desired cylinder and to keep it tracking properly over this cylinder.

In addition to this, these circuits also control coarse to fine switching and generate the On Cylinder signal. The following paragraphs describe all of these functions and is divided into these areas:

- Coarse to fine Switching
- Fine Position Signal Generation and Basic Loop Operation
- On Cylinder Detection
- Track Following

Figure 3-31 shows the fine position control circuits and figure 3-32 shows timing during fine position control.

Coarse to Fine Switching

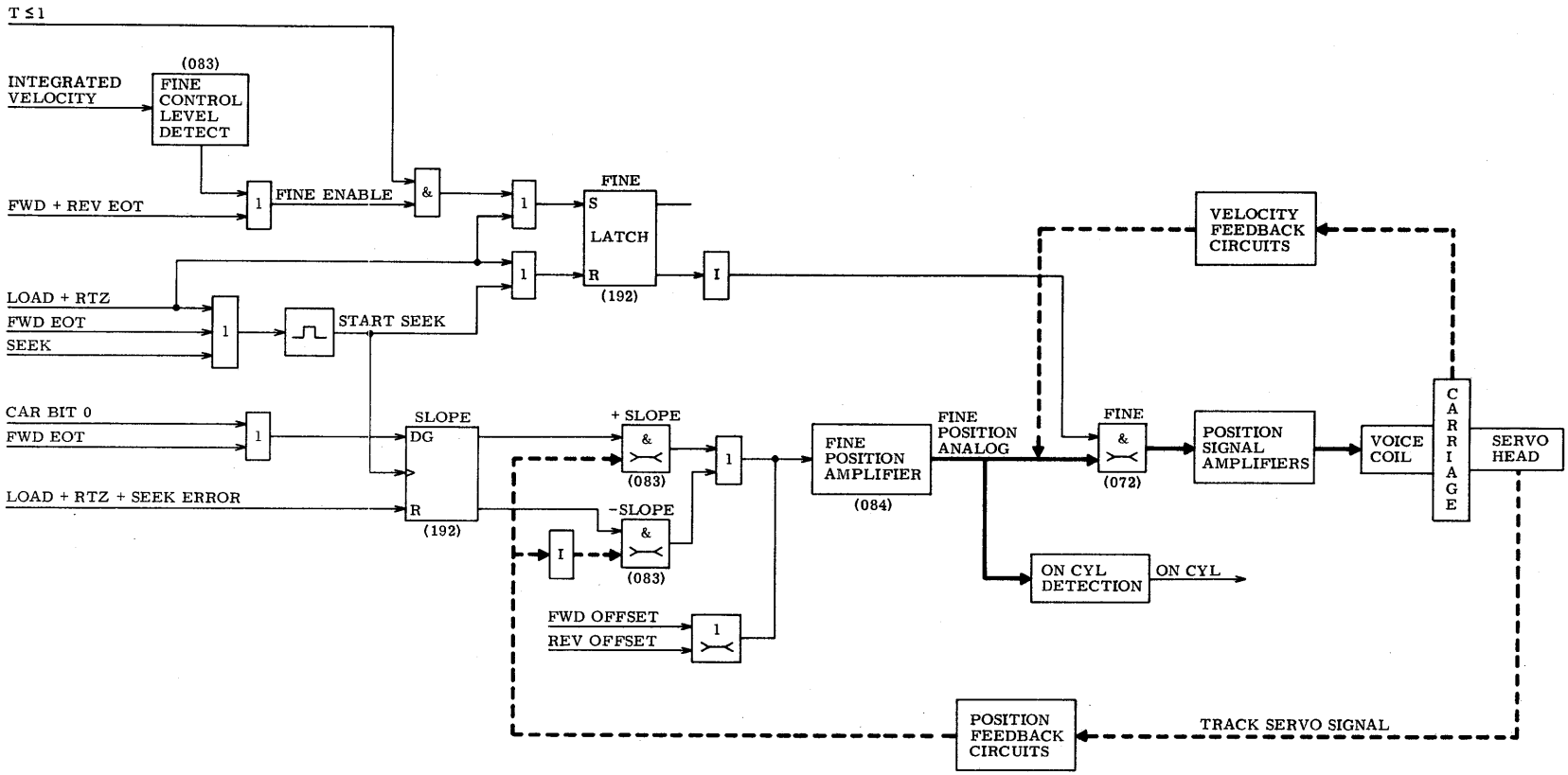
Coarse to fine switching is controlled by the Fine latch. When this latch is set, the Fine gate is enabled and the output of the fine position control circuits is gated to the position signal amplifiers. Whenever this latch is cleared, the coarse gate is enabled thus putting the servo system in coarse control.

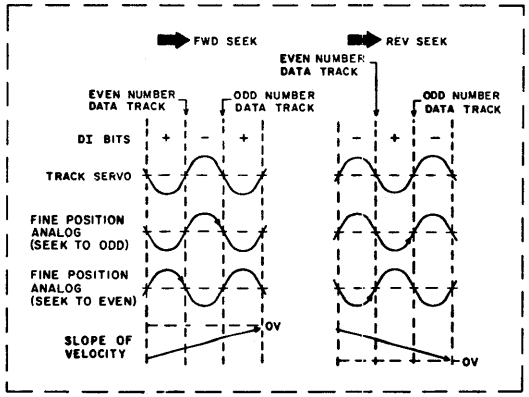
During a direct seek, the Fine latch is cleared at the start of the seek and remains clear until the heads are within one half cylinder of destination.

The coarse to fine sequence starts when the Difference counter indicates one cylinder to go. At this time the T≤1 signal goes active indicating the last cylinder is being crossed.

The one half cylinder point is sensed by the fine control level detect circuit. The input to this circuit is the Integrated Velocity signal (refer to discussion on Direct Seek Coarse Control) which is set to zero by the same cylinder pulse that decrements the Difference counter to one. When this cylinder pulse drops, the Velocity Integrator output starts to increase again. When it reaches 0.9 V, the heads are about one half cylinder from the centerline of the destination cylinder and this causes the fine control level detect output to go active. This in turn causes the Fine Enable signal to go active. The Fine Enable signal is then ANDed with the T≤1 signal to set the Fine latch.

When the Fine latch sets, the coarse gate is disabled and the Fine gate is enabled thus gating the fine positioning signal to the position signal amplifiers.



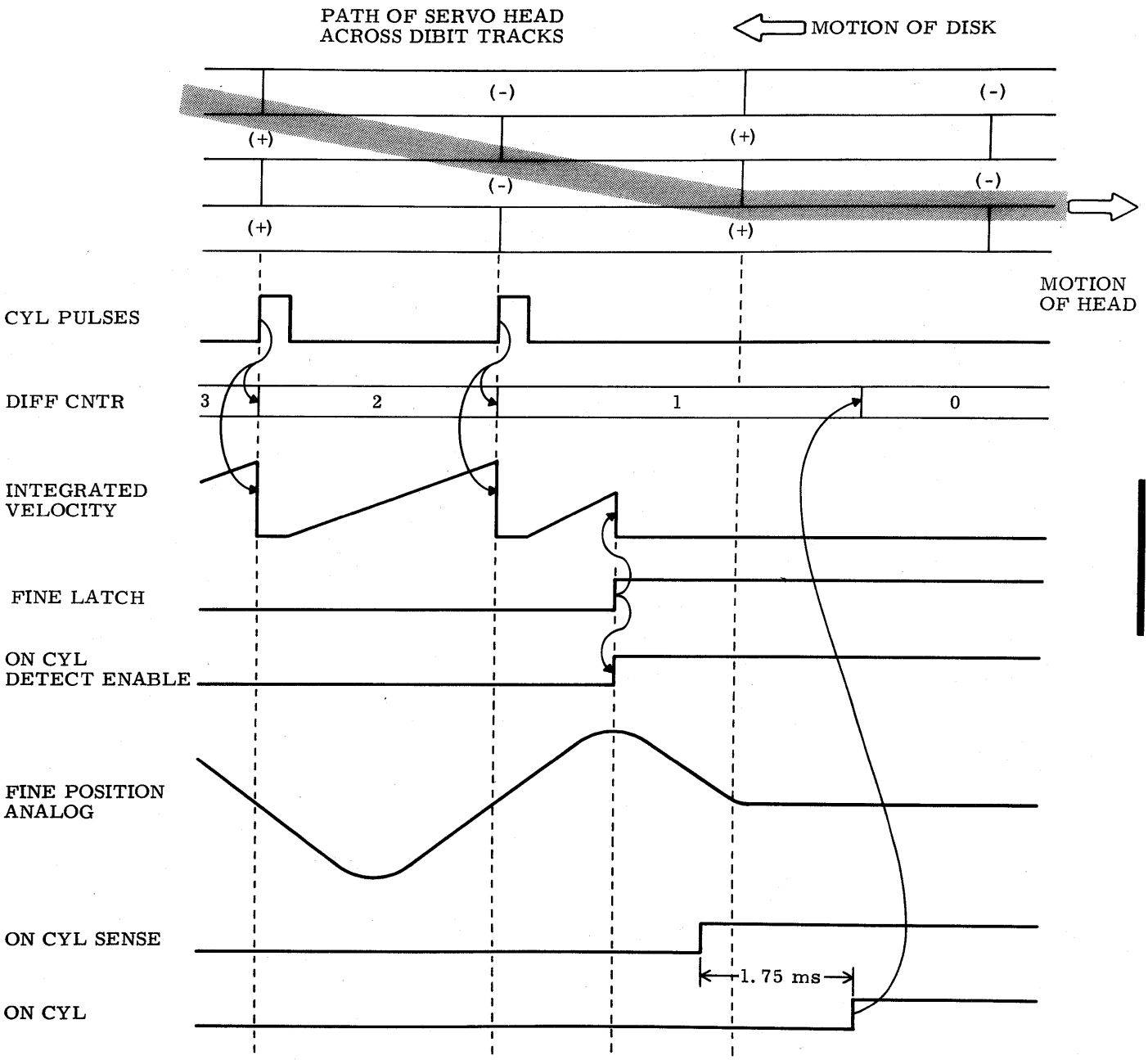


NOTES:

1. ——— POSITION SIGNAL
   - - - FEEDBACK SIGNAL
   ——— CONTROL SIGNAL
2. ASSOCIATED TIMING SHOWN ON FINE POSITION CONTROL TIMING DIAGRAM.

9H60A

Figure 3-31. Fine Position Control Circuits



NOTES:

1. REFER TO FIGURES SHOWING FINE POSITION CONTROL AND ON CYL DETECTION CIRCUITS FOR LOGIC ASSOCIATED WITH THIS TIMING.

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Figure 3-32. Fine Position Control Timing

Fine Position Signal Generation

The fine positioning signal is produced by combining the Fine Position Analog and Velocity signals. The Fine Position Analog signal varies with distance to the destination cylinder centerline and Velocity varies with speed of the carriage.

The Fine Position Analog signal is derived from the Track servo signal which is received from the position feedback circuits and provides the position feedback during fine control. The amplitude of the Fine Position Analog and Track Servo signals are directly proportional and as the heads approach the centerline of the destination cylinder both signals decrease from maximum to zero.

The Fine Position Analog signal is summed with the Velocity signal to provide speed control. These signals are of opposite polarity with the polarity of Fine Position Analog such as to cause an increase in carriage speed and the polarity of Velocity such as to cause a decrease.

Because during this phase, the carriage must decelerate, the amplitude of the Velocity signal will normally be greater than that of Fine Position Analog. How much greater depends on the speed of the carriage.

If the carriage starts moving too fast, the Velocity signal will increase and therefore exceed Fine Position Analog by a greater amount. This results in greater deceleration. However, if the carriage decelerates too quickly the Velocity signal decreases and approaches that of Fine Position Analog resulting in less deceleration.

Ideal speed is obtained when the two signals are nearly equal and the resultant signal produces a voice coil current that brings the heads to rest at the destination cylinder without overshoot or oscillation.

Because of the polarities of the Velocity and Fine Position Analog signals must be opposite, it is sometimes necessary to invert the Track Servo signal to obtain the proper polarity of Fine Position Analog. This is the case, because although the Velocity signal always has the same polarity (negative for forward seeks, positive for reverse seeks), the polarity of the Track Servo signal depends on whether it is approaching an odd or even numbered physical cylinder. On forward seeks, the Track Servo signal decreases from a maximum positive to zero when approaching an odd cylinder and increases from a maximum negative to zero when approaching an even cylinder. The opposite is true for reverse seeks. Refer to discussion on position feedback for more information on Track Servo signal generation.

What polarity the Fine Position Analog signal, which is derived from the Track Servo signal, will have is controlled by the Slope FF. This FF is either set or cleared at the start of the seek.

If the seek is to an odd numbered cylinder, the FF is set and the Fine Position Analog and Track Servo signals are of the same polarity. If the seek is to an even numbered cylinder the FF is cleared and the signals are of opposite polarities. The phase relationships between the Track Servo and Fine Position Analog signals are shown on figure 3-32.

When the heads are centered over and tracking over the destination cylinder, both the Fine Position Analog and Velocity signals are zero. When this occurs the heads are considered to be on cylinder. This condition is sensed by the on cylinder detection circuits.

On Cylinder Detection

On Cylinder detection is enabled when the servo system goes into fine control (Fine latch sets). At this time, the on cylinder detection circuits (refer to figure 3-33) start to monitor the Fine Position Analog signal. When this signal is small enough to indicate the heads are approximately over the servo track (if the destination cylinder), goes active the On Cylinder Sense signal. The On Cylinder Sense signal triggers the 1.75 ms On Cylinder Delay which allows the heads time to settle out over the servo track. When the delay times out the On Cylinder FF sets.

The On Cylinder signal causes the Seek End line to the controller to go active and is also used to perform various functions within the drive logic.

Track Following

Even after the on cylinder position is obtained it is necessary to keep the servo system under control of the fine position control circuits. This is necessary to ensure that the heads do not drift far enough off the track centerline to cause errors during a read or write operation.

If the heads should drift off centerline, the Track Servo signal will increase or decrease slightly from zero (depending on the direction of the drift) and this is translated into the Fine Position Analog signal. The polarity of the Fine Position Analog is such that the position signal amplifier generates the proper voice coil current to drive the heads back to the track centerline.

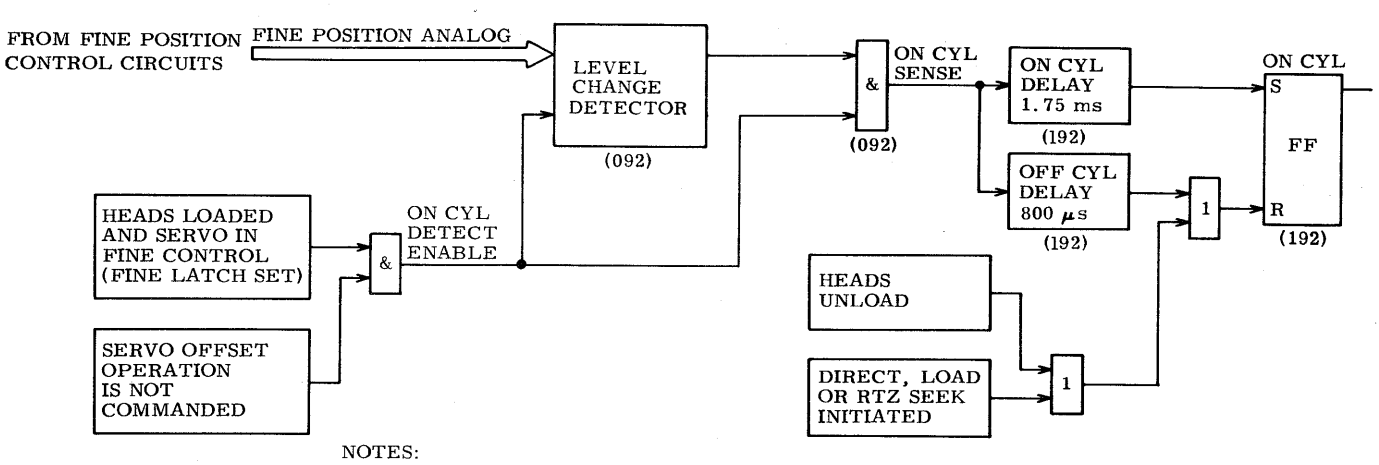


Figure 3-33. On Cylinder Detection Logic

If the heads drift sufficiently to cause a Fine Position Analog signal greater than 0.4 V for more than 800 µs, the Off Cylinder Delay times out causing the On Cylinder FF to clear.

This is turn causes a seek error to be generated (refer to discussion on Seek End and Seek Error Detection).

It is possible for the controller to command the drive to move the heads slightly off the track centerline if it is necessary for data recovery. This is done via offset command (Tag 3) and either Bus bit 2 or Bus bit 3 active.

If Bus bit 2 (Servo Offset Plus) is active, the heads move about 250 µin towards the spindle. If Bus bit 3 (Servo Offset minus) is active, the heads move about 250 µin away from the spindle.

In both cases, the bias signal is summed with the normal position signal at the input to the fine position amplifier (refer to figure 3-31). This causes the carriage to move until the Track Servo signal, which is of a polarity to move the heads back to the centerline, equals and cancels the bias signal.

LOAD SEEK POSITION CONTROL

General

During a load seek, the heads are moved from the fully retracted position and positioned out over the disk pack at cylinder 000.

The load seek must be successfully completed before the drive can respond to a read, write or seek command from the controller. When the sequence is completed, the Seek End line goes true and the Ready indicator on the drives control panel lights.

The seek is initiated at the same time as the power on sequence by pressing the START switch. However, the actual positioning does not begin until after the power on sequence is complete (disk pack is up to speed). The positioning is divided into coarse and fine modes which are explained in the following. The power on sequence is described in the Power System Discussion.

Load Seek Coarse Control

The servo system is under coarse control from the time the load is initiated until the reverse end of travel zone (refer to discussion on Servo Disk Information) is detected. The circuits involved are shown on figure 3-34 and the timing is on figure 3-35.

The load seek coarse control sequence begins when the power on sequence has been completed and the disk has reached 3000 revolutions per minute. At this time, the load latch sets and enables the Load Gate. The Load gate combines a bias signal with the Velocity signal and applies the resultant signal to the position signal amplifiers. This causes the carriage to move forward at about seven inches per second.

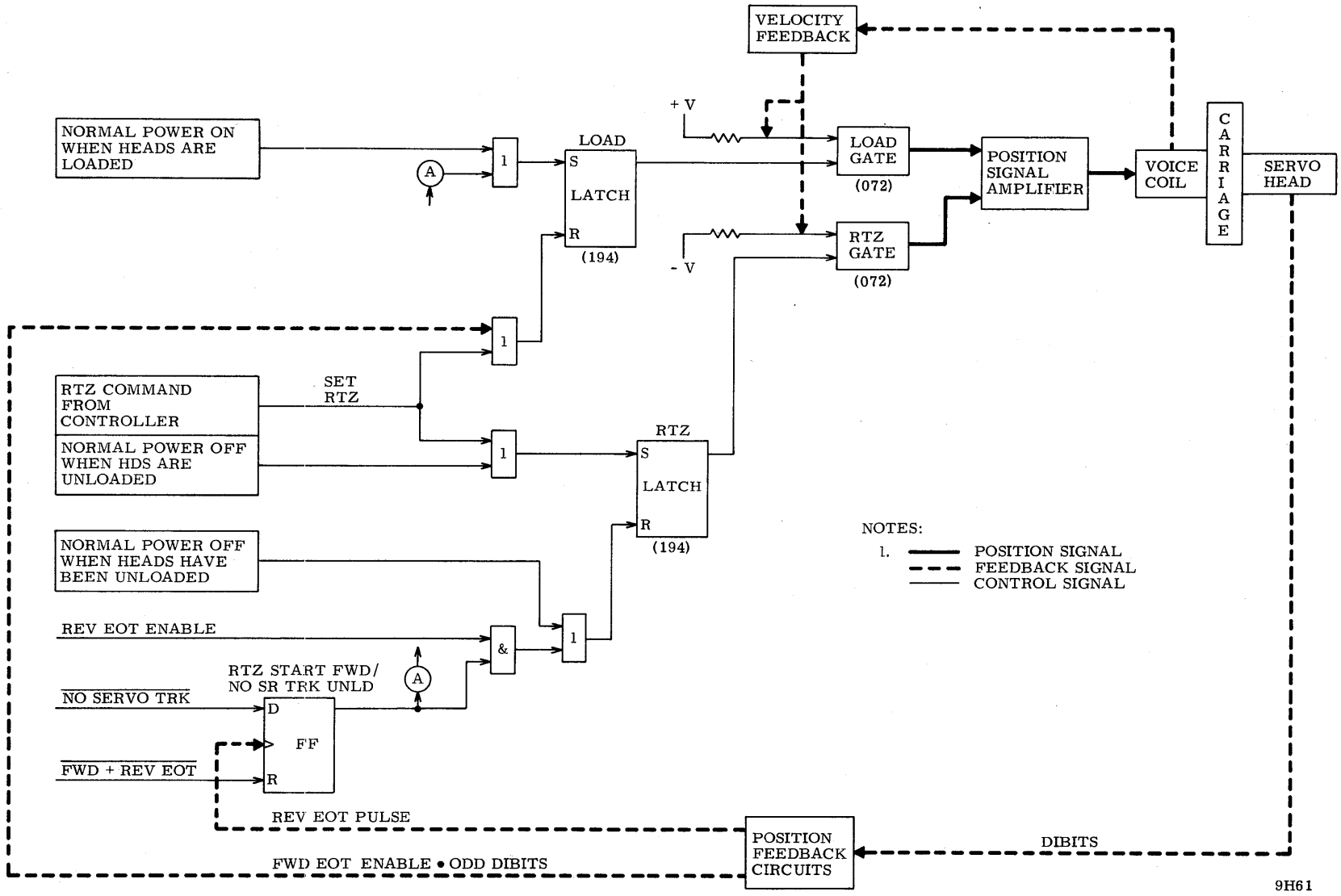


Figure 3-34. RTZ/Load/Unload Coarse Position Control Loop

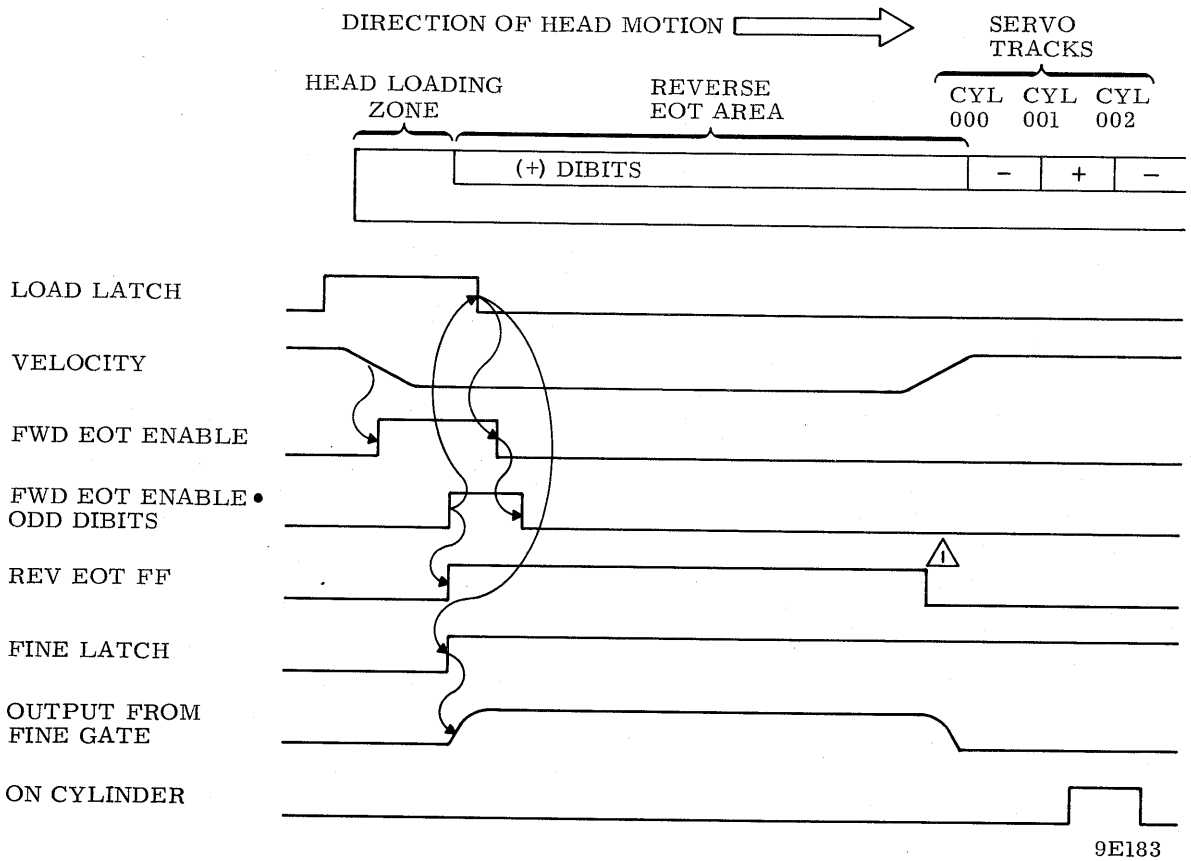


Figure 3-35. Load Seek Timing

As the heads move forward from the retracted position, the heads loaded switch transfers to the heads loaded position thus enabling the dibits sense logic (refer to discussion on Dibits Sensing). The drive now starts searching for the positive-odd dibits indicating the reverse end of travel area.

Because the heads are moving in a forward direction and the polarity of the Velocity signal is such as to cause the Forward EOT Enable signal to go active (refer to discussion on End of Travel Detection), when positive-odd dibits are detected, the Forward EOT·Odd Dibits signal also goes active. This causes the Load latch to clear thus disabling the Load gate. It also sets the Reverse EOT FF which in turn causes the Fine latch to set thus enabling the Fine gate. The carriage is now controlled by the fine position control circuits (refer to figure 3-35).

If for any reason the dibits signals are not detected within 350 ms after the Load latch is set, the RTZ latch sets and the heads unload to the fully retracted position. This also causes the Fault latch to set and FAULT indicator to light.

Pressing the FAULT switch (extinguishing the indicator) clears the fault latch and initiates another load seek. However, the heads will unload again thus lighting the FAULT indicator and setting the Fault latch if dibits are not detected within 350 ms.

Load Seek Fine Control

The fine positioning signal used during load seek fine control is the same as is used during direct seeks and the component of this signal that varies with distance to the destination is also derived from the Track Servo signal.

Therefore, because the heads are over the reverse end of travel and all positive-odd dibits are being detected, the Track Servo signal is at its maximum negative value and the Fine Position Analog signal (derived from it) is at its maximum positive value.

This value is such that a constant forward motion is obtained at the proper speed.

When the heads approach cylinder 000, negative-even dibits are detected. This causes the Track Servo signal, and therefore the Fine Position Analog signal to decrease towards zero. The carriage now decelerates and servos onto the on cylinder position. On Cylinder detection and track following are the same as discussed for direct seeks.

RETURN TO ZERO SEEK POSITION CONTROL

The return to zero seek (RTZS) function is an alternate means for the controller to command the drive to seek to cylinder 000 without issuing a direct seek command. This might be necessary in cases where a seek error has occurred.

The controller initiates a return to zero seek via a tag 3 (Control Select) accompanied by Bus bit 6 (RTZ). When the drive receives this command, the RTZ latch sets and enables the RTZ gate (refer to figure 3-34). The RTZ gate, like the Load gate, combines bias signal with the Velocity signal and applies the result to the position signal amplifiers. However, in this case the resultant signal causes the carriage to move in reverse at about seven inches per second.

When the carriage moves past cylinder 000, it enters the reverse end of travel area and no move cylinder pulses are generated. The loss of cylinder pulses allows the EOT Velocity Integrator output (which is normally reset to zero by cylinder pulses) to exceed -1.4 V. This causes the Reverse EOT Enable signal to go true and set the Reverse EOT FF (refer to discussion on End of Travel Detection). Setting the Reverse EOT FF causes the Velocity Integrator to reset but the carriage continues moving in reverse and the integrator output starts to rise again.

After an additional reverse motion of about two tracks, the Velocity Integrator output again exceeds -1.4 V. This time the Reverse EOT Enable signal enables the Set Load signal which sets the Load latch and clears the RTZ latch.

Setting the Load latch causes the carriage to reverse direction and start back towards cylinder 000. During the remainder of the operation, the drive seeks to cylinder 000 as during a load sequence (refer to discussion on Load Seek Position Control).

Figure 3-36 shows the timing for the entire return to zero seek function.

UNLOAD SEEK POSITION CONTROL

The heads are normally unloaded at the start of the power off sequence (refer to discussion on Power System). This is necessary to make certain the heads are not over the disk when it slows down as this would cause head crash. The heads are also unloaded during certain error conditions (refer to discussions on Emergency Retract and Seek End and Seek Error Detection). The following describes the heads unload sequence occurring during a normal power off.

The sequence is initiated when the START switch is pressed and the logic circuits generate a signal that sets the RTZ latch. Setting the RTZ latch enables the RTZ gate and the carriage starts retracting at seven inches per second. The action is similar to an RTZ except that the EOT detection circuit is disabled so that the Reverse EOT Enable signal never goes active. Therefore, the RTZ latch remains set and motion continues until the heads unload.

When the heads loaded switch transfers, indicating the heads are unloaded, the RTZ latch is cleared. This disables the current to the voice coil and the carriage stops driving in reverse. However, the power off sequence continues and this is described in the discussions on the Power System.

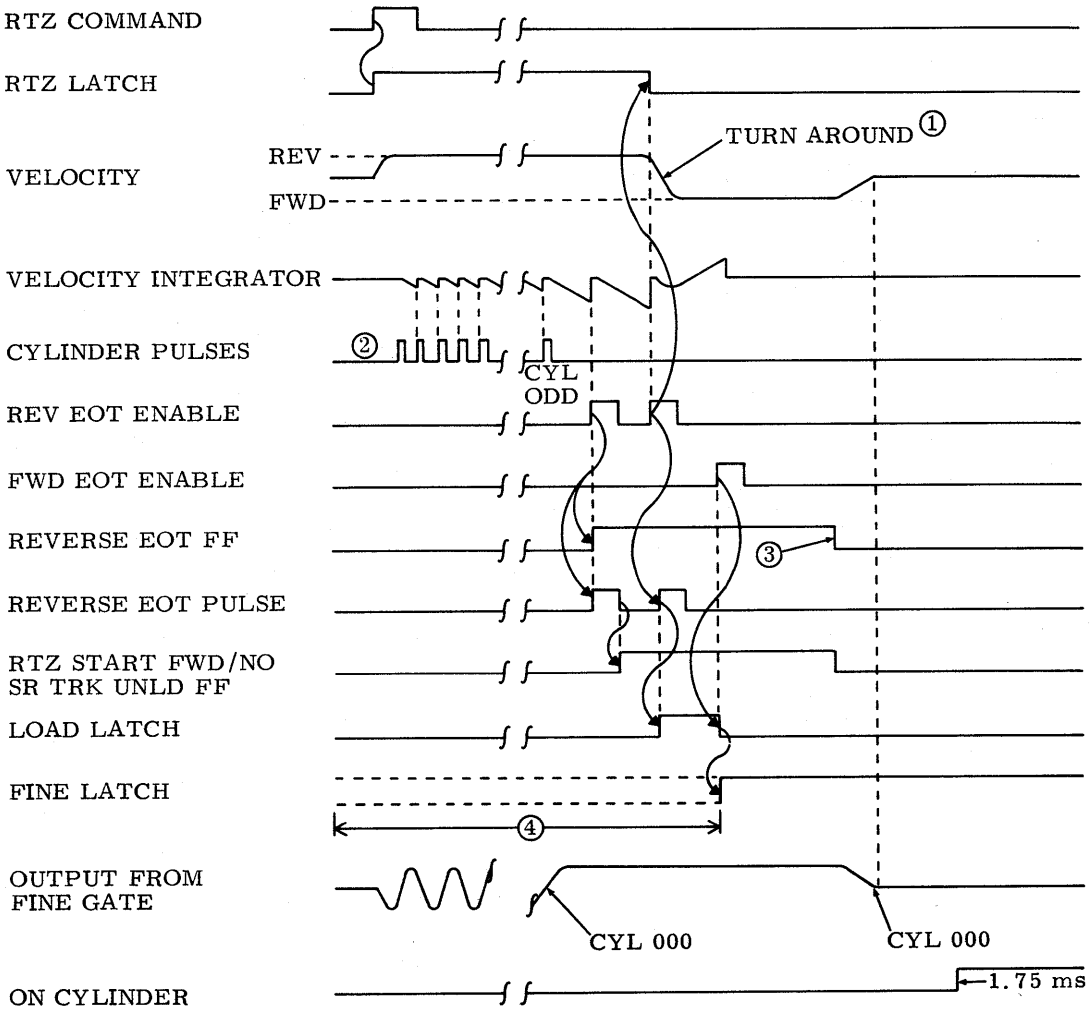
SEEK END AND ERROR DETECTION

General

The Seek End line goes true at the end of every seek operation and indicates that either the seek has been successfully completed and the heads are over the desired logical cylinder or that a seek error has occurred.

Successful completion is indicated when the drives On Cylinder signal is active and the Seek Error latch is not set. An unsuccessful seek is indicated whenever the Seek Error latch is set (either with or without On Cylinder). This occurs if the drive cannot complete the seek or if an error occurs during the seek operation. If the seek error latch is set, the drive cannot perform another seek until the latch is cleared. This is done via an RTZ command (Tag 3, Bus Bit 6).

The controller determines whether the seek was successful or unsuccessful by monitoring the On Cylinder and Seek Error lines. When On Cylinder is true it indicates heads are positioned over a cylinder and when Seek Error is ture it indicates a seek error has occurred.



NOTES:

① CLEARING RTZ AND SETTING LOAD LATCH CAUSES CARRIAGE TO REVERSE DIRECTION AND MOVE FWD.

② CYLINDER PULSES RESET VELOCITY INTEGRATOR.

③ REV EOT FF CLEARED WHEN NEGATIVE-EVEN DIBITS ARE DETECTED AS HEADS APPROACH 000.

④ FINE LATCH IS JAMMED (BOTH INPUTS HIGH) THUS DISABLING BOTH COARSE AND FINE GATES AS LONG AS EITHER LOAD OR RTZ LATCH IS SET.

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Figure 3-36. Return to Zero Seek Timing

The conditions interpreted by the drive as seek error are described in the following paragraphs. The basic logic is shown on figure 3-37.

Timeout Error

If the drive does not generate On Cylinder within 500 ms of the start of the seek the Seek Error latch sets.

Setting the Seek Error latch causes the Difference counter to be reset to zero and the Slope FF to be cleared. This in turn causes the drive to seek to the nearest even numbered cylinder and generate On Cylinder.

Maximum Address Fault

If the controller commands the drive to seek to a cylinder address greater than 410 (822) the Seek Error latch is set and the drive will not perform the seek.

End of Travel Errors

General

Whenever a direct seek is being performed and the heads are positioned outside of the normal data area, an end of travel condition exists and the Seek Error latch sets.

It is possible for the heads to be positioned over either the forward or reverse end of travel area and both of these sequences are described in the following (also refer to discussion on End of Travel Detection).

Forward End of Travel

When the heads move past cylinder 410 (822) they enter the forward end of travel area (inner guard band).

Because cylinder pulses are not generated as the heads move over this area, the EOT Velocity Integrator output is able to exceed +1.35 V (refer to discussion on End of Travel Detection). This causes the Forward EOT Enable signal to go active and set the Forward EOT FF.

This in turn causes the following:

- Seek Error latch sets thus causing a Seek End to the controller.
- Seek FF (set at start of seek) clears.
- Difference counter set to 000 (T=0).
- Fine Enable signal goes active.
- Slope FF is cleared to indicate a seek to an even numbered cylinder.

When the Fine Enable signal is active and the Difference counter equals zero the Fine latch is enabled thus enabling the Fine gate.

Because the heads are over the inner guard band and all negarive-even dibits are being detected, the Track Servo signal is at its

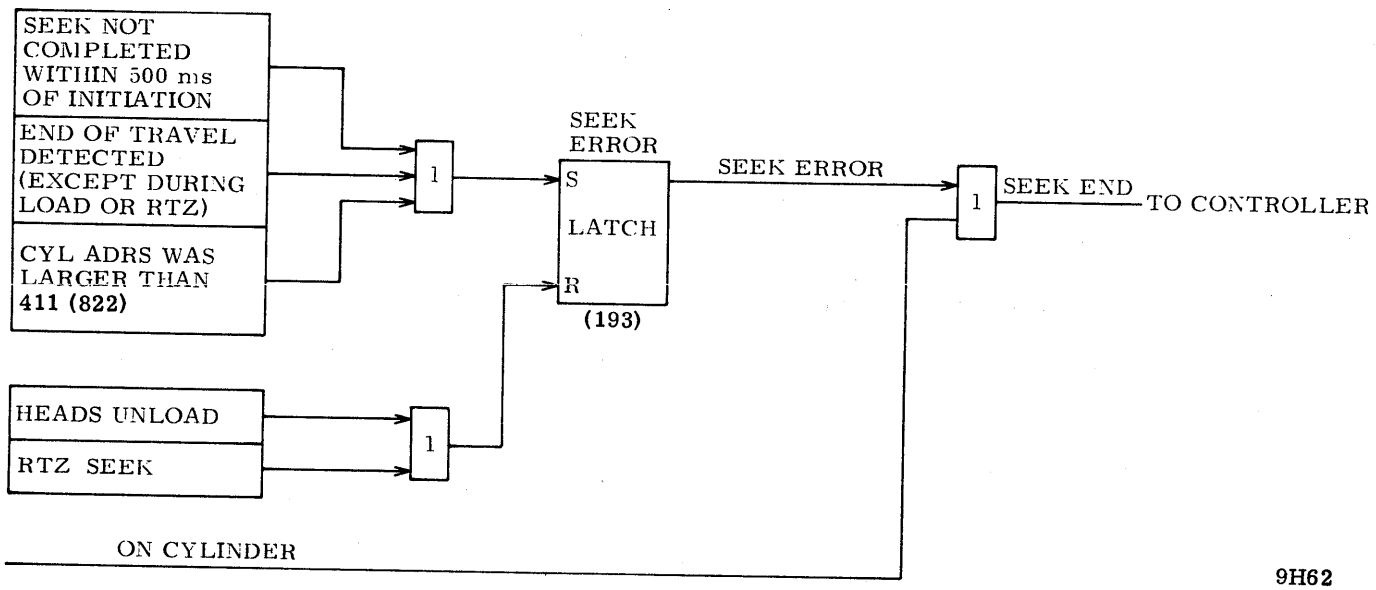


Figure 3-37. Seek End and Seek Error Detection

maximum positive value. This results in a Fine Position Analog signal that is at its maximum negative value and the carriage moves in reverse towards cylinder 410 (822).

When cylinder 410 (822) is approached, positive-odd dibits are detected, the Track Servo and Fine Position Analog signals decrease, and the carriage decelerates until it is on cylinder at physical cylinder 410 (822).

The heads remain at this location until the drive receives an RTZ command.

Reverse End of Travel

A Reverse End of Travel condition indicates the heads have moved in reverse past cylinder 000 and into the outer guard band.

When this occurs, the Reverse EOT FF sets and initiates a load sequence that returns the heads to cylinder 000. The heads remain at this location until the drive receives an RTZ command which clears the Seek Error latch.

MACHINE CLOCK

GENERAL

The machine clock circuits generate the clock signals necessary for drive operation. These circuits are divided into two areas (1) Servo Clock Multiplier and (2) Write Clock Multiplier. These are both explained in the following discussions.

SERVO CLOCK MULTIPLIER

The servo clock multiplier circuits generate clock pulses used by the sector detection, Index detection and the Read PLO circuits. It also generates the 9.67 MHz Servo Clock signal that is sent to the controller.

The main element in the servo clock multiplier circuit is the phase lock loop. This loop consists of a phase and frequency detector, error amplifier, voltage controlled oscillator and a divide by 12 circuit. The function of the loop is to adjust itself until its output is identical in phase and frequency to its output.

The input to the loop consists of the dibit signals from the track servo circuit. The nominal frequency of these signals is 806 kHz; however, their actual frequency is a function of, and varies directly with disk pack speed. This means that the output of the loop will also vary with disk pack speed.

The phase and frequency detection circuit makes the comparison between the input dibits and the output of the loop.

The input dibits are applied via two retriggerable multivibrators. One of these multivibrators provides a 750 ns (approximate) output pulse which is then fed through a pulse forming circuit to provide a 25 ns input pulse for the phase and frequency detector. These pulses vary at the dibit frequency. The other multivibrator has a 1.6 µs output which is used to enable the feedback pulses from the loop output to the input of the phase and frequence detector. The 1.6 µs pulse is longer than the period of the nominal dibit frequency (806 KHz); therefore, the feedback pulses are continuously gated as long as dibits are present.

The outputs from the detector are fixed amplitude pulses which are a function of the time (or phase) difference between the positive going edge of the two inputs (refer to figure 3-38).

These outputs are applied to the error amplifier which integrates them and generates a voltage proportional to the phase difference between them. This voltage is used as a control voltage for the Voltage controlled oscillator.

The control voltage causes the VCO frequency to vary in the direction necessary to eliminate the phase or frequency difference between the input and output fo the loop. The VCO output is then divided by 12, by the divide by 12 circuit, and fed back to the loop input.

When the VCO output is 9.67 MHz, the feedback provided by the divide by 12 circuit will be 806 KHz and the loop will be synchronized.

Both the 9.67 MHz and 806 KHz signals are divided by two thus producing 4.84 MHz and 403 KHz signals. All four of these frequencies are used by the drive as shown on figure 3-38.

WRITE CLOCK FREQUENCY MULTIPLIER

The write clock frequency multiplier circuit (refer to figure 3-39) generates the 19.34 MHz and 9.67 kHz signals used during write operations.

This circuit consists mainly of a phase lock loop and operates essentially the same as the servo clock multiplier. However, the input to the write clock multiplier is the 9.67 MHz Write Clock signals from the controller. The phase lock loop synchronizes to these signals and provides the 19.34 MHz outputs. These outputs are used by the NRZ to MFM converter and Write Compensation circuits during write operations.

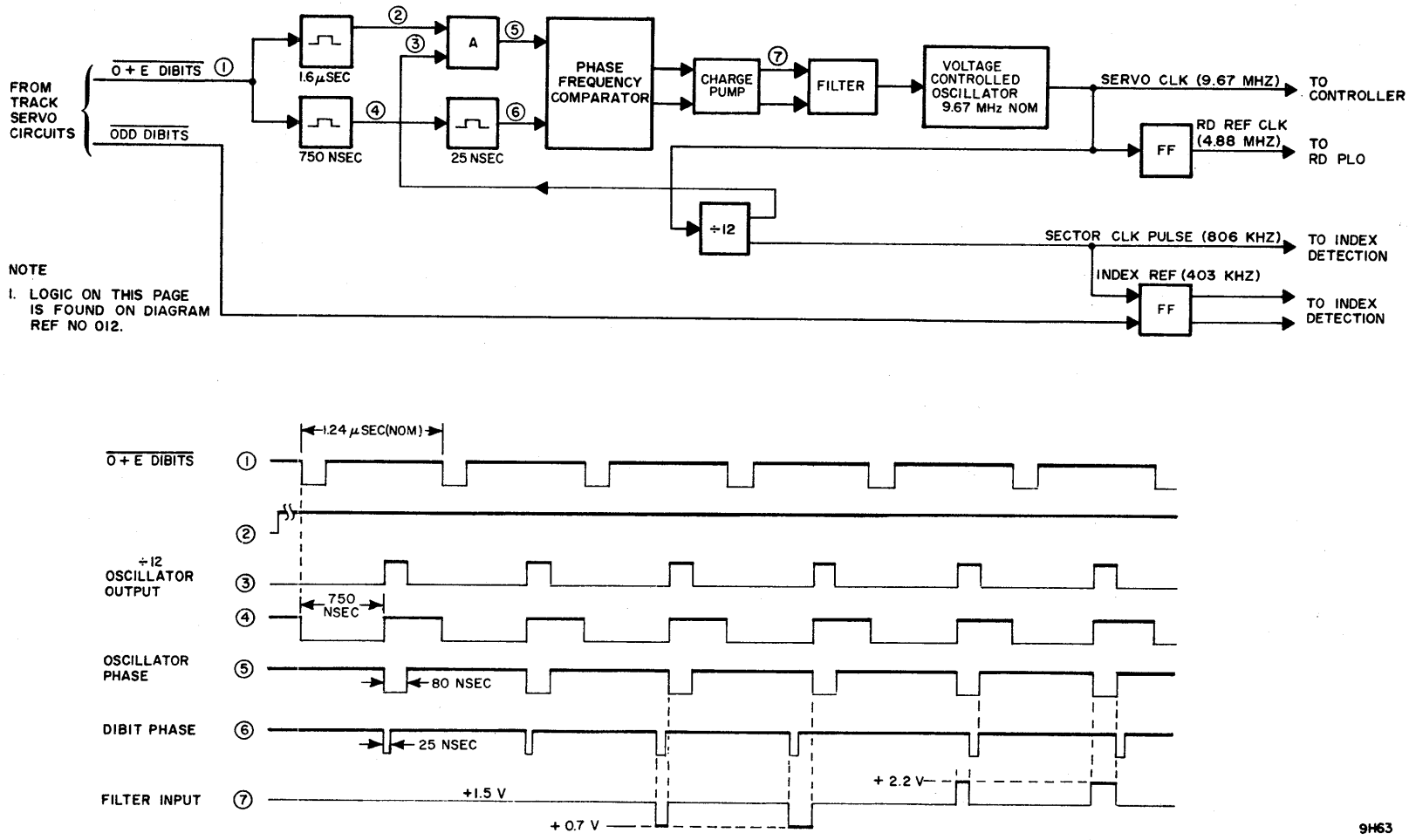


Figure 3-38. Servo Clock Multiplier

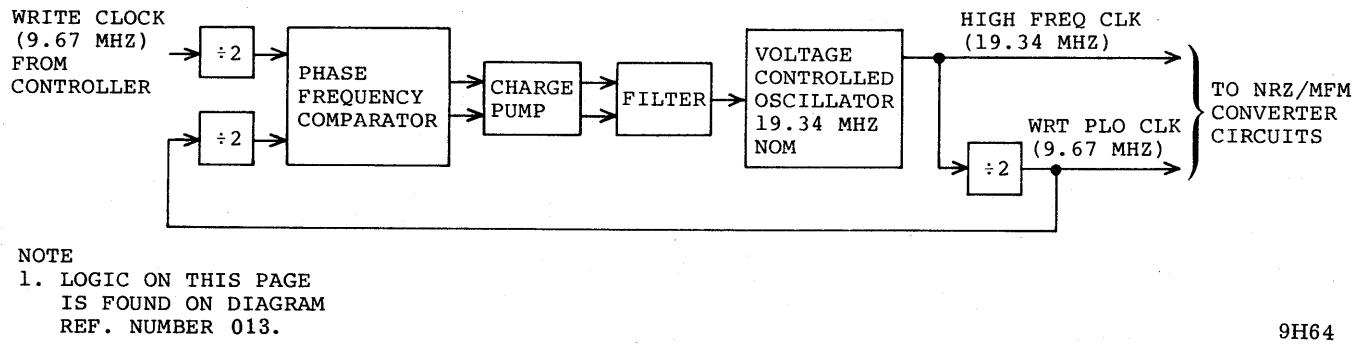


Figure 3-39. Write Clock Multiplier

HEAD OPERATION AND SELECTION

GENERAL

Information is recorded on and read from the disk by the read-write heads (refer to figure 3-40). The drive has five read-write heads, one for each data recording surface on the disk pack. For this reason, before a read or write operation can be performed, the controller must command the drive to select the head located over the disk surface where the data is to be read or written.

The following discusses how the heads read and write the data and also how the desired head is selected.

HEAD FUNCTIONAL DESCRIPTION

Data is written by passing a current through a read/write coil within the selected head. This generates a flux field across the gap in the head (figure 3-41). The flux field magnetizes the iron oxide particles bound to the disk surface. Each particle is then the equivalent of a miniature bar magnet with a north pole and a south pole. The writing process orients the poles to permanently store the direction of the flux field as the oxide passes beneath the head. The direction of the flux field is a function of Write current polarity while its amplitude depends on the amount of current: the greater the current, the more oxide particles that are affected.

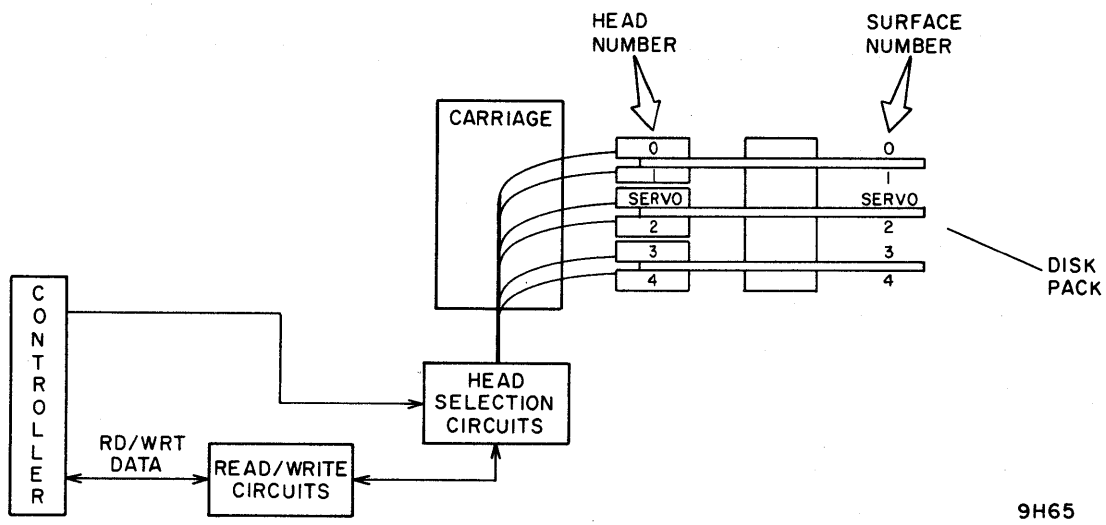


Figure 3-40. Read-Write Heads

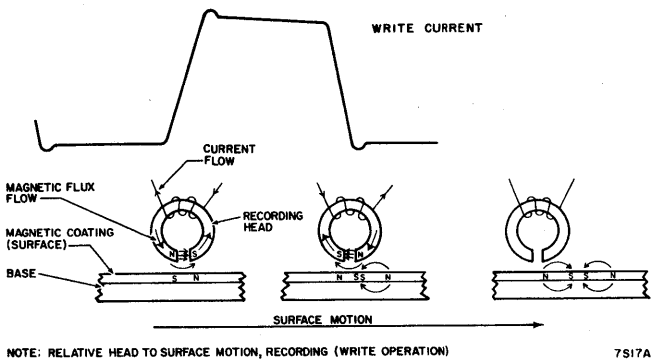


Figure 3-41. Writing Data

Information (data) is written by reversing the current through the head. This change in current polarity switches the direction of the flux field across the gap. The flux change defines a data bit.

Erasing old data is accomplished by writing over any data which may already be on the disk. The write current is zoned in four current zones to ensure proper saturation level for best head resolution (refer to discussion on Write Current Control). The write current is maximum in the outer tracks and progressively decreased for inner tracks.

During the read operation, disk motion beneath the head causes the stored flux to induce a voltage in the head windings (refer to figure 3-42). This voltage is analyzed by the read circuit to define the data recorded on the disk. Each flux reversal (caused by a current polarity change while writing) generates a readback voltage pulse. Each pulse, in turn, represents a data bit.

HEAD SELECTION

A head must be selected before a read or write operation can be performed. Head selection starts when the controller sends the drive a Head Select tag (tag 2) and a head address on the bus lines.

The Head Select tag gates the address into the Head Address register. This address is then decoded to a head enable signal. This signal then enables the head current drive associated with the addressed head and allows the head to conduct as shown on figure 3-43.

If more than one head is selected, a fault is indicated (refer to discussion on Fault and Error Conditions).

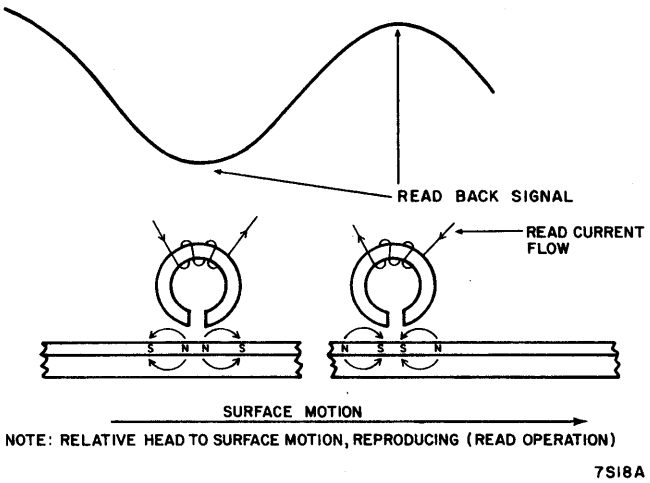


Figure 3-42. Reading Data

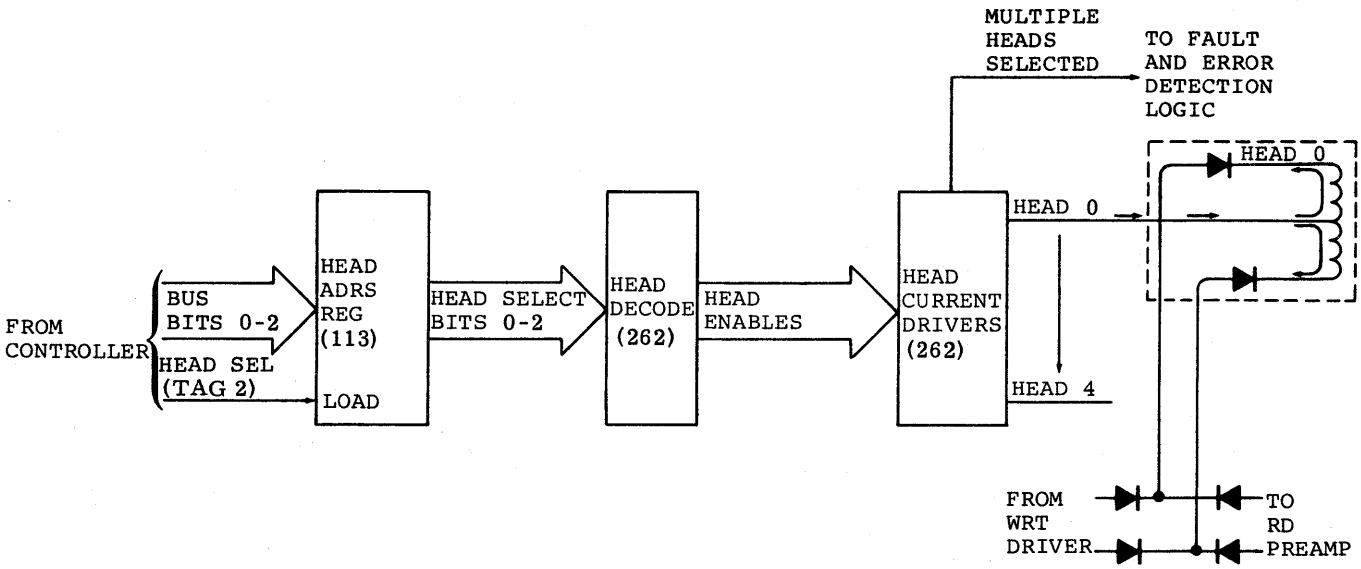


Figure 3-43. Head Select Circuits

TRACK ORIENTATION

GENERAL

After finding the proper cylinder and selecting a head, the controller still may not read or write data until it determines the head is over that part of the data track where the data is to be read or written. The controller accomplishes this by using the Index and Sector signals which are generated by the drive. How the drive generates these signals is explained in the following.

INDEX DETECTION

Each track on the servo disk contains a pattern of missing dibits referred to as the index pattern. The drives Index Detection circuits use this pattern to generate a 2.5 µs Index signal. The purpose of the Index signal is to indicate both to the drive and the controller, the logical beginning of a track.

The Index Detection circuit consists of the following three parts:

- Missing Dibits One Shot - Detects the missing dibits in the index pattern.
- Index Shift Register - Accumulates the dibit pattern so that it can be compared with the pattern occurring during index.
- Index Decoder - Compares the contents of the Index Shift register with the index pattern and generates an output signal when index is detected.

The input to the Index detection circuit is the Not Odd or Even Dibits signal. This signal is used to trigger the Missing Dibits one shot. This one shot is retriggerable and does not time out as long as dibits are present. The output of this one shot is loaded into the Index Shift register.

When the one shot is in a triggered state, the 403 KHz signals load ones into the Shift register. However, if a dibit is missed the dibits detect one shot times out and a zero loads into the register.

The content of the Index Shift register is being continuously compared to the Index pattern by the Index Decoder. When the pattern of missing dibits indicating Index occurs, the Index Shift register is loaded as shown by the timing in figure 3-44, and the Index Decoder circuit generates an Index signal.

The Index signal is sent to the controller and is also used to reset the drives sector detection circuitry.

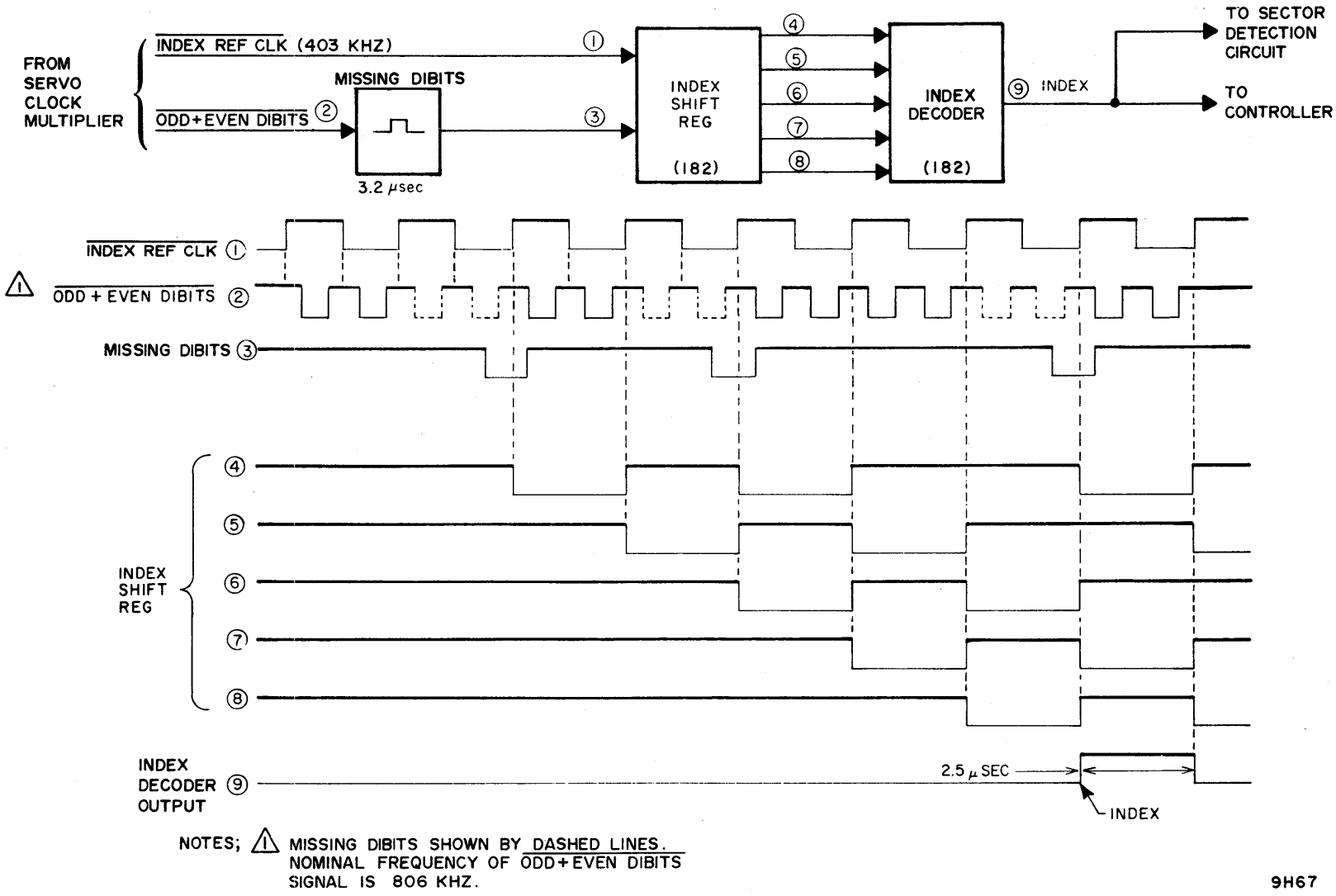


Figure 3-44. Index Detection - Logic and Timing

SECTOR DETECTION

The sector detection circuits (refer to figure 3-45) generate signals which are used by the system to determine the angular position of the heads with respect to Index. These signals are called Sector pulses and a specific number of them are generated during each revolution of the disk pack. The Sector pulses logically divide the disk into areas called sectors.

The Sector pulses are generated by the Sector counter which causes a pulse to be generated each time it indicates its maximum value of 4095.

The Sector counter is incremented by the 806 kHz clock pulses. These clock pulses are derived from the servo track dibit signals (refer to discussion on track servo circuit) and exactly 13,440 clock pulses occur during each revolution of the disk pack.

The fact that the same number of 806 kHz clock pulses occur during each revolution makes it possible to program the counter to reach the maximum count (thus generating a Sector pulse) any desired number of times per revolution. This done by presetting the counter ot the proper value at the beginning of each sector. For example, if it is desired to have 64 sectors, the counter would have to count 210 clock pulses in each sector (13,440 divided by 64) and the counter would be preset to 3886. In this case the counter starts at 3886 and increments each clock time until it reaches the maximum count of 4095. Reaching the maximum count causes the Sector pulse to be generated. The next clock pulse (210) presets the counter back to 3886 (thus disabling the Sector pulse) and the counter begins the next sector. The 3886 is obtained by subtracting 210 from 4096, which is the total number of clock pulses the counter is capable of counting (0 through 4095 = 4096).

The sector length is varied by changing the value of the preset inputs to the counter. This is done by resetting the sector switches located on the card in logic chassis position A2B08. Refer to section 1 of the maintenance manual for details regarding the setting of the sector switches.

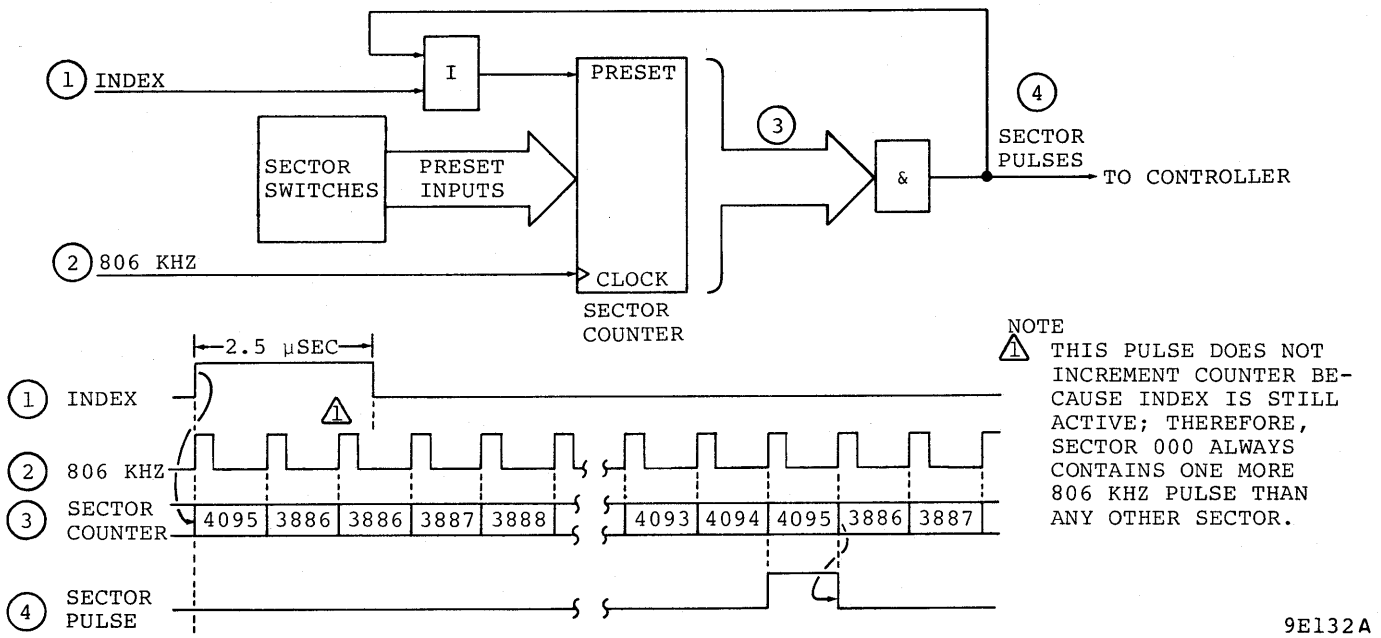


Figure 3-45. Sector Detection - Logic and Timing

READ-WRITE FUNCTIONS

GENERAL

When the drive is on cylinder, has a head selected, and has oriented to the proper place on the data track, it is ready to perform a read or write operation. The controller initiates a read or write operation by sending the drive a Control Select (Tag 3) and the proper bus bits (refer to discussion on Interface functions).

During a read operation, the drive recovers data from the disk and transfers it to the controller. During a write operation, the drive receives data from the controller and records it on the disk.

Figure 3-46 is a block diagram of the read-write circuits. The remainder of this discussion describes the read-write circuits and is divided into write operation and read operation descriptions.

WRITE OPERATIONS

General

The write circuit operation is initiated by a Control Select (Tag 3) from the controller, accompanied by Bus Bit 0. This allows the drive to start processing serial NRZ data received from the controller. The write data is received from the controller via the Write Data lines in the B cable. The write data is first processed by the NRZ to MFM converter/Write Compensation circuits. These circuits convert the data to MFM and also compensate it for problems caused by variations in data frequency. The compensated data is then processed by the write driver circuits, and then written on the disk. Figure 3-47 is a block diagram of the write circuits. Table 3-4 defines the elements of these circuits.

Principles of MFM Recording

In order to define the data stored on the pack, the frequency of the flux reversals must be carefully controlled. Several recording methods are available; each has its advantages and disadvantages. This unit uses the Modified Frequency Modulation technique.

The length of time required to define one bit of information is the cell. Each cell is nominally 103 nsec in width. The data transfer rate is, therefore, nominally 9.677 MHz.

MFM defines a "1" by writing a pulse at the half-cell time (figure 3-48). A "0" is defined by the absence of a pulse at the half-cell time. A pulse at the beginning of a cell is Clock; however, Clock is not always written. Clock is suppressed if there will be a "1" in this cell or if there was a "1" in the previous cell.

The rules for MFM recording may be summarized as follows:

- There is a flux transition for each "1" bit at the time of the "1".
- There is a flux transition between each pair of "0" bits.
- There is no flux transition between the bits of a "10" or "01" combination.

The advantages and disadvantages of MFM recording are as follows:

- Fewer flux reversals are needed to represent a given binary number because there are no flux reversals at the cell boundaries, achieving higher recording densities of data without increasing the number of flux reversals per inch.
- Signal-to-noise ratio, amplitude resolution, read chain operation, and operation of the heads are improved by the lower recording frequency achieved because of fewer flux reversals required for a given binary number.
- Pulse polarity has no relation to the value of a bit without defining the cell time along with cell polarity. This requires additional read/write logic and high quality recording media to be accomplished.

NRZ To MFM Converter/Write Compensation Circuits

The NRZ to MFM Converter/Write Compensation circuits convert the NRZ data into MFM data an and also shift the output MFM pulses to compensate for problems caused by variations in data frequency. Figures 3-49 and 3-50 show simplified logic and timing for these circuits.

The 9.67 MHz and 19.34 MHz signals from the servo frequency multiplier circuit provide basic timing signals for these circuits. The NRZ data from the controller provides the data input.

The NRZ to MFM converter converts the NRZ data, into MFM data and applies it to a delay line in the write compensation circuits. This delay line has three outputs which are combined with the outputs of the pattern decode logic (at the Early, Late, and Nominal gates) to produce compensated write data.

The pattern decode logic analyses the NRZ data and determines if its frequency is

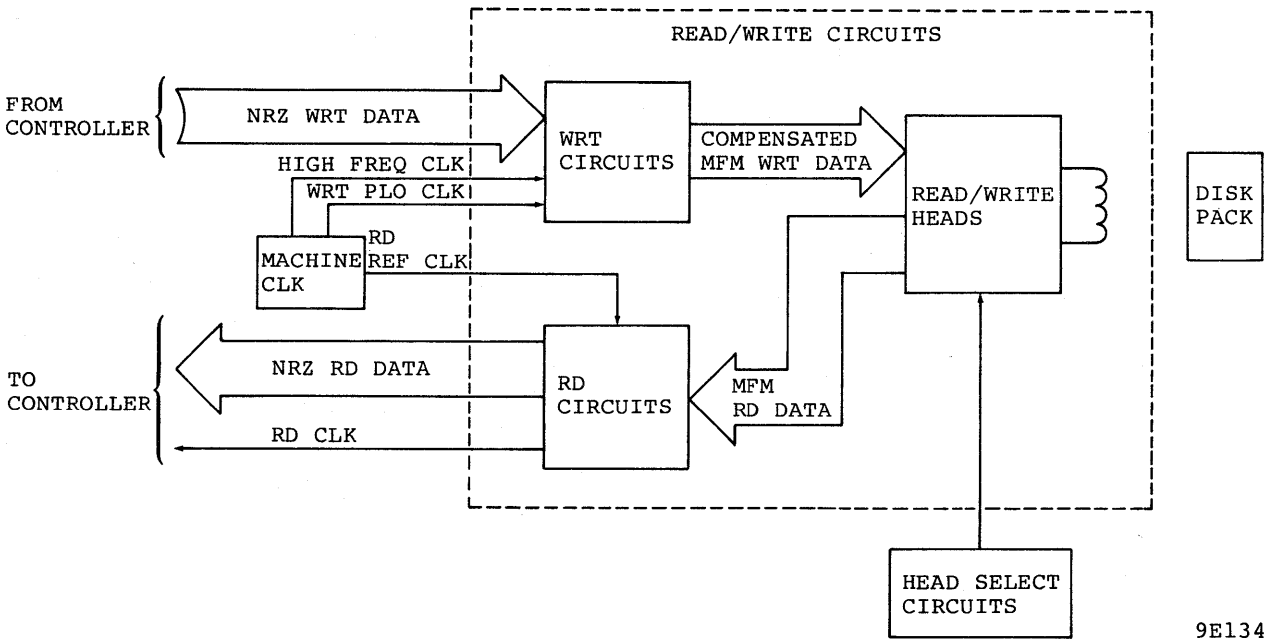


Figure 3-46. Read-Write Circuits - Block Diagram

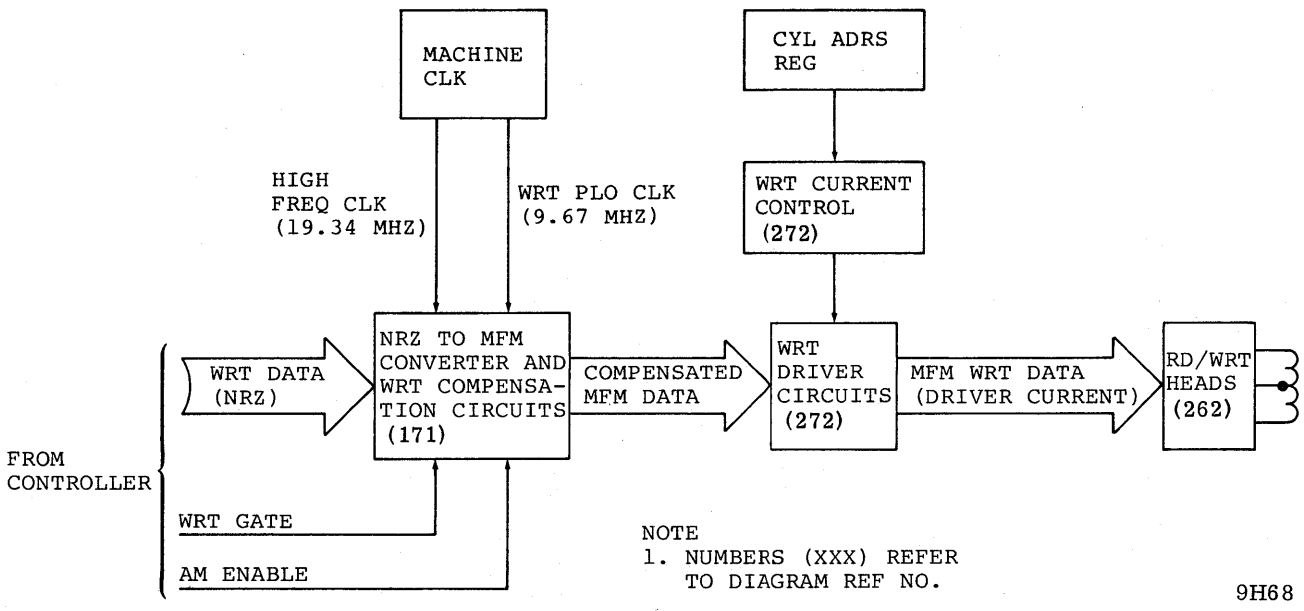


Figure 3-47. Write Circuits - Block Diagram

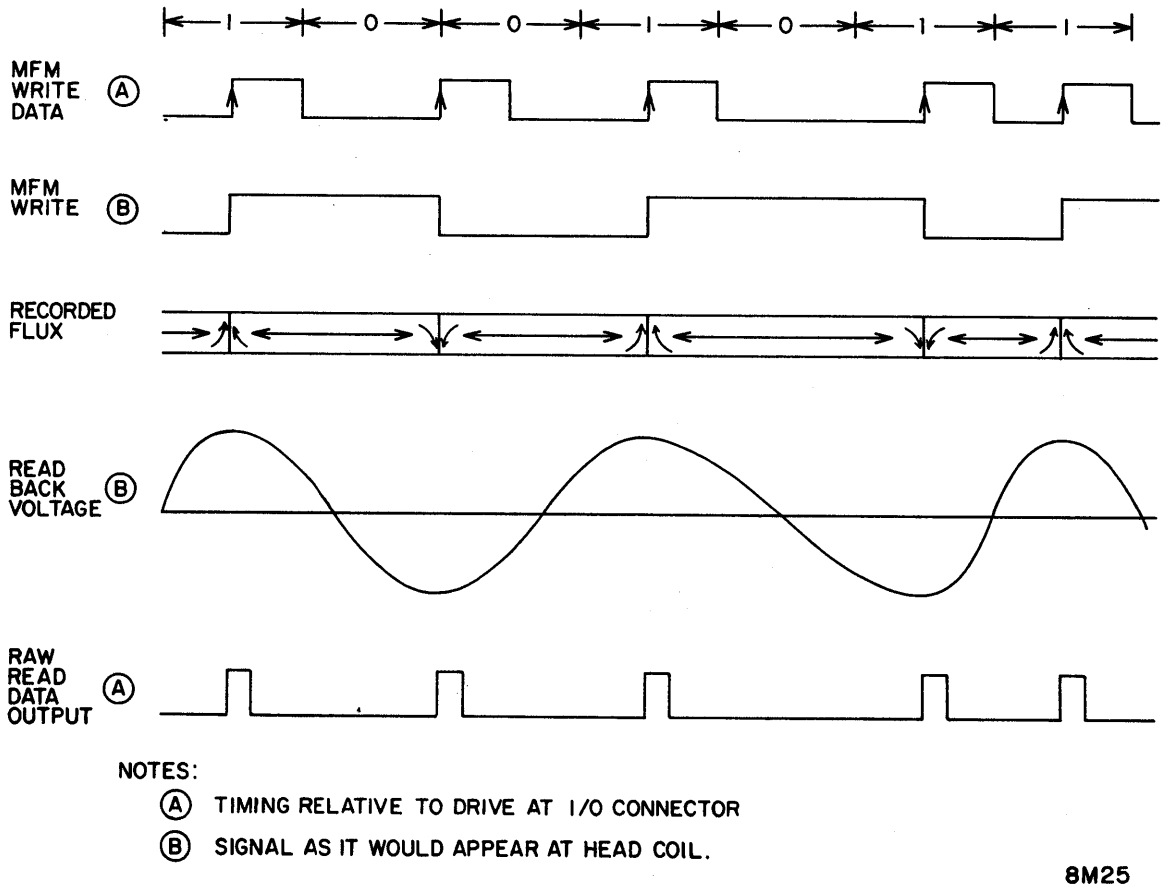


Figure 3-48. MFM Recording - Waveforms and Timing

TABLE 3-4. WRITE CIRCUIT FUNCTIONS

Circuit	Function
NRZ to MFM Converter and Write Compensation Circuits	Converts the NRZ data from the controller to MFM data and also compensates the data for problems caused by variations in the write data frequency.
Write Drive Circuits	Uses the MFM data to produce the current necessary to record data on the disk.
Write Current Control	Reduces the write current amplitude as the heads move from the outer tracks to inner tracks. This assures that the correct amount of current will be used as the circumference of the cylinders decrease.

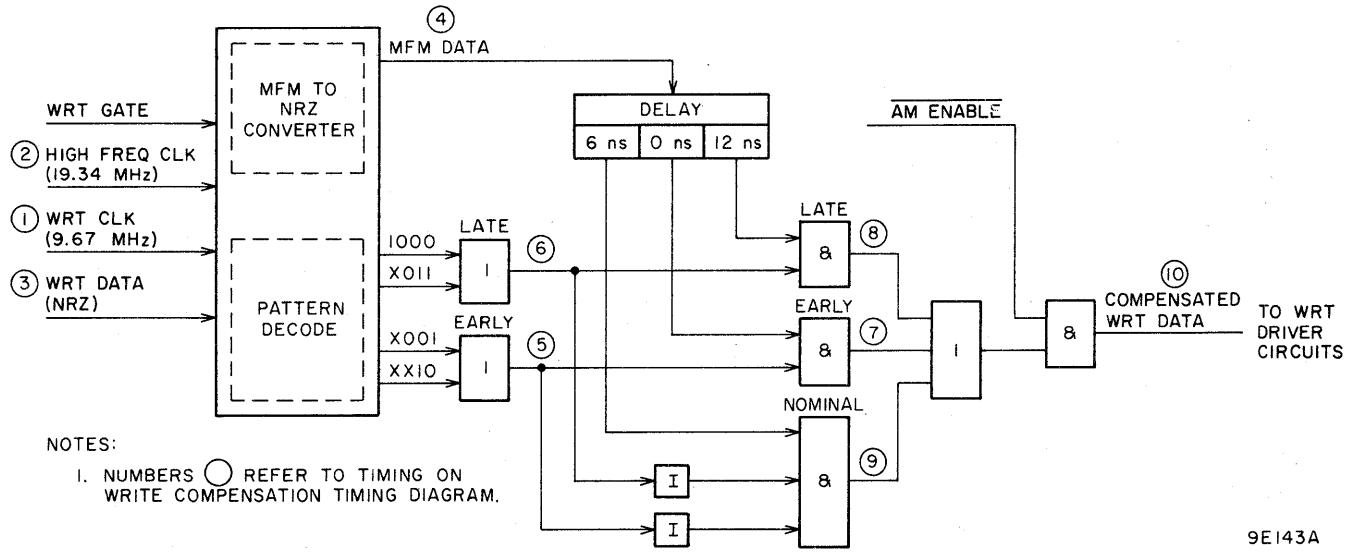


Figure 3-49. NRZ to MFM Converter/Write Compensation Circuit

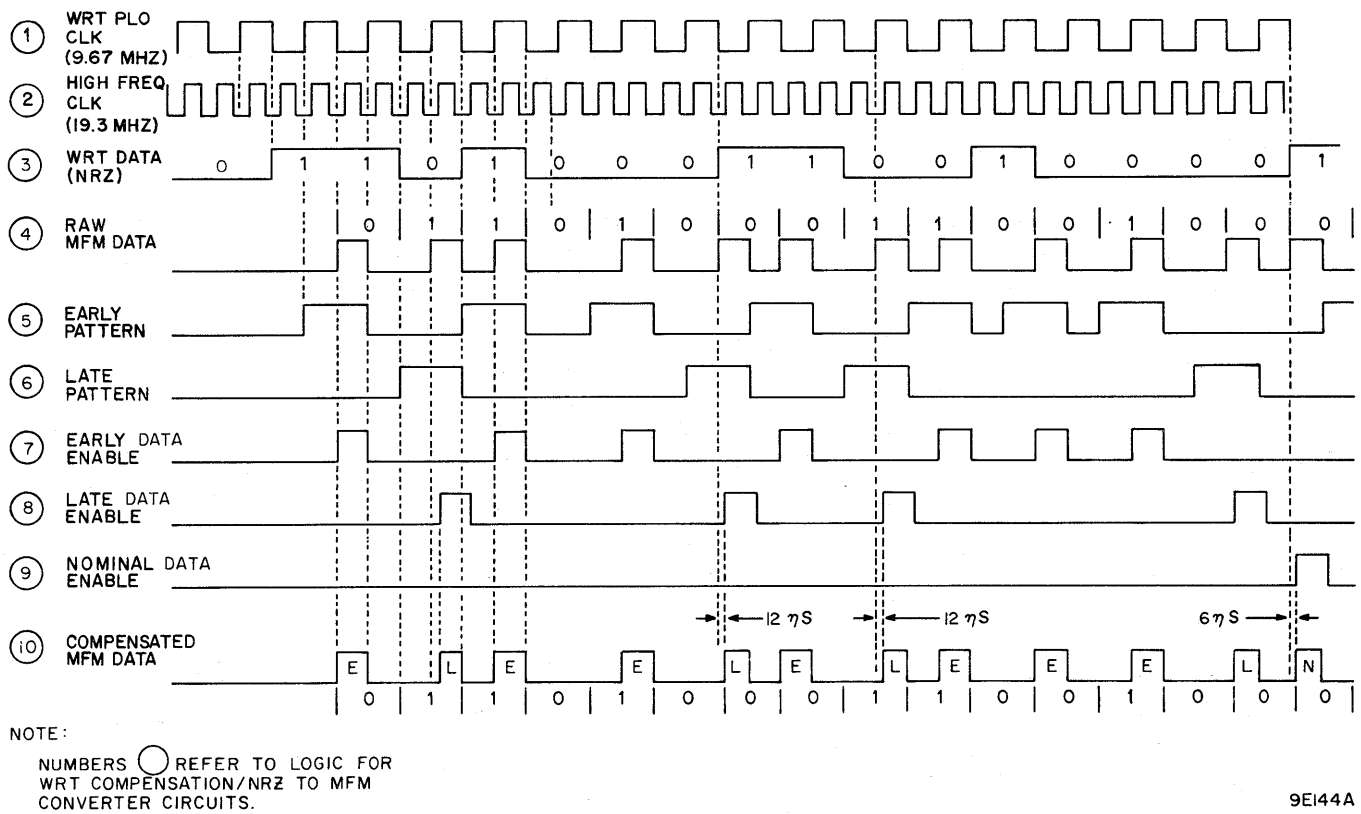


Figure 3-50. Write Compensation Timing

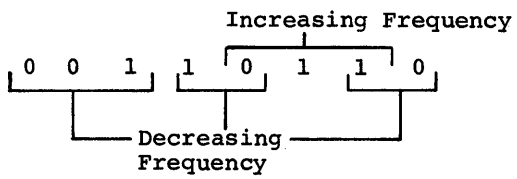
constant, increasing or decreasing. This is necessary because if the frequency is increasing or decreasing, problems can occur during subsequent read operations. These problems are eliminated by compensating the data before writing it on the disk.

The data frequency is constant whenever all ones or all zeros are being recorded because all pulses are separated by one cell (103 ns). However, a 011 pattern represents a frequency increase since there is a delay of about 1.5 cel between the 01 and only one cell between the 11. On the other hand a 10 pattern represents a frequency decrease since a pulse is not written at all in the second cell. A 001 pattern is also a frequency decrease since there is a one cell interval between the first two bits and 1.5 cell between the last two.

The previous examples examined only two or three bits without regard to the preceding or subsequent data pattern. The actual combinations are somewhat more complex. The drive logic examines and defines the following patterns:

Pattern	Frequency Change
011	Increasing
1000	Increasing
10	Decreasing
001	Decreasing

Any data pattern will have considerable overlapping of the data pattern frequency changes. Consider the overlap of these eight bits:



The outputs from the pattern decode logic enable either the Early, Late or Nominal gate (depending on the input frequency) to provide compensated Write data as follows:

- If frequency is constant, there will be no peak shift. In this case the data is defined as nominal and is delayed 6 nsec.
- If frequency is decreasing, the apparent readback peak would occur later than nominal. To compensate for this, the data is not delayed and is therefore 6 nsec earlier than the nominal data.
- If frequency is increasing, the apparent readback peak would occur earlier than nominal. Therefore, this data is delayed 12 nsec which is 6 nsec later than nominal.

After being write compensated the data is transmitted to the write driver circuits.

Write Driver Circuit

The compensated write data is sent to the read/write logic cards and applied to a differential receiver in the write driver circuits (refer to figure 3-51). The output of the receiver then serves as a clock for the Write Toggle FF. This flip flop toggles only when the Write Enable signal is active. The output of this flip flop provides the input to the Write Driver which in turn generates the current for the read/write heads. The magnitude of the current applied to the heads is controlled by the write current control circuits.

Write Current Control

The magnitude of the write current sent to the heads is controlled as a function of cylinder address. This is referred to as write current zoning. There are seven write current zones (A through G). Write current is maximum at the outer cylinders, and is reduced as each zone boundary is crossed. The cylinders in each write current zone are defined in table 3-5.

TABLE 3-5. WRITE CURRENT ZONES

ZONE	40 MB	80 MB
A	000 - 063	000 - 127
B	064 - 127	128 - 255
C	128 - 191	256 - 383
D	192 - 255	384 - 511
E	256 - 319	512 - 639
F	320 - 383	640 - 767
G	384 - 410	768 - 822

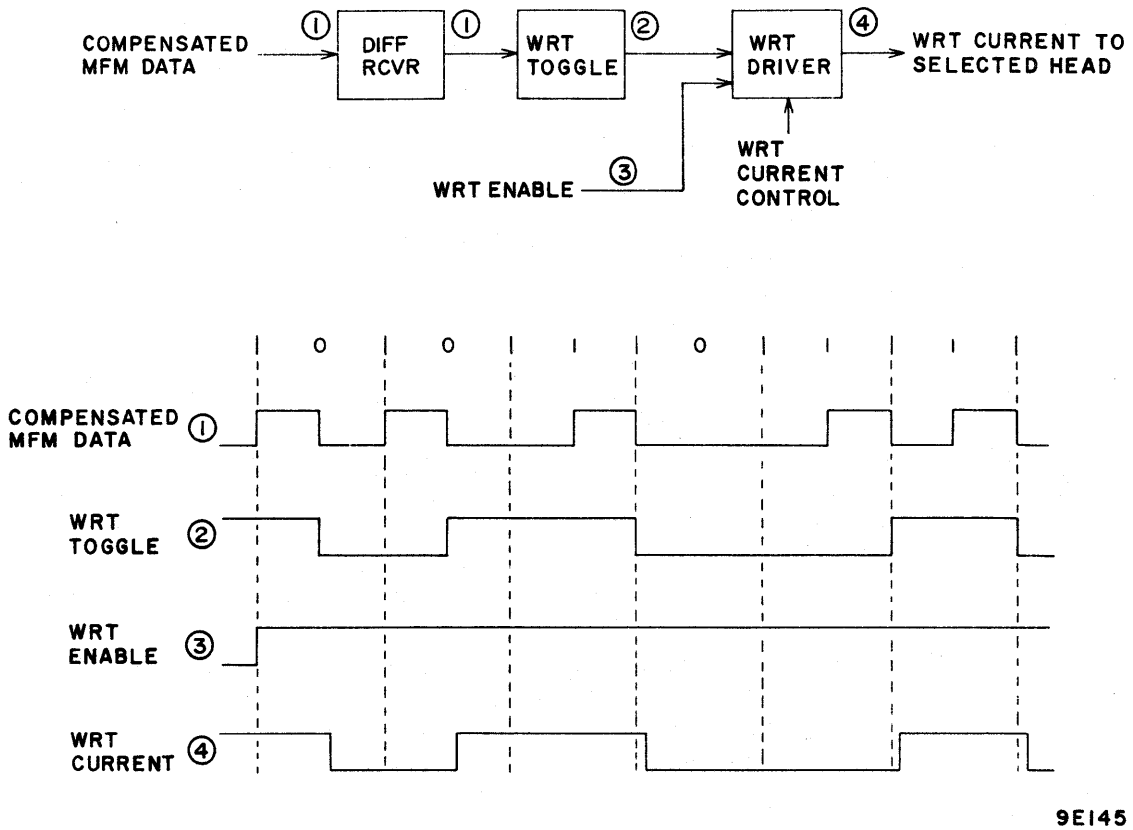


Figure 3-51. Write Driver Circuit and Timing

Writing Address Marks

The Address Mark is an area that contains neither MFM "1's" or "0's". The drive starts writing an Address Mark when it receives Control Select (Tag 3) and Bus Bits 0 through 5 from the controller. This activates the Address Mark Enable signal which prevents compensated write data from going to the write driver circuits. The Write Driver continues to generate current for the write coil but without data, no current reversals occur. The effect is to erase all information from the disk. The drive stops writing the Address Mark when the controller drops Control Select and Bus Bits 0 or 5.

Write Data Protection

As part of the data security system, the drive inhibits the write driver circuits whenever there is a danger of writing faulty data on the disk pack. The write driver is inhibited by the Write Protect signal, which is active under any of the following conditions:

- Write Protect switch on the control panel is set.
- A not up to speed condition exists.
- Servo Fault latch is set.
- The Fault latch is set.
- Head alignment is being performed.
- The heads are offset.

Some of the conditions which cause the Write Protect signal to go active, also cause an emergency retract condition. If this is true, it is possible that the voltages used to disable the write driver may not be reliable. For this reason, an 800 millisecond capacitive time delay network is built into the Write Protect circuit. If this circuit is triggered, the voltage stored in the capacitor network provides a reliable clamping circuit to ensure that the write driver is shut off, at least long enough for the heads to be retracted off the disk. This ensures that other data, already recorded on the disk, will not be destroyed by the heads writing during the retract operation.

READ OPERATIONS

General

Read operations are initiated by a Control Select (Tag 3) and Bus Bit 1. This enables the analog data detection circuits, which sense the data written on the disk and generate analog read data signals.

The analog data goes to the read analog to digital converter which changes it into digital MFM data. The read PLO and data separator change the MFM data to NRZ data and also generate a 9.67 MHz Read Clock signal. Both data and clock are than sent to the controller.

The read circuits also detect the Address Mark area and send an Address Mark Found signal to the controller.

Figure 3-52 shows the main elements in the read circuits and table 3-6 briefly describes each of these elements.

TABLE 3-6. READ CIRCUIT FUNCTIONS

Circuit	Function
Analog Read Data Detection Circuits	Processes the analog signals sensed by the read/write heads so that they can be used by the digital to analog converter.
Digital to Analog Converter	Changes the analog MFM data into digital MFM data. This data is sent to the read PLO and data separator.
Read PLO and Data Separator	This circuit converts the MFM data to NRZ and also generates a 9.67 MHz Read Clock signal. It transmits both of these to the controller.
Address Mark Detection	Detects the Address Mark and transmits an Address Mark Found signal to the controller.

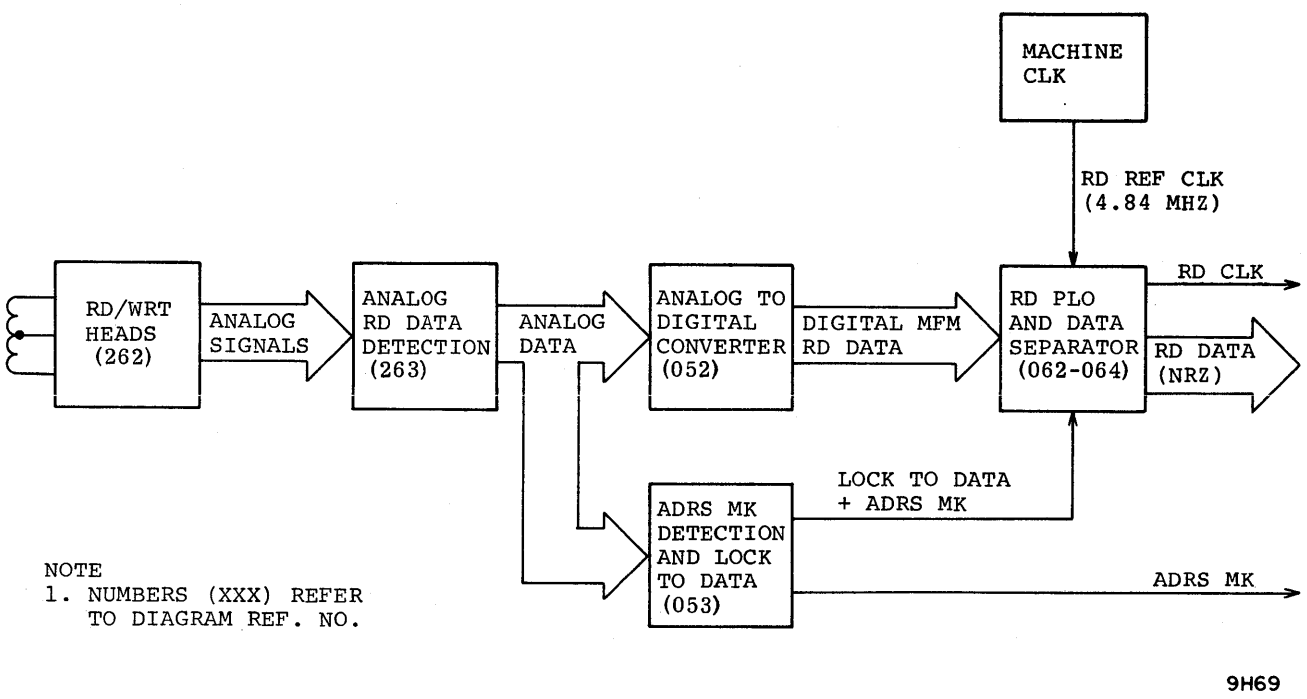


Figure 3-52. Read Circuits - Block Diagram

Analog Read Data Detection Circuits

The analog read data detection circuits (refer to figure 3-53) process the analog MFM data detected from the disk so it can be used by the analog to digital converter circuits.

The Read Pre-amplifier provides preliminary amplification of the analog voltage induced in the read coil. This voltage is induced in the coil by the magnetic flux stored in the disk oxide during write operations (refer to discussion on General Write Operation). The frequency of the analog voltage is proportional to the frequency of the magnetic field flux transitions sensed by the read coil.

The low pass filter on the output of the Read Pre-amplifier attenuates the high frequency noise on the read data signals and provides a linear phase response over the range of read data frequencies. The output of the filter is applied to the AGC amplifier. This circuit generates an output signal amplitude that remains within certain limits regardless of the amplitude of the input signal. The AGC Gain Control circuit provides the control voltage for the AGC amplifier and also provides inputs to the Address Mark detection circuits.

The Buffer amplifier processes the AGC amplifier output to provide the proper input for the analog to digital converter circuit.

Read Analog to Digital Converter

The read analog to digital converter circuits (refer to figure 3-54) receive analog MFM read data from the analog read data detection circuit and convert it to digital MFM data.

The analog to digital converter circuit consists of high and low resolution channels and the Data Latch FF. The high and low resolution channels detect the analog data by means of zero cross detectors consisting of Schmitt triggers. The zero cross detectors convert the analog data to digital pulses which are then applied to the Data Latch FF. The FF uses the outputs of both channels to produce a digital MFM data output. The low resolution channel provides the D input to the FF and the high resolution channel provides the clock. This produces an output from the Data Latch FF which retains the timing of the high resolution channel.

Both channels are necessary because of certain high frequency components present in the analog read data signals. These components can cause extraneous zero crossings which are detected by the zero cross detectors. However, the low pass filter in the low resolution channel attenuates the high frequency components thus eliminating any possible extraneous outputs from the channels zero crossing detector.

The high resolution channel still detects the crossings and generates clock inputs to the FF, but without the D input provided by the low resolution channel the extraneous clock pulses are ignored.

The digital MFM read data is sent to the PLO and data separator which use it to generate the NRZ data and Read clock.

Lock To Data And Address Mark Detection Circuits

These circuits generate (refer to figure 3-55) the Lock to Data signal and also detect the Address Mark area. The Lock to Data signal is used to synchronize the Read PLO and

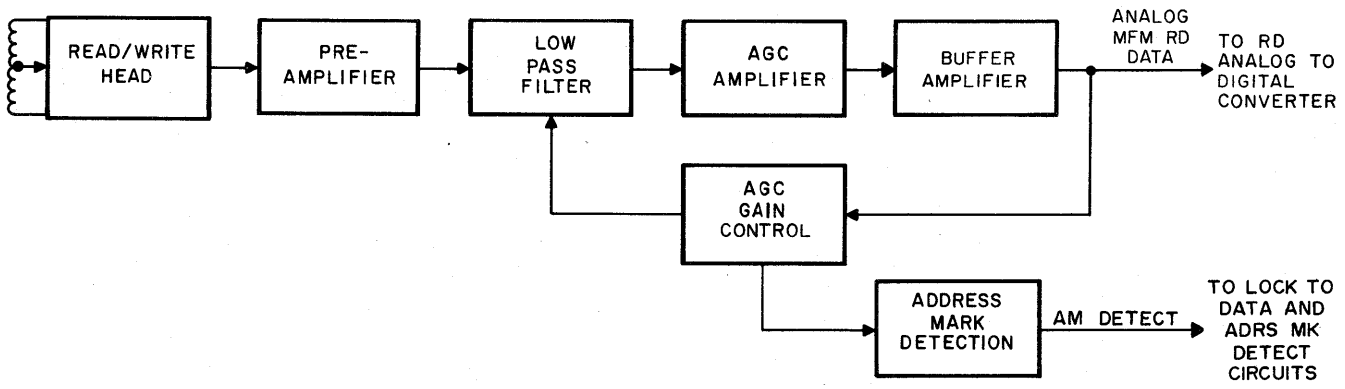


Figure 3-53. Analog Read Data Detection Circuits

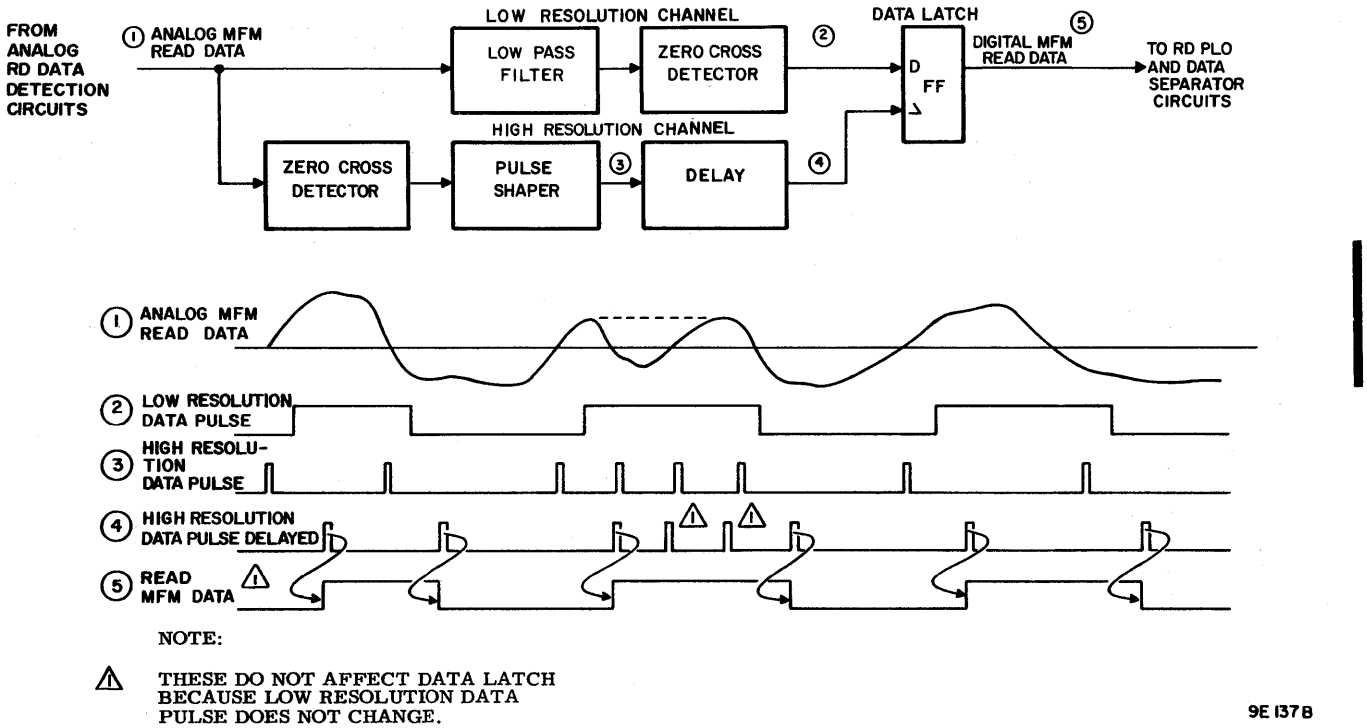


Figure 3-54. Read Analog to Digital Converter - Logic and Timing

Data Separator circuits. Detecting the address mark sets the Address Mark Found line to the controller.

The Lock to Data signal is active whenever the Lock to Data one shot is in the set state. This one shot is triggered (to the set state) when either the Read Gate signal goes inactive or the Address Mark is detected.

When the Read Gate signal goes inactive it triggers the one shot and also causes it to be held in the set state. When the Read Gate signal goes active again, it removes the set conditions from the one shot and allows it to time out after 7.75 µsec. Therefore, a 7.75 µsec lock to data period occurs at the beginning of every read operation. Detecting the Address Mark also triggers a 7.75 µsec pulse from the one shot.

The Address Mark consists of an area about 2.4 µsec in length that contains neither MFM ones or zeros.

The address mark detection circuit is enabled only during read operation. The controller activates the circuit by raising Bus Out bit 4 (Address Mark Enable).

The Address Mark Enable signal causes the comparator to start generating output pulses that trigger and retrigger the Data Detect one shot. The comparator generates the output pulses only when there are input data pulses. Therefore, during the Address Mark area, the comparator stops generating pulses and the one shot times out 1.7 µsec after the last data pulse was detected. The first data pulse following the Address Mark area enables the Address Mark Detect gate. This triggers the Lock to Data one shot which causes a 7.75 µsec Lock to Data period and also a 7.75 µsec Address Mark signal.

Read PLO And Data Separator

General

This circuit has two functions: (1) to convert the MFM data from the analog to digital converter into NRZ data and (2) to generate a Read Clock signal which is locked to the frequency of the read data (9.67 MHz nominal). Both the NRZ data and the Read Clock signal are transmitted to the controller.

The read PLO and data separator circuits consist of four main parts (refer to figure 3-56):

- Input Control - Controls whether MFM data or 4.84 MHz clock pulses will furnish the input to the circuit.

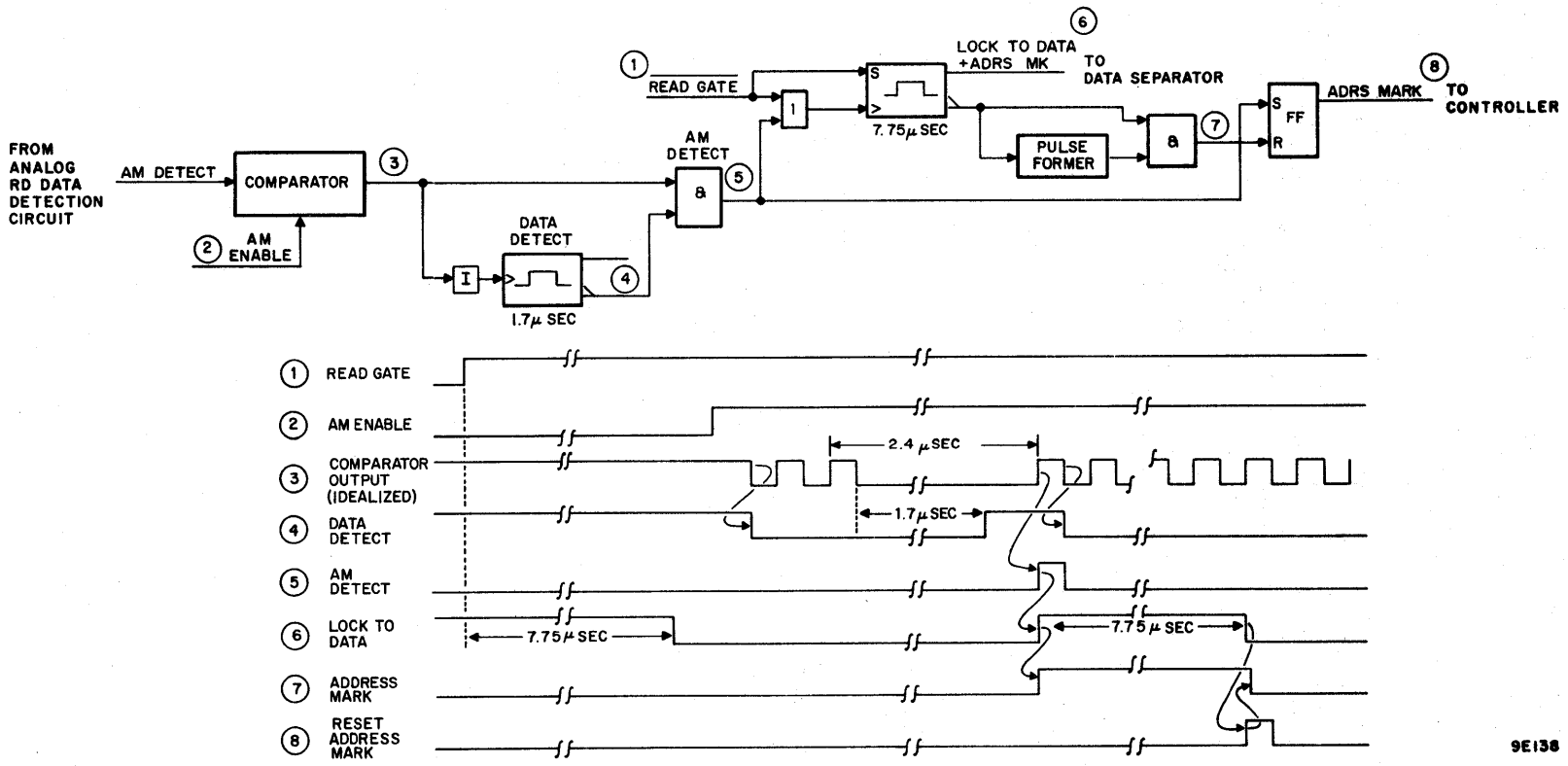


Figure 3-55. Lock to Data/Address Mark Detection - Logic and Timing

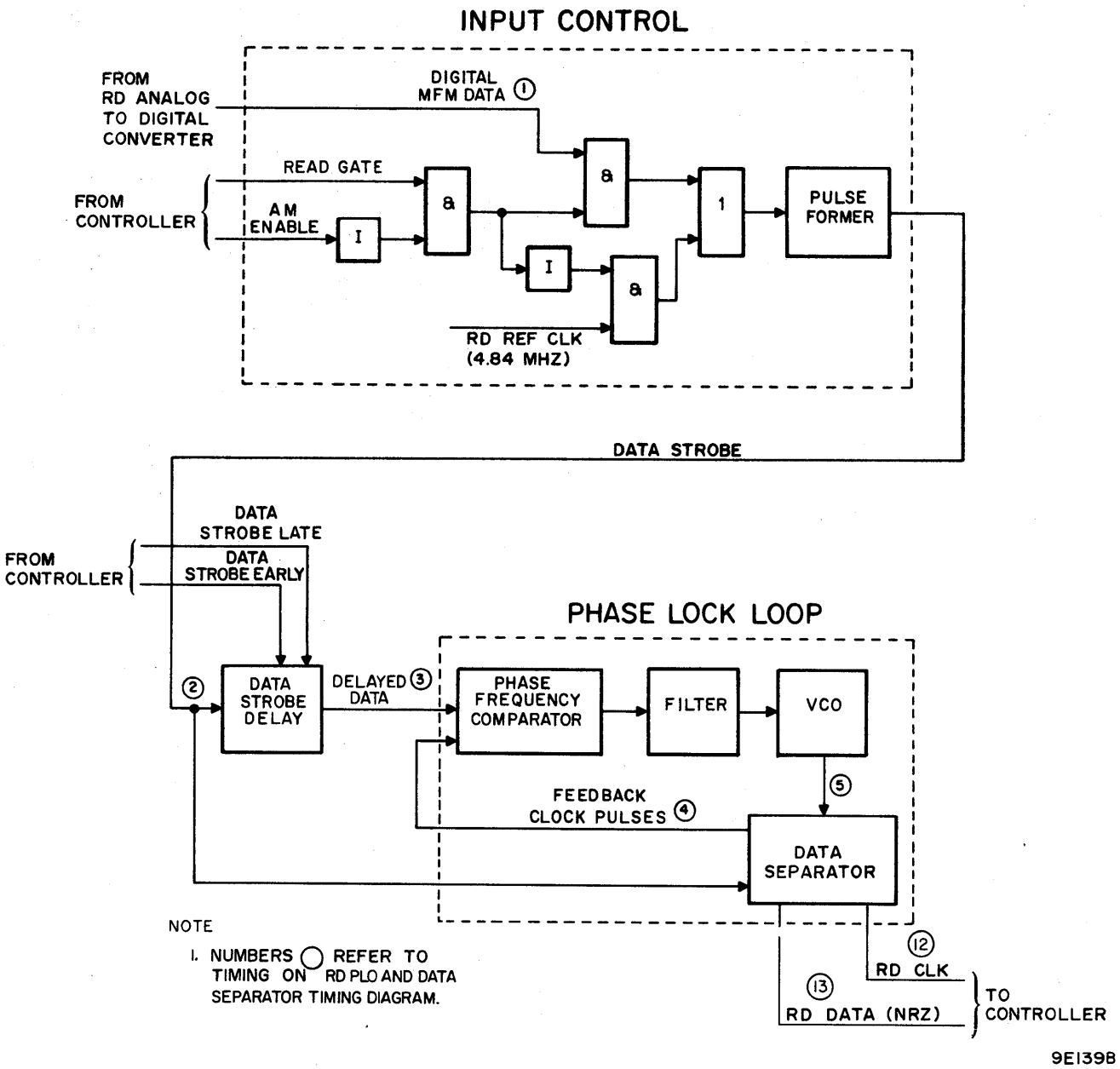


Figure 3-56. Read PLO and Data Separator Circuits

- Data Strobe Delay - Delays the pulses to provide the proper input to the VCO. These circuits also provide error recovery capability.

- Phase Lock Loop - Synchronizes the circuit outputs to the phase and frequency of the inputs.

- Data Separator - Converts the MFM data to NRZ data and generates the Read clock. This circuit is actually a part of the phase lock loop.

The remainder of this discussion further describes the read PLO and data separator circuits.

Input Control

The input control circuit (refer to figure 3-56) selects the input that will be used by the read PLO and data separator circuits. This input will always be either MFM data from the read analog to digital converter or 4.84 MHz clock pulses from the servo frequency multiplier circuit.

The 4.84 MHz clock signal is used only when the drive is not reading MFM data, such as before Read Gate is raised. It also uses the 4.84 MHz clock whenever the Address Mark Enable signal is active because this indicates the drive is expecting the Address Mark which contains no MFM data. The drive uses the clock signal as a substitute for the read data for two reasons: (1) the signal is derived from the track servo dibits and therefore, its frequency (like that of the read data) varies directly with disk pack speed and (2) after being processed by the pulse forming circuits, it has about the same nominal frequency as the read data (9.67 MHz). This results in it being easier for the phase lock loop to synchronize to the proper frequency when switching from one of the signals to the other.

Once selected the signal is applied to a pulse forming network which generates a 10 nsec pulse for each transition of the input. These pulses are then applied to the data strobe delay circuits and also furnish the data input to the data separator.

Data Strobe Delay

The purpose of the data strobe delay circuit (refer to figure 3-56) is to delay the data pulses sufficiently to provide the proper timing relationship at the input to the phase lock loop. The output of the data strobe delay circuit is delayed by a time determined by the state of the Data Strobe Early and Data Strobe Late signals. These signals facilitate the recovery of marginal data and are enabled by Control Select (Tag 3) and Bus Bits 7 or 8.

The output of this circuit is the Delayed Data signals which are sent to the input of the phase lock loop.

Phase Lock Loop

The phase lock loop (refer to figure 3-56) synchronizes the read PLO/data separator circuit outputs (NRZ data and Read Clock) to the input (either MFM data or 4.84 MHz clock). The loop accomplishes this by comparing and following two signals: (1) the Delayed Data signals which have a constant phase and frequency relationship to the input MFM data or 4.84 MHz Clock (whichever is used) and (2) the Feedback Clock Pulse signals which have a constant phase and frequency relationship to the output NRZ data and Read Clock signals. The loop inputs are applied to the phase/frequency comparator.

The phase/frequency comparator generates output pulses which are a function of the phase and frequency between the positive going edges of the inputs. The filter circuit uses the comparator outputs to generate a control voltage for the voltage controlled oscillator (VCO).

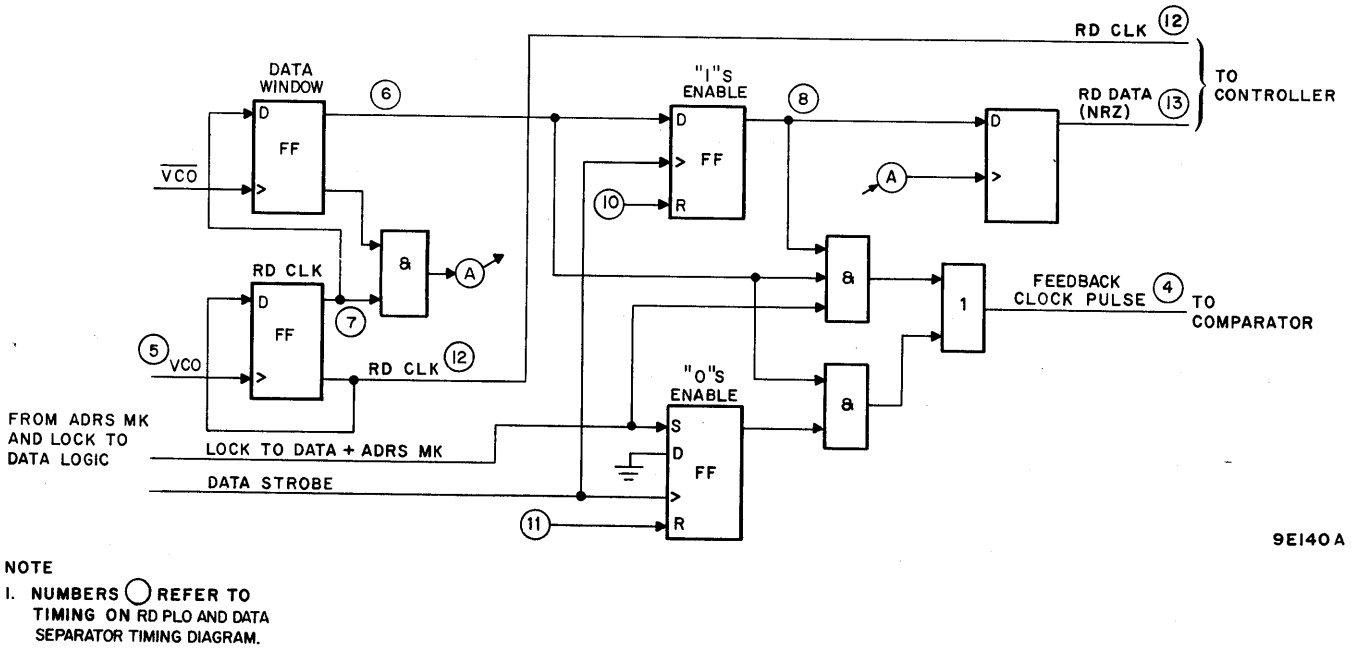
This control voltage causes the frequency of the VCO to vary in the direction necessary to eliminate the phase and frequency differences between the two signals that were input to the comparator.

The output frequency of the VCO is actually twice that of the input so for an input of 9.67 MHz it has an output of 19.34 MHz. However, the data separator divides this by two before generating the Feedback Clock Pulse signals thereby providing a feedback to the comparator that satisfies the loop.

Data Separator

This circuit determines if the data pulses represent a one or zero and then converts the data to NRZ. It also generates the Feedback Clock Pulses to the comparator and the 9.67 MHz Read Clock that is sent to the controller. Figures 3-57 and 3-58 show simplified logic and timing for the data separator circuit.

The VCO outputs provide the proper timing relationships for the data separator by controlling the Data Window and Read Clock FFs. The Read Clock FF generates the 9.67 MHz Read Clock signal and also provides timing signals to the data separator logic.



NOTE

1. NUMBERS ◯ REFER TO TIMING ON RD PLO AND DATA SEPARATOR TIMING DIAGRAM.

Figure 3-57. Data Separator Logic

The Data Window FF generates the Data window which is used to determine whether the input data pulses represent ones or zeros. The actual decoding of the data is done by the "1's" Enable and "0's" Enable FFs.

If a data pulse represents a one it occurs during the data window and sets the "1's" Enable FF. Setting this FF generates a Feedback Clock pulse and causes the Data Buffer FF to generate a NRZ one.

If the data pulse represents a zero the "1's" Enable FF is not set and the Data Buffer FF generates a NRZ zero. In this case the "0's" Enable FF which is set by every data pulse generates the Feedback Clock Pulse signal.

Before accurate detection of data can begin, the proper phase relationship must be established between the data (representing ones and zeros) and the VCO output pulses. This is done during a 7.75 µsec lock to data period which is initiated by the Lock to Data signal. This signal is a 7.75 µsec pulse that occurs when the Read Gate signal goes true or when the Address Mark is detected. The Lock to Data signal holds the "0's" Enable FF set and disables the output of the "1's" Enable FF. Therefore, if the circuit is to synchronize properly the pulse must occur during a period when the drive is reading only zeros.

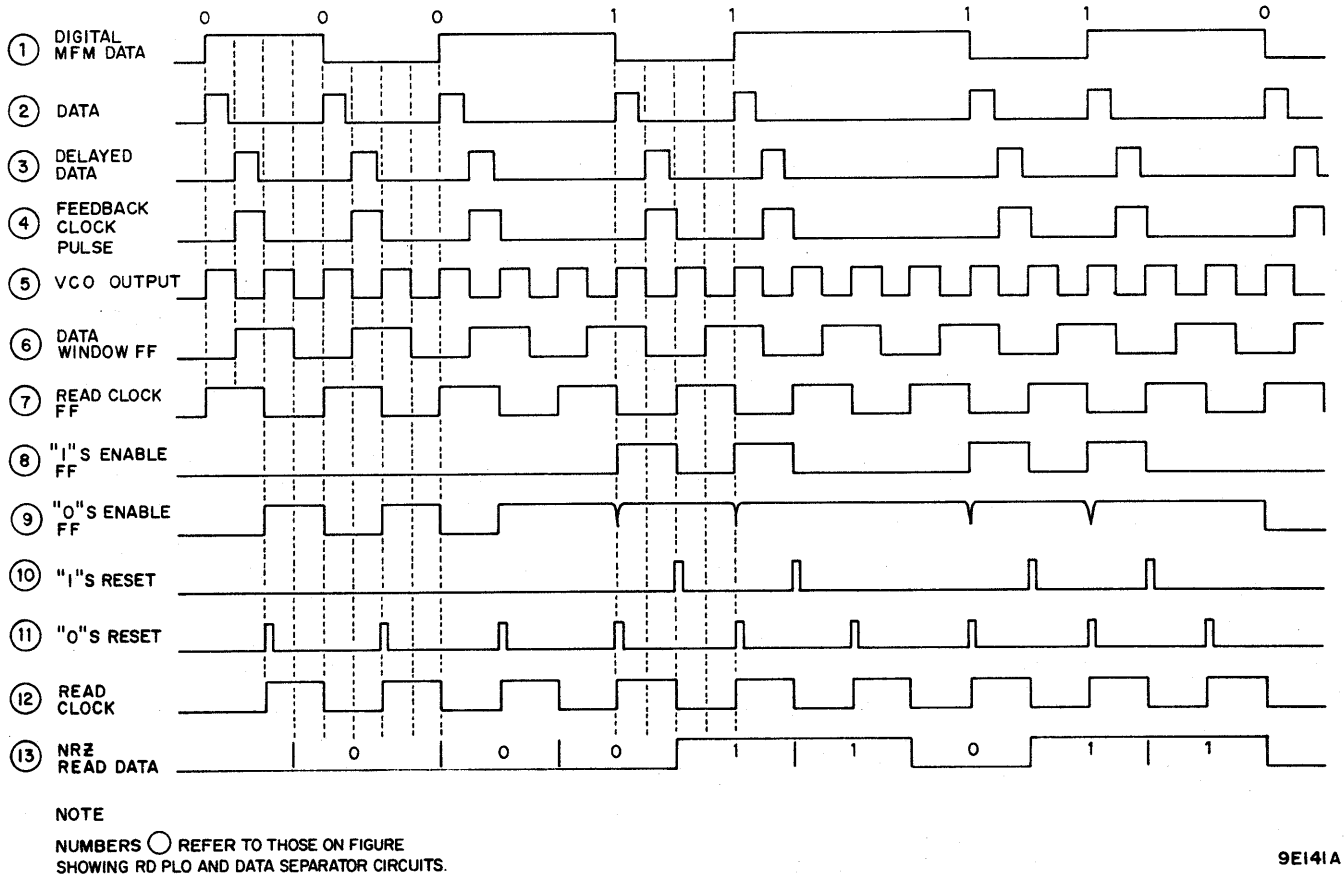


Figure 3-58. Read PLO and Data Separator Timing

FAULT AND ERROR CONDITIONS

GENERAL

The following describes those conditions which are interpreted by the drive as errors. All of these conditions either light an indicator at the drive and/or send a signal to the controller indicating an error has occurred.

These errors are divided into two categories:
(1) those indicated by a Fault Latch
(2) those not indicated by a Fault Latch
Both are explained in the following (refer to figure 3-59).

ERRORS INDICATED BY FAULT LATCH

General

Certain errors set the drives Fault latches associated with the error condition.

Setting the Fault Latch does four things (1) enables the fault line to the controller (2) lights the FAULT indicator on the drives control panel (3) clears the drives Unit Ready signal (4) inhibits the drives write and load circuitry. These events prevent further drive operations from being performed until the error is corrected and the Fault latch is cleared.

Providing the error condition or conditions no longer exist, the Fault latch is cleared by any of the following:

- FAULT switch on operator panel.
- Controller Fault Clear signal from the controller.
- Maintenance Fault Clear switch on Fault card.
- Powering down the unit.

Whenever an error occurs that sets the Fault latch, it also sets an individual latch associated with that error. These latches provide a means of storing the error indication so it can be referred to later for maintenance purposes. The fault latches are cleared only by powering down the drive or by the Maintenance Fault Clear switch on the fault card.

The following describes each of the conditions causing the Fault latches to be set.

Write Fault

A write fault is indicated if any of the following conditions exist.

- Low output from write driver indicating it may not be operating properly.
- Low current input to write driver.
- Low +22 volts to write driver.
- No write data transitions when Write Gate is active.

Head Select Fault

This fault is generated whenever more than one head is selected. The outputs of the head select circuits are monitored by summing and voltage comparator circuits. If more than one head is selected, the circuit generates a Multiple Select Fault.

Read and Write Fault

This fault is generated whenever the drive receives a Read gate and Write gate simultaneously from the controller.

(Read or Write) and Off Cylinder Fault

This fault is generated if the drive is in an Off Cylinder condition and it receives a Read or Write gate from the controller.

Voltage Fault

This fault is generated whenever the ±46, ±5 or ±20 voltages are below satisfactory operating level.

ERRORS NOT INDICATED BY FAULT LATCH

General

The following errors are detected by the drive but are not stored in the fault latches. However, they do cause the drive to give other error indications and this is explained in the following paragraphs.

Low Speed or Voltage

The Speed or Voltage Fault signal goes true when the drive detects either a low voltage condition or that drive spindle speed is below 3000 r/min. When either of these are detected, the drive write circuits are disabled and the Write Protect signal is sent to the controller. These also result in an emergency retract of the heads (refer to discussion on Emergency Retract).

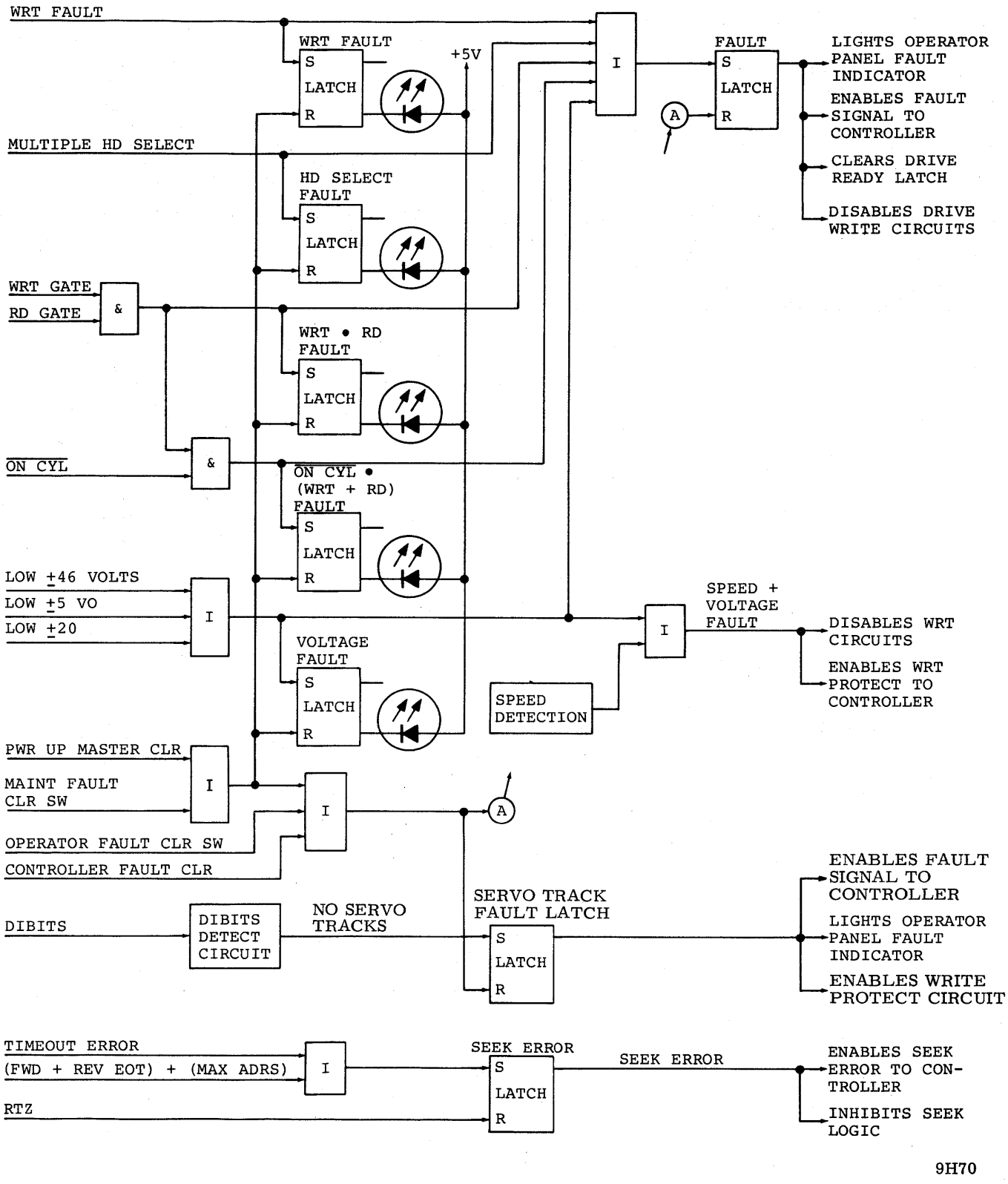


Figure 3-59. Fault and Error Detection

No Servo Tracks Fault

If dibits are not detected within 350 ms after the load seek sequence begins, the No Servo Tracks latch is set. This lights the FAULT indicator on the drive operator control panel and also enables the Return to Zero (RTZS) logic. Enabling the RTZS logic causes the heads to unload. Another load cannot be started until the No Servo Tracks latch is cleared. The No Servo Tracks latch is cleared in the same matter as the Fault latch.

Seek Error

The Seek Error latch is set by any of the following error conditions:

- On Cylinder was not obtained within 500 ms from the start of the seek.
- Forward or reverse end of travel (EOT) sensed.
- Drive is commanded to seek to a cylinder address greater than 410 (822).

Setting the Seek Error latch enables the Seek Error line to the controller and also inhibits the drive from performing another seek until the Seek Error latch is cleared. The latch is cleared by a Return to Zero Seek command.

SECTION 4

DISCRETE COMPONENT CIRCUITS

DISCRETE COMPONENT CIRCUITS 4

INTRODUCTION

This section provides descriptive information regarding the discrete component circuits used on the logic diagrams for the 40 MB and 80 MB drives. Many of the circuits made up of discrete components are represented in the logic diagrams by special symbols. The descriptive information for these symbols is provided in the form of data sheets. These data sheets provide a circuit description, a circuit schematic, and the logic symbol. In addition, some of the data sheets provide typical waveforms. Component values, voltage levels, and timing information shown on the data sheets are for reference only; as some of the values change periodically.

In addition to the data sheets, provided in this section, use the Normandale Circuits Manual. This manual provides information regarding general circuit theory, symbology used on the logic diagrams, and data sheets covering the integrated circuits used in these machines.

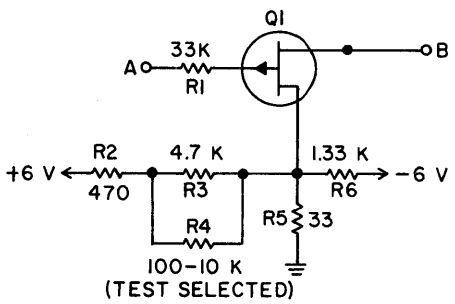
DATA SHEETS

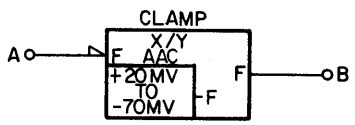
The data sheets contained in this section are arranged in alphabetical order from AAA to ZZZ. The following circuits are covered in this section:

AAC	GKF	TLZ
ALR	JMN	UBT
AZJ	LDK	UC- (S & P)
BRD	LLZ	UEB
BZJ	MZJ	ULY
CZJ	RAP	VHK
DLC	SHT	WCN
DZJ		

CLAMP - AAC

The purpose of the AAC circuit is to minimize stabilization time between read and write operations. The output at point B is connected to the AGC capacitor. During write operations, the FET is turned on, providing a low source-to-drain impedance; thus point B is clamped at the dc level determined by the voltage divider circuit (R2 through R6). R4 is test-selected to minimize stabilization time by setting the source level of Q1 between -70 and +20 mV.





AAC
Rev A
Sheet 1 of 1

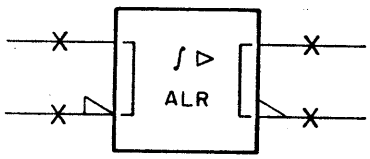
Amplifier and Filter - ALR

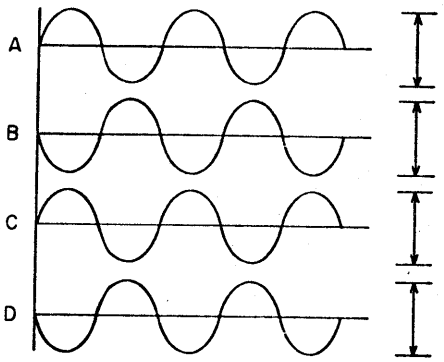
The ALR circuit is a differential amplifier and a 2 pole linear phase filter followed by a differential buffer amplifier. The amplifier stage has a gain of approximately 2.

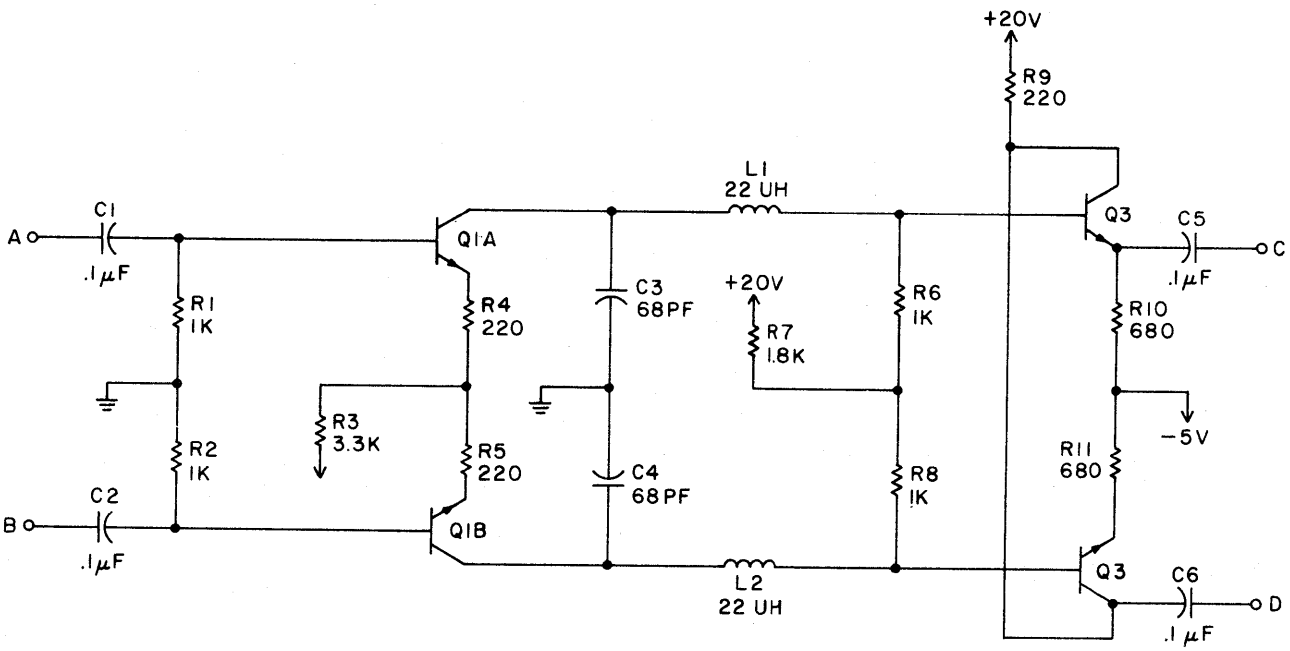
Q1A and B form the differential amp with R6 and R8 being the load resistors and also impedance matching resistors for the filter. The inductors L1 and L2 and capacitors C3 and C4 make up the rest of the filter. The upper break design frequence (-3 db point) of the filter is 3.13 MHz.

The input coupling capacitors C1 and 2 in conjunction with bias resistors R1 and 2 give the circuit a low frequency cutoff (-3 db point) of less than 2 kHz.

The output is a differential emitter follower buffer consisting of Q3 and 4 and R10 and 11, that is used to reduce the output impedance.







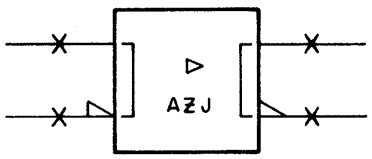
NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

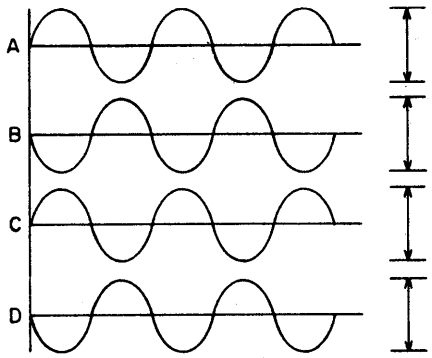
ALR
Rev A
Sheet 1 of 1

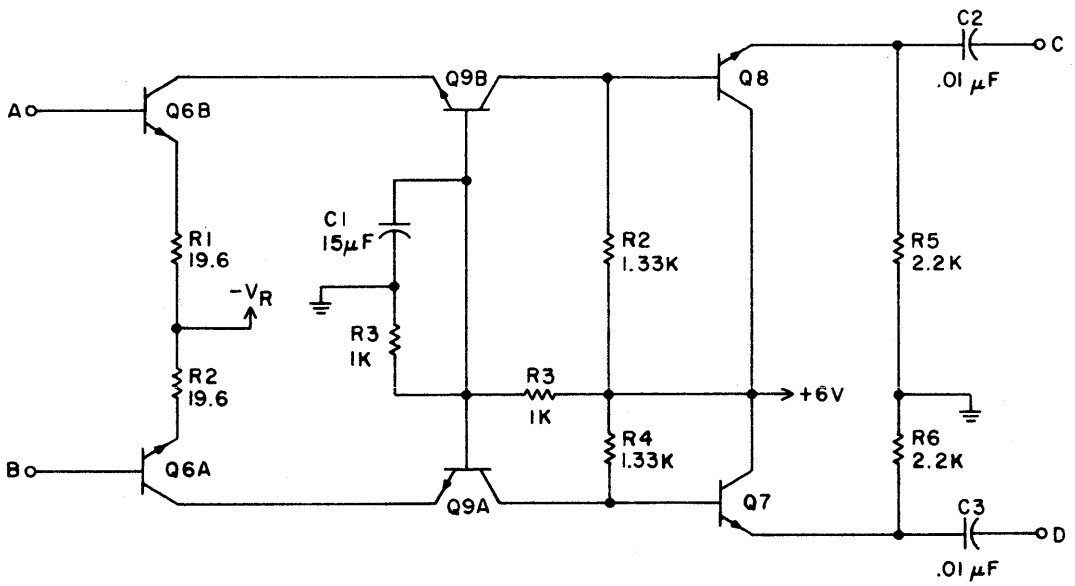
Differential Amplifier - AZJ

The preamplifier is a cascade type with a matched pain of transistors (Q6A and Q6B) used as a common emitter front end followed by another matched pain of transistors (Q9A and Q9B) used as a common base second stage, this effectively reduces the emitter collector capacitance of the common emitter front end.

The final stage of the front end is a emitter follower (Q7 and Q8) used as a buffer between the preamp and filter section. Resistors R1 and R2 in the emitter circuit give the front end a input impedance of just under the 500 ohms. The constant current source for the preamp supplies approximately 2.5 ma.







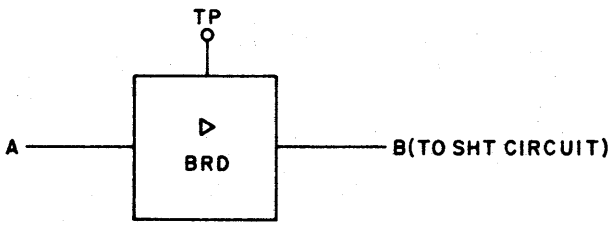
NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

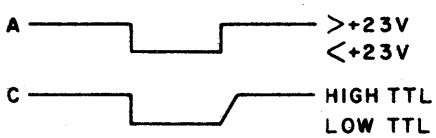
AZJ
Rev A
Sheet 1 of 1

LEVEL TRANSLATOR (COMPARATOR SECTION) - BRD

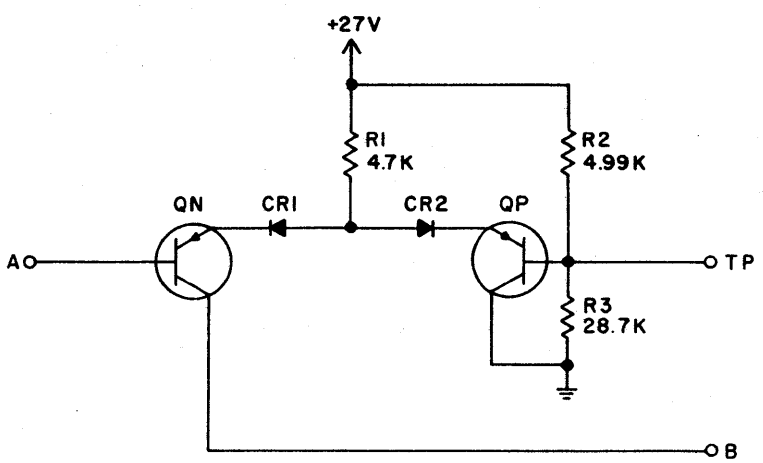
The BRD circuit is a differential voltage comparator which operates in conjunction with the SHT circuit to translate input signal levels of below +23 V to a low TTL output and input signal levels of above +23 V to a high TTL output.

The BRD circuit functions in conjunction with the SHT circuit to indicate whether or not the write current is below a minimum value. (See SHT circuit description.) A voltage reference of +23 V is applied to the base of transistor QP. With normal write current, the base of QN is below +23 V. Under these conditions transistor QN is on and transistor QP is off, and the resistor in the collector circuit of QN provides a forward bias voltage to the SHT circuit. If the write current is below the acceptable minimum, the voltage at the base of QN goes above +23 V. Then QN turns off and QP turns on, and the resistor in the collector circuit of QN does not develop sufficient forward bias for the SHT circuit.





NOTE: A IS INPUT TO BRD CIRCUIT
C IS OUTPUT OF SHT CIRCUIT



NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

BRD
Rev B
Sheet 1 of 1

Amplifier and Filter - BZJ

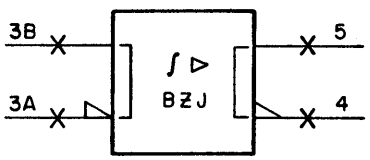
The BZJ circuit is a differential amplifier and a 4 pole low pass Butterworth filter followed by a differential buffer amplifier. The amplifier stage has a gain of approximately 7.5.

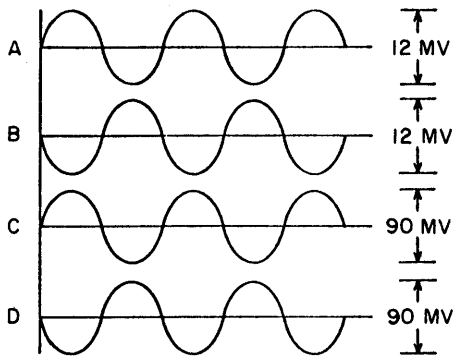
Q3A and B form the differential amplifier with R5 and R6 being the load resistors and also impedance matching resistors for the filter. The inductors L1, L2, L3, and L4 and capacitors C1, C2, C3 and C4 make up the rest of the filter. The upper break frequency (-3db point) of the filter is approximately 6.8 MHz.

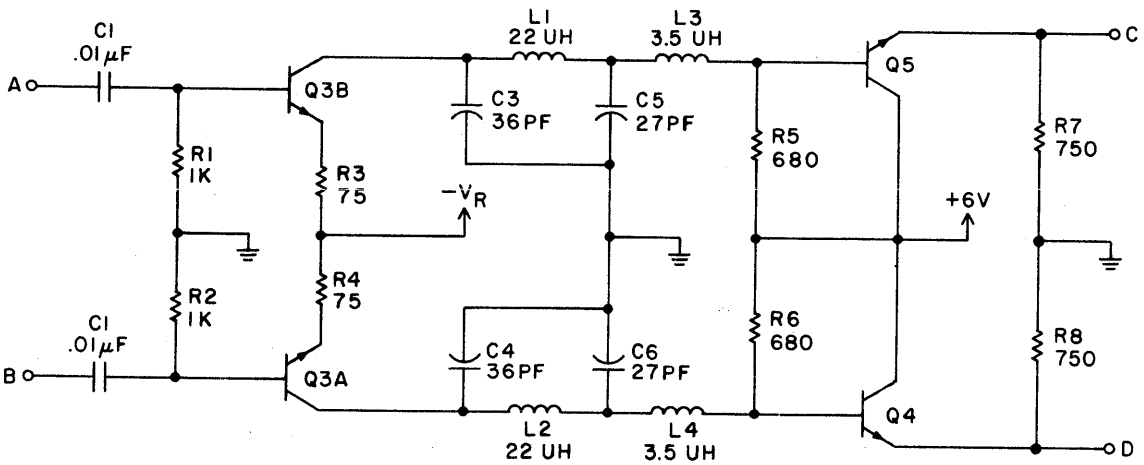
The input capacitors C1 and C2 in conjunction with resistors R1 and R2 give the circuit a low frequency cutoff (-3 db point) of less than 20 kHz.

The output is a differential buffer consisting of Q4, Q5, R7, and R8 that is used to reduce the output impedance and give more drive.

The constant current source for the differential amp supplies approximately 4.75 ma.





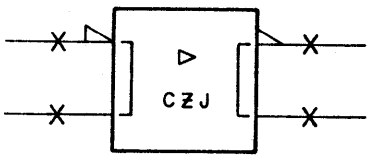


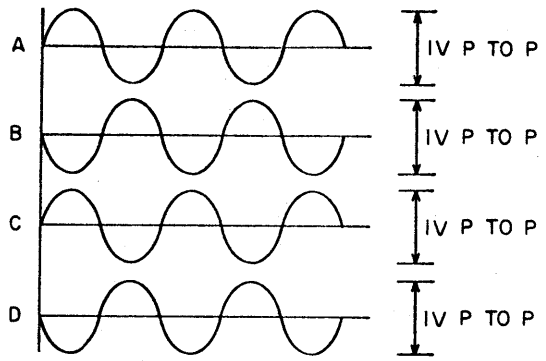
NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

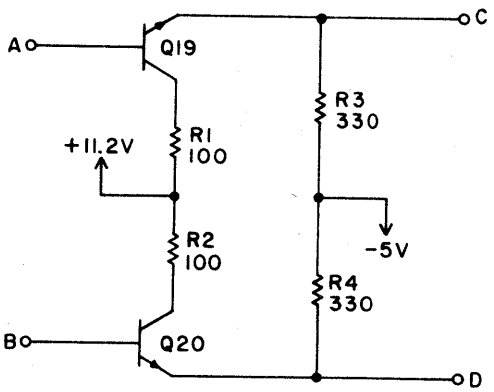
BZJ
Rev A
Sheet 1 of 1

BUFFER AMPLIFIER - CZJ

The CZJ circuit is a buffer amplifier designed to increase the output signal driving capability of a differentially amplified signal. Q19 and Q20 are emitter followers that present comparatively high input impedance and low output impedance.







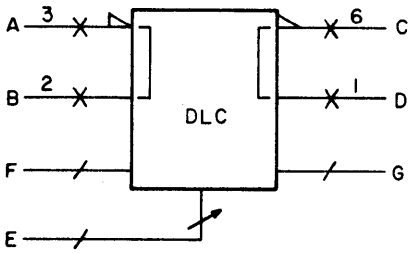
NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

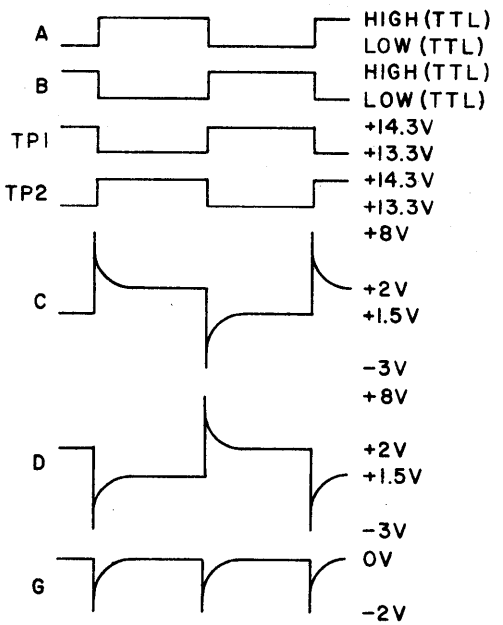
CZJ
Rev A
Sheet 1 of 1

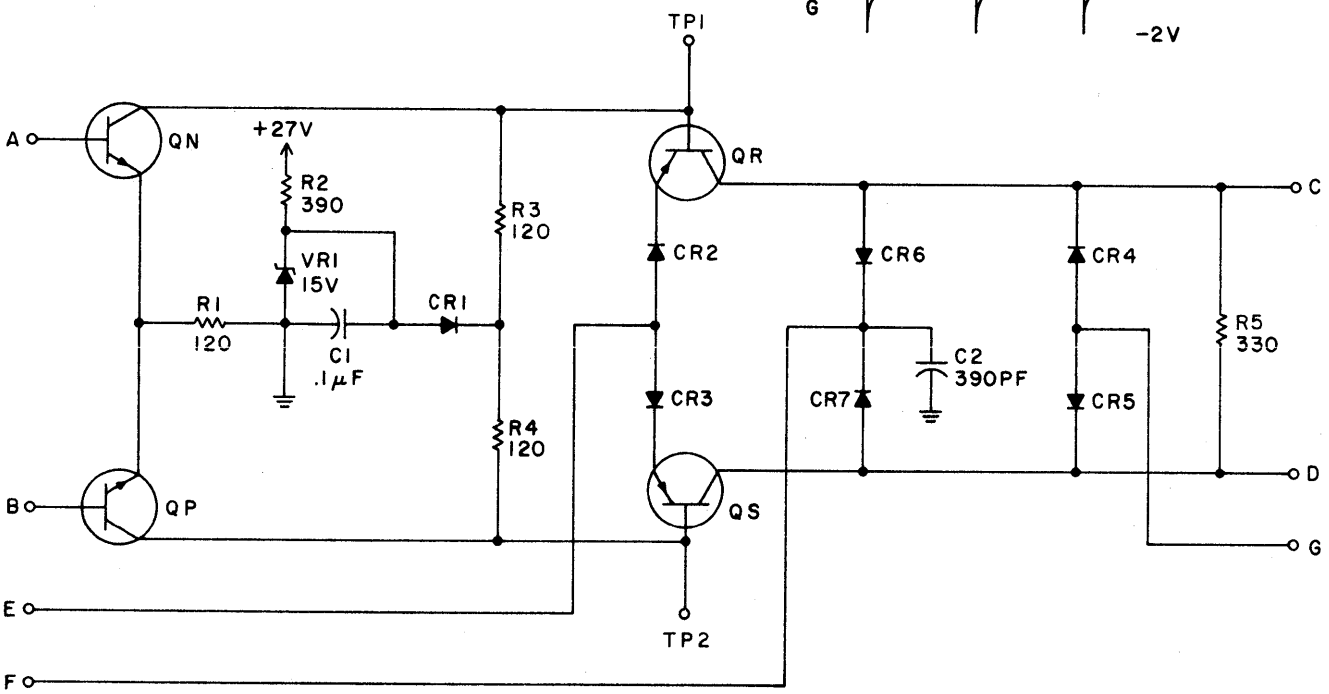
WRITE DRIVER -DLC

The DLC circuit is a differential current switch which converts voltage input signals to current for driving a differential recording head.

TTL level signals are applied to inputs A and B. Transistors QN and QP drive the bases of transistors QR and QS to control current to the head. The current source is connected to input E and supplied to the emitters of transistors QR and QS through diodes CR2 and CR3. Differentiated current is available to the head at outputs C and D. Diodes CR6 and CR7 provide a path to ground for write current when input F is grounded by a write protect circuit. Diodes CR4 and CR5 rectify the echo pulses from the head and apply them to a write voltage fault circuit through output G.







NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

DLC
Rev B
Sheet 1 of 1

Rectifier - DZJ

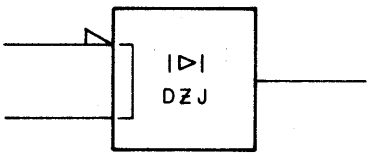
The DZJ circuit is a full wave rectifier with a differential input and single ended output.

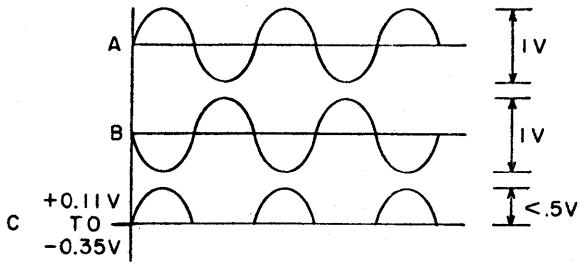
The rectifier consists of a matched pair of transistors (Q1A and B) used as a differential pair. Q1A and Q1B conduct during the positive half input cycle and back biased during the negative half input cycle. Q2 is used as a constant current source supplying about 4.5 ma.

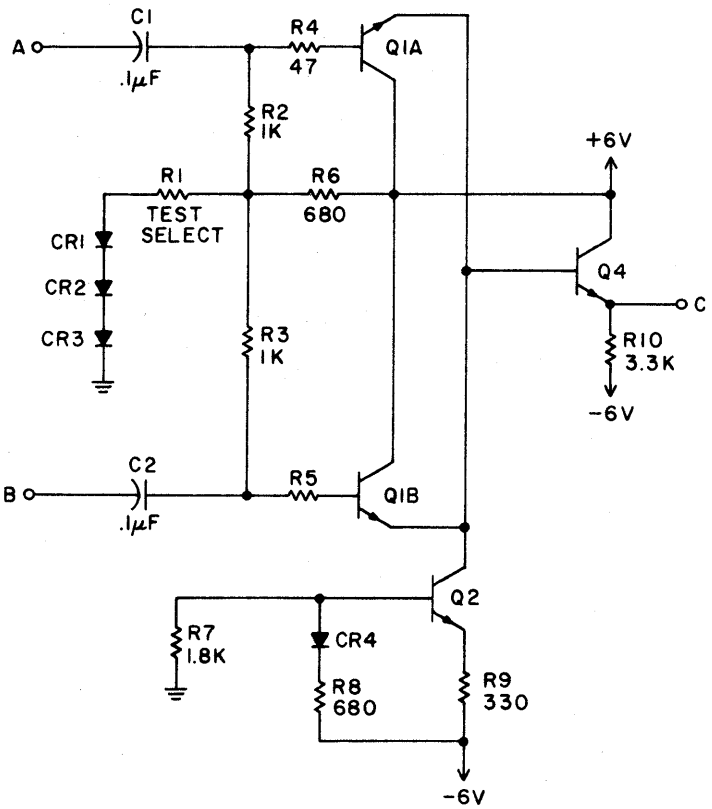
Diodes CR1, 2, and 3 along with test select R1 and R2 form an adjustable bias network. This adjusts the DC base line at output C from about -0.35v to +0.11v and is set so that the output of the AGC amplifier is 2v p-p.

The output buffer amplifier is Q4 and presents a comparatively high input impedance and a low output impedance.

The input frequence response is greater than 2 kHz.







NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

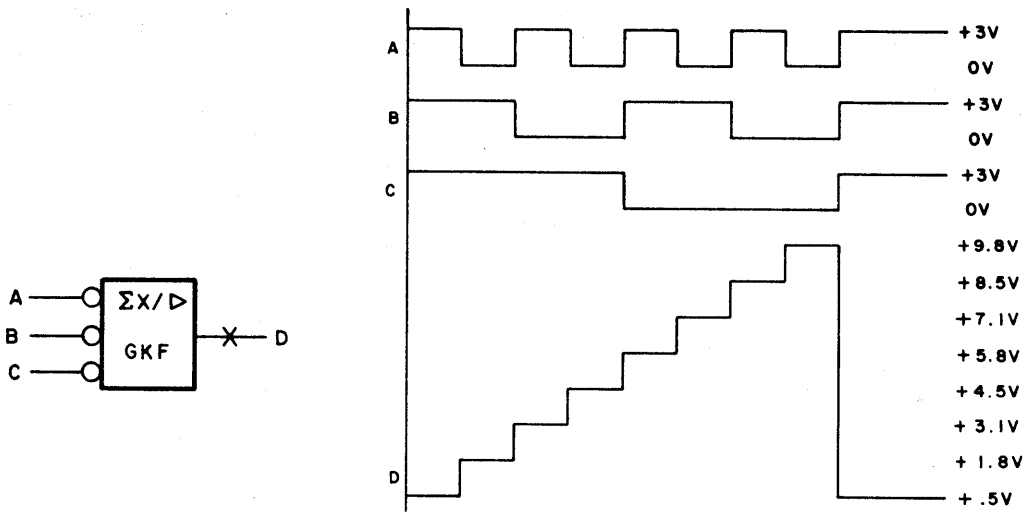
DZJ
Rev A
Sheet 1 of 1

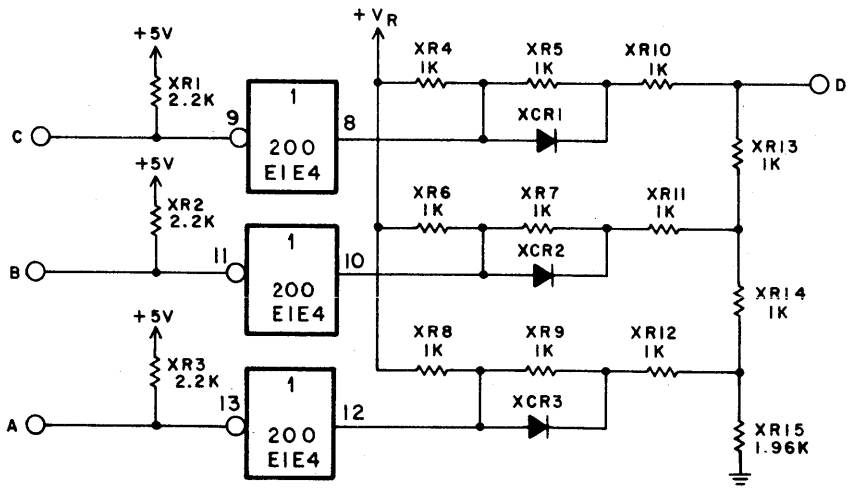
DIGITAL TO ANALOG CONVERTER - GKF

The GKF circuit converts three digital input signals to an analog output whose level depends upon the logical combination at the inputs.

The element 200 is an open collector IC. When pin 9 of element 200 is +3 volts or a "1", its output (pin 8) is 0 volts. When pin 9 is 0 volts or a "0", its output (pin 8) is open and the resistor divider (XR4, XR10, XR13, etc.) to V_r determine the voltage at an identical manner but have less influence on the voltage at point D because of their entry connection in the resistor network.

When V_r is +12 volts the output at D corresponding with the various combinations of logic input is as shown in the waveform diagram.





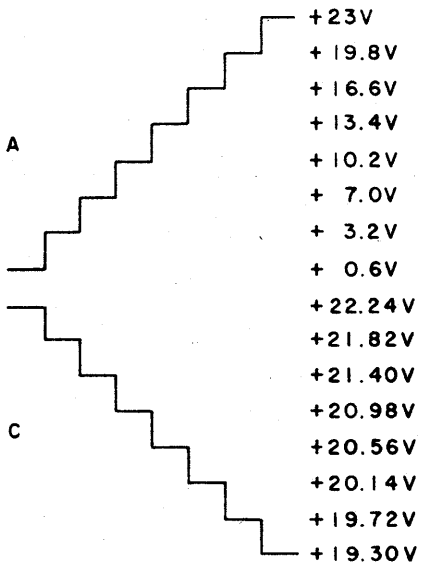
NOTE:
VOLTAGE AND COMPONENENT VALUES ARE FOR REFERENCE ONLY. 7J14

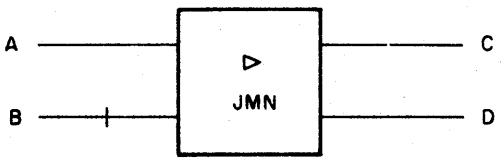
GKF
Rev A
Sheet 1 of 1

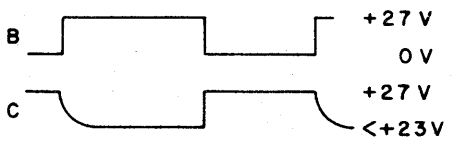
VOLTAGE CONTROLLED CURRENT SOURCE - JMN

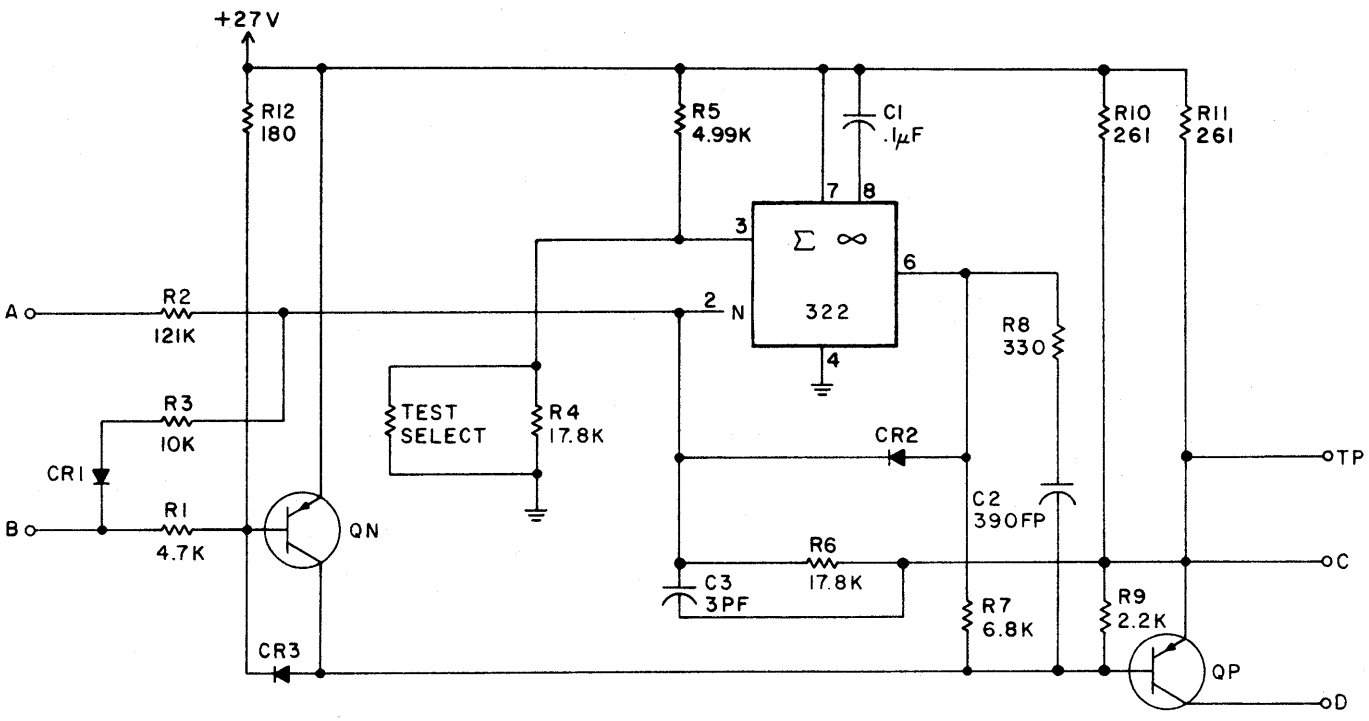
The JMN circuit accepts an analog input voltage and converts it to a voltage controlled current for the write driver.

The JMN circuit receives the analog output of a digital to analog converter. The 322 operational amplifier in the JMN circuit inverts the analog input at A and translates the voltage level to drive the base of current source transistor QP. Write current output is supplied at output D. Current sensing is provided at output C so that other circuitry can test for proper current level output. Control from a write current protect circuit is applied to input B. Current is supplied at output D when input B is +27V. Current source transistor QP is shut off when input B goes to ground.







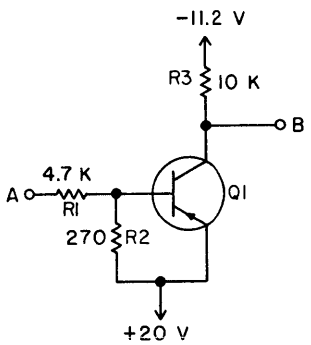


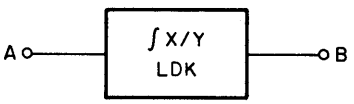
NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

JMN
Rev B
Sheet 1 of 1

DRIVER - LDK

The LDK circuit is a driver that performs level shifting of the Read Enable signal. During read operations, it switches +20 V to pin B, and this forward-biases the diodes in the read circuit. During write operations, it switches -11.2 V to pin B. This reverse-biases the diodes in the read circuit and turns on clamp circuit AAC.

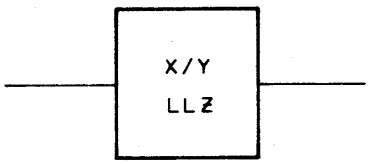


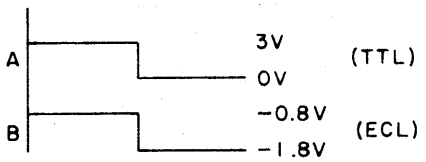


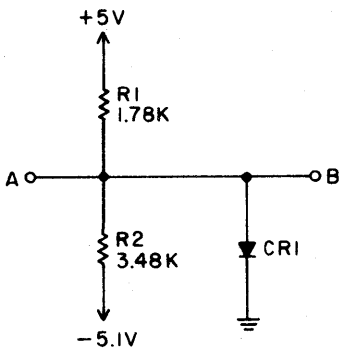
LDK
Rev A
Sheet 1 of 1

PASSIVE TRANSLATOR (TTL TO ECL) - LLZ

R3 and R2 form a resistor divider that changes normal (and worst case) TTL levels into normal (and worst case) ECL levels. A "1" TTL will translate into a "1" ECL. R1 serves as a pullup in case there is no input and causes a "1" to be outputted. CR1 is a germanium clamp to limit the output voltage to +0.2 in case an input voltage of +5 or greater is applied.



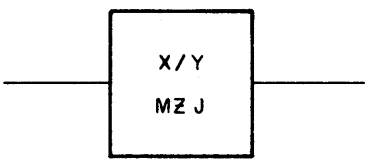


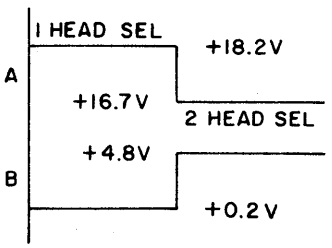


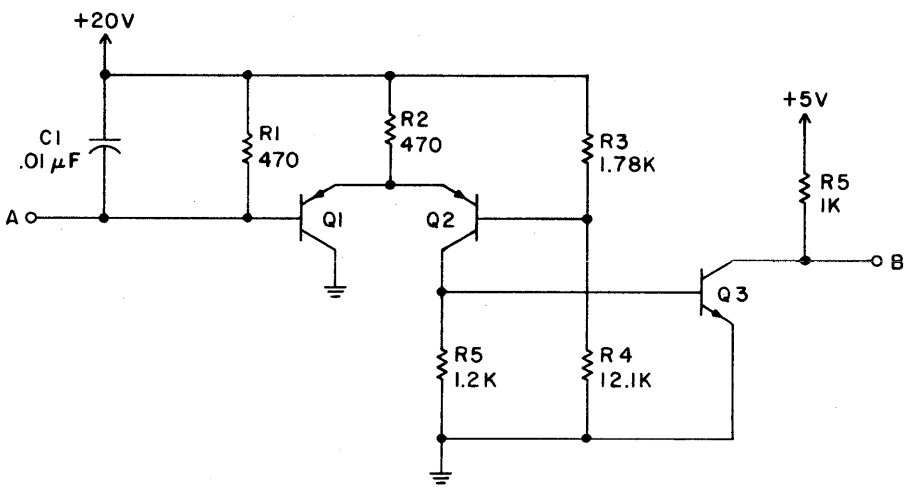
NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

Level Translator - MZJ

The multiple select fault circuitry uses a differential voltage comparitor to sense if two or more heads are selected. A voltage reference of +17.4v is established at the base of Q2 with no head selected. With one head selected the voltage at the base of Q1 will be 18.2v, thus Q2 and Q3 will conduct keeping the output of Q3 low (TTL level) indicating no fault. If two or more heads are selected at the same time the base voltage at Q1 will be 16.7v or greater causing Q1 to conduct and Q2 and Q3 to turn off. The output will then go high a (TTL level) indicating a fault.







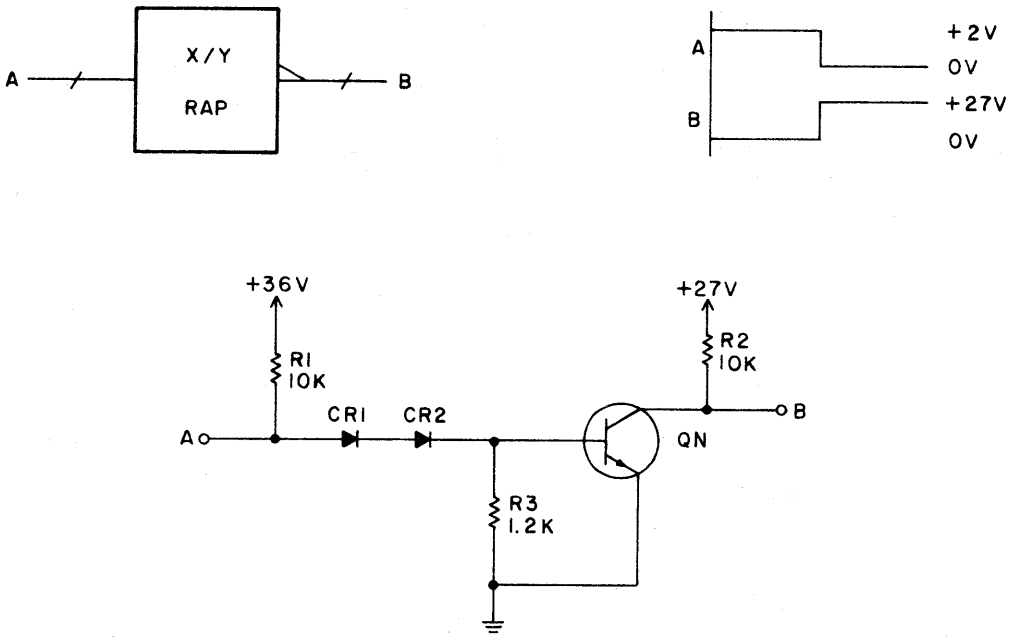
NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

MZJ
Rev A
Sheet 1 of 1

WRITE PROTECT CLAMP - RAP

The RAP circuit acts as a clamp, changing its output impedance path from high to low when the input is switched high.

When the input at A is low (TTL) Q1 is turned off, and the impedance from B to ground is high. When A is switched high (TTL) Q1 is turned on, providing a low impedance path between output B and ground for the write current.



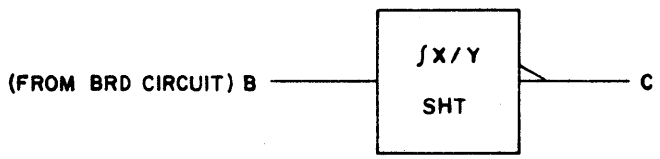
NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

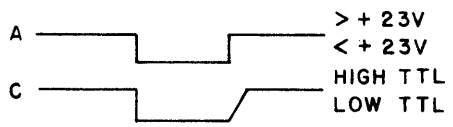
RAP
Rev B
Sheet 1 of 1

LEVEL TRANSLATOR (OUTPUT SECTION) - SHT

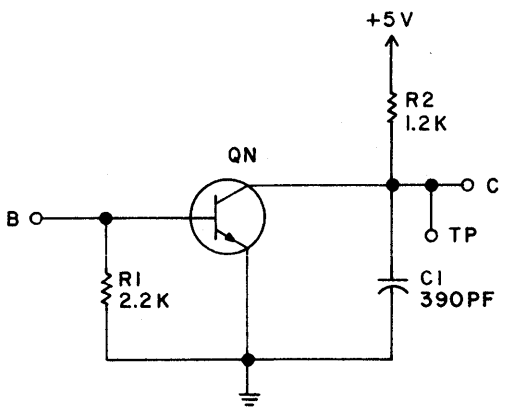
The SHT circuit provides a TTL compatible output for the comparator section of a level translator.

The SHT circuit functions in conjunction with the BRD circuit to indicate whether or not the write current is below a minimum value. (See BRD circuit description.) The output of the BRD circuit provides bias for transistor QN to turn it on or off. When the write current falls below +23V, QN is turned on to provide a low level TTL output. When the write current is above +23V, QN is turned off to provide a high level TTL output.





NOTE: A IS INPUT TO BRD CIRCUIT
C IS OUTPUT OF SHT CIRCUIT

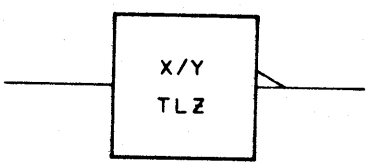


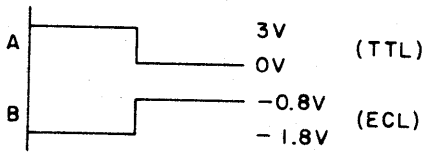
NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

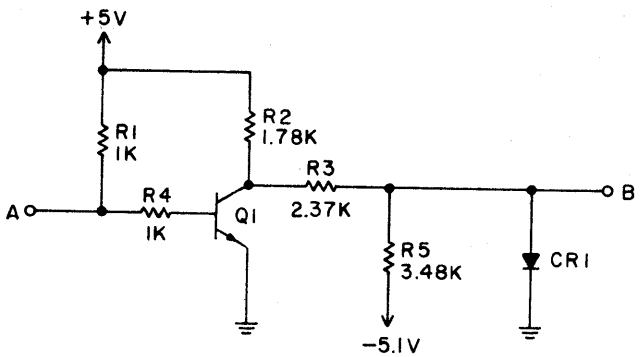
SHT
Rev B
Sheet 1 of 1

INVERTING TRANSLATOR (TTL TO ECL) - TLZ

The first part, consisting of R_1, R_4 and Q_1 form a simple transistor inverter to turn TTL "1's" into TTL "0's". The second part, R_2, R_3, R_5, and CR_1, form a LLZ passive translator which produces ECL levels from TTL inputs.







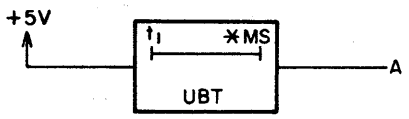
NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

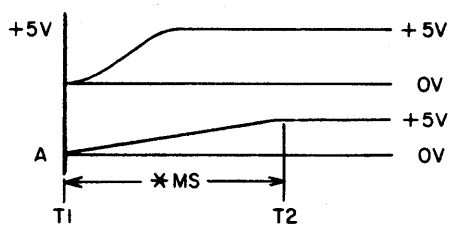
TLZ
Rev A
Sheet 1 of 1

DELAY - UBT

The UBT delay circuit delays application +5 volts to a standard TTL gate during a power up sequence.

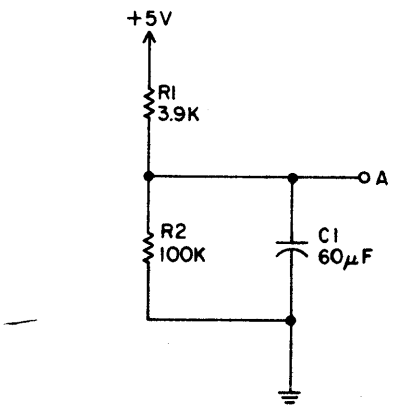
Applying +5v (T1) slowly raises output A to +5 volts as C1 is charging. As the voltage across C1 approaches 5 volts, output A raises to 5 volts after a specific delay time determined by the values of R1, R2, and C1.





* TYPICAL DELAY TIMES

R1	R2	C1	DELAY TIME
3.9K	100K	60μF	80 MS
6.8K	10K	60μF	30 MS



NOTE:
VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

UBT
Rev A
Sheet 1 of 1

DELAY - UC-

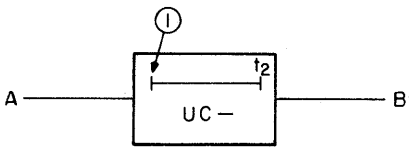
The UC-delay circuit is used to delay open-collector integrated circuits. The circuit delays a "1" input before providing a "1" output at B. The delay time for a "0" pulse is negligible. The delay circuit consists of a resistor connected to +5v and a capacitor connected to ground.

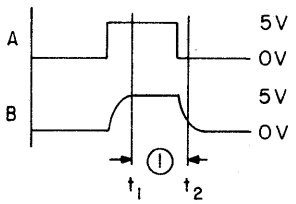
Assume that a "0" (ground) enters at A. If the capacitor is discharged, it remains discharged. The output is an immediate "0". If the capacitor is charged when the "0" signal enters, it discharges almost instantaneously. The "0" appears at output B with no noticeable delay.

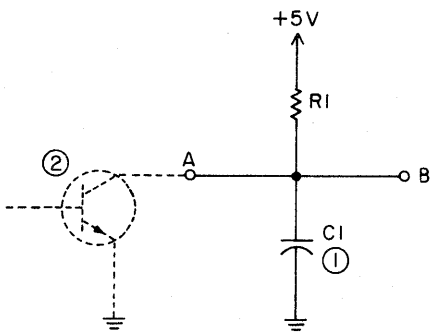
If a "1" (+3.0v) enters at A, and the capacitor is discharged, the capacitor must first charge to a minimum "1" voltage (typically +0.7v) before the "1" appears at output B. The time necessary to charge the capacitor to this minimum voltage is the delay time of the circuit. The charge time is dependent on the value of the capacitor, the value of the resistor, and the minimum voltage required to produce a "1" response.

Characteristics of the UC-circuits are as follows:

Circuit Type	Capacitance	Resistance	Delay
UCM	5600PF	1.2K	1.5US
UCP	5600PF	560	0.8US
UCR	5600PF	1K	1.3US
UCS	3.3UF	2.2K	1MS
UCV	270PF	2.61K	175NS
UCY	200PF	10K	200NS







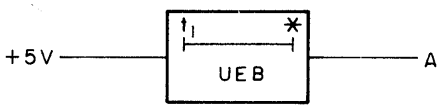
NOTES:
① DELAY TIME DEPENDENT ON CIRCUIT TYPE.
② OPEN COLLECTOR TRANSISTOR IN PRECEDING STAGE.

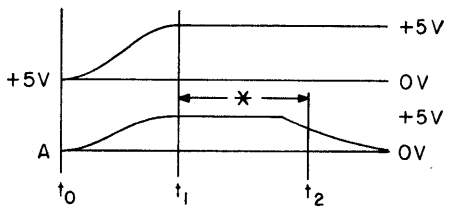
UC-
Rev B
Sheet 1 of 1

DELAY - UEB

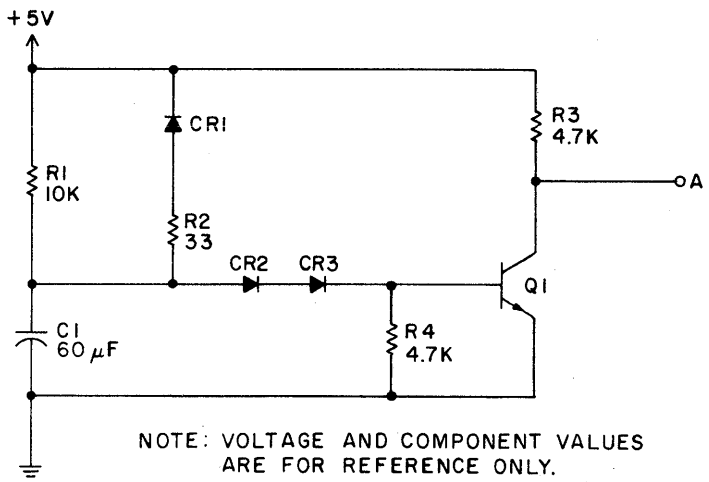
The UEB circuit delays application of ground to a standard TTL gate during a power-up sequence.

During power off phase (T_0), capacitor C1 is discharged by R4, CR2, and CR3. Applying +5v power (T_1) raises output A to +5v as power comes up. At this time (T_1) Q1 is off and C1 is charging. As the voltage across C1 approaches 5 volts, Q1 turns (T_2) on reducing output A to about 0 volts.





* DELAY TIME VARIES WITH COMPONENT VALUES, SEE LOGIC DIAGRAMS FOR SPECIFIC DELAY TIME.



NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

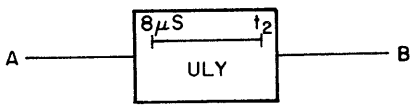
UEB
Rev A
Sheet 1 of 1

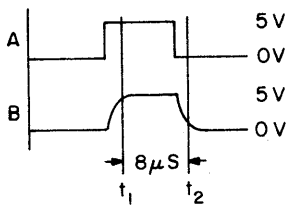
DELAY - ULY

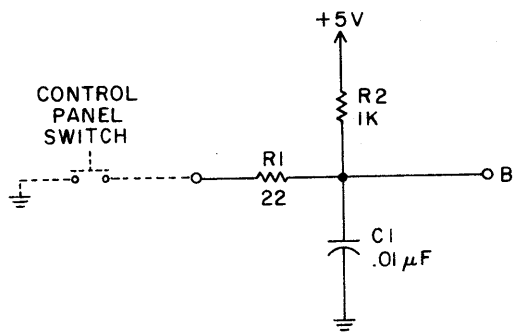
The ULY-delay circuit delays a "1" input before providing a "1" output at B. The delay time for a "0" pulse is negligible. The delay circuit consists of a resistor connected to +5v, a capacitor connected to ground, and a series input resistor.

Assume that a "0" (ground) enters at A. If the capacitor is discharged, it remains discharged. The output is an immediate "0". If the capacitor is charged when the "0" signal enters, it discharges almost instantaneously. The "0" appears at output B with no noticeable delay.

If an open circuit ("1") enters at A, and the capacitor is discharged, the capacitor must first charge to a minimum "1" voltage (typically +0.7v) before the "1" appears at output B. The time necessary to charge the capacitor to this minimum voltage is the delay time of the circuit. The charge time is dependent on the value of the capacitor, the value of the resistor, and the minimum voltage required to produce a "1" response.







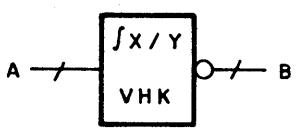
NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

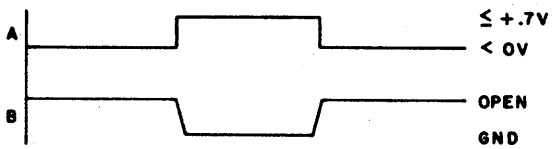
ULY
Rev A
Sheet 1 of 1

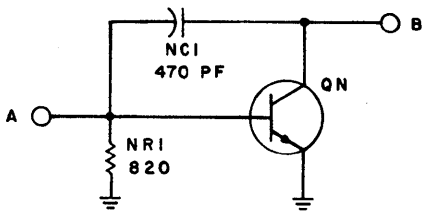
INTEGRATING LEVEL TRANSLATOR - VHK

The VHK circuit is a voltage level shifter that slows down and controls "turn on" and "turn off" transition times.

With an input to A of +.7 volts or greater (current limited to 20 ma), QN turns on with output B going to ground at a rate controlled by collector-base feedback capacitor NC1. With an input of 0 volts to -3 volts, QN turns off and output B is disconnected from ground.







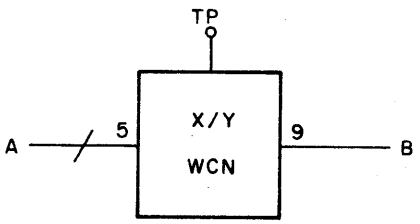
NOTE:
VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY. 7J40

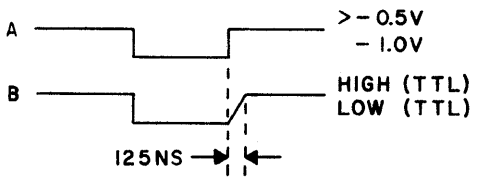
VHK
Rev A
Sheet 1 of 1

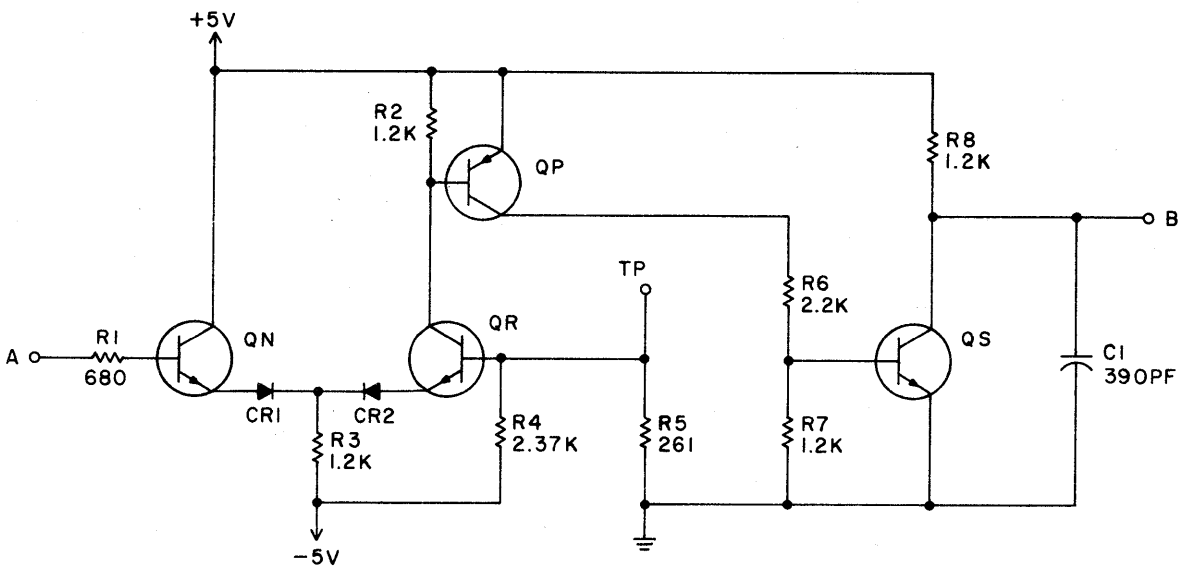
LEVEL TRANSLATOR - WCN

The WCN circuit translates input signal levels of below -0.5 V to a low TTL level output and input signal levels of above -0.5 V to a high TTL level output.

The WCN circuit has a differential voltage comparator circuit to indicate whether the write driver is on or off. A voltage reference of -0.5 V is applied to the base of transistor QR. When the write driver is off, the voltage at the base of transistor QN is -1 V, turning off QN. Therefore, transistor QR is turned on and its collector voltage goes low, turning on transistor QP. Transistor QS is then forward biased providing a low TTL output. If the write driver is on, the voltage to the base of QN goes above -0.5 V (less negative) and QN is turned on. As a result QR, QP, and QS are turned off, providing a high TTL output. Capacitor C1 delays the low to high transition by 125 ns.







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