83337530

CONTROL DATA

DISK STORAGE SUBSYSTEM

CDC 33800
CDC 895
HIS MSU 8200

BZ640

BZ8G1

BZ8H1

FV716

FV7A5

TROUBLESHOOTING INTRODUCTION
ROUTINE DESCRIPTIONS
OPERATING PROCEDURES

HARDWARE DIAGNOSTIC REFERENCE MANUAL

REVISION RECORD

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REVISION LETTERS I, O, Q AND X ARE NOT USED.

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or use Comment Sheet in the back of this manual.

LIST OF EFFECTIVE PAGES

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S-1B Div	-	1C-10	C
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1C-76	D	1D-29	D
1C-77	C	1D-30	D
1C-78	D	S-2 Div	-
1C-79	D	Blank	-
1C-80	D	2-1	D
1C-81	D	2-2	C
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Blank	-	2A-41	D
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2A-3	C	2A-44	D
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2A-8	D	2A-49	D
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2A-11	D	2A-52	D
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2A-14	D	2A-55	D
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2A-17	D	2A-58	D
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2A-19	D	2A-60	D
2A-20	D	S-3 Div	-
2A-21	D	Blank	-
2A-22	D	3-1	C
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2A-25	D	3-4	C
2A-26	D	3-5	C
2A-27	D	3-6	C
2A-28	D	3-7	D
2A-29	D	3-8	C
2A-30	D	3-9	C
2A-31	D	3-10	C
2A-32	D	3-11	C
2A-33	D	3-12	C
2A-34	D	3-13	C
2A-35	D	3-14	D
2A-36	D	3-15	D
2A-37	D	Blank	-
2A-38	D	S-3A Div	-
2A-39	D	Blank	-

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3A-1	C	3A-23	D
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3A-5	C	3A-27	D
3A-6	C	3A-28	D
3A-7	C	S-3B Div	-
3A-8	C	Blank	-
3A-9	C	3B-1	C
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PREFACE

INTRODUCTION

This manual contains troubleshooting information for customer engineers and other technical personnel who will be maintaining the CONTROL DATA® FV716/FV7A5 Head of String Controller (HSC) and BZ640/BZ8G1/BZ8H1 Disk Storage Unit (DSU).

The CDC 33800, CDC 895, and MSU 8200 disk storage subsystems are physically identical; however, the 33800 is used on IBM systems, the 895 is used on CDC systems, and the 8200 is used on HIS systems. Therefore, any internal reference in this manual pertaining to SOLEX, EREP, and OLTEP apply only to 33800 subsystems used with IBM systems.

Abbreviations are listed on page xxix.

Terminology used in this manual is as follows:

- The term "controller" refers to the next higher-level unit to which the DSU is connected.
- The terms "DSU" and "drive" are interchangeable.
- The term "device" refers to one of four possible devices (spindles) that comprise a DSU. The terms drive and device, therefore, are not interchangeable.

MANUAL ORGANIZATION

Information in this manual is divided into four sections:

- Section 1 -- Troubleshooting Introduction: provides general background information explaining the troubleshooting philosophy, troubleshooting technique, and general reference information helpful in analyzing a problem. Also contains sense information and power troubleshooting procedures.
- Section 2 -- Inline Diagnostics/Utilities: contains descriptions of inline diagnostic routines and tests, along with utility routines.

- Section 3 -- Operating Procedures: contains procedures for running diagnostic and utility routines from the maintenance panel.

- Section 4 -- Terminal Operating Procedures: contains a procedure for running diagnostics and utility routines from the terminal.

OTHER MANUALS

For error code information, refer to the Troubleshooting Guide, Publication Number 83337540.

Refer to the Disk Memory Subsystem Installation Manual (Publication Number 83321400) for the following information:

- A list of all manuals needed to maintain and troubleshoot the HSC and DSU. (This information is contained in the Preface of that manual.)

- A list of all available microprogram disks. (This information is contained in section 1 of that manual.)

- A list of all applicable equipment numbers.

CONVENTIONS

Conventions used in this manual are:

- Logical zero and logical one are abbreviated as 0 and 1, respectively.

- Bytes and bits are numbered from left to right, beginning with 0.

- The leftmost byte/bit is most significant; the rightmost bit is least significant.

- "X" in a bit position indicates unknown or don't care.

- All address references are hexadecimal.

CONTENTS

FIGURES

TABLES

ABBREVIATIONS

A/D	Analog-to-Digital
AAR	Arm Address Register
ACK	Acknowledge
ACT	Actuator, Active
ADD	Address
ADDR	Address
ADDRS	Address
ADR	Address
ADSP	A Display
AGC	Automatic Gain Control
ALT	Alternate
ALU	Arithmetic-Logical Unit
AM	Address Mark
AMP	Amplifier
AUX	Auxiliary
BDSP	B Display
BIB	Bus In Bit(s)
BIDIR	Bidirectional
BLK	Black, Block
BLU	Blue
BOB	Bus Out Bit(s)
BRN	Brown
BUF	Buffer
CAL	Calibration
CAR	Cylinder Address Register
CBUS	Control Bus
CC	Condition Code
CCA	Connection Check Alert
CCW	Channel Command Word
CDP	Controller to Device Port
CE	Customer Engineer, Channel End
CH	Channel
CHAN	Channel
CHK	Check
CIAR	Current Instruction Address Register
CIC	Carry In Control
CIF	Channel Interface
CK	Check
CKD	Count/Key/Data
CLA	Carry Look Ahead

ABBREVIATIONS (Contd)

CLK	Clock
CMD	Command
CMI	Command Modifier Information
CMP	Compensate
CMPR	Compare
CMPTR	Comparator
CNT	Count
CNTR	Counter
CNTRL	Control
CODEC	Coder/Decoder
COIN	Coincidental
COL	Column
COM	Common
COMP	Complete, Compensate/Compensation
COMPD	Compensated
COND	Condition
CONF	Configuration
CPU	Central Processing Unit
CS	Control Storage
CSM	Control Store Memory
CSW	Channel Status Word
CTLR	Controller
CTRL	Control
CTS	Clear to Send
CYL	Cylinder
DB1	Data Byte 1
DBI	Device Bus In
DBO	Device Bus Out
DBUS	Data Bus
DCC	Device-to-Controller Connection
DDC	Director-to-Device Controller
DEC	Decode, Decrement
DECR	Decrement
DEV	Device
DEV-I	Device Interface
DIFF	Difference
DISC	Disconnect
DLD	Delayed
DM	Data Memory
DP	Diagnostic Processor

ABBREVIATIONS (Contd)

DPOS	Diagnostic Processor Operating System
DPSE	Dynamic Path Selection Extended
DRVR	Driver
DSU	Disk Storage Unit
DTB	Data Transfer Buffer
DTI	Device Tag In
DTO	Device Tag Out
DVC	Device
EC	Error Code
ECC	Error Correction Code
ECO	Engineering Change Order
EMS	Electronic Media Switch
EN	Enable, Enabled
EPROM	Erasable Programmable ROM
ERDS	Error Recording Data Set
EREP	Environmental Recording, Editing, and Printing
ERP	Error Recovery Program (or procedure)
ERR	Error
EXEC	Execute
FCN	Function
FCO	Field Change Order
FDBK	Feedback
FMT	Format
FPLS	Field Programmable Logic Sequencer
FREQ	Frequency
FRU	Field-Replaceable Unit
FSC	Fault Symptom Code
GBID	Guardband Inner Diameter
GBOD	Guardband Outer Diameter
GND	Ground
GRN	Green
GRY	Gray
HA	Home Address
HAR	Head Address Register
HD	Head
HDA	Head/Disk Assembly
HEX	Hexadecimal
HI	High

ABBREVIATIONS (Contd)

HSC	Head of String Controller
I/O	Input/Output
IAR	Instruction Address Register
ICTR	Instruction Counter
ID	Identifier, Identification
IML	Initial Microcode Load
INC	Increment
INCR	Increment
INP	Input
INS	Installed
INST	Instruction
INSTR	Instruction
INT	Interrupt, Internal
INTR	Internal
INTRPT	Interrupt
IO	Input/Output
JMP	Jump
JSR	Jump to Subroutine
KEBD	Keyboard
LA	Locator A
LB0	Locator B, Byte zero
LO	Low
LSB	Least Significant Bit
LSI	Large Scale Integration
MAX	Maximum
MB	Megabytes
MD	Maintenance Device
MDI	Memory Data In
MDO	Memory Data Out
MEM	Memory
MISC	Miscellaneous
MOD	Module
MOS	Metal Oxide Semiconductor
MP	Maintenance Panel
MPCU	Master Power Control Unit
MPL	Microprogram Load
MPU	Microprocessor Unit
MPX	Multiplex Channel
MSB	Most Significant Bit
MSG	Message

ABBREVIATIONS (Contd)

MTD	Microcode Trace Device
MULT	Multiple
MUX	Multiplexer/Selector
NEUT	Neutral
NMI	Non-maskable Interrupt
NOTIF	Notification
OE	Output Enable
OP	Operation
ORN	Orange
OVFLW	Overflow
P	Parity
PA	Physical Address, PROM Address
PAC	Primary to Alternate Connection
PAR	Parity
PC	Parity Checker
PCH	Pack Change
PCI	Program-Controlled Interrupt
PCU	Power Control Unit
PIA	Peripheral Interface Adapter
PLB10	Pipeline B, bit 10
PLL	Phase Lock Loop
PLO	Phase Lock Oscillator
PLR	Pipeline Register
POLY	Polynomial
POR	Power On Reset (or Request)
POS	Positive
PRGM	Program
PRI	Primary
PROM	Programmable Read Only Memory
PWR	Power
QUAL	Qualification
R/W	Read/Write
RO	Record Zero
RAM	Random Access Memory
RCC	Request Connection Check
RCV	Receive
RCVR	Receiver
RD	Read
REF	Reference
REG	Register

ABBREVIATIONS (Contd)

REQ	Request
RES	Reserved
RGTR	Register
ROM	Read Only Memory
RPS	Rotational Position Sensing
RST	Reset
RTA	Remote Technical Assistance
RTN	Routine, Return
RTS	Request To Send
S/C	Series Code
SAR	Stack Address Register
SB	Sync Byte
SC	Storage Control (cabinet)
SD	Storage Director
SEC	Secondary
SEL	Select
SEQ	Sequence
SERDES	Serializer/Deserializer
SEW	Subsequent Error Word
SHDW	Shadow
SP	Stack Pointer
SPCU	Slave Power Control Unit
SPS	Switcher Power Supply
ST	Status
SW	Switch
SYNC	Synchronization
SYND	Syndrome
SYS	System
T&D	Test and Diagnostic
T/R	Transmit/Receive
TAR	Target Address Register
TEMP	Temperature
UNCMB	Uncorrected Memory Bit
UNFLW	Underflow
UR	Unit Ready
VIO	Violet
W/	With
W/O	Without
WD	Write Data
WG	Write Gate
WHT	White

WR	Write
WRT	Write
XCVR	Transceiver
XES	Transfer Error Status
XFER	Transfer
XFR	Transfer
XMIT	Transmit
XMT	Transmit
XMTR	Transmitter
XOR	Exclusive-OR
YEL	Yellow

SECTION 1

TROUBLESHOOTING INTRODUCTION

TROUBLESHOOTING INTRODUCTION 1

INTRODUCTION

The main objective of this manual is to help you repair failures quickly. To accomplish this objective, the main emphasis is "How to Fix" instead of "How it Works."

The section is divided as follows:

- Section 1 - General background information and troubleshooting technique: Explains general information on troubleshooting methods.
- Section 1A - Power: General information on power and troubleshooting power-related problems.
- Section 1B - Fault Symptom Code Index (FSCI): An alphanumeric list of all controller/device Fault Symptom Codes.
- Section 1C - Sense: Descriptions of all controller/device sense information.
- Section 1D - Reference Material: Contains basic reference information.

SAFETY PRECAUTIONS

WARNING

Observe all of the following safety precautions. Failure to do so may cause personal injury or equipment damage.

1. Do not work alone when exposed high voltages are present. Make sure somebody familiar with all power off controls is present.
2. Unplug ac power input cable before performing any maintenance on power cables, RFI filters, power distribution units, or ac cables to dc power supplies. Unswitched high voltages can be present in or near these assemblies.

3. Do not wear watches, rings, or other jewelry. Do not wear loose clothing.

4. Use only insulated pliers and screwdrivers.

5. Make sure that test instruments have insulated probes. Don't let the probes dangle. Also ensure that controls are set correctly.

6. Wear safety glasses whenever working with sealants or performing mechanical actions that could cause particles to fly out.

7. Keep tools in good condition. Replace them if worn or broken.

8. Keep tool boxes, test equipment, and removed machine covers out of the way where no one can trip over them.

9. Do not bend over to lift items: stand or push up with your legs. Power supplies (especially power distribution units) and voice coil magnets are very heavy. If an assembly exceeds 11 kilograms (25 pounds), two people are required to lift it.

10. Remove all power from circuits when removing logic cards or other components.

11. Be careful around the drive motors; they can get hot.

12. Maintain good housekeeping before, during, and after completing maintenance.

13. Observe all electrostatic precautions.

14. Do not place tools or other metal objects on top of logic chassis as electrical components may be shorted to ground.

15. Do not place manuals or other documents on top of logic chassis, power supplies, or PCUs as this will block cooling air flow.

ELECTROSTATICALLY SENSITIVE PRECAUTIONS

Metal oxide semiconductor (MOS) integrated circuits are used on the logic boards and I/O boards in the unit. MOS integrated circuits are extremely sensitive and therefore require special

handling to avoid damage caused by static electricity. Observe the following precautions whenever any maintenance is performed:

- Turn off power before removing and installing the logic card.
- Ensure that anything coming in contact with the card is electrically connected to ground; including tools, the body, clothing, containers, etc.
- Plug grounded wrist strap into any one of the banana jacks located as shown in figures 1-1 and 1-2.
- Touch the logic chassis to bleed off any accumulated static charge before removing or installing the card.
- Handle the card only by a noncircuit portion. Do not touch connector pins and circuit connector points.
- Never use an ohmmeter on boards having microprocessor assemblies.
- Always remove the boards before using an ohmmeter on the controller.
- Place the card in a conductive shielded bag immediately following its removal from the unit. The card and the bag must be in contact with logic chassis ground before and during the time that the card is inserted or removed from the bag. The bag should have a warning label indicating that it contains an electrostatic-sensitive device. The logic card must remain in the bag or at a properly prepared work station whenever it is not installed in the logic chassis.

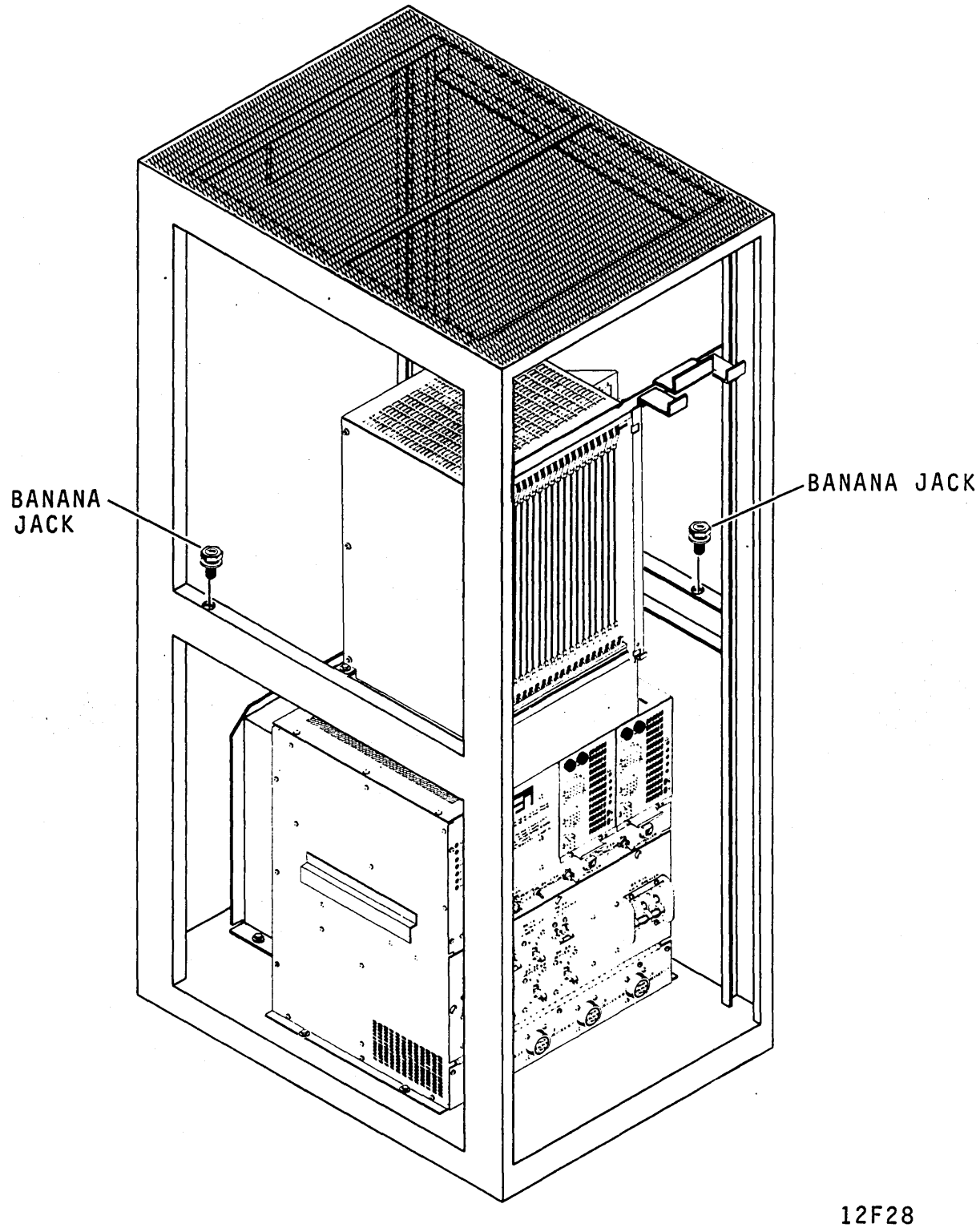

Figure 1-1. HSC Ground Points

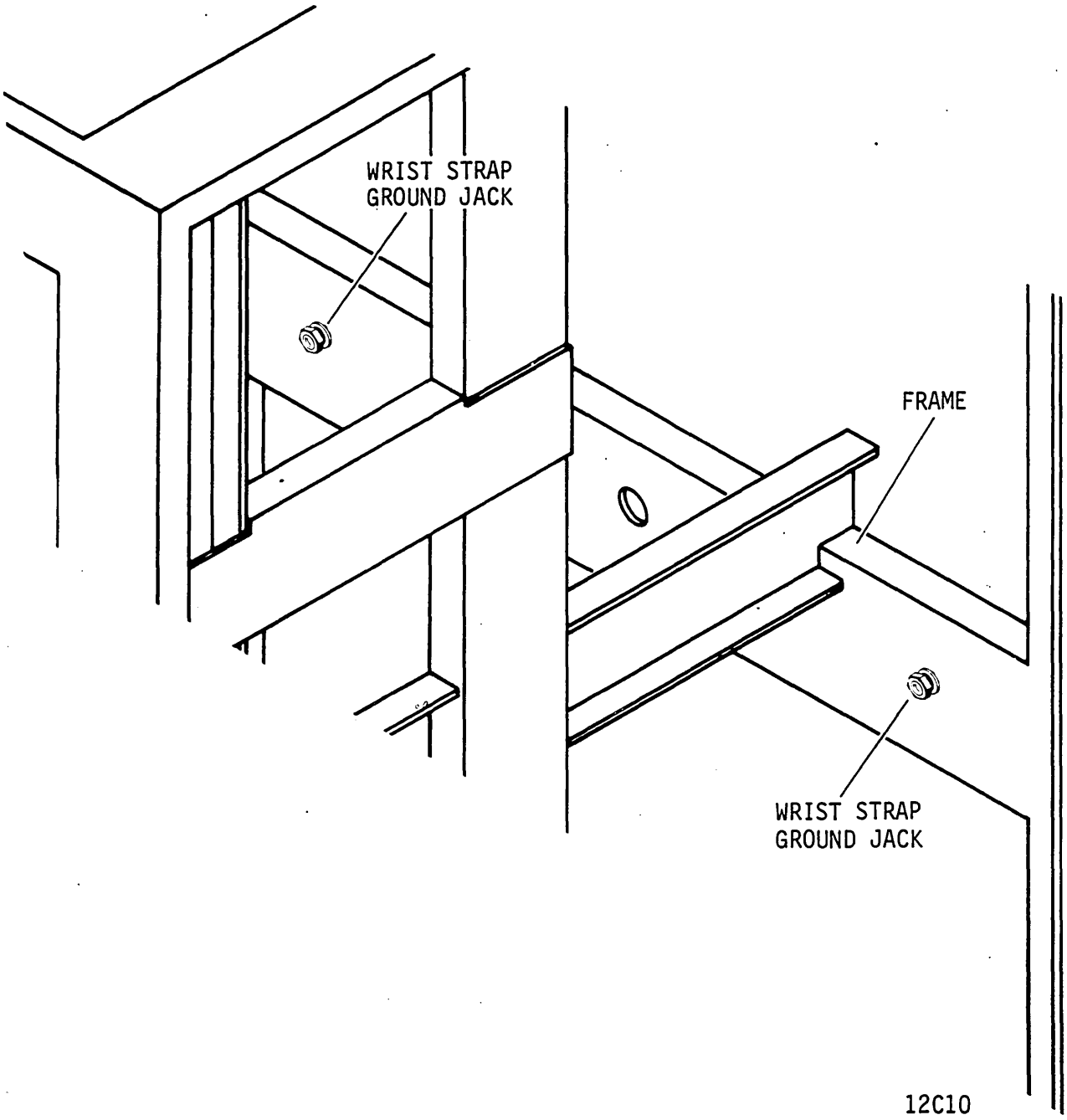

Figure 1-2. DSU Ground Points

TEST EQUIPMENT PRECAUTIONS

Misuse of the HSC convenience outlet may cause temporary equipment or system errors. When you are doing either of the following:

- Plugging (or unplugging) test equipment or other electrical devices into the convenience outlet;
- Turning equipment on or off that is plugged into the convenience outlet;

Make SURE that customer jobs are not running at the time!

USING THE SAM (STRUCTURED ANALYSIS METHOD)

The SAM is a graphic method of documenting conditional sequences, such as commonly found in flowcharts. The SAM is used to troubleshoot when diagnostics cannot be used or, in some cases, to continue troubleshooting where the diagnostics leave off. SAMs use simple "yes" or "no" responses to troubleshooting questions to lead you to appropriate corrective actions. Figure 1-3 is an annotated example of a SAM.

The SAM format is as follows:

Title - Includes a SAM ID number and description at the top of the first page of each SAM.

Page Identification - Each page within a SAM is identified by a sequential page number added to the SAM ID number. This is located in the upper right-hand corner of each SAM page.

Advisory Information - This information follows the title and precedes the fault isolation steps. This information is necessary when using the SAM and contains such things as:

- Intended purpose or application of the SAM.
- Specific warnings for personnel safety, cautions for equipment protection, and/or notes on operational highlights.

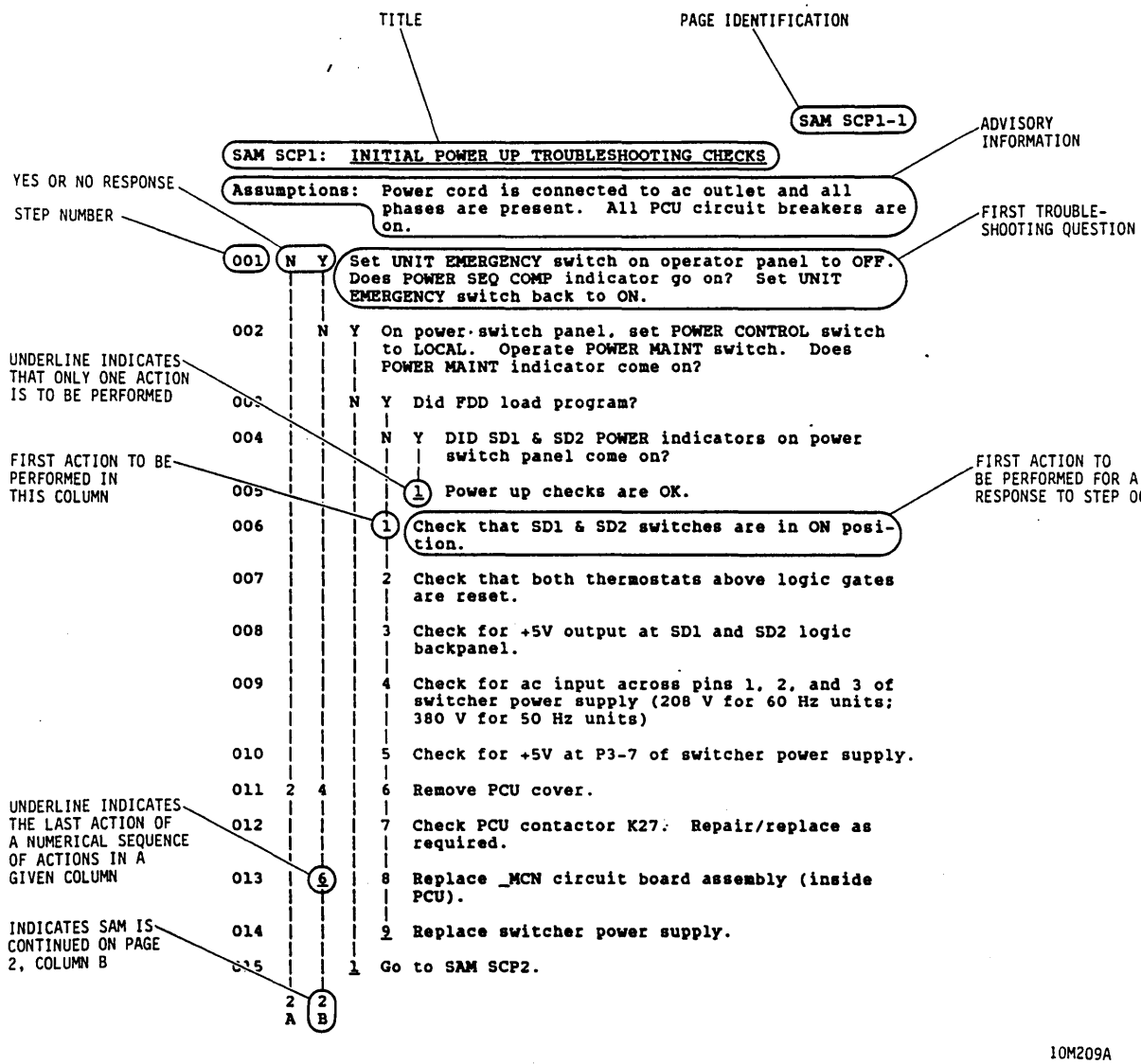

Figure 1-3. SAM Format Example

- Instructions needed to establish the required operation conditions for the following checks.

- Assumptions and/or step number references from other SAMs.

Step Number - Each condition/question and action item in a SAM contains a sequential step number for reference purposes.

Question - Troubleshooting questions that can be answered with a Y (yes) or N (no).

Action Number - Each action is assigned an action number. These action numbers indicate the order in which actions are to be performed. After doing the first recommended action, repeat the test or condition that caused the situation. If the test results or conditions have not changed (same situation), try recommended action 2, and so on, being sure to repeat the test after each action. In general, the numerical sequence of actions reflects the probability of the action correcting the problem, with the most likely as number one. However, this is weighted by the situation where a less probable action is much quicker to perform than the more probable action. Therefore, it may be more expedient in terms of time to first do the quicker action hoping that it may solve the problem. Thus, the order of actions is often a result of careful consideration between the most probable action and the quickest action that has a reasonable probability of being the fix. The last (highest number) action in a given sequence is underlined to indicate the end of the sequence. If there is only one action in a given sequence, it is also underlined.

Footnotes - Numbers in parentheses indicate footnotes. Footnotes may appear at the bottom of the page on which they occur or grouped together on the last SAM page.

Linkage - Multiple page SAMs are linked together by a page number/column letter scheme. All columns that require continuation on another page are identified from left to right as A, B, C, etc. The column letter plus the SAM page number where the column is continued are in a single vertical column as shown in figure 1-4.

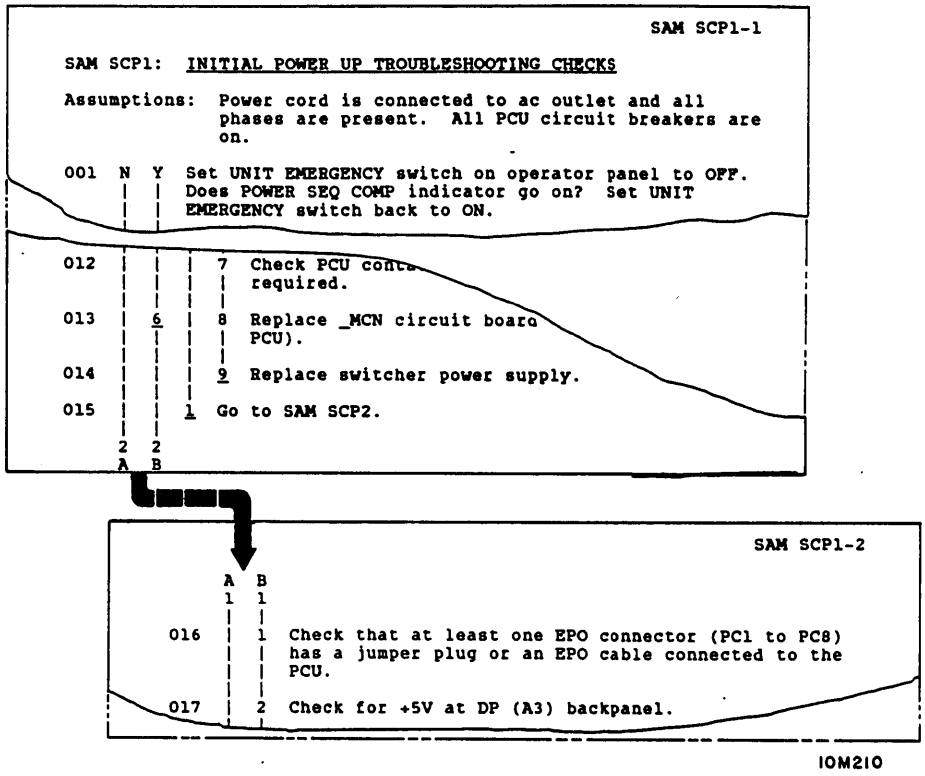

Figure 1-4. SAM Page/Column Linkage

When using a SAM, first read the advisory information and do whatever is required. Next read the first question and answer it Y or N. Then follow the selected column down to the next question and a list of action items.

TROUBLESHOOTING TECHNIQUE

Troubleshooting is a way of thinking and not a specific act. In order to be able to solve specific problems, the way of thinking must be well ordered. It is especially important that the thought process be kept well ordered when using automatic test methods. Because of the speed and quantity of data presented by automatic testing, it is often easy to overlook details that help to define a problem. A problem is some deviation from a standard, that is, a definable change in an accepted level of performance. In order to solve the problem, the following steps must be accomplished:

1. Collect all available data.
2. Define extent or nature of deviation.
3. Propose theory of cause, according to above data.
4. Test theory.

In addition to general troubleshooting methods, on-line error analysis methods are also discussed.

COLLECT AVAILABLE DATA

The collection of data must be the first step in the correction process. Since a problem rarely, if ever, identifies itself completely, it is necessary to collect all available information. This must be done with an open mind. Therefore, before going to step 2, assemble and record (WRITE DOWN) all data. Facts not recorded have a habit of adjusting themselves to fit the theory of the moment.

The type of data reasonable to collect depends on how well the original problem is defined. Following is a listing of various types of information that are helpful:

- Operator's description of problem. Remember, however, that an operator's description is very limited. Ask specific and detailed questions. Find out everything possible about when the first symptoms occurred, exactly how those symptoms were displayed (which lights, indicators, typewriter messages). Find out if anything significant occurred immediately before the problem was noted. Both the terms "significant" and "immediately before" are very relative. Using a different device could be significant, and a program change made months ago could be immediately before. Be specific when asking questions.

- Core dumps, EREP, sense information, system diagnostic information -- any hard copy information that can be obtained could be helpful.

- Indicator lights on all machines connected to subsystem/channel/CPU. The presence or absence of all indications, both normal and abnormal, is worthwhile information.

- When trying to trace an intermittent problem, it is always helpful to record such information as which interface or channel the problem occurred on.

DEFINING DEVIATION

In order to know what the problem is, it must be precisely stated and must be stated in two ways: the problem is.../the problem is not... If a problem exists, it can be determined that the problem exists to some limited extent. For example, define not only that a specific problem exists (such as device drops Ready), but also the operation being performed (seeking, reading, etc.). It is common to all units? Has an FCO just been installed? Intermittent or constant failure?

Writing down all that information does not waste time. On the contrary, that kind of definition to a problem saves time. It forces the additional information-gathering that can pin a problem to a specific cause.

Once enough data has been gathered to state the problem in these specific terms, proposing the theory of cause is at least half done.

PROPOSE THEORY OF CAUSE

It is not just guesswork that proposes a theory of cause. It is a matter of considering all the available facts, and then asking what would explain all the facts in the definition of the problem.

TEST THEORY

To test the theory of cause, change the one thing that has been identified as the cause of the problem. If the entire problem (not just some of the more obvious symptoms) goes away it can be safely assumed that that was the cause. If, however, only part of the problem is corrected, determine if the problem has

a multiple cause or another unexplained symptom. If a corrective action does not correct a problem or if it cannot be completely explained as a reasonable part of the problem, the corrective action should not be left in the machine. A change of that sort only adds another unknown to the problem and changes the data that was established to begin with. Take care not to confuse the issue with changes that are merely guesses.

INTERMITTENT PROBLEMS

Some action should be taken to correct an intermittent problem whenever possible, even if the failure cannot be duplicated. The purpose of the following is to assist in trying to duplicate the failure and, if that cannot be done, to provide some guidance as to possible corrective actions that can be taken.

1. If system type errors (Fault Symptom Codes) are being generated, determine if they are predominantly one symptom code or several related codes. Loop on these microdiagnostic routines/tests in an attempt to produce microdiagnostic errors. Looping routines/tests increases the testing frequency on specific areas of logic. If the microdiagnostics detect errors, follow the actions listed by the error stop in the error code dictionary.

2. If the microdiagnostics do not produce errors, use the most frequent Fault Symptom Codes to replace, swap, or check suspected items to correct the error.

3. Maintain a list of what has been done. This information may be valuable if additional action is required. A check of the customer's operation has to be made to determine if the problem has been corrected. If mass card replacement was used, make every attempt to determine which one caused the error by putting removed cards back in one or two at a time.

4. Other forms of stress testing, such as marginal voltages, raising and lowering temperature, and vibration may be tried but have not proven too effective. A folded tab card raked across the cards while in a test loop sometimes helps find a bad card connection or a vibration sensitive card. Moving cables and connectors under the same conditions also occasionally locates a problem.

5. It is essential to have all the information possible regarding failures. Use full dumps and analyze them fully. Understand how much of the system is working correctly as well as what is failing.

6. Determine if a failure is with one or multiple devices. With single device failures, determine the failing addresses. Determine if one or many tracks common to one head are failing.

7. For access failures, card swapping between two devices is effective in isolating card failures. Power amplifiers can be swapped between devices. Check the interconnecting cables and connectors. Check the voltages.

8. For intermittent head load and unload problems and for dropping Ready (Intervention Required), it is sometimes necessary to request that the customer leave the machine in the failing condition until the CE arrives.

9. If there are tag or bus parity problems between the controller and one string of devices, there could be a bad cable connector somewhere down the string.

10. Consider using a voltmeter to check voltage level and an oscilloscope to check voltage ripple on the power supplies.

11. Check the time when errors occur when possible. It is possible some external noise source is present only at certain times.

12. Question the customer about other possible environmental problems such as room temperature, static discharges possibly from low humidity, or other unusual occurrences.

PROBLEM NOT FOUND

The unit is failing now and the maintenance actions have not corrected the problem.

Return to the original entry and replace, swap, and check items listed. Test the machine in the original manner to determine if the trouble is corrected.

NOTE

> When replacing or swapping components, keep a list of what has been done. This is very valuable if the error is being propagated due to components being damaged.

At this point, understanding the failure becomes essential. A methodical approach must be developed and followed. Analyze

all failure information; microdiagnostic error stops, messages, or anything else pertaining to the failure. Know what is failing and what is not. If the failure can be duplicated with the same failure information, you should be close to understanding the problem.

If a fairly solid error condition exists with a microdiagnostic routine or test, loop the routine or test and scope the inputs that set the error latch or line. Try to determine the input at fault or if it is the output. At this point, you may be looking for an open or short on the board, back panel wire, or in a cable, rather than a card problem.

If the failures are random or the failure still has not been found, monitor the voltages with a voltmeter to be sure they are within specification. Check the power supplies for noise or high frequency ripple with an oscilloscope. Check grounding, cables, and connectors for bad crimps, shorts, or poor connections. Check other environmental conditions that may cause machine problems such as temperature, static, primary power, external noise, etc.

Access cards can be easily swapped between devices to help isolate access problems. This includes the power amplifier. Check the cabling and voltage.

If the problem is Data Checks, they must be isolated to the smallest element possible (one device, one HDA, all devices, etc.). Any HA or RO failures identified with an HDA must be corrected. Advise the customer to rewrite the data or assign an alternate track if data cannot be rewritten due to a surface defect. If several defects appear, check the head addresses. If the problem is common to one head, the head may be defective or the connector may be bad.

ON-LINE ERROR ANALYSIS METHODS

SOLEX

"SOLEX" stands for Standalone Online Executive. When EREP fault isolation is unsatisfactory or does not provide sufficient detail, run SOLEX and analyze the console error messages described in the SOLEX manual for the appropriate subsystem.

The preferred order of obtaining fault information in terms of impact on customer throughput is as follows:

1. Obtain EREP printout using IBM OLTEP. Refer to fault Symptom Code Index for Fault Symptom Code meaning and action.

2. Run SOLEX test. If the system is capable of multi-tasking, the system and remaining drives are available for concurrent customer jobs. Perform suggested fault correction procedures.

3. Consider running standalone microdiagnostics from the storage control. Analyze maintenance panel display for error code.

4. Rerun failing customer job. Question the customer to determine the conditions at the time of the failure. If the system is capable of multi-tasking, the customer may run other jobs concurrently.

EREP PROGRAM

"EREP" stands for Error Recording, Editing, and Printing. The primary method of locating subsystem faults is by analysis of the customer-provided Error Log Record (SYS1.LOGREC) generated by EREP. The EREP utility program provides you with two basic functions:

1. It summarizes the statistical data generated by the subsystem.

2. It prints detailed unit check records in a format that is easily readable.

The operating system determines the format and context of the statistical summary.

The statistical summary information is used to quickly determine the condition of the subsystem. This information can be used to:

1. Assist you in deciding what action to take during preventive maintenance.

2. Point out detailed unit check records.

3. Separate device, controller, and storage control problems.

Note that the EREP program is configured for IBM equipment: the indicated errors on the EREP printout may not reflect the same error on CDC equipment. This is due to differences in meaning of selected sense bits. To determine the meaning of EREP-indicated error codes, refer to the sense byte translations listed in section 1C. For discussion purposes, OS/360 terms are used to describe operating system functions. Other IBM operating systems have equivalent EREP functions and terms.

SECTION 1A

POWER

INTRODUCTION

This section contains general information on power and troubleshooting power-related problems.

When using SAMs, refer to Using the SAM (section 1) for format and description.

POWER ON/OFF PROCEDURES

During maintenance or troubleshooting, it may be necessary to turn off power in one or more pieces of equipment. Turning off power is required if a board is to be removed or added.

POWERING OFF/ON A SINGLE CONTROLLER

Use this procedure when replacing a board or dc module in a single controller.

1. At the CPU, vary offline all device paths through the controller to be powered off.
2. At the operator panel disable the controller to be powered off.
3. At the HSC PCU turn off the appropriate CB (CB9 for controller 1 or CB10 for controller 2).
4. Reverse the above procedure to restore power.

NOTE

A Check-2 error occurring during power up will delay Power Up Sequence Complete approximately four minutes.

POWERING OFF/ON A SINGLE DEVICE

Use this procedure when replacing a board, power amp, or dc module in a single device.

NOTE

Install the carriage lock if the power amp is to be removed for longer than one-half hour.

1. At the CPU, vary offline the device to be powered off.
2. Remove the device logic chassis cover (upper logic chassis for devices 0 and 1; lower logic chassis for devices 2 and 3).
3. Stop the device to be powered off by pressing down on the appropriate board-mounted switch.

   Device 0 - Board 8, upper chassis

   Device 1 - Board 28, upper chassis

   Device 2 - Board 8, lower chassis

   Device 3 - Board 28, lower chassis

NOTE

Before going to the next step, ensure that the ONLINE status LED is off in the device to be powered off.

   Device 0 - Board 7, upper chassis

   Device 1 - Board 27, upper chassis

   Device 2 - Board 7, lower chassis

   Device 3 - Board 27, lower chassis

4. On the master/slave PCU, turn off the appropriate CB.

   Device 0 - CB3 (master PCU)

   Device 1 - CB4 (master PCU)

   Device 2 - CB7 (slave PCU)

   Device 3 - CB8 (slave PCU)

5. Reverse the above procedure to restore power.

NOTE

If more than one device is to be powered up, wait for the READY LED to come on before powering up the next device.

POWERING OFF A DRIVE STRING

Use this procedure to remove all power from a drive string.

1. At the CPU, vary offline all device paths through the HSC (two controllers) to be powered off.
2. At the operator panel disable both controllers.
3. At the HSC PCU turn off CB9 and CB10 (controller 1 and controller 2).

NOTE

Ensure all air mover fans in the drive string are stopped before going to the next step.

4. At the HSC PCU turn off CB5 (main breaker).

WARNING

Unswitched line voltages are still present inside the PCU.

POWERING ON A DRIVE STRING

1. At the HSC PCU turn on CB5 (main breaker).
2. At the HSC PCU turn on CB9 (controller 1).
3. Wait at least four seconds and then turn on CB10 (controller 2).

SAMS

Use SAM DSU1 when one or more devices do not power up far enough to permit an error message.

Use SAM HSC1 when a controller will not power up far enough to produce an error message.

SAM DSU1: DSU DEAD START POWER UP CHECKS

Assumptions: DSU ac power cord and I/O cables connected to HSC. AC circuit breaker in HSC for the DSU is on and all phases are present at the MPCU. All master and slave PCU circuit breakers in the DSU are on and all cables are connected.

001	Y	N	Is +24 V present at B07/B27-11A (drive power)?
002		1	If CB2 in MPCU does not trip, replace T1 (in MPCU), air mover motor (50 Hz only), logic chassis temperature sensor(s), or check wiring.
003		2	If CB2 in MPCU trips, replace _ACV board (in MPCU) or T1.
004	Y	N	Issue power up command. Is B07-11B (Logic Power Control) high?
005		1	Command failed. Faulty I/O cable(s).
006	Y	N	Is B07-11A (drive power) low?
007		1	Replace _SCX board in logic chassis.
008	Y	N	Did K1 relay (in MPCU) pull?
009		1	Replace _ACV board or relay K1.
010	Y	N	Is the air mover fan and both logic fans spinning?
011		1	If the air mover fan spins but logic fan(s) do not, replace F2 and/or F3 (on _CMV board in MPCU) or logic fan motor.
012		2	If logic fans spin but air mover fan does not, check CB2 or replace air mover motor.
013	Y	N	Checking devices 0 and/or 1?
014		1	Checking devices 2 and/or 3; go to SAM DSU2.

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015	Y	N	Are any of the following voltages present on the logic backpanel for device 0/1? (See Note 1.) • +18 V at A01/A21-45A • -18 V at A01/A21-01A • +5 V at A01/A21-44A • -5 V at A01/A21-02A Note 1: Steps 015 through 020 may be used to check devices 0 and/or 1 by choosing the proper logic location, CB, and dc module given in the steps.
016		1	If CB3/CB4 does not trip, check device 0/1 dc module fan. If fan is running, check cabling to logic chassis or replace device 0/1 dc module. If fan is not running, check for 24 Vac between J1-1 and J1-2, also between J1-2 and J1-3 at device 0/1 dc module. If no voltage is present, MPCU or cable is bad. If voltage is present, replace device 0/1 dc module.
017		2	If CB3/CB4 trips, disconnect P2 connector from device 0/1 dc module. If CB3/CB4 continues to trip, replace device 0/1 module. If CB3/CB4 stops tripping when P2 is disconnected, there is a short in the cabling to the logic chassis or a short in one or more boards in device 0/1.
018	Y	N	Is DC Voltage Good signal at B07/B27-27A low?
019		1	Replace device 0/1 dc module.
020	1		Power up checks for device 0/1 are ok.
021	2		If another device in the same cabinet is to be checked, go to step 013.

SAM DSU2: DSU DEAD START POWER UP FOR DEVICES 2 AND 3

Assumptions: This SAM was entered from SAM DSU1, step 014.

001	Y	N	Are any of the following voltages present on the logic backpanel for device 2/3? (See Note 1.) • +18 V at A01/A21-45A • -18 V at A01/A21-01A • +5 V at A01/A21-44A • -5 V at A01/A21-02A Note 1: Steps 001 through 007 may be used to check devices 2 and/or 3 by choosing the proper logic location, CB, and dc module given in the steps.
002		1	Check for ac line voltage phases A, B, and C on pins 3, 2, and 1 of J17 on MPCU. If all phases are not present, MPCU is faulty.
003		2	If CB7/CB8 does not trip, check device 2/3 dc module fan. If fan is running, check cabling to logic chassis or replace device 2/3 dc module. If fan is not running, check for 24 Vac between J1-1 and J1-2, also between J1-2 and J1-3 at device 2/3 dc module. If no voltage is present, MPCU or cable is bad. If voltage is present, replace device 2/3 dc module.
004		3	If CB7/CB8 trips, disconnect P2 connector from device 2/3 dc module. If CB7/CB8 continues to trip, replace device 2/3 module. If CB7/CB8 stops tripping when P2 is disconnected, there is a short in the cabling to the logic chassis or a short in one or more boards in device 2/3.
005	Y	N	Is DC Voltage Good signal at B07/B27-27A low?
006		1	Replace device 2/3 dc module.
007	1		Power up checks for device 2/3 are ok.
008	2		If another device attached to the SPCU is to be checked, go to step 001.

SAM HSC1: HSC DEAD START POWER UP CHECKS

Assumptions: Power cord is connected to ac outlet and all phases are present. Main HSC circuit breaker (CB5) is on.

WARNING

Unswitched line voltages are present inside PCU.

001	Y	N	Is the PHASE GOOD indicator on PCU on?
002		1	Ensure UNIT EMERGENCY switch on the operator panel is enabled.
003		2	Ensure CB6 (Controller Power) is ON.
004		3	Phase rotation order may be wrong. The main power or HSC power cord may be miswired.
005	Y	N	Are CONTROLLER 1 ON and CONTROLLER 2 ON indicators on the PCU on?
006		1	Ensure CB7 (FAN) is ON.
007		2	Check logic chassis thermal switch (replace switch if open) and associated wiring.
008		3	If logic chassis fan(s) are not spinning, check fan cable connections or replace fan(s).
009		4	Ensure connector J8 (power control) is properly seated.
010		5	Ensure CB11 (AUXILIARY) inside PCU is ON.
011	Y	N	Is LOCAL/REMOTE switch set to LOCAL?
012		1	If POWER ON REQUEST indicator is not on, check EPO cable connection between J5 and J6 of HSC and SD at other end of EPO cables, or ensure EPO plugs are installed.
013		2	If PICK IN and HOLD IN indicators are not on, check that EPO cables are good and that the SD has tried to sequence the HSC.

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014	Y	N	Are the OUT OF TOLERANCE and OVER TEMPERATURE indicators on the dc modules off?
015		1	Ensure CB9 and CB10 (CONTROLLER 1 and CONTROLLER 2) are ON.
016		2	The OVER TEMPERATURE light indicates that the dc module is overheated. If the dc module fan is not spinning, replace the fan. If the fan is spinning, look for air flow restriction and wait for module to cool down.
017		3	If OUT OF TOLERANCE light is on, replace dc module; check for shorts in logic chassis and cabling to logic chassis.
018	Y	N	Is the CHECK-1 indicator on edge of _SJX board off?
019		1	Read out the RCC bytes using inline utility CA6. Isolate the problem using the data provided by the utility.
020	Y	N	Is 15 V power present on pin 5 of connector P3 and P4 (CONTROLLER 1 and CONTROLLER 2)? Use pin 6 as ground reference.
021		1	Replace _AMV board in PCU.
022	Y	N	Is POWER SEQUENCE COMPLETE indicator on?
023		1	HSC code is still trying to complete the power up sequence. If this condition persists for more than three minutes, the code is hung. Power down and up the associated controller using controller circuit breaker CB9 or CB10. This will repeat the power up sequence.
024		2	If problem still exists, call for assistance.

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025  Y   N  Are drives powered up?
     |   |
026  |   1  Ensure drive power circuit breakers (CB1, CB2, CB3,
     |   |  and CB4) are on.
     |   |
027  |   2  Ensure drive power cables are attached to HSC
     |   |  (J1, J2, J3, and J4) for each drive in string.
     |   |
028  |   3  Go to SAM DSU1 to troubleshoot drive power problems.
     |
029  1      Power up checks for HSC are ok.
```

HSC VOLTAGE CHECKS

HSC voltages may be checked using a digital voltmeter to measure voltages on the backpanel.

Ensure that CB9 (controller 1) and/or CB10 (controller 2) are on.

Table 1A-1 gives the backpanel measuring points and acceptable voltage ranges.

TABLE 1A-1. HSC VOLTAGE CHECK VALUES

Power Supply	Measuring Points	Acceptable Range	
		From	To
+5V DC	Measure between back-	+4.96	+5.04
-5.2V DC	panel voltage connection	-5.16	-5.24
+14V DC	point and frame GND for	+13.8	+14.2
-12V DC	controller being checked.	-11.8	-12.2

The +5V and -5.2V may be adjusted with pots on the controller power supplies. Turn the pots counterclockwise to decrease the voltage and clockwise to increase the voltage.

The +14V and -12V supplies should not need adjustments in the field.

DEVICE VOLTAGE CHECKS

Device voltages may be checked with a digital voltmeter to measure voltages. These checks should be made while performing 256-track repeat seeks.

Table 1A-2 gives the backpanel measuring points and acceptable voltage ranges.

NOTE

The ±24V and the regulators for the ±10V and ±18V supplies are not adjustable.

TABLE 1A-2. DEVICE VOLTAGE CHECK VALUES

Power Supply	Measuring Points to ground	Acceptable Range	
		From	To
+5V DC	A01 (A21) - 44A	+4.97	+5.03
-5.2V DC	A01 (A21) - 02A	-5.17	-5.23
+24V DC	_GTN J2-7	+20.5	+27
-24V DC	_GTN J2-5	-20.5	-27
+10V DC	A3AXP2-13 *	+9	+11
-10V DC	A3AXP2-15 *	-9	-11
+18V DC	A01 (A21) - 45A	+17	+19
-18V DC	A01 (A21) - 01A	-17	-19

* NOTE: X Determines which logic is being checked

SECTION 1B

FAULT SYMPTOM CODE INDEX

FAULT SYMPTOM CODE INDEX 1B

INTRODUCTION

Fault symptom codes are generated by the functional microcode when an error condition is detected while the functional microcode is running.

MULTIPLE ERROR SYMPTOMS

Multiple error symptoms indicate that more than one collecting and reporting circuit reported an error when the sense data was collected. Multiple symptoms do not necessarily indicate more than one failing circuit or function. Any of the following conditions can cause multiple error symptoms from only one failing circuit or function:

- A failing circuit causes an error that is recognized by more than one error sensing circuit. This error recognition probably occurred at different times during a machine operation.
- A failing circuit causes an error that is recognized by one error sensing circuit. The error causes the current operation to stop before the sequence is complete. Stopping the current operation causes another condition that is recognized as an error by another error sensing circuit.
- A failing circuit causes an error that is recognized by an error sensing circuit. When the sense data is collected, the same condition causes an error in the sense data.
- The reset or clock circuits are failing.
- Dropping power (input or CB tripping) can cause symptom codes not related to the power problem. Fix the power problem first. If a symptom code is then presented, use it to repair the unit.

DIAGNOSTIC PROCEDURE

When multiple errors or nonrepeating errors are reported, look at the sense data.

- Look for a pattern of sense bits to guide you to the failing area.
- One error failing at different points in an operation, or another operation, can produce different symptom codes.

FAULT SYMPTOM CODE INDEX (FSCI)

The Fault Symptom Code is a four-digit code generated from sense data information. The first hex digit of the code is derived from Sense Byte 7, Bits 0 through 3; it denotes the format of the code. Formats 0, 1, 4, 5, 6, 7, and 8 apply to errors occurring in the controller and device.

Refer to section 1C for more information on sense data.

The Fault Symptom Code may be determined in one of the following ways:

1. Observation of the EREP printout.
2. Observation of the CPU console error message at the time of the error.
3. Dump External Error Log (EEL).
4. Run Error Synthesis Program (ESP)

Table 1B-1 provides the Fault Symptom Code Index. The codes are arranged in alphanumeric order. Most, but not all, FSCs have routines and FRUs listed with their descriptions. The routines should be used to produce the error during troubleshooting and to verify that the problem is fixed. If the routines listed do not produce an error, run the linked series.

The FRUs listed should be used to fix the problem.

TABLE 1B-1. FAULT SYMPTOM CODE INDEX

FSC	Format	Byte	Bit(s)	Description
1104	1	11	5=1	Power Card Check Routine: C81 FRUs: 2007, 2010, 2850
1120	1	11	2=1	RPS Check Routine: C81, C83 FRUs: 2010, 2005, 2008, 2009, 2001, 2007, 2011, 2006
1140	1	11	1=1	Servo Control Check Routine: C81, C82 FRUs: 2010, 2006, 2009, 2008, 2007, 2005
1180	1	11	0=1	Error Flag (Checkpoint Check) Routine: C81 FRUs: 2010, 2008, 2009, 2005
1248	1	12	2-4=001	Safety Active Check (odd address matrix board) Routine: C84 FRUs: 2005, 2011, 2010, 2008, 1004, 1003, 1005, 1007
1250	1	12	2-4=010	Write Current Check (odd address matrix board) Routine: C81 FRUs: 2011, 2450, 2005, 2008, 2009, 1004, 1003

Table Continued on Next Page

TABLE 1B-1. FAULT SYMPTOM CODE INDEX (Contd)

FSC	Format	Byte	Bit(s)	Description
1258	1	12	2-4=011	Read Sequence Check (odd address matrix board) Routine: C81 FRUs: 2011, 2010, 2008, 1004, 1003
1260	1	12	2-4=100	Write Transition Check (odd address matrix board) Routine: C84 FRUs: 2011, 2450, 2005, 2008, 1004, 1003
1268	1	12	2-4=101	Write Gate Check (odd address matrix board) Routine: C84 FRUs: 2011, 2010, 2008, 1004, 1003
1270	1	12	2-4=110	Head Select Check (odd address matrix board) Routine: C84 FRUs: 2011, 2006, 2450, 2008, 2010, 1004, 1003
1278	1	12	2-4=111	±5 V and -8.2 V Safety Check (odd address matrix board) Routine: C81 FRUs: 2011, 2010, 2850
1288	1	12	2-4=001	Safety Active Check (even address matrix board) Routine: C84 FRUs: 2005, 2011, 2010, 2008, 1004, 1003, 1005, 1007

Table Continued on Next Page

TABLE 1B-1. FAULT SYMPTOM CODE INDEX (Contd)

FSC	Format	Byte	Bit(s)	Description
1290	1	12	2-4=010	Write Current Check (even address matrix board) Routine: C81 FRUs: 2011, 2450, 2005, 2008, 2009, 1004, 1003
1298	1	12	2-4=011	Read Sequence Check (even address matrix board) Routine: C81 FRUs: 2011, 2010, 2008, 1004, 1003
12A0	1	12	2-4=100	Write Transition Check (even address matrix board) Routine: C84 FRUs: 2011, 2450, 2005, 2008, 1004, 1003
12A8	1	12	2-4=101	Write Gate Check (even address matrix board) Routine: C84 FRUs: 2011, 2010, 2008, 1004, 1003
12B0	1	12	2-4=110	Head Select Check (even address matrix board) Routine: C84 FRUs: 2011, 2006, 2450, 2008, 2010, 1004, 1003
12B8	1	12	2-4=111	±5 V and -8.2 V Safety Check (even address matrix board) Routine: C81 FRUs: 2011, 2010, 2850

Table Continued on Next Page

TABLE 1B-1. FAULT SYMPTOM CODE INDEX (Contd)

FSC	Format	Byte	Bit(s)	Description
1301	1	13	7=1	HAR Parity Check Routine: C81 FRUs: 2006, 2011, 2010, 2008, 2009
1302	1	13	6=1	R/W Servo Check Routine: C84 FRUs: 2011, 2004, 2010
1304	1	13	5=1	Write Overrun Check Routine: C81 FRUs: 2011, 2005, 2010
1308	1	13	4=1	R/W Control Check Routine: C81 FRUs: 2011, 2005, 2010
1310	1	13	3=1	Read Sequence Check Routine: C81 FRUs: 2011, 2010, 2005
1320	1	13	2=1	Write Sequence Check Routine: C81 FRUs: 2011, 2010, 2005
1340	1	13	1=1	Pad Check Routine: C81 FRUs: 2011, 2005, 2010
1380	1	13	0=1	R/W Check Routine: C81 FRUs: 2011, 2010, 2005
1500	1	07	4-7=5	Device Does Not Respond To Selection Routine: C81, CA2 FRUs: 2010, 2008, 1004, 1003, 1050, 7903, 2009, 2850

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TABLE 1B-1. FAULT SYMPTOM CODE INDEX (Contd)

FSC	Format	Byte	Bit(s)	Description
1610	1	11	3=1	Checkpoint Log Parity Error Routine: C81 FRUs: 2010, 2008, 2007, 2009, 2005, 1004, 1003
17XX	1	07	4-7=0	End Op -- No Device Error (See Byte 19 for XX) Routine: Linked series FRUs: 2010, 2008, 2009, 1004, 1003
1813	1	07	4-7=3	Missing Index Routine: C81 FRUs: 2005, 2001, 2010, 1007, 1004, 1003, 2450
1814	1	07	4-7=4	Interrupt Not Resettable Routine: Linked series FRUs: 1004, 1003, 2007, 2004, 2006, 2010, 2003, 2005
1816	1	07	4-7=6	Device Check-2/Set Sector Incomplete Routine: C82, C83 FRUs: 2007, 2008, 2009, 2004, 2006, 2010, 2003, 2005
1817	1	07	4-7=7	Head Address Miscompare Routine: C82 FRUs: 2006, 2010, 2450, 2012, 2001, 1008, 2011, 1007

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TABLE 1B-1. FAULT SYMPTOM CODE INDEX (Contd)

FSC	Format	Byte	Bit(s)	Description
1818	1	07	4-7=8	Device Status 1 Invalid Routine: C81 FRUs: 2007, 2010, 2004, 2006, 2010, 2003, 2005
1819	1	07	4-7=9	Device Not Ready Routine: CA2, C81 FRUs: 2007, 2010, 2006, 2005, 2011, 2008, 2009, 2550
181C	1	07	4-7=C	Drive Motor Switch Off Routine: CA2, C81 FRUs: 2007, 2010, 2006, 2850, 2550
19XX	1	07	4-7=1	Device Status 1 Not as Expected (Byte 16 contains expected status and Byte 19 contains received status) Routine: C81, C82 FRUs: 2007, 2004, 2006, 2009, 2008, 2003, 2005, 2010
1AXX	1	07	4-7=A	PA Not as Expected While Oriented (See Byte 15 for XX) Routine: C82 FRUs: 2004, 2006, 2010, 2012, 2001, 1008, 2011, 1007

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TABLE 1B-1. FAULT SYMPTOM CODE INDEX (Contd)

FSC	Format	Byte	Bit(s)	Description
1DXX	1	07	4-7=D	Seek Incomplete (See Bytes 15 and 19) Routine: C82 FRUs: 2007, 2004, 2006, 2009, 2008, 2003, 2005, 2010
1E00	1	07	4-7=E	Cylinder Address Miscompare Routine: C81, C82 FRUs: 2004, 2006, 2010, 2012, 2001, 1008, 2011, 1007
1FXX	1	07	4-7=F	Offset Active Cannot be Reset (See Byte 15 for XX) Routine: C82, CAD FRUs: 2007, 2004, 2006, 2009, 2003, 2008
4940	4	07	4-7=0	Uncorrectable Data Check -- Home Address Routine: C84, C85, C86 FRUs: 1007, 1006, 1008, 2012, 2450, 2001, 2011, 2010
4941	4	07	4-7=1	Uncorrectable Data Check -- Count Routine: C84, C85, C86 FRUs: 1007, 1006, 1008, 2012, 2450, 2001, 2011, 2010

Table Continued on Next Page

TABLE 1B-1. FAULT SYMPTOM CODE INDEX (Contd)

FSC	Format	Byte	Bit(s)	Description
4942	4	07	4-7=2	Uncorrectable Data Check -- Key Routine: C84, C85, C86 FRUs: 1007, 1006, 1008, 2012, 2450, 2001, 2011, 2010
4943	4	07	4-7=3	Uncorrectable Data Check -- Data Routine: C84, C85, C86 FRUs: 1007, 1006, 1008, 2012, 2450, 2001, 2011, 2010
4944	4	07	4-7=4	No Sync Byte Found -- Home Address Routine: C84, C85, C86 FRUs: 1007, 1008, 1006, 2012, 2001, 2011
4945	4	07	4-7=5	No Sync Byte Found -- Count Routine: C84, C85, C86 FRUs: 1007, 1008, 1006, 2012, 2001, 2011
4946	4	07	4-7=6	No Sync Byte Found -- Key Routine: C84, C85, C86 FRUs: 1007, 1008, 1006, 2012, 2001, 2011
4947	4	07	4-7=7	No Sync Byte Found -- Data Routine: C84, C85, C86 FRUs: 1007, 1008, 1006, 2012, 2001, 2011

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TABLE 1B-1. FAULT SYMPTOM CODE INDEX (Contd)

FSC	Format	Byte	Bit(s)	Description
60XX	8			Fault Log Bit(s) Always Active (same bit always active in each sense byte) Routine: Linked series FRUs: 1005, 1004, 1006, 1007, 1250
61XX	1	23	0-7=XX	CDP Bus Bit(s) Always Active Routine: C81 FRUs: 2010, 2008, 1004, 1003, 1050, 2007, 2011
62XX	1	07	0-7=10	End Op Received From Device (see Byte 9 for XX - End Op code) Routine: Linked series FRUs: 2008, 1004, 1003, 2010, 2011, 2005, 2007, 2009
7010	7	11	2=1	DPSE Unconditional Reserve, Controller 1 Routine: CA0, CA1 FRUs: 1005, 1006, 1004, 1105, 1104
7011	7	11	3=1	DPSE Unconditional Reserve, Controller 0 Routine: CA0, CA1 FRUs: 1005, 1006 1004, 1105, 1104
7012	7	11	2,3=11	DPSE Unconditional Reserve Routine: CA0, CA1 FRUs: 1005, 1006, 1004, 1105, 1104

Table Continued on Next Page

TABLE 1B-1. FAULT SYMPTOM CODE INDEX (Contd)

FSC	Format	Byte	Bit(s)	Description
7070	7	10	0=1	CCA and No Other Errors Routine: C80 FRUs: 1006, 1005, 1007, 1105, 1250
7073	7	07	4-7=3	Invalid Tag In During Selection Sequence Routine: C80 FRUs: 1005, 1250, 1006, 1007, 1105
7074	7	07	4-7=4	Extra RCC Required Routine: C80 FRUs: 1006, 1005, 1007, 1105, 1250
7075	7	07	4-7=5	Invalid DDC Selection Response or Time Out Routine: C80 FRUs: 1005, 1006, 1004, 1003, 2010, 1250, 1050
7076	7	07	4-7=6	Missing End Op -- Data Transfer Complete Routine: C80 FRUs: 1004, 1003, 2008, 2010, 2011, 1007, 1005, 1050
7077	7	07	4-7=7	Missing End Op -- Data Transfer Not Complete Routine: C80 FRUs: 1004, 1003, 2008, 2010, 2011, 1007, 1005, 1050

Table Continued on Next Page

TABLE 1B-1. FAULT SYMPTOM CODE INDEX (Contd)

FSC	Format	Byte	Bit(s)	Description
7078	7	09	4-7=8	Invalid Tag In -- Immediate Command Routine: C80 FRUs: 1005, 1006, 1004, 1003, 2010, 2008, 2009, 1250
7079	7	07	4-7=9	Invalid Tag In -- Extended Command Routine: C80 FRUs: 1004, 1003, 2008, 2010, 2011, 1007, 1005, 1050
707A	7	07	4-7=A	SD Microcode Timed Out on Deselection Routine: C80 FRUs: 1005, 1006, 1004, 1003, 2010, 2008, 2009, 1250
707B	7	07	4-7=B	No Selection Response After Poll Interrupt Routine: C81 FRUs: 1005, 1006, 1004, 1003, 2010, 2008, 2009, 1250
70F8	7	07	0-7=78	DPSE Command Timeout Routine: CA0, CA1 FRUs: 1005,1006, 1004, 1105, 1104

Table Continued on Next Page

TABLE 1B-1. FAULT SYMPTOM CODE INDEX (Contd)

FSC	Format	Byte	Bit(s)	Description
7100	7	13/15	0=1	DDC Tag Out Sequence Check Routine: C80 FRUs: 1005, 1006, 1004, 1003, 2010, 2008, 2009, 1250
71XX	7	12/14	0-7=xx	The basic error is FSC 7100, but additional errors were also detected. After analyzing the basic error, analyze byte 12/14 bit(s) in the order shown below using the equivalent FSC given. Byte 12/14 Errors Bit(s) FSC 4=1 7208 5=1 7204 0-2=001 7220 0-2=010 7240 0-2=100 7280 0-2=110 72C0 6=1 7202 3=1 7210
7202	7	12/14	6=1	DDC Bus In Parity Check-1 Routine: C80, C81 FRUs: 1005, 1006, 1008, 1007

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TABLE 1B-1. FAULT SYMPTOM CODE INDEX (Contd)

FSC	Format	Byte	Bit(s)	Description
7204	7	12/14	5=1	Controller Sequencer Check-1 Routine: C80 FRUs: 1006, 1008, 1005
7208	7	12/14	4=1	Controller Clock Check Routine: C80 FRUs: 1007, 1008, 1006, 1004, 1005
7210	7	12/14	3=1	DDC Bus Out Parity Check Routine: C80 FRUs: 1006, 1005, 1007, 1008
7220	7	12/14	0-2=001	Parity Error Detected on Input Data Bus On Sequencer 1 Board Routine: C80 FRUs: 1005, 1006, 1004, 1003, 1008
7240	7	12/14	0-2=010	Parity Error Detected in Pipeline B Instruction Routine: C80 FRUs: 1005, 1004, 1006, 1008
7280	7	12/14	0-2=100	Parity Error Detected in Pipeline A Instruction Routine: C80 FRUs: 1006, 1005, 1008
72C0	7	12/14	0-2=110	Parity Error Detected in Data Output Bus Routine: C80 FRUs: 1005, 1006, 1008

Table Continued on Next Page

TABLE 1B-1. FAULT SYMPTOM CODE INDEX (Contd)

FSC	Format	Byte	Bit(s)	Description
7308	7	13/15	4=1	RCC Clock Check Routine: C80 FRUs: 1007, 1008, 1006, 1004, 1005
7310	7	13/15	3=1	DDC Float Check Routine: C80 FRUs: 1006, 1005, 1007, 1008
7320	7	13/15	2=1	Sequencer Detected Check-1 Routine: C80 FRUs: 1006, 1008, 1005
7340	7	13/15	1=1	Oriented Tag Sequence Check-1 Routine: C80 FRUs: 1005, 1006, 1007, 1008
7380	7	13/15	0=1	DDC Tag Out Sequence Check Routine: C80 FRUs: 1005, 1006, 1008
7410	7	10	3=1	DDC Bus In Parity Check Routine: C80, C81 FRUs: 1005, 1006, 1008, 1007, 1250
7440	7	10	1=1	Tag In Check Routine: C80, C81 FRUs: 1005, 1006, 1250, 1008

Table Continued on Next Page

TABLE 1B-1. FAULT SYMPTOM CODE INDEX (Contd)

FSC	Format	Byte	Bit(s)	Description
75XX	7	10 12/14	0=0 0-7=XX	Connection Check Alert not set, but error(s) detected in Byte 12/14. Analyze byte 12/14 bit(s) in the order shown below using the equivalent FSC given. Byte 12/14 Errors Bit(s) FSC 4=1 7208 5=1 7204 0-2=001 7220 0-2=010 7240 0-2=100 7280 0-2=110 72C0 6=1 7202 3=1 7210

Table Continued on Next Page

TABLE 1B-1. FAULT SYMPTOM CODE INDEX (Contd)

<table>
<tr><th>FSC</th><th>Format</th><th>Byte</th><th>Bit(s)</th><th>Description</th></tr>
<tr><td>76XX</td><td>7</td><td>12/14</td><td>0-7=XX</td><td>Controller Check-1. Analyze byte 12/14 bit(s) in the order shown below using the equivalent FSC given.

Byte 12/14 Errors

<u>Bit(s)</u> <u>FSC</u>
4=1 7208
5=1 7204
0-2=001 7220
0-2=010 7240
0-2=100 7280
0-2=110 72C0
6=1 7202
3=1 7210</td></tr>
<tr><td>77XX</td><td>7</td><td>13/15</td><td>0-7=XX</td><td>Controller Check-1. Analyze byte 13/15 bit(s) in the order shown below using the equivalent FSC given.

Byte 13/15 Errors

<u>Bit(s)</u> <u>FSC</u>
1=1 7340
2=1 7320
3=1 7310
4=1 7308</td></tr>
<tr><td colspan="5">Table Continued on Next Page</td></tr>
</table>

TABLE 1B-1. FAULT SYMPTOM CODE INDEX (Contd)

FSC	Format	Byte	Bit(s)	Description
7800	7	07	4-7=2	RCC1 And RCC2 Sequence Unsuccessful Routine: Linked series FRUs: 1006, 1005, 1250, 1056
7DXX	7	13/15 12/14	0=1 0-7=XX	The basic error is a DDC Tag Out Sequence Check, which is the same as FSC 7380, but additional errors were also detected. After analyzing the basic error, analyze byte 12/14 bit(s) in the order shown below using the equivalent FSC given. Byte 12/14 Errors Bit(s) FSC 4=1 7208 5=1 7204 0-2=001 7220 0-2=010 7240 0-2=100 7280 0-2=110 72C0 6=1 7202 3=1 7210

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TABLE 1B-1. FAULT SYMPTOM CODE INDEX (Contd)

<table>
<tr><th>FSC</th><th>Format</th><th>Byte</th><th>Bit(s)</th><th>Description</th></tr>
<tr><td>7EXX</td><td>7</td><td>12/14</td><td>0-7=XX</td><td>Error(s) reported in bytes 12/14 at both controllers. Analyze byte 12/14 bit(s) in the order shown below using the equivalent FSC given.

Byte 12/14 Errors

Bit(s) FSC
4=1 7208
5=1 7204
0-2=001 7220
0-2=010 7240
0-2=100 7280
0-2=110 72C0
6=1 7202
3=1 7210</td></tr>
<tr><td>7FXX</td><td>7</td><td>13/15</td><td>0-7=XX</td><td>Error(s) reported in bytes 13/15 at both controllers. Analyze byte 13/15 bit(s) in the order shown below using the equivalent FSC given.

Byte 13/15 Errors

Bit(s) FSC
1=1 7340
2=1 7320
3=1 7310
4=1 7308</td></tr>
<tr><td colspan="5">Table Continued on Next Page</td></tr>
</table>

TABLE 1B-1. FAULT SYMPTOM CODE INDEX (Contd)

FSC	Format	Byte	Bit(s)	Description
8001	8	11	7=1	Power Supply Tolerance Check Routine: C81 FRUs: 1005, 1851, 1850, 1004
8002	8	11	6=1	Internal CDP Tag/Data Out Register Parity Check Routine: C80 FRUs: 1004, 1003, 2010, 1007, 1050, 2008
8004	8	11	5=1	Power Interrupt Routine: None FRUs: 1005, 1851, 1850, 1004
8008	8	11	4=1	CDP Input Bus Parity Check Routine: C81, CA2 FRUs: 1004, 1005, 1008, 1007
8010	8	11	3=1	Missing Servo Check Routine: C81 FRUs: 1008, 2012, 2001, 2450, 1051, 1007
8020	8	11	2=1	Software Set Check-2 Routine: C80 FRUs: 1004, 1006, 1007
8040	8	11	1=1	CODEC Wrap Error Routine: C81 FRUs: 1008, 2012, 2001, 1007, 1051, 2450

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TABLE 1B-1. FAULT SYMPTOM CODE INDEX (Contd)

FSC	Format	Byte	Bit(s)	Description
8080	8	11	0=1	Serdes Error Routine: C80 FRUs: 1008, 1007, 1005, 2012
8110	8	12	3=1	DDC Bus In Parity Check-2 Routine: C85 FRUs: 1005, 1007, 1006, 1250
8120	8	12	2=1	DDC Write Op Parity Check Routine: C85 FRUs: 1005, 1007, 1006, 1250
8180	8	12	0=1	Write Control Check Routine: C80 FRUs: 1007, 1008, 1006
8201	8	13	7=1	CDP Data Lock Parity Check Routine: CA0, CA1 FRUs: 1004, 1104, 1007, 1105
8202	8	13	6=1	CDP 12 Path Busy Parity Check Routine: CA0, CA1 FRUs: 1003, 1004, 1104, 1007, 1105, 1005
8210	8	13	3=1	CDP 12 Data Output Parity Error Routine: C80 FRUs: 1003, 1005, 1007
8220	8	13	2=1	Sync In/Sync Out Error Routine: None FRUs: 1008, 1007, 2012, 2001, 1051

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TABLE 1B-1. FAULT SYMPTOM CODE INDEX (Contd)

FSC	Format	Byte	Bit(s)	Description
8240	8	13	1=1	CDP Bidirectional Data Parity Check Routine: C81 FRUs: 1004, 1005, 1007
8280	8	13	0=1	ECC Bus Parity Check Routine: C80 FRUs: 1007, 1005, 2012, 2001, 1051
8301	8	12	7=1	CDP Port Check-1 Routine: C81 FRUs: 1004, 1003, 2010, 2011, 2007, 2005, 2009, 1050
8402	8	15	6=1	DPSE Lock Bus Parity Error Routine: CA0, CA1 FRUs: 1005, 1104
8408	8	15	4=1	DPSE Address Parity Error Routine: C94, CA0, CA1 FRUs: 1005, 1105, 1006, 1106
8410	8	15	3=1	DPSE Alternate Controller Parity Error Routine: CA0, CA1 FRUs: 1105, 1005, 1106, 1006
8420	8	15	2=1	DPSE Memory Compare Check Routine: C94, CA0, CA1 FRUs: 1005, 1105, 1006, 1106

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TABLE 1B-1. FAULT SYMPTOM CODE INDEX (Contd)

FSC	Format	Byte	Bit(s)	Description
8440	8	15	1=1	DPSE Data Bus Parity Error Routine: CA0, CA1 FRUs: 1005, 1105, 1006, 1106
8480	8	15	0=1	DPSE Memory Parity Error Routine: CA0, CA1 FRUs: 1005, 1105, 1006, 1106
86XX	8	07	4-7=3	End Op Code Not Equal To Zero; Immediate Command (See Byte 9 for XX) Routine: Linked series FRUs: 1005, 1006, 1008, 1007, 1004, 1003, 2010, 2009
87XX	8	07	4-7=4	End Op Code Not Equal To Zero; Transfer Count Not Equal To Zero (See Byte 9 for XX) Routine: Linked series FRUs: 1005, 1006, 1004, 1003, 2010, 2009, 2008, 1007
88XX	8	07	4-7=5	End Op Code Not Equal To Zero; Transfer Count Equal To Zero (See Byte 9 for XX) Routine: Linked series FRUs: 1005, 1006, 1004, 1003, 2010, 2009, 2008, 1007

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TABLE 1B-1. FAULT SYMPTOM CODE INDEX (Contd)

FSC	Format	Byte	Bit(s)	Description
8A02	8	7 15	4-7=6 0-7=02	DPSE Lock Bus Parity Error. DPSE Cleanup Check on channel or System Reset. Routine: CA0, CA1 FRUs: 1005, 1104
8A08	8	7 15	4-7=6 0-7=08	DPSE Address Parity Error. DPSE Cleanup Check on channel or System Reset. Routine: CA0, CA1 FRUs: 1005, 1105, 1006, 1106
8A10	8	7 15	4-7=6 0-7=10	DPSE Alternate Controller Error. DPSE Cleanup Check on channel or System Reset. Routine: CA0, CA1 FRUs: 1105, 1005, 1106, 1006
8A20	8	7 15	4-7=6 0-7=20	DPSE Memory Compare Error. DPSE Cleanup Check on channel or System Reset. Routine: CA0, CA1 FRUs: 1005, 1105, 1006
8A40	8	7 15	4-7=6 0-7=40	DPSE Data Bus Parity Error. DPSE Cleanup Check on channel or System Reset. Routine: CA0, CA1 FRUs: 1005, 1105, 1006, 1106
8A80	8	7 15	4-7=6 0-7=80	DPSE Memory Parity Error. DPSE Cleanup Check on channel or System Reset. Routine: CA0, CA1 FRUs: 1005, 1105, 1006, 1106

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TABLE 1B-1. FAULT SYMPTOM CODE INDEX (Contd)

FSC	Format	Byte	Bit(s)	Description
8C10	8	10	3=1	DDC Bus In Parity Check Routine: C80, C81 FRUs: 1005, 1006, 1008, 1007, 1250
8C20	8	10	2=1	Sync In Check Routine: Linked series FRUs: 1007, 1005, 1008, 2012, 2001, 1051, 1250
8C40	8	10	1=1	Tag In Check Routine: C80, C81 FRUs: 1005, 1006, 1250, 1008
8DXX	8	12	7=0	CDP Port Check (See byte 14 for XX) Routine: C81 FRUs: 1004, 1003, 2010, 2011, 2007, 2005, 2009, 1050
8E08	8	18	4=1	Delta Frequency Check Routine: None FRUs: 1008, 1007, 2012, 2001, 1051
8E10	8	18	3=1	Read Parity Check Routine: C80 FRUs: 1007, 1008, 2012, 2001, 1051
8E20	8	18	2=1	Reference Data Parity Error Routine: C80 FRUs: 1007, 1008, 2012, 2001, 1051

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TABLE 1B-1. FAULT SYMPTOM CODE INDEX (Contd)

FSC	Format	Byte	Bit(s)	Description
8E40	8	18	1=1	ALU Output Parity Error Routine: C85 FRUs: 1007, 1008, 2012, 2001, 1051
8E80	8	18	0=1	R/W Bus Out Parity Check Routine: C85 FRUs: 1007, 1008, 2012, 2001, 1051

SECTION 1C

SENSE INFORMATION

INTRODUCTION

The storage director provides 24 bytes of sense information arranged in nine error formats. These nine formats are used to classify errors depending upon where they originate and are reported. The errors may originate in the channel, storage director, controller, or device.

The nine formats are:

FORMAT	CONDITION
0	Program or system checks
1	Device equipment checks
2	Storage director equipment checks
3	Storage director control checks
4	Uncorrectable data checks
5	Correctable data checks
6	Usage/overrun error statistics
7	Controller Check-1
8	Controller equipment checks (controller Check-2, device Check-1)

Of these nine, only Formats 0, 1, 4, 5, 6, 7, and 8 apply to the controller/device. Figures 1C-1 through 1C-8 provide a summary of the bytes/bits in these formats. Immediately following the summaries, each sense byte/bit is further defined by a statement. The remaining formats apply to errors detected and reported by the storage director; refer to the applicable storage control troubleshooting manual.

FORMAT 0 -- PROGRAM OR SYSTEM CHECKS

Format 0 is composed of all program or system check errors. These checks occur in the channel or channel side of the channel interface, but are detected by a storage director. Examples are an incorrectly programmed channel routine, a channel problem causing an invalid tag sequence, or a parity error.

FORMAT 1 -- DEVICE EQUIPMENT CHECKS

Format 1 consists of all device Check-2 errors, which are usually hardware or data checks and can be retried. It is generated when the storage director detects one of the following:

- An end operation response code of 20.
- A Seek Incomplete or Cylinder Address Miscompare error. When the seek check counter overflows or when in forced logging mode, this error is reported only as Byte 0 Bit 3 (permanent bit is not turned on).
- A failure as defined by the message code in Byte 7.
- An intervention required condition when the addressed device is not attached to the string (End operation response 09 results in Byte 0, Bit 1 being set by the storage director).

FORMAT 4 -- UNCORRECTABLE DATA CHECKS

Format 4 lists data checks without displacement information (uncorrectable data checks). This format is generated when:

- Retry is exhausted for an uncorrectable permanent error. Byte 0, Bit 4 (Data Check) and Byte 1, Bit 0 (Permanent Error) are also set.
- Retry is successful for a temporary error with Byte 15 (Offset Level) active. Byte 0, Bit 4 (Data Check) and Byte 2, Bit 3 (Environmental Data Present) are also set.
- Retry is successful for a temporary error. A data check temporary error rate counter overflow occurs (nominal data check rate exceeded). Byte 0, Bit 4 (Data Check), Byte 1, Bit 3 (Message to Operator), Byte 2, Bit 2 (First Logging Mode Error), and Byte 2, Bit 3 (Environmental Data Present) are also set.
- Retry is successful for a temporary error. Forced Logging Mode is set, Byte 0, Bit 4 (Data Check) and Byte 2, Bit 3 (Environmental Data Present) are also set.

FORMAT 5 -- CORRECTABLE DATA CHECKS

Format 5 lists data checks with displacement information (correctable data checks). This format is generated when:

- Data checks that are correctable by error correction code (ECC) occurring in a data area. These data checks are not logged even though this format is used to report the checks to the operating system error recovery program (ERP).

- Data checks that occur in a Home Address (HA), count, or key area are corrected within the storage director and contain data that is not needed by the system ERP. Corrected HA, count, or key area sense data is only transmitted to the operating system ERP when logging mode is set to have the data checks logged.

When in logging mode, two Format 5 sense values are presented to the system when there are conditions that require correction. The first value (Byte 2, Bit 3 equals 0) is used by the ERP and is not logged. The second value (Byte 2, Bit 3 equals 1) is not used by the ERP and is logged.

FORMAT 6 -- USAGE/OVERRUN ERROR STATISTICS

Format 6 does not result directly from a fault or check condition. Format 6 sense information is generated after the channel issues a Read and Reset Buffered Log Command. The channel requests Format 6 information to prepare a report on device and channel usage or to flag an unusually high number of overruns or intermittent failures. A storage director can request the channel to read the log because a counter has overflowed.

FORMAT 7 -- CONTROLLER CHECK-1

Format 7 lists controller and director-to-device interface equipment checks. It is generated when:

- A Check-1 error is detected within the controller logic.

- The storage director to controller interface fails inbound.

- A timer in the storage director overflows while waiting for a response from the controller.

- A control interface tag in sequence or a bus parity failure is detected by the storage director.

Check-1 logic failures block normal controller communications with the storage director. Controller logic errors are collected in the connection check shift register and signaled to the storage director by a storage director to controller interface connection check alert (CCA). The storage director gathers the failure data with a request connection checks (RCC) sequence.

The storage director monitors the storage director-to-device (DDC) interface during the transfer of control signals and reports Bus In and Tag In errors. These errors are classed as controller errors and are reported in Format 7 sense data. Comparable errors in outbound storage director to controller interface control or data signals are classed as storage director errors.

The storage director microcode times event durations. If the controller exceeds the allotted amount of response time, a message is generated in Byte 7. The collected sequencer address in the sense data can point to the cause of the time out.

The controller saves the sequencer address whenever a Check-1 or Check-2 occurs or when an RCC sequence is initiated. An RCC sequence collects this address and passes it to the storage director along with active controller checks.

FORMAT 8 -- CONTROLLER EQUIPMENT CHECKS

Format 8 is generated when a storage director detects controller Check-2 or device Check-1 equipment failures. Controller Check-2 conditions do not prevent selection, normal communications on the director-to-device controller interface, or operations of the controller sequencer. Controller Check-2 and device Check-1 equipment conditions are reported to the storage director by normal director-to-device controller end operation codes.

SENSE BYTES 0 THROUGH 7

Sense Bytes 0 through 7 are common to all formats (0 through 8). See Figures 1C-1 through 1C-8.

BYTE	BITS 0	1	2	3	4	5	6	7
0	COMMAND REJECT	INTERVENTION REQUIRED	CH BUS OUT PARITY CHECK	EQUIPMENT CHECK	DATA CHECK	OVERRUN	ZERO	ZERO
1	PERMANENT ERROR	INVALID TRACK FORMAT	END OF CYLINDER	MESSAGE TO OPERATOR	NO RECORD FOUND	FILE PROTECTED	ZERO	ZERO
2	ZERO	CORRECTABLE DATA CHK	FIRST LOGGING MODE ERROR	ENVIRONMENTAL DATA PRESENT	INTENT VIOLATION	IMPRECISE ENDING	ZERO	ZERO
3	RESTART COMMAND/CONTROLLER PHYSICAL IDENTIFIER**/RESIDUAL RECORD COUNT							
4	DPS FUNCTION	ZERO	PERMANENT PATH ERROR	RESERVED	DEVICE ADDRESS 8	4	2	1
5*	LOW-ORDER PHYSICAL CYLINDER ADDRESS 128	64	32	16	8	4	2	1
6*	ZERO	ZERO	HIGH-ORDER PHYSICAL CYLINDER ADDRESS 512	256	HEAD ADDRESS 8	4	2	1
7	FORMAT (BITS 0-3 HEX)				MESSAGE CODE (BITS 4-7 HEX)			

FORMAT	DESCRIPTION
0	PROGRAM OR SYSTEM CHECKS ***
1	DEVICE EQUIPMENT CHECKS
2	SD EQUIPMENT CHECKS ***
3	SD CONTROL CHECKS *** MICROCODE DETECTED HARDWARE DETECTED
4	UNCORRECTABLE DATA CHECKS
5	CORRECTABLE DATA CHECKS
6	USAGE AND ERROR STATISTICS
7	CONTROLLER CHECK-1
8	CONTROLLER EQUIPMENT CHECKS

SEE FIGURE 1C-2

* NOT USED FOR FORMAT 6

** NOT USED FOR FORMATS 4 AND 5

*** REFER TO APPLICABLE STORAGE CONTROL TROUBLESHOOTING MANUAL

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Figure 1C-1. Sense Bytes 0 thru 7 Summary

MESSAGE	FORMAT 1	FORMAT 4	FORMAT 5
0	NO MESSAGE	HA ECC UNCORRECTABLE	HA AREA
1	DEVICE STATUS 1 NOT AS EXPECTED	COUNT ECC UNCORRECTABLE	COUNT AREA
2	RESERVED	KEY ECC UNCORRECTABLE	KEY AREA
3	INDEX MISSING	DATA ECC UNCORRECTABLE	DATA AREA
4	INT NOT RESETTABLE	HA NO SYNC BYTE FOUND	
5	DEVICE DOES NOT RESPOND TO SELECT	COUNT NO SYNC BYTE FOUND	
6	DEVICE CHK-2 OR SET SECTOR INCOMPLETE	KEY NO SYNC BYTE FOUND	
7	HEAD ADDRESS MISCOMPARE	DATA NO SYNC BYTE FOUND	
8	DEVICE STATUS 1 INVALID	HA ECC UNCORRECTABLE WITH OFFSET	HA AREA OFFSET ACTIVE
9	DEVICE NOT READY FOR CUSTOMER WORK	COUNT ECC UNCORRECTABLE WITH OFFSET	COUNT AREA OFFSET ACTIVE
A	PA MISCOMPARE WHILE ORIENTED	KEY ECC UNCORRECTABLE WITH OFFSET	KEY AREA OFFSET ACTIVE
B		DATA ECC UNCORRECTABLE WITH OFFSET	DATA AREA OFFSET ACTIVE
C	DRIVE MOTOR SWITCH SENSED OFF	HA NO SYNC BYTE WITH OFFSET	
D	SEEK INCOMPLETE	COUNT NO SYNC BYTE WITH OFFSET	
E	CYLINDER ADDRESS MISCOMPARE	KEY NO SYNC BYTE WITH OFFSET	
F	OFFSET ACTIVE NOT RESETTABLE	DATA NO SYNC BYTE WITH OFFSET	

12F45-1

Figure 1C-2. Sense Byte 7 Message Summary (Sheet 1 of 2)

MESSAGE	FORMAT 7	FORMAT 8
0	RCC INITIATED BY CCA	NO MESSAGE
1	RCC1 SEQUENCE UNSUCCESSFUL	ECC HARDWARE CHECK
2	RCC1 AND RCC2 SEQUENCE UNSUCCESSFUL	RESERVED
3	INVALID TAG IN DURING SELECTION SEQUENCE	UNEXPECTED END OP RESPONSE CODE
4	EXTRA RCC REQUIRED	END OP WITH XFER CNT NOT EQUAL TO ZERO
5	INVALID DDC SELECTION RESPONSE OR TIMEOUT	END OP WITH XFER CNT EQUAL TO ZERO
6	MISSING END OP DATA XFER COMPLETE	DPSE CLEANUP CHK ON CH OR SYSTEM RESET
7	MISSING END OP DATA XFER INCOMPLETE	
8	INVALID TAG IN FOR IMMEDIATE COMMAND	
9	INVALID TAG IN FOR EXTENDED COMMAND	
A	SD MICROCODE TIMED OUT ON DESELECTION	
B	NO SELECTION RESPONSE AFTER POLL INTERRUPT	
C	CONTROLLER UNAVAILABLE	
D		
E		
F		

12F45-2B

Figure 1C-2. Sense Byte 7 Message Summary (Sheet 2)

BYTE NAME	BYTE	BIT		
		0	1	2
DDC BUS OUT 0	8			
DDC BUS IN 1	9			
DEVICE POWER STATUS	10	VOLTAGE MARGINS ACTIVE	MOTOR THERMAL	NO AIR FLOW
DEVICE CHECK REGISTER	11	ERROR FLAG	SERVO CONTROL CHECK	RPS CHECK
R/W STATUS 1	12	R/W CHECK RIGHT	LEFT	MATRIX SENSE 0
R/W STATUS 2	13	R/W CHECK	PAD CHECK	WRITE SEQUENCE CHECK
	14	NOT USED		
CHECK POINT LOG	15	CHECK POINT LOG		
TRACK PA READ OR EXPECTED STATUS	16	TRACK PHYSICAL ADDRESS READ OR 128	64	32
CYL/HD ADDRESS	17	NOT USED	NOT USED	CYL ADDRESS 512
	18	NOT USED		
DEVICE STATUS 1	19	PAD IN PROGRESS	SERVO INHIBITED	SEEK INCOMPLETE
DEVICE STATUS 2	20	DEVICE LOGIC DISABLED	SURGE COMPLETE	OFFSET ACTIVE
SD PHYSICAL IDENTIFIER	21			
FAULT SYMPTOM CODE	22,23			

12F46-1A

Figure 1C-3. Format 1 - Device Equipment Checks (Sheet 1 of 2)

BYTE	BIT				
	3	4	5	6	7
8					
9					
10	DEVICE SEQUENCE COMPLETE	MOTOR RUN LATCH ON	MOTOR CONTACTOR ACTIVE	MOTOR BRAKE LATCH ON	BRAKE APPLIED
11	CHECK POINT LOG PARITY CHECK	NOT USED	POWER CARD CHECK	READ/WRITE CHECK	NOT USED
12	MATRIX SENSE 1	MATRIX SENSE 2	NOT USED		
13	READ SEQUENCE CHECK	R/W CONTROL CHECK	WRITE OVERRUN CHECK	R/W SERVO CHECK	HAR PARITY CHECK
14	NOT USED				
15	CHECK POINT LOG				
16	EXPECTED DEVICE STATUS 1 16	8	4	2	1
17	CYL ADDRESS 256	8	HEAD ADDRESS 4	2	1
18	NOT USED				
19	DEVICE CHK-2 OR SET SECTOR INCOMPLETE	ON LINE	HDA ATTENTION	DEVICE BUSY	SEEK OR SET SECTOR INT OR SECTOR SEARCH
20	SPINDLE OFF	NOT USED		RIGHT ACCESS MECHANISM SELECTED	LEFT ACCESS MECHANISM SELECTED
21					
22,23					

12F46-2A

Figure 1C-3. Format 1 - Device Equipment Checks (Sheet 2)

BYTE	BIT							
	0	1	2	3	4	5	6	7
8*	NOT USED						CYLINDER ADDRESS 512	256
9*	CYLINDER ADDRESS 128	64	32	16	8	4	2	1
10*	NOT USED							
11*	NOT USED				HEAD ADDRESS 8	4	2	1
12*	RECORD NUMBER 128	64	32	16	8	4	2	1
13	SECTOR NUMBER							
14	CONTROLLER PHYSICAL IDENTIFIER							
15	HD OFFSET INCREMENT (MICRO INCHES) 320	160	80	40	NOT USED			FORWARD DIRECTION
16-20	NOT USED							
21	SD PHYSICAL IDENTIFIER							
22,23	FAULT SYMPTOM CODE							
* BYTES 8 THROUGH 12 ARE THE RECORD IDENTIFICATION								

12F47

Figure 1C-4. Format 4 - Uncorrectable Data Checks

BYTE	BIT							
	0	1	2	3	4	5	6	7
8*	NOT USED						CYLINDER ADDRESS 512	CYLINDER ADDRESS 256
9*	CYLINDER ADDRESS 128	CYLINDER ADDRESS 64	CYLINDER ADDRESS 32	CYLINDER ADDRESS 16	CYLINDER ADDRESS 8	CYLINDER ADDRESS 4	CYLINDER ADDRESS 2	CYLINDER ADDRESS 1
10*	NOT USED							
11*	NOT USED				HEAD ADDRESS 8	HEAD ADDRESS 4	HEAD ADDRESS 2	HEAD ADDRESS 1
12*	RECORD NUMBER 128	RECORD NUMBER 64	RECORD NUMBER 32	RECORD NUMBER 16	RECORD NUMBER 8	RECORD NUMBER 4	RECORD NUMBER 2	RECORD NUMBER 1
13	SECTOR NUMBER							
14	CONTROLLER PHYSICAL IDENTIFIER							
15	HD OFFSET INCREMENT (MICRO INCHES) 320	HD OFFSET INCREMENT (MICRO INCHES) 160	HD OFFSET INCREMENT (MICRO INCHES) 80	HD OFFSET INCREMENT (MICRO INCHES) 40	NOT USED			FORWARD DIRECTION
16	SD PHYSICAL IDENTIFIER/RESTART DISPLACEMENT**							
17	NOT USED/RESTART DISPLACEMENT**							
18,19	ERROR DISPLACEMENT							
20,23	ERROR PATTERN							

* BYTES 8 THROUGH 12 ARE THE RECORD IDENTIFICATION
** ONLY IF BYTE 2, BIT 3 IS OFF

12F48

Figure 1C-5. Format 5 - Correctable Data Checks

BYTE	BIT 0	1	2	3	4	5	6	7
8-11	BYTES READ/SEARCHED							
12-15	NOT USED							
16, 17	NUMBER OF MOTION SEEKS							
18-20	NOT USED							
21	SD PHYSICAL IDENTIFIER							
22,23	NOT USED							

12F49

Figure 1C-6. Format 6 -- Usage/Overrun Error Statistics

BYTE NAME	BYTE	BIT		
		0	1	2
DDC BUS OUT	8	DDC BUS OUT - COMMAND CODE		
DDC BUS IN	9	DDC BUS IN - SELECTION RESPONSE FOR MESSAGE 5		
DTI AND XES REG CONTENTS	10	CONNECTION CHECK ALERT	TAG IN CHECK	SYNC IN CHECK
CONTROLLER CHECK ALERT	11	CONTROLLER 0*	CONTROLLER 1*	CONTROLLER 0* DPSE FORCE RELEASE
CONTROLLER 0 CHECK-1 (CCA)	12	CHECK-1 ISOLATION BITS		
	13	DDC TAG OUT SEQUENCE CHECK	ORIENTED TAG SEQUENCE CHECK	SEQUENCER DETECTED CHECK-1
CONTROLLER 1 CHECK-1 (CCA)	14	SAME AS BYTE 12		
	15	SAME AS BYTE 13		
CONTROLLER 0 SEQUENCER ADDRESS	16	2048	1024	512
	17	8	4	2
CONTROLLER 1 SEQUENCER ADDRESS	18	SAME AS BYTE 16		
	19	SAME AS BYTE 17		
BYTE 7 DATA	20	BYTE 7 DATA - FOR MESSAGE C		
SD PHYSICAL IDENTIFIER	21			
FAULT SYMPTOM CODE	22,23			
* CONTROLLER IDENTIFICATION IS THE DDC ADDRESS PLUGGED INTO THE DDC XMTR/RCVR BOARD				

12F50-1A

Figure 1C-7. Format 7 - Controller Check-1 (Sheet 1 of 2)

BYTE	BIT 3	4	5	6	7
8					
9					
10	DDC BUS IN PARITY CHK	NULL DISCONNECT	VALID/SYNC IN	SELECTED NULL	END OPERATION
11	CONTROLLER 1* DPSE FORCE RELEASE	CONTROLLER POWER ON 0	CONTROLLER POWER ON 1	NOT USED	NOT USED
12	DDC BUS OUT PARITY CHK	CONTROLLER CLOCK CHK	CONTROLLER SEQUENCER CHECK-1	DDC BUS IN PARITY CHK-1	NOT USED
13	DDC FLOAT CHECK	RCC CLOCK CHECK	NOT USED		
14					
15					
16	256	128	64	32	16
17	1	POWER ON COMPLETE	CHECK-2 ACTIVE	SUCCESSFUL DATA XFER	UPPER MEMORY ENABLED
18					
19					
20					
21					
22,23					

12F50-2A

Figure 1C-7. Format 7 - Controller Check-1 (Sheet 2)

BYTE NAME	BYTE	BIT		
		0	1	2
DDC BUS OUT	8	DDC BUS OUT - COMMAND CODE		
DDC BUS IN	9	DDC BUS IN - END OPERATION CODE		
DTI AND XES REG CONTENTS	10	CONNECTION CHECK ALERT	TAG IN CHECK	SYNC IN CHECK
FAULT LOG BYTE A	11	SERDES ERROR	CODEC WRAP ERROR	SOFTWARE-SET CHECK-2
FAULT LOG BYTE B	12	WRITE CONTROL CHECK	NOT USED	DDC WRITE OP PARITY CHK
FAULT LOG BYTE C	13	ECC BUS PARITY CHECK	CDP BIDIR DATA PARITY CHK	SYNC IN/SYNC OUT ERROR
FAULT LOG BYTE D	14	DEVICE 0 CHECK-1	DEVICE 1 CHECK-1	DEVICE 2 CHECK-1
FAULT LOG BYTE E	15	DPSE MEMORY PARITY ERROR	DPSE DATA BUS PARITY ERROR	DPSE MEM COMPARE ERROR
SELECTED CONTROLLER SEQUENCER ADDRESS	16	2048	1024	512
	17	8	4	2
FAULT LOG BYTE F	18	R/W BUS OUT PARITY CHK	ALU OUTPUT PARITY ERROR	REFERENCE DATA PARITY ERROR
DEVICE STATUS 1	19	PAD IN PROGRESS	SERVO INHIBITED	SEEK INCOMPLETE
DEVICE STATUS 2	20	DEVICE LOGIC DISABLED	SURGE COMPLETE	OFFSET ACTIVE
SD PHYSICAL IDENTIFIER	21			
FAULT SYMPTOM CODE	22,23			

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Figure 1C-8. Format 8 - Controller Equipment Checks (Sheet 1 of 2)

BYTE	BIT 3	4	5	6	7
8					
9					
10	DDC BUS IN PARITY CHK	NULL DISCONNECT	VALID/SYNC IN	SELECTED NULL	END OPERATION
11	MISSING SERVO CHECK	CDP INPUT BUS PARITY CHECK	POWER INTERRUPT	INTERNAL CDP TAG OR DATA OUT REG PARITY	POWER SUPPLY TOLERANCE CHECK
12	DDC BUS IN PARITY CHK-2	PORT SELECT BIT 0	PORT SELECT BIT 1	NOT USED	CDP PORT CHECK-1
13	CDP 12 DATA OUTPUT PARITY ERROR	STRING CONFIGURATION		CDP 12 PATH BUSY PARITY ERROR	CDP DATA LOCK PARITY CHK
14	DEVICE 3 CHECK-1	DEVICE CLOCK CHK	ISOLATION BIT	PORT SELECT BIT 2	PORT SELECT BIT 3
15	DPSE ALTERNATE CTLR ERROR	DPSE ADDRESS PARITY ERROR	NOT USED	DPSE LOCK BUS PAR ERROR	NOT USED
16	256	128	64	32	16
17	1	POWER ON COMPLETE	CHECK-2 ACTIVE	SUCCESSFUL DATA XFER	ENABLE UPPER MEMORY
18	READ PARITY CHECK	DELTA FREQUENCY CHK	NOT USED		
19	DEVICE CHK-2 OR SET SECTOR INCOMPLETE	ON LINE	HDA ATTENTION	DEVICE BUSY	SEEK OR SET SECTOR INT OR SECTOR SEARCH
20	DRIVE MOTOR SWITCH	NOT USED	NOT USED	RIGHT ACCESS MECHANISM SELECTED	LEFT ACCESS MECHANISM SELECTED
21					
22,23					

12F51-2B

Figure 1C-8. Format 8 - Controller Equipment Checks (Sheet 2)

Sense Byte 0 -- Unit Check Description

Sense Byte 0 is generated when a unit check occurs.

Byte 0, Bit 0 -- Command Reject

Bit 0 sets after a channel command to the storage director is rejected. Refer to applicable storage control troubleshooting manual for additional information.

Byte 0, Bit 1 -- Intervention Required

Specified device is not available (not physically attached to the system), is not Ready, a diagnostic write or load command is being executed in the storage director, or device is in CE mode.

Byte 0, Bit 2 -- Channel Bus Out Parity Check

Refer to applicable storage control troubleshooting manual.

Byte 0, Bit 3 -- Equipment Check

An unusual hardware condition exists in the channel, storage director, controller, or device (defined in Sense Bytes 7 through 23).

Byte 0, Bit 4 -- Data Check

Caused by either of the following conditions:

1. Byte 1, Bit 1 on indicates a correctable error in data read from device. Correction information is provided in Format 5, Sense Bytes 15 through 23.

2. Byte 2, Bit 1 off indicates an uncorrectable error in data read from device. Format 4, Byte 7 contains more information.

Byte 0, Bit 5 -- Channel Overrun

Bit 5 sets after data transfer between the storage director and channel is not completed in the time permitted by the storage director. Refer to applicable storage control troubleshooting manual for additional information.

Byte 0, Bits 6 and 7 -- Not Used

Sense Byte 1 -- Unit Check Description

Sense Byte 1 is generated when a unit check occurs.

Byte 1, Bit 0 -- Permanent Error

Refer to applicable storage control troubleshooting manual.

Byte 1, Bit 1 -- Invalid Track Format (w/o SMB)

Bit 1 sets after an attempt is made to write data that exceeds the track capacity. Bit 1 is also set during a read or search operation when Index is detected in the gap after a count or key field. This bit indicates a programming error or an expected programming condition.

Byte 1, Bit 1 -- Invalid Track Format (w/SMB)

Bit 1 sets when one of the following commands do not find a record after Home Address:

- Write CKD Next Track
- Write Update Data
- Write Updated Key and Data.

Byte 1, Bit 2 -- End of Cylinder

Bit 2 sets after a read multitrack or search multitrack operation continues beyond the last track on the cylinder. This bit indicates a programming error or an expected programming condition.

Byte 1, Bit 3 -- Message to Operator

Bit 3 causes the error recovery procedure to print on error message (defined by Byte 7) to the system operator. Refer to applicable storage control troubleshooting manual for additional information.

Byte 1, Bit 4 -- No Record Found (w/o SMB)

Bit 4 sets after the index point at the beginning of the selected logical track is detected twice in the same command chain without an intervening:

- Read operation in the Home Address (HA) or in a data field
- Write, sense, or control command

The SD verifies that the access mechanism is properly positioned before setting Bit 4. This bit indicates a programming error or an expected programming condition.

Byte 1, Bit 4 -- No Record Found (w/SMB)

Bit 4 sets after index is sensed twice in the same command chain without an intervening:

- Read operation in the Home Address field
- Read operation in a data field
- Write, sense, or control command.

Bit 4 is also set by the search function of a Locate Record command.

The SD verifies that the access mechanism is properly positioned before setting Bit 4. This bit indicates a programming error or an expected programming condition.

Byte 1, Bit 5 -- File Protected

Refer to applicable storage control troubleshooting manual.

Byte 1, Bits 6 and 7 -- Not Used

Sense Byte 2 -- Unit Check Description

Sense Byte 2 is generated when a unit check occurs.

Byte 2, Bit 0 -- Not Used

Byte 2, Bit 1 -- Correctable Error

Data field Data Check posted in Sense Byte 0, Bit 4 is correctable. Sense Bytes 15 through 22 identify the error pattern, error pattern displacement, and restart displacement.

Byte 2, Bit 2 -- First Logged Error

Bit 2 sets on the first logged error when an error threshold is exceeded for Data and Seek Checks. Refer to applicable storage control troubleshooting manual for more information.

Byte 2, Bit 3 -- Environmental Data Present

Bit 3 indicates that Sense Bytes 8 through 23 contain either usage and error statistics or error log information.

Bit 3 is set when Format 6 is indicated, and is caused by any of the following:

- A usage overflow or error counter overflow
- A force-error-log mode
- A read and reset buffered log command.

When Bit 3 is set along with Byte 2, Bit 2, a message is sent to the operator. See Byte 1, Bit 3 (Message to Operator) for more details.

Byte 2, Bits 4 and 5 -- Not Used (w/o SMB)

Byte 2, Bit 4 --Intent Violation (w/SMB)

Refer to applicable storage control troubleshooting manual.

Byte 2, Bit 5 -- Imprecise Ending (w/SMB)

Refer to applicable storage control troubleshooting manual.

Byte 2, Bits 6 and 7 -- Not Used

Sense Byte 3 -- Restart Command/Controller Physical Identifier (w/o SMB)

Sense Byte 3 has variable meanings as follows (Byte 1, Bit 7 is Operation Incomplete):

Format	Byte 1,Bit 7	Byte Meaning
0	0	Byte=0
0	1	See Text #1
1	-	See Text #2
2	-	See Text #2
3	0	Byte=0
3	1	See Text #1
4	-	Not Used
5	-	Not Used
6	-	See Text #2
7	-	See Text #3
8	-	See Text #2

#1. The byte contains the restart command, which identifies the operation in progress when the interrupt occurred. This byte is set to 06 to indicate that a read operation was in progress or 05 to indicate a write operation. The system recovery program uses this command -- along with the information in the Channel Status Word (CSW) -- to make a new Channel Command Word (CCW). The new CCW is issued to the storage director, after correcting the unusual condition, to continue the operation following the interrupt.

#2. The byte indicates the controller physical identifier byte assigned during installation. The storage director reads and stores the identifier for use in sense messages.

#3. The byte indicates the controller physical identifier of the selected controller, but not necessarily the controller with a Check-1 condition. If:

- Byte 3, Bit 0 and Byte 11, Bit 0 are off

or if

- Byte 3, Bit 0 is on and Byte 11, Bit 1 is off;

then the other controller on the director-to-device controller (DDC) interface has the Check-1.

Sense Byte 3 -- Residual Record Count (w/SMB)

Byte 3 is set when a Locate Record channel command word is terminated by a Unit Check and Byte 2, Bit 5 (Imprecise Ending) is set. Byte 3 contains the number of unprocessed records remaining when the unit check occurs. The count includes the record in which the error occurred.

Sense Byte 4 -- Device Physical Identifier

Sense Byte 4 contains the device physical identifier and configuration data.

Byte 4, Bit 0 -- DPSE Function

Bit 4 sets if the dynamic path selection extended function is installed.

Byte 4, Bit 1 -- Not Used

Byte 4, Bit 2 -- Permanent Path Error

Bit 2 sets in Format 7 when the path to the controller has a permanent error. (Bit 2 is reserved in all other formats except Format 7.) It is a signal to the operating systems to attempt device selection through another path. Any error recovery actions or new requests for the device should be sent over alternate paths if any exist.

After assembly of Format 7 sense bytes (controller Check-1), the check condition should be reset. If the check condition (connection check alert) persists after the reset, Format 7 sense data contains the permanent path error, indicating the failing controller is partitioned off. Partitioning is done to provide availability to a second controller that can be attached to the same storage director. Only a system reset or se-

lective reset partitions on the failing controller. Once a controller is partitioned off, any Start I/O or Test I/O command addressed to any device on that string receives:

- Format 7 sense data with the permanent path error bit set
- Condition code 3

Since a request connection check (RCC) sequence cannot be used to assemble this sense data, no controller Check-1 information is included.

Byte 4, Bit 3 -- Reserved

Byte 4, Bits 4-7 -- Device Address

These bits identify the device address.

Sense Bytes 5 and 6 -- Seek Address

Sense Bytes 5 and 6 contain the physical cylinder and head address sent by the storage director to the device.

Sense Bytes 5 and 6 are not used in Format 6.

Sense Byte 7 -- Format/Message

Byte 7, Bits 0 through 3 -- Sense Byte Format

Identify the meaning (format) of Sense Bytes 8 through 23. Formats are as follows:

FORMAT	CONDITION
0	Program or system checks (messages only; Sense Bytes 8-23 are not used). Refer to applicable storage control troubleshooting manual.
1	Device equipment checks
2	Storage director equipment checks. Refer to applicable storage control troubleshooting manual.

FORMAT	CONDITION
3	Storage director control checks. Refer to applicable storage control troubleshooting manual.
4	Data checks not providing displacement information (uncorrectable data checks). Contents of Bytes 8-13 are unreliable if message in Byte 7 is 0, 1, 4, or 5.
5	Data checks providing displacement information (correctable data check). Contents of Bytes 8-12 are unreliable if message in Byte 7 is 0, 1, or 9.
6	Usage/error statistics
7	Controller Check-1
8	Controller equipment checks

Byte 7, Bits 4 through 7 -- Message Code

Describe the specific nature of the error described in Sense Bytes 8 through 23 for each format.

Format 1 Messages, Byte 7

The message code is in Bits 4 through 7 of Byte 7.

Format 1, Byte 7, Message 0 -- No Message

Format 1, Byte 7, Message 1 -- Device Status 1 Not As Expected

This message indicates the storage director has received an unexpected status from the device following an interrupt from the device. In this case, Sense Byte 9 contains the actual status received from the device and Byte 18 contains the status expected by the storage director.

Format 1, Byte 7, Message 2 -- Reserved

Format 1, Byte 7, Message 3 -- Index Missing

The storage director detected a missing index.

Format 1, Byte 7, Message 4 -- Interrupt Not Resettable

When resetting an interrupt, the storage director notes if the condition immediately appears again. The storage director masks the interrupt from the device. A Start I/O or Test I/O command allows the interrupt to be seen again by the storage director. Sense Bytes 8 and 9 contain a command code and response that are valid but may not indicate the interrupt condition.

Format 1, Byte 7, Message 5 -- Device Does Not Respond to Selection

No selection response from device - This message is set when the controller does not receive the CDP tag valid status on device selection.

Format 1, Byte 7, Message 6 -- Device Check-2 or Set Sector Incomplete

The device detects a Check-2 condition or is unable to complete a Locate Record command or operation (offset cylinder and locate record). Bits 3 and 7 are on in Sense Byte 19.

Format 1, Byte 7, Message 7 -- Head Address Miscompare

Following any seek operation, the storage director detects a difference between the expected head address and the head address read from the Home Address (HA) or count field when unoriented. Sense Bytes 16 and 17 contain the address read from the disk. Bytes 5 and 6 contain the desired address.

Format 1, Byte 7, Message 8 -- Device Status 1 Invalid

The storage director, on initial selection, receives an invalid combination of bits in device status 1. The actual status received is in Sense Byte 19. Byte 8 contains the command executed.

Format 1, Byte 7, Message 9 -- Device Not Ready For Customer Work

The device is in either a power-on or power-off sequence.

Format 1, Byte 7, Message A -- Track Physical Address Miscompare While Oriented

The storage director detects a difference between the expected and the actual cylinder head address read from the HA or count field. Before this check, track orientation is established, and the physical address read from the disk is correct. Sense Bytes 16 and 17 contain the actual address read from the disk, while Bytes 5 and 6 contain the expected address.

Format 1, Byte 7, Message B -- Not Used

Format 1, Byte 7, Message C -- Drive Motor Switch Sensed

The front or rear drive motor switch is in the OFF position.

Format 1, Byte 7, Message D -- Seek Incomplete

The device cannot correctly position the access mechanism after a seek or rezero operation. Bits 2 and 7 are on in Sense Byte 19.

Format 1, Byte 7, Message E -- Cylinder Address Miscompare

Following any seek, the storage director detects a difference between the expected cylinder address and the cylinder address in the physical address bytes of an HA or count area read from an unoriented state. Sense Bytes 16 and 17 contain the actual address read from the disk, while Bytes 5 and 6 contain the expected address.

Format 1, Byte 7, Message F -- Offset Active Not Resettable

The storage director cannot reset the Offset Active bit in the device status 2 byte (Bit 2 of Sense Byte 20).

Format 4 Messages, Byte 7

The message is in Bits 4 through 7 of Byte 7.

Format 4, Byte 7, Message 0 -- Home Address, ECC Uncorrectable

This message is generated if an error occurs in the Home Address area and the error is not correctable by error checking and correction (ECC).

Format 4, Byte 7, Message 1 -- Count Area, ECC Uncorrectable

This message is generated if an error occurs in the count area and the error is not correctable by error checking and correction (ECC).

Format 4, Byte 7, Message 2 -- Key Area, ECC Uncorrectable

This message is generated if an error occurs in the key area and the error is not correctable by error checking and correction (ECC).

Format 4, Byte 7, Message 3 -- Data Area, ECC Uncorrectable

This message is generated if an error occurs in the data area and the error is not correctable by error checking and correction (ECC).

Format 4, Byte 7, Message 4 -- Home Address Area, No Sync Byte Found

This message is generated if the sync byte in the Home Address area is not detected.

Format 4, Byte 7, Message 5 -- Count Area, No Sync Byte Found

This message is generated if the sync byte in the count area is not detected, but count area information is detected.

Format 4, Byte 7, Message 6 -- Key Area, No Sync Byte Found

This message is generated if data synchronization on the key area is unsuccessful.

Format 4, Byte 7, Message 7 -- Data Area, No Sync Byte Found

This message is generated if data synchronization on the data area is unsuccessful.

Format 4, Byte 7, Message 8 -- HA Area, ECC Uncorrectable with Offset Active

This message is generated if a successful recovery is made from an ECC data check in the Home Address area using head offset.

Format 4, Byte 7, Message 9 -- Count Area, ECC Uncorrectable with Offset Active

This message is generated if a successful recovery is made from an ECC data check in the count area using head offset.

Format 4, Byte 7, Message A -- Key Area, ECC Uncorrectable with Offset Active

This message is generated if a successful recovery is made from an ECC data check in the key area using head offset.

Format 4, Byte 7, Message B -- Data Area, ECC Uncorrectable with Offset Active

This message is generated if a successful recovery is made from an ECC data check in the data area using head offset.

Format 4, Byte 7, Message C -- HA Area, No Sync Byte Found with Offset Active

This message is generated if a successful recovery is made from a no sync byte found condition in the Home Address area using head offset.

Format 4, Byte 7, Message D -- Count Area, No Sync Byte Found with Offset Active

This message is generated if a successful recovery is made from a no sync byte found condition in the count area using head offset.

Format 4, Byte 7, Message E -- Key Area, No Sync Byte Found with Offset Active

This message is generated if a successful recovery is made from a no sync byte found condition in the key area using head offset.

Format 4, Byte 7, Message F -- Data Area, No Sync Byte Found with Offset Active

This message is generated if a successful recovery is made from a no sync byte found condition in the data area using head offset.

Format 5 Messages, Byte 7

The message code is in Bits 4 through 7 of Byte 7. Messages in Format 5 identify the portion of the record where the data check occurs. Correctable data checks are normally entered in the storage director buffered logs and only recorded on counter overflow.

Format 5, Byte 7, Message 0 -- Home Address Area

This message is generated if the correctable error occurs in the Home Address area.

Format 5, Byte 7, Message 1 -- Count Area

This message is generated if the correctable error occurs in the count area.

Format 5, Byte 7, Message 2 -- Key Area

This message is generated if the correctable error occurs in the key area.

Format 5, Byte 7, Message 3 -- Data Area

This message is generated if the correctable error occurs in the data area.

Format 5, Byte 7, Messages 4-7 -- Not Used

Format 5, Byte 7, Message 8 -- Home Address Area, Offset Active

This message is generated if the correctable error occurs in the Home Address area with offset active.

Format 5, Byte 7, Message 9 -- Count Area, Offset Active

This message is generated if the correctable error occurs in the count area with offset active.

Format 5, Byte 7, Message A -- Key Area, Offset Active

This message is generated if the correctable error occurs in the key area with offset active.

Format 5, Byte 7, Message B -- Data Area, Offset Active

This message is generated if the correctable error occurs in the data area with offset active.

Format 5, Byte 7, Messages C-F -- Not Used

Format 7 Messages, Byte 7

The message code is in Bits 4 through 7 of Byte 7.

Format 7, Byte 7, Message 0 -- RCC Initiated by a Connection Check Alert

This message is generated when the storage director finds the Connection Check Alert (CCA) line active or detected a tag in check.

Format 7, Byte 7, Message 1 -- RCC1 Sequence Not Successful

This message is generated when the storage director performs a request connection Check-1 (RCC1) sequence to the selected controller and does not find a successful transfer indication. A successful transfer is indicated as follows:

- Byte 11, Bits 4 or 5 = 1
- Bytes 17 or 19, Bit 6 = 1

All other combinations indicate an unsuccessful transfer.

Format 7, Byte 7, Message 2 -- RCC1 and RCC2 Sequence Not Successful

This message is generated when the storage director cannot complete an RCC2 sequence after an unsuccessful RCC1 sequence. The storage director finds either the Power bit off or the Clear bit on. The storage director does not replace an existing message with this message.

Format 7, Byte 7, Message 3 -- Invalid Tag In During Selection Sequence

This message is generated when one of the following occurs:

- Before controller selection, the storage director notes that the inbound tags are not in a null condition, or that the CCA or tag in check bits are active.

- After selection, the controller fails to respond to a tag out other than a command tag within the permitted response time.

- After selection the response received was other than the tag expected. See Byte 8 for more details.

Format 7, Byte 7, Message 4 -- Extra RCC Required

An extra RCC was required because the controller isolated itself or the storage director found a CCA on cleanup when it performed an RCC without a CCA.

Format 7, Byte 7, Message 5 -- Invalid DDC Selection Response

This message is generated when one of the following occurs:

- The storage director microcode does not successfully compare the data on bus in 1 and the correct address of the desired controller (the response received in Byte 9, Bits 6 and 7) during a selection sequence.

- The storage director times out waiting for a response during a selection sequence. In this case, the permanent path error bit was off and the controller identifier stored in the storage director was not FF. This could be caused by the Enable/Disable switch being in the Disable position.

Format 7, Byte 7, Message 6 -- Missing End Operation, Transfer Was Complete

This message is generated when the storage director completes a data transfer, the transfer count equals zero, and the storage director does not receive an associated end operation signal from the controller within the time allowed.

Format 7, Byte 7, Message 7 -- Missing End Operation, Transfer Was Incomplete

This message is generated when a read or write operation does not complete the data transfer and the end operation signal does not return within the time allowed.

Format 7, Byte 7, Message 8 -- Invalid Tag In for an Immediate Command Sequence

The storage director was in an immediate command sequence and found one of the following:

- The tag in was in an unexpected state before the command was issued.
- The tag in response was not returned within the expected time.
- The tag in response was not either valid or end operation. See Byte 8 for more details.

Format 7, Byte 7, Message 9 -- Invalid Tag In for an Extended Command Sequence

The storage director was in an extended command sequence and found one of the following:

- The tag in was in an unexpected state before the command was issued.
- The tag in response was not returned within the expected time.
- The tag in response was not either end operation or selected null.

Format 7, Byte 7, Message A -- Storage Director Microcode Timed Out on Deselection

This message is generated when the storage director microcode time out exceeds the allotted time during deselection while waiting for deselection to complete.

Format 7, Byte 7, Message B -- No Selection Response After Poll Interrupt

This message is generated when the storage director does not receive response from the device presenting a poll interrupt.

Format 7, Byte 7, Message C -- Controller Not Available

This message is generated when the storage director cannot communicate with the controller because it could not, on a previously detected Check-1 error, reset the CCA line. It indicates that the path is unusable because the interface is in a fenced condition.

The Sense Bytes, 8 through 23, assigned with this message are from the sense data collected from the controller after the error that caused the fence condition, with Byte 7 placed in Byte 20.

Format 7, Byte 7, Messages D through F -- Not Used

Format 8 Messages, Byte 7

The message code is in Bits 4 through 7 of Byte 7.

Format 8, Byte 7, Message 0 -- No Message

This message is generated if no additional information is available. Byte 9 contains the end operation response if Byte 10, Bit 7 is a one.

Format 8, Byte 7, Message 1 -- ECC Hardware Check

This message is generated when the pattern portion of the error correction code syndrome passed to the storage director after a data check contains all zeros. This error probably occurs because of a hardware failure within the error checking and correction circuits.

Format 8, Byte 7, Message 2 -- Reserved

Format 8, Byte 7, Message 3 -- Unexpected End Operation Response Code Received

This message is generated when the storage director receives an unexpected response to the command issued. Byte 8 contains the command issued and Byte 9 contains the response.

Format 8, Byte 7, Message 4 -- End Operation Received with Transfer Count Not Equal to Zero

This message is generated when the storage director receives an end operation tag during a read or write operation and the storage director transfer count is not zero. Byte 9 contains the end operation code.

Format 8, Byte 7, Message 5 -- End Operation Received with Transfer Count Equal to Zero

This message is generated when the storage director receives an end operation tag during a read or write operation and the storage director transfer count is zero. Byte 9 contains the end operation code.

Format 8, Byte 7, Message 6 -- DPSE Cleanup Checks on Channel or System Reset

During a channel or system reset, the storage director had difficulty in reading or writing into the controller DPSE arrays.

Format 8, Byte 7, Messages 7-F -- Not Used

FORMAT 1, SENSE BYTES 8 THROUGH 23 -- DEVICE EQUIPMENT CHECKS

Format 1 consists of all device check-2 errors. It is generated when the storage director detects:

- An end operation response code of 20.
- A seek incomplete or cylinder address miscompare error when the seek check counter overflows, or when in forced logging mode.
- A failure as defined by the message code in Byte 7.

Format 1, Sense Byte 8 -- DDC Bus Out 0

Sense Byte 8 contains the command or command modifier issued by the storage director before error detection.

Format 1, Sense Byte 9 -- DDC Bus In 1

Sense Byte 9 shows the contents of DDC Bus In (bus 1) to the storage director, during initial selection, ending operations, or after sensing device status information. The message in Byte 7 defines the byte contents if it does not contain the end operation tag response.

The controller end operation response code to the storage director is contained in DDC Bus In 1 when the end operation tag is active. When the end operation response code is important, it is reported in Byte 9 of Format 1 or Format 8. End operation bit definition when the end operation tag is active is:

Bit 0	Index found
Bit 1	No sync byte and no data found (No Record Found)
Bit 2	End operation code
Bit 3	End operation code
Bit 4	End operation code
Bit 5	End operation code
Bit 6	End operation code
Bit 7	End operation code

Format 1, Byte 9, Bit 0 -- Index Found

Bit 0 sets when index occurs during the execution of any oriented command that causes the command to be terminated, or that prevents following oriented commands from being issued. The index found bit is included in the ending status for that command.

Format 1, Byte 9, Bit 1 -- No Sync Byte Found and No Data Found

Bit 1 sets when the sync byte or data transitions are not detected by the serializer/deserializer (SERDES) shift register during the preceding read or search operation. This bit indicates that there are no more records on the track.

Format 1, Byte 9, Bits 2-7 -- End Operation Codes

These are hexadecimal codes of Bits 2 through 7 of the end operation bus 1 byte. These codes indicate the cause of the end operation response.

00 No check and successful completion of the preceding command.

01 DDC command overrun -- This code sets when the controller indicates to the storage director that while the controller was oriented, the command did not arrive on time. The storage director then retries the operation up to two times. If this code repeats, the storage director collects Format 8 sense data.

02 Sync byte missing but data found -- This code sets when the controller indicates to the storage director that the expected sync byte is not found. The storage director retries the operation using data check recovery procedures and reports failures in Format 4, Sense Byte 7, error messages to identify the area with a missing sync byte.

03 Data check -- This code sets when the controller detects a Data Check. Errors are reported in Formats 4 or 5. The end operation code does not appear in the sense bytes.

06 Invalid command code -- This code sets when the controller detects an invalid command code. The storage director reports a Format 8 equipment check and performs ERP equipment check recovery procedures.

07 Not used.

08 HAR modifier overrun on set HAR oriented -- This code sets when the controller detects that the HAR modifier did not arrive in time to remain oriented. The storage director reports a Format 8 equipment check and performs ERP equipment check recovery procedures.

09 No selection response from device -- This code sets when the controller-to-device port (CDP) tag valid is not received on device selection by the controller.

10 Check-2 detected within the controller or Check-1 detected in the device logic -- This code sets when a Check-2 condition is detected within the controller or when a Check-1 is detected in the CDP or device logic. Check conditions are detected by the controller hardware or the microcode. If the storage director receives 10 as the end operation code, the storage director collects the controller fault log bytes, and reports the assembled bytes in Format 8.

11 Device Check-1 on selection -- This code sets when the controller detects a device Check-1 condition, whether or not the device on the active port is selected or unselected. A Format 8 error message is assembled and reported, and the failing operation is retried.

13 CDP hung due to late or missing device response -- This code sets when the controller did not receive a device response within the correct time after device selection on an immediate command or command modifier.

14 Not used.

15 Not used.

16 Not used.

17 Not used.

18 Not used.

19 Device dropped to null -- This code sets when the controller detects that the CDP device tag in is at null instead of tag valid, or end operation.

1B Index found during defect skip in Home Address area -- This code sets when the controller finds the index bit on while performing a defect skip in the Home Address area.

20 Device check active -- The storage director assembles the Format 1 sense bytes when device check is active. The device sense bytes are collected and ERP equipment check procedures are performed.

Format 1, Sense Byte 10 -- Device Power Status

Sense Byte 10 lists the status of motors, motor brakes, motor thermals, air flow, and drive sequence completion.

Format 1, Byte 10, Bit 0 -- Voltage Margins Active

Bit 1 is a status bit set when a command is received to set high or low voltage margins.

Format 1, Byte 10, Bit 1 -- Motor Thermal

Bit 1 is an error condition set when the drive motor thermal is open. The two most probable causes of this motor thermal are overheating or an open thermal sense circuit.

Format 1, Byte 10, Bit 2 -- No Air Flow

Bit 2 is an error condition that sets if there is no air flow at the exit of the air mover assembly. The air flow is sensed by an air pressure switch. This switch causes the four drives to stop or fail to start if there is no air flow.

Format 1, Byte 10, Bit 3 -- Device Sequence Complete

Bit 3 is a status bit set when either of the two device sequences complete a normal power-on sequence. The bit is set after the rezero operation and a three minute warm-up clean cycle.

Format 1, Byte 10, Bit 4 -- Motor Run Latch On

Bit 4 is a status bit set when the motor run latch is activated during the device sense command.

Format 1, Byte 10, Bit 5 -- Motor Contactor Active

Bit 5 is a status bit set when the motor contactor relay is activated.

Format 1, Byte 10, Bit 6 -- Motor Brake Latch On

Bit 6 is a status bit set when the motor brake latch is in a brake condition during the device sense command.

Format 1, Byte 10, Bit 7 -- Brake Applied

Bit 7 is a status bit set when the motor brake is applied and the motor is not running.

Format 1, Sense Byte 11 -- Device Check Register

Sense byte 11 defines a register that contains device associated checks.

Format 1, Byte 11, Bit 0 -- Error Flag (Checkpoint Check)

Bit 0 sets when an error is detected in one of the checkpoint log monitored routines. The error status is displayed in Byte 15.

Format 1, Byte 11, Bit 1 -- Servo Control Check

Bit 1 sets when one of the error detection circuits on the servo analog control board detects an error in the servo control logic. The error can be due to an error in the servo analog control board or in one of the interacting field-replaceable units (FRUs).

Format 1, Byte 11, Bit 2 -- RPS Check

Bit 2 sets when one of the error detection circuits on the rotational position sensing (RPS) board detects one of the following errors:

- Missing index
- Extra index
- Sector compare fault
- Cell fault
- Incorrect pattern
- Clock fault
- Target register parity fault

Format 1, Byte 11, Bit 3 -- Checkpoint Log Parity Error

Bit 3 sets when a parity check is detected in the checkpoint log.

Format 1, Byte 11, Bit 4 -- Not Used

Format 1, Byte 11, Bit 5 -- Power Card Check

Bit 5 sets when there is a power problem. Examine Byte 10 (device power status) and the checkpoint log (Byte 15) for the cause.

Format 1, Byte 11, Bit 6 -- Read/Write Check

Bit 6 sets when any read/write check occurs. See Bytes 12, 13, or 14 for additional details about read/write checks.

Format 1, Byte 11, Bit 7 -- Not Used

Format 1, Sense Byte 12 -- Read/Write Status 1

Sense Byte 12 indicates checks on the actuator matrix board, detector board, and data path.

Format 1, Byte 12, Bits 0 and 1 -- Read/Write Check

Bit 0 sets if there is an error in the even address matrix board. Bit 1 sets if there is an error in the odd address matrix board. The matrix errors are described in more detail in Bits 2 through 4.

Format 1, Byte 12, Bits 2-4 -- Matrix Sense

Bits 2 through 4 further define Bits 0 and 1 of Byte 12 and indicate the type of check detected on the actuator matrix board.

000 Not used.

100 Write Transition Check -- This check occurs when there are no write transitions in write mode.

010 Write Current Check -- This check occurs when write current is present in any read/write control other than write, or no write current in write mode. It indicates no write current is present during a write operation.

110 Head Select Check -- This check occurs when a head is not selected when there should be, or more than one head is selected at the same time during a read operation.

001 Safety Active Check -- This check occurs when the Safety Active line remains up after a write operation starts.

101 Write Gate Check -- This check occurs when Write Gate comes up before write select.

011 Read Sequence Check -- This check occurs when Bit 7 (Unsquelch) is active before Bit 5 (Read Gate).

111 Voltage Safety Check (±5 and -8.2 volts) -- This check occurs when the power lines to the actuator matrix board are open or shorted. The required voltage is missing.

Format 1, Byte 12, Bits 5-7 -- Not Used

Format 1, Sense Byte 13 -- Read/Write Status 2

Sense Byte 13 lists checks that involve control lines for read/write operations.

Format 1, Byte 13, Bit 0 -- Read/Write Check

Bit 0 sets when more than one actuator matrix board or no actuator matrix board is selected during a read/write operation. This check stops a write operation.

Format 1, Byte 13, Bit 1 -- Pad Check

Bit 1 sets when a Pad Check is detected during a device pad operation. The Pad Check is caused by an error during padding or by the controller stopping the operation.

Format 1, Byte 13, Bit 2 -- Write Sequence Check

Bit 2 sets when the read/write control board receives an incorrect sequence of signals for a write operation or when a read/write control hardware failure occurs.

Format 1, Byte 13, Bit 3 -- Read Sequence Check

Bit 3 sets when the read/write control board receives an incorrect sequence of signals for a read operation or when a read/write control hardware failure occurs.

Format 1, Byte 13, Bit 4 -- Read/Write Control Check

Bit 4 sets when the read/write control circuits determine than both read and write operations are active at the same time.

Format 1, Byte 13, Bit 5 -- Write Overrun Check

Bit 5 sets when Write Gate is active when passing both edges of index. This check stops the write operation.

Format 1, Byte 13, Bit 6 -- Read/Write Servo Check

Bit 6 sets when the servo loses a coarse track signal during a read operation or loses a write ready signal during a write operation.

Format 1, Byte 13, Bit 7 -- HAR Parity Check

Bit 7 sets when there is a parity error in the Head Address register (HAR).

Format 1, Sense Byte 14 -- Not Used

Format 1, Sense Byte 15 -- Checkpoint Log

The checkpoint log is a register on the device sequencer write bus (physically located on the servo analog control board). Important checkpoints are identified in several device sequencer code routines and, under normal operation, the register is updated each time the device sequencer code passes a given

checkpoint successfully. When Device Check becomes active, the contents of the Checkpoint register are held until read out and check reset is activated.

Format 1, Byte 15, Bits 0-3 -- Routine

Bits 0 through 3 list the microcode routine in use when an error occurs. Routines are defined as follows:

Bits 0	1	2	3	
0	0	0	0	Clear, purge and idle
0	0	0	1	Common servo failures
0	0	1	0	Drive power on
0	0	1	1	Drive power off
0	1	0	0	Rezero operation
0	1	0	1	Seek operation
0	1	1	0	Offset operation
0	1	1	1	Record search operation
1	0	0	0	I/O
1	0	0	1	Self test
1	0	1	0	Power up
1	0	1	1	Power down
1	1	0	0	Seek to -3
1	1	0	1	Self test
1	1	1	0	Not used
1	1	1	1	Search power up/down

Format 1, Byte 15, Bits 4-7 -- Checkpoints

Bits 4 through 7 list the last checkpoint successfully passed before an error occurs. Refer to table 1C-1.

TABLE 1C-1. FORMAT 1, BYTE 15, BITS 4-7 CHECKPOINTS

Code	Checkpoint
00	Idle loop entered and TDF code
01	DC not good
02	Fan stopped
03	AGC not good
04	Motor not up to speed
05	AGC and no motor
06	Speed and no motor
09	First check reset
0B	Second check reset
0C	Diagnostic parity check
0F	Write inhibit not active
18	EMS recovery routine entered
19	Other device not spinning
1A	No response from switch
1B	Other device - servo not ready
1C	EMS normal routine entered
1D	Normal device - servo not ready
20	Drive motor power-on sequence started
21	Guardband 2 found
22	3-minute clean routine started
23	MPU fault
24	Seek to -3 cylinder command accepted
26	Sequence timeout - servoing
27	Access error during first seek
28	AGC, greater than 2400 r/min, motor sense, or motor good failed during first seek

Table Continued on Next Page

TABLE 1C-1. FORMAT 1, BYTE 15, BITS 4-7 CHECKPOINTS (Contd)

Code	Checkpoint
2A	Set check point log
2B	Brake pulled
2C	Compress
2D	Motor on
2E	Surge complete, compress on
30	Drive motor power-off sequence started
31	Power off, park complete
32	Drive motor contactor off as expected
33	Brake dropped
3B	Register 1 parity check command accepted
3C	Register 2 parity check command accepted
40	Rezero command accepted
47	AGC or PLL failed during rezero
48	GBID error
49	Motor not on
4A	On track error
4B	GBOD error
4D	Access timeout
4F	Overshoot check
50	Seek command accepted
51	Track crossing error
52	Track following in progress
55	Set checkpoint log
56	AGC or PLL failed during seek
57	Illegal length seek

Table Continued on Next Page

TABLE 1C-1. FORMAT 1, BYTE 15, BITS 4-7 CHECKPOINTS (Contd)

Code	Checkpoint
59	Track following failed
5A	Guardband sensed during seek motion
5B	Access timeout
5C	Overshoot during seek operation
5E	Error - offset active
60	Offset command accepted
63	Access timeout
64	Track following failed
65	On track error
66	AGC or PLL failed during offset
68	Offset exceeded offset value
69	Offset in guardband
6E	Diagnostic set difference hi
6F	Diagnostic set difference lo
70	Search sector command accepted
71	Sector search in progress
72	Sector found
73	Go-around, search sector in progress
74	Search routine exit
75	Reset interrupt routine entered
76	Diagnostic set TAR
7F	RAS write inhibit active
83	Illegal command code
87	Busy with no pad in progress
88	Device busy (command rejected)

Table Continued on Next Page

TABLE 1C-1. FORMAT 1, BYTE 15, BITS 4-7 CHECKPOINTS (Contd)

Code	Checkpoint
89	AGC up but spindle not spinning
8A	Parameter transfer timeout
8B	Command timeout
90	Test bits lower B14=0 not reset
91	Test bits upper B14=0 not reset
92	Test bits lower B14=1 not reset
93	Test bits upper B14=1 not reset
94	Flags failed to set
95	Flags failed to clear
96	Flags failed to set
97	Flags failed to clear
98	Timer test started
99	Can't force timeout
9A	Can't inhibit timeout
9B	Timer Bit 2 doesn't load
9C	Can't inhibit timer clock
9D	Time failed to count
9E	Timer Bit 1 doesn't load
9F	Time clock chip bad
A0	Airflow during power-on sequence
A5	Drive motor switch off, command reject
A7	Compress current still on after park
A9	AGC not active at end of 9-second compress
AB	AGC lost during 3-minute clean cycle
AC	Drive motor not running after 9 seconds

Table Continued on Next Page

TABLE 1C-1. FORMAT 1, BYTE 15, BITS 4-7 CHECKPOINTS (Contd)

Code	Checkpoint
AE	AGC active, expected not active
B1	Park failed during power off sequence
B2	Drive motor relay failed to drop
B5	AGC active and drive motor off in idle routine
B9	Brake on, expected off
B9	Compress current on before drive motor on
BA	Compress failed before drive motor on
BC	Spindle not coasting
BE	AGC fault during search
BF	Speed loss during search
C0	Device busy (command reject)
C1	GBID error
C2	GBOD error
C3	Access timeout
C4	Overshoot check
C5	Track following failed
C6	Track crossing error
C7	CAR not equal to zero
CA	AGC or PLL failed during -3 seek
D0	Timer Bit 4 doesn't load
D1	Timer Bit 8 doesn't load
F0	Brake on and motor on
F1	MPU fault
F2	Speed loss
F3	Hard index failure

Table Continued on Next Page

TABLE 1C-1. FORMAT 1, BYTE 15, BITS 4-7 CHECKPOINTS (Contd)

Code	Checkpoint
F4	HDA cable fault
F5	Busy after reset interrupt
F6	Sector flag not set
F7	PLL fault
F8	Sector not found
F9	Power off condition during sector search
FB	Motor switch off during sector search
FC	Brake failed to pick
FD	Guardband 2 not found
FE	DC voltage fault
FF	TDF code

Format 1, Sense Bytes 16 and 17 -- Physical Track Address Read or Expected Status

Sense Bytes 16 and 17 show mismatched cylinder addresses. If the storage director detects an address miscompare between the addresses (cylinder and head) expected and the addresses read, these bytes show the address bytes read. These bytes are referred to in Format 1 messages 7, A, and E. If the message is 1 (device status not as expected), then Byte 16 contains the expected device status 1.

Format 1, Sense Byte 18 -- Not Used

Format 1, Sense Byte 19 -- Device Status 1

The bits in sense byte 19 indicate the functional status of the device selected.

Format 1, Byte 19, Bit 0 -- Pad in Progress

Bit 0 sets when the selected device read/write path is write-padding and not available.

Format 1, Byte 19, Bit 1 -- Servo Inhibited

Bit 1 sets when the servo system in not track following and loses all orientation. Recovery is attempted by executing a Rezero command.

Format 1, Byte 19, Bit 2 -- Seek Incomplete

Bit 2 sets when the device sequencer times out on a seek operation. The device sequencer times and checks each seek operation. An interrupt (Bit 7) is set on timeout and remains set until reset by a successful rezero operation. Bit 7 is also active if the device must signal an interrupt.

Format 1, Byte 19, Bit 3 -- Device Check-2 or Set Sector Incomplete

Bit 3 sets when the device sequencer times out on a set sector operation. The set sector operation is part of the locate record, locate cylinder and record, and offset cylinder and record commands. The device sequencer times and checks each set sector. An interrupt is issued on time out. This bit remains active until reset by the storage director. Bit 7 is also active. Check-2 is defined as any bit active in the Check register (Byte 11).

Format 1, Byte 19, Bit 4 -- On Line

Bit 4 is set by the device sequencer logic when the device power-on sequence is successfully completed and the device is ready to resume normal operations. This bit remains active until the logic power or the motor switch is turned off. A device that is not on line indicates Device Busy in device status 1 (Byte 19) or Spindle Off in device status 2 (Byte 20).

Format 1, Byte 19, Bit 5 -- HDA Attention

Bit 5 sets when the device sequencer starts an HDA attention interrupt at the completion of the device power-on sequence.

Format 1, Byte 19, Bit 6 -- Device Busy

Bit 6 is set by the device sequencer during any of the following operations:

- Locate
- Offset
- Rezero
- Pad in progress
- Search sector
- Power on or power off

The device sequencer resets device busy at completion of the operation or when a clock timeout occurs. During the search sector operation, the device busy bit remains active until the desired sector is found. Device busy can be active with an outstanding interrupt that has not been serviced. Device busy indicates that the device is not ready (during power-on or power-off sequence for HDA or logic) with Bit 4 off (not On Line). Sense Byte 0, Bit 1 (Intervention Required) is active if a device is selected that is not ready.

Format 1, Byte 19, Bit 7 -- Seek or Set Sector Interrupt or Sector Search

Bit 7 is set by the device sequencer during these conditions:

- A successful or unsuccessful completion of a Locate, Offset, or Rezero command. The device must signal an interrupt.
- A Locate or Offset command is in progress. The locate interrupt bit is set during the locate record portion of these commands.
- A pad complete is being executed in either device. The device must signal an interrupt.
- The busy-to-not-busy transition is in progress and the device is selected while busy.
- The HDA attention is in progress.

For each of these commands from a storage director, an interrupt must be returned to that storage director to indicate successful or unsuccessful completion of the command.

- Locate record command
- Locate cylinder command (when the cylinder difference is not zero)
- Locate cylinder and record command
- Start rezero command
- Offset cylinder command
- Offset cylinder and record command

If another device on the same read/write path is padding, the locate, offset, or rezero complete interrupt is not presented until the padding is complete.

When a storage director selects a busy device, the interrupt is returned when the device is no longer busy.

When a storage director requires an HDA interrupt during the device power-on sequence, the interrupt is presented at the completion of the power-on sequence. The reset interrupt command resets any interrupt or pending interrupt except a pending HDA attention interrupt. The check reset command resets any interrupt or pending interrupt except a pending or active HDA attention interrupt.

Format 1, Sense Byte 20 -- Device Status 2

The bits of Sense Byte 20 show the status of the hardware.

Format 1, Byte 20, Bit 0 -- Device Logic Disabled

Bit 0 active indicates a device logic switch is in the disabled position.

Format 1, Byte 20, Bit 1 -- Surge Complete

Bit 1 on indicates early completion of the motor start current surge (within nine seconds after HDA power on). This bit is used only by the controller or CE diagnostic programs.

Format 1, Byte 20, Bit 2 -- Offset Active

Bit 2 on indicates the servo circuits are being operated with offset active. The device sequencer resets this bit when an offset operation is performed with a zero value in the Difference counter or a Rezero command.

Format 1, Byte 20, Bit 3 -- Spindle Off

Bit 3 on indicates the motor switch is off. Sense Byte 0, Bit 1 (Intervention Required) is set when a device is selected with device power off.

Format 1, Byte 20, Bits 4 and 5 -- Not Used

Format 1, Byte 20, Bit 6 -- Right Access Mechanism Selected

Bit 6 on indicates the right access mechanism logic or the even address device is selected.

Format 1, Byte 20, Bit 7 -- Left Access Mechanism Selected

Bit 7 on indicates the left access mechanism logic or the odd address device is selected.

Format 1, Sense Byte 21 -- Storage Director Physical Identifier

Sense Byte 21 is the storage director identifier that is assigned by the CE. This identifier appears in environmental recording, editing, and printing (EREP) reports to identify the storage director in use at the time of failure.

Format 1, Sense Bytes 22 and 23 -- Fault Symptom Code

The symptom code displayed is generated by the storage director from sense data.

FORMAT 4, SENSE BYTES 8 THROUGH 23 -- UNCORRECTABLE DATA CHECKS

Format 4 lists data checks without displacement information. This format is generated when:

- Errors that were not correctable by error-checking and correction (ECC) are detected after retry has been unsuccessful. Byte 1, Bit 0 (Permanent Error) is also set.
- ECC uncorrectable errors were detected in the count, key or data field. Byte 7 identifies the field that caused the error.
- Error log information was off-loaded after an ECC uncorrectable error occurred during error logging. Information was recovered through use of command retry. Byte 2, Bit 3 (Environmental Data Present) is also set.

Format 4, Sense Bytes 8-12 -- Record Identification

Sense Bytes 8 through 12 contain the record identification (CCHHR) obtained from the count field for the record in which the error occurs (C-cylinder, H-head, R-record number).

The contents of Bytes 8 through 12 are unreliable if the message code in Byte 7 is either 0 or 4 (error occurred in Home Address) or 1 or 5 (error occurred in count field).

Sense Byte 12, the record number, is set to zero if the error occurs in Home Address. This byte is unreliable after a space count.

Bytes 5 and 6 contain the physical address of the data. Bytes 8 through 12 contain the logical address assigned by the system for other than the Home Address area.

Format 4, Sense Byte 13 -- Sector Number

Sense Byte 13 contains the sector number of the record. This byte may not be valid if there is a count area data check.

The contents of Byte 13 are unreliable if the message code in Byte 7 is 0, 1, 4, or 5.

Format 4, Sense Byte 14 -- Controller Physical Identifier

Sense Byte 14 is the controller physical identifier. It identifies the controller in use when the failure occurs.

Format 4, Sense Byte 15 -- Head Offset Increment/Direction

Sense Byte 15 indicates the amount of offset and direction used to perform a successful recovery from an uncorrectable data check while in logging mode. Recovery is accomplished without an ECC correctable data check.

Format 4, Sense Bytes 16-20 -- Not Used

Format 4, Sense Byte 21 -- Storage Director Physical Identifier

Sense Byte 21 is the storage director identifier that is assigned by the CE. This identifier appears in environmental, recording, and printing (EREP) reports to identify the storage director in use at the time of failure.

Format 4, Sense Bytes 22 and 23 -- Fault Symptom Code

The symptom code displayed is generated by the storage director from sense data.

FORMAT 5, SENSE BYTES 8 THROUGH 23 -- CORRECTABLE DATA CHECKS

Format 5 lists data checks with displacement information. Format 5 is generated when:

- ECC correctable data checks are detected in the data areas.
- ECC uncorrectable data checks occur which have been successfully retried but the system file mask indicates PCI (program controlled interrupt) fetch.
- Data checks are detected while processing the second or following records during a read multiple count, key, and data channel command word.

- Error log information is off-loaded after an ECC correctable error occurred during error logging. Byte 2, Bit 3 (environmental data present) is also set.

Format 5, Sense Bytes 8-12 -- Record Identification

Sense Bytes 8 through 12 contain the record identification (CCHHR) obtained from the count area of the record in which the error occurs (C-cylinder, H-head, R-record number).

Sense Byte 12, the record number from the count area, is set to zero if the error occurs in the Home Address area. This byte is unreliable after a space count.

Bytes 5 and 6 contain the physical address of the data. Bytes 8 through 12 contain the logical address assigned by the system for other than the Home Address area.

Format 5, Sense Byte 13 -- Sector Number

Sense Byte 13 contains the sector number of the record. This byte may not be valid if there is a count area data check.

Format 5, Sense Byte 14 -- Controller Physical Identifier

Sense Byte 14 contains the controller physical identifier in environmental recording, editing, and printing (EREP) reports.

Format 5, Sense Bytes 15, 16, and 17 -- With Sense Byte 2, Bit 3 On

When Sense Byte 2, Bit 3 is on, Sense Bytes 15, 16, and 17 contain environmental data.

Sense Byte 15, with Byte 2, Bit 3 on, reflects the amount of head offset used to recover from an initially uncorrectable data check while in logging mode. During retry, the data is read with an ECC correctable check. With the aid of the ECC corrections, the data is successfully read. The correction data and the original data is reported to the system.

Sense Byte 16, with Byte 2, Bit 3 on, reflects the storage director identifier (ID). The identifier indicates the storage director in use when the error occurred.

Sense Byte 17 is not used when Byte 2, Bit 3 is on.

Format 5, Sense Bytes 15, 16, and 17 -- With Sense Byte 2, Bit 3 Off

When sense Byte 2, Bit 3 is off, Bytes 15, 16, and 17 contain restart displacement information for the error recovery procedures.

Format 5, Sense Bytes 18 and 19 -- Error Displacement

Sense Bytes 18 and 19 specify the location of the first byte in error, within the data area, counting from the end of that data area.

Format 5, Sense Bytes 20-23 -- Error Pattern

Sense Bytes 20 through 23 identify which bits of a correctable data check are in error. A logical 1 represents an incorrect bit.

FORMAT 6, SENSE BYTES 8 THROUGH 23 -- USAGE/OVERRUN ERROR STATISTICS

Format 6 is generated by the storage director if:

- A Read and Reset Buffered Log command is issued by the operating system.
- The device usage statistics require off-loading because the counters in the storage director are full.

These counters are reset by powering off the SD.

The storage director maintains the following statistical data for each device:

- Access motions
- Bytes read and searched

Format 6, Sense Bytes 8-11 -- Bytes Read/Searched

Sense Bytes 8 through 11 provide an accumulated count of the number of bytes read from this device address in read or search operations. With the exception of bytes read during retry operation, all bytes read and checked for error are counted, including:

- Complete count of each Home Address or count area read
- Filler bytes used to extend a key or data area to a segment boundary
- Twelve check bytes for each area

Gaps between areas, defect skipping gaps, address marks, and sync bytes are excluded.

Format 6, Sense Bytes 12-15 -- Not Used

Format 6, Sense Bytes 16 and 17 -- Number of Motion Seeks

Sense Bytes 16 and 17 provide the number of access motions initiated by the channel to this device.

Format 6, Sense Bytes 18-20 -- Not Used

Format 6, Sense Byte 21 -- Storage Director Physical Identifier

Sense Byte 21 is the storage director identifier that is assigned by the CE. This identifier appears in environmental recording, editing, and printing (EREP) reports to identify the storage director in use at the time of failure.

Format 6, Sense Bytes 22 and 23 -- Not Used

FORMAT 7, SENSE BYTES 8 THROUGH 23 -- CONTROLLER CHECK-1

Format 7 lists controller and director-to-device interface equipment checks. Format 7 is generated when:

- A Check-1 error is detected within the controller logic

- The storage director-to-device controller interface fails inbound
- A timer in the storage director overflows while waiting for a response from the controller
- A control interface tag in sequence or a bus parity failure is detected by the storage director

Check-1 logic failures block normal controller communications with the storage director. Controller logic errors are collected in the connection check shift register and signaled to the storage director by a storage director-to-device controller interface connection check alert. The storage director gathers the failure data with a request connection check (RCC) sequence.

The storage director monitors the storage director-to-device controller (DDC) interface during the transfer of control signals and reports bus in and tag in errors. These errors are classed as controller errors and are reported in Format 7 sense data. Comparable errors in outbound storage director-to-device controller interface control or data signals are classed as storage director errors.

The storage director microcode times event durations.. If the controller exceeds the allotted amount of response time, a message is generated in Byte 7. The collected sequencer address in the sense data can point to the cause of the time out.

The controller saves the sequencer address whenever a Check-1 or Check-2 occurs, or when an RCC sequence is initiated. An RCC sequence collects this address and passes it to the storage director along with active controller checks.

Format 7, Sense Byte 8 -- DDC Bus Out - Command Code

Sense Byte 8 indicates the command code issued by the storage director and is used for messages 3, 8, and 9. This byte also contains the DDC bus out when the RCC sequence is executed.

Sense Byte 8 contains the last command issued by the storage director when tag out is activated. This byte may contain a previous command if the storage director detected an error after placing data on the bus.

Format 7, Sense Byte 9 -- DDC Bus In

Sense Byte 9 indicates the selection response received by the storage director. Byte 9 is used for message 5 and contains the DDC bus in bits when the RCC sequence is executed.

Format 7, Sense Byte 10 -- DTI and XES Register Contents

Sense Byte 10 reflects the contents of the storage director Device Tag In (DTI) and Transfer Error Status (XES) registers.

Format 7, Byte 10, Bit 0 -- Connection Check Alert

Bit 0 sets whenever any Check-1 error alert bit is set. This bit may be on for Format 7, but is always off for Format 8. This bit reflects Bit 0 of the DTI register.

Format 7, Byte 10, Bit 1 -- Tag In Check

Bit 1 sets when the storage director detects an invalid tag in sequence. This bit reflects Bit 1 of the DTI register.

Format 7, Byte 10, Bit 2 -- Sync In Check

If this bit is active, it should cause a Format 8 check.

Format 7, Byte 10, Bit 3 -- DDC Bus In Parity Check

Bit 3 sets if the storage director detects a bus in parity error. This bit reflects Bit 2 of the XES register.

Format 7, Byte 10, Bit 4 -- Null Disconnect

Bit 4 sets when tag in is in a null disconnect condition when the storage director detects an error. This bit reflects Bit 4 of the DTI register.

Format 7, Byte 10, Bit 5 -- Valid/Sync In

Bit 5 sets when tag in is in a valid/sync in condition when the storage director detects an error. This bit reflects Bit 5 of the DTI register.

Format 7, Byte 10, Bit 6 -- Selected Null

Bit 6 sets when tag in is in a selected null condition when the storage director detects an error. This bit reflects Bit 6 of the DTI register.

Format 7, Byte 10, Bit 7 -- End Operation

Bit 7 sets when tag in is in an end operation condition when the storage director detects an error. This bit reflects Bit 7 of the DTI register.

Format 7, Sense Byte 11 -- Controller Check Alert

Sense Byte 11 indicates which controller detected a connection check or have power on. This data is collected during an RCC sequence.

Format 7, Byte 11, Bit 0 -- Controller 0 CCA

Bit 0 is active if the connection check shift register of controller 0 had any Check-1 errors set.

Format 7, Byte 11, Bit 1 -- Controller 1 CCA

Bit 1 is active if the connection check shift register of controller 1 had any Check-1 errors set.

Format 7, Byte 11, Bit 2 -- Controller 0 DPSE Force Release

Bit 2 is active to indicate that the alternate controller of this string forced this controller to release a selected device. This status message is not an error indication, but a logged indication of the dynamic path selection extended (DPSE) activity.

Format 7, Byte 11, Bit 3 -- Controller 1 DPSE Force Release

Bit 3 is active to indicate that the alternate controller of this string forced this controller to release a selected device. This status message is not an error indication, but a logged indication of the dynamic path selection extended (DPSE) activity.

Format 7, Byte 11, Bit 4 -- Controller 0 Power On

Bit 4 is active to indicate that this controller has power and can provide valid RCC data. If this bit is not active, it indicates that either the RCC was not successfully performed or that the controller does not have power.

Format 7, Byte 11, Bit 5 -- Controller 1 Power On

Bit 5 is active to indicate that this controller has power and can provide valid RCC data. If this bit is not active, it indicates that either the RCC was not successfully performed or that the controller does not have power.

Format 7, Byte 11, Bits 6 and 7 -- Not Used

Format 7, Sense Byte 12 - Controller 0 Check-1 (CCA)

Sense Byte 12 contains part of the controller 0 Check-1 conditions that are active when the storage director receives a connection check alert (CCA). This data is collected during an RCC sequence. Byte 12 is equivalent to Byte 14.

Format 7, Byte 12, Bits 0-2 -- Check-1 Isolation Bits

Bits 0, 1, and 2 are multiplexed to indicate the type of error detected on the input/output control 1 board.

Bits 0	1	2	
0	0	0	No error present
0	0	1	Parity error detected on Input Data bus on sequencer I board
0	1	0	Parity error detected in Pipeline B instructional fields decoded to enable an input or output port on the sequencer II board
0	1	1	Not used
1	0	0	Parity error detected in Pipeline A instruction on sequencer I board

Bits 0	1	2	
1	0	1	Not used
1	1	0	Parity error detected in Data Output bus either as Tag In is sent to the DDC interface, or as a transceiver gating signal is enabled on the sequencer II board
1	1	1	Not used

Format 7, Byte 12, Bit 3 -- DDC Bus Out Parity Check

Bit 3 sets when a parity error is detected on the DDC Byte 0 bus while a command or command modifier is present.

Format 7, Byte 12, Bit 4 -- Controller Clock Check

Bit 4 sets when extra system clock signals (A through H) occur.

Format 7, Byte 12, Bit 5 -- Controller Sequencer Check-1

Bit 5 sets when a pipeline B parity error is detected on the sequencer 1 board.

Format 7, Byte 12, Bit 6 -- DDC Bus In Parity Check-1

Bit 6 sets when a parity check occurs on the DDC Byte 1 bus from the Data Output bus on the sequencer II board. This bit is also set by gating the wrong bus to the DDC Byte 1 bus during a read operation.

Format 7, Byte 12, Bit 7 -- Not Used

Format 7, Sense Byte 13 -- Controller 0 Check-1 (CCA)

Byte 13 contains part of the controller 0 Check-1 conditions that are active when the storage director receives a connection check alert (CCA). This data is collected during an RCC sequence. Byte 13 is equivalent to Byte 15.

Format 7, Byte 13, Bit 0 -- DDC Tag Out Sequence Check

Bit 0 sets when the controller detects an invalid tag out sequence change from the storage director. The controller detects multiple changes in the tag out lines without an intermediate tag in change.

Format 7, Byte 13, Bit 1 -- Oriented Tag Sequence Check-1

Bit 1 sets on an extended command with a change on the tag out lines into an invalid sequence state. The following tags set the check:

Bits 0	1	2	
0	0	0	null
1	0	0	poll
1	1	0	hardware immediate

Format 7, Byte 13, Bit 2 -- Sequencer Detected Check-1

Bit 2 is set by the controller sequencer microcode when a Check-1 error is detected in software. The address returned during the RCC sequence identifies the source of the error (usually an invalid Tag Out state).

Format 7, Byte 13, Bit 3 -- DDC Float Check

Bit 3 sets if DDC Byte 0 or Byte 1 bus is not being driven in the right direction by the controller during a control operation. The controller should be driving Byte 1 and not driving Byte 0.

Format 7, Byte 13, Bit 4 -- RCC Clock Check

Bit 4 sets if the RCC clocks decoded from the DDC Byte 0 bus overlap, or if a bit in the Check-1 log is still active after an RCC tag sequence ends.

Format 7, Byte 13, Bits 5-7-- Not Used

Format 7, Sense Byte 14 -- Controller 1 Check-1 (CCA)

Byte 14 contains part of the controller 1 Check-1 conditions that are active when the storage director receives a connection check alert (CCA). This data is collected during an RCC sequence. Byte 14 is equivalent to Byte 12.

Format 7, Byte 14, Bits 0-2 -- Check-1 Isolation Bits

Bits 0, 1, and 2 are multiplexed to indicate the type of error detected on the input/output control 1 board.

Bits 0	1	2	
0	0	0	No error present
0	0	1	Parity error detected on Input Data bus on sequencer I board
0	1	0	Parity error detected in Pipeline B instructional fields decoded to enable an input or output port on the sequencer II board
0	1	1	Not used
1	0	0	Parity error detected in Pipeline A instruction on sequencer I board
1	0	1	Not used
1	1	0	Parity error detected in Data Output bus either as Tag In is sent to the DDC interface, or as a transceiver gating signal is enabled on the sequencer II board
1	1	1	Not used

Format 7, Byte 14, Bit 3 -- DDC Bus Out Parity Check

Bit 3 sets when a parity error is detected on the DDC Byte 0 bus while a command or command modifier is present.

Format 7, Byte 14, Bit 4 -- Controller Clock Check

Bit 4 sets when extra system clock signals (A through H) occur.

Format 7, Byte 14, Bit 5 -- Controller Sequencer Check-1

Bit 5 sets when a pipeline B parity error is detected on the sequencer 1 board.

Format 7, Byte 14, Bit 6 -- DDC Bus In Parity Check

Bit 6 sets when a parity check occurs on the DDC Byte 1 bus from the Data Output bus on the sequencer II board. This bit is also set by gating the wrong bus to the DDC Byte 1 bus during a read operation.

Format 7, Byte 14, Bit 7 -- Not Used

Format 7, Sense Byte 15 -- Controller 1 Check-1 (CCA)

Byte 15 contains part of the controller 1 Check-1 conditions that are active when the storage director receives a connection check alert (CCA). This data is collected during an RCC sequence. Byte 15 is equivalent to Byte 13.

Format 7, Byte 15, Bit 0 -- DDC Tag Out Sequence Check

Bit 0 sets when the controller detects an invalid tag out sequence change from the storage director. The controller detects multiple changes in the tag out lines without an intermediate tag in change.

Format 7, Byte 15, Bit 1 -- Oriented Tag Sequence Check-1

Bit 1 sets on an extended command with a change on the tag out lines into an invalid sequence state. The following tags set the check:

Bit 0	Bit 1	Bit 2	
0	0	0	null
1	0	0	poll
1	1	0	hardware immediate

Format 7, Byte 15, Bit 2 -- Sequencer Detected Check-1

Bit 2 is set by the controller sequencer microcode when a Check-1 error is detected in software. The address returned during the RCC sequence identifies the source of the error (usually an invalid Tag Out state).

Format 7, Byte 15, Bit 3 -- DDC Float Check

Bit 3 sets if DDC Byte 0 or Byte 1 bus is not being driven in the right direction by the controller during a control operation. The controller should be driving Byte 1 and not driving Byte 0.

Format 7, Byte 15, Bit 4 -- RCC Clock Check

Bit 4 sets if the RCC clocks decoded from the DDC Byte 0 bus overlap, or if a bit in the Check-1 log is still active after an RCC tag sequence ends.

Format 7, Byte 15, Bits 5-7 -- Not Used

Format 7, Sense Bytes 16 and 17 -- Controller 0 Sequencer Address and Status

Bytes 16 and 17 contain twelve sequencer address bits (0-11) and four status bits (Byte 17, Bits 4-7).

The sequencer address is saved at the time a Check-1 error is detected. If a Check-2 error occurs but no Check-1, these bits contain the sequencer address when the Check-2 error occurred.

Format 7, Byte 17, Bit 4 -- Power On Complete

Bit 4 sets when all device power up sequencing is complete.

Format 7, Byte 17, Bit 5 -- Check-2 Active

Bit 5 sets if any Check-2 error has been detected. This bit is cleared by a Check-1 or Check-2 reset.

Format 7, Byte 17, Bit 6 -- Successful Data Transfer

Bit 6 is set and sent to the SD to ensure the validity of the RCC data.

Format 7, Byte 17, Bit 7 -- Upper Memory Enabled

Bit 7 indicates whether sequencer execution was in functional memory (0) or diagnostic memory (1). This bit is, in effect, a 13th sequencer address bit.

Format 7, Sense Bytes 18 and 19 -- Controller 1 Sequence Address and Status

Bytes 18 and 19 contain twelve sequencer address bits (0-11) and four status bits (Byte 18, Bits 4-7).

The sequencer address is saved at the time a Check-1 error is detected. If a Check-2 error occurs but no Check-1, these bits contain the sequencer address when the Check-2 error occurred.

Format 7, Byte 19, Bit 4 -- Power On Complete

Bit 4 sets when all device power up sequencing is complete.

Format 7, Byte 19, Bit 5 -- Check-2 Active

Bit 5 sets if any Check-2 error has been detected. This bit is cleared by a Check-1 or Check-2 reset.

Format 7, Byte 19, Bit 6 -- Successful Data Transfer

Bit 6 is set and sent to the SD to ensure the validity of the RCC data.

Format 7, Byte 19, Bit 7 -- Upper Memory Enabled

Bit 7 indicates whether sequencer execution was in functional memory (0) or diagnostic memory (1). This bit is, in effect, a 13th sequencer address bit.

Format 7, Sense Byte 20 -- Byte 7 Data - For Message C

If the storage director cannot communicate with the controller because of message C conditions, Byte 20 will contain Byte 7 of the initial error data.

Format 7, Sense Byte 21 -- Storage Director Physical Identifier

Sense Byte 21 is the storage director identifier that is assigned by the CE. This identifier appears in environmental recording, editing, and printing (EREP) reports to identify the storage director in use at the time of the error.

Format 7, Sense Bytes 22 and 23 -- Fault Symptom Code

The symptom code displayed is generated by the storage director from sense data.

FORMAT 8, SENSE BYTES 8 THROUGH 23 -- CONTROLLER EQUIPMENT CHECKS

Format 8 is generated when a storage director detects controller Check-2 or device Check-1 equipment failures. Controller Check-2 conditions do not prevent selection, normal communications by the director-to-device controller, or operation of the controller sequencer. Controller Check-2 and device Check-1 equipment conditions are reported to the storage director by normal director-to-device controller end operation codes.

If the controller has a fault that causes it to disconnect from the device while selected, there will be an uncollected device Check-1 in the device at its next selection. On a dynamic path selection string, this next selection may be from another CPU and a different ERDS. With this alternate path selection, the device will report an error, which will be recoverable at the first retry, yet will be logged on the other system ERDS. While this error is of lower priority than the primary error, it appears in the combined EREP reports.

Format 8, Sense Byte 8 -- DDC Bus Out

Sense Byte 8 can contain the command or command modifier issued by the storage director at the time of failure.

Format 8, Sense Byte 9 -- DDC Bus In (End Operation Code)

Sense Byte 9 contains the end operation code if Byte 10, Bit 7 is on, or if the Byte 7 message is 3, 4, or 5.

These checks are all Format 8 errors. The controller collects sense bytes and standard error recovery procedure (ERP) equipment check procedures are followed.

00 No check and successful completion of the preceding command.

01 DDC command overrun -- This code sets when the controller indicates to the storage director that while the controller was oriented, the command did not arrive on time. The storage director then retries the operation up to two times. If this code repeats, the storage director collects Format 8 sense data.

02 Sync byte missing but data found -- This code sets when the controller indicates to the storage director that the expected sync byte is not found. The storage director retries the operation using data check recovery procedures and reports failures in Format 4, Sense Byte 7, error message to identify the area with a missing sync byte.

03 Data check -- This code sets when the controller detects a data check. Errors are reported in Formats 4 or 5. The end operation code does not appear in the sense bytes.

06 Invalid command code -- This code sets when the controller detects an invalid command code. The storage director reports a Format 8 equipment check and performs ERP equipment check recovery procedures.

07 Not used

08 HAR modifier overrun on set HAR oriented -- This code sets when the controller detects this overrun condition. The storage director reports a Format 8 equipment check and performs ERP equipment check recovery procedures.

09 No selection response from device -- This code sets when the controller-to-device port (CDP) tag valid is not received on device selection by the controller.

10 Check-2 detected within the controller or Check-1 detected in the drive logic -- This code sets when a Check-2 condition is detected within the controller or when a Check-1 is detected in the CDP or device logic. Check conditions are detected by the controller hardware or the microcode. If the storage director receives 10 as the end operation code, the storage director collects the controller fault log bytes, and reports the assembled bytes in Format 8.

11 Device Check-1 on selection -- This code sets when the controller detects a device Check-1 condition, whether or not the device on the active port is selected or unselected. A Format 8 error message is assembled and reported, and the failing operation is retried.

13 CDP hung due to late or missing device response -- This code sets when the controller did not receive a device response within the correct time after device selection on an immediate command or command modifier.

14 Precompensation failure, set or reset -- This code sets when an attempt to set or reset the controller precompensation circuits fails.

15 Not used

16 Not used

17 Not used

18 Not used

19 Device dropped to null -- This code sets when the controller detects that the CDP device tag in is at null instead of tag valid, or end operation.

1A Device pad in progress on erroneously -- This code sets when the controller finds the device pad bit on instead of off at the end of the write sequence.

1B Index found during defect skip in Home Address area -- This code sets when the controller finds the index bit on while performing a defect skip in the Home Address area.

20 Device check active -- The storage director assembles the Format 1 sense bytes when device check is active. This check is a Format 1 error. The device sense bytes are collected and ERP equipment check procedures are performed.

Format 8, Sense Byte 10 -- DTI and XES Register Contents

Byte 10 reflects the contents of the storage director device tag in (DTI) and transfer error status (XES) registers.

Format 8, Byte 10, Bit 0 -- Connection Check Alert

Bit 0 indicates a connection check alert. This bit may be on for Format 7, but is always off for Format 8. This bit reflects Bit 0 of the DTI register.

Format 8, Byte 10, Bit 1 -- Tag In Check

Bit 1 sets when the storage director detects an invalid tag in sequence. This bit reflects Bit 1 of the DTI register.

Format 8, Byte 10, Bit 2 -- Sync In Check

Bit 2 sets when the storage director detects too many or not enough sync in tags during data transfer operations. This bit reflects Bit 5 of the XES register.

Format 8, Byte 10, Bit 3 -- DDC Bus In Parity Check

Bit 3 sets if the storage director detects a bus in parity error. This bit reflects Bit 2 of the XES register.

Format 8, Byte 10, Bit 4 -- Null/Disconnect

Bit 4 sets when tag in is in a null/disconnect condition when the storage director detects an error. This bit reflects Bit 4 of the DTI register.

Format 8, Byte 10, Bit 5 -- Valid/Sync In

Bit 5 sets when tag in is in a valid/sync in condition when the storage director detects an error. This bit reflects Bit 5 of the DTI register.

Format 8, Byte 10, Bit 6 -- Selected Null

Bit 6 sets when tag in is in a selected null condition when the storage director detects an error. This bit reflects Bit 6 of the DTI register.

Format 8, Byte 10, Bit 7 -- End Operation

Bit 7 sets when tag in is in an end operation condition when the storage director detects an error. This bit reflects Bit 7 of the DTI register.

Format 8, Sense Byte 11 -- Fault Log Byte A

Sense Byte 11 contains Check-2 error summary information.

Format 8, Byte 11, Bit 0 -- SERDES Error

Bit 0 sets if there is a parity check in SERDES input bus or a control check in SERDES LSI chip.

Format 8, Byte 11, Bit 1 -- CODEC Wrap Error

Bit 1 sets during a write operation when the data is encoded and decoded, then compared with the original unencoded data to test the CODEC.

Format 8, Byte 11, Bit 2 -- Software-Check-2

Bit 2 sets if the microcode detects a noncritical error.

Format 8, Byte 11, Bit 3 -- Missing Servo Check

Bit 3 sets if servo clock is missing from selected device while Lock to Servo is active.

Format 8, Byte 11, Bit 4 -- CDP Input Bus Parity Check

Bit 4 sets if a parity error is detected on the internal CDP data input bus while Device Drivers Active is on.

Format 8, Byte 11, Bit 5 -- Power Interrupt

Bit 5 sets when the power supply is being interrupted, but will be active for at least another 40 milliseconds at full load.

Format 8,Byte 11, Bit 6 -- Internal CDP Tag or Data Out Register Parity

Bit 6 sets if a parity error is detected on the data output bus or on the tag out bus registers on the CDP board.

Format 8, Byte 11, Bit 7 -- Power Supply Tolerance Check

Bit 7 sets when dc power supply voltages are not within allowable tolerances.

Format 8, Sense Byte 12 -- Fault Log Byte B

Sense Byte 12 contains Check-2 error summary information.

Format 8, Byte 12, Bit 0 -- Write Control Check

Bit 0 sets when the write control lines have illegal combinations of signals.

Format 8, Byte 12, Bit 1 -- Not Used

Format 8, Byte 12, Bit 2 -- DDC Write OP Parity Check

Bit 2 sets if a parity error is detected on the DDC interface while transferring data during a write operation.

Format 8, Byte 12, Bit 3 -- DDC Bus In Parity Check

Bit 3 sets if a parity error is detected on DDC bus in Byte 0 or 1 on the sequencer II board during a read operation.

Format 8, Byte 12, Bits 4 and 5 -- Port Select Bits 0 and 1

These two bits, along with Bits 6 and 7 of Byte 14, indicate the port address of the selected device at the time of the check. The four bits form a 4-bit binary port address.

Format 8, Byte 12, Bit 6 -- Not Used

Format 8, Byte 12, Bit 7 -- CDP Port Check-1

Bit 7 sets when the selected port returns a Check-1 error.

Format 8, Sense Byte 13 -- Fault Log Byte C

Sense Byte 13 contains Check-2 error summary information.

Format 8, Byte 13, Bit 0 -- ECC Bus Parity Check

Bit 0 sets if a parity error is detected on the ECC bus, Bytes 0 and 1.

Format 8, Byte 13, Bit 1 -- CDP Bidir Data Parity Check

Bit 1 sets if a parity error is detected on the bidirectional data lines from CDP 4 board to CDP 12 board.

Format 8, Byte 13, Bit 2 -- Sync In/Sync Out Error

Bit 2 sets if a failure is detected in the Sync In/Sync Out handshaking sequence.

Format 8, Byte 13, Bit 3 -- CDP 12 Data Output Parity Error

Bit 3 sets if a parity error is detected on the data output bus of sequencer I board.

Format 8, Byte 13, Bits 4 and 5 -- String Configuration

Bits 4 and 5 indicate the number of B units in the string.

	Bit 4	Bit 5
1 B unit installed	0	0
2 B units installed	0	1
3 B units installed	1	0
4 B units installed	1	1

Format 8, Byte 13, Bit 6 -- CDP 12 Path Busy Parity Error

Bit 6 sets if a parity error is detected on the DPSE lock bus from the DPSE board to CDP 12 board.

Format 8, Byte 13, Bit 7 -- CDP Data Lock Parity Check

Bit 7 sets if a parity error is detected on the DPSE lock bus from the DPSE board to CDP 4 board.

Format 8, Sense Byte 14 -- Fault Log Byte D

Sense Byte 14 contains device Check-1 conditions.

Format 8, Byte 14, Bits 0-3 -- Device Check-1

Each device on the port reports any active Check-1 errors over the assigned CDP bus in bit line when gated by a gate checks signal from the controller.

The port in use when a Sense Error Log command is issued by the storage director is indicated by the binary decode of Bits 6 and 7. See Bits 6 and 7 for a description of the ports in use when a Sense Error Log command is issued. Only one bit can be set if in 16-port configuration.

Format 8, Byte 14, Bit 4 -- Device Clock Check

Bit 4 sets if the selected device indicates a problem with the multiphase clock.

Format 8, Byte 14, Bit 5 -- Isolation Bit

Bit 5 sets if a device Select Check or Clock Check is detected.

Format 8, Byte 14, Bits 6 and 7 -- Port Select Bits 2 and 3

These two bits, along with Bits 4 and 5 of Byte 12, indicate the port address of the selected device at the time of the check. The four bits form a 4-bit binary port address.

Format 8, Sense Byte 15 -- Fault Log Byte E

Sense Byte 15 contains the dynamic path selection extended (DPSE) function error latches.

Format 8, Byte 15, Bit 0 -- DPSE Memory Parity Error

Bit 0 sets if a parity error is detected on DPSE Memory Data bus during a DPSE Write operation.

Format 8, Byte 15, Bit 1 -- DPSE Data Bus Parity Error

Bit 1 sets if a parity error is detected on data out bus and if there are multiple drivers on data out bus.

Format 8, Byte 15, Bit 2 -- DPSE Memory Compare Error

Bit 2 sets if the data read from alternate controller's memory does not compare with data read from current controller's memory.

Format 8, Byte 15, Bit 3 -- DPSE Alternate Controller Parity Error

Bit 3 sets if alternate controller detects a parity error in its memory address or memory data.

Format 8, Byte 15, Bit 4 -- DPSE Address Parity Error

Bit 4 sets if parity on DPSE memory address bus does not compare with expected parity.

Format 8, Byte 15, Bit 5 -- Not Used

Format 8, Byte 15, Bit 6 -- DPSE Lock Bus Parity Error

Bit 6 sets if a parity error occurs on the DPSE lock bus data coming from the alternate controller.

Format 8, Byte 15, Bit 7 -- Not Used

Format 8, Sense Bytes 16 and 17 -- Selected Controller Sequencer Address and Status

Bytes 16 and 17 contain twelve sequencer address bits (0-11) and four status bits (Byte 17, Bits 4-7). The address is the selected controller sequencer address that is trapped with the setting of any controller Check-2. If this selected controller sequencer address is not already trapped, the address is trapped during a request connection check (RCC) sequence. (Addresses are collected during an RCC sequence.)

If Bit 5 (Check-2) is active, it indicates that one or more Check-2 conditions cannot be reset by a sense error log command or an RCC sequence.

Format 8, Byte 17, Bit 4 -- Power On Complete

Bit 4 sets when all device power up sequencing is complete.

Format 8, Byte 17, Bit 5 -- Check-2 Active

Bit 5 sets if any Check-2 error has been detected. This bit is cleared by a Check-1 or Check-2 reset.

Format 8, Byte 17, Bit 6 -- Successful Data Transfer

Bit 6 is set and sent to the SD to ensure the validity of the RCC data.

Format 8, Byte 17, Bit 7 -- Upper Memory Enabled

Bit 7 indicates whether sequencer execution was in functional memory (0) or diagnostic memory (1). This bit is, in effect, a 13^{th} sequencer address bit.

Format 8, Sense Byte 18 -- Fault Log Byte F

Sense Byte 18 contains Check-2 error summary information.

Format 8, Byte 18, Bit 0 -- R/W BusOut Parity Check

Bit 0 sets if a parity error is detected on R/W bus Bytes 0/1 when DDC data is gated onto the bus.

Format 8, Byte 18, Bit 1 -- ALU Output Parity Error

Bit 1 sets if a parity error is detected on R/W bus Bytes 0/1 when the ALU output is gated onto the bus.

Format 8, Byte 18, Bit 2 -- Reference Data Parity Error

Bit 2 sets if a parity error is detected on R/W bus Bytes 0/1 when pipeline A data is gated onto the bus.

Format 8, Byte 18, Bit 3 -- Read Parity Check

Bit 3 sets if a parity error is detected on R/W bus Bytes 0/1 when SERDES read data is gated onto the bus.

Format 8, Byte 18, Bit 4 -- Delta Frequency Check

Bit 4 sets if the PLO tries to lock to a frequency that is too far from the nominal frequency.

Format 8, Byte 18, Bits 5-7 -- Not Used

Format 8, Sense Byte 19 -- Device Status I

Byte 19 indicates the status of functional operations being performed.

Format 8, Byte 19, Bit 0 -- Pad In Progress

Bit 0 sets when the selected device read/write path is write-padding and not available.

Format 8, Byte 19, Bit 1 -- Servo Inhibited

Bit 1 sets when the servo system is not track following and loses all orientation. Recovery is attempted by executing a Rezero command.

Format 8, Byte 19, Bit 2 -- Seek Incomplete

Bit 2 sets when the device sequencer times out on a seek operation. The device sequencer times and checks each seek operation. An interrupt (Bit 7) is set on timeout and remains set until reset by a successful rezero operation. Bit 7 is also active if the device must signal an interrupt.

Format 8, Byte 19, Bit 3 -- Device Check-2 or Set Sector Incomplete

Bit 3 sets when the device sequencer times out on a set sector operation. The set sector operation is part of the locate record, locate cylinder and record, and offset cylinder and record commands. The device sequencer times and checks each set sector. An interrupt is issued on timeout. This bit remains

active until reset by the storage director. Bit 7 is also active. Check-2 is defined as any bit active in the Check register (Byte 11).

Format 8, Byte 19, Bit 4 -- On Line

Bit 4 is set by the device sequencer logic when the device power-on sequence is successfully completed and the device is ready to resume normal operations. This bit remains active until the logic power or the motor switch is turned off. A device that is not On Line indicates Device Busy in device status 1 (Byte 19) or Spindle Off in device status 2 (Byte 20).

Format 8, Byte 19, Bit 5 -- HDA Attention

Bit 5 sets when the device sequencer starts an HDA attention interrupt at the completion of the device power-on sequence.

Format 8, Byte 19, Bit 6 -- Device Busy

Bit 6 is set by the device sequencer during any of the following operations:

- Locate
- Offset
- Rezero
- Pad in progress
- Search sector
- Power on or power off

The device sequencer resets device busy at completion of the operation or when a clock timeout occurs. During the search sector operation, the device busy bit remains active until the desired sector is found. Device busy can be active with an outstanding interrupt that has not been serviced. Device busy indicates that the device is not ready (during power-on or power-off sequence for HDA or logic) with Bit 4 off (not On Line). Sense Byte 0, Bit 1 (Intervention Required) is active if a device is selected that is not ready.

Format 8, Byte 19, Bit 7 -- Seek or Set Sector Interrupt or Sector Search

Bit 7 is set by the device sequencer during these conditions:

- A successful or unsuccessful completion of a locate, offset, or rezero command. The device must signal an interrupt.
- A locate or offset command is in progress. The locate interrupt bit is set during the locate record portion of these commands.
- A pad complete is being executed in either device. The device must signal an interrupt.
- The busy-to-not-busy transition is in progress and the device is selected while busy.
- The HDA attention is in progress.

For each of these commands from a storage director, an interrupt must be returned to that storage director to indicate successful or unsuccessful completion of the command.

- Locate record command
- Locate cylinder command (when the cylinder difference is not zero)
- Locate cylinder and record command
- Start rezero command
- Offset cylinder command
- Offset cylinder and record command

If another device on the same read/write path is padding, the locate, offset, or rezero complete interrupt is not presented until the padding is complete.

When a storage director selects a busy device, the interrupt is returned when the device is no longer busy.

When a storage director requires an HDA interrupt during the device power-on sequence, the interrupt is presented at the completion of the power-on sequence. The reset interrupt command resets any interrupt or pending interrupt except a pending

HDA attention interrupt. The check reset command resets any interrupt or pending interrupt except a pending or active HDA attention interrupt.

Format 8, Sense Byte 20 -- Device Status 2

Sense Byte 20 indicates the status of hardware under various operating conditions.

Format 8, Byte 20, Bit 0 -- Device Logic Disabled

Bit 0 active indicates a device logic switch is in the disabled position.

Format 8, Byte 20, Bit 1 -- Surge Complete

Bit 1 on indicates early completion of the motor start current surge (within nine seconds after HDA power on). This bit is used only by the controller or CE diagnostic programs.

Format 8, Byte 20, Bit 2 -- Offset Active

Bit 2 on indicates the servo circuits are being operated with offset active. The device sequencer resets this bit when an offset operation is performed with a zero value in the Difference counter or a rezero command.

Format 8, Byte 20, Bit 3 -- Drive Motor Switch

Bit 3 on indicates the motor switch is turned off. Sense Byte 0, Bit 1 (Intervention Required) is set when a device is selected with device power off.

Format 8, Byte 20, Bits 4 and 5 -- Not Used

Format 8, Byte 20, Bit 6 -- Left Access Mechanism Selected

Bit 6 on indicates the odd address device is selected (odd address matrix board).

Format 8, Byte 20, Bit 7 -- Right Access Mechanism Selected

Bit 7 on indicates the even address device is selected (even address matrix board).

Format 8, Sense Byte 21 -- Storage Director Physical Identifier

Sense Byte 21 is the storage director identifier that is assigned by the CE. This identifier appears in environmental recording, editing, and printing (EREP) reports to identify the storage director in use at the time of the error.

Format 8, Sense Bytes 22 and 23 -- Fault Symptom Code

The symptom code displayed is generated by the storage director from sense data.

SECTION 1D

REFERENCE MATERIAL

DECIMAL-TO-HEXADECIMAL CONVERSION

Table 1D-1 contains decimal numbers 000 through 999 and their hexadecimal equivalents. These may be useful when entering parameters such as cylinder and head addresses and other times when cylinder conversion is required.

TABLE 1D-1. DECIMAL-TO-HEXADECIMAL CONVERSION

Dec	Hex	Dec	Hex	Dec	Hex	Dec	Hex	Dec	Hex
000	000	040	028	080	050	120	078	160	0A0
001	001	041	029	081	051	121	079	161	0A1
002	002	042	02A	082	052	122	07A	162	0A2
003	003	043	02B	083	053	123	07B	163	0A3
004	004	044	02C	084	054	124	07C	164	0A4
005	005	045	02D	085	055	125	07D	165	0A5
006	006	046	02E	086	056	126	07E	166	0A6
007	007	047	02F	087	057	127	07F	167	0A7
008	008	048	030	088	058	128	080	168	0A8
009	009	049	031	089	059	129	081	169	0A9
010	00A	050	032	090	05A	130	082	170	0AA
011	00B	051	033	091	05B	131	083	171	0AB
012	00C	052	034	092	05C	132	084	172	0AC
013	00D	053	035	093	05D	133	085	173	0AD
014	00E	054	036	094	05E	134	086	174	0AE
015	00F	055	037	095	05F	135	087	175	0AF
016	010	056	038	096	060	136	088	176	0B0
017	011	057	039	097	061	137	089	177	0B1
018	012	058	03A	098	062	138	08A	178	0B2
019	013	059	03B	099	063	139	08B	179	0B3
020	014	060	03C	100	064	140	08C	180	0B4
021	015	061	03D	101	065	141	08D	181	0B5
022	016	062	03E	102	066	142	08E	182	0B6
023	017	063	03F	103	067	143	08F	183	0B7
024	018	064	040	104	068	144	090	184	0B8
025	019	065	041	105	069	145	091	185	0B9
026	01A	066	042	106	06A	146	092	186	0BA
027	01B	067	043	107	06B	147	093	187	0BB
028	01C	068	044	108	06C	148	094	188	0BC
029	01D	069	045	109	06D	149	095	189	0BD
030	01E	070	046	110	06E	150	096	190	0BE
031	01F	071	047	111	06F	151	097	191	0BF
032	020	072	048	112	070	152	098	192	0C0
033	021	073	049	113	071	153	099	193	0C1
034	022	074	04A	114	072	154	09A	194	0C2
035	023	075	04B	115	073	155	09B	195	0C3
036	024	076	04C	116	074	156	09C	196	0C4
037	025	077	04D	117	075	157	09D	197	0C5
038	026	078	04E	118	076	158	09E	198	0C6
039	027	079	04F	119	077	159	09F	199	0C7

Table Continued on Next Page

TABLE 1D-1. DECIMAL-TO-HEXADECIMAL CONVERSION (Contd)

Dec	Hex	Dec	Hex	Dec	Hex	Dec	Hex	Dec	Hex
200	0C8	240	0F0	280	118	320	140	360	168
201	0C9	241	0F1	281	119	321	141	361	169
202	0CA	242	0F2	282	11A	322	142	362	16A
203	0CB	243	0F3	283	11B	323	143	363	16B
204	0CC	244	0F4	284	11C	324	144	364	16C
205	0CD	245	0F5	285	11D	325	145	365	16D
206	0CE	246	0F6	286	11E	326	146	366	16E
207	0CF	247	0F7	287	11F	327	147	367	16F
208	0D0	248	0F8	288	120	328	148	368	170
209	0D1	249	0F9	289	121	329	149	369	171
210	0D2	250	0FA	290	122	330	14A	370	172
211	0D3	251	0FB	291	123	331	14B	371	173
212	0D4	252	0FC	292	124	332	14C	372	174
213	0D5	253	0FD	293	125	333	14D	373	175
214	0D6	254	0FE	294	126	334	14E	374	176
215	0D7	255	0FF	295	127	335	14F	375	177
216	0D8	256	100	296	128	336	150	376	178
217	0D9	257	101	297	129	337	151	377	179
218	0DA	258	102	298	12A	338	152	378	17A
219	0DB	259	103	299	12B	339	153	379	17B
220	0DC	260	104	300	12C	340	154	380	17C
221	0DD	261	105	301	12D	341	155	381	17D
222	0DE	262	106	302	12E	342	156	382	17E
223	0DF	263	107	303	12F	343	157	383	17F
224	0E0	264	108	304	130	344	158	384	180
225	0E1	265	109	305	131	345	159	385	181
226	0E2	266	10A	306	132	346	15A	386	182
227	0E3	267	10B	307	133	347	15B	387	183
228	0E4	268	10C	308	134	348	15C	388	184
229	0E5	269	10D	309	135	349	15D	389	185
230	0E6	270	10E	310	136	350	15E	390	186
231	0E7	271	10F	311	137	351	15F	391	187
232	0E8	272	110	312	138	352	160	392	188
233	0E9	273	111	313	139	353	161	393	189
234	0EA	274	112	314	13A	354	162	394	18A
235	0EB	275	113	315	13B	355	163	395	18B
236	0EC	276	114	316	13C	356	164	396	18C
237	0ED	277	115	317	13D	357	165	397	18D
238	0EE	278	116	318	13E	358	166	398	18E
239	0EF	279	117	319	13F	359	167	399	18F

Table Continued on Next Page

TABLE 1D-1. DECIMAL-TO-HEXADECIMAL CONVERSION (Contd)

Dec	Hex	Dec	Hex	Dec	Hex	Dec	Hex	Dec	Hex
400	190	440	1B8	480	1E0	520	208	560	230
401	191	441	1B9	481	1E1	521	209	561	231
402	192	442	1BA	482	1E2	522	20A	562	232
403	193	443	1BB	483	1E3	523	20B	563	233
404	194	444	1BC	484	1E4	524	20C	564	234
405	195	445	1BD	485	1E5	525	20D	565	235
406	196	446	1BE	486	1E6	526	20E	566	236
407	197	447	1BF	487	1E7	527	20F	567	237
408	198	448	1C0	488	1E8	528	210	568	238
409	199	449	1C1	489	1E9	529	211	569	239
410	19A	450	1C2	490	1EA	530	212	570	23A
411	19B	451	1C3	491	1EB	531	213	571	23B
412	19C	452	1C4	492	1EC	532	214	572	23C
413	19D	453	1C5	493	1ED	533	215	573	23D
414	19E	454	1C6	494	1EE	534	216	574	23E
415	19F	455	1C7	495	1EF	535	217	575	23F
416	1A0	456	1C8	496	1F0	536	218	576	240
417	1A1	457	1C9	497	1F1	537	219	577	241
418	1A2	458	1CA	498	1F2	538	21A	578	242
419	1A3	459	1CB	499	1F3	539	21B	579	243
420	1A4	460	1CC	500	1F4	540	21C	580	244
421	1A5	461	1CD	501	1F5	541	21D	581	245
422	1A6	462	1CE	502	1F6	542	21E	582	246
423	1A7	463	1CF	503	1F7	543	21F	583	247
424	1A8	464	1D0	504	1F8	544	220	584	248
425	1A9	465	1D1	505	1F9	545	221	585	249
426	1AA	466	1D2	506	1FA	546	222	586	24A
427	1AB	467	1D3	507	1FB	547	223	587	24B
428	1AC	468	1D4	508	1FC	548	224	588	24C
429	1AD	469	1D5	509	1FD	549	225	589	24D
430	1AE	470	1D6	510	1FE	550	226	590	24E
431	1AF	471	1D7	511	1FF	551	227	591	24F
432	1B0	472	1D8	512	200	552	228	592	250
433	1B1	473	1D9	513	201	553	229	593	251
434	1B2	474	1DA	514	202	554	22A	594	252
435	1B3	475	1DB	515	203	555	22B	595	253
436	1B4	476	1DC	516	204	556	22C	596	254
437	1B5	477	1DD	517	205	557	22D	597	255
438	1B6	478	1DE	518	206	558	22E	598	256
439	1B7	479	1DF	519	207	559	22F	599	257

Table Continued on Next Page

TABLE 1D-1. DECIMAL-TO-HEXADECIMAL CONVERSION (Contd)

Dec	Hex	Dec	Hex	Dec	Hex	Dec	Hex	Dec	Hex
600	258	640	280	680	2A8	720	2D0	760	2F8
601	259	641	281	681	2A9	721	2D1	761	2F9
602	25A	642	282	682	2AA	722	2D2	762	2FA
603	25B	643	283	683	2AB	723	2D3	763	2FB
604	25C	644	284	684	2AC	724	2D4	764	2FC
605	25D	645	285	685	2AD	725	2D5	765	2FD
606	25E	646	286	686	2AE	726	2D6	766	2FE
607	25F	647	287	687	2AF	727	2D7	767	2FF
608	260	648	288	688	2B0	728	2D8	768	300
609	261	649	289	689	2B1	729	2D9	769	301
610	262	650	28A	690	2B2	730	2DA	770	302
611	263	651	28B	691	2B3	731	2DB	771	303
612	264	652	28C	692	2B4	732	2DC	772	304
613	265	653	28D	693	2B5	733	2DD	773	305
614	266	654	28E	694	2B6	734	2DE	774	306
615	267	655	28F	695	2B7	735	2DF	775	307
616	268	656	290	696	2B8	736	2E0	776	308
617	269	657	291	697	2B9	737	2E1	777	309
618	26A	658	292	698	2BA	738	2E2	778	30A
619	26B	659	293	699	2BB	739	2E3	779	30B
620	26C	660	294	700	2BC	740	2E4	780	30C
621	26D	661	295	701	2BD	741	2E5	781	30D
622	26E	662	296	702	2BE	742	2E6	782	30E
623	26F	663	297	703	2BF	743	2E7	783	30F
624	270	664	298	704	2C0	744	2E8	784	310
625	271	665	299	705	2C1	745	2E9	785	311
626	272	666	29A	706	2C2	746	2EA	786	312
627	273	667	29B	707	2C3	747	2EB	787	313
628	274	668	29C	708	2C4	748	2EC	788	314
629	275	669	29D	709	2C5	749	2ED	789	315
630	276	670	29E	710	2C6	750	2EE	790	316
631	277	671	29F	711	2C7	751	2EF	791	317
632	278	672	2A0	712	2C8	752	2F0	792	318
633	279	673	2A1	713	2C9	753	2F1	793	319
634	27A	674	2A2	714	2CA	754	2F2	794	31A
635	27B	675	2A3	715	2CB	755	2F3	795	31B
636	27C	676	2A4	716	2CC	756	2F4	796	31C
637	27D	677	2A5	717	2CD	757	2F5	797	31D
638	27E	678	2A6	718	2CE	758	2F6	798	31E
639	27F	679	2A7	719	2CF	759	2F7	799	31F

Table Continued on Next Page

TABLE 1D-1. DECIMAL-TO-HEXADECIMAL CONVERSION (Contd)

Dec	Hex	Dec	Hex	Dec	Hex	Dec	Hex	Dec	Hex
800	320	840	348	880	370	920	398	960	3C0
801	321	841	349	881	371	921	399	961	3C1
802	322	842	34A	882	372	922	39A	962	3C2
803	323	843	34B	883	373	923	39B	963	3C3
804	324	844	34C	884	374	924	39C	964	3C4
805	325	845	34D	885	375	925	39D	965	3C5
806	326	846	34E	886	376	926	39E	966	3C6
807	327	847	34F	887	377	927	39F	967	3C7
808	328	848	350	888	378	928	3A0	968	3C8
809	329	849	351	889	379	929	3A1	969	3C9
810	32A	850	352	890	37A	930	3A2	970	3CA
811	32B	851	353	891	37B	931	3A3	971	3CB
812	32C	852	354	892	37C	932	3A4	972	3CC
813	32D	853	355	893	37D	933	3A5	973	3CD
814	32E	854	356	894	37E	934	3A6	974	3CE
815	32F	855	357	895	37F	935	3A7	975	3CF
816	330	856	358	896	380	936	3A8	976	3D0
817	331	857	359	897	381	937	3A9	977	3D1
818	332	858	35A	898	382	938	3AA	978	3D2
819	333	859	35B	899	383	939	3AB	979	3D3
820	334	860	35C	900	384	940	3AC	980	3D4
821	335	861	35D	901	385	941	3AD	981	3D5
822	336	862	35E	902	386	942	3AE	982	3D6
823	337	863	35F	903	387	943	3AF	983	3D7
824	338	864	360	904	388	944	3B0	984	3D8
825	339	865	361	905	389	945	3B1	985	3D9
826	33A	866	362	906	38A	946	3B2	986	3DA
827	33B	867	363	907	38B	947	3B3	987	3DB
828	33C	868	364	908	38C	948	3B4	988	3DC
829	33D	869	365	909	38D	949	3B5	989	3DD
830	33E	870	366	910	38E	950	3B6	990	3DE
831	33F	871	367	911	38F	951	3B7	991	3DF
832	340	872	368	912	390	952	3B8	992	3E0
833	341	873	369	913	391	953	3B9	993	3E1
834	342	874	36A	914	392	954	3BA	994	3E2
835	343	875	36B	915	393	955	3BB	995	3E3
836	344	876	36C	916	394	956	3BC	996	3E4
837	345	877	36D	917	395	957	3BD	997	3E5
838	346	878	36E	918	396	958	3BE	998	3E6
839	347	879	36F	919	397	959	3BF	999	3E7

HSC CHECK-1 ERRORS (CCA)

The Check-1 Error indicates a controller has sensed a hardware check that prevents normal operation, or a wrong tag out sequence occurred. The Check-1 Error generates the CCA (Connection Check Alert).

The storage director responds by activating RCC1 (Request Connection Check) tag out. RCC1 causes the controller to send 33 bits of error data serially to the storage director. This is done through DDC Byte 1, Bit 0 for controller 0, Bit 1 for controller 1.

When either controller in an HSC detects a Check-1 error, error data is gathered from both controllers. This error data is displayed in the SEWs as CCA Bytes 0, 1, 2, and 3 for inline errors.

The CCA bytes for both controllers are available any time a Check-1 error is detected. Table 1D-2 shows the format of the CCA bytes (Check-1 Error Summary). Table 1D-3 describes each error, lists the FRUs that may fix the error, and lists inline routine(s) that may reproduce the error. If the error is not forced, no routine is listed.

Check-1 error bits are also displayed in sense Format 7. Table 1D-3 gives the byte/bit used to display these errors.

TABLE 1D-2. CHECK-1 ERROR SUMMARY

Byte	Bit 0	Bit 1	Bit 2	Bit 3
0	CCA (Any Check-1) Board: SJX	DPSE Force Release Board: SKX	Check-1 Isolation Bit 0 ←------See Note 3-----→ Board: SKX	Check-1 Isolation Bit 1 ←------See Note 3-----→ Board: SKX
1	DDC Bus In Par Sel Check Error Board: SKX	Not Used	DDC Tag Out Seq Check Board: SKX	Oriented Tag Seq Check-1 Board: SKX
2	Seq Addr Bit 0 (MSB) Board: SJX	Seq Addr Bit 1 Board: SJX	Seq Addr Bit 2 Board: SJX	Seq Addr Bit 3 Board: SJX
3	Seq Addr Bit 8 Board: SJX	Seq Addr Bit 9 Board: SJX	Seq Addr Bit 10 Board: SJX	Seq Addr Bit 11 (LSB) Board: SJX

TABLE 1D-2. CHECK-1 ERROR SUMMARY (Contd)

Byte	Bit 4	Bit 5	Bit 6	Bit 7
0	Check-1 Isolation Bit 2 See Note 3 Board: SKX	DDC Bus Out Par Check Board: SJX	Controller Clock Check Board: SNX	Controller Sequencer Check-1 Board: SJX
1	Sequencer Detected Check-1 Board: SKX	DDC Float Check Board: SKX	RCC Clock Check Board: SJX	Controller Power On Bit Board: SJX
2	Seq Addr Bit 4 Board: SJX	Seq Addr Bit 5 Board: SJX	Seq Addr Bit 6 Board: SJX	Seq Addr Bit 7 Board: SJX
3	Power On (Sequence) Complete Board: SLX	Check-2 Active Board: SNX	Successful RCC Data Transfer Board: SNX	Enable Upper Memory Board: SJX

NOTES:

1. The above 32 bits are sent serially on DDC Byte 1 (via Bit 0 for controller 0, and via Bit 1 for controller 1) in the order shown.

2. A clear bit occurs after the first 16 serial bits, making a total of 33 bits.

3. Isolation bit definitions:

   000 No Error
   001 Input Data Bus Parity Error (_SJX)
   010 Input/Output Port Pipeline Parity Error (_SKX)
   011 Not Used
   100 Pipeline A Parity Error (_SJX)
   101 Not Used
   110 Drvr/Rcvr or DDC Tag In Reg Parity Error (_SKX)
   111 Not Used

4. Bytes 0, 1, 2, and 3 are latched in a shift register on _SJX.

TABLE 1D-3. CHECK-1 ERROR MEANINGS

CCA Byte/Bit	Format 7 Byte/Bit	Name	Meaning
0/0	10/0	CCA	This bit is active whenever any Check-1 error bit is on. Routine: C80
0/1	11/2,3	DPSE Force Release	Controller 1 sends this bit to controller 2 (or vice-versa) to indicate forced release of a selected device. Routine: CA0, CA1
0/2,3,4	12/0,1,2	Check-1 Isolation Bits	These three bits are encoded to indicate one of the following eight possible conditions: 000- No error present 001- Parity error detected on Input data bus on _SJX board Routine: C80 FRUs: 1005, 1006, 1004, 1003, 1008

Table Continued on Next Page

TABLE 1D-3. CHECK-1 ERROR MEANINGS (Contd)

CCA Byte/Bit	Format 7 Byte/Bit	Name	Meaning
			010- Parity error detected in Pipeline B instructional fields decoded to enable an input or output port on _SKX board Routine: C80 FRUs: 1005, 1004, 1006, 1008 011- Not used 100- Parity error detected on Pipeline A instruction on _SJX board Routine: C80 FRUs: 1006, 1005, 1008 101- Not used
Table Continued on Next Page			

TABLE 1D-3. CHECK-1 ERROR MEANINGS (Contd)

CCA Byte/Bit	Format 7 Byte/Bit	Name	Meaning
			110- Parity error detected on Data Output bus as Tag In is sent to DDC interface, or as a transceiver gating signal is enabled on _SKX board Routine: C80 FRUs: 1005, 1006, 1008 111- Not used
0/5	12/3	DDC Bus Out Par Check-1	When on, this bit indicates a parity error on the DDC Byte 0 bus while a command or command modifier is present. Routine: C80 FRUs: 1006, 1005, 1007, 1008
0/6	12/4	Controller Clock Check	This bit becomes active when the controller system clock ring contains extra signals. Routine: C80 FRUs: 1007, 1008, 1006, 1004, 1005

Table Continued on Next Page

TABLE 1D-3. CHECK-1 ERROR MEANINGS (Contd)

CCA Byte/Bit	Format 7 Byte/Bit	Name	Meaning
0/7	12/5	Controller Sequencer Check-1	When on, this bit indicates a parity error was detected on Pipeline B on _SJX board. Bits not included in this check are those used to decode the input and output port enable signals. Routine: C80 FRUs: 1006, 1008, 1005
1/0	12/6	DDC Bus In Parity Sel Check Error	This bit is set by incorrect parity on DDC Byte 1 bus (from Data Output bus on _SLX board) or by gating wrong bus onto DDC Byte 1 bus during a Read operation. Routine: C80 FRUs: 1005, 1006, 1008, 1007
1/1		Not Used	
1/2	13/0	DDC Tag Out Seq Check	This bit is set by two Tag Out changes without an intervening Tag in response on the _SKX board. Routine: C80 FRUs: 1005, 1006, 1008

Table Continued on Next Page

TABLE 1D-3. CHECK-1 ERROR MEANINGS (Contd)

CCA Byte/Bit	Format 7 Byte/Bit	Name	Meaning
1/3	13/1	Oriented Tag Sequencer Check-1	This bit is set when an illegal Tag Out sequence is detected while the controller is oriented. Routine: C80 FRUs: 1005, 1006, 1007, 1008
1/4	13/2	Sequencer Detected Check-1	The functional microcode sets this bit when a Check-1 error is detected in software. The address returned during the RCC sequence will identify the source of the error. Routine: C80 FRUs: 1006, 1008, 1005
1/5	13/3	DDC Float Check	This bit sets (on the _SKX board) if the DDC Byte 0 or 1 bus is not being driven correctly during a control operation. The controller should be driving the Byte 1 bus, not the Byte 0 bus. Routine: C80 FRUs: 1006, 1005, 1007, 1008

Table Continued on Next Page

TABLE 1D-3. CHECK-1 ERROR MEANINGS (Contd)

CCA Byte/Bit	Format 7 Byte/Bit	Name	Meaning
1/6	13/4	RCC Clock Check	This error bit is active if the RCC clocks decoded from the DDC Byte 0 bus overlap, or if a bit in the Check-1 log is still active after an RCC tag sequence ends. Routine: C80 FRUs: 1007, 1008, 1006, 1004, 1005
1/7	11/4,5	Controller Power On Bit	This bit indicates that the HSC's power supply is still present. The storage director expects a one in this bit position; if not, the RCC data is assumed to be invalid.
-	-	Clear Bit	SD expects a zero to be sent here; if not, the RCC data is assumed invalid.
2/0-7 & 3/0-3	16/0-7 & 17/0-3	Sequencer Address Bits 1 to 11	These bits represent the Sequencer's address at the time a Check-1 or a Check-2 error was detected.
3/4	17/4	Power On (Sequence) Complete	This bit becomes active when all drive power-up sequencing is complete.

Table Continued on Next Page

TABLE 1D-3. CHECK-1 ERROR MEANINGS (Contd)

CCA Byte/Bit	Format 7 Byte/Bit	Name	Meaning
3/5	17/5	Check-2 Active	This bit sets if any Check-2 error was detected; it is cleared by a Check-1 Reset or a Check-2 Reset.
3/6	17/6	Successful RCC Data Transfer	This bit sets to inform the storage director that the RCC data is valid.
3/7	17/7	Enable Upper Memory	When a 0, this bit indicates that sequencer execution was in functional memory; when a 1, that execution was in diagnostic memory. It is, in effect, a 13th sequencer address bit.

HSC CHECK-2 FAULT LOG

The controller collects Check-2 errors into six bytes (Fault Log A through F). Data in the Fault Log is available to the storage director on execution of command 10.

Check-2 error data is displayed in the SEWs as Fault Log Bytes A through F for certain inline errors. Table 1D-4 shows the format for Fault Log Bytes A through F (Check-2 Error Summary). Table 1D-5 describes each error, lists FRUs that may fix the error, and lists routine(s) that may reproduce the error. If the error is not forced, no routine is listed.

Check-2 errors are also displayed in sense Format 8. Table 1D-5 gives the byte/bit used to display these errors.

TABLE 1D-4. CHECK-2 ERROR SUMMARY

Byte	Bit 0	Bit 1	Bit 2	Bit 3
A	Serdes Error Board: SPX	Codec Wrap Error Board: SPX	Software - Set Check-2 Board: SLX	Missing Servo Check Board: SPX
B	Write Control Check Board: SNX	Not Used	DDC Write Op Parity Check-2 Board: SKX	DDC Bus In Par Check 2 Board: SKX
C	ECC Bus Parity Check Board: SNX	CDP Bidir Data Par Check Board: SMX	Sync In/Out Error Board: SPX	CDP 12 Data Output Par Error Board: SMX
D	Device 0 Check-1 Board: SLX	Device 1 Check-1 Board: SLX	Device 2 Check-1 Board: SLX	Device 3 Check-1 Board: SLX
E	DPSE Memory Par Error Board: SKX	DPSE Data Bus Par Error Board: SKX	DPSE Mem Compare Error Board: SKX	DPSE Alt Controller Par Error Board: SKX
F	R/W Bus Out Par Check Board: SNX	ALU Output Parity Error Board: SNX	Ref. Data Parity Error Board: SNX	Read Parity Check Board: SNX

TABLE 1D-4. CHECK-2 ERROR SUMMARY (Contd)

Byte	Bit 4	Bit 5	Bit 6	Bit 7
A	CDP Input Bus Parity Error Board: SLX	Power Interrupt (From PCU)	Int. CDP Tag or Data Out Reg Par Board: SLX	Power Supply Tolerance Check (PCU)
B	Port Select Bit 0 Board: SLX	Port Select Bit 1 Board: SLX	Not Used	CDP Port Check-1 Board: SLX
C	String Config.	String Config.	CDP 12 Path Busy Parity Err Board: SMX	CDP Data Lock Par Check Board: SLX
D	Device Clock Check Board: SLX	Isolation Bit Board: SLX	Port Select Bit 2 Board: SLX	Port Select Bit 3 Board: SLX
E	DPSE Addr Parity Error Board: SKX	Not Used	DPSE Lock Parity Error Board: SKX	Not Used
F	Delta Frequency Check Board: SPX	Not Used	Not Used	Not Used

NOTES: Bytes A, B, C, and F are assembled on _SNX board.

Byte D is on _SLX, and Byte E is on _SKX.

TABLE 1D-5. CHECK-2 ERROR MEANINGS

Fault Log Byte/Bit	Format 8 Byte/Bit	Name	Meaning
A/0	11/0	Serdes Error	Parity check on SERDES input bus or control check in SERDES LSI chip (on _SPX board) will set the error. Routine: C80 FRUs: 1007, 1008, 1006, 1005
A/1	11/1	CODEC Wrap Error	During a Write operation, the data is encoded and decoded, then compared with the original, unencoded data to test the CODEC. Routine: C81 FRUs: 1008, 1007, 1004, 1005
A/2	11/2	Software Set Check-2	If a noncritical error is detected by microcode, the program will set this Check-2 bit. Routine: C80 FRUs: 1004, 1005, 1007

Table Continued on Next Page

TABLE 1D-5. CHECK-2 ERROR MEANINGS (Contd)

Fault Log Byte/Bit	Format 8 Byte/Bit	Name	Meaning
A/3	11/3	Missing Servo Check	Detects missing Servo Clock from selected device while Lock to Servo is active. Routine: C81 FRUs: 1008, 1007, 1005
A/4	11/4	CDP Input Bus Parity Error	Checks parity on Internal CDP Data Input Bus while Device Drivers Active is on. Routine: C81, CA2 FRUs: 1004, 1007, 2010, 1003, 1050
A/5	11/5	Power Interrupt	Indicates that the power supply is being interrupted, but will be active for at least another 40 milliseconds at full load. Routine: None FRUs: 1007, 1005, 1004, 1006, 1850
A/6	11/6	Internal CDP Tag or Data Out Register Parity	Checks parity on Data Output Bus and on Tag Out lines on CDP board (_SLX). Routine: C80 FRUs: 1004, 1007, 1005, 1006

Table Continued on Next Page

TABLE 1D-5. CHECK-2 ERROR MEANINGS (Contd)

Fault Log Byte/Bit	Format 8 Byte/Bit	Name	Meaning
A/7	11/7	Power Supply Tolerance Check	Detects when power supply voltages are not within allowable tolerances. Routine: C81 FRUs: 1851, 1007, 1004, 1850, 1005, 1006
B/0	12/0	Write Control Control Check	Sets if Write control lines have illegal combinations of signals. Routine: C80 FRUs: 1007, 1008, 1006, 1005
B/1	12/1	Not used.	
B/2	12/2	DDC Write Op Parity Check 2	Detects incorrect parity on DDC interface as data passes through _SKX board to _SNX board during a Write operation. Routine: C85 FRUs: 1007, 1008, 1006, 1004, 2011, 2010, 2008, 1003

Table Continued on Next Page

TABLE 1D-5. CHECK-2 ERROR MEANINGS (Contd)

Fault Log Byte/Bit	Format 8 Byte/Bit	Name	Meaning
B/3	12/3	DDC Bus In Parity Check-2	Checks parity of DDC Bus In Byte 0 or Byte 1 on Sequencer 2 board (_SKX) during a Read operation. Routine: C85 FRUs: 1007, 1008, 1006, 1004, 2011, 2010, 2008, 1003
B/4,5	12/4,5	Port Select Bits 0, 1	See definition for Log D, Bits 6 & 7. Routine: CA2
B/6	12/6	Not Used.	
B/7	12/7	CDP Port Check-1	Active when the selected port returns a Check-1 error. Routine: C81 FRUs: 1003, 1004, 2010, 1007, 1005, 1006
C/0	13/0	ECC Bus Parity Check	Detects incorrect parity on ECC Bus, Bytes 0 and 1. Routine: C80 FRUs: 1007, 1008, 1006, 1005

Table Continued on Next Page

TABLE 1D-5. CHECK-2 ERROR MEANINGS (Contd)

Fault Log Byte/Bit	Format 8 Byte/Bit	Name	Meaning
C/1	13/1	CDP Bidir Data Parity Check	Detects incorrect parity on bidirectional data lines from CDP 4 board (_SLX) to CDP 12 board (_SMX). Routine: C81 FRUs: 1003, 1007, 1004
C/2	13/2	Sync In/Out Error	Detects a failure in the Sync In/Sync Out exchange sequence. Routine: None FRUs: 1008, 1007, 1005, 1006, 1051
C/3	13/1	CDP 12 Data Output Par Error	Checks parity on Data Output Bus from Processor-Sequencer board (_SJX) to CDP 12 board (_SMX). Routine: C80 FRUs: 1003, 1006, 1004, 1005

Table Continued on Next Page

TABLE 1D-5. CHECK-2 ERROR MEANINGS (Contd)

Fault Log Byte/Bit	Format 8 Byte/Bit	Name	Meaning
C/4,5	13/4,5	String Configuration Bits	Bits 4 and 5 indicate the number of B drives in the string: 1 drive — Bit 4: 0, Bit 5: 0 2 drives — Bit 4: 0, Bit 5: 1 3 drives — Bit 4: 1, Bit 5: 0 4 drives — Bit 4: 1, Bit 5: 1
C/6	13/6	CDP 12 Path Busy Parity Error	Checks parity on DPSE Lock Bus from DPSE board (_SKX) to CDP 12 board (_SMX). Routine: CA0, CA1 FRUs: 1004, 1003, 1006, 1106, 1007, 1105, 1005
C/7	13/7	CDP Lock Data Parity Check	Checks parity on DPSE Lock Bus from DPSE board (_SKX) to CDP 4 board (_SLX). Routine: CA0, CA1 FRUs: 1004, 1007, 1005, 1105, 1106, 1006

Table Continued on Next Page

TABLE 1D-5. CHECK-2 ERROR MEANINGS (Contd)

Fault Log Byte/Bit	Format 8 Byte/Bit	Name	Meaning
D/0-3	14/0-3	Device Check Bits	Each device on a 4-driver port will set a bit if that device has a Check-1 error. Routine: C81, C84, C85, C88, CA2 FRUs: 1004, 1003, 2010, 2005, 2009, 1050
D/4	14/4	Device Clock Check	Active on a signal from the selected device indicating a problem with the device's multiphase clock. Routine: None FRUs: 1004, 1003, 2010, 2005, 2009, 1050
D/5	14/5	Isolation Bit	Sets if a device Select Check or Clock Check is detected. Routine: C81, CA2 FRUs: 2010, 1004, 2008, 2009, 1003, 2005, 2007, 2011
D/6,7	14/6,7	Port Select Bits	These two bits, along with Bits 4 and 5 of Log B, indicate port address of selected device at time of the check. Routine: CA2

Table Continued on Next Page

TABLE 1D-5. CHECK-2 ERROR MEANINGS (Contd)

Fault Log Byte/Bit	Format 8 Byte/Bit	Name	Meaning
E/0	15/0	DPSE Memory Par Error	Checks parity on DPSE Memory Data bus during a DPSE Write operation. Routine: CA0, CA1 FRUs: 1005, 1006, 1105, 1106
E/1	15/1	DPSE Data Bus Par Error	Checks parity on Data Out bus, and also checks for multiple drivers on Data Out bus. Routine: CA0, CA1 FRUs: 1005, 1004, 1006
E/2	15/2	DPSE Memory Compare Error	Compares data read from alternate controller's memory with data from current controller's memory. Error is set if data does not compare. Routine: C94, CA0, CA1 FRUs: 1005, 1006, 1105, 1106
E/3	15/3	DPSE Alt-ernate Controller Par Error	Error is set if alter-nate detects incorrect parity in its memory ad-dress or memory data. Routine: CA0, CA1 FRUs: 1005, 1006, 1105, 1106

Table Continued on Next Page

TABLE 1D-5. CHECK-2 ERROR MEANINGS (Contd)

Fault Log Byte/Bit	Format 8 Byte/Bit	Name	Meaning
E/4	15/4	DPSE Address Par Error	Compares parity on DPSE Memory Address bus with expected parity. Routine: C94, CA0, CA1 FRUs: 1005, 1004, 1006, 1105, 1104, 1106
E/5	15/5	Not Used	
E/6	15/6	DPSE Lock Bus Par Error	Checks parity on DPSE Lock Bus data coming from alternate controller. Routine: CA0, CA1 FRUs: 1005, 1006, 1105, 1106
E/7	15/7	Not Used	
F/0	18/0	R/W Bus Out Par Check	Detects parity error on R/W Bus bytes 0/1 when DDC data is gated onto the bus. Routine: C85 FRUs: 1007, 1008, 1006, 1004, 2011, 2010, 2008, 1003

Table Continued on Next Page

TABLE 1D-5. CHECK-2 ERROR MEANINGS (Contd)

Fault Log Byte/Bit	Format 8 Byte/Bit	Name	Meaning
F/1	18/1	ALU Output Par Error	Detects incorrect parity on R/W Bus bytes 0/1 when output from the ALU is gated onto the bus. Routine: C80 FRUs: 1007, 1005, 1004, 1006, 1008
F/2	18/2	Reference Data Parity Error	Detects parity error on R/W bus bytes 0/1 when PLA data is gated onto the bus. Routine: C80 FRUs: 1007, 1004, 1006, 1005
F/3	18/3	Read Parity Check	Detects parity error on R/W Bus Bytes 0/1 when SERDES read data is gated onto the bus. Routine: C80 FRUs: 1007, 1008, 1006, 1005

Table Continued on Next Page

TABLE 1D-5. CHECK-2 ERROR MEANINGS (Contd)

Fault Log Byte/Bit	Format 8 Byte/Bit	Name	Meaning
F/4	18/4	Delta Frequency Check	Error is set when the PLO tries to lock to a frequency which is too far from the nominal frequency. Routine: None FRUs: 1008, 1007, 1005, 1006,1051
F/5-7	18/5-7	Not Used.	

SECTION 2

INLINE DIAGNOSTICS/UTILITIES

INLINE DIAGNOSTICS/UTILITIES 2

INTRODUCTION

This section contains information on inline diagnostics and utility routines. This section is divided into subsections as follows:

Section 2 - Contains a table of all available inline diagnostics and utilities.

Section 2A - Contains descriptions of all available inline diagnostics and utilities.

Each routine description contains the following:

- Class - There are two classes: diagnostic and utility. Diagnostics are designed to test specific circuit functions in the controller and device. Utility routines are general purpose in nature and may not test anything. They provide the subsystem with additional capabilities.

- Linking - Gives the number of the previous routine and the number of the next routine. This applies only when linking is allowed and selected.

  The linked series is as follows: C80→CA0→CA2→C81→C82→C83→C84→C85→C86→C87→C88→C92.

  C92 links to C80 if loop linked series is selected.

- Parameters - Provide control functions that may or may not be the same for each routine.

- Description - Explains briefly what the routine/test will be testing and why it operates in a prescribed manner.

Refer to table 2-1 for a complete list of diagnostic and utility routines.

Refer to section 3 for operating procedures.

TABLE 2-1. INLINE DIAGNOSTICS/UTILITIES

Routine	Test	Test Name
B81	-	Inline Control Programs (ICP)
BFA	-	Terminate Inline Execution
BFB	-	Controller/Device Voltage Margin Status
BFC	-	Set/Reset Controller/Device Voltage Margins
BFD	-	Reset All Voltage Margins
BFE	-	Inhibit Timeouts
BFF	-	ICP and Storage Director DP Reset
C80	-	Basic Controller Logic
C80	1	Controller Selection
C80	2	Check-1 Verification
C80	3	Check-2 Verification
C81	-	Basic Device Logic
C81	1	Device Status
C81	2	Force Check-2
C81	3	Voltage Margins
C81	4	Register Checker
C81	5	CDP Wrap
C81	6	Difference Counter

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B81IC0

1790B

TABLE 2-1. INLINE DIAGNOSTICS/UTILITIES (Contd)

Routine	Test	Test Name
C81	7	Target Register
C81	8	Head Address Register
C81	9	Servo Register Parity
C81	A	Index Timing
C82	-	Dynamic Servo
C82	1	Rezero Verification
C82	2	Seek Verification - No Motion Seek
C82	3	Device Offset Verification
C82	4	R/W Mode Verification
C82	5	Read Home Address Verification
C82	6	Set HAR Oriented
C82	7	Incremental Seeks of 01 Cylinders
C82	8	Incremental Seeks of 02 Cylinders
C82	9	Incremental Seeks of 6E Cylinders
C82	A	Incremental Seeks of 1BB Cylinders
C82	B	Seeks of 376 Cylinders
C82	C	Invalid Seeks
C83	-	Set Sector
C83	1	Invalid Sector Verification
C83	2	Set Sector Verification
C83	3	Sector Compare Timing
C83	4	Verify Locate Cylinder and Sector

Table Continued on Next Page

TABLE 2-1. INLINE DIAGNOSTICS/UTILITIES (Contd)

Routine	Test	Test Name
C84	-	Write Functions
C84	1	Device R/W Checks
C84	2	Write Pad Verification
C84	3	Erase Verification
C84	4	Overrun Check Verification
C84	5	R/W Off Track Error Verification
C84	6	Clock Data Verification
C84	7	Write Inhibit
C84	8	Write Transition Check Verification
C85	-	Write/Read
C85	1	R/W Check-2 Verification
C85	2	Write Worst Case Data Pattern
C85	3	Write Count Field/Address Mark
C85	4	Padding Status
C85	5	Miscellaneous R/W
C86	-	ECC Verification
C86	0	Initialization
C86	1	ECC Write Burst
C86	2	ECC Correctable Pattern Part 1
C86	3	ECC Correctable Pattern Part 2
C86	4	ECC Uncorrectable Pattern
C86	5	Short Byte Count Read

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TABLE 2-1. INLINE DIAGNOSTICS/UTILITIES (Contd)

Routine	Test	Test Name
C87	-	Defect Skipping
C87	1	Write HA Defect Testing
C87	2	Write Full Track Defect Testing
C88	-	Force Write Padding Errors
C88	1	Force Write Padding Errors
C90	-	Pack Scan
C92	-	Track Reformat
C93	-	Force Device Available for Inline Routines
C93	1	Sense Functional Tables
C93	2	Force Device Available for Inlines
C94	-	Read/Write DPSE Array
C94	1	Read DPSE Array
C94	2	Write/Read DPSE Array
C95	-	Subsystem Exerciser
C95	0	Initialization
C95	1	Subsystem Exerciser
C9F	-	Continuous Seek

Table Continued on Next Page

TABLE 2-1. INLINE DIAGNOSTICS/UTILITIES (Contd)

Routine	Test	Test Name
CA0	-	Master Dynamic Path Selection
CA0	0	Initialization
CA0	1	Set/Reset DPSE Locks Command
CA0	2	Single SD Array R/W
CA0	3	Set/Reset Under Mask
CA0	4	Single SD Check-2
CA0	5	Dual SD Check-2
CA0	6	Set/Reset Array Locks
CA0	7	Copy Array
CA0	8	Main Array R/W
CA0	9	Device Selection
CA0	A	Selection Contention
CA0	B	R/W Device Parameters
CA0	C	Cleanup Commands
CA0	D	Device Unconditional Release
CA1	-	Slave Dynamic Path Selection
CA1	0	Initialization
CA1	1	Set/Reset DPSE Locks Command
CA1	2	Single SD Array R/W
CA1	3	Set/Reset under Mask
CA1	4	Single SD Check-2
CA1	5	Dual SD Check-2
CA1	6	Set/Reset Array Locks
CA1	7	Copy Array
CA1	8	Main Array R/W
CA1	9	Device Selection

Table Continued on Next Page

TABLE 2-1. INLINE DIAGNOSTICS/UTILITIES (Contd)

Routine	Test	Test Name
CA1	A	Selection Contention
CA1	B	R/W Device Parameters
CA1	C	Cleanup Commands
CA1	D	Device Unconditional Release
CA2	-	Device Selection Logic
CA6	-	Command Cycle
CA7	-	FSC/FRU Generator/Sense Byte Collection
CA7	1	FSC Generation
CA7	2	Fault Log and Device Status
CA7	3	Report FRUs for Error Code
CA7	4	Report FRUs for Fault Symptom Code
CA9	-	Seek Timing
CA9	1	1-Cylinder Seek
CA9	2	3-Cylinder Seek
CA9	3	9-Cylinder Seek
CA9	4	21-Cylinder Seek
CA9	5	52-Cylinder Seek
CA9	6	110-Cylinder Seek
CA9	7	221-Cylinder Seek
CA9	8	295-Cylinder Seek
CA9	9	443-Cylinder Seek
CA9	A	886-Cylinder Seek

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TABLE 2-1. INLINE DIAGNOSTICS/UTILITIES (Contd)

Routine	Test	Test Name
CAA	-	Incremental Seek
CAB	-	Cylinder Seek
CAC	-	Random Seek
CAD	-	Offset Limits

SECTION 2A

ROUTINE/TEST DESCRIPTIONS

INTRODUCTION

This section contains descriptions of inline diagnostics and utility routines available for testing and analyzing the controller and device.

ROUTINE B81 -- INLINE CONTROL PROGRAMS (ICP)

This routine is a noncallable routine consisting of inline control programs, monitor, and diagnostic scheduler. The ICP controls the execution of inline diagnostic routines, interfacing to the functional and interface handler as necessary. It handles diagnostic requests from three sources: SD, controller, and CPU channel.

ROUTINE BFA -- TERMINATE INLINE EXECUTION

Class: Utility

Linking: Not Linked

Parameters: None

This routine signals the diagnostic scheduler that inline testing is complete. The diagnostic scheduler then resets the inline execution flags.

This routine should be executed after inline testing is complete. If inlines were run from the storage control, press CMD (Q), CLR (Z), and EXEC (X) also.

ROUTINE BFB -- CONTROLLER/DEVICE VOLTAGE MARGIN STATUS

Class: Utility

Linking: Not Linked

Parameters: None entered, but are used for display as explained on the next page.

NOTE

Run this routine with the maintenance panel connected to the DP or from a terminal.

This routine displays the voltage margin status stored in memory by routine BFC. If this memory area is destroyed (IML, SD power off/on, etc.), the voltage margin status will indicate no margins set, when they may be set. The reverse is also true. If a controller or device is powered off, the voltage margins in that controller or device are reset. The voltage margin status displayed comes from SD memory and may indicate margins set for that controller or device, when they are not.

Parameters are not entered in this routine, but are used to display the current voltage margin status stored in memory.

NOTE

In the parameters listed below, the following byte/bits are the same for each parameter:

Byte=00 indicates no margins set

Bit 6 set indicates margins set high

Bit 7 set indicates margins set low

Parameters: 1L - Controller 0 margins

Bit 1 set= Both -5.2-V and +5-V supplies; ignore Bit 2

Bit 2 set= -5.2-V supply; reset= +5.0-V supply

Bit 5 set= Reserved

2L - Controller 1 margins

Bit 1 set= Both -5.2-V and +5-V supplies; ignore Bit 2

Bit 2 set= -5.2-V supply; reset= +5.0-V supply

Bit 5 set= Reserved

3L Controller 0, Device 0 margins
4L - Controller 0, Device 1 margins
5L - Controller 0, Device 2 margins
6L - Controller 0, Device 3 margins
7L - Controller 0, Device 4 margins
8L - Controller 0, Device 5 margins
9L - Controller 0, Device 6 margins
10L - Controller 0, Device 7 margins
11L - Controller 0, Device 8 margins
12L - Controller 0, Device 9 margins
13L - Controller 0, Device A margins
14L - Controller 0, Device B margins
15L - Controller 0, Device C margins
16L - Controller 0, Device D margins
17L - Controller 0, Device E margins
18L - Controller 0, Device F margins
19L - Controller 1, Device 0 margins
20L - Controller 1, Device 1 margins
21L - Controller 1, Device 2 margins
22L - Controller 1, Device 3 margins
23L - Controller 1, Device 4 margins
24L - Controller 1, Device 5 margins
25L - Controller 1, Device 6 margins
26L - Controller 1, Device 7 margins
27L - Controller 1, Device 8 margins
28L - Controller 1, Device 9 margins
29L - Controller 1, Device A margins
30L - Controller 1, Device B margins
31L - Controller 1, Device C margins
32L - Controller 1, Device D margins
33L - Controller 1, Device E margins
34L - Controller 1, Device F margins

ROUTINE BFC -- SET/RESET CONTROLLER/DEVICE VOLTAGE MARGINS

Class: Utility

Linking: Not Linked

Parameters: 1H - Controller margins

- Bit 0 - Unused
- Bit 1 set= Both -5.2-V and +5-V supplies; ignore Bit 2
- Bit 2 set= -5.2 V supply; reset = +5.0 V supply
- Bit 3 - Both controllers if set
- Bit 4 - Reset margins
- Bit 5 - Reserved
- Bit 6 - Margins high
- Bit 7 - Margins low

1L - Device margins

- Bit 0 - Unused
- Bit 1 - Unused
- Bit 2 - Unused
- Bit 3 - All devices if set
- Bit 4 - Reset margins
- Bit 5 - Unused
- Bit 6 - Margins high
- Bit 7 - Margins low

NOTE

Run this routine with the maintenance panel connected to the DP or from a terminal.

This routine sets or resets any or all of the voltage margins for a controller(s) or device(s). These voltage margin settings are also stored in memory. When routine BFB is used to display voltage margin status, memory is read and displayed in the parameters. This will be the power supply setting(s) if power on the SD, controller, or device has not been turned off and on. See routine BFB description.

Inline linked series should run error-free on each unit to be placed in margins before this utility is executed.

If only one device and/or controller is to be placed in margins, run routine 102 to select the desired controller/device. Refer to SC Hardware Diagnostic Reference Manual (Publication Number 83324410) for routine 102 description and parameter values.

ROUTINE BFD -- RESET ALL VOLTAGE MARGINS

Class: Utility

Linking: Not Linked

Parameters: None

NOTE

Run this routine with the maintenance panel connected to the DP or from a terminal.

This routine resets all voltage margins in the storage director(s), controller(s), and device(s). If functional activity is present, resetting the device margins may require varying the device offline for this utility to gain access to the device. This routine is also executed on the DP operating system when the RTA switch on the operator's panel is set to position 0.

ROUTINE BFE -- INHIBIT TIMEOUTS

Class: Utility

Linking: Not Linked

Parameters: None

This routine inhibits port busy timeout errors RRRTOF, select controller retry error B811CB, DPSE synchronization timeout errors CAXXFE and CAXXFF, and voltage margin request busy timeout error B811FF.

CAUTION

If a real failure is bypassed, test execution display will be given, but the test may never execute. This is especially true when executing under loop on test mode.

ROUTINE BFF -- ICP AND STORAGE DIRECTOR DP RESET

Class: Utility

Linking: Not Linked

Parameters: None

This routine resets the storage control diagnostic processor and inline control program to the IML state. It also resets storage control diagnostic processor for failure codes 0004XX.

This routine should be executed before running inlines and after inline testing is complete. (See routine BFA.)

ROUTINE C80 -- BASIC CONTROLLER LOGIC

Class: Diagnostic

Linking: First routine in linked series; to CA0

Parameters: 1H - Test number (1-3); default=00

This routine verifies the controller logic and selection capabilities, excluding the DPSE logic interface (which is checked by routine CA0) and those Check-2 errors requiring device selection to test (see routine C81, test 3 and routine C85, test 1). This routine consists of three tests.

ROUTINE C80, TEST 1 -- CONTROLLER SELECTION

This test checks initial selection of the controller to verify that communication between the SD and the controller is functioning and that the controller itself is working. It verifies that no Check-2 errors are active on entry. Tag sequences and responses for the controller are checked with command 11 (sense features command). Next a hardware immediate is issued to the controller to verify that the basic self-test in the controller executes correctly. A DDC bus out to bus in wrap and a DDC tag out to tag in gray code wrap is performed and checked. Last, the SD sends the command for the controller to execute its basic self-test via the diagnostic macro 0B verifying the sequencer's instruction set execution and that no CCAs or error responses are returned.

NOTE

Basic self-test is an automatic diagnostic that is used to ensure that the HSC's basic instruction execution is functional. The test groups are executed in an inverted pyramid fashion so that, as much as possible, no instruction or logic is used before it has been tested.

Self-test is divided into two groups of instructions:

- Primary group of instructions
- Secondary group of instructions

A failure in the primary group of instructions will set a Check-1 error and display error code C80104. The sequencer is stopped and CCA information is set for the SD.

A failure in the secondary group of instructions will produce an error code.

There are three ways to initiate self-test. Each one executes differently:

- Initial HSC power on -- Self-test executes all of the primary group of instructions.
- Hardware Immediate/Hang Reset -- Self-test executes only part of the primary group of instructions.
- Inline routine C80, test 1 -- Self-test executes all of the primary and secondary groups of instructions.

ROUTINE C80, TEST 2 -- CHECK-1 VERIFICATION

This test exercises Check-1 error circuitry in the controller and verifies that the correct response for the Check-1 error being tested is indicated in the CCA bytes. The test verifies that a CCA is not present at the start of testing. The Check-1 errors are then forced and the expected response for each Check-1 error is verified. (DPSE force release is tested in routine CA0, test 9.)

ROUTINE C80, TEST 3 -- CHECK-2 VERIFICATION

This test exercises those Check-2 errors that can be forced with controller selection. It tests for the correct response for the Check-2 being tested in the fault log and that the Check-2 Bus In response is received with End Op. It then performs a hardware immediate to reset the Check-2 condition and verifies that the error is reset in the fault log.

ROUTINE C81 -- BASIC DEVICE LOGIC

Class: Diagnostic

Linking: From CA2; to C82

Parameters: 1H - Test number (1-A); default=00

This routine is the first check of device logic. The device must be powered up. This routine consists of ten tests.

ROUTINE C81, TEST 1 -- DEVICE STATUS

The device status tags are issued and verified for normal status. Then diagnostic command 5F is issued to force a Device Check. The device check bits and the isolation bit in fault log D (Sense Byte 14) are verified for the proper error condition and that the device check and fault log can be reset.

ROUTINE C81, TEST 2 -- FORCE CHECK-2

This test uses diagnostic macros to force Check-2 errors similar to routine C80, test 3, except that device selection is required to force these errors. The errors are checked for the correct response for the Check-2 being tested in the fault log. The Check-2 bus in end op response is verified. A hardware immediate is performed to reset the Check-2, and the fault log is sensed to verify that the Check-2 is reset.

ROUTINE C81, TEST 3 -- VOLTAGE MARGIN

Controller Out of Tolerance Check-2 is tested with the controller margined at: +5 V extended low, +5 V extended high, -5.2 V extended low, and -5.2 V extended high.

The device margin capability is tested by setting device margins low and high, checking that margins active command 51 Bit 0 is set for both cases. Margins are reset and verified to be

reset between each margin case tested. The device and controller margins set at the start of the test are saved and restored after voltage margin testing if no failure occurs. If a failure occurs, zero voltage margins are attempted to be restored. This should be verified by using routine BFB before further testing.

ROUTINE C81, TEST 4 -- REGISTER CHECKER

This test forces parity checks on the Difference counter, Target register, and Head Address register using diagnostic device command 49. This causes an RPS Check and a Servo Control Check. After the CDP bus is split using a diagnostic macro, an HAR Parity Check is forced. These three checks are then checked, reset, and verified reset.

ROUTINE C81, TEST 5 -- CDP WRAP

This test forces an Internal Mux CDP/DPSE Check using the device diagnostic command 5E. The check is verified set, reset and verified reset. Using the Head Address register, a CDP bus out wrap is performed using sliding 1's, 5A, A5, FF, and 00 patterns. Internal Mux CDP/DPSE check is verified reset after each pattern. The device diagnostic command 45 is then used to perform a bus in wrap of FF by setting the check point log to FF and sensing it via the sense selected device checks command 55. A Check Point Check is also verified set from the 45 command and that the check can be reset.

ROUTINE C81, TEST 6 -- DIFFERENCE COUNTER

This test verifies the setting of data into the Difference counter independent of a seek operation. Incorrect setting of the Difference counter will be indicated by the Servo Control Check that was verified in test 4. Data patterns are sent to Difference counter low while Difference counter high is set to 00. If Difference counter low does not fail, data patterns are sent to Difference counter high while Difference counter low is set to 00.

ROUTINE C81, TEST 7 -- TARGET REGISTER

This test verifies the setting of data into the Target register independent of a set sector operation. Incorrect setting of the Target register will be indicated by the RPS Check that was verified in test 5.

ROUTINE C81, TEST 8 -- HEAD ADDRESS REGISTER

This test verifies the setting of data into HAR. A special diagnostic macro is issued to set the CDP bus into split bus mode independent of a set R/W command. The HAR Parity Check is examined after each pattern is sent. The HAR Parity Check was verified in test 5.

ROUTINE C81, TEST 9 -- SERVO REGISTER PARITY

This test checks that the parity checker on Servo Register 1 is working properly. Bad parity is forced by the 72 command, followed by a verification of Servo Control Check from the 55 command (indicating bad parity was detected).

ROUTINE C81, TEST A -- INDEX TIMING

This test uses a special diagnostic macro to send the index pulse from the device to the DDC interface so that it can be measured by the SD. A set R/W command is performed to split the CDP bus, allowing the transmission of index pulse from the device to the controller. The index pulse is then measured for width to be between 10.2 and 10.9 microseconds and that the time between index pulses is between 16.247 and 16.916 milliseconds.

ROUTINE C82 -- DYNAMIC SERVO

Class: Diagnostic

Linking: From C81; to C83

Parameters: 1H - Test number (1-C); default=00

1L - Head number (00-0E); default=head 00

2H - Test mode (tests 5 and 6 only)

80= Default - test all heads, ignore parameter 1L

00= Test only head specified in parameter 1L

This routine checks the proper operation of the device access mechanism and related logic. The ability to read Home Address is also tested and is used to verify the access positions. This routine consists of twelve tests.

ROUTINE C82, TEST 1 -- REZERO VERIFICATION

This test rezeros the device, checking that the device accepts and executes the command. Sense device status 1 response is checked for Busy to be on and correct ending status at completion of the Rezero Seek. After the reset interrupts command, the sense device status 1 response is checked for Online only. If a servo inhibit occurs, a Rezero Seek will be performed in an attempt to clear the servo inhibit.

After the Rezero Seek is verified, bad parity is forced on Servo Register 2 and checks that a Servo Control Check indication is received. The servo inhibit produced by this command is reset by a Rezero Seek.

ROUTINE C82, TEST 2 -- SEEK VERIFICATION - NO MOTION SEEK

This test performs a no motion seek, checking that the device accepts and executes the command. Sense device status 1 response is checked for Busy to be on and correct ending status at completion of the Seek. The poll devices response is checked for an interrupt from this device and, if no other interrupts are active, the poll controller combined device interrupt bit is checked. After the reset interrupts command, these interrupts are verified to be reset; the sense device status 1 response is checked for Online only. If a servo inhibit occurs, a Rezero Seek will be performed in an attempt to clear the servo inhibit.

ROUTINE C82, TEST 3 -- DEVICE OFFSET VERIFICATION

This test performs a device Offset command, verifying that the device accepts the command and starts execution. Device Busy should be on at this time. Completion status is verified when Device Busy is off. The Offset Active indicator is checked to be on after each nonzero offset and that it is off for a zero offset. If a servo inhibit condition occurs, the device will be rezeroed before reporting the error. A check is made that when the Offset Active indicator is on the locate cylinder command is terminated with Seek Incomplete status. A check is also made to verify that the Rezero Seek resets the Offset Active indicator.

ROUTINE C82, TEST 4 -- R/W MODE VERIFICATION

This test performs a Set R/W command, checked that the End Op DBI response equals 00. An End R/W command is then issued.

ROUTINE C82, TEST 5 -- READ HOME ADDRESS VERIFICATION

This test performs a Rezero Seek followed by reading Home Address on one or all heads, depending upon parameter 2H. A Set R/W command is issued for each headed tested. The Home Address read is checked for the expected physical address bytes.

ROUTINE C82, TEST 6-- SET HAR ORIENTED

This test performs a Rezero Seek followed by a Set R/W. Then Set HAR Oriented is tested for one or all heads depending upon parameter 2H. The Home Address read is checked for the expected physical address bytes.

ROUTINE C82, TEST 7 -- INCREMENTAL SEEKS OF 01 CYLINDERS

This test performs 16 forward and reverse incremental one-cylinder seeks. The access position is verified by reading the Home Address of the head specified in parameter 1L. The test performs a Rezero Seek, seeks incrementally to cylinder 16, and then seeks incrementally back to cylinder zero.

ROUTINE C82, TEST 8 -- INCREMENTAL SEEKS OF 02 CYLINDERS

This test performs eight forward and reverse incremental seeks with 2-cylinder increments. The access position is verified by reading the Home Address of the head specified in parameter 1L. The test performs a Rezero Seek, seeks incrementally to cylinder 16, and then seeks incrementally back to cylinder zero.

ROUTINE C82, TEST 9 -- INCREMENTAL SEEKS OF 6E CYLINDERS

This test performs four forward and reverse incremental seeks with $6E_{16}$-cylinder increments. The access position is verified by reading the Home Address of the head specified in parameter 1L. The test performs a Rezero Seek, seeks incrementally to cylinder 1B8, and then seeks incrementally back to cylinder zero.

ROUTINE C82, TEST A -- INCREMENTAL SEEKS OF 1BB CYLINDERS

This test performs two forward and reverse incremental seeks with $1BB_{16}$-cylinder increments. The access position is verified by reading the Home Address of the head specified in parameter 1L. The test performs a Rezero Seek, seeks incrementally to cylinder 376 (CE cylinder), and then seeks incrementally back to cylinder zero.

ROUTINE C82, TEST B -- SEEKS OF 376 CYLINDERS

This test performs one forward and reverse seek of 376_{16}-cylinders. The access position is verified by reading the Home Address of the head specified in parameter 1L. The test performs a Rezero Seek, seeks to cylinder 376 (CE cylinder), and then seeks back to cylinder zero.

ROUTINE C82, TEST C -- INVALID SEEKS

This test checks that a seek with a invalid length produces an error and that issuing a second seek before Seek Complete is received produces an error.

ROUTINE C83 -- SET SECTOR

Class: Diagnostic

Linking: From C82; to C84

Parameters: 1H - Test number (1-4); default=00

This routine checks the proper operation of the RPS logic. This routine consists of four tests.

ROUTINE C83, TEST 1 -- INVALID SECTOR VERIFICATION

This test sets up an invalid sector argument of DE (sector 223) and executes a Set Sector command, checking Sense device status 1 for Search Sector in Progress. When Busy is inactive, the status is checked for Set Sector Not Complete active, and that a Check Reset command clears this condition. A Rezero Seek is performed before exiting the test.

ROUTINE C83, TEST 2 -- SET SECTOR VERIFICATION

This test performs a Set Sector command for all valid sector arguments. Each Set Sector is checked for Search Sector in Progress, Busy, and Set Sector Not Complete. Poll device is performed to check for Interrupt Active from each Set Sector command, and that the interrupt is reset after a Reset Interrupts command.

ROUTINE C83, TEST 3 -- SECTOR COMPARE TIMING

This test performs a Set Sector command for 16 values, checking that the sector compare time is approximately 75 microseconds long. It also checks that a sector compare is found within one revolution.

ROUTINE C83, TEST 4 -- VERIFY LOCATE CYLINDER AND SECTOR

A Rezero Seek is performed and the Locate Cylinder and Sector command is issued for the CE cylinder and sector 20. After the seek completes, the set sector portion of the command is verified similar to test 2. The locate cylinder portion of the command is verified by reading the Home Address of CE cylinder head 0 and comparing expected and received physical address bytes.

ROUTINE C84 -- WRITE FUNCTIONS

Class: Diagnostic

Linking: From C83; to C85

Parameters: 1H - Test number (1-8); default=00

1L - Head number (00-0E); default=head 00

This routine checks for the proper operation of pad, erase, and clock functions. It also forces Padding Check, Write Overrun, Write Encoder error, and other device R/W checks. Test 7 checks the Write Inhibit condition. This routine consists of eight tests.

ROUTINE C84, TEST 1 -- DEVICE R/W CHECKS

This test selects the device and resets any outstanding checks and interrupts. The test then seeks to the CE cylinder and verifies access position by reading the Home Address of the

head specified by parameter 1L. The following device R/W checks are forced by a diagnostic macro, checking that the checks can be set and reset: Matrix error, Safety Active Check, Matrix Selection Check, Padding Check, Write Sequence Check, R/W Check, and Read Sequence Check.

ROUTINE C84, TEST 2 -- WRITE PAD VERIFICATION

This test selects the device and resets any outstanding checks and interrupts. The test then seeks to the CE cylinder and verifies access position by reading the Home Address of the head specified by parameter 1L. The test then write pads four segments and verifies the padding operation by attempting to read the padded area, checking for First Sync In and End of Transfer not received.

ROUTINE C84, TEST 3 -- ERASE VERIFICATION

This test selects the device and resets any outstanding checks and interrupts. The test then seeks to the CE cylinder and verifies access position by reading the Home Address of the head specified by parameter 1L. The test then erases four segments and verifies the erase operation by attempting to read the erased area, checking for First Sync In and End of Transfer not received.

ROUTINE C84, TEST 4 -- OVERRUN CHECK VERIFICATION

This test selects the device and resets any outstanding checks and interrupts. The test then seeks to the CE cylinder and verifies access position by reading the Home Address of the head specified by parameter 1L. R/W and Write Overrun Checks are forced by a diagnostic macro. The proper check indications are tested to be set and that they can be reset.

ROUTINE C84, TEST 5 -- R/W OFF TRACK ERROR VERIFICATION

This test selects the device and resets any outstanding checks and interrupts. The test then seeks to the CE cylinder and, while the seek is in progress, attempts to read Home Address. A R/W Off Track error is verified set and that it can be reset.

ROUTINE C84, TEST 6 -- CLOCK DATA VERIFICATION

This test selects the device and resets any outstanding checks and interrupts. The test then seeks to the CE cylinder and verifies access position by reading the Home Address of the head specified by parameter 1L. A clock data command is executed and checks are made for any R/W Check active.

ROUTINE C84, TEST 7 -- WRITE INHIBIT

This test issues a Rezero Seek to the selected device and checks for Write Inhibit not active, then checks that Write Inhibit is active for a forward and a reverse offset. Diagnostic device command 5A is used to load the check point log with the write inhibit status. The status is then sensed with sense check point log command 57.

ROUTINE C84, TEST 8 -- WRITE TRANSITION CHECK VERIFICATION

This test selects the device and resets any outstanding checks and interrupts. The test then seeks to the CE cylinder and verifies access position by reading the Home Address of the head specified by parameter 1L. Write Transition and Matrix Checks are forced by a diagnostic macro. The proper check indications are tested to be set and that they can be reset.

ROUTINE C85 -- WRITE/READ

Class: Diagnostic

Linking: From C84; to C86

Parameters: 1H - Test number (1-5); default=00

1L - Head number (00-0E) default=80, test all heads

2H - R/W option; default=00, write and read once. If loop on test option is selected, the following bits are valid:

- Bit 0 set= write once and loop on read
- Bit 1 set= loop on write
- Bits 0 and 1 set= loop on write
- Bits 2 thru 7= not used

2L - Not used

3H - Write/read pattern; default=31

3L - Write/read pattern; default=8C

4H - Write/read pattern; default=63

4L - Write/read pattern; default=18

5H - Write/read pattern; default=C6

5L - Not used

NOTE

Parameters 1L through 5H are used for tests 2 and 3 only.

This routine checks the remaining Check-2 bits in the fault log. A worst case data pattern (or CE pattern entered) is written and read back, comparing each byte with the expected data. The ability to write and read an address mark is also tested. This routine consists of five tests.

Test 4 checks the device status indications during and after a pad operation. Test 5 checks for no sync byte but data found response, and for no sync byte and no data found response (indicating no more records on the track).

ROUTINE C85, TEST 1 -- R/W CHECK-2 VERIFICATION

This test seeks to the CE cylinder and verifies the access position by reading Home Address and comparing the expected physical address bytes read. A DDC Write Op Parity Check is forced by performing a write with bad parity from the storage director. A diagnostic macro is issued to inhibit R/W Bus Out Parity Check. The check is forced once for bad parity on Byte 0 and then again for bad parity on Byte 1. A R/W Bus Out Parity Check is forced the same way, except the diagnostic macro inhibits the DDC Write Op Parity Check. Then a DDC Bus In Parity Check is checked by an extended diagnostic macro, followed by a read Home Address to force the error. Each check is verified set, that it can be reset, and that the expected End Op DBI of 10 is received.

ROUTINE C85, TEST 2 -- WRITE WORST CASE DATA PATTERN

This test seeks to the CE cylinder and verifies the access position by reading Home Address and comparing the expected physical address bytes read.

Default mode writes the worst case data pattern (default parameters 3H-5H) in a defect-free area of the CE cylinder and reads the data back. The data read back is compared with the worst case data pattern or some other pattern if parameters 3H-5H are changed by the CE.

ROUTINE C85, TEST 3 -- WRITE COUNT FIELD/ADDRESS MARK

This test seeks to the CE cylinder and verifies the access position by reading Home Address and comparing the expected physical address bytes read. A non-record zero count field is written, preceded by a pad of 10 segments. This count field is then read with an address mark search operation starting at the beginning of the padded 10 segments. The bytes read are compared with the data written.

ROUTINE C85, TEST 4 -- PADDING STATUS

This test seeks to the CE cylinder and verifies the access position by reading Home Address and comparing the expected physical address bytes read. A format write operation is performed, followed by device padding. The device padding status is verified.

ROUTINE C85, TEST 5 -- MISCELLANEOUS R/W

This test seeks to the CE cylinder and verifies the access position by reading Home Address and comparing the expected physical address bytes read. A non-record zero count field is written. Then an attempt is made to read this field after spacing over the sync byte. Sync byte missing but data found response is verified. During pass 2 the count field is spaced over and a read is attempted in the padded area. No Sync Byte Found and No Data Found response is verified, indicating no more records on the track.

ROUTINE C86 -- ECC VERIFICATION

Class: Diagnostic

Linking: From C85; to C87

Parameters: 1H - Test number (1-5); default=00

1L - Head number (00-0E); default=head 00

This routine checks for proper operation of the ECC logic. The routine consists of an initialization test which tests the initial ECC registers. The five other tests check the ECC logic for good, correctable, and uncorrectable data patterns. A check is also made that a read with a short data length produces a Data Check. The data pattern is 123456789ABCDEF02130-000000000000, which tests all 16 bits of the ECC generation logic to be on and off.

ROUTINE C86, TEST 0 -- INITIALIZATION

This test checks reset ECC registers. It performs a hardware immediate that resets the ECC registers, then does a seek to the CE cylinder and reads Home Address, verifying access position and setting Cable Calibration. The ECC registers are then sensed and verified for the expected pattern of 12 bytes of 00.

ROUTINE C86, TEST 1 -- ECC WRITE BURST

This test seeks to the CE cylinder and reads Home Address to verify the access position. The ability of the controller to calculate the correct ECC is checked by writing the data pattern and then reading back with a long byte count to read the ECC bytes as data. The ECC bytes read are then compared with the expected values.

ROUTINE C86, TEST 2 -- ECC CORRECTABLE PATTERN PART 1

This test seeks to the CE cylinder and reads Home Address to verify the access position. The data pattern bytes and ECC bytes are written with a correctable error in the ECC bytes. Only the data is read back, resulting in a correctable error due to the ECC bytes written. End Op DBI is checked for no Data Check received. Eleven cases are tried, six cases where each ECC word is inverted and five cases where each two ECC words are inverted. (Note: A word is two bytes.)

ROUTINE C86, TEST 3 -- ECC CORRECTABLE PATTERN PART 2

This test seeks to the CE cylinder and reads Home Address to verify the access position. The data pattern bytes and ECC bytes are written with a correctable error in the data bytes. Only the data is read back, resulting in a correctable error due to the data bytes written. End Op DBI is checked to verify that expected Data Check was received. The ECC bytes are sensed and are verified for the expected values. The five patterns written are:

- Pattern 1 -- the first data word is inverted
- Pattern 2 -- the second data word is inverted
- Pattern 3 -- the first and second data words are inverted
- Pattern 4 -- the second and third data words are inverted
- Pattern 5 -- the last data word and the first ECC word are inverted

ROUTINE C86, TEST 4 -- ECC UNCORRECTABLE PATTERN

This test seeks to the CE cylinder and reads Home Address to verify the access position. The data pattern bytes and ECC bytes are written with an uncorrectable error in the data bytes. Only the data is read back, resulting in an uncorrectable error due to the data bytes written. End Op DBI is checked to verify that the expected Data Check was received. The ECC bytes are sensed and are verified for the expected values. The four patterns written are:

- Pattern 1 -- the first and third data words are inverted
- Pattern 2 -- the second and fourth data words are inverted
- Pattern 3 -- the first and fourth data words are inverted
- Pattern 4 -- the second and fifth data words are inverted

ROUTINE C86, TEST 5 -- SHORT BYTE COUNT READ

This test seeks to the CE cylinder and reads Home Address to verify the access position. A data pattern (84 bytes) is written and then read back with a short byte count (52 bytes). End Op DBI is verified for the expected Data Check.

ROUTINE C87 -- DEFECT SKIPPING

Class: Diagnostic

Linking: From C86; to C88

Parameters: 1H - Test number (1-2); default=00

1L - Head number (00-0E); default=80

- Bit 0 set= Scan heads 01-0E for a defect-free test track
- Bit 0 reset= Use head specified by Bits 4-7 as the defect-free test track

This routine writes various fields on the CE cylinder using simulated defects, verifying that these fields can be correctly read. Test 1 performs Home Address defect testing. Test 2 performs full track read and write defect testing.

The test track will be reformatted with a standard Home Address and a standard Record Zero (no key field and a data field equal to eight bytes of zeroes) at test completion. The test track must be defect-free and not flagged as either defective or alternate. C87XFE errors will be bypassed if linked series is looped.

ROUTINE C87, TEST 1 -- WRITE HA DEFECT TESTING

This test seeks to the CE cylinder and verifies the access position using the head specified by parameter 1L if Bit 0 is reset, or else head 01-0E, checking the CE cylinder for a defect-free test track. Skip control words are written simulating defects in segments causing Write Home Address normal, Write Home Address moved once, twice, and three times.

Read Home Address after each write verifies the Home Address was written correctly.

The track is reformatted with the original Home Address and a standard Record Zero (no key field and a data field equal to eight bytes of zeroes) at test completion.

Reformatting may be attempted in the event of a detected error situation.

ROUTINE C87, TEST 2 -- WRITE FULL TRACK DEFECT TESTING

This test seeks to the CE cylinder and verifies the access position using the head specified by parameter 1L if Bit 0 is reset, or else head 01-0E, checking the CE cylinder for a defect-free test track. Skip Control words are written, simulating defects in full track writes of record 1 count and data fields. Five cases are tested.

All cases orient on index and space to segment 34, followed by various writes of record 1 count and data fields. After each write, an unoriented address mark search is performed, and the data is read, verifying that index is received following the last segment read. The track will be reformatted with the original Home Address and a standard Record Zero (no key field and a data field equal to eight bytes of zeroes) at test completion.

- Case 1 -- Move count field seven times
- Case 2 -- Move data field seven times
- Case 3 -- Split data of 320 bytes, following by seven skips and then the remaining 47 156 bytes
- Case 4 -- Split data of 320 bytes, followed by four skips and then another 320 bytes followed by three skips and then the remaining 46 836 bytes
- Case 5 -- Split data of 320 bytes, followed by six skips and then 47 136 bytes followed by one skip and then the remaining 20 bytes.

Reformatting may be attempted in the event of a detected error situation.

ROUTINE C88 -- FORCE WRITE/PADDING ERRORS

Class: Diagnostic

Linking: From C87; to C92

Parameters: None

This routine forces write and padding errors by attempting to write up to, and over, index.

Reformatting will be attempted in the event of a detected error situation and at routine completion.

NOTE

This routine will destroy the Home Address area on the CE cylinder for the track tested. Do not attempt to execute this routine until routine C87 executes error-free.

ROUTINE C88, TEST 1 -- FORCE WRITE/PADDING ERRORS

This test seeks to the CE cylinder and verifies the access position. Heads 0 through E are then scanned for the first defect-free track. If a defect-free track is not found and the linked series is not being executed, error C881FE will be posted. If executing the linked series, this test will be skipped.

A Write Overrun is forced by spacing up to index and writing over index via a diagnostic macro. Padding errors are forced by spacing over the Home Address and using a diagnostic macro to initiate a pad operation. This pad sequence is stopped and R/W mode is held until index.

ROUTINE C90 -- PACK SCAN

Class: Utility

Linking: Not Linked

Parameters: 1H - Test option; default=00

- Bit 0=Scan single track only
- Bit 1=Immediate error reporting
- Bit 2=Read HA and R0 fields only
- Bits 3-7=Not Used

1L - Head number (00-0E); default=00. Used only by single track option.

2 - Starting cylinder (0000-0376); default=0376

3 - Ending cylinder (0000-0376); default=0376. Not used with single-track option.

This routine checks for correct format and ECC bytes. It may be performed on a single track, any range of starting and ending cylinders, or all cylinders. The starting cylinder must be less than, or equal to, the ending cylinder; except for the

single-track option, where only the starting cylinder is used. For a single cylinder, the starting and ending cylinders must be equal.

- With immediate error reporting active, failure data is reported immediately following each read failure. If more than one track has been selected, the test continues with the next head when the test is restarted.

- Selecting single track option forces immediate error reporting.

- With immediate error reporting inactive, only the physical addresses of the failing tracks are reported. While scanning, the physical addresses of the first 15 failing tracks are collected in an error log. When all requested tracks have been scanned, the test completes and failing addresses are reported as standard SEWs 2 through 16.

- In default mode, errors other than those associated with read operations (C9012X) cause the routine to abort, without reporting any of the failing track data already collected.

- Default mode scans all heads and all fields of the CE cylinder.

- When a read failure occurs with single track option selected, the failure is reported and the inline terminates. In all other cases, summary error codes C90132 (0-14 failures) or C90130 (15 or more failures) are reported at routine completion. SEW 1L contains the low byte of the number of failures that occurred and should be verified as equalling 00 when routine ends. SEWs 2 through 16 contain the physical address of any track(s) causing a failure.

NOTE

Due to the time required to perform a Pack Scan, run it with the test device offline. Concurrent operation of the test device may not be desirable.

ROUTINE C92 -- TRACK REFORMAT

Class: Utility

Linking: From C88; last routine in linked series. Links to C80 if loop linked series is selected.

Parameters: 1H - Test options; default=04

- Bits 0-2=Not used
- Bit 3=Reformat entire logical device (Password CE must also be entered)
- Bit 4=Not used
- Bit 5=CE cylinder
- Bits 6 and 7=Not used

NOTE

If Bits 3 and 5 are both reset, reformat single track.

Loop on test and link routine run options are disabled if full pack reformat is selected.

1L - High cylinder address; default=03

2H - Low cylinder address; default=76

2L - Head number (00-0E); default=00

3H - Password; default=00 (reformat single track if format errors are found)

5D=Forced reformat 1. Reformat single track if access position is verified.

BF=Forced reformat 2. Reformat single track even if access position is not verified.

CE=Allow full pack reformat (Bit 3 of parameter 1H must also be set)

3L - Not Used

CAUTION

This routine could cause destruction of customer data if it is not used properly. It restores a track to its factory-shipped condition, unflagging all tracks flagged in the field as defective. If full pack reformat is chosen, the device involved should be placed offline before execution begins.

Before any reformatting is done, ensure that the HDA has been spinning for a minimum of one-half hour to stabilize the HDA.

This routine is normally run at the end of the linked series of routines to clean up the CE cylinder at the end of testing. It then runs in default mode, which reformats all tracks on the CE cylinder.

When this routine is run by itself (unlinked), it may be used to reformat any single track, the CE cylinder, or the entire logical device.

When called, the routine first reads the Home Address of the desired track from the Home Address Cylinder (HAC) to use in reformatting the desired track. This copy represents the Home Address field at the time of field shipment. It then attempts to read Home Address and Record Zero of the desired track, checking for format errors. If a format error is found, or if CE cylinder or full pack reformat were selected, the track is formatted unconditionally, writing a Home Address and a standard Record Zero (no key field, data field equals 8 bytes of zeros), based on the Home Address from the HAC, then padding until Index. Home Address and Record Zero are then read to verify a successful reformat.

If single-track reformat was selected, a password is used in deciding whether or not to reformat a track. Three possibilities exist:

Password	Reformat Decision Selected
00	Reformat track only if bad format found, and only if access position can be verified. This is the default option.
5D	Reformat track regardless of format found, but only if access position can be verified. This option is used if a reformat is desired following a C92234 error.

Password	Reformat Decision Selected
BF	Reformat track regardless of format found, even if access position cannot be verified. This option is used if a reformat is desired following a C92236 error.

When attempting a single-track reformat in default mode, a good track (no format errors found) is not reformatted. A bad track (format errors found) is reformatted only if the correct access position can be verified.

If no format errors are found during a test read, error C92234 is reported. If format errors were found, but the access position could not be verified, error C92236 is reported. Both conditions can be overridden and a reformat forced by using the appropriate password.

When this routine is used to reformat the entire logical unit (HDA), all tracks are reformatted unconditionally with Home Addresses read from the HAC. To reformat the entire HDA parameter 1H, Bit 3 must be set and password parameter 3H must contain CE.

NOTE

After a full pack reformat, routine C90 should be run with parameters 0000, 0000, 0376 and then checked for no errors found (SEW 1L=00) to verify that pack reformat was successful.

ROUTINE C93 -- FORCE DEVICE AVAILABLE FOR INLINE ROUTINES

Class: Utility

Linking: Not Linked

Parameters: 1H - Test number (1-2); default=00

This routine consists of two tests, both ending with an error code. The first test reads the functional tables in data memory, and if connected to a DPSE controller, the functional tables in the DPSE array. Device status 1 is also sensed. Test 2 forces the functional tables to values that will allow inline access to the desired device and resets any busy indica-

tion from the device, as indicated by sense device status 1 Bit 6. The test then senses the same information reported in test 1.

NOTE

Only test 1 runs in default mode. Test 2 must be selected using parameter 1H.

CAUTION

Test 2 must not be run with the device online as functional operations will be impacted.

ROUTINE C93, TEST 1 -- SENSE FUNCTIONAL TABLES

This test senses the functional, and if connected to a DPSE controller, the DPSE functional available tables. Device status 1 is also sensed. This test ends with expected failure code C931FF.

ROUTINE C93, TEST 2 -- FORCE DEVICE AVAILABLE FOR INLINES

CAUTION

This test must not be run with the device online as functional operations will be impacted.

This test forces the functional, and if connected to a DPSE controller, the DPSE functional available tables clear for inline execution to the test device. Any device busy indication sensed via sense device status 1 Bit 6 is reset. The test then senses the tables and status as reported by test 1 to verify that the tables and status were forced as desired. This test ends with expected failure code C932EE.

ROUTINE C94 -- READ/WRITE DPSE ARRAY

Class: Utility

Linking: Not Linked

Parameters: 1H - Test number (1-2); default=00

1L - Password; default=00
CE=Allow test 2 execution

This routine reads and/or writes the entire DPSE array, ending with expected error code C94XFF. After the DPSE array has been read, it can be displayed on the terminal.

This routine should only be run from a terminal as the maintenance panel cannot display the data read from the array. (See routine CA6 for DPSE array display to the maintenance panel.)

After either test has executed successfully, the DPSE array data read may be displayed on the terminal. Put the SD that executed the test into B memory mode (data memory, byte wide) by entering B/. Then use the D Utility command (Dump Memory) to dump array data from overlay data memory locations E800 through EFFF. This corresponds to DPSE array locations 000 through 7FF.

CAUTION

If the storage control DP cannot gain access to the overlay area in the SD that executed this routine, stopping the SD may be necessary. But this should not be done with the subsystem online as functional operations will be stopped. Try running this routine on the SD connected to the other controller before stopping this SD.

Display locations E800 through EFFF are filled with EE before the array is read and stored so that the failing address will be visibly apparent during an unexpected failure.

SD Byte Mode Address	DPSE Array Address
E800	000
E900	100
EA00	200
EB00	300
EC00	400
ED00	500
EE00	600
EF00	700

General comments on routine C94 execution:

- Extended Error Logging (EEL) should be disabled for the SD during execution of either test.
- Routine CA0, tests 1 through 3, must run error-free before running C94, test 1.
- Routines CA0/CA1 must run error-free before running C94, test 2
- For test 2, both storage directors and their devices must be varied offline as the full DPSE array is overwritten and then restored from the other controller. Both controllers must be powered on or the array will not be restored.
- Test 2 cannot be executed on both controllers at the same time or false error stops or the loss of original array data may occur.

ROUTINE C94, TEST 1 -- READ DPSE ARRAY

This test reads the DPSE array from locations 000 through 7FF and stores the data in overlay data memory locations E800 through EFFF. The DPSE array is not altered. The test ends with expected error code C941FF, indicating no errors reading the DPSE array. Data memory may now be dumped using the D utility command.

ROUTINE C94, TEST 2 -- WRITE/READ DPSE ARRAY

NOTE

To run this test, the password (CE) must be entered in parameter 1L.

This test writes into the DPSE array, filling it with a two-byte count. The full array is then read as in test 1, comparing the count read to verify that the data was written in the proper locations. On test completion, the array is restored by copying the array from the alternate controller. If the copy fails, the Array Initialized status bit is reset. The test ends with expected error code C942FF, indicating no errors reading the array. The array data written and read may now be dumped using the D utility command.

ROUTINE C95 -- SUBSYSTEM EXERCISER

Class: Utility

Linking: Not Linked

Parameters: 1H - Test options; default =00

- •Bit 0 Reset= All cylinders
- •Bit 0 Set= CE cylinder only
- •Bit 1 Reset= Random seeks
- •Bit 1 Set= Sequential seeks (Bit 0 must be reset)
- •Bit 2 Reset= Test all heads
- •Bit 2 Set= Use head in parameter 2H
- •Bit 3 Reset= Write and read (write on CE cylinder only)
- •Bit 3 Set= Read only
- •Bit 4 Reset= Read full track
- •Bit 4 set= Read Home Address and record zero only
- •Bit 5 Reset= Write key and data fields (CE cylinder only)
- •Bit 5 Set= Write data only (CE cylinder only)
- •Bit 6 Reset= Write random records of random length (CE cylinder only)
- •Bit 6 Set= Write one full track record zero data field; no key field (CE cylinder only)
- •Bit 7= Not used

1L - Not used

2H - Head number. If test option Bit 2 is set, range is 00 to 0E; default=00

2L - Write data pattern (CE cylinder only); default=00

- •00 = Worst case pattern (318C6318C6)
- •01 = Fixed pattern one (0001020408102040 80)
- •02 = Fixed pattern two (0003060C183060C0)
- •03 = Fixed pattern three (00FFAA55A55AF00F)
- •FF = Random data pattern

3 - Controller 0 test devices bit significant address (CE must enter)

4 - Controller 1 test devices bit significant address (CE must enter)

NOTE

The CE must enter parameters 3 and/or 4, using the following bit assignments:

3/4H, Bit 0=Device 0
3/4H, Bit 1=Device 1
3/4H, Bit 2=Device 2
3/4H, Bit 3=Device 3
3/4H, Bit 4=Device 4
3/4H, Bit 5=Device 5
3/4H, Bit 6=Device 6
3/4H, Bit 7=Device 7
3/4L, Bit 0=Device 8
3/4L, Bit 1=Device 9
3/4L, Bit 2=Device A
3/4L, Bit 3=Device B
3/4L, Bit 4=Device C
3/4L, Bit 5=Device D
3/4L, Bit 6=Device E
3/4L, Bit 7=Device F

This routine simulates functional activity to devices in a string or strings, checking for missing interrupts and problems due to noise and crosstalk. The inline linked series is as-

sumed to have executed error-free to all test devices. Parameters 3 and/or 4 must be entered to select the desired test devices. The device selected by routine 102 must be one of the test devices. Refer to SC Hardware Diagnostic Reference Manual (Publication Number 83324410) for routine 102 description and parameter values. The routine selects the controller or controllers, and verifies that no outstanding functional activity is present for the test devices, and then performs a rezero seek to each device.

- A display of C950 indicates that checks for functional activity are being performed.
- A display of C951 indicates that the routine is executing and no further checks for functional activity are performed at this time.

The routine executes the following operations to each test device, depending upon which device was accessed last and which devices have pending interrupts:

1. Rezero seek
2. Verify seek complete status
3. Sector search
4. Verify sector search status
5. Seek
6. Verify seek complete status
   - Steps 7-10 are repeated for all heads if test option Bit 2 is reset.
7. Read Home Address
8. Write multiple count/key/data fields (performed only if on the CE cylinder)
9. Read Home Address
10. Read multiple count/key/data fields

Restarting after an error results in error C95XFF, which reports the activity status received at the time of failure. Restarting after this display restarts the test. Error C95030 is reported if this routine is not run from the storage director maintenance panel. Default parameters execute random seeks, write worst-case data, and read full tracks (writing is done on the CE cylinder only).

If the desired test devices are shared via two DPSE controllers, only one of the controllers may be used to exercise the devices. This routine executes until you stop it or an error occurs.

CAUTION

All test devices must be offline to all paths. The storage director this routine is executed from is dedicated to this routine. Functional activity to this storage director or any devices connected to it is not allowed.

ROUTINE C95, TEST 0 -- INITIALIZATION

This test checks each test device for functional activity via tables in the storage director. If the controller has DPSE installed, the array tables are also checked. Each device is selected and checked for not busy status (50 command Bit 6 reset). If the test device is free, it is rezeroed and the checks repeated for the remaining test devices. No further checks for functional activity are performed after execution of this test. If functional activity is detected, this routine will not execute. For standalone configurations, routine C93 Test 2 may be necessary to force availability of some of the test devices (see description).

ROUTINE C95, TEST 1 -- SUBSYSTEM EXERCISER

This test performs the actual simulated functional activity as defined by the parameter entries. This test executes until you stop it or an error occurs. Run options are set by this test to loop on test.

ROUTINE C9F -- CONTINUOUS SEEK

Class: Utility

Linking: Not Linked

Parameters: 1 - Delay between strings; default = 0500 (1 minute)

2 - Delay between devices; default = 0020 (1 millisecond)

Delay Values

The delay values shown below apply if there is no contention with the functional microprogram, that is, if only standalones are being run.

0020 = 1 millisecond †
0280 = 0.5 minute
0500 = 1 minute
0780 = 1.5 minutes
0A00 = 2 minutes
0C80 = 2.5 minutes
0F00 = 3 minutes

† Delays of 0000→001F are not recommended.

This routine issues seeks to all unused devices connected to the SD with a delay of one minute between accessing strings (standalone time). If the device is busy, or if the access position was moved since the last check, then the device is skipped.

A seek to zero is performed, then a seek to cylinder 885, then seek back to zero, and then a seek back to the original cylinder.

This routine is invoked on a power up.

Patching locations 0F0D to 0000 and 0F10 to 0000 in data memory inhibit power-up execution and restarting after system resets or channel-initiated inlines.

Patching locations 0F0D to FFFF and 0F10 to 0804 in data memory enable power-up execution and restarting after system resets or channel-initiated inlines.

This routine may be selected the same as any other inline routine at either the SD or HSC. The run option byte should be set to 27 when selecting this routine.

This routine executes until stopped by pressing the command key or if a system reset occurs. If execution was from power-up, channel-initiated inlines will halt this routine, and restart the routine upon the completion of channel-initiated inlines.

Stop on error is inhibited by this routine.

ROUTINE CA0 -- MASTER DYNAMIC PATH SELECTION

Class: Diagnostic

Linking: From C80; to CA2

Parameters: 1H - Test number (1-D); default=00. (Tests executed depend upon running mode and if DPSE feature is installed.)

This routine checks the proper operation of the dynamic path selection extended (DPSE) logic. This routine consists of 13 tests.

- If the DPSE feature is not installed, only test 0 (initialization test) will execute.
- Tests 0-4 are executed with only one SD and are the only portion of the routine which is executed under default mode or when running the linked series.
- To execute tests 5-D, slave routine CA1 must first be executed.

When the slave displays E CA15, routine CA0 must be run with one of the following options:

- inhibit linking,
- loop routine, or
- loop on test.

Slave errors are reported to the master via the DPSE array. The master reports the error to the HSC maintenance panel. If the DPSE tests do not execute, the slave may be stopped with a communication error or timeout.

If the loop routine run option is invoked, the master (CA0 side) executes tests 0-C, then loops tests 1-C until stopped or an error occurs.

Test D is a standalone test; it is not linked from test C. Test D must be selected by parameter entry and when run, the test device must be offline to both HSCs.

If loop on test for tests 1-4 is desired, only routine CA0 should be executed as the slave (CA1 side) is not required.

If not in default mode and DPSE is not installed, the initialization test will execute and routine done will be displayed.

If in default mode and DPSE is not installed, the initialization test will execute and CA0 will link to routine CA2.

To run routines CA0 and CA1, refer to Additional Operating Procedures in section 3B for instructions.

ROUTINE CA0, TEST 0 -- INITIALIZATION

This test checks for the DPSE installed bit to be returned. If this bit is present, two bytes are read from the DPSE array locations 0401 and 0402. Then the Alternate Lock status is sensed. Failures from these two operations are checked via the DPSE Check-2 indications. If the DPSE feature is not installed, link to routine CA2.

ROUTINE CA0, TEST 1 -- SET/RESET DPSE LOCKS COMMAND

This test checks that the Set DPSE Locks and the Reset DPSE Locks commands are accepted by the controller by issuing the commands with 00 (no change) modifiers. Test 6 checks the actual setting and resetting of the DPSE locks.

ROUTINE CA0, TEST 2 -- SINGLE SD ARRAY R/W

This test checks the ability to write and read in the diagnostic portion of the DPSE array, starting at location 0401 for left controller (1) or location 0451 for right controller (2). Four 32-byte patterns are written and then read. Test 8 checks the shadow write and read of the full array.

Pattern 1 - 0F,5A,A5,F0,0F,5A,A5,F0, ...

Pattern 2 - 00,01,02,03,04,05,06,07, ...

Pattern 3 - 01,02,04,08,10,20,40,80, ...

Pattern 4 - 03,06,0C,18,30,60,C0,03, ...

ROUTINE CA0, TEST 3 -- SET/RESET UNDER MASK

This test checks for proper execution of the Set Under Mask and Reset Under Mask commands. A 32-byte block of the diagnostic area of the DPSE array is used for the checks. Thirty-two bytes of XX data are written, then the Set Under Mask or Reset Under Mask operation is performed on the value written for 32 bytes. The value received from the mask operation is compared to the expected value. Then the actual value in the array is read and compared to the expected data value.

Set Under Mask Checks			Reset Under Mask Checks		
Data	Mask	Expected	Data	Mask	Expected
00	FF	FF	FF	00	00
00	00	00	00	00	00
FF	FF	FF	FF	FF	FF
FF	00	FF	00	FF	FF
00	AA	AA	FF	AA	AA
00	55	55	FF	55	55
55	AA	FF	55	AA	00
AA	55	FF	AA	55	00
00	0F	0F	FF	0F	0F
00	F0	F0	FF	F0	F0
0F	F0	FF	0F	F0	00
F0	0F	FF	0F	0F	0F
			F0	0F	00
			F0	F0	F0

ROUTINE CA0, TEST 4 -- SINGLE SD CHECK-2

This test forces a DPSE Data Bus Parity Check-2 via a diagnostic macro. It tests for the correct response for the Check-2 in the fault log and that the Check-2 Bus In response is received with End Op. Those DPSE Check-2 errors requiring two storage directors to test are exercised by test 5.

ROUTINE CA0, TEST 5 -- DUAL SD CHECK-2

This test checks those DPSE Check-2 errors requiring two storage directors. The errors are forced using diagnostic macros on one or both controllers. Both controllers are required to be synchronized to perform the forcing of the errors and the following cleanup for each error. The Check-2 error is checked in the fault log on the controller receiving the error, and also that the Check-2 can be reset. The following Check-2 errors are tested: CDP12 Path Busy Parity error, DPSE Address Parity error, DPSE Lock Bus Check error, CDP Lock Bus Parity error, DPSE Memory Parity error, DPSE Alternate Controller error, and DPSE Data Compare error.

ROUTINE CA0, TEST 6 -- SET/RESET ARRAY LOCKS

This test checks that the array initialization response can be set and reset. This response is verified in the select response and in the other controller's Sense DPSE status response. The array update notification is set and the response is verified in the other controller's poll controller response. That controller then resets array update notification and checks the poll controller response for the array update notification response to be reset. Array locks 1 and 2 are set and reset in all combinations and verified that both controllers sense the correct status. All status is saved before testing is performed, and each controller attempts to restore that status at test completion or on an error exit.

ROUTINE CA0, TEST 7 -- COPY ARRAY

This test checks the proper execution of the shadow write and copy array operations. First the array is written and verified. Next the primary operation only logic is invoked and the array is written. With shadow write disabled, the array is written on one side only. The primary operation only logic is disabled and the array is copied from the other side. The data copied is then verified to be the original data written. All write operations are performed in the diagnostic area only.

ROUTINE CA0, TEST 8 -- MAIN ARRAY R/W

This test checks the proper execution of the shadow write and shadow read logic by reading and writing in the functional areas of the array. The array is tested in 128-byte blocks. Each block is read and saved by both master and slave sides. Testing is performed on that block, and the original data is restored. If a failure occurs, both controllers attempt to restore the original data.

ROUTINE CA0, TEST 9 -- DEVICE SELECTION

This test checks the DPSE device selection without actually selecting the device itself. Normal functional selection sequence is used, except only two of the three Sync Out/Sync In sequences in the selection are performed, followed by setting the interface back to the null disconnect. Controller 1 and 2 indications in the Sense DPSE status response are sensed and compared between the two controllers. The functional tables for the device specified by routine 102 are saved and replaced with a test pattern. Busy, Owed Device End, and Pack Change Interrupt bits in select response 2 DBI are verified to be set and reset at the proper times (as indicated by the bits in the array at location XX20 and the device selection status of the other controller). Unconditional Reserve is tested and the CCA indication is verified for the other controller in addition to the Busy response indication in the select response 2 DBI. Path Busy response is tested in the Read Alternate DPSE Lock Status response and in the Poll Path Busy response.

NOTE

Be sure that the same device address is entered for both controllers via routine 102. Refer to the SC Hardware Diagnostic Reference Manual (Publication 83324410) for routine 102 description and parameter values.

ARRAY XX20	left									right							
CHANNEL	A	B	C	D	E	F	G	H	*	A	B	C	D	E	F	G	H
AVAIL	1	0	0	0	0	1	0	0		1	0	0	0	0	0	0	0
ODE	0	0	1	0	0	1	0	0		0	0	1	0	0	0	0	0
PCH	0	0	0	1	0	1	0	0		0	0	0	1	0	0	0	0

ROUTINE CA0, TEST A -- SELECTION CONTENTION

This test checks the DPSE device selection contention logic without selecting the device itself. Normal functional selection sequence is used, except only two of the three Sync Out/ Sync In selection sequences are performed, followed by setting the interface back to null disconnect. Several near and simultaneous selections are performed from both sides of DPSE. Checks are made on each pass to verify that only one side successfully gains selection, as indicated by the Select Response 2 DBI.

ROUTINE CA0, TEST B -- R/W DEVICE PARAMETERS

This test verifies the proper execution of the read and write device parameters commands. The device parameter table for the device specified by routine 102 is saved, and replaced with a test pattern. Both sides then issue the Read and Write device parameters commands. The data written is verified by the Read DPSE array command. The device is selected as in test 9 to set the correct device in the controller sequencer register.

NOTE

Refer to the SC Hardware Diagnostic Reference Manual (Publication 83324410) for routine 102 description and parameter values.

ROUTINE CA0, TEST C -- CLEANUP COMMANDS

This test verifies the proper execution of the DPSE cleanup commands 1A and 1B. Four cases are tested.

ROUTINE CA0, TEST D -- DEVICE UNCONDITIONAL RELEASE

This test checks the unconditional release of the device. Test 9 only tests the controller's DPSE logic. In this test, the device is fully selected and an unconditional release is issued by the opposite HSC. After issuing the unconditional release,

the HSC selects the device to verify that the device can now be fully selected.

This test is a standalone test and is not linked with test C.

NOTE

Be sure that the same device address is entered for both controllers via routine 102.

The test device must be offline to both HSCs before executing this test.

ROUTINE CA1 -- SLAVE DYNAMIC PATH SELECTION

Class: Diagnostic, to be used with routine CA0 only

Linking: Not Linked

Parameters: None

This routine checks the proper operation of the dynamic path selection extended (DPSE) logic. This routine consists of 13 tests:

- Tests 0-4 are executed with only one SD.
- Tests 5-D are set up to execute with routine CA0 where routine CA1 is executed first. At Test 5, CA1 will wait for routine CA0 to be executed on the alternate side. The slave will then display E CA15 when it is waiting to synchronize with master routine CA0.

Errors for tests 5-D are reported to the master (CA0 side) with the exception of CA1X0X, CA1XFF, and CA1XFD errors, which are unexpected failures. The slave will report these errors on its own side as it is likely the reporting of errors via the DPSE array will fail.

Run options are valid only for the master (CA0 side).

If loop routine run option is invoked, the slave (CA1 side) loops routine on tests 5-C as indicated by the master (CA0 side).

Test D is a standalone test; it is not linked from test C. When test D is run, the test device must be offline to both HSCs.

Single test selection is done by parameter entry in routine CA0.

If DPSE is not installed and routine CA1 is attempted, only the initialization test will execute and error F CA1020 will be displayed.

To run routines CA0 and CA1, refer to Additional Operating Procedures in section 3B for instructions.

ROUTINE CA1, TEST 0 -- INITIALIZATION

This test checks for the DPSE installed bit to be returned from the sense features command before any other tests are allowed to execute.

ROUTINE CA1, TEST 1 -- SET/RESET DPSE LOCKS COMMAND

This test checks that the Set DPSE Locks and the Reset DPSE Locks commands are accepted by the controller by issuing the commands with 00 (no change) modifiers. Test 6 checks the actual setting and resetting of the DPSE locks.

ROUTINE CA1, TEST 2 -- SINGLE SD ARRAY R/W

This test checks the ability to write and read in the diagnostic portion of the DPSE array, starting at location 0401 for left controller (1) and location 0451 for right controller (2). Four 32-byte patterns are written and then read. Test 8 checks the shadow write and read of the functional areas of the DPSE array.

Pattern 1 - 0F,5A,A5,F0,0F,5A,A5,F0, ...

Pattern 2 - 00,01,02,03,04,05,06,07, ...

Pattern 3 - 01,02,04,08,10,20,40,80, ...

Pattern 4 - 03,06,0C,18,30,60,C0,03, ...

ROUTINE CA1, TEST 3 -- SET/RESET UNDER MASK

This test checks for proper execution of the Set Under Mask and Reset Under Mask commands. A 32-byte block of the diagnostic area of the DPSE array is used for the checks. Thirty-two bytes of XX data are written, then the Set Under Mask or Reset Under Mask operation is performed on the value written for 32

bytes. The value received from the mask operation is compared to the expected value. Then the actual value in the array is read and also compared to the expected data value.

Set Under Mask Checks			Reset Under Mask Checks		
Data	Mask	Expected	Data	Mask	Expected
00	FF	FF	FF	00	00
00	00	00	00	00	00
FF	FF	FF	FF	FF	FF
FF	00	FF	00	FF	FF
00	AA	AA	FF	AA	AA
00	55	55	FF	55	55
55	AA	FF	55	AA	00
AA	55	FF	AA	55	00
00	0F	0F	FF	0F	0F
00	F0	F0	FF	F0	F0
0F	F0	FF	0F	F0	00
F0	0F	FF	0F	0F	0F
			F0	0F	00
			F0	F0	F0

ROUTINE CA1, TEST 4 -- SINGLE SD CHECK-2

This test forces a DPSE Data Bus Parity Check-2 via a diagnostic macro. It tests for the correct response for the Check-2 in the fault log and that the Check-2 Bus In response is received with End Op. Those DPSE Check-2 errors requiring two storage directors to test are exercised by test 5.

ROUTINE CA1, TEST 5 -- DUAL SD CHECK-2

This test checks those DPSE Check-2 errors requiring two storage directors. The errors are forced using diagnostic macros on one or both controllers. Both controllers are required to be synchronized to perform the forcing of the errors and the following cleanup for each error. The Check-2 error is checked in the fault log on the controller receiving the error, and also that the Check-2 can be reset. The following Check-2 errors are tested: CDP12 Path Busy Parity error, DPSE Address Parity error, DPSE Lock Bus Check error, CDP Lock Bus Parity error, DPSE Memory Parity error, DPSE Alternate Controller error, and DPSE Data Compare error.

ROUTINE CA1, TEST 6 -- SET/RESET ARRAY LOCKS

This test checks that the array initialization response can be set and reset. This response is verified in the select response and in the other controller's Sense DPSE status response. The array update notification is set and the response is verified in the other controller's poll controller response. That controller then resets array update notification and checks the poll controller response for the array update notification response to be reset. Array locks 1 and 2 are set and reset in all combinations and verified that both controllers sense the correct status. All status is saved before testing is performed, and each controller attempts to restore that status at test completion or on an error exit.

ROUTINE CA1, TEST 7 -- COPY ARRAY

This test checks the proper execution of the shadow write and copy array operations. First the array is written and verified. Next the primary operation only logic is invoked and the array is written. With shadow write disabled, the array is written on one side only. The primary operation only logic is disabled and the array is copied from the other side. The data copied is then verified to be the original data written. All write operations are performed in the diagnostic area only.

ROUTINE CA1, TEST 8 -- MAIN ARRAY R/W

This test checks the proper execution of the shadow write and shadow read logic by reading and writing in the functional areas of the array. The array is tested in 128-byte blocks. Each block is read and saved by both master and slave sides. Testing is performed on that block, and the original data is restored. If a failure occurs, both controllers attempt to restore the original data.

ROUTINE CA1, TEST 9 -- DEVICE SELECTION

This test checks the DPSE device selection without actually selecting the device itself. Normal functional selection sequence is used, except only two of the three Sync Out/Sync In sequences in the selection are performed, followed by setting the interface back to the null disconnect. Controller 1 and 2 indications in the Sense DPSE status response are sensed and compared between the two controllers. The functional tables for the device specified by routine 102 are saved and replaced with a test pattern. Busy, Owed Device End, and Pack Change

Interrupt bits in select response 2 DBI are verified to be set and reset at the proper times (as indicated by the bits in the array at location XX20 and the device selection status of the other controller). Unconditional Reserve is tested and the CCA indication is verified for the other controller in addition to the Busy response indication in the select response 2 DBI. Path Busy response is tested in the Read Alternate DPSE Lock Status response and in the Poll Path Busy response.

NOTE

Be sure that the same device address is entered for both controllers via routine 102. Refer to the SC Hardware Diagnostic Reference Manual (Publication 83324410) for routine 102 description and parameter values.

ARRAY XX20	left									right							
CHANNEL	A	B	C	D	E	F	G	H	*	A	B	C	D	E	F	G	H
AVAIL	1	0	0	0	0	1	0	0		1	0	0	0	0	0	0	0
ODE	0	0	1	0	0	1	0	0		0	0	1	0	0	0	0	0
PCH	0	0	0	1	0	1	0	0		0	0	0	1	0	0	0	0

ROUTINE CA1, TEST A -- SELECTION CONTENTION

This test checks the DPSE device selection contention logic without selecting the device itself. Normal functional selection sequence is used, except only two of the three Sync Out/Sync In selection sequences are performed, followed by setting the interface back to null disconnect. Several near and simultaneous selections are performed from both sides of DPSE. Checks are made on each pass to verify that only one side successfully gains selection, as indicated by the Select Response 2 DBI.

ROUTINE CA1, TEST B -- R/W DEVICE PARAMETERS

This test verifies the proper execution of the read and write device parameters commands. The device parameter table for the device specified by routine 102 is saved, and replaced with a test pattern. Both sides then issue the Read and Write device parameters commands. The data written is verified by the Read

DPSE array command. The device is selected as in test 9 to set the correct device in the controller sequencer register.

NOTE

Refer to the SC Hardware Diagnostic Reference Manual (Publication 83324410) for routine 102 description and parameter values.

ROUTINE CA1, TEST C -- CLEANUP COMMANDS

This test verifies the proper execution of the DPSE cleanup commands 1A and 1B. Four cases are tested.

ROUTINE CA1, TEST D -- DEVICE UNCONDITIONAL RELEASE

This test checks the unconditional release of the device. Test 9 only tests the controller's DPSE logic. In this test, the device is fully selected and an unconditional release is issued by the opposite HSC. After issuing the unconditional release, the HSC selects the device to verify that the device can now be fully selected.

This test is a standalone test and is not linked with test C.

NOTE

Be sure that the same device address is entered for both controllers via routine 102.

The test device must be offline to both HSCs before executing this test.

ROUTINE CA2 -- DEVICE SELECTION LOGIC

Class: Diagnostic

Linking: From CA0; to C81

Parameters: None

This routine tests the port selection capability, the physical address switch, and performs the initial device selection.

ROUTINE CA6 -- COMMAND CYCLE

Class: Utility

Linking: Not Linked

Parameters: See table 2A-1

This routine allows the CE to build a test from the various subroutines contained in this routine. The desired command cycle is built by entering the desired subroutine(s) in the desired order in the routine parameter words. (A parameter word is two bytes.)

The command cycle may be ended in three ways:

1. Expected error display. Note: Only the last error display information will be displayed. For example, if subroutine 03XX and then later in the chain 05XX is used, the 05XX will be the information displayed.

2. End command cycle after one pass, subroutine 1400.

3. Loop command cycle, subroutine 0000.

The command cycle subroutines require one or two parameter words. If only one parameter word is defined, the second parameter word should not be entered. The next parameter word is the first parameter word for the next subroutine desired in the chain.

The total delay for delay X microseconds or delay X milliseconds must not exceed 25 milliseconds or functional operations will be impacted. However, if necessary, delays of 25 milliseconds can follow each other resulting in a total delay that will exceed the 25 millisecond limit. The delay limit should be exceeded only with the subsystem offline.

Checks are made for valid parameter entries. Invalid command cycle chains will result in CA610X errors or parameter entry errors.

Some command cycle routines contain expected error stops to display information. Some examples are:

- Subroutine 03XX contains error stop CA6133;
- Subroutine 0B00 contains error stop CA613B.

General comments on this routine are:

- All seeks or offsets must be preceded by a rezero seek.
- DPSE must be installed for DPSE operations.
- End of chain parameter 0000 is not required if all parameters are used, but looping still occurs if no errors are encountered.
- Default mode will select and deselect the controller; however, the first pass will select the device.
- Device select, controller select, poll device, or poll controller subroutines must be preceded by a deselect, if previously selected.

Refer to table 2A-1 for command cycle subroutines.

Three examples of command cycle programs are given below. Note that, in the first example, all of the parameter bytes are used -- so the End of Chain command (0000) is not needed.

Examples:

Parameter word	1	1900	Deselect controller
	2	0100	Select device
	3	0E00	Rezero seek
	4	0F80	Seek to CE cylinder 376 (hex)
	5	0376	
	6	1010	Offset forward 10 microinches
	7	1205	Read Home Address head 5
	8	0376	and display first half of Home Address

Response: Error CA6142 with Home Address field read as error bytes 2H through 15L.

• • •

Parameter word	1	1501	Write DPSE array location 0418
	2	0203	with 15 bytes of the pattern 010203 ... 010203
	3	1600	Rezero seek
	4	0418	Read 15 bytes from DPSE array location 0418
	5	0000	

Response: Error CA6146 with the 15 bytes read from DPSE array location 0418 as error bytes 1L through 8H.

• • •

Parameter word			
	1	1900	Deselect
	2	0600	RCC 1 sequence
	3	0100	Select device
	4	0243	Check Reset command
	5	0C00	Sense fault log and device status
	6	0000	

Response: Error CA613C with the fault log bytes and device status sensed as error bytes 2H through 8L.

TABLE 2A-1. COMMAND CYCLE SUBROUTINES

Parameter Word 1	Parameter Word 2	Description
0000		Loop at end of chain if no expected or unexpected errors occur.
0100		Select device.
02XX		Command XX no modifiers allowed.
03XX		Same as 02XX, but display command XX DBI in error byte 1L of error code CA6133. Valid commands for XX in 02XX/03XX: 09, 11, 12, 15, 16, 18, 19, 40, 43, 45, 4A, 4C, 4F, 50, 51, 53, 54, 55, 56, 57, 58, 5E, 5F, 5A
04XX	YY00	Command XX modifier YY.
05XX	YY00	Same as 04XX, but display command. XX DBI in error byte 1L of error code CA6135. Valid commands for XX in 04XX/05XX: 2A, 30, 31, 3A, 46, 47, 48, 62, 63.
0600		RCC 1 sequence. Display CCA bytes as error words 7 and 8 of error code CA6136.
0700		RCC 2 sequence. Display CCA bytes as error words 7 and 8 of error code CA6137.
0800		Hardware immediate.
0900	XXXX	Delay XXXX microseconds. XXXX equals 0000 through 61FF (hex).
0AXX		Delay XX milliseconds. XX equals 00 through 19 (hex).

Table Continued on Next Page

TABLE 2A-1. COMMAND CYCLE SUBROUTINES (Contd)

Parameter Word 1	Parameter Word 2	Description
0B00		Sense fault log bytes and display as error words 2, 3, and 4 of error code CA613B.
0C00		Sense fault log bytes and status command DBI values. Display fault log bytes in error words 2, 3, and 4 of error code CA613C. Display status command DBI values in error code CA613C as follows: • Error word 5 = CMD 50 and 51 DBI • Error word 6 = CMD 53 and 54 DBI • Error word 7 = CMD 55 and 56 DBI • Error word 8 = CMD 57 and 58 DBI
0D00		Reset command sequence. Commands 43 and 4A followed by a hardware immediate.
0E00		Rezero seek sequence.
0F80 0F00	ZZZZ ZZZZ	Seek sequence. 0F80=forward; 0F00=reverse; ZZZZ=number of tracks to seek-range=0000 to 0376.
10XX		Offset forward. XX values of 00, 10, 20, 30, 40, and 50 microinches are valid.
11XX		Offset reverse. XX values of 00, 10, 20, 30, 40, 50 microinches are valid.
12XX	ZZZZ	Read Home Address sequence. Display Home Address bytes as error bytes 2H to 15L of error code CA6142. XX=head 0-E; ZZZZ= physical cylinder address 0000-0376.

Table Continued on Next Page

TABLE 2A-1. COMMAND CYCLE SUBROUTINES (Contd)

Parameter Word		Description
1	2	
1400		End of chain and end routine, display D CA61.
15XX	YYZZ	Write DPSE array. Write 15 bytes of pattern XX, YY, ZZ starting at location 0418.
1600	ZZZZ	Read DPSE array. Read 15 bytes starting at location ZZZZ and display as error bytes 1L to 8H of error CA6146. ZZZZ range=0000 through 7FFF.
17MM	ZZZZ	Set under mask. Set under mask one byte at location ZZZZ. MM=mask; ZZZZ range= 0418 through 04FF.
18MM	ZZZZ	Reset under mask. Reset under mask one byte at location ZZZZ. MM=mask; ZZZZ range=0418 through 04FF.
1900		Deselect.
1A00		Select controller.
1B00		Poll device. Display poll response as error byte 1L of error code CA614B.
1C00		Poll controller. Display poll response as error byte 1L of error code CA614C.
1D00		Bypass expected error display and loop on chain at this point.

ROUTINE CA7 -- FSC/FRU GENERATOR/SENSE BYTE COLLECTION

Class: Utility

Linking: Not Linked

Parameters: 1H - Test number (1-4); default=01

1L - Not used

2 - XXX (Error Code/FSC); default=0000

- Test 1: Not used
- Test 2: Not used
- Test 3: XXXX=RRRT of error code RRRTMM
- Test 4: XXXX=Fault symptom code

3H - MM (Error code); default=00

- Test 1: Not used
- Test 2: Not used
- Test 3: MM=MM of error code RRRTMM
- Test 4: Not used

3L - Not used

This routine generates fault symptom codes, collects fault log bytes and device status, or displays the FRUs for an error code or fault symptom code.

General comments to this routine are:

- To display FRUs for an FSC or error code, the option byte must be in display FRUs mode 0X or 8X. See inline run options in section 3A.
- Restarting test 3 or 4 will produce an operator error.
- If the FSC or error code entered for test 3 or 4 cannot be found on the floppy disk, a load error will be displayed.

ROUTINE CA7, TEST 1 -- FSC GENERATION

This test attempts to generate a fault symptom code. This test is executed in default mode. The test ends with an expected error stop of CA71F8 with SEW 2 set to the FSC or 0000 if no fault symptom code could be generated.

ROUTINE CA7, TEST 2 -- FAULT LOG AND DEVICE STATUS

This test collects fault log bytes and device status for display. The test ends with an expected error stop of CA72FF.

ROUTINE CA7, TEST 3 -- REPORT FRUS FOR ERROR CODE

This test reports the FRUs for the desired error code as entered by parameters 2 and 3H. Test 3 ends with the failure display set to the error code entered in parameter 2 and 3H. The FRUs may then be displayed.

ROUTINE CA7, TEST 4 -- REPORT FRUS FOR FAULT SYMPTOM CODE

This test reports the FRUs for the desired fault symptom code as entered by parameter 2. Test 4 ends with the failure display set to F F8XXXX, where XXXX is the fault symptom code entered in parameter 2. The FRUs may then be displayed.

ROUTINE CA9 -- SEEK TIMING

Class: Utility

Linking: Not Linked

Parameters: 1H - Test number (1-A); default=00

1L - Head number (00-0E); default=head 00

This routine consists of 10 tests, each of which checks a specific seek length for correct timing. The total seek times for each test are averaged by the number of seeks in the test. The number of seeks in each test is fixed. Each seek time is measured from Busy to Seek Complete.

NOTE

Due to the amount of time this routine uses, run it with the test device offline.

ROUTINE CA9, TEST 1 -- 1-CYLINDER SEEKS

This test checks the average seek time of 1772_{10} 1-cylinder seeks and reports an error if the time is too long or too short. The test starts at cylinder 0, going sequentially forward to cylinder 886_{10}, then sequentially backward to cylin-

der 0. The access position is verified after each seek by reading Home Address. Minimum=1 millisecond; maximum=3.5 milliseconds.

ROUTINE CA9, TEST 2 -- 3-CYLINDER SEEKS

This test checks the average seek time of 590_{10} 3-cylinder seeks and reports an error if the time is too long or too short. The test starts at cylinder 0 and seeks sequentially forward, in 3-cylinder increments, to cylinder 885_{10}, then sequentially backward to cylinder 0. The access position is verified after each seek by reading Home Address. Minimum=3 milliseconds; maximum=27 milliseconds.

ROUTINE CA9, TEST 3 -- 9-CYLINDER SEEKS

This test checks the average seek time of 196_{10} 9-cylinder seeks and reports an error if the time is too long or too short. The test starts at cylinder 0 and seeks sequentially forward, in 9-cylinder increments, to cylinder 882_{10}, then backward to cylinder 0. The access position is verified after each seek by reading Home Address. Minimum=3 milliseconds; maximum=27 milliseconds.

ROUTINE CA9, TEST 4 -- 21-CYLINDER SEEKS

This test checks the average seek time of 84_{10} 21_{10}-cylinder seeks and reports an error if the time is too long or too short. The test starts at cylinder 0 and seeks sequentially forward, in 21_{10}-cylinder increments, to cylinder 882_{10}, then backward to cylinder 0. The access position is verified after each seek by reading Home Address. Minimum=3 milliseconds; maximum=27 milliseconds.

ROUTINE CA9, TEST 5 -- 52-CYLINDER SEEKS

This test checks the average seek time of 34_{10} 52_{10}-cylinder seeks and reports an error if the time is too long or too short. The test starts at cylinder 0 and seeks sequentially forward, in 52_{10}-cylinder increments, to cylinder 884_{10}, then backward to cylinder 0. The access position is verified after each seek by reading Home Address. Minimum=3 milliseconds; maximum=27 milliseconds.

ROUTINE CA9, TEST 6 -- 110-CYLINDER SEEKS

This test checks the average seek time of 16_{10} 110_{10}-cylinder seeks and reports an error if the time is too long or too short. The test starts at cylinder 0 and seeks sequentially forward, in 110_{10}-cylinder increments, to cylinder 880_{10}, then backward to cylinder 0. The access position is verified after each seek by reading Home Address. Minimum=3 milliseconds; maximum=27 milliseconds.

ROUTINE CA9, TEST 7 -- 221-CYLINDER SEEKS

This test checks the average seek time of 16_{10} 221_{10}-cylinder seeks and reports an error if the time is too long or too short. The test starts at cylinder 0 and seeks sequentially forward, in 221_{10}-cylinder increments, to cylinder 884_{10}, then backward to cylinder 0. This sequence is repeated two times. The access position is verified after each seek by reading Home Address. Minimum=3 milliseconds; maximum=27 milliseconds.

ROUTINE CA9, TEST 8 -- 295-CYLINDER SEEKS

This test checks the average seek time of 16_{10} 295_{10}-cylinder seeks and reports an error if the time is too long or too short. The test starts at cylinder 0 and seeks sequentially forward, in 295_{10}-cylinder increments, to cylinder 885_{10}, then backward to cylinder 0. The sequence is repeated until 16 seeks have been performed. The access position is verified after each seek by reading Home Address. Minimum=3 milliseconds; maximum=27 milliseconds.

ROUTINE CA9, TEST 9 -- 443-CYLINDER SEEKS

This test checks the average seek time of 16_{10} 443_{10}-cylinder seeks and reports an error if the time is too long or too short. The test starts at cylinder 0 and seeks sequentially forward, in 443_{10}-cylinder increments, to cylinder 886_{10} (CE cylinder), then sequentially backward to cylinder 0. This sequence is repeated four times. The access position is verified after each seek by reading Home Address. Minimum=3 milliseconds; maximum=27 milliseconds.

ROUTINE CA9, TEST A -- 886-CYLINDER SEEKS

This test checks the average seek time of 100_{10} 886_{10}-cylinder seeks and reports an error if the time is too long or too short. The test starts at cylinder 0 and seeks forward to cylinder 886_{10} (CE cylinder) and then backward to cylinder 0. This sequence is repeated 50 times. The access position is verified after each seek by reading Home Address. Minimum=3 milliseconds; maximum=30 milliseconds.

ROUTINE CAA -- INCREMENTAL SEEK

Class: Utility

Linking: Not Linked

Parameters: 1H - Not used

1L - Head number (00-0E); default=head 00

2 - Seek length (0000-0376); default=000F

This routine performs a series of incremental seek operations; first in the forward direction, until 256 (decimal) seeks have been performed, or until no more forward seeks are possible; then reverse seeks until cylinder 0 is reached. Access position is verified after each seek.

NOTE

Due to the amount of time this routine uses, run it with the test device offline.

ROUTINE CAB -- CYLINDER SEEK

Class: Utility

Linking: Not Linked

Parameters: 1H - Not used

1L - Head number (00-0E); default=head 00

2 - From cylinder (0000-0376); default=0010

3 - To cylinder (0000-0376); default=001F

This routine continuously seeks between two cylinders (from "From Cyl" to "To Cyl"). The access position is verified after each seek.

Sixteen seeks are performed between cylinders before an inline check is done. The test then restarts with a rezero seek and repeats the 16 seeks. This routine automatically runs in the loop on routine option. Use CMD (Q) key to stop routine execution.

ROUTINE CAC -- RANDOM SEEK

Class: Utility

Linking: Not Linked

Parameters: 1H - Not used

1L - Head number (00-0E); default=head 00

2 - Number of random seeks; default=0100

This routine performs a series of random seek operations. The number of random seeks to be performed is specified by parameter 2. A rezero seek is performed at the start and the end of this routine. The access position is verified after each seek.

NOTE

Due to the amount of time this routine uses, run it with the test device offline.

ROUTINE CAD -- OFFSET LIMITS

Class: Utility

Linking: Not Linked

Parameters: 1H - Not used

1L - Head number (00-0E); default=head 00

2 - Cylinder address (0000-0376); default=0376

This routine offsets 3.6 microinches of forward offset, then reads Home Address and checks for a good read of the Home Address field. It continues offsetting by 3.6 additional microinches and verifying correct PA bytes read until an error is returned when reading Home Address, indicating acceptable offset limits have been exceeded. The same procedure is followed using reverse offsets. The final results from each direction are used to calculate the average offset. This average describes the distance and direction from the nominal track position to the center of the track's bandwidth as determined by offset testing.

If either forward or reverse offsets reached the maximum value (226.8 microinches) without failure in reading the Home Address, normal completion code CAD132 is displayed. If neither offset reached the maximum value, completion code CAD130 is displayed.

SECTION 3

OPERATING PROCEDURES

OPERATING PROCEDURES 3

INTRODUCTION

This section is divided into subsections to provide operating procedures as follows:

- Section 3 - Contains descriptions of controls and indicators on the HSC operator panel, PCU, and dc power supply. Also describes controls and indicators on DSU PCU.
- Section 3A - Contains descriptions of maintenance panel switches and indicators. This maintenance panel is used with both the storage control and the HSC. Also contains detailed instructions for running inline diagnostics.
- Section 3B - Contains instructions for running inline diagnostics from a local/remote terminal.

HSC OPERATOR PANEL

The HSC operator panel contains all switches and indicators needed by the subsystem operator when using the HSC. The operator panel may also be required when running certain diagnostics. The panel is shown in figure 3-1 and described in table 3-1.

HSC PCU AND DC POWER SUPPLIES

The HSC PCU and dc power supplies control the application of power to the major logic assemblies in the HSC. The PCU and dc power supplies are shown in figure 3-2 and described in tables 3-2 and 3-3.

DSU PCU CONTROLS AND INDICATORS

The DSU has no operator control panel since all operations are initiated by the HSC. The DSU's PCU controls and indicators are located on the power control units inside the DSU. The PCU is shown in figure 3-3 and described in table 3-4.

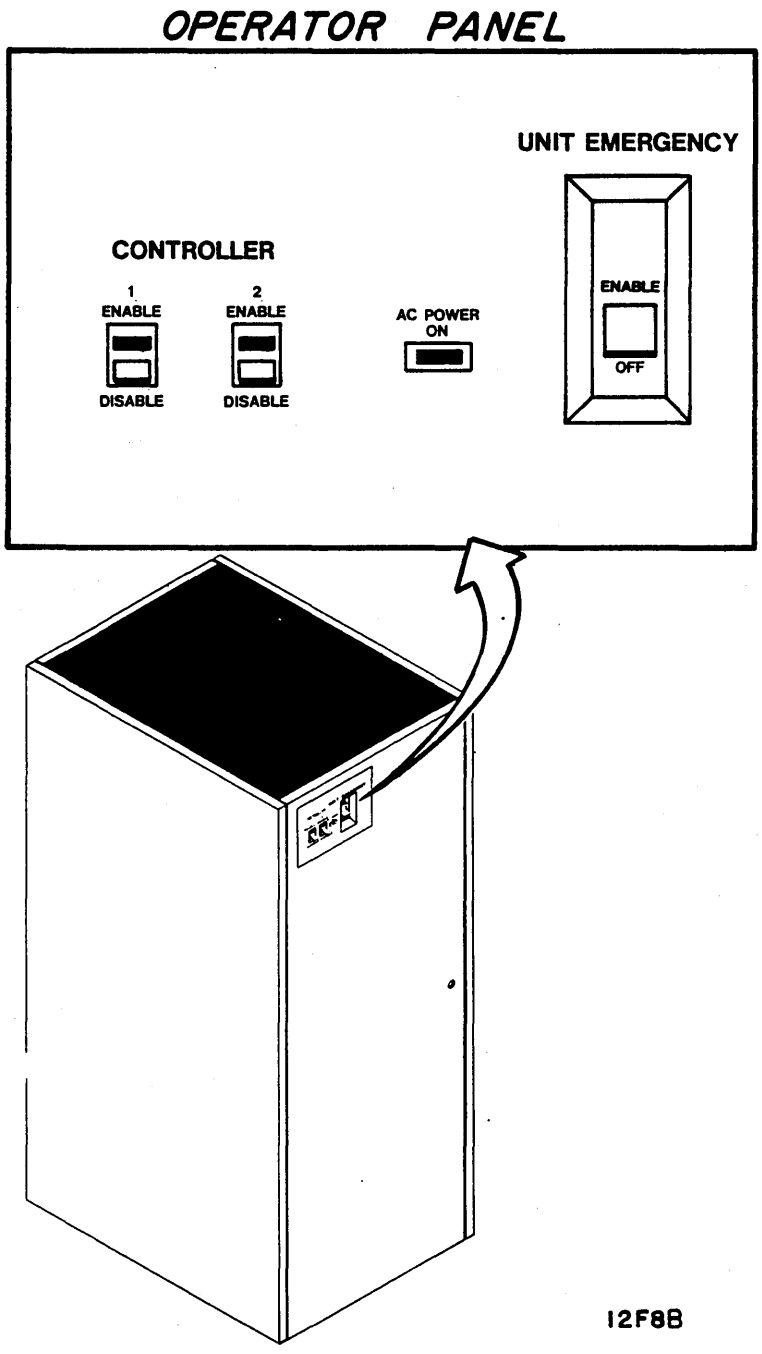
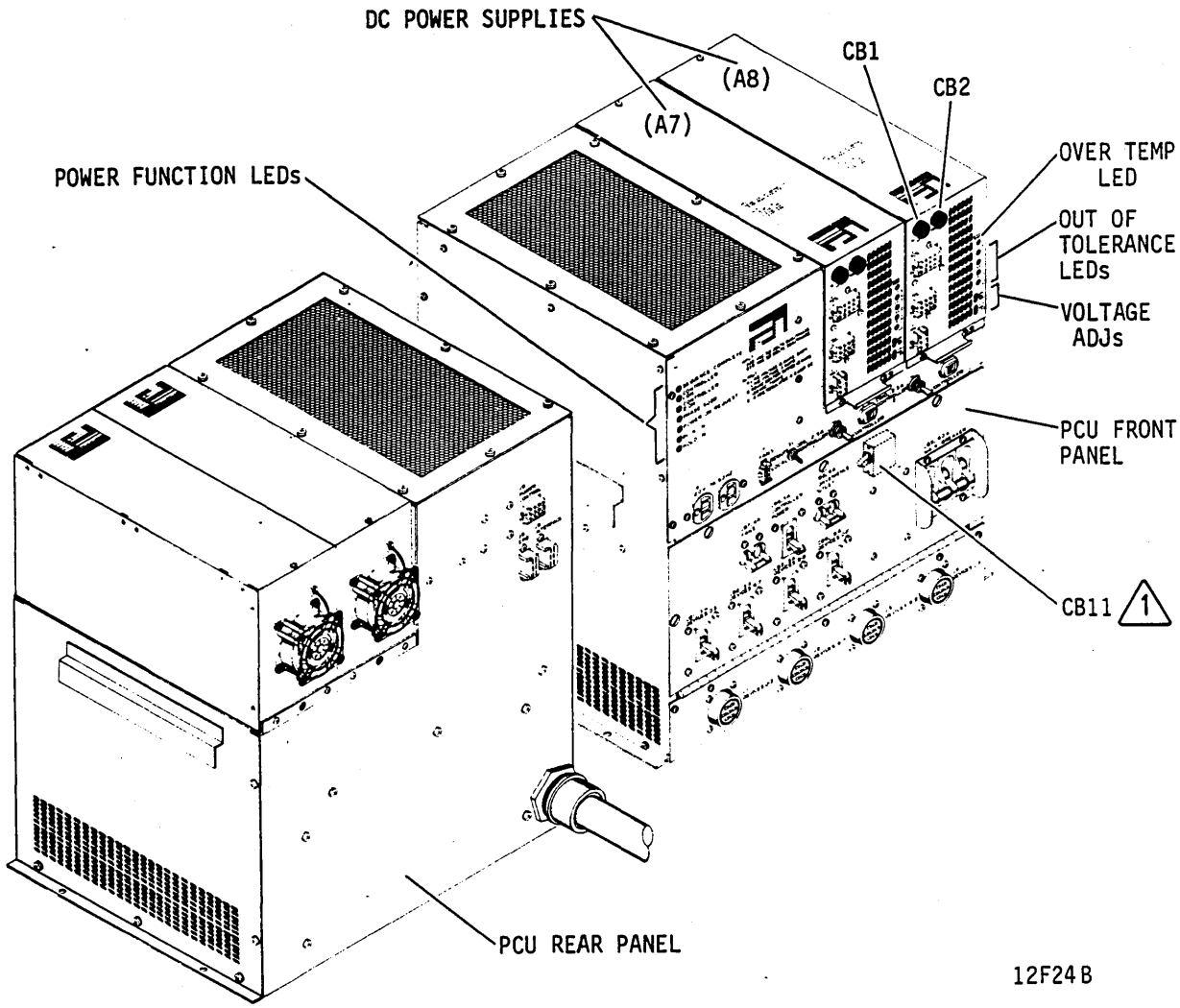


Figure 3-1. HSC Operator Panel

TABLE 3-1. HSC OPERATOR PANEL SWITCHES AND INDICATORS

Name	Type	Function
CONTROLLER 1 ENABLE/ DISABLE	Switch/LED indicator	Function of these two switches is identical except that one applies to one controller, the other to the second controller. In up position, respective controller interface is enabled and LED in switch lights. In down position, respective controller interface is disabled and LED goes out.
CONTROLLER 2 ENABLE/ DISABLE	Switch/LED indicator	
AC POWER ON	Green LED indicator	LED is on when power is applied to either controller.
UNIT EMERGENCY	Switch	Used to remove power immediately from all drives in the string; however, power to dc power supplies in the HSC remains on. **CAUTION** To avoid damaging drives, do not use this switch to power up or down a string of drives except for life-threatening emergencies.



NOTES:

1 CB11 LOCATED INSIDE; OPEN PCU FRONT PANEL FOR ACCESS

2 CONVENIENCE OUTLET USED ON 60 Hz UNITS ONLY

Figure 3-2. HSC PCU and DC Power Supply

TABLE 3-2. HSC PCU CONTROLS AND INDICATORS

Name	Type	Function
FRONT PANEL OF PCU		
PHASE GOOD	Green LED indicator	When on, indicates that AC phase rotation is correct.
CONTROLLER 2 ON	Green LED indicator	Indicates that power is applied to controller 2 within the HSC.
CONTROLLER 1 ON	Green LED indicator	Indicates that power is applied to controller 1 within the HSC.
POWER ON REQUEST	Green LED indicator	Indicates that either POR input is active.
PICK IN	Green LED indicator	Indicates when either of the Pick In signals is active
HOLD IN	Green LED indicator	Indicates when either of the Hold In signals is active
SEQUENCE COMPLETE	Green LED indicator	When on, indicates that power sequencing is complete and that Sequence Complete is being provided to the EPO interface.
J9 120 V 7A 60 Hz	Duplex receptacle	Provides a source of non-isolated 120 v ac, @ 7.5 amperes for external equipment (60-Hz units only).
S1 REMOTE/ LOCAL	Toggle switch	Used to select the source of power for power sequencing. In LOCAL (down) position, a start sequence is initiated by the PCU, provided the thermal switch on the logic
Table Continued on Next Page		

TABLE 3-2. HSC PCU CONTROLS AND INDICATORS (Contd)

Name	Type	Function
S1 REMOTE/ LOCAL (Contd)		chassis is closed and the UNIT EMERGENCY switch is on. In REMOTE (up) position, all LOCAL mode conditions must be satisfied and the Pick In and the Hold In signals from the storage director must be high to initiate a start sequence. (Pick In may be released after the power up begins.)
CB9, 15A CONTROLLER 1	Circuit breaker	In the 1 position (up) enables the PCU to supply ac power to the DC power supply module for controller 1.
P3 CONTROLLER 1	Connector	Provides output connection for ac power supplied by PCU to the DC power supply module for controller 1.
CB10, 15A CONTROLLER 2	Circuit breaker	In the 1 position (up) enables the PCU to supply ac power to the DC power supply module for controller 2.
P4 CONTROLLER 2	Connector	Provides output connection for ac power supplied by PCU to the DC power supply module for controller 2.
CB11, 15 A (AUX)		Located inside the PCU, this breaker provides a margin of safety for other PCU components. If it is not on, the fans will not run and power will not be supplied to the drives or to the dc power supplies.

Table Continued on Next Page

TABLE 3-2. HSC PCU CONTROLS AND INDICATORS (Contd)

Name	Type	Function
J7 FANS	Connector	Provides output connection for ac power supplied by PCU to air circulating fans.
CB7, 4A FANS	Circuit breaker	When closed, routes ac power to air circulating fans.
CB6, 15A CONTROLLER POWER	Circuit breaker	When closed, routes ac power to CONTROLLER 1 and 2 circuit breakers (CB9 and CB10) and to power sequence board A4A1.
CB8, 4A CONVENIENCE OUTLET	Circuit breaker	When closed allows convenience outlet, J9, to provide 120 V ac for external uses (on 60-Hz units only).
CB1, 20A DEVICES 0-3	Circuit breaker	When closed, applies ac power to devices 0 through 3 (drive 0)
CB2, 20A DEVICES 4-7	Circuit breaker	When closed, applies ac power to devices 4 through 7 (drive 1)
CB3, 20A DEVICES 8-B	Circuit breaker	When closed, applies ac power to devices 8 through B (drive 2)
CB4, 20A DEVICES C-F	Circuit breaker	When closed, applies ac power to devices C through F (drive 3)
CB5, 60A MAIN BREAKER	Circuit breaker	When closed, supplies the HSC with 3-phase power from the site source of power.

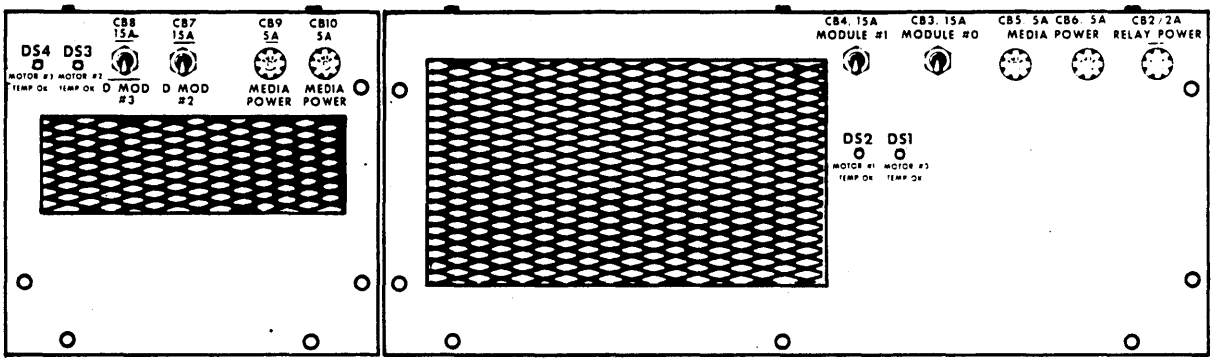
Table Continued on Next Page

TABLE 3-2. HSC PCU CONTROLS AND INDICATORS (Contd)

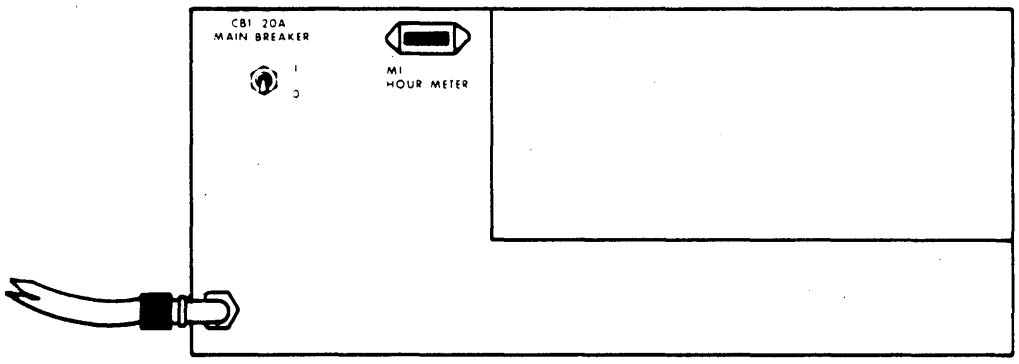
Name	Type	Function
J1 DEVICES 0-3	Connector	Used as the output connection for routing power to drive 1 (devices 0-3).
J2 DEVICES 4-7	Connector	Used as the output connection for routing power to drive 2 (devices 4-7).
J3 DEVICES 8-B	Connector	Used as the output connection for routing power to drive 3 (devices 8-B).
J4 DEVICES C-F	Connector	Used as the output connection for routing power to drive 4 (devices C-F).
REAR PANEL OF PCU		
J8 POWER CONTROL	Connector	Used for routing power sequencing signals between the logic and the PCU.
J5/J6 EPO INTERFACE	Connectors	Used for routing Emergency Power Off signals between HSC and the SCs connected to this HSC.

TABLE 3-3. HSC DC POWER SUPPLY CONTROLS AND INDICATORS

Name	Type	Function
CB1, +24V .5A CB2, -24V .5A	Circuit breaker Circuit breaker	Used for protecting the +24 and -24 volt circuits, respectively, in the dc power supplies.
J2 OUTPUT	Connector	Used to route dc supply's voltages to the logic chassis.
J1 LOGIC	Connector	Used to route and exchange power control signals between controller and dc power supply.
J3 INPUT	Connector	Used to route PCU power to the input of the dc supply.
OVER TEMP	Red LED indicator	Lights if an over temperature condition is reached in the power supply.
OUT OF TOLERANCE +14, +5, -5, -12	Four green LED indicators	If an out-of-voltage-tolerance occurs in any of these power supply voltages, the appropriate indicator lights.
+14V ADJ -12V +5V ADJ -5V	Four adjustable pots	These four potentiometers provide the means for adjusting the +14, -12, or ±5-volt circuits to bring their outputs back into tolerance.



SLAVE PCU MASTER PCU



MASTER PCU (REAR VIEW)

NOTES:

1. DS1-DS4 USED ON 50 Hz UNITS ONLY.

12C40

Figure 3-3. DSU PCU Controls and Indicators

TABLE 3-4. DSU PCU CONTROLS AND INDICATORS

Designator	Name	Function
M1	HOUR METER	Indicates accumulated power on time in hours. The indicator is active whenever power is applied and is located at the rear of the MPCU. Applies to older units only.
CB1	MAIN BREAKER	This circuit breaker applies main ac power to the DSU. The circuit breaker is on in the up position and off in the down position and is located at the rear of the MPCU.
CB2	RELAY POWER	This circuit breaker protects the main ac contactor and is located at the front of the MPCU. The center button protrudes from the breaker to indicate a tripped condition. The center button is flush with the body of the breaker in the normal (reset) condition.
CB3	MODULE 0	This circuit breaker applies low voltage ac to the dc power supply module for device 0. This circuit breaker is on in the up position, off in the down position, and is located at the front of the MPCU.
CB4	MODULE 1	Same as CB3 but for device 1.
CB5-CB6	MEDIA POWER	These circuit breakers protect the +10 V and -10 V media outputs that are shared by devices 0 and 1. These circuit breakers are located on the front of the MPCU. The center button protrudes to indicate a tripped condition.

Table Continued on Next Page

TABLE 3-4. DSU PCU CONTROLS AND INDICATORS (Contd)

Designator	Name	Function
CB7	MODULE 2	This circuit breaker applies low voltage ac to the dc power supply module for device 2. This circuit breaker is located at the front of the SPCU and is off in the down position and on in the up position.
CB8	MODULE 3	Same as CB7 but for device 3.
CB9-CB10	MEDIA POWER	These circuit breakers protect the +10 V and -10 V media outputs that are shared by devices 2 and 3. These circuit breakers are located at the front of the SPCU. The center button protrudes from the circuit breaker to indicate a tripped condition.
CB1-CB2	+24/-24	Each dc power supply module has two circuit breakers on its rear panel. These circuit breakers protect the +24 V and -24 V output respectively. The center button protrudes from the circuit breaker to indicate a tripped condition.
DS1-DS4	MOTOR TEMP OK	These indicators are provided on 50-Hz units only. When lit, the associated drive motor is connected and the motor thermostat is closed. When off, the motor is disconnected or an overtemperature condition exists. Indicators DS1 and DS2 are located on the master PCU and pertain to devices 0 and 1 respectively. DS2 and DS3 are located on the slave PCU and pertain to devices 2 and 3 respectively.

MISCELLANEOUS SWITCHES AND INDICATORS

There are several switches and indicators located in the controller and device that you will be required to use under certain conditions. Tables 3-5 and 3-6 describe the location and use of the switches and indicators for the controller and device, respectively.

TABLE 3-5. CONTROLLER MISCELLANEOUS SWITCHES/INDICATORS

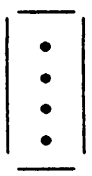
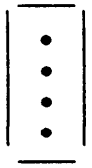
Switch/Indicator	Location	Use
STATUS indicators	On _SLX board 	These indicators provide visual indications of various status conditions. See diagram below. Select Power on sequence complete (PSC) Not Used Not Used
Controller ID switches	On _SLX board	These eight switches identify the controller to the storage control. Refer to the subsystem installation manual for setup procedure.
STATUS indicators	On _SJX board 	These indicators provide visual indications of various status conditions. See diagrams below. Check-1 Check-2 Not Used Not Used
Trace Enable/ DPSE switches	On _SJX board	The upper seven switches are used to set the trace address for troubleshooting. The bottom switch is used to indicate that DPSE is installed. This switch is set to ON when two controllers are installed in the HSC.

TABLE 3-6. DEVICE MISCELLANEOUS SWITCHES/INDICATORS

Switch/Indicator	Location	Use
MPU ERROR indicator	On _MKX board	Indicates MPU hardware fault during initial self-test.
STATUS indicators	On _SCX board	These 12 indicators provide visual indications of various status conditions. See diagrams below. R/W Check Access Check RPS Check Error Flag Device Check Voltage Check Clock Check Port Check Selected Busy Ready On-Line
POWER ON/OFF switch	On _SDX board	Three-position, center-off switch that provides local control of motor power. Up position turns motor on and down position turns motor off.
Device Select switches	On _SFX board	These four switches provide each device with a unique selection code. Refer to subsystem installation manual for setup procedure.

SECTION 3A

MAINTENANCE PANEL OPERATING PROCEDURES

INTRODUCTION

The maintenance panel is a removable storage control panel that contains a display, keys, and indicators needed to maintain and troubleshoot the storage control, controller, and device. The panel may be disconnected from the storage control and attached to the HSC to maintain and troubleshoot at the HSC level. Figure 3A-1 illustrates the panel; table 3A-1 describes its functions.

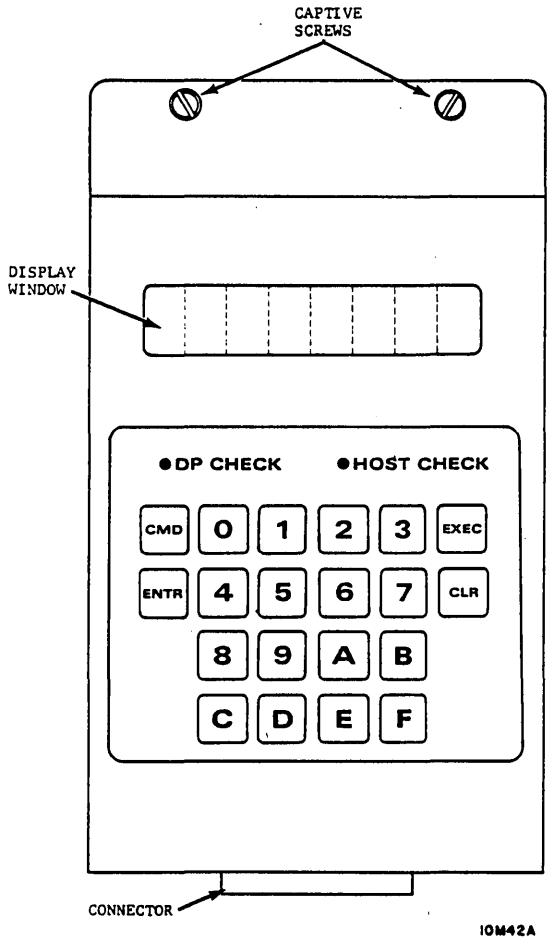


Figure 3A-1. Maintenance Panel

TABLE 3A-1. MAINTENANCE PANEL SWITCHES AND INDICATORS

DISPLAY AREA (TOP)
The 8-character display has three formats. The meaning and use of the formats will be explained as they are encountered.

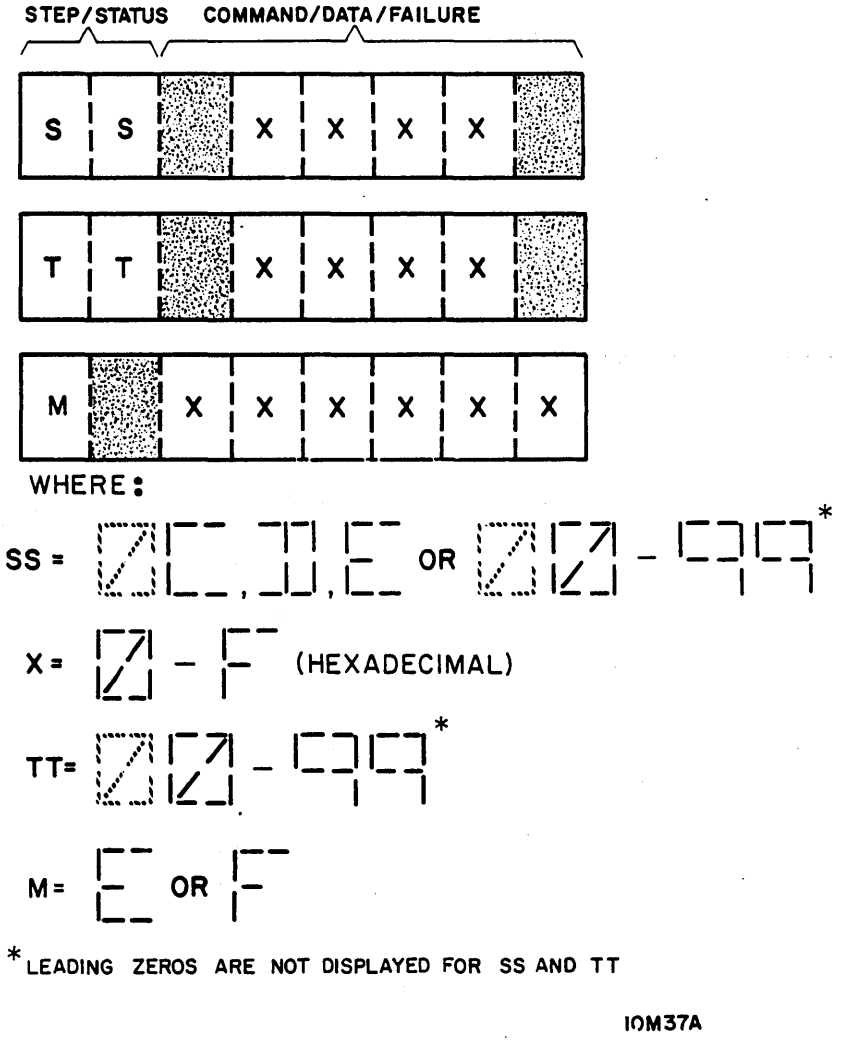


Table Continued on Next Page

TABLE 3A-1. MAINTENANCE PANEL SWITCHES AND INDICATORS (Contd)

KEYPAD AREA (BOTTOM)		
Key/Indicator	Legend	Function
Hexadecimal Keys	0-F	Used to enter commands or data. Pressing one of these keys after having pressed either CMD or ENTR clears the display and enters the key's value in the rightmost window of the display. Pressing another key shifts the display left one position and displays the newest value.
Command Key	CMD	Interrupts the currently executing routine, if any, and allows the operator to enter another command or additional data.
Enter Key	ENTR	Store run options/parameters for routine execution; step through stored options/parameters; step through stored information.
Execute Key	EXEC	Executes the last command stored by the ENTR key.
Clear Key	CLR	Clears the display and allows reentry of desired information.
Table Continued on Next Page		

TABLE 3A-1. MAINTENANCE PANEL SWITCHES AND INDICATORS (Contd)

Key/Indicator	Legend	Function
DP CHECK Indicator		Signifies that a hardware failure has been detected in the DP logic by the DP's self-testing hardware and software. During power-up, the indicator is initially lit by DP hardware. If DP ROM and RAM tests run without error, the indicator is turned off until an error is detected in the remaining hardcore diagnostics.
HOST CHECK Indicator		Hardware or microcode detected check condition has been detected in SD1 or SD2. Not used when maintenance panel is connected to the HSC.

PROCEDURES AND PRECAUTIONS FOR MAINTAINING DISK SUBSYSTEMS WITH DPSE FEATURE

When an operating system that supports Dynamic Path Selection Extended (DPSE) is IPLed, it creates arrays in the controllers. These arrays define paths that the system has to each of the devices. This allows the SD to take a reserve command and, instead of allowing access to the device over only this one path, it allows access over all the paths that the issuing system has to the device (system wide reserve). After an IPL, the following actions ensure that the DPSE arrays and the operating system are updated to reflect the current configuration:

- A vary path command to put a path offline/online
- A vary channel command to put a channel offline/online
- A vary device command to put a device offline/online

This makes the DPSE arrays a valuable communication link between controller and SD for devices having two accesses. Any action that causes a reset to the SD interface causes the SD to remove this interface from the group (in the DPSE array) that this interface belongs to. All of the following actions cause a reset, but not necessarily a problem:

- System IPL-- operating system creates the DPSE arrays (groups) during IPL
- System Reset
- Disabling a channel on the SD operator panel
- IMLing the SD
- Switching a channel interface via a switching device

To keep the operating system in synchronization with the DPSE arrays, a strict procedure must be followed when any of the above resets are performed.

The procedure if <u>not</u> doing an IPL is:

- At the CPU, vary path/channel/device offline.
- Perform any of the necessary reset actions (except IPL).
- At the CPU, vary path/channel/device online.

IPL establishes new DPSE arrays to include all equipments that are enabled at the time of the IPL. Ensure that all equipments that are to be used are enabled. If equipment is to be added after the IPL, it must be enabled and then varied online at the CPU. This will update the DPSE arrays.

Some indications of having not followed the procedure are:

- Slowdown of system throughput or,
- Busy Allocated Reserve (A-BSY-R) indications in the UCB for devices, followed by a system message 1GF9901 (Device End Missing for Device xxx), followed by system message 1GF996E (Probable Device Failure, cannot Initiate I/O to xxx) or,
- System hangs.

If the procedure is not followed and problems occur, perform the appropriate vary offline command, followed by a vary online command, in an attempt to reestablish the DPSE arrays. However, trying to reestablish the DPSE arrays after they are out of sync may not recover all outstanding operations.

If a full recovery cannot be made using the vary command, an IPL must be performed. Remember to enable all equipments that are to be included in the DPSE arrays before the IPL is performed.

If recabling at the channel or DDC interface has been done and the above procedure does not recover (including IPL), the HSC must be powered off and on to clear the DPSE arrays. Then the system can be IPLed.

COMMAND ENTRY

When a diagnostic routine is to be run the order of entry is: CMD RRRT EXEC. RRR is the desired routine and T is set to zero. A routine may contain up to 16 (0-F) individual tests and are selected with a parameter entry (see table 3A-4). When execution starts, E RRRT is displayed. If run options are set so that routine linking is used, RRR and T are updated as each routine/test is executed. When execution is complete, D RRRT is displayed, where RRRT is the last routine/test executed and D indicates routine is done.

RUN OPTION ENTRY

All diagnostic and support routines execute subject to preset conditions known as run options. Run options allow you to specify actions to be taken when a diagnostic or support routine completes execution or detects an error. These actions include stopping/looping on a normal completion/error or going on to the next test/routine. These actions may be specified for a linked series of routines, a single routine, or a test within a routine.

Run options are not changed when routines are loaded, so run options are carried from one routine to the next.

To enter, change, or examine a run option, the order of entry is: CMD RRRT ENTR. After ENTR is pressed, a 0 is displayed in the status display and the run option is displayed in the least significant byte of the command/data/failure display. The most significant byte shows controller/device address.

The run option displayed may be changed by entering a new one byte run option. Following the display and optional entry of a new option byte, do one of the following:

- Press ENTR to store the new option byte, increment the status display from 0 to 1, and display parameter 1.

or

- Press EXEC to store the new option byte and execute the routine/test entered during CMD entry.

Table 3A-2 defines the run option bits within the run option byte.

By using table 3A-2, you can create a run option byte to control diagnostic routines. Some examples are:

- 00 = Run the linked series and stop. If an error occurs, stop and display normal FRU list when error information is displayed.

- A6 = Run a single routine and loop that routine. If an error occurs, stop and display error information (not FRUs). Bit 0 is ignored because Bit 2 is set.

INLINE RUN OPTION BIT 0

Bit 0 controls normal/extended FRU display. Normal FRUs have the highest probability of fixing a problem and are displayed when Bit 0 is reset. Extended FRUs have a lower probability of fixing a problem and are displayed when Bit 0 is set. Normal FRUs should be done before extended FRUs.

INLINE RUN OPTION BIT 2

Bit 2 controls FRU display and error/message display. When Bit 2 is reset, the FRU list called out by Bit 0 is displayed. When Bit 2 is set, error or message bytes are displayed and Bit 0 is ignored.

TABLE 3A-2. INLINE RUN OPTION BITS

Bit	Definition
MSB 0	0 = Normal FRU display. 1 = Extended FRU display.
1	Not Used.
2	0 = Display FRU list. 1 = Display error/message bytes.
3	Not Used.
4	Not Used.
5	0 = Run linked series. 1 = Run single routine.
6	0 = Stop at end of routine or linked series. 1 = Loop at end of routine or linked series.
7 LSB	0 = Stop on error. 1 = Continue on error; Display error code.

INLINE RUN OPTION BIT 5

Bit 5 controls routine linking. When Bit 5 is reset, the linked series is run, starting with the routine entered and going to the last routine in the linked series. When the last routine is done, the setting of run option Bit 6 determines if execution stops or if the linked series is looped. When Bit 5 is set, only the routine entered is run. The setting of run option Bit 6 determines if execution stops or if the single routine is looped.

The routines link in the following sequence:

C80 → CA0 → CA2 → C81 → C82 → C83 → C84 → C85 → C86 →
C87 → C88 → C92

INLINE RUN OPTION BIT 6

Bit 6 controls routine looping. When Bit 6 is reset, execution stops at the end of a routine or linked series. When Bit 6 is set, the selected routine or linked series will loop indefinitely. When the last routine of the linked series is done, it loops back to routine C80. This process continues until an error occurs or CMD is pressed.

INLINE RUN OPTION BIT 7

Bit 7 controls stop on error. When Bit 7 is reset, execution stops when an error occurs. When Bit 7 is set, execution continues on error with the error code displayed. This process continues until CMD is pressed. The display is maintained until some condition occurs that requires a display change, such as:

- A different error is detected.
- A new routine or test is started.

FRUs and SEWs are not available when run on error is selected and an error occurs.

PARAMETERS

Parameters provide control information to diagnostic and utility routines. Parameters specify such things as test selection and R/W test patterns.

The number of parameters vary depending on the routine. Most routines provide default parameter values that allow parameter entry to be bypassed.

To examine or change parameters the entry sequence is: CMD RRRT ENTR ENTR. The first ENTR displays the run options (status display = 0). The second ENTR displays the first parameter in command/data/failure display, with status display = 1. If the parameter is to be changed, use the keyboard and enter the new parameter. All four digits must be entered. If additional parameters are to be examined/changed, pressing ENTR steps through the parameters until the last parameter is displayed, at which time the display returns to the run option display (status display = 0). This sequence repeats until you press EXEC or CMD.

It is not necessary to examine or change all parameters once the sequence is started. Pressing EXEC ends the sequence and starts routine/test execution.

MAINTENANCE/FAILURE MESSAGES

Maintenance and failure messages provide information on the condition of routines as they are being loaded or executed. See table 3A-3.

When CMD is pressed, C is displayed in step/status. Command/data/failure displays the last routine/test executed (RRRT). A different routine/test may now be entered using CMD entry or the displayed routine/test may be run by pressing EXEC.

D displayed in step/status indicates routine/test RRRT is done.

E displayed in step/status indicates routine/test RRRT is executing. When run option Bit 7 is set (continue on error) and an error is detected, E is displayed along with error code RRRTMM.

TABLE 3A-3. MAINTENANCE/FAILURE MESSAGE FORMATS

Step/Status Display	Command/Data/Failure Display
C	R R R T
D	R R R T
E	R R R T
F or E	R R R T M M
0	K K P P
1	A S N N or XXXX
2	A S N N or XXXX
↓	↓ ↓ ↓ ↓ ↓
n	A S N N or XXXX

Where:

C - CMD has been pressed.
D - Routine done.
E - Routine executing or an error occurred with loop on error set (run option Bit 7 set).
F - Error has occurred.
n - The number of FRUs or SEWs for a particular failure code.
RRR - Routine number.
T - Test number.
MM - Failure code.
KK - Selected SD.
PP - Run option.
ASNN - 4 digit FRU code if run option Bit 2 is reset.
XXXX - 4 digit SEW if run option Bit 2 is set.

F displayed in step/status indicates an error has been detected and execution stopped. Command/data/failure display indicates the routine/test that failed and error code (RRRTMM).

- To continue execution, press EXEC.
- To display additional information about the error, press ENTR.

When you press ENTR, the step/status display shows 0 and command/data/failure display shows KKPP. When ENTR is pressed again, step/status display increments to 1 and command/data/failure displays the first FRU or SEW, depending on the setting of run option Bit 2.

- With run option Bit 2 reset, FRUs are displayed (ASNN).
- With run option Bit 2 set, SEWs are displayed (XXXX).

When ENTR is pressed again, step/status increments to 2 and command/data/failure displays the second FRU or SEW. The step/status display increments with each pressing of ENTR until the last FRU or SEW is displayed. When the last FRU or SEW is displayed, the step/status display changes to 0 and the sequence starts over. EXEC may be pressed at any time to resume execution or CMD pressed to begin a new routine or test.

ATTACHING MAINTENANCE PANEL TO HSC

The inline diagnostics may be run with the maintenance panel attached to the storage control or with the maintenance panel attached to the HSC. Use the following procedure to attach the maintenance panel to the HSC.

1. Remove the panel from the storage control by loosening the two captive screws holding it to the power panel and lift it up to disengage the connectors.
2. Open the HSC rear door and place maintenance panel in the bracket located in the upper right corner. Tighten the two captive screws to hold panel in place. Refer to figure 3A-2.
3. Attach one end of the maintenance panel round cable (part number 73164620) to the connector on the bottom of the maintenance panel. Refer to figure 3A-2.

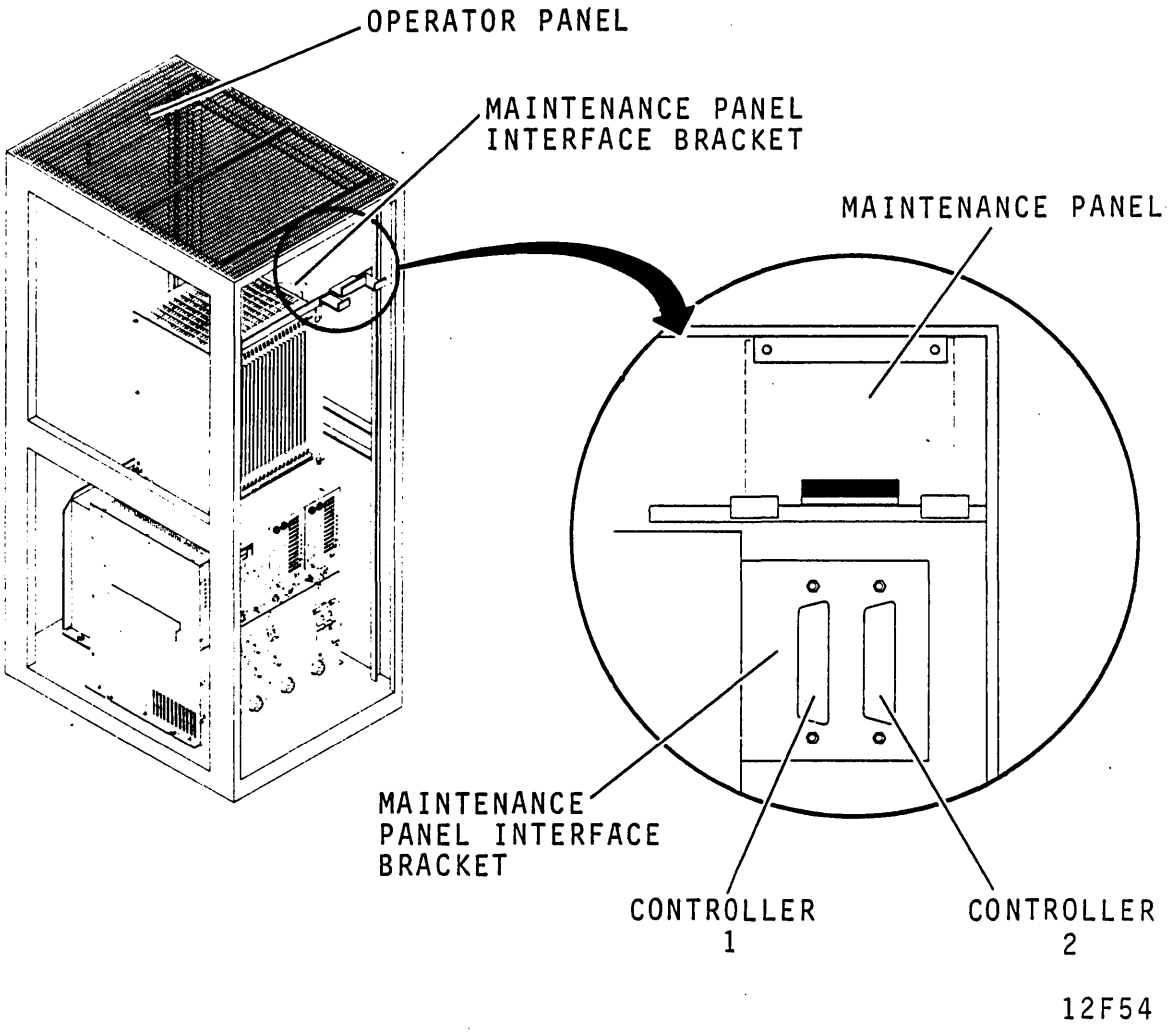


Figure 3A-2. Maintenance Panel Attachment

4. Attach the other end of the cable to one of the connectors on the maintenance panel interface bracket. Left connector for controller 1 or right connector for controller 2. Refer to figure 3A-2.

INLINE OPERATING PROCEDURE

During inline routine execution, routines/tests may appear to hang or not execute. When this happens, it is very difficult to identify what occurred. Several actions are listed below to attempt to identify the cause of the problem:

- Suspect the maintenance panel and/or the cables attaching the maintenance panel to the DP or HSC. Ensure all cable connectors are properly attached and tight.

- With the DP and SD assumed to be good, perform the following HSC FRUs in the order given:

  → 1053

  → 1005

  → 1006

  → 1008

  → 1250

  → 1550

  → 1004.

- When running inlines from the HSC, and if the subsystem seems to hang or inlines not execute, move the maintenance panel from the HSC to the storage control. A status or error display at the SD indicates a probable communication problem between the SD and controller. Run diagnostics on the SD to check the maintenance panel and communication between the SD and maintenance panel. Then run diagnostics on the controller/device to check communications between the SD and controller. If no problems are encountered, move the maintenance panel to the HSC and run diagnostics on the controller/device from the controller.

This is a basic operating procedure that applies to most inline routines. Some routines require manual intervention and/or special operating procedures. Any such difference from the basic operating procedure has an additional operating procedure. Refer to Additional Operating Procedures, section 3B, for the following routines:

- CA0
- CA1

You can use this procedure when running inlines from either the maintenance panel or the terminal. The maintenance panel may

be mounted in the storage control or attached to the HSC. The terminal must be in panel mode to run inline diagnostics. When this procedure is used on a terminal, the equivalent terminal key is given after the maintenance panel key. Example: CMD(Q).

1. Set the RTA switch (storage control operator panel) to level 1.

2. Select SD and/or controller/device to be tested by running routine/test 102 1 as follows:

   a. Press CMD(Q) Key.

      - Display = C RRRT. Because this is the start of testing, RRRT is unknown. Normally it is the last routine/test run.

   b. Enter 1021 and press ENTR(S) key.

      - Display = 0 XXXX, where XX is don't care.

   c. Press ENTR(S) key.

      - Display = 1 XXXX, parameter 1.

   d. This step varies depending on where inline diagnostics are controlled.

      - If inline diagnostics are run from the storage control, enter 1 or 2 to select the SD to be used for testing.

      - If inline diagnostics are run from the HSC, enter the system address of the HSC and device to be tested.

   e. Press ENTR(S) key.

      - Display = 2 XXXX, parameter 2.

   f. This step varies depending on where inline diagnostics are controlled.

      - If inline diagnostics are run from the storage control, enter system address of HSC and device to be tested.

      - If inline diagnostics are run from the HSC, parameter 2 is not used. Go to next step.

g. Press EXEC(X) key to start routine execution.

- Display = E 1021, changing to D 1021 when routine is done.

3. Run routine BFF.

4. Press CMD(Q) key.

- Display = C RRRT, indicates last routine/test run.

5. Enter desired inline routine/test number using the format RRRT, where RRR is the routine and T is set to zero. Go to next step if displayed RRRT equals desired routine/test.

6. Press ENTR(S) key.

- Display = 0 KKPP, where KK is the address of the currently selected controller and device at the DDC interface (Bit 2=controller and Bits 4-7=device) and PP is the current run option. To change the run option, continue at next step. To use current run option, continue at step 6b.

a. Refer to table 3A-2, Inline Run Option Bits, to generate a new run option. Enter the new run option.

b. Press ENTR(S) key.

- Display = 0 KKPP Parameter entry not allowed.

or

1 XXXX Default parameter 1.

7. If parameter entry is not allowed or default parameters are acceptable, continue at step 9. If parameters are to be entered, continue at next step.

8. Refer to table 3A-4 for routines and their parameters. Enter the desired parameter(s) and press ENTR(S) key. Repeat this step for each parameter entered.

NOTE

The display changes to 0 KKPP when all parameters have been entered.

9. Press EXEC(X) key to start routine execution.

   - Display = E RRRT, indicates routine/test RRRT is running.

10. One of four displays indicate an end condition:

    - Display = D RRRT: indicates successful completion of routine RRR, test T. To load a new routine/test go to step 4 and continue. To end inline testing, go to step 11 and continue.

    - Display = C RRRT: indicates CMD(Q) key was pressed to stop routine RRR, test T execution. To load a new routine, go to step 5 and continue. To end inline testing, go to step 11 and continue.

    - Display = F RRRTMM: indicates a failure occurred in routine RRR, test T, producing error code MM. Display FRUs and/or SEWs as follows:

      a. Press ENTR(S) key. Display = 0 KKPP, where KK is the address of the selected controller and device at the DDC interface (Bit 2=controller and Bits 4-7=device) and PP is the run option.

      NOTE

      Bit 2 of PP determines FRU or SEW display:

      Bit 2=0 . . . . display FRUs
      Bit 2=1 . . . . display SEWs

      b. Change run option if FRU/SEW selection is not the desired one. Press ENTR(S) key.

      - Display = 0 KKPP: No FRUs/SEWs available, change run option bit 2.

        or

      - Display = 1 XXXX: First FRU or SEW. Step/Status increments each time ENTR(S) is pressed, displaying the next FRU/SEW. The display returns to 0 KKPP when all FRUs/SEWs have been displayed.

c. Press EXEC(X) key to continue routine/test execution or CMD(Q) key to load a new routine/test.

- Display = E RRRTMM: indicates a dynamic error display. A failure occurred in routine RRR, test T, producing error code MM, while run on error option was selected. Press CMD(Q) key to stop execution. If (after pressing CMD(Q) key) display=C RRRT, then FRUs/SEWs are not available in this situation. Routine CA7, test 2, may be run to get FRUs or the routines run option may be changed to stop on error to get FRUs/SEWs.

  → To change run options, go to step 6 and continue.

  → To load a new routine, go to step 5 and continue.

  → To end inline testing, go to step 11 and continue.

11. End inline testing as follows:

    a. Run routine BFF.

    b. Run routine BFA.

NOTE

Do not perform step 11c if inlines were run from a maintenance panel attached to the HSC. Go to step 11d.

    c. Press CMD(Q), CLR(Z), and EXEC(X) keys.

    d. Set RTA switch (storage control operator panel) to 0.

TABLE 3A-4. INLINE ROUTINE PARAMETERS

Routine	Parameter	Default Value	Meaning	Range Available
ALL	0		Run Options	See table 3A-2
C80	1H	00	Test Number	01 thru 03
	1L		Not Used	
C81	1H	00	Test Number	01 thru 0A
	1L		Not Used	
C82	1H	00	Test Number	01 thru 0C
	1L	00	Head Number	00 thru 0E
	2H	80	Test mode - tests 5 & 6 only	80= Test all heads, ignore parameter 1L 00= Test only head specified in parameter 1L
	2L		Not Used	
C83	1H	00	Test Number	01 thru 04
	1L		Not Used	

Table Continued on Next Page

TABLE 3A-4. INLINE ROUTINE PARAMETERS (Contd)

Routine	Parameter	Default Value	Meaning	Range Available
C84	1H	00	Test Number	01 thru 08
	1L	00	Head Number	00 thru 0E
C85	1H	00	Test Number	01 thru 05
	1L	80	Head Number	80= Test all heads; 00 thru 0E=head number
	2H	00	R/W Option	00= Write and read once 80= Write once, loop on read 40= Loop write C0= Loop write
	2L		Not Used	
	3H 3L 4H 4L 5H	31 8C 63 18 C6	Parameters 3H thru 5H are Tests 2 & 3 W/R pattern	00 00 00 00 00 thru FF FF FF FF FF
	5L		Not Used	
C86	1H	00	Test Number	01 thru 05
	1L	00	Head Number	00 thru 0E

Table Continued on Next Page

TABLE 3A-4. INLINE ROUTINE PARAMETERS (Contd)

Routine	Parameter	Default Value	Meaning	Range Available
C87	1H	00	Test Number	01 and 02
	1L	80	Head Number	80= Scan heads 01-0E; Use first defect-free head 00= Use head specified in Bits 4-7 as defect-free head.
C90	1H	00	Test Option	80=Scan single track 40=Inhibit error logging 20=Read HA and R0 only 00=Scan all tracks with error logging
	1L	00	Head Number	00 thru 0E
	2	0376	Starting Cylinder	0000 thru 0376
	3	0376	Ending Cylinder	0000 thru 0376

Table Continued on Next Page

TABLE 3A-4. INLINE ROUTINE PARAMETERS (Contd)

Routine	Parameter	Default Value	Meaning	Range Available
C92	1H	04	Test Option	Bits 0-2=Not used Bit 3=Reformat entire HDA Bit 4=Not used Bit 5=CE cylinder Bit 6=Not used Bit 7=3380 mode
	1L	03	High Cylinder Address	00 thru 03
	2H	76	Low Cylinder Address	00 thru 76
	2L	00	Head Number	00 thru 0E
	3H	00	Password	00=Reformat single track if errors found 5D=Reformat track if position verified BF=Reformat track if position not verified CE=Allow full pack reformat
	3L		Not Used	

Table Continued on Next Page

TABLE 3A-4. INLINE ROUTINE PARAMETERS (Contd)

Routine	Parameter	Default Value	Meaning	Range Available
C93	1H	00	Test Number	01 and 02 NOTE Only test 1 runs in default. Test 2 must be run offline.
C94	1H 1L	00 00	Test Number Password	01 and 02 CE= Allow test 2 execution
C95	1H	00	Test Options	Bit 0: all cylinders Reset Bit 0: CE cylinder Set only Bit 1: Random seeks Reset Bit 1: Sequential Set seeks (Bit 0 must be reset) Bit 2: Test all heads Reset Bit 2: Use head in Set parameter 2H

Table Continued on Next Page

TABLE 3A-4. INLINE ROUTINE PARAMETERS (Contd)

Routine	Parameter	Default Value	Meaning	Range Available
C95 (Contd)	1H		Test Options (Contd)	Bit 3: Write and read Reset (write on CE cylinder only) Bit 3: Read only Set Bit 4: Read full track Reset Bit 4: Read HA and R0 Set only Bit 5: Write key and Reset data fields (CE cylinder) Bit 5: Write data (CE Set cylinder) Bit 6: Write random Reset records of random length (CE cylinder) Bit 6: Write one full Set track Record Zero data field (CE cylinder)
	1L		Not Used	
	2H	00	Head Number	00 thru 0E with Bit 2 set
Table Continued on Next Page				

TABLE 3A-4. INLINE ROUTINE PARAMETERS (Contd)

Routine	Parameter	Default Value	Meaning	Range Available
C95 (Contd)	2L	00	Write Data Pattern	00= Worst case pattern; pattern= 318C6318C6 01= Fixed pattern one Pattern= 0001020408102040 80 02= Fixed pattern two Pattern= 0003060C183060C0 03= Fixed pattern three; Pattern= 00FFAA55A55AF00F FF= Random data pattern
	3	None	CTLR 0 Test Device(s) Bit Significant Address	The CE must enter parameters 3 and/or 4, using the following bit assignments:
	4	None	CTLR 1 Test Devices(s) Bit Significant Address	3/4H, Bit 0=Device 0 3/4H, Bit 1=Device 1 3/4H, Bit 2=Device 2 3/4H, Bit 3=Device 3 3/4H, Bit 4=Device 4 3/4H, Bit 5=Device 5 3/4H, Bit 6=Device 6 3/4H, Bit 7=Device 7 3/4L, Bit 0=Device 8 3/4L, Bit 1=Device 9 3/4L, Bit 2=Device A 3/4L, Bit 3=Device B 3/4L, Bit 4=Device C 3/4L, Bit 5=Device D 3/4L, Bit 6=Device E 3/4L, Bit 7=Device F

Table Continued on Next Page

TABLE 3A-4. INLINE ROUTINE PARAMETERS (Contd)

Routine	Parameter	Default Value	Meaning	Range Available
C9F	1	0500	Delay between strings	Delay Values 0020 = 1 ms 0280 = 0.5 min 0500 = 1.0 min 0780 = 1.5 min 0A00 = 2.0 min 0C80 = 2.5 min 0F00 = 3.0 min
	2	0020	Delay between devices	
CA0	1H	00	Test Number	01 thru 0D
	1L		Not Used	
CA1	1H	00	Test Number	01 thru 0D
	1L		Not Used	
CA6	Refer to Routine Description			
CA7	1H	01	Test Number	01 - 04
	1L		Not Used	
	2	0000	Error Code/ FSC	Test 1= Not Used Test 2= Not Used Test 3= RRRT of error code RRRTMM Test 4= FSC

Table Continued on Next Page

TABLE 3A-4. INLINE ROUTINE PARAMETERS (Contd)

Routine	Parameter	Default Value	Meaning	Range Available
CA7 (Contd)	3H	00	Error Code	Test 1= Not Used Test 2= Not Used Test 3= MM of error code RRRTMM Test 4= Not Used
	3L		Not Used	
CA9	1H	00	Test Number	01 thru 0A
	1L	00	Head Number	00 thru 0E
CAA	1H		Not Used	
	1L	00	Head Number	01 thru 0E
	2	000F	Seek Length	0000 thru 0376
CAB	1H		Not Used	
	1L	00	Head Number	00 thru 0E
	2	0010	From cylinder	0000 thru 0376
	3	001F	To cylinder	0000 thru 0376

Table Continued on Next Page

TABLE 3A-4. INLINE ROUTINE PARAMETERS (Contd)

Routine	Parameter	Default Value	Meaning	Range Available
CAC	1H		Not Used	
	1L	00	Head Number	00 thru 0E
	2	0100	Number of Random Seeks	0001 thru FFFF
CAD	1H		Not Used	
	1L	00	Head Number	00 thru 0E
	2	0376	Cylinder Address	0000 thru 0376

SECTION 3B

ADDITIONAL OPERATING PROCEDURES

ADDITIONAL OPERATING PROCEDURES 3B

INTRODUCTION

Some routines require operating procedures in addition to, or in place of, the standalone operating procedure. These additional operating procedures are given here.

Routine descriptions list the procedure(s) required to execute the routine.

ROUTINES CA0 AND CA1 -- DYNAMIC PATH SELECTION

Make sure to read routine CA0 and CA1 descriptions before attempting to run them.

NOTE

When running CA0 and CA1, first attach the maintenance panel to the HSC. See procedure in section 3A for Attaching Maintenance Panel to HSC.

1. Attach the maintenance panel to controller 2 of the HSC.
2. Use the inline operating procedure to load and execute routine CA1. For test purposes, this path will be called the slave side.

NOTE

If controller 2 is not the slave, some FRU codes will indicate the correct board but the wrong controller.

3. A slave display of E CA15 indicates that the slave is waiting to synchronize with routine CA0.

NOTE

CAXXFF timeout errors while trying to synchronize can be bypassed by executing routine BFE prior to executing CA0/CA1.

4. Disconnect the maintenance panel from controller 2 and attach it to controller 1 of the same HSC.

5. Use the inline operating procedure to load and execute routine CA0. For test purposes, this path will be called the master side.

   When routine CA0 is being loaded, one of the following run options must be entered:

   - Inhibit linking,
   - Loop routine, or
   - Loop test

   NOTE

   If CA0 and CA1 or be stopped, both sides must be stopped. To restart routines CA0 and CA1, return to step 1. When run to completion, CA0 will stop, but CA1 will be in an idle loop.

6. End testing as follows:

   a. Attach maintenance panel to controller 1, if not already attached.

   b. Run routine BFF.

   c. Run routine BFA.

   NOTE

   Do not perform step 6d if routines were run from a maintenance panel attached to the HSC. Go to step 6e.

   d. Press CMD(Q), CLR(Z), and EXEC(X) keys.

   e. Set RTA switch (SC operator panel) to 0.

   f. Disconnect maintenance panel from controller 1 and attach it to controller 2.

   g. Run routine BFF.

h. Run routine BFA.

NOTE

Do not perform step 6i if routines were run from a maintenance panel attached to the HSC. Go to step 6j.

i. Press CMD(Q), CLR(Z), and EXEC(X) keys.

j. Set RTA switch (SC operator panel) to 0.

SECTION 4

TERMINAL OPERATING PROCEDURES

TERMINAL OPERATING PROCEDURES 4

INTRODUCTION

This section applies only if the HSC is attached to a storage control that has terminal capabilities.

The inline diagnostics may be run from the local and/or remote terminal that is attached to the storage control. For information on local/remote terminals, refer to the storage control Hardware Diagnostic Reference Manual (Publication 83324410).

RUNNING INLINES FROM A TERMINAL

Use the following procedure to run inlines from either the local or remote terminal:

1. Attach local and/or remote terminal to the storage control. Refer to the storage control Hardware Diagnostic Reference Manual, section 4, for procedure.

2. Put local and/or remote terminal into panel mode. Refer to the storage control Hardware Diagnostic Reference Manual, section 4, for procedure.

3. When the terminal is in panel mode, use the standard Inline Operating Procedure, section 3A of this manual, to run inlines. The following terminal-maintenance panel key relationships must be used:

Maintenance panel key	Use terminal key:
CMD	Q
ENTR	S
EXEC	X
CLR	Z
1-9	1-9
A-F	A-F

NOTE

When in panel mode, all local and remote terminal keys, other than those listed, are ignored.

4. Go to maintenance panel inline operation procedure, section 3A of this manual, to run inline diagnostics.

5. To take the terminal out of panel mode and end inline testing, refer to the last step of Panel Mode Operating Procedure in the storage control Hardware Diagnostic Reference Manual.

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