60458110

CONTROL DATA

CPU, CM, IOU MAINTENANCE REGISTERS

CODES BOOKLET

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PREFACE

This maintenance register codes booklet provides bit descriptions of all maintenance registers for the CONTROL DATA® CYBER 170 Computer Systems, Models 815, 825, 835, 845, and 855, the CDC® CYBER 180 Computer Systems, Models 810, 830, 835, 840, 845, 850, 855, 860, 990, and the CDC CYBER 840S, 845S, 855S, 840A, 850A, 860A, 870A, 990E, 992, 994, and 995E Computer Systems.

The systems publication index following the preface lists the hardware reference manuals that are applicable to the computer systems listed above.

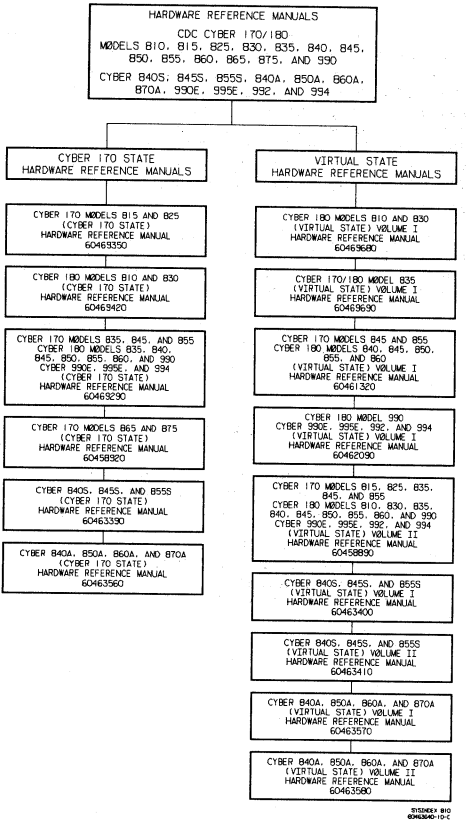
Refer to the Literature and Distribution Services Catalog for the latest manual revision levels and literature ordering procedures.

NOTE

Abbreviations listed under the Detected Uncorrected Error (DUE) columns refer to:

P = Precise DUE (retryable)
I = Imprecise DUE (non-retryable)
N = Non-retryable DUE

SYSTEM PUBLICATION INDEX



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INTRODUCTION

This codes booklet is a complete listing of all the maintenance registers and codes related to the CYBER 170 Computer Systems, Models 815, 825, 835, 845, and 855, the CYBER 180 Computer Systems, Models 810, 830, 835, 840, 845, 850, 855, 860, 990, and the CYBER 840S, 845S, 855S, 840A, 850A, 860A, 870A, 992, 994, 990E, and 995E Computer Systems. Additional information may be found in the appropriate computer systems hardware reference manual listed in the preface. All mnemonics listed in this booklet apply to the COMPASS assembly language.

SS REGISTER (00) (MODELS 810 THROUGH 990; CYBER 840S, 845S, 855S, 840A, 850A, 860A, 870A, 992, 994, 990E, 995E)

Byte	Bit(s)	IOU-810 through 860 IOU(NIO)-840S, 845S, 855S, 840A, 850A, 860A, 990, 992, 994, 990E, 870A, 995E	MEM-810 through 990 840S, 845S, 855S, 840A, 850A, 860A, 870A, 992, 994, 990E, 995E	PROC-810 through 990 840S, 845S, 855S, 840A, 850A, 860A, 870A, 992, 994, 990E, 995E
0	00 through 07	(Not used)	(Not used)	(Not used)
1	08 through 15	(Not used)	(Not used)	(Not used)
2	16 through 23	(Not used)	(Not used)	(Not used)
3	24 through 31	(Not used)	(Not used)	(Not used)
4	32 through 39	(Not used)	(Not used)	(Not used)
5	40 through 47	(Not used)	(Not used)	(Not used)
6	48 through 55	(Not used)	(Not used)	(Not used)
	56	(Not used)	Oscillator selected*	(Not used)
	57	(Not used)	Oscillator selected*	(Not used)
	58	(Not used)	Clock tuning mode	C180 monitor mode
7	59	Summary status	(Not used)	Short warning
	60	Processor halt	(Not used)	Processor halt
	61	Uncor error	Uncor error	Uncor error
	62	(Not used)(810-860)	Cor error	Cor error
	62	Cor error(990, 992, 994, 990E, 995E, 845S thru 870A)	-	-
	63	Long warning	Long warning	Long warning

*Bits 56,57:

00 normal
10 +2 percent
01 -2 percent

EID REGISTER (10) (MODELS 810 THROUGH 990; CYBER 840S, 845S, 855S, 840A, 850A, 860A, 870A, 992, 994, 990E, 995E (Sheet 1 of 2)

Element	Element No.*	Model No.*
PROC-810	00	14
IOU-810	02	14
PROC-815	00	11
MEM-815	01	11
IOU-815	02	11
PROC-825**	00	12
MEM-825	01	12
IOU-825	02	12
PROC-830**	00	13
MEM-830	01	13
IOU-830	02	13
PROC-835**	00	20

*Bits 32 through 39 = element number
Bits 40 through 47 = model number
Bits 48 through 63 = serial number
**Applies to both single and (optional) dual CP.

EID REGISTER (10) (MODELS 810 THROUGH 990; CYBER 840S, 845S, 855S, 840A, 850A, 860A, 870A, 992, 994, 990E, 995E) (Sheet 2 of 2)

Element	Element No.*	Model No.*
MEM-835	01	20
IOU-835 through 860	02	20
IOU(NIO)-840S, 845S, 855S, 840A, 850A, 860A, 870A, 990, 994, 990E, 995E	02	40
IOU(CIO)-992	02	44
PROC-845	00	31
MEM-845, 855	01	30
MEM-840, 845, 850, 855, 860, 840S, 845S, 855S, 840A, 850A, 860A	01	31
PROC-840, 840A	00	34
PROC-850, 850A	00	33
PROC-860**, 860A**, 870A	00	32
PROC-855**	00	30
PROC-840S	00	37
PROC-845S	00	35
PROC-855S	00	36
PROC-990**	00	40
PROC-992	00	42
PROC-994	00	44
PROC-990E, 995E	00	41
MEM-990	01	40
MEM-992	01	42
MEM-994	01	42
MEM-990E, 995E	01	41
ECS coupler	03	20
PEM	04	20

*Bits 32 through 39 = element number
Bits 40 through 47 = model number
Bits 48 through 63 = element serial number
**Applies to both single and (optional) dual CP.

PROC-810, 830 CONTROL STORE SECDED ERRORS REGISTER (81)

Any ones in bits 24 to 63 indicate a Control Store error on the associated pak.

Bits 24-31	DR location 16
Bits 32-39	DR location 17
Bits 40-47	DR location 18
Bits 48-55	DR location 19
Bits 56-63	DR location 20

DBE = Double Bit Error. C.S. = Chip Sel (8k = 2 x 4k chips)

SYNDROME CODE Vs. Pak bit (16 or 18 bits per Pak)

CODE	bit	CODE	bit	CODE	bit
38	0	29	8	2F	16
34	1	19	9	1F	17
2C	2	25	10	20	ECC bit 0
1C	3	15	11	10	ECC bit 1
2A	4	23	12	08	ECC bit 2
1A	5	13	13	04	ECC bit 3
26	6	0B	14	02	ECC bit 4
16	7	37	15	01	ECC bit 5

Micr Byte Distribution

Byte -	0	1	2	3	4	5	6	7	8	9	10
Pak Location -	16	17	18	19	16	17	18	19	20	20	20

PROC-810, 830 MCEL REGISTER (93)

Byte	Bit(s)	Description
0	00 through 07	(Not used)
1	08 through 15	(Not used)
2	16 through 23	(Not used)
3	24 through 31	(Not used)
4	32 through 39	(Not used)
5	40 through 47	(Not used)
6	48 through 55	(Not used)
7	56	File 0, pak location C22, C23, or C24
	57	File 0, pak location D25 or D26
	58	File 1, pak location C22, C23, or C24
	59	File 1, pak location D25 or D26
	60	File 2, pak location C22, C23, or C24
	61	File 2, pak location D25 or D26
	62	File 3, pak location C22, C23, or C24
	63	File 3, pak location D25 or D26

PROC-815, 825 MCEL REGISTER (93)

Byte	Bit(s)	Description
0	00 through 07	(Not used)
1	08 through 15	(Not used)
2	16 through 23	(Not used)
3	24 through 31	(Not used)
4	32 through 39	(Not used)
5	40 through 47	(Not used)
6	48 through 55	(Not used)
7	56	File 0, pak location C22, C23, or C24
	57	File 0, pak location D1 or D2
	58	File 1, pak location C22, C23, or C24
	59	File 1, pak location D1 or D2
	60	File 2, pak location C22, C23, or C24
	61	File 2, pak location D1 or D2
	62	File 3, pak location C22, C23, or C24
	63	File 3, pak location D1 or D2

PROC-810 THROUGH 990, 840S, 845S, 855S, 840A, 850A, 860A, 870A, 992, 994, 990E, 995E PID REGISTER (11)

Byte	Bit(s)	Description
0	00 through 07	(Not used)
1	08 through 15	(Not used)
2	16 through 23	(Not used)
3	24 through 31	(Not used)
4	32 through 39	(Not used)
5	40 through 47	(Not used)
6	48 through 55	(Not used)
7	56 through 63	Processor Identification (Primary processor = 00, Optional processor = 01)

PROC-810 THROUGH 990, 840S, 845S, 855S, 840A, 850A, 860A, 870A, 992, 994, 990E, 995E OI REGISTER (12) (Sheet 1 of 4)

Byte	Bit(s)	Description
	810, 815, 825, 830	
0	00 through 07	(Not used)
1	08 through 15	(Not used)
2	16 through 23	(Not used)
3	24 through 27	(Not used)
	28	Concurrent 170 option installed
	29	A170 mode option installed
	30	SECDED cont store installed
	31	PMF installed
4	32 through 39	(Not used)
5	40 through 47	(Not used)
6	48 through 55	(Not used)
7	56 through 63	(Not used)

PROC-810 THROUGH 990, 840S, 845S, 855S, 840A, 850A, 860A, 870A, 992, 994, 990E, 995E OI REGISTER (12) (Sheet 2 of 4)

Byte	Bit(s)	Description
	835	
0	00 through 07	(Not used)
1	08 through 15	(Not used)
2	16 through 23	(Not used)
3	24 through 31	(Not used)
4	32 through 39	(Not used)
5	40 through 47	(Not used)
6	48 through 55	(Not used)
	56 through 59	(Not used)
	60	A170 mode option installed
7	61	32K-byte cache installed
	62	Second central mem port installed
	63	PMF installed

PROC-810 THROUGH 990, 840S, 845S, 855S, 840A, 850A, 860A, 870A, 992, 994, 990E, 995E OI REGISTER (12) (Sheet 3 of 4)

Byte	Bit(s)	Description
	840, 845, 850, 855, 860, 840S, 845S, 855S, 840A, 850A, 860A, 870A	
0	00 through 07	(Not used)
1	08 through 15	(Not used)
2	16 through 23	(Not used)
3	24 through 31	(Not used)
4	32 through 39	(Not used)
5	40 through 47	(Not used)
6	48 through 55	(Not used)
7	56 through 58	(Not used)
	59	Optional second processor installed
	60	(Not used)
	61	PMF/ECS I/F option installed
	62	32K-byte cache installed
	63	PMF installed

PROC-810 THROUGH 990, 840S, 845S, 855S, 840A, 850A, 860A, 870A, 992, 994, 990E, 995E OI REGISTER (12) (Sheet 4 of 4)

Byte	Bit(s)	Description
	990, 992, 994, 990E, 995E	
0	00 through 07	(Not used)
1	08 through 15	(Not used)
2	16 through 23	(Not used)
3	24 through 31	(Not used)
4	32 through 39	(Not used)
5	40 through 47	(Not used)
6	48 through 55	(Not used)
	56 through 58	(Not used)
	59	Optional second processor installed
7	60,61	(Not used)
	62	Vector instr option installed
	63	PMF installed

PROC-810, 815, 825, 830 DEC REGISTER (30) (Sheet 1 of 2)

Byte	Bit(s)	Description
	00 through 04	(Not used)
0	05	Cont store micro-step enbld
	06	Processor fault status traps enbld
	07	(Not used)
	08,09	(Not used)
1	10	Pulse width margins +15% (810,830), not used (815,825)
	11	Pulse width margins -15% (810,830), not used (815,825)
	12 through 15	(Not used)
2	16 through 23	(Not used)
	24	Processor fault status enbld
	25	Map real mem adrs mode enbld
	26	Map file 0 enbld
3	27	Map file 1 enbld
	28	Map file 2 enbld
	29	Map file 3 enbld
	30	Instr retry enbld
	31	Instr step enbld

PROC-810, 815, 825, 830 DEC REGISTER (30) (Sheet 2 of 2)

Byte	Bit(s)	Description
	32	Maint scan halt enbld
	33	Test mode enbld
	34	Physical ECS present (never set)
4	35	Dsbl cor error to SS rgtr (MEM-810 through 830)
	36	Cont store bkpt enbld
	37	Cont store sweep enbld
	38	Force good response on SBE (MEM-810 through 830)
	39	Dsbl cor error log (MEM-810 through 830)
5	40 through 47	(Not used)
6	48 through 55	(Not used)
7	56 through 63	(Not used)

PROC-810, 815, 825, 830 CSA REGISTER (31)

Byte	Bit(s)	Description
0	00 through 07	(Not used)
1	08 through 15	(Not used)
2	16 through 23	(Not used)
3	24 through 31	(Not used)
4	32 through 39	(Not used)
5	40 through 47	(Not used)
6	48 through 50	(Not used)
7	51 through 63	"a" bits are Cont Store Next Adrs (usually Last Adrs +1).

PROC-810, 815, 825, 830 CSB REGISTER (32)

Byte	Bit(s)	Description
0	00 through 07	(Not used)
1	08 through 15	(Not used)
2	16 through 23	(Not used)
3	24 through 31	(Not used)
4	32 through 39	(Not used)
5	40 through 47	(Not used)
6	48 through 50	(Not used)
	51 through 55	"a" bits are the adrs where the Cont Store will halt if bit 36 in the PROC ENVIRONMENT CONTROL REGISTER (30) is set.
7	56 through 63	"a" bits are the adrs where the Cont Store will halt if bit 36 in the PROC ENVIRONMENT CONTROL REGISTER (30) is set.

NOTE

After the Halt, the PROC CONTROL STORE ADDRESS REGISTER (31) will not contain the Breakpoint Address. Register 32 will have the next Control Store Address, which depends on the Micrand in the Breakpoint Address.

PROC-810, 815, 825, 830 PFS0/PCEL REGISTER (80/90) (Sheet 1 of 2)

Byte	Bit(s)	Description
0	00 through 07	(Not used)
1	08 through 15	(Not used)
2	16 through 23	(Not used)
3	24 through 31	(Not used)
	32	ARVI PE bits 0 through 7, 32 through 39
	33	ARVI PE bits 8 through 15, 40 through 47
	34	ARVI PE bits 16 through 23, 48 through 55
4	35	ARVI PE bits 24 through 31, 56 through 63
	36	Uncor mem write error
	37	Mem reject
	38	Mem tag PE
	39	Response code PE
	40	FP exception trap index ROM PE
	41	AD or BD bits 0 through 15 PE
	42	LD box ROM PE
5	43	ADS or BDS ROM PE
	44	Shift type ROM PE or shifter input
	45	Uncor mem read error
	46	AD or BD bits 16 through 31 PE
	47	AD-UN PE, MAC write PE

PROC-810, 815, 825, 830 PFS0/PCEL REGISTER (80/90) (Sheet 2 of 2)

Byte	Bit(s)	Description
	48	Mem response time-out
	49	CYBER ROM PE
	50	Instr PE
6	51	XBD ROM PE
	52	AD or BD bits 32 through 47 PE
	53	BDP adder, data ROM, RJB, RKB PE
	54	Immed ROM
	55	AD or BD bits 48 through 63 PE
	56	Map PE bits 32 through 39
	57	Map PE bits 40 through 47
	58	Map PE bits 48 through 55
7	59	Map PE bits 56 through 63
	60	Map multiple hit fault
	61	(Not used)
	62	MAC error
	63	Double bit error if SECDED is installed (810 and 830). Any CS data PE (815, 825)

PROC-810, 815, 825, 830 PTM REGISTER (A0)

Bit(s)	Description
00 through 47	(Not used)
Hexadecimal Code (48 through 63)	
0800	Nanocode ROM
0900	Invert mem fctn parity
0A00	Invert mem tag parity
0B00	Invert mem mark parity
0C00	Invert execution data/adrs parity, byte 0, 1
0D00	Invert execution data/adrs parity, byte 2, 3
0E00	Invert execution data/adrs parity, byte 4, 5
0F00	Invert execution data/adrs parity, byte 6, 7
0008	(Not used)
0009	Invert floating-point trap index
000A	Invert floating-point trap ROM
000B	Invert MAC bus data parity
000C	Invert adder latch data parity
000D	(Not used)
000E	(Not used)
000F	(Not used)

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PROC-835 EC/DEC REGISTER (20/30) (Sheet 1 of 2)

Byte	Bit(s)	Description
	00	Cont store sweep mode selected
	01	Micro-step enbld
	02	Instr step enbld
0	03	Cont store bkpt enbld
	04	Mem port 0 enbld
	05	Mem port 1 enbld
	06	Mem port 0 parity check dsbld
	07	Mem port 1 parity check dsbld
	08	Cache enbld: 1st quarter, 0 through 7K
	09	Cache enbld: 2nd quarter, 8 through 15K
	10	Cache enbld: 3rd quarter, 16 through 23K
1	11	Cache enbld: 4th quarter, 24 through 32K
	12	Cache conflict: rgtr 0 enbld
	13	Cache conflict: rgtr 1 enbld
	14	Cache conflict: rgtr 2 enbld
	15	Cache conflict: rgtr 3 enbld
	16	Enbl retry diagnostic check
	17	Enbl deadstart diagnostic check
	18	Force page file hit
2	19	(Not used)
	20	Cache CEL logging dsbld
	21	Map DEL logging dsbld
	22	Test port number
	23	(Not used)
	24	Map dsbl, page bfr 0
	25	Map dsbl, page bfr 1
	26	Map dsbl, page bfr 2
3	27	Map dsbl, page bfr 3
	28	Map dsbl, seg/bfr 0
	29	Map dsbl, seg/bfr 1
	30	Map RMA mode enbld
	31	Lock last translation into map

PROC-835 EC/DEC REGISTER (20/30) (Sheet 2 of 2)

Byte	Bit(s)	Description
	32	Preserve and dsbl PP exchanges
	33	Test mode enbld
	34	Physical ECS present
4	35	Dsbl cor error to status summary rgtr
	36	(Not used)
	37	Enbl mem port sel
	38	Sel mem port
	39	Cache allocation on read miss enbld
	40	Maint scan halt enbld
	41	Instr cntr halt enbld
5	42 through 45	(Not used)
	46	PFS micro-traps dsbld
	47	Instr retry enbld
	48	(Not used)
	49	Dsbl cache kill on input PE
	50	Dsbl rgtr file write kill on PE
6	51	Dsbl port 1 response
	52	Force wide margins, panel A
	53	Force wide margins, panel B
	54	Force wide margins, panel C
	55	Force wide margins, panel C
	56	Force wide margins, panel D
	57	Force wide margins, panel E
	58	Force narrow margins, panel A
7	59	Force narrow margins, panel B
	60	Force narrow margins, panel C
	61	Force narrow margins, panel C
	62	Force narrow margins, panel D
	63	Force narrow margins, panel E

PROC-835 PFS0 REGISTER (80) (Sheet 1 of 2)

Byte	Bit(s)	Description
	00	Cache input, bytes 0 and 1, adrs 0
	01	Cache input, bytes 2 and 3, adrs 1
	02	Cache input, bytes 4 and 5, adrs 2
0	03	Cache input, bytes 6 and 7, adrs 3
	04	Cache output, bytes 0 and 1
	05	Cache output, bytes 2 and 3
	06	Cache output, bytes 4 and 5
	07	Cache output, bytes 6 and 7
	08	Data, port 0, bytes 0 and 1
	09	Data, port 0, bytes 2 and 3
	10	Data, port 0, bytes 4 and 5
1	11	Data, port 0, bytes 6 and 7
	12	Data, port 1, bytes 0 and 1
	13	Data, port 1, bytes 2 and 3
	14	Data, port 1, bytes 4 and 5
	15	Data, port 1, bytes 6 and 7
	16	Identifier/response code, port 0
	17	Identifier/response code, port 1
	18	Identifier, fctn, partial-write cache input
2	19	(Not used)
	20	CPR status good
	21	Response code = 1 error
	22	Response code = 5 error
	23	Response code = 7 error
	24	Cache ID and CPR empty
	25	CPR multiple hit
	26	Identifier, cache out
3	27	Cache time-out
	28	No overflow on simultaneous response bfr
	29	Fctn code valid, cache input
	30	Incremented ident, cache input
	31	MAC ROMs

PROC-835 PFS0 REGISTER (80) (Sheet 2 of 2)

Byte	Bit(s)	Description
	32	Rgtr file, byte 0
	33	Rgtr file, byte 1
	34	Rgtr file, byte 2
4	35	Rgtr file, byte 3
	36	Rgtr file, byte 4
	37	Rgtr file, byte 5
	38	Rgtr file, byte 6
	39	Rgtr file, byte 7
	40	Seg number
	41 through 44	I mux, B mux adrs
5	45	Ring parity
	46	Adrs sel ROMs
	47	(Not used)
	48	Invalidation adrs, exchange adrs
	49	(Not used)
	50	BDP J stream PE
6	51	BDP K stream PE
	52	BDP output PE
	53	BDP cont to edit
	54	BDP branch or CYBER convert ROM
	55	(Not used)
	56	Floating-point trap ROM
	57	Exponent adrs fctn adrs decode
	58	ROM and partial write
7	59	(Not used)
	60	Identifier from cache
	61	Immed cont ROMs
	62,63	(Not used)

PROC-835 PFS1 REGISTER (81)

Byte	Bit(s)	Description
0	00	Cont store PE, byte 0
	01 through 07	(Not used)
1	08	Cont store PE, byte 1
	09 through 15	(Not used)
2	16	Cont store PE, byte 2
	17 through 23	(Not used)
3	24	Cont store PE, byte 3
	25 through 31	(Not used)
4	32	Cont store PE, byte 4
	33 through 39	(Not used)
5	40	Cont store PE, byte 5
	41 through 47	(Not used)
6	48	Cont store PE, byte 6
	49 through 55	(Not used)
7	56	Cont store PE, byte 7
	57 through 63	(Not used)

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PROC-835 CCEL/MCEL REGISTER (92/93) (Sheet 1 of 2)

Byte	Bit(s)	Description
	00	Valid cache CEL entry
	01	Unlogged error
0	02	(Not used)
	03	PE, LRU status array cntrs
	04 through 06	(Not used)
	07	Multiple hit in tag arrays
	08	No PE, BN in tag array, blocks 0 and 1
	09	No PE, BN in tag array, blocks 2 and 3
	10	No PE, BN in tag array, blocks 4 and 5
1	11	No PE, BN in tag array, blocks 6 and 7
	12	No PE, ASID in tag array, blocks 0 and 1
	13	No PE, ASID in tag array, blocks 2 and 3
	14	No PE, ASID in tag array, blocks 4 and 5
	15	No PE, ASID in tag array, blocks 6 and 7
	16	ASID compare, block 0
	17	ASID compare, block 1
	18	ASID compare, block 2
2	19	ASID compare, block 3
	20	ASID compare, block 4
	21	ASID compare, block 5
	22	ASID compare, block 6
	23	ASID compare, block 7
	24	BN compare, block 0
	25	BN compare, block 1
	26	BN compare, block 2
3	27	BN compare, block 3
	28	BN compare, block 4
	29	BN compare, block 5
	30	BN compare, block 6
	31	BN compare, block 7

PROC-835 CCEL/MCEL REGISTER (92/93) (Sheet 2 of 2)

Byte	Bit(s)	Description
	32	Valid map CEL entry
	33	Unlogged error
4	34 through 36	(Not used, always zero)
	37	PE, seg file tag
	38	Multiple hit, seg file
	39	Multiple hit, page file
	40	PE seg, file 0, pak location D06
	41	PE seg, file 1, pak location D06
	42	PE seg, file 0, pak location D07
5	43	PE seg, file 1, pak location D07
	44	PE seg, file 0, pak location D08
	45	PE seg, file 1, pak location D08
	46	PE seg, file 0, pak location D09
	47	PE seg, file 1, pak location D09
	48	PE page, file 0, pak location D06
	49	PE page, file 1, pak location D06
	50	PE page, file 2, pak location D06
6	51	PE page, file 3, pak location D06
	52	PE page, file 0, pak location D07
	53	PE page, file 1, pak location D07
	54	PE page, file 2, pak location D07
	55	PE page, file 3, pak location D07
	56	PE page, file 0, pak location D08
	57	PE page, file 1, pak location D08
	58	PE page, file 2, pak location D08
7	59	PE page, file 3, pak location D08
	60	PE page, file 0, pak location D09
	61	PE page, file 1, pak location D09
	62	PE page, file 2, pak location D09
	63	PE page, file 3, pak location D09

PROC-835 PTM REGISTER (A0) (Sheet 1 of 2)

Byte	Bit(s)	Description
	00	Force bad parity to WAR, byte 0
	01	Invert adrs parity, byte 5
	02	Invert adrs parity, byte 4
0	03,04	Invert seg parity
	05	Invert rgtr file parity, byte 7
	06	Invert rgtr file parity, byte 6
	07	Invert rgtr file parity, byte 5
	08	Force bad parity to WAR, byte 1
	09	Invert rgtr file parity, byte 4
	10	Invert rgtr file parity, byte 3
1	11	Invert rgtr file parity, byte 2
	12	Invert rgtr file parity, byte 1
	13	Invert rgtr file parity, byte 0
	14	Invert exponent adder ROMs parity
	15	Invert floating-point trap ROMs parity
	16	Force bad parity to WAR, byte 2
	17 through 19	Invert seg file parity
2	20	Invert adrs parity, byte 7
	21	Invert adrs parity, byte 6
	22	Invert data parity, byte 2
	23	Invert data parity, byte 1
	24	Force bad parity to WAR, byte 3
	25	Invert data parity, byte 0
3	26	Invert gen identifier/LRU cntr parity
	27	Invert ASID parity, byte 1
	28	Invert ASID parity, byte 0
	29 through 31	Invert page file parity

PROC-835 PTM REGISTER (A0) (Sheet 2 of 2)

Byte	Bit(s)	Description
	32	Force bad parity to WAR, byte 4
4	33 through 37	Invert page file parity
	38	Invert seg file parity
	39	Invert identifier/AD sel ROM parity
	40	Force bad parity to WAR, byte 5
	41	Invert fctn code parity
	42	Invert mark lines parity
5	43	Invert tag in parity
	44	Invert adrs parity, byte 3
	45	Invert adrs parity, byte 2
	46	Invert adrs parity, byte 1
	47	Invert adrs parity, byte 0
	48	Force bad parity to WAR, byte 6
	49	Invert data parity, byte 7
	50	Invert data parity, byte 6
6	51	Invert data parity, byte 5
	52	Invert data parity, byte 4
	53	Invert data parity, byte 3
	54	Invert BDP K stream input parity
	55	Invert BDP J stream input parity
	56	Force bad parity to WAR, byte 7
	57	Invert BDP output ROMs parity
	58	Invert BDP cont ROMs parity
7	59	Invert MAC ROMs parity
	60	Invert CYBER convert ROMs parity
	61	Invert immed sel ROMs parity
	62	Invert exchange/invalidate adrs parity
	63	Invert partial-write parity

PROC-840, 845, 850, 855, 860, 840S, 845S, 855S, 840A, 850A, 860A, 870A DEC REGISTER (30) (Sheet 1 of 2)

Byte	Bit(s)	Description
0	00 through 07	(Not used)
1	08 through 15	(Not used)
2	16 through 23	(Not used)
3	24 through 31	(Not used)

PROC-840, 845, 850, 855, 860, 840S, 845S, 855S, 840A, 850A, 860A, 870A DEC REGISTER (30) (Sheet 2 of 2)

Byte	Bit(s)	Description
	32	(Not used 845, 855) Directs Reads/Writes of Cont Store (840, 850, 860, 840S through 870A only)
	33	Test mode enbld
	34	(Not used)
4	35	Dsbl cor error to PROC-840 through 860, 840S through 870A status summary rgtr
	36	Page map configuration, enbl set 0
	37	Page map configuration, enbl set 1
	38	Page map configuration, enbl set 2
	39	Page map configuration, enbl set 3
	40	Seg map configuration, enbl set 0
	41	Seg map configuration, enbl set 1
	42	Cont store sweep
5	43	(Not used)
	44	Cont store bkpt enbl
	45	Instr step enbl
	46	(Not used)
	47	Dsbl detected uncor error
	48	Wide clock margins applied (+10 percent)
	49	Narrow clock margins applied (-10 percent)
6	50	Enbl cache lookahead
	51	Dsbl unconditional cache lookahead
	52 through 55	Error retry limit
	56	Error retry limit parity
	57	Cache configuration, enbl set 0
	58	Cache configuration, enbl set 1
7	59	Cache configuration, enbl set 2
	60	Cache configuration, enbl set 3
	61	Cache fake central mem
	62	Force real mem adrs
	63	(Not used)

PROC-840, 845, 855, 860, 840S, 845S, 855S, 840A, 850A, 860A, 870A CSA REGISTER (31)

Byte(s)	Bit(s)	Description
0	00 through 07	(Not used)
1	08 through 15	(Not used)
2	16 through 23	(Not used)
3	24 through 31	(Not used)
4	32 through 39	(Not used)
5	40 through 47	(Not used)
6	48 through 52	(Not used)
6,7	53 through 63	CSA

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PROC-840, 845, 850, 855, 860, 840S, 845S, 855S, 840A, 850A, 860A, 870A PFS0 REGISTER (80) (Sheet 1 of 3)

Byte	Level 3 Diagram	Bit	Description
	ICC 3.1	00	R60 after PONR MCR bit 0: uncor PE
	ICC 3.1	01	Cor/soft/bypass error, MAC opn PDM
	AC 3.15	02	AC adrs mux to LM PE, byte 2
	AC 3.15	03	AC adrs mux to LM PE, byte 3
0	AC 3.15	04	AC adrs mux to LM PE, byte 4
	AC 3.15	05	AC adrs mux to LM PE, byte 5
	AC 3.15	06	AC adrs mux to LM PE, byte 6
	AC 3.15	07	AC adrs mux to LM PE, byte 7
	AC 3.8	08	A/C stream data assy rgtr PE, byte 0
	AC 3.8	09	A/C stream data assy rgtr PE, byte 1
	AC 3.8	10	A/C stream data assy rgtr PE, byte 2
1	AC 3.8	11	A/C stream data assy rgtr PE, byte 3
	AC 3.8	12	A/C stream data assy rgtr PE, byte 4
	AC 3.8	13	A/C stream data assy rgtr PE, byte 5
	AC 3.8	14	A/C stream data assy rgtr PE, byte 6
	AC 3.8	15	A/C stream data assy rgtr PE, byte 7
	AC 3.9	16	A/C stream data bfr rgtr PE, byte 0
	AC 3.9	17	A/C stream data bfr rgtr PE, byte 1
	AC 3.9	18	A/C stream data bfr rgtr PE, byte 2
2	AC 3.9	19	A/C stream data bfr rgtr PE, byte 3
	AC 3.9	20	A/C stream data bfr rgtr PE, byte 4
	AC 3.9	21	A/C stream data bfr rgtr PE, byte 5
	AC 3.9	22	A/C stream data bfr rgtr PE, byte 6
	AC 3.9	23	A/C stream data bfr rgtr PE, byte 7

PROC-840, 845, 850, 855, 860, 840S, 845S, 855S, 840A, 850A, 860A, 870A PFSO REGISTER (80) (Sheet 2 of 3)

Byte	Level 3 Diagram	Bit	Description
	AC 3.12	24	B stream data bfr rgtr PE, byte 0
	AC 3.12	25	B stream data bfr rgtr PE, byte 1
	AC 3.12	26	B stream data bfr rgtr PE, byte 2
3	AC 3.12	27	B stream data bfr rgtr PE, byte 3
	AC 3.12	28	B stream data bfr rgtr PE, byte 4
	AC 3.12	29	B stream data bfr rgtr PE, byte 5
	AC 3.12	30	B stream data bfr rgtr PE, byte 6
	AC 3.12	31	B stream data bfr rgtr PE, byte 7
	AC 3.15	32	A/C stream ASID rgtr PE, byte 0
	AC 3.15	33	A/C stream ASID rgtr PE, byte 1
	AC 3.15	34	B stream ASID rgtr PE, byte 0
4	AC 3.15	35	B stream ASID rgtr PE, byte 1
	AC 3.13	36	Address offset sel mux PE, byte 2
	AC 3.13	37	Address offset sel mux PE, byte 3
	AC 3.0/18	38	AC micr PE, byte 0
	AC 3.0/18	39	AC micr PE, byte 1
	AC 3.15	40	Recovery adrs rgtr PE, byte 0
	AC 3.15	41	Recovery adrs rgtr PE, byte 1
	AC 3.15	42	Recovery adrs rgtr PE, byte 2
5	AC 3.15	43	Recovery adrs rgtr PE, byte 3
	ALN 3.1	44	ALN soft cont data-out rgtr PE
	AC 3.2	45	AC soft cont 2 data-out rgtr PE
	AC 3.1	46	AC soft cont 1 data-out rgtr PE
	AC 3.14	47	ALN shift count rgtr PE

Byte	Level 3 Diagram	Bit	Description
	AC 3.13/18	48	A/C stream length cntr PE
	AC 3.13/18	49	B stream length cntr PE
	AC 3.9	50	A stream data byte to BDP PE
6	AC 3.12	51	B stream data byte to BDP PE
	AC 3.8	52	Store bit/all other opn sel mux PE
	ALN 3.15/24	53	Conv-to-binary data byte from BDP PE
	BDP 3.8/33	54	B stream stage 1 data rgtr PE
	BDP 3.5/33	55	A stream stage 1 data rgtr PE
	BDP 3.15/33	56	Rgtr file A adrs cntr PE
	BDP 3.15/33	57	Rgtr file B adrs cntr PE
7	BDP 3.16/33	58	Rgtr file A data PE
	BDP 3.16/33	59	Rgtr file B data PE
	BDP 3.25/33	60	Dec adder bits 10 through 17, conv-to-dec PE
	BDP 3.15/33	61	Table load limit rgtr stage 3 PE
	BDP 3.13/33	62	Common stage 7 rgtr PE
	MAC 3.11/9	63	PFS board 0 int PE

PROC-840, 845, 850, 855, 860, 840S, 845S, 855S, 840A, 850A, 860A, 870A PFS1 REGISTER (81)

Byte	Level 3 Diagram	Bit(s)	Description
	BDP 3.14/33	00	Buffer RAM adrs cntr PE
	BDP 3.20/33	01	C stream stage 2 data rgtr PE
	BDP 3.3/33	02	Spec error RAM, x256 RAM adrs PE
0	BDP 3.3/33	03	Spec error RAM, x256 RAM out data PE
	BDP 3.5/33	04	A stream stage 2 data rgtr PE
	BDP 3.8/33	05	B stream stage 2 data rgtr PE
	BDP 3.2/33	06	Aj descr PE
	BDP 3.2/33	07	Ak descr PE
	BDP 3.22/33	08	Translate RAM adrs PE
	BDP 3.22/33	09	Translate RAM output data PE
	BDP 3.23/33	10	Conv-to-binary/dec RAM adrs PE
1	BDP 3.23/33	11	Conv-to-binary/dec RAM output data PE
	BDP 3.1/33	12	BDP micr byte 0 or 1 PE
	BDP 3.1/33	13	BDP micr byte 2 or 3 PE
	BDP 3.1/33	14	BDP micr byte 4 or 5 PE
	BDP 3.1/33	15	BDP micr byte 6 or 7 PE
2		16 through 23	(Not used)
3		24 through 31	(Not used)
4		32 through 39	(Not used)
5		40 through 47	(Not used)
6		48 through 55	(Not used)
7		56 through 63	(Not used)

PROC-840, 845, 850, 855, 860, 840S, 845S, 855S, 840A, 850A, 860A, 870A PFS2 REGISTER (82) (Sheet 1 of 2)

Byte	Level 3 Diagram	Bit(s)	Description
	BDP 3.11/33	00	Immed data byte in scale cntr PE
	BDP 3.29/33	01	Edit mask byte rgtr PE
	LM 3.21	02	Cache adrs rgtr PE, byte 0
	LM 3.21	03	Cache adrs rgtr PE, byte 1
0	LM 3.21	04	Cache adrs rgtr PE, byte 2
	LM 3.21	05	Cache adrs rgtr PE, byte 3
	LM 3.21	06	Cache adrs rgtr PE, byte 4
	LM 3.21	07	Cache adrs rgtr PE, byte 5
	LM 3.21	08	Cache write-data PE, byte 0
	LM 3.21	09	Cache write-data PE, byte 1
	LM 3.21	10	Cache write-data PE, byte 2
1	LM 3.21	11	Cache write-data PE, byte 3
	LM 3.21	12	Cache write-data PE, byte 4
	LM 3.21	13	Cache write-data PE, byte 5
	LM 3.21	14	Cache write-data PE, byte 6
	LM 3.21	15	Cache write-data PE, byte 7
	LM 3.20	16	Multiple cache hit
	LM 3.20	17	Multiple cache allocate error
	LM 3.14	18	Cache tag file PE
	LM 3.14	19	Cache tag file adrs PE
2	OPI 3.19	20	DAI PE: LM read data mux, direct CMC data 3
	OPI 3.19	21	DAI PE: LM read data mux, cache read data 2
	OPI 3.19	22	DAI PE: LM read data mux, real memory adrs 1
	OPI 3.19	23	DAI PE: LM read data mux, bfr CMC data 0
	LM 3.21	24	Cache write data from CPU PE
	LM 3.21	25	Cache block fill data from CM port PE
	LM 3.5/21	26	Cache adrs rgtr PE 4: cache associative tag
	LM 3.21	27	Cache mark data PE
3	LM 3.21	28	Cache adrs rgtr PE: adrs mux 0: invalidate
	LM 3.21	29	Cache adrs rgtr PE: adrs mux 1: AC adrs
	LM 3.21	30	Cache adrs rgtr PE: adrs mux 2: IF adrs
	LM 3.21	31	Cache adrs rgtr PE: adrs mux 3: interrupt

PROC-840, 845, 850, 855, 860, 840S, 845S, 855S, 840A, 850A, 860A, 870A PFS2 REGISTER (82) (Sheet 2 of 2)

Byte	Level 3 Diagram	Bit(s)	Description
	LM 3.3/21	32	Modified purge code (from SM) PE
	LM 3.3/21	33	LM micr PE, byte 0
	LM 3.3/21	34	LM micr PE, byte 1
		35	(Not used)
	LM 3.12	36	Page map status PE, set 0
4	LM 3.12	37	Page map status PE, set 1
	LM 3.12	38	Page map status PE, set 2
	LM 3.12	39	Page map status PE, set 3
	LM 3.12	40	Page map PE, set 0
	LM 3.12	41	Page map PE, set 1
	LM 3.12	42	Page map PE, set 2
5	LM 3.12	43	Page map PE, set 3
	LM 3.12	44	Page frame adrs PE
		45 through 47	(Not used)
	LM 3.10	48	Page table length rgtr PE
6	LM 3.10	49	Page table adrs rgtr PE
	LM 3.10	50	Page offset rgtr PE
	LM 3.6	51	Page size mask PE
	LM 3.7	52	Stream mode exchange word tag PE
		53 through 55	(Not used)
	LM 3.8	56	CMC response 2: cor error write
	LM 3.8	57	CMC response 6: cor error read
	LM 3.8	58	CMC response 1: uncor error write
7	LM 3.8	59	CMC response 5: uncor error read
	LM 3.8	60	CMC response 7: reject
	LM 3.8	61	CMC response code: PE
	LM 3.8	62	CMC tag rgtr PE
	MAC 3.11/9	63	PFS board 1 int PE

Byte	Level 3 Diagram	Bit(s)	Description
	LM 3.21	00	Cache adrs PE, set 0
	LM 3.21	01	Cache adrs PE, set 1
	LM 3.21	02	Cache adrs PE, set 2
0	LM 3.21	03	Cache adrs PE, set 3
	LM 3.21	04	Cache tag RAM PE, set 0
	LM 3.21	05	Cache tag RAM PE, set 1
	LM 3.21	06	Cache tag RAM PE, set 2
	LM 3.21	07	Cache tag RAM PE, set 3
	OPI 3.19	08	DAI PE, cache data, set 0
	OPI 3.19	09	DAI PE, cache data, set 1
	OPI 3.19	10	DAI PE, cache data, set 2
1	OPI 3.19	11	DAI PE, cache data, set 3
	OPI 3.19	12	DAI PE: DAI mux, local mem read data 3
	OPI 3.19	13	DAI PE: DAI mux, byte load data 2
	OPI 3.19	14	DAI PE: DAI mux, ALN result data 1
	OPI 3.19	15	DAI PE: DAI mux, functional unit micr 0
2		16 through 23	(Not used)
3		24 through 31	(Not used)
4		32 through 39	(Not used)
5		40 through 47	(Not used)
6		45 through 55	(Not used)
7		56 through 63	(Not used)

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PROC-840, 845, 850, 855, 860, 840S, 845S, 855S, 840A, 850A, 860A, 870A PFS4 REGISTER (84) (Sheet 1 of 2)

Byte	Level 3 Diagram	Bit(s)	Description
	SM 3.3/5	00	Seg descr mux-out PE, set 0
	SM 3.3/5	01	Seg descr mux-out PE, set 1
	SM 3.1/5	02	Seg descr mux PE, byte 0
0	SM 3.1/5	03	Seg descr mux PE, byte 1
	SM 3.1/5	04	Seg descr mux PE, byte 2
	SM 3.1/5	05	Seg descr mux PE, byte 3
	SM 3.1/5	06	Seg descr mux PE, byte 4
	SM 3.1/5	07	Seg descr mux PE, byte 5
	SM 3.0/5	08	Seg table length PE, byte 0
	SM 3.0/5	09	Seg table length PE, byte 1
	SM 3.0/5	10	Seg table adrs rgtr PE, bytes 0 and 3
1	SM 3.0/5	11	Seg table adrs rgtr PE, bytes 1 and 2
	SM 3.1/5	12	New P rgtr PE, byte 0
	SM 3.1/5	13	New P rgtr PE, byte 1
	SM 3.1/5	14	New P rgtr PE, byte 2
	SM 3.1/5	15	New P rgtr PE, byte 3
	SM 3.0/5	16	PVA rgtr bits 4 through 7 (CBP VMID) PE
	SM 3.0/5	17	PVA rgtr bits 12 through 15 (CBP R3) PE
	SM 3.0/5	18	PVA rgtr PE, byte 2
2	SM 3.0/5	19	PVA rgtr PE, byte 3
	SM 3.3/5	20	Seg descr mux-out PE: neither set sel
	SM 3.3/5	21	Valid status RAM error: PE or double hit
	SM 3.4/5	22	SM micr PE, byte 0
	SM 3.4/5	23	SM micr PE, byte 1
	SM 3.4/5	24	Purge code PE
	ICP 3.1	25	Rank 32 BDP descr data type rgtr PE
	ICP 3.1	26	Rank 32 j,k rgtr PE
3	ICP 3.0	27	Rank 50 UTP rgtr PE, byte 2
	ICP 3.0	28	Rank 50 UTP rgtr PE, byte 4
	ICP 3.0	29	Rank 50 UTP rgtr PE, byte 5
	ICP 3.0	30	Rank 50 UTP rgtr PE, byte 6
	ICP 3.0	31	Rank 50 UTP rgtr PE, byte 7

PROC-840, 845, 850, 855, 860, 840S, 845S, 855S, 840A, 850A, 860A, 870A PFS4 REGISTER (84) (Sheet 2 of 2)

Byte	Level 3 Diagram	Bit(s)	Description
	ICC 3.3	32	Live rgtr write-data PE, byte 0
	ICC 3.3	33	Live rgtr write-data PE, byte 1
	ICC 3.3	34	Rank 41 general micr PE 2, byte 3
4	ICC 3.3	35	Rank 41 general micr PE 1, byte 2
	ICP 3.0	36	Rank 50 P rgtr PE, byte 4
	ICC 3.0	37	Rank 50 P rgtr PE, byte 5
	ICC 3.0	38	Rank 50 P rgtr PE, byte 6
	ICC 3.0	39	Rank 50 P rgtr PE, byte 7
	ICP 3.3	40	Rank 41 general micr PE 3 (byte 4)
	ICP 3.3	41	Successful retry
	ICP 3.6	42	Deadman time-out
5	ICP 3.7	43	Debug mask PE
	ICC 3.0	44	MAC opn PDM
	ICC 3.9	45	Retry cntr rgtr PE
	ICC 3.6	46	PDM during exchange (exchange mode set)
	ICC 3.7	47	Rank 50 before PONR PDM
	OPI 3.12	48	DAI PE 1: rgtr file write data PE, byte 0
	OPI 3.12	49	DAI PE 2: rgtr file write data PE, byte 1
	OPI 3.12	50	DAI PE 3: rgtr file write data PE, byte 2
6	OPI 3.12	51	DAI PE 4: rgtr file write data PE, byte 3
	OPI 3.12	52	DAI PE 5: rgtr file write data PE, byte 4
	OPI 3.12	53	DAI PE 6: rgtr file write data PE, byte 5
	OPI 3.12	54	DAI PE 7: rgtr file write data PE, byte 6
	OPI 3.12	55	DAI PE 8: rgtr file write data PE, byte 7
	OPI 3.1	56	Minipipe rank 50 rgtr file write adrs PE
	OPI 3.5	57	Rgtr file read data rgtr PE, bytes 0 through 3
7	OPI 3.5	58	Rgtr file read data rgtr PE, bytes 4 through 7
	OPI 3.16/19	59	CMC tag (from LM) PE
		60 through 62	(Not used)
	MAC 3.11/9	63	PFS board 2 int PE

PROC-840, 845, 850, 855, 860, 840S, 845S, 855S, 840A, 850A, 860A, 870A PFS5 REGISTER (85)

Byte	Level 3 Diagram	Bit(s)	Description
	OPI 3.6	00	Rank 22 P rgtr PE, byte 4
	OPI 3.6	01	Rank 22 P rgtr PE, byte 5
	OPI 3.6	02	Rank 22 P rgtr PE, byte 6
0	OPI 3.6	03	Rank 22 P rgtr PE, byte 7
	OPI 3.6	04	R22 BDP descr data type field PE
	OPI 3.6	05	Rank 22 j,k field PE
	OPI 3.6	06	Rank 22 immed operand PE, byte 0
	OPI 3.6	07	Rank 22 immed operand PE, byte 1
	OPI 3.0	08	Functional unit micr PE, byte 6
	OPI 3.0	09	Functional unit micr PE, byte 7
	OPI 3.16/19	10	Rgtr data sel write field PE, byte 0
1	OPI 3.16/19	11	Rgtr data sel write field PE, byte 1
	OPI 3.16/19	12	Increment j,k field PE
		13	(Not used)
	OPI 3.17	14	Microsecond cntr PE
		15	(Not used)
2		16 through 23	(Not used)
3		24 through 31	(Not used)
4		32 through 39	(Not used)
5		40 through 47	(Not used)
6		48 through 55	(Not used)
7		56 through 63	(Not used)

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PROC-840, 845, 850, 855, 860, 840S, 845S, 855S, 840A, 850A, 860A, 870A PFS6 REGISTER (86) (Sheet 1 of 2)

Byte	Level 3 Diagram	Bit(s)	Description
		00 through 02	(Not used)
	CST 3.4	03	Micrand adrs rgtr PE
	CST 3.5	04	CST write data (from MAC) PE, byte 0
0	CST 3.5	05	CST write data (from MAC) PE, byte 1
	CST 3.1/0	06	MSC field rgtr PE, byte 0
	CST 3.1/0	07	MSC field rgtr PE, byte 1
	CST 3.5	08	FU micr bfr rgtr (t23) PE, byte 0
	CST 3.5	09	FU micr bfr rgtr (t23) PE, byte 1
	CST 3.5	10	FU micr bfr rgtr (t23) PE, byte 2
1	CST 3.5	11	FU micr bfr rgtr (t23) PE, byte 3
	CST 3.5	12	FU micr bfr rgtr (t23) PE, byte 4
	CST 3.5	13	FU micr bfr rgtr (t23) PE, byte 5
	CST 3.5	14	FU micr bfr rgtr (t23) PE, byte 6
	CST 3.5	15	FU micr bfr rgtr (t23) PE, byte 7
	CST 3.5	16	FU micr rgtr (t31) PE, byte 0
	CST 3.5	17	FU micr rgtr (t31) PE, byte 1
	CST 3.5	18	FU micr rgtr (t31) PE, byte 2
2	CST 3.5	19	FU micr rgtr (t31) PE, byte 3
	CST 3.5	20	FU micr rgtr (t31) PE, byte 4
	CST 3.5	21	FU micr rgtr (t31) PE, byte 5
	CST 3.5	22	FU micr rgtr (t31) PE, byte 6
	CST 3.5	23	FU micr rgtr (t31) PE, byte 7
	CST 3.5	24	General micr rgtr (t22) PE, byte 2
	CST 3.5	25	General micr rgtr (t22) PE, byte 3
	CST 3.5	26	General micr rgtr (t22) PE, byte 4
3	CST 3.5	27	General micr rgtr (t22) PE, byte 5
	CST 3.5	28	General micr rgtr (t22) PE, byte 6
	CST 3.5	29	General micr rgtr (t22) PE, byte 7
	OPI 3.14	30	A-start, X-start cntr rgtr PE
	OPI 3.14	31	A-terminate, X-terminate cntr rgtr PE

PROC-840, 845, 850, 855, 860, 840S, 845S, 855S, 840A, 850A, 860A, 870A PFS6 REGISTER (86) (Sheet 2 of 2)

Byte	Level 3 Diagram	Bit(s)	Description
	MAC 3.1/8	32	Maint chan out rgtr (to IOU) PE
	MAC 3.8	33	Maint chan input: write data or fctn word PE
	MAC 3.0/8	34	Maint chan input: data fanout PE
4	MAC 3.0/8	35	Read data (to maint chan out rgtr) mux PE
	MAC 3.6/8	36	Reference ROM adrs PE
	MAC 3.5/8	37	Address translation mux PE
	MAC 3.6/8	38	Reference ROM data PE
	OPI 3.14	39	N cntr rgtr PE
	IF 3.1/4	40	First level instr C170 odd RAM A PE
	IF 3.1/4	41	First level instr C170 even RAM A PE
	IF 3.1/4	42	First level instr C180 RAM A PE
5	IF 3.3/4	43	IB12 P rgtr, byte 4
	IF 3.3/4	44	IB12 P rgtr, byte 5
	IF 3.3/4	45	Rank 12 instr bfr opcode
	IF 3.3/4	46	IB12 instr mux bits 3, 12 through 15, 24
	IF 3.3/4	47	IB12 instr mux bits 16 through 23
	IF 3.1/4	48	First level instr C170 odd RAM B PE
	IF 3.1/4	49	First level instr C170 even RAM B PE
	IF 3.1/4	50	First level instr C180 RAM B PE
6	IF 3.3/4	51	IB12 P rgtr, byte 6
	IF 3.3/4	52	IB12 P rgtr, byte 7
	IF 3.3/4	53	IB12 P instr mux bits 33 through 40
	IF 3.3/4	54	IB12 P instr mux bits 25 through 32
		55	(Not used)
	IF 3.5	56	Branch adrs A rgtr PE, byte 0
	IF 3.5	57	Branch adrs A rgtr PE, byte 1
	IF 3.5	58	Branch adrs A rgtr PE, byte 2
7	IF 3.5	59	Branch adrs A rgtr PE, byte 3
	IF 3.5	60	Branch adrs B rgtr PE, byte 1
	IF 3.5	61	Branch adrs B rgtr PE, byte 2
	IF 3.5	62	Branch adrs B rgtr PE, byte 3
	MAC 3.11/9	63	PFS board 3 int PE

Byte	Level 3 Diagram	Bit(s)	Description
	IF 3.5/4	00	Branch adrs adder input PE, byte 0
	IF 3.5/4	01	Branch adrs adder input PE, byte 1
	IF 3.5/4	02	Branch adrs adder input PE, byte 2
0	IF 3.5/4	03	Branch adrs adder input PE, byte 3
	IF 3.5	04	Branch adrs rgtr PE, byte 4
	IF 3.5	05	Branch adrs rgtr PE, byte 5
	IF 3.5	06	Branch adrs rgtr PE, byte 6
	IF 3.5	07	Branch adrs rgtr PE, byte 7
	IF 3.2	08	IB02 PE, byte 0; Instr mux bits 3, 12 through 15, 24
	IF 3.2	09	IB02 PE, byte 1; Instr mux bits 16 through 23
	IF 3.2	10	IB02 PE, byte 2; Instr mux bits 25 through 32
1	IF 3.2	11	IB02 PE, byte 3; Instr mux bits 33 through 40
	IF 3.3	12	IB11 PE, byte 0; Instr mux bits 3, 12 through 15, 24
	IF 3.3	13	IB11 PE, byte 1; Instr mux bits 16 through 23
	IF 3.3	14	IB11 PE, byte 2; Instr mux bits 25 through 32
	IF 3.3	15	IB11 PE, byte 3; Instr mux bits 33 through 40
2		16 through 23	(Not used)
3		24 through 31	(Not used)
4		32 through 39	(Not used)
5		40 through 47	(Not used)
6		48 through 55	(Not used)
7		56 through 63	(Not used)

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PROC-840, 845, 850, 855, 860, 840S, 845S, 855S, 840A, 850A, 860A, 870A PFS8 REGISTER (88) (Sheet 1 of 2)

Byte	Level 3 Diagram	Bit(s)	Description
	IF 3.0/4	00	Instr assy rgtr PE, byte 0
	IF 3.0/4	01	Instr assy rgtr PE, byte 1
	IF 3.0/4	02	Instr assy rgtr PE, byte 2
0	IF 3.0/4	03	Instr assy rgtr PE, byte 3
	IF 3.0/4	04	Instr assy rgtr PE, byte 4
	IF 3.0/4	05	Instr assy rgtr PE, byte 5
	IF 3.0/4	06	Instr assy rgtr PE, byte 6
	IF 3.0/4	07	Instr assy rgtr PE, byte 7
	IF 3.0/4	08	Parcel 3 save rgtr PE, byte 0
	IF 3.0/4	09	Parcel 3 save rgtr PE, byte 1
	IF 3.4	10	P mux PE, byte 0
1	IF 3.4	11	P mux PE, byte 1
	IF 3.4	12	P mux PE, byte 2
	IF 3.4	13	P mux PE, byte 3
	ALN 3.2/24	14	Multiply/divide minor cycle cont rgtr PE, byte 0
	ALN 3.2/24	15	Multiply/divide minor cycle cont rgtr PE, byte 1
	ALN 3.13/24	16	C rgtr data PE, byte 0
	ALN 3.13/24	17	C rgtr data PE, byte 1
	ALN 3.13/24	18	C rgtr data PE, byte 2
2	ALN 3.13/24	19	C rgtr data PE, byte 3
	ALN 3.13/24	20	C rgtr data PE, byte 4
	ALN 3.13/24	21	C rgtr data PE, byte 5
	ALN 3.13/24	22	C rgtr data PE, byte 6
	ALN 3.13/24	23	C rgtr data PE, byte 7
	ALN 3.14/24	24	B rgtr data PE, byte 0
	ALN 3.14/24	25	B rgtr data PE, byte 1
	ALN 3.14/24	26	B rgtr data PE, byte 2
3	ALN 3.14/24	27	B rgtr data PE, byte 3
	ALN 3.14/24	28	B rgtr data PE, byte 4
	ALN 3.14/24	29	B rgtr data PE, byte 5
	ALN 3.14/24	30	B rgtr data PE, byte 6
	ALN 3.14/24	31	B rgtr data PE, byte 7

PROC-840, 845, 850, 855, 860, 840S, 845S, 855S, 840A, 850A, 860A, 870A PFS8 REGISTER (88) (Sheet 2 of 2)

Byte	Level 3 Diagram	Bit(s)	Description
	ALN 3.10	32	Large adder input PE, byte 0
	ALN 3.10	33	Large adder input PE, byte 1
	ALN 3.10	34	Large adder input PE, byte 2
4	ALN 3.10	35	Large adder input PE, byte 3
	ALN 3.10	36	Large adder input PE, byte 4
	ALN 3.10	37	Large adder input PE, byte 5
	ALN 3.10	38	Large adder input PE, byte 6
	ALN 3.10	39	Large adder input PE, byte 7
	ALN 3.10	40	Large adder input PE, byte 8
	ALN 3.10	41	Large adder input PE, byte 9
	ALN 3.10	42	Large adder input PE, byte 10
5	ALN 3.10	43	Large adder input PE, byte 11
	ALN 3.10	44	Large adder byte 0 carry error
	ALN 3.10	45	Large adder byte 1 carry error
	ALN 3.10	46	Large adder byte 2 carry error
	ALN 3.10	47	Large adder byte 3 carry error
	ALN 3.10	48	Large adder byte 4 carry error
	ALN 3.10	49	Large adder byte 5 carry error
	ALN 3.10	50	Large adder byte 6 carry error
6	ALN 3.10	51	Large adder byte 7 carry error
	ALN 3.10	52	Large adder byte 8 carry error
	ALN 3.10	53	Large adder byte 9 carry error
	ALN 3.10	54	Large adder byte 10 carry error
	ALN 3.10	55	Large adder byte 11 carry error
		56,57	(Not used)
	ALN 3.4/24	58	Shift count (from AC) PE, byte 0
7	ALN 3.4/24	59	Shift count (from AC) PE, byte 1
	ALN 3.16/24	60	Multiply final adder carry error, byte 0
	ALN 3.16/24	61	Multiply final adder carry error, byte 1
		62	(Not used)
	MAC 3.11/9	63	PFS board 4 int PE

PROC-840, 845, 850, 855, 860, 840S, 845S, 855S, 840A, 850A, 860A, 870A PFS9 REGISTER (89)

Byte	Level 3 Diagram	Bit(s)	Description
	ALN 3.16/24	00	Multiply final adder carry error, byte 2
	ALN 3.16/24	01	Multiply final adder carry error, byte 3
	ALN 3.16/24	02	Multiply final adder carry error, byte 4
0	ALN 3.16/24	03	Multiply final adder carry error, byte 5
	ALN 3.16/24	04	Multiply final adder carry error, byte 6
	ALN 3.16/24	05	Multiply final adder carry error, byte 7
	ALN 3.16/24	06	Multiply final adder carry error, byte 8
	ALN 3.16/24	07	(Not used)
	ALN 3.0/24	08	ALN micr PE, byte 0
	ALN 3.0/24	09	ALN micr PE, byte 1
	ALN 3.0/24	10	ALN micr PE, byte 2
1	ALN 3.0/24	11	ALN micr PE, byte 3
	ALN 3.0/24	12	ALN micr PE, byte 4
	ALN 3.0/24	13	ALN micr PE, byte 5
	ALN 3.0/24	14	ALN micr PE, byte 6
	ALN 3.3/24	15	ALN micr PE, byte 7
2		16 through 23	(Not used)
3		24 through 31	(Not used)
4		32 through 39	(Not used)
5		40 through 47	(Not used)
6		48 through 55	(Not used)
7		56 through 63	(Not used)

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PROC-840, 845, 850, 855, 860, 840S, 845S, 855S, 840A, 850A, 860A, 870A PTM REGISTER (A0) (Sheet 1 of 2)

Byte	Bit(s)	Description
	00	Address cont, data to length cntr
	01	Address cont, 8-bit adder
	02	Address cont, ALN shift count
0	03	BDP, AJ port formatting
	04	BDP, AK port formatting
	05	BDP, scan rgtr file adrs
	06	BDP, spec error ROM adrs
	07	BDP, encode
	08	IC, test retry hardware
	09	Address cont, mark lines
	10	Local mem, page offset
1	11	Local mem, seg/page identifier
	12	Operand issue, write adrs pipeline input
	13	Operand issue, data subfctn sel
	14	Operand issue, literal data
	15	Instr fetch, instr decode muxes
	16	ALN, force C rgtr PE
	17	ALN, force shift fault
	18	MAC, MAC data output
2	19	CMC partial parity dsbl
	20	CSU partial parity dsbl
	21	(Not used)
	22	Purge adrs cntr parity invert
	23	Page map status parity invert, set 0
	24	Page map status parity invert, set 1
	25	Page map status parity invert, set 2
	26	Page map status parity invert, set 3
3	27	Tag file parity invert
	28	Local mem tag to CMC parity invert
	29	CMC response code parity invert
	30,31	Local mem, RMA

PROC-840, 845, 850, 855, 860, 840S, 845S, 855S, 840A, 850A, 860A, 870A PTM REGISTER (A0) (Sheet 2 of 2)

Byte	Bit(s)	Description
	32,33	Local mem, RMA
	34	Local mem, fctn code
	35	Operand issue, (companion with bit 13)
4	36	Operand issue, force PE on RDSW to instr cntr
	37	Operand issue, force PE on microsecond cntr
	38	(Not used)
	39	Force cache set 1 allocate
	40	Force tag file 0 valid
	41	Force tag file 1 valid
	42	Force tag file 2 valid
5	43	Force LM tag PE
	44	Force minipipe PE
	45 through 47	(Not used)
6	48 through 55	(Always zero)
7	56 through 63	(Always zero)

PROC-990, 992, 994, 990E, 995E DEC REGISTER (30) (Sheet 1 of 4)

Byte	Bit(s)	Due	Level 3 Diagram	Level 4 Diagram	Unit	Signal Name	Description	FRU
	00		INU 3.5B	IN1 4.3-04	IN1	GOSETXO	Dsbl IBS set 0	
	01		INU 3.5B	IN1 4.3-04	IN1	GOSETX1	Dsbl IBS set 1	
	02		INU 3.5B	IN1 4.3-04	IN1	GOSETX2	Dsbl IBS set 2	
	03		INU 3.5B	IN1 4.3-04	IN1	GOSETX3	Dsbl IBS set 3	
0	04		INU 3.2D	IN1 4.0-02	IN1	MAXLAC0	Set max lookahead count bit 4	
	05		INU 3.2D	IN1 4.0-02	IN1	MAXLAC1	Set max lookahead count bit 5	
	06		INU 3.2D	IN1 4.0-02	IN1	MAXLAC2	Set max lookahead count bit 6	
	07		INU 3.2D	IN1 4.0-02	IN1	MAXLAC3	Set max lookahead count bit 7	
	08		AC1 3.27A	AC1 4.2-11	AC1	PEMSSG	Force miss on seg map PE	
	09		AC2 3.10C	AC2 4.3-00	AC2	PEMSPG	Force miss on page map PE	
	10		AC1 3.29C	AC1 4.2-06	AC1	ENBSMO	Enbl seg map 0	
1	11		AC1 3.29C	AC1 4.2-06	AC1	ENBSM1	Enbl seg map 1	
	12		AC2 3.8D	AC2 4.0-07	AC2	ENBPM0	Enbl page map set 0	
	13		AC2 3.8D	AC2 4.0-07	AC2	ENBPM1	Enbl page map set 1	
	14		AC2 3.8D	AC2 4.0-07	AC2	ENBPM2	Enbl page map set 2	
	15		AC2 3.8D	AC2 4.0-07	AC2	ENBPM3	Enbl page map set 3	
	16		PSR 3.0E	PSR 4.0-02	PSR	ENERRC	Enbl MC of the asynchronous error bfr	
	17		PSR 3.8B	PSR 4.5B-03	PSR	EHLTER	Enbl halt on error	
	18		PSR 3.0F	PMF 4.0-08	PMF	ICBSTR	Enbl start fctn/DUE to trigger capture bfr	
2	19		DIV 3.7C	DIV 4.0-31	SCU	NETSELO	Div net result sel bit 0	
	20		DIV 3.7C	DIV 4.0-31	SCU	NETSEL1	Div net result sel bit 1	
	21		DIV 3.7C	DIV 4.0-31	SCU	NETSEL2	Div net sel for compare bit 0	
	22		DIV 3.7C	DIV 4.0-31	SCU	NETSEL3	Div net sel for compare bit 1	
	23		DIV 3.7C	DIV 4.0-31	SCU	NETSEL4	Enbl maint mode	
	24		OCA 3.7C	OCA 4.7-04	OCA	DESTALE	Dsbl stale data	
	25						(Not used)	
	26		INU 3.19A	IN2 4.0-15	IN2	DISTMR	Dsbl issue timer	
3	27		INU 3.19A	IN2 4.0-15	IN2	DECTM0	DEC timeout interval cont bit 0	
	28		INU 3.19A	IN2 4.0-15	IN2	DECTM1	DEC timeout interval cont bit 1	
	29		INU 3.19A	IN2 4.0-15	IN2	DECTM2	DEC timeout interval cont bit 2	
	30		INU 3.19A	IN2 4.0-15	IN2	DECTM3	DEC timeout interval cont bit 3	
	31		INU 3.19A	IN2 4.0-15	IN2	DECTM4	DEC timeout interval cont bit 4	

PROC-990, 992, 994, 990E, 995E DEC REGISTER (30) (Sheet 2 of 4)

Byte	Bit(s)	Due	Level 3 Diagram	Level 4 Diagram	Unit	Signal Name	Description	FRU
	32		AC1 3.32A	AC1 4.4-00	AC1	ENPLMC	Enbl P left MC	
	33		MAC 3.3B	MAC 4.1-05	MAC	DCBT33	Enbl PTM sel	
	34		PMF 3.3B	PMF 4.1-02	PMF	DECCNT	Test event state cntrs rgtr	
4	35		MAC 3.6D	MAC 4.0-20	MAC	DCBT35	Enbl cor error cond	
	36		PSR 3.14A	PSR 4.4-04	PSR	MSTMON	Master set monitor mode	
	37		AC1 3.29C	AC1 4.2-06	AC1	ENSGMC	Enbl seg map MC	
	38		AC2 3.8D	AC2 4.0-07	AC2	ENPGMC	Enbl page map MC	
	39		EPN 3.8A	EPN 4.13-00	EPN	LNGMCN	Enbl initialize on MAC access	
	40		PSR 3.10A	PSR 4.4-05	PSR	ITRCNT0	Initialize retry cntr set bit 0	
	41		PSR 3.10A	PSR 4.4-05	PSR	ITRCNT1	Initialize retry cntr set bit 1	
	42		PSR 3.10A	PSR 4.4-05	PSR	ITRCNT2	Initialize retry cntr set bit 2	
	43		PSR 3.10A	PSR 4.4-05	PSR	ITRCNT3	Initialize retry cntr set bit 3	
	44		IDU 3.21A	IDU 4.7-11	IDU	DECBPE	Enbl CSA bkpt halt	
	44		INU 3.18B	IN2 4.0-04	IN2	NDECBP	Breakpoint enbl	
5	45		IDU 3.21A	IDU 4.7-11	IDU	DECCMP	Enbl PFS-CSA bkpt compare	
	46		IDU 3.21C	IDU 4.7-07	IDU	DECMHT	Set microcode halted	
	46		INU 3.18A	IN2 4.0-00	IN2	DECPRG	CIR purge	
	47		EPN 3.2F	EPN 4.6-00	EPN	DCBT47	Dsbl errors	
	47		IDU 3.8A	IDU 4.2-12	IDU	DECDER	Enbl CWD error tags	
	47		INU 3.11B	IN1 4.7-01	IN1	DBADEC	Complement of DCBT 47	
	47		AC1 3.37B	AC2 4.4-01	AC1	NPDM	Block DUE error	
			AC2 3.27C	AC1 4.8-12	AC2	BLKDUE	Dsbl PDMs	
	48		OCA 3.10B,J	OCA 4.0-05	OCA	PREFWD	Enbl prefetch forward	
	49		OCA 3.10B,J	OCA 4.0-05	OCA	PREREV	Enbl prefetch reverse	
	50		OCA 3.10B	OCA 4.1-04	OCA	PRESTO	Enbl prefetch on all stores	
6	51		OCA 3.10B	OCA 4.1-04	OCA	PSTORO	Enbl prefetch on stores to word 0	
	52		OCA 3.10B	OCA 4.1-04	OCA	PSTOR3	Enbl prefetch on stores to word 3	
	53		OCA 3.10B	OCA 4.1-04	OCA	PREMIS	Enbl prefetch on miss	
	54		AC1 3.15B	AC1 4.0-01	AC1	INC32B	Incr prefetch by 32 bytes	
	55		AC1 3.15B	AC1 4.0-00	AC1	INC64B	Incr prefetch by 64 bytes	

PROC-990, 992, 994, 990E, 995E DEC REGISTER (30) (Sheet 3 of 4)

Byte	Bit(s)	Due	Level 3 Diagram	Level 4 Diagram	Unit	Signal Name	Description	FRU
	56		OCA 3.7K	OCA 4.0-04	OCA	ENABS0	Enbl set 0	
	57		OCA 3.7K	OCA 4.0-04	OCA	ENABS1	Enbl set 1	
	58		OCA 3.7K	OCA 4.0-04	OCA	ENABS2	Enbl set 2	
7	59		OCA 3.7K	OCA 4.0-04	OCA	ENABS3	Enbl set 3	
	60		INU 3.12A	IN1 4.7-04	IN1	BRNDEC	Force predict branch taken	
	61		OCA 3.11B		OCA	OCASTP	OCA serial mode	
	62		AC1 3.28B		AC1	RMAMOD	Bypass seg map	
			AC2 3.8A	AC2 4.0-024	AC2	FRCRMA	Bypass page map	
	63		PSR 3.18B	PSR 4.6A-08	PSR	CDVMID	PSR VMID initial value	

PROC-990, 992, 994, 990E, 995E DEC REGISTER (30) (Sheet 4 of 4)

DIVIDE NETS (DEC BITS 19-23)*

NET	RESULT 19,20	COMPARE 21,22	ENABLE 23
1	00	00	1
2	01	01	1
3	10	10	1
4	11	11	1

*Use the indicated values for bits 19-23 to compare a divide net to itself.

DUE definition for registers 80-8F:
I = Imprecise DUE (nonretryable)
P = Precise DUE (retryable)
P,I = Precise or imprecise DUE
N = Nonretryable DUE

PROC-990, 992, 994, 990E, 995E PFS0 REGISTER (80) (Sheet 1 of 2)

Byte	Bit(s)	Due	Level 3 Diagram	Level 4 Diagram	Unit	Signal Name	Description	FRU
	00		PSR 3.11F	PSR 4.5B-02	PSR	DUEMAC	Detected uncor error	151-2B5FU-B01
	01		PSR 3.11F	PSR 4.5B-02	PSR	CORERR	Corrected error	151-2B5FU-B01
	02		MAC 3.0A	MAC 4.0-03	MAC	PFS32	IOU data PE	0FVH-1D1-EL
0	03		MAC 3.8B	MAC 4.1-03	MAC	PFS33	Read mux PE	CB-1D1-H09
	04		MAC 3.6B	MAC 4.1-09	MAC	PFS34	Initial cont store adrs rgtr, byte 0	CE-1D1-J11
	05		MAC 3.6B	MAC 4.1-09	MAC	PFS35	Initial cont store adrs rgtr, byte 1	CE-1D1-J11
	06		MAC 3.6B	MAC 4.1-09	MAC	PFS36	Control store bkpt rgtr, byte 0	CE-1D1-K11
	07		MAC 3.6B	MAC 4.1-09	MAC	PFS37	Control store bkpt rgtr, byte 1	CE-1D1-K11
	08		MAC 3.7A	MAC 4.1-08	MAC	PFS0	MAC copy data out rgtr, byte 0	CE-1D1-G15
	09		MAC 3.7A	MAC 4.1-08	MAC	PFS1	MAC copy data out rgtr, byte 1	CE-1D1-G15
	10		MAC 3.7A	MAC 4.1-08	MAC	PFS2	MAC copy data out rgtr, byte 2	CE-1D1-H15
1	11		MAC 3.7A	MAC 4.1-08	MAC	PFS3	MAC copy data out rgtr, byte 3	CE-1D1-H15
	12		MAC 3.7A	MAC 4.1-08	MAC	PFS4	MAC copy data out rgtr, byte 4	CE-1D1-J15
	13		MAC 3.7A	MAC 4.1-08	MAC	PFS5	MAC copy data out rgtr, byte 5	CE-1D1-J15
	14		MAC 3.7A	MAC 4.1-08	MAC	PFS6	MAC copy data out rgtr, byte 6	CE-1D1-K15
	15		MAC 3.7A	MAC 4.1-08	MAC	PFS7	MAC copy data out rgtr, byte 7	CE-1D1-K15
	16		MAC 3.7B	MAC 4.1-10	MAC	PFS8	MAC disassy rgtr, byte 0	CB-1D1-G14
	17		MAC 3.7B	MAC 4.1-10	MAC	PFS9	MAC disassy rgtr, byte 1	CB-1D1-H14
	18		MAC 3.7B	MAC 4.1-10	MAC	PFS10	MAC disassy rgtr, byte 2	CB-1D1-J14
2	19		MAC 3.7B	MAC 4.1-10	MAC	PFS11	MAC disassy rgtr, byte 3	CB-1D1-K14
	20		MAC 3.7B	MAC 4.1-10	MAC	PFS12	MAC disassy rgtr, byte 4	CB-1D1-G13
	21		MAC 3.7B	MAC 4.1-10	MAC	PFS13	MAC disassy rgtr, byte 5	CB-1D1-H13
	22		MAC 3.7B	MAC 4.1-10	MAC	PFS14	MAC disassy rgtr, byte 6	CB-1D1-J13
	23		MAC 3.7B	MAC 4.1-10	MAC	PFS15	MAC disassy rgtr, byte 7	CB-1D1-K13
	24	I	MAC 3.4B	MAC 4.1-04	MAC	PFS16	Copy data in rgtr, byte 0	CB-1D1-A15
	25	I	MAC 3.4B	MAC 4.1-04	MAC	PFS17	Copy data in rgtr, byte 1	CE-1D1-A15
	26	I	MAC 3.4B	MAC 4.1-04	MAC	PFS18	Copy data in rgtr, byte 2	CE-1D1-A13
3	27	I	MAC 3.4B	MAC 4.1-04	MAC	PFS19	Copy data in rgtr, byte 3	CE-1D1-A13
	28	I	MAC 3.4B	MAC 4.1-04	MAC	PFS20	Copy data in rgtr, byte 4	CE-1D1-A12
	29	I	MAC 3.4B	MAC 4.1-04	MAC	PFS21	Copy data in rgtr, byte 5	CE-1D1-A12
	30	I	MAC 3.4B	MAC 4.1-04	MAC	PFS22	Copy data in rgtr, byte 6	CE-1D1-A11
	31	I	MAC 3.4B	MAC 4.1-04	MAC	PFS23	Copy data in rgtr, byte 7	CE-1D1-A11

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Byte	Bit(s)	Due	Level 3 Diagram	Level 4 Diagram	Unit	Signal Name	Description	FRU
	32		MAC 3.4A	MAC 4.1-05	MAC	PFS24	MAC assy rgtr, byte 0	CE-1D1-A01
	33		MAC 3.4A	MAC 4.1-05	MAC	PFS25	MAC assy rgtr, byte 1	CE-1D1-A01
	34		MAC 3.4A	MAC 4.1-05	MAC	PFS26	MAC assy rgtr, byte 2	CE-1D1-A03
4	35		MAC 3.4A	MAC 4.1-05	MAC	PFS27	MAC assy rgtr, byte 3	CE-1D1-A03
	36		MAC 3.4A	MAC 4.1-05	MAC	PFS28	MAC assy rgtr, byte 4	CE-1D1-A04
	37		MAC 3.4A	MAC 4.1-05	MAC	PFS29	MAC assy rgtr, byte 5	CE-1D1-A04
	38		MAC 3.4A	MAC 4.1-05	MAC	PFS30	MAC assy rgtr, byte 6	CE-1D1-A05
	39		MAC 3.4A	MAC 4.1-05	MAC	PFS31	MAC assy rgtr, byte 7	CE-1D1-A05
	40	I	RGU 3.8B	RGU 4.19-00	RGU	PFS0	History file X output data rgtr, byte 0	CB-1C1-A08
	41	I	RGU 3.8B	RGU 4.19-00	RGU	PFS1	History file X output data rgtr, byte 1	CB-1C1-A09
	42	I	RGU 3.8B	RGU 4.19-00	RGU	PFS2	History file X output data rgtr, byte 2	CB-1C1-B08
5	43	I	RGU 3.8B	RGU 4.19-00	RGU	PFS3	History file X output data rgtr, byte 3	CB-1C1-C07
	44	I	RGU 3.8B	RGU 4.19-00	RGU	PFS4	History file X output data rgtr, byte 4	CB-1C1-F07
	45	I	RGU 3.8B	RGU 4.19-00	RGU	PFS5	History file X output data rgtr, byte 5	CB-1C1-F08
	46	I	RGU 3.8B	RGU 4.19-00	RGU	PFS6	History file X output data rgtr, byte 6	CB-1C1-G08
	47	I	RGU 3.8B	RGU 4.19-00	RGU	PFS7	History file X output data rgtr, byte 7	CB-1C1-H09
	48	I	RGU 3.8B	RGU 4.19-00	RGU	PFS8	History file A output data rgtr, byte 2	CB-1C1-B09
	49	I	RGU 3.8B	RGU 4.19-00	RGU	PFS9	History file A output data rgtr, byte 3	CB-1C1-C09
	50	I	RGU 3.8B	RGU 4.19-00	RGU	PFS10	History file A output data rgtr, byte 4	CB-1C1-D07
6	51	I	RGU 3.8B	RGU 4.19-00	RGU	PFS11	History file A output data rgtr, byte 5	CB-1C1-D08
	52	I	RGU 3.8B	RGU 4.19-00	RGU	PFS12	History file A output data rgtr, byte 6	CB-1C1-G09
	53	I	RGU 3.8B	RGU 4.19-00	RGU	PFS13	History file A output data rgtr, byte 7	CB-1C1-H10
	54	I	RGU 3.8B	RGU 4.19-00	RGU	PFS14	History file mem P-right, byte 0	CU-1C1-F12
	55	I	RGU 3.8B	RGU 4.19-00	RGU	PFS15	History file mem P-right, byte 1	CU-1C1-F12
	56	I	RGU 3.8B	RGU 4.19-00	RGU	PFS16	History file mem P-right, byte 2	CU-1C1-F12
	57	I	RGU 3.8B	RGU 4.19-00	RGU	PFS17	History file mem P-right, byte 3	CU-1C1-F12
	58	I	RGU 3.8B	RGU 4.19-00	RGU	PFS18	History file mem MAC or IDU enter sel	CU-1C1-F12
7	59						(Not used)	
	60		IDU 3.21A	IDU 4.7-11	RGU	PFS128	PFS-CSA bkpt compare	CU-1D5-D11
	61		IDU 3.21A	IDU 4.7-11	RGU	PFS129	CSA bkpt halt	CU-1D5-D11
	62	I	IDU 3.21A	IDU 4.7-09	RGU	PFS130	CSA sequencing error	0GAH-2D3-GL
	63	I	IDU 3.17P	IDU 4.6-02	RGU	PFS131	CS/CW mem access error validation	HE-2D2-H09B

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Byte	Bit(s)	Due	Level 3 Diagram	Level 4 Diagram	Unit	Signal Name	Description	FRU
	00		IDU 3.20C	IDU 4.7-04	IDU	PFS112	MAC write data assy rgtr PE, byte 0	CU-1D1-C04
	01		IDU 3.20C	IDU 4.7-04	IDU	PFS113	MAC write data assy rgtr PE, byte 1	CU-1D5-C04
	02		IDU 3.20C	IDU 4.7-04	IDU	PFS114	MAC write data assy rgtr PE, byte 2	CU-1D5-D05
0	03		IDU 3.20C	IDU 4.7-04	IDU	PFS115	MAC write data assy rgtr PE, byte 3	CU-1D5-D05
	04		IDU 3.20C	IDU 4.7-04	IDU	PFS116	MAC write data assy rgtr PE, byte 4	CU-1D5-E04
	05		IDU 3.20C	IDU 4.7-04	IDU	PFS117	MAC write data assy rgtr PE, byte 5	CU-1D5-E04
	06		IDU 3.20C	IDU 4.7-04	IDU	PFS118	MAC write data assy rgtr PE, byte 6	CU-1D5-F04
	07		IDU 3.20C	IDU 4.7-04	IDU	PFS119	MAC write data assy rgtr PE, byte 7	CU-1D5-F04
	08		IDU 3.20C	IDU 4.7-04	IDU	PFS120	MAC write data assy rgtr PE, byte 8	CU-1D5-G03
	09		IDU 3.20C	IDU 4.7-04	IDU	PFS121	MAC write data assy rgtr PE, byte 9	CU-1D5-G03
	10		IDU 3.20C	IDU 4.7-04	IDU	PFS122	MAC write data assy rgtr PE, byte 10	CU-1D5-H03
1	11		IDU 3.20C	IDU 4.7-04	IDU	PFS123	MAC write data assy rgtr PE, byte 11	CU-1D5-H03
	12		IDU 3.20C	IDU 4.7-04	IDU	PFS124	MAC write data assy rgtr PE, byte 12	CU-1D5-J03
	13		IDU 3.20C	IDU 4.7-04	IDU	PFS125	MAC write data assy rgtr PE, byte 13	CU-1D5-J03
	14		IDU 3.20C	IDU 4.7-04	IDU	PFS126	MAC write data assy rgtr PE, byte 14	CU-1D5-K03
	15		IDU 3.20C	IDU 4.7-04	IDU	PFS127	MAC write data assy rgtr PE, byte 15	CU-1D5-K03
	16	P,I	IDU 3.8A	IDU 4.2-10	IDU	PFS36	CST data PE byte 8 or SM mem check 0	AF-2D2-J11
	17	P,I	IDU 3.8A	IDU 4.2-10	IDU	PFS38	CST data PE byte 9 or SM mem check 1	AF-2D2-J11
	18	P,I	IDU 3.8A	IDU 4.2-10	IDU	PFS40	CST data PE byte 10 or SM mem check 2	AF-2D2-J11
2	19	P,I	IDU 3.8A	IDU 4.2-10	IDU	PFS42	CST data PE byte 11 or SM mem check 3	AF-2D2-J11
	20	P,I	IDU 3.8A	IDU 4.2-10	IDU	PFS44	CST data PE, byte 12 or SM mem check 4	AF-2D2-J09
	21	P,I	IDU 3.8A	IDU 4.2-10	IDU	PFS46	CST data PE byte 13 or SM mem check 5	AF-2D2-J09
	22	P,I	IDU 3.8A	IDU 4.2-10	IDU	PFS48	CST data PE byte 14 or SM mem check 6	AF-2D2-J09
	23	P,I	IDU 3.8A	IDU 4.2-10	IDU	PFS50	CST data PE byte 15 or SM mem check 7	AF-2D2-J09
	24	P,I	IDU 3.8A	IDU 4.2-10	IDU	PFS37	CST data PE, byte 0 or 16	AF-2D2-J11
	25	P,I	IDU 3.8A	IDU 4.2-10	IDU	PFS39	CST data PE, byte 1 or 17	AF-2D2-J11
	26	P,I	IDU 3.8A	IDU 4.2-10	IDU	PFS41	CST data PE, byte 2 or 18	AF-2D2-J11
3	27	P,I	IDU 3.8A	IDU 4.2-10	IDU	PFS43	CST data PE, byte 3 or 19	AF-2D2-J11
	28	P,I	IDU 3.8A	IDU 4.2-10	IDU	PFS45	CST data PE, byte 4 or 20	AF-2D2-J09
	29	P,I	IDU 3.8A	IDU 4.2-10	IDU	PFS47	CST data PE, byte 5 or 21	AF-2D2-J09
	30	P,I	IDU 3.8A	IDU 4.2-10	IDU	PFS49	CST data PE, byte 6 or 22	AF-2D2-J09
	31	P,I	IDU 3.8A	IDU 4.2-10	IDU	PFS51	CST data PE, byte 7 or 23	AF-2D2-J09

PROC 990, 992, 994, 990E, 995E PFS1 REGISTER (81) (Sheet 2 of 2)

Byte	Bit(s)	Due	Level 3 Diagram	Level 4 Diagram	Unit	Signal Name	Description	FRU
	32	I	IDU 3.8A	IDU 4.2-13	IDU	PFS76	CIR cont word PE, byte 0	CU-1D5-K07
	33	I	IDU 3.8A	IDU 4.2-13	IDU	PFS79	CIR cont word PE, byte 3	CU-1D5-K07
	34	I	IDU 3.8A	IDU 4.2-13	IDU	PFS82	CIR cont word PE, byte 6	CU-1D5-K07
4	35	I	IDU 3.8A	IDU 4.2-13	IDU	PFS85	CIR cont word PE, byte 9	CU-1D5-K07
	36	I	IDU 3.8A	IDU 4.2-13	IDU	PFS88	CIR cont word PE, byte 12	CU-1D5-K07
	37	I	IDU 3.8A	IDU 4.2-13	IDU	PFS91	CIR cont word PE, byte 15	CU-1D5-K07
	38	I	IDU 3.8A	IDU 4.2-13	IDU	PFS94	CIR cont word PE, byte 18	CU-1D5-C08
	39	I	IDU 3.8A	IDU 4.2-13	IDU	PFS97	CIR cont word PE, byte 21	CU-1D5-C08
	40	I	IDU 3.8A	IDU 4.2-13	IDU	PFS77	CIR cont word PE, byte 1	CU-1D5-K07
	41	I	IDU 3.8A	IDU 4.2-13	IDU	PFS80	CIR cont word PE, byte 4	CU-1D5-K07
	42	I	IDU 3.8A	IDU 4.2-13	IDU	PFS83	CIR cont word PE, byte 7	CU-1D5-K07
5	43	I	IDU 3.8A	IDU 4.2-13	IDU	PFS86	CIR cont word PE, byte 10	CU-1D5-K07
	44	I	IDU 3.8A	IDU 4.2-13	IDU	PFS89	CIR cont word PE, byte 13	CU-1D5-K07
	45	I	IDU 3.8A	IDU 4.2-13	IDU	PFS92	CIR cont word PE, byte 16	CU-1D5-C08
	46	I	IDU 3.8A	IDU 4.2-13	IDU	PFS95	CIR cont word PE, byte 19	CU-1D5-C08
	47	I	IDU 3.8A	IDU 4.2-13	IDU	PFS98	CIR cont word PE, byte 22	CU-1D5-C08
	48	I	IDU 3.8A	IDU 4.2-13	IDU	PFS78	CIR cont word PE, byte 2	CU-1D5-K07
	49	I	IDU 3.8A	IDU 4.2-13	IDU	PFS81	CIR cont word PE, byte 5	CU-1D5-K07
	50	I	IDU 3.8A	IDU 4.2-13	IDU	PFS84	CIR cont word PE, byte 8	CU-1D5-K07
6	51	I	IDU 3.8A	IDU 4.2-13	IDU	PFS87	CIR cont word PE, byte 11	CU-1D5-K07
	52	I	IDU 3.8A	IDU 4.2-13	IDU	PFS90	CIR cont word PE, byte 14	CU-1D5-K07
	53	I	IDU 3.8A	IDU 4.2-13	IDU	PFS93	CIR cont word PE, byte 17	CU-1D5-C08
	54	I	IDU 3.8A	IDU 4.2-13	IDU	PFS96	CIR cont word PE, byte 20	CU-1D5-C08
	55	I	IDU 3.8A	IDU 4.2-13	IDU	PFS99	CIR cont word PE, byte 23	CU-1D5-C08
	56		IDU 3.14B	IDU 4.4-01	IDU	PFS72	CWD BDP descr PE, byte 0	CB-2D1-G03
	57		IDU 3.14B	IDU 4.4-01	IDU	PFS73	CWD BDP descr PE, byte 1	CB-2D1-H03
	58		IDU 3.14B	IDU 4.4-01	IDU	PFS74	CWD BDP descr PE, byte 2	CB-2D1-J03
7	59		IDU 3.14B	IDU 4.4-01	IDU	PFS75	CWD BDP descr PE, byte 3	CB-2D1-K03
	60	I	IDU 3.8A	IDU 4.2-13	IDU	PFS108	CIR BDP descr PE, byte 0	CU-1D5-F12
	61	I	IDU 3.8A	IDU 4.2-13	IDU	PFS109	CIR BDP descr PE, byte 1	CU-1D5-F12
	62	I	IDU 3.8A	IDU 4.2-13	IDU	PFS110	CIR BDP descr PE, byte 2	CU-1D5-F12
	63	I	IDU 3.8A	IDU 4.2-13	IDU	PFS111	CIR BDP descr PE, byte 3	CU-1D5-F12

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Byte	Bit(s)	Due	Level 3 Diagram	Level 4 Diagram	Unit	Signal Name	Description	FRU
	00		IDU 3.7A	IDU 4.2-00	IDU	PFS0	CSA P-rgtr PE, byte 4	CB-2D3-H14
	01		IDU 3.7A	IDU 4.2-00	IDU	PFS1	CSA P-rgtr PE, byte 5	CB-2D3-H15
	02		IDU 3.7A	IDU 4.2-00	IDU	PFS2	CSA P-rgtr PE, byte 6	CB-2D3-J15
0	03		IDU 3.7A	IDU 4.2-00	IDU	PFS3	CSA P-rgtr PE, byte 7	CB-2D3-K15
	04		IDU 3.7C	IDU 4.2-00	IDU	PFS20	CSD P-rgtr PE, byte 4	CE-2D3-H02
	05		IDU 3.7C	IDU 4.2-00	IDU	PFS21	CSD P-rgtr PE, byte 5	CE-2D3-H02
	06		IDU 3.7C	IDU 4.2-00	IDU	PFS22	CSD P-rgtr PE, byte 6	CE-2D3-J02
	07		IDU 3.7C	IDU 4.2-00	IDU	PFS23	CSD P-rgtr PE, byte 7	CE-2D3-J02
	08		IDU 3.11E	IDU 4.5H-03	IDU	PFS60	CWA P-rgtr PE, byte 4	0GAH-2D2-GL
	09		IDU 3.11E	IDU 4.5G-03	IDU	PFS61	CWA P-rgtr PE, byte 5	0GAH-2D2-GU
	10		IDU 3.11E	IDU 4.5F-03	IDU	PFS62	CWA P-rgtr PE, byte 6	0GAH-2D2-FL
1	11		IDU 3.11E	IDU 4.5E-03	IDU	PFS63	CWA P-rgtr PE, byte 7	0GAH-2D2-FU
	12	I	IDU 3.8A	IDU 4.5H-03	IDU	PFS100	CIR P-rgtr PE, byte 4	0GAH-2D2-GL
	13	I	IDU 3.8A	IDU 4.5G-03	IDU	PFS101	CIR P-rgtr PE, byte 5	0GAH-2D2-GU
	14	I	IDU 3.8A	IDU 4.5F-03	IDU	PFS102	CIR P-rgtr PE, byte 6	0GAH-2D2-FL
	15	I	IDU 3.8A	IDU 4.5E-03	IDU	PFS103	CIR P-rgtr PE, byte 7	0GAH-2D2-FU
	16		IDU 3.7A	IDU 4.2-00	IDU	PFS4	CSA UTP rgtr PE, byte 0	CU-2D3-K14
	17		IDU 3.7A	IDU 4.2-00	IDU	PFS5	CSA UTP rgtr PE, byte 1	CU-2D3-K14
	18		IDU 3.7A	IDU 4.2-00	IDU	PFS6	CSA UTP rgtr PE, byte 2	CU-2D3-K13
2	19		IDU 3.7A	IDU 4.2-00	IDU	PFS7	CSA UTP rgtr PE, byte 3	CU-2D3-K13
	20		IDU 3.11E	IDU 4.5D-03	IDU	PFS64	CWA UTP rgtr PE, byte 0	0GAH-2D2-EL
	21		IDU 3.11E	IDU 4.5C-03	IDU	PFS65	CWA UTP rgtr PE, byte 1	0GAH-2D2-EU
	22		IDU 3.11E	IDU 4.5B-03	IDU	PFS66	CWA UTP rgtr PE, byte 2	0GAH-2D2-DL
	23		IDU 3.11E	IDU 4.5A-03	IDU	PFS67	CWA UTP rgtr PE, byte 3	0GAH-2D2-DU
	24	I	IDU 3.8A	IDU 4.5D-03	IDU	PFS104	CIR UTP rgtr PE, byte 0	0GAH-2D2-EL
	25	I	IDU 3.8A	IDU 4.5C-03	IDU	PFS105	CIR UTP rgtr PE, byte 1	0GAH-2D2-EU
	26	I	IDU 3.8A	IDU 4.5B-03	IDU	PFS106	CIR UTP rgtr PE, byte 2	0GAH-2D2-DL
3	27	I	IDU 3.8A	IDU 4.5A-03	IDU	PFS107	CIR UTP rgtr PE, byte 3	0GAH-2D2-DU
	28		IDU 3.7A	IDU 4.2-01	IDU	PFS8	CSA instr rgtr PE, byte 0	CU-2D3-A15
	29		IDU 3.7A	IDU 4.2-01	IDU	PFS9	CSA instr rgtr PE, byte 1	CU-2D3-A15
	30		IDU 3.7A	IDU 4.2-01	IDU	PFS10	CSA instr rgtr PE, byte 2	CU-2D3-B15
	31		IDU 3.7A	IDU 4.2-01	IDU	PFS11	CSA instr rgtr PE, byte 3	CU-2D3-B15

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Byte	Bit(s)	Due	Level 3 Diagram	Level 4 Diagram	Unit	Signal Name	Description	FRU
	32		IDU 3.7C	IDU 4.2-01	IDU	PFS24	CSD instr rgtr PE, byte 0	CE-2D3-H05
	33		IDU 3.7C	IDU 4.2-01	IDU	PFS25	CSD instr rgtr PE, byte 1	CE-2D3-H05
	34		IDU 3.7C	IDU 4.2-01	IDU	PFS26	CSD instr rgtr PE, byte 2	CE-2D3-J05
4	35		IDU 3.7C	IDU 4.2-01	IDU	PFS27	CSD instr rgtr PE, byte 3	CU-2D3-J05
	36	I	IDU 3.11D	IDU 4.2-05	IDU	PFS68	CWA instr rgtr PE, byte 0	HE-2D1-H11B
	37	I	IDU 3.11D	IDU 4.2-05	IDU	PFS69	CWA instr rgtr PE, byte 1	HE-2D1-H11B
	38	I	IDU 3.11D	IDU 4.2-05	IDU	PFS70	CWA instr rgtr PE, byte 2	HE-2D1-H11B
	39	I	IDU 3.11D	IDU 4.2-05	IDU	PFS71	CWA instr rgtr PE, byte 3	HE-2D1-H11B
	40		IDU 3.7A	IDU 4.2-02	IDU	PFS12	CSA first BDP descr PE, byte 0	CE-2D3-B13
	41		IDU 3.7A	IDU 4.2-02	IDU	PFS13	CSA first BDP descr PE, byte 1	CE-2D3-B13
	42		IDU 3.7A	IDU 4.2-02	IDU	PFS14	CSA first BDP descr PE, byte 2	CE-2D3-B14
5	43		IDU 3.7A	IDU 4.2-02	IDU	PFS15	CSA first BDP descr PE, byte 3	CE-2D3-B14
	44		IDU 3.7C	IDU 4.2-02	IDU	PFS28	CSD first BDP descr PE, byte 0	CE-2D3-J03
	45		IDU 3.7C	IDU 4.2-02	IDU	PFS29	CSD first BDP descr PE, byte 1	CE-2D3-J03
	46		IDU 3.7C	IDU 4.2-02	IDU	PFS30	CSD first BDP descr PE, byte 2	CE-2D3-H03
	47		IDU 3.7C	IDU 4.2-02	IDU	PFS31	CSD first BDP descr PE, byte 3	CE-2D3-H03
	48		IDU 3.11B	IDU 4.2-04	IDU	PFS52	CWA first BDP descr PE, byte 0	CE-2D1-J12
	49		IDU 3.11B	IDU 4.2-04	IDU	PFS53	CWA first BDP descr PE, byte 1	CE-2D1-J12
	50		IDU 3.11B	IDU 4.2-04	IDU	PFS54	CWA first BDP descr PE, byte 2	CE-2D1-J13
6	51		IDU 3.11B	IDU 4.2-04	IDU	PFS55	CWA first BDP descr PE, byte 3	CE-2D1-J13
	52		IDU 3.7A	IDU 4.2-02	IDU	PFS16	CSA last/only BDP descr PE, byte 0	CE-2D3-C14
	53		IDU 3.7A	IDU 4.2-02	IDU	PFS17	CSA last/only BDP descr PE, byte 1	CE-2D3-C14
	54		IDU 3.7A	IDU 4.2-02	IDU	PFS18	CSA last/only BDP descr PE, byte 2	CE-2D3-C15
	55		IDU 3.7A	IDU 4.2-02	IDU	PFS19	CSA last/only BDP descr PE, byte 3	CE-2D3-C15
	56		IDU 3.7C	IDU 4.2-02	IDU	PFS32	CSD last/only BDP descr PE, byte 0	CE-2D3-J04
	57		IDU 3.7C	IDU 4.2-02	IDU	PFS33	CSD last/only BDP descr PE, byte 1	CE-2D3-J04
	58		IDU 3.7C	IDU 4.2-02	IDU	PFS34	CSD last/only BDP descr PE, byte 2	CE-2D3-H04
7	59		IDU 3.7C	IDU 4.2-02	IDU	PFS35	CSD last/only BDP descr PE, byte 3	CE-2D3-H04
	60		IDU 3.11C	IDU 4.2-04	IDU	PFS56	CWA last/only BDP descr PE, byte 0	CE-2D1-H12
	61		IDU 3.11C	IDU 4.2-04	IDU	PFS57	CWA last/only BDP descr PE, byte 1	CE-2D1-H12
	62		IDU 3.11C	IDU 4.2-04	IDU	PFS58	CWA last/only BDP descr PE, byte 2	CE-2D1-H13
	63		IDU 3.11C	IDU 4.2-04	IDU	PFS59	CWA last/only BDP descr PE, byte 3	CE-2D1-H13

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Byte	Bit(s)	Due	Level 3 Diagram	Level 4 Diagram	Unit	Signal Name	Description	FRU
	00-02						(Not used)	
	03	I	BDP 3.3A	BDP 4.0-08	BDP	PFS59	SC right invalid operand	FT-1C2-EL
0	04	I	BDP 3.3A	BDP 4.0-08	BDP	PFS60	SC left invalid operand	FT-1C2-EU
	05		BDP 3.1B	BDP 4.0-03	BDP	PFS0	LSU mark line PE	CB-1B2-J13
	06	P,I	BDP 3.4A	BDP 4.1-00	BDP	PFS1	SVA-byte number rgtr PE	CU-1C2-F12
	07		BDP 3.1B	BDP 4.3-02	BDP	PFS50	Mark lines rgtr PE	CU-1C2-B14
	08		BDP 3.5A	BDP 4.1-02	BDP	PFS2	Aj BFR B rgtr PE, byte 0	CE-1C2-F04
	09		BDP 3.5A	BDP 4.1-02	BDP	PFS3	Aj BFR B rgtr PE, byte 1	CE-1C2-F05
	10		BDP 3.5A	BDP 4.1-02	BDP	PFS4	Aj BFR B rgtr PE, byte 2	CE-1C2-G03
1	11		BDP 3.5A	BDP 4.1-02	BDP	PFS5	Aj BFR B rgtr PE, byte 3	CE-1C2-G04
	12		BDP 3.5A	BDP 4.1-02	BDP	PFS6	Aj BFR B rgtr PE, byte 4	CE-1C2-G05
	13		BDP 3.5A	BDP 4.1-02	BDP	PFS7	Aj BFR B rgtr PE, byte 5	CE-1C2-G06
	14		BDP 3.5A	BDP 4.1-02	BDP	PFS8	Aj BFR B rgtr PE, byte 6	CE-1C2-H04
	15		BDP 3.5A	BDP 4.1-02	BDP	PFS9	Aj BFR B rgtr PE, byte 7	CE-1C2-H05
	16		BDP 3.5A	BDP 4.1-02	BDP	PFS10	Aj BFR A rgtr PE, byte 0	CE-1C1-F04
	17		BDP 3.5A	BDP 4.1-02	BDP	PFS11	Aj BFR A rgtr PE, byte 1	CE-1C2-F05
	18		BDP 3.5A	BDP 4.1-02	BDP	PFS12	Aj BFR A rgtr PE, byte 2	CE-1C2-G03
2	19		BDP 3.5A	BDP 4.1-02	BDP	PFS13	Aj BFR A rgtr PE, byte 3	CE-1C2-G04
	20		BDP 3.5A	BDP 4.1-02	BDP	PFS14	Aj BFR A rgtr PE, byte 4	CE-1C2-G05
	21		BDP 3.5A	BDP 4.1-02	BDP	PFS15	Aj BFR A rgtr PE, byte 5	CE-1C2-G06
	22		BDP 3.5A	BDP 4.1-02	BDP	PFS16	Aj BFR A rgtr PE, byte 6	CE-1C2-H04
	23		BDP 3.5A	BDP 4.1-02	BDP	PFS17	Aj BFR A rgtr PE, byte 7	CE-1C2-H05
	24		BDP 3.7A	BDP 4.1-08	BDP	PFS18	Ak BFR B/immed byte/scale count rgtr PE	CE-1C2-G10
	25		BDP 3.7A	BDP 4.1-08	BDP	PFS19	Ak BFR B rgtr PE, byte 1	CE-1C2-F09
	26		BDP 3.7A	BDP 4.1-08	BDP	PFS20	Ak BFR B rgtr PE, byte 2	CE-1C2-F10
3	27		BDP 3.7A	BDP 4.1-08	BDP	PFS21	Ak BFR B rgtr PE, byte 3	CE-1C2-G08
	28		BDP 3.7A	BDP 4.1-08	BDP	PFS22	Ak BFR B rgtr PE, byte 4	CE-1C2-G09
	29		BDP 3.7A	BDP 4.1-08	BDP	PFS23	Ak BFR B rgtr PE, byte 5	CE-1C2-G10
	30		BDP 3.7A	BDP 4.1-08	BDP	PFS24	Ak BFR B rgtr PE, byte 6	CE-1C2-J11
	31		BDP 3.7A	BDP 4.1-08	BDP	PFS25	Ak BFR B rgtr PE, byte 7	CE-1C2-H09

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Byte	Bit(s)	Due	Level 3 Diagram	Level 4 Diagram	Unit	Signal Name	Description	FRU
	32		BDP 3.7A	BDP 4.1-08	BDP	PFS26	Ak BFR A rgtr PE, byte 0	CE-1C2-D14
	33		BDP 3.7A	BDP 4.1-08	BDP	PFS27	Ak BFR A rgtr PE, byte 1	CE-1C2-D14
	34		BDP 3.7A	BDP 4.1-08	BDP	PFS28	Ak BFR A rgtr PE, byte 2	CE-1C2-C14
4	35		BDP 3.7A	BDP 4.1-08	BDP	PFS29	Ak BFR A rgtr PE, byte 3	CE-1C2-C14
	36		BDP 3.7A	BDP 4.1-08	BDP	PFS30	Ak BFR A rgtr PE, byte 4	CE-1C2-C15
	37		BDP 3.7A	BDP 4.1-08	BDP	PFS31	Ak BFR A rgtr PE, byte 5	CE-1C2-C15
	38		BDP 3.7A	BDP 4.1-08	BDP	PFS32	Ak BFR A rgtr PE, byte 6	CE-1C2-D15
	39		BDP 3.7A	BDP 4.1-08	BDP	PFS33	Ak BFR A rgtr PE, byte 7	CE-1C2-D15
	40	P,I	BDP 3.9A	BDP 4.2-00	BDP	PFS34	Aj descr rgtr PE	CU-1C2-J01
	41	P,I	BDP 3.9A	BDP 4.2-00	BDP	PFS35	Ak descr rgtr PE	CU-1C2-J02
	42		BDP 3.10B	BDP 4.2-02	BDP	PFS36	Aj subtrahend PE	CB-1C2-A03
5	43		BDP 3.10C	BDP 4.2-03	BDP	PFS37	Ak subtrahend PE	CB-1C2-A05
	44		BDP 3.11A	BDP 4.2-04	BDP	PFS38	Aj length count PE	AM-1C2-B01
	45	P,I	BDP 3.11B	BDP 4.2-05	BDP	PFS39	Aj length decrementor PE	CA-1C2-A02
	46		BDP 3.12A	BDP 4.2-06	BDP	PFS40	Ak length count PE	CE-1C2-C04
	47		BDP 3.12B	BDP 4.2-07	BDP	PFS41	Ak length decrementor PE	CA-1C2-B05
	48		BDP 3.13B	BDP 4.3-00	BDP	PFS42	BDP data result mux rgtr PE, byte 0	CB-1C2-J13
	49		BDP 3.13B	BDP 4.3-00	BDP	PFS43	BDP data result mux rgtr PE, byte 1	CB-1C2-J14
	50		BDP 3.13B	BDP 4.3-00	BDP	PFS44	BDP data result mux rgtr PE, byte 2	CB-1C2-J15
6	51		BDP 3.13B	BDP 4.3-00	BDP	PFS45	BDP data result mux rgtr PE, byte 3	CB-1C2-H13
	52		BDP 3.13B	BDP 4.3-00	BDP	PFS46	BDP data result mux rgtr PE, byte 4	CB-1C2-H14
	53		BDP 3.13B	BDP 4.3-00	BDP	PFS47	BDP data result mux rgtr PE, byte 5	CB-1C2-H15
	54		BDP 3.13B	BDP 4.3-00	BDP	PFS48	BDP data result mux rgtr PE, byte 6	CB-1C2-G14
	55		BDP 3.13B	BDP 4.3-00	BDP	PFS49	BDP data result mux rgtr PE, byte 7	CB-1C2-G15
	56	I	BDP 3.16E	BDP 4.4-03	BDP	PFS51	Soft cont B1 data PE	FT-1C2-EU
	57	I	BDP 3.16E	BDP 4.4-03	BDP	PFS52	Soft cont B2 data PE	FT-1C2-EL
	58		BDP 3.14B	BDP 4.3-04	BDP	PFS53	Convert byte, overflow byte rgtr A PE	CE-1B2-H03
7	59		BDP 3.14B	BDP 4.3-04	BDP	PFS54	Convert byte, overflow byte rgtr B PE	CE-1B2-H03
	60	I	BDP 3.15A	BDP 4.4-00	BDP	PFS55	BDP micr rgtr bits 0-2 PE	CE-1C2-A07
	61	I	BDP 3.15A	BDP 4.4-00	BDP	PFS56	BDP micr rgtr bits 3-9 PE	CE-1C2-A07
	62	I	BDP 3.16B	BDP 4.4-03	BDP	PFS57	Soft cont mem adrs PE board 1	HA-1C2-C08B
	63	I	BDP 3.16B	BDP 4.4-03	BDP	PFS58	Soft cont mem adrs PE board 2	HA-1C2-C08B

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Byte	Bit(s)	Due	Level 3 Diagram	Level 4 Diagram	Unit	Signal Name	Description	FRU
	00	I	SCX 3.0E	SCX 4.0-04	SCU	PFS0	IMU/FPU compare error	CE-1B4-K15
0	01	P	DIV 3.19B	DIV 4.0-49	SCU	PFS1	Div network compare error	AF-1A3-A01
	02	P,I	IMU 3.3B	IMU 4.0-05	SCU	PFS2	PE on byte from BDP	HB-1A4-E14
	03-07						(Not used)	
1	08-15						(Not used)	
2	16-23						(Not used)	
3	24-31						(Not used)	
	32						(Not used)	
	33	I	AC2 3.4C	AC2 4.4-02	AC2	PFS94	Store wait DUE	CU-2A3-D14
	34		AC2 3.27A	AC2 4.4-00	AC2	PFS90	Rank 6 and backup of error cond PE	CE-2A5-C05
4	35	I	AC2 3.2E	AC2 4.4-02	AC2	PFS91	Invalid SCM4 read	CU-2A3-D14
	36		AC2 3.19C	AC2 4.4-00	AC2	PFS92	Port A tag PE	CE-2A5-E01
	37	I	AC2 3.5A	AC2 4.4-01	AC2	PFS93	SCM4 fctn PE	HE-2A5-C02B
	38	I	AC2 3.27B	AC2 4.7-02	AC2	PFS37	Page map multiple hit	CU-2A4-F12
	39	I	AC2 3.2B	AC2 4.7-02	AC2	PFS87	SCM4 PE	CU-2A4-F12
	40		AC2 3.18C	AC2 4.6-01	AC2	PFS28	Port A RMA PE, byte 4	CB-2A5-B15
	41		AC2 3.18C	AC2 4.6-01	AC2	PFS29	Port A RMA PE, byte 5	CB-2A5-C15
	42		AC2 3.18C	AC2 4.6-01	AC2	PFS30	Port A RMA PE, byte 6	CB-2A5-C10
5	43		AC2 3.18C	AC2 4.6-01	AC2	PFS31	Port A RMA PE, byte 7	CB-2A5-E15
	44		AC2 3.17B	AC2 4.7-04	AC2	PFS32	Port B RMA PE, byte 4	HA-2A5-H15B
	45		AC2 3.17B	AC2 4.7-04	AC2	PFS33	Port B RMA PE, byte 5	CU-2A5-C01
	46		AC2 3.17B	AC2 4.7-04	AC2	PFS34	Port B RMA PE, byte 6	CU-2A5-C01
	47		AC2 3.17B	AC2 4.7-04	AC2	PFS35	Port B RMA PE, byte 7	HA-2A5-H15A

PROC-990, 992, 994, 990E, 995E PFS4 REGISTER (84) (Sheet 2 of 2)

Byte	Bit(s)	Due	Level 3 Diagram	Level 4 Diagram	Unit	Signal Name	Description	FRU
	48		AC2 3.23B	AC2 4.8-02	AC2	PFS60	Port C RMA PE, byte 4	CB-2A5-F15
	49		AC2 3.23B	AC2 4.8-02	AC2	PFS61	Port C RMA PE, byte 5	CB-2A5-E13
	50		AC2 3.23B	AC2 4.8-02	AC2	PFS62	Port C RMA PE, byte 6	CB-2A5-D11
6	51		AC2 3.23B	AC2 4.8-02	AC2	PFS63	Port C RMA PE, byte 7	CB-2A5-E12
	52	I	AC2 3.15A	AC2 4.8-05	AC2	PFS50	Port C SVA cntr PE, byte 4	CU-2A5-F09
	53	I	AC2 3.15A	AC2 4.8-05	AC2	PFS51	Port C SVA cntr PE, byte 5	HE-2A5-C06B
	54	I	AC2 3.15A	AC2 4.8-05	AC2	PFS52	Port C SVA cntr PE, byte 6	HE-2A5-C06B
	55	I	AC2 3.15A	AC2 4.8-05	AC2	PFS53	Port C SVA cntr PE, byte 7	HE-2A5-C06B
	56	I	AC2 3.19D	AC2 4.6-00	AC2	PFS54	Port A length cntr PE, byte 0	HA-2A5-D01A
	57	I	AC2 3.19D	AC2 4.6-00	AC2	PFS55	Port A length cntr PE, byte 1	CU-2A5-F09
	58	I	AC2 3.22D	AC2 4.8-00	AC2	PFS64	Port C length cntr PE, byte 0	CU-2A5-F09
7	59	I	AC2 3.22D	AC2 4.8-00	AC2	PFS65	Port C length cntr PE, byte 1	CU-2A5-F09
	60		AC2 3.22B	AC2 4.8-08	AC2	PFS59	Store tag PE	CB-2A5-G07
	61		AC2 3.16B	AC2 4.3-04	AC2	PFS44	Rank 6 page frame adrs bits 31-38 PE	CE-2A5-D12
	62		AC2 3.16B	AC2 4.3-04	AC2	PFS45	Rank 6 page frame adrs bits 39-46 PE	CE-2A5-D12
	63		AC2 3.16B	AC2 4.3-04	AC2	PFS46	Rank 6 page frame adrs bits 47-54 PE	CE-2A5-E14

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Byte	Bit(s)	Due	Level 3 Diagram	Level 4 Diagram	Unit	Signal Name	Description	FRU
	00		AC2 3.13B	AC2 4.9-01	AC2	PFS26	Page table adrs PE, bits 40-47	HA-2A5-A15A
	01		AC2 3.13B	AC2 4.9-01	AC2	PFS27	Page table adrs PE, bits 48-51	HA-2A5-A15A
	02		AC2 3.14A	AC2 4.0-01	AC2	PFS6	Rank 5 SVA PE, byte 2	CE-2A3-B10
0	03		AC2 3.14A	AC2 4.0-01	AC2	PFS7	Rank 5 SVA PE, byte 3	CE-2A3-B10
	04		AC2 3.14A	AC2 4.0-01	AC2	PFS8	Rank 4 SVA PE, byte 4	CE-2A3-B11
	05		AC2 3.14A	AC2 4.0-01	AC2	PFS9	Rank 4 SVA PE, byte 5	CE-2A3-B12
	06		AC2 3.14A	AC2 4.0-01	AC2	PFS10	Rank 4 SVA PE, byte 6	CE-2A3-B13
	07		AC2 3.14A	AC2 4.0-01	AC2	PFS11	Rank 4 SVA PE, byte 7	CE-2A3-B13
	08		AC2 3.13B	AC2 4.9-01	AC2	PFS25	Page table length PE	HA-2A5-A15B
	09	I	AC2 3.14D	AC2 4.4-01	AC2	PFS76	Rank 6 SVA PE, byte 0	CE-2A3-F14
	10	I	AC2 3.14D	AC2 4.4-01	AC2	PFS77	Rank 6 SVA PE, byte 2	CE-2A3-F09
1	11	I	AC2 3.14D	AC2 4.4-01	AC2	PFS78	Rank 6 SVA PE, byte 3	CE-2A3-F10
	12	I	AC2 3.14D	AC2 4.4-01	AC2	PFS79	Rank 6 SVA PE, byte 4	CE-2A3-F11
	13	I	AC2 3.14D	AC2 4.4-01	AC2	PFS80	Rank 6 SVA PE, byte 5	CE-2A3-F12
	14	I	AC2 3.14D	AC2 4.4-01	AC2	PFS81	Rank 6 SVA PE, byte 6	CE-2A3-F13
	15	I	AC2 3.14D	AC2 4.4-01	AC2	PFS82	Rank 6 SVA PE, byte 7	CE-2A3-F15
	16		AC2 3.29A	AC2 4.0-01	AC2	PFS56	Rank 5 ring and seg number, byte 2	CE-2A3-F03
	17		AC2 3.29A	AC2 4.0-01	AC2	PFS57	Rank 5 ring and seg number, byte 3	CE-2A3-F03
	18		AC2 3.15A	AC2 4.8-01	AC2	PFS48	Port C SVA PE, byte 2	CE-2A3-A07
2	19		AC2 3.15A	AC2 4.8-01	AC2	PFS49	Port C SVA PE, byte 3	CE-2A3-A07
	20		AC2 3.15A	AC2 4.8-01	AC2	PFS72	Port C SVA PE, byte 4	CE-2A3-F04
	21		AC2 3.15A	AC2 4.8-01	AC2	PFS73	Port C SVA PE, byte 5	CE-2A3-F04
	22		AC2 3.15A	AC2 4.8-01	AC2	PFS42	Port C SVA PE, byte 6	CE-2A3-F05
	23		AC2 3.15A	AC2 4.8-01	AC2	PFS43	Port C SVA PE, byte 7	CE-2A3-F05
	24		AC2 3.29B	AC2 4.4-01	AC2	PFS88	Rank 6 ring and seg number PE, byte 2	CE-2A3-A09
	25		AC2 3.29B	AC2 4.4-01	AC2	PFS89	Rank 6 ring and seg number PE, byte 3	CE-2A3-A10
	26	I	AC2 3.5A	AC2 4.4-01	AC2	PFS4	LSU micr length bits 0-7, 48	CE-2A3-F04
3	27	I	AC2 3.5A	AC2 4.4-01	AC2	PFS5	LSU micr length bits 8-15, 49	CE-2A5-F05
	28	I	AC2 3.5A	AC2 4.4-01	AC2	PFS36	LSU micr length bits 16-23, 50	CE-2A5-F06
	29	I	AC2 3.5A	AC2 4.4-01	AC2	PFS74	LSU micr length bits 24-31, 51	CE-2A5-F03
	30	I	AC2 3.5A	AC2 4.4-01	AC2	PFS58	LSU micr length bits 32-37, 56-57, 66	CE-2A5-K01
	31	I	AC2 3.5A	AC2 4.4-01	AC2	PFS75	LSU micr length bits 58-65, 67	CE-2A5-K02

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Byte	Bit(s)	Due	Level 3 Diagram	Level 4 Diagram	Unit	Signal Name	Description	FRU
	32		AC2 3.30B	AC2 4.11-01	AC2	PFS12	MAC write or table read PE, byte 0	CU-2A3-F02
	33		AC2 3.30B	AC2 4.11-01	AC2	PFS13	MAC write or table read PE, byte 1	CU-2A3-E02
	34		AC2 3.30B	AC2 4.11-01	AC2	PFS14	MAC write or table read PE, byte 2	CU-2A3-D02
4	35		AC2 3.30B	AC2 4.11-01	AC2	PFS15	MAC write or table read PE, byte 3	CU-2A3-C02
	36		AC2 3.30B	AC2 4.11-01	AC2	PFS16	MAC write or table read PE, byte 4	CU-2A3-B02
	37		AC2 3.30B	AC2 4.11-01	AC2	PFS17	MAC write or table read PE, byte 5	CU-2A3-A01
	38		AC2 3.30B	AC2 4.11-01	AC2	PFS18	MAC write or table read PE, byte 6	CU-2A3-B01
	39		AC2 3.30B	AC2 4.11-01	AC2	PFS19	MAC write or table read PE, byte 7	CU-2A4-A02
	40		AC2 3.30B	AC2 4.11-01	AC2	PFS1	Alternate PTE PE, byte 5	CE-2A4-A01
	41		AC2 3.30B	AC2 4.11-01	AC2	PFS2	Alternate PTE PE, byte 6	CE-2A4-B01
	42		AC2 3.30B	AC2 4.11-01	AC2	PFS3	Alternate PTE PE, byte 7	CE-2A4-A02
5	43		AC2 3.13A	AC2 4.9-00	AC2	PFS20	Seg page ID PE, byte 2	CU-2A3-A15
	44		AC2 3.13A	AC2 4.9-00	AC2	PFS21	Seg page ID PE, byte 3	CU-2A3-A15
	45		AC2 3.13A	AC2 4.9-00	AC2	PFS22	Seg page ID PE, byte 4	CU-2A3-B15
	46		AC2 3.13A	AC2 4.9-00	AC2	PFS23	Seg page ID PE, byte 5	CU-2A3-B15
	47		AC2 3.13A	AC2 4.9-00	AC2	PFS24	Page ID PE, byte 6	CU-2A4-B08
	48		AC2 3.29F	AC2 4.10-00	AC2	PFS0	Debug mask rgtr PE	CU-2A5-F09
	49		AC2 3.6A	AC2 4.10-02	AC2	PFS47	Page size mask PE	CU-2A5-F09
	50		AC2 3.29C	AC2 4.10-01	AC2	PFS66	Data results, ring and seg number, byte 2	CE-2A3-E05
6	51		AC2 3.29C	AC2 4.10-01	AC2	PFS67	Data results, ring and seg number, byte 3	CE-2A3-E06
	52		AC2 3.29C	AC2 4.10-01	AC2	PFS68	Data results sel PE, byte 4	CE-2A5-A01
	53		AC2 3.29C	AC2 4.10-01	AC2	PFS69	Data results sel PE, byte 5	CE-2A5-B01
	54		AC2 3.29C	AC2 4.10-01	AC2	PFS70	Data results sel PE, byte 6	CE-2A5-B02
	55		AC2 3.29C	AC2 4.10-01	AC2	PFS71	Data results sel PE, byte 7	CE-2A5-E11
	56		AC2 3.21A	AC2 4.7-05	AC2	PFS38	Port B miss tag PE, byte 0	CB-2A5-J01
	57		AC2 3.21A	AC2 4.7-05	AC2	PFS39	Port B miss tag PE, byte 1	CB-2A5-J02
	58		AC2 3.21A	AC2 4.7-05	AC2	PFS40	Port B miss tag PE, byte 3	CB-2A5-J04
7	59		AC2 3.21A	AC2 4.7-05	AC2	PFS41	Port B miss tag PE, byte 4	CB-2A5-J05
	60	I	AC2 3.10B	AC2 4.4-02	AC2	PFS83	Page map PE, set 0	CU-2A4-N12
	61	I	AC2 3.10B	AC2 4.4-41	7-1	=J 73	=age map PE, set 1	HE-2A4-H01B
	62	I	AC2 3.10B	AC2 4.4-02	AC2	PFS85	Page map PE, set 2	CU-2A4-H12
	63	I	AC2 3.10B	AC2 4.4-02	AC2	PFS86	Page map PE, set 3	HE-2A4-H01B

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Byte	Bit(s)	Due	Level 3 Diagram	Level 4 Diagram	Unit	Signal Name	Description	FRU
	00	P,I	BP3 3.1A	BP3 4.0-03	BP3	PFS0	BP3 micr rgtr PE, byte 0 or 1	CU-1D2-B01
	01	P,I	BP3 3.1A	BP3 4.0-03	BP3	PFS1	BP3 micr rgtr PE, byte 2 or 3	CU-1D2-H01
	02	P,I	BP3 3.1A	BP3 4.0-03	BP3	PFS2	BP3 micr rgtr PE, byte 4 or 5	CU-1D2-J01
0	03	P,I	BP3 3.1A	BP3 4.0-03	BP3	PFS3	BP3 micr rgtr PE, byte 6 or 7	CU-1D2-K01
	04	P,I	BP3 3.11A	BP3 4.0-02	BP3	PFS4	Immed byte PE	HA-1D2-H03A
	05	P,I	BP3 3.14B	BP3 4.3-02	BP3	PFS5	BFR adrs PE	HA-1D2-K10B
	06	P,I	BP3 3.15B	BP3 4.4-00	BP3	PFS6	Rgtr file A adrs PE	HA-1D2-H03A
	07	P,I	BP3 3.15F	BP3 4.4-00	BP3	PFS7	Rgtr file B adrs PE	HA-1D2-G10A
	08	P,I	BP3 3.16C	BP3 4.4-01	BP3	PFS8	Rgtr file A PE	HA-1D2-F06A
	09	P,I	BP3 3.29E	BP3 4.9-04	BP3	PFS9	Edit mask PE	CN-1D2-AU
	10	P,I	BP3 3.25B	BP3 4.10-00	BP3	PFS10	Convert to dec PE	CN-1D2-K11
1	11	P,I	BP3 3.20A	BP3 4.5-00	BP3	PFS11	C stream stage 2 data PE	CN-1D2-D04
	12	P,I	BP3 3.2A	BP3 4.0-00	BP3	PFS12	Aj descr PE	CU-1D2-H02
	13	P,I	BP3 3.2D	BP3 4.0-00	BP3	PFS13	Ak descr PE	CU-1D2-J02
	14	P,I	BP3 3.5C	BP3 4.1-04	BP3	PFS14	A stream stage 2 data PE	CL-1D2-BU
	15	P,I	BP3 3.8C	BP3 4.2-04	BP3	PFS15	B stream stage 2 data PE	CL-1D2-CU
	16	P,I	BP3 3.13B	BP3 4.3-01	BP3	PFS16	Common stage 7 data PE	CB-1D2-D08
	17	P,I	BP3 3.15A	BP3 4.4-01	BP3	PFS17	Table load limit rgtr PE	CB-1D2-F13
	18	P,I	BP3 3.16D	BP3 4.4-01	BP3	PFS18	Rgtr file B PE	CU-1D2-F09
2	19	P,I	BP3 3.23C	BP3 4.6-05	BP3	PFS19	Binary/dec RAM adrs PE	AF-1D2-AL
	20	P,I	BP3 3.22C	BP3 4.6-05	BP3	PFS20	Translate RAM adrs PE	AF-1D2-AL
	21	P,I	BP3 3.3B	BP3 4.11-05	BP3	PFS21	Spec error or mult by 256 adrs PE	AF-1D2-BL
	22	P,I	BP3 3.3B	BP3 4.11-05	BP3	PFS22	Spec error or mult by 256 RAM output PE	AF-1D2-BL
	23	P,I	BP3 3.5C	BP3 4.1-01	BP3	PFS23	A stream stage 1 data PE	CL-1D2-BU
	24	P,I	BP3 3.22C	BP3 4.6-05	BP3	PFS24	Translate RAM data PE	AF-1D2-AL
	25		BP3 3.23E	BP3 4.6-05	BP3	PFS25	Binary/dec RAM data PE	AF-1D2-AL
	26	P,I	BP3 3.8C	BP3 4.2-01	BP3	PFS26	B stream stage 1 data PE	CL-1D2-CU
3	27	I	CMC 3.32A	CM4 4.4x-02	CMC	PFS0	PW adrs PE	HF-3D1-J10B
	28		AC1 3.27F	CM3 4.2-02	CMC	PFS1	Maint rgtr write data PE	0FPH-3A1-EU
	29	I	BP3 3.36B	AC1 4.7-00	AC1	PFS79	SCM 2 PE	CE-2A1-H11
	30	I	BP3 3.37C	AC1 4.7-01	AC1	PFS80	SCM 3 PE	CU-2A1-J09
	31	I	BP3 3.37B	AC1 4.7-03	AC1	PFS83	Rank 4 soft cont rgtr PE	CU-2A1-K11

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Byte	Bit(s)	Due	Level 3 Diagram	Level 4 Diagram	Unit	Signal Name	Description	FRU
	32	I	AC1 3.15B	AC1 4.0-0	AC1	PFS0	Transfer count PE	CE-2A2-E01
	33	I	AC1 3.17A	AC1 4.0-2	AC1	PFS5	Instr descr rgtr PE, byte 0	CE-2A2-C01
	34	I	AC1 3.17A	AC1 4.0-2	AC1	PFS6	Instr descr rgtr PE, byte 1	CE-2A2-C01
4	35	I	AC1 3.17A	AC1 4.0-2	AC1	PFS7	Instr descr rgtr PE, byte 2	CE-2A2-J01
	36	I	AC1 3.15C	AC1 4.0-2	AC1	PFS8	BDP descr, bytes 0 and 1	CE-2A2-H01
	37	I	AC1 3.15C	AC1 4.0-2	AC1	PFS9	BDP descr, bytes 2 and 3	CE-2A2-H01
	38	I	AC1 3.15C	AC1 4.0-2	AC1	PFS10	BDP descr, bytes 4 and 5	CE-2A2-C02
	39	I	AC1 3.15C	AC1 4.0-2	AC1	PFS11	BDP descr, bytes 6 and 7	CE-2A2-C02
	40	I	AC1 3.0D	AC1 4.7-0	AC1	PFS75	M1 micr rgtr PE, byte 1	CE-2A1-D13
	41	I	AC1 3.0D	AC1 4.7-0	AC1	PFS76	M1 micr rgtr PE, byte 2	CE-2A1-D13
	42	I	AC1 3.0D	AC1 4.7-0	AC1	PFS77	M1 micr rgtr PE, byte 3	CE-2A1-D13
5	43	I	AC1 3.0D	AC1 4.7-0	AC1	PFS78	M1 micr rgtr PE, byte 4	CE-2A1-D13
	44	I	AC1 3.16A	AC1 4.0-1	AC1	PFS1	P right rgtr PE, byte 4	CE-2A2-G01
	45	I	AC1 3.16A	AC1 4.0-1	AC1	PFS2	P right rgtr PE, byte 5	CE-2A2-G01
	46	I	AC1 3.16A	AC1 4.0-1	AC1	PFS3	P right rgtr PE, byte 6	CE-2A2-J02
	47	I	AC1 3.16A	AC1 4.0-1	AC1	PFS4	P right rgtr PE, byte 7	CE-2A2-J02
	48	I	AC1 3.18D	AC1 4.0-5	AC1	PFS12	SVA byte number mux/rgtr PE, byte 4	CB-2A2-D09
	49	I	AC1 3.18D	AC1 4.0-5	AC1	PFS13	SVA byte number mux/rgtr PE, byte 5	CB-2A2-E09
	50	I	AC1 3.18D	AC1 4.0-5	AC1	PFS14	SVA byte number mux/rgtr PE, byte 6	CB-2A2-F09
6	51	I	AC1 3.18D	AC1 4.0-5	AC1	PFS15	SVA byte number mux/rgtr PE, byte 7	CB-2A2-G09
	52		AC1 3.18D	AC1 4.0-5	AC1	PFS16	SVA byte number bfr rgtr PE, byte 4	CE-2A2-B03
	53		AC1 3.18D	AC1 4.0-5	AC1	PFS17	SVA byte number bfr rgtr PE, byte 5	CE-2A2-B03
	54		AC1 3.18D	AC1 4.0-5	AC1	PFS18	SVA byte number bfr rgtr PE, byte 6	CE-2A2-B04
	55		AC1 3.18D	AC1 4.0-5	AC1	PFS19	SVA byte number bfr rgtr PE, byte 7	CE-2A2-B04
	56		AC1 3.18A	AC1 4.0-9	AC1	PFS20	Byte number holding rgtr PE, byte 4	CB-2A2-D10
	57		AC1 3.18A	AC1 4.0-9	AC1	PFS21	Byte number holding rgtr PE, byte 5	CB-2A2-E10
	58		AC1 3.18A	AC1 4.0-9	AC1	PFS22	Byte number holding rgtr PE, byte 6	CB-2A2-F10
7	59		AC1 3.18A	AC1 4.0-9	AC1	PFS23	Byte number holding rgtr PE, byte 7	CB-2A2-G11
	60		AC1 3.19C	AC1 4.2-14	AC1	PFS24	Incr adder operand B rgtr PE, byte 4	CU-2A1-H09
	61		AC1 3.19C	AC1 4.2-14	AC1	PFS25	Incr adder operand B rgtr PE, byte 5	CU-2A1-H09
	62		AC1 3.19C	AC1 4.2-14	AC1	PFS26	Incr adder operand B rgtr PE, byte 6	CU-2A1-H09
	63		AC1 3.19C	AC1 4.2-14	AC1	PFS27	Incr adder operand B rgtr PE, byte 7	CU-2A1-H09

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Byte	Bit(s)	Due	Level 3 Diagram	Level 4 Diagram	Unit	Signal Name	Description	FRU
	00	I	AC1 3.37A	AC1 4.7-01	AC1	PFS60	Seg descr RMA adder PE, byte 4	CU-2A1-A10
	01	I	AC1 3.37A	AC1 4.7-01	AC1	PFS61	Seg descr RMA adder PE, byte 5	CU-2A1-A10
	02	I	AC1 3.37A	AC1 4.7-01	AC1	PFS62	Seg descr RMA adder PE, byte 6	CU-2A1-A10
0	03	I	AC1 3.37A	AC1 4.7-01	AC1	PFS63	Seg descr RMA adder PE, byte 7	CU-2A1-A10
	04	I	AC1 3.37A	AC1 4.7-01	AC1	PFS64	Seg descr RMA carry error, byte 5	CU-2A1-A10
	05	I	AC1 3.37A	AC1 4.7-01	AC1	PFS65	Seg descr RMA carry error, byte 6	CU-2A1-A10
	06	I	AC1 3.37A	AC1 4.7-01	AC1	PFS66	Seg descr RMA carry error, byte 7	CU-2A1-A10
	07	I	AC1 3.22A	AC1 4.1-02	AC1	PFS28	Length rgtr PE	CU-2A2-J10
	08	I	AC1 3.37B	AC1 4.7-03	AC1	PFS50	Rank 4 seg descr rgtr PE, byte 4	CU-2A1-K11
	09	I	AC1 3.37B	AC1 4.7-03	AC1	PFS51	Rank 4 seg descr rgtr PE, byte 5	CU-2A1-K11
	10	I	AC1 3.34E	AC1 4.4-10	AC1	PFS52	Rank 4 seg descr rgtr PE, byte 7	CE-2A1-D13
1	11	I	AC1 3.17A	AC1 4.0-02	AC1	PFS67	Instr descr rgtr PE copy 2, byte 2	CU-2A2-J01
	12	I	AC1 3.23G	AC1 4.7-01	AC1	PFS36	Seg table length rgtr PE, bits 4-7	CU-2A1-A10
	13	I	AC1 3.23G	AC1 4.7-01	AC1	PFS37	Seg table length rgtr/comparator,bits 4-11	CU-2A1-A10
	14	I	AC1 3.37C	AC1 4.7-01	AC1	PFS81	Rank 3 fctn code rgtr/bfr PE, byte 0	CU-2A1-J09
	15	I	AC1 3.37B	AC1 4.7-03	AC1	PFS82	SCM 4 fctn code rgtr PE, byte 0	CU-2A1-K11
	16		AC1 3.3A	AC1 4.5-10	AC1	PFS84	LSU tag rank 3 rgtr/bfr PE, bits 5-12	CE-2A1-H14
	17		AC1 3.4A	AC1 4.5-12	AC1	PFS86	Rank 5 LSU tag rgtr PE, byte 0	CU-2A1-C09
	18		AC1 3.4A	AC1 4.5-12	AC1	PFS87	Rank 5 LSU tag rgtr PE, byte 1	CU-2A1-C09
2	19		AC1 3.4A	AC1 4.5-12	AC1	PFS88	Rank 5 LSU tag rgtr PE, byte 3	CU-2A1-D08
	20	I	AC1 3.37B	AC1 4.7-03	AC1	PFS85	Vector length rank 4 rgtr PE, bits 58-65	CU-2A1-L11
	21		AC1 3.4A	AC1 4.5-13	AC1	PFS91	Rank 5 LSU tag rgtr PE, byte 0	CU-2A1-C08
	22		AC1 3.4A	AC1 4.5-13	AC1	PFS92	Rank 5 LSU tag rgtr PE, byte 1	CU-2A1-C08
	23		AC1 3.4A	AC1 4.5-13	AC1	PFS93	Rank 5 LSU tag rgtr PE, byte 3	CU-2A1-D08
	24	I	AC1 3.7A	AC1 4.5-06	AC1	PFS38	SCM 2 invalid fctn code	CU-2B2-D03
	25	I	AC1 3.10A	AC1 4.5-07	AC1	PFS39	SCM 3 invalid fctn code	CU-2B2-D03
	26	I	AC1 3.36B	AC1 4.7-00	AC1	PFS72	P left rgtr ring and seg PE, byte 2	CE-2A1-H11
3	27	I	AC1 3.36B	AC1 4.7-00	AC1	PFS73	P left rgtr ring and seg PE, byte 3	CE-2A1-H11
	28	I	AC1 3.37B	AC1 4.7-03	AC1	PFS44	Ring/seg rgtr rank 4 PE, byte 2	CU-2A1-K11
	29	I	AC1 3.37B	AC1 4.7-03	AC1	PFS45	Ring/seg rgtr rank 4 PE, byte 3	CU-2A1-K11
	30		AC1 3.24C	AC1 4.2-01	AC1	PFS40	Rank 3 ring and seg rgtr PE, byte 2	CE-2B2-D02
	31		AC1 3.24C	AC1 4.2-01	AC1	PFS41	Rank 3 ring and seg rgtr PE, byte 3	CE-2B2-D01

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Byte	Bit(s)	Due	Level 3 Diagram	Level 4 Diagram	Unit	Signal Name	Description	FRU
	32		ACl 3.24A	ACl 4.2-03	ACl	PFS42	Ring/seg hold rgtr PE, byte 2	CE-2B2-J03
	33		ACl 3.24A	ACl 4.2-03	ACl	PFS43	Ring/seg hold rgtr PE, byte 3	CE-2B2-J03
	34		ACl 3.4B	ACl 4.5-12	ACl	PFS89	Rank 5 length rgtr PE, bits 50-57	CU-2A1-F10
4	35		ACl 3.4B	ACl 4.5-12	ACl	PFS90	Rank 5 length rgtr PE, bits 58-65	CU-2A1-F10
	36	I	ACl 3.32A	ACl 4.7-00	ACl	PFS68	P left rgtr keys PE, byte 0	CE-2A1-C11
	37	I	ACl 3.32A	ACl 4.7-00	ACl	PFS69	P left rgtr keys PE, byte 1	CE-2A1-B10
	38	I	ACl 3.32A	ACl 4.7-00	ACl	PFS70	P left rgtr or seg PE, byte 2	CE-2A1-E11
	39	I	ACl 3.32A	ACl 4.7-00	ACl	PFS71	P left rgtr or seg PE, byte 3	CE-2A1-D10
	40	I	ACl 3.34E	ACl 4.4-10	ACl	PFS58	Seg number hold rgtr PE, byte 2	HE-2A1-E15A
	41	I	ACl 3.34E	ACl 4.4-10	ACl	PFS59	Seg number hold rgtr PE, byte 3	HE-2A1-E15A
	42	I	ACl 3.34E	ACl 4.4-10	ACl	PFS57	Ring number hold rgtr PE, byte 2	CE-2A1-D13
5	43	I	ACl 3.37C	ACl 4.7-01	ACl	PFS29	Port B length cntr PE, bits 0-7	CU-2A1-J09
	44		ACl 3.26A	ACl 4.2-10	ACl	PFS46	ASID holding rgtr PE, byte 2	CE-2B2-G12
	45		ACl 3.26A	ACl 4.2-10	ACl	PFS47	ASID holding rgtr PE, byte 3	CE-2B2-G12
	46	I	ACl 3.37B	ACl 4.7-03	ACl	PFS48	ASID rgtr rank 4 PE, byte 2	CU-2A1-K11
	47	I	ACl 3.37B	ACl 4.7-03	ACl	PFS49	ASID rgtr rank 4 PE, byte 3	CU-2A1-K11
	48	I	ACl 3.34E	ACl 4.4-10	ACl	PFS55	Global key hold rgtr PE, byte 0	CE-2A1-D13
	49	I	ACl 3.37C	ACl 4.7-01	ACl	PFS30	RAC and FLC rgtr and comparator PE, byte 5	CU-2A1-J09
	50	I	ACl 3.37C	ACl 4.7-01	ACl	PFS31	RAC and FLC rgtr and comparator PE, byte 6	CU-2A1-J09
6	51	I	ACl 3.37C	ACl 4.7-01	ACl	PFS32	RAC and FLC rgtr and comparator PE,bits 56-60	CU-2A1-J09
	52	I	ACl 3.34C	ACl 4.4-10	ACl	PFS56	Local key hold rgtr PE, byte 7	HE-2A1-E15A
	53	I	ACl 3.37C	ACl 4.7-01	ACl	PFS33	RAC and FLC rgtr and comparator PE, byte 5	CU-2A1-J09
	54	I	ACl 3.37C	ACl 4.7-01	ACl	PFS34	RAC and FLC rgtr and comparator PE, byte 6	CU-2A1-J09
	55	I	ACl 3.37C	ACl 4.7-01	ACl	PFS35	RAC and FLC rgtr and comparator PE, bits 56-60	CU-2A1-J09
	56	I	ACl 3.31E	ACl 4.2-02	ACl	PFS53	Seg map 1 PE	CU-2B2-D03
	57	I	ACl 3.31D	ACl 4.2-11	ACl	PFS54	Seg map 0 PE	CU-2B2-D12
7	58	I	ACl 3.37C	ACl 4.7-02	ACl	PFS74	Multiple seg map hits	CU-2B2-A11
	59	I	ACl 3.37C	ACl 4.7-01	ACl	PFS94	Port B length cntr PE, bits 8-15	
	60-63						(Not used)	

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Byte	Bit(s)	Due	Level 3 Diagram	Level 4 Diagram	Unit	Signal Name	Description	FRU
0	00-07						(Not used)	
	08	I	LSU 3.22C	LSU 4.0-02	LSU	PFS24	Load BDP mux/rgtr PE, byte 0	CB-2C4-B11
	09	I	LSU 3.22C	LSU 4.0-02	LSU	PFS25	Load BDP mux/rgtr PE, byte 1	CB-2C4-C11
	10	I	LSU 3.22C	LSU 4.0-02	LSU	PFS26	Load BDP mux/rgtr PE, byte 2	CB-2C4-D11
1	11	I	LSU 3.22C	LSU 4.0-02	LSU	PFS27	Load BDP mux/rgtr PE, byte 3	CB-2C4-E11
	12	I	LSU 3.22C	LSU 4.0-02	LSU	PFS28	Load BDP mux/rgtr PE, byte 4	CB-2C4-G11
	13	I	LSU 3.22C	LSU 4.0-02	LSU	PFS29	Load BDP mux/rgtr PE, byte 5	CB-2C4-H11
	14	I	LSU 3.22C	LSU 4.0-02	LSU	PFS30	Load BDP mux/rgtr PE, byte 6	CB-2C4-J11
	15	I	LSU 3.22C	LSU 4.0-02	LSU	PFS31	Load BDP mux/rgtr PE, byte 7	CB-2C4-K11
	16	I	LSU 3.22A	LSU 4.0-02	LSU	PFS32	Load state mux/rgtr PE, byte 0	CB-2C4-B15
	17	I	LSU 3.22A	LSU 4.0-02	LSU	PFS33	Load state mux/rgtr PE, byte 1	CB-2C4-C15
	18	I	LSU 3.22A	LSU 4.0-02	LSU	PFS34	Load state mux/rgtr PE, byte 2	CB-2C4-D15
2	19	I	LSU 3.22A	LSU 4.0-02	LSU	PFS35	Load state mux/rgtr PE, byte 3	CB-2C4-E15
	20	I	LSU 3.22A	LSU 4.0-02	LSU	PFS36	Load state mux/rgtr PE, byte 4	CB-2C4-G15
	21	I	LSU 3.22A	LSU 4.0-02	LSU	PFS37	Load state mux/rgtr PE, byte 5	CB-2C4-H15
	22	I	LSU 3.22A	LSU 4.0-02	LSU	PFS38	Load state mux/rgtr PE, byte 6	CB-2C4-J15
	23	I	LSU 3.22A	LSU 4.0-02	LSU	PFS39	Load state mux/rgtr PE, byte 7	CB-2C4-K15
	24		LSU 3.30B	LSU 4.0-05	LSU	PFS182	A data bfr output rgtr PE, byte 0	CU-2C4-D08
	25		LSU 3.30B	LSU 4.0-05	LSU	PFS183	A data bfr output rgtr PE, byte 1	CU-2C4-D08
	26		LSU 3.30B	LSU 4.0-05	LSU	PFS184	A data bfr output rgtr PE, byte 2	CU-2C4-D08
3	27		LSU 3.30B	LSU 4.0-05	LSU	PFS185	A data bfr output rgtr PE, byte 3	CU-2C4-D08
	28		LSU 3.30B	LSU 4.0-05	LSU	PFS186	A data bfr output rgtr PE, byte 4	CU-2C4-D08
	29		LSU 3.30B	LSU 4.0-05	LSU	PFS187	A data bfr output rgtr PE, byte 5	CU-2C4-D08
	30		LSU 3.30B	LSU 4.0-05	LSU	PFS188	A data bfr output rgtr PE, byte 6	CU-2C4-D08
	31		LSU 3.30B	LSU 4.0-05	LSU	PFS189	A data bfr output rgtr PE, byte 7	CU-2C4-K10

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Byte	Bit(s)	Due	Level 3 Diagram	Level 4 Diagram	Unit	Signal Name	Description	FRU
	32		LSU 3.30B	LSU 4.0-05	LSU	PFS198	A data bfr output rgtr 1, byte 0	CU-2C4-A09
	33		LSU 3.30B	LSU 4.0-05	LSU	PFS199	A data bfr output rgtr 1, byte 1	CU-2C4-A09
	34		LSU 3.30B	LSU 4.0-05	LSU	PFS200	A data bfr output rgtr 1, byte 2	CU-2C4-A10
4	35		LSU 3.30B	LSU 4.0-05	LSU	PFS201	A data bfr output rgtr 1, byte 3	CU-2C4-A10
	36		LSU 3.30B	LSU 4.0-05	LSU	PFS202	A data bfr output rgtr 1, byte 4	CU-2C4-A11
	37		LSU 3.30B	LSU 4.0-05	LSU	PFS203	A data bfr output rgtr 1, byte 5	CU-2C4-A11
	38		LSU 3.30B	LSU 4.0-05	LSU	PFS204	A data bfr output rgtr 1, byte 6	CU-2C4-A12
	39		LSU 3.30B	LSU 4.0-05	LSU	PFS205	A data bfr output rgtr 1, byte 7	CU-2C4-A12
	40		LSU 3.30B	LSU 4.0-04	LSU	PFS16	A data bfr output rgtr 2, byte 0	CU-2A1-E08
	41		LSU 3.30B	LSU 4.0-04	LSU	PFS17	A data bfr output rgtr 2, byte 1	CU-2A1-E08
	42		LSU 3.30B	LSU 4.0-04	LSU	PFS18	A data bfr output rgtr 2, byte 2	CU-2A1-E07
5	43		LSU 3.30B	LSU 4.0-04	LSU	PFS19	A data bfr output rgtr 2, byte 3	CU-2A1-E07
	44		LSU 3.30B	LSU 4.0-04	LSU	PFS20	A data bfr output rgtr 2, byte 4	CU-2A1-F07
	45		LSU 3.30B	LSU 4.0-04	LSU	PFS21	A data bfr output rgtr 2, byte 5	CU-2A1-F07
	46		LSU 3.30B	LSU 4.0-04	LSU	PFS22	A data bfr output rgtr 2, byte 6	CU-2A1-G07
	47		LSU 3.30B	LSU 4.0-04	LSU	PFS23	A data bfr output rgtr 2, byte 7	CU-2A1-G07
	48	I	LSU 3.20A	LSU 4.0-00	LSU	PFS190	B data bfr output rgtr, byte 0	CU-2C4-H03
	49	I	LSU 3.20A	LSU 4.0-00	LSU	PFS191	B data bfr output rgtr, byte 1	CU-2C4-H03
	50	I	LSU 3.20A	LSU 4.0-00	LSU	PFS192	B data bfr output rgtr, byte 2	CU-2C4-K08
6	51	I	LSU 3.20A	LSU 4.0-00	LSU	PFS193	B data bfr output rgtr, byte 3	CU-2C4-K08
	52	I	LSU 3.20A	LSU 4.0-00	LSU	PFS194	B data bfr output rgtr, byte 4	CU-2C4-H03
	53	I	LSU 3.20A	LSU 4.0-00	LSU	PFS195	B data bfr output rgtr, byte 5	CU-2C4-K08
	54	I	LSU 3.20A	LSU 4.0-00	LSU	PFS196	B data bfr output rgtr, byte 6	CU-2C4-K08
	55	I	LSU 3.20A	LSU 4.0-00	LSU	PFS197	B data bfr output rgtr, byte 7	CU-2C4-K08
	56	I	LSU 3.20C	LSU 4.0-00	LSU	PFS0	B input data rgtr, byte 0	CU-2C4-K08
	57	I	LSU 3.20C	LSU 4.0-00	LSU	PFS1	B input data rgtr, byte 1	CU-2C4-K08
	58	I	LSU 3.20C	LSU 4.0-00	LSU	PFS2	B input data rgtr, byte 2	CU-2C4-K08
7	59	I	LSU 3.20C	LSU 4.0-00	LSU	PFS3	B input data rgtr, byte 3	CU-2C4-K08
	60	I	LSU 3.20C	LSU 4.0-00	LSU	PFS4	B input data rgtr, byte 4	CU-2C4-K08
	61	I	LSU 3.20C	LSU 4.0-00	LSU	PFS5	B input data rgtr, byte 5	CU-2C4-K08
	62	I	LSU 3.20C	LSU 4.0-00	LSU	PFS6	B input data rgtr, byte 6	CU-2C4-K08
	63	I	LSU 3.20C	LSU 4.0-00	LSU	PFS7	B input data rgtr, byte 7	CU-2C4-K08

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Byte	Bit(s)	Due	Level 3 Diagram	Level 4 Diagram	Unit	Signal Name	Description	FRU
	00	I	LSU 3.20F	LSU 4.0-01	LSU	PFS8	Load X rgtr PE, byte 0	CU-2C3-A11
	01	I	LSU 3.20F	LSU 4.0-01	LSU	PFS9	Load X rgtr PE, byte 1	CU-2C3-A11
	02	I	LSU 3.20F	LSU 4.0-01	LSU	PFS10	Load X rgtr PE, byte 2	CU-2C3-A11
0	03	I	LSU 3.20F	LSU 4.0-01	LSU	PFS11	Load X rgtr PE, byte 3	CU-2C3-A11
	04	I	LSU 3.20F	LSU 4.0-01	LSU	PFS12	Load X rgtr PE, byte 4	CU-2C3-A11
	05	I	LSU 3.20F	LSU 4.0-01	LSU	PFS13	Load X rgtr PE, byte 5	CU-2C3-A11
	06	I	LSU 3.20F	LSU 4.0-01	LSU	PFS14	Load X rgtr PE, byte 6	CU-2C3-A11
	07	I	LSU 3.20F	LSU 4.0-01	LSU	PFS15	Load X rgtr PE, byte 7	CU-2C3-A11
	08		LSU 3.43B	LSU 4.1-01	LSU	PFS40	Store data input mux/rgtr, byte 0	CU-2B4-D15
	09		LSU 3.43B	LSU 4.1-01	LSU	PFS41	Store data input mux/rgtr, byte 1	CU-2B4-D15
	10		LSU 3.43B	LSU 4.1-01	LSU	PFS42	Store data input mux/rgtr, byte 2	CU-2B4-D15
1	11		LSU 3.43B	LSU 4.1-01	LSU	PFS43	Store data input mux/rgtr, byte 3	CU-2B4-D15
	12		LSU 3.43B	LSU 4.1-01	LSU	PFS44	Store data input mux/rgtr, byte 4	CU-2B4-D15
	13		LSU 3.43B	LSU 4.1-01	LSU	PFS45	Store data input mux/rgtr, byte 5	CU-2B4-D15
	14		LSU 3.43B	LSU 4.1-01	LSU	PFS46	Store data input mux/rgtr, byte 6	CU-2B4-D15
	15		LSU 3.43B	LSU 4.1-01	LSU	PFS47	Store data input mux/rgtr, byte 7	CU-2B4-D15
	16		LSU 3.54B	LSU 4.1-07	LSU	PFS48	Store data output PE, byte 0	CU-2B4-D15
	17		LSU 3.54B	LSU 4.1-07	LSU	PFS49	Store data output PE, byte 1	CU-2B4-D15
	18		LSU 3.54B	LSU 4.1-07	LSU	PFS50	Store data output PE, byte 2	CU-2B4-D15
2	19		LSU 3.54B	LSU 4.1-07	LSU	PFS51	Store data output PE, byte 3	CU-2B4-D15
	20		LSU 3.54B	LSU 4.1-07	LSU	PFS52	Store data output PE, byte 4	CU-2B4-D15
	21		LSU 3.54B	LSU 4.1-07	LSU	PFS53	Store data output PE, byte 5	CU-2B4-D15
	22		LSU 3.54B	LSU 4.1-07	LSU	PFS54	Store data output PE, byte 6	CU-2B4-D15
	23		LSU 3.54B	LSU 4.1-07	LSU	PFS55	Store data output PE, byte 7	CU-2B4-D15
	24		LSU 3.50B	LSU 4.1-03	LSU	PFS56	Store data mux/rgtr 3 PE, byte 0	CB-2B4-H05
	25		LSU 3.50B	LSU 4.1-03	LSU	PFS57	Store data mux/rgtr 3 PE, byte 1	CB-2B4-H06
	26		LSU 3.50B	LSU 4.1-03	LSU	PFS58	Store data mux/rgtr 3 PE, byte 2	CB-2B4-H07
3	27		LSU 3.50B	LSU 4.1-03	LSU	PFS59	Store data mux/rgtr 3 PE, byte 3	CB-2B4-H08
	28		LSU 3.50B	LSU 4.1-03	LSU	PFS60	Store data mux/rgtr 3 PE, byte 4	CB-2B4-H10
	29		LSU 3.50B	LSU 4.1-03	LSU	PFS61	Store data mux/rgtr 3 PE, byte 5	CB-2B4-H11
	30		LSU 3.50B	LSU 4.1-03	LSU	PFS62	Store data mux/rgtr 3 PE, byte 6	CB-2B4-H12
	31		LSU 3.50B	LSU 4.1-03	LSU	PFS63	Store data mux/rgtr 3 PE, byte 7	CB-2B4-H13

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Byte	Bit(s)	Due	Level 3 Diagram	Level 4 Diagram	Unit	Signal Name	Description	FRU
	32	I	LSU 3.23G	LSU 4.4-00	LSU	PFS151	Load A input data rgtr PE, byte 0	CU-2C4-A08
	33	I	LSU 3.23G	LSU 4.4-00	LSU	PFS152	Load A input data rgtr PE, byte 1	CU-2C4-A08
	34	I	LSU 3.23G	LSU 4.4-00	LSU	PFS153	Load A input data rgtr PE, byte 2	CU-2C4-A07
4	35	I	LSU 3.23G	LSU 4.4-00	LSU	PFS154	Load A input data rgtr PE, byte 3	CU-2C4-A07
	36	I	LSU 3.23G	LSU 4.4-00	LSU	PFS155	Load A input data rgtr PE, byte 4	CU-2C4-B07
	37	I	LSU 3.23G	LSU 4.4-00	LSU	PFS156	Load A input data rgtr PE, byte 5	CU-2C4-B07
	38	I	LSU 3.23G	LSU 4.4-00	LSU	PFS157	Load A input data rgtr PE, byte 6	CU-2C4-B08
	39	I	LSU 3.23G	LSU 4.4-00	LSU	PFS158	Load A input data rgtr PE, byte 7	CU-2C4-B08
	40	I	LSU 3.24A	LSU 4.4-01	LSU	PFS143	170 RAC rgtr PE, byte 0	CU-2C4-B02
	41	I	LSU 3.24A	LSU 4.4-01	LSU	PFS144	170 RAC rgtr PE, byte 1	CU-2C4-B02
	42	I	LSU 3.24A	LSU 4.4-01	LSU	PFS145	170 RAC rgtr PE, byte 2	CU-2C4-B01
5	43	I	LSU 3.24A	LSU 4.4-01	LSU	PFS146	170 RAC rgtr PE, byte 3	CU-2C4-B01
	44	I	LSU 3.24C	LSU 4.4-01	LSU	PFS147	170 temporary rgtr PE, byte 0	CU-2C4-A02
	45	I	LSU 3.24C	LSU 4.4-01	LSU	PFS148	170 temporary rgtr PE, byte 1	CU-2C4-A02
	46	I	LSU 3.24C	LSU 4.4-01	LSU	PFS149	170 temporary rgtr PE, byte 2	CU-2C4-A01
	47	I	LSU 3.24C	LSU 4.4-01	LSU	PFS150	170 temporary rgtr PE, byte 3	CU-2C4-A01
	48		LSU 3.54B	LSU 4.1-07	LSU	PFS98	Mark output PE	CU-2B4-G12
	49		LSU 3.51C	LSU 4.5-08	LSU	PFS178	BDP mark lines rgtr PE	CU-2B5-E05
	50		LSU 3.5A	LSU 4.9-04	LSU	PFS78	Hit bfr input rgtr PE, byte 6	CB-2C2-G01
6	51		LSU 3.5A	LSU 4.9-04	LSU	PFS79	Hit bfr input rgtr PE, byte 7	CB-2C2-H01
	52		LSU 3.5A	LSU 4.9-04	LSU	PFS80	Hit bfr input rgtr PE, byte 8	CB-2C2-G02
	53		LSU 3.5A	LSU 4.9-04	LSU	PFS81	Hit bfr input rgtr PE, byte 9	CB-2C2-H02
	54		LSU 3.5A	LSU 4.9-04	LSU	PFS82	Hit bfr input rgtr PE, byte 10	CB-2C2-G03
	55		LSU 3.5A	LSU 4.9-04	LSU	PFS83	Hit bfr input rgtr PE, byte 11	CB-2C2-H03
	56	I	LSU 3.39C	LSU 4.5-00	LSU	PFS173	BDP store cont rgtr PE	CU-2B4-F06
	57	I	LSU 3.4B	LSU 4.9-09	LSU	PFS206	BDP load cont input rgtr PE	CU-2C2-A09
	58		LSU 3.5A	LSU 4.9-04	LSU	PFS137	Hit bfr output rgtr PE, byte 6	CU-2C2-C11
7	59		LSU 3.5A	LSU 4.9-04	LSU	PFS138	Hit bfr output rgtr PE, byte 7	CU-2C2-C11
	60		LSU 3.5A	LSU 4.9-04	LSU	PFS139	Hit bfr output rgtr PE, byte 8	CU-2C2-A10
	61		LSU 3.5A	LSU 4.9-04	LSU	PFS140	Hit bfr output rgtr PE, byte 9	CU-2C2-A10
	62		LSU 3.5A	LSU 4.9-04	LSU	PFS141	Hit bfr output rgtr PE, byte 10	CU-2C2-A06
	63		LSU 3.5A	LSU 4.9-04	LSU	PFS142	Hit bfr output rgtr PE, byte 11	CU-2C2-A06

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Byte	Bit(s)	Due	Level 3 Diagram	Level 4 Diagram	Unit	Signal Name	Description	FRU
	00	I	LSU 3.8A	LSU 4.3-04	LSU	PFS64	Load cont 1 PE, byte 0	CU-2C2-J15
	01	I	LSU 3.8A	LSU 4.3-04	LSU	PFS65	Load cont 1 PE, byte 1	CU-2C2-J15
	02	I	LSU 3.8A	LSU 4.3-04	LSU	PFS66	Load cont 1 PE, byte 2	CU-2C2-J15
0	03	I	LSU 3.8A	LSU 4.3-04	LSU	PFS67	Load cont 1 PE, byte 3	CU-2C2-J15
	04	I	LSU 3.8A	LSU 4.3-04	LSU	PFS68	Load cont 1 PE, byte 4	CU-2C2-J15
	05	I	LSU 3.8A	LSU 4.3-04	LSU	PFS69	Load cont 1 PE, byte 5	CU-2C2-J15
	06	I	LSU 3.8A	LSU 4.3-04	LSU	PFS70	Load cont 1 PE, byte 6	CU-2C2-J15
	07	I	LSU 3.8A	LSU 4.3-04	LSU	PFS71	Load cont 1 PE, byte 7	CU-2C2-J15
	08	I	LSU 3.8A	LSU 4.3-04	LSU	PFS72	Load cont 1 PE, byte 8	CU-2C2-J15
	09	I	LSU 3.8A	LSU 4.3-04	LSU	PFS73	Load cont 1 PE, byte 9	CU-2C2-J15
	10	I	LSU 3.8A	LSU 4.3-04	LSU	PFS74	Load cont 1 PE, byte 10	CU-2C2-J15
1	11	I	LSU 3.8A	LSU 4.3-04	LSU	PFS75	Load cont 1 PE, byte 11	CU-2C2-J15
	12	I	LSU 3.8A	LSU 4.3-04	LSU	PFS76	Load cont 1 PE, byte 12	CU-2C2-J15
	13	I	LSU 3.8A	LSU 4.3-04	LSU	PFS77	Load cont 1 PE, byte 13	CU-2C2-J15
	14	I	LSU 3.36B	LSU 4.9-02	LSU	PFS96	Vector cont input rgtr PE	CE-2C2-C03
	15		LSU 3.2D	LSU 4.9-08	LSU	PFS99	Illegal soft cont adrs	HE-2C2-A12B
	16	I	LSU 3.8A	LSU 4.3-03	LSU	PFS84	IDU cont rgtr PE, byte 0	CU-2C3-G04
	17	I	LSU 3.8A	LSU 4.3-03	LSU	PFS85	IDU cont rgtr PE, byte 1	CU-2C3-G04
	18	I	LSU 3.8A	LSU 4.3-03	LSU	PFS86	IDU cont rgtr PE, byte 2	CU-2C3-G03
2	19	I	LSU 3.8A	LSU 4.3-03	LSU	PFS87	IDU cont rgtr PE, byte 3	CU-2C3-G03
	20	I	LSU 3.8A	LSU 4.3-03	LSU	PFS88	IDU cont rgtr PE, byte 12	CU-2C3-G05
	21	I	LSU 3.8A	LSU 4.3-04	LSU	PFS89	ACU load cont rgtr PE, byte 6	CU-2C3-G02
	22	I	LSU 3.8A	LSU 4.3-04	LSU	PFS90	ACU load cont rgtr PE, byte 7	CU-2C3-G02
	23	I	LSU 3.8A	LSU 4.3-04	LSU	PFS91	ACU load cont rgtr PE, byte 8	CU-2C3-G06
	24		LSU 3.32A	LSU 4.12-01	LSU	PFS125	Vector tag input rgtr PE, byte 0	CU-2A1-F05
	25		LSU 3.32A	LSU 4.12-01	LSU	PFS126	Vector tag input rgtr PE, byte 1	CU-2A1-F05
	26	I	LSU 3.0A	LSU 4.9-00	LSU	PFS101	IDU load conts input rgtr PE, byte 0	CU-2C2-J06
3	27	I	LSU 3.0A	LSU 4.9-00	LSU	PFS102	IDU load conts input rgtr PE, byte 12	CU-2C2-J07
	28	I	LSU 3.0A	LSU 4.9-00	LSU	PFS103	IDU load conts input rgtr PE, byte 13	CU-2C2-J07
	29	I	LSU 3.0A	LSU 4.9-00	LSU	PFS104	IDU load conts input rgtr PE, byte 14	CU-2C2-J05
	30	I	LSU 3.0A	LSU 4.9-00	LSU	PFS105	IDU load conts input rgtr PE, byte 15	CU-2C2-J05
	31	I	LSU 3.0A	LSU 4.9-00	LSU	PFS106	IDU load conts input rgtr PE, byte 16	CU-2C2-J05

PROC-990, 992, 994, 990E, 995E PFSA REGISTER (8A) (Sheet 2 of 2)

Byte	Bit(s)	Due	Level 3 Diagram	Level 4 Diagram	Unit	Signal Name	Description	FRU
	32	I	LSU 3.33A	LSU 4.12-02	LSU	PFS127	Vector tag output rgtr PE, byte 0	CU-2C4-D02
	33	I	LSU 3.33A	LSU 4.12-02	LSU	PFS128	Vector tag output rgtr PE, byte 1	CU-2C4-D02
	34	I	LSU 3.1C	LSU 4.9-01	LSU	PFS111	ACU B load cont bfr 0 error 4	0EZH-2C2-BU
4	35	I	LSU 3.1C	LSU 4.9-01	LSU	PFS112	ACU B load cont bfr 0 error 5	0EZH-2C2-BU
	36	I	LSU 3.1C	LSU 4.9-01	LSU	PFS113	ACU B load cont bfr 0 error 6	0EZH-2C2-BU
	37	I	LSU 3.1C	LSU 4.9-01	LSU	PFS114	ACU B load cont bfr 1 error 4	0EZH-2C2-BL
	38	I	LSU 3.1C	LSU 4.9-01	LSU	PFS115	ACU B load cont bfr 1 error 5	0EZH-2C2-BL
	39	I	LSU 3.1C	LSU 4.9-01	LSU	PFS116	ACU B load cont bfr 1 error 6	0EZH-2C2-BL
	40	I	LSU 3.1C	LSU 4.9-01	LSU	PFS117	Soft cont mem 0 output rgtr error 0	0EZH-2C2-BU
	41	I	LSU 3.1C	LSU 4.9-01	LSU	PFS118	Soft cont mem 0 output rgtr error 1	0EZH-2C2-BU
	42	I	LSU 3.1C	LSU 4.9-01	LSU	PFS119	IDU cont bfr output rgtr, byte 12	CU-2C2-A07
5	43	I	LSU 3.1C	LSU 4.9-01	LSU	PFS120	IDU cont bfr output rgtr, byte 13	CU-2C2-A07
	44	I	LSU 3.1C	LSU 4.9-01	LSU	PFS121	IDU cont bfr output rgtr, byte 14	CU-2C2-A07
	45	I	LSU 3.1C	LSU 4.9-01	LSU	PFS122	Soft cont mem 1 output rgtr error 0	0EZH-2C2-BL
	46	I	LSU 3.1C	LSU 4.9-01	LSU	PFS123	Soft cont mem 1 output rgtr error 1	0EZH-2C2-BL
	47	I	LSU 3.1C	LSU 4.9-01	LSU	PFS124	IDU cont bfr output rgtr, byte 15	CU-2C2-A07
	48	I	LSU 3.1C	LSU 4.9-01	LSU	PFS107	Soft cont mem 0 input rgtr error 0	0EZH-2C2-BU
	49	I	LSU 3.1C	LSU 4.9-01	LSU	PFS108	Soft cont mem 0 input rgtr error 1	0EZH-2C2-BU
	50	I	LSU 3.1C	LSU 4.9-01	LSU	PFS109	Soft cont mem 1 input rgtr error 0	0EZH-2C2-BL
6	51	I	LSU 3.1C	LSU 4.9-01	LSU	PFS110	Soft cont mem 1 input rgtr error 1	0EZH-2C2-BL
	52	I	LSU 3.11A	LSU 4.3-05	LSU	PFS92	Load cont rgtr 2, byte 0	CU-2C4-B05
	53	I	LSU 3.11A	LSU 4.3-05	LSU	PFS93	Load cont rgtr 2, byte 1	CU-2C4-B05
	54	I	LSU 3.11A	LSU 4.3-05	LSU	PFS94	Load cont rgtr 2, byte 2	CU-2C4-B04
	55	I	LSU 3.11A	LSU 4.3-05	LSU	PFS95	Load cont rgtr 2, byte 8	CU-2C4-B04
	56	I	LSU 3.11A	LSU 4.3-07	LSU	PFS100	Load cont rgtr 3, byte 0	CU-2C3-C12
	57	I	LSU 3.4C	LSU 4.9-08	LSU	PFS97	Input MAC load cont rgtr	CU-2C2-D05
	58	I	LSU 3.25A	LSU 4.4-02	LSU	PFS159	A Output mux/rgtr 1	CB-2C3-A03
7	59	I	LSU 3.25B	LSU 4.4-05	LSU	PFS160	A Output mux/rgtr 2, byte 3	CB-2C3-A02
	60	I	LSU 3.25B	LSU 4.4-05	LSU	PFS161	A Output mux/rgtr 2, byte 4	CB-2C3-A01
	61	I	LSU 3.25D	LSU 4.4-05	LSU	PFS162	A Output mux/rgtr 3, byte 5	CB-2C3-A05
	62	I	LSU 3.25D	LSU 4.4-05	LSU	PFS163	A Output mux/rgtr 3, byte 6	CB-2C3-A07
	63	I	LSU 3.25D	LSU 4.4-05	LSU	PFS164	A Output mux/rgtr 3, byte 7	CB-2C3-A08

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Byte	Bit(s)	Due	Level 3 Diagram	Level 4 Diagram	Unit	Signal Name	Description	FRU
	00	I	LSU 3.39A	LSU 4.5-00	LSU	PFS165	Store path cont input rgtr 1, byte 0	CU-2B4-H01
	01	I	LSU 3.39A	LSU 4.5-00	LSU	PFS166	Store path cont input rgtr 1, byte 1	CU-2B4-H01
	02	I	LSU 3.39A	LSU 4.5-00	LSU	PFS167	Store path cont input rgtr 1, byte 2	CU-2B4-J01
0	03	I	LSU 3.39A	LSU 4.5-00	LSU	PFS168	Store path cont input rgtr 1, byte 4	CU-2B4-J01
	04	I	LSU 3.39B	LSU 4.5-00	LSU	PFS169	Store path cont input rgtr 2, byte 0	CU-2B4-D09
	05	I	LSU 3.39B	LSU 4.5-00	LSU	PFS170	Store path cont input rgtr 2, byte 1	CU-2B4-D09
	06	I	LSU 3.39B	LSU 4.5-00	LSU	PFS171	Store path cont input rgtr 2, byte 2	CU-2B4-D08
	07	I	LSU 3.39B	LSU 4.5-00	LSU	PFS172	Store path cont input rgtr 2, byte 4	CU-2B4-D08
	08	I	LSU 3.41A	LSU 4.5-04	LSU	PFS174	Store cont sel/bfr 1, byte 0	CU-2B5-E05
	09	I	LSU 3.41A	LSU 4.5-04	LSU	PFS175	Store cont sel/bfr 1, byte 1	CU-2B5-E05
	10	I	LSU 3.41A	LSU 4.5-04	LSU	PFS176	Store cont sel/bfr 1, byte 2	CU-2B4-E14
1	11	I	LSU 3.41A	LSU 4.5-04	LSU	PFS177	Store cont sel/bfr 1, byte 3	CU-2B5-E05
	12	I	LSU 3.42A	LSU 4.5-07	LSU	PFS179	Store cont rgtr 2/bfr, byte 0	CU-2B4-A07
	13	I	LSU 3.42A	LSU 4.5-07	LSU	PFS180	Store cont rgtr 2/bfr, byte 1	CU-2B4-A07
	14	I	LSU 3.43A	LSU 4.5-08	LSU	PFS181	Store cont rgtr 3A, byte 3	CU-2B4-E14
	15						(Not used)	
	16-20						(Not used)	
2	21	N	INU 3.19A	IN2 4.1-07	IN2	PFS43	Issue timeout	CU-2D1-D07
	22		INU 3.23B	IN2 4.1-01	IN2	PFS1	RPL stage 1 PE 2, byte 0,	CE-2D1-B10
	23		INU 3.23B	IN2 4.1-01	IN2	PFS2	RPL stage 1 PE 2, byte 1,	CE-2D1-C10
	24		INU 3.23B	IN2 4.1-01	IN2	PFS3	RPL stage 1 PE 2, byte 2,	CE-2D1-D10
	25		INU 3.23B	IN2 4.1-01	IN2	PFS4	RPL stage 1 PE 1, byte 0,	CE-2D1-B10
	26		INU 3.23B	IN2 4.1-01	IN2	PFS5	RPL stage 1 PE 1, byte 1,	CE-2D1-C10
3	27		INU 3.23B	IN2 4.1-01	IN2	PFS6	RPL stage 1 PE 1, byte 2,	CE-2D1-D10
	28		INU 3.23B	IN2 4.1-02	IN2	PFS7	RPL stage 1 PE 0, byte 0,	CE-2D1-B05
	29		INU 3.23B	IN2 4.1-02	IN2	PFS8	RPL stage 1 PE 0, byte 1,	CE-2D1-C05
	30		INU 3.23B	IN2 4.1-02	IN2	PFS9	RPL stage 1 PE 0, byte 2,	CE-2D1-D05
	31		INU 3.23B	IN2 4.1-02	IN2	PFS10	RPL stage 9 PE, byte 0	CE-2D1-B09

PROC-990, 992, 994, 990E, 995E PFSB REGISTER (8B) (Sheet 2 of 2)

Byte	Bit(s)	Due	Level 3 Diagram	Level 4 Diagram	Unit	Signal Name	Description	FRU
	32		INU 3.23B	IN2 4.1-02	IN2	PFS11	RPL stage 9 PE, byte 1	CE-2D1-C09
	33		INU 3.23B	IN2 4.1-02	IN2	PFS12	RPL stage 9 PE, byte 2	CE-2D1-D09
	34		INU 3.23B	IN2 4.1-02	IN2	PFS13	RPL stage 8 PE, byte 0	CE-2D1-B09
4	35		INU 3.23B	IN2 4.1-02	IN2	PFS14	RPL stage 8 PE, byte 1	CE-2D1-C09
	36		INU 3.23B	IN2 4.1-02	IN2	PFS15	RPL stage 8 PE, byte 2	CE-2D1-D09
	37		INU 3.23B	IN2 4.1-03	IN2	PFS16	RPL stage 7 PE, byte 0	CE-2D1-B04
	38		INU 3.23B	IN2 4.1-03	IN2	PFS17	RPL stage 7 PE, byte 1	CE-2D1-C04
	39		INU 3.23B	IN2 4.1-03	IN2	PFS18	RPL stage 7 PE, byte 2	CE-2D1-D04
	40		INU 3.23B	IN2 4.1-03	IN2	PFS19	RPL stage 6 PE, byte 0	CE-2D1-B04
	41		INU 3.23B	IN2 4.1-03	IN2	PFS20	RPL stage 6 PE, byte 1	CE-2D1-C04
	42		INU 3.23B	IN2 4.1-03	IN2	PFS21	RPL stage 6 PE, byte 2	CE-2D1-D04
5	43	I	INU 3.23B	IN2 4.1-04	IN2	PFS22	RPL stage 5 PE, byte 0	CE-2D1-B08
	44	I	INU 3.23B	IN2 4.1-04	IN2	PFS23	RPL stage 5 PE, byte 1	CE-2D1-C08
	45	I	INU 3.23B	IN2 4.1-04	IN2	PFS24	RPL stage 5 PE, byte 2	CE-2D1-D08
	46	I	INU 3.23B	IN2 4.1-04	IN2	PFS25	RPL stage 4 PE, byte 0	CE-2D1-B08
	47	I	INU 3.23B	IN2 4.1-04	IN2	PFS26	RPL stage 4 PE, byte 1	CE-2D1-C08
	48	I	INU 3.23B	IN2 4.1-04	IN2	PFS27	RPL stage 4 PE, byte 2	CE-2D1-D08
	49	I	INU 3.23B	IN2 4.1-05	IN2	PFS28	RPL stage 3 PE, byte 0	CU-2D1-C03
	50	I	INU 3.23B	IN2 4.1-05	IN2	PFS29	RPL stage 3 PE, byte 1	CU-2D1-B03
6	51	I	INU 3.23B	IN2 4.1-06	IN2	PFS30	RPL stage 3 PE, byte 2	CE-2D1-D03
	52	I	INU 3.23B	IN2 4.1-06	IN2	PFS31	RPL stage 2 PE, byte 0	CU-2D1-B07
	53	I	INU 3.23B	IN2 4.1-06	IN2	PFS32	RPL stage 2 PE, byte 1	CU-2D1-B07
	54	I	INU 3.23B	IN2 4.1-06	IN2	PFS33	RPL stage 2 PE, byte 2	CE-2D1-D03
	55	I	INU 3.23B	IN2 4.1-07	IN2	PFS34	Result error tag PE	HB-2D1-A07B
	56	N	INU 3.19A	IN2 4.0-15	IN2	PFS35	Partial issue 1A timeout	
	57	N	INU 3.19A	IN2 4.0-15	IN2	PFS36	Partial issue 1B timeout	
	58	N	INU 3.19A	IN2 4.0-15	IN2	PFS37	Partial issue 2A timeout	
7	59	N	INU 3.19A	IN2 4.0-15	IN2	PFS38	Partial issue 2B timeout	
	60	N	INU 3.19A	IN2 4.0-15	IN2	PFS39	Partial issue 3A timeout	
	61	N	INU 3.19A	IN2 4.0-15	IN2	PFS40	Partial issue 3B timeout	
	62	N	INU 3.19A	IN2 4.0-15	IN2	PFS41	Partial issue 4A timeout	
	63	N	INU 3.19A	IN2 4.0-15	IN2	PFS42	Partial issue 4B timeout	

PROC-990, 992, 994, 990E, 995E PFSC REGISTER (8C) (Sheet 1 of 2)

Byte	Bit(s)	Due	Level 3 Diagram	Level 4 Diagram	Unit	Signal Name	Description	FRU
	00		PSR 3.0B	PSR 4.0-00	PSR	PFS0	State load input rgtr PE, byte 0	CU-2B5-J05
	01		PSR 3.0B	PSR 4.0-00	PSR	PFS1	State load input rgtr PE, byte 1	CU-2B5-J05
	02		PSR 3.0B	PSR 4.0-00	PSR	PFS2	State load input rgtr PE, byte 2	CU-2B5-J12
0	03		PSR 3.0B	PSR 4.0-00	PSR	PFS3	State load input rgtr PE, byte 3	CU-2B5-J12
	04		PSR 3.0B	PSR 4.0-00	PSR	PFS4	State load mux PE, byte 4	CB-2B5-K10
	05		PSR 3.0B	PSR 4.0-00	PSR	PFS5	State load mux PE, byte 5	CB-2B5-K11
	06		PSR 3.0B	PSR 4.0-00	PSR	PFS6	State load mux PE, byte 6	CB-2B5-K09
	07		PSR 3.0B	PSR 4.0-00	PSR	PFS7	State load mux PE, byte 7	CB-2B5-J10
	08	I	PSR 3.0C	PSR 4.0-04	PSR	PFS8	State load data rgtr PE, byte 0	CU-2C5-A03
	09	I	PSR 3.0C	PSR 4.0-04	PSR	PFS9	State load data rgtr PE, byte 1	CU-2C5-A03
	10	I	PSR 3.0C	PSR 4.0-04	PSR	PFS10	State load data rgtr PE, byte 2	CU-2C5-A15
1	11	I	PSR 3.0C	PSR 4.0-04	PSR	PFS11	State load data rgtr PE, byte 3	CU-2C5-A15
	12	I	PSR 3.0C	PSR 4.0-04	PSR	PFS12	State load data rgtr PE, byte 4	CU-2C5-B14
	13	I	PSR 3.0C	PSR 4.0-04	PSR	PFS13	State load data rgtr PE, byte 5	CU-2C5-B14
	14	I	PSR 3.0C	PSR 4.0-04	PSR	PFS14	State load data rgtr PE, byte 6	CU-2C5-B13
	15	I	PSR 3.0C	PSR 4.0-04	PSR	PFS15	State load data rgtr PE, byte 7	CU-2C5-B13
	16		PSR 3.26C	PSR 4.9-00	PSR	PFS72	Store rgtr PE, byte 0	CU-2B5-A05
	17		PSR 3.26C	PSR 4.9-00	PSR	PFS73	Store rgtr PE, byte 1	CU-2B5-A05
	18	I	PSR 3.26A	PSR 4.9-01	PSR	PFS74	Store history tag completion rgtr PE, byte 0	CE-2B5-A11
2	19		PSR 3.26A	PSR 4.9-01	PSR	PFS75	Store history tag completion rgtr PE, byte 1	CE-2B5-A11
	20		PSR 3.27A	PSR 4.9-02	PSR	PFS76	Load path history tag mux 1 PE, byte 0	CB-2B5-A15
	21	I	PSR 3.27A	PSR 4.9-02	PSR	PFS77	Load path history tag rgtr 1 PE, byte 1	CE-2B5-C10
	22	I	PSR 3.0C	PSR 4.0-01	PSR	PFS16	State load rgtr PE, byte 6	CE-2B5-D15
	23	I	PSR 3.0C	PSR 4.0-01	PSR	PFS17	State load rgtr PE, byte 7	CE-2B5-D15
	24	I	PSR 3.23A	PSR 4.8-08	PSR	PFS56	State copy muxes PE, byte 0	CU-2C5-G03
	25	I	PSR 3.23A	PSR 4.8-08	PSR	PFS57	State copy muxes PE, byte 1	CU-2C5-G03
	26	I	PSR 3.23A	PSR 4.8-08	PSR	PFS58	State copy muxes PE, byte 2	CU-2C5-G14
3	27	I	PSR 3.23A	PSR 4.8-08	PSR	PFS59	State copy muxes PE, byte 3	CU-2C5-G14
	28	I	PSR 3.23A	PSR 4.8-08	PSR	PFS60	State copy muxes PE, byte 4	CU-2C5-G03
	29	I	PSR 3.23A	PSR 4.8-08	PSR	PFS61	State copy muxes PE, byte 5	CU-2C5-G03
	30	I	PSR 3.23A	PSR 4.8-08	PSR	PFS62	State copy muxes PE, byte 6	CU-2C5-G03
	31	I	PSR 3.23A	PSR 4.8-08	PSR	PFS63	State copy muxes PE, byte 7	CU-2C5-G03

PROC-990, 992, 994, 990E, 995E PFSC REGISTER (8C) (Sheet 2 of 2)

Byte	Bit(s)	Due	Level 3 Diagram	Level 4 Diagram	Unit	Signal Name	Description	FRU
	32	I	PSR 3.22B	PSR 4.8-07	PSR	PFS64	Exchange call trap mux PE, byte 0	HA-2C5-K13B
	33	I	PSR 3.22B	PSR 4.8-07	PSR	PFS65	Exchange call trap mux PE, byte 1	HA-2C5-K13B
	34	I	PSR 3.22B	PSR 4.8-07	PSR	PFS66	Exchange rgtr PE, byte 2	CU-2C5-K15
4	35	I	PSR 3.22B	PSR 4.8-07	PSR	PFS67	Exchange rgtr PE, byte 3	CU-2C5-K15
	36	I	PSR 3.22B	PSR 4.8-07	PSR	PFS68	Exchange rgtr PE, byte 4	CU-2C5-G13
	37	I	PSR 3.22B	PSR 4.8-07	PSR	PFS69	Exchange rgtr PE, byte 5	CU-2C5-G13
	38	I	PSR 3.22B	PSR 4.8-07	PSR	PFS70	Exchange rgtr PE, byte 6	CU-2C5-K14
	39	I	PSR 3.22B	PSR 4.8-07	PSR	PFS71	Exchange rgtr PE, byte 7	CU-2C5-K14
	40		PSR 3.27B	PSR 4.9-03	PSR	PFS83	Load path history tag rgtr 3 PE	CE-2B5-A13
	41		PSR 3.27B	PSR 4.9-08	PSR	PFS84	Virtual machine history tag PE	CU-2A5-J15
	42		PSR 3.27B	PSR 4.9-03	PSR	PFS85	Load path history tag mux 2 PE	CB-2B5-H13
	43		PSR 3.29B	PSR 4.9-07	PSR	PFS78	History tag PE	CE-2B5-A14
5	44		PSR 3.28A	PSR 4.9-05	PSR	PFS79	PSR tag sel mux PE	HA-2B5-A10
	45		PSR 3.28A	PSR 4.9-04	PSR	PFS80	PSR history tag rgtr 1 PE	CE-2B5-J09
	46		PSR 3.28A	PSR 4.9-04	PSR	PFS81	PSR history tag rgtr 3 PE	CE-2B5-C14
	47		PSR 3.28A	PSR 4.9-04	PSR	PFS82	PSR tag rgtr PE	CE-2B5-J09
	48		PSR 3.24F	PSR 4.7-00	PSR	PFS54	MAC data rgtr PE	CE-2A1-J02
	49		PSR 3.25B	PSR 4.7-04	PSR	PFS55	Disassy rgtr PE	CE-2A1-G02
	50		PSR 3.2C	PSR 4.4-03	PSR	PFS30	UTP bfr rgtr PE, byte 2	CU-2A5-K05
	51		PSR 3.2C	PSR 4.4-03	PSR	PFS31	UTP bfr rgtr PE, byte 3	CU-2A5-K04
6	52		PSR 3.2C	PSR 4.4-03	PSR	PFS32	UTP bfr rgtr PE, byte 4	CB-2A5-K15
	53		PSR 3.2C	PSR 4.4-03	PSR	PFS33	UTP bfr rgtr PE, byte 5	CB-2A5-K14
	54		PSR 3.2C	PSR 4.4-03	PSR	PFS34	UTP bfr rgtr PE, byte 6	CB-2A5-K13
	55		PSR 3.2C	PSR 4.4-03	PSR	PFS35	UTP bfr rgtr PE, byte 7	CB-2A5-K12
	56		PSR 3.25A	PSR 4.7-01	PSR	PFS46	Data assembler rgtr PE, byte 0	CB-2A1-E01
	57		PSR 3.25A	PSR 4.7-01	PSR	PFS47	Data assembler rgtr PE, byte 1	CB-2A1-E02
	58		PSR 3.25A	PSR 4.7-02	PSR	PFS48	Data assembler rgtr PE, byte 2	CB-2A1-G01
7	59		PSR 3.25A	PSR 4.7-02	PSR	PFS49	Data assembler rgtr PE, byte 3	CB-2A1-E04
	60		PSR 3.25A	PSR 4.7-02	PSR	PFS50	Data assembler rgtr PE, byte 4	CB-2A1-E05
	61		PSR 3.25A	PSR 4.7-03	PSR	PFS51	Data assembler rgtr PE, byte 5	CB-2A1-F04
	62		PSR 3.25A	PSR 4.7-03	PSR	PFS52	Data assembler rgtr PE, byte 6	CB-2A1-F01
	63		PSR 3.25A	PSR 4.7-03	PSR	PFS53	Data assembler rgtr PE, byte 7	CB-2A1-F02

PROC-990, 992, 994, 990E, 995E PFSD REGISTER (8D) (Sheet 1 of 2)

Byte	Bit(s)	Due	Level 3 Diagram	Level 4 Diagram	Unit	Signal Name	Description	FRU
	00	I	PSR 3.19B	PSR 4.6A-04	PSR	PFS43	Load and vector response code PE, byte 0	0FZH-2B5-GL
	01	I	PSR 3.19B	PSR 4.6A-04	PSR	PFS44	Load and vector response code PE, byte 1	0FZH-2B5-GL
	02	I	PSR 3.19D	PSR 4.6B-04	PSR	PFS45	Store response code PE, byte 0	0FZH-2B5-FL
0	03	I	PSR 3.7B	PSR 4.4-02	PSR	PFS18	Job process state pointer PE, bytes 4, 5	0FUH-2C5-CL
	04	I	PSR 3.7B	PSR 4.4-02	PSR	PFS19	Job process state pointer PE, bytes 6, 7	0FUH-2C5-CU
	05	I	PSR 3.7B	PSR 4.4-02	PSR	PFS21	MM bytes 6, 7 or UM byte 7 PE	0FUH-2C5-EU
	06		PSR 3.2A	PSR 4.0-03	PSR	PFS22	Model dependent word PE, byte 0	CU-2C5-K01
	07		PSR 3.2A	PSR 4.0-03	PSR	PFS23	Model dependent word PE, byte 1	CU-2C5-K01
	08						(Not used)	
	09		PSR 3.7B	PSR 4.4-02	PSR	PFS20	PTL or STL or KM PE, bytes 6, 7	0FUH-2C5-DU
	10		PSR 3.3B	PSR 4.1C-00	PSR	PFS24	Bytes 2 and 3 board A output mux PE	0FUH-2C5-EL
1	11		PSR 3.3B	PSR 4.1B-00	PSR	PFS25	Bytes 4 and 5 board A output mux PE	0FUH-2C5-CL
	12		PSR 3.3B	PSR 4.1A-00	PSR	PFS26	Bytes 6 and 7 board A output mux PE	0FUH-2C5-CU
	13		PSR 3.5D	PSR 4.2B-00	PSR	PFS27	Bytes 4 and 5 board B output mux PE	0FUH-2C5-DL
	14		PSR 3.5D	PSR 4.2A-00	PSR	PFS28	Bytes 6 and 7 board B output mux PE	0FUH-2C5-DU
	15		PSR 3.7D	PSR 4.3-00	PSR	PFS29	Bytes 6 and 7 board C output mux PE	0FUH-2C5-EU
	16						(Not used)	
	17		PSR 3.0D	PSR 4.4-03	PSR	PFS36	Data result rgtr PE, byte 0	CE-2A5-K11
	18		PSR 3.0D	PSR 4.4-03	PSR	PFS37	Data result rgtr PE, byte 2	CU-2A5-K06
2	19		PSR 3.0D	PSR 4.4-03	PSR	PFS38	Data result rgtr PE, byte 3	CU-2A5-K06
	20		PSR 3.0D	PSR 4.4-03	PSR	PFS39	Data result rgtr PE, byte 4	CU-2A5-K07
	21		PSR 3.0D	PSR 4.4-03	PSR	PFS40	Data result rgtr PE, byte 5	CU-2A5-K07
	22		PSR 3.0D	PSR 4.4-03	PSR	PFS41	Data result rgtr PE, byte 6	CU-2A5-K08
	23		PSR 3.0D	PSR 4.4-03	PSR	PFS42	Data result rgtr PE, byte 7	CU-2A5-K08
	24,25						(Not used)	
	26		PSR 3.29B	PSR 4.9-07	PSR	PFS86	Port A response code, bit 1	CU-2B5-B09
	27	I	PSR 3.29B	PSR 4.9-07	PSR	PFS87	Port A response code, bit 2	CU-2B5-B09
3	28		PSR 3.29B	PSR 4.9-07	PSR	PFS88	Port B response code, bit 1	CU-2B5-B09
	29	I	PSR 3.29B	PSR 4.9-07	PSR	PFS89	Port B response code, bit 2	CU-2B5-B09
	30		PSR 3.29B	PSR 4.9-07	PSR	PFS90	Port C response code, bit 1	0FZH-2B5-FL
	31	I	PSR 3.29B	PSR 4.9-07	PSR	PFS91	Port C response code, bit 2	0FZH-2B5-FL

PROC-990, 992, 994, 990E, 995E PFSD REGISTER (8D) (Sheet 2 of 2)

Byte	Bit(s)	Due	Level 3 Diagram	Level 4 Diagram	Unit	Signal Name	Description	FRU
	32	I	PSR 3.4F	PSR 4.4-02	PSR	PFS92	PTA PE	0FUH-2C5-DL
4	33		PSR 3.30A	PSR 4.9-07	PSR	PFS93	Test retry	CU-2B5-B09
	34-39						(Not used)	
	40,41						(Not used)	
	42		PMF 3.2B	PMF 4.0-07	PMF	PFS0	Rgtr 22 byte 3 PE, bits 0-7	CE-1B1-B09
	43		PMF 3.2C	PMF 4.0-07	PMF	PFS1	Rgtr 22 byte 2 PE, bits 0-7	CE-1B1-B09
5	44		PMF 3.2A	PMF 4.1-00	PMF	PFS2	Rgtr 22 byte 8 PE, bits 0-7	CE-1B1-D01
	45		PMF 3.2A	PMF 4.1-00	PMF	PFS3	Rgtr 22 byte 9 PE, bits 0-7	CE-1B1-D01
	46		PMF 3.2A	PMF 4.1-00	PMF	PFS4	Rgtr 22 byte 10 PE, bits 0-7	CE-1B1-G01
	47		PMF 3.2A	PMF 4.1-00	PMF	PFS5	Rgtr 22 byte 11 PE, bits 0-7	CE-1B1-E01
	48		PMF 3.2A	PMF 4.1-01	PMF	PFS6	Rgtr 22 byte 12 PE, bits 0-7	CE-1B1-A01
	49		PMF 3.2A	PMF 4.1-01	PMF	PFS7	Rgtr 22 byte 13 PE, bits 0-7	CE-1B1-A01
6	50		PMF 3.2A	PMF 4.1-01	PMF	PFS8	Rgtr 22 byte 14 PE, bits 0-7	CE-1B1-B01
	51		PMF 3.2A	PMF 4.1-01	PMF	PFS9	Rgtr 22 byte 15 PE, bits 0-7	CE-1B1-B01
	52-55						(Not used)	
	56-62						(Not used)	
7	63		PMF 3.7D	PMF 4.4-04	PMF	PFS21	Last stage of PMF read mux PE	CE-1B1-E05

PROC-990, 992, 994, 990E, 995E PFSE REGISTER (8E) (Sheet 1 of 2)

Byte	Bit(s)	Due	Level 3 Diagram	Level 4 Diagram	Unit	Signal Name	Description	FRU
	00	P	INU 3.10B	IN1 4.7-03	IN1	PFS19	180 instr map PE, byte 0	CU-2D4-C09
	01	P	INU 3.10B	IN1 4.7-03	IN1	PFS20	180 instr map PE, byte 1	CU-2D4-C09
	02	P	INU 3.10B	IN1 4.7-03	IN1	PFS21	180 instr map PE, byte 2	CU-2D4-C09
0	03	P	INU 3.10B	IN1 4.7-03	IN1	PFS22	180 instr map PE, byte 3	CU-2D4-C09
	04	P	INU 3.10B	IN1 4.7-03	IN1	PFS23	180 instr map PE, byte 4	CU-2D4-C09
	05	P	INU 3.10B	IN1 4.7-03	IN1	PFS24	180 instr map PE, byte 5	CU-2D4-C09
	06	P	INU 3.10B	IN1 4.7-03	IN1	PFS25	170 instr map PE, byte 0	CU-2D4-C09
	07	P	INU 3.10B	IN1 4.7-03	IN1	PFS26	170 instr map PE, byte 1	CU-2D4-C09
	08		INU 3.8C	IN1 4.8-00	IN1	PFS27	Instr output rgtr PE, byte 0	CU-2D4-K07
	09		INU 3.8C	IN1 4.8-00	IN1	PFS28	Instr output rgtr PE, byte 1	CU-2D4-K07
	10		INU 3.8C	IN1 4.8-00	IN1	PFS29	Instr output rgtr PE, byte 2	CU-2D4-K06
1	11		INU 3.8C	IN1 4.8-00	IN1	PFS30	Instr output rgtr PE, byte 3	CU-2D4-K06
	12		INU 3.11B	IN1 4.8-00	IN1	PFS31	Instr adrs output rgtr PE, byte 0	CU-2D5-F01
	13		INU 3.11B	IN1 4.8-00	IN1	PFS32	Instr adrs output rgtr PE, byte 1	CU-2D5-F01
	14		INU 3.11B	IN1 4.8-00	IN1	PFS33	Instr adrs output rgtr PE, byte 2	CU-2D5-G01
	15		INU 3.11B	IN1 4.8-00	IN1	PFS34	Instr adrs output rgtr PE, byte 3	CU-2D5-G01
	16		INU 3.1C	IN1 4.0-02	IN1	PFS0	IBA rank 1 rgtr PE, byte 4	CE-2D5-B01
	17		INU 3.1C	IN1 4.0-02	IN1	PFS1	IBA rank 1 rgtr PE, byte 5	CE-2D5-B01
	18		INU 3.1C	IN1 4.0-02	IN1	PFS2	IBA rank 1 rgtr PE, byte 6	CE-2D5-A01
2	19		INU 3.1C	IN1 4.8-02	IN1	PFS3	IBA rank 1 rgtr PE, byte 7	CE-2D5-A01
	20	I	INU 3.0F	IN1 4.1-04	IN1	PFS10	SVA rgtr PE, byte 4	CU-2D4-H01
	21	I	INU 3.0F	IN1 4.1-04	IN1	PFS11	SVA rgtr PE, byte 5	CU-2D4-H01
	22	I	INU 3.0F	IN1 4.1-04	IN1	PFS12	SVA rgtr PE, byte 6	CU-2D4-H02
	23	I	INU 3.0F	IN1 4.1-04	IN1	PFS13	SVA rgtr PE, byte 7	CU-2D4-H02
	24	P	INU 3.0C	IN1 4.1-05	IN1	PFS14	Real mem adrs rgtr PE, byte 4	CU-2D4-K01
	25	P	INU 3.0C	IN1 4.1-05	IN1	PFS15	Real mem adrs rgtr PE, byte 5	CU-2D4-K01
	26	P	INU 3.6B	IN1 4.4-00	IN1	PFS16	Error rgtr PE, byte 0	CU-2D5-K03
3	27	P	INU 3.6B	IN1 4.4-00	IN1	PFS17	Error rgtr PE, byte 1	CU-2D5-K03
	28	I	INU 3.3A	IN1 4.3-02	IN1	PFS35	Outstanding request cntr A response error	CD-2D4-G12
	29	I	INU 3.3A	IN1 4.3-02	IN1	PFS36	Outstanding request cntr B response error	CD-2D4-F12
	30	I	INU 3.3A	IN1 4.3-02	IN1	PFS37	Outstanding request cntr C response error	CD-2D4-G13
	31	I	INU 3.3A	IN1 4.3-02	IN1	PFS38	Outstanding request cntr D response error	CD-2D4-G14

PROC-990, 992, 994, 990E, 995E PFSE REGISTER (8E) (Sheet 2 of 2)

Byte	Bit(s)	Due	Level 3 Diagram	Level 4 Diagram	Unit	Signal Name	Description	FRU
	32	P	INU 3.6C	IN1 4.4-00	IN1	PFS18	Response code PE, byte 0	HA-2D5-G02B
	33	P	INU 3.0B	IN1 4.1-04	IN1	PFS7	Page frame adrs rgtr PE, byte 4	CU-2D4-A06
	34	P	INU 3.0B	IN1 4.1-04	IN1	PFS8	Page frame adrs rgtr PE, byte 5	CU-2D4-A06
4	35	P	INU 3.0B	IN1 4.1-04	IN1	PFS9	Page frame adrs rgtr PE, byte 6	CU-2D4-J08
	36		INU 3.8C	IN1 4.8-00	IN1	PFS39	IBS set 0 PE	HE-2D4-K03B
	37		INU 3.8C	IN1 4.8-00	IN1	PFS40	IBS set 1 PE	HE-2D4-K03B
	38		INU 3.8C	IN1 4.8-00	IN1	PFS41	IBS set 2 PE	HE-2D4-K03B
	39		INU 3.8C	IN1 4.8-00	IN1	PFS42	IBS set 3 PE	HE-2D4-K03B
	40	P	INU 3.5C	IN1 4.3-06	IN1	PFS5	Multiple lookahead hits	CU-2D4-A15
	41	P	INU 3.5C	IN1 4.3-06	IN1	PFS6	Multiple read hits	CU-2D4-A15
5	42-45						(Not used)	
	46	I	EPN 3.2D	EPN 4.1-00	EPN	PFS12	LSU fatal X tag error	HE-1A5-J13B
	47	I	EPN 3.2D	EPN 4.1-00	EPN	PFS13	RPL fatal X tag error	SG-1A5-H12
	48	I	EPN 3.6B	EPN 4.12-02	EPN	PFS11	Soft cont error halt	AF-1A5-K14
	49		EPN 3.7A	EPN 4.1-01	EPN	PFS14	Fetch error missed	AF-1A5-D15
6	50-52						(Not used)	
	53	I	EPN 3.1A	EPN 4.2-00	EPN	PFS7	EPN micr PE, byte 0	SP-1A5-C13
	54						(Not used)	
	55	I	EPN 3.7F	EPN 4.7-00	EPN	PFS9	Delayed entry count rgtr PE	CU-1A5-J01
	56	I	EPN 3.4D	EPN 4.7-02	EPN	PFS10	Instr completion rgtr PE	CU-1A5-H06
	57	I	EPN 3.2E	EPN 4.1-01	EPN	PFS0	RPL tag PE	HA-1A5-D14B
	58	I	EPN 3.2E	EPN 4.1-01	EPN	PFS1	LSU tag PE	HA-1A5-D14B
7	59	I	EPN 3.0B	EPN 4.1-01	EPN	PFS2	ACU tag PE	CU-1A5-D12
	60	I	EPN 3.6F	EPN 4.12-01	EPN	PFS3	SCM data rgtr PE, byte 0	CE-1A5-D08
	61	I	EPN 3.6F	EPN 4.12-01	EPN	PFS4	SCM data rgtr PE, byte 1	CE-1A5-D06
	62	I	EPN 3.6F	EPN 4.12-01	EPN	PFS5	SCM data rgtr PE, byte 2	CE-1A5-D07
	63	I	EPN 3.6F	EPN 4.12-01	EPN	PFS6	Unused soft cont entry	CE-1A5-D06

PROC-990, 992, 994, 990E, 995E PFSF REGISTER (8F) (Sheet 1 of 2)

Byte	Bit(s)	Due	Level 3 Diagram	Level 4 Diagram	Unit	Signal Name	Description	FRU
	00		OCA 3.5K	OCA 4.6C-06	OCA	PFS0	Data set 0 PE	EU-2B3-AU
	01		OCA 3.5K	OCA 4.6E-06	OCA	PFS1	Data set 1 PE	EU-2B3-AU
	02		OCA 3.5K	OCA 4.6C-06	OCA	PFS2	Data set 2 PE	EU-2B3-AU
0	03		OCA 3.5K	OCA 4.6E-06	OCA	PFS3	Data set 3 PE	EU-2B3-AU
	04		OCA 3.3L	OCA 4.5A-05	OCA	PFS10	Tag data set 0 PE	EX-2B3-FL
	05		OCA 3.3L	OCA 4.5B-05	OCA	PFS11	Tag data set 1 PE	EX-2B3-FU
	06		OCA 3.3L	OCA 4.5C-05	OCA	PFS12	Tag data set 2 PE	EX-2B3-EL
	07		OCA 3.3L	OCA 4.5D-05	OCA	PFS13	Tag data set 3 PE	EX-2B3-EU
	08		OCA 3.3L	OCA 4.5A-05	OCA	PFS20	Tag set 0 adrs PE	EX-2B3-FL
	09		OCA 3.3L	OCA 4.5B-05	OCA	PFS21	Tag set 1 adrs PE	EX-2B3-FU
	10		OCA 3.3L	OCA 4.5C-05	OCA	PFS22	Tag set 2 adrs PE	EX-2B3-EL
1	11		OCA 3.3L	OCA 4.5D-05	OCA	PFS23	Tag set 3 adrs PE	EX-2B3-EU
	12		OCA 3.4H	OCA 4.5A-06	OCA	PFS24	Set 0 stale data	EX-2B3-FL
	13		OCA 3.4H	OCA 4.5B-06	OCA	PFS49	Set 1 stale data	EX-2B3-FU
	14		OCA 3.4H	OCA 4.5C-06	OCA	PFS50	Set 2 stale data	EX-2B3-EL
	15		OCA 3.4H	OCA 4.5D-06	OCA	PFS62	Set 3 stale data	EX-2B3-EU
	16		OCA 3.5C	OCA 4.6A-06	OCA	PFS53	Data PE, byte 0	EU-2B3-AU
	17		OCA 3.5C	OCA 4.6B-06	OCA	PFS54	Data PE, byte 1	EU-2B3-AL
	18		OCA 3.5C	OCA 4.6C-06	OCA	PFS55	Data PE, byte 2	EU-2B3-BL
2	19		OCA 3.5C	OCA 4.6D-06	OCA	PFS56	Data PE, byte 3	EU-2B3-CU
	20		OCA 3.5C	OCA 4.6E-06	OCA	PFS57	Data PE, byte 4	EU-2B3-BU
	21		OCA 3.5C	OCA 4.6F-06	OCA	PFS58	Data PE, byte 5	EU-2B3-CL
	22		OCA 3.5C	OCA 4.6G-06	OCA	PFS59	Data PE, byte 6	EU-2B3-DL
	23		OCA 3.5C	OCA 4.6H-06	OCA	PFS60	Data PE, byte 7	EU-2B3-DU
	24		OCA 3.0A	OCA 4.0-00	OCA	PFS52	Upper adrs mux/rgtr PE, byte 7	CB-2A3-H13
	25	I	OCA 3.4B	OCA 4.0-03	OCA	PFS25	Multiple set tag compare	
	26		OCA 3.2E	OCA 4.4-04	OCA	PFS61	Set allocation error	
3	27						(Not used)	
	28		OCA 3.0E	OCA 4.0-00	OCA	PFS26	Lower adrs mux/rgtr PE	AM-2A3-K15
	29		OCA 3.0A	OCA 4.0-00	OCA	PFS27	Upper adrs mux/rgtr PE, byte 2	CB-2A3-G13
	30		OCA 3.0A	OCA 4.0-00	OCA	PFS28	Upper adrs mux/rgtr PE, byte 3	CB-2A3-G14
	31		OCA 3.0A	OCA 4.0-00	OCA	PFS29	Upper adrs mux/rgtr PE, byte 4	CB-2A3-G15

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Byte	Bit(s)	Due	Level 3 Diagram	Level 4 Diagram	Unit	Signal Name	Description	FRU
	32		OCA 3.0A	OCA 4.0-00	OCA	PFS30	Upper adrs mux/rgtr PE, byte 5	CB-2A3-J14
	33		OCA 3.0A	OCA 4.0-00	OCA	PFS31	Upper adrs mux/rgtr PE, byte 6	CB-2A3-H14
	34		OCA 3.0B	OCA 4.0-01	OCA	PFS14	Address mux/rgtr 1 PE, byte 2	CB-2B2-G14
4	35		OCA 3.0B	OCA 4.0-02	OCA	PFS15	Address mux/rgtr 1 PE, byte 3	CB-2B2-G15
	36		OCA 3.0B	OCA 4.0-01	OCA	PFS16	Address mux/rgtr 1 PE, byte 4	CB-2B3-K11
	37		OCA 3.0B	OCA 4.0-01	OCA	PFS17	Address mux/rgtr 1 PE, byte 5	CB-2B3-K07
	38		OCA 3.0B	OCA 4.0-01	OCA	PFS18	Address mux/rgtr 1 PE, byte 6	CB-2B3-K03
	39		OCA 3.0B	OCA 4.0-01	OCA	PFS19	Address mux/rgtr 1 PE, byte 7	CB-2B3-K01
	40		OCA 3.0D	OCA 4.0-02	OCA	PFS4	SVA rgtr 2 PE, byte 2	CE-2A3-G06
	41		OCA 3.0D	OCA 4.0-02	OCA	PFS5	SVA rgtr 2 PE, byte 3	CE-2A3-K01
	42		OCA 3.0D	OCA 4.0-02	OCA	PFS6	SVA rgtr 2 PE, byte 4	CE-2A3-G07
5	43		OCA 3.0D	OCA 4.0-02	OCA	PFS7	SVA rgtr 2 PE, byte 5	CE-2A3¬J01
	44		OCA 3.0D	OCA 4.0-02	OCA	PFS8	SVA rgtr 2 PE, byte 6	CE-2A3-G02
	45		OCA 3.0D	OCA 4.0-02	OCA	PFS9	SVA rgtr 2 PE, byte 7	CE-2A3-G01
	46		OCA 3.0D	OCA 4.0-02	OCA	PFS32	SVA rgtr 3 PE, byte 2	CE-2A3-G06
	47		OCA 3.0D	OCA 4.0-02	OCA	PFS33	SVA rgtr 3 PE, byte 3	CE-2A3-K01
	48		OCA 3.0D	OCA 4.0-02	OCA	PFS34	SVA rgtr 3 PE, byte 4	CE-2A3-G07
	49		OCA 3.0D	OCA 4.0-02	OCA	PFS35	SVA rgtr 3 PE, byte 5	CE-2A3¬J01
	50		OCA 3.0D	OCA 4.0-02	OCA	PFS36	SVA rgtr 3 PE, byte 6	CE-2A3-G02
6	51		OCA 3.0D	OCA 4.0-02	OCA	PFS37	SVA rgtr 3 PE, byte 7	CE-2A3-G01
	52		OCA 3.10E	OCA 4.0-06	OCA	PFS38	Prefetch rgtr 4 PE, byte 2	CU-2A3-H04
	53		OCA 3.10E	OCA 4.0-06	OCA	PFS39	Prefetch rgtr 4 PE, byte 3	CU-2A3-H04
	54		OCA 3.10E	OCA 4.0-06	OCA	PFS40	Prefetch rgtr 4 PE, byte 4	CU-2A3-J05
	55		OCA 3.10E	OCA 4.0-06	OCA	PFS41	Prefetch rgtr 4 PE, byte 5	CU-2A3¬J05
	56		OCA 3.10E	OCA 4.0-06	OCA	PFS42	Prefetch rgtr 4 PE, byte 6	CU-2A3-H05
	57		OCA 3.2B	OCA 4.0-08	OCA	PFS51	Cache load rgtr 2 PE	CE-2A3-K09
	58		OCA 3.2B	OCA 4.0-07	OCA	PFS43	Cache load rgtr 1 PE, byte 2	CE-2A3-K09
7	59		OCA 3.2B	OCA 4.0-07	OCA	PFS44	Cache load rgtr 1 PE, byte 3	CE-2A3¬J10
	60		OCA 3.2B	OCA 4.0-07	OCA	PFS45	Cache load rgtr 1 PE, byte 4	CE-2A3-J11
	61		OCA 3.2B	OCA 4.0-07	OCA	PFS46	Cache load rgtr 1 PE, byte 5	CE-2A3-K11
	62		OCA 3.2B	OCA 4.0-07	OCA	PFS47	Cache load rgtr 1 PE, byte 6	CE-2A3-K10
	63		OCA 3.2B	OCA 4.0-07	OCA	PFS48	Cache load rgtr 1 PE, byte 7	CE-2A3¬J13

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Byte	Bit(s)	Due	Level 3 Diagram	Level 4 Diagram	Unit	Signal Name	Description	FRU
	00		IDU 3.18A	IDU 4.5H-04	IDU	PTM38	Force MAC CIR read data PE board H	
	01		IDU 3.18A	IDU 4.5G-04	IDU	PTM39	Force MAC CIR read data PE board G	
	02		IDU 3.18A	IDU 4.5F-04	IDU	PTM40	Force MAC CIR read data PE board F	
0	03		IDU 3.18A	IDU 4.5E-04	IDU	PTM41	Force MAC CIR read data PE board E	
	04		IDU 3.18A	IDU 4.5D-04	IDU	PTM42	Force MAC CIR read data PE board D	
	05		IDU 3.18A	IDU 4.5C-04	IDU	PTM43	Force MAC CIR read data PE board C	
	06		IDU 3.18A	IDU 4.5B-04	IDU	PTM44	Force MAC CIR read data PE board B	
	07		IDU 3.18A	IDU 4.5A-04	IDU	PTM45	Force MAC CIR read data PE board A	
	08		IDU 3.9A	IDU 4.3-04	IDU	PTM37	Force PE on number of words rgtr	
	09		IDU 3.17H	IDU 4.6-02	IDU	PTM3	Force PE on LSU cont 2 data	
	10						(Not used)	
1	11		IDU 3.17Q	IDU 4.6-02	IDU	PTM4	Force PE on ACU micr, byte 0	
	12		IDU 3.17Q	IDU 4.6-02	IDU	PTM5	Force PE on ACU micr, byte 1	
	13		IDU 3.17Q	IDU 4.6-02	IDU	PTM6	Force PE on ACU micr, byte 2	
	14		IDU 3.17Q	IDU 4.6-02	IDU	PTM7	Force PE on ACU micr, byte 3	
	15		IDU 3.17Q	IDU 4.6-02	IDU	PTM8	Force PE on ACU micr, byte 4	
	16		IDU 3.21A	IDU 4.7-08	IDU	PTM12	Force PE on CSA sequencing fault	
	17		IDU 3.17S	IDU 4.6-01	IDU	PTM1	Force PE on result destn tag, byte 0	
	18		IDU 3.17S	IDU 4.6-01	IDU	PTM2	Force PE on result destn tag, byte 1	
2	19		IDU 3.17J	IDU 4.6-02	IDU	PTM14	Force PE on LSU cont 4 data	
	20		IDU 3.17F	IDU 4.6-02	IDU	PTM20	Force PE on LSU cont 7 data	
	21		IDU 3.14B	IDU 4.6-02	IDU	PTM21	Force PE on CWD instr descr, byte 0	
	22		IDU 3.14B	IDU 4.6-02	IDU	PTM22	Force PE on CWD instr descr, byte 1	
	23		IDU 3.14B	IDU 4.6-02	IDU	PTM23	Force PE on CWD instr descr, byte 2	
	24		IDU 3.17L	IDU 4.6-02	IDU	PTM18	Force PE on BDP micr, byte 0	
	25		IDU 3.17L	IDU 4.6-02	IDU	PTM19	Force PE on BDP micr, byte 1	
	26		IDU 3.17M	IDU 4.6-02	IDU	PTM9	Force PE on LSU cont 1, byte 0	
3	27		IDU 3.17M	IDU 4.6-02	IDU	PTM10	Force PE on LSU cont 1, byte 1	
	28		IDU 3.17M	IDU 4.6-02	IDU	PTM11	Force PE on LSU cont 1, byte 2	
	29		IDU 3.17E	IDU 4.6-02	IDU	PTM15	Force PE on LSU cont 5, byte 0	
	30		IDU 3.17E	IDU 4.6-02	IDU	PTM16	Force PE on LSU cont 5, byte 1	
	31		IDU 3.17E	IDU 4.6-02	IDU	PTM17	Force PE on LSU cont 5, byte 2	

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Byte	Bit(s)	Due	Level 3 Diagram	Level 4 Diagram	Unit	Signal Name	Description	FRU
	32,33						(Not used)	
	34		PMF 3.0F	PMF 4.0-08	PMF	PTM2	Select scope sync start trigger	
	35		PMF 3.0F	PMF 4.0-08	PMF	PTM3	Select CSA compare start trigger	
4	36		PMF 3.0F	PMF 4.0-08	PMF	PTM4	Select scope sync stop trigger	
	37		PMF 3.0F	PMF 4.0-08	PMF	PTM5	Select CSA compare stop trigger	
	38		PMF 3.5A	PMF 4.3-00	PMF	PTM6	Force parity on byte 0 of bfr data	
	39		PMF 3.5A	PMF 4.3-00	PMF	PTM7	Force parity on byte 1 of bfr data	
	40		PMF 3.5A	PMF 4.3-00	PMF	PTM8	Force parity on byte 2 of bfr data	
	41		PMF 3.5A	PMF 4.3-00	PMF	PTM9	Force parity on byte 3 of bfr data	
	42		PMF 3.5A	PMF 4.3-00	PMF	PTM10	Force parity on byte 4 of bfr data	
5	43		PMF 3.5A	PMF 4.3-00	PMF	PTM11	Force parity on byte 5 of bfr data	
	44		PMF 3.5A	PMF 4.3-00	PMF	PTM12	Force parity on byte 6 of bfr data	
	45		PMF 3.5A	PMF 4.3-00	PMF	PTM13	Force parity on byte 7 of bfr data	
	46		PMF 3.0F,5A	PMF 4.0-08	PMF	PTM14	Test write, sel zeros, stop on overflow	
	47		PMF 3.0E	PMF 4.0-08	PMF	PTM15	Select 20 pattern as test write data	
	48		IDU 3.4B	IDU 4.1H-04	IDU	PTM28	Force seg map mem check error board 0	
	49		IDU 3.4B	IDU 4.1G-04	IDU	PTM29	Force seg map mem check error board 1	
	50		IDU 3.4B	IDU 4.1F-04	IDU	PTM30	Force seg map mem check error board 2	
6	51		IDU 3.4B	IDU 4.1E-04	IDU	PTM31	Force seg map mem check error board 3	
	52		IDU 3.4B	IDU 4.1D-04	IDU	PTM32	Force seg map mem check error board 4	
	53		IDU 3.4B	IDU 4.1C-04	IDU	PTM33	Force seg map mem check error board 5	
	54		IDU 3.4B	IDU 4.1B-04	IDU	PTM34	Force seg map mem check error board 6	
	55		IDU 3.4B	IDU 4.1A-04	IDU	PTM35	Force seg map mem check error board 7	
	56		IDU 3.0A	IDU 4.0-04	IDU	PTM36	Force branch cond	
	57,58						(Not used)	
	59		IDU 3.7A	IDU 4.2-00	IDU	PTM24	Enbl CSA instr to CSA UTP rgtr	
7	60						(Not used)	
	61		IDU 3.7A	IDU 4.2-00	IDU	PTM46	Enbl MAC write of CSA P-right	
	62		IDU 3.17V	IDU 4.6-01	IDU	PTM0	Force PE on EPN micr, byte 0	
	63		IDU 3.4A	IDU 4.6-00	IDU	PTM13	Force PE on PSR write adrs	

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Byte	Bit(s)	Due	Level 3 Diagram	Level 4 Diagram	Unit	Signal Name	Description	FRU
	00-03						(Not used)	
0	04		MAC 3.0A	MAC 4.1-01	MAC	PTM0	Force MAC write data PE	
	05		MAC 3.7A	MAC 4.1-08	MAC	PTM1	Force PFS/DEC/PTM read data PE	
	06,07						(Not used)	
	08		AC1 3.22A	AC1 4.1-01	AC1	PTM0	Force PE on length rgtr	
	09		AC1 3.18C	AC1 4.0-04	AC1	PTM1	Force PE on byte number adder	
	10		AC1 3.19E	AC1 4.0-06	AC1	PTM2	Force interval holding rgtr PE	
1	11		AC1 3.3B	AC1 4.5-01	AC1	PTM3	Force LSU tag rank 4 rgtr PE	
	12		AC1 3.26A	AC1 4.2-00	AC1	PTM5	Force valid holding rgtr PE	
	13		AC1 3.32B	AC1 4.4-00	AC1	PTM6	Force X rgtr data rgtr PE	
	14		AC1 3.34A	AC1 4.4-02	AC1	PTM7	Force stack frame save area local/global key rgtr PE	
	15		AC1 3.24B	AC1 4.2-14	AC1	PTM15	Force carry on SDF/RMA adder	
	16		AC1 3.28A	AC1 4.2-13	AC1	PTM16	Block STA invalidation	
	17						(Not used)	
	18		AC1 3.19C	AC1 4.0-06	AC1	PTM9	Force byte length PE	
2	19		AC1 3.13D	AC1 4.8-00	AC1	PTM11	Force rank 1 and 2 backup	
	20		AC1 3.13G	AC1 4.8-03	AC1	PTM12	Force rank 3 and 4 backup	
	21		AC1 3.25B	AC1 4.0-09	AC1	PTM13	Execute privilege in-RMA mode	
	22		AC1 3.25B	AC1 4.0-09	AC1	PTM14	Execute privilege in-RMA mode	
	23		AC1 3.15D	AC1 4.0-08	IN2	PTM0	Force slow unit delay	
	24		AC1 3.19A	IN2 4.0-08	IN2	PTM1	Issue timeout timer set, bit 5	
	25		AC1 3.19A	IN2 4.0-08	IN2	PTM2	Issue timeout timer set, bit 6	
	26		AC1 3.19A	IN2 4.0-08	IN2	PTM3	Issue timeout timer set, bit 7	
3	27		AC1 3.19C	IN2 4.0-08	IN2	PTM4	Enbl FPU and IGU short stop cntrs	
	28		AC1 3.23D	AC1 4.2-01	AC1	PTM4	Force PE on rank 2 ring and seg rgtr	
	29						(Not used)	
	30		AC1 3.37B	AC1 4.7-03	AC1	PTM8	Force error rgtr rank 5 PE	
	31		AC1 3.32C	AC1 4.4-09	AC1	PTM10	Force largest ring number rgtr PE	

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Byte	Bit(s)	Due	Level 3 Diagram	Level 4 Diagram	Unit	Signal Name	Description	FRU
	32		AC2 3.13B	AC2 4.9-0	AC2	PTM102	Toggle page index bits 56-60 parity	
	33		AC2 3.24A	AC2 4.8-03	AC2	PTM103	Force LSU store data ready	
	34						(Not used)	
	35		AC2 3.17A	AC2 4.3-01	AC2	PTM105	Toggle page offset upper parity	
4	36						(Not used)	
	37		AC2 3.21A	AC2 4.7-05	AC2	PTM107	Dsbl port B miss bytes 4 and 5	
	38		AC2 3.2D	AC2 4.7-00	AC2	PTM108	Toggle CMC fctn parity	
	39		AC2 3.17D	AC2 4.3-01	AC2	PTM109	Toggle page RMA sel parity	
	40						(Not used)	
	41		AC2 3.3B	AC2 4.5-00	AC2	PTM112	Dsbl backup enable	
	42		AC2 3.19B	AC2 4.6-03	AC2	PTM113	Toggle port A tag parity	
5	43		AC2 3.14B	AC2 4.0-01	AC2	PTM114	Toggle rank 4 masked SVA parity	
	44		AC2 3.29C	AC2 4.10-01	AC2	PTM115	Toggle data result masked debug parity bit	
	45		AC2 3.2C	AC2 4.0-04	AC2	PTM110	Toggle SCM4 backup delay rgtr parity	
	46		AC2 3.30C	AC2 4.5-03	AC2	PTM100	Force store wait cntr DUE	
	47		AC2 3.22B	AC2 4.8-08	AC2	PTM101	Force store tag PE	
	48		DIV 3.8A	DIV 4.0-32	SCU	PTM0	Enbl result compare, byte 0	
	49		DIV 3.6A	DIV 4.0-58	SCU	PTM1	Enbl result compare, byte 1	
	50		DIV 3.6C	DIV 4.0-58	SCU	PTM2	Enbl result compare, byte 2	
6	51		DIV 3.6C	DIV 4.0-58	SCU	PTM3	Enbl result compare, byte 3	
	52		DIV 3.6C	DIV 4.0-58	SCU	PTM4	Enbl result compare, byte 4	
	53		DIV 3.7A	DIV 4.0-30	SCU	PTM5	Enbl result compare, byte 5	
	54		DIV 3.8A	DIV 4.0-32	SCU	PTM6	Stop after first iteration of instr	
	55		DIV-B 3.12A	DIV-B 4.0-70	SCU	PTM7	Enbl double-precision data to output (990E, 995E)	
	56		IMU 3.1A	IMU 4.0-18	SCU	PTM8	Clear FPM result catch rgtr	
	57		IMU 3.4D, 3.0C	IMU 4.0-17	SCU	PTM14	Force IMU output mux to C input	
	58						(Not used)	
7	59		IMU 3.5A	IMU 4.0-12	SCU	PTM9	Select error cntr attempt count	
	60		IMU 3.5A	IMU 4.0-12	SCU	PTM10	Force error and attempt count to zero	
	61		IMU 3.5A	IMU 4.0-12	SCU	PTM11	Dsbl FPM and IMU compare	
	62		IMU 3.5A	IMU 4.0-12	SCU	PTM12	Force error in FP compare	
	63		IMU 3.5C	IMU 4.0-10	SCU	PTM13	Force BDP overflow byte rgtr PE	

PROC-990, 992, 994, 990E, 995E PTM REGISTER (A2) (Sheet 1 of 2)

Byte	Bit(s)	Due	Level 3 Diagram	Level 4 Diagram	Unit	Signal Name	Description	FRU
	00		CMC 3.0C	CM1 4.0B-06	CM1	PTM0	Force adrs PE, bits 34-39 port 0B	
	01		CMC 3.0C	CM1 4.0A-06	CM1	PTM1	Force adrs PE, bits 34-39 port 0A	
	02		CMC 3.0C	CM1 4.0C-06	CM1	PTM2	Force adrs PE, bits 34-39 port 0C	
0	03		CMC 3.9D	CM1 4.6-03	CM1	PTM3	Force adrs PE, bits 34-39 port 1S	
	04		CMC 3.0C	CM1 4.3B-06	CM1	PTM4	Force adrs PE, bits 34-39 port 2B	
	05		CMC 3.0C	CM1 4.3A-06	CM1	PTM5	Force adrs PE, bits 34-39 port 2A	
	06		CMC 3.0C	CM1 4.3C-06	CM1	PTM6	Force adrs PE, bits 34-39 port 2C	
	07		CMC 3.9D	CM1 4.9-03	CM1	PTM7	Force adrs PE, bits 34-39 port 3S	
	08		CMC 3.0C	CM1 4.0B-06	CM1	PTM8	Force adrs PE, bits 40-47 port 0B	
	09		CMC 3.0C	CM1 4.0A-06	CM1	PTM9	Force adrs PE, bits 40-47 port 0A	
	10		CMC 3.0C	CM1 4.0C-06	CM1	PTM10	Force adrs PE, bits 40-47 port 0C	
1	11		CMC 3.9D	CM1 4.6-03	CM1	PTM11	Force adrs PE, bits 40-47 port 1S	
	12		CMC 3.0C	CM1 4.3B-06	CM1	PTM12	Force adrs PE, bits 40-47 port 2B	
	13		CMC 3.0C	CM1 4.3A-06	CM1	PTM13	Force adrs PE, bits 40-47 port 2A	
	14		CMC 3.0C	CM1 4.3C-06	CM1	PTM14	Force adrs PE, bits 40-47 port 2C	
	15		CMC 3.9D	CM1 4.9-03	CM1	PTM15	Force adrs PE, bits 40-47 port 3S	
	16		CMC 3.0C	CM1 4.0B-06	CM1	PTM16	Force adrs PE, bits 56-60 port 0B	
	17		CMC 3.0C	CM1 4.0A-06	CM1	PTM17	Force adrs PE, bits 56-60 port 0A	
	18		CMC 3.0C	CM1 4.0C-06	CM1	PTM18	Force adrs PE, bits 56-60 port 0C	
2	19		CMC 3.9D	CM1 4.6-03	CM1	PTM19	Force adrs PE, bits 56-60 port 1S	
	20		CMC 3.0C	CM1 4.3B-06	CM1	PTM20	Force adrs PE, bits 56-60 port 2B	
	21		CMC 3.0C	CM1 4.3A-06	CM1	PTM21	Force adrs PE, bits 56-60 port 2A	
	22		CMC 3.0C	CM1 4.3C-06	CM1	PTM22	Force adrs PE, bits 56-60 port 2C	
	23		CMC 3.9D	CM1 4.9-03	CM1	PTM23	Force adrs PE, bits 56-60 port 3S	
	24		INU 3.6B	IN1 4.4-00	IN1	PTM7	Force error rgtr PE, bits 8-12	
	25		INU 3.11D	IN1 4.7-01	IN1	PTM8	Dsbl branch	
	26		INU 3.4A	IN1 4.1-02	IN1	PTM9	Force lookahead hit	
3	27		CMC 3.27D	CM3 4.2-01	CM3	PTM1	Stop FRC	
	28		CMC 3.28A	CM1 4.1A-00	CM1	PTM24	Enbl short warning	
	29		CMC 3.28A	CM1 4.1A-00	CM1	PTM25	Enbl long warning	
	30		CMC 3.28A	CM3 4.2-04	CM3	PTM0	Force read PE on MAC read data	
	31		CMC 3.32C	CM4 4.1A-02	CM4	PTM0	Force response code PE all distributors	

PROC-990, 992, 994, 990E, 995E PTM REGISTER (A2) (Sheet 2 of 2)

Byte	Bit(s)	Due	Level 3 Diagram	Level 4 Diagram	Unit	Signal Name	Description	FRU
	32		INU 3.12A	IN1 4.7-04	IN1	PTM10	Dsbl branch prediction RAM, bit 0	
	33		INU 3.6C	IN1 4.4-00	IN1	PTM0	Force response code PE	
	34		INU 3.5C	IN1 4.3-06	IN1	PTM1	Dsbl multiple lookahead hits	
4	35		INU 3.5C	IN1 4.3-06	IN1	PTM2	Dsbl multiple read hits	
	36		INU 3.0C	IN1 4.1-05	IN1	PTM3	Force read memory adrs PE, bytes 6, 7	
	37		INU 3.6A	IN1 4.4-02	IN1	PTM4	Force 170 mode CMC read data errors	
	38		INU 3.1C	IN1 4.4-02	IN1	PTM5	Force IBA rank 1 PE, bytes 4-7	
	39		INU 3.0K	IN1 4.1-03	IN1	PTM6	Force destn tag PE	
	40		LSU 3.51A	LSU 4.1-04	LSU	PTM2	Toggle mark shift output mux parity	
	41						(Not used)	
	42		LSU 3.6A	LSU 4.9-08	LSU	PTM4	Read state cont parity toggle	
5	43		LSU 3.4A	LSU 4.9-08	LSU	PTM5	Write state cont parity toggle	
	44		LSU 3.25A	LSU 4.4-02	LSU	PTM6	Toggle ring number parity	
	45		LSU 3.25A	LSU 4.4-02	LSU	PTM7	Toggle load A data fanout parity	
	46		LSU 3.24D	LSU 4.4-04	LSU	PTM8	Toggle parity on the 170 exchange mux	
	47		LSU 3.23G	LSU 4.4-04	LSU	PTM9	Toggle parity on A-data bytes 5-7	
	48		LSU 3.22B	LSU 4.0-02	LSU	PTM10	Toggle parity on X-data bytes 0-7	
	49		LSU 3.41A	LSU 4.5-12	LSU	PTM11	Toggle parity on mem to mem cont	
6	50		LSU 3.32A	LSU 4.12-01	LSU	PTM1	Toggle parity on vector tag, byte 0	
	51		LSU 3.32A	LSU 4.12-01	LSU	PTM3	Toggle parity on vector tag, byte 1	
	52		LSU 3.49B	LSU 4.1-02	LSU	PTM0	Toggle parity on store data mux/rgtr 2	
	53						(Not used)	
	54		INU 3.3A	IN1 4.3-01	IN1	PTM11	Dsbl outstanding request cntr sets 0-3	
	55		INU 3.3A	IN1 4.3-02	IN1	PTM12	Dsbl request response error	
	56-58						(Not used)	
	59		OCA 3.0B	OCA 4.0-01	OCA	PTM0	Toggle adrs mux/rgtr 1, bit 77	
7	60		OCA 3.0B	OCA 4.0-01	OCA	PTM1	Toggle adrs mux/rgtr 1, bit 78	
	61		OCA 3.4G	OCA 4.5X-04	OCA	PTM2	Force OCA miss	
	62		OCA 3.7A	OCA 4.7-00	OCA	PTM3	Toggle MAC adrs rgtr parity	
	63		OCA 3.6D	OCA 4.7-03	OCA	PTM4	Toggle prefetch and validity data byte 2 parity	

PROC-990, 992, 994, 990E, 995E PTM REGISTER (A3) (Sheet 1 of 2)

Byte	Bit(s)	Due	Level 3 Diagram	Level 4 Diagram	Unit	Signal Name	Description	FRU
	00		EPN 3.8C	EPN 4.11-00	EPN	PTM0	Force not cancel	
	01		EPN 3.7C	EPN 4.13-00	EPN	PTM1	Force EIT rgtr PE	
	02		EPN 3.0D	EPN 4.0-00	EPN	PTM2	Force SCU error, bits 5 and 8	
0	03		EPN 3.0D	EPN 4.0-00	EPN	PTM3	Force IGU error, bits 0 and 3	
	04		EPN 3.0D	EPN 4.0-00	EPN	PTM4	Force FPU error, bits 1 and 9	
	05		EPN 3.7H	EPN 4.5-01	EPN	PTM5	Force entry cntrs parity bit	
	06		EPN 3.3C	EPN 4.6-00	EPN	PTM6	Dsbl tag count to delay store F/F	
	07		EPN 3.3D	EPN 4.3-00	EPN	PTM7	Set fatal P and P+ error flip-flops	
	08		PSR 3.1D	PSR 4.4-09	PSR	PTM0	Toggle monitor process state pointer parity	
	09		PSR 3.3A	PSR 4.4-09	PSR	PTM1	Toggle system interval timer parity	
	10		PSR 3.18B	PSR 4.6A-04	PSR	PTM2	Toggle VMID parity	
1	11		PSR 3.24A	PSR 4.7-00	PSR	PTM3	Toggle MAC cont and assy word PE	
	12		PSR 3.4E	PSR 4.4-09	PSR	PTM4	Toggle seg table adrs parity	
	13		PSR 3.5C	PSR 4.4-07	PSR	PTM5	Toggle process interval timer parity	
	14		PSR 3.1B	PSR 4.4-09	PSR	PTM6	Toggle TP parity	
	15		PSR 3.18C	PSR 4.6B-04	PSR	PTM7	Toggle UVMID parity	
	16		PSR 3.18A	PSR 4.6B-04	PSR	PTM8	Toggle trap enable parity	
	17		PSR 3.6E	PSR 4.3-01	PSR	PTM9	Toggle debug mask parity	
	18		PSR 3.6B	PSR 4.3-01	PSR	PTM10	Toggle page size mask parity	
2	19		PSR 3.7C	PSR 4.3-02	PSR	PTM11	Toggle debug index parity	
	20		PSR 3.11D	PSR 4.4-05	PSR	PTM12	Toggle user cond rgtr parity	
	21		PSR 3.21A	PSR 4.8-00	PSR	PTM13	Toggle call trap mux input 1 parity	
	22		PSR 3.21B	PSR 4.8-03	PSR	PTM14	Toggle flags parity	
	23		PSR 3.7A	PSR 4.4-06	PSR	PTM15	Toggle PTA parity, byte 4	
	24		PSR 3.28A	PSR 4.9-05	PSR	PTM16	Toggle load history tag mux 2 parity	
	25		PSR 3.11F	PSR 4.4-05	PSR	PTM17	Toggle monitor cond rgtr parity	
	26		PSR 3.18B	PSR 4.6A-04	PSR	PTM18	Enbl VMID to be loaded at MC	
3	27		PSR 3.4B	PSR 4.2A-01	PSR	PTM19	Toggle STL, PYA parity, byte 6	
	28		PMF 3.2E	PSR 4.0-00	PMF	PTM0	Force rgtr 22 PE, byte 0 (bits 0-7)	
	29		PSR 3.30A	PSR 4.3X-09	PSR	PTM23	Enbl retry cond 0	
	30		PSR 3.30A	PSR 4.9-08	PSR	PTM20	Enbl retry test cond - monitor mode	
	31		PSR 3.30A	PSR 4.9-08	PSR	PTM21	Enbl retry test cond - trap enable	

PROC-990, 992, 994, 990E, 995E PTM REGISTER (A3) (Sheet 2 of 2)

Byte	Bit(s)	Due	Level 3 Diagram	Level 4 Diagram	Unit	Signal Name	Description	FRU
	32		PSR 3.30A	PSR 4.9-08	PSR	PTM22	Enbl retry test cond - VMID	
	33		PMF 3.2D	PSR 4.0-00	PMF	PTM1	Force rgtr 22 PE, byte 1	
	34		EPN 3.3A	PSR 4.8-00	EPN	PTM8	Set error flip-flops 1-12	
4	35		EPN 3.3A	PSR 4.8-02	EPN	PTM9	Set error flip-flops 13-26	
	36		EPN 3.4A	PSR 4.5-00	EPN	PTM10	Block initialization of active flags	
	37		EPN 3.7F	PSR 4.5-00	EPN	PTM11	Forces PE on instr comp & delay entry cntr	
	38			PSR 4.11-00	EPN	PTM12	Dsbl EPN interrupt handling	
	39						(Not used)	
	40		PSR 3.30A	PSR 4.5X-09	PSR	PTM24	Enbl retry cond 1 - job mode	
	41		PSR 3.30A	PSR 4.5X-09	PSR	PTM25	Enbl retry cond 1 - monitor mode	
	42						(Not used)	
5	43		BDP 3.6C	BDP 4.1-05	BDP	PTM0	Force Aj stream pause	
	44		BDP 3.8B	BDP 4.1-11	BDP	PTM1	Force Ak stream pause	
	45		BDP 3.1B	BDP 4.3-02	BDP	PTM3	Toggle mark lines parity	
	46		BDP 3.14C	BDP 4.3-03	BDP	PTM6	Toggle LSU load fctn parity	
	47		BDP 3.3B	BDP 4.0-09	BDP	PTM7	Toggle BDP error tag parity	
	48		BDP 3.10A	BDP 4.2-02	BDP	PTM2	Toggle significant byte parity	
	49		BDP 3.1B	BDP 4.0-03	BDP	PTM4	Toggle move bytes mark lines parity	
	50		BDP 3.13E	BDP 4.3-02	BDP	PTM5	Toggle store cont parity	
6	51		BDP 3.15B	BDP 4.4-01	BDP	PTM8	Toggle MAC adrs parity	
	52						(Not used)	
	53		RGU 3.6A	RGU 4.15-02	RGU	PTM0	Force history file X data input mux PE	
	54		RGU 3.6A	RGU 4.15-02	RGU	PTM1	Force history file A data input mux PE	
	55		RGU 3.6A	RGU 4.15-02	RGU	PTM2	Force MAC or IDU enter sel PE	
	56-58						(Not used)	
	59		BP3 3.5F	BP3 4.1-01	BP3	PTM3	Complement A stream digit parity	
	60		BP3 3.8D	BP3 4.2-01	BP3	PTM4	Complement B stream digit parity	
7	61		BP3 3.28D, 14E, 29E	BP3 4.9-06	BP3	PTM5	Force edit mask to all ones	
							(Not used)	
	62		BP3 3.2B	BP3 4.0-00	BP3	PTM6	Force spec error RAM adrs PE	
	63		BP3 3.20B	BP3 4.5-02	BP3	PTM7	Force C stream stage 3 rgtr to zeros	

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MEM-810, 830 OI REGISTER (12)

Byte	Bit(s)	Description
	01	2 Megabyte CM Installed
	02	(Not used)
0	03	4 Megabyte CM Installed
	04 through 06	(Not used)
	07	8 Megabyte CM Installed
	08	(Not used)
	09	12 Megabyte CM Installed
	10	(Not used)
	11	16 Megabyte CM Installed
1	12	32 Megabyte CM Installed
	13	48 Megabyte CM Installed
	14	(Not used)
	15	64 Megabyte CM Installed (uses 256 Kilobit chips)
	16	Any one of the CM Degrade Switches is ON
	17,18	(Not used)
	19	8 or 64 Megabyte Degrade Switch 3 is ON
2	20	4 or 32 Megabyte Degrade Switch 4 is ON
	21	2 or 16 Megabyte Degrade Switch 5 is ON
	22,23	(Not used)
3	24 through 31	(Not used)
4	32 through 39	(Not used)
5	40 through 47	(Not used)
6	48 through 55	(Not used)
7	56 through 63	(Not used)

MEM-810, 830 EC REGISTER (20) (Sheet 1 of 2)

Byte	Bit(s)	Description
0	00	Dsbl Parity Checking
	01	Dsbl SECDED Gen and Checking (use Parity)
	03,04	Test CM word SECDED Code area (8) bits 00 = Normal 01 = Write bits 0,1,4,5,8,9,12,13 to Check Code 10 = Read bits 0,1,4,5,8,9,12,13 from Check Code 11 = Read Syndrome Code to bits 0,1,4,5,8,9,12,13
	05,06	(Not used)
	07	Invert Response Code Parity
1	08	Dsbl CPU 0 Port
	09	Dsbl IOU Port
	10	Dsbl CPU 1 Port
	11 through 15	(Not used)
2	16	IOU Pulse Width Margins + 15%
	17	IOU Pulse Width Margins -15%
	18	CM Pulse Width Margins +15%
	19	CM Pulse Width Margins -15%
	20 through 23	(Not used)
3	24 through 31	(Not used)

MEM-810, 830 EC REGISTER (20) (Sheet 2 of 2)

Byte	Bit(s)	Description
4	32 through 39	(Not used)
5	40 through 47	(Not used)
6	48 through 55	(Put voltage margins on Logic Power Supplies)
7	49 through 63	(Put voltage margins on Logic Power Supplies)

Bit	Effect.....	Bit	Effect.....
48	+5% CPU 1 -2.2 V	56	+5% CPU 0 -5.2 V
49	-5% CPU 1 -2.2 V	57	-5% CPU 0 -5.2 V
50	+5% CPU 0 -2.2 V	58	+5% CM -5.2 V
51	-5% CPU 0 -2.2 V	59	-5% CM -5.2 V
52	+5% CM & IOU -2.2 V	60	+5% IOU -5.2 V
53	-5% CM & IOU -2.2 V	61	-5% IOU 5.2 V
54	+5% CPU 1 -5.2 V	62	+5% CM & IOU +5 V
55	-5% CPU 1 -5.2 V	63	-5% CM & IOU +5 V

MEM-810, 830 B REGISTER (21) (Sheet 1 of 2)

Byte	Bit(s)	Description
0	00	Adrs from CPU 0 Port must be within the bounds
	01	Adrs from IOU Port must be within the bounds
	02	Adrs from CPU 1 Port must be within the bounds
	03 through 07	(Not used)
1	08 through 15	(Not used)
2	16 through 23	(Not used)
3	24 through 31	(Not used)

MEM-810, 830 B REGISTER (21) (Sheet 2 of 2)

Byte	Bit(s)	Description
4	32 through 38	(Not used)

	Central Mem Address Bit(s)	Upper Bounds Address Bit(s)	Lower Bounds Address Bit(s)
	39	35	51
	40	36	52
	41	37	53
	42	38	54
	43	39	55
5	44	40	56
	45	41	57
	46	42	58
	47	43	59
	48	44	60
	49	45	61
	50	46	62
	51	47	63

Byte	Bit(s)	Description
6	52 to 55	All Zeros
7	56 to 63	All Zeros

If the Port Cont bit is set, the CM Adrs sent to the Port must be within the limits (below) or a Bounds Fault will occur.

Upper Bound = 0000 000u uuuu uuuu uuuu 0000 0000 0000

Central Memory Real Adrs † < > or = † Upper Bound Lower Bound

Lower Bound = 0000 000b bbbb bbbb bbbb 0000 0000 0000

Bounds bits shown in Byte Adrs

MEM-810, 830 CEL REGISTER (A0) (Sheet 1 of 2)

Byte	Bit(s)	Description
	00	Valid bit
	01	Unlogged cor error
0	02 through 04	(Not used)
	05	Port code → 00 -
	06	Port code → 01 CP-1
	07	(Not used) → 10 I/O, 11 CP-0
	08	(Not used)
	09	Adrs bit 38
	10	Adrs bit 39
1	11	Adrs bit 40
	12	Adrs bit 41
	13	Adrs bit 42
	14	Adrs bit 43
	15	Adrs bit 44
	16	Adrs bit 45
	17	Adrs bit 46
	18	Adrs bit 47
2	19	Adrs bit 48
	20	Adrs bit 49
	21	Adrs bit 50
	22	Adrs bit 51
	23	Adrs bit 52
	24	Adrs bit 53
	25	Adrs bit 54
	26	Adrs bit 55
3	27	Adrs bit 56
	28	Adrs bit 57
	29	Adrs bit 58
	30	Adrs bit 59
	31	Adrs bit 60

MEM-810, 830 CEL REGISTER (A0) (Sheet 2 of 2)

Byte	Bit(s)	Description
	32	Syndrome bit 0
	33	Syndrome bit 1
	34	Syndrome bit 2
4	35	Syndrome bit 3
	36	Syndrome bit 4
	37	Syndrome bit 5
	38	Syndrome bit 6
	39	Syndrome bit 7
5	40 through 47	(Not used)
6	48 through 55	(Not used)
7	56 through 63	(Not used)

MEM-810, 830 UEL1 REGISTER (A4) (Sheet 1 of 2)

Byte	Bit(s)	Description		
	00	Valid bit		
	01	Unlogged uncor error		
	02	+Illegal fctn		
0	03	+Mem bounds fault		
	04	Partial write error		
	05	Port code	00	-
	06	Port code	01	CP-1
	07	N/A Port Code 00 = Refresh or 2 Pass fault	10	I/O
			11	CP-0
	08	(Not used)		
	09	Adrs bit 38		
	10	Adrs bit 39		
1	11	Adrs bit 40		
	12	Adrs bit 41		
	13	Adrs bit 42		
	14	Adrs bit 43		
	15	Adrs bit 44		
	16	Adrs bit 45		
	17	Adrs bit 46		
	18	Adrs bit 47		
2	19	Adrs bit 48		
	20	Adrs bit 49		
	21	Adrs bit 50		
	22	Adrs bit 51		
	23	Adrs bit 52		
	24	Adrs bit 53		
	25	Adrs bit 54		
	26	Adrs bit 55		
3	27	Adrs bit 56		
	28	Adrs bit 57		
	29	Adrs bit 58		
	30	Adrs bit 59		
	31	Adrs bit 60		

MEM-810, 830 UEL1 REGISTER (A4) (Sheet 2 of 2)

Byte	Bit(s)	Description
	32	Data-in PE, pak DD1
	33	Data-in PE, pak DD2
4	34	Data-in PE, pak DD3
	35	Data-in PE, pak DD4
	36 through 39	(Not used)
	40 through 42	(Not used)
	43	+Tag-in PE
5	44	+Fctn PE
	45	+Mark PE
	46	+Adrs PE 4
	47	+Adrs PE 5
	48	+Adrs PE 6
	49	+Adrs PE 7
6	50 through 53	Fctn code associated with uncor error
	54	Fctn code parity
	55	Mark bits parity
7	56 through 63	Mark bits associated with uncor error

MEM-810, 830 UEL2 REGISTER (A8) (Sheet 1 of 2)

Byte	Bit(s)	Description		
	00	Valid bit		
	01	Unlogged uncor error		
	02	Data-out path PE		
0	03	SECDED double bit error		
	04	+Tag-out PE		
	05	Port code	00	-
	06	Port code	01	CP-1
	07	N/A Port Code 00 = Refresh or 2 Press fault	10	I/O
			11	CP-0
	08	(Not used)		
	09	Adrs bit 38		
	10	Adrs bit 39		
1	11	Adrs bit 40		
	12	Adrs bit 41		
	13	Adrs bit 42		
	14	Adrs bit 43		
	15	Adrs bit 44		
	16	Adrs bit 45		
	17	Adrs bit 46		
	18	Adrs bit 47		
2	19	Adrs bit 48		
	20	Adrs bit 49		
	21	Adrs bit 50		
	22	Adrs bit 51		
	23	Adrs bit 52		
	24	Adrs bit 53		
	25	Adrs bit 54		
	26	Adrs bit 55		
3	27	Adrs bit 56		
	28	Adrs bit 57		
	29	Adrs bit 58		
	30	Adrs bit 59		
	31	Adrs bit 60		

MEM-810, 830 UEL2 REGISTER (A8) (Sheet 2 of 2)

Byte	Bit(s)	Description
	32	+Data-out path PE, byte 0
	33	+Data-out path PE, byte 1
	34	+Data-out path PE, byte 2
4	35	+Data-out path PE, byte 3
	36	+Data-out path PE, byte 4
	37	+Data-out path PE, byte 5
	38	+Data-out path PE, byte 6
	39	+Data-out path PE, byte 7
5	40 through 47	Reserved for ext port bfr error detection
6	48 through 55	Reserved for ext port bfr error detection
7	56 through 63	(Not used)

MEM-815, 825 EC REGISTER (20) (Sheet 1 of 2)

Byte	Bit(s)	Description
	00	Dsbl parity checking (MEM-815, 825)
	01	Dsbl SECDED (MEM-815, 825)
	02	Noninterleaved mode (MEM-815, 825)
0	03 → 04	00 Normal 01 Write byte 0 10 Read byte 0 11 Read syndrome
	05	Micro step (PROC-815, 825)
	06	Enbl PFS trap (PROC-815, 825)
	07	Force even parity
	08	P port (MEM-815, 825)
1	09	I and J ports (MEM-815, 825)
	10	Dsbl M port (MEM-815, 825)
	11 through 15	(Not used)
	16	Pulse width margin, UP pak +15 percent
	17	Pulse width margin, UP pak -15 percent
2	18	Pulse width margin, SA pak +15 percent
	19	Pulse width margin, SA pak -15 percent
	20	Exchange preserve (PROC-815, 825)
	21 through 23	(Not used)
3	24 through 31	(Refer to PROC-810 through 830 DEC rgtr)

MEM-815, 825 EC REGISTER (20) (Sheet 2 of 2)

Byte	Bit(s)	Description
	32 through 37	(Refer to PROC-810 through 830 DEC rgtr)
4	38	Suppress cor error reporting via ports
	39	Dsbl cor error log
5	40 through 47	(Not used)
6	48 through 55	(Not used)
7	56 through 63	(Not used)

MEM-815, 825 CEL REGISTER (A0) (Sheet 1 of 2)

Byte	Bit(s)	Description
	00	Valid bit
	01	Unlogged cor error
0	02 through 04	(Not used)
	05	Port code → 00 J port, 01 M port, 10 I port, 11 C port
	06	Port code → 00 J port, 01 M port, 10 I port, 11 C port
	07	(Not used)
	08	Adrs bit 40
	09	Adrs bit 41
	10	Adrs bit 42
1	11	Adrs bit 43
	12	Adrs bit 44
	13	Adrs bit 45
	14	Adrs bit 46
	15	Adrs bit 47
	16	Adrs bit 48
	17	Adrs bit 49
	18	Adrs bit 50
2	19	Adrs bit 51
	20	Adrs bit 52
	21	Adrs bit 53
	22	Adrs bit 54
	23	Adrs bit 55
	24	Adrs bit 56
	25	Adrs bit 57
	26	Adrs bit 58
3	27	Adrs bit 59
	28	Adrs bit 60
	29	Adrs bit P5
	30	Adrs bit P6
	31	Adrs bit P7

MEM-815, 825 CEL REGISTER (A0) (Sheet 2 of 2)

Byte	Bit(s)	Description
	32	Syndrome bit 0
	33	Syndrome bit 1
	34	Syndrome bit 2
4	35	Syndrome bit 3
	36	Syndrome bit 4
	37	Syndrome bit 5
	38	Syndrome bit 6
	39	Syndrome bit 7
5	40 through 47	(Not used)
6	48 through 55	(Not used)
7	56 through 63	(Not used)

MEM-815, 825 UEL1 REGISTER (A4) (Sheet 1 of 2)

Byte	Bit(s)	Description		
	00	Valid bit		
	01	Unlogged uncor error		
	02	+Illegal fctn		
0	03	+Mem bounds fault		
	04	Partial write error		
	05	Port code →	00	J port
	06	Port code →	01	M port
	07	Refresh port	10	I port
			11	C port-CPU
	08	Adrs bit 40		
	09	Adrs bit 41		
	10	Adrs bit 42		
1	11	Adrs bit 43		
	12	Adrs bit 44		
	13	Adrs bit 45		
	14	Adrs bit 46		
	15	Adrs bit 47		
	16	Adrs bit 48		
	17	Adrs bit 49		
	18	Adrs bit 50		
2	19	Adrs bit 51		
	20	Adrs bit 52		
	21	Adrs bit 53		
	22	Adrs bit 54		
	23	Adrs bit 55		
	24	Adrs bit 56		
	25	Adrs bit 57		
	26	Adrs bit 58		
3	27	Adrs bit 59		
	28	Adrs bit 60		
	29	Adrs bit P5		
	30	Adrs bit P6		
	31	Adrs bit P7		

MEM-815, 825 UEL1 REGISTER (A4) (Sheet 2 of 2)

Byte	Bit(s)	Description
	32	+Write data PE, byte 0
	33	+Write data PE, byte 1
	34	+Write data PE, byte 2
4	35	+Write data PE, byte 3
	36	+Write data PE, byte 4
	37	+Write data PE, byte 5
	38	+Write data PE, byte 6
	39	+Write data PE, byte 7
	40 through 42	(Not used)
	43	+Tag-in PE
5	44	+Fctn PE
	45	+Mark PE
	46	+Adrs PE 4
	47	+Adrs PE 5
	48	+Adrs PE 6
	49	+Adrs PE 7
6	50 through 53	Fctn code associated with uncor error
	54	Fctn code parity
	55	Mark bits parity
7	56 through 63	Mark bits associated with uncor error

MEM-815, 825 UEL2 REGISTER (A8) (Sheet 1 of 2)

Byte	Bit(s)	Description
	00	Valid bit
	01	Unlogged uncor error
	02	Data-out path PE
0	03	SECDED double bit error
	04	+Tag-out PE
	05	Port code
	06	Port code
	07	Refresh port
	08	Adrs bit 40
	09	Adrs bit 41
	10	Adrs bit 42
1	11	Adrs bit 43
	12	Adrs bit 44
	13	Adrs bit 45
	14	Adrs bit 46
	15	Adrs bit 47
	16	Adrs bit 48
	17	Adrs bit 49
	18	Adrs bit 50
2	19	Adrs bit 51
	20	Adrs bit 52
	21	Adrs bit 53
	22	Adrs bit 54
	23	Adrs bit 55
	24	Adrs bit 56
	25	Adrs bit 57
	26	Adrs bit 58
3	27	Adrs bit 59
	28	Adrs bit 60
	29	Adrs bit P5
	30	Adrs bit P6
	31	Adrs bit P7

Port code (bits 05, 06):

00	J port
01	M port
10	I port
11	C port

MEM-815, 825 UEL2 REGISTER (A8) (Sheet 2 of 2)

Byte	Bit(s)	Description
	32	+Data-out path PE, byte 0
	33	+Data-out path PE, byte 1
	34	+Data-out path PE, byte 2
4	35	+Data-out path PE byte 3
	36	+Data-out path PE, byte 4
	37	+Data-out path PE, byte 5
	38	+Data-out path PE, byte 6
	39	+Data-out path PE, byte 7
5	40 through 47	Reserved for ext port bfr error detection
6	48 through 55	Reserved for ext port bfr error detection
7	56 through 63	(Not used)

MEM-810 THROUGH 990, 840S, 845S, 855S, 840A, 850A, 860A, 870A, 992, 994, 990E, 995E OI REGISTER (12) (Sheet 1 of 2)

Byte	Bit(s)	Description	Column A: Bit 12 = 0	Column B: Bit 12 = 1
	00	Memory installed:	1MB	2048 MB
	01	Memory installed:	2MB	1024 MB
	02	Memory installed:	3MB	512 MB
0	03	Memory installed:	4MB	256 MB
	04	Memory installed:	5MB	128 MB
	05	Memory installed:	6MB	64 MB
	06	Memory installed:	7MB	32 MB
	07	Memory installed:	8MB	16 MB
	08	Memory installed:	10MB	8 MB
	09**	Memory installed:	12MB	4 MB
	10**	Memory installed:	14MB	2 MB
1	11**	Memory installed:	16MB	1 MB
	12*	Memory installed cont bit	-	-
	13	Model-dependent options (64K chip for 990E, 995E)		
	14	Model-dependent options (256K chip for 990E, 995E)		
	15**	Model-dependent options		

* If bit 12 = 0, interpret bits 0 through 11 as shown in column A. If bit 12 = 1, interpret bits 0 through 11 as shown in column B.
** Bits 9 through 11 and 15 are not used on 990, 990E, and 995E.

MEM-810 THROUGH 990, 840S, 845S, 855S, 840A, 850A, 860A, 870A, 992, 994, 990E, 995E OI REGISTER (12) (Sheet 2 of 2)

Byte	Bit(s)	Description
	16	Any mem configuration switch up**
	17	Mem configuration switch SW1 (845S through 860A), Not used (990/992), UEM option installed (994, 990E, 995E)
	18	Mem configuration switch SW2**
2	19	Mem configuration switch SW3
	20	Mem configuration switch SW4
	21	Mem configuration switch SW5
	22	Mem configuration switch SW6
	23	(Reserved)*
	24	(Not used)
3	25	Ext port installed (MEM-815, 825 only)
	26 through 31	(Not used)
4	32 through 39	(Not used)
5	40 through 47	(Not used)
6	48 through 55	(Not used)
7	56 through 63	(Not used)

* If bit 23=0, bits 16 through 22 apply to model 30 memory.
If bit 23=1, bits 17 through 22 apply to model 31 memory.
** Column degrade switch on 990E, 995E

Byte(s)	Bit(s)	Description
0	00 through 07	(Not used)
1	08 through 15	(Not used)
2-7	16 through 63	48-bit counter*

* Increments once each microsecond.

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MEM-835, 990 CEL REGISTER (A0 THROUGH A3) (Sheet 1 of 2)

Byte	Bit(s)	Description
	00	Valid bit
0	01	Unlogged cor error
	02 through 07	(Not used)
	08	Port number
	09	Port number
	10	Port number
1	11	Adrs plus parity (835), Adrs parity byte 4 (990)
	12	Adrs plus parity (835), Adrs parity byte 5 (990)
	13	Adrs plus parity (835), Adrs bit 37 (990)
	14	Adrs plus parity (835), Adrs bit 38 (990)
	15	Adrs plus parity (835), Adrs bit 39 (990)
	16	Adrs plus parity (835), Adrs bit 40 (990)
	17	Adrs plus parity (835), Adrs bit 41 (990)
	18	Adrs plus parity (835), Adrs bit 42 (990)
2	19	Adrs plus parity (835), Adrs bit 43 (990)
	20	Adrs plus parity (835), Adrs bit 44 (990)
	21	Adrs plus parity (835), Adrs bit 45 (990)
	22	Adrs plus parity (835), Adrs bit 46 (990)
	23	Adrs plus parity (835), Adrs bit 47 (990)
	24	Adrs plus parity (835), Adrs bit 48 (990)
	25	Adrs plus parity (835), Adrs bit 49 (990)
	26	Adrs plus parity (835), Adrs bit 50 (990)
3	27	Adrs plus parity (835), Adrs bit 51 (990)
	28	Adrs plus parity (835), Adrs bit 52 (990)
	29	Adrs plus parity (835), Adrs bit 53 (990)
	30	Adrs plus parity (835), Adrs bit 54 (990)
	31	Adrs plus parity (835), Adrs bit 55 (990)

0	Port 0
1	Port 1
2	Port 2
3	Port 3
4	(Not used)
5	(Not used)
6	No request
7	Refresh

MEM-835, 990 CEL REGISTER (A0 THROUGH A3) (Sheet 2 of 2)

Byte	Bit(s)	Description
	32	Adrs plus parity (835), Adrs bit 56 (990)
	33	Adrs plus parity (835), Adrs bit 57 (990)
	34	Adrs plus parity (835), Adrs bit 58 (990)
4	35	Adrs plus parity (835), Adrs bit 59 (990)
	36	Adrs plus parity (835), Adrs bit 60 (990)
	37	Adrs plus parity (835), Adrs parity byte 6 (990)
	38	Adrs plus parity (835), Adrs parity byte 7 (990)
	39	(Not used)
	40	(Not used, (835)), Syndrome bit 0 (990)
	41	(Not used, (835)), Syndrome bit 1 (990)
	42	Syndrome bit 0 (835), Syndrome bit 2 (990)
5	43	Syndrome bit 1 (835), Syndrome bit 3 (990)
	44	Syndrome bit 2 (835), Syndrome bit 4 (990)
	45	Syndrome bit 3 (835), Syndrome bit 5 (990)
	46	Syndrome bit 4 (835), Syndrome bit 6 (990)
	47	Syndrome bit 5 (835), Syndrome bit 7 (990)
	48	Syndrome bit 6 (835), not used (990)
6	49	Syndrome bit 7 (835), not used (990)
	50 through 55	(Not used)
7	56 through 63	(Not used)

Register No.	Distributor No.
A0	0
A1	1
A2	2
A3	3

MEM-992, 994, 990E, 995E CEL REGISTER (A0 THROUGH A3) (Sheet 1 of 2)

Byte	Bit(s)	Description	Bits 5 through 7	Port	Port Code
	00	Valid bit	000	0	CP-0 port B
0	01	Unlogged cor error	001	1	CP-0 port A
	02 through 04	(Not used)	010	2	CP-0 port C
	05 through 07	Port number ——→	011	3	Standard port 1
			100	4	CP-1 port B
	08	(Not used)	101	5	CP-1 port A
	09	Adrs parity byte 4	110	6	CP-1 port C
1	10	Adrs Parity byte 5	111	7	Standard port 2
	11	Adrs bit 35			
	12	Adrs bit 36			
	13	Adrs bit 37			
	14	Adrs bit 38			
	15	Adrs bit 39			
	16	Adrs bit 40			
	17	Adrs bit 41			
	18	Adrs bit 42			
2	19	Adrs bit 43			
	20	Adrs bit 44			
	21	Adrs bit 45			
	22	Adrs bit 46			
	23	Adrs bit 47			
	24	Adrs bit 48			
	25	Adrs bit 49			
	26	Adrs bit 50			
3	27	Adrs bit 51			
	28	Adrs bit 52			
	29	Adrs bit 53			
	30	Adrs bit 54			
	31	Adrs bit 55			

MEM-992, 994, 990E, 995E CEL REGISTER (A0 THROUGH A3) (Sheet 2 of 2)

Byte	Bit(s)	Description
	32	Adrs bit 56
	33	Adrs bit 57
	34	Adrs bit 58
4	35	Adrs bit 59
	36	Adrs bit 60
	37	Adrs parity byte 6
	38	Adrs parity byte 7
	39	(Not used)
	40	Syndrome bit 0
	41	Syndrome bit 1
	42	Syndrome bit 2
5	43	Syndrome bit 3
	44	Syndrome bit 4
	45	Syndrome bit 5
	46	Syndrome bit 6
	47	Syndrome bit 7
6	48 through 55	(Not used)
7	56 through 63	(Not used)

Register No.	Distributor No.
A0	0
A1	1
A2	2
A3	3

MEM-835, 840, 845, 850, 855, 860, 990, 840S, 845S, 855S, 840A, 850A, 860A, 870A, 992, 994, 990E, 995E EC REGISTER (20) (Sheet 1 of 2)

Byte	Bit(s)	Description
	00	Dsbl parity checking
	01	Dsbl SECDED
	02	Noninterleaved mode (Not used on 990E, 995E)
	03 04	00 Normal 01 Write byte 0 10 Read byte 0 11 Read syndrome (Check byte/syndrome control)
0		Timing margins (MEM-835 through 860, 840S, 845S, 855S, 840A, 850A, 860A, 870A)
	05	00 Normal 01 Narrow 10 Wide 11 Wide
	06	Force adrs to cor error log (MEM-990, 990E, 995E) Timing margins (MEM-835 through 860, 840S, 845S, 855S, 840A, 850A, 860A, 870A) (refer to bit 05)
	07	Not used (MEM-990, 990E, 995E) Priority port (MEM-835 only)
1	08 through 15	(Not used)

MEM-835, 840, 845, 850, 855, 860, 990, 840S, 845S, 855S, 840A, 850A, 860A, 870A, 992, 994, 990E, 995E EC REGISTER (20) (Sheet 2 of 2)

Byte	Bit(s)	Description
	16	Bit vector for half-speed port 0 (MEM-835 only)
	17	Bit vector for half-speed port 1 (MEM-835 only)
2	18	Bit vector for half-speed port 2 (MEM-835 only)
	19	Bit vector for half-speed port 3 (MEM-835 only)
	20 through 23	(Not used)
3	24 through 31	(Not used)
	32	Bit vector for port 0 dsbl (MEM-835, 990, 990E, 995E), port dsbl on CP-0 (MEM-840 through 860, 840S, 845S, 855S, 840A, 850A, 860A, 870A)
	33	Bit vector for port 1 dsbl (MEM-835, 990, 990E, 995E), port dsbl on CP-1 (MEM-855, 860, 860A, 870A)
	34	Bit vector for port 2 dsbl (MEM-835, 990, 990E, 995E), standard port dsbl (STDP) (MEM-840 through 860, 840S, 845S, 855S, 840A, 850A, 860A, 870A)
4	35	Bit vector for port 3 dsbl (MEM-835, 990, 990E, 995E), port dsbl on IOU (MEM-840 through 860, 840S, 845S, 855S, 840A, 850A, 860A, 870A)
	36	(Not used)
	37	Dsbl refresh (MEM-840 through 860, 840S, 845S, 855S, 840A, 850A, 860A, 870A only)
	38	Suppress cor error reporting to ports
	39	Dsbl cor error log
5	40 through 47	(Not used)
6	48 through 55	(Not used)
7	56 through 63	(Not used)

MEM-835, 840, 845, 850, 855, 860, 840S, 845S, 855S, 840A, 850A, 860A, 870A UEL1 REGISTER (A4) (Sheet 1 of 4)

Byte	Bit(s)	Description
	00	Valid bit
	01	Unlogged uncor error
	02	Illegal fctn (MEM-835, 845, 855), multiple-bit mem error (MEM-840, 850, 860, 840S, 845S, 855S, 840A, 850A, 860A, 870A)
	03	Multiple-bit error (MEM-835, 845, 855), CMC PE (MEM-840, 850, 860, 840S, 845S, 855S, 840A, 850A, 860A, 870A)
0	04	Mem bounds fault (MEM-835, 845, 855), CSU PE (MEM-840, 850, 860, 840S, 845S, 855S, 840A, 850A, 860A, 870A)
	05	lst level PE (MEM-835), CMC PE (MEM-845, 855), port number (MEM-840, 850, 860, 840S, 845S, 855S, 840A, 850A, 860A, 870A) (same as CEL and UEL2)
	06	2nd level PE (MEM-835), CSU PE (MEM-845, 855), port number (MEM-840, 850, 860, 840S, 845S, 855S, 840A, 850A, 860A, 870A) (same as CEL and UEL2)
	07	Common mem request from port bfr (MEM-835), common mem adrs bit 01 (MEM-845, 855), port number (MEM-840, 850, 860, 840S, 845S, 855S, 840A, 850A, 860A, 870A) (same as CEL and UEL2)
	08 through 10	Port number (MEM-835, 845, 855) (same as CEL and UEL2), adrs plus parity (MEM-840, 850, 860, 840S, 845S, 855S, 840A, 850A, 860A, 870A)
1	11,12	Adrs plus parity, (not used)
	13,14	Adrs plus parity, array pak sel
	15	Adrs plus parity, chip row sel

NOTE

CYBER 170/180 models 845/855 normally have a model 30 memory. The models 845/855 with memory upgrade have a model 31 memory. For models 845/855 with the model 31 memory, use the models 840, 850, 860, 840S, 845S, 855S, 840A, 850A, 860A, 870A bit configuration.

MEM-835, 840, 845, 850, 855, 860, 840S, 845S, 855S, 840A, 850A, 860A, 870A UEL1 REGISTER (A4) (Sheet 2 of 4)

Byte	Bit(s)	Description
2	16	Adrs plus parity, chip row sel
	17 through 23	Adrs plus parity, chip column adrs
	24 through 28	Adrs plus parity, chip row adrs
3	29	Adrs plus parity, chip row adrs
	30	Adrs bit 57, chip row adrs
	31	Adrs bit 58, bank
	32	Adrs bit 59, bank
	33	Adrs bit 60, bank
4	34	Adrs parity, parity 4
	35	Adrs parity, parity 5
	36	Adrs parity, parity 6
	37	Adrs parity, parity 7

NOTE

CYBER 170/180 models 845/855 normally have a model 30 memory. The models 845/855 with memory upgrade have a model 31 memory. For models 845/855 with the model 31 memory, use the models 840, 850, 860, 840S, 845S, 855S, 840A, 850A, 860A, 870A bit configuration.

MEM-835, 840, 845, 850, 855, 860, 840S, 845S, 855S, 840A, 850A, 860A, 870A UEL1 REGISTER (A4) (Sheet 3 of 4)

Byte	Bit(s)	Description
	38	PE byte position*
	39	PE byte position*
	40	PE byte position*
5	41	PE byte position*
	42 through 47	Data-in PE bits

* Bits 38 - 41

	MEM-835	MEM 840-860, 840S, 845S, 855S, 840A, 850A, 860A, 870A
1111	No error	Tag PE
1110	Fctn code PE	Write data byte 7 PE
1101	Mark PE	(Not used)
1100	(Not used)	(Not used)
1011	Adrs byte 5 PE	(Not used)
1010	Adrs byte 6 PE	(Not used)
1001	Adrs byte 7 PE	(Not used)
1000	Data byte 0 PE	(Not used)
0111	Data byte 1 PE	Adrs byte 3 PE
0110	Data byte 2 PE	Adrs byte 2 PE
0101	Data byte 3 PE	Adrs byte 1 PE
0100	Data byte 4 PE	Adrs byte 0 PE
0011	Data byte 5 PE	(Not used)
0010	Data byte 6 PE	Mark PE
0001	Data byte 7 PE	Fctn code PE
0000	Tag PE	No error

MEM-835, 840, 845, 850, 855, 860, 840S, 845S, 855S, 840A, 850A, 860A, 870A UEL1 REGISTER (A4) (Sheet 4 of 4)

Byte	Bit(s)	Description
	48,49	Data-in PE bits
6	50 through 55	Mark bits
	56,57	Mark bits
7	58	Mark parity bit
	59 through 62	Fctn bits
	63	Fctn parity bit

MEM-835, 840, 845, 850, 855, 860, 840S, 845S, 855S, 840A, 850A, 860A, 870A UEL2 REGISTER (A8) (Sheet 1 of 2)

Byte	Bit(s)	Description		
	00	Valid bit		
	01	Unlogged uncor error		
	02	Partial-write PE (MEM-835, 845, 855), illegal fctn (MEM-840, 850, 860, 840S, 845S, 855S, 840A, 850A, 860A, 870A)		
	03	Data-out path PE (MEM-835, 840, 845, 855), bounds fault (MEM-840, 850, 860, 840S, 845S, 855S, 840A, 850A, 860A, 870A)		
0	04	(Not used)	0	Port 0
	05	Not used (MEM-835, 845, 855), port number (MEM-840, 850, 860)	1	Port 1
	06	Not used (MEM-835, 845, 855), port number (MEM-840, 850, 860)	2	Port 2
	07	Not used (MEM-835, 845, 855), port number (MEM-840, 850, 860, 840S, 845S, 855S, 840A, 850A, 860A, 870A)	3	Port 3
			4	(Not used)
	08	Not used (MEM-840, 850, 860), port number (MEM-835, 845, 855)	5	(Not used)
	09	Not used (MEM-840, 850, 860), port number (MEM-835, 845, 855)	6	No request
1	10	Not used (MEM-840, 850, 860), port number (MEM-835, 845, 855)	7	Refresh
	11,12	Adrs plus parity, (not used)		
	13,14	Adrs plus parity, array pak sel		
	15	Adrs plus parity, chip row sel		
	16	Adrs plus parity, chip row sel		

NOTE

CYBER 170/180 models 845/855 normally have a model 30 memory. The models 845/855 with memory upgrade have a model 31 memory. For models 845/855 with the model 31 memory, use the models 840, 850, 860, 840S, 845S, 855S, 840A, 850A, 860A, 870A bit configuration.

MEM-835, 840, 845, 850, 855, 860, 840S, 845S, 855S, 840A, 850A, 860A, 870A UEL2 REGISTER (A8) (Sheet 2 of 2)

Byte	Bit(s)	Description
	32,33	Adrs plus parity, bank
	34	Adrs plus parity, (not used)
	35	Adrs plus parity, parity 5
4	36	Adrs plus parity, parity 6
	37	Adrs plus parity, parity 7
	38	Data-out path PE, byte 0
	39	Data-out path PE, byte 1
	40	Data-out path PE, byte 2
	41	Data-out path PE, byte 3
	42	Data-out path PE, byte 4
5	43	Data-out path PE, byte 5
	44	Data-out path PE, byte 6
	45	Data-out path PE, byte 7
	46	Partial-write PE, byte 0
	47	Partial-write PE, byte 1
	48	Partial-write PE, byte 2
	49	Partial-write PE, byte 3
	50	Data-out path PE, byte 4
6	51	Partial-write PE, byte 5
	52	Partial-write PE, byte 6
	53	Partial-write PE, byte 7
	54	Tag PE (MEM-835 only)
	55	(Not used)
7	56 through 63	(Not used)

MEM-840, 845, 850, 855, 860, 840S, 845S, 855S, 840A, 850A, 860A, 870A CEL REGISTER (A0) (Sheet 1 of 2)

Byte	Bit(s)	Description
	00	Valid bit
	01	Unlogged cor error
0	02 through 04	(Not used)
	05 through 07	Not used (MEM-845, 855), port number (MEM-840, 850, 860, 840S, 845S, 855S, 840A, 850A, 860A, 870A) (refer to detail)
	08 through 10	Port number (MEM-845, 855) (refer to detail), adrs plus parity (MEM-840, 850, 860, 840S, 845S, 855S, 840A, 850A, 860A, 870A)
1	11,12	Adrs plus parity, (not used)
	13,14	Adrs plus parity, array pak sel
	15	Adrs plus parity, chip row sel
2	16	Adrs plus parity, chip row sel
	17 through 23	Adrs plus parity, chip column adrs
	24 through 29	Adrs plus parity, chip row adrs
3	30	Adrs bit 57, chip row adrs
	31	Adrs bit 58, bank

Bits 05 through 07 (Models 840, 850, and 860; CYBER 840S, 845S, 855S, 840A, 850A, 860A, 870A); Bits 08 through 10 (Models 845 and 855)

Port
0 CP-0
1 IOU
2 CP-1
3 Standard port
4 (Not used)
5 (Not used)

NOTE

CYBER 170/180 models 845/855 normally have a model 30 memory. The models 845/855 with the memory upgrade have a model 31 memory. For models 845/855 with the model 31 memory, use the 840, 850, 860, 840S, 845S, 855S, 840A, 850A, 860A, 870A bit configuration.

MEM-840, 845, 850, 855, 860, 840S, 845S, 855S, 840A, 850A, 860A, 870A CEL REGISTER (A0) (Sheet 2 of 2)

Byte	Bit(s)	Description
	32	Adrs bit 59, bank
	33	Adrs bit 60, bank
	34	Adrs parity, parity 4
4	35	Adrs parity, parity 5
	36	Adrs parity, parity 6
	37	Adrs parity, parity 7
	38,39	(Not used)
	40,41	(Not used)
	42	Syndrome bit 0
	43	Syndrome bit 1
5	44	Syndrome bit 2
	45	Syndrome bit 3
	46	Syndrome bit 4
	47	Syndrome bit 5
	48	Syndrome bit 6
6	49	Syndrome bit 7
	50 through 55	(Not used)
7	56 through 63	(Not used)

MEM-990 UEL1 REGISTER (A4 THROUGH A7) (Sheet 1 of 2)

Byte	Bit(s)	Description
	00	Valid bit
	01	Unlogged uncor error
	02	Illegal fctn
0	03	Multiple-bit mem error
	04	Mem bounds fault
	05	Port Adrs PE
	06	CSU PE
	07	Adrs bit 33
	08 through 10	Port number
	11	Adrs parity, byte 4
1	12	Adrs parity, byte 5
	13	Adrs bit 37
	14	Adrs bit 38
	15	Adrs bit 39
	16	Adrs bit 40
	17	Adrs bit 41
	18	Adrs bit 42
2	19	Adrs bit 43
	20	Adrs bit 44
	21	Adrs bit 45
	22	Adrs bit 46
	23	Adrs bit 47
	24	Adrs bit 48
	25	Adrs bit 49
	26	Adrs bit 50
3	27	Adrs bit 51
	28	Adrs bit 52
	29	Adrs bit 53
	30	Adrs bit 54
	31	Adrs bit 55

Bits 8 through 10	Port	Port Code
000	0	CP-0 port B
001	1	CP-0 port A
010	2	CP-0 port C
011	3	Standard port 1
100	4	CP-1 port B
101	5	CP-1 port A
110	6	CP-1 port C
111	7	Standard port 2

MEM-990 UEL1 REGISTER (A4 THROUGH A7) (Sheet 2 of 2)

Byte	Bit(s)	Description
	32	Adrs bit 56
	33	Adrs bit 57
	34	Adrs bit 58
4	35	Adrs bit 59
	36	Adrs bit 60
	37	Adrs byte 6
	38	Adrs byte 7
	39	(Not used)
	40	Write data PE, byte 0
	41	Write data PE, byte 1
	42	Write data PE, byte 2
5	43	Write data PE byte 3
	44	Write data PE, byte 4
	45	Write data PE, byte 5
	46	Write data PE, byte 6
	47	Write data PE, byte 7
	48	Read or partial-write data PE, byte 0
	49	Read or partial-write data PE, byte 1
	50	Read or partial-write data PE, byte 2
6	51	Read or partial-write data PE, byte 3
	52	Read or partial-write data PE, byte 4
	53	Read or partial-write data PE, byte 5
	54	Read or partial-write data PE, byte 6
	55	Read or partial-write data PE, byte 7
	56	Adrs PE, byte 4
	57	Adrs PE, byte 5
	58	Adrs PE, byte 6
7	59	Adrs PE, byte 7
	60	Mark PE
	61	Tag PE
	62	Fctn PE
	63	Partial-write PE

Register No.	Distributor No.
A4	0
A5	1
A6	2
A7	3

MEM-990E, 995E UEL1 REGISTER (A4 THROUGH A7) (Sheet 1 of 2)

Byte	Bit(s)	Description
	00	Valid bit
	01	Unlogged uncor error
	02	Illegal fctn
0	03	Multiple-bit mem error
	04	Mem bounds fault
	05 through 07	Port number
	08	CSU PE
	09	Adrs parity, byte 4
1	10	Adrs parity, byte 5
	11	Adrs bit 35
	12	Adrs bit 36
	13	Adrs bit 37
	14	Adrs bit 38
	15	Adrs bit 39
	16	Adrs bit 40
	17	Adrs bit 41
	18	Adrs bit 42
2	19	Adrs bit 43
	20	Adrs bit 44
	21	Adrs bit 45
	22	Adrs bit 46
	23	Adrs bit 47
	24	Adrs bit 48
	25	Adrs bit 49
	26	Adrs bit 50
3	27	Adrs bit 51
	28	Adrs bit 52
	29	Adrs bit 53
	30	Adrs bit 54
	31	Adrs bit 55

Bits 5 through 7	Port	Port Code
000	0	CP-0 port B
001	1	CP-0 port A
010	2	CP-0 port C
011	3	Standard port 1
100	4	CP-1 port B
101	5	CP-1 port A
110	6	CP-1 port C
111	7	Standard port 2

MEM-990E, 995E UEL1 REGISTER (A4 THROUGH A7) (Sheet 2 of 2)

Byte	Bit(s)	Description
	32	Adrs bit 56
	33	Adrs bit 57
	34	Adrs bit 58
4	35	Adrs bit 59
	36	Adrs bit 60
	37	Adrs parity, byte 6
	38	Adrs parity, byte 7
	39	Port adrs PE
	40	Write data PE, byte 0
	41	Write data PE, byte 1
	42	Write data PE, byte 2
5	43	Write data PE, byte 3
	44	Write data PE, byte 4
	45	Write data PE, byte 5
	46	Write data PE, byte 6
	47	Write data PE, byte 7
	48	Read or partial-write data PE, byte 0
	49	Read or partial-write data PE, byte 1
	50	Read or partial-write data PE, byte 2
6	51	Read or partial-write data PE, byte 3
	52	Read or partial-write data PE, byte 4
	53	Read or partial-write data PE, byte 5
	54	Read or partial-write data PE, byte 6
	55	Read or partial-write data PE, byte 7
	56	Adrs PE, byte 4
	57	Adrs PE, byte 5
	58	Adrs PE, byte 6
7	59	Adrs PE, byte 7
	60	Mark PE
	61	Tag PE
	62	Pctn PE
	63	Partial-write PE

Register No.	Distributor No.
A4	0
A5	1
A6	2
A7	3

IOU-810 THROUGH 830 TM REGISTER (A0) (Sheet 1 of 2)

Byte	Bit(s)	Description
0	00 through 07	(Not used)
1	08 through 15	(Not used)
2	16 through 23	(Not used)
3	24 through 31	(Not used)
4	32 through 39	(Not used)
5	40 through 47	(Not used)
6	48 through 50	(Not used)
	51	Logical barrel and bits (IOU-810 through 830)
	52 through 55	Logical PP, 00 through 11 (IOU-810 through 830)

IOU-810 THROUGH 830 TM REGISTER (A0) (Sheet 2 of 2)

Byte	Bit(s)	Description
	56 through 58	(Not applicable)
	59	Test code (IOU-810, 830) (not available) Not used (IOU-815, 825)
	60	Test code (IOU-810, 830) (not available) Test code (IOU-815, 825) (refer to detail)
7	61	Test code (IOU-810, 830) (not available) Test code (IOU-815, 825) (refer to detail)
	62	Test code (IOU-810, 830) (not available) Test code (IOU-815, 825) (refer to detail)
	63	Test code (IOU-810, 830) (not available) Test code (IOU-815, 825) (refer to detail)

Detail, bits 60 through 63
IOU-815, 825: invert parity

0	(Not used)
1	Invert Y rgtr parity
2	Invert PP to chan parity
3	Invert A rgtr parity at output of A adder and shifter
4	Force error at firmware parity checker
5	Force error at A shifter cont ROM parity checker
6	Invert CM fctn code parity
7	Force zero CM adrs-in parity (4 bits)
8	Force error at bounds rgtr parity checker
9	Invert Q rgtr parity at output of Q mux
A	Invert CM tag-in parity
B	Force zero CM data-in parity (8 bits)
C	Invert data-out parity (bytes 0 through 7)
D-F	(Not used)

IOU-810 THROUGH 860 OI REGISTER (12) (Sheet 1 of 2)

Byte	Bit(s)	Description
0	00 through 07	(Not used)
1	08 through 15	(Not used)
	16 through 19	(Not used)
	20	Barrel 3, PP25 through 31
2	21	Barrel 2, PP20 through 24
	22	Barrel 1, PP5 through 11
	23	Barrel 0, PP0 through 4
	24	Channel 7
	25	Channel 6
	26	Channel 5
3	27	Channel 4
	28	Channel 3
	29	Channel 2
	30	Channel 1
	31	Channel 0

IOU-810 THROUGH 860 OI REGISTER (12) (Sheet 2 of 2)

Byte	Bit(s)	Description
	32	Channel 17
	33	(Not used)
	34	Channel 15
4	35	(Not used)
	36	Channel 13
	37	Channel 12
	38	Channel 11
	39	Channel 10
	40	Channel 27
	41	Channel 26
	42	Channel 25
5	43	Channel 24
	44	Channel 23
	45	Channel 22
	46	Channel 21
	47	Channel 20
	48 through 51	(Not used)
	52	Channel 33
6	53	Channel 32
	54	Channel 31
	55	Channel 30
	56 through 58	(Not used)
	59	Radial interface 5, 6 (835 through 860), not used (810 through 830)
7	60	Radial interface 2, 3 (810 through 830), radial interface 3,4 (835 through 860)
	61	Radial interface 0, 1 (810 through 830), radial interface 1,2 (835 through 860)
	62	Two-port mux
	63	CC545 controller

IOU-810 THROUGH 860 FSM (18) (Sheet 1 of 3)

Byte	Bit(s)	Description
	00 through 02	(Not used)
	03	Mask vector, barrel 0 PP4 (IOU-810 through 860)
0	04	Mask vector, barrel 0 PP3 (IOU-810 through 860)
	05	Mask vector, barrel 0 PP2 (IOU-810 through 860)
	06	Mask vector, barrel 0 PP1 (IOU-810 through 860)
	07	Mask vector, barrel 0 PP0 (IOU-810 through 860)
	08 through 10	(Not used)
	11	Mask vector, barrel 0 PP11 (IOU-810 through 830), B1 PP4 (IOU-835 through 860)
1	12	Mask vector, barrel 0 PP10 (IOU-810 through 830), B1 PP3 (IOU-835 through 860)
	13	Mask vector, barrel 0 PP7 (IOU-810 through 830), B1 PP2 (IOU-835 through 860)
	14	Mask vector, barrel 0 PP6 (IOU-810 through 830), B1 PP1 (IOU-835 through 860)
	15	Mask vector, barrel 0 PP5 (IOU-810 through 830), B1 PP0 (IOU-835 through 860)
	16 through 18	(Not used)
	19	Mask vector, barrel 1 PP4 (IOU-810 through 830), B2 PP4 (IOU-835 through 860)
2	20	Mask vector, barrel 1 PP3 (IOU-810 through 830), B2 PP3 (IOU-835 through 860)
	21	Mask vector, barrel 1 PP2 (IOU-810 through 830), B2 PP2 (IOU-835 through 860)
	22	Mask vector, barrel 1 PP1 (IOU-810 through 830), B2 PP1 (IOU-835 through 860)
	23	Mask vector, barrel 1 PP0 (IOU-810 through 830), B2 PP0 (IOU-835 through 860)
	24 through 26	(Not used)
	27	Mask vector, barrel 1 PP11 (IOU-810 through 830), B3 PP4 (IOU-835 through 860)
	28	Mask vector, barrel 1 PP10 (IOU-810 through 830), B3 PP3 (IOU-835 through 860)
	29	Mask vector, barrel 1 PP7 (IOU-810 through 830), B3 PP2 (IOU-835 through 860)
	30	Mask vector, barrel 1 PP6 (IOU-810 through 830), B3 PP1 (IOU-835 through 860)
	31	Mask vector, barrel 1 PP5 (IOU-810 through 830), B3 PP0 (IOU-835 through 860)

IOU-810 THROUGH 860 FSM (18) (Sheet 2 of 3)

Byte	Bit(s)	Description
	32	Mask vector, channel 7
	33	Mask vector, channel 6
	34	Mask vector, channel 5
4	35	Mask vector, channel 4
	36	Mask vector, channel 3
	37	Mask vector, channel 2
	38	Mask vector, channel 1
	39	Mask vector, channel 0
	40	Mask vector, channel 17
	41	(Not used)
	42	Mask vector, channel 15
5	43	(Not used)
	44	Mask vector, channel 13
	45	Mask vector, channel 12
	46	Mask vector, channel 11
	47	Mask vector, channel 10

IOU-810 THROUGH 860 FSM (18) (Sheet 3 of 3)

Byte	Bit(s)	Description
	48	Mask vector, channel 27
	49	Mask vector, channel 26
	50	Mask vector, channel 25
6	51	Mask vector, channel 24
	52	Mask vector, channel 23
	53	Mask vector, channel 22
	54	Mask vector, channel 21
	55	Mask vector, channel 20
	56	(Not used)
	57	Mask vector, radial interface 5/6 (IOU-835 through 860) not used (IOU-810 through 830)
	58	Mask vector, radial interface 3/4 (IOU-835 through 860), not used (IOU-810 through 830)
7	59	Mask vector, radial interface 2/3 (IOU-810 through 830), 1/2 (IOU-835 through 860)
	60	Mask vector, channel 33
	61	Mask vector, channel 32
	62	Mask vector, channel 31
	63	Mask vector, channel 30

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IOU-810 THROUGH 860 OSB REGISTER (21) (Sheet 1 of 2)

Byte	Bit(s)	Description
	00 through 02	(Not used)
	03	Bit vector, B0 PP4 (IOU-810 through 860)
0	04	Bit vector, B0 PP3 (IOU-810 through 860)
	05	Bit vector, B0 PP2 (IOU-810 through 860)
	06	Bit vector, B0 PP1 (IOU-810 through 860)
	07	Bit vector, B0 PP0 (IOU-810 through 860)
	08 through 10	(Not used)
	11	Bit vector, B0 PP11 (IOU-810 through 830), B1 PP4 (IOU-835 through 860)
1	12	Bit vector, B0 PP10 (IOU-810 through 830), B1 PP3 (IOU-835 through 860)
	13	Bit vector, B0 PP7 (IOU-810 through 830), B1 PP2 (IOU-835 through 860)
	14	Bit vector, B0 PP6 (IOU-810 through 830), B1 PP1 (IOU-835 through 860)
	15	Bit vector, B0 PP5 (IOU-810 through 830), B1 PP0 (IOU-835 through 860)
	16 through 18	(Not used)
	19	Bit vector, B1 PP4 (IOU-810 through 830), B2 PP4 (IOU-835 through 860)
2	20	Bit vector, B1 PP3 (IOU-810 through 830), B2 PP3 (IOU-835 through 860)
	21	Bit vector, B1 PP2 (IOU-810 through 830), B2 PP2 (IOU-835 through 860)
	22	Bit vector, B1 PP1 (IOU-810 through 830), B2 PP1 (IOU-835 through 860)
	23	Bit vector, B1 PP0 (IOU-810 through 830), B2 PP0 (IOU-835 through 860)
	24 through 26	(Not used)
	27	Bit vector, B1 PP11 (IOU-810 through 830), B3 PP4 (IOU-835 through 860)
3	28	Bit vector, B1 PP10 (IOU-810 through 830), B3 PP3 (IOU-835 through 860)
	29	Bit vector, B1 PP7 (IOU-810 through 830), B3 PP2 (IOU-835 through 860)
	30	Bit vector, B1 PP6 (IOU-810 through 830), B3 PP1 (IOU-835 through 860)
	31	Bit vector, B1 PP5 (IOU-810 through 830), B3 PP0 (IOU-835 through 860)

IOU-810 THROUGH 860 OSB REGISTER (21) (Sheet 2 of 2)

Byte	Bit(s)	Description
4	32 through 39	(Not used)
	40 through 45	(Not used)
5	46	OS boundary adrs (36)
	47	OS boundary adrs (37)
6	48 through 55	OS boundary adrs (38 through 45)
7	56 through 63	OS boundary adrs (46 through 53)

IOU-810 THROUGH 860 EC REGISTER (30)

Byte	Bit(s)	Description
0	00 through 07	(Not used)
1	08 through 15	(Not used)
2	16 through 23	(Not used)
3	24 through 31	(Not used)
	32,33	(Not used)
4	34	Auto mode (IOU-835 through 860)
	35 through 39	PP number
5	40 through 42	(Not used)
	43 through 47	Chan number
	48 through 50	(Not used)
	51	Load mode
6	52	Dump mode
	53	Idle mode
	54	Rgtr sel } A, P, Q, K
	55	Rgtr sel }
	56	Pulse width margin, wide } (IOU-835 through 860 only)
	57	Pulse width margin, narrow }
	58	Enbl deadstart/dump/idle
7	59	Enbl test mode
	60	Enbl OS bounds checking
	61	Enbl (R) + (A) to PP mem
	62	(Not used)
	63	Enbl error stop

IOU-810 THROUGH 860 S REGISTER (40)

Byte	Bit(s)	Description
0	00 through 07	(Not used)
1	08 through 15	(Not used)
2	16 through 23	(Not used)
3	24 through 30	(Not used)
	31	Battery on line (IOU-810 and 830)
4	32 through 37	(Not used)
	38, 39	Int rgtr (A, P, Q, K)
5	40 through 47	Int rgtr (A, P, Q, K)
6	48 through 55	Int rgtr (A, P, Q, K)
	56	LDS bit
	57	Timing margin - fast (IOU-835 through 860)
	58	Timing margin - slow (IOU-835 through 860)
7	59	Barrel reconfiguration (IOU-810 through 860)
	60	PP reconfiguration (IOU-810 through 830), barrel reconfiguration (IOU-835 through 860)
	61 through 63	PP reconfiguration (IOU-810 through 860)

IOU-810 THROUGH 860 FS1 REGISTER (80) (Sheet 1 of 4)

Byte	Bit(s)	Description
	00 through 02	(Not used)
	03	Error, B0 PP4 (IOU-810 through 860)
0	04	Error, B0 PP3 (IOU-810 through 860)
	05	Error, B0 PP2 (IOU-810 through 860)
	06	Error, B0 PP1 (IOU-810 through 860)
	07	Error, B0 PP0 (IOU-810 through 860)
	08 through 10	(Not used)
	11	Error, B0 PP11 (IOU-810 through 830), B1 PP4 (IOU-835 through 860)
1	12	Error, B0 PP10 (IOU-810 through 830), B1 PP3 (IOU-835 through 860)
	13	Error, B0 PP7 (IOU-810 through 830), B1 PP2 (IOU-835 through 860)
	14	Error, B0 PP6 (IOU-810 through 830), B1 PP1 (IOU-835 through 860)
	15	Error, B0 PP5 (IOU-810 through 830), B1 PP0 (IOU-835 through 860)
	16 through 18	(Not used)
	19	Error, B1 PP4 (IOU-810 through 830), B2 PP4 (IOU-835 through 860)
2	20	Error, B1 PP3 (IOU-810 through 830), B2 PP3 (IOU-835 through 860)
	21	Error, B1 PP2 (IOU-810 through 830), B2 PP2 (IOU-835 through 860)
	22	Error, B1 PP1 (IOU-810 through 830), B2 PP1 (IOU-835 through 860)
	23	Error, B1 PP0 (IOU-810 through 830), B2 PP0 (IOU-835 through 860)
	24 through 26	(Not used)
	27	Error, B1 PP11 (IOU-810 through 830), B3 PP4 (IOU-835 through 860)
3	28	Error, B1 PP10 (IOU-810 through 830), B3 PP3 (IOU-835 through 860)
	29	Error, B1 PP7 (IOU-810 through 830), B3 PP2 (IOU-835 through 860)
	30	Error, B1 PP6 (IOU-810 through 830), B3 PP1 (IOU-835 through 860)
	31	Error, B1 PP5 (IOU-810 through 830), B3 PP0 (IOU-835 through 860)

IOU-810 THROUGH 860 FS1 REGISTER (80) (Sheet 2 of 4)

Byte	Bit(s)	Description
	32	Error on YJ (IOU-815, 825), on CL pak OS bounds rgtr or CM adrs (IOU-810, 830), on 7VDO (IOU-835 through 860)
	33	Error on YG (IOU-815, 825), on CR pak A, R, Q, or P barrel or G mux or shift cont ROM (IOU-810, 830), on 7VEO (IOU-835 through 860)
	34	Firmware error (on CP pak for IOU-810, 830), microcode or code adrs
	35	PP mem data-out error on YM (IOU-815, 825, 835 through 860), PP mem data in or out error on CM pak (IOU-810, 830)
4	36	PPM error on YP (IOU-815, 825), on CP pak chan data or bit 34 (IOU-810, 830), on 7VGO (IOU-835 through 860)
	37	Error on YH (IOU-815, 825), data conversion error on CP pak (IOU-810, 830), on 7VJO (IOU-835 through 860)
	38	PP mem adrs error (IOU-815, 825, 835 through 860), not used (IOU-810 and 830)
	39	PP mem data-in error (on CM pak for IOU-810, 830)
	40 through 44	(Not used)
5	45	Error on CL pak, OS bounds violation (IOU-810, 830)
	46	Error on CL pak, OS bounds adrs (IOU-810, 830)
	47	ADU barrel priority, ROM PE (IOU-835 through 860), not used (IOU-810 through 830)

IOU-810 THROUGH 860 FS1 REGISTER (80) (Sheet 3 of 4)

Byte	Bit(s)	Description
	48	CM data-out error on DD paks, (IOU-810, 830) CM read-bfr error (IOU-835 through 860), not used (IOU-815, 825)
	49	Uncorrected CM read error
	50	Uncorrected CM write error
	51	CM reject
6	52	Input CM tag error (IOU-835 through 860), CM tag-out error (IOU-810 through 830)
	53	CM response code error
	54	CM data-in error (IOU-815, 825), CM data-out error (IOU-835 through 860), not used (IOU-810 and 830)
	55	CM adrs-out and/or funct. code-out error (IOU-835 through 860), not used (IOU-810 through 830)
	56	CM data-out error (IOU-815, 825), data-in error (IOU-835 through 860), not used (IOU-810 and 830), byte 0
	57	CM data-out error (IOU-815, 825), data-in error (IOU-835 through 860), not used (IOU-810 and 830), byte 1
	58	CM data-out error (IOU-815, 825), data-in error (IOU-835 through 860), not used (IOU-810 and 830), byte 2
	59	CM data-out error (IOU-815, 825), data-in error (IOU-835 through 860), not used (IOU-810 and 830), byte 3
7	60	CM data-out error (IOU-815, 825), data-in error (IOU-835 through 860), not used (IOU-810 and 830), byte 4
	61	CM data-out error (IOU-815, 825), data-in error (IOU-835 through 860), not used (IOU-810 and 830), byte 5
	62	CM data-out error (IOU-815, 825), data-in error (IOU-835 through 860), not used (IOU-810 and 830), byte 6
	63	CM data-out error (IOU-815, 825), data-in error (IOU-835 through 860), not used (IOU-810 and 830), byte 7

IOU-810 THROUGH 860 FS1 REGISTER (80) (Sheet 4 of 4)

Notes on Error Analysis (IOU-810 and 830):

35, 39 = PP Mem Data In

35, $\overline{39}$ = PP Mem Data Out

34, 36 = Microcode PE

36, $\overline{34}$ = Chan data PE, CP or any chan (CJ,CH,CQ) pak

Rgtr Analysis Examples (IOU-810 and 830):

80 = 00 00 10 00 00 00 04 00. CM Response code PE - PP 24 failed - DC pak in CM, CN pak in IOU.

80 = 00 02 00 00 11 00 00 00. PP Mem data in PE - PP 6 failed - CM, CP or CR in Barrel 0 or DD in CM.

80 = 10 00 00 00 41 00 00 00. PP Mem data out PE - PP 4 failed = PP mem bank 2. CM pak in Barrel 0.

80 = 1F 1F 1F 1F 80 00 00 00. OS bounds rgtr or CM Adrs PE - CL pak.

IOU-810 THROUGH 860 FS2 REGISTER (81) (Sheet 1 of 2)

Byte	Bit(s)	Description
0	00 through 07	(Not used)
1	08 through 15	(Not used)
2	16 through 23	(Not used)
3	24 through 31	(Not used)

IOU-810 THROUGH 860 FS2 REGISTER (81) (Sheet 2 of 2)

Byte	Bit(s)	Description
	32	Error, channel 7
	33	Error, channel 6
	34	Error, channel 5
4	35	Error, channel 4
	36	Error, channel 3
	37	Error, channel 2
	38	Error, channel 1
	39	Error, channel 0
	40	Error, channel 17
	41	(Not used)
	42	Error, channel 15
	43	(Not used)
5	44	Error, channel 13
	45	Error, channel 12
	46	Error, channel 11
	47	Error, channel 10
	48	Error, channel 27
	49	Error, channel 26
	50	Error, channel 25
6	51	Error, channel 24
	52	Error, channel 23
	53	Error, channel 22
	54	Error, channel 21
	55	Error, channel 20
	56	(Not used)
	57	Error, radial interface 5/6 (IOU-835 through 860), not used (IOU-810 through 830)
	58	Error, radial interface 3/4 (IOU-835 through 860), not used (IOU-810 through 830)
7	59	Error, radial interface 1/2 (IOU-835 through 860), 2/3 (IOU-810 through 830)
	60	Error, channel 33
	61	Error, channel 32
	62	Error, channel 31
	63	Error, channel 30

IOU-835, 840, 845, 850, 855, 860 TM REGISTER (A0) (Sheet 1 of 2)

Byte	Bit(s)	Description	
0	00 through 07	(Not used)	
1	08 through 15	(Not used)	
2	16 through 23	(Not used)	
3	24 through 31	(Not used)	
4	32 through 39	(Not used)	
5	40 through 47	(Not used)	barrel 0
	48	Barrel sel	barrel 1
6	49	Barrel sel	barrel 2
	50	(Not used)	barrel 3
	51 through 55*	Invert PP parity code	

*Detail, bits 51 through 55 (IOU-835 through 860): invert parity

1	A-adder input B (PP mem)
2	A-adder input A (A barrel on chan)
3	Shift ROM
4	Firmware ROM (00 through 07)
5	PP mem data to Q-adder (B) or P-incrementor
6	P-incrementor input
7	Q-adder input A (P or Q barrel)
8	Firmware ROM (08 through 15)
9	PP mem data
A	F/W ROM (16 through 35, 46, and 47, 58 through 82)
B	Selected ROM adrs
C	PP mem data
D	R-barrel
E	A-barrel data to R-adder
F	PP mem data
10	Channel data
11	Adrs to PP mem
12	Data written into PP mem
13	Data to PP mem from CM read bfrs
14-1F	(Not used)

IOU-835, 840, 845, 850, 855, 860 TM REGISTER (A0) (Sheet 2 of 2)

Byte	Bit(s)	Description
	56 through 58	Force errors in IOU maint rgtr
	59	Force zero chan parity
7	60 through 63*	Invert parity

0-7	(Not used)
8	Invert mem FCN code parity
9	Invert mark parity

*Detail, bits 60 through 63 (IOU-835 through 860): invert parity

A	Force ones on CM adrs parity
B	Force ones on CM data parity
C	Invert tag parity
D	Invert write parity ROM parity bit
E	Invert response code parity
F	Invert input data parity

IOU (NIO)-840S, 845S, 855S, 840A, 850A, 860A, 870A, 990, 992, 994, 990E, 995E OI REGISTER (12) (Sheet 1 of 2)

Byte	Bit(s)	Description
0	00 through 07	(Not used)
1	08 through 15	(Not used)
	16 through 19	(Not used)
	20	Barrel 3, PP25 through 31
2	21	Barrel 2, PP20 through 24
	22	Barrel 1, PP5 through 11
	23	Barrel 0, PP0 through 4
	24	Channel 7
	25	Channel 6
	26	Channel 5
3	27	Channel 4
	28	Channel 3
	29	Channel 2
	30	Channel 1
	31	Channel 0

IOU (NIO)-840S, 845S, 855S, 840A, 850A, 860A, 870A, 990, 992, 994, 990E, 995E OI REGISTER (12) (Sheet 2 of 2)

Byte	Bit(s)	Description
	32	Channel 17
	33	(Not used)
	34	Channel 15
4	35	(Not used)
	36	Chnnel 13
	37	Channel 12
	38	Channel 11
	39	Channel 10
	40	Channel 27
	41	Channel 26
	42	Channel 25
	43	Channel 24
	44	Channel 23
	45	Channel 22
	46	Channel 21
	47	Channel 20
	48	Channel code 0
	49	Channel code 1
	50	Channel code 2
	51	Channel code 3
	52	Channel 33
	53	Channel 32
	54	Channel 31
	55	Channel 30
	56	CIO
	57 through 59	(Not used)
	60	Radial interface 4,5,6
	61	Radial interface 1,2,3
	62	Two-port mux
	63	CC545 controller

IOU (NIO)-840S, 845S, 855S, 840A, 850A, 860A, 870A, 990, 992, 994, 990E, 995E FSM REGISTER (18) (Sheet 1 of 2)

Byte	Bit(s)	Description
	00 through 02	(Not used)
	03	Mask vector, barrel 0 PP4
	04	Mask vector, barrel 0 PP3
0	05	Mask vector, barrel 0 PP2
	06	Mask vector, barrel 0 PP1
	07	Mask vector, barrel 0 PP0
	08 through 10	(Not used)
	11	Mask vector, barrel 1 PP4
	12	Mask vector, barrel 1 PP3
1	13	Mask vector, barrel 1 PP2
	14	Mask vector, barrel 1 PP1
	15	Mask vector, barrel 1 PP0
	16 through 18	(Not used)
	19	Mask vector, barrel 2 PP4
	20	Mask vector, barrel 2 PP3
2	21	Mask vector, barrel 2 PP2
	22	Mask vector, barrel 2 PP1
	23	Mask vector, barrel 2 PP0
	24 through 26	(Not used)
	27	Mask vector, barrel 3 PP4
	28	Mask vector, barrel 3 PP3
3	29	Mask vector, barrel 3 PP2
	30	Mask vector, barrel 3 PP1
	31	Mask vector, barrel 3 PP0

IOU (NIO)-840S, 845S, 855S, 840A, 850A, 860A, 870A, 990, 992, 994, 990E, 995E FSM REGISTER (18) (Sheet 2 of 2)

Byte	Bit(s)	Description
	32	Mask vector, channel 7
	33	Mask vector, channel 6
	34	Mask vector, channel 5
4	35	Mask vector, channel 4
	36	Mask vector, channel 3
	37	Mask vector, channel 2
	38	Mask vector, channel 1
	39	Mask vector, channel 0
	40	Mask vector, channel 17
	41	(Not used)
5	42	Mask vector, channel 15
	43	(Not used)
	44	Mask vector, channel 13
	45	Mask vector, channel 12
	46	Mask vector, channel 11
	47	Mask vector, channel 10
	48	Mask vector, channel 27
	49	Mask vector, channel 26
	50	Mask vector, channel 25
	51	Mask vector, channel 24
6	52	Mask vector, channel 23
	53	Mask vector, channel 22
	54	Mask vector, channel 21
	55	Mask vector, channel 20
	56	MAC mask vector
	57	(Not used)
	58	Mask vector, radial interface 4/5/6
7	59	Mask vector, radial interface 1/2/3
	60	Mask vector, channel 33
	61	Mask vector, channel 32
	62	Mask vector, channel 31
	63	Mask vector, channel 30

IOU (NIO)-840S, 845S, 855S, 840A, 850A, 860A, 870A, 990, 992, 994, 990E, 995E OSB REGISTER (21) (Sheet 1 of 2)

Byte	Bit(s)	Description
	00 through 02	(Not used)
	03	Bit vector, barrel 0 PP4
	04	Bit vector, barrel 0 PP3
0	05	Bit vector, barrel 0 PP2
	06	Bit vector, barrel 0 PP1
	07	Bit vector, barrel 0 PP0
	08 through 10	(Not used)
	11	Bit vector, barrel 1 PP4
	12	Bit vector, barrel 1 PP3
1	13	Bit vector, barrel 1 PP2
	14	Bit vector, barrel 1 PP1
	15	Bit vector, barrel 1 PP0
	16 through 18	(Not used)
	19	Bit vector, barrel 2 PP4
	20	Bit vector, barrel 2 PP3
2	21	Bit vector, barrel 2 PP2
	22	Bit vector, barrel 2 PP1
	23	Bit vector, barrel 2 PP0
	24 through 26	(Not used)
	27	Bit vector, barrel 3 PP4
	28	Bit vector, barrel 3 PP3
3	29	Bit vector, barrel 3 PP2
	30	Bit vector, barrel 3 PP1
	31	Bit vector, barrel 3 PP0

IOU (NIO)-840S, 845S, 855S, 840A, 850A, 860A, 870A, 990, 992, 994, 990E, 995E OSB REGISTER (21) (Sheet 2 of 2)

Byte	Bit(s)	Description
4	32 through 39	(Not used)
	40 through 45	(Not used)
5	46	OS boundary adrs 36
	47	OS boundary adrs 37
	48	OS boundary adrs 38
	49	OS boundary adrs 39
	50	OS boundary adrs 40
6	51	OS boundary adrs 41
	52	OS boundary adrs 42
	53	OS boundary adrs 43
	54	OS boundary adrs 44
	55	OS boundary adrs 45
	56	OS boundary adrs 46
	57	OS boundary adrs 47
	58	OS boundary adrs 48
7	59	OS boundary adrs 49
	60	OS boundary adrs 50
	61	OS boundary adrs 51
	62	OS boundary adrs 52
	63	OS boundary adrs 53

IOU (NIO)-840S, 845S, 855S, 840A, 850A, 860A, 870A, 990, 992, 994, 990E, 995E EC REGISTER (30) (Sheet 1 of 2)

Byte	Bit(s)	Description
0	00 through 07	(Not used)
1	08 through 15	(Not used)
2	16 through 23	(Not used)
3	24 through 31	(Not used)

IOU (NIO)-840S, 845S, 855S, 840A, 850A, 860A, 870A, 990, 992, 994, 990E, 995E EC REGISTER (30) (Sheet 2 of 2)

Byte	Bit(s)	Description
	32	8K PP memory
	33	System initialized
4	34	(Not used)
	35 through 39	PP number
5	40 through 42	(Not used)
	43 through 47	Chan number
	48 through 50	(Not used)
	51	Load mode
6	52	Dump mode
	53	Idle mode
	54,55	Rgtr sel (A,P,Q,K)
	56	Clock wide
	57	Clock narrow
	58	Enbl deadstart/dump/idle
7	59	Enbl test mode
	60	Enbl OS bounds checking
	61	Enbl (R) + (A) to PP mem
	62	Individual chan MC
	63	Enbl PP stop on error

IOU (NIO)-840S, 845S, 855S, 840A, 850A, 860A, 870A, 990, 992, 994, 990E, 995E S REGISTER (40)

Byte(s)	Bit(s)	Description
0	00 through 07	(Not used)
1	08 through 15	(Not used)
2	16 through 23	(Not used)
3	24 through 31	(Not used)
4	32 through 37	(Not used)
4-6	38 through 55	Int rgtr (A,P,Q,K)
7	56	LDS bit
	57	Timing margin (fast)
	58	Timing margin (slow)
	59,60	PP barrel reconfiguration switches
	61 through 63	PP reconfiguration switches

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IOU (NIO)-840S, 845S, 855S, 840A, 850A, 860A, 870A, 990, 992, 994, 990E, 995E FS1 REGISTER (80) (Sheet 1 of 2)

Byte	Bit(s)	Description
	00 through 02	(Not used)
	03	Error, barrel 0 PP4
	04	Error, barrel 0 PP3
0	05	Error, barrel 0 PP2
	06	Error, barrel 0 PP1
	07	Error, barrel 0 PP0
	08 through 10	(Not used)
	11	Error, barrel 1 PP4
	12	Error, barrel 1 PP3
1	13	Error, barrel 1 PP2
	14	Error, barrel 1 PP1
	15	Error, barrel 1 PP0
	16 through 18	(Not used)
	19	Error, barrel 2 PP4
	20	Error, barrel 2 PP3
2	21	Error, barrel 2 PP2
	22	Error, barrel 2 PP1
	23	Error, barrel 2 PP0
	24 through 26	(Not used)
	27	Error, barrel 3 PP4
	28	Error, barrel 3 PP3
3	29	Error, barrel 3 PP2
	30	Error, barrel 3 PP1
	31	Error, barrel 3 PP0

IOU (NIO)-840S, 845S, 855S, 840A, 850A, 860A, 870A, 990, 992, 994, 990E, 995E FS1 REGISTER (80) (Sheet 2 of 2)

Byte	Bit(s)	Description
	32	Error detected on JW module
	33	Error detected on KR module
	34	Error detected on JA module
4	35	Error detected on KB module
	36	Error detected on JC module
	37	Error detected on JD module
	38	Error detected on JE module
	39	Error detected on JF module
	40	SECDED error barrel 0
	41	SECDED error barrel 1
	42	SECDED error barrel 2
5	43	SECDED error barrel 3
	44	12/16 conversion error
	45	OS bounds violation
	46	OS boundary adrs PE
	47	Firmware error
	48	Response code error
	49	Uncorrected CM read error
	50	Uncorrected CM write error
6	51	CM reject
	52	Data in error - CMI/ADU
	53	Tag in error - CMI/ADU
	54	Data out error - CMI/ADU
	55	Address/function error - CMI/ADU/BAS
	56	Tag out error - CMI/ADU
	57	CMI error - JJ module (A06)
	58	CMI error - JJ module (A07)
	59	CMI error - JG module (A08)
7	60	CMI error - JH module (A02)
	61	CMI error - JH module (A03)
	62	CMI error - JH module (A04)
	63	CMI error - JH module (A05)

IOU (NIO)-840S, 8455, 855S, 840A, 850A, 860A, 870A, 990, 992, 994, 990E, 995E FS2 REGISTER (81) (Sheet 1 of 2)

Byte	Bit(s)	Description
0	00 through 07	(Not used)
1	08 through 15	(Not used)
2	16 through 23	(Not used)
3	24 through 31	(Not used)

IOU (NIO)-840S, 845S, 855S, 840A, 850A, 860A, 870A, 990, 992, 994, 990E, 995E FS2 REGISTER (81) (Sheet 2 of 2)

Byte	Bit(s)	Description
	32	Error, channel 7
	33	Error, channel 6
	34	Error, channel 5
4	35	Error, channel 4
	36	Error, channel 3
	37	Error, channel 2
	38	Error, channel 1
	39	Error, channel 0
	40	Error, channel 17
	41	(Not used)
	42	Error, channel 15
	43	(Not used)
5	44	Error, channel 13
	45	Error, channel 12
	46	Error, channel 11
	47	Error, channel 10
	48	Error, channel 27
	49	Error, channel 26
	50	Error, channel 25
	51	Error, channel 24
6	52	Error, channel 23
	53	Error, channel 22
	54	Error, channel 21
	55	Error, channel 20
	56	MAC error
	57	(Not used)
	58	Error, radial interface 4/5/6
7	59	Error, radial interface 1/2/3
	60	Error, channel 33
	61	Error, channel 32
	62	Error, channel 31
	63	Error, channel 30

Byte	Bit(s)	Description
0	00 through 07	(Not used)
1	08 through 15	(Not used)
2	16 through 23	(Not used)
3	24 through 31	(Not used)
4	32 through 39	(Not used)
5	40 through 47	(Not used)
6	48 through 50	(Not used)
	51,52	Logical barrel number
	53 through 55	Logical PP number
7	56,57	(Not used)
	58 through 63*	Test code

*Details for bits 58 through 63:

NOTE

The test codes, 00-27, apply to barrels 0-3.

Test Code(s)	Function
00	(Not used)
01	Invert chan to PP parity at generator
02	Invert PP to chan parity at generator
03	Invert PPM to R rgtr parity at generator
04	Invert PPM parity at checker
05	Invert microcode data parity at checker

IOU (NIO)-840S, 845S, 855S, 840A, 850A, 860A, 870A, 990, 992, 994, 990E, 995E TM REGISTER (A0) (Sheet 2 of 3)

Test Code(s)	Function
06	Invert PPM parity at generator
07	Invert CM fctn code parity at generator
10	Invert Y rgtr parity at generator
11	Invert A rgtr parity at generator
12	Invert shift control ROM parity at checker
13	Invert Q rgtr parity at generator
14	Invert P rgtr parity at generator
15	Invert G rgtr partity at generator
16	Invert R to Y parity at generator
17	Invert PPM adrs parity at checker
20	Invert tag out parity at generator (ADU) JE pak
21	Invert data-in parity at generator (ADU) JF pak
22	Invert central mem adrs
23	Invert SECDED code to PP mem
24 through 27	(Not used)

NOTE

The test codes, 30-37, apply to the CMI.

Test Code(s)	Function
30	Force CM request priority/resynch error
31	Force tag in PE
32	Force tag out PE
33	Force response code PE
34	Invert fctn out parity bit
35	Force adrs out parity bit low
36	Force data in parity bit low
37	Force data out parity bit low

NOTE

The test codes, 40-47, apply to the MAC.

Test Code(s)	Function
40	Invert chan parity
41	Invert MR write parity
42	Invert nano code parity
43	Invert read parity bit
44	Invert chan 15 data bus parity at checker
45	Invert R/I read data parity
46	Invert R/I read data parity
47	(Not used)

NOTE

The test codes, 50-57, apply to the ADU/CMI.

Test Code(s)	Function
50	Force central mem request (ADU) JD pak
51	Force tag in PE (ADU) JD pak
52	Force response code parity error (ADU) JD pak
53	Block D5 FULL (ADU) JD pak
54	Force CMC busy at CMI
55	Force OSB adrs PE
56	Set inhibit PP CM request
57	Clear inhibit PP CM request

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IOU (CIO)-840A, 850A, 860A, 870A, 990, 992, 994, 990E, 995E OI REGISTER (16) (Sheet 1 of 2)

Byte	Bit(s)	Description
0	00 through 07	(Not used)
1	08 through 15	(Not used)
	16 through 21	(Not used)
2	22	Barrel 1
	23	Barrel 0
	24	Channel 7
	25	Channel 6
	26	Channel 5
3	27	Channel 4
	28	Channel 3
	29	Channel 2
	30	Channel 1
	31	Channel 0

IOU (CIO)-840A, 850A, 860A, 870A, 990, 992, 994, 990E, 995E OI REGISTER (16) (Sheet 2 of 2)

Byte	Bit(s)	Description	Code	Type
	32	Channel 17		
	33	(Not used)		
	34	Channel 15		
4	35 through 37	(Not used)		
	38	Channel 11		
	39	Channel 10		
5	40 through 47	(Not used)		
	48	Channel code 0	03	ISI
	49	Channel code 1		
6	50	Channel code 2	05	170
	51	Channel code 3	07	IPI
	52 through 55	(Not used)		
7	56 through 63	(Not used)		

IOU (CIO)-840A, 850A, 860A, 870A, 990, 992, 994, 990E, 995E FSM REGISTER (1C) (Sheet 1 of 2)

Byte	Bit(s)	Description
	00 through 02	(Not used)
	03	Mask vector, barrel 0 PP4
	04	Mask vector, barrel 0 PP3
0	05	Mask vector, barrel 0 PP2
	06	Mask vector, barrel 0 PP1
	07	Mask vector, barrel 0 PP0
	08 through 10	(Not used)
	11	Mask vector, barrel 1 PP4
	12	Mask vector, barrel 1 PP3
1	13	Mask vector, barrel 1 PP2
	14	Mask vector, barrel 1 PP1
	15	Mask vector, barrel 1 PP0
2	16 through 23	(Not used)
3	24 through 31	(Not used)

IOU (CIO)-840A, 850A, 860A, 870A, 990, 992, 994, 990E, 995E FSM REGISTER (1C) (Sheet 2 of 2)

Byte	Bit(s)	Description
	32	Mask vector, channel 7
	33	Mask vector, channel 6
	34	Mask vector, channel 5
4	35	Mask vector, channel 4
	36	Mask vector, channel 3
	37	Mask vector, channel 2
	38	Mask vector, channel 1
	39	Mask vector, channel 0
	40 through 45	(Not used)
5	46	Mask vector, channel 11
	47	Mask vector, channel 10
6	48 through 55	(Not used)
7	56 through 63	(Not used)

IOU (CIO)-840A, 850A, 860A, 870A, 990, 992, 994, 990E, 995E, OSB REGISTER (25)

Byte	Bit(s)	Description
	00 through 02	(Not used)
	03	Bit vector, barrel 0 PP4
	04	Bit vector, barrel 0 PP3
0	05	Bit vector, barrel 0 PP2
	06	Bit vector, barrel 0 PP1
	07	Bit vector, barrel 0 PP0
	08 through 10	(Not used)
	11	Bit vector, barrel 1 PP4
	12	Bit vector, barrel 1 PP3
1	13	Bit vector, barrel 1 PP2
	14	Bit vector, barrel 1 PP1
	15	Bit vector, barrel 1 PP0
2	16 through 23	(Not used)
3	24 through 31	(Not used)
4	32 through 39	(Not used)
5	40 through 47	(Not used)
6	48 through 55	(Not used)
7	56 through 63	(Not used)

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IOU (CIO)-840A, 850A, 860A, 870A, 990, 992, 994, 990E, 995E EC REGISTER (34) (Sheet 1 of 2)

Byte	Bit(s)	Description
0	00 through 07	(Not used)
1	08 through 15	(Not used)
2	16 through 23	(Not used)
3	24 through 31	(Not used)

IOU (CIO)-840A, 850A, 860A, 870A, 990, 992, 994, 990E, 995E EC REGISTER (34) (Sheet 2 of 2)

Byte	Bit(s)	Description
	32	Constant ONE
4	33 through 35	(Not used)
	36 through 39	PP number
5	40 through 43	(Not used)
	44 through 47	Channel number
	48 through 50	(Not used)
	51	Load mode
6	52	Dump mode
	53	Idle mode
	54,55	Rgtr sel (A,P,Q,K)
	56,57	(Not used)
	58	Enbl deadstart/dump/idle
7	59	Enbl test mode
	60	Enbl OS bounds checking
	61	Enbl (R)+(A) to PP mem
	62	Individual chan MC
	63	Enbl error stop

IOU (CIO)-840A, 850A, 860A, 870A, 990, 992, 994, 990E, 995E S REGISTER (44)

Byte(s)	Bit(s)	Description
0	00 through 07	(Not used)
1	08 through 15	(Not used)
2	16 through 23	(Not used)
3	24 through 31	(Not used)
4	32 through 37	(Not used)
4-6	38 through 55	Int rgtr (A,P,Q, or K)
7	56 through 63	(Not used)

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IOU (CIO)-840A, 850A, 860A, 870A, 990, 992, 994, 990E, 995E FS1 REGISTER (84) (Sheet 1 of 2)

Byte	Bit(s)	Description
	00 through 02	(Not used)
	03	Error, barrel 0 PP4
	04	Error, barrel 0 PP3
0	05	Error, barrel 0 PP2
	06	Error, barrel 0 PP1
	07	Error, barrel 0 PP0
	08 through 10	(Not used)
	11	Error, barrel 1 PP4
	12	Error, barrel 1 PP3
1	13	Error, barrel 1 PP2
	14	Error, barrel 1 PP1
	15	Error, barrel 1 PP0
2	16 through 23	(Not used)
3	24 through 31	(Not used)

IOU (CIO)-840A, 850A, 860A, 870A, 990, 992, 994, 990E, 995E FS1 REGISTER (84) (Sheet 2 of 2)

Byte	Bit(s)	Description
	32	Error detected on JW module
	33	Error detected on KR module
	34	(Not used)
4	35	Error detected on KB module
	36	Error detected on JC module
	37	Error detected on JD module
	38	Error detected on JE module
	39	Error detected on JF module
	40	SECDED error barrel 0
	41	SECDED error barrel 1
	42,43	(Not used)
5	44	12/16 conversion error
	45	OS bounds violation
	46	OS boundary adrs PE
	47	Firmware error
	48	Response code error
	49	Uncorrected CM read error
	50	Uncorrected CM write error
6	51	CM reject
	52	Data in error - CMI/ADU
	53	(Not used)
	54	Data out error - CMI/ADU
	55	Address/function error - CMI/ADU/BAS
7	56 through 63	(Not used)

IOU (CIO)-840A, 850A, 860A, 870A, 990, 992, 994, 990E, 995E FS2 REGISTER (85)

Byte	Bit(s)	Description
0	00 through 07	(Not used)
1	08 through 15	(Not used)
2	16 through 23	(Not used)
3	24 through 31	(Not used)
4	32	Error, channel 7
	33	Error, channel 6
	34	Error, channel 5
	35	Error, channel 4
	36	Error, channel 3
	37	Error, channel 2
	38	Error, channel 1
	39	Error, channel 0
5	40 through 45	(Not used)
	46	Error, channel 11
	47	Error, channel 10
6	48 through 55	(Not used)
7	56 through 63	(Not used)

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IOU (CIO)-840A, 850A, 860A, 870A, 990, 992, 994, 990E, 995E TM REGISTER (A4) (Sheet 1 of 2)

Byte	Bit(s)	Description
0	00 through 07	(Not used)
1	08 through 15	(Not used)
2	16 through 23	(Not used)
3	24 through 31	(Not used)
4	32 through 39	(Not used)
5	40 through 47	(Not used)
6	48 through 50	(Not used)
	51,52	Logical barrel number
	53 through 55	Logical PP number
7	56,57	(Not used)
	58 through 63*	Test code

*Details for bits 58-63:

IOU (CIO)-840A, 850A, 860A, 870A, 990, 992, 994, 990E, 995E TM REGISTER (A4) (Sheet 2 of 2)

NOTE

The test codes, 00 through 27, apply to barrels 0 through 3.

Test Code(s)	Function
00	(Not used)
01	Invert chan to PP parity at generator
02	Invert PP to chan parity at generator
03	Invert PPM to rgtr parity at generator
04	Invert PPM parity at checker
05	Invert microcode data parity at checker
06	Invert PPM parity at generator
07	Invert CM fctn code parity at generator
10	Invert Y rgtr parity at generator
11	Invert A rgtr parity at generator
12	Invert shift control ROM parity at checker
13	Invert Q rgtr parity at generator
14	Invert P rgtr parity at generator
15	Invert G rgtr parity at generator
16	Invert R to Y parity at generator
17	Invert PPM adrs parity at checker
20	Invert tag out parity at generator (ADU) JE pak
21	Invert data-in parity at generator (ADU) JF pak
22	Invert central mem adrs
23	Invert SECDED code to PP mem
24 through 27	(Not used)

ISI CHANNEL ADAPTER

Byte(s)	Bit(s)	Description
	00,01	(Not used)
	02	Uncorrected CM error
	03	CM reject
0	04	Invalid CM response
	05	Response code PE
	06	CMI read data PE
	07	TM compare error
	08	Overflow error
	09	ISI input
	10	ISI timeout
	11	JY data error
1	12	BAS PE
	13	JZ error
	14	JY error
	15	JX error
2	16 through 23	(Not used)
	24	(Not used)
	25	Input bfr full
	26	Pause
3	27	Sync in
	28	Sync out
	29	Command sequence
	30	Select active
	31	Select hold

ISI CHANNEL ADAPTER

Byte(s)	Bit(s)	Description
	32	(Not used)
	33	Echo mode
	34	Output mode
4	35	PP mode
	36	DMA mode
	37	Non-interlocked mode
	38	T rgtr empty
	39	Transfer in progress
	40 through 43	(Not used)
	44	Active flag
5	45	Full flag
	46	Error flag
	47	Chan flag
	48	Enbl cache invalidate
	49	Port B enbl
	50	Dsbl ISI
6	51	Enbl test mode
	52	Inhibit TM incr
	53	Inhibit sync out
	54	Inhibit out request cntr
	55	Enbl idle mode
	56	Enbl force error codes
	57,58	(Not used)
	59	Force error 0
7	60	Force error 1
	61	Force error 2
	62	Force error 3
	63	Force error 4

170 CHANNEL ADAPTER

Byte(s)	Bit(s)	Description
	00,01	(Not used)
	02	Uncorrected CM Error
	03	CM reject
0	04	Invalid response
	05	Any response code PE
	06	CMI read data PE
	07	Clock fault
	08	Overflow error
	09	Input data error
	10	12/16 conversion error
1	11	A/D data error
	12	BAS PE
	13	KZ board error
	14	JY board error
	15	KX board error
2	16 through 23	PP word counter bits 56 through 63
	24 through 27	(Not used)
	28	Output buffer full
3	29	Input buffer full
	30	Data available to channel
	31	Fast transfer

170 CHANNEL ADAPTER

Byte(s)	Bit(s)	Description
	32	External clock present
	33	Test mode
	34	PP word count = 0
4	35	DMA output
	36	DMA input
	37	DMA halted
	38	T register empty
	39	Transfer in progress
	40,41	(Not used)
	42	Full I
	43	Full II
5	44	Active
	45	Full I or Full II
	46	Error flag
	47	Channel flag
	48	Enable cache invalidate
	49	(Not used)
	50	60-bit mode
6	51	Enable test clock
	52	Disable external clock
	53	Block full out
	54	Enable overflow
	55	Disable error register clear
	56	Enable force error codes
7	57,58	(Not used)
	60 through 63	Force error code bits 0 through 4

IPI CHANNEL ADAPTER

Byte(s)	Bit(s)	Description
	00	(Not used)
	01	Illegal function or sequence
	02	Uncorrected CM Error
	03	CM reject
0	04	Invalid response code
	05	CM response code PE
	06	CMI read data PE
	07	IPI error
	08	DMA register PE
	09	MAC status PE
	10	Timeout
1	11	A/D data error
	12	BAS reject PE
	13	LZ board error
	14	JY board error
	15	LX board error
	16	Buffer count PE
	17	(Not used)
	18	Sync count PE
2	19	Period count PE
	20	Function upper PE
	21	Function lower PE
	22, 23	(Not used)
	24	Lost data
	25	ICI upper data PE
	26	ICI lower data PE
3	27	IPI sequence error
	28	IPI bus A PE
	29	IPI bus B PE
	30	Illegal operation
	31	(Not used)

IOU (CIO)-840A, 850A, 860A, 870A, 990, 992, 994, 990E, 995E CHANNEL 0 THROUGH 11 S REGISTERS (B0 THROUGH B9) (Sheet 6 of 6)

IPI CHANNEL ADAPTER

Byte(s)	Bit(s)	Description
	32, 33	(Not used)
	34	Output mode
	35	(Not used)
4	36	DMA/IPI mode
	37	DMA/IPI inactive
	38	T prime register empty
	39	Transfer in progress
	40 through 43	(Not used)
	44	Active
5	45	Full
	46	Error
	47	Flag
	48	Enable cache invalidate
	49	(Not used)
	50	Disable timeout
6	51	Enable test mode
	52	Inhibit test mode increment
	53	Enable transfer in progress flag
	54	Enable T prime empty flag
	55	(Not used)
	56	Error
	57	Attention
	58	Buffer not empty
7	59	Select out
	60	Slave in
	61	Master out
	62	Sync in
	63	Sync out

NOTES

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