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New features, as well as changes, deletions, and additions to information in this manual, are indicated by bars in the margins or by a dot near the page number if the entire page is affected. A bar by the page number indicates pagination rather than content has changed.

PAGE	REV
Cover	-
Title Page	-
ii	A
iii/iv	A
v/vi	A
vii	A
viii	A
1	A
2	A
3	A
4	A
5	A
6	A
7	A
8	A
9/10	A
11	A
12	A
13	A
14	A
15	A
16	A
17	A
18	A
19	A
20	A
21	A
22	A
23	A

PAGE	REV
24	A
25	A
26	A
27	A
28	A
29	A
30	A
31	A
32	A
33	A
34	A
35	A
36	A
37	A
38	A
39	A
40	A
41	A
42	A
43	A
44	A
45	A
46	A
47	A
48	A
49	A
50	A
51	A
Cover	-

PREFACE

This manual contains code and timing information for the CONTROL DATA®CYBER 170 Computer Systems, Models 172 through 175. Data is derived from the hardware reference manuals listed below. The information contained in this code book does not supplant information contained in the reference manuals; nor is the information contained in this book as complete as that in the reference manuals. In cases of conflict, consider the reference manuals more authoritative, reliable, and current.

The following manuals provide detailed information. Refer to the CDC Literature and Distribution Services catalog for the latest revision levels and literature ordering procedures.

CDC Publication	Publication Number
CDC CYBER 170 Hardware Reference Manual	60420000
7030-1XX ECS Subsystem and 6642-2 Distributive Data Path	60430000
CC545-A/B Display Station Hardware Reference/Customer Engineering Manual	62978200
CC545-C/D/E/F Display Station Hardware Reference/Customer Engineering Manual	62952600

CONTENTS

FIGURES

TABLES

PERIPHERAL AND CONTROL PROCESSOR INSTRUCTIONS

This segment of the manual describes the peripheral processor (PP) instructions identical for all models.

INSTRUCTION FORMATS

Two instruction formats are used. The 12-bit format (figure 1) has a 6-bit operation code f and a 6-bit operand or operand address d. The 24-bit format (figure 2) uses the 12-bit quantity m, the content of the next program address (P plus 1), with d to form an 18-bit operand address.

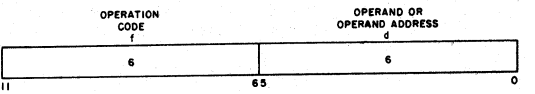


Figure 1. 12-Bit Instruction Format (PP)

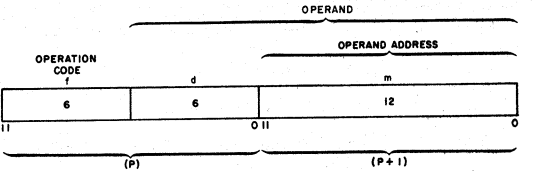


Figure 2. 24-Bit Instruction Format (PP)

INSTRUCTION DESIGNATOR DESCRIPTIONS

Instruction designators are listed and described in table 1.

TABLE 1. PERIPHERAL PROCESSOR INSTRUCTION DESIGNATORS

Designator	Use
A	A register
d	6-bit operand address, jump count, shift count, channel designator, or additional instruction code
f	12-bit operand address, 12-bit jump address, 12-bit function code, or 12-bit quantity used with d to form an 18-bit operand
m	12-bit quantity used with d to form an 18-bit operand or operand address
P	Program address register
Q	Q register
( )	Content of a register or location
(( ))	Indirect addressing

Designator use in the PP instruction listings is as follows.

d	Implies d itself
(d)	Implies the contents of d
((d))	Implies the contents of the location specified by d
m	Implies m itself used as an address
m + (d)	The contents of d are added to m to form an operand (jump address)
(m + (d))	The contents of d are added to m to form the address of the operand
dm	Implies an 18-bit quantity with d as the upper 6 bits and m as the lower 12 bits

PP INSTRUCTION LISTINGS

The PP operates in a 1000-nanosecond (1X mode) major cycle time or in a 500-nanosecond (2X mode) major cycle time. Execution times are given in minor cycles (100 nanoseconds in 1X mode, and 50 nanoseconds in 2X mode). The PP instructions are listed in table 2 (numeric sequence) and table 3 (functional groups).

TABLE 2. PERIPHERAL PROCESSOR INSTRUCTIONS, NUMERICAL SEQUENCE

Instruction Code	Description	Execution	
		Time	Notes
0000	Pass	10	
01dm	Long jump to m + (d)	-	1
02dm	Return jump to m + (d)	-	2
03d	Unconditional jump d	10	
04d	Zero jump d	10	
05d	Nonzero jump d	10	
06d	Plus jump d	10	
07d	Minus jump d	10	
10d	Shift d	10	
11d	Logical difference d	10	
12d	Logical product d	10	
13d	Selective clear d	10	
14d	Load d	10	
15d	Load complement d	10	
16d	Add d	10	
17d	Subtract d	10	
20dm	Load dm	20	
21dm	Add dm	20	
22dm	Logical product dm	20	
23dm	Logical difference dm	20	
2400	Pass	10	
2500	Pass	10	
260x	Exchange jump	-	3, 9
261x	Monitor exchange jump	-	3, 9
262x	Monitor exchange jump to MA	-	3, 9
27x	Read program address	10	
30d	Load (d)	20	
31d	Add (d)	20	
32d	Subtract (d)	20	

TABLE 2. PERIPHERAL PROCESSOR INSTRUCTIONS, NUMERICAL SEQUENCE (Contd)

Instruction Code	Description	Execution	
		Time	Notes
33d	Logical difference (d)	20	
34d	Store d	20	
35d	Replace add (d)	30	
36d	Replace add one (d)	30	
37d	Replace subtract one (d)	30	
40d	Load ((d))	30	
41d	Add ((d))	30	
42d	Subtract ((d))	30	
43d	Logical difference ((d))	30	
44d	Store ((d))	30	
45d	Replace add ((d))	40	
46d	Replace add one ((d))	40	
47d	Replace subtract one ((d))	40	
50dm	Load (m + (d))	-	2
51dm	Add (m + (d))	-	2
52dm	Subtract (m + (d))	-	2
53dm	Logical difference (m + (d))	-	2
54dm	Store (m + (d))	-	2
55dm	Replace add (m + (d))	-	4
56dm	Replace add one (m + (d))	-	4
57dm	Replace subtract one (m + (d))	-	4
60d	Central read from (A) to d	-	5, 8
61dm	Central read (d) words to (A) from m	-	6, 8
62d	Central write to (A) from d	-	5, 8
63dm	Central write (d) words to (A) from m	-	6, 8
64dm	Jump to m if channel d active	20	
65dm	Jump to m if channel d inactive	20	

TABLE 2. PERIPHERAL PROCESSOR INSTRUCTIONS, NUMERICAL SEQUENCE (Contd)

Instruction Code	Description	Execution	
		Time	Notes
66dm	Jump to m if channel d full	20	
67dm	Jump to m if channel d empty	20	
70d	Input to A from channel d	20	
71dm	Input (A) words to m from channel d	-	7, 10
72d	Output from A on channel d	20	
73dm	Output (A) words from m on channel d	-	7, 10
74d	Activate channel d	20	
75d	Disconnect channel d	20	
76d	Function (A) on channel d	20	
77dm	Function m on channel d	20	

Timing Notes:

0. Execution times in this table are expressed in minor cycles.
1. 30 cycles; if d = 0, 20 cycles.
2. 40 cycles; if d = 0, 30 cycles.
3. Executes in 10 cycles if no CMC conflict occurs.
4. 50 cycles; if d = 0, 40 cycles.
5. Minimum of 60 cycles.
6. 60 cycles plus 50 cycles per word.
7. 50 cycles plus 10 cycles per word.
8. Conflicts in CM cause indeterminate delays.
9. Following an exchange jump instruction, the CP must complete the exchange jump before further PPM references or exchange jump instructions can be executed.
10. Instructions for input/output (I/O) and for PPM references can transfer a word every 10 cycles although the peripheral equipment seldom permits this rate for I/O operations.

TABLE 3. PERIPHERAL PROCESSOR INSTRUCTIONS, FUNCTIONAL GROUPS

Instruction Code	Description	Execution Time	Execution Notes
No Operation			
0000	Pass	10	
2400	Pass	10	
2500	Pass	10	
Data Transmission			
14d	Load d	10	
15d	Load complement d	10	
20dm	Load dm	20	
30d	Load (d)	20	
34d	Store d	20	
40d	Load ((d))	30	
44d	Store ((d))	30	
50dm	Load (m + (d))	-	2
54dm	Store (m + (d))	-	2
Arithmetic			
16d	Add d	10	
17d	Subtract d	10	
21dm	Add dm	20	
31d	Add (d)	20	
32d	Subtract (d)	20	
41d	Add ((d))	30	
42d	Subtract ((d))	30	
51dm	Add (m + (d))	-	2
52dm	Subtract (m + (d))	-	2
Shift			
10d	Shift d	10	

TABLE 3. PERIPHERAL PROCESSOR INSTRUCTIONS, FUNCTIONAL GROUPS (Contd)

Instruction Code	Description	Execution	
		Time	Notes
Logical			
11d	Logical difference d	10	
12d	Logical product d	10	
13d	Selective clear d	10	
22dm	Logical product dm	20	
23dm	Logical difference dm	20	
33d	Logical difference (d)	20	
43d	Logical difference ((d))	30	
53dm	Logical difference (m + (d))	-	2
Replace			
35d	Replace add (d)	30	
36d	Replace add one (d)	30	
37d	Replace subtract one (d)	30	
45d	Replace add ((d))	40	
46d	Replace add one ((d))	40	
47d	Replace subtract one ((d))	40	
55dm	Replace add (m + (d))	-	4
56dm	Replace add one (m + (d))	-	4
57dm	Replace subtract one (m + (d))	-	4
Branch			
01dm	Long jump to m + (d)	-	1
02dm	Return jump to m + (d)	-	2
03d	Unconditional jump d	10	
04d	Zero jump d	10	
05d	Nonzero jump d	10	
06d	Plus jump d	10	
07d	Minus jump d	10	

TABLE 3. PERIPHERAL PROCESSOR INSTRUCTIONS, FUNCTIONAL GROUPS (Contd)

Instruction Code	Description	Execution	
		Time	Notes
CP and CM			
260x	Exchange jump	-	3, 9
261x	Monitor exchange jump	-	3, 9
262x	Monitor exchange jump to MA	-	3, 9
27x	Read program address	10	
60d	Central read from (A) to d	-	5, 8
61dm	Central read (d) words to (A) from m	-	6, 8
62d	Central write to (A) from d	-	5, 8
63dm	Central write (d) words to (A) from m	-	6, 8
Input/Output			
64dm	Jump to m if channel d active	20	
65dm	Jump to m if channel d inactive	20	
66dm	Jump to m if channel d full	20	
67dm	Jump to m if channel d empty	20	
70d	Input to A from channel d	20	
71dm	Input (A) words to m from channel d	-	7, 10
72d	Output from A on channel d	20	
73dm	Output (A) words from m on channel d	-	7, 10
74d	Activate channel d	20	
75d	Disconnect channel d	20	
76d	Function (A) on channel d	20	
77dm	Function m on channel d	20	

Timing Notes:

See applicable timing notes at the end of table 2.

CENTRAL PROCESSOR INSTRUCTIONS

This segment of the manual describes the central processor (CP) instructions. Some differences exist in the CP instructions because of model differences. The instruction differences are identified with the applicable model numbers (172, 173, 174, and 175).

INSTRUCTION FORMATS

Program instruction words are divided into 15-bit fields called parcels. The first parcel (parcel 0) is the highest-order 15 bits of the 60-bit word. The second, third, and fourth parcels (parcels 1, 2, and 3) follow in order. An instruction may occupy one, two, or four parcels, depending on the type of instruction. When an instruction occupies two parcels, it must occupy two parcels within the same program word. Possible parcel arrangements are illustrated in figure 3. Instruction designators are listed and defined in table 4.

A program word may be filled with a one-parcel pass instruction or an instruction acting as a two-parcel pass instruction. These instructions are used to fill a program word when necessary to place a particular instruction in the first parcel of a program word or to avoid starting a two-parcel instruction in the fourth parcel of a program word. Pass instructions may also be used for branch entry points because a branch instruction destination address must begin with a new word. One-parcel instructions are 460xx through 463xx. Instructions 60xxx through 62xxx may be used as two-parcel pass instructions by setting the i instruction designator to zero.

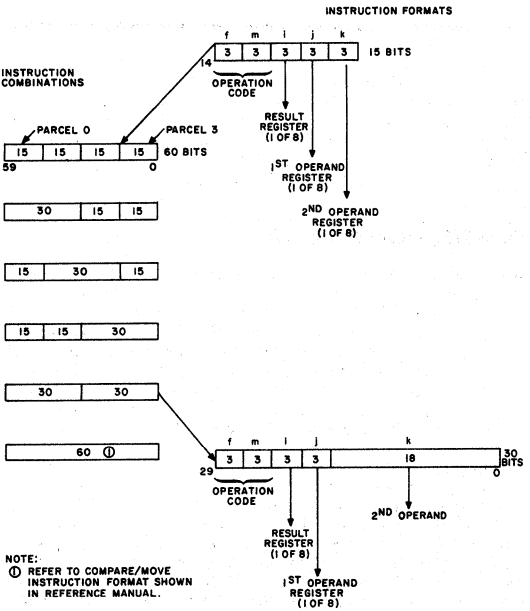


Figure 3. Central Processor Instruction Formats

TABLE 4. CENTRAL PROCESSOR INSTRUCTION DESIGNATORS

Designator	Use
fm	6-bit instruction code
fmi	9-bit instruction code
i	3-bit code specifying one of eight registers
j	3-bit code specifying one of eight registers
jk	6-bit code specifying amount of shift or mask
k	3-bit code specifying one of eight registers
K	18-bit operand or address
x	Unused designator
A	One of eight 18-bit address registers
B	One of eight 18-bit index registers; B0 is fixed and equal to zero
X	One of eight 60-bit operand registers
( )	Content of a register or location
	Compare/Move (Models 172, 173, and 174)
C1	Offset (character address) of the first character in the first word of the source field
C2	Character address of the first character in the first word of the result field
K1	18-bit address indicating the central memory location of the first (leftmost) character of the source field
K2	18-bit address indicating the central memory location of the first (leftmost) character of the result field
LL	Lower 4 bits of the field length (character count) for a move or compare instruction; used with LU to specify field length
LU	Upper 9 bits of the field length (character count) for indirect move instruction or the upper 3 bits for direct instructions; used with LL to specify field length

CP INSTRUCTION LISTINGS

Execution times for the CP instructions are given in tables 5 and 6 for models 172 through 174; tables 7 and 8 for model 175. The times listed in the execution time columns assume that no conflicts occur. Execution times are expressed in clock periods. Models 172 through 174 have 50-nanosecond clock periods. Model 175 has a 25-nanosecond clock period.

EXIT MODE

UNCONDITIONAL

If the error is an illegal instruction, breakpoint, or an address-range error on an RNI or branch, the program interruption is unconditional.

SELECTED

Mode selection bits determine program interruption for other types of errors. If the mode selection bit is set and the corresponding error condition is detected, the program is interrupted. Exit selection bits and the actual error condition bits set in RA are as follows:

Condition Bit	Mode Selection Bit	Error Condition
48	48	Address range error
49	49	Infinite mode
50	50	Indefinite mode
51	57	Parity error on ECS flag register operation
52	58	Address and data parity error at CMC
53	59	Double error or CMC→CPU data parity error

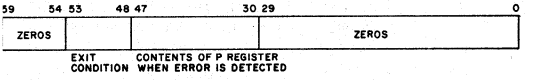


Figure 4. Relative Address Zero on Error Exit

TABLE 5. CENTRAL PROCESSOR INSTRUCTIONS NUMERIC SEQUENCE; MODELS 172, 173, AND 174

Instruction Code	Description	Execution Time		
		172	173/174	Notes
00xxx	Error exit to MA or program stop	-	-	9
010xK	Return jump to K	36	29	-
011jK	Block copy (Bj) + K words from ECS to CM	-	-	3
012jK	Block copy (Bj) + K words from CM to ECS	-	-	3
013jK	Central exchange jump to (Bj) + K	49	42	-
02ixK	Jump to (Bi) + K	29	22	-
030jK	Branch to K if (Xj) = 0	29	22	1
031jK	Branch to K if (Xj) ≠ 0	29	22	1
032jK	Branch to K if (Xj) positive	29	22	1
033jK	Branch to K if (Xj) negative	29	22	1
034jK	Branch to K if (Xj) in range	29	22	1
035jK	Branch to K if (Xj) out of range	29	22	1
036jK	Branch to K if (Xj) definite	29	22	1
037jK	Branch to K if (Xj) indefinite	29	22	1
04ijK	Branch to K if (Bi) = (Bj)	29	22	1
05ijK	Branch to K if (Bi) ≠ (Bj)	29	22	1
06ijK	Branch to K if (Bi) ≥ (Bj)	29	22	1
07ijK	Branch to K if (Bi) < (Bj)	29	22	1
10ijx	Transmit (Xj) to Xi	10	4	-
11ijk	Logical product of (Xj) and (Xk) to Xi	12	6	-

TABLE 5. CENTRAL PROCESSOR INSTRUCTIONS NUMERIC SEQUENCE; MODELS 172, 173, AND 174 (Contd)

Instruction Code	Description	Execution Time		
		172	173/174	Notes
12ijk	Logical sum of (Xj) and (Xk) to Xi	12	6	-
13ijk	Logical difference of (Xj) and (Xk) to Xi	12	6	-
14ixk	Transmit complement of (Xk) to Xi	10	4	-
15ijk	Logical product of (Xj) and complement of (Xk) to Xi	12	6	-
16ijk	Logical sum of (Xj) and complement of (Xk) to Xi	12	6	-
17ijk	Logical difference of (Xj) and complement of (Xk) to Xi	12	6	-
20ijk	Left shift (Xi) by jk	12	6	-
21ijk	Right shift (Xi) by jk	12	6	-
22ijk	Left shift (Xk) nominally (Bj) places to Xi	12	6	-
23ijk	Right shift (Xk) nominally (Bj) places to Xi	12	6	-
24ijk	Normalize (Xk) to Xi and Bj	13	7	-
25ijk	Round normalize (Xk) to Xi and Bj	13	7	-
26ijk	Unpack (Xk) to Xi and Bj	12	6	-
27ijk	Pack (Xk) and (Bj) to Xi	12	6	-
30ijk	Floating sum of (Xj) and (Xk) to Xi	17	11	-
31ijk	Floating difference of (Xj) and (Xk) to Xi	17	11	-
32ijk	Floating DP sum of (Xj) and (Xk) to Xi	17	11	-

TABLE 5. CENTRAL PROCESSOR INSTRUCTIONS NUMERIC SEQUENCE; MODELS 172, 173, AND 174 (Contd)

Instruction Code	Description	Execution Time		
		172	173/174	Notes
33ijk	Floating DP difference of (Xj) and (Xk) to Xi	17	11	-
34ijk	Round floating sum of (Xj) and (Xk) to Xi	17	11	-
35ijk	Round floating difference of (Xj) and (Xk) to Xi	17	11	-
36ijk	Integer sum of (Xj) and (Xk) to Xi	12	6	-
37ijk	Integer difference of (Xj) and (Xk) to Xi	12	6	-
40ijk	Floating product of (Xj) and (Xk) to Xi	64	58	-
41ijk	Round floating product of (Xj) and (Xk) to Xi	64	58	-
42ijk	Floating DP product of (Xj) and (Xk) to Xi	64	58	-
43ijk	Form mask of jk bits to Xi	12	6	-
44ijk	Floating divide (Xj) by (Xk) to Xi	64	58	-
45ijk	Round floating divide (Xj) by (Xk) to Xi	64	58	-
460xx	No operation (pass)	10	3	-
464jK	Move indirect	-	-	4, 6
465	Move direct	-	-	4, 5
466	Compare collated	-	-	4, 8
467	Compare uncollated	-	-	4, 7
47ixk	Population count of (Xk) to Xi	73	67	-
50ijK	Set Ai to (Aj) + K	-	-	2
51ijK	Set Ai to (Bj) + K	-	-	2
52ijK	Set Ai to (Xj) + K	-	-	2
53ijk	Set Ai to (Xj) + (Bk)	-	-	2

TABLE 5. CENTRAL PROCESSOR INSTRUCTIONS NUMERIC SEQUENCE; MODELS 172, 173, AND 174 (Contd)

Instruction Code	Description	Execution Time		
		172	173/174	Notes
54ijk	Set Ai to (Aj) + (Bk)	-	-	2
55ijk	Set Ai to (Aj) - (Bk)	-	-	2
56ijk	Set Ai to (Bj) + (Bk)	-	-	2
57ijk	Set Ai to (Bj) - (Bk)	-	-	2
60ijK	Set Bi to (Aj) + K	11	5	-
61ijK	Set Bi to (Bj) + K	11	5	-
62ijK	Set Bi to (Xj) + K	11	5	-
63ijk	Set Bi to (Xj) + (Bk)	11	5	-
64ijk	Set Bi to (Aj) + (Bk)	11	5	-
65ijk	Set Bi to (Aj) - (Bk)	11	5	-
66ijk	Set Bi to (Bj) + (Bk)	11	5	-
67ijk	Set Bi to (Bj) - (Bk)	11	5	-
70ijK	Set Xi to (Aj) + K	12	6	-
71ijK	Set Xi to (Bj) + K	12	6	-
72ijK	Set Xi to (Xj) + K	12	6	-
73ijk	Set Xi to (Xj) + (Bk)	12	6	-
74ijk	Set Xi to (Aj) + (Bk)	12	6	-
75ijk	Set Xi to (Aj) - (Bk)	12	6	-
76ijk	Set Xi to (Bj) + (Bk)	12	6	-
77ijk	Set Xi to (Bj) - (Bk)	12	6	-

Timing Notes:

0. Execution times in this table are given in clock periods. Models 172, 173, and 174 have 50-nanosecond clock periods.
1. 5 clock periods if jump condition not present.
2. If i = 0, model 172 - 12 clock periods; models 173 and 174 - 5 clock periods.
   If i = 1 through 5, model 172 - 28 clock periods; models 173 and 174 - 21 clock periods.
   If i = 6 or 7, model 172 - 17 clock periods; models 173 and 174 - 10 clock periods.
3. Refer to ECS timing information in volume 3 of publication number 60347100.

TABLE 5. CENTRAL PROCESSOR INSTRUCTIONS
NUMERIC SEQUENCE; MODELS 172, 173, AND 174 (Contd)

4. Formulas for instruction execution times (given in notes 5 through 8) give only approximate times. The following assumptions make the formulas useful only as best-case calculations.
   a. No offset in either the souce field or the destination field (C1=C2=zero).
   b. No memory conflicts from the rest of the system (peripheral processors [PPs] , second central processor [CP] ,or extended core storage [ECS] subsystem).
   c. No memory refresh conflicts or conflicts within the instruction.
   d. All words compare for instruction 467.
   e. 17 clock periods are required following compare/move instructions to complete next instruction word RNI.

NOTE

Formula term explanations for notes 5 through 8 are:

T = Time required for instruction execution in nanoseconds
L = Number of characters in the operation
N = Word count, calculated as L/10
X = Number of collate operations which require two memory references
Y = Number of collate operations which require one memory reference
Z = Number of collate operations which do not require memory references

5. Execution time for model 172:
   T = 1250 + 500N, for N greater than or equal to 5
   T = 1750 + 300N, for N = 1 through 4
   Execution time for models 173 or 174:
   T = 900 + 500N, for N greater than or equal to 5
   T = 1750 + 300N, for N = 1 through 4
6. Execution time for model 172, 173, or 174:
   T = 1000 + move direct instruction execution time (refer to note 5)
7. Execution time for model 172:
   T = 1150 + 725N, if N is even
   T = 1375 + 725N, if N is odd
   Execution time for model 173 or 174:
   T = 800 + 725N, if N is even
   T = 1025 + 725N, if N is odd
8. Execution time for model 172:
   T = 1150 + 725N + 1600X + 1350Y + 300Z, if N is even
   T = 1375 + 725N + 1600X + 1350Y + 300Z, if N is odd
   Execution time for model 173 or 174:
   T = 800 + 725N + 1600X + 1350Y + 300Z, if N is even
   T = 1025 + 725N + 1600X + 1350Y + 300Z, if N is odd
9. When used as error exit, 00 instructions take 52 clock periods.

TABLE 6. CENTRAL PROCESSOR INSTRUCTIONS
FUNCTIONAL GROUPS; MODELS 172, 173, AND 174

Instruction Code	Description	Execution Time		
		172	173/174	Notes
Program Stop and No Operation				
00xxx	Error exit to MA or program stop	-	-	9
460xx	No operation (pass)	10	3	-
Increment				
50ijK	Set Ai to (Aj) + K	-	-	2
51ijK	Set Ai to (Bj) + K	-	-	2
52ijK	Set Ai to (Xj) + K	-	-	2
53ijk	Set Ai to (Xj) + (Bk)	-	-	2
54ijk	Set Ai to (Aj) + (Bk)	-	-	2
55ijk	Set Ai to (Aj) - (Bk)	-	-	2
56ijk	Set Ai to (Bj) + (Bk)	-	-	2
57ijk	Set Ai to (Bj) - (Bk)	-	-	2
60ijK	Set Bi to (Aj) + K	11	5	-
61ijK	Set Bi to (Bj) + K	11	5	-
62ijK	Set Bi to (Xj) + K	11	5	-
63ijk	Set Bi to (Xj) + (Bk)	11	5	-
64ijk	Set Bi to (Aj) + (Bk)	11	5	-
65ijk	Set Bi to (Aj) - (Bk)	11	5	-
66ijk	Set Bi to (Bj) + (Bk)	11	5	-
67ijk	Set Bi to (Bj) - (Bk)	11	5	-
70ijK	Set Xi to (Aj) + K	12	6	-
71ijK	Set Xi to (Bj) + K	12	6	-
72ijK	Set Xi to (Xj) + K	12	6	-
73ijk	Set Xi to (Xj) + (Bk)	12	6	-
74ijk	Set Xi to (Aj) + (Bk)	12	6	-
75ijk	Set Xi to (Aj) - (Bk)	12	6	-
76ijk	Set Xi to (Bj) + (Bk)	12	6	-
77ijk	Set Xi to (Bj) - (Bk)	12	6	-

TABLE 6. CENTRAL PROCESSOR INSTRUCTIONS
FUNCTIONAL GROUPS; MODELS 172, 173, AND 174 (Contd)

Instruction Code	Description	Execution Time		
		172	173/174	Notes
Fixed Point Arithmetic				
36ijk	Integer sum of (Xj) and (Xk) to Xi	12	6	-
37ijk	Integer difference of (Xj) and (Xk) to Xi	12	6	-
47ixk	Population count of (Xk) to Xi	73	67	-
Logical				
10ijx	Transmit (Xj) to Xi	10	4	-
11ijk	Logical product of (Xj) and (Xk) to Xi	12	6	-
12ijk	Logical sum of (Xj) and (Xk) to Xi	12	6	-
13ijk	Logical difference of (Xj) and (Xk) to Xi	12	6	-
14ixk	Transmit complement of (Xk) to Xi	10	4	-
15ijk	Logical product of (Xj) and complement of (Xk) to Xi	12	6	-
16ijk	Logical sum of (Xj) and complement of (Xk) to Xi	12	6	-
17ijk	Logical difference of (Xj) and complement of (Xk) to Xi	12	6	-
Shift				
20ijk	Left shift (Xi) by jk	12	6	-
21ijk	Right shift (Xi) by jk	12	6	-
22ijk	Left shift (Xk) nominally (Bj) places to Xi	12	6	-
23ijk	Right shift (Xk) nominally (Bj) places to Xi	12	6	-

TABLE 6. CENTRAL PROCESSOR INSTRUCTIONS
FUNCTIONAL GROUPS; MODELS 172, 173, AND 174 (Contd)

Instruction Code	Description	Execution Time		
		172	173/174	Notes
24ijk	Normalize (Xk) to Xi and Bj	13	7	-
25ijk	Round normalize (Xk) to Xi and Bj	13	7	-
26ijk	Unpack (Xk) to Xi and Bj	12	6	-
27ijk	Pack (Xk) and (Bj) to Xi	12	6	-
43ijk	Form mask of jk bits to Xi	12	6	-
Floating-Point Arithmetic				
30ijk	Floating sum of (Xj) and (Xk) to Xi	17	11	-
31ijk	Floating difference of (Xj) and (Xk) to Xi	17	11	-
32ijk	Floating DP sum of (Xj) and (Xk) to Xi	17	11	-
33ijk	Floating DP difference of (Xj) and (Xk) to Xi	17	11	-
34ijk	Round floating sum of (Xj) and (Xk) to Xi	17	11	-
35ijk	Round floating difference of (Xj) and (Xk) to Xi	17	11	-
40ijk	Floating product of (Xj) and (Xk) to Xi	64	58	-
41ijk	Round floating product of (Xj) and (Xk) to Xi	64	58	-
42ijk	Floating DP product of (Xj) and (Xk) to Xi	64	58	-
44ijk	Floating divide (Xj) by (Xk) to Xi	64	58	-
45ijk	Round floating divide (Xj) by (Xk) to Xi	64	58	-

TABLE 6. CENTRAL PROCESSOR INSTRUCTIONS
FUNCTIONAL GROUPS; MODELS 172, 173, AND 174 (Contd)

Instruction Code	Description	Execution Time		
		172	173/174	Notes
Branch/Jump				
010xK	Return jump to K	36	29	-
013jK	Central exchange jump to (Bj) + K	49	42	-
02ixK	Jump to (Bi) + K	29	22	-
030jK	Branch to K if (Xj) = 0	29	22	1
031jK	Branch to K if (Xj) ≠ 0	29	22	1
032jK	Branch to K if (Xj) positive	29	22	1
033jK	Branch to K if (Xj) negative	29	22	1
034jK	Branch to K if (Xj) in range	29	22	1
035jK	Branch to K if (Xj) out of range	29	22	1
036jK	Branch to K if (Xj) definite	29	22	1
037jK	Branch to K if (Xj) indefinite	29	22	1
04ijK	Branch to K if (Bi) = (Bj)	29	22	1
05ijK	Branch to K if (Bi) ≠ (Bj)	29	22	1
06ijK	Branch to K if (Bi) ≥ (Bj)	29	22	1
07ijK	Branch to K if (Bi) < (Bj)	29	22	1
ECS Communication				
011jK	Block copy (Bj) + K words from ECS to CM	-	-	3
012jK	Block copy (Bj) + K words from CM to ECS	-	-	3

TABLE 6. CENTRAL PROCESSOR INSTRUCTIONS FUNCTIONAL GROUPS; MODELS 172, 173 AND 174 (Contd)

Instruction Code	Description	Execution Time		
		172	173/174	Notes
Compare/Move				
464jK	Move indirect	-	-	4, 6
465	Move direct	-	-	4, 5
466	Compare collated	-	-	4, 8
467	Compare uncollated	-	-	4, 7
Timing Notes: See applicable timing notes at the end of table 5.				

TABLE 7. CENTRAL PROCESSOR INSTRUCTIONS NUMERIC SEQUENCE; MODEL 175

Instruction Code	Description	Execution Time	
		Model 175	Notes
00xxx	Error edit to MA or program stop	-	-
010xK	Return jump to K	28	1, 2, 3
011jK	Block copy (Bj) + K words from ECS to CM	[(Bj) + K] 4	4, 5, 6, 7, 9
012jK	Block copy (Bj) + K words from CM to ECS	[(Bj) + K] 4	4, 5, 6, 7, 9
013jK	Central exchange jump to (Bj) + K (monitor flag set)	91	1, 2, 4
013xx	Central exchange jump to MA (monitor flag not set)	91	1, 2, 4

TABLE 7. CENTRAL PROCESSOR INSTRUCTIONS
NUMERIC SEQUENCE; MODEL 175 (Contd)

Instruction Code	Description	Execution Time	
		Model 175	Notes
02ixK	Jump to (Bi) + K	26	1, 2, 3, 8, 18
030jK	Branch to K if (Xj) = 0	26	1, 2, 3, 10, 11, 18
031jK	Branch to K if (Xj) ≠ 0	26	1, 2, 3, 10, 11, 18
032jK	Branch to K if (Xj) positive	26	1, 2, 3, 10, 11, 18
033jK	Branch to K if (Xj) negative	26	1, 2, 3, 10, 11, 18
034jK	Branch to K if (Xj) in range	26	1, 2, 3, 10, 11, 18
035jK	Branch to K if (Xj) out of range	26	1, 2, 3, 10, 11, 18
036jK	Branch to K if (Xj) definite	26	1, 2, 3, 10, 11, 18
037jK	Branch to K if (Xj) indefinte	26	1, 2, 3, 10, 11, 18
04ijK	Branch to K if (Bi) = (Bj)	26	1, 2, 3, 10, 11, 18
05ijK	Branch to K if (Bi) ≠ (Bj)	26	1, 2, 3, 10, 11, 18
06ijK	Branch to K if (Bi) ≥ (Bj)	26	1, 2, 3, 10, 11, 18
07ijK	Branch to K if (Bi) < (Bj)	26	1, 2, 3, 10, 11, 18

TABLE 7. CENTRAL PROCESSOR INSTRUCTIONS
NUMERIC SEQUENCE; MODEL 175 (Contd)

Instruction Code	Description	Execution Time	
		Model 175	Notes
10ijx	Transmit (Xj) to Xi	2	8, 12, 13
11ijk	Logical product of (Xj) and (Xk) to Xi	2	8, 12, 13
12ijk	Logical sum of (Xj) and (Xk) to Xi	2	8, 12, 13
13ijk	Logical difference of (Xj) and (Xk) to Xi	2	8, 12, 13
14ixk	Transmit complement of (Xk) to Xi	2	8, 12, 13
15ijk	Logical product of (Xj) and complement of (Xk) to Xi	2	8, 12, 13
16ijk	Logical sum of (Xj) and complement of (Xk) to Xi	2	8, 12, 13
17ijk	Logical difference of (Xj) and complement of (Xk) to Xi	2	8, 12, 13
20ijk	Left shift (Xi) by jk	2	8, 12, 13
21ijk	Right shift (Xi) by jk	2	8, 12, 13
22ijk	Left shift (Xk) nominally (Bj) places to Xi	2	8, 12, 13
23ijk	Right shift (Xk) nominally (Bj) places to Xi	2	8, 12, 13
24ijk	Normalize (Xk) to Xi and Bj	3	8, 12, 13
25ijk	Round normalize (Xk) to Xi and Bj	3	8, 12, 13
26ijk	Unpack (Xk) to Xi and Bj	2	8, 12, 13
27ijk	Pack (Xk) and (Bj) to Xi	2	8, 12, 13
30ijk	Floating sum of (Xj) and (Xk) to Xi	4	8, 12, 13
31ijk	Floating difference of (Xj) and (Xk) to Xi	4	8, 12, 13

TABLE 7. CENTRAL PROCESSOR INSTRUCTIONS
NUMERIC SEQUENCE; MODEL 175 (Contd)

Instruction Code	Description	Execution Time	
		Model 175	Notes
32ijk	Floating double-precision sum of (Xj) and (Xk) to Xi	4	8, 12, 13
33ijk	Floating double-precision difference of (Xj) and (Xk) to Xi	4	8, 12, 13
34ijk	Round floating sum of (Xj) and (Xk) to Xi	4	8, 12, 13
35ijk	Round floating difference of (Xj) and (Xk) to Xi	4	8, 12, 13
36ijk	Integer sum of (Xj) and (Xk) to Xi	2	8, 12, 13
37ijk	Integer difference of (Xj) and (Xk) to Xi	2	8, 12, 13
40ijk	Floating product of (Xj) and (Xk) to Xi	5	8, 12, 13, 14
41ijk	Round floating product of (Xj) and (Xk) to Xi	5	8, 12, 13, 14
42ijk	Floating double-precision product of (Xj) and (Xk) to Xi	5	8, 12, 13, 14
43ijk	Form mask of jk bits to Xi	2	8, 12, 13
44ijk	Floating divide (Xj) by (Xk) to Xi	20	8, 12, 13, 15
45ijk	Round floating divide (Xj) by (Xk) to Xi	20	8, 12, 13, 15
460xx	Pass	1	-
47ixk	Population count of (Xk) to Xi	2	8, 12, 13
50ijK	Set Ai to (Aj) + K	23	2, 3, 8, 16, 17, 18

TABLE 7. CENTRAL PROCESSOR INSTRUCTIONS
NUMERIC SEQUENCE; MODEL 175 (Contd)

Instruction Code	Description	Execution Time	
		Model 175	Notes
51ijK	Set Ai to (Bj) + K	23	2, 3, 8, 16, 17, 18
52ijK	Set Ai to (Xj) + K	23	2, 3, 8, 16, 17, 18
53ijk	Set Ai to (Xj) + (Bk)	23	2, 3, 8, 16, 17, 18
54ijk	Set Ai to (Aj) + (Bk)	23	2, 3, 8, 16, 17, 18
55ijk	Set Ai to (Aj) - (Bk)	23	2, 3, 8, 16, 17, 18
56ijk	Set Ai to (Bj) + (Bk)	23	2, 3, 8, 16, 17, 18
57ijk	Set Ai to (Bj) - (Bk)	23	2, 3, 8, 16, 17, 18
60ijK	Set Bi to (Aj) + K	2	8, 12, 13
61ijK	Set Bi to (Bj) + K	2	8, 12, 13
62ijK	Set Bi to (Xj) + K	2	8, 12, 13
63ijk	Set Bi to (Xj) + (Bk)	2	8, 12, 13
64ijk	Set Bi to (Aj) + (Bk)	2	8, 12, 13
65ijk	Set Bi to (Aj) - (Bk)	2	8, 12, 13
66ijk	Set Bi to (Bj) + (Bk)	2	8, 12, 13
67ijk	Set Bi to (Bj) - (Bk)	2	8, 12, 13
70ijK	Set Xi to (Aj) + K	2	8, 12, 13
71ijK	Set Xi to (Bj) + K	2	8, 12, 13
72ijK	Set Xi to (Xj) + K	2	8, 12, 13
73ijk	Set Xi to (Xj) + 9Bk)	2	8, 12, 13
74ijk	Set Xi to (Aj) + (Bk)	2	8, 12, 13
75ijk	Set Xi to (Aj) - (Bk)	2	8, 12, 13
76ijk	Set Xi to (Bj) + (Bk)	2	8, 12, 13
77ijk	Set Xi to (Bj) - (Bk)	2	8, 12, 13

TABLE 7. CENTRAL PROCESSOR INSTRUCTIONS NUMERIC SEQUENCE; MODEL 175 (Contd)

Timing Notes:

0. Execution times in this table are given in clock periods. Model 175 has a 25-nanosecond clock period.
1. All previous instruction fetches are completed.
2. No CM conflicts or SAS backup caused by CM conflicts exist.
3. No PPS request occurs.
4. All operating registers are free.
5. ECS is not busy.
6. All ECS banks have completed previously initiated read/write cycles.
7. Time does not include startup time.
8. The requested operating register(s) is free.
9. Time assumes no ECS record gaps.
10. If the address is in the IAS, the execution time is 3 clock periods.
11. If the branch conditions are not met, the execution time is 2 clock periods.
12. The requested destination register(s) input data path is free during the required clock period.
13. After the instruction has issued to the functional unit, no further delay is possible.
14. The multiple unit is free.
15. The divide unit is free.
16. If i = 0, execution time is 2 clock periods, and no storage reference is required.
    If i = 1 through 5, execution time is 23 clock periods, and a storage reference is required.
    If i = 6 or 7, execution time is 2 clock periods, and a storage reference continues after instruction execution.
17. After the instruction has issued to the increment unit, no further delays are possible in the delivery of data to the Ai register. However, CM conflicts may delay the resulting storage reference.
18. If memory enable is present when the address is gated into SAS, additional clock period is required.

TABLE 8. CENTRAL PROCESSOR INSTRUCTIONS
FUNCTIONAL GROUPS; MODEL 175

Instruction Code	Description	Execution Time	
		Model 175	Notes
Program Stop and No Operation			
00xxx	Error exit to MA or program stop	-	-
460xx	Pass	1	-
Increment			
50ijK	Set Ai to (Aj) + K	23	2, 3, 8, 16, 17, 18
51ijK	Set Ai to (Bj) + K	23	2, 3, 8, 16, 17, 18
52ijK	Set Ai to (Xj) + K	23	2, 3, 8, 16, 17, 18
53ijk	Set Ai to (Xj) + (Bk)	23	2, 3, 8, 16, 17, 18
54ijk	Set Ai to (Aj) + (Bk)	23	2, 3, 8, 16, 17, 18
55ijk	Set Ai to (Aj) - (Bk)	23	2, 3, 8, 16, 17, 18
56ijk	Set Ai to (Bj) + (Bk)	23	2, 3, 8, 16, 17, 18
57ijk	Set Ai to (Bj) - (Bk)	23	2, 3, 8, 16, 17, 18
60ijK	Set Bi to (Aj) + K	2	8, 12, 13
61ijK	Set Bi to (Bj) + K	2	8, 12, 13
62ijK	Set Bi to (Xj) + K	2	8, 12, 13
63ijk	Set Bi to (Xj) + (Bk)	2	8, 12, 13
64ijk	Set Bi to (Aj) + (Bk)	2	8, 12, 13
65ijk	Set Bi to (Aj) - (Bk)	2	8, 12, 13
66ijk	Set Bi to (Bj) + (Bk)	2	8, 12, 13
67ijk	Set Bi to (Bj) - (Bk)	2	8, 12, 13
70ijK	Set Xi to (Aj) + K	2	8, 12, 13
71ijK	Set Xi to (Bj) + K	2	8, 12, 13

TABLE 8. CENTRAL PROCESSOR INSTRUCTIONS
FUNCTIONAL GROUPS; MODEL 175 (Contd)

Instruction Code	Description	Execution Time	
		Model 175	Notes
72ijK	Set Xi to (Xj) + K	2	8, 12, 13
73ijk	Set Xi to (Xj) + (Bk)	2	8, 12, 13
74ijk	Set Xi to (Aj) + (Bk)	2	8, 12, 13
75ijk	Set Xi to (Aj) - (Bk)	2	8, 12, 13
76ijk	Set Xi to (Bj) + (Bk)	2	8, 12, 13
77ijk	Set Xi to (Bj) - (Bk)	2	8, 12, 13
Fixed Point Arithmetic			
36ijk	Integer sum of (Xj) and (Xk) to Xi	2	8, 12, 13
37ijk	Integer difference of (Xj) and (Xk) to Xi	2	8, 12, 13
47ixk	Population count of (Xk) to Xi	2	8, 12, 13
Logical			
10ijx	Transmit (Xj) to Xi	2	8, 12, 13
11ijk	Logical product of (Xj) and (Xk) to Xi	2	8, 12, 13
12ijk	Logical sum of (Xj) and (Xk) to Xi	2	8, 12, 13
13ijk	Logical difference of (Xj) and (Xk) to Xi	2	8, 12, 13
14ixk	Transmit complement of (Xk) to Xi	2	8, 12, 13
15ijk	Logical product of (Xj) and complement of (Xk) to Xi	2	8, 12, 13
16ijk	Logical sum of (Xj) and complement of (Xk) to Xi	2	8, 12, 13
17ijk	Logical difference of (Xj) and complement of (Xk) to Xi	2	8, 12, 13

TABLE 8. CENTRAL PROCESSOR INSTRUCTIONS FUNCTIONAL GROUPS; MODEL 175 (Contd)

Instruction Code	Description	Execution Time	
		Model 175	Notes
Shift			
20ijk	Left shift (Xi) by jk	2	8, 12, 13
21ijk	Right shift (Xi) by jk	2	8, 12, 13
22ijk	Left shift (Xk) nominally (Bj) places to Xi	2	8, 12, 13
23ijk	Right shift (Xk) nominally (Bj) places to Xi	2	8, 12, 13
24ijk	Normalize (Xk) to Xi and Bj	3	8, 12, 13
25ijk	Round normalize (Xk) to Xi and Bj	3	8, 12, 13
26ijk	Unpack (Xk) to Xi and Bj	2	8, 12, 13
27ijk	Pack (Xk) and (Bj) to Xi	2	8, 12, 13
43ijk	Form mask of jk bits to Xi	2	8, 12, 13
Floating-Point Arithmetic			
30ijk	Floating sum of (Xj) and (Xk) to Xi	4	8, 12, 13
31ijk	Floating difference of (Xj) and (Xk) to Xi	4	8, 12, 13
32ijk	Floating double-precision sum of (Xj) and (Xk) to Xi	4	8, 12, 13
33ijk	Floating double-precision difference of (Xj) and (Xk) to Xi	4	8, 12, 13
34ijk	Round floating sum of (Xj) and (Xk) to Xi	4	8, 12, 13
35ijk	Round floating difference of (Xj) and (Xk) to Xi	4	8, 12, 13
40ijk	Floating product of (Xj) and (Xk) to Xi	5	8, 12, 13, 14

TABLE 8. CENTRAL PROCESSOR INSTRUCTIONS FUNCTIONAL GROUPS; MODEL 175 (Contd)

Instruction Code	Description	Execution Time	
		Model 175	Notes
41ijk	Round floating product of (Xj) and (Xk) to Xi	5	8, 12, 13, 14
42ijk	Floating double-precision product of (Xj) and (Xk) to Xi	5	8, 12, 13, 14
44ijk	Floating divide (Xj) by (Xk) to Xi	20	8, 12, 13, 15
45ijk	Round floating divide (Xj) by (Xk) to Xi	20	8, 12, 13, 15
Branch/Jump			
010xK	Return jump to K	28	1, 2, 3
013jK	Central exchange jump to (Bj) + K (monitor flag set)	91	1, 2, 4
013xx	Central exchange jump to MA (monitor flag not set)	91	1, 2, 4
02ixK	Jump to (Bi) + K	26	1, 3, 3, 8, 18
030jK	Branch to K if (Xj) = 0	26	1, 2, 3, 10, 11, 18
031jK	Branch to K if (Xj) ≠ 0	26	1, 2, 3, 10, 11, 18
032jK	Branch to K if (Xj) positive	26	1, 2, 3, 10, 11, 18
033jK	Branch to K if (Xj) negative	26	1, 2, 3, 10, 11, 18
034jK	Branch to K if (Xj) in range	26	1, 2, 3, 10, 11, 18

TABLE 8. CENTRAL PROCESSOR INSTRUCTIONS
FUNCTIONAL GROUPS; MODEL 175 (Contd)

Instruction Code	Description	Execution Time	
		Model 175	Notes
035jK	Branch to K if (Xj) out of range	26	1, 2, 3, 10, 11, 18
036jK	Branch to K if (Xj) definite	26	1, 2, 3, 10, 11, 18
037jK	Branch to K if (Xj) indefinite	26	1, 2, 3, 10, 11, 18
04ijK	Branch to K if (Bi) = (Bj)	26	1, 2, 3, 10, 11, 18
05ijK	Branch to K if (Bi) ≠ (Bj)	26	1, 2, 3, 10, 11, 18
06ijK	Branch to K if (Bi) ≥ (Bj)	26	1, 2, 3, 10, 11, 18
07ijK	Branch to K if (Bi) < (Bj)	26	1, 2, 3, 10, 11, 18
ECS Communication			
011jK	Block copy (Bj) + K words from ECS to CM	[(Bj) + K] 4	4, 5, 6, 7, 9
012jK	Block copy (Bj) + K words from CM to ECS	[(Bj) + K] 4	4, 5, 6, 7, 9

Timing Notes:

See applicable timing notes at the end of table 7.

EXTERNAL FUNCTION CODES AND STATUS RESPONSES

STATUS/CONTROL REGISTERS

DESCRIPTOR WORD FORMAT

The descriptor word format shown in figure 5 has 12 bits. I defines a word or bit address and a function code; bit 8 is no used.

Function Code	Description
0	Read word
1	Test bit
2	Clear bit
3	Test/clear bit
4	Set bit
5	Test/set bit
6	Clear all bits
7	Test error bits

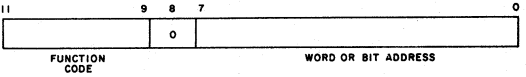


Figure 5. Status/Control Descriptor Word Format

BIT ASSIGNMENTS

Table 9 lists the bit assignments. The significance of eac column is as follows:

Column	Description
Word	Register word listed in octal
Bit	Register bit listed in decimal and in octal
Model	CDC CYBER 170 models that the bit is applicable to. All = all models; 2=172; 3=173; 4=174; 5=175
S/C	S = Status bit; C = Control bit
Function	Applicable programming functions: TE = Read, test, clear, test/clear, set, test/set, clear all, and test error (status bit included in test error) R = Read D = Read, test, clear, test/clear, test, test/set, and clear all Blank = Read, test, clear, test/clear, set test/set, and clear all
Notes	Applicable notes are at the end of the table.

The channel 36 S/C register is available for 20 PPU systems and is applicable to bits 0, 6, 7, 12 - 35, 37, 38, 60 - 83, 85, 95, 120 - 126, 174, 175, 188, and 189.

TABLE 9. STATUS/CONTROL REGISTER BIT ASSIGNMENTS

Word (8)	Bit No. (10)	Bit No. (8)	Description	Model	S/C	Function	Notes
0	0	0	Read pyramid parity error	All	S	TE	-
	1	1	CSU-0 address parity error	All	S	TE	-
	2	2	CSU-1 address parity error	All	S	TE	-
	3	3	SECDED error	All	S	TE	1
	4	4	Not used	-	-	-	-
	5	5	CMC parity error	All	S	TE	2
	6	6	PE on data received from external channel	All	S	TE	-
	7	7	PE on data transmitted from external PP	All	S	TE	-
	8	10	CSU-0 fault	All	S	TE	-
	9	11	CSU-1 fault	All	S	TE	-
	10	12	Error in second PPS	All	S	TE	3
	11	13	ECS error	All	S	TE	4
1	12	14	CP-0 P register parity error	All	S	TE	-
	13	15	CP-1 register parity error	4	S	TE	-
	14	16	PP0 memory parity error	All	S	TE	-
	15	17	PP1 memory parity error	All	S	TE	-
	16	20	PP2 memory parity error	All	S	TE	-
	17	21	PP3 memory parity error	All	S	TE	-
	18	22	PP4 memory parity error	All	S	TE	-
	19	23	PP5 memory parity error	All	S	TE	-
	20	24	PP6 memory parity error	All	S	TE	-

TABLE 9. STATUS/CONTROL REGISTER
BIT ASSIGNMENTS (Contd)

Word (8)	Bit No. (10)	Bit No. (8)	Description	Model	S/C	Function	Notes
	21	25	PP7 memory parity error	All	S	TE	-
	22	26	PP8 memory parity error	All	S	TE	-
	23	27	PP9 memory parity error	All	S	TE	-
2	24	30	Channel 0 parity error	All	S	TE	5
	25	31	Channel 1 parity error	All	S	TE	5
	26	32	Channel 2 parity error	All	S	TE	5
	27	33	Channel 3 parity error	All	S	TE	5
	28	34	Channel 4 parity error	All	S	TE	5
	29	35	Channel 5 parity error	All	S	TE	5
	30	36	Channel 6 parity error	All	S	TE	5
	31	37	Channel 7 parity error	All	S	TE	5
	32	40	Channel 10 parity error	All	S	TE	5
	33	41	Channel 11 parity error	All	S	TE	5
	34	42	Channel 12 parity error	All	S	TE	5
	35	43	Channel 13 parity error	All	S	TE	5
3	36	44	Mains power failure	All	S	TE	6
	37	45	Shutdown imminent	All	S	TE	6
	38	46	Not used	-	-	TE	-
	39	47	Not used	-	-	TE	-
	40	50	Syndrome bit 0	All	S	R	7

TABLE 9. STATUS/CONTROL REGISTER
BIT ASSIGNMENTS (Contd)

Word (8)	Bit No. (10)	Bit No. (8)	Description	Model	S/C	Function	Notes
	41	51	Syndrome bit 1	All	S	R	7
	42	52	Syndrome bit 2	All	S	R	7
	43	53	Syndrome bit 3	All	S	R	7
	44	54	Syndrome bit 4	All	S	R	7
	45	55	Syndrome bit 5	All	S	R	7
	46	56	Syndrome bit 6	All	S	R	7
	47	57	Syndrome bit 7	All	S	R	7
4	48	60	Syndrome address bit 0	All	S	R	7
	49	61	Syndrome address bit 1	All	S	R	7
	50	62	Syndrome address bit 2	All	S	R	7
	51	63	Syndrome address bit 16	All	S	R	7
	52	64	Syndrome address bit 17	All	S	R	7
	53	65	Syndrome address bit 3	All	S	R	7
	54	66	Parity error port code bit 0	All	S	R	8
	55	67	Parity error port code bit 1	All	S	R	8
	56	70	Breakpoint port code bit 0	All	S	R	9
	57	71	Breakpoint port code bit 1	All	S	R	9
	58	72	Breakpoint function code bit 0	All	S	R	9
	59	73	Breakpoint function code bit 1	All	S	R	9
5	60	74	PPS P register bit 0	All	S	R	10
	61	75	PPS P register bit 1	All	S	R	10

TABLE 9. STATUS/CONTROL REGISTER
BIT ASSIGNMENTS (Contd)

Word (8)	Bit No. (10)	Bit No. (8)	Description	Model	S/C	Function	Notes
	62	76	PPS P register bit 2	All	S	R	10
	63	77	PPS P register bit 3	All	S	R	10
	64	100	PPS P register bit 4	All	S	R	10
	65	101	PPS P register bit 5	All	S	R	10
	66	102	PPS P register bit 6	All	S	R	10
	67	103	PPS P register bit 7	All	S	R	10
	68	104	PPS P register bit 8	All	S	R	10
	69	105	PPS P register bit 9	All	S	R	10
	70	106	PPS P register bit 10	All	S	R	10
	71	107	PPS P register bit 11	All	S	R	10
6	72	110	PP code bit 0	All	S	R	10
	73	111	PP code bit 1	All	S	R	10
	74	112	PP code bit 2	All	S	R	10
	75	113	PP code bit 3	All	S	R	10
	76	114	PPS breakpoint bit	All	S	-	-
	77	115	CMC breakpoint match	All	S	-	11
	78	116	Clear central memory busy	All	C	-	12
	79	117	Set C5 full	All	C	-	13
	80	120	Force zero parity on channels	All	C	D	13
	81	121	Force zero parity on PPM	All	C	D	-

TABLE 9. STATUS/CONTROL REGISTER
BIT ASSIGNMENTS (Contd)

Word (8)	Bit No. (10)	Bit No. (8)	Description	Model	S/C	Function	Notes
	82	122	Not used	-	-	-	-
	83	123	PPS breakpoint mode select	All	C	D	10
7	84	124	All PPs 500-nanosecond major cycle	All	C	D	14
	85	125	Inhibit PPS request to CMC	All	C	D	-
	86	126	Not used	-	-	-	-
	87	127	Not used	-	-	-	-
	88	130	Not used	-	-	-	-
	89	131	Not used	-	-	-	-
	90	132	Not used	-	-	-	-
	91	133	Not used	-	-	-	-
	92	134	Not used	-	-	-	-
	93	135	Not used	-	-	-	-
	94	136	Not used	-	-	-	-
	95	137	Stop on PPM parity error	All	C	D	15
10	96	140	Breakpoint address bit 0	All	C	-	16
	97	141	Breakpoint address bit 1	All	C	-	16
	98	142	Breakpoint address bit 2	All	C	-	16
	99	143	Breakpoint address bit 3	All	C	-	16
	100	144	Breakpoint address bit 4	All	C	-	16
	101	145	Breakpoint address bit 5	All	C	-	16
	102	146	Breakpoint address bit 6	All	C	-	16
	103	147	Breakpoint address bit 7	All	C	-	16

TABLE 9. STATUS/CONTROL REGISTER
BIT ASSIGNMENTS (Contd)

Word (8)	Bit No. (10)	Bit No. (8)	Description	Model	S/C	Function	Notes
	104	150	Breakpoint address bit 8	All	C	-	16
	105	151	Breakpoint address bit 9	All	C	-	16
	106	152	Breakpoint address bit 10	All	C	-	16
	107	153	Breakpoint address bit 11	All	C	-	16
11	108	154	Breakpoint address bit 12	All	C	-	-
	109	155	Breakpoint address bit 13	All	C	-	-
	110	156	Breakpoint address bit 14	All	C	-	-
	111	157	Breakpoint address bit 15	All	C	-	-
	112	160	Breakpoint address bit 16	All	C	-	-
	113	161	Breakpoint address bit 17	All	C	-	-
	114	162	Breakpoint condition code bit 18	All	C	-	17
	115	163	Breakpoint condition code bit 19	All	C	-	17
	116	164	Breakpoint condition code bit 20	All	C	-	17
	117	165	Breakpoint condition code bit 21	All	C	-	17
	118	166	Inhibit single error report	All	C	-	29
	119	167	Not used	-	-	-	-
12	120	170	PP select code bit 0	All	C	D	18
	121	171	PP select code bit 1	All	C	D	18
	122	172	PP select code bit 2	All	C	D	18
	123	173	PP select code bit 3	All	C	D	18

TABLE 9. STATUS/CONTROL REGISTER
BIT ASSIGNMENTS (Contd)

Word (8)	Bit No. (10)	Bit No. (8)	Description	Model	S/C	Function	Notes
	124	174	PP select auto/ manual mode	All	C	D	19
	125	175	Force exit on selected PP	All	C	D	13
	126	176	Force PP deadstart on selected PP	All	C	D	20
	127	177	CSU, CMC, CPU master clear	All	C	D	-
	128	200	Force zero SECDED code and parity CMC to CM	All	C	-	-
	129	201	Force zero address parity CMC to CM	All	C	-	-
	130	202	Not used	-	-	-	-
	131	203	Not used	-	-	-	-
13	132	204	Force zero parity code 0	All	C	-	21
	133	205	Force zero parity code 1	All	C	-	21
	134	206	Refresh margin slow	All	C	-	-
	135	207	Refresh margin fast	All	C	-	-
	136	210	ECS transfer error code 0	All	S	R	4
	137	211	ECS transfer error code 1	All	S	R	4
	138	212	ECS transfer error code 2	All	S	R	4
	139	213	CMC address/data parity error	All	S	R	-
	140	214	Not used	-	-	-	-
	141	215	Clock frequency magnitude 0	All	C	D	22
	142	216	Clock frequency magnitude 1	All	C	D	22
	143	217	Clock frequency slow/fast	All	C	D	23

TABLE 9. STATUS/CONTROL REGISTER
BIT ASSIGNMENTS (Contd)

Word (8)	Bit No. (10)	Bit No. (8)	Description	Model	S/C	Function	Notes
14	144	220	RVM address bit 0 status	5	S	-	24
	145	221	RVM address bit 1 status	5	S	-	24
	146	222	RVM address bit 2 status	5	S	-	24
	147	223	RVM address bit 3 status	5	S	-	24
	148	224	RVM address bit 4 status	5	S	-	24
	149	225	RVM address bit 5 status	5	S	-	24
	150	226	RVM hi/lo	5	S	-	25
	151	227	RVM all/one	5	S	-	26
	152	230	Clock pulse width narrow	5	C	-	-
	153	231	Clock pulse width wide	5	C	-	-
	154	232	Select hi/lo RVM	5	C	-	25
	155	233	Select all/one RVM	5	C	-	26
15	156	234	RVM quadrant 0 select	5	C	-	-
	157	235	RVM quadrant 1 select	5	C	-	-
	158	236	RVM quadrant 2 select	5	C	-	-
	159	237	RVM quadrant 3 select	5	C	-	-
	160	240	RVM quadrant 4 select	5	C	-	-
	161	241	RVM quadrant 5 select	5	C	-	-
	162	242	RVM quadrant 6 select	5	C	-	-
	163	243	RVM quadrant 7 select	5	C	-	-

TABLE 9. STATUS/CONTROL REGISTER
BIT ASSIGNMENTS (Contd)

Word (8)	Bit No. (10)	Bit No. (8)	Description	Model	S/C	Function	Notes
	164	244	RVM quadrant 8 select	5	C	-	-
	165	245	RVM quadrant 9 select	5	C	-	-
	166	246	RVM quadrant 10 select	5	C	-	-
	167	247	RVM quadrant 11 select	5	C	-	-
16	168	250	RVM module address bit 0	5	C	-	-
	169	251	RVM module address bit 1	5	C	-	-
	170	252	RVM module address bit 2	5	C	-	-
	171	253	RVM module address bit 3	5	C	-	-
	172	254	RVM module address bit 4	5	C	-	-
	173	255	RVM module address bit 5	5	C	-	-
	174	256	PPS to CMC zero address parity	All	C	-	-
	175	257	PPS to CMC zero data parity	All	C	-	-
	176	260	Not used	-	-	-	-
	177	261	Not used	-	-	-	-
	178	262	Not used	-	-	-	-
	179	263	Not used	-	-	-	-
17	180	264	Not used	-	-	-	-
	181	265	Not used	-	-	-	-
	182	266	Not used	-	-	-	-
	183	267	Double error	All	S	-	-
	184	270	CP-0 to CMC zero address parity	2,3,4	C	-	-

TABLE 9. STATUS/CONTROL REGISTER BIT ASSIGNMENTS (Contd)

Word (8)	Bit No. (10)	Bit No. (8)	Description	Model	S/C	Function	Notes
	185	271	CP-1 to CMC zero address parity	4	C	-	-
	186	272	CP-0 to CMC zero data parity	2,3,4	C	-	-
	187	273	CP-1 to CMC zero data parity	4	C	-	-
	188	274	Software flag 0	All	C	-	27
	189	275	Software flag 1	All	C	-	27
	190	276	Not used	-	-	-	-
	191	277	Not used	-	-	-	-
20	192	300	CP-0 stopped	All	S	R	-
	193	301	CP-1 stopped	4	S	R	-
	194	302	ECS in progress flag	All	S	R	-
	195	303	Monitor flag CP-0	All	S	R	-
	196	304	Monitor flag CP-1	4	S	R	-
	197	305	PPM reconfiguration bit 0	All	S	R	-
	198	306	PPM reconfiguration bit 1	All	S	R	-
	199	307	PPM reconfiguration bit 2	All	S	R	-
	200	310	PPM reconfiguration bit 3	All	S	R	-
	201	311	PPM reconfiguration bit 4	All	S	R	28
	202	312	Not used	-	-	-	-
	203	313	Not used	-	-	-	-

TABLE 9. STATUS/CONTROL REGISTER BIT ASSIGNMENTS (Contd)

Notes:

1. Loads and locks bits 40 through 53
2. Loads and locks bits 54, 55, and 139
3. Tests 0 through 39 of PPS-1
4. Bit 11 loads and locks bits 136 through 138
5. For channel 36, channel numbers 20 through 33 (octal) apply
6. Power/environmental abnormal condition
7. Loaded and locked by bit 3
8. From CMC, identifies port, loaded and locked by bit 5
9. Loaded and locked by bit 77
10. If bit 83 is clear, bits 60 through 71 display P of the PPU selected by bits 120 through 123, and bits 72 through 75 display selected PP. If bit 83 is set, the content of the P register is latched and retained on every CM breakpoint bit. If bit 76 sets when bit 83 is set, bits 60 through 75 are held until bit 76 is cleared.
11. Loads and locks bits 56 through 59
12. Clear busy FF in PPS
13. One-shot operation
14. Controls PPS-0 and PPS-1
15. Applies to all PPUs
16. Absolute 18-bit address (bits 96 through 113 are sent to and used by CMC to establish a breakpoint address when bits 116 and/or 117 are set)
17. Select function RD/WT/RNI or all three to CMC for port selection
18. Select 1 of 10 PPUs for forced exit, deadstart, or display
19. Clear = manual
20. Set forces deadstart (PPU remains in deadstart condition until bit is cleared)
21. ECS coupler
22. Bits 141 through 143 are coded bits for selecting clock margins
23. Clear = fast
24. Indicates module with reference voltage margins (RVM) applied
25. Clear = lo
26. Clear = one
27. Diagnostic aids
28. PPS select
29. Single errors are not recorded in SCR when set

DISPLAY STATION CC545

KEYBOARD

A PP must transmit a one-word function code (7020_8) to request data from the keyboard of the display station. The code prepares the display controller for an input operation. The PP then checks for an active channel and receives one character from the keyboard. This character is entered as the lower six bits of the word. The upper bits are cleared. There is no status report by the keyboard. Table 10 lists the keyboard character codes.

TABLE 10. DISPLAY STATION CHARACTER CODES

6-Bit Octal Code	Display Character	Keyboard Input
00	Space	No Data
01	A	A
02	B	B
03	C	C
04	D	D
05	E	E
06	F	F
07	G	G
10	H	H
11	I	I
12	J	J
13	K	K
14	L	L
15	M	M
16	N	N
17	O	O
20	P	P
21	Q	Q
22	R	R
23	S	S
24	T	T
25	U	U

TABLE 10. DISPLAY STATION CHARACTER CODES
(Contd)

6-Bit Octal Code	Display Character	Keyboard Input
26	V	V
27	W	W
30	X	X
31	Y	Y
32	Z	Z
33	0	0
34	1	1
35	2	2
36	3	3
37	4	4
40	5	5
41	6	6
42	7	7
43	8	8
44	9	9
45	+	+
46	-	-
47	*	*
50	/	/
51	(	(
52	)	)
53	Not Used	Clear (Note 1)
54	=	=
55	Not Used	Not Used (Note 2)
56	, (Comma)	, (Comma)
57	. (Period)	. (Period)
60	Not Used	CR (Carriage Return)
61	Not Used	BKSP (Backspace)
62	Not Used	Space (Space Bar)

Notes: 1. Eleventh key on top row.
2. Thirteenth key on top row.

DATA DISPLAY

The data display can be alphanumeric (character mode) or graphic (dot mode).

Character Mode

Large, medium, and small characters are provided; 16, 32, and 64 characters per line, respectively. Table 10 lists the display character codes.

Dot Mode

Display dots are positioned by X and Y coordinates. The X coordinates position dots horizontally; Y coordinates position dots vertically and unblank the CRT for each dot.

Codes

A single function word is transmitted to select the presentation, mode, and character size (character mode only). Figure 6 illustrates the function word format. The word following the function word specifies the starting coordinates for the display (for either mode). Figure 7 illustrates the coordinate data word. In character mode, the subsequent words are display character codes. Figure 8 illustrates the character data word.

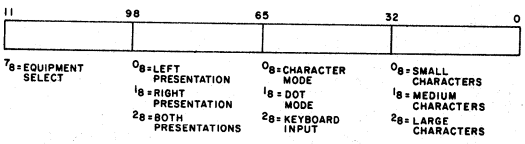
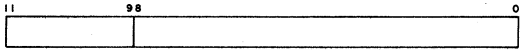


Figure 6. Display Station Function Word Format



6_{8} = X
7_{8} = Y

NOTE:
IN DOT MODE, EACH Y COORDINATE TRANSMITTED FORCES A DOT DISPLAY

Figure 7. Display Station Coordinate Data Word

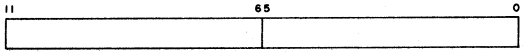


Figure 8. Display Station Character Data Word

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