MEMO

CONTROL DATA CORPORATION

TO:	LOCATION:	FROM	EXT.	LOCATION:
J. L. Chapman	ARH229	E. H. Michehl	2669	ARH293

SUBJECT: CYBER 180 A0/R, Rev. C

DATE: 6/12/78

Attached is the NPP-approved CYBER 180 Architectural Objectives, Revision C. This document should be reviewed against existing DR's per the BCCB direction memo of 6/6/78.

The three change summaries attached outline changes in content between Revision B (Rev. 9) and Revision C (Rev. 12). Please submit your updated statements of compliance to the NPP Program Office as soon as possible.

E. H. Michehl
Director
AD&C

paj

Attachments

JUN 20 REC'D

AA187 REV. 7/78 PRINTED IN U.S.A.

MEMO

CONTROL DATA CORPORATION

TO:	LOCATION:	FROM	EXT.	LOCATION:
Distribution		Baseline Change Control Board		ARH0PS

SUBJECT: Effect of A0/R Revisions on Existing DR's

DATE: 6/6/78

When Revision C of the CYBER 180 A0/R is approved by NPP, the following procedure applies.

All projects operating against an existing CYBER 180 DR will carefully review the revised A0/R and submit a new statement of compliance to the CYBER 180 Program Office within 10 working days of A0/R distribution.

H. N. Frazier 6/7/78
Vice President
Computer Programming Division

L. E. Jodsaas
Vice President
New Product Program

M. J. McHale 6/8/78
Vice President
Computer Development

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CHANGES - REV. 11 TO REV. 12

Section	
1.3	Clarifies S1/THETA project objectives without compromising product line objectives.
2.0	No. 15 - a reference for security design objectives.
3.2.6.1	Clarifies between sensing and recording in the power system. More precision on which disks are brought up by single button power-on. "Quietizing" dropped as a generally required option. Feature matrix moved to section 11.1.5.
3.2.6.2	Auto Power Recovery is to require a 2.5 second ride-through MG Set.
3.2.6.4	Further definition of short and long warnings.
3.3.4	5) - Same function, less implementation detail. 10) - Clearer terminology. 19) - Eliminates redundant information.
3.3.8.2	Clarification of intent relative to compilers and compiler users.
3.4.1	O.S. independence made a general product set requirement.
3.4.2.1	In the matrix - added WPASCAL (Wirth PASCAL). 17) - Corrects compatibility objective of ALGOL 60 relative to ALGOL 68
3.4.3.2	Classification "medium, large and very large" revised. O.S. independence requirement moved to Section 3.4.1.
3.5	CYBER 180 will comply with basis DoD security requirements.
3.8	Maximum terminal capacity (logical) has been expanded.
5.2.2.1	The Basic O.S. is also prohibited from source code release for system software security considerations.
6.0	Dual State link is a 170/180 feature only. MMF shared peripherals restricted to RMS and Front-ends. User validation phased over 2 releases. Accounting phased over 2 releases. Tasking added to R1. Job Dependency to R2. 180 state Basic tape I/O and volumes to R1. Online maintenance of tape in R1 via C170. Index Sequential to R1. All of DBMS phased.

Section	
7.4.4.9	Two sentences were removed as irrelevant: 1. Restricting objectives to R1 2. Comparative CPU times.
7.4.4.10.1	Paragraph removed - not directly related to objectives.
7.5.1	BASIC speeds and benchmarks redefined.
8.2.3	Will support CYBERAMA.
8.4	Clarification.
8.4.7	MTTR average <u>includes</u> necessary trips for parts. Clarify assumption regarding degraded interruption.
8.6.4	Clarifies critical PSR status of initial release.
9.1	DoD Security Compliance is no longer excluded.
10.4.1	Clarification, modification for performance is encouraged.
10.4.2	Clarification of intent, remote maintenance interfaces are standard, the subsystem remains to be defined.
11.1.2	2 port MUX is part of the basic mainframe in both C170 and C180 state.
11.1.5	MG Set Options reduced to eliminate proliferation of development projects.
11.2	Maintenance cost objectives stated in dollars and %.
11.4.2	Minimum THETA configuration is 4MB. Maximum defined real memory now is 32MB.
12.3.1	Clarifies future terminals intent and relation to value added networks.
12.4.2-3	System Power cost changes.
12.5	Previous forecasts have been dropped.
12.7.2	Schedul clarification.
12.7.2.2.5	Some items delayed until 6/79.

Change Summary - CYBER 180 A0/R Second Draft of Rev. C (Rev. 11)
Rev 10 to Rev 11

Section	
1.3	Major Objectives - The specific areas of emphasis for S1 and THETA have been noted along with potential for impact on priority trade-offs.
1.3.1	The release dates for S1 have been clarified.
1.3.3	The base for performance measurement remains CYBER 73.
2.0	Reference 10 has been updated and reference 15 added.
3.1.1.1	Per request of Engineering the terminology for input/output unit has been revised.
3.1.1.2	The probable support of a two IOU configuration has been noted and a reference to varying memory capacities added.
3.1.1.4	Minor wording changes to reduce the confusion regarding common memory vs. shared memory (the latter is low cost communication medium for dual mainframe configurations only). All other multi-mainframe configurations are independent of requirements for a common memory and the term has been dropped.
3.1.2	Batch processing has been dropped in priority and further clarification on the relationship between transaction processing and time-sharing has been made.
3.2.4	c) Clarifies the S1 channel restrictions f) defines the 2 port console multiplexor and reserves 1 port for remote hardware and software maintenance.
3.2.4.2	Clarifies the PP's restricted accessing to central memory as a software restriction. Clarifies PP software's relationship to controlware.
3.2.4.3	Adds requirement for controllers to interface to the configuration environment monitor.
3.2.4.4	Defines the minimum functional characteristics of the basic operator control console, beyond which operating system or diagnostic software cannot use. Clarifies the role of the CYBER 170 CC545 console with regard to these requirements (the role of the CC545 in C180 systems remains weekly defined.)
3.2.6.1	Temperature monitoring and power control need not be "internal" to a mainframe. Clarifies the use of the dewpoint recorder on 180 systems. Revises the power requirement for multi-mainframe configurations to greater power supply availability for shared elements. Clarifies motor generator sets options.

Section	
3.2.6.2	Minor wording changes to clarify the role of automatic power recovery. Requires that automatic power recovery be implemented in a safe manner.
3.2.6.4	The time constraints of short and long warnings are clarified.
3.2.6.5	CEM does not monitor ESM or ECS. Added bullet regarding one button power for equipment other than the basic elements.. Clarifies the relationship of equipment monitoring and power availability to peripherals in a multi-mainframe configuration.
3.3.2	A reference to PP usage has been dropped (it was redundant to the earlier description).
3.3.4	The entire section on Transaction Processing has been replaced.
3.3.7	Sentence calling program structuring a subset of CYBER 170 Segment Loader has been dropped, was misleading. The discussion of relative importance of loading performance vs. generalized library format has been clarified.
3.3.8.2	The requirements for interchangeable file formats, etc. have been clarified to apply to compilers and system utilities (removing the requirement from data management subsystems).
3.3.9.5	Functionally remains the same, the implication of multiple separate files has been removed.
3.3.9.6	Further modification/clarification to the accounting section.
3.3.10	A minimum configuration for pure 170 state has been added to support performance objectives in section 7.
3.4.1	The applicability of these general product set technical requirements to interpretive compilers is clarified. Several minor typographical corrections are made within the paragraph. The very last bullet regarding CYBER 180 system interface standard was redundant and removed.
3.4.2.1	Requires that Class I-III compilers must all honor the System Interface Standard. Minor changes support levels in the descriptive matrix. Add transaction interface to the matrix.
3.4.2.2	Clarifies FORTRAN's relationship to ANSI standard. Restructures COBOL section with no change of content. Clarifies BASIC relationship between interpretive and object code generation. Several minor editorial changes made to the other paragraphs with no change in substance.

Section	
3.4.2.3	Editorial changes have been made to improve clarity without changing basic content. "Random memory management" dropped - only a confusion factor.
3.4.3.1	Requirement for a Direct access method has been added. (The Basic Operating System will no longer support a built-in Actual Key access method.)
3.4.3.1	The last bullet regarding design trade-offs was removed. This information also appears in the design priority matrix.
3.4.3.2	The DBMS requirement description of concurrent access drops "improved performance for key batch jobs." Dual logging and dual recording has been changed to a separate, medium priority, item. A definition of data base sizes has been added. Several minor editorial changes are made to this section.
3.4.3.4	Data Dictionary System(s) allows a choice between one generalized or two specialized products.
3.4.4.1	APL 2 replaces APLUM.
3.4.4.3	Some priority changes have been made for DDL. All priority 4's dropped. The paragraph has been flagged as preliminary.
3.4.4.5	APL work space conversion utility has been added.
3.6	The introduction has been expanded.
3.6.1.2	The dual state requirements have been reorganized for clarity and generality. Some restrictions have been added, and this section should be carefully reviewed.
3.6.2.1	The objectives for CYBER 170 FTN5 conversion aids have been relaxed. The approach for CYBER 180 conversion aids has changed.
3.6.2.6	The requirement to process 170 work spaces has been relaxed to the ability to convert those work spaces.
3.6.3	File Conversion - this is a new section which replaces the corresponding section that appeared in A0/R Rev. B.
3.8	This section has been expanded and some of the line speed requirements changed.
4.3	The relationship between 170 and 180 maintenance software products has been reworded for clarity.

Section	
5.2.1	"Minor degradation in performance" means compile speed.
5.2.4	Global cross-reference listings apply to PASCAL, SYMPL, and the assembler.
6.0	This section has been completely rewritten in response to many questions. It should be carefully reviewed, although it is still preliminary.
7.0	The relationship of the Environments and Workload Spec to these performance objectives is described.
7.1	The BMC80 performance base has been corrected (the base line had been measured incorrectly on a CYBER 73).
7.2	Performance ratio for P3 PASCAL-X changed from 8.7 to 8.4 and special cases dropped to conform to the objectives in Rev. B. This section has been revised for greater clarity.
7.2.3	The block copy performance requirement applies to all systems not just THETA.
7.3.2	Requirement clarified to specify dual mainframe shared memory not a generalized common memory.
7.4.2	Terminology for the IOU cleaned up.
7.4.4.1	Clarifies relationship of block and record sizes.
7.4.4.3	Clarifies the number of exchanges permitted.
7.4.4.4	Eliminates abnormal termination and paging as considerations.
7.4.4.9	This paragraph was rewritten.
7.4.4.10	New section on Network Products Performance (with several changes from the earlier draft).
7.5.1	Wirth PASCAL added. BASIC production and development added. SYMPL field length requirements reduced and PL/I objectives deferred.
7.5.2	THETA Math Library performance increased.
8.1.1.3	Cache/Map bypass does not apply to S1.
8.2.1, 8.2.2 and 8.2.3	Have been organized by responsibility area (hardware, software, diagnostics or combinations) and minor editorial changes have been made. The requirement to repair memory concurrent with system operation has been dropped (it is not feasible). The requirement to repair the second CPU of a dual CPU mainframe has been added.

Section	
8.2.4.3	Applicable to mainframes only. Subparagraph 3)A) clarifies off-line engineering file analysis capabilities.
8.3.1.1	FCO's for THETA revised to more accurately reflect current schedule projections.
8.3.1.2	First year software maintenance costs are increased to more accurately reflect the special support requirements of that early time period.
8.3.2.1	System hardware maintenance cost objectives have been corrected (they were previously calculated against the wrong base cost).
8.4.3/8.4.4	System lost time for OS interruptions has been changed to reflect processor speed.
8.4.7	Clarification of parts availability. System availability objectives have changed due to increased THETA MTTR and reduced NOS/180 rerun time.
8.5.3	The DPSR objectives for S1 have been divided into processor, memory and IOU. Totals are corrected.
8.6.2	Correction to Sort objective.
8.6.5	New requirements on subsystem reliability.
9.2	STAR100 as a computational facility will not be precluded by current design activities.
10.1	This section and its sub-sections have been edited for clarity, and more detail. Minor revisions have been made, as well. The section should be reviewed carefully.
10.4.1	We <u>may</u> support the C180 parallel FMD on THETA/170 state. Minor changes in CMU interpretation requirements. a) the important distinction that a CYBER 170 lower system will deadstart and run an A170 deadstart tape rather than vice versa is clearly spelled out. This is an important distinction.
10.4.2	c) clarifies PP access to central memory, e) makes on-line remote maintenance an objective for software enhancements to the A170 state. Note that this maintenance must use standard communications subsystems.
10.6	Benchmark configurations have been added.
10.7	Configuration cost adjusted for changes in component cost objectives.
10.8.3, 10.8.4	O.S. lost time assumptions revised.

Section	
10.8.7	Minor changes in availability objectives, as a result of revised NOS objectives.
10.8.1	NOS objectives modified.
10.8.8	The relationship between CYBER 170 and CYBER 180 maintenance software objectives is clarified.
11.1.2	Cost distribution between the basic S1 and the 2 port MUX has changed. The total remains the same.
11.1.4	The target manufacturing cost for the basic IO Unit has been raised to compensate for added requirements on this product since Rev. A of the A0/R.
11.1.5	MG Sets and power control panels added to this section with corresponding changes in the configuration appendix.
11.2	Component Maintenance Cost Objectives have been revised.
11.3	Previous error in THETA processor functional inherent MTBF has been corrected and MTTR increased to reflect the greater complexity of the machine. IOU configurations having fewer channels than PP's have been eliminated. (Note, it is <u>not</u> a requirement to have at least two channels more PP's.
12.1	Development cost has been updated.
12.3	Peripherals Supported has been revised to include C180 O.S. release objectives and to make minor typographical changes.
12.3.1	Terminal Supported has been added.
12.4	Changes in response to cost objectives changed elsewhere in the document. Revises target communications configuration. More information on system power support.
12.5.5	Most recent shipment forecast has been added.
12.6	Corrections to schedule objectives.
12.7	Appendix G - Migration Action Plan - a first preliminary plan has been added to this document.

MEMO

CONTROL DATA CORPORATION

TO:	LOCATION:	FROM	EXT.	LOCATION:
Distribution		E. H. Michehl	2669	ARH293
SUBJECT:				DATE:
Draft 1 of CYBER 180 A0/R, Rev. C				4/6/78

Rev9 to Rev10

Since there were some pervasive terminology changes in this document (e.g., CYBER 180 superceded CYBER 80), the automatic change bar mechanism of text editor did not work reliably. We have hand-marked those changes which are "worth mentioning". A summary of those changes follows:

Section	
1.3.1	a) S1 target ship date has been added to this list.
1.3.3	The speed objective for the high end 180 processor is now 36 x CYBER 73, and the paragraph disclaiming the S1 system has been removed.
1.4	An added emphasis on the long term nature of CYBER 170 to CYBER 180 migration.
2.0	References - Under 10) - the shipment forecast reference has been updated.
3.1.1.2	Maximum central memory size changed from 64MB to 32MB.
3.1.1.4	The requirement for shared common memory in all multi-mainframe configurations has been removed and failure mode requirements restated. The reasons for dropping common memory were configuration flexibility and CEM and MCU control of shared components (especially common memory).
3.1.2	The qualifying phrase "listed in priority order for design trade offs" has been modified to "for functional design trade offs". We hope this will clarify the intent to provide a basic design which will support transaction processing but not compromise time-sharing system performance.
3.1.2.3	Communications/Networks has been moved to section 3.8.
3.2.2	Central Memory - In setting the THETA central memory cost/performance is not a driving factor. The THETA system is performance driven with manufacturing cost being a secondary consideration.
3.2.4	I/O Unit (IOU) - This has been restructured to incorporate the I/O Unit for the S1 system as well as S2, S3, THETA. Some configurability limitations of S1 IOU's are reflected.

Section	
3.2.4.2	The paragraph on functional usage of a peripheral processor by the C180 operating system has been expanded to more clearly illustrate the intent of those restrictions.
3.2.4.3	Multi-mainframe configurations will support shared access tapes.
3.2.4.4	An editorial comment was removed from the first paragraph. The requirement for ASCII character translation and display capability in C180 mode CC545 console is introduced.
3.2.5	The restriction on channel transmission structure has been removed. (The maintenance channel protocol is similar to but cheaper than that of the IOU.)
3.2.6.1	A requirement for air cooling for S1 is added, one button power-on removed as a requirement for ECS, and requirements against the power system in multi-mainframe configurations were added.
3.2.6.2	Automatic Power Recovery - This was added in response to a PLM requirement.
3.2.6.3	System Initialization - The nature of the storage device containing firmware/controlware was clarified.
3.2.6.4	System Monitoring - This was expanded to classify the types of warnings that must be monitored by the mainframe.
3.2.6.5	Configuration and Environment Monitor adds configuration capacity and clarifies multi-mainframe requirements.
3.2.7	Performance Monitor - The optional performance monitor will not be available on the S1. The sentence regarding OS and compiler support requirements was dropped.
3.3	Operating System - Multiple processors were added as a mandatory hardware support requirement.
3.3.2	System Code Organization was rewritten for clarity.
3.3.4	Transaction Processing - this is a new section.
3.3.5.2	Real Memory Management - the paragraph showing the distinction between central and bulk and private and common memory was removed because of the de-emphasis on common memory as a multi-mainframe linking device.

Section	
3.3.8.2	Basic Record Manager - A distinction has been made between basic record manager capabilities (sequential and byte-addressable) in NOS/180 and advanced access methods which are part of DMS180. The objectives for basic record manager remain essentially unchanged. Index sequential and multiple index file organizations are part of the advanced access methods.
3.3.8.5.3	Unit Record Equipment - rewritten for clarity.
3.3.9.6	Accounting - a bullet was added for support of application accounting.
3.3.9	Networks - this was moved to section 3.8.
3.3.10	Minimum NOS/180 Configuration - this was expanded to include minimum configurations for running dual state.
3.4.1	A bullet was added regarding the use of common modules within the product set.
3.4.2	Languages - this is a new section outlining a general language strategy for the C180 line.
3.4.3	Data Management - this section has been significantly expanded from its predecessor.
3.4.4	Design Objectives/Priorities - definition of execution speed was clarified.
3.4.4.1	Language Processors - Sort/Merge and the Implementation Languages were removed. PASCAL and JOVIAL and ALGOL-68 were added. This PASCAL should not be confused with the implementation language, PASCAL-X.
3.4.4.2	Support Services - Sort/Merge was added to this paragraph and Advanced Access Methods were moved to data management.
3.4.4.3	Data Management - this section has been completely revised in conjunction with the revised data management objectives.
3.4.5	Utilities - Index Management dropped and Data Base Creation and File Conversion/reformatting added.
3.6	Migration - the intent to add the migration plan to the C180 AO/R is announced here. It is not part of this document but will be added before the final submission.
3.6.1	Requirements for dual state O.S. processing have been expanded and rewritten.

Section	
3.6.2	The relationship of CYBER 170 SYMPL to product migration is reworded.
3.6.2.1	The use of a CYBER 180 common code generator for FORTRAN was introduced. The second section on breakages from C170 FORTRAN 5 has been expanded and rewritten.
3.6.2.2	COBOL - some O.S. and data dependent breakages will be converted by the C180 product and a COBOL-5-mode compile option will be allowed.
3.6.2.4	The C180 product migration assumptions for BASIC have been rewritten with the emphasis on conversion aid coverage being placed in the C170 product.
3.6.2.5 thru 3.6.2.8	All this material is new.
3.7.1	On-Line Monitor - Bullet 7 added requirements to the independence of this on-line monitor.
3.8	Networks - this is a new, separate section consolidating previous network comments. It is preliminary and will be extended for the final revision C.
5.1	The standards list is now Appendix H.
5.2	Tools and Services - parts of the text of this material have been written as a result of a recent C180 tools working group. This section represents the latest understanding of tools requirements.
6.0	Product Phasing Objectives - this section has been completely rewritten and reflects preliminary information with regard to all three C180 software releases. We expect to have a detailed definition of the contents of R1 of C180 software by 1Q79.
7.1	System Performance Goals - Goals for the S1 and THETA systems have been added.
7.2	Processor Performance - Goals for the P1 and THETA have been added along with several new footnotes detailing assumptions for this chart.
7.2.1	Memory Assumptions - assumptions for the P1 processor have been added. There are no assumptions or constraints applied to the THETA processor as is explained in footnote 9 to the preceeding section.

Section	
7.2.2	Cache Assumptions - P1 and THETA have been added.
7.2.3	Block Copy Performance has been added.
7.3.1	Central Memory Requirements - have been added for S1 and THETA.
7.4.2	IOU Performance has been updated to include the S1 IOU.
7.4.4.1	Record Manager - the instruction count allocations have been raised to reflect clarification of a mis-understanding regarding CALL overhead and to represent a better understanding of the requirements for key operations.
7.4.4.6	Periodic Functions - a new section combining all known sources of periodic CPU overhead.
7.4.4.8	The loader performance requirements have been restated and moved to this position.
7.4.4.9	Dual state performance requirements are new and preliminary.
7.5.1	Language Performance Level - an introductory paragraph has been added and objectives revised for several compilers.
7.5.2	Requirements on FORTRAN and COBOL run time code efficiency have been consolidated into one paragraph.
7.5.3	DMS180 - performance requirements have been withdrawn and will be resubmitted at a later time.
7.5.4	Sort/Merge performance requirements have been separated from record manager time and raised.
8.1.1.1	Duty Factors - the duty factor assumptions for peripherals have been clarified.
8.1.1.3	Component Criticality - some redundancy has been allowed for the IOU.
8.1.3	Associated RAM Requirements - this is a new paragraph in response to the previous A0/R review comments.
8.2	RAM Features - the cost/performance/reliability trade-offs for THETA CPU are outlined.
8.2.1	The parity checking on major data paths requirement is less rigid for THETA than for other processors because of the very demanding performance objectives.

Section	
8.2.2	Capability to fault a PPU was added. The requirement to provide information for customer maintenance was dropped to discourage third party maintenance. The descriptions of supporting data integrity and continuity of system operations have been clarified.
8.2.3	Micro-program control is not a THETA requirement. The description of the system maintenance panel has been dropped from this section. The requirement that no operator intervention be required for deadstart recovery condition logging has been added.
8.2.4.3	The first bullet under tests is a consolidation of two previous bullets reworded for clarity. The requirement for 100% protection of customer security has been added to "Tests" and "Diagnostics".
8.3.1.1	Number of FCO's per equipment per year has been added as as information only item.
8.3.1.2	The percentage distribution of PSR bug reports between the operating system and the DMS180 has been changed.
8.3.2.1	The objectives for hardware maintenance costs as a percentage of manufacturing cost have been revised downward.
8.4	RAM Performance Objectives - S1 and THETA have been added thruout.
8.4.7	Net Availability - the statement regarding rerun time has been changed to reflect use of fixed values in allocating rerun time against system net availability.
8.5.3	DPSR rates have been established for THETA.
8.6.1	DMS180 has been expanded to reflect the revised plan.
8.6.2	DMS180 has been expanded to include the revised plan. The operating system and sort/merge product input data failure rates have been revised.
8.6.4	DMS180 PSR receipt rate has been raised.
10.1.1	CYBER 170 Features Supported - this section has been reorganized for clarity and also adds information regarding instruction stack purging, pass instructions used for A170 features, and maintenance support of ESM maintenance features.
10.1.2	CYBER 170 Features Unsupported - this has been reorganized similarly to 10.1.1.

Section

10.1.3 Advanced C170 Features - additional information added regarding the use of the PP in A170 state.

10.4 CYBER 170 State Software - this section supersedes the previous one on compatibility and outlines the extent to which C170 software will be modified and enhanced in conjunction with C180 hardware.

10.5 CPU Performance - P1 and THETA have been added to this chart and S3 objectives raised.

10.7 Mainframe Costs - S1 and THETA have been added. S2 and S3 were revised slightly.

10.8 RAM - S1 and THETA values have been added thruout.

10.8.7 Net Availability - Method of determining rerun time is redefined and S1 and THETA are added to availability objectives.

11.1 Component Cost Objectives - Introductory remarks on memory costs have been omitted, as no longer applicable.

11.1.1 CPU's - Option for 16 KByte control memory for the P2 has been dropped. THETA CPU costs have been added.

11.1.2 S1 System Cost Objectives have been added.

11.1.3 Memory - THETA memory has been added.

11.1.5 Other - 752 console and S1 interface to high performance console controller have been added.

11.2 Component Maintenance Cost Objectives as a percentage of manufacturing cost have been revised.

11.3 THETA and S1 have been added to Component Reliability Objectives.

11.4.1 Central Memory Sizes - S1 and THETA have been added to this table.

11.4.2 Central Memory sizes above 32 MB have been dropped.

11.6 Preventive Maintenance - S1 and THETA have been added.

12.2 Appendix B - Standards was moved to Appendix H. {The unnumbered pages caused human factors problems.} It was replaced with C180 System Objectives Summary which has been updated to include S1 and THETA.

Section

12.3 Appendix C - Peripherals Supported - It is planned to support FMD parallel recording on a C180 channel in the C170 state, for THETA.

- 8000 and 20,000 line per minute non-impact printers have been added.
- 600 card per minute reader and 100 card per minute punch have been dropped.
- 6681-2 data channel converter costs have been revised.
- 6683 channel coupler and CYBER 18-5 batch terminal have been added.

12.4 Appendix D - System Configurations and Costs - the configuration information for S1 and THETA systems have been added and the configurations for S2 and S3 have been adjusted.

12.5 Appendix E - Shipment Forecasts - has been revised in accordance with various C180 program forecasts.

12.6 Appendix F - S1 System development milestones have been added.

12.7 Appendix G - Migration Action Plan - this is a new section which will be furnished with the next update to this revision of the A0/R.

E. H. Michehl
Director
Architectural Design & Control

paj

Attachment

CONTROL DATA CORPORATION
MINNEAPOLIS, MINNESOTA

DESIGN OBJECTIVES/REQUIREMENTS APPROVAL

COMPANY PRIVATE

New Product Program DIVISION

AO/R [~~DO~~ / ~~DR~~] # ARH1688

REV. # 12

Architectural Objectives/Requirements

~~DESIGN~~ * [~~OBJECTIVES~~ / ~~REQUIREMENTS~~] FOR: CYBER 180

(*Strike out term that does not apply)

SIGNATURES – DEVELOPING COMPANY		DATE
PREPARED BY: Architectural Design and Control		
REVIEWED BY: PROJECT MANAGER	E. H. Michehl	
	E. H. Michehl	6/12/78
DIVISION ENDORSEMENT: GENERAL MANAGER	[illegible]	
COMPANY ENDORSEMENT: COMPANY DELEGATE		

RESPONSE TO REVIEW DISTRIBUTION

	RESPONSE
SYSTEMS AND SERVICES COMPANY	
PERIPHERAL PRODUCTS COMPANY	
MARKETING COMPANY	
SERVICE BUREAU COMPANY	
PRODUCT AND SERVICES STRATEGY	

APPROVED: _____ _____

COMPANY DELEGATE DATE

AA5441 12/74

CYBER 180 ARCHITECTURAL OBJECTIVES/REQUIREMENTS

ARCHITECTURAL DESIGN AND CONTROL

DOC. NO. ARH1688

REV. 12

Table of Contents

REVISION DEFINITION SHEET

REVISION	DATE	DESCRIPTION
1	10/6/76	FIRST REVIEW COPY
2	10/19/76	UPDATED PER 10/6 REVIEW
3	11/24/76	UPDATED PER 11/8 REVIEW
4	01/14/77	UPDATED PER 12/13 REVIEW
5	02/17/77	UPDATED PER S/DS/M REVIEW 1/31
A	05/11/77	CDC APPROVED
6	07/15/77	FIRST DRAFT REVISION B
7	08/15/77	SECOND DRAFT REVISION B
8	10/21/77	SUBMITTED FOR COMPANY APPROVAL
9	01/20/78	UPDATED IN RESPONSE TO COMPUTER GROUP REVIEW OF 11/18/77
B	04/24/78	CDC APPROVED
10	04/03/78	FIRST DRAFT REVISION C
11	05/18/78	SECOND DRAFT REVISION C
12	06/12/78	SUBMITTED FOR COMPANY APPROVAL

NOTE:
This document was previously issued under DOC. NO. ASL00404, which is now obsolete.

1.0 INTRODUCTION

1.1 DEFINITION

These Architectural Objectives/Requirements (AO/R) define the general goals established by CDC for the CYBER 180 (C180) line. The goals for CYBER 180 hardware operating as a CYBER 170 (C170) (advanced CYBER 170, or C170) are in Section 10.

Where sections contain preliminary information, they are noted by the symbol, (#), where they contain "informational" objectives, they are noted by (#I).

This document satisfies the requirement for individual Design Objectives (DO) documents for elements of the CYBER 180 line, and supersedes all existing CYBER 180 and IPL DO's.

1.2 DOCUMENT ORGANIZATION

The Architectural Objectives/Requirements (AO/R) are in three parts: the Introduction, which describes the system in general objectives form; the body, which describes the major functional elements and characteristics of the system in specific terms; the appendices, which furnish detailed specifics of the system definition.

1.3 MAJOR OBJECTIVES

The major design objectives influencing the CYBER 180 are listed below in priority order:

- TIMELINESS
- RELIABILITY/AVAILABILITY/MAINTAINABILITY
- SPAN OF PRODUCT OFFERING

- COST/PERFORMANCE
- USABILITY
- PROTECTION/SECURITY
- STORAGE STRUCTURE

A balance among these general objectives is to be maintained. No high priority factor is to be allowed to compromise a lower factor below acceptable levels.

The specific objectives of low manufacturing cost for the S1 and high CPU performance for the THETA system are to receive special emphasis. Any exceptions are noted in the text of the AO/R where known, and will be fully defined in the specific products' DR's.

1.3.1 TIMELINESS

Several planning dates are key to the CYBER 180 product definition:

a) Shipment of new hardware in CYBER 170 state -

S1 - 12/19/80 (internal release)
- 3/15/81 (external release)
S2 - 1/15/80
S3 - 11/01/80
THETA - TBD

b) First release of CYBER 180 state O.S. 12/01/81.

Design trade-offs which cummulatively affect the program schedule more than three months will be submitted for upper management review and approval.

1.3.2 RELIABILITY/AVAILABILITY/MAINTAINABILITY (RAM)

It is a requirement to maximize time between interruptions, to continue operations in degraded mode and to minimize repair time and cost. Emphasis will be placed on software checking/recovery features and hardware assists to RAM (to the extent of adding 10-15% to manufacturing cost).

Hardware redundancy will be required for higher MTBF configurations, passing this cost to those users requiring it.

1.3.3 SPAN OF PRODUCT OFFERING

The hardware/software system is to span a large range ($150-2000K in 1976 manufacturing cost terms) of configurations, applications and processing power. The line is to encompass central processors of the range 1 to 36 times the speed of CYBER 73. (In the context of this document, the CYBER 73 may be assumed to be equivalent to the CYBER 172, but the measurement base remains CYBER 73.)

1.3.3.1 Applications

CYBER 180 is to be cost/performance effective in support of general scientific and engineering applications. It is required to effectively function in network and data base environments and to allow user access in transaction, batch or timesharing modes.

1.3.3.2 Compatibility Within The Line

CYBER 180 is to be compatible across its range in source languages, instruction set, data formats, recording media and the user interface. Feature and capability subsetting are acceptable for high and low performance configurations.

1.3.3.3 Commonality

To reduce development, manufacturing and maintenance costs, common elements are to be used across CYBER 180. At least:

- Software product set
- Basic operating system
- I/O channels and controllers
- Peripheral devices
- Peripheral and controller diagnostics
- Model-independent tests, e.g., memory tests
- Diagnostic utilities

Additionally, CYBER 170 elements will be carried forward to the CYBER 180 line, where possible.

1.3.3.4 Continuity

An incremental progression in processing power, system throughput and system capability is to be achieved through hardware configurability, specialized software scheduling algorithms and selective addition/deletion of software features.

1.3.3.5 Implementation Control

A broad range of applicability for the hardware/software products is to be assured through specification and use of engineering standards, software conventions and common implementation tools.

1.3.4 COST/PERFORMANCE

The CYBER 170's market strength is high system throughput. This remains a major design factor for CYBER 180, however, the priority is lower than it has been for CYBER 170 systems.

1.3.5 USABILITY

CYBER 180 is to emphasize usability by applications programmers. Application programs are to be easy to develop and debug. The interactive interface is to be simple to learn and to use.

The major design criterion is to define the essential features of the user interface in a simple and consistent manner. Where a tradeoff must be made between NOS/NOS-BE evolution and simplicity, simplicity prevails.

1.3.6 PROTECTION/SECURITY

CYBER 180 is to supply a basic level of hardware/software protection which significantly exceeds CYBER 170. More sophisticated security and checking features must be furnished as software options. (It is expected that a requirement for "certifiable security" will exist during the lifetime of CYBER 180.)

1.3.7 STORAGE STRUCTURE

A major CYBER 180 objective is provision of progressively more powerful memory and storage capabilities relative to CYBER 170 and early versions of CYBER 180. This includes:

- large real memories
- virtual memory mechanism

Longer range CYBER 180 objectives are to effectively support new storage technologies and storage hierarchies.

1.4 MIGRATION

After having defined a product line which is competitive in the marketplace of the 1980's, migration of the existing CYBER 170 customer base becomes a major consideration in CYBER 180 definition. Conversion from a CYBER 170 to a CYBER 180 state system must be significantly less expensive than conversion to a competitor system. The migration strategy will emphasize an extended period of conversion from CYBER 170 state to CYBER 180 state.

The chief elements of the migration strategy are:

a) Hardware

CYBER 170 State - CYBER 180 hardware is to be capable of replacing a CYBER 170 mainframe and executing its code unchanged. Execution of the CYBER 170 instruction set on CYBER 180 hardware is defined as CYBER 170 state. (Refer to Section 10 for all objectives of the CYBER 170 state.)

Peripherals - selected CYBER 170 peripheral devices and controllers will be supported in CYBER 180 native state.

b) Operating System

Target Operating System - define a target operating system specification for CYBER 180 and then "bend" CYBER 170 systems and products toward that target. The driving forces on the user interface are simplicity and consistency.

Multiple job streams - initial versions of the CYBER 180 operating system will support a dual-state CYBER 170 and CYBER 180 job stream.

c) Product Set

Product Set Development - apply as much new CYBER 170 product set development to CYBER 180 as possible (even if it means delays to the 170 program). Advise users of recommended source and data usages which will ease their conversion to CYBER 180.

User Programs - aim for source language compatibility between CYBER 180 and the equivalent 1981 CYBER 170 product. The driving force on the user interface is data/machine independence.

d) Data/Files

A set of logical recording conventions will be established on both lines to ease file conversion.

2.0 REFERENCES

1) Computer System Architecture Sub-Strategy (Revised 6/5/73)

2) EDP Systems Strategic Plan, 1977-1981 (Approved 7/6/77)

3) CPD CYBER 170 Software Implementation Plan (Network Products information only), October 1976.

4) CDC Market Requirements Document (11/10/76)

5) Environments & Workloads Specification, ARH1858

6) IPL Processor/Memory MIGDS,* ASL00211 Rev. G

7) IPL Hardware Maintenance Strategy, ASL00270 Rev. A

8) CYBER Operating System Security Requirements and Status, August 31, 1976, Daniel Zak.

9) Large Computer Mainframe Reliability Growth Study, 11/22/76, K.J.Bradford

10) CYBER 180 Product Life Forecast, 04/14/78, D.L.Mueller, B.L.Thompson

11) CYBER 180 Program Plan, NPP Program Office

12) CYBER 180/170 Maintenance Software Strategy/Development Plan, 4/4/77, J.W.Sundet

13) CYBER 180 System Interface Standard, S2196

14) CYBER 180 Maintenance Objectives and Requirements, 8/2/77

15) CYBER 180 Product Line Plan, F.Vince/B.L.Wissner, April 1978

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* Reference 6 is considered to be the base hardware specification for this AO/R, although it now is superseded by the CYBER 180 Mainframe MIGDS, ARH1700.

16) DoD Directive 5200.28-M ADP Security Manual, January 1973

3.0 CHARACTERISTICS AND FEATURES

3.1 CONFIGURATIONS

3.1.1 HARDWARE CONFIGURATIONS

It is the intent of CYBER 180 to achieve a smooth progression of computing power by offering a limited number of multi-processor and multi-mainframe growth options at each system level. This limited number of configurations is chosen to allow simpler design and installation characteristics to improve cost effectiveness. Cost data for various configurations is contained in Appendix D.

3.1.1.1 Terminology

Terms to reference hardware elements:

Mainframe = central processor(s) + central memory + I/O unit

Mainframe system = Mainframe + Peripherals

Designators used to reference hardware elements (except THETA):

Central processor = Pn

Central memory = Mn

Mainframe system = Sn

Input/Output Unit = In

where larger n indicates increased capacity and/or speed.

3.1.1.2 Mainframe Systems

A CYBER 180 mainframe system is memory centered with emphasis on configuration growth and connectability:

- 1MByte-32MByte central memory.* Each memory accessible by:
  - 1-2 identical central processor units.
  - 1 (or (8) 2) I/O Units, each consisting of:
    - 5-20 Peripheral Processors (PP)
    - 8-24 channels

* Varies by system type (see 11.4.1)

3.1.1.3 Reconfigurability

Specific device classes may be required to run the system but not specific device models.

Facilities will be provided that allow for incremental system expansion with minimum site disruption. It will be possible to add or delete peripheral devices from a running system.

Facilities will be provided that allow for dynamic reconfiguration around failed critical components (especially CPU's in a two-CPU system, memory, and PP's).

It will be possible to power-up and power-down all equipment without affect to the MTBI. In addition, power-up and power-down shall not require the assistance of a maintenance engineer.

3.1.1.4 Multi-mainframe Systems

Multiple mainframe system support will include:

- Job/file routing via I/O channel connections (local or remote) to a dual CYBER 180 or to a CYBER 180-CYBER 170 mainframe system.
- Shared mass storage devices, magnetic tape devices, communications front-end, mass storage files and input/output queues among two to four mainframe systems running the CYBER 180 operating system. Jobs executing in different mainframes have the same file sharing

capabilities as two jobs executing in the same mainframe. Jobs may be dedicated to specific mainframes (e.g., jobs using non-shared equipments or requiring a unique processor type).

In the general multi-mainframe configuration loose coupling (e.g., no direct access common memory element) is used for system control. An optional dual mainframe configuration using a shared area of one mainframe's central memory for coupling is supported.

In the event of a single mainframe failure the remaining mainframes can continue to function in a multiple mainframe environment. In the event of a mass storage failure (device/controller) only the failed physical element would be inaccessible to the mainframe complex. Configurations that allow for dyramic reconfiguration around link-medium failures are supported.

3.1.2 SOFTWARE CONFIGURATIONS

The system will support concurrent processing in any or all of the following operating modes (listed in priority order for functional design trade offs):

- transaction and limited time-sharing
- general purpose time-sharing
- batch (remote and local)

The intent is to provide a basic design which will support transaction processing but not compromise time-sharing system performance. All modes of operation must meet configuration and performance requirements.

The system is to be capable of optimization for a specific operating mode. Implementation of a time-critical operating mode will not be specifically supported nor deliberately precluded.

3.1.2.1 Software Feature Configurability

Software feature design and implementation will support CDC's separate element pricing strategy. A limited number of major software features and products will be developed and offered as optional capabilities. The system design will also allow for feature and capability subsetting to achieve high performance or

maximum capability software configurations.

3.1.2.2 Reconfigurability

Reconfiguration of specific critical software components to obtain different system performance, capability and RAM characteristics will be possible in a user's running production environment.

3.2 HARDWARE ELEMENTS

3.2.1 CENTRAL PROCESSOR (CPU)

A series of CPU's are required to support a range of performance and applications; specifically, capabilities for Scientific, BDP and for CYBER 170 state.

The CYBER 180 CPU will be based on the CYBER 180 Mainframe MIGOS, ARH1700.

3.2.1.1 Instruction Set

The native CYBER 180 instruction set will handle the applications above with emphasis on:

- linkage for switching control between CYBER 180 and CYBER 170 state.
- floating point orientation, emphasizing execution speed.
- BDP orientation, emphasizing balance between instruction speed and code compaction.
- memory management, emphasizing protection and large address spaces.

3.2.1.2 Virtual Memory Mechanism

Provide a virtual memory mechanism to support a large virtual address space by means of segmentation and paging. The mechanism is to include protection schemes for inter/intra job protection.

3.2.1.3 Other CPU Features

- Software managed, interrupt driven processor.
- Fixed support to connect an optional performance monitoring facility (not to exceed 0.2% CPU cost, excluding real estate costs).
- Process separation (protection) and memory interlocks.

- Procedure switching assistance, including stack operations.

3.2.2 CENTRAL MEMORY

Central memory objectives are:

- Span the product range (excluding THETA) with the best cost/performance. This implies:
  - Exploiting the advantages of cost reductions in memory component technology.
  - Use of cache memory in the CPU for performance improvements.
  - Minimize cost/bit including cache costs (memory volatility is acceptable).
- Maximize availability through:
  - Single Error Correction/Double Error Detection SEC/DED
  - Reconfigurability around faulty memory elements.
- Logical byte addressability

3.2.3 (#) BULK MEMORY

Bulk Memory objectives are:

- Provide facilities to fully utilize bulk memory technologies e.g., electronic beam access memory (EBAM) or bubble type device when available.
- Optionally support bulk memory to supplement central memory.
- Bulk memory will be addressed in the same manner as central memory (including execution).
- Bulk memory will be non-volatile (i.e., retains information 24 hours without power). Software will not compensate for volatile media.

3.2.4 I/O UNIT (IOU)

The I/O Unit provides the input/output capability for CYBER 180, in 180 state, 170 state and dual state operations. The primary objectives are:

- support for CYBER 170 state.
- support a high speed I/O system architecture that performs most of the equipment oriented functions for the CPU.
- provide connectability to CYBER 170 peripheral devices.
- provide flexible configuration options.

To satisfy these objectives the IOU shall provide:

a) CYBER 170 as a subset of the full peripheral processor (PP) instruction set.

b) Any combination of 5-20 PP's in increments of 5.

c) Any combination of 8-24 channels in increments of 2.

- at least 1 channel per PP
- both of a channel pair are of the same channel type (170 or 180)
- S1 supports only C170 channels up to a maximum of 22.

d) Full cross connection between PP's and central memory.

e) Full cross connection between PP's and channels

- limited to 10 x 12 on S1, restricting S1/170 state configurations to 10 PP's (one cluster) maximum.
- 20 PP S1 configurations (180 state only) require two channels for cluster interconnection.
- CYBER 180 state O.S. and maintenance software will restrict their use of full PP-channel interconnectability in anticipation of future models eliminating this capability.

f) Provide a two-port operator console multiplexor (see section 3.2.4.4).

- one port reserved for local operator console.
- one port reserved for remote maintenance.

Peripheral devices supported in both CYBER 170 state and CYBER 180 state use the CYBER 170 channel and unmodified controller. Changes in controlware and recording format are allowed for CYBER 180 mode support.

3.2.4.1 Channels

The channel configuration allows connection of CDC 3000 Series (via a CDC 6681 Data Channel Converter or equivalent), 6000 Series, CYBER 70 or CYBER 170 peripherals. In addition, a unique CYBER 180 channel will be provided that has the following capabilities:

- high transfer rate, see Section 7
- channel width of 16 data bits plus parity
- cost efficient electrical transmission scheme for cable lengths up to 200 ft.
- error detection, error isolation, and error reporting hardware which allows system RAM objectives to be met.

3.2.4.2 Peripheral Processors

The PP's will be 16-bit processors that use the CYBER 170 PP instruction set. In addition, instruction set extensions allow the addressing of all of central memory, and the efficient transmission of 8-bit oriented data.

To insure system integrity, the level of function performed by the PP and its access to central memory is restricted by the design of the software. As a C180 system element, the PP mainly performs functions related to input/output operations. Predominately compute oriented functions (e.g., scheduling the CPU) are not performed by the PP. PP's are dedicated to perform specific functions (e.g., mass storage I/O, tape I/O, front-end I/O). Central memory request queues managed by the operating system describe logical functions (e.g., fill these buffers from position X of disk Y) to be performed by the PP. The PP interprets these requests into device dependent operations. It also performs basic error recovery operations.

The system function of monitoring for software and hardware errors or failures is performed by a PP (On-line Monitor).

C180 PP software will be treated as controlware (see 5.2.2.1).

3.2.4.3 Device Controllers

Device controllers will provide the following capabilities (except where not appropriate to the device type):

- shared access or multiple data stream as necessary to support multi-mainframe systems (RMS, tapes and communications front ends only)
- support several models of the same device or device class
- attachment of up to 64 devices
- maximum overlap of operations on separate devices
- single functional design for a device class
- provide interface to CEM for power control and environmental monitoring (see 3.2.6.5).

3.2.4.4 Operator Console

The operator control console for CYBER 180 consists of one or more interactive terminals which interface to the CYBER 180 OS by means of standard interactive terminal mechanisms. The intent is limited operator/system interaction.

Basic operator control console functional characteristics:

- 300 baud for remote consoles
- 9600 baud for local consoles
- CRT screen of 24 lines by 80 characters
- cursor control capability
- standard ASCII keyboard

No CYBER 180 (nor new 170 state) operating system or diagnostic software will require functional capability greater than that of the basic control console to operate.

Extended system status display capability will be available using more powerful, optional display consoles, which provide a superset of the functional characteristics of the basic control console and which may replace it. (The current C170 CC-545

console (only) will be allowed to fill this requirement on an exception basis.)

The operator interface will support:

- single, multiple and remote operator console configurations.
- minimum requirements for operator intervention (i.e., design to execute in an unattended manner).
- use of standard I/O interfaces and equipments for operator communications.

3.2.4.5 Peripheral Devices

Peripherals to be supported are listed in Appendix C.

3.2.5 MAINTENANCE CHANNEL

There will be a Maintenance Channel with the following characteristics:

- Connect to the CPU's, memory, I/O Unit and other intelligent devices in the system.
- Provide the means for master clearing/initializing the connected system elements.
- Provide the interface for the Environment Monitor and Performance Monitor.
- Provide a privileged access to the system for maintenance and reconfiguration.

3.2.6 HARDWARE SUPPORT FACILITIES

There will be a set of hardware support facilities which provide the following functions:

- Power-on/Environmental Monitoring
- System Initialization

- On-Line System Monitoring

- Off-Line Diagnostic Control

3.2.6.1 Power System

The basic system will have temperature monitoring and power control local to each equipment and operating independently of all other system equipments. The basic system equipment requirements are:

- MG Set/Controller
- Power Control Box (include dewpoint sensing for liquid cooled system)
- Environment (temp/humidity) recording
- Terminator Power Supply
- Chilled water is an acceptable requirement for S2, S3, and THETA systems; S1 must be air cooled.

For operational convenience, it will be possible to power up the mainframe and certain peripherals from a single power-on button. This will apply as a minimum to all mainframe components, to all controllers, and to system disk drive and controller. The system will also include a manual emergency off control.

Multiple mainframe systems will be treated as separate mainframes each having their own power supply, either from their own MG set or from a single MG set via load controllers. Elements common to these mainframes (e.g., memory, disks, etc.) shall either have their own, independent power supply or use a single MG set via load controllers.

MG sets will be offered either at minimum cost or with maximum reliability (to the system). The high reliability sets will provide a 2 1/2 second ride-through capability. See section 11.1.5 for details.

3.2.6.2 Automatic Power Recovery

As an option, an automatic power recovery feature will be provided. This feature will have the following capabilities:

- When the power supply is interrupted for a period not exceeding one hour, power will automatically be returned to

key system elements.

- A deadstart signal will be provided and a recovery deadstart can be performed without operator assistance.

- Equipment sequenced up will include as a minimum: all mainframe components; system disks, permanent file disks and their controllers; remote terminal multiplexers/front-ends (ie., 2550) and other MGs; magnetic tapes and unit record equipment will be excluded.

This option will require a Configuration and Environment Monitor (CEM) and 2.5 sec ride-through as part of the configuration. There may be legal implications which could nullify this objective. However, until these legalities are resolved, development should assume the objective stands, and design this feature with the appropriate safety features.

3.2.6.3 System Initialization

System initialization places a minimum set of hardware in a known operational state, ready to deadstart the operating system or execute off-line diagnostics. This automated process is initiated by pressing the system initialization button. The minimum set of hardware initialized is the hardcore system elements which are those affected by one-button power on, plus the system console. As each hardcore element is initialized, confidence level tests are run against it before proceeding to the next element. The final step of system initialization is to pass control to the Operating System. The Off-Line Diagnostic Monitor or the Operating System will have the responsibility for initializing the remainder of the system.

The system initialization process begins in the IOU and requires:

- A PP

- A prestored program accessible by that PP from read only memory.

- A storage device containing the firmware/controlware for the hard-core system elements. Under normal operating conditions this will be the system mass storage device; otherwise it will be a removable media device (see 3.3.10).

- A console, as in paragraph 3.2.4.4.

The prestored program validates the PP being initialized and validates and provides the code necessary to read a record from the input device. The MTBF of these components significantly exceeds the system MTBF and will not be less than 10,000 hours.

3.2.6.4 System Monitoring

For hardware support monitoring in the on-line and off-line environment see Sections 3.7.1. and 3.7.2.

All mainframe components shall be monitored for environmental conditions out of range. Mainframe components comprise: processors, IOU, memories (excluding ECS), and ECS coupler in CYBER 170 state. Environmental conditions shall be divided into two categories:

Short Warnings

These are warnings of an imminent failure, typically to a system critical element, which shall be reported by interrupting the CPU a minimum of 2.5 seconds before the failure occurs.

Long Warnings

Long warnings are provided without interrupting the CPU whenever environmental conditions are such that an element may be expected to power down unless the condition clears. These warnings shall be provided a minimum of 2 minutes prior to power-down.

3.2.6.5 Configuration and Environment Monitor (CEM)

An optional Configuration and Environment Monitor will be developed that performs the following functions:

- Monitors systems for environmental/power faults and warnings. When present in the system, the CEM will monitor the mainframe components for environmental/power faults and warnings. The minimum types of equipment to be monitored are (see Appendix C for more detail):
  - Processor
  - Memory

  - IOU
  - System disk controller
  - System disk
  - Permanent file controller
  - Permanent file device
  - Base unit record equipment (batch or communication oriented)
- Monitors environmental status information from the computer room such as dewpoint, power brown-out, etc.
- Disseminates alerts to processors that indicate a system failure is imminent.
- Powers-up and powers-down mainframe components and selected peripheral equipment under program control as an energy conservation measure.
- Provides one-button power on/off to equipment other than the basic group specified in paragraph 3.2.6.1.
- Connects to a maximum of 64 system elements or element groups (e.g., a group of disks or magnetic tapes).

In multiple mainframe configurations:

- The CEM is optional to each mainframe.
- A mainframe monitors itself and its peripherals.
- Shared peripherals are monitored by one mainframe only. Note that when one mainframe is powered down the shared peripherals will still be available to the other mainframe. However, if the mainframe which is powered down was responsible for monitoring environmental conditions on the shared peripherals, then they will no longer be monitored.

3.2.7 PERFORMANCE MONITOR

Except for S1 the CPU will support an optional Performance Monitor hardware facility that collects data describing the dynamics of system execution. This data includes measures of interrupt frequency, processor state changes, cache management, etc. that can be used in the analysis of system performance.

Test points are furnished on the IOU to allow monitoring of external device and channel utilization by means of commercially

available recording devices. Suitable test points will also be furnished on the S1.

Performance Monitoring will be extendable, will not interfere with the system when inactive and will not violate system security.

3.3 OPERATING SYSTEM

The CYBER 180 operating system (NOS/180) has the following design objectives:

1) Take advantage of CYBER 180 hardware capabilities.

2) Make user interfaces:

   a) NOS/170 compatible, or
   b) Key migration interfaces of NOS/170 may be mapped onto NOS/180 interfaces through command language procedures or object library programs and services, or
   c) Extensions beyond NOS/170.

3) Satisfy the needs of the software products, in priority order:

   a) FORTRAN (interactive,batch)
   b) Communications
   c) Data Management
   d) COBOL
   e) BASIC
   f) APL

Early releases of NOS/180 are primarily concerned with the migration of NOS/170 users. CYBER 180 hardware support will be phased across several releases.

Mandatory
- dual state (CYBER 170 and CYBER 180)
- large real memory
- segmented virtual memory
- rings of protection
- I/O channel bandwidth
- multiple processors

Highly Desirable
- code segment sharing

- dynamic paging

Desirable
- data segment sharing
- two speed memories (central/bulk)
- key/lock protection

CYBER 180 hardware and NOS/180 use multiple mainframes as the primary path for increased availability with growth. NOS/180 supports the distribution of major system functions among separate mainframes or subordinate processors.

3.3.1 SYSTEM STRUCTURE

NOS/180 has four major functional elements, each with its own objectives, guidelines, interface rules and restricted set of functions. The elements are:

1) Monitor functions - the fundamental functions of software that translate hardware conditions and signals into standard software conventions and data structures and that manage the CPU. NOS/180 and stand-alone CYBER 170 state require an implementation of monitor functions.

   Monitor Objectives

   - Correct functional distribution
   - Reliability of function
   - Speed.

2) Basic Operating System (BOS) functions - basic functions most closely associated with managing system elements (jobs, tasks, files, memory, peripherals). BOS functions are primitive and are not directly interfaced by end users. PP functions are part of BOS.

   BOS Objectives

   - Correct functional distribution
   - Reliability of function
   - Speed of function and program call
   - Stability of interface definition
   - Effective use of CYBER 180 hardware
   - Consistent and symmetric interfaces for all elements

3) Support Functions - general service functions available to

executing programs (e.g., loader, basic record manager, operator communication). These routines are structured to allow selective replacement by user or site supplied routines.

Support Objectives

- Performance of the function and the program call
- Reliability of function
- Stability of specification
- Adaptability to future change without forcing user conversion until the new feature is used

4) Extended Operating System (EOS) functions - functions that manage the flow of work. EOS provides the command language interface to the end user. An NOS/180 configuration may have multiple instances of EOS, each tailored to the needs of different users (e.g., transaction oriented application).

EOS Objectives

- Ease of use
- Adaptability to future change without conversion or retraining
- Performance
- Packaging

3.3.2 SYSTEM CODE ORGANIZATION

Where possible NOS/180 system functions execute in the same environment as user programs. System functions execute at more protected ring levels. One copy of the code for these functions is shared among multiple user programs. NOS/180 also supports many features in the manner of utility programs with mechanisms for adding, deleting and overriding these programs.

3.3.3 JOB PROCESSING

A job is the major unit of work managed by NOS/180. Users and NOS/180 submit jobs to perform work within the system. Resource assignment and usage accounting is associated with a job. Each job has a single owner and is known by a unique name. Access to resources and protected elements in the system is granted to the

owner of the job.

The job deck/file structure resembles NOS/170; a set of command language statements followed by data elements.

A job step is the work done as a result of a single command in the job deck/file. Job steps execute sequentially within a job.

A task is an instance of execution of a program. Multiple tasks can execute within a single job step. Each task has its own address space (set of memory segments). Tasks may be initiated either synchronously or asynchronously to the initiating task.

All command language statements are processed within the environment of the job. Terminal sessions are processed as a job; login is job initiation and logout is job termination.

Jobs may submit other jobs for processing. NOS/180 provides commands to assist users and operators in controlling the progress of submitted jobs.

3.3.4 TRANSACTION PROCESSING

NOS/180 processes transactions using concepts (user's viewpoint) similar to those of CYBER 170 TAF/NOS. Transactions are processed utilizing the tasking features of NOS/180, and permit transaction applications to have the same access to system resources (i.e., tapes, files, databases, private packs, etc.) as do batch-mode and interactive-mode jobs. Transaction processing is offered in NOS/180 in a manner which permits tradeoff of performance versus features, and provides effective control of the system resources devoted to such processing.

NOS/180 supports multiple transaction applications with concurrent access to shared databases. Individual applications may be remotely controlled by Application Administrators. Recovery of transactions is coordinated with data management and communications products so as to provide a system which features high integrity, continuous operation, and ease of use.

While recognizing the need for high-performance transaction processing, CYBER 180 emphasizes the low to mid performance range in commercially-oriented applications. A basic transaction processing capability will be provided in NOS/180 R2, and a competitive transaction processing capability will be provided in

NOS/180 R3.

NOS/180 transaction processing objectives include the following:

1) Transaction Priorities. It will be possible to process transactions on the basis of transaction priority within an application. It will be possible to alter a transaction's priority during its execution.

2) MME Load-Leveling. It will be possible to achieve load-leveling in a multi-mainframe configuration by sharing an application's transaction load between mainframes. This will not be dynamic load-leveling. All transactions from a given terminal are processed on a single mainframe. Terminal connection is made at LOGIN by NHP's Communication Supervisor.

3) Single Owner. Each transaction application will have a single owner. This owner will also own all resources of the application, and will be accountable for all resources consumed by the application.

4) Task Chains. It will be possible for one task to initiate another task or task chain, with the option of continuing execution or awaiting completion of the called task or task chain.

5) Communication Block. A variable-length data block may be passed from one task to another during a transaction. This block may be saved between transactions.

6) Unsolicited Input. When an unsolicited input is received, a communication block will be prepared with the appropriate entries, and an initial task will be initiated. Applications will be capable of accepting unsolicited input while a transaction is in progress.

7) Terminal Status. It will be possible for a terminal user to status the system at any time. A terminal user may receive the input and output messages associated with the last successfully completed transaction for the terminal.

8) NAM Messages. It will be possible to initiate execution of a task as a result of a terminal being newly connected, reconnected during recovery, disconnected, or logged out from an application.

9) Standard Interfaces. Transaction applications will use standard NOS/180 interfaces, and will have the same access to system resources (e.g., tapes, files, databases, and network products) as do other applications.

10) Lock Control. DMS180 will provide lock capabilities at record type and individual record levels. Record types and records which remain locked but not accessed for some installation-defined timeout period will be unlocked.

11) Quiet-Point. DMS180 will process Quiet-Point requests. Most database failures will be recovered by DMS180 without user application intervention or knowledge.

12) Cancel/Checkpoint. DMS180 will process Cancel and Checkpoint requests, and will ensure that "all or none" of each set of updates are performed.

13) Test Mode. It will be possible for Application Administrators to test selected transactions in a "live" environment without endangering databases.

14) Database Recovery. In the event a database is not fully recoverable, it will be possible to restore the database concurrently with other system operations.

15) Message Routing. Terminals will be able to send messages and transmit files to a single destination, or broadcast to a number of destinations. Each destination may be a device, a user, or a network queue; and may be referenced by logical name. This facility will be CDC's Message Control System (MCS) offering.

16) Page Browsing. Display terminal outputs which exceed one page (screen) will be queued, and an alert will be given at the terminal indicating more pages are available. The operator may access these pages randomly or sequentially.

17) Formatted I/O. Application Administrators will be able to create new or modify existing screen image definitions from remote consoles using Format Services. These image definitions will be used during formatted-screen I/O.

18) Off-Line Spooling. Terminal operators will be able to perform display-to-tape cassette operations in an off-line (local) mode, and later transmit the cassette messages to a host computer.

19) Terminal/Protocol Support. NOS/180 network products will support the terminal types and line protocols defined in Section 3.8 and Appendix C.

20) Distributed Processing. Transaction applications will be able to distribute their function and database throughout a computer network by routing messages to network queues. Message routing will be performed using standard NOS/180 interfaces.

3.3.5 MEMORY MANAGEMENT APPROACH

NOS/180 use of the CYBER 180 memory organization has the following objectives:

1) Increase reliability and integrity of all software products, especially the operating system.

2) Increase security and protection of user and system programs and data.

3) Provide coverage of a broad range of configurations.

4) Increase flexibility to meet future requirements for new features and capabilities in an upwards compatible fashion.

5) Share code and data among system and user jobs.

6) Support uniform addressing across code and data as experience and technology dictate.

The memory of CYBER 180 is managed at two levels, virtual and real. Virtual memory mechanisms provide the user's view of memory while real memory management is associated with the physical memory resources of a CYBER 180 system.

3.3.5.1 Virtual Memory Management

Virtual memory (or user memory) is a set of memory segments. Individual segments are units of protection and sharing within a task's address space.

Access to segments is regulated by access mode control, ring protection, and key/lock hardware features of the CYBER 180 hardware. Shared segments can have different access and

protection rights for each task's address space. Segments can be transferred between tasks within a job and can be paged.

The system software is a set of segments, some of which appear in every task's address space. This sharing is managed by NOS/180.

3.3.5.2 Real Memory Management

NOS/180 uses paging hardware to manage the allocation and use of real memory. Paging allows:

1) Overcommitment of virtual to real memory.

2) Performance optimization of virtual memory use.

3) Memory degradation and partitioning.

Job swapping is also used to manage real memory.

3.3.5.3 Cache Management

Software management of the CPU cache is required when one processor accesses a segment that may be written into by another processor. To avoid conflicts, NOS/180 bypasses cache memory for such segments.

3.3.6 USER INTERFACES

The user interface supports a wide variety of users. NOS/180 functions will be made available to as many access modes (e.g., interactive, batch, operator) as possible. These functions will be identical externally within the constraints of functional security and hardware, regardless of the mode of access.

The NOS/180 command statements are a simple language that adheres to the CYBER 180 system interface standard. The command language includes:

- Control functions to direct job flow (e.g., conditional, iterative and assignment statements).

- Functions that define and manage the job environment through variables used by the command language and

executing programs. NOS/180 services use these variables (e.g., file descriptions, program descriptions, job step termination status) to interface between the user and the operating system.

- Execution of programs and assignment of resources (e.g., files, equipment, memory).

- Execution of predefined sequences of command statements from procedure files. User command calls and command procedure calls are interchangeable as need dictates.

- Operator control functions.

NOS/180 provides complete and descriptive status and error information to the user. All status and error information presented to a user is controlled by a system message generator utility. A user may select the level of detail desired for information messages received from the system.

3.3.7 LOADER/LIBRARIES

The NOS/180 loader loads object modules into memory and establishes linkages to other object modules. It accepts object modules output from compilers or the link-editor via sequential or library files. Multiple system and user libraries are supported. A default search list is unique to each job (user) and can be modified during job execution.

The link-editor structures programs and combines object modules. The user structures programs to control the working set size, to group modules functionally and to improve performance.

NOS/180 provides source code and object library maintenance utilities. The packaging of programs and libraries is important to performance in NOS/180. The link-editor and the object library maintenance utility support this packaging process. In NOS/180 the objective is high performance loading from an object library in preference to supporting a broadly generalized library file format for source and object library files. Any library file is processable by the record manager and by the general file utilities.

3.3.8 INPUT/OUTPUT

3.3.8.1 Files

A file stores information (jobs, data, programs, libraries) within the system environment. It has one owner and is a primary object of security and protection controls. File access may be shared among multiple users at the discretion of its owner and users.

NOS/180 supports permanent files (registered and saved for subsequent access) and temporary files (discarded at job termination). NOS/180 supports multiple cycles of a permanent file.

One permanent file mechanism is provided. The user may access a file directly or indirectly, i.e., a copy of the file.

Mass storage file labels describe the attributes of the file. The attributes include file identification, file organization and structure, accounting information, type of data as well as optional user information. The label is normally transparent to the user, but the user may alter attributes (those that will not cause integrity or security violations) during the life of the file.

NOS/180 supports automatic permanent file archiving and retrieval from tapes and the Mass Storge Subsystem.

3.3.8.2 Basic Record Manager

The basic record manager supports sequential and byte addressable file organizations. The advanced access methods are described in section 3.4.3 on DMS180. The NOS/180 basic record manager design priorities are:

1) Support the FORTRAN user (performance, simplicity)

2) Provide an interchangeable file format between products

3) Support the Data Management and advanced access methods products

4) Support the COBOL user

5) Comply with ANSI standards.

The basic record manager provides a consistent interface to sequentially accessed files across all device types. There is at least one interchangeable file format among users of all compilers and system utilities.

Record manager provides record locking facilities for at least one mass storage file organization in support of shared files modified by concurrent users.

Record manager supports the record-partition-file hierarchy in a sequential file organization. These files are processed sequentially or randomly. Delimiters (e.g., record boundaries, partitions) and control information (e.g., compression, deleted records) are processed by the record manager.

The NOS/180 system files are processable by the record manager and are recorded using one of the standard file organizations. For record oriented files there is a single default file organization and record format that is used by all compilers and utilities.

3.3.8.3 Physical Input/Output

The physical I/O manager transfers data between memory and devices. A few primitive physical I/O functions are provided. They are device independent; the same function is defined for all devices and does the same thing for all where meaningful (if not an appropriate status is returned).

Physical I/O transfers byte streams and is unaware of the logical structure (e.g., records) of the file. Files are recorded on permanent media (tape, disk) such that the system can recover partially destroyed files and determine how much data was lost.

Physical I/O performance objectives are to:

- Minimize disk access time or tape "start-up" time
  - a) minimize the number of requests issued
  - b) transfer as much data as possible per request
  - c) achieve overlap between I/O and processing.
- Take advantage of maximum device transfer rates.

- Provide seek and latency optimization

3.3.8.4 Segment Level Access

A file may be associated with a memory segment so that the data elements can be referenced as a byte string in memory.

3.3.8.5 Device Handling

3.3.8.5.1 MAGNETIC TAPE

NOS/180 supports unlabelled tapes and ANSI standard labelled tapes. A file always resident on magnetic tape can be registered in the permanent file system.

3.3.8.5.2 ROTATING MASS STORAGE

Each rotating mass storage device is self describing such that usage information (e.g., device label, allocation and flaw map, file data) can be determined independent of information recorded external to the device. Flexible configuration capabilities are provided to allow for online reconfiguration and maintenance.

NOS/180 requires all mass storage devices of the same type to have the same sector size. Different device types can have different sector sizes.

Space is allocated on mass storage in terms of allocation units (one or more sectors). The system dynamically assigns allocation units to a file as it is written. The user can optionally specify the number of allocation units to be allocated to a file at any one assignment. NOS/180 also provides options to preallocate a specified number of allocation units to a file and to direct allocation to a specific device.

NOS/180 provides for removal and transport of mass storage devices within a system and between NOS/180 systems. A set concept is used to manage mass storage devices. A set is one or more logically related mass storage volumes. One volume can be a member of one set only. A set may contain one or more files, which may span volumes within a set but may not span sets. NOS/180 requires an online system set for system files, queue files and default residency for user files.

3.3.8.5.3 UNIT RECORD EQUIPMENT

The NOS/180 batch facility handles local and remote unit record equipment. It provides a unified external interface for users and operators to local or remote devices. This interface includes job structure, job/file routing and job control commands/displays. The batch facility uses the NOS/180 file interface to access local and remote batch devices.

3.3.9 SYSTEM MANAGEMENT

3.3.9.1 Resource Control

NOS/180 regulates all user access to system resources (e.g., device assignment, memory management, media mounting). Initial user validation based on user identification and mode of operation (e.g., batch, time-sharing, transaction) establishes limits for use of available system resource (e.g., devices, memory, CPU). The user may schedule the use of resources within those limits. Resources are assigned and released dynamically during task execution.

For named resources (e.g., mass storage files, tape files, volumes) NOS/180 maintains a catalog to associate the name with the resource, to regulate access to the resource, and to store attributes of the resource and its usage. Non-cataloged resources (e.g., tapes) are also processed by NOS/180.

Resources are made operational or non-operational at deadstart or by operator assignment or by the system error detection/recovery process. Operating system functions are provided to idle down and free up devices. Non-operational resources may be assigned to validated maintenance jobs.

3.3.9.2 Error Diagnostics and Recovery

NOS/180 emphasizes error checking and recovery. During execution NOS/180:

- logs errors in the system engineering file
- executes recovery sequences for peripheral equipments
- reconfigures around failed components

3.3.9.3 On-line Maintenance

Maintenance/diagnostic jobs may execute concurrently with user jobs. These jobs use standard job and operator services plus privileged operating system functions to assist in fault detection and isolation. Initiation of maintenance/diagnostic jobs and their use of system resources is subject to standard access control mechanisms.

The On-line Monitor is responsible for maintenance action when the Environmental Monitor detects an imminent system/device failure or when the IOU, processors or memory fail. If possible the failing element is dynamically reconfigured out of the system.

When the system cannot function normally, the appropriate diagnostic sequence will be initiated and the operator alerted. NOS/180 will attempt to save all jobs in process prior to giving control to a diagnostic sequence.

3.3.9.4 System Deadstart/Recovery

NOS/180 supports many configurations. The operating configuration is established or altered at deadstart. Several levels of recovery from system crashes are provided (e.g., recover jobs from the last system checkpoint, recover jobs in the swap queue, recover contents of input/output queues).

The on-line monitor alerts NOS/180 when a hardware system failure is imminent. The minimum level of recovery includes job and output queues, permanent files and all valid swap files. For an environmental failure the system is idled and a system checkpoint is taken ensuring the recovery of all jobs. Operators may idle the system and initiate the system checkpoint sequence at any time assuring recovery of the system environment after a restart recovery.

Most system software is replaceable in a production environment without requiring a system deadstart. Some operator scheduling control is required (e.g., idle the system) when changing the basic system modules.

3.3.9.5 System Statistics

NOS/180 records usage and performance information on system files. This information includes:

- job and system activities.
- usage statistics, equipment errors encountered and types of system recoveries. For non-fatal errors (e.g., solid single bit failures in memory), thresholds prevent logging the same error repeatedly.
- use of system resources and charge information.
- security events (e.g., access denials, user logins, configuration changes, access to secure objects).
- job and system execution data for performance analysis.

3.3.9.6 Accounting

NOS/180 accounting provides detection, measurement, and recording of system use for the purpose of billing and cost recovery. This includes:

- support for application accounting which allows authorized applications to unit price their services (e.g., charge for the number of plots produced rather than the resources used to generate the plots).
- consistent accounting information for each execution of a process based on a single billing unit that reflects all charges accrued by a job. The single billing unit is a function of detailed system usage information that is available to users and installations personnel to support charges. The usage information is recorded in a set of job resource and application usage counters. These counters are protected from direct access by a job but may be interrogated during execution with NOS/180 requests.
- installation options allow tailoring of which resource, usage events or services are to comprise the billing unit and of the relative "weight" of each datum used in the billing unit algorithm. Authorized applications may also alter the "weight" of each datum used in the billing unit.

- accounting information for resources or services whose use is controllable by the user is available in "user" terms (e.g., number of files accessed, number of linear equations solved).
- support of a hierarchy concept of accounts, projects within accounts and members (users) within projects. Limits can be placed on accounts, projects and users.
- support for billing and inter-installation cost recovery in multi-computer networks.

3.3.10 MINIMUM NOS/180 CONFIGURATION

	Ratio of Workloads (170/180)			
	100/0	70/30	30/70	0/100
Processor	1	1	1	1
Memory	1MB	2MB	2MB	1MB
I/O Unit	1	1	1	1
- PP's	10	15(10/2)	15(8/5)	5
- Channels	12	16	16	8
Mass storage spindles (100MB each)	2	4(2/2)	4(2/2)	2
Removable device for system installation	tape	tape	tape	tape or disk
Job input device	1	1	1	1
Job output device	1	1	1	1
System console	CC545	CC545	CC545	1

3.4 PRODUCT SET

A major CYBER 180 development constraint is to apply future CYBER 170 product set development to CYBER 180 wherever possible. Within that constraint, the CYBER 180 product set objectives are:

1) Span
Provide a single product set to span the CYBER 180 range without breaks in compatibility. Use common modules (code generators, run time libraries) where feasible.

2) Migration
Maximize user source code compatibility between the then-current CYBER 170 and initial CYBER 180 product versions.

3) Usability

Present a consistent external user interface across the whole product set. Minimize local conventions and special cases for one product.

4) Execution Efficiency
Exceed product set performance and reliability objectives established in Sections 7 and 8.

3.4.1 GENERAL PRODUCT SET TECHNICAL REQUIREMENTS

The following requirements apply to all product set members. Requirements on the production of object code do not apply to products which generate no object code (including interpreter).

- Code sharing will be supported:
  - Product set members will be sharable (i.e., one copy of code in memory at execution time which is utilized by all users).
  - Compiler generated object code will be sharable.
- Define and adhere to a common system interface standard to provide:
  - Object code communication across the product set (e.g., a COBOL program can call a FORTRAN subroutine).
  - Common object text format to allow the linking of object programs produced by two or more compilers.
  - One or more record and file formats common across the product set.
  - One or more data representations common across the product set.
  - Compatible external user interfaces to all similar CYBER 180 product set members, including the calls to all compilers, the output formats from all compilers, and diagnostic messages from all compilers.
- Provide statistical, performance and system debugging facilities for both system and user level use.
- For products covered by standards in Appendix B (e.g., BASIC, COBOL, FORTRAN), provide options to flag, accept and/or reject all non-standard statements.
- All compilers will allow:

  - Initiating a batch compilation by an interactive user.
  - Interactive communications with a terminal during execution of user programs.

- Common modules will be used where practical to provide reduced development and maintenance costs and consistency of results (e.g., common math library and numeric conversion routines.)

- CYBER 170 based products will retain their basic designs and techniques in their CYBER 180 implementations. Modifications are made according to the following guidelines:

  - Existing functional structures (e.g., phases/passes, overlays) are retained. These structures provide the logical grouping of code and data needed to assist NOS/180 memory management. NOS/180 commands and loader directives that manage those structures are not the same as NOS/170.

  - NOS/180 loader tables are similar to CYBER 170 and include separate sections for code and data. Loading functions interpret tables and organize code and data into separate segments.

  - Code is sharable among multiple users of a compiler. Separate data segments are assigned for each instance of execution. Product set programs are not aware of this sharing since it is managed by NOS/180.

  - Product set programs manage memory within their data segments according to conventions defined in the CYBER 180 System Interface Standard.

  - NOS/180 record manager is used for input and output files. The internal character data format is 8-bit ASCII.

  - Product Set software (Compilers, Data Management and System Utilities) is to be as independent from the operating system as possible. After the initial O.S. release, no new product release or re-release may require a new version of the O.S. If a particular feature requires special O.S. assistance, the remainder of the new product must still run on the previous operating system release.

3.4.2 LANGUAGES

The CYBER 180 language strategy is oriented towards three key user languages: FORTRAN, COBOL and BASIC. Each of these has a distinct orientation towards scientific, business, and time-sharing respectively. The importance of FORTRAN and COBOL in the marketplace is well-known, and both will continue COC strengths developed on previous machine lines. BASIC is currently the most common time-sharing oriented language.

These three languages will place a high premium on CYBER 170 compatibility in order to ease user migration, will have the stiffest requirements on performance (particularly FORTRAN), and will provide the fullest support of the language. Trade-offs in the operating system for product set support will be made in favor of these languages.

The remaining languages will play more supporting roles in the CYBER 180 product offering. A possible exception to this is APL, which is currently enjoying an increase in usage and could eventually equal BASIC in usage.

3.4.2.1 Compiler Classes

Another way of looking at the CYBER 180 language strategy is through the concept of compiler classes. This concept centers on the degree to which a language is supported and interfaced with the rest of the system. All classes will conform to the System Interface Standard.

A Class I compiler is fully supported and interfaced to the system in terms of feature richness, debugging aids, usability, interface to other systems, access to operating system features, etc.

A Class II compiler is not fully supported in all aspects but nonetheless provides an important language with heavy customer use. Certain characteristics will usually be stressed over others.

A Class III compiler will be required to meet only the minimum language standards and will be implemented and supported more as a free-standing application package. It is meant primarily to respond to RFP's and to be able to say we have it. A Class III compiler is expected to use common compiler elements (e.g., common syntax table generator) to the greatest extent possible,

3.0 CHARACTERISTICS AND FEATURES
3.4.2.1 Compiler Classes

even at the expense of performance.

Usage trends for class II and class III compilers will be watched closely and the relative priority of these compilers may change. For example ALGOL-60, ALGOL-68, and PASCAL all may be able to satisfy the non-U.S. market individually. If so, one will be picked and stressed over the others.

The following chart breaks down the CYBER 180 languages into classes and provides more detail on the level of support provided by each. The languages are listed in decreasing order of priority.

3.0 CHARACTERISTICS AND FEATURES
3.4.2.1 Compiler Classes

Degree Supported & Integrated	CLASS I: FORTRAN	CLASS II: COBOL	CLASS II: BASIC	CLASS II: ALGOL	CLASS II: C	CLASS III: PL/1	CLASS III: ADA	CLASS III: JOVIAL J73/I	CLASS III: PL/6
1) Usability features	H	H	H	M	M	M			
2) Debugging assists	H	H	H	M	M	M			
3) Code optimization options	H	H			M	M			
4) Access to operating system features	H	H							
5) Interface to other systems (e.g., DMS180)	H	H		M					
6) Handling variety of std.data types	H	H	H	M	M	M			
7) Common calling sequence	H	H	H	H	H	M	H	M	M
8) Compile speed and efficiency	H	H	H	H	H	M	M		
9) Speed and efficiency of generated code	H	H			M	M			
10) Conformance to ANSI/ISO Std.	H	H	H		H			M	
11) Extensions to standard	M		M						
12) Migration tools	H	H	M						
13) Training	H	H	H	M	M	M			
14) User documentation	H	H	H	M	M	M	M	M	
15) Performance Measurement assistance	H	H	M	M	M	M	M	M	M
16) Quality and size of test base	H	H	H	M	M	M	H	M	M
17) CYBER 170 compatibility	H	H	H	H	H	M	M	M	
18) Transaction interface	H	H							

H = extensive support
M = medium support
blank = little or no support

3.4.2.2 Individual Languages

- FORTRAN

This is the most important language for CYBER 180. It will provide both a production mode stressing execution speed and a development mode stressing compile speed and diagnostics; both modes will provide high-level ANSI-77

support. FORTRAN usage is expected to remain very high with virtually all sites using it; requirements will be driven by Systems.

- COBOL

  COBOL is almost as important as FORTRAN. It will fully support the new ANSI standard. The expanded BDP instructions of the CYBER 180 will make it much more performance competitive. The forecast is for increased overall usage by our customer base; requirements for COBOL also come from Systems.

- BASIC

  C180 BASIC is intended primarily for interactive use. BASIC will initially offer an interpretive mode and later an option to produce compiled object code. It will conform to the new ANSI standard plus extensions for enhanced C170 compatibility. Usage is expected to remain constant over the next 5 years; requirements come primarily from Services.

- APL

  APL is intended for interactive use. While the current forecast does not project an increase in use on C170 (still less than half of BASIC), some industry sources see a dramatic increase in use in the 1980's.

- ALGOL-60

  ALGOL requirements come primarily from Systems outside the U.S. Usage projections are not currently available; however, either PASCAL or ALGOL-68 could replace ALGOL-60 and its current position in that marketplace within the 1982 timeframe.

- PASCAL

  PASCAL is the language defined by Wirth, rather than the C180 implementation language, PASCAL-X. It is growing in popularity, particularly in the university and overseas environments. Requirements are driven primarily by Systems. PASCAL may be the best choice to push due to its acceptance in the U.S. and its potential for replacing ALGOL in the European market.

- PL/I

  PL/I is primarily intended to respond to RFP's and will be a minimal implementation. Requirements are driven primarily by systems.

- JOVIAL, ALGOL-68

  If provided at all, the primary requirement would be to satisfy RFP's. Specifically these two compilers will not be planned for development from R&D funds. Development would be tied to specific accounts and funded at least partially from COS.

  JOVIAL could be one of three defined variants; J3, J4 or J74. The requirement for JOVIAL would come from certain U.S. Government contracts. ALGOL-68 is completely different from ALGOL-60 and would not be a replacement unless marketplace abandons ALGOL-60 in favor of ALGOL-68. Requirements for ALGOL-68 would come from the overseas Systems markets, particularly from the academic world.

3.4.2.3 Common Compiler Elements

It is a CYBER 180 objective for compilers to share components wherever possible and practical, and where schedule permits. Listed below are the major areas of commonality to be considered:

- Common Code Generator (CCG)

  FORTRAN and SYMPL will both use the C180 CCG. COBOL, PASCAL-X, and BASIC will be designed so that they can eventually interface to CCG. Other compilers will be required to use CCG unless shown to be impractical.

- Common Math Library

  All mathematical languages (FORTRAN, ALGOL-60, PL/I, BASIC, APL, JOVIAL) will use a common math library, including numerical conversion routines.

- Common Syntax Table Generator

  This will be considered for all Class III, and perhaps Class II compilers. This can simplify the syntax analysis phase of compilation at the expense of compilation speed.

- Common Cradle Components

  The cradle code is those modules used by compilers and the common code generator to perform service functions. These modules should shield the compiler from the OS interface to provide a more easily changable set of compilers. Possible modules are I/O, control card cracking, cross reference maps, diagnostic interface, termination processing, etc. The use of common cradle modules must be enforced in certain areas for all compilers to achieve the degree of compatibility specified in the SIS.

- Common Debug Aids

  This covers such things as interactive debug, traceback, and post-mortum dump analysis. All compilers are potential users of these common components.

3.4.3 (#) DATA MANAGEMENT (DMS180)

The primary objective of DMS180 is to span the range of CYBER 180 processors and applications with a set of secure and compatible DMS capabilities. Target applications areas may be supported by separate products rather than one data base manager. The compatibility across separate products will be aimed at uniform user interface conventions, utilities and some forms of interchangeable media.

The basic vehicles for DMS180 are CYBER's DMS170 and EDMS systems. These products will be used as the design and experience base for selecting those DMS capabilities to offer as separate products in specific applications areas. Wherever feasible, existing CYBER 170 source code will be used to implement the elements of DMS180.

The future need for ANSI compliance is recognized although the current direction is obscure. DMS180 will support one data model which is oriented towards CODASYL and which will eventually provide a minimum level ANSI compliance.

DMS180 includes products supporting two distinct environments: file processing and data base processing. File processing is provided by the advanced access methods of the Record Manager; data base processing is provided by the DBMS. In addition, a complementary set of support functions will support both environments. These include a query language, data dictionary, and report writer. Unlike DMS170, DMS180 will stress the differences between the two environments in order to get the proper marketing mileage out of both. The emphasis will be on consistent and complementary external interfaces, common only where they should be.

3.4.3.1 File Processing

File processing capabilities will include:

- Advanced Access Methods (Direct, Indexed Sequential and Multiple Indexing) providing concurrent updating of a single file by multiple users.

- File Management utility supporting conversion between record manager files and to and from certain IBM formats, as well as record qualification, reformatting, etc. This utility will be functionally equivalent to C170 FORM but

will stress usability and consistency with other C180 DBM products over C170 compatibility.

- Except where provided explicitly by the language (i.e., COBOL) access to AAM files will be provided by a common set of interface routines for all Class I and II compilers.

3.4.3.2 Data Base Processing

The C180 DBMS will be based primarily on EDMS which provides a 3-level schema (conceptual, physical, and external) and CODASYL-type set processing as defined by the EDMS "COSET" approach. A long term objective is to provide support for the relational data model plus any CODASYL extensions required to meet the minimum ANSI standards. Support of a "DMS170 View" is described in Section 3.6.2, Product Set Transition.

The data base requirements described below define a "traditional DBMS" with little uniqueness over the competition with the exception of the EDMS philosophy on information processing and its 3-schema approach. AD&C is currently investigating the desirability of additional requirements/capabilities in support of our key industries and the scientific orientation of our traditional business. Such additional capabilities would be intended to provide a competitive edge in certain key areas, rather than just meeting the competition.

DBMS Requirements	Importance
- Concurrent access from transaction, batch, and interactive environments. In order to provide for ease of application checkout, and a better fit in the Services environment, the DBMS, as an optional capability should be able to execute in a non-concurrent mode.	High
- System is to be geared towards the transaction environment with the other two environments of secondary importance. User interface will be compatible across all three environments.	High
- Host language interface to all Class I compilers (FORTRAN, COBOL), plus selected Class II compilers where the need is clear. DML will be processed by a pre-processor rather than through modifications to the host language compiler.	High

- Data base integrity. This includes optional integrity constraints to prevent orphan records from existing in the data base, journal logging and audit trails, and proper coordination of concurrent processing.	High
- Dual logging and dual recording should be provided as an option.	Medium
- Data base security. This includes access control to the item level, access controls on data dictionary, schema, and utility usage and display, and prevention of direct user processing of data base files (i.e., circumventing the DBMS).	High
- Data base recovery. This includes off-line recovery using journal logs and automatic recovery from system failures, with minimal operator intervention, and on-line rollback of incomplete transactions. Coordination of recovery with user-defined, operator initiated and possibly automatically timed quiet points is required.	High
- Multiple data base support. The ability to process multiple data bases concurrently, and to add and delete data bases without having to take the DBMS down.	High
- Ability to "down" certain parts of a data base for repair, dumping, etc., without having to take the entire data base down.	Medium
- The DBMS access method will use, at a minimum, the basic access methods of the C180 Record Manager. It will, however, be transparent to the user, i.e., he will not be able to access the data base outside of the DBMS. Multiple access paths to data base records and data compression will be provided.	High
- Data Independence. Programs accessing data bases (or conventional files for that matter) will be independent of medium and device type, volume residency, and storage structure, format and address. Data base programs should be insulated from changes to the physical data base (e.g., a program should be tied to its	High

external schema; it should not have to be recompiled when the conceptual or physical schema is changed and the external schema does not). Trade-offs should be made in favor of increased program and data independence over performance or implementation convenience.

- Distributed Data Base and Multi-Mainframe Support. Medium
  The DBMS must be able to support a shared data base by multiple mainframes. Some form of distributed data base capability will be required; the extent and exact mechanism is not known at this time.

- The DBMS will be oriented towards medium and large size data bases, but must be able to handle very large data bases:

small	up to 1 million bytes
medium	up to 100 million bytes
large	up to 2 billion bytes
very large	up to 9 trillion bytes

- Maintenance ease. The design of the DBMS shall contain a maintenance mode to aid users isolate and document software errors. Where possible these aids should work automatically without having to be turned on. Medium

- Training. Must adequately cover the information theory behind EDMS as well as the standard "how to use the product." High

DBMS by its nature is a complicated product. It is therefore important that design tradeoffs be made in favor of ease of use and simplicity of installation over flexibility of capabilities and performance beyond the AD/R objectives. Reliability is also very important for DBMS as its use generally requires a major customer commitment and increased vulnerability of his operations to the system. In short, the DBMS should do what it does well and be easy to learn and use.

3.4.3.3 End-User Query Language

The C180 Query Language should appear to the user as a single product supporting both a conventional file and data base environment. First priority is support of data bases, conventional files is of secondary importance. The query

language provides extensive query capabilities, a simple update capability, and an expanded display capability providing at least headings, paging, and minimal formatting. The query language also interfaces to the stand-alone report writer for more complicated reports.

Query Language objectives include:

- The existing QU language will serve as the base specification. This will be significantly reduced in size and complexity, and minimal extensions added to support new capabilities of EDMS and the expanded display capability.

- A common language for both file and DBMS environments. Some language features will be restricted to one or the other environment.

- The query language should operate in both a batch and interactive mode.

- Where possible the query language should share common modules with C180 compilers. This ensures consistency of numeric processing and conversion, and reduces development costs.

- A stand-alone schema for conventional files will not be provided. Instead, the description will come from either end-user directives or the data dictionary.

- It would be desirable for a user to be able to process files and a data base at the same time. This allows him to interact between the two environments and to convert from one to the other. This has a low priority and will not be done if it overly complicates either environment.

Design tradeoffs in the query language will be made in favor of quality of code, and human engineering over performance and features. Where commands must take considerable processing time to complete, periodic statuses should be provided to keep the user informed of progress.

3.4.3.4 Data Dictionary

The C180 Data Dictionary System(s) will be used to describe both conventional files and DMS180 data bases. In the data base environment the data dictionary system will be integrated with the data definition capabilities of the DBMS.

3.4.3.5 Report Writer

The C180 Report Writer will be a stand-alone package which will be able to produce reports from both the conventional file and data base environments. It would be desirable for the Report Writer to be able to function both independently, without the need for an initial processing step with the query language, as well as in conjunction with the query language where it simplifies user processing. Report Writer directives, where possible, will be compatible with their C170 QU counterparts.

3.4.3.6 Foreign Systems

The system will not prevent the use of a foreign data base management system, e.g., TOTAL in lieu of the CYBER 180 DBM system. Foreign and CYBER 180 DBM systems are not required to share data bases but must be capable of sharing physical resources.

3.4.4 PRODUCT SET DESIGN OBJECTIVES/PRIORITIES

The priority matrices which follow indicate resource and design trade-offs to be made in planning subject products. Given that a product meets minimum feature level and functional/RAM performance requirements, design and resource optimization should be made in a manner which emphasizes the higher priority trade-offs. The definitions of these design trade-offs are:

COMPATIBLITY - Source level compatibility with the predecessor CYBER 170 product if no specification is noted in "REMARKS".

REAL MEMORY USE - The "working set size" (or maximum overlay length) to process a nominally sized task (compilation or other).

EXECUTION SPEED - For compilers, efficiency of generated object code in terms of CPU speed in executing representative sequences of code; for other products, CPU and throughput time to process representative product inputs.

COMPILE SPEED - CPU and throughput time to process source input.

CODE COMPACTION - Efficiency of generated object code in terms of instruction space necessary to execute representative sequences of code.

TEST BASE SIZE - A wide range of user applications is expected to be run against this product. Where resource trade-offs exist, they should be directed toward a large and comprehensive test base.

FEATURE RICHNESS - Emphasis is to be given to adding user or marketing requested features to this product beyond those necessary to minimally support standards and other products requirements.

3.4.4.1 Language Processors

	PRODUCT TRADE-OFFS						
	F	R	E	C			
	E	R	E	C			
	A	E	X	T	O		
	C	T	A	C	E	E	D
	O	U	L	O	C	S	E
	M	R	M	U	T	T	
	P	E	M	P	T	T	C
	A		E				B
	T		R	M	L	O	A
				O	E	N	S
	B	C	R		E	A	
			H	Y	S	S	C
	L	N		P	P	S	T
			E	U	E	E	
	T	S	S	E	E	Z	O
	Y	S	E	D	D	E	N
REMARKS							
ALGOL-60	1		2			3	Compatible with ALGOL5
ALGOL-68	1		2				Compatible with COC Holland version
APL	1	2	3				Compatible with APL2 (APLUM)
BASIC	1	3					Compatible with ANSI 7X over 170 extensions 2nd priority=interactive usability
COBOL	1	3			2		
FORTRAN							1981 FTN5 over ANSI 7X
PRODUCTION	2			1	3		
DEVELOPMENT	3	2	1	1			
JOVIAL	1			2			J3 variant
PASCAL			2	1	1		
PL/I	2				1		Exists to satisfy RFP's

3.4.4.2 Support Services

	PRODUCT TRADE-OFFS				
	F	R			
	E	E	E		
	A	A	X		
	C	T	L	E	
	O	U		C	
	M	R	M	U	
	P	E	E	T	
	A		M	I	
	T	I	R	O	O
		I	I	R	N
	B	I	C	Y	
		I	H		S
	L	I	N	U	P
		I	E	S	E
	T	I	S	E	E
	Y	S		O	
REMARKS					
Basic Record Manager	3	1	2	1	1
Loader		3	1	2	1
Sort/Merge	2	1	3	1	1

compatible with Sort/Merge 5.0

3.4.4.3 (#) Data Management (DMS180)

EASE OF USE	TEST BASE SIZE	EXECUTION SPEED	REAL MEMORY USE	FEATURE RICHNESS	COMPATIBILITY	REMARKS
Access Methods		3		2	1	Compatible subset of C170 access methods
File Mgmt Utility	1		3		2	Compatibility with FORM
DBMS	3			2	1	
DBMS Support Utilities	1			3	2	
DDL	2			3	1	Execution speed of DBMS
Query Language	1	1		2		3 Compatibility with C170 QU
Data Dictionary	1		2		3	
Report Writer	1		3		2	Compatibility with C170 QU

3.4.5 UTILITIES TO BE SUPPLIED

PROGRAM ORIENTED	Source code maintenance
	Object code maintenance
	Link editor
	Line and text editor
	Text and source code formatters
	Debugging aids
DATA ORIENTED	General utilities
	Copy (records, partitions, files)
	Compare
	File display
	Data management
	Index management
	Restructure/reorganization
	Usage analysis
	Log/audit
	Recover/restore
	DB creation
	File conversion/reformatting
MEDIA ORIENTED	Initialization
	Dump/restore
SYSTEM ORIENTED	Maintenance log analysis
	System use log analysis
	Dump/load job queue
	System generation/modification
	Terminal use
	System/job/file status
	Message capability
	Permanent files
	Dump/load
	Audit
	Archiving
	Print memory or file
	Volume initialization
	User validation
	User accounting
MIGRATION CONVERSION AIDS	APL work space conversion
	File conversion
	Data conversion
	Program conversion

3.5 SECURITY AND PROTECTION

CYBER 180 will comply with section IV of D.o.D. Directive 5200-28M.

The security objectives for CYBER 180 software are to prevent

1) unauthorized access to information
2) unauthorized information modification
3) unauthorized denial of use

in an environment in which multiple users with multiple levels of clearance will be accessing and sharing computer resources, programs, and data which have multiple levels of accessibility.

The five major components of the CYBER 180 operating system security capabilities are described below.

1) Identification - Every user of the system has a unique identification that is used to regulate access to the system and its resources. Interfaces are provided that allow installations and users to regulate job initiation and termination sequences.

2) Control Access - Access control lists are the basic resource protection mechanism. They identify all legal users of a resource and the user's mode of access. Each resource known to the system has a single owner who is responsible for the resource, its usage, protection and accounting. A single module of code is responsible for assuring that resource access is in conformance with the access controls for that resource. Interfaces are provided that allow installations and users to provide additional control of user access to resources and information. Access to resources is regulated according to:

   .the level of access of the user
   .the level of allowed access for a resource
   .the security level of the system environment, both internal and external.

   For example, a request for execution of a secure program by an authorized user could be

   prohibited if general purpose time sharing sessions are active.

3) Integrity - The segment and ring memory protection capabilities of CYBER 180 hardware are used to control access and to isolate the activities of concurrent users.

4) Surveillance - A system log describing security related events is maintained.

5) Protection - optional data encryption is provided.

- The overall protection objectives for CYBER 180 are to protect the user from other users, the system from users, users from the system, and system elements from other system elements.

- Data will be protected at the:
  - file level
  - record level (through Record Manager)
  - element level (through DMS180)

3.6 (#) MIGRATION

Migration is the process of moving COC products and its customer base from the CYBER 170 to the CYBER 180. It must provide a set of CYBER 170/CYBER 180 product capabilities and conversion aids which will minimize the impact of migration on the user base over an extended period (10 years).

Initial CYBER 180 hardware will be introduced and supported as Advanced 170 systems which are capable of replacing a CYBER 170 mainframe and executing its code. CYBER 190 software (NOS190) will be introduced later.

CYBER 180 target specifications to support migration include:

- the definition of the user interface for the operating system based on CYBER 170 NOS.

- source language definitions that are the same for CYBER 170 and CYBER 180.

- program and file conversion aids that assist the user in

moving to the CYBER 180.

- a dual state execution environment wherein both CYBER 170 and CYBER 180 workloads may be processed concurrently.

3.6.1 OPERATING SYSTEM IMPLICATIONS

3.6.1.1 Dual State Processing

NOS/180 processes either NOS/180 and NOS/170, or NOS/180 and NOS/BE 170 jobs. The initial design model for dual state processing is that of a symmetric link configuration, one executing NOS/170, the other executing NOS/180. This sharing of a single mainframe is known only to the most basic elements of NOS/180.

3.6.1.2 Dual State Requirements

The following dual state functions are provided through NOS, NOS/BE and NOS/180. Where tradeoffs must be made, NOS/BE migration and conversion support takes priority. Wherever possible dual state functions are symmetric between C170 and 180 states.

- Ability to submit a job from one state to the other state.
- Ability to status and control jobs across the dual state from a terminal or operator console.
- Ability to select C170 or C180 primary mode of execution at interactive login
- Support the symmetric link protocol between states. Provide standard requests to send and receive messages across the link.
- Support for the C170 multi mainframe link functions (e.g., get and save permanent files, route files, etc.) for file access across the link.
- Provide mechanisms for OWNCODE exits on a file basis. These exits will allow communication across the dual state link with system-supplied record access routines.

- Programs accessing files in the other state need not be recompiled when the file is moved to the program's state. Control card changes are permissible.
- Dual state operational control is provided from a single operator console (similar to NOS/BE multi-mainframe) where NOS/180 displays are a subset of NOS/170. At deadstart; memory, PP's and channels are assigned to the C170 state or C180 state until the systems are idled and a recovery deadstart is taken. Dual access controllers may be accessible by both states concurrently but not through the same channels. Device assignments may be switched between states by operator control.
- In a multi-mainframe environment external mainframes view the dual state processor as two mainframes and interface to either the C170 or C180 O.S. directly via the symmetric link.
- Dual state must support the following RAM requirements:

  An O.S. failure in one state cannot cause an O.S. failure in the other.

  Independent recovery deadstart is desirable; idle down of one state while the other is being deadstarted is acceptable.

  One MCU/control facility supports both states.

  On-line maintenance, error logging, etc., for NOS, NOS/BE and NOS180 are centralized.

3.6.1.3 Operating System User Interface

The CYBER 180 Operating System target specification is based on NOS/170, modified as necessary to present a consistent user interface across the various modes of access and to accommodate new hardware features. On an exception basis, important NOS/BE capabilities will be in the target specification. Subsequent CYBER 170 development will bend toward that target specification to achieve a more uniform user interface when NOS/180 is released.

3.6.2 PRODUCT SET TRANSITION

The objective is to offer application source code compatibility between the CYBER 180 product and the CYBER 170 1981 products. This can be achieved by:

- Implementing the product or front-ends on the two machines to a common external specification.
- Using a common test base.
- Carrying across the product (or its front-end) written in a common implementation language.

The emphasis for "new" CYBER 170 front-ends and products will be to code in SYMPL for both CYBER 180 and CYBER 170 systems, i.e., machine independent implementation.

Existing CYBER 170 products (or those in development) written in SYMPL will be made more transportable by supporting SYMPL on CYBER 180.

3.6.2.1 FORTRAN

CYBER 170 Base - FTN5

- Successor to FTN4
- Breakages will be introduced to reduce machine and data dependent usages. Usages such as SHIFT and MASK operations, Hollerith data, etc. will be flagged and require manual conversion.
- Breakages will be introduced for ANSI compliance and to remove archaic usages. 98% of the jobs so affected will be translatable by conversion aids

CYBER 180 Product

- FTN5 reimplemented in CYBER 180 Implementation Language
- Use common code generator
- Same external specification and test base as CYBER 170 version

- Machine and O.S. dependent breakages only. A conversion aid will be provided to flag possible machine dependent usages for hand translation and to convert O.S. dependent breakages (e.g., OVERLAY) where possible.

3.6.2.2 COBOL

CYBER 170 Base - COBOL 6

- COBOL 5, extended to meet ANSI-79 requirements
- 100% conversion aid coverage of COBOL-5 to COBOL-6 breakages

CYBER 180 Product

- COBOL6 Front End transported to CYBER 180
- New code generator
- Breakages only in areas of O.S. Support and machine dependent data types. A conversion aid will convert all those breakages that can be converted; those that cannot will be flagged to aid in hand translation.
- Control card option to compile C170 COBOL 5 programs as required by new ANSI standard. Will work for all programs unless unsupported system capabilities used or machine dependent data manipulation done.

3.6.2.3 SORT/MERGE

CYBER 170 Base - SORT/MERGE 5

- New compile phase meets CYBER 180 System Interface Standards
- S/M5 processes old and new sort directives, no conversion aids

CYBER 180 Product

- S/M5 compile phase
- New sort phase

- No conversion aids other than system utilities for file conversion.

- Breakages in areas of OS support and data dependencies.

3.6.2.4 BASIC

CYBER 170 Base - Interactive BASIC 4

- New implementation; runs interpretively and produces object code

- Modest feature enhancements to 1977 BASIC 3

- Removes semantic deviations from ANSI-78 BASIC

- 100% conversion aid coverage for data-independent language differences.

CYBER 180 Product

- BASIC 4 front end and interpreter transported to CYBER 180

- Compliant with expanded ANSI standard; retains non-conflicting extensions from CYBER 170 BASIC 4

- Very few breakages and only in area of O.S. support; all of these will be diagnosed by the compiler.

- No object code available from early version.

3.6.2.5 ALGOL-60

CYBER 170 Base - ALGOL 5

CYBER 180 Product

- ALGOL 5 front end transported to C180

- Machine and NOS/180 dependent breakages to be diagnosed by the compiler

3.6.2.6 APL

CYBER 170 Base - APL2 (APLUM)

CYBER 180 Product

- A new implementation compatible with APL2 (APLUM)

- Breakages only in areas of O.S. support and machine dependent data types

- Will be able to convert C170 APL work spaces and files

3.6.2.7 PASCAL, JOVIAL, ALGOL-68, PL/I

The CYBER 170 base for these products is too small to warrant special migration planning.

3.6.2.8 DMS180 User Migration/Product Transition

DMS180 will be designed to support a "DMS170 View" to help ease user migration. Providing a 100% compatible DMS170 View will not be possible in either the DDL or DML. The major emphasis will be placed on migration of user source programs and sub-schemas wherever possible. The actual implementation decision will be deferred until 1981 and will depend on the number of active users of CDCS.

The approach will be to translate existing CDCS data structures (relations) into the equivalent DMS180 structures (sets). A conversion utility will translate CDCS calls within user COBOL and FORTRAN source programs into equivalent DMS180 DML statements. The DMS170 data model will not be processed directly by DMS180. Some form of conversion aid will be required to convert a data base from DMS170 to DMS180.

3.6.3 FILE CONVERSION

3.6.3.1 Off-Line

A symmetric (between C180 and C170) set of copy and conversion utilities will be provided for tape-to-tape and

disk-to-tape-to-disk file conversion. They will handle:

a) All access methods and record types supported by C170 Record Manager (V1.4 and V1.5).

b) All C170 character codes to/from ASCII.

c) C170 18-bit integer to/from C180 half word.

d) Full word integer and floating point.

e) ANSI 69 (read only) and ANSI 76 labels.

f) 7600 SCOPE 2, Sequential and Word Addressable file organizations.

g) 3000L, MASTER Sequential and Linked Indexed Sequential.

3.6.3.2 On-Line

When executing in dual state, a program may access disk files from the other state. Access to 170 files from the 180 state is mandatory. Access to 180 files from the 170 state is required unless that access is damonstrated to be seldom-used or prohibitively expensive to implement.

3.6.3.2.1 SYSTEM SUPPORTED

Single data type (character *, integer or floating point) files can be accessed on a file or record basis.

a) Files of the following types may be transmitted, in their entirety, between states:

- Sequential organization, record type W or Z, block type C

b) Files of the following types may be designated for record-level access between the states:

- Sequential organization, record type W or Z, block type C

- Index Sequential

* 6-bit, one code type for 170, 8-bit ASCII for 180.

3.6.3.2.2 USER INTERVENTION

On a file basis, OWNCODE exits will be supported which allow a user to request a raw binary record from the other state, convert data fields as necessary and return the record to its requesting program. (Disk) file types to be supported are:

- Sequential
- Indexed Sequential

Any CYBER 170 file can be accessed on a PRU basis. An entire file or a single PRU can be transmitted between states. The user program or owncode exit is responsible for interpretation and conversion of the PRU content.

3.7 MAINTENANCE SOFTWARE

Maintenance Software is organized into three major categories:

1) On-line Monitor
2) Off-line Monitor
3) Tests, Diagnostics and Utilities

The functional objectives for CYBER 180 Level II and III Maintenance Software are described in the following paragraphs. These objectives apply to both the CYBER 170 and CYBER 180 states of operation except where noted otherwise.

3.7.1 ON-LINE MONITOR

The CYBER 180 state On-line Monitor shall improve maintainability of system critical elements by:

1) Observing system operation via hardware RAM features.
2) Reporting and logging errors.
3) Activate/deactive hardware RAM features as requested by the OS and/or tests and diagnostics.
4) Notifying OS of hardware failures.
5) Being designed to function in a "crash-proof" manner to ensure retention of pertinent failure data.
6) Providing a console interface to the maintenance engineer both locally and remotely. However does not supply the remote access driver software.
7) Monitoring system mainframe components (processors,

memories, IOU) for environmental power faults and warnings. It shall be independent of hardware failures, except its own, and independent of Operating System failures.

In addition, the on-line monitor shall:

- Limit the equipment dedicated to the on-line monitor to a maintenance channel and PP for CYBER 180 state, and to a maintenance channel for CYBER 170-state.

- Be logically independent from the system. A failure of these facilities will not cause a system failure.

3.7.2 OFF-LINE MONITOR

The Off-line Monitor shall:

1) Provide a load and control capability for both CYBER 180 and CYBER 170 tests and diagnostics.
2) Provide ability to examine failure information on system critical devices as collected by the On-line Monitor.
3) Support verification, manufacturing, and the field environment.
4) Support remote maintenance.
5) Provide for total system exercising and verification.
6) Provide capabilities for mainframe initialization.

3.7.3 TESTS, DIAGNOSTICS, UTILITIES

1) Detect, identify and isolate hardware malfunctions in the CYBER 180.
2) Verify hardware operation prior to customer use and after repair.
3) Where possible, be able to execute in an on-line and off-line mode.
4) Provide equipment and media performance history, analysis, and predictions.
5) Provide maintenance procedures based on performance history.
6) Provide "truncated" versions of CYBER 180 tests for initializing the hardware needed for on-line or off-line system operation.

3.8 NETWORKS

CYBER 180 network products support data transmission among host computers, and between host computers and terminals over communication lines. Single and multi host configurations are supported using the CYBER 170 Network Processing Unit (255X or successor) hardware and software products. This interface allows the addition of a CYBER 180 host to an existing CYBER 170 network.

The CYBER 170 host network software is the base of CYBER 180 host software. The Network Access Method (NAM), Communications and Network Supervisors (CS, NS), and Network Definition Language (NDL) implementations will be used where they meet the structure of NOS/180. NAM will have a dedicated PP to interface to the front-end NPUs. The Remote Batch Facility (RBF) will support local and remote batch devices.

The NOS/180 host network software separates the communication function from other processing and manages the sharing of the data communication network by multiple application programs. Each program utilizes a consistent interface that provides logical connections to all terminal types. The NPU presents a virtual interface to the host for batch and interactive terminals, so that terminals appear similar to the host application programs. The network software includes buffering and queueing to efficiently configure large numbers of slow devices. Up to 10,000 active terminals may be connected to a host computer. Any application may access up to 10,000 active terminals.

The terminal types and line protocols supported are described in Appendix C. Asynchronous lines may operate at standard rates between 110 and 9600 bps. Standard speeds are 110, 134.5, 300, 600, 1200, 2400, 4800 and 9600 bps. Synchronous lines may operate at speeds between 2000 and 56,000 bps. Inter-node trunks may operate at speeds up to 56,000 bps (or higher if general industry trends dictate).

The NOS/180 file interface can be used by user and system applications to access network devices. This allows a program to handle network and non-network devices with one interface.

Support tools for managing Network Processing Unit software are provided with NOS/180.

4.0 COMPATIBILITY OBJECTIVES

4.1 WITHIN CYBER 180

CYBER 180 will present a compatible data interface that is accommodated across the line. This objective includes provisions for:

- Single instruction set across the CPU range.
- ANSI standard data representation on cards and tape.
- CYBER 180 standard data formats (internal and external).
- CYBER 180 standard disk recording formats (physical and logical file level) for each transportable media type.
- CYBER 180 standard operating system interface.

The CYBER 180 standard data formats are:

- 8-bit bytes.
- Internal representation of character data in ASCII, with special CPU provisions to take packed decimal data that had been previously translated from EBCDIC to ASCII and translate it back to its original representation.
- Fixed point numbers, 32 and 64 bit 2's complement
- Floating point numbers, 64-bit (single precision) and 128-bit (double precision) signed magnitude. The results of the CYBER 180 floating point instructions will be arithmetically compatible to the normal range of CYBER 170 floating point normalized unrounded results.
- Signed and unsigned packed decimal numbers.
- Signed (embedded and separate/leading and trailing) and unsigned zoned decimal numbers.

4.2 MEDIA INTERCHANGE

Device	Physical Recording	Conversion Code	Logical Structuring
7 Track tape	ANSI 200bpi NRZI (read only) 556bpi NRZI 800bpi NRZI	BCD	1977 ANSI standard
9 track tape	ANSI 800cpi NRZI 1600cpi PE 6250cpi GCR	ASCII EBCDIC	1977 ANSI standard
80 column cards	ANSI	ASCII 029 026 Transparent	Card Image

4.3 MAINTENANCE SOFTWARE

Predecessor Products

It is a goal of the Maintenance Software to use certain existing CYBER 170 maintenance programs. This software shall have the same external diagnostic/test procedures when run either in the CYBER 170 or the CYBER 180 state.

Companion Products

Level III Maintenance Software must perform with all operating systems supported in CYBER 180 state.

5.0 SYSTEM ENGINEERING

5.1 STANDARDS

The CYBER 180 systems will comply with all applicable CDC and industry standards. Any deviations will be identified with waiver statements in product design documents. See Appendix H for the full standards list.

5.2 TOOLS/SERVICES FOR CYBER 180/170 DEVELOPMENT & MAINTENANCE

This section gives general direction for managing the design and development of the set of software tools to be used in the migration of our software set from CYBER 170 to CYBER 180.

The design objectives for Tools and Services will be - in priority order:

1) Allow product set members spanning the CYBER 170 and CYBER 180 operating systems to be developed and maintained in one form, using the same tools.

2) Support the development and maintenance of products to be used in a dual OS state environment (CYBER 170 state and CYBER 180 state).

3) Support the requirements of the CYBER 180 OS development project and their language, PASCAL Extended (PASCAL-X).

4) Ease the transition of CYBER 170 trained programmers onto the CYBER 180 system.

The CYBER 170 will be the primary software development vehicle for early releases of CYBER 180 software. Both ARHOPS and SVLOPS development sites will have C170's dedicated to C180 development running the same set of tools under NOS170. These systems will be stabilized versions of NOS 170.

The C180 Development Support System, DSS180, will be the central tools agency to develop major tools and to ensure commonality and stability of the tools at the development sites.

All tools will be interactively oriented as well as usable in batch mode. The tools will be structured as an integrated system, providing simple and fast primitives usable in combination. System building/checkout capabilities will emphasize binary module replacement and incremental, continuing software integration.

The standard mode of release of software is binary code. C180 development tools and CPU system source code will be available to customers as an extra cost option.

The great majority of C180 system programming, including tools, will be developed in high level language, hence the tools requirements include language processors and subordinate tools.

The anticipated heavy dependence on C170 systems for the bulk of C180 development makes it very important that the major OSS180 tools be of releasable quality. In particular, they should support the CYBER 180 System Interface Standard and System Command Language interfaces and should track the NOS/180 command and program interfaces. This includes supporting files in full 8-bit ASCII. All new tools should be written in PASCAL-X for the 170, and designed and coded to transport with minimum effort to the CYBER 180.

Testing of CYBER 180 software will involve heavy use of automated testing aids which are also part of the tools requirements.

5.2.1 LANGUAGE PROCESSORS

General

a) Higher level languages will be used for CYBER 170/180 system programming.

   1) Products designed for release only on CYBER 180 will be written in PASCAL Extended.

   2) Products designed for release on CYBER 170 will use SYMPL.

   3) Products designed for release on both 170 and 180 will use SYMPL.

   4) Subject to AD&C approval, compilers and their object time routines may be written in their own language, where there is a significant cost advantage to do so.

b) The need for assemblers is acknowledged. In practice initial implementation will be in higher level languages. When tuning, critical modules will be redesigned for the assembler as dictated by performance and hardware considerations. Because of severe memory constraints of the CYBER 170, CYBER 170 state codes usually resident in central memory will be done in assembly language.

c) PPU code will be done in assembly language. CYBER 180 PPU source code will not be released to the field.

Environment

Close coordination with tools subsystems is mandatory, with special emphasis on:

a) Coexistence with the source code maintenance subsystem.

b) Separate specification of frequently used declarations for centralized control and flexible access by PASCAL Extended and Assembler modules with minor degradation in compile speed.

c) Assembler Linkage

- Definition in the System Interface Standard.
- Minimum overhead linkage.

5.2.2 ASSEMBLERS

5.2.2.1 Internal

The source code for CPU microcode or PPU and Basic operating system and diagnostic code (180 state only) will not be released.

Microcode assemblers are controlled, documented and maintained by the responsible engineering development division. They are not to be released.

The internal PPU assembler is an extension of the C170 COMPASS PPU assembler.

5.2.2.2 External

There will be one external assembly language definition and implementation for the CYBER 180 CPU and IOU. The CPU portion must accept PASCAL-X variable, type and constant declarations.

5.2.3 LIBRARY SUPPORT AND CONTROL

In general, existing CYBER 170 products will be used as the design base for these packages. Transition plans will be prepared for each, showing additions and deletions necessary to operate in an interactive/batch environment and to meet the CYBER 180 System Interface Standard.

The product capabilities listed below are a minimum set. They are in priority order with regard to the importance of providing a compatible bridge between CYBER 170 and CYBER 180:

a) One source code maintenance package compatible to UPDATE in that it can create 180 PL's from 170 PL's, and a utility to generate a 170 PL including folding 8-bit characters to 6 bits.

b) "Common deck" capability - available for both source code and job deck maintenance.

c) Object code library maintenance package capable of handling code produced by any of the language processors, based on LIBEDIT.

d) Job Deck Maintenance - dynamic modification and selective execution of jobs for use in libraries of test and system generation jobs, similar to DEVOUR and included in a), above.

e) Modification Change Control, similar to the Production Control System (PCS), to include modules' histories of change rate.

5.2.4 OTHER SUPPORT PACKAGES

a) Documentation facilities - TEXTFORM with improved usability.

b) Produce global cross reference listings for the OS and

Product Set, to include data items, module names, and error messages for PASCAL-X, SYMPL and the assembler.

c) Simulate the CYBER 180 as a system, with a simulated to real instruction performance ratio of 1000 to 1.

d) Simulate the CYBER 180 CPU with soft simulation of OS I/O requests.

e) A fast file transfer capability for 8-bit or binary information via communications line between the ARHOPS and SVLOPS development systems.

f) A form of channel coupled link between the ARHOPS development CYBER 170 and the checkout CYBER 180.

g) Symbolic interactive debugger for PASCAL-X and Assembly language.

5.2.5 TEST BASE DEVELOPMENT

a) Standards and automated result checking routines for positive and negative testing.

b) Support the requirement that test case definition be an integral part of a test, and that tests are characterized and indexed for automated retrieval.

c) A stimulator will be required to simulate interactive usage and remote batch traffic in order to test the communications capabilities of the total system.

d) O.S. performance kernels to allow repetitive and weighted verification of O.S. instruction allocations.

e) RMS I/O performance kernels to test streaming rates and average random access rates.

f) Utilities to monitor code coverage during test base execution.

5.2.6 EXTERNAL DISTRIBUTION

The following CYBER 180 tools (at least) will be available as Central Enhancement and Maintenance Services (CEMS) products in CYBER 180 mode:

SYMPL
PASCAL-X
ASSEMBLER
UPDATE
LIBEDIT

"Cross-products" (executing on C170, producing code for C180) will not be released without explicit permission from AD&C.

6.0 PRODUCT PHASING OBJECTIVES(#)

6.0 PRODUCT PHASING OBJECTIVES(#)

It is a design objective to accommodate a phased implementation and release of selected products, functions, and features consistent with the major design objectives identified in Section 1.3.

The first release of the Network Operating System for CYBER 180 (NOS/180) will have limited features and will be provided to selected customers. The major orientation of this release will be towards supporting mixed CY170/CY180 job stream processing and providing the first set of conversion aids. NOS/180 Release 1 (R1) will provide a limited production capability; production or operations in the NOS/180 R1 timeframe is expected to be performed in CY170 mode with NOS/170 or NOS-BE.

NOS/180 Release 2 (R2) will provide a production environment while continuing the emphasis on migration and conversion aids (particularly for NOS/BE 170). NOS/180 R2 will be a complete release within the schedule constraints. Only seldomly used products, functions or features will be deferred. NOS/180 Release 3 will be a complete and competitive release. The following provides an overview of product phasing by major program elements:

Notes: 1) C170 indicates a capability provided by C170 software and used by the 180 system.
2) A single X indicates full capability with normal enhancements in later releases
3) Multiple X indicates phasing of the capability.

6.0 PRODUCT PHASING OBJECTIVES(#)

Capability	NOS/180 R1	NOS/180 R2 (Incl.R1)	NOS/180 R3 (Incl.R2)
I.Operating System			
A)Hardware Support	(See Appendix C)		
B)System Capabilities			
Normal State-Maintenance State	X		
Dual State	X		
Submit and control a job			
To C180 from C170	X		
From C180 to C170		X	
File/Record			
Copy by C180 Job	X		
Copy by C170 Job		X	
Route to C170 by C180	X		
Record Access to C170 File	X		
Linked Mainframes (Jobs, Files, Message)			
NOS/180 to NOS/170 or NOS-BE			
Dual State Link	X		
Channel Link (6683)		X	
Remote Link			X
NOS/180 to NOS/180		X	
Channel Link (6683)		X	
Remote Link			X
Multi Mainframes (shared RMS/FE)			X
User Access Control			
User Validation	X	X	
Families-Prolog/Epilog	X		
Limit Monitoring	X		
Security Levels			X
Secure State			X
Logging			
System, Acct., CE,			
Job Statistics	X		
Accounting			
SRU, Cost Recovery, Installation Hooks	X	X	
Application		X	
Program Services			
Tasking	X		
LOADER-Object Libraries,	X		
Time, Date, etc.	X		
Queues, Signals	X		
User Aids			
HELP	X	X	X
Debug	X	X	X

6.0 PRODUCT PHASING OBJECTIVES(#)

Capability	NOS/180 R1	NOS/180 R2 (Incl.R1)	NOS/180 R3 (Incl.R2)
Performance Analysis	X	X	X
Editing	X	X	
Source Code Maintenance	C170	X	
C)Job Capabilities			
Job Type			
Standard	X		
Maintenance	X		
Basic transaction support		X	
Full transaction support			X
Job Submission			
Batch Devices (Local/Remote)	C170	X	
Interactive Sessions	C170	X	
Executing Program	X		
Job Scheduling			
Basic Priority,Operator Tuning	X		
User Priority	X		
User Defined Events			X
Job Dependency		X	X
Job to Job Communication		X	
Command Language			
Procedure-Basic Structures	X		
Extended Structures		X	
D)Storage Capabilities			
Mass Storage Files			
Permanent-Queue-Temporary	X		
Magnetic Tape Files			
Basic support, Labelled, Unlabelled	X		
FULL ANSI support	C170	X	
Permanent (cataloged)			X
Mass Storage Sets			
Family-Online	X		
Removable-Auxiliary		X	
Magnetic Tape Volumes			
Auxiliary Volume-Volume Sets	X		
Family Volumes (Tape			
Reservation)			X
Catalogs			
Master, Access Control	X		
Subcatalogs		X	
Permanent File Utilities			
Dump, Load, Audit	X		
Archiving - To/From Mag Tape			X

6.0 PRODUCT PHASING OBJECTIVES(#)

Capability	NOS/180 R1	NOS/180 R2 (Incl.R1)	NOS/180 R3 (Incl.R2)
File/Set Utilities			
COPY File/Records/Partitions	X		
Initialize, Add, Delete,			
Recover Set	X		
Basic Record Manager			
Sequential,Byte Addressable	X		
Record Formats			
H,U,170 Interchange	X		
ANSI Record Formats		X	
File Access			
Physical Read/Write	X		
Record Manager	X		
Segment Access	X		
File Sharing			
Exclusive Read/Write -			
Multi Read	X		
Multi Re d, Single Write	X		
Multi Read, Multi Write			X
Memory Management			
Segment Allocation-Swapping	X		
Paging - Rings	X		
Key/Lock			X
E)RAM Capabilities			
Checkpointing			
System Initiated (of System)	X		
Job/Program Initiated (of Job)		X	
System Idle (Initiated by			
System/Operator)	X		
Operator Initiated (of Job)		X	
Restart			
Deadstart Recovery of System			
(Operator)	X		
Job/Program (Job Initiated)		X	
Job (Operator Initiated)		X	
System Initiated	X	X	
Hardware Errors			
Detection	X		
Error Logging	X		
Error Recovery (retry,etc)	X		
System Idle			
Operator Initiated	X	X	
Environmental monitor	X	X	
Reconfiguration			

6.0 PRODUCT PHASING OBJECTIVES(#)

Online, operator controlled			
Basic (On/Off equipments)	X		
Extended (Reconfigure,add,etc)		X	
Dynamic by system due to error detection		X	
Maintenance mode	X		
Online Maintenance (maintenance and repair)			
Mass storage	X		
CPU (second of dual)		X	
Magnetic Tape	C170	X	
Unit record	C170	X	
2550	C170	X	
Remote Maintenance	C170	X	
Common Test & Initialization(CTI)	X		
Online Diagnostics (periodic confidence testing)			
Mass storage	X		
CPU	X		
Memory	X		
Magnetic tape	C170	X	
Unit record	C170	X	
2550	C170	X	

6.0 PRODUCT PHASING OBJECTIVES(#)

Capability	NOS/180 R1	NOS/180 R2 (Incl.R1)	NOS/180 R3 (Incl.R2)
II.Product Set			
FORTRAN 5	X		
COBOL 6	X	X (MCS)	
BASIC 4	X		
SORT/MERGE	X		
ALGOL 5		X	
APL		X	
PASCAL (WIRTH)		X	
PL/I			X
SYMPL	X		
PASCAL-X	X		
Assembler	X		
Advanced Access Methods			
Direct Access		X	
Index Sequential	X		
Multiple Index		X	
File Maintenance Utilities	X		
DMS/180			
Query Language		X	X
Report Generator			X
DBMS		X	X
Data Dictionary		X	
CROSS (2550/CY18 Software Maint)		X	
Conversion Aids			
COBOL-FORTRAN-BASIC	X		
Files	X		
ALGOL-APL		X	
Applications			
Math Science Library	X		
APEX,TIGS,SIMSCRIPT,GPSS		X	
APT,PERT,Uniplot,Total			X
Network Products	C170		
NETWORK Access Methods		X	X
Batch Facility		X	
Interactive Facility		X	
Transaction Facility			X

7.0 PERFORMANCE OBJECTIVES

The CYBER 180 architecture must allow the largest cost/performance range possible between the smallest model and the largest model. The range must be covered continuously with no cost and/or performance gaps within the line.

Identifiable processor models must occur at performance level ratios of 3 (+/- 0.5). At each level, a minimum starter system must be configurable with growth through add-on and/or replacement of hardware modules to allow the user to grow in smaller steps than total system replacement.

The actual code sequences to be used in measuring performance are specified in the Environments & Workload Specification (see section 2.0), along with the source language kernels and the various benchmarks used to establish the performance objectives.

7.1 SYSTEM PERFORMANCE GOALS

System performance objectives are based on the target configurations described in Appendix D.

System elapsed time is a function of the number of disks and the O/S utilization of the disks. System elapsed time ratios (CYBER-73/CYBER-180) are stated, based on the target configurations in Appendix D, to establish objectives for the O/S.

ENVIRONMENT	SYSTEM PERFORMANCE (CPU SECONDS)					BENCHMARK (2)
	CYBER-73 (1)	S1	S2	S3	THETA	
Transaction	TBF	1.2	3.0	7.5	25.0	TBL
Batch						
Scientific	3154	1.2	3.0	9.0	34.0	SBL
Commercial	657	1.2	3.0	7.5	25.0	SIMBDP
	954	1.2	3.0	7.5	25.0	BMC80
	2650	1.2	3.0	7.5	25.0	CBL
Interactive	TBF	1.2	3.0	7.5	25.0	IBL

ENVIRONMENT	SYSTEM PERFORMANCE (ELAPSED TIME) (3)					BENCHMARK
	CYBER-73 (1)	S1	S2	S3	THETA	
Transaction	TBF	TBF	TBF	TBF	TBF	TBL
Batch						
Scientific	3500	1.2	3.0	9.0 (2)	27.0 (2)	SBL
Commercial	730	1.2	3.0	7.3 (2)	10.0 (4)	SIMBDP
	2945	1.2	3.0	7.3 (2)	10.0 (4)	CBL
Interactive	TBF	TBF	TBF	TBF	TBF	IBL

(1) CYBER-73 timings are in seconds, and are based on NOS 1.1 430/428 (8/76), and assume a 90% CPU utilization.

(2) Multiple copies of the benchmark are required to achieve these ratios - at least 9 for S3, and at least 20 for THETA.

(3) CYBER 180 ratios are based on target configurations.

(4) To achieve a ratio of 18:1 at least 30 disks are required and multiple copies of the benchmark must be run.

7.2 PROCESSOR PERFORMANCE

To support the System Performance Goals above, processors must meet performance goals at the relative speeds listed below.

	PROCESSOR PERFORMANCE *					
	BASE	P1	P2	P3	THETA	BENCHMARK
SCIENTIFIC	280.5(1)	1.3	3.3	10.3	36.0	FORTRAN Kernels
BDP	8.3(2)	2.7	7.5	19.3	42.8 (4)	Composite
	21.9(3)	2.7	7.5	19.3	42.8 (4)	S-Profile
PASCAL Extended	2.26(5)	1.3	2.9	8.4	32.0	PASCAL-X Extended Profile 2

* These objectives assume no memory interference, except for THETA. THETA's objective must include the effect of whatever single CPU memory interference exists while executing the kernels. When evaluating processor's performance relative to goals, the memory and cache assumptions stated below will be constraining factors.

(1) Time to execute the 10 FTN Kernels, seconds

(2) Time per loop of the composite kernel, milliseconds

(3) Average time per COBOL statement, microseconds

(4) The THETA BDP ratio is a preliminary estimate, to be reduced if implementation costs are excessive.

(5) Average time per instruction for the PASCAL-X Kernel (including 115, 116, and 117 instructions) microseconds

7.2.1 MEMORY ASSUMPTIONS

- Central memory access time (A) including cables and bandwidth (B) as defined below:

Processor	Memory Access Time (A)	Memory Bandwidth (B)
P1	750 ns	64 MB/s
P2	840 ns	64 MB/s
P3	616 ns	128 MB/s
THETA	N/A	N/A

- No conflict in central memory.

7.2.2 CACHE ASSUMPTIONS

PROCESSOR	CACHE DATA HIT RATE (C)	CACHE INST. HIT RATE (I)	CACHE SIZE	MAP HIT RATE (M)
P1	-	-	No Cache	0.98
P2	0.75	0.92	16KB	0.98
P3	0.82	0.95	32KB	0.99
THETA	0.82	0.95	32KB	0.995

Where 1KB=1024 bytes and C, I and M are defined so that:

- (1-C) of data words accesses shall require a central memory reference.
- (1-I) of the instructions (not instruction words) shall require a central memory reference.
- (1-M) of the process virtual address to real memory address

translations shall require central memory reference for segment and page table information.

The cache sizes shown are recommended. Trade-offs between cache size and processor design can be made within the constraints of manufacturing cost and processor performance.

Hit rates higher than shown should not be assumed when estimating CPU performance.

7.2.3 BLOCK COPY PERFORMANCE

The transfer rate for the Central Memory Block Copy instructions (soft ECS feature) shall be at least one word every other clock cycle assuming no conflicts. (Major cycle for P3)

7.3 MEMORY PERFORMANCE

7.3.1 CENTRAL MEMORY

To support the system performance goals above, central memory must perform the requirements listed below.

	S1	S2	S3	THETA
Maximum Memory Capacity				
-single CPU system	8 MB	8 MB	16 MB	16 MB
-dual CPU system	8 MB	16 MB	32 MB(1)	16 MB
Maximum Total Memory Bandwidth	64 MB/s	64 MB/s	128 MB/s	1000 MB/s
No conflict CPU Access Time (2)				No objective
-single CPU system	600 ns	728 ns	616 ns	
-dual CPU system	750 ns	784 ns	672 ns	
No conflict IOU Access Time (2)	600 ns	896 ns	896 ns	896 ns

(1) Not required until January 1, 1983.

(2) All access times are measured at the memory ports. Additional delay may have to be added for calculations of CPU or IOU access. For dual-CPU configurations, the access times are the average of two CPU's.

7.3.2 DUAL MAINFRAME SHARED MEMORY

The maximum total memory bandwidth between the central processor and a shared memory is 41 MB/s (one 64-bit word every 192 ns). This is applicable to all systems (see section 3.1.1.4).

7.3.3 CONFIGURATION AND ENVIRONMENT MONITOR (CEM)

The CEM reports power faults within one-half cycle of their occurrence, and responds to all other environmental faults in 10ms.

Digital sensors activate in response to threshold crossings or pulsed inputs within 5 ms. The transmission rate is at least 4800 bits/second.

The level of electromagnetic interference introduced as a result of sensing either within a monitored unit or transmitted from it, is insignificant. The CEM and sensors must meet CDC EMC standards.

7.4 OPERATING SYSTEM PERFORMANCE

7.4.1 MONITORING/TUNING

Mechanisms supporting measuring of operating system and general software performance and usage characteristics will be provided. Basic analysis tools for presenting this data in meaningful terms are to be included. Measurement tools and services may be optionally selected.

Capabilities for system tuning at system generation, system load and execution times will be provided. Include tuning options to maximize performance in the following areas:

- transaction
- batch, local/remote
- time sharing

The level of performance achievable in any particular area is not required to be at the level of specifically developed dedicated application systems. The standard CYBER 180 operating system must be able to supply the majority of code that would

make up such dedicated special systems.

7.4.2 IOU PERFORMANCE

The CYBER 180 must provide a highly efficient I/O capability in both multi-programming and mono-programming modes. The I/O Unit provides:

- Maximum burst transfer rate to central memory
  - 32 megabytes/second for I1 (S1)
  - 50 megabytes/second for I2 (S2,S3,THETA)
- Device transfer rates, both burst and sustained, not limited by I/O system (within bandwidth limits).
- Ability to allow consecutive I/O requests to the same device to be processed as if they were a single request, so as to eliminate a time penalty of separate accesses. This is called "data streaming" and requires that the consecutive requests be overlapped such that successor requests occur before the completion of current requests.
- Ability to allow 9-18 concurrent I/O transfers (9 dual PP transfers, 18 single PP transfers, or combinations thereof).
- CYBER 180 external channel transfer speed of 5 megabytes/second.
- PPU major cycle time, I1-500ns.; I2-250ns
- PPU minor cycle time, 50ns.

7.4.3 OS WORKLOADS

The following workloads must be able to run on a minimum configuration:

- Dedicated Batch Mode - Minimum of 3 concurrent jobs (1 compilation and 2 production jobs, BDP oriented)
- On-line/Batch Mode - One on-line transaction application with up to 35 terminals, mixed types with a throughput of 3 to 4 transactions per second. (For measurement purposes, a transaction is an externally generated

INPUT/PROCESS/OUTPUT sequence requiring no more than 6 to 8 accesses to RMS during processing.) Two batch jobs (1 compilation and 1 production job, BOP oriented).

- Dedicated On-line Mode - One on-line transaction application with up to 100 terminals, mixed types, DMS180 access, with a throughput of 6 transactions per second.

7.4.4 O/S INSTRUCTION ALLOCATION

Performance objectives for specific functions within NOS/180 are established below. Achievement of these objectives is necessary for the overall system performance goals established in section 7.1.

These instruction counts will be superceded by O.S. performance kernels which incorporate the allocations, but allow design trade-offs to achieve the objectives.

These allocations represent the number of machine instructions executed in the normal processing path associated with the requests. Error handling and other exception processing is not included. The counts are in terms of CYBER 180 instructions. If used, the 115, 116, or 117 instruction counts as 20 instructions each and the use of exchange shall count as 40 each.

7.4.4.1 Record Manager

The instruction allocations for the Record Manager are given below:

	Instruction Count
Record in Buffer	
Get/Put Sequential	< 220
Get/Put Random byte address	< 320
Get/Put Key	< 1000
Record not in Buffer (Physical I/O Manager not included)	
Get/Put Sequential	< 520
Get/Put Random byte address	< 620
Get/Put Key (index in buffer)	< 1800
Get/Put Key (index not in buffer)	< 2500

This includes the epilog and prolog of the record manager procedure. If any other procedures are called, the set up, call and execution of the called procedures must be

included.

These instruction counts are independent of record and block length having been based on a range of these parameters in both scientific and commercial environments.

7.4.4.2 Physical I/O Manager

The instruction allocation for the Physical I/O Manager is given below:

	Instruction Count
Generate PP request	< 350
Request Completion	< 400

This includes the epilog and prolog of the Physical I/O Manager. If other procedures are called, their total instruction count must be included.

7.4.4.3 Task Switching

The instruction count for task switching upon suspension of a task due to I/O, time slice, etc. shall be:

	Instruction Count
Task Switching	< 500

This includes the instruction necessary to suspend a task, perform needed accounting for the suspended task, select a new task from a ready list, etc. A maximum of four (4) exchanges are permitted, in addition to the instruction count given above.

7.4.4.4 Batch Job Initiation and Termination (Normal Case)

The maximum instruction count for initiating or terminating a batch job shall be:

	Instruction Count
Initiation or Termination	<25000

The maximum number of disk accesses (excluding paging) for initiation and termination shall be:

	Disk Accesses
Initiation	
Read	4
Write	1
Termination	
Read	0
Write	3

7.4.4.5 Page Fault Handling

The instruction allocation for handling a page fault is given below:

	Instruction Count
Page Available	< 400
Page on Mass Storage (Physical I/O Manager not included)	< 500

This includes all instructions needed to process a page fault.

7.4.4.6 Periodic Function

In total these shall not consume more than 2.5% of the total CPU resource, as detailed below:

- Page Aging 0.5%
- Task scheduling - priority changing 0.5%
- Error monitoring (see section 7.6) 0.5%
- All other periodic functions 1.0%

7.4.4.7 Job Swapping

The rate of swapping shall be a variable parameter. The CYBER 180 instructions used shall not exceed 5000.

7.4.4.8 Loader

The table below states the loader requirements.

	CPU TIME	
Processor	Ratio to CY73	Benchmarks
P1	1.3	SBL,CBL and BMC80
P2	2.8	SBL,CBL and BMC80
P3	6.6	SBL,CBL and BMC80
THETA	32.0	SBL,CBL and BMC80

7.4.4.9 Dual State Performance

- Throughput using an SBL workload (see section 3.3.10 for configurations):

%170	%180	Elapsed Time
100	0	1.0
70	30	1.04
30	70	1.08
0	100	1.12

- Interstate Communication

The CPU overhead per request for inter-state communication in dual state mode must not exceed the CPU overhead associated with the NOS/170 symmetric link MMF interface in either an idle or active status.

7.4.4.10 Network Products Performance

7.4.4.10.1

7.4.4.10.2 CPU UTILIZATION

The table below indicates the percentage of CPU time to be utilized by NAM and BF to support 112 communication lines configured as follows:

-12 are synchronous 2000-56,000 bps lines used for batch input/output averaging 9600 bps/line.

-100 are asynchronous 110-9600 bps lines used for interactive applications averaging 600 bps/line.

The CPU time used by NAM and BF is dependent on the sustained data transfer rate.

	NAM CPU % (11.2KB/sec total, 112 terminals)	BF CPU % (10.2KB/sec)
S1	5.2%	3.3%
S2	3.5%	1.8%
S3	2.5%	0.8%
THETA	2.2%	0.6%

7.4.4.10.3 MEMORY UTILIZATION

The amount of real memory required by NAM and BF to support 112 communication lines configured with two 2550 processors shall be:

NAM 90K Bytes

BF 30K Bytes

7.5 PRODUCT SET PERFORMANCE

7.5.1 LANGUAGE PERFORMANCE LEVELS

The following table indicates the language processor performance objectives. It specifies the performance values to be achieved (compile rate and disk accesses) when running the indicated benchmark at the indicated memory allocation.

Where two levels of compilation performance are specified in the table below, they are defined as follows:

DEV - Development mode. Characterized by extensive diagnostics and fast compilation rate at the expense of object code efficiency.

PROD - Production mode. Characterized by highly efficient object code (space/speed) generated at the expense of compilation rates.

LANGUAGE PROCESSORS PERFORMANCE OBJECTIVES (1)

Product	Real Memory Allocation (2)	Minimum Statements Compiled Per CPU Min (3)	Maximum Disk Accesses Per CPU Sec Allowed (4)	Benchmark (5)
ALGOL-60	150KB	5,100	22	ALGOL 5 Test Base
ALGOL-68	TBF	TBF	TBF	
APL	100KB	NA	TBF	
ASSEMBLER	150KB	15,000	25	FCT
BASIC				
PROD	TBF	TBF	TBF	BASIC JOB
DEV	100KB	20,000	25	1,2,3,4,5
COBOL	150KB	8,700	37	CBL,BMC80 & SIMBDP
FORTRAN				
PROD (OPT=2)	150KB	7,000	56	SBL
DEV(TS)	125KB	13,000	23	SBL
PL/1	TBF	TBF	TBF	
WIRTH PASCAL	100KB	30,000	20	
PASCAL-Extenced				Compile itself
PROD	150KB	4,000	TBF	
DEV	125KB	10,000	TBF	
SYMPL				Compile
PROD	150KB	4,000	56	itself
DEV	125KB	10,000	23	

(1) Performance values are for P2; values for other processors (including disk accesses) are proportionate to the performance figures for PASCAL-X in the table in section 7.2.

(2) Real memory allocation is the amount of real memory, including buffers and table space, to be assigned the compiler in running the indicated benchmark when measuring compile rate and disk accesses.

(3) Statements compiled per CPU minute do NOT include comments. The CPU time includes O/S time during compilations.

(4) Disk accesses per CPU minute is a measure of the load, in I/O requests, the compiler is placing on the system. The value indicates the maximum number allowed when running the indicated benchmark at the indicated memory allocation. Disk accesses for paging are included.

(5) If no benchmark is indicated, a "typical" program has >500 data names, >1000 statements.

TBF - To be furnished in subsequent revisions

7.5.2 CODE EFFICIENCY

a) FORTRAN supplied run time and mathematical routines shall execute at the following speed ratios:

Processor Performance

	CYBER 73(1)	P1	P2	P3	THETA
FORTRAN Run Time Routines and Math Library	1.0	1.3	3.2	9.6	36.0

(1) NOS 1.1 430/428 (6/76) base

b) FORTRAN and COBOL generated code shall be as efficient as or better than the code sequences given in the Environment and Workload Specification, ARH1058, for CPU kernels.

7.5.3 DMS180

TBF

7.5.4 SORT/MERGE PERFORMANCE

Processor	Minimum Working Set Size (K Bytes)	Records Sorted Per CPU Min (1)	Disk Access Per CPU Second (3)	B/M
P1	100 (2)	1.3 X CYBER 73	120*F	T3F
P2	Same	4.5 X CYBER 73	500*F	Same
P3	Same	12.2 X CYBER 73	1500*F	Same
THETA	Same	34.7 X CYBER 73	4500*F	Same

(1) Same sort benchmark between CYBER 73 and PN in that the same number of strings will be produced by the internal sort phase. This will be controlled by the amount of memory dedicated to this phase. The ratio applies only to the time in the sort code.

(2) The minimum shall not exceed the given value.

(3) F equals $\frac{(100{,}000)}{(\text{Actual WS})} * \frac{(\text{Actual Record Length})}{(100)}$

7.6 MAINTENANCE SOFTWARE

- Error monitoring will not reduce system throughput by more than 0.5%.
- No single test will exceed 50000 lines of source code.
- The object code size of tests is limited to 176KB maximum, and the working set size is limited to 100KB maximum.
- Initialization utilities will not exceed two minutes run time for the maximum configuration.

8.0 RELIABILITY, AVAILABILITY AND MAINTAINABILITY (RAM)

8.1 OPERATING AND SUPPORT CONDITIONS

The anticipated usage and maintenance of the system(s) specified below describe the environment and assumptions used in predicting RAM performance parameter values.

8.1.1 OPERATING CONDITIONS

8.1.1.1 Duty Factors

It has been assumed that all mainframe components are powered up 100% of the time - that is 720 hours/month. For peripherals the reliability data (MTBI) have been based on field observations, and therefore the duty factors encountered in the field have been assumed implicitly.

8.1.1.2 Target Configuration

The target configuration(s) of the CYBER 180 Systems is as specified in Appendix D.

8.1.1.3 Component Criticality

Processor cache and MAP can be bypassed (except S1).

Up to 25% of central memory may be flawed by software techniques.

There will be only one I/O Unit. It has been assumed that there will always be a spare PP, hence in a configuration of n PP's only (n-1) are required for normal operation.

Whenever a degradation occurs in the mainframe, the system throughput is expected to decrease.

The following equipment has been configured redundantly. That

is, it has been assumed that loss of a redundant equipment does not degrade system throughput.

Only four of six removable disk storage units are required for normal operation.

The loss of a removable disk storage unit controller will not cause the system to fail.

Only three of four or four of six tape drives are required for normal operation.

The loss of a communications processor will not cause a system crash.

A single controller failure does not cause a system down. For system mass storage devices, there are two mass storage controllers for every four spindles.

The operating system requires a designated spindle on the system mass storage device. Of the remaining spindles if one is lost the system does not crash.

8.1.2 SUPPORT CONDITION STRATEGY SUMMARY

The maintenance strategy is as defined in the reference documents noted in Section 2.0.

Where redundant equipment is provided Preventive Maintenance does not interfere with normal system operation.

Preventive maintenance intervals will be optimized around MTBI and life-cycle maintenance cost.

8.1.3 ASSOCIATED RAM REQUIREMENTS

The reliability, availability and maintainability of the CYBER 180 systems is derived from the RAM of:

- the individual hardware elements
- the Operating System software
- the tests and diagnostics used to maintain the hardware.

Failure of any one of these components to meet its RAM objectives could compromise the system RAM. It should be noted that the Operating System reliability objectives have been set

significantly higher than has ever been achieved for new software running on new hardware.

8.2 RAM FEATURES

The guidelines for total costs for RAM features for a given mainframe element will be 10-15% of hardware manufacturing cost except for the THETA CPU. The guideline for the THETA CPU RAM costs will be 3%-15% of manufacturing cost, subject to the constraint that scientific performance is degraded by no more than 2%.

8.2.1 RELIABILITY FEATURES

Reliability features reduce failure rates of hardware and software, and minimize component faults from becoming equipment and system failures. Specifically, reliability is defined as preventing the occurrence or propagation of errors. Reliability features will include:

Hardware

- Parity checking on major data paths, address paths, channels, registers and memories except for the THETA CPU, which shall include parity checking within restrictions listed in paragraph 8.2.
- Error status registers.
- Time-out mechanisms to provide continuous operation of system facilities.
- Methods of forcing conditions so that checks can be made of the reliability circuitry.

Software

- A validation check of disk write positioning.
- Checksum techniques for key system tables.
- Except for offline diagnostics, validate a link using software checks (e.g., transferring data blocks and checksums) before actual data transmission.
- Other checks by I/O drivers for malfunctions that are

characteristic of a device.

Diagnostics

- The system initialization process to include confidence level tests run against critical system components.

8.2.2 AVAILABILITY FEATURES

Availability features are defined as those providing alternate paths around failing or failed system functional components to minimize impact on a running production system. Availability features will include:

Hardware

- Single error correction/double error detection (SEC/DED) implemented on central memory.
- Hardware instruction retry providing the instruction fails before destroying any information.
- Use of motor generator sets to decrease sensitivity to commercial power (2.5 second ride through).

Software

- Execution of user supplied data recovery algorithms after standard system error recovery procedures.
- Checkpoint recovery facilities both at the individual job and at the system level, such that the environment may be re-established after a system failure. These facilities will apply to single and multi-mainframe environments.

Hardware Supported by Software

- Capability to "fault" portions of the cache buffer and map buffer except on S1.
- Capability to idle a PP in the IOU and assign another PP to perform its task.
- Reconfiguration by a combination of hardware and software techniques following failures, automated as far as possible.

Diagnostics

- The ability to run diagnostics concurrently with customer operations to isolate faults in one of dual processors, peripherals, peripheral controllers, and certain modes of failure in memory.

- Through the standard support, 80% of the hardware problems associated with a second processor and peripherals will be repairable concurrent with system operations.

- Support of data integrity by all maintenance software, in that this software shall never over write those areas of disk, etc. while reserved for customer use.

- Support of deferred maintenance by the on-line monitor.

- Reduced repair time on system elements through the use of isolation diagnostics and remote maintenance.

- Minimizing preventive maintenance on all equipments. The Engineering file analyzer will trigger maintenance actions based on usage and error rates. On new hardware being developed for CYBER 180 the objective should be minimum preventive maintenance.

8.2.3 MAINTAINABILITY FEATURES

Maintainability features are intended to optimize the effectiveness of error isolation and maintenance support. They will include:

Hardware

- Error signals which localize faults.

- Microprogram control of CPU instruction execution except for THETA.

- Minimize the number of mainframe module types with all like modules fully interchangeable. Mainframe modules will be replaceable when power is on, but C.S. down.

- Privileged operational modes to execute maintenance service facilities. For example, vary clock pulse-width margins under program control, or vary voltage margins manually.

Software

- Logging of transient and permanent faults. Logging of operating system deadstart recovery and obtain supplemental information statistical RAM information from operator initiated restarts.

- Relinquish all but a minimum of system critical components to concurrent maintenance as needed, while normal customer operation continues.

- Remote access to those facilities under off-line or on-line maintenance control which can be used for hardware and software maintenance.

Diagnostics

- Design CYBER 180 Maintenance Software to allow hardware maintenance to be performed concurrent with customer operation.

8.2.4 MAINTENANCE SOFTWARE

The performance objectives for CYBER 180 Level II and III maintenance software are described in the following paragraphs.

8.2.4.1 On-Line Monitor

1) Be "crash-proof" for at least 95% of all hardware and system software failures.
2) Provide 100% adherence to OS requirements for security, file structures and resource access.

8.2.4.2 Off-Line Monitor

1) Provide 100% validation of all operator actions.

8.2.4.3 Tests, Diagnostics, Utilities (mainframe only)

1) Tests

- Shall detect 95% of all solid, software detectable failures, and 90% of the same failures when run in their shortened versions as determined by default parameter selection.
- Shall correctly identify the functional area for at

least 90% of all failures detected.
- Shall provide a detection capability which supports the MTTR goals of the various products.
- Provide 100% protection for all customers security and file structure requirements.

2) Diagnostics

- Shall isolate to three or less replaceable subassemblies for 90% of all solid failures identified to a functional area.
- Shall provide an isolation capability which supports the MTTR goals of the various products.
- Provide 100% protection for all customers security and file structure requirements.

NOTE: The cost effectiveness of isolation diagnostics will be examined in detail prior to submission of DR's.

3) Utilities

A) Engineering File Analysis

- Shall provide 100% adherence to all OS requirements for security, file structure and resource access.
- Shall provide an on-line analysis capability for 100% of all errors logged
- Shall provide an off-line capability for fatal errors on system critical elements.

B) Maintenance Scheduler (CAMS)

- Shall provide maintenance schedules for 100% of all supported CYBER 180 equipment on each site.

C) Initialization/Deadstart Tests

- Shall be capable of detecting 70% of all solid software detectable failures in the associated hardware.

8.3 RAM SUPPORT COSTS

8.3.1 FACTORY CONTINUATION COSTS

8.3.1.1 Field Change Orders

FCO Hours/Equip/Year

	1980	1981	1982	1983	1984	1985	1986
S1 Mainframe		75	15	23	15	8	8
P2	75	15	23	15	8	8	0
M2	10	15	10	5	5	0	0
P3		30	35	40	30	20	10
M3		10	15	10	5	5	0
THETA CPU				20	50	40	30
THETA MEMORY				3	10	15	10
I/O	10	15	20	5	5	0	0

Number of FCO's/Equip/Year (#I)

	1980	1981	1982	1983	1984	1985	1986
S1 Mainframe		30	6	10	6	4	4
P2	30	6	10	6	4	4	0
M2	4	6	4	2	2	0	0
P3		12	14	16	12	8	4
M3		4	6	4	2	2	0
THETA CPU				4	20	16	12
THETA MEMORY				2	4	6	4
I/O	4	6	8	2	2	0	0

8.3.1.2 Software Maintenance Costs

The estimates below are software maintenance objectives for the first five-years following release. The following assumptions apply:

- cost to fix one bug $500 except first year (vs. 1976 CYBER 170 cost of $675).
- distribution of bug reports to be 45% operating system, 15% FORTRAN, 15% COBOL/SORT, 15% DMS180 and 10% other.
- once released, only validated bug fixes are added to a software system. No PSR's are accepted 3 years after release.
- when the next version software system is released, current version users will convert at 50% per year.

- Year	1982	1983	1984	1985	1986
% Shipped As CYBER 180	10	20	40	80	100
% C170 Mode Converting To C180	10	20	30	40	50

SOFTWARE MAINTENANCE COSTS

YEAR	1982	1983	1984	1985	1986
Cumulative Number C180 Systems	25	95	233	442	624
"maintenance" cost in millions	0.9	1.1	1.7	2.6	2.6
monthly receipt of error reports	65	185	290	440	440

8.3.2 FIELD MAINTENANCE COSTS

8.3.2.1 Hardware Maintenance Costs - Mainframe System

Emphasis will be placed on ease of installation including parameters such as:

1) Physical interconnectability
2) Environmental requirements

to the end of reducing installation costs.

The monthly maintenance cost for CYBER 180 mainframe systems (excluding peripheral equipment) incurred by the supporting field service organization must not exceed the following levels (expressed as a percentage of manufacturing cost):

System Model	Life Cycle Average Monthly Maintenance Cost	Second Year Monthly Maintenance Cost Objective
S1	0.67%	0.85%
S2	0.53%	0.67%
S3	0.53%	0.67%
THETA	0.45%	0.54%

"System model" includes processor, memory and IOU. These costs include both the direct cost of maintaining the equipment and the allocation of various indirect costs, as follows:

Direct Cost

Direct Costs include the following labor, travel and parts category:

- Remedial Maintenance Labor
- Preventive Maintenance Labor
- Associated Repair Labor
- Consumable Parts
- Rework of Replaceable Modules
- Travel Time and Expenses (for field service personnel)

Indirect Cost

Indirect costs include the allocation of the following expense

categories:

- Training (for field service personnel)
  Note: These costs are minimized by utilizing tools such as isolation diagnostics which will allow the use of MAL-8 trained personnel.
- Tools and Test Equipment
  Note: These costs are minimized by utilizing tools such as isolation diagnostics which eliminate the need for portable testers.
- Spare Parts Inventory
- Diagnostic Software Maintenance and Distribution
- Home Office Support

8.4 RAM PERFORMANCE OBJECTIVES

Values are specified for field release of first system: six months after release; and 18 months after release. Expected values for the hardware have been based on the growth curves established in reference 9.

Formulas used are as follows:

S1, P2, IOU : MTBI = MTBF (0.60-0.35 exp (-0.035T))

M2 : MTBI = MTBF (0.60-0.35 exp (-0.035T))

M3 : MTBI = MTBF (0.60-0.40 exp (-0.035T))

M4 : MTBI = MTBF (0.60-0.45 exp (-0.035T))

P3 : MTBI = MTBF (0.60-0.45 exp (-0.02T))

THETA : MTBI = MTBF (0.60-0.45 exp (-0.02T))

Where:

MTBI is the expected, observed MTBI

MTBF is the inherent MTBF

and T is in months after release

In addition, the expected values on release take into account the effect of degradability (e.g., cache, MAP bypass) as follows

Expected MTBI = MTBI / P

Where P is the probability that a failure to a component in the equipment causes the equipment and system to fail.

Probability factors have been set as follows:

S1 - 60%

P2 - 80%

P3 - 70%

THETA - 90-95%

Memory - 75%

IOU - 90-95%

Finally, the affect of redundancy has been accommodated. This means that memory reliability includes the benefits of SECDED. Although it is a requirement for the Operating System to degrade the IOU this is not factored into the objectives which follow.

8.4.1 MEAN TIME BETWEEN SYSTEM DOWN INTERRUPTIONS (MTBI DOWN)

The operating system components are estimates based on the following assumptions:

- The same basic software system is used throughout with only validated bug fixes added.
- There is no radical change in the nature of the user's production workload.
- The O.S. MTBI is inversely proportional to the square root of processor speed.
- Automated restart features (defined to return system to productive state within 1 minute) effectively increase the MTBI by a factor of 2.

The objectives stated below ignore failures due to brown-outs and other power fluctuations. They indicate the factor of two derived from the automated restart feature of the Operating System. In all cases values are expected, observed values.

8.0 RELIABILITY, AVAILABILITY AND MAINTAINABILITY (RAM)
8.4.1 MEAN TIME BETWEEN SYSTEM DOWN INTERRUPTIONS (MTBI DOWN)

MTBI(dn) (hrs) TARGET S1 SYSTEM

POINT IN TIME	CPU	MEMORY	I/O	PERIPHS	O/S	TOTAL H/W	TOTAL SYS
On Release	555	-INC-	-INC-	3000	500	468	242
Six Months	620	-INC-	-INC-	3000	500	514	253
18 Months	717	-INC-	-INC-	3000	1600	578	425

MTBI(dn) (hrs) TARGET S2 SYSTEM

POINT IN TIME	CPU	MEMORY	I/O	PERIPHS	O/S	TOTAL H/W	TOTAL SYS
On Release	1010	1017	1347	3000	300	328	157
Six Months	1075	1083	1433	3000	300	347	161
18 Months	1169	1177	1559	3000	900	373	264

MTBI(dn) (hrs) TARGET S3 SYSTEM

POINT IN TIME	CPU	MEMORY	I/O	PERIPHS	O/S	TOTAL H/W	TOTAL SYS
On Release	633	607	1214	3000	167	228	96
Six Months	736	696	1292	3000	167	256	101
18 Months	907	828	1406	3000	533	298	191

8.0 RELIABILITY, AVAILABILITY AND MAINTAINABILITY (RAM)
8.4.1 MEAN TIME BETWEEN SYSTEM DOWN INTERRUPTIONS (MTBI DOWN)

MTBI(dn) (hrs) TARGET THETA SYSTEM

POINT IN TIME	CPU	MEMORY	I/O	PERIPHS	O/S	TOTAL H/W	TOTAL SYS
On Release	191	447	942	3000	100	113	53
Six Months	222	528	978	3000	100	129	56
18 Months	274	649	1029	3000	267	154	98

INC means included in the CPU.

8.4.2 (#I) MEAN TIME BETWEEN SYSTEM DEGRADED INTERRUPTIONS

MTBI(dg) (hrs) TARGET S1 SYSTEM

POINT IN TIME	CPU	MEMORY	I/O	PERIPHS	O/S	TOTAL H/W	TOTAL SYS
On Release	833	-INC-	-INC-	9000	151	751	151
Six Months	930	-INC-	-INC-	9000	151	829	151
18 Months	1075	-INC-	-INC-	9000	491	942	471

8.0 RELIABILITY, AVAILABILITY AND MAINTAINABILITY (RAM)
8.4.2 (#I) MEAN TIME BETWEEN SYSTEM DEGRADED INTERRUPTIONS

MTBI(dg) (hrs) TARGET S2 SYSTEM

POINT IN TIME	CPU	MEMORY	I/O	PERIPHS	O/S	TOTAL H/W	TOTAL SYS
On Release	4040	3052	7633	9000	91	1224	91
Six Months	4300	3248	8120	9000	91	1291	91
18 Months	4675	3532	8833	9000	281	1386	271

MTBI(dg) (hrs) TARGET S3 SYSTEM

POINT IN TIME	CPU	MEMORY	I/O	PERIPHS	O/S	TOTAL H/W	TOTAL SYS
On Release	1477	1820	6880	9000	51	674	51
Six Months	1717	2088	7320	9000	51	764	51
18 Months	2117	2484	7967	9000	161	900	161

MTBI(dg) (hrs) TARGET THETA SYSTEM

POINT IN TIME	CPU	MEMORY	I/O	PERIPHS	O/S	TOTAL H/W	TOTAL SYS
On Release	1720	1340	5340	9000	31	615	31
Six Months	2000	1564	5540	9000	31	703	31
18 Months	2470	1948	6833	9000	81	833	81

INC means included in the CPU.

8.0 RELIABILITY, AVAILABILITY AND MAINTAINABILITY (RAM)
8.4.3 MEAN LOST TIME DUE TO SYSTEM DOWN INTERRUPTIONS

8.4.3 MEAN LOST TIME DUE TO SYSTEM DOWN INTERRUPTIONS

Mean lost time is defined in units of minutes per failure. Objectives for S1-THETA systems are shown in the following tables:

MLT(dn) (mins) TARGET S1 SYSTEM

POINT IN TIME	CPU	MEMORY	I/O	PERIPHS	O/S	TOTAL H/W	TOTAL SYS
On Release	150	-INC-	-INC-	180	36	155	97
Six Months	150	-INC-	-INC-	180	36	155	95
18 Months	135	-INC-	-INC-	180	36	144	115

MLT(dn) (mins) TARGET S2 SYSTEM

POINT IN TIME	CPU	MEMORY	I/O	PERIPHS	O/S	TOTAL H/W	TOTAL SYS
On Release	135	105	135	180	24	130	75
Six Months	135	105	135	180	24	131	73
18 Months	126	105	126	180	24	126	96

8.0 RELIABILITY, AVAILABILITY AND MAINTAINABILITY (RAM)
8.4.3 MEAN LOST TIME DUE TO SYSTEM DOWN INTERRUPTIONS

MLT(dn) (mins) T A R G E T S 3 S Y S T E M

POINT IN TIME	CPU	MEMORY	I/O	PERIPHS	O/S	TOTAL H/W	TOTAL SYS
On Release	150	111	135	180	18	135	67
Six Months	150	111	135	180	18	135	64
18 Months	135	105	126	180	18	127	68

MLT(dn) (mins) T A R G E T T H E T A S Y S T E M

POINT IN TIME	CPU	MEMORY	I/O	PERIPHS	O/S	TOTAL H/W	TOTAL SYS
On Release	210	111	126	180	12	174	88
Six Months	210	105	126	180	12	172	82
18 Months	150	105	120	180	12	136	91

INC means included in the CPU.

8.0 RELIABILITY, AVAILABILITY AND MAINTAINABILITY (RAM)
8.4.4 (#I) MEAN LOST TIME DUE TO SYSTEM DEGRADED INTERRUPTIONS

8.4.4 (#I) MEAN LOST TIME DUE TO SYSTEM DEGRADED INTERRUPTIONS

The objectives in this area are based on the following assumptions:

1) When a degraded interruption occurs, the job which was in execution at the time of the interruption is aborted.

2) The system throughput in degraded mode is 50% of the normal system throughput for all system degradations.

3) A Customer Engineer is contacted immediately to correct the problem.

MLT(dg) (mins) T A R G E T S 1 S Y S T E M

POINT IN TIME	CPU	MEMORY	I/O	PERIPHS	O/S	TOTAL H/W	TOTAL SYS
On Release	90	-INC-	-INC-	105	10	90	12
Six Months	90	-INC-	-INC-	105	10	90	11
18 Months	83	-INC-	-INC-	105	10	83	14

MLT(dg) (mins) T A R G E T S 2 S Y S T E M

POINT IN TIME	CPU	MEMORY	I/O	PERIPHS	O/S	TOTAL H/W	TOTAL SYS
On Release	83	68	83	105	6	80	7
Six Months	83	68	83	105	6	80	7
18 Months	78	68	78	105	6	78	7

8.0 RELIABILITY, AVAILABILITY AND MAINTAINABILITY (RAM)
8.4.4 (#I) MEAN LOST TIME DUE TO SYSTEM DEGRADED INTERRUPTIONS

MLT(dg) (mins) T A R G E T S 3 S Y S T E M

POINT IN TIME	CPU	MEMORY	I/O	PERIPHS	O/S	TOTAL H/W	TOTAL SYS
On Release	90	70	83	105	4	83	5
Six Months	90	70	83	105	4	83	5
18 Months	83	68	78	105	4	79	5

INC means included in the CPU.

8.4.5 DATA ERROR RATES

Data error rates are dominated by peripheral data error rates on all systems. The objectives stated below apply to S1 through THETA systems on release, six months and 18 months after release. This data shall be measured at the user I/O interface.

a) Recoverable data errors
The recoverable data error rate shall be one error per 10**9 bits of correct data.

b) Unrecoverable data errors
The unrecoverable data error rate shall be one error per 10**11 bits of correct data.

c) Undetected data errors
The undetected data error rate shall be less than one error per 10**16 bits of correct data.

8.4.6 USER AVAILABILITY

The user availability includes all items listed under net availability below, except preventive maintenance time which does not form part of the scheduled operating time. User availability of all systems at release and thereafter shall exceed 99%.

8.0 RELIABILITY, AVAILABILITY AND MAINTAINABILITY (RAM)
8.4.7 NET AVAILABILITY

8.4.7 NET AVAILABILITY

The objectives include:

- the time taken for an engineer to get to the site to repair the failure.
- the time taken to effect the repair (MTTR).
- the time taken to restore the system to its original state and re-run time necessitated by the failure. Weighted rerun times are used in the calculations, based on the failing equipment type.
- time taken on preventive maintenance, assuming this is conducted by a single engineer.
- time lost due to degraded interruptions.

The objectives exclude :

- time to make changes to the hardware (ECO's).
- time to make changes to the software (PSR's).
- the affect of on-line maintenance software failures on the overall system.

SYSTEM AVAILABILITY OBJECTIVES - CYBER 180

TIME PERIOD	S1	S2	S3	THETA
On Release	99.05	98.65	98.14	96.12
6 Months	99.10	98.68	98.25	96.47
18 Months	99.27	98.84	98.54	97.34

8.5 MAINTENANCE SOFTWARE RAM PARAMETERS

8.5.1 RAM PERFORMANCE PARAMETERS (LEVEL III)

The following RAM parameters for Level III maintenance software are based on a duty factor of 1% for the diagnostics. For example, if the diagnostics were run continuously then once every 175 hours they would cause a system down interruption at release. However, based on the typical field usage (1% duty factor) system down interruptions should not occur more frequently than every 17,500 hours.

Parameter	Release	6mo.After Release	18mo.After Release
MTBI Down	175 hrs	200 hrs	250 hrs
MTBI Degraded (#I)	125 hrs	142 hrs	175 hrs
MLT Down	0.6 hrs	0.6 hrs	0.6 hrs
MLT Degraded (#I)	0.8 hrs	0.8 hrs	0.8 hrs
A (U)	99.1%	99.2%	99.3%

8.5.2 UPDATE AND INSTALLATION

Maintenance Software components shall be designed and constructed to permit library maintenance and update using standard system software and firmware. Hardware required to support said maintenance shall be any standard configuration as stated in Appendix D.

It is estimated that one (1) MAL C trained CE shall be able to install or update the Maintenance Software Library in the following times:

	RELEASE	6 MOS	18 MOS./COST
Install New System	2.0 hrs.	1.5 hrs	1.0 hrs/$300 per year
Update Old System	1.0 hrs.	.5 hrs	.2 hrs/$150 per year

8.5.3 FAILURE RATES

Backlog of All Maintenance Software	Release	6 Mos	18 Mos
Critical DPSRs/PSRs	0	1	0
Major DPSRs/PSRs	2	2	1
Minor DPSRs/PSRs	17	8	6
Information DPSRs/PSRs	6	5	2
	25	16	9
Failure Rates/1000 Jobs	0.1%	0.05%	0.005%

Individual Objectives are as follows:

	DPSR's/Mo at Release	DPSR's/Mo at 6 Mo.	DPSR's/Mo at 18 Mo.
On-Line Monitor	2	1	0.5
Off-Line Monitor	1	1	0.5
I/O Unit Tests/Diag.	3	2	1.0
P1 Tests/Diags	3	2	1.0
P2 Tests/Diags.	3	2	1.0
P3 Tests/Diags.	3	2	1.0
THETA Tests/Diags.	3	2	1.0
Central Memory Tests/Diags.	2	1	0.5
Periph.Tests/Diags.	6	4	3.0
Utilities	2	1	0.5
	28	18	10.0

8.6 PRODUCT SET RAM PARAMETERS

Where applicable, product set members will support the RAM features described in CDC System Standard 1.12.004 as specified in the CYBER 180 System Interface Standard.

8.6.1 PRODUCT FAILURE RATE

A test base shall be established for each product representing customers' use of the product. The failure rate for each product against its test base is given below in failures per 1000 unique jobs run as measured in the internal system test phase (excluding

informational errors).

PRODUCT	Release	6mo.After Release	18mo.After Release
ALGOL	6	3	1
APL	8	4	2
ASSEMBLER *	2	2	1
BASIC	8	4	2
COBOL	6	3	1
DMS180			
AAM	4	2	1
FMU	8	4	2
DBMS	4	2	1
DBMS Util.	6	3	1
DDL	6	3	1
Query Lang.	6	3	1
Report Writer	8	4	2
FORTRAN	6	3	1
PL/1	10	5	3
PASCAL EXT. *	2	1	1
SORT/MERGE	2	1	1
SYMPL *	2	1	1
OPERATING SYSTEM			
BOS	0.01	0.005	0.002
SFS	0.1	0.05	0.02
EOS	1	0.5	0.2

* No failures in system generation.

8.6.2 PRODUCT INPUT DATA FAILURE RATE (PIDFR)

The PIDFR is stated in terms of failures per million inputs processed. A failure is a job abort and is measured in the live field environment.

PRODUCT (unit of input)	Release	6mo.After Release	18mo.After Release
ALGOL (ss)	0.6	0.5	0.4
APL (ss)	0.4	0.2	0.1
ASSEMBLER (ss)	0.1	0.05	0.02
BASIC (ss)	0.4	0.2	0.1
COBOL (ss)	0.2	0.1	0.05
DMS180			
AAM (fr)	0.01	0.005	0.002
FMU (rp)	0.1	0.05	0.02
DBMS (fr)	0.02	0.01	0.005
DBMS Util.(rp)	0.02	0.01	0.005
DDL (ss)	0.2	0.1	0.05
Query Lang.(fr)	0.4	0.2	0.1
Report Writer(rp)	0.4	0.2	0.1
FORTRAN (ss)	0.2	0.1	0.05
PL/1 (ss)	1.0	0.6	0.5
PASCAL EXT. (ss)	0.1	0.05	0.02
SORT/MERGE (rp)	0.01	0.005	0.002
SYMPL (ss)	0.1	0.05	0.02
OPERATING SYSTEM(fr)			
BOS	0.005	0.002	0.001
SFS	0.05	0.02	0.01
EOS	0.5	0.2	0.1

ss = source statement, including comments.

fr = functional request.
rp = records processed.

8.6.3 INSTALLABILITY

Installability features will emphasize:

1) Simple field operating system installation sequence.

2) Automated or semi automated configuration definition.

No product shall require more than one hour preparation time to install or replace (update) by a programmer analyst with 6 months experience and 1 month training on CYBER 180 hardware and software. In addition, no product shall require more than two minutes CPU time on an S2 system for its installation (assuming binary code distribution with adjustment for installation options has been accomplished prior to shipment).

8.6.4 MAINTENANCE

The total number of PSR's received per month, for the Operating System and product set are shown below:

PRODUCT	Backlog at Release	Rate 6mo.After Release	Rate 18mo.After Release
ALGOL	3	4	6
APL	3	4	6
ASSEMBLER	1	2	3
BASIC	3	4	6
COBOL	10	14	24
DMS180	15	21	36
FORTRAN	13	18	30
PL/1	3	4	6
PASCAL EXT.	1	2	3
SORT/MERGE	3	4	6
SYMPL	1	2	3
OPERATING SYSTEM	45	60	100

The number of critical PSR's, (either backlog or monthly rate) shall not exceed 5% of the objectives stated above for any product. PSR's are unique problems, internally and externally generated, excluding informational errors. See Section 8.3.1.2 for costs. In addition, there shall be no backlog of critical PSR's at the time that the system/product enters its final build, nor any unanswered critical PSR's at release.

8.6.5 SUBSYSTEM RELIABILITY

A subsystem is a software service routine, not part of the basic Operating System, which interfaces between multiple users or jobs and CYBER-180 system resources. Some specific examples are:

Dual state link

Multi-mainframe

Data management systems

Network products.

All subsystems must meet the following reliability goals:

1) Cannot cause NOS/180 to crash

2) Cannot cause all users to reinitialize:

- due to subsystem failure at an interval less than three times the NOS/180 MTBI.
- when the subsystem drops or adds system resources (such as terminals, front ends, data bases, etc. - through a defined range of configurations).

9.0 OBJECTIVES EXCLUDED

9.1 OBJECTIVES SPECIFICALLY EXCLUDED

These objectives are not and will not be included in the CYBER 180 program as defined in this document.

- Interface to IBM System Network Architecture.
- Support for direct execution (emulation) of processors other than CYBER 170.

9.2 OBJECTIVES NOT SPECIFICALLY PRECLUDED

These objectives are not included but could be included in the CYBER 180 program as defined in this document.

- Support of most compiler languages.
- Implementation of a time-critical software operating mode (see 3.1.2).
- Support of the STAR 100 system as a computational facility.

10.0 CYBER 170 STATE

10.1 MAINFRAME FEATURES

10.1.1 CURRENT CYBER 170 FEATURES SUPPORTED

a) CYBER 173 CPU instruction set

- CMU instruction hardware detection
- C176 instruction stack purging (normal)
- C173 compatible instruction stack purging (selectable, with 35% CPU slow down)
- CEJ/MEJ permanently enabled
- C176 014, 015 instructions are supported

b) 131K, 262K 60 bit words central memory (except THETA - 524K, 1048K)

c) Extended memory (not supported on S1)

- ECS (I and II)
- DDP model DC145
- Extended Semiconductor memory in ECS Mode
  - High Speed Port Maintenance Functions are supported in off-line mode only
  - Side Door Maintenance access is supported on-line by NOS only to the extent of maintaining the ESM single bit error hardware logs

d) 10x12, 15x24, 20x24 PP and Channel combinations

e) CYBER 170 PP instruction set

10.1.2 CURRENT CYBER 170 FEATURES NOT SUPPORTED

a) CPU

- Hardware error exit within CYBER 170 state
- Hardware CMU instructions (interpretive software)
- CPU halt on error exit with Monitor Flag set
- Dual processor configurations
- Hardware initialization of CYBER 170 state
- 017, 660 and 670 PASS instructions are used for A170 features (10.4.2)

b) 32K, 49K, 65K, 98K, 196K Central Memory

c) Extended Memory

- DDP model DC 135
- Extended semiconductor memory in ESM mode

d) Peripheral Processors

- Status Control Register
- Addressing 262K memory via the A register
- RPN instruction
- Multiple PP speeds
- 14 and 17 PP configurations (and 20 PP configuration for S1).
- 24XX, 25XX, 27XX, 641CH, 651CH, 661CH and 671CH PP instructions are used for A170 features (10.4.2).

10.1.3 EXTENSIONS TO CURRENT CYBER 170 (A170)

a) Required

- Up to two million words of executable memory (jobs restricted to 131K FL)

- A single job may address data arrays of greater than 131K (soft ECS)
- Extended PP access to central memory
- Very limited use of extended PP instruction set (16 bit instructions)
- Support of C180 maintenance channel

b) Not Supported

- Single job's code area greater than 131K
- Code and data sharing
- Security enhancements
- Virtual memory

10.2 PERIPHERALS SUPPORTED

Refer to Appendix C for a list of peripheral equipment supported in CYBER 170 state.

10.3 ECS COUPLER

- Optional and supports ECS and ESM, in ECS mode only
- Manufacturing cost objective is $10K/10th unit (including cabinet and cable)
- MTBF inherent objective is 15,000 hours
- Must be able to sustain a block transfer rate of one word every 100 ns

10.4 CYBER 170 STATE SOFTWARE

NOS/170 and NOS/BE operating system and product set software will initially be modified to run on C180 hardware in C170 state with the then current 170 capabilities. A subsequent release of NOS/170 (and NOS/BE) will be enhanced to support Advanced CYBER

170 features.

C170 SCOPE 2.0 software will not be supported on C180 systems.

10.4.1 SOFTWARE MODIFICATIONS

NOS and NOS/BE modification will be limited to those changes necessary to support the hardware differences listed in paragraphs 10.1.1 and 10.1.2. The modifications will be generally limited to the deadstart process, maintenance software, and PP routines which depend on timing characteristics, RPN or the Status Control Register. Exceptions may be granted by CPD system design, with ADLC approval, where the software modifications are minor or limited to support of specific CYBER 180 RAM features, peripherals or performance.

A CYBER 180 state system monitor is required to execute specific versions of NOS and NOS/BE in CYBER 170 state. This system monitor will be distributed in binary form. Source language, tools, and modifications to support non-standard systems will require a QSS. This monitor will not exceed 1024 words central memory resident on a 262K configuration.

The A170 software modifications must insure:

a) Deadstart

- Initialization and deadstart procedures are externally compatible.
- A C171-C175 system is able to deadstart and run specific versions of NOS and NOS/BE from the same deadstart tape or disk as an A170 system.
- Memory and system integrity are maintained when performing system initialization/deadstart and deadstart dumping procedures to guarantee proper restart/recoverability.
- A single deadstart dump capability which detects machine dependent conditions and presents all appropriate information to the user in a consistent notation.

b) CPU

- A consistent method of voiding the C170 and A170 instruction stacks for all O.S. and Product Set

software.

c) Software interpretation of CMU instructions

- When executing the CBL benchmark (paragraph 10.6), the total P2 time required to simulate CMU instructions must not exceed 19 times the CP time required to execute these same CMU instructions on the base CYBER 73 with CMU.

- No increase in 170 state memory requirements for system resident or individual jobs, beyond that taken by the CYBER 180 state system monitor.

- CMU instruction interpretation must be interruptable when execution time exceeds 0.3ms (P2).

- CMU instruction interpretation must cause no changes to users object code, i.e., no recompilation is required.

- CMU instruction interpretation solution must be the same for both NOS and NOS/BE.

- Resource accounting for CMU interpretation must be chargeable to the user.

- The CMU instruction interpretation solution must not inhibit compatibility between C170 and A170 system in a multi-mainframe environment.

- System throughput performance objectives as defined in Section 10.6 shall be achieved. (Benchmarks which realize more than 15% CPU time improvement between a non-CMU and CMU CYBER 73 need not meet these throughput objectives.)

10.4.2 SOFTWARE ENHANCEMENTS

a) NOS/170 only will be enhanced to extend the maximum amount of central memory supported from 262K words to 2M words. Since jobs remain restricted to 131K of executable CM, this implies more concurrent jobs and open files. Some job mixes may not realize significant performance improvement with the increased central memory. Extensions to NOS to relieve job/file limitations will be kept to a minimum and in reaction to specific marketing situations.

b) NOS/170 and NOS/BE will be enhanced to allow a single jobs

data area in extended central memory to be greater than 131K words (soft ECS). Total executable memory and soft ECS areas together cannot exceed 2 million words. When a configuration consists of both hard and soft ECS, only soft ECS will be available for user access.

c) Extended PP access to central memory will be provided in NOS to support greater than 262K of executable memory.

d) Use of C180 extended 16-bit PP instructions is allowed in C170 state only where no other mechanism is available to support the modifications or enhancements listed above. Any use of these instructions in C170 state requires approval by AD&C.

e) On-line remote maintenance, via standard communications interfaces.

10.5 CPU PERFORMANCE

Using the kernels (10 FTN Kernels, S-Profile, Composite), execute at the ratios:

	FTN Execution Ratio	Commercial Execution Ratio (4)	COST ADDITION PERCENTAGE Total (1) Incremental	COST ADDITION PERCENTAGE Fixed (2) Incremental
CYBER-73	1.0	1.0 (3)	N/A	N/A
P1	1.1	0.9	10.0	7.5
P2	2.9	1.5	4.8	2.4
P3	8.0	4.0	5.0	3.0
THETA	34.0	10.0	No Objective	No objective

(1) Total Incremental = total tenth unit CPU cost to provide CYBER 170 state

(2) Fixed Incremental = that portion of the incremental cost not subject to future cost elimination

(3) CYBER 73 base uses the CMU

(4) A170 ratios are for recompiled non-CMU code on A170 versus CMU code base on CYBER 73

10.6 SYSTEM PERFORMANCE

Running the SBL benchmark (scientific) and CBL benchmarks (commercial), achieve system throughput (elapsed time) at the following ratios (CYBER 73/CYBER 180):

	Scientific Elapsed Time	Commercial (2)(3) Elapsed Time	Configuration (5) Mem Size	Configuration (5) No.of Disks
CYBER 73 (1)	1.0	1.0	131KW	2
S1	1.0	1.0	2MB	5
S2	2.5	2.1	2MB	7
S3	7.5 (4)	6.0 (4)	4MB	12
THETA	25.0 (4)	9.1 (4)	8MB	18

(1) Base system is 131K CYBER 73 with CMU running NOS 1.1 level 430/428.

(2) A170 ratios use a recompiled non-CMU base versus CMU base for CYBER 73.

(3) The THETA commercial objectives are soft and subject to change based on cost- return evaluations.

(4) Multiple copies of the benchmark are run to achieve these ratios (9 for S3 and greater than 25 for THETA).

(5) The complete configuration is given in the Configuration Notebook.

10.7 MAINFRAME COSTS

Mainframe costs are based on assumptions given in 11.1.

10.0 CYBER 170 STATE
10.7 MAINFRAME COSTS

System	Processor	Memory	PP	Channels	Mainframe Cost
S1 Entry	1	1MB	10	12	$ 93,300
S1 Target	1	2MB	10	12	$105,800
S2 Entry	1	1MB	10	12	$208,000
S2 Target	1	2MB	15	18	$231,700
S3 Entry	1	2MB	10	12	$335,000
S3 Target	1	4MB	20	24	$376,000
THETA Entry	1	4MB	20	24	$967,000
THETA Target	1	8MB	20	24	$1,172,000

Packaging - The initial entry and target systems have 3 separate cabinets (CPU, Memory, IOU) costing an estimated $60-75,000. It is a requirement for S2 and an objective for S3 that subsequent packaging redesign accommodate these configurations in a manner which saves $25,000.

10.8 RAM

No separate CYBER 170 software support of CYBER 180 RAM hardware features is planned. This means that degrading either processors (by-pass cache, MAP) or memory will necessitate a deadstart recovery.

10.8.1 MEAN TIME BETWEEN SYSTEM DOWN INTERRUPTIONS (MTBI DOWN)

10.0 CYBER 170 STATE
10.8.1 MEAN TIME BETWEEN SYSTEM DOWN INTERRUPTIONS (MTBI DOWN)

MTBI(dn) (hrs) TARGET S1 SYSTEM 170 mode

POINT IN TIME	CPU	MEMORY	I/O	PERIPHS	O/S	TOTAL H/W	TOTAL SYS
On Release	225	-INC-	-INC-	3000	150	209	87
Six Months	285	-INC-	-INC-	3000	250	260	126
18 Months	372	-INC-	-INC-	3000	500	331	199

MTBI(dn) (hrs) TARGET S2 SYSTEM 170 mode

POINT IN TIME	CPU	MEMORY	I/O	PERIPHS	O/S	TOTAL H/W	TOTAL SYS
On Release	450	700	475	3000	100	164	62
Six Months	569	886	601	3000	200	205	101
18 Months	744	1158	786	3000	400	262	158

MTBI(dn) (hrs) TARGET S3 SYSTEM 170 mode

POINT IN TIME	CPU	MEMORY	I/O	PERIPHS	O/S	TOTAL H/W	TOTAL SYS
On Release	270	460	703	3000	75	131	48
Six Months	362	634	786	3000	150	168	79
18 Months	515	890	907	3000	300	222	126

10.0 CYBER 170 STATE
10.8.1 MEAN TIME BETWEEN SYSTEM DOWN INTERRUPTIONS (MTBI DOWN)

MTBI(dn) (hrs) T A R G E T T H E T A S Y S T E M 170 mode

POINT IN TIME	CPU	MEMORY	I/O	PERIPHS	O/S	TOTAL H/W	TOTAL SYS
On Release	105	255	718	3000	50	66	28
Six Months	141	400	764	3000	75	89	41
18 Months	200	613	831	3000	100	122	55

INC means included in the CPU.

10.0 CYBER 170 STATE
10.8.2 (#I) MEAN TIME BETWEEN SYSTEM DEGRADED INTERRUPTIONS

10.8.2 (#I) MEAN TIME BETWEEN SYSTEM DEGRADED INTERRUPTIONS

MTBI(dg) (hrs) T A R G E T S 1 S Y S T E M 170 mode

POINT IN TIME	CPU	MEMORY	I/O	PERIPHS	O/S	TOTAL H/W	TOTAL SYS
On Release	INFIN.	-INC-	-INC-	9000	6	7627	6
Six Months	INFIN.	-INC-	-INC-	9000	10	7627	10
18 Months	INFIN.	-INC-	-INC-	9000	21	7627	21

MTBI(dg) (hrs) T A R G E T S 2 S Y S T E M 170 mode

POINT IN TIME	CPU	MEMORY	I/O	PERIPHS	O/S	TOTAL H/W	TOTAL SYS
On Release	INFIN.	INFIN.	INFIN.	9000	4	9000	4
Six Months	INFIN.	INFIN.	INFIN.	9000	8	9000	8
18 Months	INFIN.	INFIN.	INFIN.	9000	17	9000	17

MTBI(dg) (hrs) T A R G E T S 3 S Y S T E M 170 mode

POINT IN TIME	CPU	MEMORY	I/O	PERIPHS	O/S	TOTAL H/W	TOTAL SYS
On Release	INFIN.	INFIN.	INFIN.	9000	3	9000	3
Six Months	INFIN.	INFIN.	INFIN.	9000	6	9000	6
18 Months	INFIN.	INFIN.	INFIN.	9000	13	9000	12

10.0 CYBER 170 STATE
10.8.2 (#I) MEAN TIME BETWEEN SYSTEM DEGRADED INTERRUPTIONS

MTBI(dg) (hrs)	T A R G E T	T H E T A	S Y S T E M	170 mode			
POINT IN TIME	CPU	MEMORY	I/O	PERIPHS	O/S	TOTAL H/W	TOTAL SYS
On Release	INFIN.	INFIN.	INFIN.	9000	2	9000	2
Six Months	INFIN.	INFIN.	INFIN.	9000	3	9000	3
18 Months	INFIN.	INFIN.	INFIN.	9000	4	9000	4

INC means included in the CPU.

INFIN. means no redundancy, so any failure causes a system interruption.

10.0 CYBER 170 STATE
10.8.3 MEAN LOST TIME DUE TO SYSTEM DOWN INTERRUPTIONS (MLT DOWN)

10.8.3 MEAN LOST TIME DUE TO SYSTEM DOWN INTERRUPTIONS (MLT DOWN)

The Mean Lost Time is defined in units of minutes per failure. Objectives for S1-THETA systems are shown in the following tables.

MLT(dn) (mins)	T A R G E T	S 1	S Y S T E M	170 mode			
POINT IN TIME	CPU	MEMORY	I/O	PERIPHS	O/S	TOTAL H/W	TOTAL SYS
On Release	150	-INC-	-INC-	180	36	152	84
Six Months	150	-INC-	-INC-	180	36	153	93
18 Months	150	-INC-	-INC-	180	36	153	107

MLT(dn) (mins)	T A R G E T	S 2	S Y S T E M	170 mode			
POINT IN TIME	CPU	MEMORY	I/O	PERIPHS	O/S	TOTAL H/W	TOTAL SYS
On Release	150	120	150	180	24	145	70
Six Months	150	120	150	180	24	145	84
18 Months	150	111	150	180	24	144	96

10.0 CYBER 170 STATE
10.8.3 MEAN LOST TIME DUE TO SYSTEM DOWN INTERRUPTIONS (MLT DOWN)

MLT(dn) (mins) T A R G E T S 3 S Y S T E M 170 mode

POINT IN TIME	CPU	MEMORY	I/O	PERIPHS	O/S	TOTAL H/W	TOTAL SYS
On Release	150	120	150	180	18	143	63
Six Months	150	120	150	180	18	144	77
18 Months	150	111	135	180	18	139	87

MLT(dn) (mins) T A R G E T T H E T A S Y S T E M 170 mode

POINT IN TIME	CPU	MEMORY	I/O	PERIPHS	O/S	TOTAL H/W	TOTAL SYS
On Release	210	150	135	180	12	167	87
Six Months	210	150	135	180	12	167	92
18 Months	210	150	126	180	12	164	90

INC means included in the CPU.

10.0 CYBER 170 STATE
10.8.4 MEAN LOST TIME DUE TO SYSTEM DEGRADED INTERRUPTIONS(MLT DG)

10.8.4 MEAN LOST TIME DUE TO SYSTEM DEGRADED INTERRUPTIONS(MLT DG)

MLT(dg) (mins) T A R G E T S 1 S Y S T E M 170 mode

POINT IN TIME	CPU	MEMORY	I/O	PERIPHS	O/S	TOTAL H/W	TOTAL SYS
On Release	0	-INC-	-INC-	105	10	89	10
Six Months	0	-INC-	-INC-	105	10	89	10
18 Months	0	-INC-	-INC-	105	10	89	10

MLT(dg) (mins) T A R G E T S 2 S Y S T E M 170 mode

POINT IN TIME	CPU	MEMORY	I/O	PERIPHS	O/S	TOTAL H/W	TOTAL SYS
On Release	0	0	0	105	6	105	6
Six Months	0	0	0	105	6	105	6
18 Months	0	0	0	105	6	105	6

MLT(dg) (mins) T A R G E T S 3 S Y S T E M 170 mode

POINT IN TIME	CPU	MEMORY	I/O	PERIPHS	O/S	TOTAL H/W	TOTAL SYS
On Release	0	0	0	105	4	105	4
Six Months	0	0	0	105	4	105	4
18 Months	0	0	0	105	4	105	4

10.0 CYBER 170 STATE
10.8.4 MEAN LOST TIME DUE TO SYSTEM DEGRADED INTERRUPTIONS(MLT DG)

MLT(dg) (mins) T A R G E T T H E T A S Y S T E M 170 mode

POINT IN TIME	CPU	MEMORY	I/O	PERIPHS	O/S	TOTAL H/W	TOTAL SYS
On Release	0	0	0	105	2	105	2
Six Months	0	0	0	105	2	105	2
18 Months	0	0	0	105	2	105	2

INC means included in the CPU.

Zero MLT occurs when all failures are interrupts, i.e., no degraded failures.

10.8.5 DATA ERRORS

a) Recoverable Data Errors
To be furnished

b) Unrecoverable Data Errors
To be furnished

c) Undetected Data Errors
To be furnished

10.8.6 USER AVAILABILITY

To be furnished

10.8.7 NET AVAILABILITY

The objectives include:

- the time taken for an engineer to get to the site to repair the failure.

- the time taken to effect the repair (MTTR).

10.0 CYBER 170 STATE
10.8.7 NET AVAILABILITY

- the time taken to restore the system to its original state and re-run time necessitated by the failure. Weighted rerun times are used in the calculations, based on the failing equipment type.

- time taken on preventive maintenance, assuming this is conducted by a single engineer.

10.0 CYBER 170 STATE
10.8.7 NET AVAILABILITY

The objectives exclude:

- time to make changes to the hardware (FCO's).

- time to make changes to the software (PSR's).

SYSTEM AVAILABILITY OBJECTIVES - CYBER 170

TIME PERIOD	S1	S2	S3	THETA
On Release	98.11	97.58	97.09	93.76
6 Months	98.51	98.06	97.68	95.12
18 Months	98.83	98.43	98.16	96.18

10.8.8 MAINTENANCE SOFTWARE

All maintenance software objectives in this document are the same as CYBER 180 objectives unless specifically stated for CYBER 170 state.

11.0 COMPONENT CHARACTERISTICS

11.0 COMPONENT CHARACTERISTICS

11.1 COMPONENT COST OBJECTIVES

- Processor and memory costs are for the 10th unit.

- The manufacturing learning curve is assumed to be 90% exclusive of cost inflation.

- The memory and processor costs are quoted for the year in which the 10th unit would be sold according to the forecasts in Appendix E.

- System Test and Checkout (STCO) costs are included on a component basis. All system tests beyond STCO are cost of sales incurred by Systems Division and not included in manufacturing standard cost.

- Cost inflation rate for mainframe components is assumed to continue at rate of most recent five years.

11.1.1 CPU'S

		Target MFG Cost
P2 (no options)		72,000
Options	a) 16K byte cache (performance)	4,500
	b) Performance Monitoring Facility	2,000
P3 (no options)		184,000
	d) 16K byte cache (performance)	8,000
	e) Performance Monitoring Facility	2,000
THETA CPU (including Performance Monitoring Facility)		550,000

11.1.2 S1

	Target MFG Cost
Basic S1 includes:	75,800
1 P1	
1 M1 with 1M byte	
1 S1 IOU cluster with:	
-5 PP's	
-8 CYBER 170 I/O Channels	
-maintenance channel connections to P1 & M1	
-2 port MUX (for console)	
S1 Mainframe add-ons	
1M byte Central Memory increment, applies up to a total of 4M bytes	7,500
5 PP increment applies up to a total of 10 PP's	3,500
2 Channel increment applies up to a total size of 12 channels	1,500

11.1.3 MEMORY

	Target MFG Cost
Memory, 16K Chip	
M2-1 (MB)	72,000
M2-2 (MB)	78,000
M2-4 (MB)	89,000
M2-6 (MB)	104,000
M2-8 (MB)	115,000
M2-12 (MB)	141,000
M2-16 (MB)	166,000
M3-2 (MB)	85,000
M3-4 (MB)	98,000
M3-6 (MB)	115,000

M3-8 (MB)	125,000
M3-12 (MB)	155,000
M3-16 (MB)	180,000
IHEIA Memory, If 4K Chip	
4 MB	330,000
8 MB	530,000
12 MB	860,000
16 MB	1,050,000

11.1.4 STAND-ALONE I/O UNIT (IOU2)

	Target MFG Cost
Basic I/O Unit includes - 5 PP's X 8 Channels - 2 Port MUX - 2 maintenance channel connections	47,000
Additional 5-PP increments (up to a maximum of 20 PP's)	3,000
Additional 2-Channel increments (up to a maximum of 24 Channels)	1,500
Optional maintenance channel pair connections (up to a maximum of 6 connections)	700

11.1.5 OTHER

Motor Generator Set

KVA	Frequency (Hz)	Ride-Thru (Secs)	Quietized	Target Cost ($)
112.5	50	0.075	Yes	9750
112.5	60	0.075	Yes	7400
125.0	50	0.5	No	9000
125.0	60	0.5	No	9000
125.0	50	2.5	Yes	13000
125.0	60	2.5	Yes	13000
140.0	50	2.5	No	13000
140.0	60	2.5	No	13000
180.0	50	2.5	No	22000*
180.0	60	2.5	No	22000*

* Approximate figures.

	Target MFG Cost
Power Control Panel	*
S1	2,000
S2-THETA w/Dewpoint Sensing	2,700
Optional	
Environment Monitor	5,000
Console (752)	1,000
High-performance Console	7,700
High-performance Console Controller	
S2 and above	800
S1	500
Power Control Panel Including Dewpoint Sensing	2,700

11.2 COMPONENT MAINTENANCE COST OBJECTIVES

The monthly maintenance cost for CYBER 180 mainframe components incurred by the supporting field service organization must not exceed the following levels (expressed as a percentage of manufacturing cost):

Mainframe Component	Life Cycle Average Monthly Maintenance Cost	Second Year Monthly Maintenance Cost Objective
S1	0.67% (590)	0.85% (750)
P2	0.61% (430)	0.76% (545)
M2	0.42% (360)	0.52% (462)
P3/M3	0.51% (1540)	0.64% (1970)
THETA	0.44% (4660)	0.54% (5800)

11.0 COMPONENT CHARACTERISTICS
11.2 COMPONENT MAINTENANCE COST OBJECTIVES

IOU	0.65% (380)	0.81% (480)

These costs are defined to include both the direct cost of maintaining the equipment and the allocation of various indirect costs as described in 8.3.2.1. The dollar figures are given, for information, in parentheses. The figures for the IOU represent a 10PP, 15 channel configuration.

11.0 COMPONENT CHARACTERISTICS
11.3 COMPONENT RELIABILITY OBJECTIVES

11.3 COMPONENT RELIABILITY OBJECTIVES

COMPONENT	Funct'l Inher't MTBF (Hours)	Elemntl Inherent MTBF (Hours)	MTTR (mins) Release	6 Mths	18 Mths	36 Mths
S1 Mainframe,1MB	1600	1300	60	60	45	30
P2 Processor	2250	1800	60	60	45	30
P3 Processor	2570	1800	60	60	45	30
THETA Processor	760	700	120	120	90	60
M2-1 Memory	2800	1400	30	30	20	15
M2-2 Memory	2300	900	30	30	20	15
M2-4 Memory	1700	600	30	30	20	15
M2-6 Memory	1350	500	30	30	20	15
M2-8 Memory	1100	403	30	30	20	15
M2-12 Memory	800	335	30	30	20	15
M2-16 Memory	700	270	30	30	20	15
M3-2 Memory	2300	900	30	30	20	15
M3-4 Memory	1700	600	30	30	20	15
M3-6 Memory	1350	500	30	30	20	15
M3-8 Memory	1100	400	30	30	20	15
M3-12 Memory	800	335	30	30	20	15
M3-16 Memory	700	270	30	30	20	15
THETA-4 Memory	1350	500	30	30	20	15
THETA-8 Memory	1100	400	30	30	20	15
THETA-12 Memory	800	335	30	30	20	15
THETA-16 Memory	700	270	30	30	20	15
I/O Unit	(See Below)	(See Below)	60	60	45	30
System Power		45000	120	120	120	120

The functional and elemental inherent MTBF objectives for the stand-alone IOU are identical for each configuration. Representative IOU configurations are shown below:

PPU'S	CHANNELS				
	8	12	16	20	24
5	2900	2800	2600	2500	2300
10	N/A	2500	2300	2200	2100
15	N/A	N/A	2000	1900	1800
20	N/A	N/A	N/A	1700	1600

The functional and elemental inherent MTBF for the Configuration and Environment Monitor (CEM) will exceed 15000 hours.

11.4 COMPONENT CONFIGURATION OBJECTIVES

11.4.1 CENTRAL MEMORY SIZES

The major requirements for central memory sizes of two megabyte and below for the M1, M2 and M3 are to provide additional models in CYBER 170 state. The memory sizes identified are the increments to be offered from a marketing standpoint. This does not mean that costs must be directly relatable to memory sizes.

Central Memory Size	M1	M2	M3	IHEIA
1 MB	X	X	X	
2 MB	X	X	X	
3 MB	X	X	X	
4 MB	X	X	X	X
5 MB	X	X		
6 MB	X	X	X	
7 MB	X	X		
8 MB	X	X	X	X
10 MB		X		
12 MB		X	X	X
14 MB		X		
16 MB		X	X	X
20 MB			X	
24 MB			X	
28 MB			X	
32 MB			X	

11.4.2 CENTRAL MEMORY DEGRADE CAPABILITY

Central memory degradation is required primarily in CYBER 170 state operations. A physical switch in M1, M2, M3 or THETA reduces memory capacity by an increment that varies depending on the failing address(es), but in no case to a degraded size less than the minimum shown below (except THETA 4MB memory is not degradable).

Initial Central Memory Size	Minimum Degraded Size
2-3 MB	1 MB
4-7 MB	2 MB
8-12 MB	4 MB
14 MB	6 MB
16-24 MB	8 MB
28 MB	12 MB
32 MB	16 MB

11.5 CALENDAR LIFE

The calendar life for all CYBER 180 mainframe components is not less than ten years.

11.6 PREVENTIVE MAINTENANCE (PM)

The number of hours or preventive maintenance per 1000 scheduled operating hours shall not exceed the numbers quoted below. This includes "hands-on" PM as well as PM performance from a remote location, but excludes PM normally performed by an operator.

Mainframe Component	Hours PM per 1000 Hours Operated
S1	1.5
P2	1.5
M2	1.5
P3/M3	3.0
THETA	8.0
IOU	1.5

12.0 APPENDICES

12.1 (#) APPENDIX A - DEVELOPMENT COST

The following cost forecast appeared in the CYBER 180 Program Plan, Rev. E, dated 04/15/78. Check the Program Plan, Appendix C, for the most current cost forecast.

AREA Summary — LIFE COSTS — REPORT DATED 4/15/78
FUNDING TYPE R&D and OCS

		YEAR									
PRODUCT	PRIOR YR.	1978	1979	1980	1981	1982	1983	1984	1985	1986	FUTURE	TOTAL
R&D												
Hardware	13883	13573	14539	12137	11190	7207	6878	3160	2296	2422	9253	96538
Software	3592	3675	6183	9381	10575	8238	7893	7651	7500	7500	13000	85188
Publications	299	450	886	1482	1573	1716	1784	1366	1250	1167	3610	15803
NPP	1446	620	665	750	880	950	1020	1050	1050	1050	3000	12481
Subtotal	19220	18318	22273	23750	24238	18111	17575	13227	12096	12139	29063	210010
OCS												
Hardware	50	73	127	1393	2800	3898	4009	3999	2849	2631	6236	28065
Software	0	0	0	51	105	1588	1816	1779	1855	1948	18000	27144
Publications	0	0	22	240	378	283	286	456	525	451	1291	3931
Subtotal	50	73	149	1684	3283	5769	6111	6234	5229	5030	25527	59140
TOTAL	19270	18467	22422	25434	27521	23880	23686	19461	17325	17169	54590	269150

12.2 APPENDIX B - CYBER 180 SYSTEM DESIGN OBJECTIVES

The S1, S2, S3 and THETA Systems will conform to the objectives stated in the main body of this Architectural Objectives/Requirements document. This appendix describes the unique characteristics of the S1, S2, S3 and THETA Systems as they fall within the range of the CYBER 180 product line.

For CYBER 180, this document takes the place of the various System Design Objectives (DO) documents usually written for a new product line. Information normally found in a System DO but not included in the body of the Architectural Objectives/Requirements is contained in this appendix.

OBJECTIVE	S1	S2	S3	THETA
Schedule/Milestone	APP.F	APP.F	APP.F	APP.F
Target Lease Range	$14-35K	$30-65K	$60-120K	TBF
System Configurations	APP.D	APP.D	APP.D	APP.D
Number of CPU's	1-2	1-2	1-2	1-2
Memory				
-Size	1MB-8MB	1MB-16MB	2MB-32MB	4MB-16MB
-Number of Memory Ports	3	4	5	5
-Memory Interleave	4-8	4-8	8-16	16-32
-Reconfigure/ Hardware	Interleave/ Non-Interl.	Interleave/ Non-Interl.	Interleave/ Non-Interl.	Interleave/ Non-Interl.
-Reconfigure/ Software	Page Size (512B-65KB)	Page Size (512B-65KB)	Page Size (512B-65KB)	Page Size (512B-65KB)
I/O				
-Concurrent I/O	18 contr.	18 contr.	18 contr.	18 contr.
-I/O Bandwidth	12 MB/s	50 MB/s	50 MB/s	50 MB/s
-Maximum Peripheral Rate	2 MB/s	5 MB/s	5 MB/s	5 MB/s
System Performance	Sec.7	Sec.7	Sec.7	Sec.7
System Reliability	Sec.8	Sec.8	Sec.8	Sec.8
System Availability	Sec.8	Sec.8	Sec.8	Sec.8
Manufacturing Cost	APP.D	APP.D	APP.D	APP.D
System Maintenance Cost	Sec.8	Sec.8	Sec.8	Sec.8
FCO Rate	Sec.8	Sec.8	Sec.8	Sec.8
PSR Rate	Sec.8	Sec.8	Sec.8	Sec.8

MB = Megabyte
TBF = To Be Furnished

12.0 APPENDICES
12.2 APPENDIX B - CYBER 180 SYSTEM DESIGN OBJECTIVES

Glossary for CYBER 180 System Objectives

SCHEDULE/MILESTONES	The quarter in which pre-production systems are delivered to controlled customer installations.
TARGET LEASE RANGE	The Auerbach lease range to be covered by the system, including maintenance and software.
NO. OF CPU'S	System software will support hardware configurations with this range of like central processors.
NO. MEMORY PORTS	Number of memory ports available for CPU, IOU, ECS or Common memory.
MEMORY SIZE	The range of central memory capacity that can be configured into the system. Note that the maximum capacities are required only for large dual-CPU systems and can be satisfied with two memory units.
MEMORY INTERLEAVE	The number of individually cyclable memory modules over which 64 bit word addresses are sequentially assigned to assist in randomizing accesses to those modules.
RECONFIGURE BY HARDWARE	Hardware capability to reconfigure around memory failures.
RECONFIGURE BY SOFTWARE	The page sizes of memory that can be mapped out of use by software to minimize the effects of error conditions.
CONCURRENT I/O	The number of peripheral controllers or communications controllers that can be operating concurrently under system software control.
I/O BANDWIDTH	The maximum I/O bandwidth that the system must support in simultaneous transfers to or from I/O devices.
MAX. PERIPHERAL RATE	The highest instantaneous transfer rate from a single peripheral that will be supported by the system.

12.0 APPENDICES
12.2 APPENDIX B - CYBER 180 SYSTEM DESIGN OBJECTIVES

SYSTEM PERFORMANCE	System performance objectives and benchmarks.
SYSTEM RELIABILITY	System MTBI and MLT Objectives.
SYSTEM AVAILABILITY	System Availability objectives.
MANUFACTURING COST	System and component manufacturing costs.
SYSTEM MAINTENANCE COST	System and component maintenance costs.
FCO RATE	Field change order objectives for hardware.
PSR RATE	Software maintenance cost objectives.

12.3 (#) APPENDIX C - PERIPHERALS SUPPORTED AND COSTS

"Supported CYBER 170 O.S." means supported by NOS or NOS/BE software.

"Supported CYBER 180 O.S." means supported by NOS/BE. Where a product is supported in both states, the CYBER 170 channel and unmodified controller is used for CYBER 180 state. Changes in controlware and recording format are not precluded.

Manufacturing costs are for 1980. If the equipment is in production now, the cost is based on the present standard manufacturing cost. For new equipment, the cost is an estimate by the appropriate development organization.

PERIPHERAL EQUIPMENT & CONTROLLERS	COST	SUPPORTED CYBER 170 O.S.	SUPPORTED CYBER 180 O.S.
MASS STORAGE EQUIPMENT			
885 Fixed Module Disk Drive (FMD) (two spindles)	14800	Serial Recording	Serial (R1) & Parallel (R1) Recording
FMD/844 Disk Controller (7155-X) (Serial Recording) (C170 Channel)	9000	Yes	Yes (R1)
FMD/844 Disk Controller (Serial & Parallel Recording) (C180 Channel)	9000	Yes*	Yes (R2)
844-4X Disk Drive	6100	Yes	Yes (R1)
844-4X Disk Controller (7154-X)	14000	Yes	Yes (R1)
819 Disk Drive	tbf	No	No
819 Disk Controller	tbf	No	No

* THETA/170 only.

PERIPHERAL EQUIPMENT & CONTROLLERS	COST	SUPPORTED CYBER 170 O.S.	SUPPORTED CYBER 180 O.S.
MAGNETIC TAPE EQUIPMENT			
66X Tape Drive	12000	Yes	Yes (R2)
66X Tape Controller (7021-21,-22)	11500	Yes	Yes (R2)
67X Tape Drive	10000	Yes	Yes (R1)
67X Tape Controller (7021-3X)	11100	Yes	Yes (R1)
MSS Tape Library (Includes controller)	130000	Yes	No
MSS Tape Library (Second Generation)	TBF	No	Yes (TBD)
PRINTER EQUIPMENT			
580-12,-16,-20 Printer (1200,1600,2000 lpm) (Includes controller)	21500	Yes	Yes (R2)
580-120,-160,-200 Printer (1200, 1600, 2000 lpm) (Includes controller)	21500	Yes	Yes (R2)
596 Train	1740	Yes	Yes (R2)
Non-Impact Printer (8000 lpm) (Includes C170 controller)	20600	Yes	Yes (R2)
Non-Impact Printer (8000 lpm) (Includes C180 controller)	27100	No	Yes (R3)
Non-Impact Printer (20000 lpm)	tbf	No	Yes (TBD)

12.0 APPENDICES
12.3 (8) APPENDIX C - PERIPHERALS SUPPORTED AND COSTS

PERIPHERAL EQUIPMENT & CONTROLLERS	COST	SUPPORTED CYBER 170 O.S.	SUPPORTED CYBER 180 O.S.
CARD EQUIPMENT			
405 Card Reader (1200 cpm)	16200	Yes	Yes (R2)
405 Card Reader Controller	4500	Yes	Yes (R2)
415 Card Punch (250 cpm) (includes 3446/3644 controller)	20500	Yes	No
MISCELLANEOUS EQUIPMENT			
2550-2, 2552-1 Communication Cont		Yes	No
12 lines	37000		
20 lines	41000		
100 lines	105000		
2551-1,-2 Communication Contr.	tbf	Yes	Yes (R2)
752-10 Display/keyboard (as console)	1000	No	Yes (R2)*
CC545 Display/keyboard Console	7700	Yes	(R2)
6681-2 Data Channel Converter		Yes	Yes
1 channel	4100		(R2)
2 channels	6400		
3 channels	8700		
4 channels	11000		
6683 Channel Coupler	tbf	Yes	Yes (R2-180/170) (R3-180/180)
BATCH TERMINAL EQUIPMENT			
CYBER 18-5 Batch Terminal	19000	Yes	Yes (R2)

12.0 APPENDICES
12.3 (8) APPENDIX C - PERIPHERALS SUPPORTED AND COSTS

1829-60 Card Reader (600 cpm)		Yes	Yes (R2)	
1827-600 Band Printer (600lpm)		Yes	Yes (R2)	
Card Punch (100cpm)	tbf	Yes	Yes (R2)	

* Supported at R1 for debug facility.

12.3.1 TERMINALS SUPPORT (APP.C)

The following terminals are supported by Network Products in CYBER 170 and CYBER 180 states:

CDC 200 UT, 214, 217, 731-12, 732-12, 734-1

CDC 711-10 with option 102-Data Control

CDC 714 except for impact printer/non-impact printer

CDC CY18-xx as 200 UT, 2780/3780, or HASP multi-leaving terminal

CDC 713-10, 751, 752, 756

TTY M33, M35, M37, M38, M40

IBM 2741 (EBCDIC or Correspondence) - with Transmit and Receive Interrupt features

IBM 2780/3780

IBM 360/20 as a HASP multi-leaving terminal

IBM 3270

Tektronix 4010, 4014, 4013

Hazeltine 2000

GSI 300, 300Q

DEC writer II

Anderson-Jacobson 803 with Diablo wheel

HARRIS 1200 HASP multi-leaving terminal

DATA100 78 HASP multi-leaving terminal

C18 based Full Duplex Batch terminal

Commonly used future terminals

These terminals are supported using the CDC Mode 4, HASP, Binary synchronous and asynchronous line protocols. The APL character set is supported on those terminals which offer it as an option. New terminal developments needed in industries in which CYBER 180 is marketed will be supported.

In addition, the network provides the basis for an interface to Value Added Networks (VANs), such as TELENET, DATAPAC and TRANSPAC, using the X.25 communications protocol. Support is provided for a subset of X.25 consisting of Level 1, Level 2 and the Permanent Virtual Circuits only of Level 3. It is the intent to track standardization activities in this area and implement to the standards as they evolve.

12.4 (#) APPENDIX D - SYSTEM CONFIGURATIONS AND COSTS

The configuration assumptions and component characteristics were used as the base to calculate the RAM objectives, Performance Objectives, and Cost Objectives.

General Remarks

- The system configurations shown are representative systems. Optimal configuration for each installation, as a function of its application environment, may deviate significantly from the typical system.
- Only single mainframe system configurations are included at this time, multi-mainframe configurations will be added.
- New peripheral products, e.g., Mass Storage Subsystem, non-impact printer, helical scan tapes, swapping memory,etc. will be included as design specifications become firm.
- Entry system is defined as the minimum system to run production. Target system is one that runs a full production load reliably, and is the one against which objectives will be measured. Large system is defined as a dual-CPU system with representative supporting components. The target systems have been configured to maximize reliability regardless of cost. For example, they contain MG sets with 2 1/2 second ride-through capabilities as opposed to the entry and large system which do not.
- Mainframe costs are based on the assumptions given in 11.1, and peripheral costs are based on those given in Appendix C.
- The power requirements for an individual system must be assessed for that system. The ratings of the MG-sets specified for "entry", "target" and "large" systems have been calculated for those specific configurations.

12.4.1 S1 SYSTEM (APP.D)

S1 SYSTEM/C180 STATE	ENTRY		TARGET		LARGE	
COMPONENT	QUANT	MFG COST	QUANT	MFG COST	QUANT	MFG COST
Processor	1	75300	1	87800	2	155800
Memory	1MB	(incl.)	2MB	(incl.)	4MB	(incl.)
I/O Unit		(incl.)		(incl.)		(incl.)
-PP'S	5		10		10	
-I/O Channels	8		10		12	
-Maintenance Channels	3		3		3	
-Two Port Multiplexer	1	500	1	500	1	500
System Power	1	7400	1	13000	1	9000
Power Control Panel	1	2000	1	2000	1	2000
Environment Monitor			1	5000.	1	5000
MAINFRAME COST		85200		108300		172300

S1 SYSTEM/C180 STATE	ENTRY		TARGET		LARGE	
COMPONENT	QUANT	MFG COST	QUANT	MFG COST	QUANT	MFG COST
Fixed Module Disk Drive (Two Spindles/Module)			1	14800	2	29600
844-4X Disk Drive	2	12200	2	12200	4	24400
FMD/844 Disk Controller	1	9000	2	18000	2	18000
67X Tape Drive			3	30000	6	60000
67X Tape Controller (7021-3X)			1	11100	2	22200
6681-2 Data Channel Converter					1	4100
405 Card Reader/Ctr					1	20700
580-20 Line Printer					1	21500
CYBER 18-5 Batch Terminal 600 lpm Band Printer 600 cpm Card Reader	1	19000	2	38000		
255X Comm. Front End - Communication Lines	1 12	37000	2 112	105000	2 112	105000
752-10 System Console	1	1000	1	1000		
CC545 System Console/Ctr					1	8000
PERIPHERAL COST		78200		230100		313500
TOTAL COST		164100		339100		486500
RMS STORAGE BILLION BYTES	0.4		1.6		3.2	

Note: System costs are based on assumptions given in 11.1

12.0 APPENDICES
12.4.2

12.4.2 S2 SYSTEM (APP. D)

S2 SYSTEM/C180 STATE	ENTRY		TARGET		LARGE	
COMPONENT	QUANT	MFG COST	QUANT	MFG COST	QUANT	MFG COST
Processor	1	72000	1	72000	2	144000
Memory	1MB	72000	4MB	89000	8MB	130000
I/O Unit	1	47000	1	51500	1	59000
-PP'S	5		10		15	
-I/O Channels	8		10		16	
-Maintenance Channels	2		4	700	4	700
-Two Port Multiplexer	1		1		1	
System Power	1	9000	1	13000	1	13000
Power Control Panel	1	2700	1	2700	1	2700
Environment Monitor			1	5000	1	5000
MAINFRAME COST		202700		233900		339400

12.0 APPENDICES
12.4.2 S2 SYSTEM (APP.D)

S2 SYSTEM/C180 STATE	ENTRY		TARGET		LARGE	
COMPONENT	QUANT	MFG COST	QUANT	MFG COST	QUANT	MFG COST
Fixed Module Disk Drive (Two Spindles/Module)			1	14800	4	59200
844-4X Disk Drive	2	12200	3	18300	6	36600
FMD/844 Disk Controller	1	9000	2	18000	4	36000
67X Tape Drive	2	20000	4	40000	8	80000
67X Tape Controller	1	11100	1	11100	2	22200
6681-2 Data Channel Converter			1	4100	1	4100
405 Card Reader/Ctr			1	20700	2	41400
580-20 Line Printer			1	21500	1	21500
NIP - 8000 lpm (C180)					1	27100
CYBER 18-5 Batch Terminal 600 lpm Band Printer 600 cpm Reader	1	19000				
255X Comm. Front End - Communication Lines	1 12	37000	2 112	105000	2 112	105000
752-10 System Console	1	1000				
CC545 System Console/Ctr			1	8500	1	8500
PERIPHERAL COST		109300		262000		441600
TOTAL COST		312000		495900		781000
RMS STORAGE BILLION BYTES	0.4		1.8		6.0	

** Packaging - The initial ENTRY and TARGET systems have 3 separate cabinets (CPU, Memory, IOU) costing an estimated $60-75,000 of mainframe. It is a requirement that subsequent packaging redesign accommodate these configurations in a manner which saves $25,000.

12.0 APPENDICES
12.4.2 S2 SYSTEM (APP.D)

Note: System costs are based on assumptions given in 11.1.

12.0 APPENDICES
12.4.3 S3 SYSTEM (APP.D)

12.4.3 S3 SYSTEM (APP.D)

S3 SYSTEM/C180 STATE	ENTRY		TARGET		LARGE	
COMPONENT	QUANT	MFG COST	QUANT	MFG COST	QUANT	MFG COST
Processor	1	184000	1	184000	2	368000
16K Byte Cache Increment			1	8000	2	16000
Memory	2MB	85000	6MB	130000	12MB	155000
I/O Unit	1	51300	1	59000	1	66000
-PP*S	10		15		20	
-I/O Channels	10		16		24	
-Maintenance Channels	2		2		2	
-Two Port Multiplexer	1		1		1	
System Power	1	13000	1	13000	1	22000
Power Control Panel	1	2700	1	2700	1	2700
Environment Monitor			1	5000	1	5000
MAINFRAME COST		336200		390200		636700

12.0 APPENDICES
12.4.3 S3 SYSTEM (APP.D)

S3 SYSTEM/C160 STATE	ENTRY		TARGET		LARGE	
COMPONENT	QUANT	MFG COST	QUANT	MFG COST	QUANT	MFG COST
Fixed Module Disk Drive (Two Spindles/Module)	1	14800	4	59200	8	118400
844-4X Disk Drive	3	18300	4	24400	8	48800
FMD/844 Disk Controller	2	18000	4	36000	7	63000
67X Tape Drive	4	40000	6	60000	8	80000
67X Tape Controller	1	11100	2	22200	2	22200
6661-2 Data Channel	1	4100	1	4100	1	4100
405 Card Reader/Ctr	1	20700	2	41400	2	41400
580-20 Line Printer	1	21500	1	21500	2	43000
NIP - 8000 lpm (C160)			1	27100	1	27100
2550 Comm. Front End	1	42000	2	105000	2	105000
- Communication Lines	20		112		112	
CC545 System Console/Ctr	1	8500	1	8500	1	8500
PERIPHERAL COST		199000		409400		561500
TOTAL COST		535200		799600		1198200
FMS STORAGE BILLION BYTES	1.8		5.6		11.2	

** Packaging - The initial ENTRY and TARGET system have 3 separate cabinets (CPU, Memory, IOU) costing an estimated $60-75,000. It is an objective that subsequent packaging redesign accommodate these configurations in a manner which save $25,000.

Note: System costs are based on assumptions given in 11.1

12.0 APPENDICES
12.4.4 THETA SYSTEM (APP.D)

12.4.4 THETA SYSTEM (APP.D)

THETA SYSTEM/C160 STATE	ENTRY		TARGET		LARGE	
COMPONENT	QUANT	MFG COST	QUANT	MFG COST	QUANT	MFG COST
Processor	1	550000	1	550000	2	1100000
Memory	4MB	330000	8MB	530000	16MB	1050000
I/O Unit	1	51500	1	68000	1	68000
-PP*S	10		20		20	
-I/O Channels	10		24		24	
-Maintenance Channels	2		2		2	
-Two Port Multiplexer	1		1		1	
System Power	1	22000	1	22000	1	44000
Power Control Panel	1	2700	1	2700	1	2700
Environment Monitor			1	5000	1	5000
MAINFRAME COST		956200		1177700		2269700

12.0 APPENDICES
12.4.4 THETA SYSTEM (APP.D)

THETA SYSTEM/C180 STATE	ENTRY		TARGET		LARGE	
COMPONENT	QUANT	MFG COST	QUANT	MFG COST	QUANT	MFG COST
Fixed Module Drive (4 Head Parallel) (Two Spindles/Module)	3	44400	7	103600	12	177600
844-4X Disk Drive	4	24400	6	36600	8	48800
FHD/844 Controller (Parallel)	3	27000	6	54000	8	72000
67X Tape Drive	4	40000	6	60000	8	80000
67X Tape Controller	1	11100	2	22200	2	22200
6681-2 Data Channel Converter	1	4100	1	4100	1	4100
405 Card Reader/Ctr	1	20700	2	41400	2	41400
580-20 Line Printer	1	21500	2	43000	2	43000
NIP - 8000 lpm (C180)	1	27100	1	27100	2	54200
2550 Comm. Front End	1	52500	2	105000	3	157500
- Communication Lines	50		112		150	
CC545 System Console/Ctr	1	8500	1	8500	1	8500
PERIPHERAL COST		281300		505500		709300
TOTAL COST		1237500		1683200		2979000
RMS STORAGE BILLION BYTES	4.4		9.6		16.0	

Note: System costs are based on assumptions given in 11.1.

12.0 APPENDICES
12.5 APPENDIX E - SHIPMENT FORECASTS

12.5 APPENDIX E - SHIPMENT FORECASTS

The following data is based on the CYBER 180 Product Life Forecast by D.L.Mueller and B.L.Thompson, dated April 14, 1978. The figures are for system acceptances, including both new builds and returned systems. Reconciliation with previous forecasts are as follows:

Model 820 was formerly the S1.
Model 840 was formerly the S2.
Model 850 was formerly the S3.
Model 860 is a new model, not yet defined in AO/R.
Model 870 was formerly the C-170 and S4, now THETA.
Model 880 was formerly the S5, not yet defined in AO/R.

	1980	1981	1982	1983	1984	1985	1986	1987	1988	1989	1990	TOTAL
820	-	18	40	38	37	34	31	29	25	24	21	297
840	24	33	49	48	41	34	36	44	37	36	33	415
850	-	7	13	25	25	23	23	25	23	21	20	205
860	-	-	-	7	12	15	17	19	17	15	12	114
870	-	-	4	5	6	7	10	10	9	7	6	64
880	-	-	-	-	-	-	3	4	5	6	5	23
TOT	24	58	106	123	121	113	120	131	116	109	97	1118

12.6 APPENDIX F - CYBER 180 DEVELOPMENT MILESTONES

	TARGET DATE
S1 SYSTEM	
-Release of S1 (CYBER 170 state) (First preproduction S1 shipment)	12/19/80
-First external user shipment of S1	03/15/81
-Release of S1 (CYBER 180 state)	03/31/82 (est.)
S2 SYSTEM	
-Release of S2 (CYBER 170 state) (First preproduction S2 shipment)	01/15/80
-Release of S2 (CYBER 180 state)	12/01/81
S3 SYSTEM	
-Release of S3 (CYBER 170 state) (First preproduction S3 shipment)	11/01/80
-Release of S3 (CYBER 180 state)	03/31/82
THETA SYSTEM	
-Release of THETA (CYBER 170 state) (First preproduction THETA shipment)	TBF
-Release of THETA (CYBER 180 state)	TBF
CYBER 180 SOFTWARE	
-Operating System & Product Set Released	
.Phase 1 (OS, FTN, COBOL, SORT)	12/01/81
.Phase 2 (Additional Features/Products)	04/01/83
.Phase 3 (All AO/R requirements)	12/01/84

These development milestones were approved by the CYBER 180 Baseline Change Control Board on December 16, 1977. It is the objective of the CYBER 180 program to meet these schedules. Check the Program Plan, Section 3, and Appendixes A and B for the most current schedule.

12.7 (#) APPENDIX G - MIGRATION ACTION PLAN

12.7.1 MIGRATION ALTERNATIVES

This section describes a few of the reasonable alternatives for migration and some of their advantages and limitations. Each alternative is considered as though it were the only one selected. The next section sets forth the recommended migration path for CDC and its customers.

12.7.1.1 Migrate via Training

A process of training customers/users in the appropriate actions required to ease the conversion process. Examples include defining: file formats most easily converted, source language features that will not convert, peripheral devices that will or will not be supported in CYBER 180 mode, physical environment requirements of CYBER 180 hardware and administrative and operational procedure rules for CYBER 180. The expectation is that the customer/user will convert to the most CYBER 180 like state possible on CYBER 170 prior to CYBER 180 installation. The conversion to CYBER 180 products then procedes via user conversion. CDC internal groups and external application vendors will be trained in the CYBER 180 mode of processing prior to announcement time.

Advantages	Limitations
1) Least direct cost to CDC.	1) Lowest appearance of user support
2) Must be done at some level for any alternative.	

12.7.1.2 Common Products and/or Interfaces (APP.G)

In this alternative maximum emphasis is placed on the development of common products between CYBER 170 and CYBER 180. This is referred to as "banding". A product may be either a software product (both product set and applications) or a hardware product. Wherever common products are not practical then a common product interface is enforced between the separate implementations. Again the expectation is that customer/users will begin to bend towards CYBER 180 like products on CYBER 170. This can be encouraged by: pricing actions, feature enhancement,

etc.

Advantages	Limitations
1) Presents the simplest path for user conversion.	1) Maximum impact on current CYBER 170 Product development.
	2) Users may not follow the bending.
	3) CYBER 180 products may not perform at maximum efficiency due to CYBER 170 orientation.

12.7.1.3 Conversion Tools and Services

A comprehensive set of tools and services are provided by CDC to assist users in their conversion efforts.

Advantages	Limitations
1) Indicates support by CDC for the user conversion problems.	1) Such tools are very difficult to produce when both ends of the conversion process are changing.
2) For simple cases of conversion such tools are very effective.	2) Development of conversion tools is expensive. Unless carefully selected, they are only of short term value.
	3) General purpose conversion tools are often more difficult to use than simply writing a specific conversion program.
	4) It is very difficult to determine which situations warrant conversion and in what order tools should be produced.

12.7.1.4 Dual State Processing (APP.G)

A single CYBER 180 system can execute both CYBER 170 and CYBER 180 jobs. CYBER 180 dual state operation is provided by hardware partition control and communication control between CY180 and CY170 environments. Dual state processing will be based upon extensions to Symmetric Link capabilities being developed for NOS and NOS/BE. The capabilities will allow interconnection of NOS and NOS/BE software operating in CY170 mainframes or in CY170 state of CY180 with NOS/180 software. Both job control and program level control is provided in both batch and interactive modes. This provides permanent file and record level transmission between states, submission of jobs between states and linkage to both CDC provided and user developed conversion and reformatting routines. This capability will be used to provide for record conversion and reformatting to assist in migration from CY170 state to CY180 state. Note that dual state does not eliminate the conversion problem it only extends the time period within which conversion can take place. If dual state support is provided indefinitely some conversions will never take place.

Advantages	Limitations
1) Allows customer/user choice as to when conversion of a particular job, program or file will take place.	1) Performance degradation relative to pure CYBER 170 or CYBER 180 state.
2) An industry accepted migration path.	2) Increased hardware costs.
	3) Requires CDC maintenance support for CYBER 170 products for an extended time period.

12.7.2 MIGRATION ACTION PLAN (APP.G)

The recommended solution for CDC and customer migration to CYBER 180 is a combination of all of the previous mentioned alternatives with specific techniques for each aspect of system usage. Although all alternatives are equally important, emphasis will be placed on common products, conversion aids and dual state processing.

The timeframe for accomplishing the major elements of the Migration Action Plan is expected to be:

Migration Plan Approved - ADLC	4/3/78
Conversion Action Plan - Draft	4/28/78
Migration Plan as part of CY180 AO/R, Rev.C - submitted for Company approval	6/2/78
Migration Plan as part of CY170 AO/R - Submitted for Company approval	10/78
Training Plan - PLM Approved	TBD
Start Training Implementation Plan	TBD
Conversion Action Plan - Approved	10/78
Conversion Aids GDS - ADLC Approved	10/78
Migration developments (i.e., tools, aids, conversion programs) defined in NOS-NOS/BE R5 + DR's	TBD
Conversion Aids User Guide	2Q79

12.7.2.1 General

1) Training

- no single activity is more important than training. All people within CDC systems business, software vendors, and the customer base must be trained in CYBER 180 processing operations. Training can be done on both a formal (e.g., classes, PLATO documents) and informal (e.g., press releases, strategy documents) basis.

- Training will be regulated by Product Line Management and New Product Programs so as to assure correctness, continuity and consistency.

12.7.2.2 Customer/User Conversion (APP.G)

This section defines the specific actions to be taken for various aspects of customer/user conversion. The action descriptions are grouped into the four conversion areas defined previously under "Conversion" and are further divided into specific areas of concern within each group. A set of solution actions are defined, in priority order, for each area of concern (e.g., Source programs). The actions stated are limited to those previously described under "Migration Alternatives".

12.7.2.2.1 PROCESSING OPERATIONS (APP.G)

1) Source programs	- Common Source Language Standards - Common Products (Compiler Front Ends) - Conversion Aids for FORTRAN, COBOL, BASIC, APL, ALGOL & PL/I
2) Object programs/libraries	- Dual state execution
3) Source Libraries	- Common Products (development tools) - Conversion Aids
4) Job deck structure	- Training - Dual state execution
5) Job processing concepts	- Training - Dual state execution
6) User Command Language	- Training - Common Products - Dual state execution - Conversion Aids
7) Accounting/Billing	- Training
8) Operations	- Training
9) Product Maintenance Procedures	- Training
10) Run time services	- Training - Common interfaces - Common products
11) Applications	- Common products - Common interfaces

- Training (both CDC and vendor)
- Source Language and File Conversion Aids

12.7.2.2.2 INFORMATION STORAGE

1) Files
- Conversion Aids
- Dual state execution

2) File Management Services
- Common interfaces
- Training

3) Data Bases
- Common interfaces
- Conversion Aids
- Dual state execution
- Common Products

4) Devices/Media
- Common Products (subset of CYBER 170 supported products)
- Dual state execution

12.7.2.2.3 HARDWARE FACILITIES

1) Front-ends
- Common products
- Dual state execution

2) Terminals
- Common products
- Dual state execution

3) Non-CDC Hardware
- Training
- PSO Contract

12.7.2.2.4 HUMAN AND ADMINISTRATIVE PROCEDURES

1) Terminal Services
- Common products
- Common interfaces
- Dual state execution

2) Network Services
- Common interfaces
- Common products
- Dual state execution

3) Administration
- Training

4) User Control and Administration
- Common products
- Training

5) User Interfaces
- Training (where not covered in other areas)

12.7.2.2.5 CONVERSION ACTION PLAN (APP.G)

The near term requirement of the Conversion Action Plan is to produce General Design Specifications of the conversion aids for the products to be provided with NOS/180 R1. These GDS documents will be collected into one document to be used in support of training. Additionally, software publications for the CY170 product set (CPS R7) will include recommended usages, i.e., files, commands, etc. to reduce future conversion.

ACTIONS

Conversion Aids	Responsibility	GDS Required By
A) Source Language		
Release 1		
CY170 FORTRAN 5 to CY180 FORTRAN 5	R.Ragan	12/78
CY170 BASIC 4 to CY180 BASIC 4	J.Elliott	12/78
CY170 COBOL 6 to CY180 COBOL 6	W.Hubrick/ D.Nelson	12/78
SYMPL Conversion Aids	L.Magee/ R.Ragan	12/78
Release 2		
CY170 ALGOL to CY180 ALGOL	R.Ragan/ J.Schlichting	12/79
CY170 APL to CY180 APL	B.Pommers	12/79
Release 3		
CY170 PL/I to CY180 PL/I	R.McAllester	12/80
B) Files		
Release 1		
User Data Files - CRM/BAM AAM		
C170 BAM to/from C180 BAM -Sequential Sequential -Word Add. Byte Add.	T.McGee	6/79
C170 AAM to/from C180 AAM -Index Seq. Index Seq. -Multi Index Multi Index -Direct Access/Actual Key to	W.Ceaglio	6/79
Index Sequential	R.Ragan	6/79
RANMS - FORTRAN	W.Hubrick/	6/79
Relative - COBOL	D.Nelson	
C) Data Management		
COCS (relations) to DMS180 (sets)	S.Radcliffe	12/79
DMS170 Data Base to DMS 180 Data Base	S.Radcliff	12/79
Query Update	J.delaBeaujardiere	12/79

D) Utility Programs		
Control Card/CCL Conv.Aids	G.Nelson	12/78
Update Conv.Aids	B.Pommers	6/79
Editor File Conv.Aids	D.Elefson	6/79
Permanent File Dump Conv.Aid	S.Fewer	12/78
E) CY180 Inherent Conversion		
Dual State - Linked File Conversion	S.Fewer/G.Matkovits	12/78
Dual State - ASCII to/from Display Code	S.Fewer/G.Matkovits	12/78

12.7.2.3 Software Products

This section is now included in Section 3.6 - Migration of the CY180 AO/R, Rev.C.

12.7.2.4 Software Product Phasing

This section is now included in Section 6.0 - Product Phasing Objectives or the CY180 AO/R Rev. C.

12.7.3 MIGRATION ACTION LIST

These product descriptions are grouped according to the migration alternatives that they represent and define responsibilities in support of the Migration Plan.

12.7.3.1 Training (APP.G)

1) A long term development strategy that can be presented to all CDC system business employees external software vendors and to all customers. The migration activities set forth in this plan should be included.

   Responsibility: New Product Programs

2) A training plan for internal CDC and external vendor use. It will be oriented to three levels of people, first, middle and top management and will include technical, marketing, and business perspectives.

   Responsibility: Product Line Management

3) For each area where training is specifically called out a training guide will be produced. The guide will contain two major types of information: 1) variances between CYBER 170 and CYBER 180, and 2) lists of both CYBER 170 and CYBER 180 reference manuals that describe the affected area.

Responsibility: Product development groups

12.7.3.2 Common Products (CYBER 170 and CYBER 180)

1) Compiler front-ends for FORTRAN, COBOL, SYMPL, ALGOL and BASIC (if compiler is used).

Responsibility: Sunnyvale System Design

2) Source code maintenance utilities (i.e., Update).

Responsibility: SES Development

3) User Command Language processor. This product will not replace the NOS/BE or NOS products but will augment them so as to allow gradual user conversion on CYBER 170.

Responsibility: CYBER 180 System Design

4) All application products. Operating System requirements to ease migration of applications.

Responsibility: APL0 and Application Resource Center

5) Configuration Control. Peripheral Devices and Media will be able to be attached to both CYBER 170 and CYBER 180 mainframes. Firmware will be common where practical. Communication front-ends will be able to be attached to both CYBER 170 and CYBER 180 simultaneously. Terminals can select connection.

Responsibility: Architectual Design & Control

6) Terminal services products such as editors, formatters, and information aids.

Responsibility: CYBER 180 System Design

7) Network products.

Responsibility: CYBER 180 System Design and Sunnyvale System Design

12.7.3.3 Common Interfaces (APP.G)

1) Source languages shall have common external specifications for CYBER 170 and CYBER 180 covering the majority of the language definition. System or machine dependent features will be minimized.

Responsibility: Sunnyvale System Design

2) Run time services (i.e., Loader, Math Science Library) will be equivalent in capability and will have common interfaces where practical.

Responsibility: CYBER 180 System Design
Sunnyvale System Design

3) Application codes that cannot be implemented as common products will present a common user interface.

Responsibility: CYBER 180 System Design and Application Software Development

4) File management services will be functionally upwards compatible from NOS.

Responsibility: CYBER 180 System Design

5) Data base management services.

Responsibility: Sunnyvale System Design

6) Terminal services.

Responsibility: CYBER 180 System Design

7) Network services.

Responsibility: CYBER 180 System Design

12.7.3.4 Conversion Tools and Services (APP.G)

1) FORTRAN, COBOL, ALGOL, BASIC, PL/I and APL source language translators, as required.

Responsibility: Sunnyvale System Design

2) Data file translators for files that contain well defined record structures. In particular, all character, all

integer or all real data or a mixture of those types in a fixed format within each and every record. These translators may operate as standalone utilities or as on-the-fly translation routines.

Responsibility: Sunnyvale System Design
CYBER 180 System Design

3) Conversion subroutines that users may include in their programs to convert more complex file situations.

Responsibility: Sunnyvale System Design

4) Data base translators for both schema definitions and data contents.

Responsibility: Sunnyvale System Design

12.7.3.5 Dual State Processing

1) At a minimum a means to concurrently execute CYBER 170 NOS and NOS/BE jobs and CYBER 180 jobs.

Responsibility: CYBER 180 System Design

2) Communication and network oriented users may submit jobs to either system although the communication hardware may only be connected to one operating system.

Responsibility: CYBER 180 System Design

12.8 APPENDIX H - STANDARDS

CYBER 180 systems will comply with the standards indicated in the attached master CDC Standards Checklist. Standards definitely not applicable are marked "NA". Those left unmarked in the categories of Codes, Data Representation, Data Communication, Keyboards, Character Recognition and various Media are relative to Network Products and peripheral devices and are applicable to the appropriate implementing divisions.

Product Design Requirements (DR) will include a CDC Standards Checklist calling out those standards applicable to that particular product, in compliance with this master checklist.

TITLE	Available Standards	Applicable Standards See 2.2	Option Chosen See 2.3	Waiver See 2.4	Verify/ Certify See 2.5
Category - CODES					
Code for Information Interchange Code for Information Interchange 7-Bit Coded Character Set for Information Processing Interchange	ANSI X3.4 FIPS PUB 1 ISO 646	X3.4 PUB 1			
Implementation of the Code for Information Interchange and Related Media Standards	FIPS PUB 7	PUB 7			
Code Extension Techniques for Use With The 7-Bit Coded Character Set of ASCII Code Extension Techniques In 7 or 8 Bits Code Extension Techniques for Use With The 7-Bit Coded Character Set	ANSI X3.41 FIPS PUB 35 ISO 2022	X3.41 PUB 35			
Control Data Subset of ASCII *Subsets of the Standard Code for Information Interchange	1.10.003 FIPS PUB 15	1.10.003			
Perforated Tape Code for Information Interchange Perforated Tape Code for Information Interchange Representation of 6 and 7-Bit Coded Character Sets on Punched Tape	ANSI X3.6 FIPS PUB 2 ISO 1113	NA NA NA			
Hollerith Punched Card Code Hollerith Punched Card Code Representation of the 7-Bit Coded Character Set on 12-Row Punched Cards Representation of 8-Bit Patterns on 12-Row Punched Cards	ANSI X3.26 FIPS PUB 14 ISO 1679 ISO/R 2021	X3.26 PUB 14			
Representation of Numbers in Packed Decimal Form	1.10.016	1.10.016			
Representation of Numeric Values in Character Strings for Information Interchange	ANSI X3.42	X3.42			
Category - PAPER CARD MEDIA		NA			
General Purpose Paper Cards and Punched Hole Requirements 80-Column Card Files for Information Interchange	1.10.008 1.10.009				

*The standard has selectable options

TITLE	Available Standards	Applicable Standards See 2.2	Option Chosen See 2.3	Waiver See 2.4	Verify/ Certify See 2.5
Category - PAPER TAPE MEDIA		NA			
Eleven-Sixteenth Inch Perforated Paper Tape for Interchange One-Inch Perforated Paper Tape for Information Interchange One-Inch Perforated Paper Tape for Information Interchange Dimensions of Punched Paper Tape for Information Interchange	ANSI X3.19 ANSI X3.18 FIPS PUB 26 ISO 1154				
Take-Up Reels for One-Inch Perforated Paper Tape for Information Interchange Take-Up Reels for One-Inch Perforated Paper Tape for Information Interchange	ANSI X3.20 FIPS PUB 27				
Specifications for Properties of Unpunched Oiled Paper Perforator Tape Properties of Unpunched Paper Tape	ANSI X3.29 ISO 1729				
Interchange Rolls of Perforated Paper Tape for Information Interchange Data Interchange on Rolled Up Paper Tape	ANSI X3.34 ISO 2195				
Category - MAGNETIC CASSETTE/CARTRIDGE MEDIA		NA			
Implementation of the 7-Bit Coded Character Set and its 7-Bit and 8-Bit Extensions on 3.81 mm Magnetic Tape Cassettes for Information Interchange 3.81 mm Magnetic Tape Cassette for Information Interchange	ISO 3275 ISO 3407				
Category - MAGNETIC TAPE MEDIA		NA			
Recorded Magnetic Tape, 0.50 Inch, 9-track, 800 CPI, NRZI Recorded Magnetic Tape, 0.50 Inch, 9-Track, 1600 CPI, Phase Encoded Unrecorded Magnetic Tape, 0.50 Inch Recorded Magnetic Tape, 0.50 Inch, 7-Track, 200 CPI, NRZI	1.10.005 1.10.006 1.10.007 1.10.013				

CDC STANDARDS CHECKLIST (REV. E)

TITLE	Available Standards	Applicable Standards See 2.2	Option Chosen See 2.3	Waiver See 2.4	Verify/ Certify See 2.5
Category - ROTATING MAGNETIC MEDIA		NA			
Unrecorded Magnetic Six-Disk Pack (General, Physical and Magnetic Characteristics)	ANSI X3.46				
Unrecorded Single-Disk Cartridge (Front-Loading, 2200 BPI)	ANSI X3.52				
Interchangeable Magnetic Six-Disk Pack - Physical and Magnetic Characteristics	ISO 2864				
Interchangeable Magnetic Six-Disk Pack - Track Format	ISO 3561				
Interchangeable Magnetic Single-Disk Cartridge	ISO 3562				
Interchangeable Magnetic Eleven-Disk Pack	ISO 3564				
Category - CHARACTER RECOGNITION		NA			
Print Specifications for Magnetic Ink Character Recognition	ANSI X3.2				
Print Specifications for Magnetic Ink Character Recognition	ISO/R 1073				
Bank Check Specifications for Magnetic Ink Character Recognition	ANSI X3.3				
Coding of Character Sets for MICR and OCR	ISO 2033				
Character Set and Print Quality for Optical Character Recognition (OCR-A)	ANSI X3.17				
Character Set for Optical Character Recognition (OCR-B)	ANSI X3.49				
*Optical Character Recognition Character Sets	FIPS PUB 32				
*Alphanumeric Character Sets for Optical Recognition	ISO/R 1073				
Printing Specifications for Optical Character Recognition	ISO/R 1831				
Character Set for Handprinting	ANSI X3.45				
Character Set for Handprinting	FIPS PUB 33				
Specifications for Credit Cards	ANSI X4.13				
Optical Reader Subsystem Testing	1.88.001				

*The standard has selectable options

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TITLE	Available Standards	Applicable Standards See 2.2	Option Chosen See 2.3	Waiver See 2.4	Verify/ Certify See 2.5
Category - DATA COMMUNICATION					
Mode 4C Data Communication Control Procedures	1.10.020	1.10.020			
Synchronous Signalling Rates	ANSI X3.1	X3.1			
Synchronous High Speed Signalling Rates	ANSI X3.36	X3.36			
Synchronous Signalling Rates Between Data Terminal and Data Communication Equipment	FIPS PUB 22	PUB 22			
Bit Sequencing of ASCII in Serial-by-Bit Data Transmission	ANSI X3.15	X3.15			
Bit Sequencing of the Code for Information Interchange In Serial-by-Bit Data Transmission	FIPS PUB 16	PUB 16			
Character Structure and Character Parity Sense for Serial-by-Bit Data Communication In ASCII	ANSI X3.16	X3.16			
Character Structure and Character Parity Sense for Serial-by-Bit Data Communication in the Code for Information Interchange	FIPS PUB 17	PUB 17			
Character Structure for Start/Stop and Synchronous Transmission	ISO 1177	ISO 1177			
Character Structure and Character Parity Sense for Parallel-by-Bit Data Communication In ASCII	ANSI X3.25	NA			
Character Structure and Character Parity Sense for Parallel-by-Bit Data Communication in the Code for Information Interchange	FIPS PUB 18	NA			
Signal Quality at the Interface Between Data Processing Terminal Equipment and Synchronous Data Communication Equipment for Serial Data Transmission	ANSI X3.24	X3.24			
Procedures for Using the Control Characters of ASCII In Specified Data Communication Links	ANSI X3.28	X3.28			
Basic Mode Control Procedures for Data Communication Systems	ISO 1745	ISO 1745			
Electrical Characteristics of Balanced Voltage Digital Interface Circuits	EIA RS-422	RS-422			
Electrical Characteristics of Unbalanced Voltage Digital Interface Circuits	EIA RS-423	RS-423			
Interface Between DTE and DCE Employing Serial Binary Interchange	EIA RS-232	RS-232			
List of Definitions for Interchange Circuits Between DTE and Data Circuit-Terminating Equipment	CCITT V.24	V.24			

CDC STANDARDS CHECKLIST (REV. E)

TITLE	Available Standards	Applicable Standards See 2.2	Option Chosen See 2.3	Waiver See 2.4	Verify/ Certify See 2.5
Category - DATA COMMUNICATION (Continued)					
Data Terminal and Data Communication Interchange Circuits - Assignment of Connector Pin Numbers	ISO 2110	ISO 2110			
Connector Pin Allocations for Use With High-Speed Data Terminals	ISO 2593	ISO 2593			
Basic Mode Control Procedures - Code Independent Information Transfer	ISO 2111	NA			
Basic Mode Control Procedures - Complements	ISO 2628	NA			
Basic Mode Control Procedures - Conversational Information Message Transfer	ISO 2629	NA			
Use of Longitudinal Parity to Detect Errors in Information Messages	ISO 1155	NA			
Determination of the Performance of Data Communication Systems	ANSI X3.44	NA			
High-Level Data Link Control Procedures - Frame Structure	ISO 3309	ISO 3309			
Pending ADCCP Standard		when avail.			
Pending CCITT Standard	X.25	when avail.			
Category - KEYBOARDS		NA			
Ten-Key Keyboards for Numeric Data Entry	1.10.004				
Typewriter Keyboards	ANSI X4.7				
Alphanumeric Keyboard Arrangements for ASCII and OCR	ANSI X4.14				
Keyboard for International Information Processing Interchange	ISO 2530				
Keyboards for Countries Whose Languages Have Alphabetic Extenders - Guidelines for Harmonization	ISO 3243				
Function Key Symbols on Typewriters	ISO/R 1090				
Layout of Printing and Function Keys on Typewriters	ISO/R 1091				
Basic Arrangement for the Alphabetic Sections of Keyboards	ISO/R 2126				
Principles Governing the Positioning of Control Keys on Keyboards	ISO/R 3244				

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TITLE	Available Standards	Applicable Standards See 2.2	Option Chosen See 2.3	Waiver See 2.4	Verify/ Certify See 2.5
Category - DATA REPRESENTATION					
Representation of Calendar Date and Ordinal Date for Information Interchange	ANSI X3.30	X3.30			
Calendar Date	FIPS PUB 4				
Representation of Ordinal Dates	ISO 2711				
Guidelines for Describing Information Interchange Formats	FIPS PUB 20	NA			
Representation of SI and Other Units in Systems With Limited Character Sets	ISO 2955	NA			
Representations of Universal Time	ANSI X3.51				
Representations of Time of Day	ISO 3307	ISO 3307			
Rep. of Local Time of Day	ANSIX3.43	X3.43			
Category - PROGRAMMING LANGUAGES					
COBOL	ANSI X3.23	X3.23(74)			
COBOL	FIPS PUB 21				
Programming Language COBOL	ISO/R 1989				
FORTRAN	ANSI X3.9	X3.9(78)			
Basic FORTRAN	ANSI X3.10				
Programming Language FORTRAN	ISO/R 1539				
ALGOL-60	1.86.003	1.86.003			
Programming Language PL/I	ANSI X3.53	NA			
Category - SPECIAL PURPOSE LANGUAGES		NA			
APT	ANSI X3.37				
Industrial Computer System FORTRAN Procedures for Executive Functions and Process Input-Output	ISA S61.1				

CDC STANDARDS CHECKLIST (REV. E)

TITLE	Available Standards	Applicable Standards See 2.2	Option Chosen See 2.3	Waiver See 2.4	Verify/ Certify See 2.5
Category - OPERATING SYSTEMS					
Magnetic Tape Labels for Information Interchange	1.87.002	1.87.002			
Magnetic Tape Error Detection and Recovery	1.87.004	1.87.004			
System Error Recovery for Rotating Mass Storage	1.87.005	1.87.005			
Category - GENERAL DESIGN					
Component Selection	1.03.002	1.03.002			
Component Qualification	1.03.003	1.03.003			
Qualified Vendor List	1.03.005	1.03.005			
Electronic Logic Packaging	1.03.006	1.03.006			
Microcircuit Selection	1.03.010	1.03.010			
Reliability, Availability and Maintainability Standards	1.12.000	1.12.000			
Category - ELECTRICAL DESIGN					
General Design Standard for Electronic Power Supplies	1.30.001	1.30.001			
Color Coding of Wires, Harnesses and Cables	1.30.005	1.30.005			
Cable Classification and Marking	1.30.008	1.30.008			
Computer and Peripheral Equipment Design Requirements	1.30.011	1.30.011			
EMC Performance Requirements	1.30.022	1.30.022			
Digital Computer System Grounding	1.30.023	1.30.023			
Analog Computer System Grounding	1.30.024	-			
EMI Suppression and Certification	1.30.025	1.30.025			

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TITLE	Available Standards	Applicable Standards See 2.2	Option Chosen See 2.3	Waiver See 2.4	Verify/ Certify See 2.5
Category - MECHANICAL DESIGN					
Product Identification Emblems	1.20.006	1.20.006			
Operating and Maintenance Meters	1.20.009	1.20.008			
Industrial Design	1.20.010	1.20.010			
Category - DOCUMENTATION					
Hardware Configuration Management Standards Manual (Entire Contents Including 1.01.006)	1.01.000	1.01.000			
Software Configuration Management Standards Manual (Entire Contents Included)	1.01.100	1.01.100			
Preparation of Microcircuit Procurement and Acceptance Test Specifications	1.03.007	1.03.007			
Graphic Symbols for Electrical and Electronic Diagrams	1.41.101	1.41.101			
Reference Designations for Electrical and Electronic Parts and Equipment	1.41.102	1.41.102			
Graphic Symbols for Logic Diagrams	1.41.104	1.41.104			
Logic Diagrams	1.41.108	1.41.108			
Hardware and Software Product Support Manual Standards Manual (Entire Contents Included)	1.50.000	1.50.000			
Flowchart Symbols and Usage	1.80.003	-			

CDC STANDARDS CHECKLIST (REV. E)

TITLE	Available Standards	Applicable Standards See 2.2	Option Chosen See 2.3	Waiver See 2.4	Verify/ Certify See 2.5
Category - ENVIRONMENTAL					
*Application Guidelines	1.03.201	1.03.201	NA		
*Temperature, Humidity and Barometric Pressure	1.03.202	1.03.202	TH-R2 P-R1		
Vibration and Shock	1.03.203	1.03.203			
Acoustical Noise	1.03.204	1.03.204			
*Air Cleanliness	1.03.205	1.03.205	R3		
Illumination	1.03.206	1.03.206			
*Input Power and Grounding	1.03.207	1.03.207	FV-04 T-R1		
*Physical Characteristic	1.03.209	1.03.209	R3		
Category - PRODUCT SAFETY					
Use and Disposal of Capacitors Containing Polychlorinated Biphenyl	1.05.002	1.05.002			
Product Safety	1.05.003	1.05.003			

*The standard has selectable options

12.9 APPENDIX I - STATEMENTS OF COMPLIANCE

DESIGN OBJECTIVES/REQUIREMENTS APPROVAL

COMPANY-PRIVATE

MINNEAPOLIS MINNESOTA

COMPUTER DEVELOPMENT DIVISION

MAY 19 1977
Product Line Mgmnt.

[XXX / DR] # ARH1012

REV. # 08

DESIGN [XXXXXXXXX / REQUIREMENTS] FOR: CYBER 80 M2 CENTRAL MEMORY

(*Strike out term that does not apply)

SIGNATURES – DEVELOPING COMPANY		DATE
PREPARED BY	R.E. Moritz	5/5/77
	J.J. Turner	5/5/77
	M. Bergmanis	5/5/77
REVIEWED BY: PROJECT MANAGER	G.D. Floss	5/5/77
	D.L. Serreyn	5/6/77
DEPARTMENT MANAGER	R.C. Eppel	5/6/77
DIVISION ENDORSEMENT: GENERAL MANAGER	M.J. McHale	5/9/77
5/9/77		5/10/77
COMPANY ENDORSEMENT: COMPANY DELEGATE		7/25/77

RESPONSE TO REVIEW DISTRIBUTION

	RESPONSE
DATA SERVICES....................	approved/ no response
SYSTEMS AND SERVICES COMPANY	approved/ memo June 27/77
PERIPHERAL PRODUCTS COMPANY	approved/ no response
XXXXXXXXXXXXXX Corp.Bus.Strat.	approved/ no response
SERVICE BUREAU COMPANY	
PRODUCT AND SERVICES STRATEGY	

APPROVED: ______________ COMPANY DELEGATE   DATE 8/15/77

AA5441 12-74

CONTROL DATA CORPORATION
Computer Development DIVISION

DOCUMENT CLASS DESIGN REQUIREMENTS PAGE NO. 6
PRODUCT NAME CYBER 80 M2 MEMORY
PRODUCT MODEL NO. 33133-A MACHINE SERIES CYBER 80

0.0 STATEMENT OF COMPLIANCE

The M2 Design Requirements Document (CYBER 80 M2 Central Memory - ARH1012 Rev. 08) is in compliance with the objectives stated in the CYBER 80 Architectural Objectives/Requirements Document (ARH1638 Rev. 05) with the following exceptions.

	AO/R	DR
MTBI (Degraded)	PAR. 8.4.2	PAR. 3.2.2.7.1
CYBER /M2-4 at Release	1800 Hours	1335 Hours
80 MODE M2-4 6 Mo. Later	2038 Hours	1455 Hours-
\M2-4 18 Mo. Later	2484 Hours	1600 Hours
MTBI (Degraded)	PAR. 10.7.2	PAR. 3.2.2.7.1
CYBER /M2-1 at Release	Infin.	720 Hours
170 MODE M2-1 6 Mo. Later	Infin.	920 Hours
\M2-1 18 Mo. Later	Infin.	1200 Hours
MANUFACTURING COST	PAR. 11.1.2	PAR. 3.4.1.1
M2-4	$ 89,000	$ 91,416
M2-6	104,000	111,649
M2-8	115,000	125,559
M2-12	141,000	163,642
M2-16	166,000	202,021
MTBF Elemental (Inherent)	PAR. 11.2	PAR. 3.2.2.5.1
M2-1	1400 Hours	1220 Hours
M2-6	500 Hours	450 Hours
M2-8	400 Hours	365 Hours
M2-12	335 Hours	255 Hours
M2-16	270 Hours	200 Hours
MTBF Functional (Inherent)	PAR. 11.2	PAR. 3.2.2.6.2
M2-1	2800 Hours	2435 Hours
MTTR	PAR. 11.2	PAR. 3.2.2.6.4
At Release	30 Minutes	36 Minutes
6 Mo. Later	30 Minutes	36 Minutes
18 Mo. Later	20 Minutes	30 Minutes
36 Mo. Later	15 Minutes	24 Minutes

for EHMuchile ADEC 7/10/77

DESIGN OBJECTIVES/REQUIREMENTS APPROVAL

F.V.

COMPANY PRIVATE

Canadian Development DIVISION

RECEIVED MAY 19 1977 Product Line Mgmnt.

[~~OBJ~~ DR] # ARH1127

REV. # H

DESIGN [~~OBJECTIVES~~ REQUIREMENTS] FOR: CYBER 80 P2 PROCESSOR

(*Strike out term that does not apply)

SIGNATURES – DEVELOPING COMPANY		DATE
PREPARED BY:	R.J. Potter, TTOFAC, Ext 301	02May77
REVIEWED BY: PROJECT MANAGER	R.J. Potter	02May77
DIVISION ENDORSEMENT: GENERAL MANAGER		
COMPANY ENDORSEMENT: COMPANY DELEGATE	Robert E. Washburn	

** See next page for Division approvals **

RESPONSE TO REVIEW DISTRIBUTION

	RESPONSE
DATA SERVICES.....	~~approved/ no response~~
SYSTEMS AND SERVICES COMPANY	approved memo 6/27/77
PERIPHERAL PRODUCTS COMPANY	approved/ no response
~~XXXXXXXXXXXXXXX~~ Corp.Bus.Strat.	approved/ no response
SERVICE BUREAU COMPANY	
PRODUCT AND SERVICES STRATEGY	

APPROVED: Robert E. Washburn
COMPANY DELEGATE

DATE 8/15/77

COMPANY PRIVATE

1.2 STATEMENT OF COMPLIANCE

This DR defines the P2 processor of the CDC Cyber 80 Product Line, and as such, conforms with the CDC Cyber 80 System Baseline Definition, with the following exceptions:

Item	This DR Reference	A.O/R Reference
Scientific Performance CY170 Mode	3.2.1.5 2.8	10.4 2.9
Mfg Cost	3.4.1.1 $90246	11.1.1 $72000
MTBF Elemental	3.2.2.1 1760	11.2 1800
MTBI System Down, CY170 Mode At release 6 months 18 months	3.2.2.3.2 440 557 728	10.7.1 450 569 744

Jack Wilson for E.J. Michel AD&C 6/10/77

DESIGN OBJECTIVES/REQUIREMENTS APPROVAL

COMPANY PRIVATE

RECEIVED
JUN 2 [82 / 08] # ARH1767

COMPUTER DEVELOPMENT DIVISION

Product Line REVIEW _____

DESIGN* [XXXXXXXXX / REQUIREMENTS] FOR: CDC CYBER 80 P3 PROCESSOR AND M3 MEMORY

(*Strike out term that does not apply)

SIGNATURES – DEVELOPING COMPANY		DATE
PREPARED BY:	FOR CDED DIVISIONAL APPROVALS	
REVIEWED BY: PROJECT MANAGER	SEE NEXT PAGE.	
NRP 170/80 PROG. MGR.	T E Edwards/DPJ	6/1/77
COMPANY APPROVAL: VICE PRESIDENT (company delegate)	R.E. Willard/DPJ	5/31/77
	R E Willard	

RESPONSE TO REVIEW DISTRIBUTION

	RESPONSE
DATA SERVICES.....	approved; no response
SYSTEMS AND SERVICES COMPANY	approved; memo 7/25/77
PERIPHERAL PRODUCTS COMPANY	approved; no response
XXXXXXXXXXXXXXX Corp.Bus.Strat	approved; no response
PRODUCT AND SERVICES STRATEGY	
CORPORATE ENGINEERING AND SOFTWARE	
CORPORATE MANUFACTURING, MTL., AND QA	

APPROVED: R E Willard Corp C
VICE PRESIDENT
(company delegate)

DATE 8-30-77

AAD441 7/73

CONTROL DATA CORPORATION
Computer Development DIVISION

DOCUMENT CLASS Design Requirements PAGE NO. v
PRODUCT NAME CDC CYBER 80 P3 Processor & M3 Memory
DOCUMENT NO. ARH1767, Revision A DATE June 1, 1977

0.0 P3/M3 DR CONFORMANCE TO ARCHITECTURAL OBJECTIVES

The CDC CYBER 80 P3 Processor and M3 Memory conform with the CDC CYBER 80 System Baseline Definition (Architectural Objectives/Requirements Rev. 05) with the following exceptions:

0.1 PERFORMANCE

Both BDP and SWL objectives will be met or exceeded. FORTRAN performance in both CYBER 80 and CYBER 170 mode will be slightly below objectives.

	AO	DR	% Difference
Scientific CYBER 80 Mode	10.3	9.9	-4%
Scientific CYBER 170 Mode	8.0	7.7	-4%
BDP	19.3	19.3	0
SWL	8.4	9.0	+7%

References: AO Section 7.2.1 and 10.4
DR Section 3.2.1

0.2 CENTRAL MEMORY CAPACITY & BANDWIDTH

The following S3 dual-CPU configuration requirements will not be supported. Waiver for these requirements has been granted via PAP No. CDED 019. Revision 06 of the AO document will incorporate this change.

	AO	DR
Maximum Capacity, MBytes	32	16
Total Bandwidth MBytes/Sec.	256	128

References: AO Section 7.2.2
DR Sections 3.1.3 and 3.2.1.7

0.3 MANUFACTURING COSTS

The 10th unit P3/M3 manufacturing costs will be approximately 15% higher than AO objectives. The following comparison is in $1000's and includes 16K byte cache, all ports, and system clock/fanout.

Configuration Description	DR Requirement				Architectural Objectives		
	P3/ CMC Cab.	M3 CSU Cab.	Remote Cndns. Unit	TOTAL	P3	M3	TOTAL
P3 and 1M byte M3 (M3-1)	243	50	10	303	184	N/A	N/A
P3 and 2M byte M3 (M3-2)	243	57	10	310	184	85	269
P3 and 4M byte M3 (M3-4)	243	71	10	324	184	98	282
P3 and 6M byte M3 (M3-6)	243	91	10	344	184	115	299
P3 and 8M byte M3 (M3-8)	243	105	10	358	184	125	309
P3 and 12M byte M3 (M3-12)	243	139	10	392	184	155	339
P3 and 16M byte M3 (M3-16)	243	172	10	425	184	180	364

References: AO Section 11.1
DR Section 3.4.1

0.4 RELIABILITY

The P3/M3 reliability will fall short of AO objectives for certain configurations.

0.4.1 Inherent Elemental MTBF - CYBER 80 Mode

The following comparison is made of AO objectives and DR requirements. The P3/M3 includes 16K byte cache, all ports, and system clock/fanout. All calculations are in hours.

The calculations are separated on cabinet (equipment boundaries) to allow for later comparison with field data. The Processor is therefore combined with the CMC since both are located in the same cabinet. The P3 Processor (without CMC) inherent elemental MTBF is 1,695 hrs for CYBER 80 Mode.

Configuration Description	DR Requirements			AO Objectives		
	P3 & CMC	CSU	Total	P3	M3	Total
P3 & M3-2	1,405	1,210	650	1,800	900	600
P3 & M3-4	1,405	735	483	1,800	600	450
P3 & M3-6	1,405	520	360	1,800	500	391
P3 & M3-8	1,405	400	311	1,800	400	327
P3 & M3-12	1,405	275	230	1,800	335	282
P3 & M3-16	1,405	210	183	1,800	270	235

References: AO Section 11.1
DR Section 3.2.2.6.1

0.4.2 Inherent Functional MTBF - CYBER 80 Mode

The following comparison is made of AO objectives and DR requirements. The P3/M3 includes 16K byte cache, all ports, and system clock/fanout. All calculations are in hours.

The calculations are separated on functional unit boundaries. The P3 processor is separate from the M3 CMC/CSU. The remote condensing unit is included with P3.

Configuration Description	DR Requirements			Architectural Objectives		
	P3	CMC & CSU	Total	P3	M3	Total
P3 & M3-2	1,770	2,350	993	2,570	2,300	1,213
P3 & M3-4	1,770	2,310	977	2,570	1,700	1,023
P3 & M3-6	1,770	1,960	901	2,570	1,350	885
P3 & M3-8	1,770	1,935	889	2,570	1,100	770
P3 & M3-12	1,770	1,665	820	2,570	800	610
P3 & M3-16	1,770	1,460	763	2,570	700	550

References: AO Section 11.2
DR Section 3.2.2.6.2

0.4.3 MTBI

The complete MTBI calculations and their comparison against AO/AR objectives will be provided by 12/31/77.

0.5 Mean Time to Repair.

The mean time to repair (MTTR) objectives for P3 will be met. For M3 the MTTR will be longer than AO objectives due to the strategy of array replacement at the component level precipitated by the assumption that sockets will be used. All calculations are in minutes.

	DR Requirements	AO Objectives
M3 MTTR at Release	36	30
6 mo after release	36	30
18 mo after release	30	20
36 mo after release	24	15

Reference AO Section 11.2
DP Section 3.2.2.6.4

MINNEAPOLIS MINNESOTA

DESIGN OBJECTIVES/REQUIREMENTS APPROVAL

COMPANY PRIVATE

Computer Development DIVISION

~~OBJECTIVES~~ DR # ARH1881

REV. # _____

DESIGN ~~OBJECTIVES~~ REQUIREMENTS FOR: CDC CYBER 80 MODEL INDEPENDENT MEMORY TEST

(*Strike out term that does not apply)

SIGNATURES – DEVELOPING COMPANY		DATE
PREPARED BY:	G. J. Hagfors	8-4-77
REVIEWED BY PROJECT MANAGER	J.U. Sundet E.H. Michehl	
	R.J. Brush R.L. Young	8/4/77
DIVISION ENDORSEMENT: GENERAL MANAGER	R.D. Kazda M.J. McHale	8/4/77
	D.B. Robinson D.L. Slais	9/30/77
COMPANY ENDORSEMENT: COMPANY DELEGATE	R.L. Uesslund	10/6/77

RESPONSE TO REVIEW DISTRIBUTION

	RESPONSE
DATA SERVICES..... SYSTEMS AND SERVICES COMPANY	approved; memo 10/24/77 approved; memo 10/30/77
PERIPHERAL PRODUCTS COMPANY	approved; memo 10/24/77
~~XXXXXXXXXXXXXX~~ Corp.Bus.Strat.	approved
SERVICE BUREAU COMPANY	
PRODUCT AND SERVICES STRATEGY	

RECEIVED

E. H. MICHEHL

APPROVED R.E. Uesslund

COMPANY DELEGATE

DATE 11-15-77

AA (11-74)

CONTROL DATA CORPORATION
Computer Development DIVISION

DOCUMENT CLASS Design Requirement PAGE NO. 1
PRODUCT NAME (MIL) Memory Maintenance Software
PRODUCT MODEL NO. DR SR 1 84 MACHINE SERIES CYBER 81

0.0 STATEMENT of COMPLIANCE

This DR document complies with all CYBER 80 Maintenance Software objectives set down within the AO and M/S DO except those listed in the following sections. Also, any waivers or deviations from the standards checked on the standards checklist.

0.1 AO ARH1588, EXCEPTIONS

None

0.2 M/S DO ARH934, EXCEPTIONS

The detection requirements of the PP test of CM do not meet the M/S DO objective due to the nature of the hardware architecture. Access time and speed of execution from the I/O Unit are the primary reasons.

	Detection Effectiveness	
CMP (central memory test from PP)	A22	HIP3
Quick Look Mode	80%	75%
Default Parameters	80%	85%

0.3 STANDARDS, EXCEPTIONS

0.3.1 CDC STANDARDS

CDC Std. 1.52.007 Section 5.3, Subroutine descriptions will be in the listings.

CDC Std. 1.52.007 Section 7.0, no flowcharts will be provided, but HIPO diagrams will be part of the IMS package.

CDC Std. 1.12.003 Section 4.5.1, there are no MTTR/MS figures included for tests. Isolation diagnostics will be used for actual hardware repair and these tests are only detection vehicles to assist that isolation process. However, the tests and diagnostics will support the Central Memory model DRs MTTR requirements.

0.3.2 NATIONAL, INTERNATIONAL, and INDUSTRY STANDARDS

None

DESIGN OBJECTIVES/REQUIREMENTS APPROVAL

COMPANY PRIVATE

Canadian Development DIVISION

[~~DO~~ / DR] # ARH2092

REV. # 2

DESIGN* [~~OBJECTIVES~~ / REQUIREMENTS] FOR: Fixed Instruction Command Tests (FCT)

(*Strike out term that does not apply)

SIGNATURES – DEVELOPING COMPANY	DATE
PREPARED BY. [redacted]	3 Oct 77
REVIEWED BY: PROJECT MANAGER K.J. Dykstra, W.B. Robinson	
M.U. McHale, R.L. Young	
DIVISION ENDORSEMENT: GENERAL MANAGER R.D. Kazda, E.H. Michenl	
D. L. Slais	10/24/77
COMPANY ENDORSEMENT: COMPANY DELEGATE R. E. Wesslund	1-13-78

RESPONSE TO REVIEW DISTRIBUTION

	RESPONSE
DATA SERVICES.........	Approved
SYSTEMS AND SERVICES COMPANY	Approved: memo 11/30/77
~~XXXXXXXXXXXXXXXXXXXXXX~~	
PERIPHERAL PRODUCTS COMPANY	Approved
~~XXXXXXXXXXXXX~~ Corp. Bus. Strat.	Approved
SERVICE BUREAU COMPANY	
PRODUCT AND SERVICES STRATEGY	

APPROVED: ______________ COMPANY DELEGATE

DATE ______________

AA5441 12/74

1.0 STATEMENT_OF_COMPLIANCE

This DR document complies with all CYBER 80 Maintenance Software objectives set down within the AD and the M/S DO, and complies with all applicable standards, except those specifically listed in the following sections, or so marked in the standards checklist.

1.1 AD_(ARH1688)_EXCEPTIONS

None.

1.2 M/S_DO_(ARH____)_EXCEPTIONS

None.

1.3 CONTROL_DATA_STANDARDS_EXCEPTIONS

CDC Standard 1.12.033 Section 4.5.1, there are no MTTF/MTTR figures included for the tests. Tests are seldom used for actual hardware repair and are only detection vehicles to assist repair.

The Diagnostic Reference Manual Standard 1.52.007 will be complied with, with the following exceptions:

(1) Subroutine descriptions will be omitted in the published documentation, but will be included in the source code.

(2) Flowcharts will not be provided in the published documentation except where a particular programming sequence cannot be satisfactorily explained without flowcharts.

(3) Message codes will not be provided for FCT2, FCT3, and FCT4, since the messages they will generate will be fully self explanatory, and since the source of each message will be indicated via the section, condition, etc. numbers. Message codes will be documented wherever they are used in FCT1 and FCT5.

CONTROL DATA CORPORATION
MINNEAPOLIS, MINNESOTA

DESIGN OBJECTIVES/REQUIREMENTS APPROVAL

COMPANY PRIVATE

COMPUTER DEVELOPMENT DIVISION

[~~de~~ DR] # ARH2110

REV. # 2

DESIGN [~~OBJECTIVES~~ REQUIREMENTS] FOR: COMMON MAINTENANCE SOFTWARE EXECUTIVE (CMSE)

(*Strike out term that does not apply)

SIGNATURES – DEVELOPING COMPANY	DATE
PREPARED BY: U. F. SATCHELL	
REVIEWED BY: PROJECT MANAGER: R. J. BRUSH M. J. MCHALE	9/13/77
J. D. ROBINSON R. L. YOUNG	11/1/77
DIVISION ENDORSEMENT: GENERAL MANAGER: R. D. KAZDA E. H. MICHEHL	10/26/77
D. L. SLAIS H. N. FRAZIER	10/27/77
COMPANY ENDORSEMENT: COMPANY DELEGATE: R. E. Wesslund	11/7/77

RESPONSE TO REVIEW DISTRIBUTION

	RESPONSE
DATA SERVICES.....	~~Approved, memo 2/8/78~~
SYSTEMS AND SERVICES COMPANY	Approved, memo 11/30/77
PERIPHERAL PRODUCTS COMPANY	Approved, non-response
XXXXXXXXXXXXXXXCorp.Bus.Strat.	Approved, non-response
SERVICE BUREAU COMPANY	
PRODUCT AND SERVICES STRATEGY	

APPROVED: _____ _____
COMPANY DELEGATE DATE

AA5441 12/74

0.0 STATEMENT OF COMPLIANCE

This DR document complies with all CYBER 80 Maintenance Software objectives set down within the CYBER 80 Architectural Objectives (AO) and MS/20 except those listed in the following sections. Also any 'waivers' or deviations from the standards checked on the standards checklist.

0.1 AO ARH 1648 - Exceptions

- Sec. 3.2.4.4 A CC545 display is planned for the initial phase of the project. It will be supported by CMSE until there is no longer a requirement for the faster display.
- 3.2.2 Item 2 CMSE cannot be provide 100% customer security and still provide maintenance. It must be the responsibility of CMSE, the tests, diagnostics and the utilities to stay within the disk address boundaries specified by the Operator/CE. The Operator/CE will have the responsibility of providing the correct disk address boundaries.
- Sec. 3.2.6.2 - System Initialization - The Common Maintenance Software Executive will reside on the same media as the firmware/controlware and is planned as being the same as the operating system media.
- Sec. 3.2.8 - 6th item - A dedicated input/output device for maintenance usage does not appear to be feasible.

0.2 Maintenance Software 72 ARH 2144 Exceptions

- Sec. 3.1.2 - #2 - For CYBER 170 only the executive will not retrieve on-line error reports. The CYBER 72 executive will retrieve the error reports if the operating system has loaded them on a disk area that is known and accessible to CMSE.

0.3 Standards Exceptions

0.3.1 CDC Standards

None.

0.3.2 National, International, and Industry Standards

None.

CONTROL DATA

DESIGN OBJECTIVES/REQUIREMENTS APPROVAL

COMPANY PRIVATE

COMPUTER DEVELOPMENT DIVISION

[~~DO~~ / DR] # ARH2110

REV. # 2

DESIGN [~~OBJECTIVES~~ / REQUIREMENTS] FOR: COMMON MAINTENANCE SOFTWARE EXECUTIVE (CMSE)

(*Strike out term that does not apply)

SIGNATURES – DEVELOPING COMPANY	DATE
PREPARED BY: W. F. SATCHELL	
REVIEWED BY: PROJECT MANAGER — R. J. BRUSH, M. J. MICHALE	9/28/77
J. ROBINSON, R. L. YOUNG	10/11/77
DIVISION ENDORSEMENT: GENERAL MANAGER — R. D. KAZDA, E. H. MICHEAL (*Conditional AC – See Memo from R.L.Young to W.F. Satchell)	10/20/77
D. D. SLAIS, H. N. FRAZIER	10/25/77
COMPANY ENDORSEMENT. COMPANY DELEGATE — R. E. Wesslund	1-19-78

RESPONSE TO REVIEW DISTRIBUTION

	RESPONSE
DATA SERVICES...............	~~Approved, memo 2/8/78~~
SYSTEMS AND SERVICES COMPANY	Approved, memo 11/30/77
PERIPHERAL PRODUCTS COMPANY	Approved, non-response
XXXXXXXXXXXXXXXXCorp.Bus.Strat.	Approved, non-response
SERVICE BUREAU COMPANY	
PRODUCT AND SERVICES STRATEGY	

APPROVED: R. E. Wesslund
COMPANY DELEGATE

DATE

AA5441 12/74

CONTROL DATA CORPORATION
Engineering Services DIVISION

DOCUMENT CLASS Design Requirements PAGE NO. 2
PRODUCT NAME Common Maintenance Software Executive
PRODUCT MODEL NO. CYBER 80 MACHINE SERIES S2 S3 S4

0.0 STATEMENT OF COMPLIANCE

This DR document complies with all CYBER 80 Maintenance Software objectives set down within the CYBER 80 Architectural Objectives (AO) and MS/DO except those listed in the following sections. Also any waivers or deviations from the standards checked on the standards checklist.

0.1 AO ARH 1688 - Exceptions

- Sec. 3.2.4.4 A CC545 display is planned for the initial phase of the project. It will be supported by CMSE until there is no longer a requirement for the faster display, but not required by CMSE. *(O.K. as modified)*
- 3.2.2 Item 2 CMSE cannot be provide 100% customer security and still provide maintenance. It must be the responsiblity of CMSE, the tests, diagnostics and the utilities to stay within the disk address boundaries specified. ~~by the Operator/CE. The Operator/CE will have the responsibility of providing the correct disk address boundaries.~~ *(OK as modified)*
- Sec. 3.2.6.2 - System Initialization - The Common Maintenance Software Executive will reside on the same media as the firmware/controlware and is planned as being the same as the operating system media. *(OK)*
- Sec. 8.2.3 - 6th item - A dedicated input/output device for maintenance usage does not appear to be feasible. *(OK — signed 10/20/77)*

0.2 Maintenance Software DO ARH 914, Exceptions

- Sec. 3.1.2 - #2 - For CYBER 170 mode the executive will not retrieve on-line error reports. The CYBER 80 executive will retrieve the error reports if the operating system has logged them on a disk area that is known and accessable to CMSE.

0.3 Standards, Exceptions

0.3.1 CDC Standards

None.

0.3.2 National, International, and Industry Standards

None.

MINNEAPOLIS, MINNESOTA

DESIGN OBJECTIVES/REQUIREMENTS APPROVAL

COMPANY PRIVATE

Canadian Development DIVISION

[DO / DR] # ARH2130

REV. # 03

DESIGN [OBJECTIVES / REQUIREMENTS] FOR: CYBER 80 I/O

(*Strike out term that does not apply)

SIGNATURES – DEVELOPING COMPANY		DATE
PREPARED BY: B. E. Brookes, TTOFAC, X513		
REVIEWED BY: PROJECT MANAGER	B.E. Brookes by ND Flora	12/5/77
DIVISION ENDORSEMENT: GENERAL MANAGER	M J McHale	
COMPANY ENDORSEMENT: COMPANY DELEGATE	Robert E. Wunstel	1-31-78

RESPONSE TO REVIEW DISTRIBUTION

	RESPONSE
DATA SERVICES.....	Approved, non-response
SYSTEMS AND SERVICES COMPANY	Approved, memo 1/12/78
PERIPHERAL PRODUCTS COMPANY	Approved, non-response
xxxxxxxxxxxxxxx Corp.Bus.Strat.	Approved, non-response
SERVICE BUREAU COMPANY	
PRODUCT AND SERVICES STRATEGY	

APPROVED: R. E. Wunstel
COMPANY DELEGATE

DATE 3-1-78

1.0 DEFINITION

Cyber 80 I/O is the I/O System for the Cyber 80 S2 and S3 Mainframes. Its main characteristics are:

- Common I/O Hardware for advanced Cyber 170 NOS and NOS/BE and Cyber 80 OS.
- Plug Compatibility at the channel level with Cyber 170 Peripherals.
- 5 to 20 Peripheral Processors.
- 8 to 24 Channels.
- 2 to 6 Independent interfaces for connection to the Cyber 80 Maintenance Channel.
- 16-Bit internal processing with 12-bit processing for the Advanced Cyber 170.
- Ability to support low cost operator console and remote maintenance.

1.2 STATEMENT OF COMPLIANCE

CY80 I/O conforms to the AO/R Rev A except as follows:

Item	DR	AO/R
• Mfg. Cost of Target System 10PP/16CH	$67.6K*	$53K
Allowance for Maintenance Processer	0.	5
	$67.6K	$58K
• MTBF Elemental 10PP/16CH	2160 hrs	2300 hrs
• MTBUA (at CY80 release)	970	1032
• MTBI down CY170 (at release)	437	475

NOTE *: Manufacturing Cost Breakdown

• Pak including +10% variance	$23.5K
• Cabinet and STCO	44.1K
TOTAL	$67.6K

- The most recent manufacturing cost information, dated 6 Oct 1977, estimates the 10th unit cost of the target system to be $71,246.

R E Wunstel 11/30/77

DESIGN OBJECTIVES/REQUIREMENTS APPROVAL

COMPANY PRIVATE

COMPUTER DEVELOPMENT DIVISION

[XXX / DR] # ARH2249

REV. # 0

DESIGN [OBJECTIVES / REQUIREMENTS] FOR: CYBER 80 ECS COUPLER

(*Strike out term that does not apply)

SIGNATURES – DEVELOPING COMPANY	DATE
PREPARED BY: N.G.Horning N. G. Horning	9/21/77
REVIEWED BY: PROJECT MANAGER N.G.Horning/V.H.Hill 9/21/77 V. H. Hill 9/23/77	9/22/77
R.L.Wilson/R.C.Eppel 9/21/77 R. L. Wilson 9/21/77 R. C. Eppel	9/21/77
G.D.Elbess/M.J.Mohler 9/21/77 M. D. Elbess 9/21/77 M. J. Mohler	10/5/77
D.L.Davis 9/21/77 D. L. Davis	10/6/77
COMPANY APPROVAL: VICE PRESIDENT (company delegate)	

RESPONSE TO REVIEW DISTRIBUTION

	RESPONSE
SYSTEMS AND SERVICES COMPANY	
PERIPHERAL PRODUCTS COMPANY	
MARKETING COMPANY	
PRODUCT AND SERVICES STRATEGY	
CORPORATE ENGINEERING AND SOFTWARE	
CORPORATE MANUFACTURING, MTL., AND QA	

APPROVED: _____ _____

VICE PRESIDENT (company delegate) DATE _____

AASM-1173

CYBER 80 ECS COUPLER DR

0.0 Statement of Compliance

The Cyber 80 ECS Coupler will comply with the applicable sections of the Cyber 85 Architectural Objectives/Requirements Document, No. ARH1686, Rev. 07 (second draft revision 5, 8-15-77) except for the following:

Section 10.3 ECS Coupler

- The AO statement is - Manufacturing cost objective is $10K/10th unit (including cabinet and cable).
- The exception is based on a Manufacturing Cost Estimate (dated 8/29/77) which estimated a cost of $12,800 for the 10th production coupler. For a cost breakdown, see Section 3.4.1.

O.K (Cost is still small relative to ECS/ESM)
L W K 10/3/77

MINNEAPOLIS, MINNESOTA

DESIGN OBJECTIVES/REQUIREMENTS APPROVAL

COMPANY PRIVATE

COMPUTER DEVELOPMENT DIVISION

*[XX / DR] # ARH2568

REV. # 01

DESIGN *[OBJECTIVES / REQUIREMENTS] FOR: Configuration and Environment Monitor - CYBER 80

(*Strike out term that does not apply)

SIGNATURES – DEVELOPING COMPANY		DATE
PREPARED BY: L. R. Hartung		12/20/77
REVIEWED BY: PROJECT MANAGER	G. R. Norberg/E. A. Swanson	
E. A. Stoffel	R. J. Brush	1/13/78
J. L. Chapman		
E. R. Vankrevelen	R. C. Eppel	1/6/78
M. A. Doyle		
G. D. Floss	M. J. McHale	
K. J. Dykstra		
COMPANY APPROVAL: VICE PRESIDENT (company delegate)		

AD&C – E. H. Michehl 3/6/78

RESPONSE TO REVIEW DISTRIBUTION

NPP Program OFFICE – D. L. Slais 3/5/78

NPP – L. E. Jodsaas

	RESPONSE
SYSTEMS AND SERVICES COMPANY	
PERIPHERAL PRODUCTS COMPANY	
MARKETING COMPANY	
PRODUCT AND SERVICES STRATEGY	
CORPORATE ENGINEERING AND SOFTWARE	
CORPORATE MANUFACTURING, MTL., AND OA	

APPROVED: _____ _____

VICE PRESIDENT (company delegate) DATE _____

AA5441 7/73

1.3 STATEMENT OF COMPLIANCE

This DR defines the CEM, and as such, conforms with the CDC CYBER 80 System Baseline Definition, with the following exceptions.

Item	This DR Reference	A.O/R Reference
Mfg Cost CEM	3.4.1 $5,900	11.1.3 [12.4.1] $5,000
S2 Power System	3.4.3 $12,404	12.4.1 $11,000

OK R. H. Michehl 3/6/78