Control Data® CYBER 170 Model 750 Computer System

CONTROL DATA

The CDC® CYBER 170 Model 750 Computer is a multipurpose system that provides real-time/time-critical network, commercial, data management and scientific capabilities. This computer system is field-upgradable to a Model 760. Series 700 provides performance enhancement over the previous CDC CYBER 170 series, but maintains software and application compatibility with previous products.

Model 750 features a single central processor that uses subnanosecond Emitter-Coupled Logic (ECL) integrated circuits to provide high reliability, compact physical packaging and low power requirements. Access to the central processor is provided via central memory and optional groups of peripheral processors. Isolated memory facilities within each of the peripheral processors enable programs to be executed independently within each of the peripheral processors. In solving a problem, peripheral processors provide high-speed information transfer in and out of the system. A number of problems can be processed concurrently by the parallel action of various peripheral units.

Central Processor

The Central Processor Unit (CPU) is composed of nine phased arithmetic functional units and the central memory control. The nine functional units operate as independent, specialized units that concurrently perform all computations. Data moves in and out of the functional units through the internal operating registers.

Central Memory Control

Central Memory Control (CMC) circuits direct arithmetic operation and provide interface between the functional units and central memory. CMC also performs instruction retrieving, address preparation, memory protection, and data retrieving and storing.

Central Memory

Central memory is organized into logically independent banks and many banks can be in operation simultaneously. These circuits are composed of 4K static-type Metallic-Oxide Semiconductor (MOS) chips, which provide memory access time of 400 nanoseconds. Memory banks are phased so that successive addresses are in different banks, permitting operation at much higher rates than the basic cycle time. Memory is formatted in 60-bit words that permit data to be either ten 6-bit characters or a floating-point number with a 48-bit coefficient and 11-bit exponent. Maximum data transfer rate is 10 characters per 50 nanoseconds. Memory size of the Model 750 may range from 1.31 million characters to 2.62 million characters.

Peripheral Processor Subsystem

Model 750 can be configured to include one or two Peripheral Processor Subsystems (PPS). The basic PPS consists of 10 Peripheral Processors (PPs) and 12 data channels. The second PPS (optional) can be selected to expand to 14, 17 or 20 PPs overall and includes an additional 12 data channels, providing a total of 20 PPs and 24 data channels. Each PP is a functionally independent computer comprising 8K 6-bit characters of MOS memory and arithmetic section that support a full repertoire of arithmetic and input/output instructions. Depending on the options used, 12 or 24 data channels are serviced by the PPUs and each bi-directional data channel has a maximum data rate of 4 million characters per second.

Extended Core Storage

The optional Extended Core Storage (ECS) subsystem includes a controller and one or more distributive data paths that attach to input/output channels. The transfer rate between ECS and central memory is up to 100 million 6-bit characters per second, where at least 5 million characters are available. ECS is available in sizes from 2.6 million characters to 20 million characters and can be shared by separate CDC CYBER 170 Systems.

Peripheral Equipment

The following peripheral equipment can be attached to the Model 750:

- Magnetic Tape Transports
- Line Printers
- Console Displays
- Rotating Mass Storage
- Communication Interfaces
- Card Readers
- Card Punches
- Graphics Terminals
- Interactive Terminals
- Remote Batch Terminals

Interfacing equipment used with mass storage devices and communications subsystems has independent memory facilities and is programmable via controlware (vendor-installed software). This allows distribution of control functions to these subsystems.

Software

All members of the CDC CYBER 170 Series 700 family are supported by the CDC CYBER 170 Network Operating System—a powerful, multimode operating system. This system operates with an extensive software and product set which includes: COMPASS (assembler language), FORTRAN, COBOL, ALGOL, APL, SORT/MERGE, BASIC, GPSS, SIMSCRIPT, APT (numerical control for machine tools), and a comprehensive set of basic data management software.

Specifications

Central Processor	
Instruction Stack	Holds up to twelve 60-bit instruction words
Computation	In floating-point and fixed point, single and double precision
Phased Functional Units	Boolean, shift, normalize, integer add, floating add, multiply, divide, population count and increment
Central Memory	
Storage Circuits	MOS 4K
Access Time	400 ns (phased)
Capacity	1.31M, 1.96M and 2.62M 6-bit characters
Memory Organization	Logically independent banks of words with corresponding multiphasing of banks
Transfer Rate	Up to 10 characters each 50 ns (phased operation)
Peripheral Processor Subsystem	
Configurations	10 peripheral processors (an additional 4, 7 or 10 optional)
Memory	MOS, 8K characters
Data Channels	12 or 24 input/output
Major Cycle Time	500 ns
Computation	Fixed point
Extended Core Storage	
Transfer Rate	100 M characters/s
Capacity	2.62M to 20M characters
Distributive Data Path	Up to 4 peripheral processor units per path access to ECS. A 480-bit data path connects input/output to ECS.

Specifications subject to change without notice

201,814 LITHO IN U.S.A. 4/79