CONTROL DATA
CORPORATION

CONTROL DATA®
7077-1
COMMUNICATIONS STATION

REFERENCE MANUAL

REVISION RECORD

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PREFACE

This manual contains programming information for the CONTROL DATA® 7077-1 Communications Station.

The following manuals contain customer engineering information for the equipments which comprise the station:

Title	Pub. No.
DT175-A/B PPU-SAC Coupler	60352300
FJ430-A/B Storage Access Controller	60316500
GH408-A/B Central Storage Cabinet	60316600

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SYSTEM DESCRIPTION 1

INTRODUCTION

The CDC® 7077-1 Communications Station is a subsystem which provides interface and storage capability between a CDC® 6000 or CDC® CYBER 72, 73, or 74 PPU and up to three CDC® 791-1 Communications Subsystem Controllers (controllers). The station communicates with the controller(s) via the compatible trunk interface.

The station consists of:

- Storage access controller (SAC) which utilizes a processor port, function port, two storage channels, and three I/O channels.
- Central storage cabinet (CSC) containing 8192 18-bit words of magnetic core storage with a memory cycle time of 1.1 microsecond and an access time of 460 nanoseconds.
- PPU-SAC coupler (coupler) which provides interface capability between the PPU I/O channel and the SAC/CSC.

The memory (CSC) can be expanded in increments of 8192 words to a maximum of 32,768 words by adding the following options:

10262-1 Memory Increment Module (8K)

10262-2 Memory Expansion Module (8K)

10262-3 Memory Increment Module (8K)

Figure 1-1 is a basic block diagram of the station configuration.

The software elements of the coupler and the storage system (SAC/CSC) are discussed in detail in Sections 2 and 3 respectively.

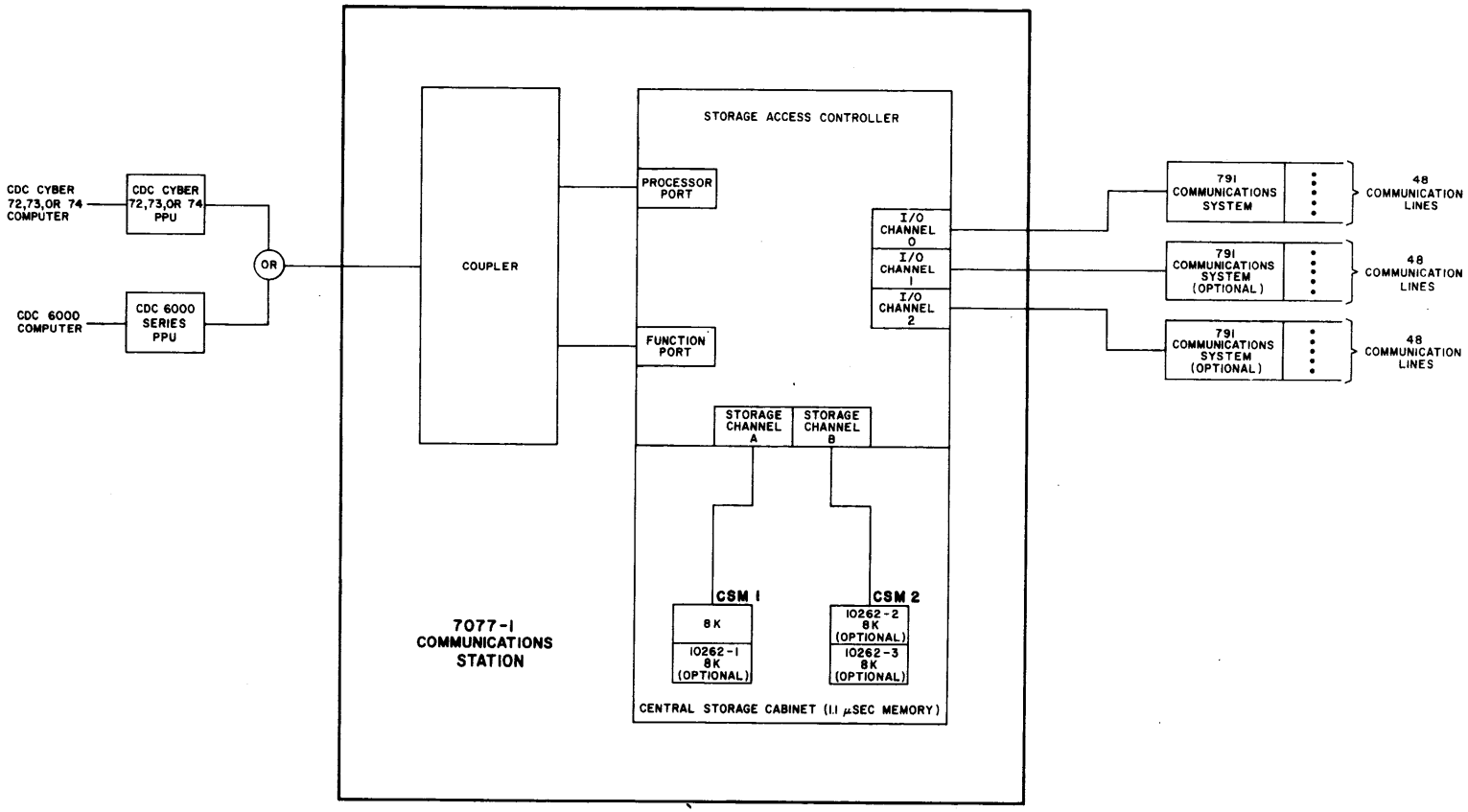


Figure 1-1. 7077-1 Communications Station Configuration

PHYSICAL CHARACTERISTICS

COUPLER

Dimensions and Weight

Height	62 in. (158 cm)
Width	27 in. (69 cm)
Depth	29.5 in. (75 cm)
Weight	400 lb. (180 kg)

Power Requirements

Power Supply	208 volts, 400 Hz, 3 phase
Blower	
60 Hz	120 volts, 60 Hz, 1 phase
50 Hz	240 volts, 50 Hz, 1 phase

Environmental Requirements

Cooling method	Forced air (internal blower)
Operating temperature	$40^{\circ}F$ ($4.4^{\circ}C$) - $120^{\circ}F$ ($49^{\circ}C$)
Operating humidity	5 percent relative humidity (RH) - 95 percent RH

SAC/CSC

Dimensions

Height	62 in. (158 cm)
Width	70.5 in. (179 cm)
Depth	29.5 in. (75 cm)

Power Requirements

Power supply	208 volts, 400 Hz, 3 phase
Blowers	
60 Hz	120 volts, 60 Hz, 1 phase
50 Hz	240 volts, 50 Hz, 1 phase

Environmental Requirements

Cooling method	Forced air (internal blowers)
Operating temperature	$40^{\circ}F$ ($4.4^{\circ}C$) - $100^{\circ}F$ ($37.8^{\circ}C$)
Operating humidity	10 percent RH - 90 percent RH

EXTERNAL INTERFACE

PPU/STATION INTERFACE

The standard PPU input/output instructions, flags, and data transfer procedures are used for the PPU/station interface. Reference the appropriate PPU system reference manual for the I/O description.

STATION/CONTROLLER INTERFACE

The station and CDC® 791-1 Communications Subsystem Controller interface via the compatible trunk interface. Section 3 (SAC I/O Channel Operations) contains a general description of this interface. For a detailed description, including such parameters as transmission rates, pulse widths, etc., refer to the CONTROL DATA® Compatible Trunk Interface Specifications Manual, Pub. No. 60365900.

PPU/SAC COUPLER 2

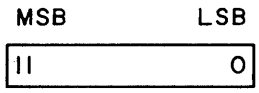
INTRODUCTION

The PPU-SAC coupler (coupler) interfaces the PPU via the I/O channel with the storage access controller (SAC) and central storage cabinet (CSC). The coupler permits the PPU to function and status the SAC and perform read/write operations in the CSC. The coupler:

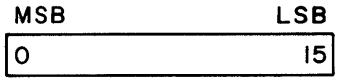
- Performs assembly/disassembly
- Operates in one of eight modes selected by a PPU function code

ASSEMBLY/DISASSEMBLY

Address and data transfers between the PPU and the coupler are in 12-bit words shown as follows.



Address and data transfers between the SAC/CSC and the coupler are in 16-bit words shown as follows.



Note that bit 0 of the PPU word is the least significant bit and bit 0 of the SAC/CSC word is the most significant bit.

ADDRESS ASSEMBLY

Addresses are assembled as shown in Figure 2-1.

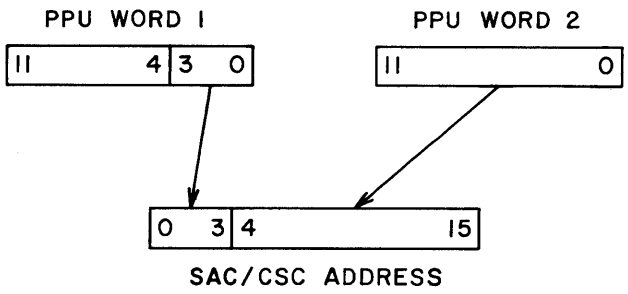


Figure 2-1. Address Assembly

Bits 3 to 0 of the first PPU word become bits 0 to 3 of the address. Bits 11 to 0 of the second PPU word become bits 4 to 15 of the address. Thus, the first PPU word is the stack number and the second PPU word is the address within the 4K stack. (See Figure 3-1.) The coupler disregards bits 11 to 4 of the first PPU word.

DATA ASSEMBLY/DISASSEMBLY

8-BIT MODE

Data assembly/disassembly in 8-bit mode is shown in Figure 2-2.

In 8-bit mode two PPU words correspond to one SAC/CSC word. Bits 7 to 0 of the first word transferred correspond to bits 0 to 7 of the SAC/CSC data word. Bits 7 to 0 of the second word transferred correspond to bits 8 to 15 of the SAC/CSC data word. The most significant four bits of both PPU words are not used. They are set to zero on a read and disregarded on a write.

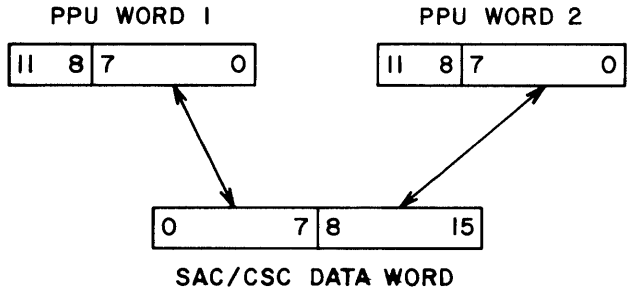


Figure 2-2. 8-Bit Assembly/Disassembly

12-BIT MODE

Data assembly/disassembly in 12-bit mode is shown in Figure 2-3.

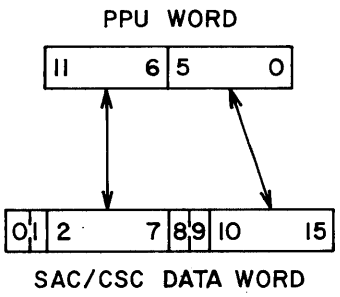


Figure 2-3. 12-Bit Assembly/Disassembly

In 12-bit mode one PPU word corresponds to one SAC/CSC word. Bits 11 to 6 of the PPU word correspond to bits 2 to 7 of the SAC/CSC word. Bits 5 to 0 of the PPU word correspond to bits 10 to 15 of the SAC/CSC word. Bits 0, 1, 8, and 9 of the SAC/CSC word are not used. They are set to zero on a write and disregarded on a read.

COUPLER/SAC INTERFACE

The coupler and SAC are connected by 81 signal lines as shown in Figure 2-4.

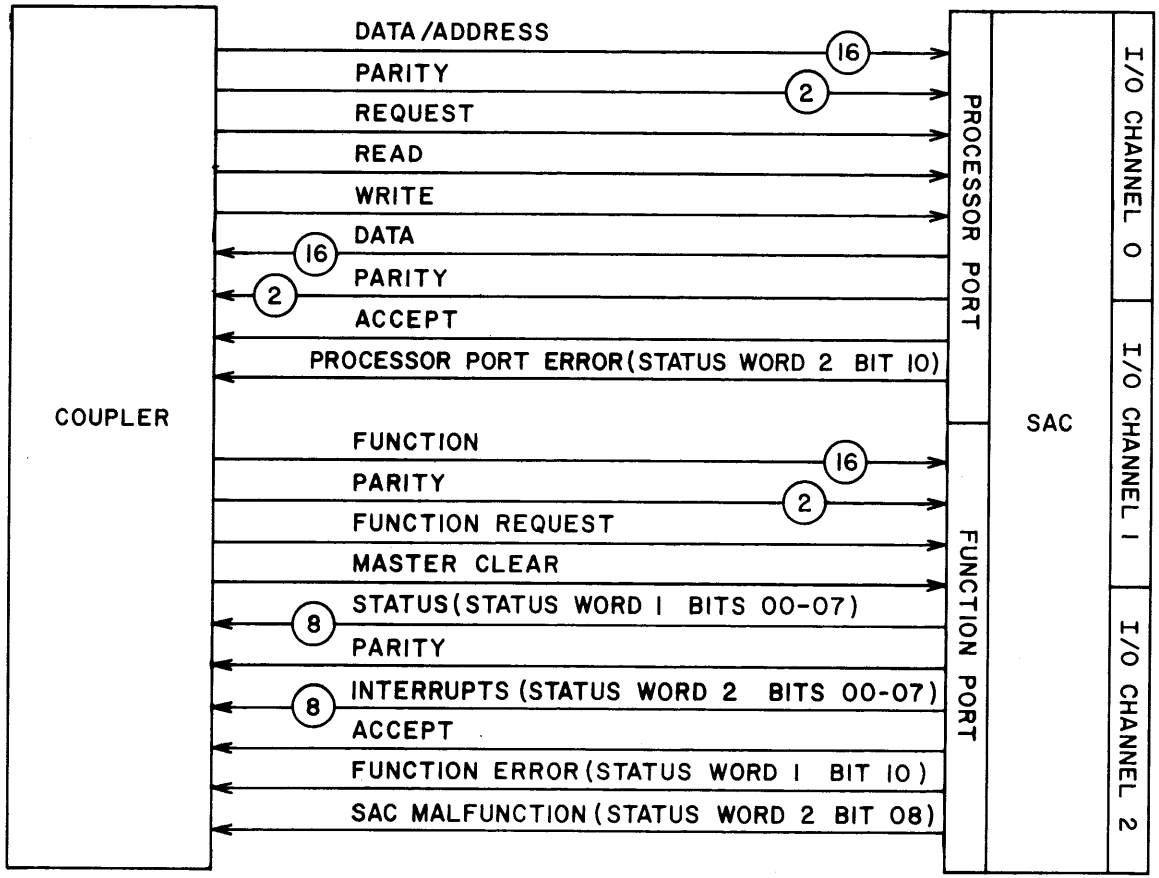


Figure 2-4. Coupler/SAC Interface

MODES OF OPERATION

The coupler has eight modes of operation which are selected by sending a function signal and a 12-bit octal function code from the PPU to the coupler. Only one mode of operation may be selected at one time. Table 2-1 lists the eight operational mode function codes and their associated descriptions.

TABLE 2-1. MODE SELECTION FUNCTION CODES

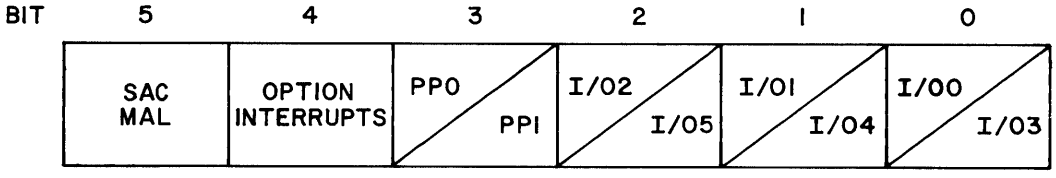
Function Code	Description
70xx	Disconnect/Clear Interrupts
7100	8-Bit Block Read
7200	8-Bit Block Write
7300	Request Status Word 1
7400	Request Status Word 2
7500	12-Bit Block Read
7600	12-Bit Block Write
7700	Function Mode

All read/write operations are block transfers. When an address is transferred from the PPU to the coupler, sequential reads or writes are performed as long as the PPU inputs or outputs data. The PPU terminates a write operation by disconnecting the I/O channel and requesting status word 2. (Table 2-3, Bit 11.) The coupler terminates a read operation by decrementing the read word count to zero.

The following paragraphs describe the eight modes of operation.

DISCONNECT/CLEAR INTERRUPTS (70XX)

When this code is received from the PPU with a function signal, the interrupts specified by bits 5 to 0 are cleared. Assignments to the six bit positions are shown as follows.



When bit 5 is set, SAC Malfunction (Table 2-3, Bit 8) is cleared.

With bit 4 clear, the basic SAC channel interrupts (I/O 0, I/O 1, I/O 2, PP0) are cleared by setting the assigned bit(s) 0, 1, 2, 3 (Table 2-3, Bits 0 to 3 respectively). Coupler hardware permits the optional SAC channel interrupts (I/O 3, I/O 4, I/O 5, PP1) to be cleared by setting the assigned bit(s) 0, 1, 2, 3 with bit 4 set. Although the station uses only the basic SAC channels, all bits should be cleared upon initialization.

Up to four interrupts plus SAC Malfunction may be cleared at one time.

A function code of 7000 disconnects the coupler from the I/O channel. When the coupler is disconnected, it does not respond to full, empty, active, or inactive from the PPU. The I/O channel may then be used for inter-PPU communications. A function signal reconnects the coupler.

8-BIT BLOCK READ (7100)

When this code is received from the PPU with a function signal followed by three words of data, the coupler reads from the SAC/CSC. The first two data words are assembled to make a 16-bit CSC address (Figure 2-1). The third word is the number of CSC words to be read. After the word count is received by the coupler, a memory reference is initiated via the SAC processor port.

When a 16-bit word is received from the SAC, it is broken into two 8-bit bytes (Figure 2-2). SAC/CSC bits 0 to 7 are sent to the PPU as bits 7 to 0. PPU bits 11 to 8 are zero.

After the first 8 bits are accepted by the PPU, the second 8 bits are sent. SAC/CSC bits 8 to 15 become PPU bits 7 to 0. PPU bits 11 to 8 are zero.

When the second 8-bit byte is sent to the PPU, the coupler increments the CSC address by one, decrements the word count by one, and initiates another memory reference before the second byte is accepted by the PPU. When the word count reaches zero, the coupler disconnects the I/O channel.

8-BIT BLOCK WRITE (7200)

When this code is received from the PPU with a function signal followed by at least four words from the PPU, the coupler initiates a write to CSC.

The first and second words from the PPU become the CSC address (Figure 2-1) and the third and fourth words become one 16-bit CSC word. Bits 7 to 0 of the third PPU word become SAC/CSC bits 0 to 7, and bits 7 to 0 of the fourth PPU word become SAC/CSC bits 8 to 15 (Figure 2-2). The four most significant bits of the PPU words are not used.

After the 16-bit word is assembled, it is written into CSC, the CSC address is incremented by one, and the coupler is ready to receive two more words from the PPU.

Each subsequent two word combination received from the PPU is assembled into a 16-bit word. Assembled 16-bit words are written into consecutive CSC addresses.

REQUEST STATUS WORD 1 (7300)

When this code is received from the PPU with a function signal and the I/O channel is made active, the coupler sends a 12-bit status word to the PPU with a full signal. The bit assignments for status word 1 are shown in Table 2-2. Bits 0 to 7 and bit 10 are generated by the SAC (Figure 2-4). Bits 08, 09, and 11 are generated by the coupler.

TABLE 2-2. STATUS WORD 1 BIT ASSIGNMENTS

Bit	Description
0	Status from Function Port Bit 15
1	Status from Function Port Bit 14
2	Status from Function Port Bit 13
3	Status from Function Port Bit 12
4	Status from Function Port Bit 11
5	Status from Function Port Bit 10
6	Status from Function Port Bit 9
7	Status from Function Port Bit 8
8	Set Status
9	Sense Error
10	Function Error
11	Function Complete

Bits 0 to 7 are set if the corresponding function port bit is set. Table 2-4 lists the bit assignments under the column "PPU Input Channel".

Bit 8 (set status) is set if the last function sent to the SAC function port was a function to set status. It is cleared by master clear or by transmitting a sense status function to the function port.

Bit 9 (sense error) is set if the coupler detects a SAC function port parity error. It is cleared by master clear or by the receipt of a Function Mode function code (7700) from the PPU.

Bit 10 (function error) is set if the SAC detects a function port error. It is cleared by master clear or by transmitting a function to the function port.

Bit 11 (function complete) is set when SAC has finished processing a function. When a sense status function has been transmitted, this bit set indicates that the least significant 8 bits of status word 1 contain the desired status from SAC.

REQUEST STATUS WORD 2 (7400)

When this code is received from the PPU with a function signal and the I/O channel is made active, the coupler sends a 12-bit status word to the PPU. The bit assignments for status word 2 are shown in Table 2-3. Bits 0 to 7, bit 8 and bit 10 are generated by the SAC (Figure 2-4). Bits 9 and 11 are generated by the coupler.

TABLE 2-3. STATUS WORD 2 BIT ASSIGNMENTS

Bit	Description	
0	I/O 0 Interrupt	
1	I/O 1 Interrupt	
2	I/O 2 Interrupt	
3	PP 0 Interrupt	
4	I/O 3 Interrupt	Not Used
5	I/O 4 Interrupt	
6	I/O 5 Interrupt	
7	PP 1 Interrupt	
8	SAC Malfunction	
9	Data Error	
10	Processor Port Error	
11	Write Busy	

Bits 0 to 7 (interrupts) are set when a device on a SAC I/O channel or processor port sends an interrupt to the SAC. They are cleared by a clear interrupt function (70xx) from the PPU.

Bit 8 (SAC malfunction) is set if the SAC detects an I/O channel or processor port error. It is cleared by master clear or a clear interrupt function (70xx) from the PPU.

Bit 9 (data error) is set if the coupler detects a parity error on data received from the SAC processor port. It is cleared by master clear or by transmitting a new read or write function.

Bit 10 (processor port error) is set if the SAC detects a processor port error. It is cleared by master clear or by transmitting a new read or write function.

Bit 11 (write busy) is set if the last write operation is still in progress. The PPU should sense this bit following a write operation. No new read, write, or function mode operation should be started until this bit is cleared by the completion of the write operation or by master clear.

12-BIT BLOCK READ (7500)

When this code is received from the PPU with a function signal followed by three words from the PPU, the coupler reads from the SAC/CSC. The first two data words are assembled to make a 16-bit CSC address (Figure 2-1). The third word is the number of CSC words to be read. After the word count is received by the coupler, a memory reference is initiated via the SAC processor port.

When a 16-bit word is received from the SAC, 12 bits are sent to the PPU (Figure 2-3). SAC/CSC bits 2 to 7 become PPU bits 11 to 6. SAC/CSC bits 10 to 15 become PPU bits 5 to 0. SAC/CSC bits 0, 1, 8, and 9 are not used.

When the data is transmitted to the PPU, the coupler increments the CSC address by one, decrements the word count by one, and initiates another memory reference. When the word count reaches zero, the coupler disconnects the I/O channel.

12-BIT BLOCK WRITE (7600)

When this code is received from the PPU with a function signal followed by at least three words from the PPU, the coupler initiates a write to CSC.

The first and second words from the PPU become the CSC address (Figure 2-1), and the third 12-bit PPU word becomes a 16-bit SAC/CSC word (Figure 2-3). Bits 11 to 6 of the PPU word become SAC/CSC bits 2 to 7, and PPU bits 5 to 0 become SAC/CSC bits 10 to 15. SAC/CSC bits 0, 1, 8, and 9 are zero.

The 16-bit word is written into CSC, the CSC address is incremented by one, and the coupler is ready to receive another word from the PPU.

Subsequent words from the PPU are written into consecutive CSC addresses.

FUNCTION MODE (7700)

When this code is received from PPU with a function signal followed by two words from the PPU, the coupler assembles a 16-bit function port code and sends it to the SAC function port. The function port code is assembled as shown in Figure 2-5.

Bits 8 to 1 of the first PPU word become bits 0 to 7 of the function port code. Bits 7 to 0 of the second PPU word become bits 8 to 15 of the function port code. All other PPU bits are not used by the coupler and are disregarded.

When the coupler receives the second PPU word, the assembled function code is sent to the SAC function port, and the coupler is ready for another word from the PPU. After the coupler receives an accept from SAC and sets function complete, the coupler is ready to send another function to SAC. Each subsequent two additional words received from the PPU are assembled into a 16-bit function port code and sent to the SAC function port. Table 2-4 lists the function codes as exchanged between the PPU and the coupler.

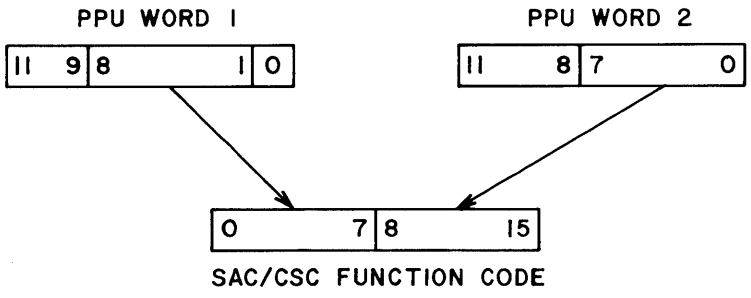
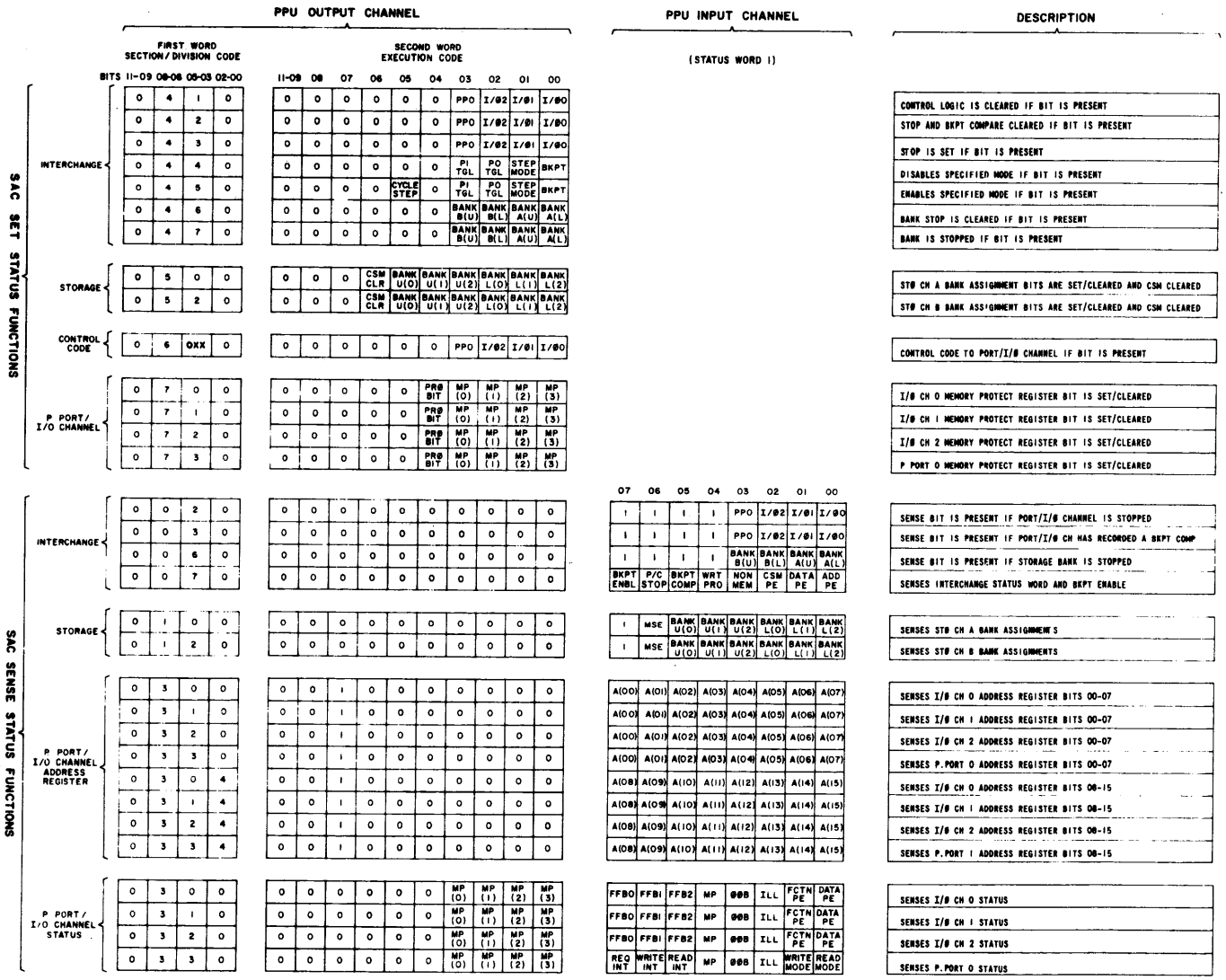


Figure 2-5. Function Port Code Assembly

TABLE 2-4. FUNCTION PORT CODES (PPU-COUPLER)



MASTER CLEAR

This signal is sent from the PPU to the coupler where it clears control logic and registers. The coupler then passes the signal on to the SAC. A master clear disconnects the coupler which can be reconnected by a new function from the PPU.

STATION STORAGE UNIT (SAC/CSC) 3

INTRODUCTION

The station storage unit consists of a storage access controller (SAC) and a central storage cabinet (CSC) which contains 8192 18-bit words of core memory with a 1.1 microsecond cycle time. The memory can be expanded to a maximum of 32,768 words in 8K increments.

The storage unit provides high-speed, random access magnetic core storage for the communications station. Function codes are sent to the SAC from the PPU to control the functions of the SAC. The following paragraphs describe the operation of the storage system.

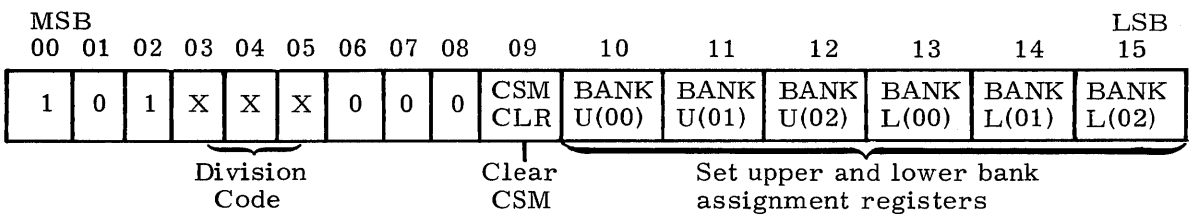
CENTRAL STORAGE CABINET (CSC)

The CSC (1.1 microsecond memory) consists of two central storage module chassis (CSM 1, CSM 2). With a maximum memory configuration (32K memory), each CSM chassis contains four 4K-memory stacks. Within each CSM the stacks are arranged in banks, each bank containing two stacks or 8K of memory. The banks are designated upper bank and lower bank.

Prior to initially using the 1.1 microsecond memory, the SAC storage channels must be assigned a unique 3-bit upper and lower bank number via software. This is accomplished by setting bank assignment registers within the storage channels of the SAC. Figure 3-1 shows the initialization of the 1.1 microsecond memory with typical bank numbers assigned.

The banks may be assigned any number between 000_2 and 111_2 providing no two banks are assigned the same number. For continuous addressing, the banks may be numbered 000_2 starting at the lower bank of channel A through 011_2 ending at the upper bank of channel B.

The bank assignment registers are set by a SAC set status function code via the function port of the SAC. The specific format for setting the bank assignment registers is as follows:



Division Code:

Bit 03	04	05	Channel select
0	0	0	A
0	1	0	B

Clear CSM

Bit 09

0	Selected CSM control logic unchanged
1	Selected CSM control logic cleared

Bits 10 - 15

0	Clears respective bank assignment register of selected channel
1	Sets respective bank assignment register of selected channel

Figure 3-1 shows the bank assignment registers sequentially numbered 000_2 through 011_2. The storage request address from the SAC interchange is 0001100000001111_2, with the three most significant bits (00 through 02) equal to 000_2.

Bits 00 through 02 of the storage request address are compared with the bank assignment numbers of each storage channel. Since a comparison is made in the lower bank of channel A, the control logic of channel A is selected and bit 02 of the storage request address is a 0 indicating selection of a lower bank. If the lower bank of channel A had been assigned a number where bit 02 was a 1, bit 02 of the storage request address would have been changed to a 0 after the compare was made, thereby indicating selection of a lower bank.

After the channel and CSM bank have been selected in the SAC storage channels, bits 02 through 15 are sent to the appropriate CSM within the central storage cabinet. Bits 02 and 03 are translated within the CSM for stack selection. Bits 04 through 15 are the stack address for the selected stack within the CSM. In Figure 3-1, stack 1 has been selected with a stack address of 100000001111_2.

STORAGE ACCESS CONTROLLER (SAC)

The storage access controller (SAC) connects I/O channels and a processor port to two storage channels through the SAC interchange. Control of the SAC is accomplished through the function port which connects to the PPU I/O channel via the coupler.

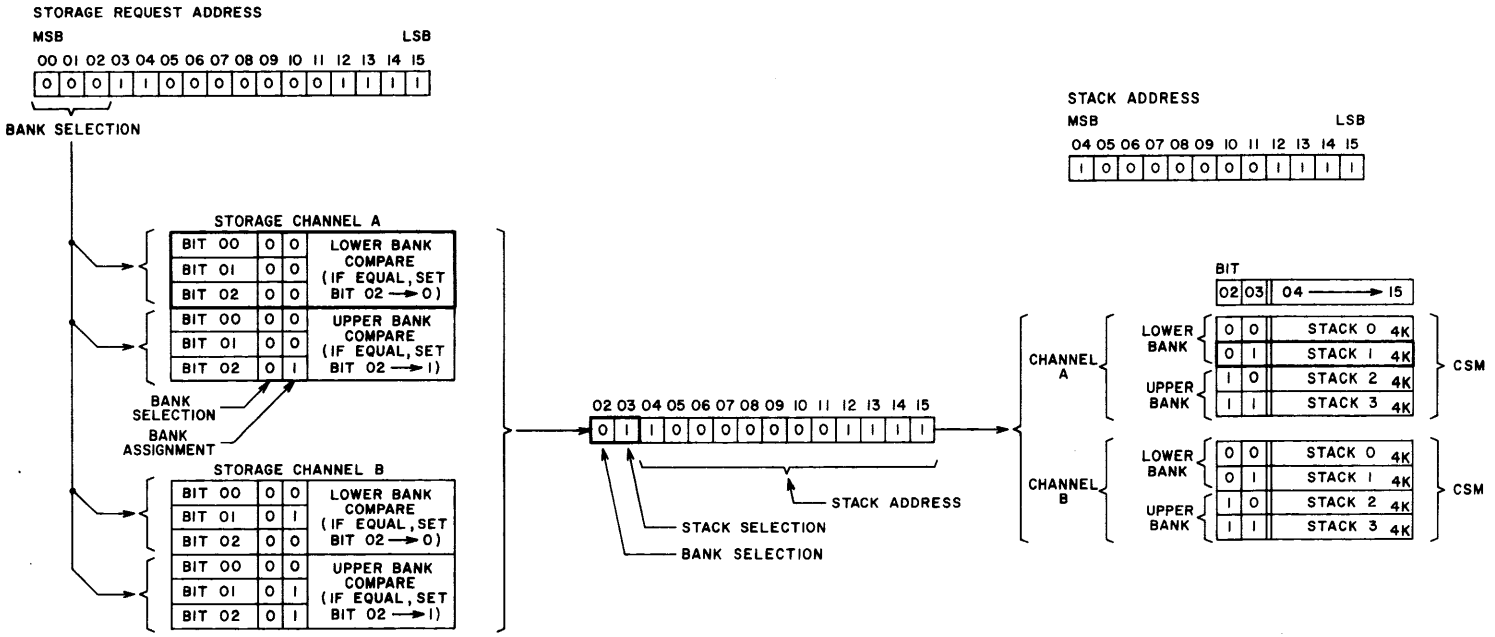


Figure 3-1. 1.1 Microsecond Memory Configuration and Initialization

SAC INTERCHANGE

The interchange interconnects the I/O channels and processor port with the storage channels. The interchange is capable of one transfer to a storage channel approximately every 275 nanoseconds. A SAC I/O channel or processor port cannot transfer data (read or write) any faster than one word each memory cycle time, or 1.1 microsecond. Assuming maximum storage the SAC can maintain a 1.1 microsecond transfer rate on two I/O channels simultaneously, providing each unit is communicating with a different storage channel.

INTERCHANGE PRIORITIES

The interchange may be requested by the I/O channels, by the processor port, or by SAC functions.

When two or more requests occur at the same time, the SAC executes one request according to predetermined priorities. SAC functions have the highest priority over port and channel requests. The port and channel priorities are set by a switch on the SAC. Table 3-1 lists the switch settings for the port and channels with the highest priority listed first under each position setting. Once a request has been recognized by the interchange, it will be completely executed regardless of the level of priority.

TABLE 3-1. INTERCHANGE PRIORITY SETTINGS

Switch	
Position 1 (Low)	Position 2 (High)
I/O Channel 0	Processor Port 0
I/O Channel 1	I/O Channel 2
I/O Channel 2	I/O Channel 1
Processor Port 0	I/O Channel 0

A storage request never locks up the interchange longer than 2 microseconds. If the request takes longer than 2 microseconds, the source of the request is stopped, a SAC Malfunction is recorded, and the interchange is released.

Since only a single operation can occur in each storage channel, no output priority is necessary providing that I/O channels and the processor port requesting information can accept the information and that all CSC access times are identical.

The interchange can be cycle stepped under SAC function control. In this mode, only one interchange memory request may be processed per function command.

PARITY CHECKING

The interchange checks parity on address and data transfers to the storage channels. Odd parity is used. If a parity error is detected, the I/O channel or processor port is stopped, a SAC Malfunction is recorded, and a read request is sent to the CSC. If the original request was a write it is automatically changed to a read. A stopped channel or port may not transfer data, but may execute SAC functions.

Parity is checked by the storage channels on data transfers from the CSC to the I/O channels and processor port. Parity is checked by the I/O channels on transfers from the I/O devices.

SAC BREAKPOINT AND STORAGE PROTECTION

There are manual switches on the SAC which can be used as a breakpoint or storage protection feature. However, the switch panel is primarily used for maintenance.

The breakpoint compare is made at the interchange level for each memory reference. All of the following conditions must be met for a compare to occur:

1. Each bit of the memory reference address must match its corresponding address bit switch setting.
2. The requesting I/O channel or port must have its Enable switch set to ON.
3. If the operation is a read or destructive read, the Breakpoint Mode Enable Read switch must be set to ON.
4. If the operation is a write, the Breakpoint Mode Enable Write switch must be set to ON.
5. Either the Breakpoint Mode Enable Force switch must be set to ON, or the breakpoint must be enabled by software (SAC function code).

When a breakpoint compare occurs, the compare is recorded and a SAC malfunction is sent to the PPU via the SAC function port. If the Breakpoint Mode Enable Stop switch is in the OFF position, the SAC operation continues in a normal manner. If the Stop switch is ON, the I/O channel or port in which the compare occurred stops (not allowed to reference memory) and the memory reference in progress changes to a no operation.

TABLE 3-2. SAC BREAKPOINT SWITCH FUNCTIONS

Switch	Function
PROCESSOR PORT PRIORITIES	
BASIC	This switch provides a means of setting the processor ports and I/O channel priorities for the basic SAC (processor port 0 and I/O channels 0 through 2). If the switch is in the High position, the processor port will have the highest priority. If the switch is in the Low position, the processor port will have the lowest priority. Table 3-1 lists the actual priorities.
BREAKPOINT ADDRESS BITS	These 16 toggle switches can be used as a breakpoint, address trigger, or a storage protection feature. The switches may be set to a logical 1 (1), a logical 0 (0), or either (X).
I/O CHANNEL/PORT ENABLES	These switches enable the breakpoint compare when the respective I/O channel or port switch is ON.
BREAKPOINT MODE ENABLES	
STOP	When this switch is in the ON position, the SAC interchange will stop the requesting I/O channel or port when a breakpoint compare occurs.
FORCE	When this switch is ON, the breakpoint compare circuitry is enabled regardless of software function coding.
READ	When this switch is ON, the breakpoint compare circuitry will function only during read or destructive read operations.
WRITE	When this switch is ON, the breakpoint compare circuitry will function only during write operations.

SAC FUNCTION CODES

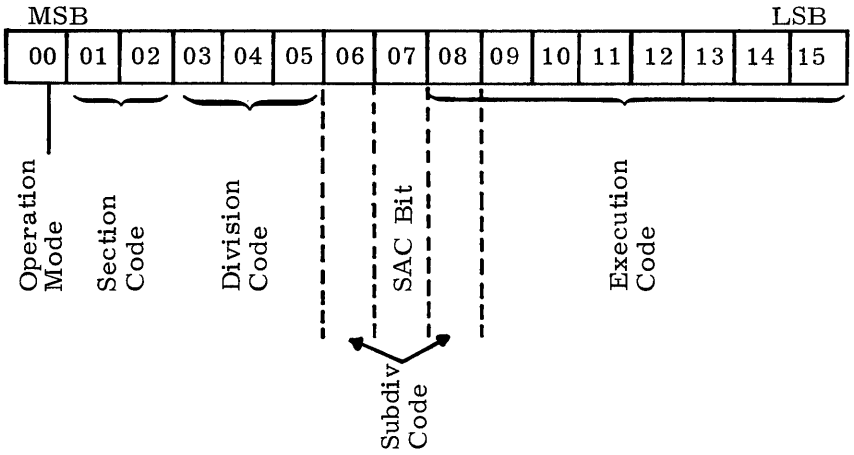
SAC functions are initiated via the SAC function port. The function port interfaces the SAC with the PPU via the coupler. The port contains input and output signals which are used to encode functions to be executed by the SAC or status signals to be sensed by the PPU.

SAC functions are encoded in the PPU, transmitted to the SAC via the coupler, decoded in the SAC, and executed when they obtain priority in the interchange. SAC status is sensed by the PPU via the function port and coupler. The PPU sends signals to the SAC which indicates the encoding of the status to be sent to the PPU.

Table 3-3 is a chart of the function codes as exchanged between the SAC and the coupler. See Figure 2-5 for function code assembly/disassembly performed by the coupler.

FUNCTION CODE FORMAT

The function code format which is encoded via software and transmitted to the SAC is as follows:

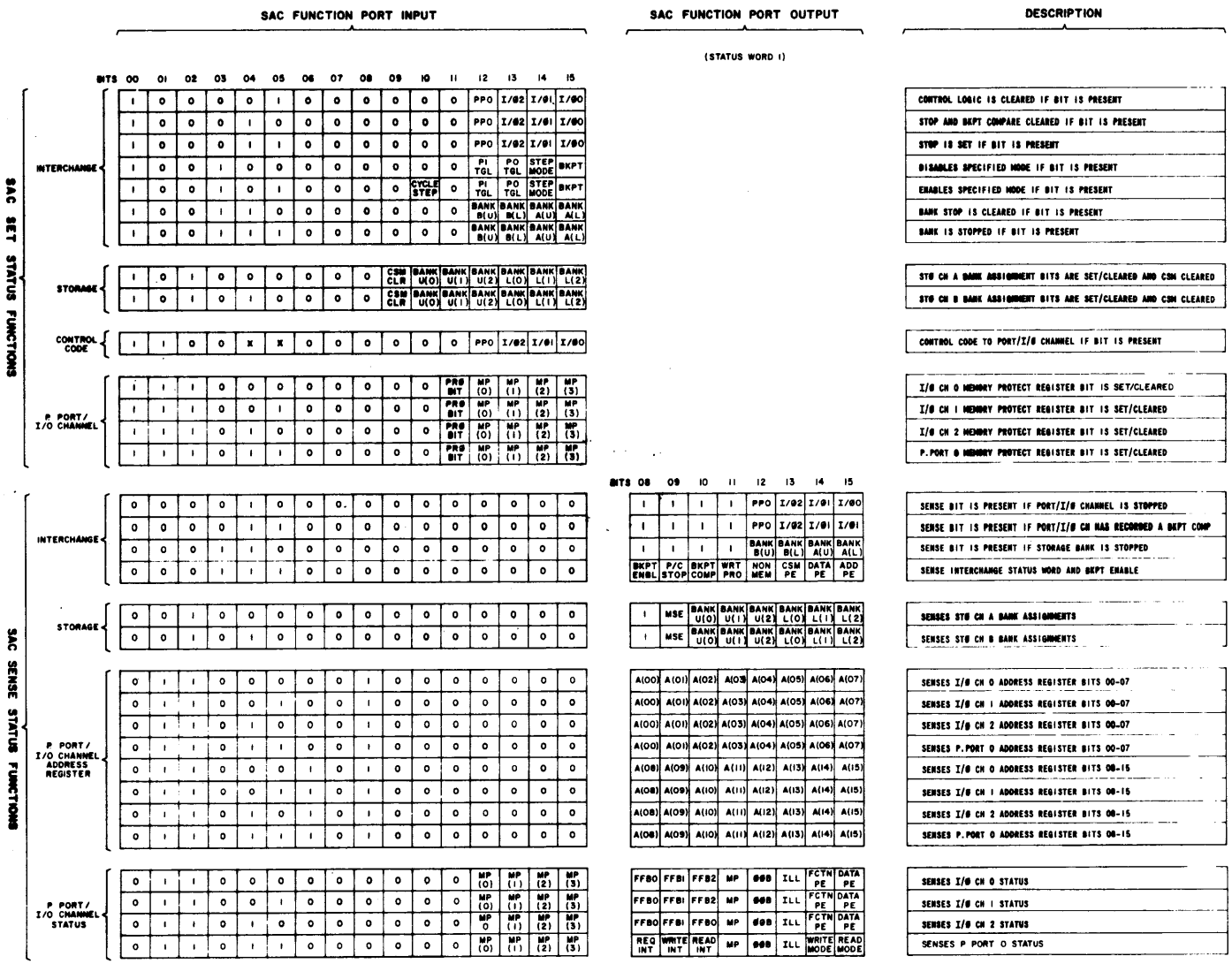


OPERATION MODE (BIT 00)

This bit determines whether the function is a set or sense status operation.

Bit 00	Operation
1	Set status
0	Sense status

TABLE 3-3. FUNCTION PORT CODES (SAC-COUPLER)



SECTION CODE (BITS 01 AND 02)

The section code defines the section within the SAC where the function is to be executed.

Bit 01	Bit 02	Section
0	0	SAC interchange
0	1	SAC storage channels
1	0	I/O device system control codes
1	1	Processor port/I/O channel

DIVISION CODE (BITS 03 THROUGH 05)

The division code defines the division within a specified section of the SAC where the function is to be executed. The divisions defined are as follows:

a. Storage channel within section

b. Processor port or I/O channel within section

c. Division within interchange section

d. Control codes sent to I/O devices

SUBDIVISION CODE (BITS 06 AND 08)

The subdivision code is used when sensing a processor port or I/O channel to specify whether to sense status, most significant half of address, least significant half of address, or channel/port address register.

Bit 06	Sense
0	MS half of address (A00 - A07)
1	LS half of address (A08 - A15)

Bit 08	Sense
0	Channel/port status
1	Channel/port address register

SAC BIT (BIT 07)

Since only one SAC is associated with the station, this bit should remain cleared.

EXECUTION CODE (BITS 08 THROUGH 15)

This code specifies the function to be executed. These codes are defined under the individual descriptions of set and sense status functions.

SAC SET FUNCTIONS

The following paragraphs describe the set status function codes for the SAC. The set functions are grouped according to the section code (bits 01 and 02), with each function within a group specified by the division code (bits 03 through 05).

SET INTERCHANGE STATUS

The interchange section of the SAC is specified by a section code of 00_2. A division code of 000_2 is illegal for the set interchange status functions. Table 3-4 lists the interchange set status function codes.

TABLE 3-4. INTERCHANGE SET FUNCTION CODES

Function	MSB 00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	LSB 15
Port/Channel Clear	1	0	0	0	0	1	0	0	0	0	0	0	PP0	IO2	IO1	IO0
Stop/Bkpt Clear	1	0	0	0	1	0	0	0	0	0	0	0	PP0	IO2	IO1	IO0
Stop Port/Channel	1	0	0	0	1	1	0	0	0	0	0	0	PP0	IO2	IO1	IO0
Disable Interchange Modes	1	0	0	1	0	0	0	0	0	0	0	0	P1 TGL	P0 TGL	STEP MODE	BKPT
Enable Interchange Modes	1	0	0	1	0	1	0	0	0	0	CYCLE STEP	0	P1 TGL	P0 TGL	STEP MODE	BKPT
Clear Storage Stop	1	0	0	1	1	0	0	0	0	0	0	0	BANK B(U)	BANK B(L)	BANK A(U)	BANK A(L)
Set Storage Stop	1	0	0	1	1	1	0	0	0	0	0	0	BANK B(U)	BANK B(L)	BANK A(U)	BANK A(L)

Port/Channel Clear (Code 001)

MSB															LSB
00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15
1	0	0	0	0	1	0	0	0	0	0	0	PP0	IO2	IO1	IO0

Function Description: This function clears the control logic in the specified port (PP0) or I/O channels (IO0-IO2). If the bit corresponding to the specified port/channel is present, the port/channel is cleared. If the bit is absent, the port/channel is unaltered.

Comments: Any number of the 4 bits (12-15) in the execution code may be present or absent. Before clearing a port/channel, a SAC function should be executed to send a SUSPEND (device system control code) to each device connected to the port/channel to be cleared. In addition, the port/channel to be cleared should first be stopped. Basically, this function should be used for channel initialization only.

Stop/Bkpt Clear (Code 010)

MSB															LSB
00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15
1	0	0	0	1	0	0	0	0	0	0	0	PP0	IO2	IO1	IO0

Function Description: This function clears the stopped set state and the breakpoint compare set state of the specified processor port (PP0) or I/O channels (IO0-IO2). If the bit corresponding to the specified port/channel is present, the port/channel is cleared. If the bit is absent, the conditions are unaltered.

Comments: Any number of the 4 bits (12-15) in the execution code may be present or absent. The specified port/channel should be cleared prior to clearing the stop or breakpoint compare.

Stop Port/Channel (Code 011)

MSB															LSB
00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15
1	0	0	0	1	1	0	0	0	0	0	0	PP0	IO2	IO1	IO0

Function Description: This function sets the specified processor port (PP0) or I/O channel (IO0-IO2) to the stopped state. If the bit corresponding to the specified port or channel is present, the port/channel is stopped. If the bit is absent, the port/channel is unaltered.

Comments: Any number of the 4 bits (12-15) in the execution code may be present or absent.

Disable Interchange Modes (Code 100)

MSB LSB

00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15
1	0	0	1	0	0	0	0	0	0	0	0	P1 TGL	P0TGL	STEP	BKPT

Function Description: This function disables (clears) address parity error generator P1 (P1 TGL), address parity error generator P0 (P0 TGL), step mode enabled (STEP), and breakpoint compare enabled (BKPT) if the corresponding bit is present. States are unaltered if the corresponding bit is absent.

Enable Interchange Modes (Code 101)

MSB LSB

00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15
1	0	0	1	0	1	0	0	0	0	C STEP	0	P1 TGL	P0 TGL	STEP	BKPT

Function Description: This function enables the modes of cycle step (C STEP), address error parity generator P1 (P1 TGL), address error parity generator P0 (P0 TGL), step mode enabled (STEP), and breakpoint compare (BKPT) if the corresponding bit is present. States are unaltered if corresponding bits are absent.

Comments:

a. Breakpoint Compare Enabled: When the interchange conditions compare with the breakpoint switch settings, the recognition of this occurrence is enabled.

b. Address Parity Error Generator P0: When enabled, the parity bit for address bits 00 through 07 is toggled at the interchange parity checker and a parity error is generated.

c. Address Parity Error Generator P1: When enabled, the parity bit for address bits 08 through 15 is toggled at the interchange parity checker and a parity error is generated.

d. Step Mode and Cycle Step: When the cycle step mode is enabled, the interchange can be stepped. When both the cycle step and step mode are enabled, only one memory request will be processed by the interchange. The cycle step is cleared by the interchange after processing the memory request. A function must be executed to enable the cycle step for each memory request processed when the step mode is enabled.

Clear Storage Stop (Code 110)

MSB LSB

00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15
1	0	0	1	1	0	0	0	0	0	0	0	BANK B(U)	BANK B(L)	BANK A(U)	BANK A(L)

Function Description: If corresponding bits (12 through 15) are present, this function will clear stopped storage banks. If the corresponding bit is absent, the stopped storage banks are unaltered.

Comments:

a. A and B indicate SAC storage channels A and B.

b. (U) indicates upper or second bank in a storage channel and is independent of address assignment.

c. (L) indicates lower or first bank in a storage channel and is independent of address assignment.

Set Storage Stop (Code 111)

MSB LSB

00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15
1	0	0	1	1	1	0	0	0	0	0	0	BANK B(U)	BANK B(L)	BANK A(U)	BANK A(L)

Function Description: If corresponding bits (12 through 15) are present, this function will stop any selected storage banks. If corresponding bit is absent, the banks are unaltered.

SET STORAGE STATUS (1.1 MICROSECOND MEMORY)

The storage channels of the SAC are specified by a section code of 01_2. Table 3-5 lists set storage status function codes. These codes are described in detail at the beginning of this section.

TABLE 3-5. SET STORAGE STATUS FUNCTION CODES

Function	MSB 00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	LSB 14
Set Ch A Bank Assignment	1	0	1	0	0	0	0	0	0	CSM CLR	BANK U(0)	BANK U(1)	BANK U(2)	BANK L(0)	BANK L(1)	BANK L(2)
Set Ch B Bank Assignment	1	0	1	0	1	0	0	0	0	CSM CLR	BANK U(0)	BANK U(1)	BANK U(2)	BANK L(0)	BANK L(1)	BANK L(2)

SET I/O DEVICE SYSTEM CONTROL CODES

Setting of the I/O device system control codes is specified by a section code of 10_2. Bits 04 and 05 of the division code specify the system control code. The execution code (bits 12 through 15) indicates whether the control code is sent to an I/O device or a device other than the PPU which may be connected to a processor port.

Set Control Code (Codes 000, 001, 010, 011)

MSB 00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	LSB 15
1	1	0	0	X	X	0	0	0	0	0	0	PP0	IO2	IO1	IO0

Function Description: This function sends the specified system control code (bits 04 and 05) to the selected processor port (PP0) or I/O channel device. If the bit corresponding to the specified port/channel is present, the code is sent to the device connected to the port/channel. No code is sent if the corresponding bit is absent.

Comments:

a. No SAC interchange time is required to process this function.

b. Table 3-6 lists the control codes which are sent by this function.

TABLE 3-6. I/O DEVICE SYSTEM CONTROL CODES

Control Code Bit		Code Signal Name	Function
04	05		
0	0	Invalid	This code defines a control strobe pulse which has not been followed by a control pulse.
0	1	Channel Flag	This code indicates that a message has been placed in the predefined message area.
1	0	External Flag	This code indicates that the I/O device should initiate a master clear and enter an autoload sequence.
1	1	Suspend	This code indicates that the I/O device should stop using the interface for any further transactions and go into a standby mode.

SET PORT/CHANNEL MEMORY PROTECT REGISTERS

The memory protect registers of the processor ports and I/O channels are specified by a section code of 11_2. Table 3-7 lists the function codes for setting these registers. The memory protection system is described later in this section.

TABLE 3-7. SET PORT/CHANNEL MEMORY PROTECT REGISTER FUNCTION CODES

	MSB															LSB
Port/Channel	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15
I/O 0	1	1	1	0	0	0	0	0	0	0	0	PRO BIT	MP (0)	MP (1)	MP (2)	MP (3)
I/O 1	1	1	1	0	0	1	0	0	0	0	0	PRO BIT	MP (0)	MP (1)	MP (2)	MP (3)
I/O 2	1	1	1	0	1	0	0	0	0	0	0	PRO BIT	MP (0)	MP (1)	MP (2)	MP (3)
PP 0	1	1	1	0	1	1	0	0	0	0	0	PRO BIT	MP (0)	MP (1)	MP (2)	MP (3)

SAC SENSE FUNCTIONS

The following paragraphs describe the sense function codes for the SAC. The sense functions are grouped according to the section code (bits 01 and 02) with each function within a group specified by the division code (bits 03 through 05). The sense function is specified by bit 00 being set to 0_2.

The sense function codes are encoded in the PPU and sent to the SAC function port via the coupler. The function specified is sensed by the PPU as a status word 1 bit after being sent from the SAC function port via the coupler.

SENSE INTERCHANGE STATUS

The interchange section of the SAC is specified by a section code of 00_2. Table 3-8 lists the interchange sense function codes and Table 3-9 lists the input channel sense status translations.

Interchange division codes of 000_2, 001_2, 100_2, and 101_2 are illegal.

TABLE 3-8. SENSE INTERCHANGE STATUS FUNCTION CODES

Function	MSB 00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	LSB 15
Sense Ports/Channels Stopped	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
Sense Breakpoint Compares	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0
Sense Storage Channels Stopped	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0
Sense Interchange Status Word	0	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0

TABLE 3-9. INTERCHANGE SENSE STATUS

Function Sensed	Function Port Bit Positions 08	09	10	11	12	13	14	15
Ports/Channels Stopped	1	1	1	1	PP0	IO2	IO1	IO0
Breakpoint Compares	1	1	1	1	PP0	IO2	IO1	IO0
Storage Channels Stopped	1	1	1	1	BANK B(U)	BANK B(L)	BANK A(U)	BANK A(L)
Interchange Status Word	BKPT ENBL	P/C STOP	BKPT COMP	WRT PRO	NON MEM	CSM PE	DATA PE	ADD PE

Sense Ports/Channels Stopped (Code 010)

MSB															LSB
00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15
0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0

Function Description: This function senses the processor port and I/O channels that are stopped. If the corresponding sense bit (function port output) is present, the port/channel is stopped. If the corresponding bit is absent, the port/channel is not stopped.

Comments: The status is sensed on function port bit positions 12 through 15 as described in Table 3-9.

Sense Breakpoint Compares (Code 011)

MSB															LSB
00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15
0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0

Function Description: This function senses the processor port and I/O channels that have recorded a breakpoint compare. If the corresponding sense bit (function port output) is present, a compare has occurred. If the corresponding bit is absent, no compare has occurred.

Comments: The status is sensed on function port bit positions 12 through 15 as described in Table 3-9.

Sense Storage Channels Stopped (Code 110)

MSB															LSB
00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15
0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0

Function Description: This function senses the status of the storage banks within a storage channel. If the corresponding sense bit (function port output) is present, the specified bank is stopped. If the corresponding bit is absent, the bank is not stopped.

Comments: The status is sensed on function port bit positions 12 through 15 as described in Table 3-9.

Sense Interchange Status Word (Code 111)

MSB															LSB
00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15
0	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0

Function Description: This function senses the conditions of the interchange status word (bits 09 through 15 of function port output). The status word is cleared by the hardware after it is sensed. The status word is defined as follows:

BIT 09	10	11	12	13	14	15
P/C STOP	BKPT COMP	WRT PRO	NON MEM	CSM PE	DATA PE	ADD PE

Table 3-10 lists the conditions which set (1 state) the bits of the status word. Bit 08 of this function indicates by its presence that the breakpoint compare system has been enabled (BKPT ENBL).

Whenever the SAC detects a malfunction, the corresponding bit in the status word is set (1 state) and a SAC Malfunction is sent to the coupler.

TABLE 3-10. INTERCHANGE STATUS WORD

Status Word Bit	Set Condition
P/C STOP	This bit is set whenever a port or I/O channel detects an error within itself. Once detected, the corresponding port/channel stop flip-flop is set.
BKPT COMP	This bit is set whenever a breakpoint compare occurs. (See Table 3-2.)
WRT PRO	This bit is set whenever an attempt is made to write into a protected area of memory.
NON MEM	This bit is set whenever a reference is made to nonexistent memory locations.
CSM PE	If a memory parity error is detected during a read operation, CSM PE is set.
DATA PE	If the SAC interchange detects a data parity error during a CSM memory request, the DATA PE bit is set.
ADD PE	If the SAC interchange detects an address parity error during a CSM memory request, the ADD PE bit is set.

Comments:

a. If an ADD PE, a DATA PE, a BKPT COMP with stop-on-compare enabled, a WRT PRO, or a NON MEM occur, the following will result:

   1. A SAC Malfunction is sent to the coupler.
   2. The specific condition is recorded.
   3. The port/channel is stopped.
   4. CSM write operations are forced to read operations.

b. If a BKPT COMP occurs with record-on-compare enabled, the condition is recorded and a SAC Malfunction is sent to the coupler.

c. If a CSM PE occurs, the condition is recorded, a SAC Malfunction is sent to the coupler, the storage bank from which the bad data was read is stopped, and the port/channel receiving the data is stopped.

d. If a P/C STOP occurs, the condition is recorded, the port/channel is stopped, and a SAC Malfunction is sent to the coupler.

SENSE STORAGE CHANNEL STATUS

The storage channels of the SAC are specified by a section code of 01_2. Table 3-11 lists the function codes for selecting a specific storage channel to be sensed and Table 3-12 lists the bit positions of status word 1 which define the bank assignment register settings of the selected channel.

This function senses the bank assignment register settings within each storage channel (bits 10 through 15) and a memory sequence error (MSE, bit 09).

TABLE 3-11. SENSE STORAGE CHANNELS FUNCTION CODES (CODES 000, 010)

Channel Selected	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15
Channel A	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
Channel B	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0

TABLE 3-12. STORAGE CHANNEL SENSE STATUS

Storage Channel Sensed	Function Port Bit Positions							
	08	09	10	11	12	13	14	15
Channel A	1	MSE	BANK U(0)	BANK U(1)	BANK U(2)	BANK L(0)	BANK L(1)	BANK L(2)
Channel B	1	MSE	BANK U(0)	BANK U(1)	BANK U(2)	BANK L(0)	BANK L(1)	BANK L(2)

NOTE

The I/O device system control codes are not sensed by SAC function. In addition, the interrupts which are sent by the I/O devices are not sensed by SAC function, but are merely routed through the SAC to the coupler.

SENSE PORT/CHANNEL ADDRESS REGISTER STATUS

The processor port and I/O channels of the SAC are specified by a section code of 11_2. To sense the status of the port/channel address registers, subdivision codes (bits 06 and 08) of 01_2 and 11_2 are used to specify which 8-bit byte of the address is to be sensed. 01_2 indicates the left-most byte (bits 00-07) and 11_2 indicates the right-most byte (bits 08-15). The division code specifies which port or channel will be sensed.

Table 3-13 lists the port/channel address register function codes and Table 3-14 lists the input channel sense status translations.

TABLE 3-13. SENSE PORT/CHANNEL ADDRESS REGISTER FUNCTION CODES

Address Register Selected	MSB 00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	LSB 15
I/O Channel 0 Bits 00-07	0	1	1	0	0	0	0	0	1	0	0	0	0	0	0	0
I/O Channel 1 Bits 00-07	0	1	1	0	0	1	0	0	1	0	0	0	0	0	0	0
I/O Channel 2 Bits 00-07	0	1	1	0	1	0	0	0	1	0	0	0	0	0	0	0
Processor Port 0 Bits 00-07	0	1	1	0	1	1	0	0	1	0	0	0	0	0	0	0
I/O Channel 0 Bits 08-15	0	1	1	0	0	0	1	0	1	0	0	0	0	0	0	0
I/O Channel 1 Bits 08-15	0	1	1	0	0	1	1	0	1	0	0	0	0	0	0	0
I/O Channel 2 Bits 08-15	0	1	1	0	1	0	1	0	1	0	0	0	0	0	0	0
Processor Port 0 Bits 08-15	0	1	1	0	1	1	1	0	1	0	0	0	0	0	0	0

TABLE 3-14. PORT/CHANNEL ADDRESS REGISTER SENSE STATUS

Port/Channel	Function Port Bit Positions							
	08	09	10	11	12	13	14	15
I/O Channel 0 Bits 00-07	A(00)	A(01)	A(02)	A(03)	A(04)	A(05)	A(06)	A(07)
I/O Channel 1 Bits 00-07	A(00)	A(01)	A(02)	A(03)	A(04)	A(05)	A(06)	A(07)
I/O Channel 2 Bits 00-07	A(00)	A(01)	A(02)	A(03)	A(04)	A(05)	A(06)	A(07)
Processor Port 0 Bits 00-07	A(00)	A(01)	A(02)	A(03)	A(04)	A(05)	A(06)	A(07)
I/O Channel 0 Bits 08-15	A(08)	A(09)	A(10)	A(11)	A(12)	A(13)	A(14)	A(15)
I/O Channel 1 Bits 08-15	A(08)	A(09)	A(10)	A(11)	A(12)	A(13)	A(14)	A(15)
I/O Channel 2 Bits 08-15	A(08)	A(09)	A(10)	A(11)	A(12)	A(13)	A(14)	A(15)
Processor Port 0 Bits 08-15	A(08)	A(09)	A(10)	A(11)	A(12)	A(13)	A(14)	A(15)

SENSE PORT/CHANNEL STATUS

The processor port and I/O channels of the SAC are specified by a section code of 11_2. The desired port/channel is selected by division codes 000_2 through 111_2. Bit 08 of the subdivision code (bits 06 and 08) is set to the 0 state which indicates a sense port/channel operation. A specific bit position of the port/channel memory protect register can be sensed with this function by specifying the desired bit position with bits 12 through 15 of the execution code. This allows selection of any one of the 16 bit positions of the register.

Table 3-15 lists the function codes for sensing the status of the processor port and I/O channels. Table 3-16 lists the input channel sense status codes received by the computer when a port/channel is selected. The input channel bits are defined as follows:

Bit Position	Function
08, 09, 10	FFB0, FFB1, and FFB2 indicate the last coded mode of operation sent to the I/O channel by the I/O device. REQ INT indicates that the selected processor port has an interchange request (CSC) present. WRITE INT indicates that the selected processor port has a legal write mode or legal destructive read mode present.

Bit Position	Function
	READ INT indicates that the selected processor port has a legal read mode present.
11	MP indicates that the memory protect register bit position specified by the sense function code bits 12 through 15 is set (MP = 1).
12	OOB (Out-Of-Bounds) indicates that the selected port/channel has attempted to make a memory reference in a protected area. This condition will stop the port. The I/O channel will be stopped if the operation is a write. The channel will not be stopped on a read and the condition can be cleared by re-function from the I/O device connected to the channel.
13	ILL (illegal) indicates that the port/channel has detected an illegal operation. Hardware will stop a port that has detected this condition, but will not stop an I/O channel. The I/O channel can clear this condition by a re-function from the I/O device connected to the channel.
14	FCTN PE indicates that a function parity error has occurred on a transmission from an I/O device. WRITE MODE indicates that a port is in a write mode.
15	DATA PE indicates that a data parity error has occurred on a transmission from an I/O device. READ MODE indicates that a port is in a read mode. If bits 14 and 15 are both present when sensing a port, the port is in a destructive read mode.

TABLE 3-15. SENSE PORT/CHANNEL STATUS FUNCTION CODES

Port/Channel Selected	MSB 00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	LSB 15
I/O Channel 0	0	1	1	0	0	0	0	0	0	0	0	0	MP (0)	MP (1)	MP (2)	MP (3)
I/O Channel 1	0	1	1	0	0	1	0	0	0	0	0	0	MP (0)	MP (1)	MP (2)	MP (3)
I/O Channel 2	0	1	1	0	1	0	0	0	0	0	0	0	MP (0)	MP (1)	MP (2)	MP (3)
Processor Port 0	0	1	1	0	1	1	0	0	0	0	0	0	MP (0)	MP (1)	MP (2)	MP (3)

TABLE 3-16. PORT/CHANNEL SENSE STATUS

Port/Channel Sensed	Function Port Bit Positions							
	08	09	10	11	12	13	14	15
I/O Channel 0	FFB0	FFB1	FFB2	MP	OOB	ILL	FCTN PE	DATA PE
I/O Channel 1	FFB0	FFB1	FFB2	MP	OOB	ILL	FCTN PE	DATA PE
I/O Channel 2	FFB0	FFB1	FFB2	MP	OOB	ILL	FCTN PE	DATA PE
Processor Port 0	REQ INT	WRITE INT	READ INT	MP	OOB	ILL	WRITE MODE	READ MODE

SAC I/O CHANNEL OPERATIONS

SAC I/O operations are based on the ready/resume principle. They consist of autoload, control, address, and data transfers between the I/O channels and I/O devices via a compatible trunk line. Each SAC I/O channel connects to one I/O device.

The control transfers provide the I/O device with a means of communicating with the station software. The address and data transfers provide the I/O device with a means of accessing the CSC 1.1 microsecond memory. The autoload function enables the I/O device to perform a remote autoload from the communications station.

Memory access and software communications functions operate asynchronously with respect to each other.

Each I/O device has one interrupt line. The SAC transmits interrupts received from the I/O devices to the PPU. The interrupts are transparent to the SAC and cannot be sensed by SAC functions.

ACCESS TO STORAGE

Address and data transfers between the I/O devices and the SAC I/O channels take place in multiples of 32-bit words, that is, two transfers of 16 bits each. The transfers are initiated by the device sending a request, a function code, and the first half of a 32-bit address (16 bits). After an accept signal is received from the channel, the device sends another request, a function code, and the second half of the address (16 bits). When the channel accepts the second half of the address, data is transferred. The direction of the data transfer is determined by the function code.

Figure 3-2 shows the signal lines used during storage access functions. Table 3-17 lists the functions and function codes transmitted to the SAC I/O channel by the I/O device.

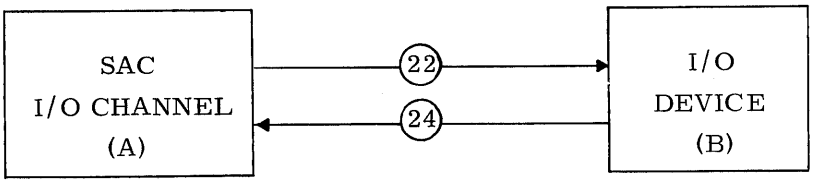
ADDRESS INCREMENT AND PARITY TOGGLE

Each 32-bit address from an I/O device accesses one 32-bit word in storage. Since the 1.1 microsecond memory stores 16-bit words (plus two parity bits), the SAC must address two 16-bit words for every 32-bit word address received from an I/O device.

Figure 3-3 shows how the address from the I/O device is incremented within the SAC interchange. The I/O channel address register uses the 15 least significant bits of the second address byte transferred from the device to form the 15 most significant bits of the address (bits 00 through 14) with bit 15 initially cleared (0 state). This address accesses the first 16-bit data word. The SAC interchange then increments bit 15 of the address and accesses the second 16-bit data word, thus supplying 32 data bits for each 32-bit word address.

The interchange increments the address by either a plus or minus one depending upon the function code specified (write or write reverse). Figure 3-4 shows address decrement during a reverse mode.

A parity toggle network within the interchange toggles the necessary parity bits of the current address to form the correct parity for the incremented address.



From A to B

Signal	Definition
DFA-00 - DFA-15	Data from A (16 lines)
DPFA-0, DPFA-1	Data parity from A (2 lines)
RFA	Request from A
AFA	Accept from A
PEFA	Parity error
IFA	Illegal from A

From B to A

DFB-00 - DFB-15	Data from B (16 lines)
DPFB-0, DPFB-1	Data parity from B (2 lines)
FFB0, FFB1, FFB2	Function code (3 lines)
FPFB	Function parity bit
RFB	Request from B
AFB	Accept from B

Figure 3-2. I/O Storage Access Signal Lines

TABLE 3-17. SAC I/O CHANNEL STORAGE ACCESS FUNCTION CODES

FFB0	FFB1	FFB2	Function	Operation
0	0	0	Null	This function is used to signify that the data lines contain the least significant half of an address or data.
0	0	1	Read	Read one word from the specified address.
0	1	0	Write	Write the data words which follow into consecutively increasing storage locations until a non-data word is received.
0	1	1	Destructive Read	Write all zeros into the specified address and then transmit the original contents of the specified address to the I/O device.
1	0	0	Data	This is a function code which is used to qualify the presence of the most significant half of a data word on the interface.
1	0	1	Block Read	Read from consecutively increasing addresses starting at the specified address until the I/O device sends a non-data function code.
1	1	0	Write Reverse	Write the data words which follow into consecutively decreasing addresses starting at the specified address until a non-data word is received.
1	1	1	End of Operation	This is a null operation which can be used to terminate a block read, write, or write reverse operation.

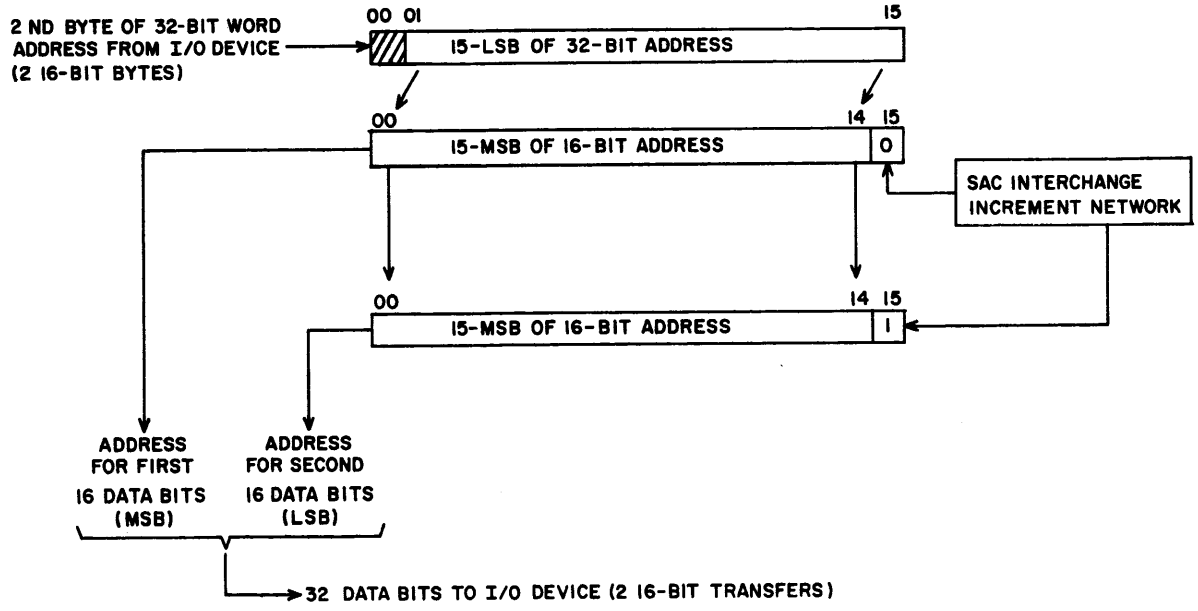


Figure 3-3. SAC I/O Channel Address Increment

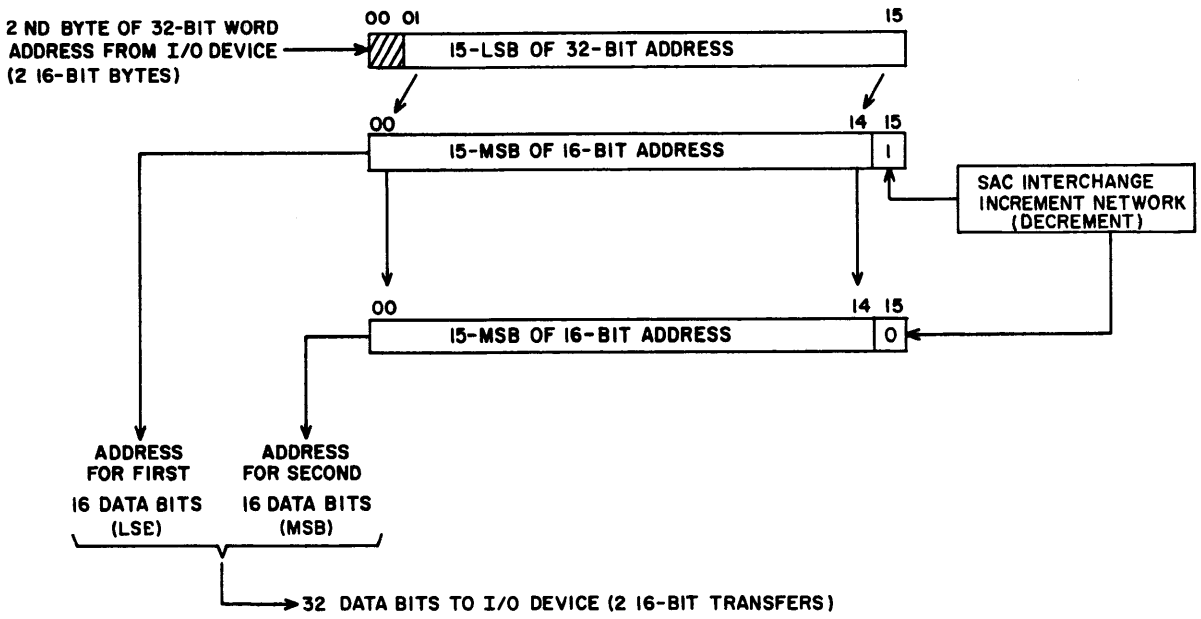


Figure 3-4. SAC I/O Channel Address Decrement

DATA ELEMENTS

The following elements are used to transfer data between the I/O channels and the I/O devices:

a. Address element

b. B to A data element

c. A to B data element

d. Final A to B data element

e. End-of-Operation (EOP) element

In order to perform a specific function (write, write reverse, read, destructive read, and block read), two or more of the elements are executed.

Address Element

This element is initiated by the I/O device with the following exchange of signals in the order listed:

a. RFB

b. Function Code (FFB0-FFB2)

c. First half of address (DFB-00 - DFB-15)

d. AFA

e. RFB

f. Null Function Code 000_2 (FFB0-FFB2)

g. Second half of address (DFB-00 - DFB-15)

h. AFA

The function codes specified by (b) include write, write reverse, read, destructive read, and block read. Table 3-17 lists the specific function codes.

B To A Data Element

This element is initiated by the I/O device with the following exchange of signals in the order listed:

a. RFB

b. Data Function Code 100_2 (FFB0-FFB2)

c. First half of data (DFB-00 - DFB-15)

d. AFA

e. RFB

f. Null Function Code 000_2 (FFB0-FFB2)

g. Second half of data (DFB-00 - DFB-15)

h. AFA

A To B Data Element

This element is initiated by the SAC with the following exchange of signals in the order listed:

a. RFA

b. First half of data (DFA-00 - DFA-15)

c. AFB

d. RFA

e. Second half of data (DFA-00 - DFA-15)

f. AFB

Final A To B Data Element

This element is initiated by the SAC as a final data transfer in a Block Read function. The exchange of signals is as follows:

a. RFA

b. First half of data (DFA-00 - DFA-15)

c. AFB

d. RFA

e. Second half of data (DFA-00 - DFA-15)

End Of Operation (EOP) Element

This element is initiated by the I/O device to signify the end of an operation. The exchange of signals is as follows:

a. RFB

b. EOP Function Code 111_2 (FFB0-FFB2)

c. Correct parity

d. AFA

e. RFB

f. Null Function Code 000_2 (FFB0-FFB2)

g. Correct parity

h. AFA

FUNCTION EXECUTION

In order to execute the function specified by the function code (Table 3-17), two or more of the data elements must be performed. The functions are as follows:

a. Write

b. Write Reverse

c. Read

d. Destructive Read

e. Block Read

Write Or Write Reverse

To execute these functions, the following elements are performed in the order listed:

a. Address element

b. B to A data element (repeated until total number of words are transferred)

c. Either address or EOP element

Read Or Destructive Read

To execute these functions, the following elements are performed in the order listed:

a. Address element

b. A to B data element

Block Read

To execute this function, the following elements are performed in the order listed:

a. Address element

b. A to B data element (repeated until total number of words are transferred)

c. Final A to B data element

d. Either address or EOP element

PARITY CHECKING

The I/O channel checks parity on all function code transfers from the I/O device and on all data transfers to and from the I/O device. Odd parity is used.

Function Code Checking

The I/O sends a function code (FFB0-FFB2) and a function parity bit (FPFB) to the I/O channel. The channel checks parity of the function code to determine if it is valid. If the channel detects a parity error, the I/O channel is stopped (not allowed to request storage) and a parity error signal (PEFA) is sent to the device. If additional requests are sent by the device (RFB), the channel replies with an accept (AFA) and an illegal signal (IFA). The channel can be re-enabled only by a SAC function code (refer to Table 3-3 for function coding information).

Data Parity Checking

The I/O channel checks parity on all data transfers with the I/O device. If a parity error is detected, the channel is stopped (not allowed to request storage) and a parity error (PEFA) is sent to the device.

If the channel is stopped and additional RFB or AFB signals are received, the internal status of the channel does not change. The channel replies to the RFB signal by sending an AFA and an IFA. The channel replies to the AFB by sending an RFA and an IFA.

The I/O channel sends the PEFA signal to the device during a read operation if a parity error is detected in the data read from the 1.1 microsecond memory.

No data or parity bits are transferred when a channel is stopped and only a SAC function code can re-enable the channel.

An address register of a stopped channel does not change, but contains the incremented memory reference address.

OUT-OF-BOUNDS MEMORY REFERENCE

If an I/O device attempts to reference an area in memory that is protected, the condition is flagged as out-of-bounds (OOB).

If the reference is for a write operation, the channel is stopped. The channel responds to requests from the device by sending an accept (AFA) and an illegal (IFA) signal. The channel can be re-enabled only by a SAC function code.

If the reference is for a read operation, the channel is not stopped and the channel responds to the device by sending a request (RFA) and an illegal (IFA). Once the out-of-bounds condition has been sensed by the SAC, no meaningful data is sent to the I/O device. The device can restore normal operation by initiating a new function code and legal address.

Nonexistent Memory

Under normal conditions, the software will not reference areas in memory which do not exist. However, should this condition occur, the I/O channel will be stopped and the channel will respond to the I/O device by sending either an AFA or RFA signal and an illegal (IFA).

Illegal Data Elements

If an I/O device sends a data element other than those described under data elements in this section, the I/O channel responds with an accept signal and an illegal (IFA). The channel is not stopped; however, no data is transferred until the device sends a correct element.

I/O Channel Status Sensing

The SAC function codes used to sense the status of an I/O channel are listed in Table 3-15. If the status of a channel is sensed when the channel is stopped, the conditions of the channel prior to the stop are truly reflected. If the channel is not stopped, the setting of the status bits are asynchronous to the sense function. Therefore, the sense bits do not truly reflect the present status of the channel.

I/O Channel Priorities

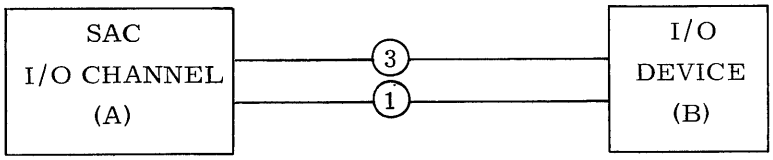
The SAC interchange interconnects the SAC I/O channels with the SAC storage channels. When more than one I/O device requests storage at the same time, the SAC executes one request according to predetermined priorities. These priorities are listed in Table 3-1.

I/O COMMUNICATION WITH SOFTWARE

In performing its function, an I/O device accesses the 1.1 microsecond memory independently of software operations within the communications station, but under the control of the PPU.

During certain operations, the station and the device must coordinate functions in order to signal tasks to be performed or to indicate tasks completed. The following paragraphs describe the functions used in order to communicate with the station software.

Figure 3-5 shows the signal lines used during software communication functions.



From A to B

Signal	Definition
CSFA	Control Strobe from A
CFA-0, CFA-1	Control code (2 lines)

From B to A

IFB	Interrupt from B

Figure 3-5. Software Communication Signal Lines

The system control codes are transmitted to the I/O device via the compatible trunk. The codes are listed in Table 3-6. The system control codes cannot be sensed by SAC functions.

CONTROL CODES

The control codes are transmitted to the I/O device by sending a control strobe (CSFA) to the device followed by the code. The control strobe is generated within the SAC whenever it receives a control code from the PPU.

Invalid (00)

This code indicates that a malfunction has occurred in the control transmission. The I/O device must assume that a suspend code was intended and generate an interrupt to inform the PPU of the malfunction.

Channel Flag (01)

This code informs the I/O device that a message concerning normal communications from the system software has been placed in the prearranged area in memory.

External Flag (10)

This code informs the I/O device to master clear and enter an autoload sequence.

Suspend (11)

This code informs the I/O device to stop using the data channel and enter a standby mode. If the next transmission from the I/O channel is a channel flag, then take normal action. If the next transmission from the channel is a data word, then interpret it as a command.

INTERRUPT

Communication from the I/O device to the PPU is achieved by the device placing a message in the prearranged area in memory and then sending an interrupt (IFB) to the I/O channel. The interrupt is transparent to the SAC and is passed on to the PPU.

Any action taken by the PPU when the interrupt is set, is a function of the system software.

AUTOLOAD

An I/O device can perform a remote autoload from the station. This is accomplished by the PPU sending a channel flag control code to the device. This code initializes the autoload function within the I/O device. Once the remote autoload sequence has been initialized, the device performs a block read as described previously in this section. The total number of words transferred during this function are determined by the hardware and software of the I/O device.

PROCESSOR PORT ERROR DETECTION AND RECOVERY

The processor port checks for legal sequences of the read (RED) and write (WRT) signals from the PPU. Upon detecting an illegal condition, the port drops the read and/or write signals to the interchange, sets itself to a stopped state, and sends an accept (AFA) and an error (ERR) to the PPU. The port doesn't check parity, but utilizes the interchange parity checkers. When the interchange detects a parity error on the data read from memory, it gives the port an indicator with the data. The port, in turn, sends an AFA followed by data (DFA), data parity (DPFA), and ERR, and sets itself to the stopped state. The interchange, when processing the port's memory request, may set the port to a stopped state or give a memory protect signal at the time it gives an interchange accept. In either case, an AFA and an ERR is sent to the PPU. The memory protect condition causes the port to set itself to the stopped state.

Once the port is set to a stopped state, this condition can be removed (port re-enabled) only via SAC function. If the port was stopped due to an illegal sequence or due to a memory

reference into a protected area, the port must be cleared by a $880X_{16}$ function (Table 3-3) to remove this status in the port and to ensure proper initialization before the port is re-enabled. It is a hardware requirement that the port be in the stopped state during the execution of a $880X_{16}$ function.

MEMORY PROTECTION

Each SAC processor port and I/O channel has a 16-bit memory protect register. When the bit positions within the register are set (1 state), a unique 4K block of address locations within the 1.1 microsecond memory are protected. If a memory reference is made to a protected area, the port or channel making the reference will be stopped, the condition logged, and a SAC Malfunction will be sent to the PPU via the coupler. This condition can be sensed via software. The memory protect register bit positions and protected memory locations are as follows:

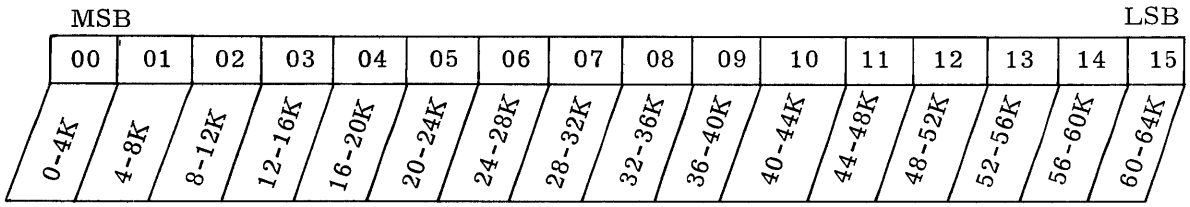


Table 3-7 lists the codes for setting the memory protect register bits. Each bit within the register is specified by a 4-bit code (MP (0)-MP (3)). The specified bit will be set to a 1 if bit 11 (PRO BIT) of the output channel is set (1 state). Table 3-18 lists the translations for the execution codes listed in Table 3-7.

NOTE

Since the maximum CSC memory configuration is 32K, only memory protect register bits 00-07 should be used.

TABLE 3-18. MEMORY PROTECT EXECUTION CODES

MSB			LSB	Memory Protect Register Bit
MP (0)	MP (1)	MP (2)	MP (3)	
0	0	0	0	00
0	0	0	1	01
0	0	1	0	02
0	0	1	1	03
0	1	0	0	04
0	1	0	1	05
0	1	1	0	06
0	1	1	1	07
1	0	0	0	08
1	0	0	1	09
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14
1	1	1	1	15

The bit positions of the memory protect registers are sensed by SAC function codes. Table 3-15 lists required encoding for selecting a desired bit position on a port/channel and Table 3-16 lists the sense status information.

SAC/CSC INITIALIZATION

The following initialization procedures should be accomplished upon powering up of the SAC and prior to attempting a CSM reference:

1. Configure all memory address banks and place them in the desired stop state.
2. Clear the CSM's.
3. Set/clear the memory protect registers.
4. Stop the I/O channels and processor port and clear their control logic.
5. Sense the interchange word via a $1C00_{16}$ function (Table 3-3) such that it is initially cleared.

6. Place the interchange modes in the desired state via $900X_{16}$ and $94XX_{16}$ functions (Table 3-3).

7. Clear the stopped state on the desired I/O channels and/or port.

NOTE

A hardware lockout disables CSM references upon powering up to keep any random CSM references from occurring until SAC is initialized. The execution of the $900X_{16}$ function disables this lockout feature and allows CSM requests to be made after powering up.

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