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**CONTROL DATA®  
1700 SYSTEM  
MAINTENANCE MONITOR**

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Volume 3 of 3

**REFERENCE MANUAL**

## REVISION RECORD

REVISION	DESCRIPTION
01 (05-13-66)	Original Printing, preliminary edition.
02 (08-08-66)	Publications Change Order 14307. Reprint with revision which obsoletes all previous editions. Tests were updated and the following new tests were added: 1711/1712 Teletype, 1729 Card Reader, 1731 Magnetic Tape, 1706/1716 Buffered Data Channel and Coupling, Random Protect, 1700 SMM Edit Routine, and Enter Program.
A (05-01-67)	Manual released. Publication Change Order 16368. The following new tests are added: 0B (1718 Satellite Coupler Test), 0C (1742 Line Printer Test), and 3D (Enter Program). Other tests were extensively revised and updated. This edition obsoletes all previous editions.
B (09-14-67)	Publication Change Order 17146. To revise existing tests and add new tests. Introduction: page 5 revised. Description: pages 7, 12, 15, 18, 25, 26, 27, 30 and 35 revised. Pages 30-a and 30-b added. Tests: pages 90-1, 90-2, 100-7, 100-8, 100-10, 101-2, 101-7, 202-1, 202-7, 205-2, 206-6 thru 206-10, 207-3, 208-2 and 208-6 revised. Page 100-8a added. Tests sections: 102, 201, 203, 212, 213, and 214 added. Sections 102 Rev A, 201 Rev A and 203 Rev A removed.
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D (06-11-68)	Publications Change Order 19818, to make miscellaneous publication corrections. Pages 37, 100-2, 100-18, 101-9, 102-7, 200-10, 201-6, 202-9, 203-7, 204-1, 204-12, 205-14, 206-9, 206-10, 207-4, 208-21, 210-4, 210-6, 211-13, and 215-23 revised. Pages 207-5 and 212-24 added.
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H (12-15-70)	Manuals revised. This publication is complete through Ed. 2.3. All previous editions are obsolete.
J (02-05-73)	Manuals revised. New tests are added and minor corrections are made. This publication is complete through Ed. 3.0.
K (09-20-73)	Manuals revised. Tests are added, deleted, and corrected.
L (02-01-74)	Manuals revised. Tests are added, deleted, and corrected. This publication is complete through Edition 3.1.
M (12-10-74)	Manuals revised. Tests are added and corrected. This publication is complete through Edition 3.1-1.
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or use Comment Sheet in the back of this manual.





# LIST OF EFFECTIVE PAGES

New features, as well as changes, deletions, and additions to information in this manual, are indicated by bars in the margins or by a dot near the page number if the entire page is affected. A bar by the page number indicates pagination rather than content has changed.

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## PREFACE

This manual is intended to serve as a reference aid for field and checkout personnel involved in the running of the CONTROL DATA® 1700 System Maintenance Monitor (SMM17).

This manual contains a detailed description of the operation and use of the monitor, instructions for the operator, restrictions, and necessary parameters. Detailed test descriptions are also included.

If information is required concerning the SMM17 QSE library, refer to SMM17 QSE Reference Manual, publication no. 60454710.





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1743-2 Asynchronous Communications Controller Test	ACC	86	II	707-1

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1700 Hardware Floating Point Unit Diagnostic	HFP	8A	II	852-1



## 1718 SATELLITE COUPLER TEST

(SC1A0B Test No. 0B)

### I. OPERATING INSTRUCTIONS

#### A. RESTRICTIONS

1. Test SC1 on the 3000 or 6000 side should be called first.
2. No other 1700 test may be run with this test. This test does not return control to the monitor.
3. Bit 5 in the SMM parameter word must be set.

#### B. LOADING PROCEDURE

This program is called as test number 0B via SMM17. The 3000 or 6000 side is called as SC1 via the SMM3L or SMM6X, respectively. The 3000 or 6000 is the master and should be called first.

#### C. PARAMETERS

##### 1. First stop

A = Test ID word (0B21)

Q = Test Stop/Jump parameter

Selective stops and jumps

Bit 0 - Parameter word (no typeout occurs)

Bit 1 - End of section (no typeouts)

Bit 2 - End of pass through test (typeout unless bit 8 is set)

Bit 3 - Error stop (typeout unless bit 8 set)

Bit 4 - Repeat conditions

Bits 5, 6, 7 - Not used

Bit 8 - No typeouts

Bit 9 - Return address corresponds to memory location rather than program listing

Bit 11 - Selects shift cable option (Set this bit when using a special data cable which is wired to shift the data cable bits left by 4 bits. When running with this option character mode is disabled.)

##### 2. Second Stop

A = Interrupt line

If bit 0 of the Stop/Jump parameter word is set, a Stop occurs with bit 6 in the A register set. This bit specifies interrupt line 6. If

the 1718 uses a different interrupt line, the operator must clear the A register, set the bit corresponding to the correct interrupt line, and run.

Q = 6000 flag

Bit 15 = 1 (6000 system)

Bit 15 = 0 (3000 system)

Sections can be selected only on the master side, the 3000 or 6000 Series Computer.

#### D. MESSAGES

##### 1. Normal Messages

- a. SC1A0B, 1718 SATELLITE COUPLER TEST 1A = XXXX, FC = XX.

Start of test. Initial address is XXXX, frequency count is XX.

- b. PROTECT STATUS SET

The Protect switch on the 1718 is set according to the status.

- c. 0B24 XXXX 00YY ZZZZ

End of test. 0B is the test number. 2 is the number of stops, if any, and the number of pairs of words typed. 4 (bit 2) is the type of stop (End of Test stop) which occurs if bit 2 of the Stop/Jump parameter word is set.

XXXX is the Stop/Jump parameter.

00YY - YY is the pass number.

ZZZZ is the return address. This is relative to the initial address (program listing) of the test unless bit 9 of the Stop/Jump parameter is set, in which case ZZZZ is the memory location.

##### 2. Error Messages

- a. Errors

All error typeouts are prefixed by 0BV8 XXXXX 0SYZ ZZZZ. 0B is the test number.

V is the number of stops (if any), or the number of pairs of words to be typed.

8 (bit 3) is the type of stop (Error stop) which will occur if bit 3 of the Stop/Jump parameter word is set.

S is the section number.

YY is the error code.

ZZZZ is the return address.

If V = 2, there is no error typeout suffix.

If V = 3, there is a suffix depending on the error code.



b. Error Codes

- 01 - Insufficient core for test
- 02 - Equipment address in error. Start over.
- 03 - Interrupt line selection in error. Start over.
- 04 - Internal reject of status input
- 05 - Internal reject of select
- 06 - Internal reject of AQ channel input or internal reject of direct input to BDC channel
- 07 - Internal reject of AQ channel output or internal reject of direct output from BDC channel
- 08 - Not used
- 09 - Not used
- 0A - Unexpected status.

A = actual status, Q = expected status.

- 0B - Data error after read.

A = actual data, Q = expected data.

After a data error is found, no more data checking is performed for that input unless bit 4 (repeat conditions) of the Stop/Jump parameter is set.

- 0C - Alarm interrupt, division A channel parity error

A = Status upon interrupt

Q = Selected interrupts

Bit 2 of Q set - Data

Bit 3 of Q set - End of Operation

Bit 4 of Q set - Alarm

- 0D - Alarm interrupt, division A computer inactive

A and Q same as for error 0C

- 0E - Interrupt status bit not set when interrupt occurred

A and Q same as for error 0C

- 0F - Non-selected interrupt occurred

A and Q same as for error 0C

- 10 - Flag interrupt did not occur when expected

A = current status

Q = current 1718 mask, 1700 side

- 11 - Not used

- 12 - Non terminating buffer occurred
- 13 - End of Operation status set before other computer

Write status is clear during Direct Read

- 14 - Not used
- 15 - Unexpected number of words read

A = actual word count

Q = expected word count

- 16 - No End of Operation interrupt during Read
- 17 - No End of Operation interrupt during Write.

### 3. Error Stops

Error stops occur if bit 3 of the Stop/Jump parameter is set. Error typeouts occur unless bit 8 of the Stop/Jump parameter is set. At error stops, the contents of the A and Q registers are the same as the typeout.

## II. DESCRIPTION

### A. GENERAL

1. The test is divided into three sections, selectable on the 3000 or 6000 (master) side. These are Flag/Status section, Write/Read section, Mask/Interrupt section.
2. Each operational check is performed first from the 3000 or 6000 side to the 1700, then from the 1700 to the 3000 or 6000 side.
3. Each operational check is repeated 64 times.

### B. DESCRIPTION OF TEST SECTIONS

#### 1. Preliminary

Because flags 6 and 7 are used for communication, these flags are checked by each side prior to entering Section 1.

#### 2. Section 1- Flag/Status Test

- a. Set all flags and check flags.
- b. Set individual flags and check.
- c. Set all but one flag and check.
- d. Clear individual flags and check.
- e. Clear all but one flag and check.

- f. Clear flags, check other computer Write/Read "1's", check for flags clear.
  - g. Set flags, check other computer Read/Write "0's", check for all flags set.
3. Section 2, Write/Read Test
- a. Check other computer Write/Read.
  - b. Check other computer Read/Write.
  - c. Read and check data, Write.
  - d. Repeat c for lengths of 4, 32, 256 words.
  - e. Repeat c and d for each of seven patterns.
  - f. Read random lengths of random pattern. Check data.
  - g. Repeat f.

In Sections 1 and 2, reads and writes are not in Interrupt mode except for some of the random length reads. The buffered reads of random length are executed in Interrupt mode. Buffered and Direct mode for reads and writes are selected at random. Character and Word mode for reads and writes are selected at random. Reads and writes in section 3 are in Interrupt mode. Alarm and End of Operation interrupts are selected for reads and writes in Interrupt mode. Also, Data interrupt is selected for reads and writes in Interrupt mode, but not in Buffered mode.

4. Section 3, Mask/Interrupt Test
- a. Clear all flags, set all masks, expect no interrupts
  - b. Set all flags, set individual masks, expect interrupts
  - c. Set individual flags, set corresponding masks, expect interrupts.
  - d. Set all but one flag, each flag. Set mask for flag not set. Expect no interrupt.
  - e. Set individual flags. Set masks except flag set. Expect no interrupts.
  - f. Read in Interrupt mode.
  - g. Write in Interrupt mode.

### III. PHYSICAL REQUIREMENTS

- A. SPACE REQUIRED - About 2600<sub>10</sub> locations
- B. TEMPORARY STORAGE - Current status of the 1718 is stored at memory location \$DD<sub>16</sub>.

C. PATTERNS

1. 000 (all "0's")
2. FFF (all "1's")
3. 000 FFF (all "0's", all "1's" alternate)
4. 555 AAA ("0", "1"; "1", "0")
5. F11 88F 47C 3E2 (3-bit end-around left shift)
6. F19 8CF 67C 3E3 (3-bit end-around left shift)
7. F11 0EE 88F 770 (complement, complement-shift) 47C B83 3E2 C1D
8. Random (word N+1 = word n + addend, first word random 12-bit number, addend random 12-bit number, 12 bit end-around carry addition used)

D. TIMING - About 4 minutes for all three sections.

E. EQUIPMENT CONFIGURATION

1. 17X4 Computer with 8K memory
2. 1705 Interrupt Data Channel
3. 1706 Buffer Data Channel (optional)
4. 1718 Satellite Coupler
5. 3000 or 6000 Series Computer with one data channel.
6. A device for loading program.

## DSC 1700 DATA SET CONTROLLER

(DSCA11 Test No. 11)

### I. OPERATIONAL PROCEDURE

#### A. RESTRICTIONS

1. Test must be run with 6X00/6675 Data Set Controller Test (6000 → RT3).
2. Operator must make section selections, and stop/jump options correspond to those of the 6X00 operator.
3. Test must be loaded first (it does not return control to SMM after an I/O operation).
4. This test MUST be started before the 6675 test is initiated.

#### B. LOADING PROCEDURE

1. Loads under SMM17
2. Test mnemonic DSC
3. Test number 11

#### C. PARAMETERS

Parameter selection follows standard 1700 SMM format. Bit 11 of the stop/jump parameter word must be set for Input/Output from A mode; if not set, test runs in Buffer mode. The test parameter stops for section selection in A (preset to 000F) and interrupt mask in Q (preset to 0000). To set the interrupt mask parameter, the bit in Q matching the interrupt line should be set to "1" (i. e. bit 5 for interrupt line 5). For a normal run, the Stop at End of Section parameter bit should not be set.

#### D. MESSAGES

1. Normal Messages

DSCA11, 1700 DATA SET CONTROLLER TEST IA = XXXX, FC = XX
---

This message is typed at the beginning of the test. All other typeouts appear in standard SMM17 format.

## 2. Error Codes

- 01 Unidentified interrupt
- 02 Either an expected interrupt did not occur or an unexpected interrupt did occur  
A = actual status  
Q = expected status
- 03 Either an expected status is not present or an unexpected status is present  
A = actual status  
Q = expected status
- 04 Data compare error between data sent and data received. If more than  $10_{16}$  errors occur or the errors occur in section 5, then  
A = number of errors  
Q = pattern number
- 05 Cyclic code from the remote controller does not compare with the cyclic code generated.
- 06 Internal reject on an I/O attempt. (Repeats attempt following error display)
- 07 Interrupt status bit is set following a Clear Interrupt function
- 08 W of the equipment code is not 0, 02, 07, or 0C.
- 09 Sync Word Not Acknowledged status bit is in error. Following a select transmit, the status bit should be set, if not, the program records the error and proceeds to attempt the output. If the status bit is not down, the output is attempted  $20_{16}$  more times before the error is reported.
- 13 Insufficient memory for test
- 14 Status after an input operation does not compare with the expected status (see error code 3).

1748-2 MULTIPLEXER CONTROLLER, CSPL COMMUNICATIONS ADAPTER  
(MCCA48 Test No. 48)

I. IDENTIFICATION

A. EQUIPMENT TESTED

1748-2 Multiplexer Controller (MC)  
DJ808A Communications Multiplexer (MUMOD) - 364-1,2  
DJ813A Communications Multiplexer (MUMIX) - 364-3  
DJ144A Synchronous Communication Adapter (SCA-1) - 361-5  
DJ145A Synchronous Communication Adapter (SCA-2) - 361-6  
DJ122A Asynchronous Communication Adapter (ACA-1) - 361-4  
DJ142A, DJ143A Communication Adapter (SACA) - 361-1

II. INTRODUCTION

The 1748-2 MC CSPL Diagnostic Program checks the function, status, and data handling capabilities of the multiplexer controller, communication multiplexers, and communication adapters (SCA-1, SCA-2, ACA, and SACA) through the use of individually selectable sections. Up to 512 single address communication adapters (CAs) or any combination of single and dual address CAs, not to exceed 512 addresses, may be tested at one time.

III. REQUIREMENTS

A. HARDWARE

1748-2 Multiplexer Controller (MC)  
DJ808A Communication Multiplexer (MUMOD)  
DJ813A Communication Multiplexer (MUMIX)  
DJ144A, DJ145A Synchronous Communications  
Adapter (SCA-1, SCA-2)  
DJ122A Asynchronous Communication Adapter (ACA)  
DJ142A, DJ143A Communication Adapter (SACA)

(See Figure 1)

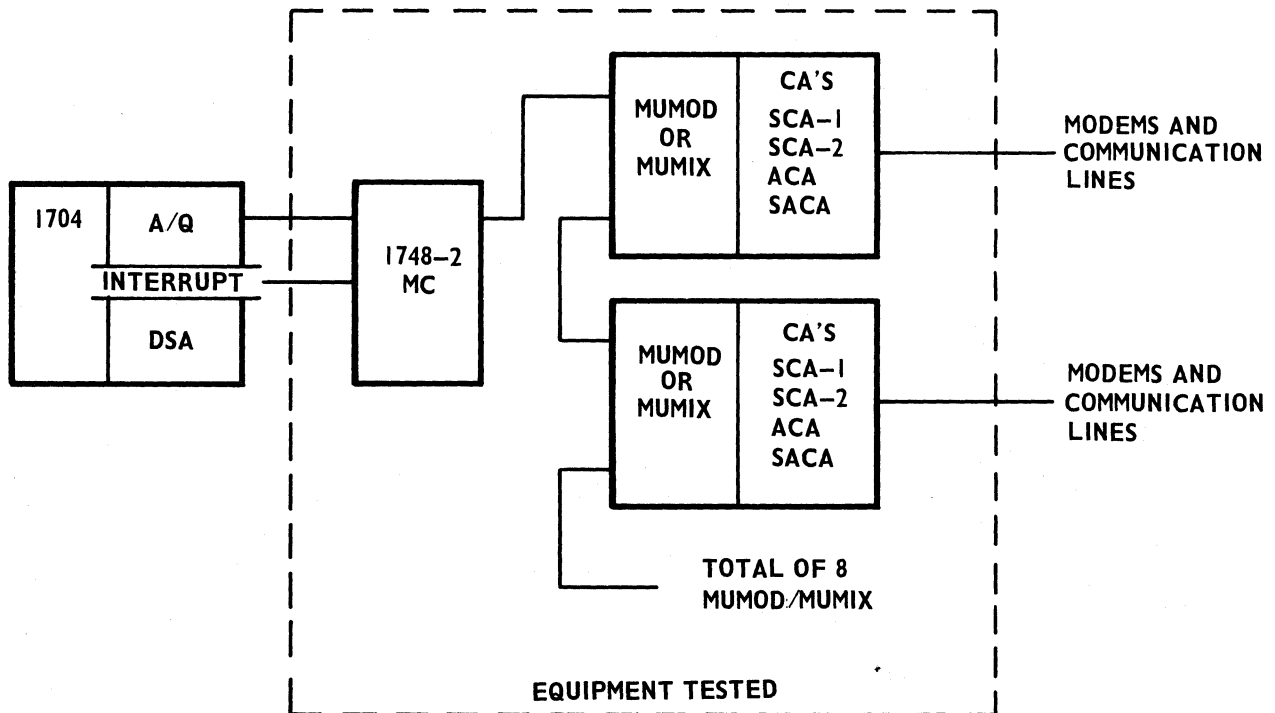


Figure 1.



## B. SOFTWARE

The 1748-2 MC CSPL Diagnostic Program operates under the SMM17 Diagnostic Monitor as a type 7 test.

## C. ACCESSORIES

No special accessories are required for test execution.

## IV. LIMITATIONS

A. Due to the limited computer hardware and time, the test is not capable of the following:

1. Testing the DJ146A (ACUCA).
2. DSA test.
3. Generating a Character Lost interrupt (bit 09), and parity (bit 08).
4. Transparent mode.
5. SACA Set and Clear Break test.

B. The following equipment is the only CSPL hardware on which the test has been executed.

1. Three DJ808A's (MUMOD)
2. Sixteen DJ142's (SACA)
3. Four DJ144A's (SCA-1)
4. Four DJ145A's (SCA-2)
5. One DJ122A's (ACA)

All of the above equipments have been simultaneously tested by this diagnostic.

C. When selecting pluggable options on the asynchronous communication adapter, the send clock rate and bit level must equal the receive clock rate and bit level.

D. When testing synchronous communication adapters, a data set or equivalent must be connected to the CA. The following data sets and their equivalents are compatible.

1. Data Sets 201-A/B
2. Data Sets X203-A
3. Data Set 303

- E. The single address communication adapter (SACA) must be placed in the echo mode before testing.
- F. Run in 32K mode only when using 1714.
- G. Prestoring Parameters - The parameters for the DJ808/813 can only be prestored in this test using edit Prestored Parameters feature. The parameter A6, Q6, however, cannot be effectively prestored.

The CA parameters may be prestored using Program Modification feature in edit for a maximum of 14 CA's.

## V. OPERATIONAL PROCEDURE

### A. LOADING PROCEDURE

1. Load the SMM17 library.
2. The computer will halt with the Overflow light lit. Set the A register equal to the desired SMM parameter word configuration (for normal operation, set bits 4 and 5 and the appropriate loader designation bit). Set the Q register equal to the desired SMM Stop/Jump parameter configuration and place the STEP/RUN switch in the Run position.
3. When the computer stops, set the A register to the desired SMM ID word configuration with the upper eight bits equal to 48. Set the Q register bits 7 through 10 equal to the 1748-2 MC equipment number and set bit 0. Place the SELECTIVE SKIP switch in the Off position. Place the STEP/RUN switch in the Run position.
4. The typewriter will type:  
MCCA48, 1748-2 MC CSPL DIAGNOSTIC - TEST. VRS. 3.1  
IA = XXXX. FC = XXXX CP 03
5. The computer will halt with the Overflow light lit. The A register will contain the test ID word and the Q register will contain the Stop/Jump word. The Stop/Jump parameter word in the Q register may be changed at this time if desired. No change is required for normal operation of the program.
6. The following stops will be parameter stops necessary for test execution.

#### NOTE

If only function tests are to be run, it is necessary to enter parameters for at least one CA, even though there is no CA to test (in the multiplexer rack).

Address 001 is sent to the 1748-2 MC along with a Set CA Address Register function. The 1748-2 is checked for Busy status. A Clear CA Address Register function is issued to the 1748-2 MC and status is checked for Not Busy. Any unexpected status, interrupt or reject will result in an error.

34. Subtest 44 - Word Mode Interrupt

This 1748-2 MC function test checks operation of the Word Mode Interrupt. Start Scan and Start Word Mode Interrupt functions are issued to the 1748-2 MC. If periodic Word Mode Interrupts are not received from the 1748-2 MC, an error is reported. If the interrupts are received, Stop Scan and Stop Word Mode Interrupt functions are issued to the 1748-2 MC. No further Word Mode Interrupts should be received. Any reject, unexpected status or unexpected interrupt, will result in an error.

35. Subtest 45 - End of Operation Interrupt

This 1748-2 MC function test verifies operation of the scanner and checks the End of Operation Interrupt. The scanner is started and the CA Address register is cleared. CA address 000 is issued and the 1748-2 MC is checked for Busy status and End of Operation Interrupt. If the interrupt is not received and/or the Busy status does not clear, an error is reported. If the End of Operation interrupt is received and the 1748-2 MC goes Not Busy, the CA address equal to the maximum scan setting is issued. The maximum scan setting is a parameter received during parameter entry which indicates the last or highest CA address to be generated by the 1748-2 MC and expansion network (MUMOD's and/or MUMIX's). If an End of Operation interrupt is not received and/or Busy status does not drop, an error is reported. Any reject, unexpected status or unexpected interrupt, will result in an error report.

36. Subtest 46 - Scan Failure Interrupt

This 1748-2 MC function test checks the Scan Failure this Unit Interrupt. Status is first checked for Not Scanning other Unit Set. The scanner is started and status is checked for bit 4 clear (Scan Failure this Unit). The scanner is stopped, a Scan Failure Interrupt this Unit is expected, error code 57 is reported if not received. Any unexpected interrupt, unexpected status, or reject will also result in an error.

37. Subtest 47 - Busy Check

This 1748-2 MC function test verifies operation of the Busy status. The CA Address register is cleared, CA address 000 is issued, and the 1748-2 MC is checked for Busy status. If Busy the CA Address register is cleared and the 1748-2 MC is checked for Not Busy. CA address 000 is issued again and Busy is checked. The scanner is then started, CA address equal to the Maximum Scan setting plus one is issued to the 1748-2 MC and Busy is checked. If the 1748-2 MC remains Busy, the CA Address register is cleared and Not Busy status is checked. Any reject, unexpected status, unexpected interrupt, or any variation from the expected will result in an error.

38. Subtest 48 - Program Protect Fault

This 1748-2 MC function test checks the Program Protect Fault Status bit. It is assumed that the 1748-2 MC and the console PROGRAM PROTECT switch is in the OFF or UNPROTECTED position. The test will issue three clear Interrupt and Status functions with the program protect bit clear and then three clear Interrupt and Status functions with the program protect bit set. With the PROGRAM PROTECT switch OFF, no Program Protect faults should be detected. This test may be selected by itself and run with the 1748-2 MC and the console PROGRAM PROTECT switch ON. In this situation three SMM 02 errors should be generated for the three unprotected Clear Interrupt and Status functions. Any unexpected status, unexpected interrupt, or reject will also result in an error.

NOTE

If SLS is set, a stop will be performed at the location Program Protect was detected. If SLS is left off, this stop will not occur and SMM will display the error.

39. Subtest 49 - Single Scan, Dual Scan

This 1748-2 MC function test verifies operation of the Single Scan and Dual Scan functions in a communications system operating in the single scan mode. Single Scan functions and Dual Scan functions are issued to the 1748-2 MC. It is assumed the DMU is not connected to the 1748, an external reject will then be expected on Dual Scan function. Any unexpected status, unexpected interrupt, or reject will also result in an error.

2. Core Requirements

The minimum amount of core required is 8K.

3. Peripheral Requirements

One standard SMM17 input device

- 1721/1722 Paper Tape Reader
- 1728/1729 Card Reader Controller
- 1726 Card Reader (405) Controller
- 1712/1713 Teletypewriter
- 1731/1732 Magnetic Tape Controller
- 1738 Disk Pack Controller
- 8000 Tape Drives

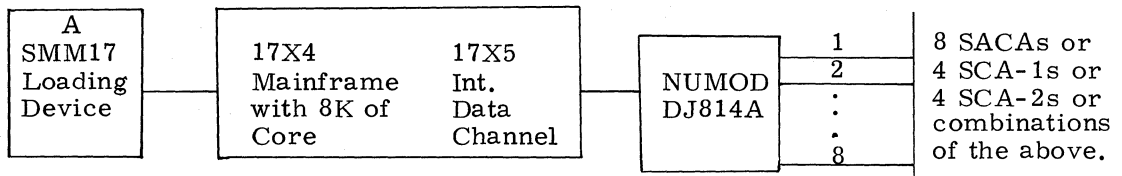
One NUMOD Communications Multiplexer

4. Maximum Configuration

All items referenced in the above paragraph, plus expansion of the CAs to the following limits:

- Eight SACAs, or
- Four SCA-1s, or SCA-2s, or
- Combinations of SCA-1, SCA-2, and SACAs (SCA-1, ACA, and SCA-2 requires two addresses per CA, SACA requires one address per CA).

5. Equipment Configuration



## B. SOFTWARE

### 1. Environment

The diagnostic program operates under control of the SMM17 Monitor in the teletypewriter non-interrupt mode. The monitor and the test require parameters which can either be supplied each time the test is initiated or the test can execute with a prestored set of parameters.

### 2. External References

The diagnostic test makes reference to the monitor-based subroutines and tables. Linkages are through low core via equates. These equates are incorporated in the diagnostic test.

## IV. OPERATIONAL PROCEDURE

### A. LOADING PROCEDURE

The diagnostic is loaded using the standard SMM17 Monitor Test loading procedure.

### B. PARAMETERS

Prestore parameter location for NUMOD Test

CATOTS + 0	First CA Parameter	First Stop	(A)	0F3D
CATOTS + 1			(Q)	0F3E
CATOTS + 2		Second Stop	(A)	0F3F
CATOTS + 3			(Q)	0F40
CATOTS + 4	Second CA Parameter	First Stop	(A)	0F41
CATOTS + 5			(Q)	0F42
CATOTS + 6		Second Stop	(A)	0F43
CATOTS + 7			(Q)	0F44
CATOTS + 8	Third CA Parameter	First Stop	(A)	0F45
CATOTS + 9			(Q)	0F46
CATOTS + A		Second Stop	(A)	0F47
CATOTS + B			(Q)	0F48
CATOTS + C	Fourth CA Parameter	First Stop	(A)	0F49
CATOTS + D			(Q)	0F4A
CATOTS + E		Second Stop	(A)	0F4B
CATOTS + F			(Q)	0F4C

CATOTS + 10	Fifth CA Parameter	First Stop	(A)	0F4D
CATOTS + 11			(Q)	0F4E
CATOTS + 12		Second Stop	(A)	0F4F
CATOTS + 13			(Q)	0F50
CATOTS + 14	Sixth CA Parameter	First Stop	(A)	0F51
CATOTS + 15			(Q)	0F52
CATOTS + 16		Second Stop	(A)	0F53
CATOTS + 17			(Q)	0F54
CATOTS + 18	Seventh CA Parameter	First Stop	(A)	0F55
CATOTS + 19			(Q)	0F56
CATOTS + 1A		Second Stop	(A)	0F57
CATOTS + 1B			(Q)	0F58
CATOTS + 1C	Eighth CA Parameter	First Stop	(A)	0F59
CATOTS + 1D			(Q)	0F5A
CATOTS + 1E		Second Stop	(A)	0F5B
CATOTS + 1F			(Q)	0F5C
ONOINT	Interrupt line number			* 0EF9
CCANUM	Number of CAs to test and NUMOD Test			* 0EFA
CDELAY	NUMOD Interrupts Clock Time			** 0EFB
CEQBAD	Illegal equipment number			** 0EFC

#### 1. Prestored Parameters

The diagnostic is set to run with a prestored set of parameters. No parameter changes are required if the prestored list of parameters are valid for the CAs being tested.

The following is a list of the prestored parameters.

- a. NUMOD equipment E.
- b. Interrupt line number 3.
- c. Illegal equipment number 0.
- d. NUMOD subtest selection 0 through 5.
- e. NUMOD clock prestored as \$64 (1 millisecond).

\* 2. b. Second stop (A) (Q) respectively.

\*\* 2. c. Third stop (A) (Q) respectively.

f. Three communications adapters are selected:

- 1) SCA-1 addresses 0 and 1
- 2) SACA address 2
- 3) SCA-2 addresses 4 and 5

g. All CAs set for 8 bits of data.

To alter the prestored parameters, follow the directions stated in SMM17 Reference Manual.

## 2. NUMOD Parameters (DJ814A)

a. First Stop (overflow light on)

- (A) = 3631 - Test ID Stop  
(Q) = Stop/Jump Parameter

b. Second Stop

- (A) = Interrupt Line assigned to NUMOD  
(Q) = WXZZ (prestored as 303F)

where: W = Q (bits 15 through 12) - Number of CAs to be tested  
(CAs with two addresses count as one CA)

X = Q (bits 11, 10, 9, 7) = 0  
(bit 8) - ACUCA Test Selection

ZZ = Q (bit 6 through 0) - NUMOD subtest selection (see Section IV.B.3.c)

c. Third Stop

(A) = (1/10 NUMOD clock setting in microseconds)<sub>16</sub>

Example: Clock set at 16 milliseconds

1) Convert to microseconds  $16 \times 1000 = 16,000_{10}$

2) Divide by 10  $16,000 \div 10 = 1600_{10}$

3) Convert to hexadecimal  $1600_{10} = 640_{16}$

(Q) = Illegal equipment number (see Section VI.B.1.a.)

### NOTE

If the ACUCA test is selected for execution, the next parameter stop will be the ACUCA parameter stop C.(4).

## 3. CA Parameters

a. SACA, SCA-1, SCA-2, ACA

The following stops (4 through 6) are required if any CAs are to be tested. Two stops are required for each CA. If eight SACAs are to be tested, stops (4 through 6) will be repeated for the last CA to be tested.



1) Fourth Stop (Overflow light on)

(A) = 36Y1 - Test ID Stop

where Y = Twice the number of CAs to be tested +1. Y max = 15 (F)

(Q) = Stop/Jump Parameter

2) Fifth Stop

(A) - CA ID Word

A = 

15-13	12	11-10	9-8	7-5	4	3-0
-------	----	-------	-----	-----	---	-----

where: A(15-13) - CA Address (even-numbered address if a 2-address CA). SCA-2 on address 0 and 1, enter 0 in bits 15-13

A(12) - Mode; SCA's 0 = Universal

1 = ASCII

ACA's 0 = SOM/EOM Not Selected

1 = SOM/EOM Selected

SACA = N/A

A(11-10) - Bits to test; 0=5, 1=6, 2=7, 3=8. 0 or 1 selection illegal for SCA-1, SCA-2.

A(9-8) - Parity (SCAs and ACA only);

00 = No Parity

01 (bit 8) = Even Parity

10 (bit 9) = Odd Parity

11 (bits 8, 9) = Illegal Selection

A(7-5) - Not Used

A(4) - EOM (SCAs ACA only); 0 = EOM Not Selected

1 = EOM Selected

A(3-0) - CA type; 4 = SACA

D = ACA

E = SCA-1

F = SCA-2

Q(15-8) = EOM only character (ACA)

Q(7-0) = SOM only character (ACA)

SYNC only character (SCA-1, SCA-2)

3) Sixth Stop

(A) = Subtest Selection, Subtests 0 through 0F

SACA has only 12 (bits 0 through 11) subtests

Q(15-8) = Selectable Data Pattern for CA Test (ACA, SCA's subtest 11, SACA subtest B)

Q(07-04) = 0

Q(03-00) = Subtest Selection, Subtests 10 through 13 (used only for  
ACA and SCA's)

If a bit is set, the corresponding subtest will be selected.

For example, A(9) = Subtest 9; Q(1) = Subtest 11, etc.

Return to CA parameter for each CA selected - Step 2 (fifth stop)

4) ACUCA Parameter Stop 1

A(2-0) = ACUCA Address (prestored \$FFFF)

A(15-3) = Not Used

(Q) = Abandon Call Retry Time-out for 801A1/801C1 Bell System  
Auxiliary Data Set

000A = 7 second time-out

000E = 10 second time-out

0014 = 15 second time-out

0020 = 25 second time-out

0030 = 40 second time-out

Parameter Stops 2 through n (stop repeated for each digit to a maxi-  
mum of 10 digits). A = 0000 Q = (digit count is displayed; do not alter)

A(3-0) = Dial Digits (maximum 10 digits)

A(14-4) = Not Used

A(15) = Setting of this bit indicates all numbers have been entered,  
ACUCA testing begins (set with last digit)

n = Last digit to be entered

NOTE

If the ACUCA has the capability of detecting  
the EON code, to place the associated data  
set in data mode, this hex number "C16"  
must be entered after the last dial digit and  
included in the digit count.

C. SECTION DESCRIPTION INDEX

1. NUMOD Test

<u>Test No.</u>	<u>Name</u>	<u>Page</u>	<u>Run Time</u>
00	Internal, External Reject Subtest		
01	Status Subtest		
02	Clear Controller Subtest		
03	Clear Interrupt Subtest		
04	Clock Interrupt Request Subtest		
05	Multiple Function Subtest		
06	NUMOD Protect Subtest		

Total Run Time

2. SACA Test

<u>Test No.</u>	<u>Name</u>	<u>Page</u>	<u>Run Time</u>
00	Disable CA Function Subtest		
01	Enable CA Function Subtest		
02	Clear Break Subtest		
03	Set Break Subtest		
04	Lost Previous Character Subtest		
05	Zero Data Pattern Subtest		
06	Ones Data Pattern Subtest		
07	Alternate ones Data Pattern Subtest		
08	Alternate Zero Data Pattern Subtest		
09	Sliding Zero Data Pattern Subtest		
0A	Sliding Ones Data Pattern Subtest		
0B	Operator Select Data Pattern Subtest		
			Total Run Time

3. SCA-1, SCA-2, ACA Test

<u>Test No.</u>	<u>Name</u>	<u>Page</u>	<u>Run Time</u>
00	Enable CA (Control Channel) Subtest		
01	Select Test Mode Subtest		
02	Enable CA (Data Channel) Subtest		
03	Disable CA (Control Channel) Subtest		
04	Disable CA (Data Channel) Subtest		
05	Program Clear Subtest		
06	Status Request Subtest		
07	Clear Test Mode Subtest		
08	Character Ready Subtest		
09	Parity Error Subtest (SCA's only)		
0A	Character Lost Subtest		
0B	Zero Data Pattern Subtest		
0C	Ones Data Pattern Subtest		
0D	Alternate Ones Data Pattern Subtest		
0E	Alternate Zeros Data Pattern Subtest		
0F	Sliding Zero Data Pattern Subtest		
10	Sliding Ones Data Pattern Subtest		
11	Operator Select Data Pattern Subtest		
12	Data Message Subtest		
13	ASCII Pattern Subtest SCA-2 Transparent Mode		
			Total Run Time

4. ACUCA Test

00 Dial a phone and check status.

V. OPERATOR COMMUNICATION

A. MESSAGE FORMATS

1. Normal Program Typeout

- a. DJ814 Test Identification during initialization  
 AQMA36, NUMOD/C.A. Test  
 CP2F, VER. 4.0  
 IA = XXXX, FC = XX

b. End of Test

A	Q	A	Q
	Stop/Jump	Pass	Return
3624	Parameter	Number	Address

2. Error Message

All Error Message displays use the standard SMM17 Error message format:

A	Q	A*	Q	A Q . . . A Q
36X8	Stop/Jump	Subtest/	Return	(See individual
	Parameter	Error	Address	Error message)

X = Number of AQ Displays

3. Loop On Subtest Halt

A	Q	A	Q
3622	Stop/Jump	Subtest/	Return
	Parameter	Device	Address

4. Loop On Test Display

A	Q	A	Q
3624	Stop/Jump	Pass	Return
	Parameter	Number	Address

5. Operator Intervention Halt (NUMOD Subtest 06)

A	Q	A	Q
3621	Stop/Jump	0001 (set NUMOD	0806
	Parameter	PROTECT and P. P.	
		switches)	

A	Q	A	Q
3621	Stop/Jump	0002 (clear	0806
	Parameter	NUMOD PROTECT	
		and P. P. switches)	

\*FFXX is typed if an error occurs while in Interrupt mode, where XX is the error number.

<u>Error Code</u>	<u>Description</u>
05	<p>Disable CA (data channel) error.  CA data word bit 10 (character request) not cleared after disable CA function to CA.</p> <p>A = Even no. 0000 through 0006 (device in error)  Q = Expected CA data word (12 bits)  A = Received CA data word (12 bits)  Q = 0000</p>
06	<p>Program Clear error.  CA status word not cleared after program Clear function to the CA. Only bits 11, 10, 9, 8, 7, 1, 0 are checked; of these, only bit 1 should be set.</p> <p>A = Odd no. 0001 through 0007 (device in error)  Q = Expected CA status word (12 bits)  A = Received CA status word (12 bits)  Q = Sent CA function word (12 bits)</p>
07	<p>Input or output reject.  A = 0000 through 0007 (device in error) (Remainder of display see Section V.C.2 error no. 07).</p>
08	<p>Disable CA (control channel) error.  CA status word bit 10 (function request) not cleared after disable function to CA.</p> <p>A = Odd no. 0001 through 0007 (device in error)  Q = Expected CA status word (12 bits)  A = Received CA status word (12 bits)  Q = 0000</p>
09	<p>Status Request error.  CA status word bit 11 (status ready) not as expected.</p> <p>A = Odd no. 0001 through 0007 (device in error)  Q = Expected CA status word (12 bits)  A = Received CA status word (12 bits)  Q = Sent CA function word (12 bits)</p>
0A	<p>Clear Test Mode error.  CA status word bit 0 (Test mode) not cleared after Clear Test Mode function to CA.</p> <p>A = Odd no. 0001 through 0007 (device in error)  Q = Expected CA status word (12 bits)  A = Received CA status word (12 bits)  Q = Sent CA function word (12 bits)</p>
0B	<p>Not used.</p>

<u>Error Code</u>	<u>Description</u>
0C	<p>Character Ready error.</p> <p>CA data word bit 11 (character ready) not set after transmission of data word to CA.</p> <p>A = Even no. 0000 through 0006 (device in error)  Q = Expected CA data word (12 bits)  A = Received CA data word (12 bits)  Q = Sent CA data word (8 bits)</p>
0D	<p>CA Data Input error.</p> <p>Data received from the CA was not as expected.</p> <p>A = Even no. 0000 through 0006 (device in error)  Q = Expected CA data (12 bits)  A = Received CA data (12 bits)  Q = Sent CA data (8 bits)</p>
0E	<p>Character Parity error.</p> <p>Data parity bit not set after forced parity error (test 9).</p> <p>A = Odd no. 0000 through 0007 (device in error)  Q = Expected CA status word (12 bits)  A = Received CA status word (12 bits)  Q = Sent CA data (8 bits)</p>
0F	<p>Character Lost error.</p> <p>CA data word bit 9 (character lost) not as expected.</p>
10	<p>EOM (bit 8 data word) error bit 8 not as expected.</p> <p>A = 0000 through 0006 (device in error)  Q = Expected CA data (12 bits)  A = Received CA data (12 bits)  Q = Sent CA data (8 bits) or 000, if waiting for EOM</p>
11	<p>Control Channel Parity error bit 9 not as expected.</p> <p>A = 0000 through 0007 (device in error)  Q = Expected CA status word (12 bits)  A = Received CA status word (12 bits)  Q = 0000</p>
12	<p>Control Channel Status error.</p> <p>CA status word bit 9 (parity error) is set after ETB/ETX is received.</p> <p>A = 0000 through 0007 (device in error)  Q = Expected CA status word (12 bits)  A = Received CA status word (12 bits)  Q = Sent CA data (8 bits)</p>

## VI. DESCRIPTION

### A. GENERAL

The diagnostic is divided into two main parts; the NUMOD tests and the CA tests. The CA tests are further divided into CA type tests, with the single address CAs (ACUCA, SACA), and the dual address CAs (ACA, SCA-1, SCA-2), using different test coding but using common coding for: Control, Parameter Entry, Interrupt Processing, Input and Output, Error Messages, End of Subtest, End of test repeating, and Elapses timing.

Control is returned to the test executive after any successful output, any successful input, data verification at the end of a subtest, and after any error messages.

The ACUCA test is a go - no go test. If an error is detected, the test will automatically repeat the condition; errors are not reported in SMM format. At the end of the test, with the SLS set, the test will stop with (Q) = FFFF. At this time the operator can repeat the test by placing the computer in run, or can start NUMOD/CA testing by setting P = IA and reentering parameters without the ACUCA test bit selected.

If an error occurs and "Loop on Error" is selected, the current subtest being executed will enter the shortest loop possible to again generate the error.

### B. TEST DESCRIPTION

#### 1. NUMOD Test

The diagnostic is designed so that the NUMOD test, if selected, is executed prior to any of the CA tests being initiated. The NUMOD test is divided into seven subtests (00 through 06). Subtests 00 through 05 are part of the prestored parameter list.

##### a. Subtest 00 - Internal External Reject Subtest

This subtest is responsible to check that a reject does occur when an illegal I/O operation is performed. Internal reject is generated by outputting to an equipment not on the system. The illegal equipment no. is supplied during parameter entry. The equipment number is prestored as equipment zero. External rejects are generated by outputting to each CA address. Since the CA has not been enabled an external reject should occur for each address.

b. Subtest 01 - Status Subtest

This subtest is responsible to check that no reject occurs when a status request is made. No attempt is made to validate the status clock bit or the protect bit. The clock bit is validated each time an interrupt occurs and the protect feature is validated by subtest 06.

c. Subtest 02 - Clear Controller Subtest

This subtest is responsible for functioning the NUMOD to clear controller, checking if a reject occurs. Clear controller function is used in subtest 00 to ensure that all the CAs are disabled.

d. Subtest 03 - Clear Interrupt Subtest

This subtest is responsible for functioning the NUMOD to clear the interrupt. A check is made to ensure that no reject has occurred.

e. Subtest 04 - Clock Interrupt Request Subtest

This subtest is responsible for functioning the NUMOD to request an interrupt. A check is made to ensure that no reject has occurred, that an interrupt does occur within the specified time (taken in as a parameter), and that the clock status bit is set when an interrupt occurs.

f. Subtest 05 - Multiple Function Subtest

This subtest is responsible to function the NUMOD with all the combinations of multiple functions (3, 5, 6, 7) to ensure that no rejects occur. Those requesting the clock interrupt (5, 6, 7) are checked for interrupts, and that the interrupt status bit (3) is set.

g. Subtest 06 - NUMOD Protect Subtest

This subtest is responsible to function the NUMOD when the equipment is protected. A Reject signal should occur. The operator is asked, at the appropriate times, to set and clear the NUMOD PROTECT switch and the 1700 PROGRAM PROTECT switch. See Section V.A.4.

2. Single Address CA (SACA) Test

The SACA test is designed to test from one to eight SACAs simultaneously. Subtests 00 through 0B are part of the prestored parameter list. Each SACA to be tested must be set (manually) in test mode and connected for Full Duplex operation. Subtests 01 through 0B are checked to ensure that no rejects occur. All subtests check all the status bits (8, 9, 10, 11) to ensure they are set or clear as required.



\$4A	ASCII	J	
\$42	ASCII	B	
\$10	ASCII	DLE	This terminates the Trans-
\$17	ASCII	ETB	parent mode
\$02	ASCII	STX	
\$10	ASCII	DLE	
\$10	ASCII	DLE	
\$03 or EOM			\$03 used for SCAs, EOM used for ACA. See Section IV.B.3.a.2).

Each character is checked for character parity (if parity selected) and data verify. The parity bit on the control channel is checked after the ETB character and the EXT (03) or EOM character.

When testing an SCA and the character sent is an ETX or ETB, a delay of 5 character times is selected. Whenever the ETX, ETB character is input, bit 8 (EOM), if selected, also received with the data.

When testing an ACA and the character sent is the selectable EOM character, bit 8 (EOM), if selected, is also received with the data.

Any rejects, unexpected status, or deviation in the message data will result in an Error message.

x. Subtest 13 - ASCII Transparent Mode

This subtest is designed to test Transparent mode, when testing an SCA-2 (DJ-145A). The subtest is not executed on an ACA or SCA-1.

In execution of this subtest, the following data block is sent and received.

\$01	SOH
\$10	DLE
\$10	DLE
\$1F	ITB
\$7F	PAD
\$10	DLE
\$02	STX

\$10	DLE
\$10	DLE
\$58	X
\$50	P
\$41	A
\$52	R
\$10	DLE
\$03	ETX

\*

} SCA-2 is in Transparent mode at this output time.

\*The SCA-2 (DJ145-A) will strip the second DLE of DLE, DLE sequence when in Transparent mode.

The only check made by the subtest to assure the CA is in Transparent mode is that the second DLE character is stripped and parity is not received. If data is not received properly, error code \$0D (Input error) is displayed. It is left up to the operator to determine the possible cause when error code 0D (CA Data Input error) is displayed. The last Q display will equal the input count.

EOM Enable should not be selected on the CA when running this test. If selected illegal (10-EOM bit 8 not as expected), errors will be displayed.

#### 4. ACUCA Test

The ACUCA test is a go-no-go test. If an error is detected, the test will automatically loop. Errors are not reported in SMM17 format. At the end of the test, with SLS set, the test will stop with (Q) = FFFF. At this time the operator can repeat the test by placing the computer in run, or can start NUMOD/CA testing by setting P = 0602 and reentering parameters without the ACUCA test bit selected. If SLS is not set, the test will automatically repeat test. If a status error occurs with the SLS set, the computer will stop with (A) = expected status, (Q) = received status. If the test appears to be hung in a loop, it is suggested the operator determines the cause by the use of SLS (status error), flow chart, and listing. Only one ACUCA is tested at one time.

#### 5. Subtest Selection

When two or three types of CAs (SCAs, ACA) are selected to be tested simultaneously, the subtest selection must be identical for all dual address CAs.

1743-2 ASYNCHRONOUS COMMUNICATION CONTROLLER TEST  
(ACCO86 Test No. 86)

I. OPERATIONAL PROCEDURE

A. REQUIREMENTS

1784-1 or -2 with 8K of memory  
1743-2 Asynchronous Controller - DJ815  
Distribution panel jumper plug or wires (optional)  
CRT or equivalent to run Section 6 - Echo Test (optional)

B. LOADING PROCEDURE

This test loads and executes correctly under SMM17. The calling sequence is specified by the SMM17 system being used. If the equipment address is zero when called, the test will use the prestored equipment address (IA+6).

C. TESTING PROCEDURE

The 1743-2 is tested in various configurations. Self-jumpered channels, channels connected to other channels, and channels connected to an I/O device are tested. The test is interrupt-driven and times out interrupts. It will release control to multiplex with other tests while awaiting an interrupt.

D. PARAMETERS

1. Stop 1

A1 = 8671 Test ID (86), seven stops (7), parameter stop (1)  
Q1 = STJP Test unique Stop/Jump parameter (see TSTJP)

2. Stop 2

A2 = 00FF Section Select parameter, bit 2 = Section 2, bit 3 = Section 3 (There are eight sections (0-7).)  
Q2 = 0200 Interrupt line select (Single bit represents interrupt line.)  
Example: 0200 = Interrupt line 10.

3. Stop 3

A3 = 0XXX Channel 0 selector (see Channel Select Codes)  
Q3 = 1XXX Channel 1 selection

4. Stop 4

A4 = 2XXX Channel 2 selection  
Q4 = 3XXX Channel 3 selection

5. Stop 5

A5 = 4XXX Channel 4 selection  
Q5 = 5XXX Channel 5 selection

6. Stop 6

A6 = 6XXX Channel 6 selection  
Q6 = 7XXX Channel 7 selection

7. Stop 7

A7 = Special data pattern (If bit 15=1, continuously send out selected character in Section 5.)

Q7 = Test mode pattern (If set to 0, random data will be used as a test mode pattern.)

8. Channel Select Codes

If channel word = 0, no modem or test cable is present.

Format of channel word:

PCDT

Where: P = Present channel number (bits 14-12)

C = Channel number (0-7), connected to present channel if test jumpers are installed (bits 10-8)

D = Number of data bits/characters (5-8), this channel jumpered for (bits 7-4).

T = Type of channel connection where (bits 2-0):

0 = No connection to this channel

1 = Modem connected to input/output device

2 = Modem in test mode or channel self-jumpered

3 = This channel test-jumpered to another channel

Examples:

A3 = 0080 Channel 0, eight data bits, no connection

Q3 = 1081 Channel 1, eight data bits, modem to I/O device

A4 = 2072 Channel 2, seven data bits, channel self-jumpered

A5 = 4563 Channel 4, six data bits, test-jumpered to channel 5

Q5 = 5463 Channel 5, six data bits, test-jumpered to channel 4

NOTE

Since internal hardware limits parameter's selection such as baud rate, data bits, parity, etc. to pairs (0-1, 2-3, 4-5, 6-7), only these pairs should be test-jumpered.

9. TSTJP - Test Stop/Jump parameters

Q1 bits 0-8 = Same meaning as SMM STJP.

E. STOPS

1. Type 1 - Parameter Entry

For information on parameters, see Parameters section. This stop will occur if STJP bit 0 is set.

A1 = 8671

Q1 = TSTJP (see Parameters)

2. Type 2 - End of Section

Stop at end of section. This stop will only occur if the test STJP bit 1 is set.

A1 = 8622 (86) test ID, (2) number of stops, (2) end of section

Q1 = TSTJP

A2 = 0S00 (S=section number)

Q2 = RTA Return address

3. Type 4 - End of Test

Stop at end of test. This stop will only occur if STJP bit 2 is set.

A1 = 8624 (86) test ID, (2) number of stops, (4) end of test

Q1 = TSTJP

A2 = NNNN (NNNN = number of passes)

Q2 = RTA Return address

F. WORD MESSAGES

Word messages are available only if there is a TTY or equivalent available. (The following messages are information to the operator.)

1. Initialization of the Test

ACC086 ASYNCHRONOUS COMMUNICATION CONTROLLER TEST

CP2F, VER. 3.1-1

IA = XXXX FC = XX

2. Parameter Selection

ERROR IN CHANNEL PARAMETER

This indicates that an error was made in the description of channel configurations. After the message is typed, parameter selection will be re-entered.

3. Echo Section - Section 6

ACC086 ECHO SECTION - CHARS TYPED ON TEST I/O  
DEV WILL BE ECHOED BACK WHEN RETURN KEY DEPRESSED.  
TYPE (Control E) TO EXIT SECTION.

This message alerts the operator that it is not actively testing but awaiting characters to echo.

G. ERROR CODES

There is a common error routine; therefore, the error parameters always have the same meanings. A description of the error parameters and codes follow.

1. A = 8658 (test number, number of stops, type of stops)  
Q = Stop/Jump word
2. A = CXZZ (C=channel, X=section, ZZ=error)  
Q = Return address
3. A = Last local I/O routine call address  
Q = Enabled-channels (bit position = 1 = ENBLD)
4. A = Input data/status word  
Q = Clock/protect status word
5. A = Function output (A register)  
Q = Equip/channel output (Q register)
6. A = Bad data word (if appropriate)  
Q = Good data word (if appropriate)

<u>Error Number</u>	<u>Error Description</u>
01	Data compare error
02	Interrupt with CLK request clear
03	No interrupt with CLK request set
04	Controller internal reject
05	Controller external reject
06	No reject output to disable channel
07	Reject on output to enable channel
08	Internal reject on input during interrupt service
09	Internal reject on output during interrupt service
0A	External reject on input during interrupt service
0B	External reject on output during interrupt service
0C	Unused bit set in clock status
0D	Unused bit set in data status

<u>Error Number</u>	<u>Error Description</u>
0E	Parity error set
0F	Character lost set
10	Break error set
11	Clock status set after clear controller
12	Clock status clear after 100 milliseconds
13	Clock set after clear interrupt
14	Clock status clear after 1000 milliseconds
15	More than one interrupt for interrupt request
16	Timed-out waiting for interrupt
17	Character request not set
18	Bit set in data word after clear
19	Wrong channel replies another enabled
1A	No character request after 250 clock pulses
1B	Reject on input from disable channel
1C	Channel enabled by a write
1D	Character ready did not set
1E	No character request after first character
1F	Character request set after two characters
20	No character request after 100-millisecond wait
21	Character lost did not set
22	No character ready after 250 clock pulses

## II. SECTION DESCRIPTION

### A. SECTION 0 - CONTROLLER STATIC TEST

The following is tested.

1. Controller can be addressed.
2. Clock status is clear after clear controller.
3. Clock status sets.
4. Clock status clears with clear interrupt.
5. Clock status stays set after long delay.
6. Unused bits in clock status word are not set.
7. Controller is not causing unexpected interrupt.
8. Clock can cause interrupt if enabled.
9. Only one interrupt occurs when clock interrupt request is enabled.

B. SECTION 1 - CHANNEL STATIC TEST

The following is tested.

1. A data input will not cause external reject if channel is disabled.
2. A data output will cause external reject if channel is disabled.
3. A data input will reply if channel is enabled; character request will be set (all other bits are clear).
4. If one channel is enabled, all others will reject using data output.
5. A data output will reply if channel is enabled and will reject if the channel is disabled by channel disable.

C. SECTION 2 - CHARACTER REQUEST TEST

The following is tested.

1. Write function does not enable channel.
2. Output null character to DTR channels. Check character request; it should be set due to double buffering.
3. Output another null character. Character request should not be set.
4. Wait 100 milliseconds; character request should be set.

D. SECTION 3 - CHARACTER READY/LOST TEST

This section tests the following on channels with modems in test mode and channels test-jumpered.

1. Character Ready sets.
2. Character Lost does not set erroneously.
3. Character Lost sets.
4. Do 1, 2, and 3 transmitting in other direction.

E. SECTION 4 - TEST MODE DATA TEST

This section exercises channels with modems in test mode or channel pairs test-jumpered.

1. Use data in test mode pattern to exercise receiver and transmitter.
2. If data in parameter is equal to zero, random data is set.



F. SECTION 5 - TRANSMIT SPECIAL PATTERN TO ALL DTR CHANNELS

1. Enable all DTR channels.
2. Transmit special pattern to all channels.
3. Check for last character (send 80).

G. SECTION 6 - ECHO TEST

1. Enable all DTR channels.
2. Scan for input.
3. Echo and store each character until 72 characters are received or carriage return is received.
4. Print a buffer of characters received.

H. SECTION 7 - TRANSMIT ASCII RIPPLE PATTERN TO ALL DTR CHANNELS

1. Enable all channels.
2. Transmit carriage return and line feed.
3. Transmit character to all channels and start pattern with a different character for each channel.
4. Update character and check for end of line (72 columns).
5. Output 64 lines.

III. MISCELLANEOUS

A. JUMPER PLUGS

The following test jumper configurations must be followed to jumper channels for self-test.

1. Channel Connected to Self

Pin 2 is connected to pin 3, and pin 4 is connected to pin 5 on appropriate channel plugs on the distribution panel.

2. Channel Pair Test Jumpered

The following example uses channels 0 and 1. This can be followed for any other legal channel pair (2-3, 4-5, 6-7).

Pin 2 (channel 0) to pin 3 (channel 1)

Pin 3 (channel 0) to pin 2 (channel 1)

Pin 4 (channel 0) to pin 5 (channel 0)

Pin 4 (channel 1) to pin 5 (channel 1)

B. CRT OR EQUIVALENT

The CRT cable has to be modified if a modem is not used.

On either end of cable, remove wires from pins 4 and 5 and install jumpers between pins 4 and 5.

On distribution panel end of cable, remove wire from pin 6 and connect to pin 20.

1743-1 SYNCHRONOUS COMMUNICATION CONTROLLER  
(SCCA87 Test No. 87)  
(FJ 606-A)

I. OPERATIONAL PROCEDURE

A. REQUIREMENTS

1784-1 or -2 with 8K of memory  
1743-1 Synchronous Communication Controller and Distribution Panel and  
RS-232-C Interface  
Jumper plug or wires (optional)  
TTY or Equivalent and a terminal to execute Section 6 - Transmit Message  
TTY or Equivalent to execute Section 7 - Loop Characters and Output on  
Comment Device  
Furnished message to terminal device (Section 6 - optional)

B. LOADING PROCEDURES

This test loads and executes correctly under SMM17. The calling sequence is specified by the SMM17 system being used. If the equipment address is zero when called, the test will use the prestored equipment address (IA+6).

C. TESTING PROCEDURE

The 1743-1 is tested in various configurations. Self-jumpered channels or channels jumpered to another are tested. If neither of the above is specified, the test will use the channel command Test Mode. Five to eight bits/character and any sync character bit configuration that is compatible with the hardware are tested. Messages, composed and entered by the operator, are sent to the terminal. The test is interrupt-driven and times out interrupts. It is stand-alone because of the response time necessary to service the incoming data.

D. STOPS

1. Type 1 - Parameter Entry (Start of Test)

a. Stop 1

A1 = 8751 test ID (87), five stops (5), parameter stop (1)

Q1 = STJP test Stop/Jump parameter

- b. Stop 2
- A2 = 01FF Section select parameter, bit 2 = Section 2, bit 3 = section 3 (There are nine sections (0-8); \$BF is prestored.)
- Q2 = 0020 Interrupt line select (Single bit represents interrupt line. \$20 is prestored. Example: 0020 = interrupt line 5.)
- c. Stop 3
- A3 = 00XX Channel 0 selector (See Channel Select Codes)
- Q3 = 00XX Channel 1 selector
- d. Stop 4
- A4 = 00XX Test mode pattern for Section 4 (If set to 0, the character A will be used as a test mode pattern.)
- Q4 = X0XX Special data pattern for Section 5 (If set to X000, the character A will be used as a pattern. If set, bit 15 indicates the character will be sent continuously.)
- e. Stop 5
- A5 = 0XX0 Repeat flags (If bit is set, character or message will be repeated continuously.)
- Bit 6 - Repeat Section 6
- Bit 7 - Repeat Section 7
- Bit 8 - Repeat Section 8
- Q5 = 000X Controller and duplex flags, bit 0, controller number (0 or 1) bit 1, 0 = full duplex, 1 = half duplex (Half duplex requires special hardware setup for testing.)
- f. Stop 6
- A6 = 00XX Sync character (This parameter must coincide with the hardware jumpers, prestored with \$16.)
- Q6 = 00XX Special output character for Sections 1 and 3 (Prestored as \$20.)

g. Channel Select Codes

If channel word = 0, no test is to be performed for this channel.

Format of channel word:

Bits 0 through 3:

- 0 = No test for this channel
- 1 = This channel test jumpered to other channel
- 2 = This channel test jumpered to self
- 3 = Modem connected to I/O device
- 4 = No terminal connection and no jumpers
- 5 = Jumpered for Section 8

The channel select codes execute program sections only as follows:

<u>Channel Select Code</u>	<u>Executed Section</u>
0	None
1	0, 4, 5, 7
2	0, 4, 5, 7
3	0, 1, 2, 3, 4, 5, 6, 7
4	0, 1, 2, 3, 4, 5, 7
5	0, 1, 2, 3, 4, 5, 7, 8

Bits 4 through 7:

Number of data bits (5-8) this channel jumpered for; 8 is pre-stored.

Section 7 will execute with 7- or 8-bit configuration only.

Bits 8 through 15:

Not used.

NOTE

When one channel is jumpered to the other channel, the recipient channel must have a select code of zero.

When Section 6 is executed, the select code must be 3.

When Section 8 is executed, the select code must be 5.

Examples:

- A3 = 0000 Channel 0, no test for this channel
- Q3 = 0080 Channel 1, no test for this channel
- A3 = 0082 Channel 0, eight data bits, channel jumpered to self
- Q3 = 0073 Channel 1, seven data bits, channel connected to I/O device

2. Type 1 - Parameter Entry (Section 6)

This stop is presented when Section 6 is executed.

a. Stop 1

A1 = 8721      Test ID (87), two stops (2), parameter stop (1)  
Q1 = STJP      Test Stop/Jump parameter

b. Stop 2

A1 = 00XX      Character n of message  
Q1 = 00XX      Character N+1 of message

Parameter entries will be repeated until zeros are entered in a stop which indicates end of the message. A maximum of 80 characters may be entered (one character per register).

3. Type 2 - End of Section

a. Stop 1

A1 = 8722      Test ID (87), two stops (2), end of section stop (2)  
Q1 = STJP      Test Stop/Jump parameter

b. Stop 2

A2 = 0X00      Section number  
Q2 = XXXX      Return address

4. Type 4 - End of Test

a. Stop 1

A1 = 8724      Test ID (87), two stops (2), end of test (4)  
Q1 = STJP      Test Stop/Jump parameter

b. Stop 2

A2 = XXXX      Pass count  
Q2 = XXXX      Return address

5. Type 8 - Error

There is a common error routine; therefore, the error parameters always have the same meanings. A description of the error parameters and codes follow.

a. Stop 1

A1 = 8778      Test ID (87), seven stops (7), error stop (8)  
Q1 = STJP      Test Stop/Jump parameter

- b. Stop 2
  - A2 = CXZZ (C=channel, X=section, ZZ=error code)
  - Q2 = Return address
- c. Stop 3
  - A3 = Last local I/O call address
  - Q3 = Second level I/O call address
- d. Stop 4
  - A4 = First level I/O call address
  - Q4 = Channel status word
- e. Stop 5
  - A5 = Data/status word
  - Q5 = Clock/protect status word
- f. Stop 6
  - A6 = Function output (A register)
  - Q6 = Equip/channel output (Q register)
- g. Stop 7
  - A7 = Input data word (if appropriate)
  - Q7 = Output data word (if appropriate) (The upper bits/character filler bits are included.)

<u>Error Number</u>	<u>Error Description</u>
1	Data compare error
2	Interrupt with clock request clear
3	No interrupt with clock request set
4	Controller internal reject
5	Controller external reject
6	No reject output to disable channel
7	Reject on input to enable channel
8	Internal reject on input during interrupt service
9	Internal reject on output during interrupt service
A	External reject on input during interrupt service
B	External reject on output during interrupt service
C	Unused bit set in clock status
D	Unused bit set in data status
E	Parity error

<u>Error Number</u>	<u>Error Description</u>
F	Character lost
10	Break error
11	Clock status set after clear controller
12	Clock status clear after 100 milliseconds
13	Clock set after clear interrupt
14	Clock status clear after 1000 milliseconds
15	More than one interrupt for interrupt request
16	Timed out waiting for interrupt
17	Character request not set
18	Bit set in data word after clear
19	Wrong channel replies another enabled
1A	No character request after 100 clock pulses
1B	Reject on input from disabled channel
1C	External reject when selecting test mode
1D	Data terminal ready bit not set after channel clear
1E	External reject when disconnecting
1F	Data terminal ready bit set after disconnecting
20	External reject when connecting
21	Data terminal ready bit not set after connecting
22	Test mode bit not set after select test mode
23	Test mode bit set after clear controller
24	Test mode bit set after clear adapter
25	Illegal bits set after clear adapter
26	External reject when clearing test mode
27	Test mode bit set after clear test mode
28	Data set ready status bit not set after request to send
29	Character ready bit set before test mode is on
2A	Function request not set after enable channel
2B	No character ready after 100 clock pulses
2C	Sync character not sent but was received
2D	Character received not a sync character
2E	Sync not established after two sync characters sent
2F	Sync not established after four sync characters sent
30	External reject when disabling channel
31	External reject when request to send
32	External reject when character request
33	Sync not established after 5 milliseconds
34	External reject when stop send



<u>Error Number</u>	<u>Error Description</u>
35	Character request should not be set
36	External reject when clear adapter
37	External reject when getting channel status
38	Sync-not-established is not set after clear
39	Function request is not set after clear
3A	Status ready is not set when carrier-on changes
3B	Ring-indicator bit is not set
3C	Status-ready is not set when ring indicator sets
3E	Character-lost status should be set when more than one character sent
40	Function request is set after disable channel
41	External reject when output character
42	Sync is established after four sync characters are sent
43	External reject when output resync command
44	Sync-not-established bit is not set after resync command
45	Character is not sent but was received
46	Carrier-on bit is not set
47	Sync-not-established bit is set after looping character
48	Character received is not the same as character sent
49	External reject when input data
4A	Character-ready is not set
4B	Character-request is set after stop send
4D	No character request after 250 clock pulses
4E	Status-ready is not set on parity error
4F	External reject when stop is sent
50	Status ready bit should not be set
51	Status ready bit should be set
52	External reject when status request
53	Illegal bit in control channel status

#### E. WORD MESSAGES

Word messages are available only if there is a TTY or equivalent available. The following messages are information to the operator.

##### 1. Initialization of the Test

SCCA87 SYNCHRONOUS COMMUNICATION CONTROLLER TEST. (FJ606-A)  
 CP2F, VER. 3.1-1  
 IA=XXXX, FC=XX

2. Parameter Selection

ERROR IN CHANNEL PARAMETER

This indicates that an error was made in the description of channel configurations. After the message is typed, parameter selection will be reentered.

3. Section 6 - Transmit Furnished Characters to Terminal Device

SCCA87 SECTION 6 - SUBMIT CHARS (THE OLD ARE DISPLAYED)  
INCLUDE ANY SYNC CHARS, MSG HEADERS AND EOT, AND PARITY  
MAX 80 CHARACTERS. 0 = END OF MESSAGE

This message alerts the operator that the test is not actively testing but awaiting characters to send.

4. Section 7 - Results of either Test Mode, Single Channel Jumpered Loop,  
or Two Channel Jumpered Loop

SCCA87 SECTION 7 - CHANNEL n LOOP RESULTS

This message alerts the operator that the complete character set (\$20 through \$5F) will follow after looping through the channel.

II. SECTION DESCRIPTIONS

A. SECTION 0 - CONTROLLER STATIC TEST

The following is tested.

1. Controller can be addressed.
2. Clock status is clear after clear controller.
3. Clock status sets.
4. Clock status clears with clear interrupt.
5. Clock status stays set after long delay.
6. Unused bits in clock status word are not set.
7. Controller is not causing unexpected interrupt.
8. Clock can cause interrupt if enabled.
9. Only one interrupt occurs when clock interrupt request is enabled.

## B. SECTION 1 - CHANNEL STATIC TEST

The following is tested.

1. A program clear causes bits 1, 2, and 10 of channel status to be set (all others except bit 6 should be reset), a disable channel command causes bit 10 of channel status to be reset, and an enable channel causes bit 10 to be set.
2. A data input will not cause external reject if channel is disabled.
3. A data output will cause external reject if channel is disabled.
4. A data input will reply if channel is enabled; character request will be set. (All other bits are clear.)
5. If one channel is enabled, all others will reject using data output.
6. A data output will reply if channel is enabled and will reject if the channel is disabled by channel disable.
7. A program clear causes bit 2 of channel status to be set, a disconnect causes bit 2 to be reset, and a connect causes bit 2 to be set.
8. A stop send command resets character-request status bit.
9. A request status command sets the status ready bit of the input control channel.

## C. SECTION 2 - TEST MODE BIT TEST

The following is tested.

1. Select-test-mode and clear-controller causes test mode status bit to be set and reset.
2. Select-test-mode and clear-adaptor causes test mode status bit to be set and reset.
3. Select-test-mode and clear-test-mode causes test mode status bit to be set and reset.

## D. SECTION 3 - ADAPTER LOOP (ECHO) TEST

This section tests the following:

1. Character-ready status bit will not set before test mode is on.
2. A character can be sent and received by the same channel when in test mode.
3. The receipt of sync characters clears the sync-not-established bit.

4. A resync command sets the sync-not-established status bit.
5. Check if sync-not-established status bit sets when complete character set (except \$16) is sent.
6. Send random characters in test mode and check received character against that sent (Loop Test).

E. SECTION 4 - TEST MODE DATA TEST

Send specified characters in test mode and check received character against that sent (Loop Test).

F. SECTION 5 - CHARACTER READY/LOST TEST

The following is tested.

1. Character-ready sets and character- lost does not set erroneously.
2. Character-lost sets correctly.

This test may be repeated if operator enters flag in parameter.

G. SECTION 6 - TRANSMIT FURNISHED CHARACTERS TO TERMINAL DEVICE

1. Pick up message from operator.
2. Clear adapter, enable channel, and request to send.
3. Transmit all characters submitted.
4. Keep looping through submitted characters if prescribed by parameter A5.
5. Do both channels before waiting for interrupt.

H. SECTION 7 - LOOP CHARACTERS AND OUTPUT OF COMMENT DEVICE

Loop the complete character set (\$20 through \$5F) through each active channel and output on the comment device. The test will be repeated if prescribed by parameter A5.

I. SECTION 8 - CHECK CARRIER-ON, RING-INDICATOR, AND STATUS-READY STATUS BITS

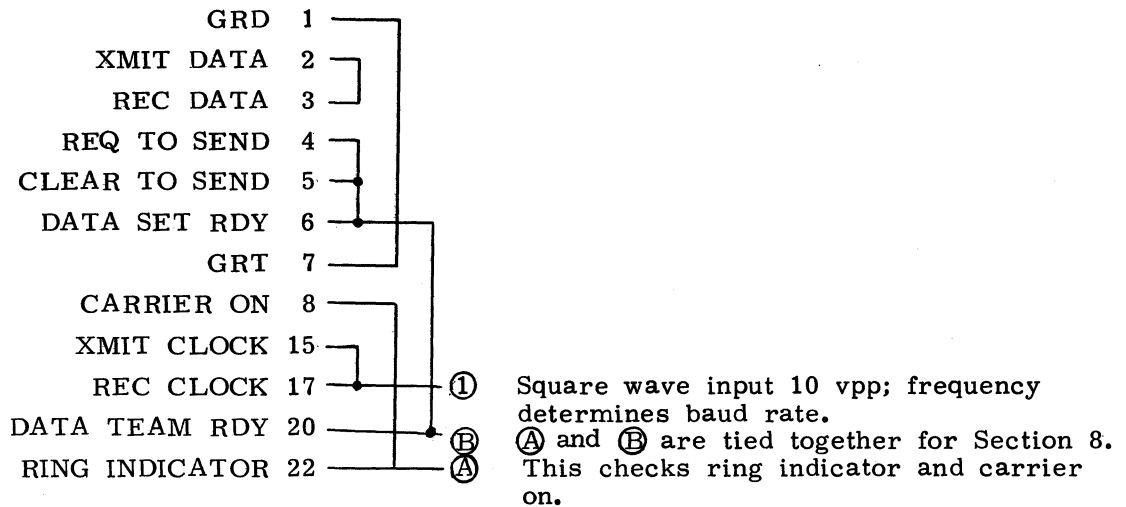
This section tests internal hardware logic only and must be jumpered from request-to-send.

### III. TEST FIXTURES

It is necessary to fabricate the following fixtures if Single Channel Loop or Channel to Channel Loop Tests of test 87 are to be run. The Single Channel Loop Test fixture must also be utilized if Internal Test Mode Tests are to be run and there is no available modem.

#### A. SINGLE CHANNEL LOOP TEST (Transmit and receive on the same channel)

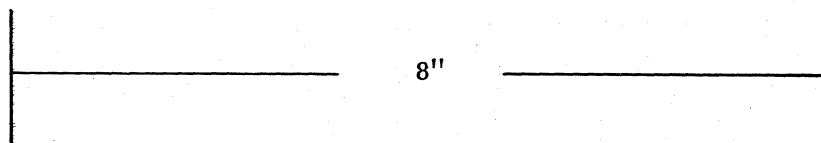
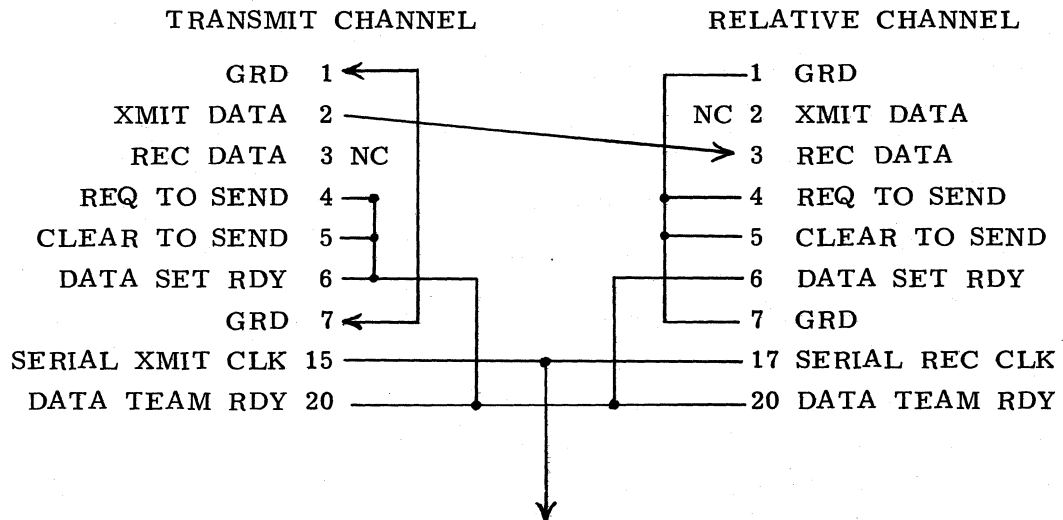
Use connector P/N 93609008 and make the following connections.



- ① This signal must be supplied by a square wave generator or an oscilloscope calibrate output of the proper amplitude. If a modem exists on the system, jumper this line to pin 15 of the connector of the cable connected to the modem.

B. CHANNEL TO CHANNEL LOOP TEST

Use two connectors each (P/N 93609008) and make the following connections.



FJ505 BISYNC CONTROLLER TEST  
(BSC089 Test No. 89)

I. OPERATIONAL PROCEDURE

A. RESTRICTIONS

Specific sections will run only if the Programmable Terminal Exerciser (PTE) is used whether the specific sections are selected or not.

1. If the PTE is selected, it must be started before this test is started (see PTE Loading Procedure).
2. If the modem is selected, it must be in Data mode.

B. LOADING PROCEDURE

1. FJ505 1700 Test Loading Procedure

This test operates under control of 1700 SMM. The calling sequence is that specified by SMM. At SMM initialization, time bits 2 and 3 of SMM's parameter word must correspond to the correct CPU memory speed.

To restart test after loading, Master Clear, set P=1A, and RUN.

2. Direct-Connected PTE Loading Procedure

- a. Connect interface cable to connector labeled RS232 to Terminus.
- b. Connect PTE to appropriate power and turn unit on.
- c. Insert cassette tape cartridge into tape unit.
- d. Set PTE switches as follows:
  - INTERFACE switch to TERMINUS
  - CLOCK switch to INTERNAL
  - MODE switch to NORMAL
  - DISPLAY 3 Select switch to KEYBOARD
  - RUN switch to OFF
  - EXECUTE switch to TAPE
  - ACCESS switch to SWEEP
  - SELECTIVE JUMP/HALT switch to OFF

- DISPLAY 1 Select switch to Z
  - Frequency input thumbwheel switches to the desired bit rate (SMM test parameters are prestored at 2400 BPS.)
- e. Master reset PTE and clear Display 3 via the KEYBOARD CLEAR button if the EBCDIC option in the FJ505 is selected. If the USASCII option is selected, set DISPLAY 3 to 0001.
  - f. Press BOT button under tape unit. After BOT light comes on, press AUTOLOAD button. When tape unit stops, check if the error light under the tape unit is on. If it is on, repeat step f.
  - g. Master reset PTE, set EXECUTE switch to ON and set RUN switch to ON.

PTE program is now running.

### 3. Modem-Connected PTE Loading Procedure

- a. Connect interface cable to connector labeled RS232 to Modem.
- b. Connect PTE to appropriate power and turn unit on.
- c. Insert cassette tape cartridge into tape unit.
- d. Set PTE switches as follows:
  - INTERFACE switch to MODEM
  - CLOCK switch to EXTERNAL
  - MODE switch to NORMAL
  - DISPLAY 3 Select switch to KEYBOARD
  - RUN switch to OFF
  - EXECUTE switch to TAPE
  - ACCESS switch to SWEEP
  - SELECTIVE JUMP/HALT switch 1 to OFF if phone line is four-wire dedicated
  - JUMP/HALT switch 1 to JUMP if phone line is two-wire dial up
  - DISPLAY 1 switch to Z
- e. Type 2c, 2f, and 2g.



### C. PARAMETERS

1. If a PTE is used, normal operation requires no parameter changes.
  - a. All sections will be run under this condition.
  - b. The test will run on equipment F, and interrupt line 15 will be used.
  - c. The PTE bit rate switches must be set to 2400 bits per second or faster.
2. To alter the parameters, follow the directions stated in the SMM17 Reference Manual. If the bit is set, the corresponding section or conditions will be selected.

The parameter words to be displayed are as follows:

a. First Stop

A = Test ID word (8941)

Q = Test Stop/Jump parameters

Bit 0 Stop to enter test parameters

Bit 1 Stop at end of test section (no typeouts)

Bit 2 Stop at end of test pass (timeout unless bit 8 is set)

Bit 3 Stop on error (timeout unless bit 8 is set)

Bit 4 Repeat conditions

Bit 5 Repeat current test section

Bit 6 Repeat test

Bit 7 Not used

Bit 8 Omit typeouts

Bit 9 Return address corresponds to memory locations rather than program listing

Bit 10 Re-enter test parameters (bit 0 must also be set)

Bit 11 Display only one data compare error per buffer

b. Second Stop

A = Interrupt line number

If bit 0 of Stop/Jump parameter word is set, a stop occurs with bit 15 in the A register set. This bit specifies Interrupt Line F.

If the FJ505 uses a different interrupt line, the operator must clear the A register, set the bit corresponding to the correct interrupt line, and run.

Q = Section select (prestored to run all sections)

Bit 0 = Section 1	Function test
Bit 1 = Section 2	Interrupt test
Bit 2 = Section 3	Data Pattern test 1
Bit 3 = Section 4	Data Pattern test 2

c. Third Stop

A = Equipment type (prestored as 0000)

Bit 0 = 0	PTE selected
1	Modem only
Bit 2 = 0	Four-wire modem with or without PTE
1	Two-wire dial up modem with or without PTE
Bit 3 = 0	Unprotected
1	Protected
Bit 4 = 0	EBCDIC mode
1	USASCII mode

Q = Not used

d. Fourth Stop

A = Upper BCD digit of line speed (prestored as 0000)

Bit 0 = 0	Line speed of 9999 bits per second or less
1	Line speed of 10,000 to 19,999 bits per second

Q = Lower four BCD digits of line speed (prestored as 2400)

## II. OPERATOR COMMUNICATION

### A. MESSAGE FORMATS

#### 1. Normal Program Typeouts

##### a. Initialization of Test

BSC089 CYBERDATA BISYNC CONTROLLER TEST

IA = XXXX FC = 01

##### b. End of One Pass through Test

A1	Q1	A2	Q2
8924	STOP/JUMP	PASS COUNT	RETURN ADDRESS

##### c. Set PROTECT switch and Go

If in parameter stop 3 with bit 3 of A set, this type will occur and the test will halt. Set the PROTECT switch and push GO.



## 2. Message Description

### a. 01 - Internal Reject - Function

A1	Q1	A2	Q2	A3	Q3	A4	Q4
8948	STJP	SS01	RTN	ACTST	EXPST	(A)	(Q)

STJP                    Stop/Jump parameter word

SS01                    Section/subsection and error code

RTN                     Return address

ACTST                  Actual status (not used)

EXPST                  Expected status (not used)

A, Q                    Register contents relative to last I/O operation

A function command was issued to the controller and an internal reject was encountered. Q4 contains the equipment number that was issued, and A4 contains the function code that was issued.

### b. 02 - External Reject - Function

The format is the same as 01 error format.

A function command was issued to the controller and an external reject was encountered. A4 contains the function code, and Q4 contains the equipment number that was issued.

### c. 03 - Data Compare Error

A4	Q4	A5	Q5	A6	Q6
(A)	(Q)	ACTDAT	EXPDAT	CTN	0000

A, Q                    Register contents relative to last I/O operation

ACTDAT                 Actual data received in input buffer

EXPDAT                 Expected data

CTN                    Character count - Relative position of character in error in receive buffer

A data buffer was sent out from the FJ505 to the PTE, and the PTE sent it back to the FJ505. After the buffer was successfully received, a compare is done between the transmitted data and the received data. If they do not compare, this error is displayed.

d. 04 - Internal Reject - Status

The format is the same as 01 error format.

A copy status command was issued to the controller, and an internal reject was encountered. Q4 contains the equipment number that was issued.

e. 05 - External Reject - Status

The format is the same as 01 error format.

A copy status command was issued to the controller, and an external reject was encountered. Q4 contains the equipment number that was issued.

f. 07 - Internal Reject - Data Out

The format is the same as 01 error format.

A write command was issued to the controller, and an internal reject was encountered. A4 contains the data that was trying to be output, and Q4 contains the equipment number that was issued.

g. 08 - External Reject - Data Out

The format is the same as 01 error format.

A write command was issued to the controller, and an external reject was encountered. A4 contains the data that was trying to be output, and Q4 contains the equipment number that was issued.

h. 0A - Internal Reject - Data Input

The format is the same as 01 error format.

A read command was issued to the controller, and an internal reject was encountered. Q4 contains the equipment number that was issued.

i. 0B - External Reject - Data Input

The format is the same as 01 error format.

A read command was issued to the controller, and an external reject was encountered. Q4 contains the equipment number that was issued.

j. 0E - Unexpected Interrupt Error

A1	Q1	A2	Q2	A3	Q3	A4	Q4
8948	STJP	SSOE	RTN	ACTST	N/I	(A)	(Q)

STJP	Stop/Jump parameters
SSOE	Section/subsection and error code
RTN	Return address
ASTST	Last status copied after interrupt occurred and before clear interrupt function was issued
N/I	Not important
A, Q	Register contents relative to clear interrupt function

An interrupt was detected at a time when no interrupt was expected. A3 contains the status that was copied after the interrupt was detected and before a clear interrupt function is issued.

k. 0F - Function Status Error

Format 1:

A1	Q1	A2	Q2	A3	Q3	A4	Q4	A5	Q5
8958	STJP	SSOF	RTN	ACTST	EXPST	(A)	(Q)	MASK	N/I

STJP	Stop/Jump parameters
SSOF	Section/subsection and error code
RTN	Return address
ACTST	Actual status
EXPST	Expected status
A, Q	Register contents relative to last I/O operation
MASK	Status mask that was used to compare the actual status against the expected status
N/I	Not important

Status other than expected was received. The copied status in A3 is masked with the mask in A5 and compared against the expected status in Q3. If they do not compare, this error is detected.

Format 2:

A1	Q1	A2	Q2	A3	Q3	A4	Q4	A5	A6	Q6
8968	STJP	SSOF	RTN	ACTST	EXPST	(A)	(Q)	MASK	TIME	COOB

RTN	Return address
ACTST	Actual status
EXPST	Expected status
A, Q	Register contents relative to last I/O operation
MASK	Status mask that was used to compare the actual status against the expected status
N/I	Not important
TIME	Time in milliseconds which expired waiting for the specified condition to occur
COOB	Control word used to monitor status

B= Bit position  
 C= 8 - Waiting for bit to go from on to off  
 0 - Waiting for bit to go from off to on

The status that is being copied while waiting for the selected bit to change was in error. The mask in A5 is used to compare the expected status in Q3 against the actual status in A3. If a non-compare is detected, this error is displayed.

1. 10 - Send Data Timeout Error

A1	Q1	A2	Q2	A3	Q3	A4	Q4	A5	Q5
8958	STJP	SS10	RTN	N/I	N/I	(A)	(Q)	TIME	N/I

STJP	Stop/Jump parameters
SS10	Section/subsection and error code
RTN	Return address
N/I	Not important
Q, A	Register contents relative to last I/O operation

Data outputs were attempted by repeating on rejects and continuing on reply. The time allotted for the output instruction to reject has expired.

m. 11 - Receive Data Timeout Error

The format is the same as 10 error format.

Data inputs were attempted by repeating on rejects and continuing on reply. The time allotted for the input instruction to reject has expired.

n. 12 - Status Change Timeout Error

The format is the same as 0F error format, of format 2.

The time has expired, waiting for bit position B in Q6 to change.

o. 13 - Data Interrupt Timeout Error

A1	Q1	A2	Q2	A3	Q3	A4	Q4	A5	Q5
8958	STJP	SS13	RTN	ACTST	EXPST	(A)	(Q)	TIME	N/I

STJP	Stop/Jump parameters
SS13	Section/subsection and error code
RTN	Return address
ACTST	Status copied after error
EXPST	Expected status
A, Q	Register contents relative to last I/O operation
TIME	Time in milliseconds which expired waiting for the data interrupt

The time expired waiting for a data interrupt. By looking at the expected status in Q3, it can be determined whether input data interrupt or output data interrupt was expected. The status in A3 is the status copied after the timeout occurred.

p. 14 - EOM Interrupt Timeout Error

The format is the same as 13 error format.

A data pattern was sent out that should generate an EOM interrupt which did not occur within the allotted time. By looking at the expected status in Q3 it can be determined whether an input EOM interrupt or an output EOM interrupt was expected. The status in A3 is the status copied after the timeout occurred.

q. 15 - CXR On Interrupt Timeout Error

The format is the same as 13 error format.

A CXR on interrupt was not detected in the allotted time. The status in A3 is the status copied after the timeout occurred.

r. 16 - CXR Off Interrupt Timeout Error

The format is the same as 13 error format.

A CXR off interrupt was not detected in the allotted time. The status in A3 is the status copied after the timeout occurred.



### III. SECTION DESCRIPTIONS

This test consists of four sections with several subsections. All sections will be executed unless the section select bits are altered by the operator.

#### A. SECTION 1 - FUNCTION STATUS TEST

1. Subsection 1 - Check Clear Controller Function

A clear controller function is issued and status is checked.

2. Subsection 2 - Check Clear Controller Function with Interaction Bits Set.

A clear controller function with all the bits set that a clear controller will take precedence over are sent, and status is checked.

3. Subsection 3 - Check Connect Function

A connect function is sent, and status is checked.

4. Subsection 4 - Check Disconnect Function

A disconnect function is sent, and status is checked.

5. Subsection 5 - Check Clock Function

A request clock timeout function is sent, and after a 1100-millisecond delay, status is checked.

6. Subsection 6 - Check Select TR Mode and Select RC Mode

TR mode is functioned, an 11-character buffer is sent, RC mode is functioned, and if the PTE is selected, the data is received and checked.

7. Subsection 7 - Check EOM Status with ETX

A data buffer with SOH as the first character and ETX as the last character is sent out. EOM status is checked after the buffer is sent. If the PTE is being used, EOM status is checked on the received buffer.

8. Subsection 8 - Check EOM Status with ETB

A data buffer with SOH as the first character and ETB as the last character is sent out. EOM status is checked after the buffer is sent. If the PTE is being used, EOM status is checked on the received buffer.

#### B. SECTION 2 - INTERRUPT TEST

1. Subsection 1 - Clock Interrupt Test

A start timeout and timeout interrupt request function is sent to the controller. A total of 1100-milliseconds is allowed for the interrupt to occur.

2. Subsection 2 - Data Interrupt Test

A select TR mode and data interrupt request function is issued. A total of 250-milliseconds is allowed for the data interrupt to occur.

3. Subsection 3 - EOM Interrupt Test

A data buffer with SOH as the first character and ETX as the last character is sent out. An EOM interrupt is expected after the buffer is sent. If the PTE is being used, an EOM interrupt is expected at the end of the receive buffer.

C. SECTION 3 - DATA PATTERN TEST 1

This section transfers data using data request interrupts. If the PTE is not used, this section is bypassed.

1. Subsection 1 - Data Pattern Test of All Ones

A 65-character data buffer with SOH as the first character, ETX as the last character, and the remaining characters having all bits set is sent and received. A character by character compare of the receive buffer against the transmit buffer is done. This subsection is repeated 10 times.

2. Subsection 2 - Data Pattern Test of All Zeros

A 65-character data buffer with SOH as the first character, ETX as the last character, and the remaining characters having all bits cleared is sent and received. A character by character compare of the receive buffer against the transmit buffer is done. This subsection is repeated 10 times.

3. Subsection 3 - Data Pattern Test of Alternating Ones and Zeros

A 65-character data buffer with SOH as the first character, ETX as the last character, and the remaining characters having an alternating one-zero pattern is sent and received. A character by character compare of the receive buffer against the transmit buffer is done. This subsection is repeated 10 times.

4. Subsection 4 - Random Data Pattern Test

A 65-character data buffer with SOH as the first character, ETX as the last character, and random data in the remaining characters is sent and received. A character by character compare of the receive buffer against the transmit buffer is done. The subsection is repeated 100 times.

#### D. SECTION 4 - DATA PATTERN TEST 2

This section transfers data using data request status. If the PTE is not used, this section is bypassed.

##### 1. Subsection 1 - Data Pattern Test of All Ones

A 65-character data buffer with STX as the first character and the remaining characters having all bits set is sent and received. A character by character compare of the receive buffer against the transmit buffer is done. This subsection is repeated 10 times.

##### 2. Subsection 2 - Data Pattern Test of All Zeros

A 65-character data buffer with STX as the first character, ETX as the last character, and the remaining characters having all bits cleared is sent and received. A character by character compare of the receive buffer against the transmit buffer is done. This subsection is repeated 10 times.

##### 3. Subsection 3 - Data Pattern Test of Alternating Zeros and Ones

A 65-character data buffer with STX as the first character, ETB as the last character, and the remaining characters having an alternating zero-one pattern is sent and received. A character by character compare of the receive buffer against the transmit buffer is done. This subsection is repeated 10 times.

##### 4. Subsection 4 - Random Data Pattern Test

A 65-character data buffer with STX as the first character, ETB as the last character, and random data in the remaining characters is sent and received. A character by character compare of the receive buffer against the transmit buffer is done. This subsection is repeated 100 times.



## IOM MOTHER UNIT DIAGNOSTIC

(IOM090 Test No. 90)

### I. OPERATING PROCEDURES

#### A. RESTRICTIONS/LIMITATIONS

1. Interrupt lines may not be defined in Stop 7 without also defining sync timing in Stop 8. Sync timing may be defined without defining interrupts.
2. The data values defined in Stop 6 will be used only if bits 5, 9, or 11 of A register Stop 3, test sections and data patterns, are selected. If Q register bit 02 is selected (non-changing data), the first digital data value defined in Stop 6 will be repeated as the output value. If bit 3 is selected (alternating data), both digital values defined in Stop 6 will be output.
3. Any combination of data patterns may be defined with any combination of data transfer test sections.
4. Only one type of sync may be defined for test execution. Repetitive sync (bit 12) is to accommodate a cyclic sync signal as would be available from a test oscillator or peripheral equipment. Multiple words will be transferred through each data channel. Manual sync (bit 13) is to accommodate one sync pulse per data channel, which might be generated by switches or test clip leads. Only one word is transferred through each data channel.
5. Test Section 6 requires that the operator ground a test point to produce an interrupt. This ground must be maintained at least for 2 seconds to combat contact bounce.
6. Bit A15 of Stop 3 (Address Increment) must be set to properly execute test Sections 0 through 5. With this bit set, the I/O address will increment when a monitor stop is processed. If not set, the address will not change.

#### B. LOADING PROCEDURE

This test is to be loaded as a standard SMM17 3.0 Library Test. The test may be loaded anywhere in core memory by using the following optional procedure when building the test execution list:

1. (A) is normally the test number and number of times to be run. Set the A register to \$FF00 test number \$FF to be run 0 times.

2. (Q) is normally the equipment number of the device under test. Set the Q register to the desired core location to begin loading the test. This location must not be less than \$0D00 so as not to destroy the monitor.

Standard execution parameters from load time are to execute test Sections 9, 10, and 11 (write only, read only, and write/read closed loop). These sections will be executed using all six data patterns (sliding 1's, sliding 0's, unchanging (repetitive 0's) alternating data (all 0's, all 1's), pseudo - random data, and frequency sensitive data). This data will be output on unit address 000 through 003 and read back in through addresses 004 through 007. The equipment code used will be that established while building the test list. These data transfers will be asynchronous without interrupts. For a valid data check, 1 to 1 cables must be used to transfer the data from the digital outputs to the digital inputs.

Sections 0 through 6 are to be used when troubleshooting suspected hardware. Flexibility has been built in through the operator defined parameters to cover most if not all failure modes. Hand routines should not be required.

#### C. PARAMETERS

If bit 0 of the Stop/Jump parameter is set, the test will stop for one monitor stop and seven parameter stops as follows:

Stop 1:	A:	ID Word
	Q:	SMM Stop/Jump Word
Stop 2:	A:	Unused
	Q:	Equipment Number for Data Writes
Stop 3:	A:	Sections to Run (Figure 1)
	Q:	Data Patterns to Run (Figure 1)
Stop 4:	A:	Starting Unit Address - Writes
	Q:	Ending Unit Address - Writes
Stop 5:	A:	Starting Unit Address - Reads
	Q:	Equipment Number for Reads
Stop 6:	A:	First Digital Output Word
	Q:	Alternate Digital Output Word
Stop 7:	A:	Interrupt Line for Output Units*
	Q:	Interrupt Line for Input Units*
Stop 8:	A:	Time to Wait for Interrupts, milliseconds
	Q:	Time to Wait for Interrupts, microseconds

\*Bit 1 defines line 1, Bit 2 defines line 2, etc.

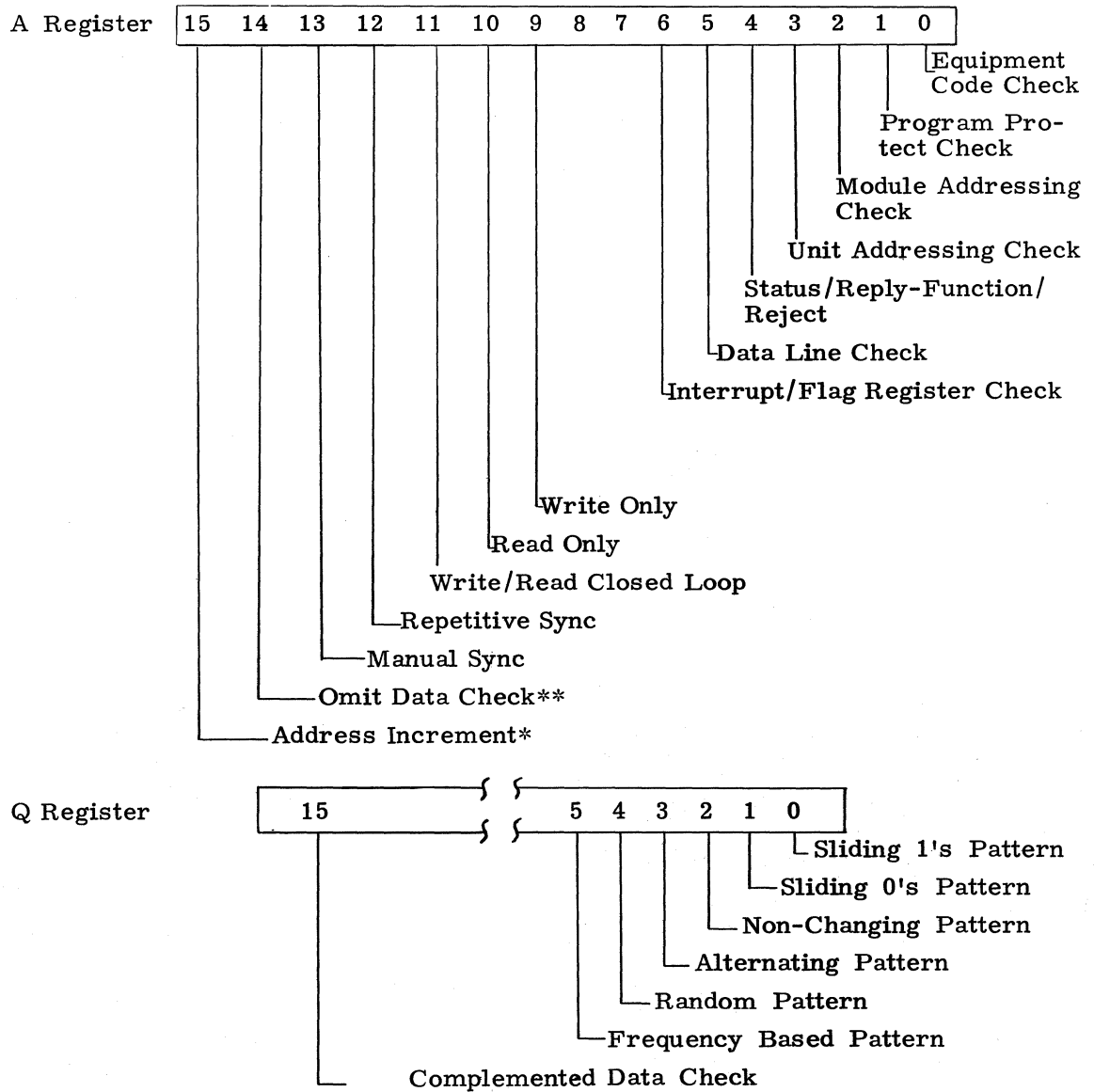


Figure 1. Parameter Stop 3  
Test Sections/Data Patterns

\*Must be set to increment the I/O address in Sections 0 through 5.

\*\*Set to delete the data check of Section 11.

#### D. STOP AND JUMP SETTINGS

Bit settings in the Stop/Jump word are the standard SMM assignments.

<u>Bit</u>	<u>Stops</u>
0	Stop to Enter Test Parameters
1	Stop at End of Test Section
2	Stop at End of Test
3	Stop on Error
	<u>Jumps</u>
4	Repeat Conditions
5	Repeat Test Section
6	Repeat Test
7	Not Used
8	Omit Typeouts
9	Display Memory Return Address
10	Re-enter Test Parameters

#### E. MESSAGES

##### 1. Initial Program Typeout

IOM Mother Unit

Digital Output/Input Test 90

VER 3.1 IA = aaaa FC = xxxx

aaaa = Test Initial Address

##### 2. Completed Pass Typeout

A	Q	A	Q
9024	NUM 1	NUM 2	NUM 3

NUM 1 = SMM Stop/Jump Word

NUM 2 = Pass Count

NUM 3 = Return Address

##### 3. Parameter Stop Typeout

After completing each parameter stop (Stop 0), the parameter block will be typed out. For this test there will be eight A/Q pairs of data presented.



#### 4. Teletype Input Driver

Setting bit 6 of the monitor control word prior to executing quick look or during any monitor parameter stop, will select the teletype input driver. This driver will allow all operator intervention to be done through the TTY rather than from the console registers. The following are the general guide lines controlling the use of this driver:

- a. The driver will first type two 4-character hexadecimal numbers which represent an A/Q pair of standard or current parameters to be altered, followed by a line feed, carriage return = 9001/0600.
- b. The operator now has the following options:
  - 1) A carriage return will signify the input is complete. If this is the only input, no parameter changes will take place.
  - 2) A slash will signify the end of one parameter input. An input of: /0 CR will indicate the parameter output is to be changed in core to be 9001/0000.
  - 3) All hexadecimal numbers on input must be preceded by a dollar sign. No prefixing character signifies a decimal number.
  - 4) The operator may set selected bits in a parameter word by preceding the bit numbers by a B, using commas as number separators:  
  
/B, 15, 11, 7, 3 CR would result in the parameter being changed to 9001/8888.
  - 5) Pressing MANUAL INTERRUPT will result in calling for an immediate monitor parameter stop.

#### 5. Error Messages

A1	Q1	A2	Q2	A3	Q3	A4	Q4	A5	Q5
ID	STJP	SSEE	RTN	MTRERR	IORP	A4	Q4	A5	Q5

##### Definitions:

ID: SMM Identification Word  
STJP: SMM Stop/Jump Parameter Word  
SSEE: Test Section and Error Pointer  
RTN: Return Address  
MTRERR: Monitor Error Code

- 02 - I/O Response Error
- 03 - Status Error
- 04 - Interrupt Time Out Error
- 05 - Data Compare Error

IORP: Last I/O Operation Performed and the Associated Response

- IO: 10-Write
- 20-Read
- 30-Function
- 40-Status

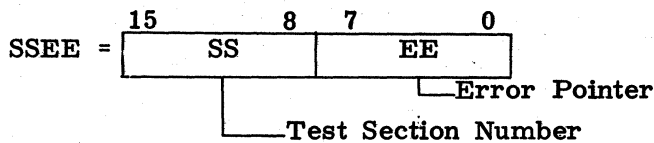
- RP: 10-Reply
- 20-External Reject
- 30-Internal Reject

For monitor error code MTRERR=05, and text section error pointer SSEE=XX20, IORP=word count of data miscompare.

The information reported in A4, Q4, A5, and Q5 varies with the monitor error code, as defined below.

<u>MTRERR:</u>	<u>A4</u>	<u>Q4</u>	<u>A5</u>	<u>Q5</u>
02	Contents A Register	Contents Q Register	-	-
03	Contents A Register	Contents Q Register	Actual Status	Expected Status
04			Interrupt Line	Expired Time, ms
05	Input Data	Output Data	Input Channel Addr.	Output Channel Addr.

The SSEE parameter reports the specific location within the test the monitor error code has occurred. This parameter is defined as follows:



The test section numbers are defined as follows:

- 00 - Equipment Code Check
- 01 - Program Protect Check
- 02 - Module Addressing Check
- 03 - Unit Addressing Check
- 04 - Status/Reply - Function/Reject Check
- 05 - Data Line Check
- 06 - Interrupt/Flag Register Check
- 09 - Write Only
- 0A - Read Only
- 0B - Write/Read Closed Loop

The error pointers are defined as follows:

- 01 - Copying Status from the IOM
- 02 - Outputting A Function to the IOM
- 03 - Outputting Data to the IOM
- 04 - Inputting Data from the IOM
- 05 - Processing a Write Interrupt
- 06 - Processing a Read Interrupt
- F0 - Operator Error - Sync I/O  
Defined, But No Time Period Defined
- F1 - Section 6, No Interrupt Line Defined
- 10 - Section 6, Interrupt Time Out Error
- 11 - Section 6, Status Error Prior to Receiving an Interrupt
- 12 - Section 6, Status Error After Receiving an Interrupt
- 13 - Section 6, Status Time Out Error After Receiving an Interrupt
- 20 - Section 11, Data Compare Error

## II. DESCRIPTION

### A. SECTION 0: EQUIPMENT CODE CHECK

The purpose of Section 0 is to allow checking of the equipment number decoding within the IOM mother unit. This section is a Hardware Exerciser only and no errors are reported by this test section. The operator is to investigate any suspect logic within the select decoding area of the IOM with an oscilloscope.

To execute this section, the operator must define or select the following entry parameters:

- |                      |     |        |
|----------------------|-----|--------|
| 1. Section 0         | A00 | Stop 3 |
| 2. Address Increment | A15 | Stop 3 |

The section will begin executing repetitive I/O to equipment number 0.

The section will remain looping on one address indefinitely without operator intervention. Test point 23 or used position 2 is the end result of the select logic and should be a 7 kHz pulse train if the hardware equipment code is jumped to match the address output by the test.

After all pertinent observations have been made, the operator must set the SKIP switch to request a monitor stop to continue the test.

During the monitor stop, the operator is to change the IOM equipment select jumper in order to select the next equipment number from 0 to 1, 1 to 2, etc., if such a check is required.

After processing the monitor stop, the test will continue execution with the equipment number incremented by 1, the I/O address incremented by \$0080.

To increment each succeeding equipment number, the operator is to change the equipment jumper and call for a monitor stop. The section will be completed after processing the monitor stop following I/O address \$0780.

#### B. SECTION 1: PROGRAM PROTECT CHECK

Section 1 executes repetitive reads from the IOM using the following address:

1. The equipment code defined in Q, Stop 2.
2. The module address defined in A, Stop 4.
3. Unit addresses of zero.

To execute this section, the operator must select or define the following:

- |                      |            |        |
|----------------------|------------|--------|
| 1. Equipment Code    | Q Register | Stop 2 |
| 2. Section 1         | A01        | Stop 3 |
| 3. Address Increment | A15        | Stop 3 |
| 4. Module Address    | A Register | Stop 4 |

All pertinent errors are reported by this test section.

Messages will be presented to the operator, if a TTY is present in the system, on how to set and clear the console PROTECT switch, and when to protect and unprotect the IOM. The section will increment through all four protect conditions in the following order:

1. Unprotected core executing I/O to an unprotected IOM.
2. Protected core executing I/O to an unprotected IOM.
3. Protected core executing I/O to a protected IOM.
4. Unprotected core executing I/O to a protected IOM.

The section will proceed to the next protect condition 10 seconds after each monitor stop. The operator is expected to set the console switches and/or change the IOM protect jumpers during the monitor stop or during the 10 second delay. Possible monitor protect violations may occur if this is not observed.

The section will exit after processing the monitor stop following the fourth protect condition.

C. SECTION 2: MODULE SELECT CHECK

The purpose of Section 2 is to allow checking of the module select decoding of the IOM mother unit. This section is a Hardware Exerciser only and no errors are reported by this test section. The operator is to investigate any suspect logic within the module select decoding area of the IOM with an oscilloscope.

To execute this section, the operator must define or select the following entry parameters:

1. Equipment Code	Q Register	Stop 2
2. Section 2	A02	Stop 3
3. Address Increment	A15	Stop 3
4. Starting Module Address	A Register	Stop 4
5. Ending Module Address	Q Register	Stop 4

The section will begin executing repetitive I/O to the starting address defined in Stops 2 and 4. The section will remain looping on one address indefinitely without operator intervention.

The following test points on card 2 will become logical 0 (during the read cycle) only for the respective address listed.

<u>Address</u>	<u>Card 2 Test Point</u>
\$0600	12
\$0610	13
\$0620	14
\$0630	15
\$0640	16
\$0650	17
\$0660	18
\$0670	19

Test point 29 on card 5 (master) will go to a logical 1 when a read cycle is performed on address \$0600. Test point 29 on card 5 (slave) will go to a logical 1 when a read cycle is performed on address \$0610, and so on for all slave units configured within the system.

The operator must set the SKIP switch to request a monitor stop to continue the test.

During the monitor stop, the operator is to change the slave select jumper so to select the next slave unit. After processing the monitor stop, the test will continue execution, now with the module address incremented by 1 - the I/O address incremented by \$0010.

To increment each succeeding module address, the operator is to change the slave select jumper and call for a monitor stop. The section will be completed after processing the monitor stop following the testing of the ending module address.

#### D. SECTION 3: UNIT SELECT CHECK

The purpose of Section 3 is to allow checking of the unit select decoding within an IOM mother or slave unit. This section is a Hardware Exerciser only and no errors are reported by this test section. The operator is to investigate any suspect logic within the unit select decoding area of the IOM with an oscilloscope.

To execute this section, the operator must define or select the following entry parameters:

1. Equipment Code	Q Register	Stop 2
2. Section 3	A03	Stop 3
3. Address Increment	A15	Stop 3
4. Starting Unit Address	A Register	Stop 4
5. Ending Unit Address	Q Register	Stop 4

The section will begin executing repetitive I/O to the starting address defined in Stops 2 and 4. The section will loop on one address indefinitely without operator intervention.

The following test points on card 5 (master) will become logical 0 (during the read cycle) only for the respective address listed.

<u>Address</u>	<u>Card 5 Test Point</u>
\$0600	1
\$0601	2
\$0602	3
\$0603	4
\$0604	5
\$0605	6
\$0606	7
\$0607	8
\$0608	9
\$0609	10
\$060A	11
\$060B	12
\$060C	13

<u>Address</u>	<u>Card 5 Test Point</u>
\$060D	14
\$060E	15
\$060F	16

After all observations have been made, the operator must set the SKIP switch to request a monitor stop to continue the test. After processing the monitor stop, the test will continue execution, now with the unit and I/O addresses incremented by 1. The section will be completed after processing the monitor stop following the testing of the ending unit address.

After observing any suspect logic, the operator must set the SKIP switch to request a monitor stop to continue the test.

After processing each monitor stop, the I/O addresses will be incremented by \$0010 and status inputs will again be executed, this time from the next module present. After processing the monitor stop following testing of the ending module address, the section will reset the addresses to the starting module address and begin executing repetitive function outputs.

To verify proper reject logic operation the operator should do the following:

1. Place an extender board in card position 8 (master). Connect a jumper between extender board pin A13 and test point 18 on card 5 (master).
2. The test will perform Write operations to the starting address. Verify 425 nanosecond  $\pm 10$  percent time delay between test point 20 (negative trigger) on card 2 and test point 18 on card 5 (master). Verify delay of 640 nanoseconds  $\pm 10$  percent between test point 20 (positive trigger) on card 5 (master) and test point 28 on card 4 (master). External rejects will occur. The test will report any replies or internal rejects as errors.

After observing any suspect logic, the operator must set the SKIP switch to request a monitor stop to continue the test.

After processing each monitor stop, the I/O addresses will be incremented by \$0010 and function outputs will again be executed, this time to the next module present. The address incrementing will be as for the status input portion of this section. The section will exit after processing the monitor stop following testing of the ending module address.

E. SECTION 4: STATUS REPLY/FUNCTION REJECT

The purpose of Section 4 is to allow checking of the status and function responses of IOM module control cards. The section will expect replies from the flag/status logic during status inputs and external rejects during function outputs.

To execute this section, the operator must define or select the following entry parameters:

- |                            |            |        |
|----------------------------|------------|--------|
| 1. Equipment Code          | Q Register | Stop 2 |
| 2. Section 4               | A04        | Stop 3 |
| 3. Address Increment       | A15        | Stop 3 |
| 4. Starting Module Address | A Register | Stop 4 |
| 5. Ending Module Address   | Q Register | Stop 4 |

The section will begin executing repetitive status inputs from the starting address defined in Stops 2 and 4. The section will loop on the starting address, doing status inputs, until operator intervention.

To verify proper reply logic operation, the operator should do the following:

Verify 425 nanosecond  $\pm 10$  percent time delay between test point 21 (negative trigger) on card 2 and test point 1 on card 5 (master). Verify delay of 640 nanoseconds  $\pm 10$  percent between test point 19 (positive trigger) on card 5 (master) and test point 27 on card 4 (master). The test will report any rejects as an error.

F. SECTION 5: DATA LINE OUTPUT CHECK

Section 5 executes repetitive outputs to the IOM using the following address:

1. The equipment code defined in Q, Stop 2.
2. The module and unit addresses between the limits defined by the starting and ending addresses in Stop 4.

This section will expect internal rejects when executing the data outputs.

To execute this section, the operator must define or select the following:

- |                          |            |        |
|--------------------------|------------|--------|
| 1. Equipment Code        | Q Register | Stop 2 |
| 2. Section 5             | A05        | Stop 3 |
| 3. Address Increment     | A15        | Stop 3 |
| 4. Starting Unit Address | A Register | Stop 4 |
| 5. Ending Unit Address   | Q Register | Stop 4 |
| 6. First Data Pattern    | A Register | Stop 6 |
| 7. Second Data Pattern   | Q Register | Stop 6 |



Both data patterns of Stop 6 will be output to each of the addresses within the limits specified in Stop 4. The two data patterns will alternate, a new pattern output each time a monitor stop is processed. Every second monitor stop, after both patterns have been output to a channel, the I/O address will increment by \$0001. The section will exit after processing the monitor stop following the outputting of both data patterns to the ending I/O address.

#### G. SECTION 6: INTERRUPT FLAG STATUS CHECK

The purpose of Section 6 is to check all 8 interrupt lines of an IOM module and all 16 flag status bits. This section will report all appropriate errors during the interrupt processing and status checking.

To execute this section, the operator must define or select the following entry parameters:

1. Equipment Code	Q Register	Stop 2
2. Section 6	A06	Stop 3
3. Manual Sync	A13	Stop 3
4. Input Interrupt Line*	Q Register	Stop 7
5. Interrupt Wait Time	A or Q Register	Stop 8

This test section is to be executed with manually producing interrupts and manually moving the interrupt cable from connector to connector on the IOM module. To allow enough time to accomplish this and to prevent diagnostic time out errors, the interrupt wait time should be set to a large number in the A register, Stop 8, representing a large time in milliseconds. An A register parameter of \$4000 milliseconds will allow 16.3 seconds for an interrupt to be generated.

To begin Section 6 execution, the interrupt cable must be connected to the IOM interrupt line 1 connector. With the test running, the operator is to ground test point 1 of the flag/status card to produce a status of \$0001 and an interrupt on IOM line 1. The diagnostic will have been checking the flag status to verify that no status bits are set prior to receiving the interrupt. When the ground is made, an interrupt will be generated and sent to the mainframe, and the flag/status will be set to \$0001. The diagnostic will verify the receipt of the interrupt and the proper status, and then ring the teletype bell to verify this to the operator.

After the bell, the operator is to advance the interrupt cable to the next IOM connector ( 1 to 2, 2 to 3, etc. ) then ground the next test point in sequence ( 1 to 2, 2 to 3, etc. ).

\* Defined at the mainframe, not the IOM.

After grounding test points 1 through 8 to check interrupts 1 through 8 and flag/status bits 0 through 7, the operator need only ground the remaining test points 9 through 16 without moving the interrupt cable. Only the flag/status bits are checked. Again the TTY bell will signal to the operator receipt of the proper flag/status bit.

The section will be completed after processing the eight interrupts associated with flag/status bits 0 through 7 and receiving flag/status bits 8 through 15.

#### H. SECTION 9: WRITE ONLY

The purpose of Section 9 is to execute repetitive writes to the unit addresses defined, in asynchronous or synchronous mode, with or without interrupts, as defined by the operator parameters. This is an open ended test, no data checking is attempted.

To execute this section, the operator must select or define the following:

1. Equipment Code	Q Register	Stop 2
2. Section 9	A09	Stop 3
3. Data Patterns	Q Register	Stop 3
4. Starting Unit Address	A Register	Stop 4
5. Ending Unit Address	Q Register	Stop 4
6. First Data Word	A Register	Stop 6
7. Alternate Data Word	Q Register	Stop 6

If the section is to run synchronous, the operator must define the following:

1. Manual Sync or	A13	Stop 3
Repetitive Sync	A12	Stop 3
2. Sync Wait Time	A or Q Register	Stop 8

If the section is to run synchronous with interrupts, the operator must define the following:

1. Manual Sync or	A13	Stop 3
Repetitive Sync	A12	Stop 3
2. Write Interrupt Line	A Register	Stop 7
3. Interrupt Wait Time	A or Q Register	Stop 8

If asynchronous or repetitive sync mode is selected, the section will transfer a total of 3100 words per data pattern selected. If manual sync is defined, one word per unit address will be transferred.

When operating in manual sync mode, the operator must short card pin A29 (request) to card test point 22 (reply). The Reply signal is used as a pulse to trigger the sync circuits. If request is grounded, or remains connected to test point 22 for any length of time, the test will apparently execute two passes per sync. In reality the Request signal is not being removed fast enough by the operator and one pass is completed on setting the Request signal, and one pass is completed on clearing the Request signal.

I. SECTION 10: READ ONLY

The purpose of Section 10 is to execute repetitive reads to the unit addresses defined, in asynchronous or synchronous mode, with or without interrupts, as defined by the operator parameters. This is an open ended test, no data checking is attempted.

To execute this section, the operator must select or define the following:

- |                          |            |        |
|--------------------------|------------|--------|
| 1. Section 9             | A09        | Stop 3 |
| 2. Data Patterns         | Q Register | Stop 3 |
| 3. Starting Unit Address | A Register | Stop 4 |
| 4. Ending Unit Address   | Q Register | Stop 4 |
| 5. Starting Unit Address | A Register | Stop 5 |
| 6. Equipment Code        | Q Register | Stop 5 |

If the section is to run synchronous, the operator must define the following:

- |                   |                 |        |
|-------------------|-----------------|--------|
| 1. Manual Sync or | A13             | Stop 3 |
| Repetitive Sync   | A12             | Stop 3 |
| 2. Sync Wait Time | A or Q Register | Stop 8 |

If the section is to run synchronous with interrupts, the operator must define the following:

- |                         |                 |        |
|-------------------------|-----------------|--------|
| 1. Manual Sync or       | A13             | Stop 3 |
| Repetitive Sync         | A12             | Stop 3 |
| 2. Write Interrupt Line | A Register      | Stop 7 |
| 3. Interrupt Wait Time  | A or Q Register | Stop 8 |

If asynchronous or repetitive sync mode is selected, the section will transfer a total of 3100 words per data pattern selected. If manual sync is defined, one word per unit address will be transferred.

This section calculates the number of channels of digital input for testing by comparing the starting and ending addresses of Stop 4. Actual transfers begin with the read starting unit address as defined in the A register of Stop 5.

When operating in manual sync mode, the operator must short card pin B28 (request) to card test point 20 (reply). The Reply signal is used as a pulse to trigger the sync circuits. If request is grounded, or remains connected to test point 20 for any length of time, the test will apparently execute two passes per sync. In reality the Request signal is not being removed fast enough by the operator and one pass is completed on setting the Request signal, and one pass is completed on clearing the Request signal.

J. SECTION 11: WRITE-READ CLOSED LOOP

The purpose of Section 11 is to output data through the digital output unit, input this data through the digital input unit, and check the validity of the input against the original output data.

To execute this section, the operator must select or define the following:

1. Equipment Code-Writes	Q Register	Stop 2
2. Section 11	A09	Stop 3
3. Data Patterns	Q Register	Stop 3
4. Starting Write Unit Address	A Register	Stop 4
5. Ending Write Unit Address	Q Register	Stop 4
6. Starting Read Unit Address	A Register	Stop 5
7. Equipment Code - Reads	Q Register	Stop 5
8. First Data Word	A Register	Stop 6
9. Alternate Data Word	Q Register	Stop 6

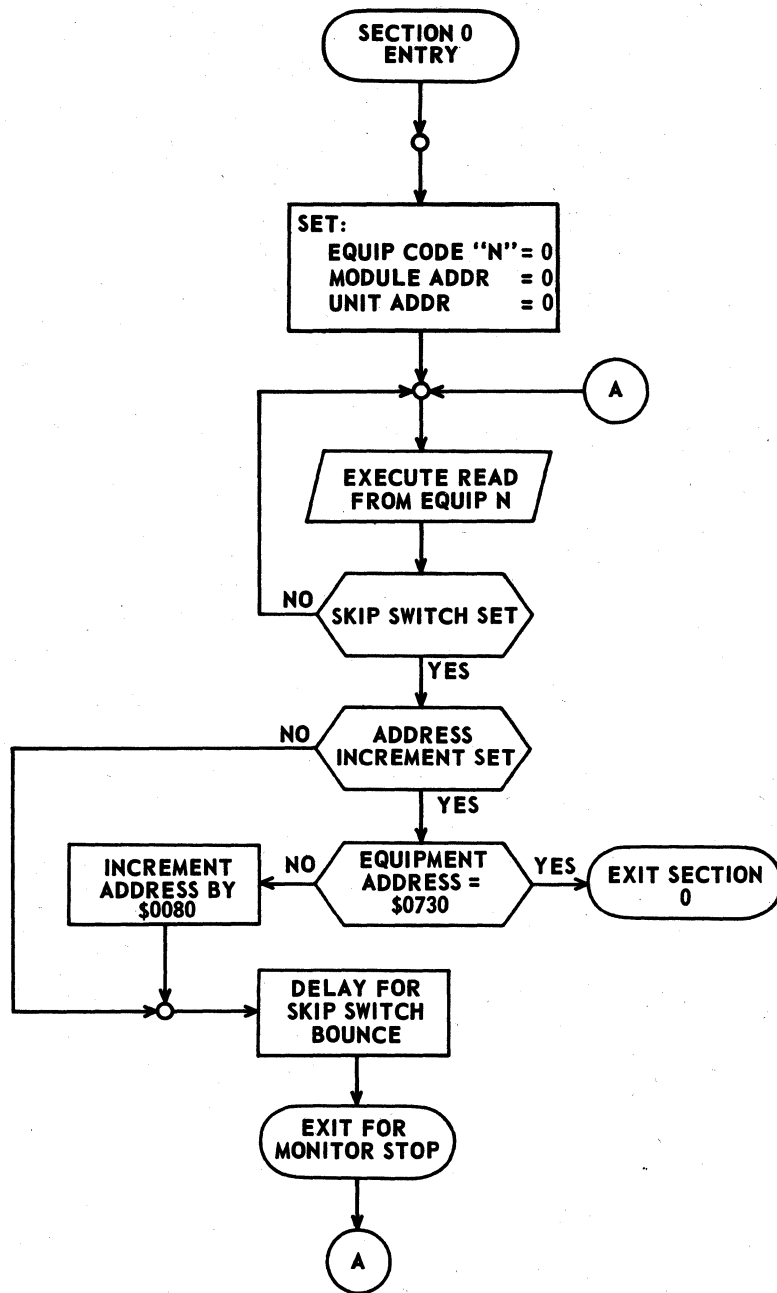
If the section is to run synchronous, the operator must define the following:

1. Manual Sync or	A13	Stop 3
Repetitive Sync	A12	Stop 3
2. Sync Wait Time	A or Q Register	Stop 8

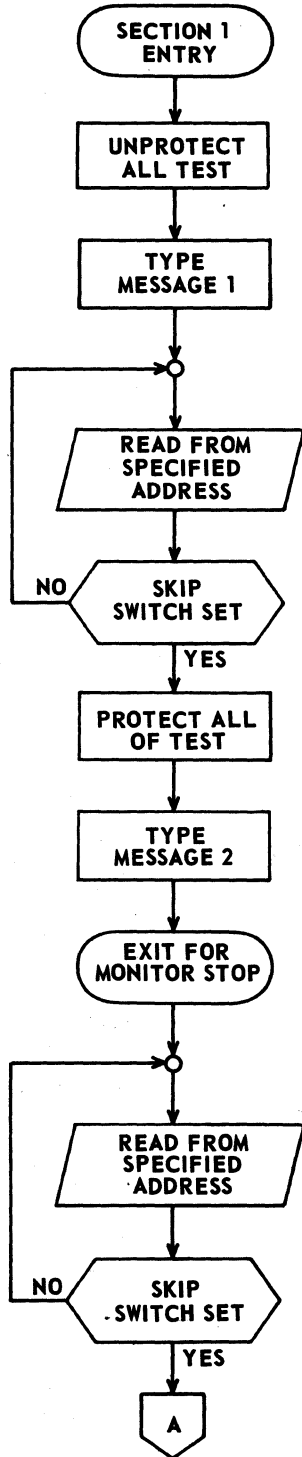
If the section is to run synchronous with interrupts, the operator must define the following:

1. Manual Sync or	A13	Stop 3
Repetitive Sync	A12	Stop 3
2. Write Interrupt Line	A Register	Stop 7
3. Interrupt Wait Time	A or Q Register	Stop 8

If asynchronous or repetitive sync mode is selected, the section will transfer a total of 3100 words per data pattern selected. If manual sync is defined, one word per unit address will be transferred. If this section is to run synchronously, the write channels must be enabled prior to the execution of the I/O. A good time to do this is during the parameter entry sequence. Here the mainframe will wait indefinitely while the hardware is readied. If the I/O is begun to an un-abled synchronous write channel, the hardware can never be made ready, and thus the write I/O will always be rejected.



SECTION ZERO - EQUIPMENT CODE CHECK



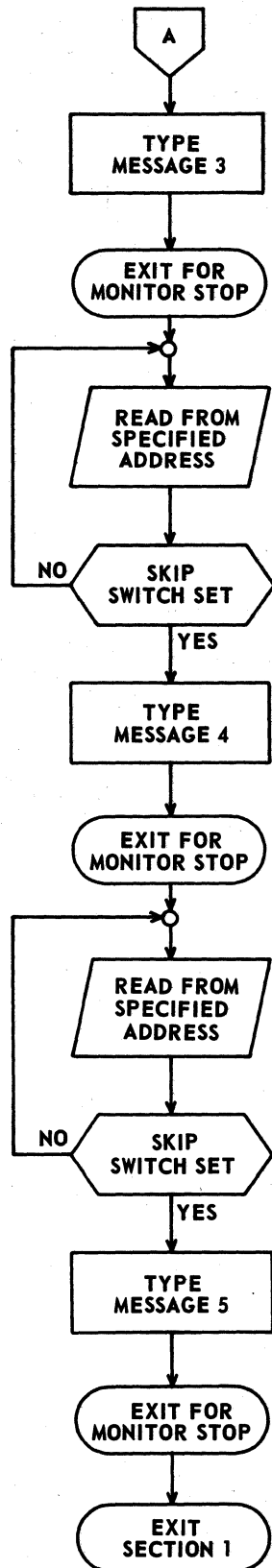
MESSAGE 1:

SET PROTECT SWITCH. CLEAR STOP SWITCH.  
UNPROTECTED I/O TO UNPROTECTED IOM.  
SET SKIP SWITCH TO ADVANCE TEST

MESSAGE 2:

PROTECTED I/O TO UNPROTECTED IOM.  
SET SKIP SWITCH TO ADVANCE TEST.

SECTION ONE - PROTECTED I/O CHECK



**MESSAGES**

**MESSAGE 3:**

**PROTECT IOM.  
PROTECTED I/O TO PROTECTED IOM.  
SET SKIP SWITCH TO ADVANCE TEST**

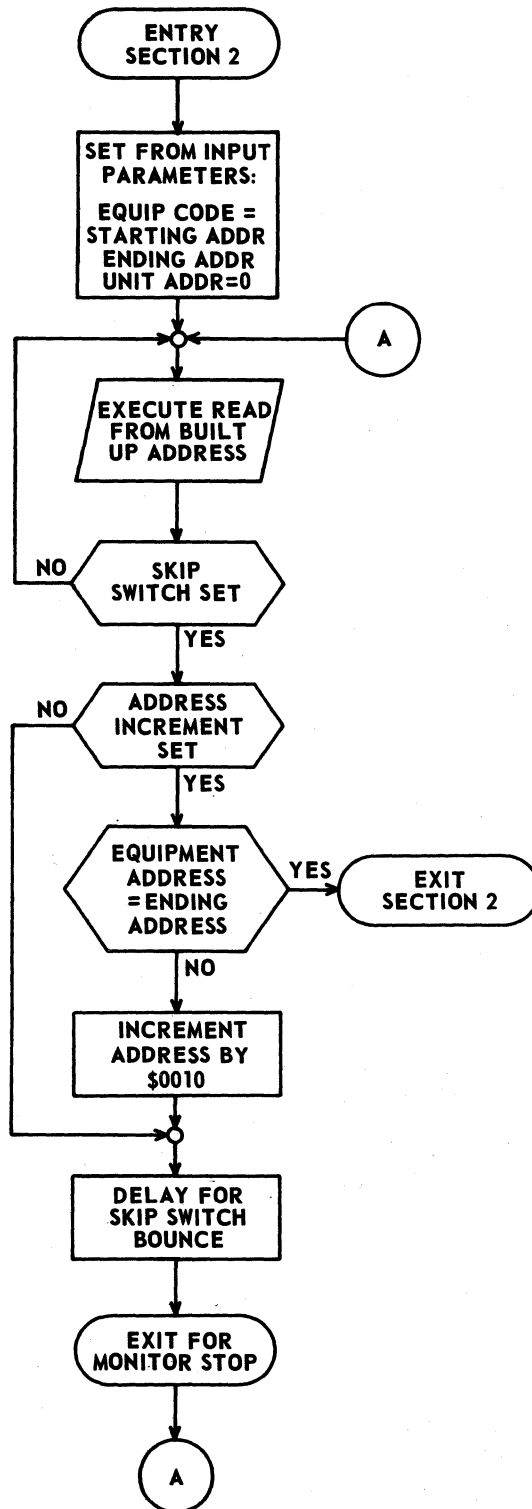
**MESSAGE 4:**

**UNPROTECTED I/O TO PROTECTED IOM.  
SET SKIP SWITCH TO ADVANCE TEST.**

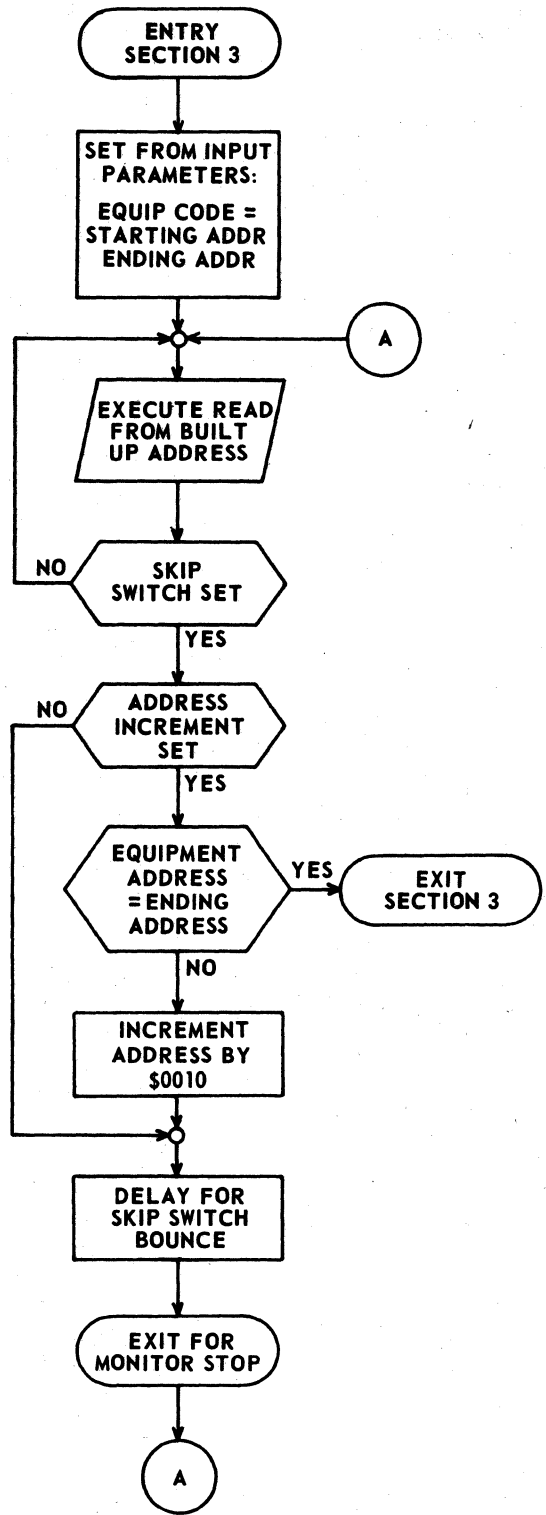
**MESSAGE 5:**

**CLEAR PROTECT SWITCH.  
SET STOP SWITCH.  
SET SKIP SWITCH TO ADVANCE TEST.**



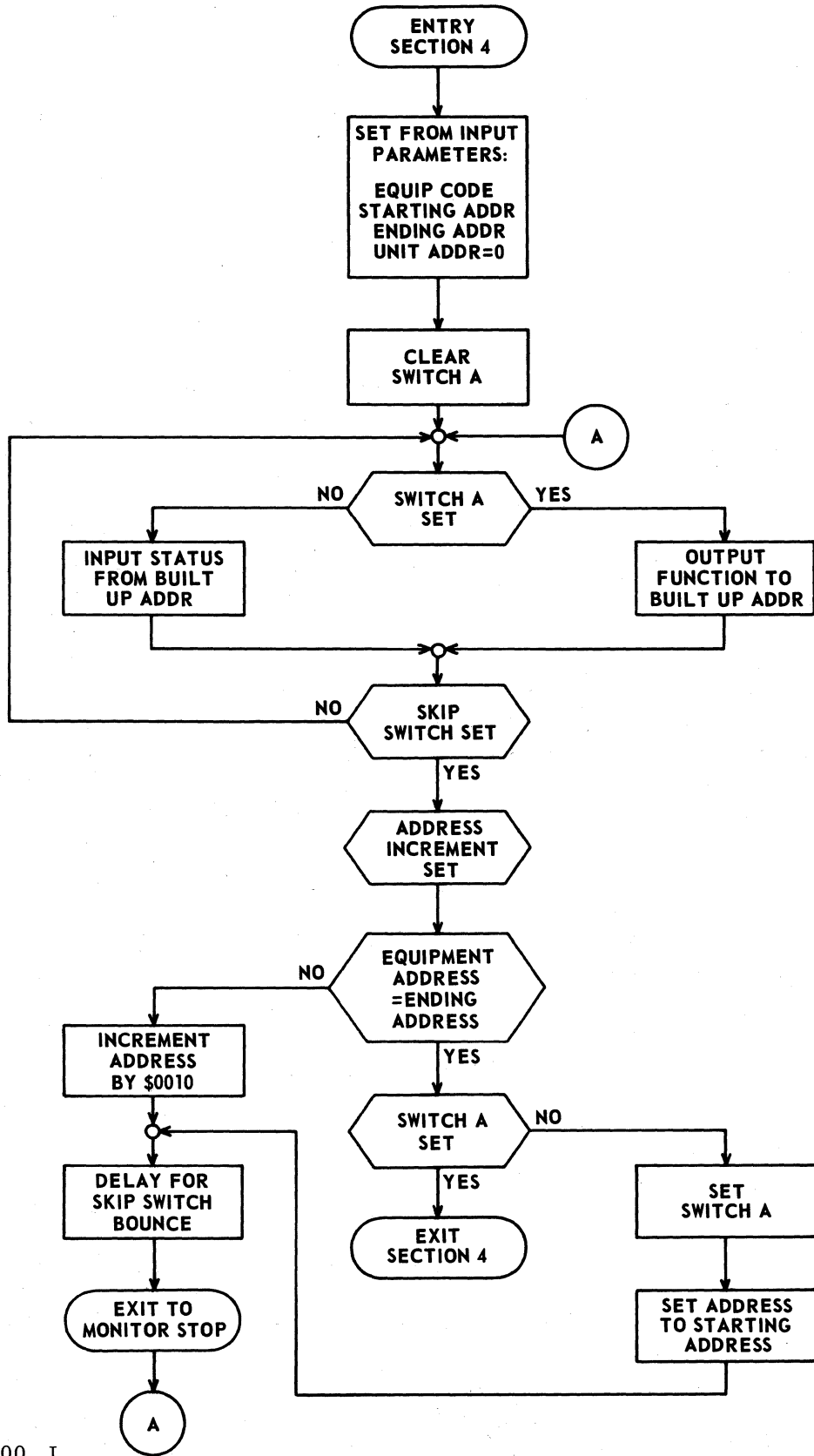


SECTION TWO - MODULE SELECT CHECK

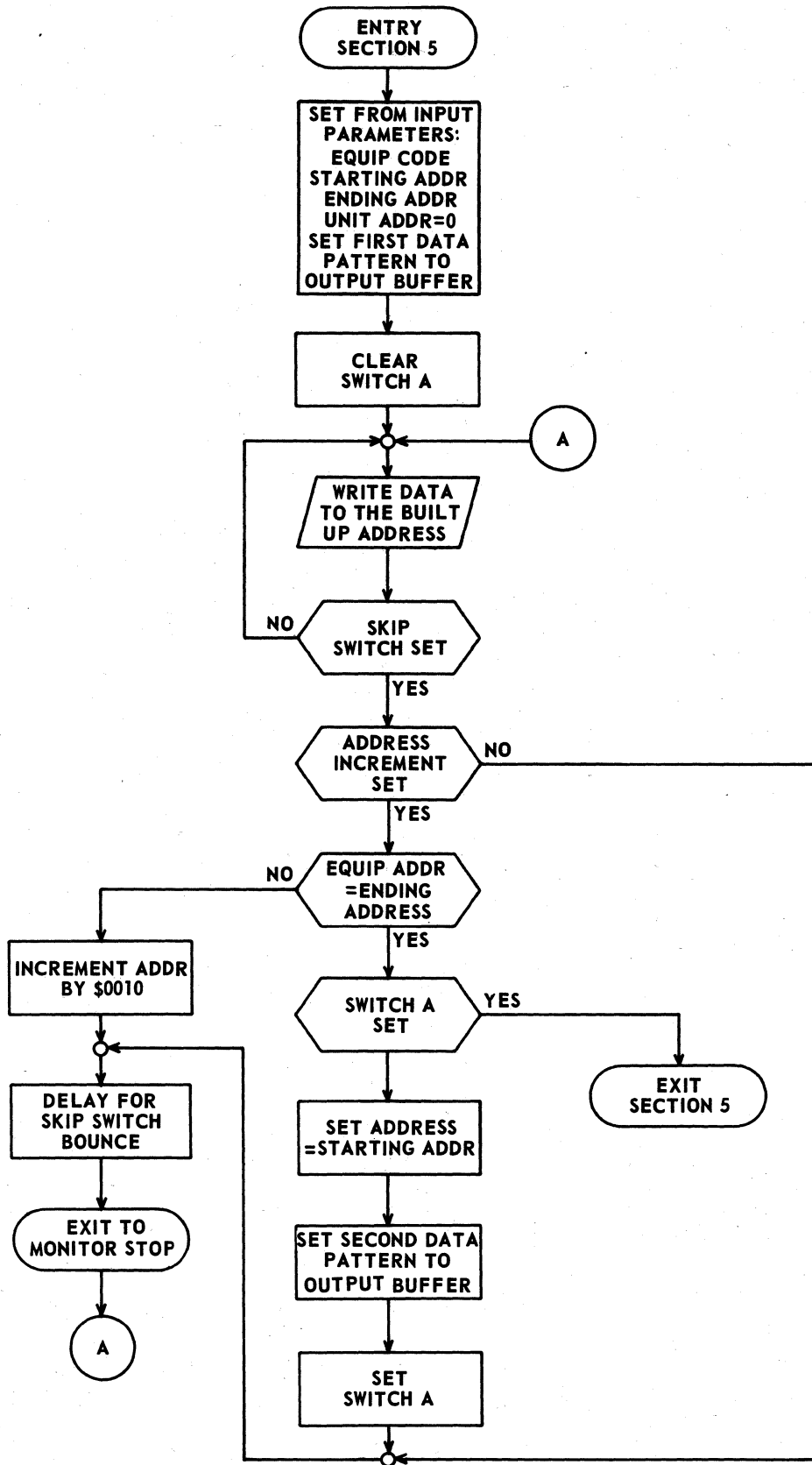


SECTION THREE - UNIT SELECT CHECK

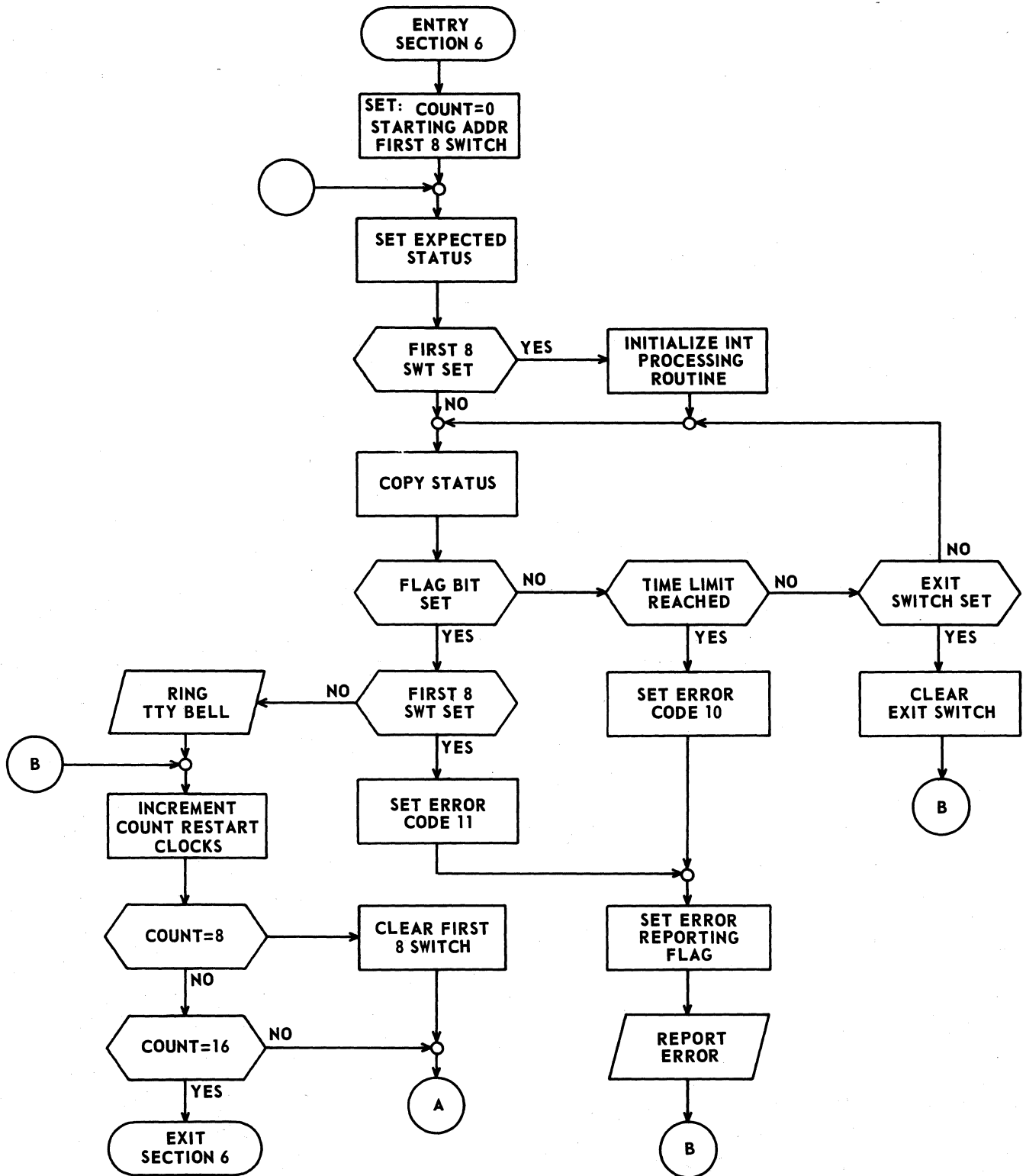
SECTION FOUR - STATUS REPLY - FUNCTION REJECT



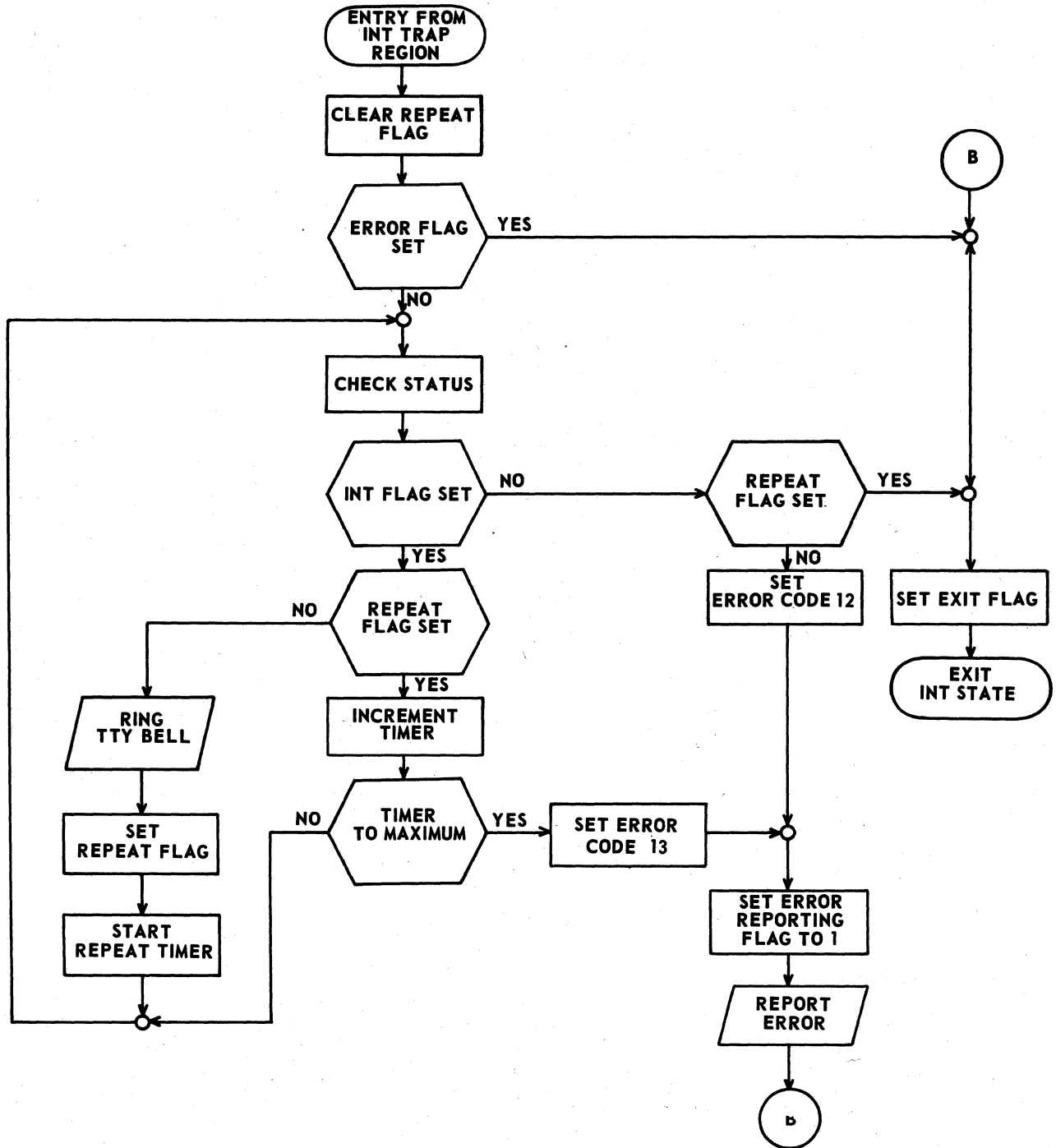
SECTION FIVE - DATA OUTPUT CHECK



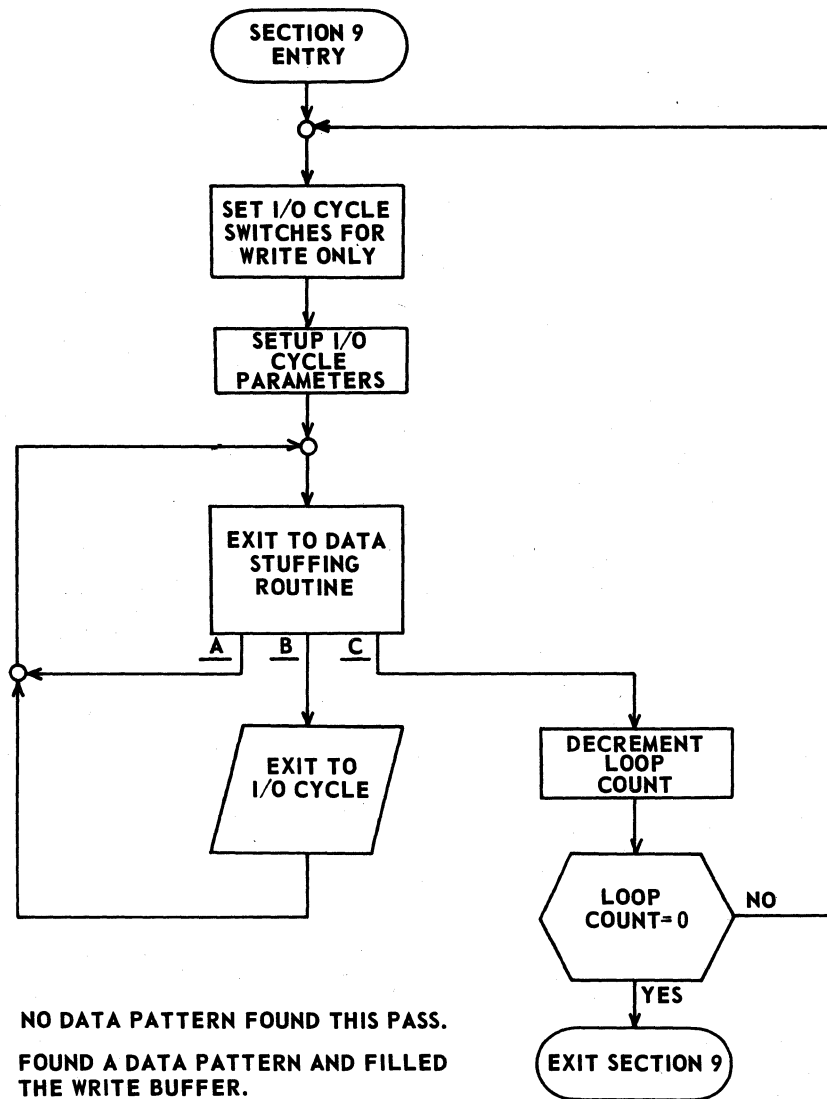
SECTION SIX - INTERRUPT/FLAG STATUS CHECK



SECTION SIX - INTERRUPT PROCESSOR

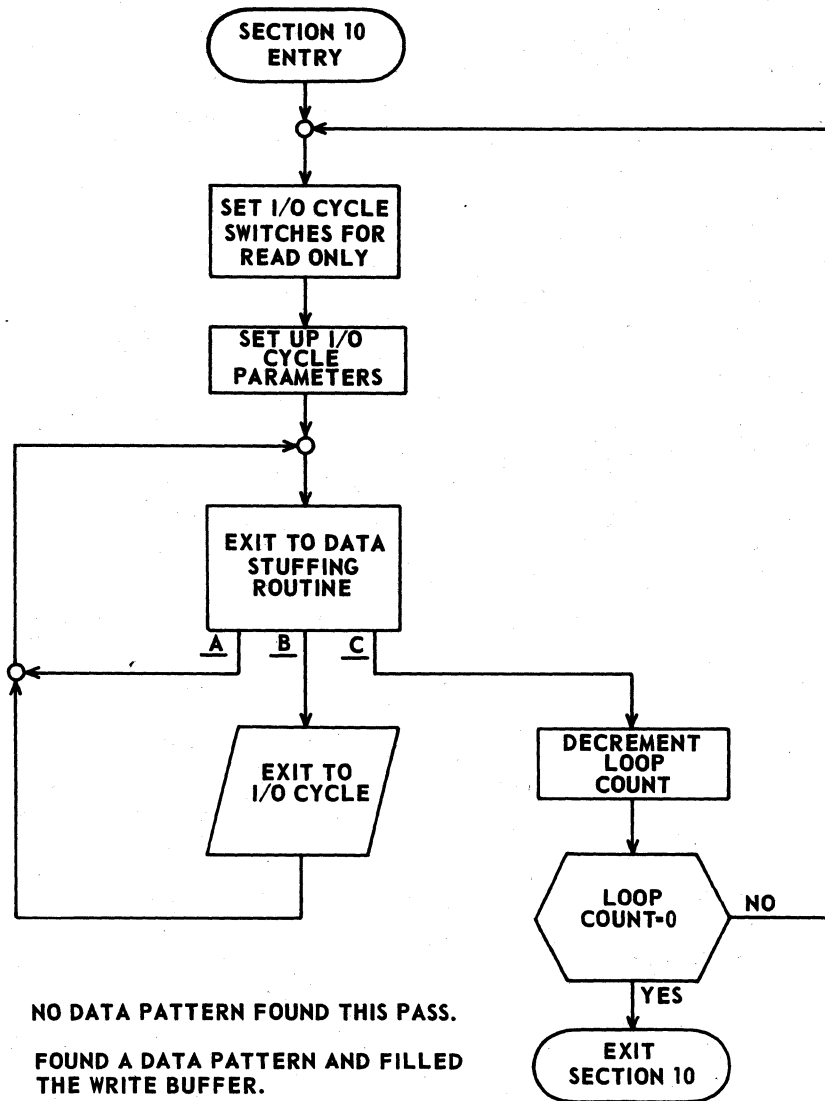


SECTION 9 - WRITE ONLY CHECK



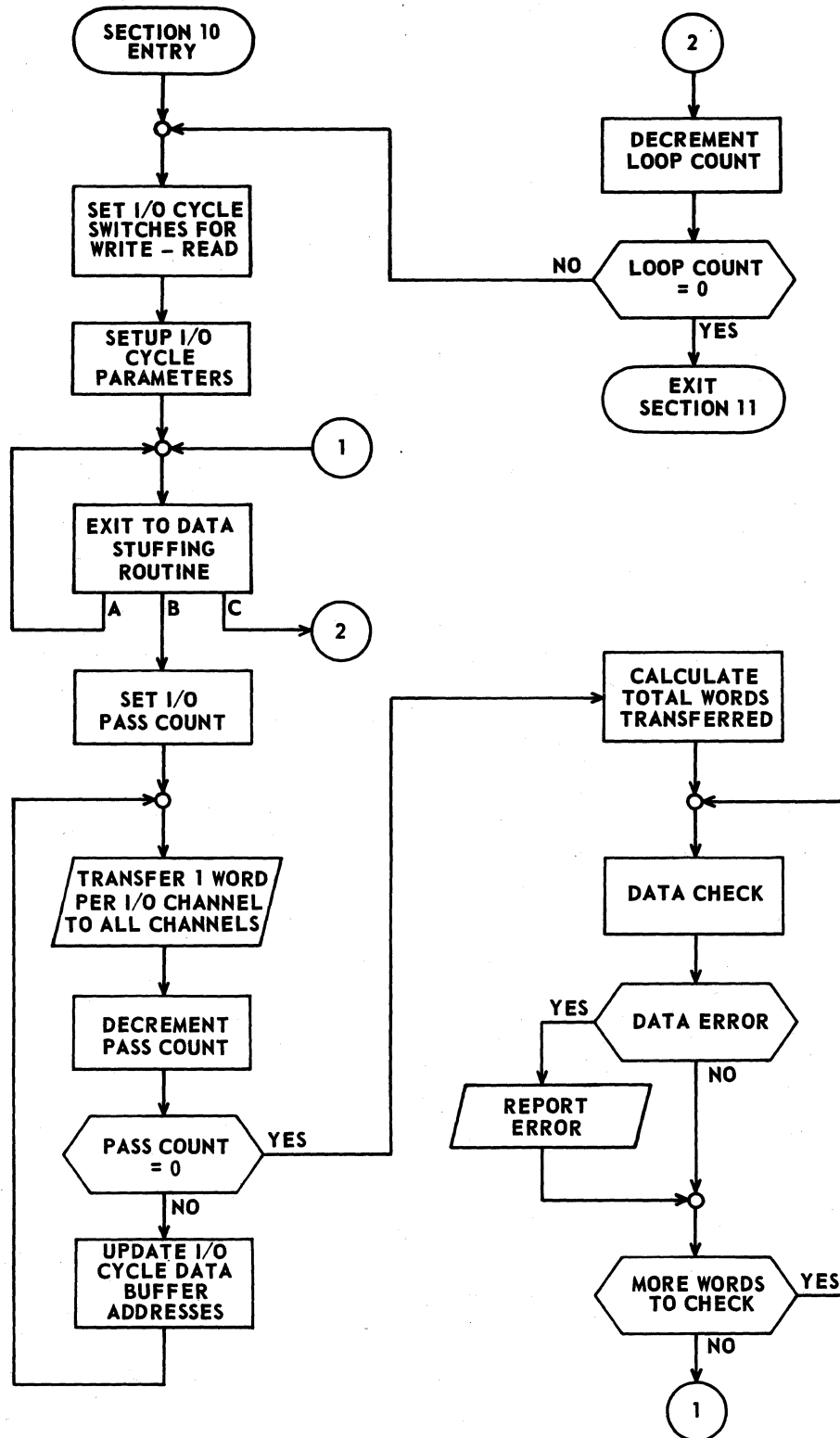
- A NO DATA PATTERN FOUND THIS PASS.
- B FOUND A DATA PATTERN AND FILLED THE WRITE BUFFER.
- C NO ADDITIONAL DATA PATTERNS.

SECTION TEN - READS ONLY

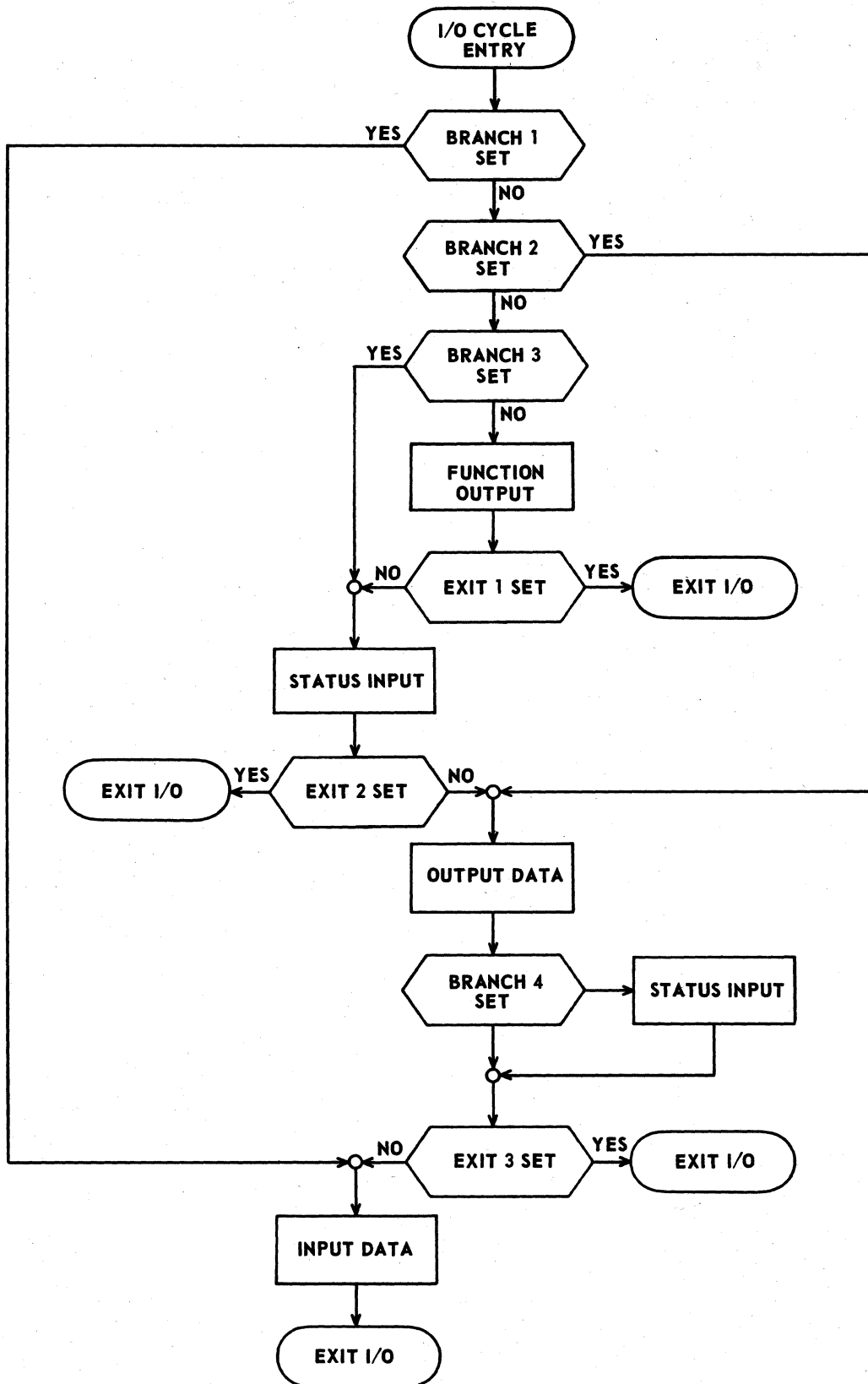


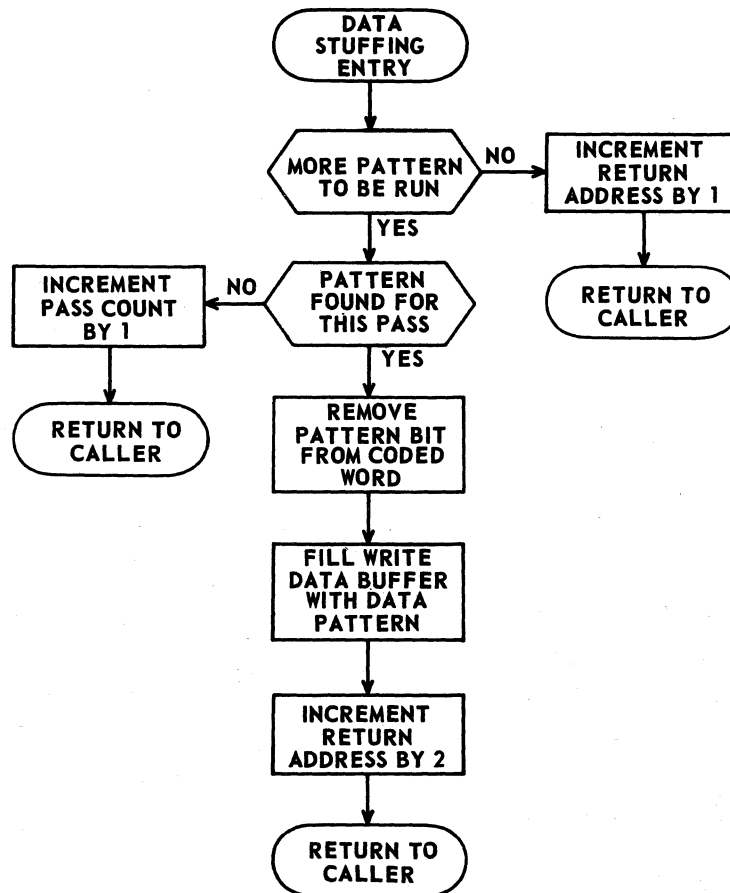
- A NO DATA PATTERN FOUND THIS PASS.
- B FOUND A DATA PATTERN AND FILLED THE WRITE BUFFER.
- C NO FURTHER DATA PATTERNS.





SECTION ELEVEN - WRITE READ CLOSED LOOP





DATA STUFFING ROUTINE



10336-1 REAL-TIME CLOCK  
(RTC091 Test No. 91)

I. OPERATIONAL PROCEDURE

A. RESTRICTIONS

Timing is critical; therefore, control is not returned to the monitor when checking the free running clock. Thus, while Section 1 is running, no other test is able to run.

B. LOADING PROCEDURE

1. This test operates under control of the 1700 System Maintenance Monitor (SMM17)
2. The calling sequence is that specified by SMM17.
3. Restart test after loading by Master Clear, set P = IA, and RUN.

C. PARAMETERS (Order in which they are entered)

A2 = SECTNS Section Select parameter, prestored as 000F<sub>16</sub>

Q2 = PRINLN Interrupt Line parameter, prestored as 2000<sub>16</sub>

A3 = BASCYL Clock Basic cycle, prestored as 5.

0 - 1 sec

1 - 100 ms

2 - 10 ms

3 - 1 ms

4 - 100 usec

5 - 10 usec

6 - 1 usec

Q3 = TIMLIM Time limit in minutes for testing the free running clock in Section 1, prestored as 5

A4 = SINTER Selected interval to be tested in Section 2, prestored as 000F<sub>16</sub>

Q4 = NUMTIM Number of times selected interval is to be tested, prestored as 0100<sub>16</sub>

D. MESSAGES

1. Test title.

RTC091 SYSTEM 17 REAL TIME CLOCK TEST.  
CPC, VER. 3.1-1

2. Initial Address Message

IA = XXXX, FC = XX  
(XXXX = starting address of test and XX = frequency count.)

3. Error Messages

a. FATAL ERROR, ENDING SECTION XX

Output when an error occurs which causes the entire section to malfunction (XX = section number).

b. All error messages are in the format specified by SMM17.

c. Individual Error Codes

<u>Error Code</u>	<u>Description</u>
1	Unexpected interrupt
2	Internal reject during interrupt processing
3	External reject during interrupt processing
4	Invalid count
5	Timeout
6	Interrupt early
7	Interrupt not enable while clock is running
8	External reject during input
9	Internal reject during input
A	External reject during function output
B	Internal reject during function output
C	External reject during read
D	Internal reject during read
E	Count not used by clear controller
F	Interrupt not disabled by clear controller
10	Reply received when reading with Q0=0
11	Internal reject when reading with Q0=0
12	Internal reject with A6 and A7 set on function output
13	Reply received with both A6 and A7 set on function output
14	With clock stopped, count changed
15	Clock stopped after an interrupt
16	Internal reject with A14 and A15 set on function output
17	Reply received with A14 and A15 set on function output
18	External reject when W ≠ 0
19	Reply received when W ≠ 0

## E. ERROR STOPS

1. First Stop  
A1 = ID word  
Q1 = Stop/Jump parameter
2. Second Stop  
A2 = Section number/error code  
Q2 = Return address
3. Third Stop  
A3 = Local I/O routine call address  
Q3 = Number of times error occurred (Section 0 only) or old clock counter value (Sections 1, 2, and 3)
4. Fourth Stop  
A4 = A register (function output)  
Q4 = Q register (equipment code)
5. Fifth Stop  
A5 = Interval being tested  
Q5 = Clock counter

## II. TEST DESCRIPTION

### A. INITIALIZATION

1. Type out test title.
2. Return control to the monitor.
3. Enter parameters if selected.
4. Request interrupt line.
5. Return control to the monitor.

### B. SECTION 0 - TIMER STATIC TEST

1. Clear the controller.
2. Check for counter zeroed.
3. Check for interrupt disabled.
4. Read with Q = 0, repeat \$100 times.
5. Check for errors (reply received or internal reject).
6. Return control to the monitor.
7. Output with A6 and A7 set. Repeat \$100 times.

8. Check for errors (reply received or internal reject).
9. Return control to the monitor.
10. Output with A14 and A15 set. Repeat \$100 times.
11. Check for errors (reply received or internal reject).
12. Return control to the monitor.
13. Output with W field = 0. Repeat \$100 times.
14. Check for errors (reply received or external reject).
15. Return control to the monitor.
16. Stop the clock; check if count changes after a long delay.
17. Check for unexpected interrupts.
18. Return control to the monitor.
19. Set up for an interrupt.
20. Check to see if the clock is still running after interrupt occurs.
21. Clear controller.
22. Start the clock.
23. Check to see that interrupts can be enabled while clock is running.
24. End of section.

C. SECTION 1 - FREE RUNNING CLOCK TEST

1. Set up Clock register and number of times to loop through section based on the clock's basic cycle and the time unit.
2. Delay.
3. Get counter value and see if it is valid.
4. Check if done; if not, jump to 2.
5. Otherwise, end of section.

D. SECTION 2 - SELECTED INTERVAL TEST

1. Load Clock register with selected interval.
2. Wait for interrupt to occur.
3. Check if counter value is valid.
4. Check for timeout.
5. No interrupt, go to 2.



6. Otherwise, check if interrupt is early.
7. Check for error during interrupt processing.
8. If done, end of section.
9. Return control to the monitor with IA+5 set to step 1.

E. SECTION 3 - TEST EACH BIT IN CLOCK REGISTER

1. Select interval.
2. If done, end of section.
3. Otherwise, load the Clock register with selected interval.
4. Wait for interrupt to occur.
5. Check if counter value is valid.
6. Check for timeout.
7. No interrupt, go to 4.
8. Otherwise, check if interrupt is early.
9. Check for error during interrupt processing.
10. Return control to the monitor with IA+5 set to step 1.

III. PHYSICAL REQUIREMENTS

A. STORAGE REQUIREMENTS

Approximately 1200 locations

B. TIMING

Variable, depending on the clock's basic cycle.

C. EQUIPMENT CONFIGURATION

1. 1784 Computer with 4K memory
2. 10336-1 Real-Time Clock
3. Device for loading test



## 1700 HARDWARE FLOATING POINT UNIT DIAGNOSTIC

(HFP08A Test No. 8A)

(CP = 2C)

### I. OPERATIONAL PROCEDURE

The original coding for this diagnostic was developed to execute under control of the Small Computer Maintenance Monitor (SCMM) diagnostic system. This SMM17 test is a result of interfacing the original SCMM test to the SMM17 library; thus, many operating characteristics of this test reflect SCMM operations.

#### A. RESTRICTIONS

1. Seven thousand words of memory are required for execution.
2. A teletype or line printer is required for reporting error messages.
3. Bits 2 and 3 of the SMM parameter must specify the correct machine type.
4. Low core locations \$E6 through \$F0 are used.
5. Stop/Jump bit 11 has been defined as terminate execution immediately.
6. This test does not respond to repeat section, stop at end of section, or repeat conditions. Repeat conditions is implemented by use of bits 15 and 14 of the flag word within the test.
7. If multiplexing this test with a second test utilizing DSA transfers, it may be required to operate the HFPU test in word mode to avoid possible lost data errors in the second test. This is due to the HFPU holding the DSA scanner for multiple DSA cycles in Block or Hog mode.

#### B. LOADING PROCEDURE

1. This test operates as a subprogram under control of the 1700 System Maintenance Monitor (SMM17).
2. The calling sequence is that specified by SMM17. Address is Director Function 1.
3. The test can be restarted by master clearing and executing from the test's initial address.

#### C. PARAMETERS

The following parameter message identifies the information in each of the stops:

ID, STSP, FLAGS, RUNS, CSQ LENGTH, MODE

The following standard SMM17 parameter stops are used:

A1 = ID word

A2 = Flag word

Q1 = Test Stop/Jump word

Q2 = Runs

### 1. FLAGS

- Bit 0 Perform test in single precision mode only.\*
- Bit 1 Perform test in double precision mode only.\*
- Bit 2 If bit 2 is set, wait for 1781-1 completion by reading FSR status and checking for active status bit to clear. If bit 2 is not set, 1791-1 completion is signaled by a reply to an input of address status with Q=XXX3 (single precision) or Q=XXX4 (double precision).
- Bit 3 Loop on Register Test.
- Bit 4-5 Not used.
- Bit 6 Minimum error printout. Only the register status and data buffer words in error will be printed.
- Bit 7 Test illegal operation codes (SPEC followed by \$A through \$F). These codes should be treated as FEND instructions.
- Bit 8 Issue a PROGRAM MASTER CLEAR before the start of each calling sequence.
- Bit 9 Request operator action after detecting an error.
- Bit 10 Suppress printout of data buffers on error.
- Bit 11 Suppress printout of calling sequence on error.
- Bit 12 Suppress printout of register status on error.
- Bit 13 Suppress all error printouts except header line.
- Bit 14 If bit 14 is set, the diagnostic will generate one calling sequence and execute it repeatedly until stopped.
- Bit 15 Restart at failing calling sequence.

### 2. RUNS

Any decimal number up to 8000 is used. If 8000 is entered, the test will execute indefinitely until the operator intervenes.

A3: Calling sequence length

Q3: Mode

### 3. CSQ LENGTH

Any decimal number up to 200 is used. If zero is specified, the CSQ length is determined randomly.

\*If neither bit 0 nor bit 1 is set, the test will randomly select single or double precision for each calling sequence.

#### 4. MODE

\$0000-Operate 1781-1 in Block mode

\$0001-Operate 1781-1 in Hog mode

\$0002-Operate 1781-1 in Word mode

Use caution when selecting mode. When operating in Block or Hog mode, the hardware holds the DSA scanner for multiple cycles. This may cause lost data errors when multiplexing this test with high throughput rate DSA devices. If multiplexing with such tests, select Word mode to guarantee error-free execution. Possible tests which will cause the DSA error are as follows:

##### a. MDC07A Cartridge Disk Test

This test initiates large DSA transfers and then allows another test to run. If the HFPU test is running with this disk test, possible disk lost data status errors will occur if the HFPU starts a DSA transfer concurrent with the disk DSA transfer. During data transfers, the HFPU may hold the DSA scanner for up to six cycles and lock out the disk, resulting in lost data. When testing these two devices under the SCMM diagnostic system, these lost data status errors occur, but the operating system drivers used by the SCMM tests attempt 10 recoveries before flagging an error; 10 lost data conditions will rarely occur in sequence.

##### b. PET04B Magnetic Tape Test

When running any test section doing data transfers in 1600 BPI phase encode, tape lost data may occur for the same preceding reasons.

#### D. MESSAGES

##### 1. Test Initial Message

1781-1 HARDWARE FLOATING POINT UNIT TEST

1A = XXXX, FC = YY, CP = 2C VER 3.2

##### 2. Parameter Stop Message

ID, STSP, FLAGS, RUNS, CSQ LENGTH, MODE

##### 3. Error Messages

When an error in results is detected, the diagnostic outputs a message. The message consists of the following four parts; three parts may be suppressed by setting the appropriate bit in Flags (A2) of the test's operational or restart parameters.

- a. HFP08A ERROR, RUN XXXX, RESTART VALUES  
XXXX XXXX XXXX XXXX

This printout can only be disabled by setting Omit typeouts in the Stop/Jump word.

- b. Calling Sequence

2A54	BA54	(FLDD FDIV FEND FEND)
2A55	2A1C	(6CD6 4EF1 E98E)
2A56	2A1F	(3C72 47E4 0B75)

Leftmost column	Core location
Center column	Contents of the core location (command word or operand address)
Entries enclosed in parentheses	Command mnemonics or operand (If the location is used by a FLST, STRI, or FLOF instruction or is used as an address for a branch instruction, this column will be blank.)

The operand value printed will be one, two, or three words, depending upon the type of operand (integer, single precision, or double precision). If the address points to a location used by FLST, STRI, or FLOF, no operand value will be printed.

This printout may be suppressed by setting bit 11 in Flags of the test's operational or restart parameters.

- c. End Register Status

	S	H
FSR	0CC	0CD0
CCR	4BA5	4BA5
IR	0000	0000
PCR	2AF7	2AF7
FPAC1	F7BE	F7BE
FPAC2	F9AF	F9AF
FPAC3	1DA4	1DA5

Leftmost column	Register designation
Center column	Software simulated value (expected value)
Rightmost column	Hardware result (actual value)

Any register disagreement is flagged by an <. If minimum error printout is selected, only the register which disagrees is printed.

The end register status printout may be disabled by setting 12 in Flags of the test's operational or restart parameters.

#### NOTE

The hardware and software FSR printouts may differ without an error occurring since the state of bits 15, 8, and 5 through 0 are not significant to the test.

#### d. Data Buffers

ADDR	S	H
287A	72C6	72C6
287B	78EB	78EB
287C	3756	3756
287D	AE08	AE08
287E	DC80	DC80
287F	C43D	C43D
2880	63C0	63C0
2881	BB8A	BB8A
2882	CB99	CB99
2883	9390	9390
2884	FF15	14F5 <
2885	4D6B	E838 <
2886	3EEC	3EEC
2887	E800	E800

Leftmost column: Core address  
Center column: Software simulated result (expected value)  
Rightmost column: Hardware result (actual value)

The data buffer location(s) in disagreement is flagged by an <. If minimum error printout is selected, only the location(s) which disagrees is printed.

This printout may be disabled by setting bit 10 in Flags of the test's operational or restart parameters.

When an error in hardware response is detected, the diagnostic outputs one of four possible messages.

- 1781-1 EXTERNAL REJECT  
A reject signal was returned to the CPU from the HFPU when a reply was expected.
- 1781-1 INTERNAL REJECT  
No reply was returned to the CPU.
- STOP/RESTART EXTERNAL REJECT  
A reject signal was returned to the CPU from the HFPU when attempting to stop and restart the HFPU.
- STOP/RESTART INTERNAL REJECT  
No reply was returned to the CPU when attempting to stop and restart the HFPU.

Entering an incorrect parameter for the calling sequence length will result in the message:

ERROR, NUMBER OF BYTES MAY NOT EXCEED 240.

New parameters will be requested from the operator.

#### 4. Restart Message

Setting bit 15 of the flag word will allow the operator to enter restart values to the test. Restart values are presented to the operator at the beginning of each error message.

When bit 15 of the flag word is set, the following message will be presented:

ENTER RESTART VALUES: ID/STAP, FLAGS/R1, R2/Rd, R4/0.

The operator should enter the desired restart parameters exactly as presented in an error message:

FLAGS	Enter a flag word value as defined in parameter Stop A2. Bits 0, 1, and 7 cannot be redefined.
R1	Critical bits of the flag word controlling this calling sequence.
R2	Calling sequence length, as defined in parameter Stop A3.
R3, R4	Initial values for the random number generator.



5. Operator after Error Message

If flag word bit 9 is set, the following message is presented:

HFP08A ERROR. Action -

The operator should enter one of the five possible responses followed by a carriage return:

- \$0000 : Stop the test and exit
- \$0001 : Ignore the error and continue the test
- \$0002 : Re-try the same calling sequence on the hardware
- \$0003 : Request a new set of parameters from the operator
- \$0004 : Loop on hardware execution of the failing calling sequence until redirected
- \$0005 : Request entry of restart parameters

6. End Message

END 1781-1 TEST, XXXX RUNS, YYYY ERRORS

8A24 STAP ZZZZ ADDR

- XXXX = Number of runs
- YYYY = Error count this run
- ZZZZ = Pass count

## II. DESCRIPTION

### A. GENERAL

This diagnostic is unique within the SMM17 Diagnostic Library for the following reasons:

1. The original design and implementation was done under control of the SCMM17 Diagnostic Library. This SMM17 test is the result of adding a software interface package to link the original SCMM17 monitor requirements to the SMM17 monitor requirements.
2. Many of the standard SMM17 operating options normally available to the operator are not available through the use of the Stop/Jump word. However, equivalent functions are available through the use of a flag word contained within the test (parameter A2).

3. There is only one test section that exercises the full capability of the device. Through judicious choice of test parameters, a hierarchy of testing can be achieved to aid in troubleshooting the device.
4. Parameters may be input to the test at initialization, restart, and error stop. Initialization parameters control the normal test execution and can be pre-stored as per standard SMM17 tests. Restart parameters are input to re-create a failing condition; they are not pre-storable and when used, must be input exactly as presented in an error message. If flag bit 9 is set, the operator has the opportunity to input parameters after the error message so as to manipulate the continued execution of the test; these parameters cannot be pre-stored.

#### B. NORMAL TEST EXECUTION

Load this test as a standard SMM17 test. Suggested parameters to utilize the full capabilities of the diagnostic and provide the most rigorous test of the 1781-1 are:

A1 = \$8A41	Test ID
Q1 = \$020D	Stop/Jump word
A2 = \$0000	Flag word
Q2 = \$0001	Runs
A3 = \$0000	Calling sequence byte length
Q3 = \$0000	Mode

With these parameters, the test will run one pass (Q2) in Block mode (Q3) with a random calling sequence length between 1 and 200 bytes (A3=0), randomly switching between single and double precision (A2 bit 0, 1 = 0) using an I/O reply to indicate completion (A2 bit 2 = 0) and allowing full error messages (A2 bits 10, 11, 12 and 13 = 0). The internal random number generator controlling the test is re-initialized each time the test is executed from its initial address, but is not re-initialized for successive passes of the test. Thus, no two successive passes will use the same data, operands, or buffer addresses unless the test is stopped and then restarted from its initial address. One pass consists of executing 10,000 calling sequences.

To significantly reduce the execution time of the test, limit the length of the calling sequence. First pass execution times are as follows:

Calling Sequence Length	Execution Times (600 nanoseconds CPU)
25	3 minutes
50	6 minutes
75	8 minutes
100	12 minutes

### C. MAINTENANCE AID EXECUTION

This description is intended to provide starting hints if failures occur during execution of the test. Refer to the following flow diagram indicating the execution paths which may be selected by various flag word bits.

1. Does the hardware get past the register check?

If not, attempt to determine which bits of which register are failing and coordinate this with the prints as to a failing board. Set bit 3 of the flag word to force the register check into a loop if it is necessary to scope the device.

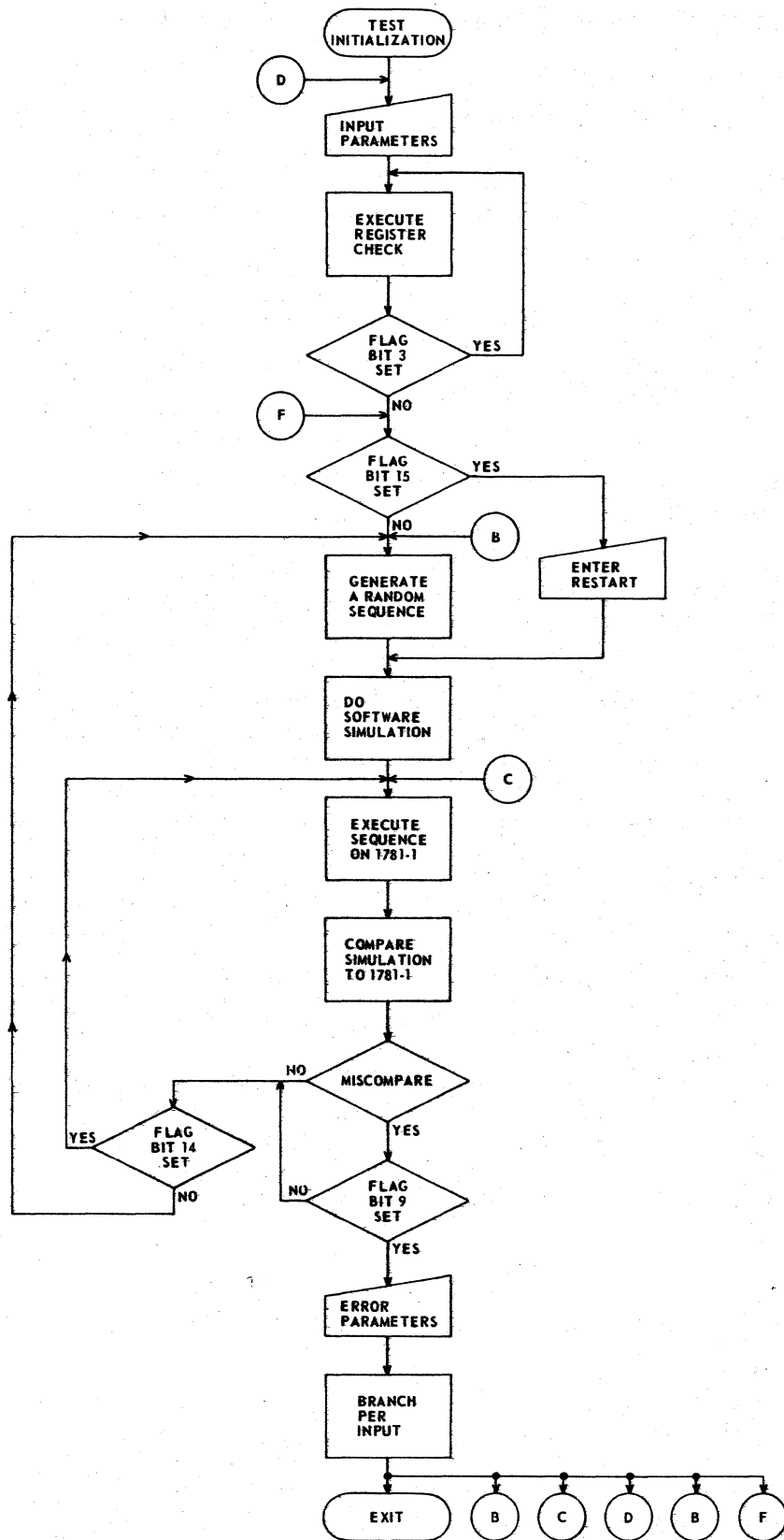
2. Is DSA suspected of malfunctions?

Select word mode in parameter 63. In this mode, one DSA access is made for each data word required for operations. Select Block mode to allow the HFPU to hold the scanner for up to five accesses at a time. Select Hog mode to allow the HFPU to hold the scanner from the time it is started until a FEND instruction is encountered.

3. Are the failures associated with single-or double-precision arithmetic?

Set bit 0 of the flag word to force continuous single-precision arithmetic, and/or set bit 1 of the flag word to force continuous double-precision arithmetic to see if the errors change.

4. Control the test to guarantee looping on or repeating the same conditions to force the same errors. Execute the test until an error occurs. Observe the restart values presented in the error message. Restart the test at its initial address, setting flag word bits 15 (restart requested) and 14 (loop on single sequence). Enter the restart values.



**COMMENT SHEET**

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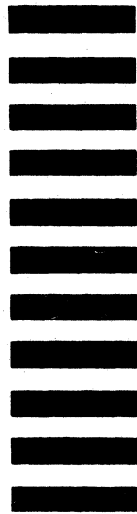
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