CONTROL DATA
CORPORATION

CONTROL DATA®
1706-A BUFFERED DATA CHANNEL AND STANDARD OPTION 10277-1

REFERENCE MANUAL

REVISION RECORD

REVISION	DESCRIPTION
A	Manual released; this manual supersedes the 1706-A Buffered Data Channel section of the
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Address comments concerning this manual to:

Control Data Corporation
Technical Publications Department
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PREFACE

This manual gives reference information for the CONTROL DATA® 1706-A Buffered Data Channel which may be used in conjunction with the 1705 Interrupt Data Channel of the 1700 Computer. For reference information on 1700 Basic Peripheral Equipments (which attach directly to the 1704 Basic Computer) see the 1700 Computer System Reference Manual, Pub. No. 60153100 or the 1714 Computer System Reference Manual, Pub. No. 60364900.

CONTENTS

1706-A BUFFERED DATA CHANNEL

INTRODUCTION

This section describes the CONTROL DATA* 1706-A Buffered Data Channel (BDC), its physical system, and programming information. There is no operating information since the 1706 has no indicators or manual controls.

FUNCTIONAL DESCRIPTION

System Relationship

The 1706 provides a 16-bit, bidirectional, buffered input/output path between the 1704 Computer with a 1705 Interrupt Data Channel (IDC) and up to eight peripheral equipments.

The 1706 may also be used with the 1714 Computer (which may have up to 65K of memory) by using Standard Option 10277-1. This option provides the 1706 with additional addressing capabilities necessary to address up to 65K of memory.

Figure 1 shows the connections between the 1706 and other equipments. The circled numbers indicate the number of connecting cables.

A maximum of three 1706 BDC's may be attached to the 1705 IDC. A 1716 Coupling Data Channel may replace any or all of the 1706's.

Since the 1706 contains no indicators or manual controls, all operations must be initiated by the computer. In response to any I/O instructions and the contents of the Q register, the 1706 connects the computer to one of the external controllers and sends the appropriate Read or Write signal. The 1706 then controls the Read or Write operation. If the contents of the Q register specify a buffered operation, the 1706 obtains access to storage via the Direct Storage Access Bus (DSA) when necessary to fetch or store information. If the (Q) specify a direct input or output, a 16-bit word is transferred from the selected peripheral device to the A register of the 1704 or vice versa.

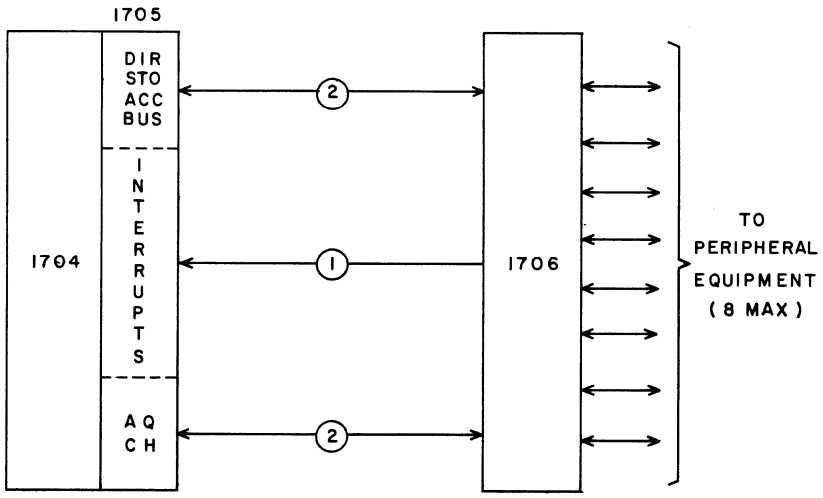

Figure 1. Typical 1704/1705/1706 Configuration.

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Interrupt

An interrupt to the computer can be generated when the 1706 terminates a buffered transfer, i.e., upon end of operation. This interrupt is enabled by an Output from A instruction with the W field (bits 11-15) of the Q register selecting a function to the 1706, and bits 15 and 00 of the A register set. It is disabled by a function to the 1706 and bit 15 of A clear, bit 00 of A set.

An interrupt itself from the 1706 is cleared by a function to the 1706 with bit 00 of A set. Thus, either reselecting or disabling the interrupt selection also clears the interrupt.

Program Protection

The 1706 rejects non-protected Status, Terminate Buffer, Function, and Current Address instructions during a buffer operation that is initiated by a protected instruction. The 1706 has no program protect switch; the program protect feature of a 1700 System is governed by the PROTECT switches on the 1704 and the specific device connected to the 1706. However, if a program protect fault occurs, a status bit is set in the 1706 status reply word.

Reply/Reject

The 1706 responds to an Input or Output instruction within 4 microseconds with either a Reply or Reject signal. The 1706 returns a Reply whenever it can perform the requested operation. Three conditions will cause a Reject to be returned to the computer.

1) The 1706 is Busy when a request for a buffered transfer, a direct input, or a direct output is received;

2) A program protect fault occurs (also see Program Protection);

3) A device returns a Reject upon a direct input/output request.

If for some reason the computer receives no response (for example, the 1706 addressed does not exist in the system), the computer will generate an Internal Reject.

PROGRAMMING

Summary of Programming Information

Tables 1, 2 and 3 are a synopsis of the information necessary to program the 1706. Explanations of the information presented here can be found in the sections following. These tables are intended as a quick reference for the experienced programmer, a preview for the reader studying the following material, and a summary for the reader interested in the general programming capabilities of the 1706.

TABLE 1. 1706 ADDRESSES AND OPERATIONS

W*			COMPUTER INSTRUCTION	
1706 No. 3	1706 No. 2	1706 No. 1	Input to A	Output from A
0C	07	02	Direct Input	Direct Output
0D	08	03	Terminate Buffer, 1706 Current Address	Function (See 1706 Function Table)
0E	09	04	1706 Status	Buffered Output
0F	0A	05	1706 Current Address	Buffered Input

* The left digit is binary, the right digit hexadecimal.

TABLE 2. 1706 FUNCTIONS

Bit in A Register	Meaning
A15 = 1	Set condition for ones in bits A14 - A00
A15 = 0	Clear condition for ones in bits A14 - A00
A14 - A01	(Not defined)
A00	Enable Interrupt on 1706 End of Operation

Addresses

Bits 11-15 of the Q register, called W, are used to select the desired 1706. Bits 00-10 of Q are used to select the peripheral device. The 1706 provides a W=0 signal to devices connected to it. Bit 15, the continue bit, is ordinarily zero when using the 1706. However, this bit may be used by:

1) Addressing the device with the correct code and Q15 set to "0".
2) Using Q15 = 1 for all succeeding addresses to this device.
3) Using Q15 = 0 and a new address to access a different device.

The 1706 interprets an access attempt with Q15 = 1 as a direct input following an Input to A instruction and as a direct output following an Output from A instruction.

Operations

Besides selecting a particular 1706, the W field of Q, combined with a 1704 Input or Output instruction, specifies an operation. The function operation may be further modified by the contents of the A register. Tables 1 and 2 list the addresses, the operations, and the functions. Because W is a 5-bit field and the upper bit (the Continue bit) has a separate use, W is written as two digits; the left digit is binary, the right digit is hexadecimal.

Operations Defined by W and Input to A

Direct Input: Whenever the computer executes an Input instruction to a 1706 with the W field of Q selecting direct input, (Q) is stored in the 1706 and presented to the devices attached to the 1706, and one 16-bit word is transferred into the A register from the selected device. The word may be a data word or the status of the device on the 1706. This mode of operation is identical in every way to that on the AQ channel. The Continue bit (Q15) functions as described under Addresses and in connection with the device being used. If an attempt is made to execute a direct input when the 1706 is busy, the 1706 responds with a Reject. For this reason, it is impossible to determine the status of a device connected to the 1706 during a buffer operation.

* Terminate Buffer, 1706 Current Address: This code terminates a buffered operation and loads into the A register the address of the current word being transferred. The Terminate Buffer operation is intended primarily to terminate hung-up input buffers and in this case the A register contains the address of the next word to have been transferred. Otherwise, the current address may be the address of the last word transferred or of the next word to be transferred, depending on when the Terminate Buffer reaches the 1706 with respect to the timing of the data transfer of the peripheral device. A buffered operation initiated by a protected instruction cannot be terminated by a non-protected Terminate Buffer instruction.

* Terminate buffer operation will cause the 1706 to remain busy for 10 μsec.

1706 Status: This code is a status request which loads into the A register a status reply word showing the current operating conditions of the 1706. A non-protected status request is rejected during a buffer operation initiated by a protected instruction.

1706 Current Address: This code is a status request which loads into the A register the address of the current word being transferred. A non-protected request for the current address is rejected during a buffer operation initiated by a protected instruction.

Operations Defined by W and Output from A

Direct Output: Whenever the computer executes an Output instruction to a 1706 with the W field of Q selecting a direct output, (Q) is stored in the 1706 and presented to the devices attached to the 1706, and one 16-bit word is transferred from the A register to the selected device. This mode of operation is identical in every way to that on the AQ Data Channel. The Continue bit (Q15) functions as described under Addresses and in connection with the device being used. If an attempt is made to do a direct output when the 1706 is busy, the 1706 responds with a Reject.

Function: This code enables and disables Interrupt on End of Operation and clears the interrupt condition, depending upon the contents of the A register. If A15 and A00 = 1, the interrupt is enabled. If A15 = 0, A00 = 1, the interrupt is disabled. When a function is executed with A00 = 1, the interrupt condition is cleared. Thus either reselecting (enabling) the interrupt or disabling the interrupt clears this interrupt condition. A non-protected function instruction is rejected during a buffer operation initiated by a protected instruction.

Buffered Output on the 1706: A buffered output is initiated when the computer executes an Output instruction and the W field of Q selects a buffered output. (Q) is stored in the 1706, then placed on the 1706 channel and the contents of A are transferred to the 1706. The contents of A specifies the first word address minus 1 (FWA-1) of the block to be transferred. The contents of location FWA-1 specifies the last word address plus one (LWA+1) of the block to be transferred. The 1706 begins the data transfer by raising the Write signal to the device. The device responds within 4 μsec by raising the Reply signal to the 1706. The 1706 then advances to the next data word, repeating this cycle until the block of data has been transferred. If the 1706 receives a Reject, it indefinitely repeats the transfer of the word until the word is accepted. The address is not reissued to storage. The 1706 does not generate an Internal Reject. If an attempt is made to establish a buffered output when the 1706 is Busy, the 1706 responds with a Reject.

Buffered Input on the 1706: A buffered input is initiated when the computer executes an Output instruction and the W field of Q selects a buffered input. (Q) is stored in the 1706, then placed on the 1706 channel and the contents of A is transferred to the 1706. The contents of A specifies the location of the first word address minus one (FWA-1) of the block where data is to be stored. The contents of location FWA-1 specifies the last word address plus 1 (LWA+1) of this block. The 1706 begins the data transfer by raising the Read signal to the device. The device responds within 4 μsec by raising the Reply signal to the 1706. The 1706 then advances to the next data word and repeats this cycle until the block of data has been transferred. If the 1706 receives a Reject from the device, it repeats the transfer of the word indefinitely until the word is accepted. The 1706 does not generate an Internal Reject. If an attempt is made to establish a buffered input when the 1706 is Busy, the 1706 will respond with a Reject.

Status Response

1706 Operating Status

Table 3 lists the bits which may be set in the A register following a status request for 1706 operating conditions. The information following Table 3 defines these bits.

TABLE 3. 1706 STATUS RESPONSE BITS

Bit Set In A Register	Meaning
0	Ready
1	Busy
2	Interrupt
3	(Not used)
4	End of Operation
5	(Not used)
6	Program Protect Fault
7	(Not used)
8	Device Reject
9	Device Reply
10 - 15	(Not used)

Ready (Bit 0 = 1) - This bit is set when power is on.

Busy (Bit 1 = 1) - This bit is set from the time the 1706 accepts an output word from the computer initiating a block transfer until the block transfer is terminated, or during a direct operation.

Interrupt (Bit 2 = 1) - An End of Operation Interrupt is being sent to the computer from the 1706.

End of Operation (Bit 4 = 1) - A buffer transfer input or output has been completed.

Program Protect Fault (Bit 6 = 1) - A reference to computer storage caused a program protect fault. The 1700 Reference Manual defines the conditions causing a program protect fault in its Interrupt Section.

Device Reject (Bit 8 = 1) - This bit, if set, means the peripheral device rejected the last word transfer attempted from the 1706.

Device Reply (Bit 9 = 1) - This bit, if set, means the peripheral device accepted the last word transfer attempted from the 1706.

1706 Current Address

This status shows the address of the current word being transferred. It is loaded into the A register following a Terminate Buffer or a 1706 Current Address operation.

1704 Instruction	Q Register	Step	Action
LDQ	Selected 1706 Status Request	1)	Initiate operating status check of desired 1706
INP		2)	A register now contains the operating status of the desired 1706
		3)	Check status in A for Ready and Not Busy
LDQ	W = Direct Input on selected 1706, Bits 0-10 specify status request for equipment	4)	Initiate status check of equipment to be used
INP		5)	A register now contains the equipment status
		6)	Check equipment status for desired conditions.
		7)	Repeat 4-6 for station and unit, if necessary.
LDQ	Selected 1706 Function	8)	Initiate selection or clearing of Interrupt on End of Operation.
LDA		9)	Load A with desired operation
OUT		10)	Interrupt on End of Operation is now enabled or disabled. Any existing interrupt is cleared.
LDQ	W = Direct Output on selected 1706. Bits 0-10 specify an operation on the equipment or station.	11)	Initiate selection of peripheral equipment operating conditions and interrupts.
LDA		12)	If necessary, load A with the code further specifying the operation indicated by (Q).
OUT		13)	Execute Output from A instruction
		14)	Repeat 11-13 until all desired operating conditions are specified.
	For a Direct Input or Output of Data		
LDQ	W = Direct Input or Direct Output on selected 1706. Bits 1-10 select equipment and station. Bit 0 = "0" for data transfer.	15D)*	Select desired type of I/O.
LDA		16D)	If doing a direct output, load the data into A; if direct input, skip this step.

* D indicates a step for the direct transfer of data.

1704 Instruction	Q Register	Step	Action
INP or OUT		17D)	Execute 1704 Input to A or Output from A, depending on desired direction of data transfer.
		18D)	Skip to 19)
	For a Buffered Transfer of Data		
LDQ	W = Buffered Input or Buffered Output on selected 1706. Bits 1-10 select equipment and station. Bit 0 = "0" for data transfer.	15B)*	Select desired type of buffered I/O.
LDA		16B)	Load A with the FWA-1 of the buffer area. The contents of memory at this address must contain the LWA + 1 of the buffer area.
OUT		17B)	The buffered transfer is now initiated and under control of the 1706.
		18B)	Go to step 19).
		19)	Status the converter (as in steps 1-3, checking for desired conditions, or by using the 1706 current address status) or proceed with the main program until an interrupt occurs. Using interrupts takes advantage of the capabilities of the buffered data channel to do I/O without hanging up the computer. It is not possible to status a device connected to the 1706 as long as the 1706 is Busy.

*B indicates a step for the buffered transfer of data.

COMMENTS

If a buffered operation becomes hung up, LDQ with W selecting Terminate Buffer for the appropriate 1706, and execute an INP instruction. The buffered operation is terminated and the current address is sent to A. The program can check this address and take the desired action.

One method of determining if the 1706 is hung up is to select the device's Interrupt on End of Operation. When the interrupt is recognized, check the operating status of the 1706. If the 1706 is still Busy, the buffered operation is hung up. Do a status check of the 1706 current address. If the current address does not equal the LWA + 1, the equipment is hung up.

A second method is to do a status check of the 1706 current address. Then wait until at least one more word should have been transferred and again check the current address. If it is unchanged, the buffered operation is hung up. This method requires knowing instruction execution times and the rate of data transfer.

If an INP or OUT instruction results in a Reject, the program proceeds as described in connection with these instructions in the computer reference manual.

COMMENT SHEET

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