CONTROL DATA
CORPORATION

CONTROL DATA® 1749

COMMUNICATIONS TERMINAL CONTROLLER

CUSTOMER ENGINEERING MANUAL

- Theory of Operation
- Maintenance
- Installation
- Parts List
- Diagrams
- Card Placement

RECORD OF REVISIONS		
Rev.	Date	Notes
A	5-22-67	Revised to reflect ECO DP-2400.
B	1-23-68	Revised to incorporate FCOs DP2715 and 2795. Pages revised: 1-6,1-7,1-10,1-11, 1-29,2-3,A-2,A-3.
C	5-7-68	Reprinted to incorporate ECOs DP2952 and DP3056 and ECO DP3014, and revisions to the manual. Pages revised: v,1-7,1-10,1-11,1-12,1-13,1-20,1-21, 1-24,1-25,1-29,A-1,A-2. New Product designation is 1749-A05.
D	12-2-68	Revised to incorporate ECO DP03118 and ECO DP03216. Pages revised 2-9,A-1 and A-2. This manual is correct through product designations 1749-A05 and 1749-B01.
E	8-25-69	Revised reprint. Incorporates ECOs DP03434, DP03484, DP03498. Pages revised: v,1-7,1-9,1-10,1-11,1-13,1-15, 1-17,1-19,1-21,1-23,1-25,1-27,1-29,2-1, 2-3,2-9,A-1,A-2,A-3. Pages added: 1-30 (p15 of 36968300). This revision supersedes all previous editions and is correct through product designations 1749-A06 and -B02.
F	10-24-69	Revised to incorporate ECO DP03526A. Pages revised: A-1, sheets 1, 15 of LD36968300. Product designation remains -A06, -B02.

36827000

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SECTION II
INSTALLATION AND MAINTENANCE

APPENDIX A
PARTS LIST

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INTRODUCTION

SCOPE

This manual contains information detailing the theory of operation, maintenance, and installation of the CONTROL DATA 1749-A (120 volt 60 Hz model) and 1749-B (220 or 240 volt 50 Hz model) Communications Terminal Controller (1749 CTC).

GENERAL

The 1749 CTC is a data-handling device that regulates data transmission between a 1700-series Computer and remote sites via up to 16 full-duplex digital communication lines. These communication lines include up to 16 teletypewriter lines or up to eight voice-grade lines via a suitable modem. The communication lines are terminated with plug-in data terminals which mount in the 1749 CTC.

REFERENCE DOCUMENTS

This manual is intended to be used with the following documents when relevant:

1749 Communications Terminal Controller Reference Manual, pub. no. 368 271 00.

1749 Communications Terminal Controller Maintenance Aids Manual, pub. no. 368 291 00.

8909-G Test Board Drawer Reference/Customer Engineering Manual, pub. no. 368 289 00.

8909-H Test Board Unit Reference Manual, pub. no. 137 973 00.

8909-H Test Board Unit Customer Engineering Manual, Vol. I of II, pub. no. 137 997 00.

8909-H Test Board Unit Customer Engineering Manual, Vol. II of II, pub. no. 416 001 00.

SECTION I
THEORY OF OPERATION/DIAGRAMS

FUNCTIONAL DESCRIPTION

Figure 1-1 is a block diagram of the 1749 CTC. The 1749 CTC scans the data terminals at the command of the computer and either receives data from the receive data terminals or outputs data to the output data terminals. Two scan modes service the input and output data terminals.

In the sequential scan mode, a four-stage scan counter is incremented so that the output of the counter corresponds to the address of a data terminal. In this mode the scan counter is incremented and the data terminals serviced sequentially according to select and function codes received from the computer. An output from the computer can also be accomplished in this mode without incrementing the counter.

In the direct address mode the select code received from the computer drives the counter to the count corresponding to the address of the data terminal. In this mode any of the 16 data terminals can be selected by the computer issuing the applicable select code.

Output data is received from the computer as an 8-bit word accompanied by an activity bit. Status is sent to the computer as a 12-bit word. Select codes are received from the computer as 11-bit words. These codes are accompanied by a control signal (Read, Write, or Program Protect) that indicates the applicable control logic sequence.

The function codes issued by the computer determine the interrupt conditions to which the 1749 CTC responds. These function codes select one of the following interrupt conditions:

(1) Timed Interrupt (Interrupt Clock Control)

(2) Interrupt on Character Ready plus timed Interrupt Interval

(3) Interrupt on Character Request plus timed Interrupt Interval

(4) Interrupt on Fault Control plus timed Interrupt Interval

These interrupt conditions are in addition to the interrupt clock cycle. Under no circumstances is an interrupt generated more often than the interrupt clock cycle.

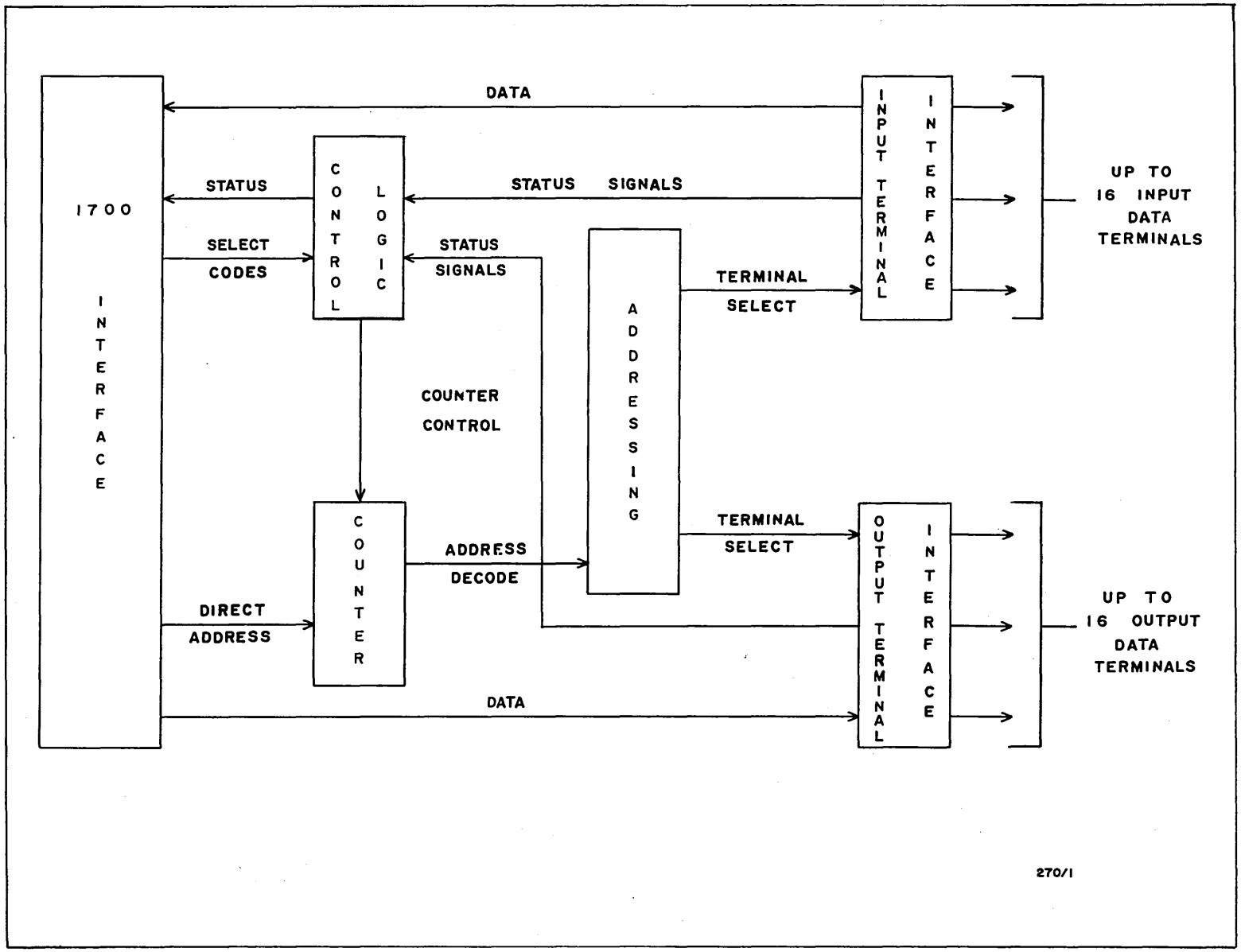


Figure 1-1. 1749 CTC - Block Diagram

LOGIC DESCRIPTION

The logic description in this section is on the page facing the logic diagram on which the circuit appears. Sheet numbers in parentheses refer to the sheet of the logic diagram where the circuit being referenced is found.

Table 1-1 lists the abbreviations used on the logic diagrams.

TABLE 1-1. ABBREVIATIONS USED ON LOGIC DIAGRAMS

ABBREVIATION	DEFINITION
ARQ	Activity Request
CFF	Clear Flip-Flop
CLK	Clock
CLR	Clear
CNT	Count
CRD	Character Ready
CRQ	Character Request
DRW	Delayed Read or Write
GFF	Gate Flip-Flop
GIA	Gate Input Acknowledge
GIP	Gate Input
GOA	Gate Output Acknowledge
GST	Gate Status (data terminal status)
INH	Inhibit
INT	Interrupt
MC	Master Clear
PP	Program Protected
PRT	Protect
Ø	Alphabetical "O"
RD	Read
RDY	Ready
REQ	Request
RJ	Reject
RP	Reply
ROW	Read or Write
SDI	Select Data In
SEL	Selected
SRW	Select Read or Write
STA	Status
ST 1	Status 1
ST 0	Status 0
WR	Write

CARD PLACEMENT

Pages 1-28 and 1-29 are diagrams illustrating the card placement of the logic cards used in the 1749 CTC. These diagrams also illustrate the switch locations and the location of the master clock oscillator on the logic rack.

SELECT CODE FORMAT

Figure 1-2 illustrates the select code format used in the 1749 CTC. Since the W field bits are not necessary to address the 16 channels in the 1749 CTC these bits are "0"s in the Q register of the 1700 Computer. These bits are expressed by the W = 0 signal which is a "1" whenever the W field bits are "0". The E field bits must correspond to the setting of the equipment select switch in the 1749 CTC. The command bits are the seven lowest order bits (Q00 through Q06) received in the select code and are expressed as two digits (i.e., C = 01). In this case, the "0" represents the highest order three bits (Q04 through Q06) and the "1" represents the lowest order four bits (Q00 through Q03).

"1"	X	X	X	X	"0"	"0"	X	X	X	X	X
W = 0	Q10	Q09	Q08	Q07	Q06	Q05	Q04	Q03	Q02	Q01	Q00
	E				COMMAND						

W = 0 is a static "1" signal
Q06 and Q05 are static "0" signals

270/3

Figure 1-2. Select Code Format

SHEET REVISION STATUS															REVISION RECORD						
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	3434	SEE ECO	T.K.S.	4-29-9	R.H.	R.H.
J	H	H	H	H	H	H	H	H	H	H	H	H	H	J	J	3498	SEE ECO	W.R.	8-18-69	R.H.	R.H.

SIDE CAR 36968300

REFERENCE DRAWINGS

COMPONENTS, EXCEPT AS NOTED	TOLERANCE	VALUE	RATING
RES			
CAP			

CONTROL DATA — COMMUNICATIONS SYSTEMS DIVISION

FIRST USED ON	1749	
DWN	J.L. WEISS	6-17-66
CHK	R. WALDACK	6-17-66
ENGR		
MFG		
APPR	R. WALDACK	6-17-66

TITLE

COMMUNICATION TERMINAL CONTROLLER

LOGIC DIAGRAM

CODE IDENT 28491 | C | DRAWING NUMBER 36968300

SHEET 1 OF 15

36968300 .1

ADDRESS AND CONTROL

The 1749 CTC receives data terminal address information as select codes at R000 through R010 via connector P4B1. These select codes together with function control signals at R040, R031, R030, and R021 initiate the logical operations necessary to select the data terminal and the input or output operation. The upper four bits (7 through 10) of the select code are decoded by the equipment select switch. This switch may be set to any equipment number (0 through F, hexadecimal). Bits 7 through 10 of the select code must agree to the setting of the equipment select switch for the 1749 CTC to be connected to the computer. A valid select code together with a Read or Write signal received from the computer sets the SEL FF (K000/001) via A011, R020, A010, and A012. The set output of K000/001 conditions AND gates in the Reject (I030) and Status (I100) inverters (sheet 4) and the Reject and Reply output cards (T030, and T031, sheet 3). If the select code received from the computer is not a valid code, K000/001 is cleared by A010. The clear output of K000/001 produces a "1" at A015. A "1" output of A015 prevents an SRW signal from being generated at A114 and a gate pulse from being generated to the counter at I111.

MASTER CLEAR

The Master Clear signal is a "1" signal received from the computer at R040. This signal clears the input/output (I/O) channels to the computer and disconnects the 1749 CTC. Receiving the Master Clear signal produces a "1" at the output of A041. The output of A041 is sent to the data terminals in the 1749 CTC, via L200 through L203. The Master Clear signal is used by the data terminals as a Disconnect signal and to return designated logic circuits to initial conditions. The "1" output of A041 also clears the Select FF (K000/001) in the 1749 CTC and generates a "1" at the CFF inverter in the input and output control logic (sheet 4) and a "1" at the CLR inverter (I104) in the counter control logic. When power is initially applied to the 1749 CTC, Y044 and A044 generate a Master Clear signal for approximately 300 ms.

PROGRAM PROTECT

The Program Protect signal is a "1" signal received by the computer, indicating that this data transfer was initiated by an I/O instruction whose program protect bit is set. The program protect mode of operation is selected in the 1749 CTC by the program protect switch on the logic rack at the back of the cabinet. With this switch at PROTECTED, the program protected indicator on the logic rack lights and the Protected FF (K002/003) sets whenever a Program Protected signal is received from the computer at R021 and a Read or Write from A034. When the Program Protect signal from the computer is not present K002/003 clears if a Read or Write signal is present at A034. The clear output of K002/003 maintains the output of A014 (Select Read or Write) at "0" and A015 at "1". A Reject signal (sheet 4) is generated if the computer outputs a select code that is not accompanied by a protect bit in this mode.

When the program protect switch is at NOT PROTECTED, the output of A021 is a constant "1". The output of A021 together with a "1" from A034 sets K002/003. This FF remains set as long as the switch is at NOT PROTECTED.

Inverters A004 and A005 select the direct address capability or addressing by sequentially advancing the counter. If direct addressing is utilized, R004 is a "1" producing a "0" at A004 and A005, and a "1" at A114. The output of A114 conditions AND gates to the first rank of the counter (sheet 5) during direct addressing. If the sequential advancing of the counter is utilized for addressing, R004 is a "0" and A114 is maintained at "0". In direct addressing, inverters A000 through A003 together with R000 through R003 drive the first rank of the counter to the count corresponding to the address of the selected data terminals.

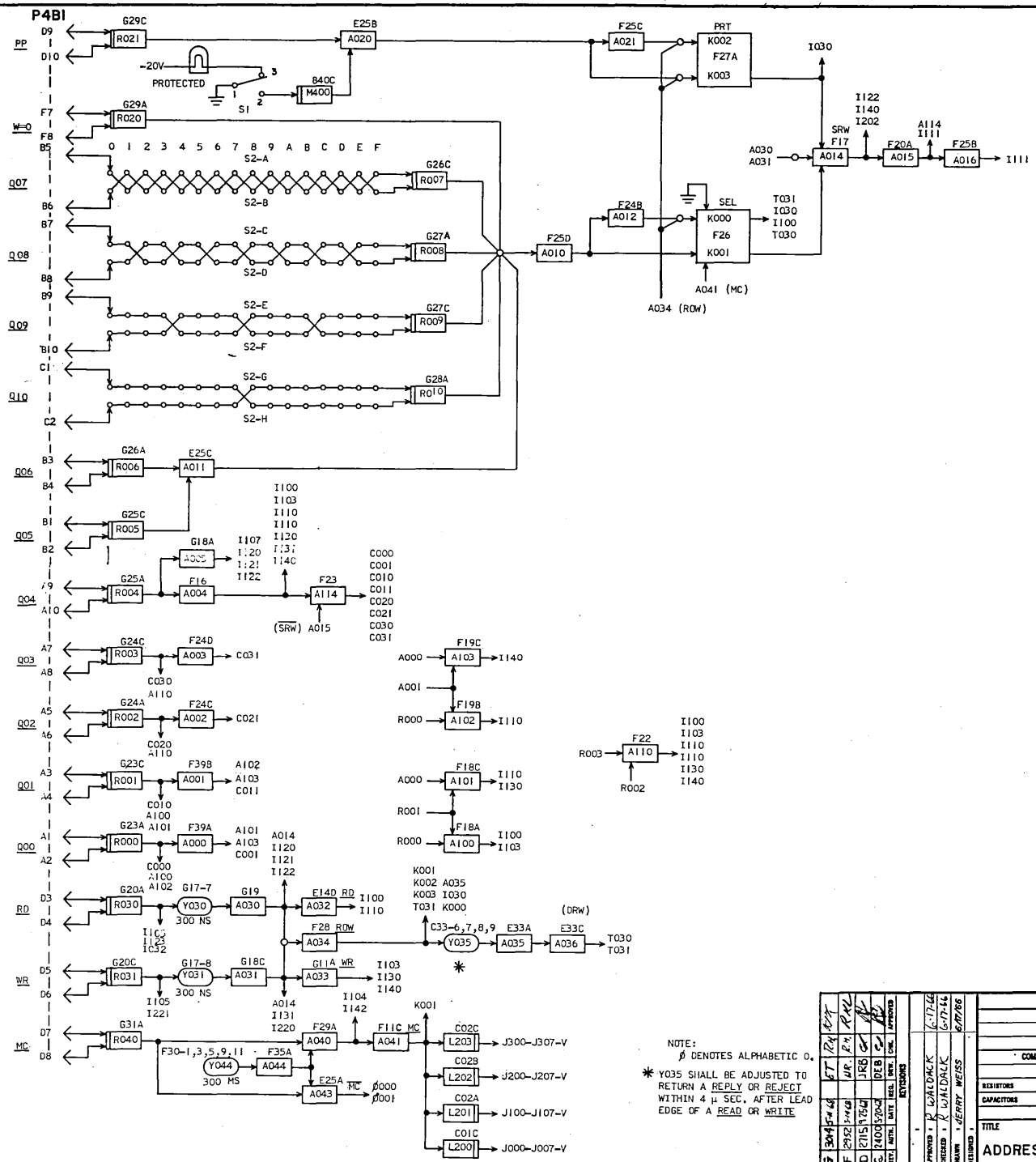
READ

The Read signal is a "1" signal received from the computer at R030, initiating an input transfer to the computer of one word. After a 300-nanosecond (nsec) delay, "1"s are produced at the outputs of the Read inverter (A032) and the Read or Write inverter (A034). The "1" output of A032 conditions AND gates to the status inverters (I100) and to gating inverter (I110). After a 3.4 ± 0.2 usec delay the "1" output of A034 produces a "1" at the DRW inverter (A036). The output of A034 conditions the AND gates to the Reject output card (T030) and the Reply output card (T031, sheet 3). The 4.0-usec delay ensures that sufficient time elapses, enabling the operation to take place before a Reply or Reject signal is returned to the computer. The output of A034 also provides a gating function to various operations (Select, Program Protect, etc.).

Receiving a Read signal also produces a "1" at the output of the SRW inverter (A014). The output of A014 conditions AND gates in the input and output control circuits (sheet 4). A "1" output of A014 also maintains A015 at "0". A "0" output at A015 enables A114 to be controlled by the data bit at R004.

WRITE

The Write function control signal is a "1" signal received from the computer at R031, initiating an output of one word. After a 300-nsec delay "1"s are produced at the output of the Write inverter (A033) and the Read or Write inverter (A034). The output of A033 conditions AND gates in the counter control circuits (sheet 5). Receiving the Write signal also produces a "1" at the output of the Select Read or Write inverter (A014).


P4B1
PP
W=0
Q07
Q08
Q09
Q10
Q06
Q05
Q04
Q03
Q02
Q01
Q00
RD
WR
MC
PROTECTED
-20V
S1
S2-A
S2-B
S2-C
S2-D
S2-E
S2-F
S2-G
S2-H
A034 (ROW)
A041 (MC)
(SRW) A015
(DRW)
F28 ROW
K001
K002 A035
K003 I030
T031 K000
C33-6,7,8,9
300 NS
300 MS
F30-1,3,5,9,11
NOTE:
Ø DENOTES ALPHABETIC O.
* Y035 SHALL BE ADJUSTED TO RETURN A REPLY OR REJECT WITHIN 4 μ SEC. AFTER LEAD EDGE OF A READ OR WRITE
REFERENCE DRAWINGS
COMPONENTS (UNLESS OTHERWISE INDICATED)
TOLERANCE
VALUE
SIZE
RESISTORS
CAPACITORS
CONTROL DATA
CORPORATION
INDUSTRIAL DATA PROCESSING DIVISION
MINNEAPOLIS, MINNESOTA
PROJECT OR PRODUCT
1749
DRAWING NUMBER
36968300
REV.
SHT
2
PAGE
TITLE
ADDRESS AND CONTROL
APPROVED
CHECKED
DRAWN
DESIGNED
REVISIONS

COMPUTER DATA INPUT AND OUTPUT INTERFACE

Data and status is exchanged between the computer and the 1749 CTC via connector P4A1. The status bits from the 1749 CTC are sent to the computer in the form of a 12-bit word. The four highest order bits (8 through 11) are status bits from the data terminals and are present if any terminal unit has its bit present. Bits 4 through 7 reflect the status of the Interrupt Control FFs, and bits 0 through 3 reflect the status of the Counter FFs.

Data is received from the computer as an 8-bit word at R100 through R107. The 8-bit data word is accompanied by an activity bit (bit 11) at R111. The activity bit must be present for an output to the output data terminals to be accomplished. The activity bit conditions AND gates in the input and output control logic (sheet 4) to generate a Reply and Acknowledge Request signal. If an output is sent to a data terminal and the activity bit is not present a Reject signal is generated in the input and output control logic via I211, I030, and I031.

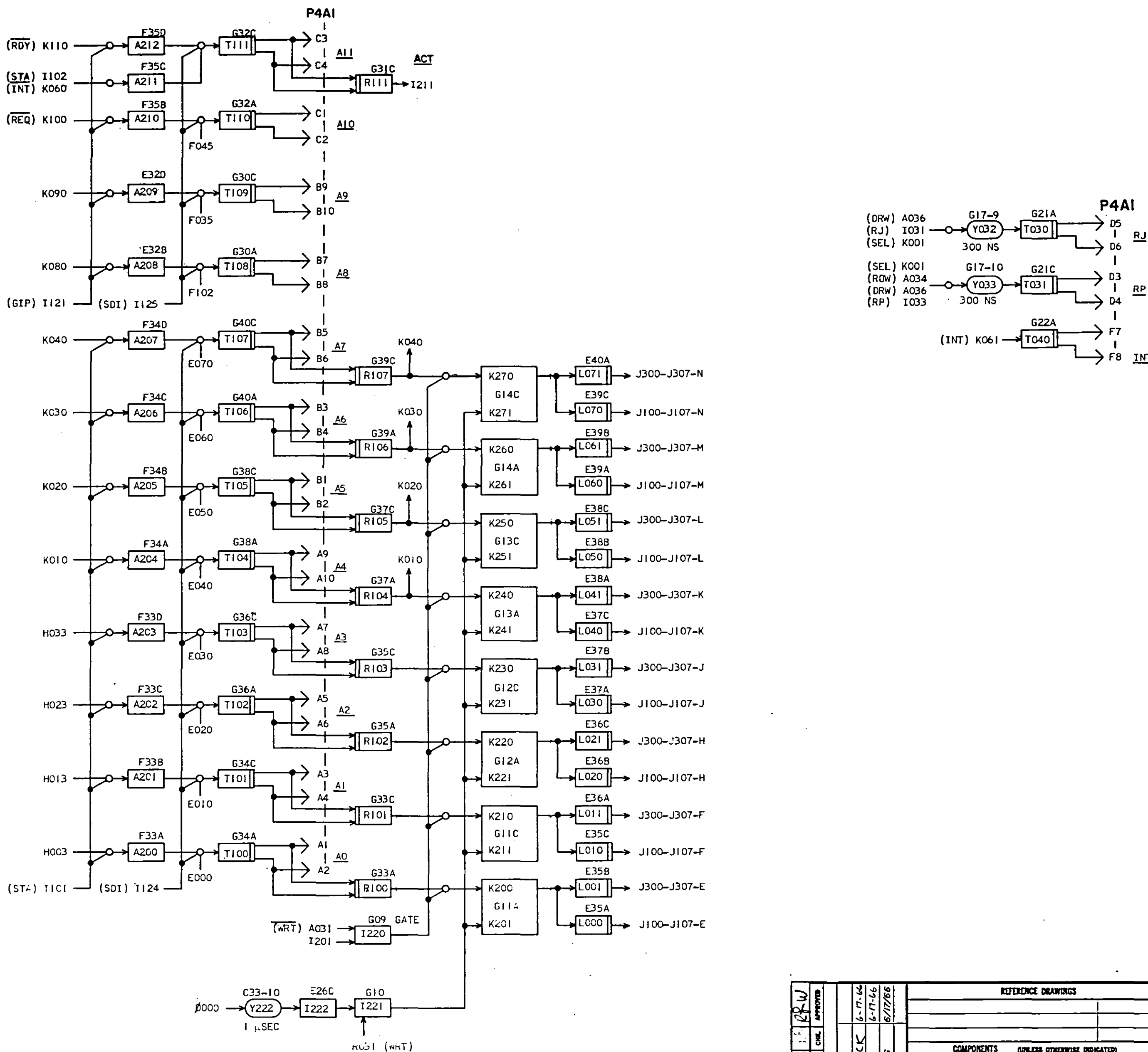
The 8-bit data word at R100 through R107 is gated to the Output FFs by the gate inverter (I220). The output of I220 is a "1" for 1 usec after the Write signal is received, gating the data word into the applicable Output FF. One usec after the Character Request signal from the output data terminal drops, a "1" is generated at I221, clearing the Output FFs.

The Reject and Reply signals are sent to the computer by T030 and T031 respectively via connector P4A1. The Reject signal is gated after a 300-nsec delay by a DRW from A036 and a SEL from K001. The Reply signal is gated after a 300-nsec delay by an SEL from A016, a ROW from A034, and a DRW from A036.

The Interrupt signal is sent to the computer by T040 via connector P4A1.

TERM	LOCATION	* PAGE	DEFINITION
A031	G18C	2	$\overline{\text{WRT}}$
A034	F28	2	ROW
A036	E33C	2	DRW
H003	F37B	5	
H013	F37D	5	
H023	F38B	5	
H033	F38D	5	
I031	F15C	4	RJ
I033	F15D	4	RP
I101	F32	4	STA
I102	E28A	4	STA
I121	E13	4	GIP
I124	F36	4	SDI
I201	G16C	4	DRW
K001	F26	2	SEL
K010	F09A	4	
K020	F09C	4	
K030	F10A	4	
K040	F10C	4	
K060	F27C	4	
K061	F27C	4	INT
K080	C23A	4	STO
K090	C23C	4	STI
K100	F14A	4	REQ
K110	F14C	4	RDY
Ø000	E05A	4	
R031	G20C	2	(WRT)

* Page denotes sheet of logic diagram.



NOTE:

ø DENOTES ALPHABETIC O.

REFERENCE DRAWINGS	

COMPONENTS (UNLESS OTHERWISE INDICATED)	TOLERANCE	VALUE	SIZE
RESISTORS			
CAPACITORS			

DESIGNED: JERRY WEISS 6/17/66

DRAWN: K. WALDACK 6-17-66

CHECKED: K. WALDACK 6-17-66

APPROVED:

TITLE: COMPUTER DATA INPUT AND OUTPUT INTERFACE

CONTROL DATA CORPORATION

INDUSTRIAL DATA PROCESSING DIVISION

MINNEAPOLIS, MINNESOTA

PROJECT OR PRODUCT: 1749

DRAWING NUMBER: 36968300

REV: H

SHT: 3

INTERRUPT AND CONTROL

The interrupt sequence is determined by control function signals issued by the computer at R104 through R107 via P4A1 (sheet 2). The control function signals are accompanied by a Write signal and a select code where C = 03 at P4B1 (sheet 2). This select code produces a "1" at the GFF (I141) and a 500-nsec "1" at the CFF (I142). The output of I141 gates the control function signal to set the applicable Interrupt Control FF. The 500-nsec output of I142 clears the Interrupt FFs not selected by the control function signals. A "1" at R104 together with I141 sets K010/011 and maintains I050 at "0". The rate at which interrupt signals are generated is determined by the interrupt clock (see clock circuit on sheet 15 of logic diagram). C050 is a free-running, unijunctional clock. The frequency of the output signals is determined by a rotary speed select switch, and by adjusting the variable resistance on C050. Three inverters (I051, I052, I053) and delay Y052 form a pulse-shaping circuit. Once every cycle of C050, a 1 usec "1" is produced at I051 which sets the Interrupt FF (K060/001). The set output of this FF is sent to the computer via T040 and P4A1. The computer issues a Write signal and a select code (where C=00) which clear FF K060/061. This select code produces a clear signal at I104 in the counter control logic (sheet 5). The output of I104 clears K060/061.

A "1" from the computer at either R105, R106, or R107 together with I141 sets Interrupt on Character Ready FF (K020/021), Interrupt on Character Request FF (K030/031), or Interrupt on Fault FF (K040/041) respectively. The set outputs of these FFs generate an Interrupt signal whenever the applicable status gate inverter (F040, F030, or F100, sheet 4) is a "1" and the Interrupt Clock generates a "1".

When the C = 03 select code from the computer drops, the selected Interrupt Control FF remains set until another control function signal is issued or a Master Clear signal is received from the computer. A Master Clear signal disables the AND gate to the CFF inverter (I142), producing a Clear signal to the Interrupt Control FFs.

INPUT AND OUTPUT CONTROL

OUTPUT

The output function (Write) is initiated by the computer issuing a Write signal together with a select code. Receiving the Write signal produces a "1" at the Select Read or Write inverter (A014, sheet 2). One usec after A014 became a "1", a "1" is generated at the DRW inverter (I201) and a "0" at NOT DRW (I200). The 1-usec delay insures that the addressing of the data terminal is completed before the read or write operation is actually initiated.

The "1" at I201 generates a 500-nsec gating pulse at the GST inverter (I107). The output of I107 conditions the AND gates to the status FFs (K080/081, ST0; K090/091, ST1; K100/101, Character Request; and K110/111, Character Ready). These AND gates are enabled by the applicable status inverter from the data terminals. If a Character Request signal is present from the data terminal addressed, the Character Request FF (K100/101) sets. The set output of K100/101 together with the activity bit from R111 produces a "1" at the Activity Request inverter (I210). The output of I210 conditions an AND gate in the GOA circuit. If the output of K101 or the activity bit is not present a Reject signal is generated via I030 and I031.

When the 1-usec delay to I202 has expired I200 becomes a "0"; enabling the output of I131 to become a "1". The output of I131 together with an Activity Request from I210 and Request from E100 produces a "1" at the Gate Output Acknowledge inverters (Ø001, Ø002, and Ø003). The output of these inverters gates the Output Acknowledge signal to the selected data terminal. These inverters are maintained in this condition until the Request signal at E100 drops.

INPUT (Read)

The input function (read) is initiated by the computer issuing a Read signal together with a select code. The Read signal after 1 usec drops the NOT DRW signal at I200 and generates a DRW signal at I201 as covered in the discussion of the output function. The "0" at I200 enables Gate Input inverters I121 and I120 to become "1"s. The outputs of I121 and I120 are also determined by the status of I110 and A005. When the NOT RD inverter (A030) and either I110 or A005 are "0"s, I121 and I120 are "1"s. The "1" output of I121 also generates "1"s at inverters I124 and I125. The outputs of I124 and I125 condition the AND gates to the output to the computer cards (T100 through T111). These AND gates must be enabled before the 1749 CTC can send data or status bits to the computer.

The "1" at I201 also generates a gating pulse to the status FFs as described in the discussion of the output operation. The set output of the status FFs together with the associated data terminal Status Input inverter (E100, E090, and E080 respectively) enables AND gates to E200. When any of these FFs is set and the status input from the data terminal is a "1", a "1" is produced at E201. The "1" output of E201 enables the holding circuit for Gate Input Acknowledge (Ø010 and Ø011) until the data terminal acknowledges receipt of Input Acknowledge by dropping the "1" at the Status Input inverter.

When the computer receives the data word the Read signal goes to a "0", making the DRW signal at I201 a "0". At this time a "1" is generated at I122 for 500 nsec. The "1" at I122 enables the AND gate to Ø010. This AND gate is conditioned by status inverter E201. Enabling this AND gate produces a "1" at the GIA inverters (Ø011, Ø012, and Ø013). The "1" outputs of these inverters send an Input Acknowledge signal to the selected input data terminal, indicating that the input to the computer is accomplished. The GIA inverters are held at "1" until E201 becomes a "0". E201 becomes a "0" when the Character Ready signal from the input data terminal drops.

STATUS INPUT

A Read signal and a select code of C = 00 received from the computer produce "1"s at inverters I101 and I102. The output of I101 conditions the status input gates to the Status Input inverters (sheet 3). These AND gates must be conditioned before a status input to the computer can be accomplished.

REJECT

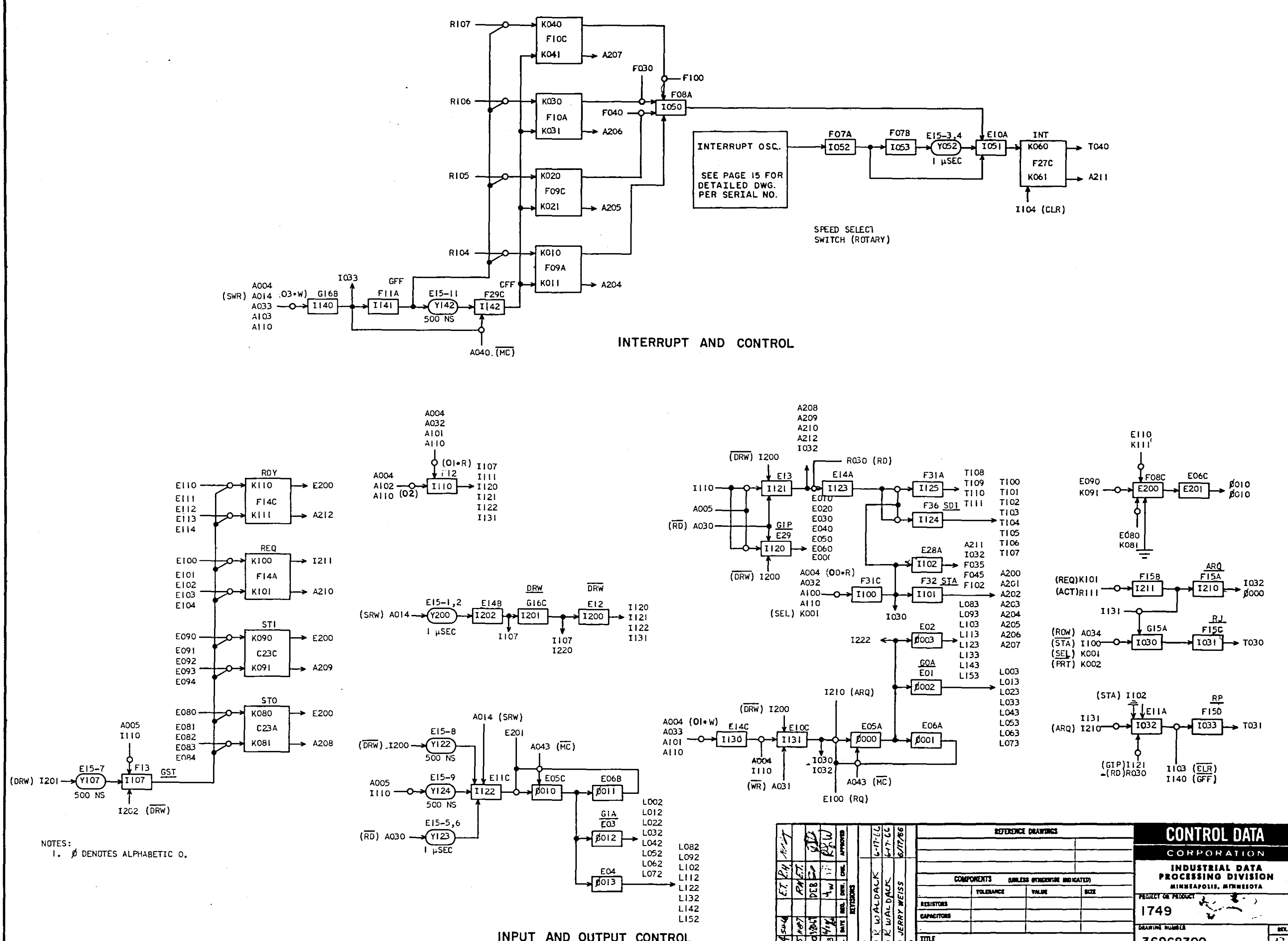
A protect fault detected by K002/003 (sheet 2) or an output sent to an output data terminal without the presence of a request of activity bit generates a "1" at the output of the Reject inverter (I031). If the Select FF (K000/001) is set the Reject signal is sent to the computer via T030 (sheet 3), indicating to the computer that the operation cannot be accomplished.

REPLY

A "1" is generated at the Reply inverter (I033) in response to the successful completion of a read or write instruction. These instructions include a "1" at either Status inverter I102, Gate Input inverter I121, and Activity Request inverter I210 together with I131 or Gate Input Inverter I121. If a Select Read or Write signal is present at A014 (sheet 2) the Reply signal is sent to the computer via T031 (sheet 3).

TERM	LOCATION	*PAGE	DEFINITION
A004	F16	2	
A005	G18A	2	
A014	F17	2	$\overline{\text{SRW}}$
A030	G19	2	$\overline{\text{RD}}$
A031	G18C	2	$\overline{\text{WR}}$
A032	E140	2	RD
A033	G11A	2	WR
A034	F28	2	ROW
A040	F29A	2	$\overline{\text{MC}}$
A043	E25A	2	MC
A100	F18A	2	
A101	F18C	2	
A102	F19B	2	
A103	F19C	2	
A110	F22	2	
E080	E09A	8	
E081	C21A	8	
E082	C21C	8	
E083	C22A	8	
E084	C22C	8	
E090	E09B	8	
E091	C25A	8	
E092	C25C	8	
E093	C26A	8	
E094	C26C	8	
E100	F20C	8	
E101	C27A	8	
E102	C27C	8	
E103	C28A	8	
E104	C28C	8	
E110	E09C	8	
E111	C29A	8	
E112	C29C	8	
E113	C30A	8	
E114	C30C	8	
F030	E34A	6	CRQ
F040	E34C	6	CRD
F100	E36A	6	
I103	E26D	5	$\overline{\text{CLR}}$
I104	E28C	5	CLR
K001	F36	2	$\overline{\text{SEL}}$
K002	F37A	2	$\overline{\text{PRT}}$
R030	G20A	2	RD
R104	G37A	3	
R105	G37C	3	
R106	G39A	3	
R107	G39C	3	
R111	G31C	3	ACT

*Page denotes sheet of logic diagram.



NOTES:
1. Ø DENOTES ALPHABETIC O.

CONTROL DATA CORPORATION
INDUSTRIAL DATA PROCESSING DIVISION
MINNEAPOLIS, MINNESOTA

PROJECT OR PRODUCT: 1749

DRAWING NUMBER: 36968300

TITLE: CONTROL AND INTERRUPT

DESIGNED: JERRY WEISS
DRAWN: K. WALDACK
CHECKED: K. WALDACK

REFERENCE DRAWINGS

COMPONENTS (UNLESS OTHERWISE INDICATED)

	TOLERANCE	VALUE	SIZE
RESISTORS			
CAPACITORS			

COUNTER

The output of the Counter FFs (C000/001, C010,/011, C020/021, and C030/C031) corresponds to the address of one of the 16 (0 through 15) data channels. The counter and consequently the addressing of the data terminals can either be advanced sequentially, by increasing the count of the counter by one, or by directly driving the counter to the desired address.

In sequential operation a Read signal together with a select code of C = 01 or a Read or Write signal and a select code of C = 02 produces a 500-usec advance pulse at I111. A "0" from the Select Read or Write inverter (A015) enables an advance pulse to be generated when a Read or Write signal is present. A "0" from I110 generates an advance pulse during a C = 01 Read or a C = 02 Read or Write.

At the same time that the first rank of the counter is advancing, the Read or Write signal produces a "0" at the Inhibit inverter (I105). A "0" at I105 disables the AND gates to the FFs in the second rank of the counter. This prevents the second rank of the counter from advancing until after the first rank count is completed.

A Write signal and a select code of C = 00 preset the counter to a count of 15 via inverter I104. The next advance pulse generated at I111 advances the counter to a count of zero. This procedure may be used to determine the starting point for sequentially servicing the data terminals.

In direct addressing the output of the counter is set to the address issued by the computer at R000 through R003 (sheet 2). In this case the first rank of the counter is either set or cleared by address bits R000 through R003 or the NOT address output of inverters A000 through A003 together with a "1" from A114.

ADDRESS DECODE

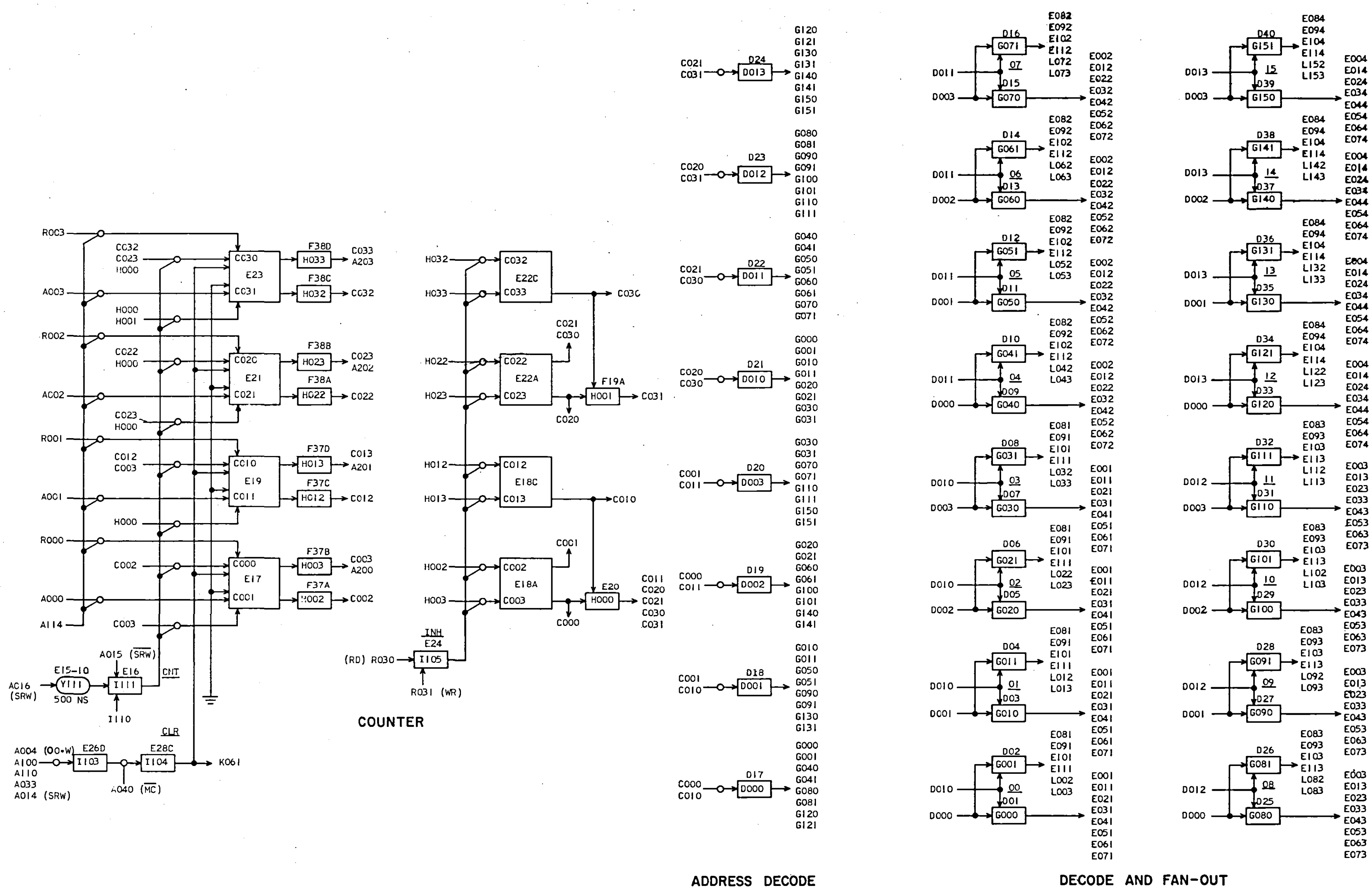
The Address Decode inverters (D000 through D013) receive addressing information from the first rank of the counter. The output of these inverters is normally a "1". The proper count from the counter enables the AND gate to the inverter, producting a "0" at the output. The output of these inverters provides the addressing information to the Decode and Fan-Out inverters.

DECODE AND FAN-OUT

The Decode and Fan-Out inverters gate the Output Acknowledge signal to the output data terminals, the Input Acknowledge signal to the input data terminals, and the channel-selected information to the Data and Status Input Gate inverters. A "0" from both Address Decoder inverters whose inputs correspond to the value of the desired channel, produces a "1" at the output of that Decode and Fan-Out inverter. This "1" output provides the gating signal to the applicable data terminal or input gate inverter.

TERM	LOCATION	*PAGE	DEFINITION
A000	F39A	2	
A001	F34B	2	
A002	F24C	2	
A003	F24D	2	
A004	F16	2	
A014	F17	2	SRW
A015	F25B	2	$\overline{\text{SRW}}$
A016	F25B	2	SRW
A033	A16A	2	$\underline{\text{WR}}$
A040	F29A	2	
A100	F18A	2	
A110	F22	2	
A114	F23	2	
I110	F12	4	
R000	G23A	2	
R001	G23C	2	
R002	G24A	2	
R003	G24C	2	
R030	G20A	2	
R031	G20C	2	

*Page denotes sheet of logic diagram.



CONTROL DATA CORPORATION

INDUSTRIAL DATA PROCESSING DIVISION
MINNEAPOLIS, MINNESOTA

REFERENCE DRAWINGS

COMPONENTS (UNLESS OTHERWISE INDICATED)

	TOLERANCE	VALUE	SIZE
RESISTORS			
CAPACITORS			

DESIGNED · JERRY WEISS 6/17/66
DRAWN · R. WALDACK 6-17-66
CHECKED · R. WALDACK 6-17-66

PROJECT OR PRODUCT: 1749

TITLE: COUNTER AND ADDRESS DECODE AND FAN-OUT

DRAWING NUMBER: 36968300

REV.: B

SHT 5

START OF DAY

The start-of-day circuit prevents erroneous data bits that may be present in the output data terminals from being transmitted at the start of a day's operation.

The start-of-day circuit is controlled by a signal line from the test board unit. When power is applied to the system the test board unit grounds this signal line. Grounding this signal line energizes relays X000 and X010. Energizing these relays applies a ground to Z000 through Z007 and Z010 through Z017 sending a static "1" Output Acknowledge signal to the output data terminals. The Output Acknowledge signal causes the output data terminal to begin to output data and to clear their holding registers. During the start-of-day operation the test board unit disables all of its send relays so that data received from the Output data terminal is not applied to the communications lines.

Actuating the START OF DAY switch (normally located on the systems console or the test board unit) removes the ground on the start-of-day signal line. This de-energizes relays X000 and X010 and resets all output data terminal clocks which assume an idle condition with their holding registers cleared.

EXTERNAL CLOCK

Connector J100 provides the electrical connection for installing a crystal oscillator assembly to operate as a master clock timing source. This oscillator is installed when operating with data terminals which require an internal timing source (i.e., 311-B Data Set Adapter).

CHARACTER AND STATUS GATES

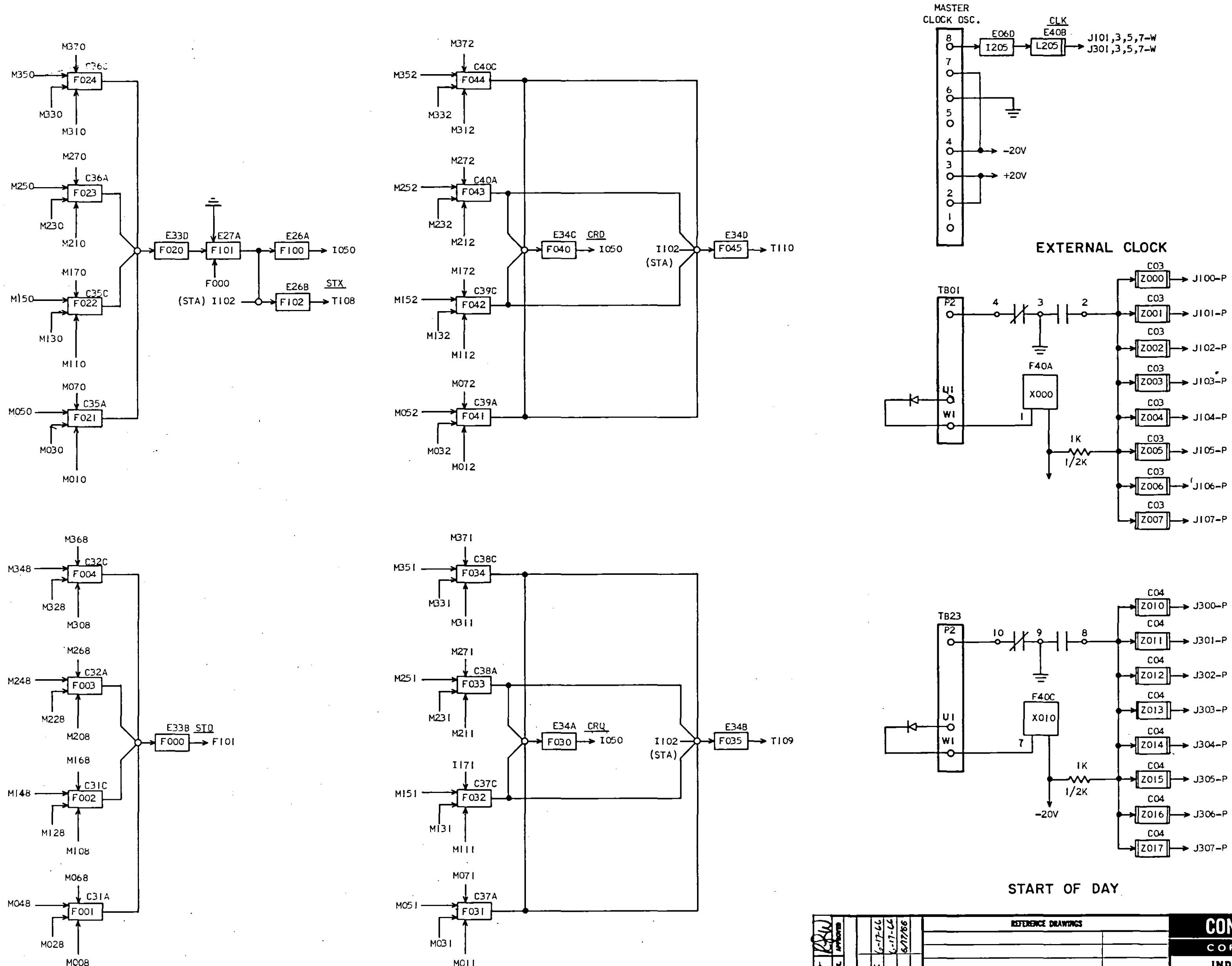
The Character and Status Gate inverters reflect the status of the data terminals. Inverters F041 through F044 receive as an input, the Character Ready signal from all the input data terminals. The outputs of these inverters condition AND gates to inverters F040 and F045. The presense of a Character Ready signal from an input data terminal produces a "0" at one of the four inverters (F041 through F044). This "0" disables the AND gate to F040 and F045, producing a "1" at the output. A "1" at F040 conditions an AND gate in the interrupt circuit (sheet 4) for use when an interrupt is desired only when a Character Ready signal is present. The output of F045 conditions the AND gate to status output card T110 (sheet 3). This enables a Character Ready status signal to be sent to the computer if an input is initiated.

The inverters for Status 1 (F021 through F024), Status 0 (F001 through F004), and Character Request (F031 through F034) operate in a similar manner to that described for Character Ready.

TERM	LOCATION	* PAGE	DEFINITION
M008	A08C	9	
M010	A13A	9	
M011	A17C	10	
M012	A10A	11	
M028	A13A	9	
M030	A13C	9	
M031	A14A	10	
M032	A14B	11	
M048	A17B	9	
M050	A18A	9	
M051	A18B	10	
M052	A18C	11	
M068	A21C	9	
M070	A22B	9	
M071	A22C	10	
M072	A23A	11	
M108	A30C	9	
M110	A35A	9	
M111	A27A	10	
M112	A27B	11	
M128	A30B	9	
M130	A31A	9	
M131	A31B	10	
M132	A31C	11	
M148	A34C	9	
M150	A35B	9	
M151	A35C	10	
M152	A36A	11	
M168	A39A	9	
M170	A39C	9	
M172	A39B	11	
M208	B08C	11	

* Page denotes sheet of logic diagram.

TERM	LOCATION	PAGE	DEFINITION
M210	B09B	11	
M211	B09C	12	
M212	B10A	11	
M228	B17C	11	
M230	B22A	11	
M231	B14A	12	
M232	B14B	11	
M248	B17B	11	
M250	B18A	11	
M251	B18B	12	
M252	B18C	11	
M268	B21C	11	
M270	B22B	11	
M271	B22C	12	
M272	B23A	11	
M308	B30C	11	
M310	B35A	11	
M311	B27A	12	
M312	B27B	11	
M328	B30B	11	
M330	B31A	11	
M331	B31B	12	
M332	B31C	11	
M348	B34C	11	
M350	B35B	11	
M351	B35C	12	
M352	B36A	11	
M368	B39A	11	
M370	B39C	11	
M371	B40A	12	
M372	B40B	11	
M171	B09A	10	



CHARACTER AND STATUS GATES

REV.	AUTH.	DATE	DWG. CHK.	APPROVED
A	DP 2133	6/21/66	JLW	

APPROVED: R. WALDACK 6-17-66
CHECKED: R. WALDACK 6-17-66
DRAWN: JERRY WEISS 6/17/66

REFERENCE DRAWINGS

COMPONENTS (UNLESS OTHERWISE INDICATED)

	TOLERANCE	VALUE	SIZE
RESISTORS			
CAPACITORS			

TITLE: STATUS, CONTROL, MASTER CLOCK, AND START-OF-DAY

CONTROL DATA CORPORATION
INDUSTRIAL DATA PROCESSING DIVISION
MINNEAPOLIS, MINNESOTA

PROJECT OR PRODUCT: 1749
DRAWING NUMBER: 36968300
REV. B
SHT 6
PAGE

DATA INPUT GATES

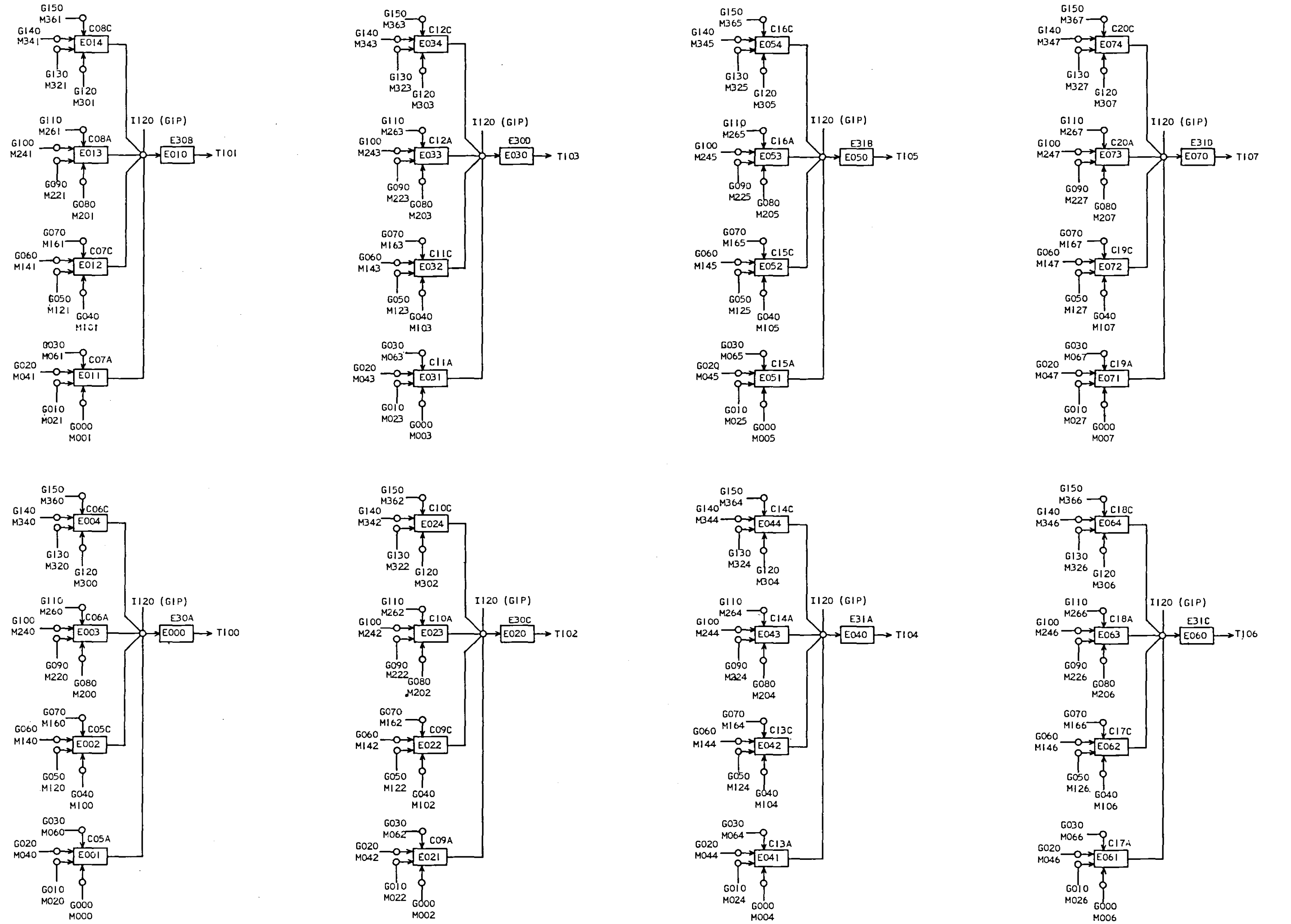
The Data Input inverters monitor the input data line interface for incoming data bits. For example, inverters E001 through E004 monitor the 16 input terminal channels for data bit 0. Each of these inverters has as input, four AND gates, with the data bit 0 and the Decode and Fan-Out inverter for that data terminal conditioning the AND gate. A "1" from the selected Decode and Fan-Out inverter and a data bit 0 from that channel enable the AND to that inverter producing a "0" at the output. The "0" output disables the AND gate to E000 and produces a "1" at the output. The output of E000 conditions the AND gate to data and status input card T100.

The inverters for the other data bits operate in the same manner according to the following relationships:

(1) E011 through E014 - Data bit 1
(2) E021 through E024 - Data bit 2
(3) E031 through E034 - Data bit 3
(4) E041 through E044 - Data bit 4
(5) E051 through E054 - Data bit 5
(6) E061 through E064 - Data bit 6
(7) E071 through E074 - Data bit 7

TERM	LOCATION	* PAGE	DEFINITION
G000	D01	5	Channel 00
G010	D03	5	Channel 01
G020	D05	5	Channel 02
G030	D07	5	Channel 03
G040	D09	5	Channel 04
G050	D11	5	Channel 05
G060	D13	5	Channel 06
G070	D15	5	Channel 7
G080	D25	5	Channel 8
G090	D27	5	Channel 9
G100	D29	5	Channel 10
G110	D31	5	Channel 11
G120	D33	5	Channel 12
G130	D35	5	Channel 13
G140	D37	5	Channel 14
G150	D39	5	Channel 15
G151	D40	5	Channel 15
I120	E29	4	GIP
M000 through M167 originate on sheet 9			
M200 through M367 originate on sheet 11			

* Page denotes sheet of logic diagram.



REV.	AUTH.	DATE	REG.	DRW.	CHK.	APPROVED
C	PP 2800	3/24/..		DEB		

REVISIONS

APPROVED: E WALDACK 6-17-66
CHECKED: E WALDACK 6-17-66
DRAWN: JERRY WEISS 6/17/66
DESIGNED:

REFERENCE DRAWINGS

COMPONENTS (UNLESS OTHERWISE INDICATED)

	TOLERANCE	VALUE	SIZE
RESISTORS			
CAPACITORS			

TITLE
DATA INPUT GATES

CONTROL DATA CORPORATION
INDUSTRIAL DATA PROCESSING DIVISION
MINNEAPOLIS, MINNESOTA

PROJECT OR PRODUCT: 1749
DRAWING NUMBER: 36968300
REV.: A
SHT: 7
PAGE: [redacted]

STATUS INPUT GATES

The Status Input inverters monitor the input and output data terminals for status signals. For example, inverters E081 through E084 monitor the 16 input data terminals for ST1 and ST0. Each of these inverters has four AND gates with the ST1 and ST0 input from the input data terminal and the Decode and Fan-Out inverter for that data terminal conditioning the AND gate. When the Decode and Fan-Out inverter for a selected input data terminal is a "1" and a ST1 or ST0 status bit is present from that input data terminal, the AND gate is enabled and the output of the inverter becomes a "0". The "0" output disables the AND gate to inverter E080 and produces a "1" at the output. The output of E080 is the set input to ST0 Status FF (K080/081), and an input to Status inverter E200. The NOT ST1 and ST0 inverter (E081 through E084) output is the clear input to ST0 Status FF (K080/081).

The inverters for the other status bits operate in the same manner with the following relationship:

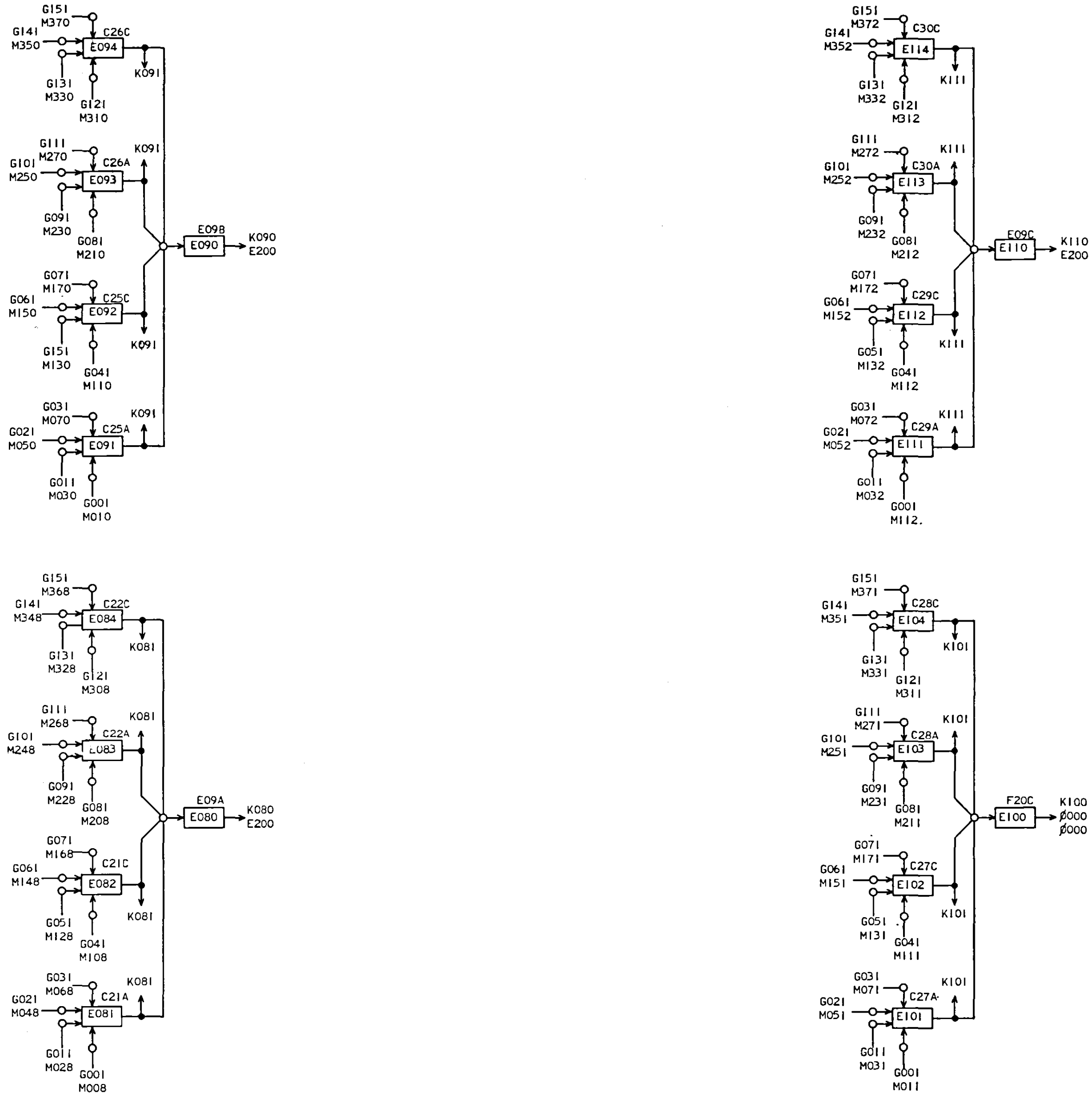
(1) E091 through E094 - Status 2

(2) E101 through E104 - Character Request

(3) E111 through E114 - Character Ready

TERM	LOCATION	PAGE*	DEFINITION
G001	D02	5	
G011	D04	5	
G021	D06	5	
G031	D08	5	
G041	D10	5	
G051	D12	5	
G061	D14	5	
G071	D16	5	
G081	D26	5	
G091	D28	5	
G101	D30	5	
G111	D32	5	
G121	D34	5	
G131	D36	5	
G141	D38	5	
G151	D40	5	
M008	A08C	9	
M010	A13A	9	
M011	A17C	10	
M028	A13A	9	
M030	A13C	9	
M031	A14A	10	
M032	A14B	9	
M048	A17B	9	
M050	A18A	9	
M051	A18B	10	
M052	A18C	9	
M068	A21C	9	
M070	A22B	9	
M071	A22C	10	
M072	A23A	9	
M108	A30C	9	
M110	A35A	9	
M111	A27A	10	
M112	A27B	9	
M128	A30B	9	
M130	A31A	9	
M131	A31B	10	
M132	A31C	9	
M148	A34C	9	
M150	A35B	9	
M151	A35C	10	
M152	A36A	9	
M168	A39A	9	
M170	A39C	9	
M171	B09A	10	
M172	A39B	9	
M208	B08C	11	
M210	B09B	11	
M211	B09C	12	
M212	B10A	11	
M228	B17C	11	
M230	B22A	11	
M231	B14A	12	
M232	B14B	11	
M248	B17B	11	
M250	B18A	11	
M251	B18B	12	
M252	B18C	11	
M268	B21C	11	
M270	B22B	11	
M271	B22C	12	
M272	B23A	11	
M308	B20C	11	
M310	B35A	11	
M311	B27A	12	
M312	B27B	11	
M328	B30B	11	
M330	B31A	11	
M331	B31B	12	
M332	B31C	11	
M348	B34C	11	
M350	B35B	11	
M351	B35C	12	
M352	B36A	11	
M368	B39A	11	
M370	B39C	11	
M371	B40A	12	
M372	B40B	11	

* Page denotes sheet of logic diagram.



NOTE:
Ø DENOTES ALPHABETICAL O.

REVISIONS — LTR. AUTH. DATE SEC. DEV. CHK. APPROVED

APPROVED: R. WALDALK 6-17-66
CHECKED: R. WALDALK 6-17-66
DRAWN: JERRY WEISS 6/17/66
DESIGNED:

REFERENCE DRAWINGS

COMPONENTS (UNLESS OTHERWISE INDICATED)	TOLERANCE	VALUE	SIZE
RESISTORS			
CAPACITORS			

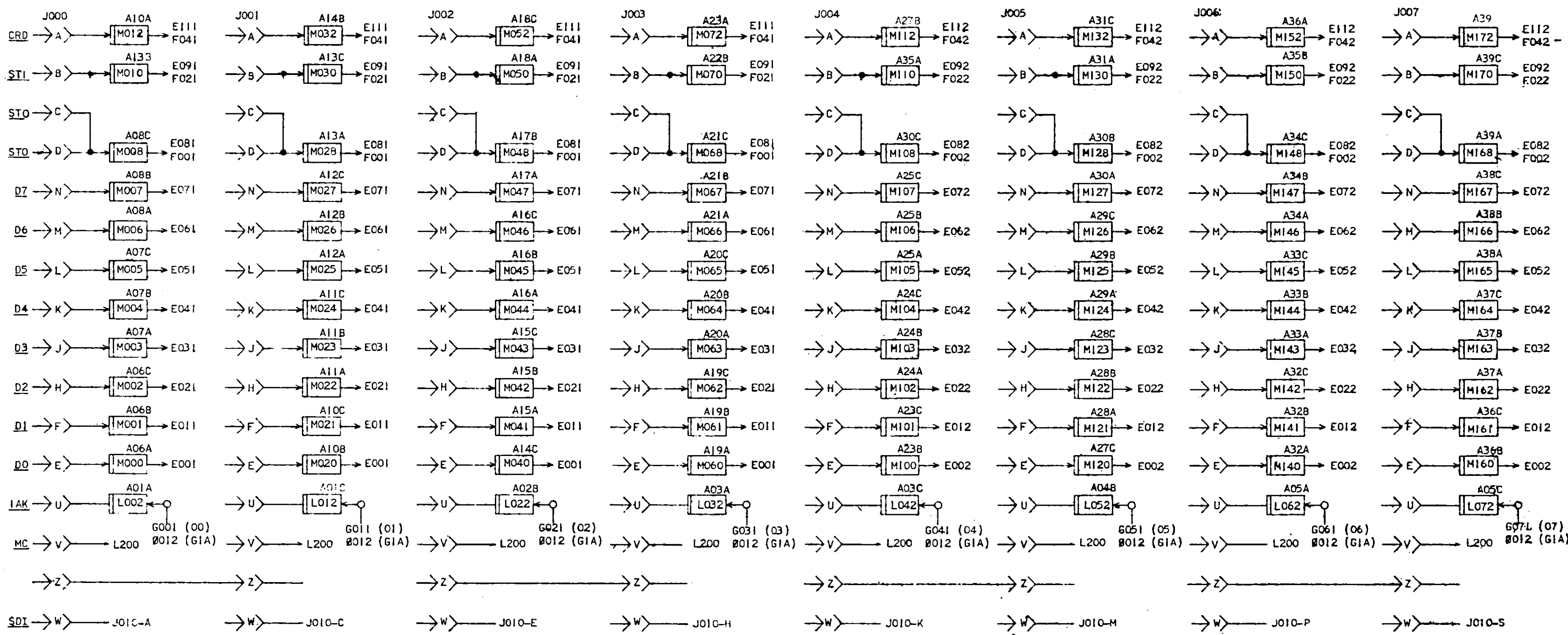
TITLE: STATUS INPUT GATES

CONTROL DATA CORPORATION
INDUSTRIAL DATA PROCESSING DIVISION
MINNEAPOLIS, MINNESOTA

PROJECT OR PRODUCT: 1749
DRAWING NUMBER: 36968300
REV.: H
SHT: 8
PAGE: [redacted]

TERM	LOCATION	*PAGE	DEFINITION
G001	D02	5	(00)
G011	D04	5	(01)
G021	D06	5	(02)
G031	D08	5	(03)
G041	D10	5	(04)
G051	D12	5	(05)
G061	D14	5	(06)
G071	D16	5	(07)
Ø012	E03	4	(G1A)
L200	C01C	2	

*Page denotes sheet of logic diagram.



INPUT

NOTE:

Ø DENOTES ALPHABETICAL O.

REFERENCE DRAWINGS	
COMPONENTS (UNLESS OTHERWISE INDICATED)	TOLERANCE / VALUE / SIZE
RESISTORS	
CAPACITORS	
DRAWN	JERRY WEISS 6/17/66
CHECKED	K. WALDACK
APPROVED	K. WALDACK
TITLE	INPUT DATA LINE INTERFACE

CONTROL DATA CORPORATION

INDUSTRIAL DATA PROCESSING DIVISION
MINNEAPOLIS, MINNESOTA

PROJECT OR PRODUCT: 1749

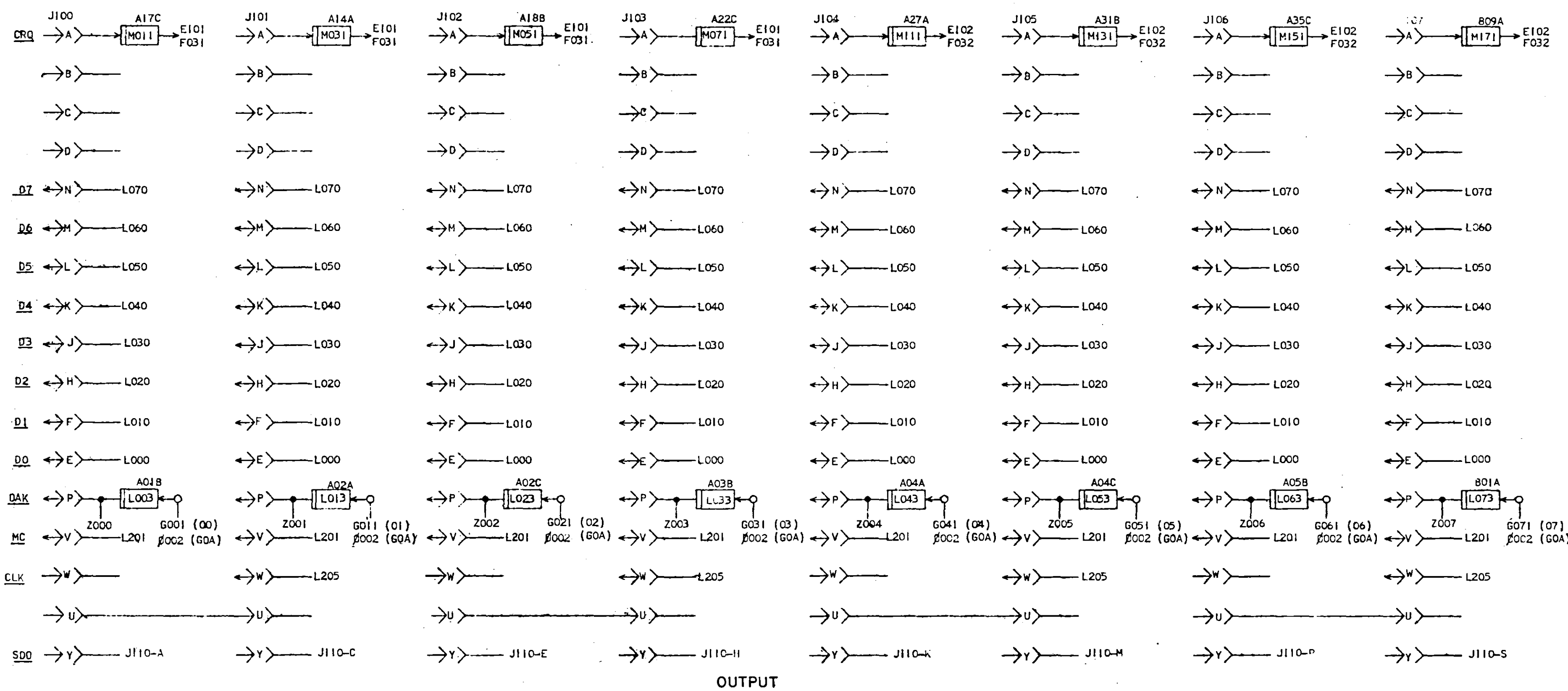
DRAWING NUMBER: 36968300

REV. H

9

PAGE [redacted]

TERM	LOCATION	* PAGE	DEFINITION
G001	D02	5	
G011	D04	5	
G021	D06	5	
G031	D08	5	
G041	D10	5	
G051	D12	5	
G061	D14	5	
G071	D16	5	
L000	E35A	3	Data bit 01
L010	E35C	3	Data bit 01
L020	E36B	3	Data bit 02
L030	E37A	3	Data bit 03
L040	E37C	3	Data bit 04
L050	E38B	3	Data bit 05
L060	E39A	3	Data bit 06
L070	E39C	3	Data bit 07
L201	C02A	6	CLK
Ø002	E01	4	GOA
Z000	C03	6	Start of day
Z001	C03	6	Start of day
Z002	C03	6	Start of day
Z003	C03	6	Start of day
Z004	C03	6	Start of day
Z005	C03	6	Start of day
Z006	C03	6	Start of day
Z007	C03	6	Start of day



REFERENCE DRAWINGS		
COMPONENTS (UNLESS OTHERWISE INDICATED)		
RESISTORS		
CAPACITORS		

APPROVED R. WALDAUF 6-17-66
CHECKED R. WALDAUF 6-17-66
DRAWN JERRY WEISS 6/17/66
DESIGNER

REV. B — 2141 — 4/66 — JLW — REVISIONS

TITLE: OUTPUT DATA LINE INTERFACE

CONTROL DATA CORPORATION
INDUSTRIAL DATA PROCESSING DIVISION
MINNEAPOLIS, MINNESOTA

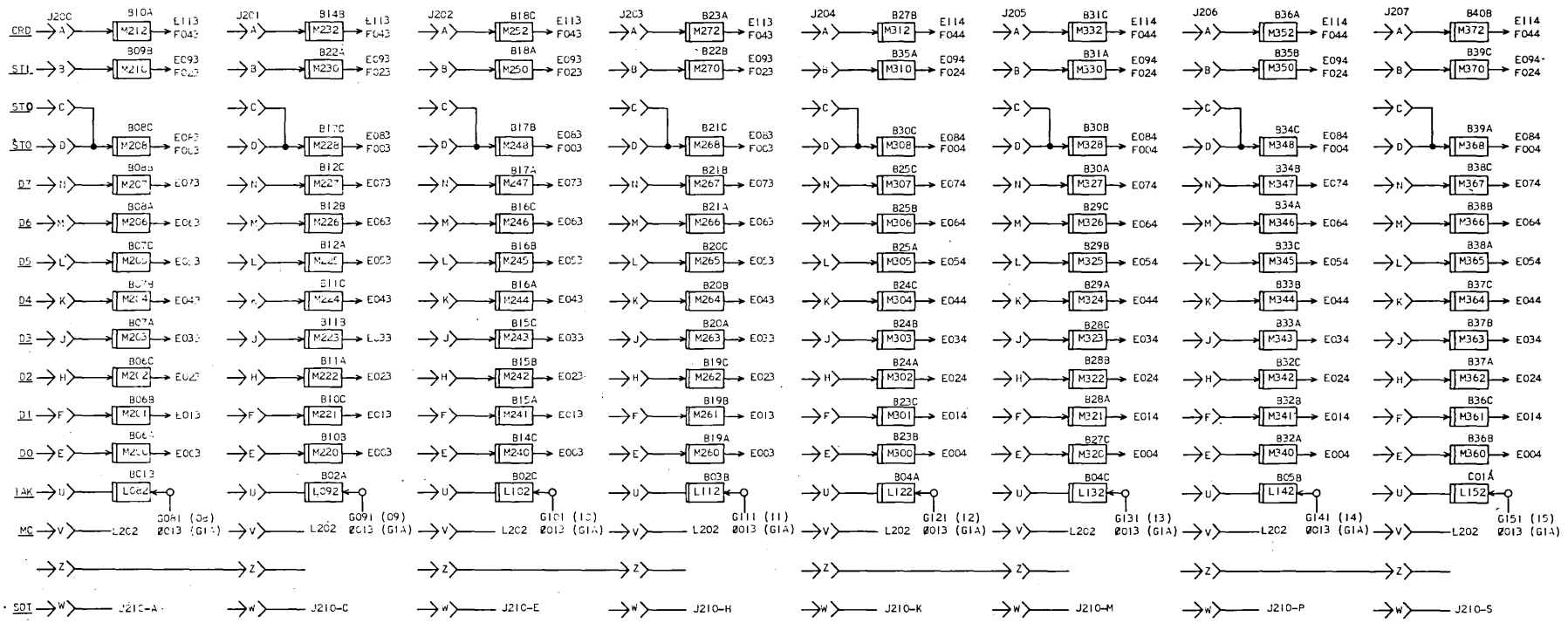
PROJECT OR PRODUCT: 1749

DRAWING NUMBER: 36968300 REV. H

SHT 10

TERM	LOCATION	*PAGE	DEFINITION
G081	D26	5	(08)
G091	D28	5	(09)
G101	D30	5	(10)
G111	D32	5	(11)
G121	D34	5	(12)
G131	D36	5	(13)
G141	D38	5	(14)
G151	D40	5	(15)
Ø013	E04	4	(G1A)
L202	C02B	2	

*Page denotes sheet of logic diagram.



INPUT

NOTE:

Ø DENOTES ALPHABETICAL O.

REV.	NOTE	DATE	REVISIONS	APPROVED
B	DP 2141	4/15/66		

APPROVED • R. WALDALE 6/17/66
CHECKED • K. WALDALE 6/17/66
DRAWN • JERRY WEISS 6/17/66
DESIGNED •

REFERENCE DRAWINGS

COMPONENTS (UNLESS OTHERWISE INDICATED)

	TOLERANCE	VALUE	SIZE
RESISTORS			
CAPACITORS			

TITLE

INPUT DATA LINE INTERFACE

CONTROL DATA CORPORATION
INDUSTRIAL DATA PROCESSING DIVISION
MINNEAPOLIS, MINNESOTA

PROJECT OR PRODUCT
1749

DRAWING NUMBER
36968300

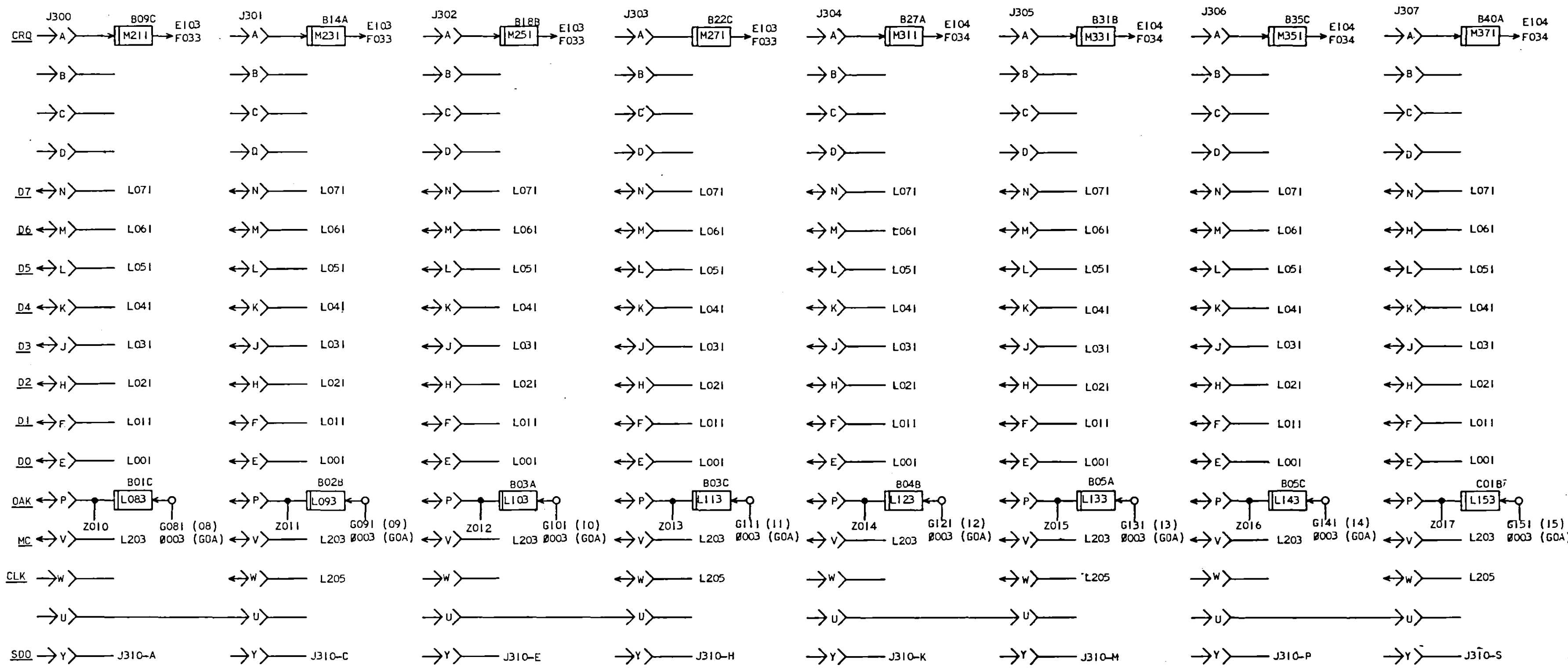
REV. H

SHT 11

PAGE

TERM	LOCATION	PAGE	DEFINITION
G081	D26	5	
G091	D28	5	
G101	D30	5	
G111	D32	5	
G121	D34	5	
G131	D36	5	
G141	D38	5	
G151	D40	5	
L001	E35B	3	Data bit 00
L011	E36A	3	Data bit 01
L021	F36C	3	Data bit 02
L031	E37B	3	Data bit 03
L041	E38A	3	Data bit 04
L051	E38C	3	Data bit 05
L061	E39B	3	Data bit 06
L071	E40A	3	Data bit 07
L205	E40B	6	CLK
Ø003	E02	4	GOA
Z010	C04	6	Start of day
Z011	C04	6	Start of day
Z012	C04	6	Start of day
Z013	C04	6	Start of day
Z014	C04	6	Start of day
Z015	C04	6	Start of day
Z016	C04	6	Start of day
Z017	C04	6	Start of day

* Page denotes sheet of logic diagram.



OUTPUT

NOTE:

Ø DENOTES ALPHABETICAL O.

REFERENCE DRAWINGS	
COMPONENTS (UNLESS OTHERWISE INDICATED)	TOLERANCE / VALUE / SIZE
RESISTORS	
CAPACITORS	
DESIGNED	JERRY WEISS 6/17/66
CHECKED	R. WALDACK 6-17-66
APPROVED	R. WALDACK 6-17-66
REV.	B

CONTROL DATA CORPORATION

INDUSTRIAL DATA PROCESSING DIVISION

MINNEAPOLIS, MINNESOTA

PROJECT OR PRODUCT: 1749

DRAWING NUMBER: 36968300 REV. H

TITLE: OUTPUT DATA LINE INTERFACE

SHEET 12

CARD PLACEMENT 1749

Row A

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
A	L 002	L 013	L 032	L 043	L 062	M 000	M 003	M 006		M 012	M 022	M 025	M 028	M 031	M 041	M 044	M 047	M 050	M 060	M 063
A	L 003	L 022	L 033	L 052	L 063	M 001	M 004	M 007		M 020	M 023	M 026	M 010	M 032	M 042	M 045	M 048	M 051	M 061	M 064
A	L 012	L 023	L 042	L 053	L 072	M 002	M 005	M 008		M 021	M 024	M 027	M 030	M 040	M 043	M 046	M 011	M 052	M 062	M 065
A	69	69	69	69	69	61	61	61		61	61	61	61	61	61	61	61	61	61	61

	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40
A	M 066		M 072	M 102	M 105		M 111	M 121	M 124	M 127	M 130	M 140	M 143	M 146	M 110	M 152	M 162	M 165	M 168	
A	M 067	M 070	M 100	M 103	M 106		M 112	M 122	M 125	M 128	M 131	M 141	M 144	M 147	M 150	M 160	M 163	M 166	M 172	
A	M 068	M 071	M 101	M 104	M 107		M 120	M 123	M 126	M 108	M 132	M 142	M 145	M 148	M 151	M 161	M 164	M 167	M 170	
A	61	61	61	61	61		61	61	61	61	61	61	61	61	61	61	61	61	61	

Row B

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
B	L 073	L 092	L 103	L 122	L 133	M 200	M 203	M 206	M 171	M 212	M 222	M 225		M 231	M 241	M 244	M 247	M 250	M 260	M 263
B	L 082	L 093	L 112	L 123	L 142	M 201	M 204	M 207	M 210	M 220	M 223	M 226		M 232	M 242	M 245	M 248	M 251	M 261	M 264
B	L 083	L 102	L 113	L 132	L 143	M 202	M 205	M 208	M 211	M 221	M 224	M 227		M 240	M 243	M 246	M 228	M 252	M 262	M 265
B	69	69	69	69	69	61	61	61	61	61	61	61		61	61	61	61	61	61	61

	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40
B	M 266	M 230	M 272	M 302	M 305		M 311	M 321	M 324	M 327	M 330	M 340	M 343	M 346	M 310	M 352	M 362	M 365	M 368	M 371
B	M 267	M 270	M 300	M 303	M 306		M 312	M 322	M 325	M 328	M 331	M 341	M 344	M 347	M 350	M 360	M 363	M 366		M 372
B	M 268	M 271	M 301	M 304	M 307		M 320	M 323	M 326	M 308	M 332	M 342	M 345	M 348	M 351	M 361	M 364	M 367	M 370	M 400
B	61	61	61	61	61		61	61	61	61	61	61	61	61	61	61	61	61	61	61

Row C

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
C	L 152 L 153	L 201 L 202	Z000 Z001 Z002 Z003	Z010 Z011 Z012 Z013	E 001	E 003	E 011	E 013	E 021	E 023	E 031	E 033	E 041	E 043	E 051	E 053	E 061	E 063	E 071	E 073
C	L 200	L 203	Z004 Z005 Z006 Z007	Z014 Z015 Z016 Z017	E 002	E 004	E 012	E 014	E 022	E 024	E 032	E 034	E 042	E 044	E 052	E 054	E 062	E 064	E 072	E 074
C	69	69	82–9	82–9	24	24	24	24	24	24	24	24	24	24	24	24	24	24	24	24

	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40
C	E 081	E 083	K 080 K 081		E 091	E 093	E 101	E 103	E 111	E 113	F 001	F 003	Y035		F 021	F 023	F 031	F 033	F 041	F 043
C	E 082	E 084	K 090 K 091		E 092	E 094	E 102	E 104	E 112	E 114	F 002	F 004	Y035 Y035 Y035 Y222		F 022	F 024	F 032	F 034	F 042	F 044
C	24	24	30		24	24	24	24	24	24	24	24	82–7		24	24	24	24	24	24

Row D

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
D	G 000	G 001	G 010	G 011	G 020	G 021	G 030	G 031	G 040	G 041	G 050	G 051	G 060	G 061	G 070	G 071	D 000	D 001	D 002	D 003
D	12	12	12	12	12	12	12	12	12	12	12	12	12	12	12	12	11	11	11	11

	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40
D	D 010	D 011	D 012	D 013	G 080	G 081	G 090	G 091	G 100	G 101	G 110	G 111	G 120	G 121	G 130	G 131	G 140	G 141	G 150	G 151
D	11	11	11	11	12	12	12	12	12	12	12	12	12	12	12	12	12	12	12	12

REV. | AUTH. | DATE | REQ. | DRN. | CHK. | APPROVED — REVISIONS

APPROVED: K. WALDACK 6-17-66
CHECKED: E. WALDACK 6-17-66
DRAWN: JERRY WEISS 6/17/66
DESIGNED

REFERENCE DRAWINGS

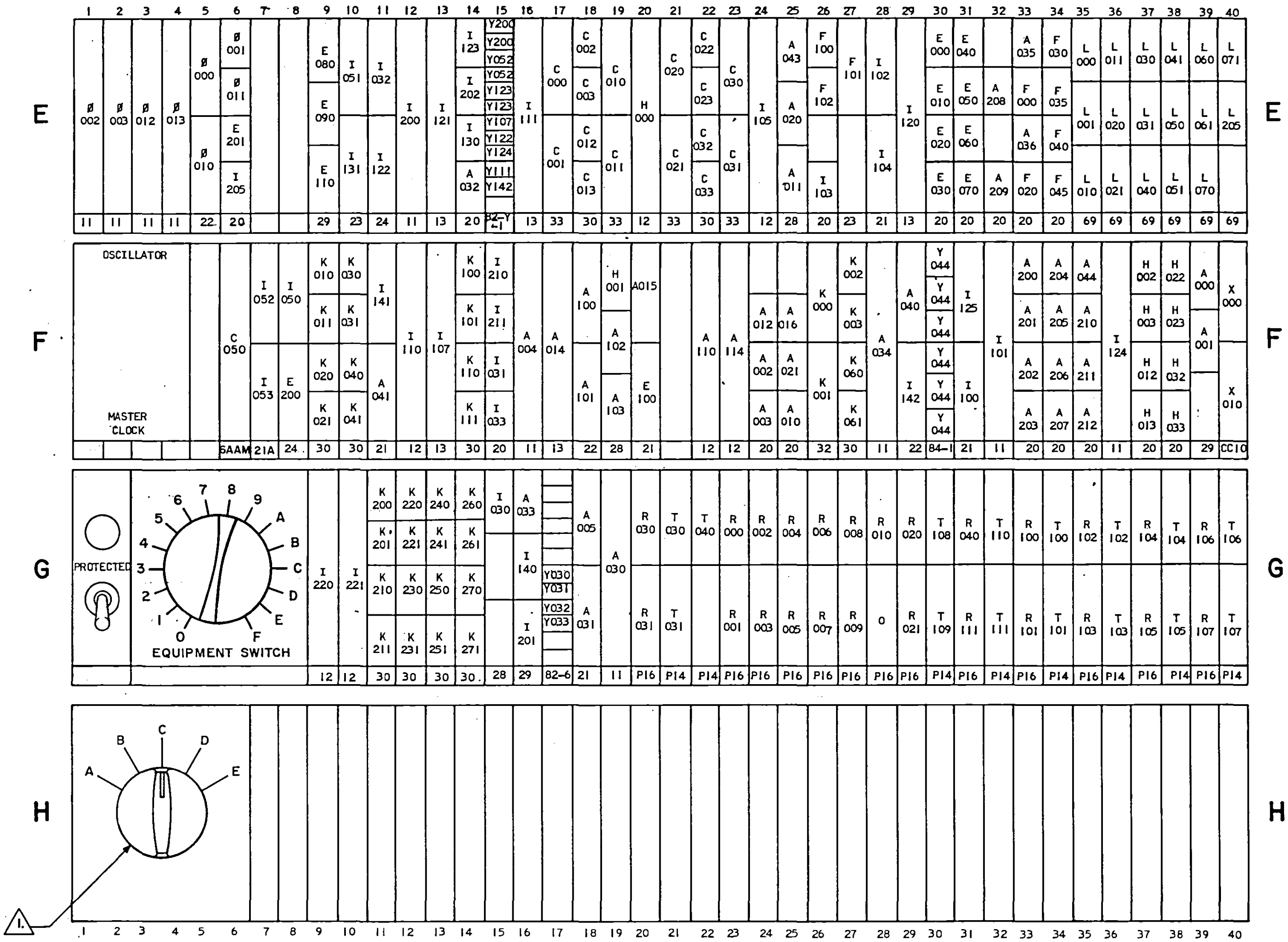
COMPONENTS (UNLESS OTHERWISE INDICATED) — TOLERANCE | VALUE | SIZE
RESISTORS
CAPACITORS

TITLE: CARD PLACEMENT DIAGRAM (A—D)

CONTROL DATA CORPORATION
INDUSTRIAL DATA PROCESSING DIVISION
MINNEAPOLIS, MINNESOTA

PROJECT OR PRODUCT: 1749
DRAWING NUMBER: 36968300
REV.: H
SHT: 13
PAGE

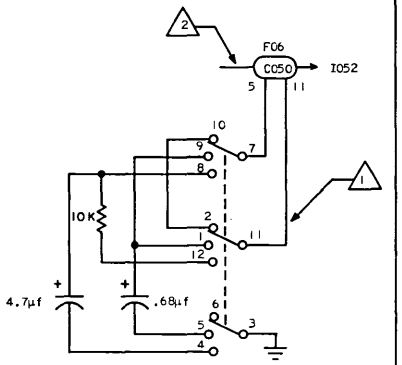
CARD PLACEMENT 1749



NOTES:

1. UNITS WITH SERIAL NO. BELOW 179 HAVE A THREE POSITION SWITCH WITH TTY, VOICE BAND, AND WIDE BAND POSITIONS.

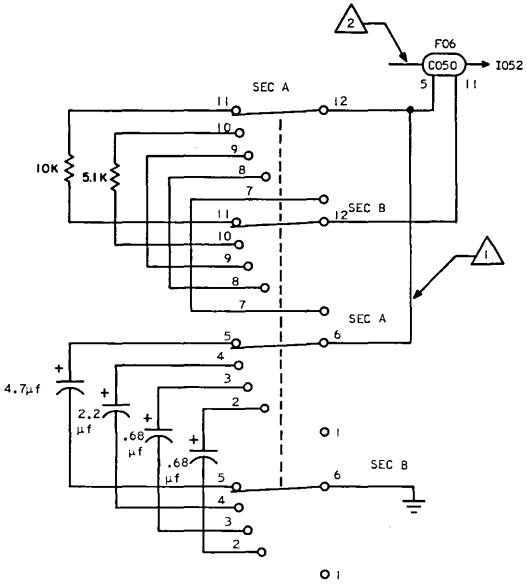
CONTROL DATA	INDUSTRIAL DATA PROCESSING DIVISION, MINNEAPOLIS, MINNESOTA
TITLE	CARD PLACEMENT DIAGRAM (E—H)
PROJECT OR PRODUCT	1749
DRAWING NUMBER	36968300
REV.	H
SET	14
PAGE	1-29
DRAWN	JERRY WEISS 6/17/66
CHECKED	R. WALDACK 6/17/66
APPROVED	R. WALDACK 6/17/66



INTERRUPT SPEED SELECT SWITCH
SERIAL NO. 101 THRU 178

RANGES

TTY	=	60 MS TO 137 MS
VOICE BAND	=	2.5 MS TO 18 MS
WIDE BAND	=	50μS TO 275μS



RANGES

A = 60 MS TO 137 MS
B = 18 MS TO 60 MS
C = 2.5 MS TO 18 MS
D = 325 μS TO 2 MS
E = 50 μS TO 275 MS

INTERRUPT SPEED SELECT SWITCH
SERIAL NO. 179 AND UP

NOTES:

1. TO CHANGE INTERRUPT PERIODS SELECT ONE OF THE ABOVE RANGES PER SERIAL NO. THEN ADJUST C50 TO THE DESIRED TIME.
2. INPUT PIN 1 OF LOGIC ELEMENT C050 IS LEFT OPEN. THIS EXHIBITS A CONSTANT LOGIC LEVEL "1" ON THE INPUT WHICH INTURN CAUSES THE UNIJUNCTION DELAY TO PULSE FREELY.

REV. AUTH. | DATE | REVISIONS | REL. DRW. | CHK. | APPROVED

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CHECKED
DRAWN T. Scully 4-29-69
DESIGNED

REFERENCE DRAWINGS

COMPONENTS (UNLESS OTHERWISE INDICATED)

	TOLERANCE	VALUE	SIZE
RESISTORS			
CAPACITORS			

TITLE
INTERRUPT OSC.

CONTROL DATA
CORPORATION
INDUSTRIAL DATA PROCESSING DIVISION
MINNEAPOLIS, MINNESOTA

PROJECT OR PRODUCT
1749

DRAWING NUMBER
36968300

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SHT
15 OF 15

PAGE

SECTION II
INSTALLATION AND MAINTENANCE

INSTALLATION

POWER REQUIREMENTS

The 1749-A CTC operates on 120 +10 -20 vac, 60 ± 0.3 Hertz, 22.6 ampere maximum, single-phase power. The 1749-B CTC operates on 220 +15 -33 vac (or 240 +16 -36 vac), 50 ± 0.25 Hertz, 14.8 ampere maximum, single-phase power; the blower requires 120-volt, 50 Hertz, single-phase power, and must be controlled by the site. The power from an external power source is supplied to the 1749 CTC via J50 on the power supply terminal plate assembly. The 40 vdc terminator power is supplied to TB47 from the 1700 Computer.

SYSTEM INTERCONNECTION

The 1749 CTC interconnects with other system components through input and output cables. The cables plug into connectors on the connector panel assembly (figure 2-1). The 1749 CTC interfaces the computer via a 61-pin data and status connector (J4A2 or J4A3) and a 61-pin select code and control signal connector (J4B2 or J4B3). Connectors J010, J110, J210, and J310 connect the 1749 CTC to a test board unit, required when operating with some data terminals. Connector J410 connects the interrupt line from the 1749 CTC to the computer. Terminal board TB47 connects the 1749 CTC to an external 40-vdc terminator power supply. A cable harness jack assembly is required with those data terminals not requiring the use of a test board unit. This assembly is mounted in the 1749 CTC and provides the interface to the communication lines.

The 1749 CTC connects to the data terminals via 22-pin connectors at the back of the data terminal mounting sections.

PIN ASSIGNMENTS

Tables 2-1 through 2-5 list the pin assignments for the connectors interfacing the computer, data terminals, and power supply.

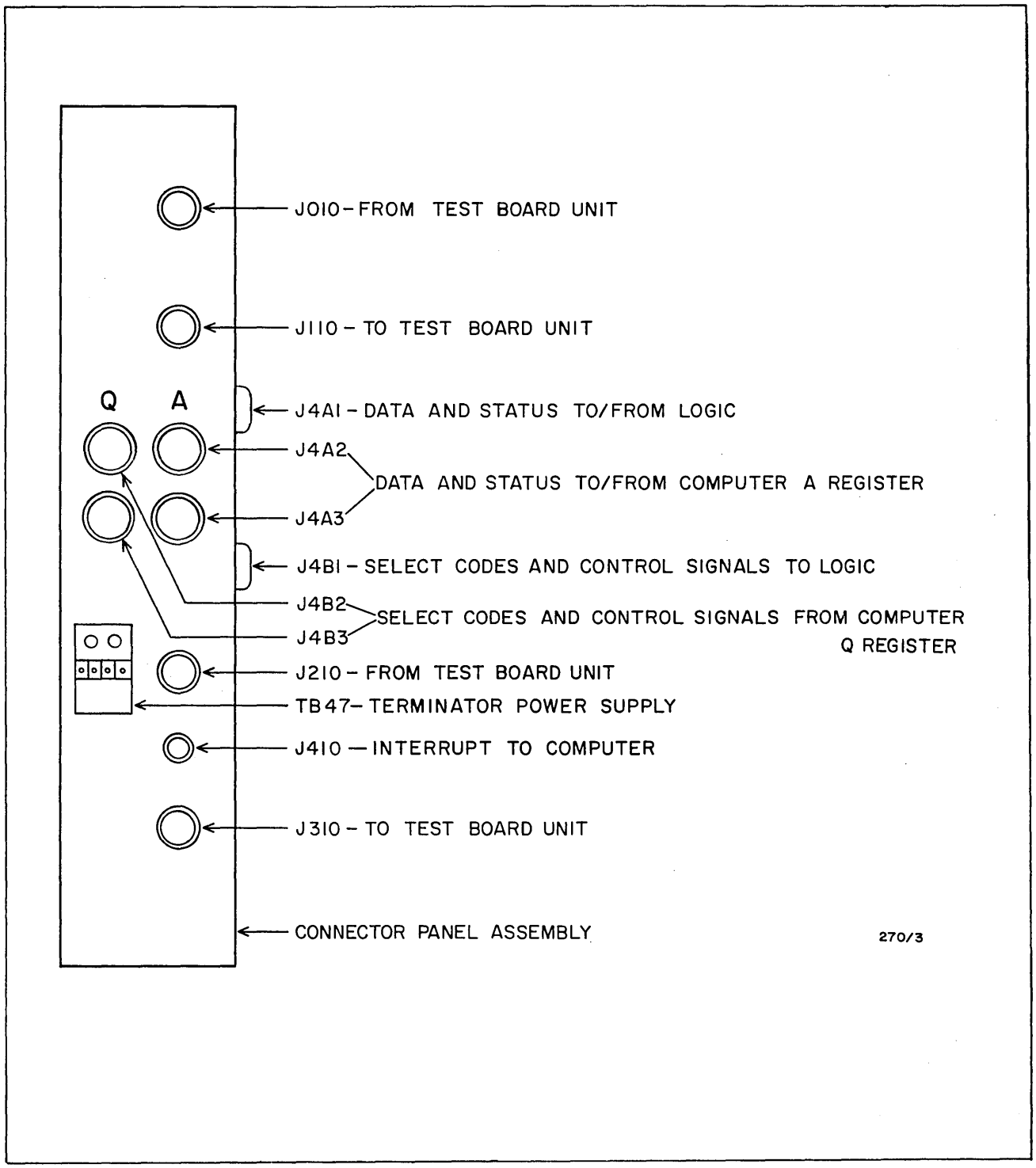

Figure 2-1. 1749 CTC - Interconnecting Cabling Jacks

MAINTENANCE

GENERAL

The 1749 CTC does not require any periodic or preventive maintenance other than weekly removing and washing of the filter for the ventilating fan. The filter is removed by rotating the tabs on the bottom of the filter screen panel clockwise and pushing down and out on the panel. Wash the filter thoroughly in plain water, then dry. Restore the filter's dirt collecting capability by spray coating both sides of the filter using filter fluid aerosol P/N 12210958.

POWER VERIFICATION

Test points are available on the front panel for verifying the + and - 20-vdc power.

INTERRUPT CLOCK ADJUSTMENT

The 1749 CTC interrupt clock cycle is determined by two factors. First, the general rate is selected by a rotary speed select switch (three- or five-position, depending on the serial number of the CTC) located on row "H" of the swing-out chassis in the rear of the CTC. After selection has been made, fine adjustments for more precise rates are made by adjusting the unijunctional delay C050.

To adjust C050 for a given rate, set the oscilloscope TRIGGER switches to external negative, and connect the TRIGGER INPUT and one input probe to C050 (F06), test point "A". Synchronize and set up the oscilloscope so that the cycle duration of C050 can be adjusted to a rate that is slightly less than the minimum character interval.

TABLE 2-1. COMPUTER DATA AND STATUS INTERFACE PIN ASSIGNMENTS

PIN	CONNECTORS J4A1, J4A2, AND J4A3
A1, A2	Data bit 0 and counter bit 0
A3, A4	Data bit 1 and counter bit 1
A5, A6	Data bit 2 and counter bit 2
A7, A8	Data bit 3 and counter bit 3
A9, A10	Data bit 4 and Interrupt on Interrupt Clock
B1, B2	Data bit 5 and Interrupt on Character Ready
B3, B4	Data bit 6 and Interrupt on Character Request
B5, B6	Data bit 7 and Interrupt on Fault
B7, B8	Data bit 8 and Status 0
B9, B10	Data bit 9 and Status 1
C1, C2	Character Request
C3, C4	Activity bit and Character Ready
C5, C6	Not used
C7, C8	Not used
C9, C10	Not used
D1, D2	Not used
D3, D4	Reply
D5, D6	Reject
D7, D8	*Interrupt
D9, D10	Not used
E1, E2	Not used
E3, E4	Not used
E5, E6	Not used
E7, E8	Not used
E9, E10	Not used
F1, F2	Not used
F3, F4	Not used
F5, F6	Not used
F7, F8	Not used
F9, F10	Termination power

*This signal does not appear in the computer logic cables but is jumpered to the interrupt connector (J410).

TABLE 2-2. COMPUTER SELECT CODES AND CONTROL SIGNAL INTERFACE

PIN	CONNECTORS J4B1, J4B2, AND J4B3
A1, A2	Address bit 00
A3, A4	Address bit 01
A5, A6	Address bit 02
A7, A8	Address bit 03
A9, A10	Address bit 04
B1, B2	Address bit 05
B3, B4	Address bit 06
B5, B6	Address bit 07
B7, B8	Address bit 08
B9, B10	Address bit 09
C1, C2	Address bit 10
C3, C4	Not used
C5, C6	Not used
C7, C8	Not used
C9, C10	Not used
D1, D2	Not used
D3, D4	Read
D5, D6	Write
D7, D8	Master Clear
D9, D10	Program Protect
E1, E2	Not used
E3, E4	Not used
E5, E6	Not used
E7, E8	W = 0
E9, E10	Not used
F1, F2	Not used
F3, F4	Not used
F5, F6	Not used
F7, F8	Not used
F9, F10	Termination power

TABLE 2-3. TEST BOARD UNIT INTERFACE PIN ASSIGNMENTS

PIN	FUNCTION		
	RECEIVE CONNECTORS	* J010	* J210
A	Serial data input	0	10
B	Serial data return		
C	Serial data input	1	11
D	Serial data return		
E	Serial data input	2	12
F	Serial data return		
H	Serial data input	3	13
J	Serial data return		
K	Serial data input	4	14
L	Serial data return		
M	Serial data input	5	15
N	Serial data return		
P	Serial data input	6	16
R	Serial data return		
S	Serial data input	7	17
T	Serial data return		
U	Not used		
V	Not used		
W	Not used		
Y	Not used		
Z	Not used		
a	Start-of-day input		
b	Chassis ground		

* = Numbers in this column refer to channels.

TABLE 2-3. TEST BOARD UNIT INTERFACE PIN ASSIGNMENTS (CONT)

PIN	FUNCTION		
	SEND CONNECTORS	* J110	* J310
A	Serial data out	0	10
B	Ground		
C	Serial data out	1	11
D	Ground		
E	Serial data out	2	12
F	Ground		
H	Serial data out	3	13
J	Ground		
K	Serial data out	4	14
L	Ground		
M	Serial data out	5	15
N	Ground		
P	Serial data out	6	16
R	Ground		
S	Serial data out	7	17
T	Ground		
U	Not used		
V	Not used		
W	Not used		
X	Not used		
Y	Not used		
Z	Not used		
a	Start-of-day input		
b	Chassis ground		

* = Numbers in this column refer to channels.

TABLE 2-4. TERMINAL UNIT INTERFACE PIN ASSIGNMENT

PIN	FUNCTION	
	CONNECTORS J000 THRU J007, J200 THRU J207	CONNECTORS J100 THRU J107, J300 THRU J307
A	Character ready	Character request
B	Status 1	Not used
C	Status 0	Not used
D	Status 0	Not used
E	Data bit 0	Data bit 0
F	Data bit 1	Data bit 1
H	Data bit 2	Data bit 2
J	Data bit 3	Data bit 3
K	Data bit 4	Data bit 4
L	Data bit 5	Data bit 5
M	Data bit 6	Data bit 6
N	Data bit 7	Data bit 7
P	Not used	Output acknowledge
R	+20 vdc	+20 vdc
S	Ground	Ground
T	-20 vdc	-20 vdc
U	Input acknowledge	*Serial data output jumper
V	Master clear	Master clear
W	Serial data input	Master clock (odd numbered jacks only)
X	Not used	Not used
Y	Not used	Serial data output
Z	*Serial data input jumper	Not used

* These jumpers are utilized only for operation with data set adapters.

TABLE 2-5, POWER SUPPLY INTERFACE PIN ASSIGNMENTS

PIN	FUNCTION
J51 (power supply A)	
A	+20-vdc to pans A and B
B	120-vac input
C	dc power ground
D	120-vac return
E	-20-vdc to pans A and B
F	120-vac output to fan
G	ac power ground
J52 (power supply B)	
A	+20-vdc to pans C, D, and E
B	120-vac input
C	dc power ground
D	120-vac return
E	-20-vdc to pans C, D, and E
F	120-vac output to fan
G	ac power ground
J50 (primary power)	
Y	120-vac input
X	120-vac return
W	ac power ground

APPENDIX A
PARTS LIST

1749 CTC

PART NO.	DESCRIPTION	UNITS PER ASSEMBLY
36961100/01	1749 CTC Final Assembly	
36104401	Gasket, sponge rubber	A/R
36085001	Filter, air	1
36446900	Clamp, cable	2
36440802	Plug, cable	14
8275-1	Latch, magnetic	2
47055900	Power Supply, 60 Hertz	1
47055901	Power Supply, 50 Hertz	1
245135	Fuse Holder	10
245129-1	Fuse, fast action, 2 amp, 250v	4
245129-24	Fuse, fast action, 3 amp, 250v	1
245129-30	Fuse, fast action, 10 amp, 250v	5
36149500	Chain, bend	2
36129400	Diode, silicon	2
23468001	Hook, chain	2
31000400	Cable Assy, special purpose	A/R
18201900	Cable Assy, 3-pin	A/R
245005-12	Cable, power, electrical	A/R
36439100	Grill Assy, front	1
36439300	Latch, swing	1
36441300	Blower Assy	1
36441200	Blower, modified	1
36962700	Jack Panel Assy, receive A and B	
36115001	Connector, 22-pin	8
36109400	Clamp, cable	2
36963500	Jack Panel Assy, send A and B	
36115001	Connector, 22-pin	8
36109400	Clamp, cable	2
36960800	Connector Panel Assy	
36960400	Bracket, input connector	1
36953500	Bracket, 61-pin connector	1
245120-1	Connector Receptacle, 24-pin socket	4
245267	Terminal Block	6
36961601	Cable Assy, 1749 (J4A2)	1

PART NO.	DESCRIPTION	UNITS PER ASSEMBLY
36961602	Cable Assy, 1749 (J4A3)	1
36961603	Cable Assy, 1749 (J4B1)	1
36961604	Cable Assy, 1749 (J4B2)	1
36961605	Cable Assy, 1749 (J4B3)	1
17896900	Connector Receptacle, 3-pin socket	1
245135	Fuse Holder	2
245129-20	Fuse, 1 amp, 250v	2
24501502	Strip, terminal	1
245282-5	Strip, terminal	1
36964500	Power Supply Terminal Plate Assy (60 Hz)	
36445900	Bracket, connector	1
24556501	Connector, plug, electrical	1
36086100	Connector, receptacle	2
245012-13	Strip, terminal	1
36144300	Filter, RFI	2
36969200	Chassis Assy	
36959100	Bracket, oscillator	1
24547900	Socket, tube	1
245181-1	Connector, flexible, conduit	1
24518105	Connector, flexible, conduit	8
36138300	Connector, 30 contact	134
245159	Switch, toggle, SPDT	1
360807-03	Indicator Light	1
245282-12	Strip, terminal	1
36962500	Cable Assy	1
36962600	Cable Assy	1
36150000	Switch, rotary, 16-position	1
36124100	Knob, rotary switch	1
	Logic Card Assemblies	
10201801	Card Assy, Type 11A	18
10201901	Card Assy, Type 12A	39
10202000	Card Assy, Type 13A	5
10232201	Card Assy, Type 20A	16
10202801	Card Assy, Type 21A	6
10203401	Card Assy, Type 22A	3
10203501	Card Assy, Type 23A	2
10203601	Card Assy, Type 24A	34
10232501	Card Assy, Type 28A	3
10232801	Card Assy, Type 29A	3
10334401	Card Assy, Type 30A	11
10203801	Card Assy, Type 32A	1
10203901	Card Assy, Type 33A	4
10206001	Card Assy, Type 61	65

1749 CTC (CONT)

PART NO.	DESCRIPTION	UNITS PER ASSEMBLY
10212101	Card Assy, Type 69	18
17683900	Card Assy, Type P14	8
17684500	Card Assy, Type P16	13
65172100	Card Assy, Type CC10	1
65128600	Card Assy, Type CC82-6	1
65128800	Card Assy, Type CC82-9	2
13770000	Card Assy, Type 6AAM	1
65196400	Card Assy, Type 84-1	2
	Card Assy, Type 82-Y-1	1
65129000	Card Assy, Type CC82-7	1
13646500	Power Supply Terminal Plate Assy (50 Hz)	1
36445900	Bracket, connector	1
17634301	Connector, plug, cable	1
36086100	Connector, receptacle	2
36144300	Filter, RFI	2
94030023	Fuse, 3 amp, blower	1
94029002	Fuseholder, blower	1
24501215	Strip, terminal (TB50, TB51)	2
94031000	Retaining clip, fuseholder	1

COMMENT SHEET

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Customer Engineering Manual

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