SERIES E2000 STRIPED LEDGER

DIRECT ACCOUNTING COMPUTER

Burroughs

FIELD ENGINEERING

INSTRUCTION BOOK

PROPERTY OF AND TO BE RETURNED TO

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Form 3738

SERIES E2150 INSTRUCTION BOOK

The E2150 series of machines is the E2100 series with the added ability to store data on stripes of magnetic ink on the back of the forms. Data stored in the stripes can be read and stored in memory. This data can be used during arithmetic operations. If the machine is constructed with the Type To and From Memory feature, the data can be used to control the typewriter.

STRIPED LEDGER CARD

There are three stripes approximately 3/8" apart on the back of each form. The center stripe is located 2" from the right edge of the form. The stripe nearest the edge of the form is the line find stripe. When encoded, this stripe contains the data necessary to cause the form to be stopped at the printing line. The center stripe is the X stripe and the stripe furtherest from the edge is the Y stripe.

WORD STORAGE IN THE STRIPES

In a Single Stripe (SS) machine, a maximum of ten, twelve-digit words of data with signs and parity, can be stored in the X stripe. A SYNC pulse is also stored in the X stripe and is located approximately 3/4" above the data. The purpose of this pulse is to cause a reversal of the direction of form travel on the READ LEDGER (RL) and WRITE LEDGER (WL) operations. The Y stripe is not used on a SS machine.

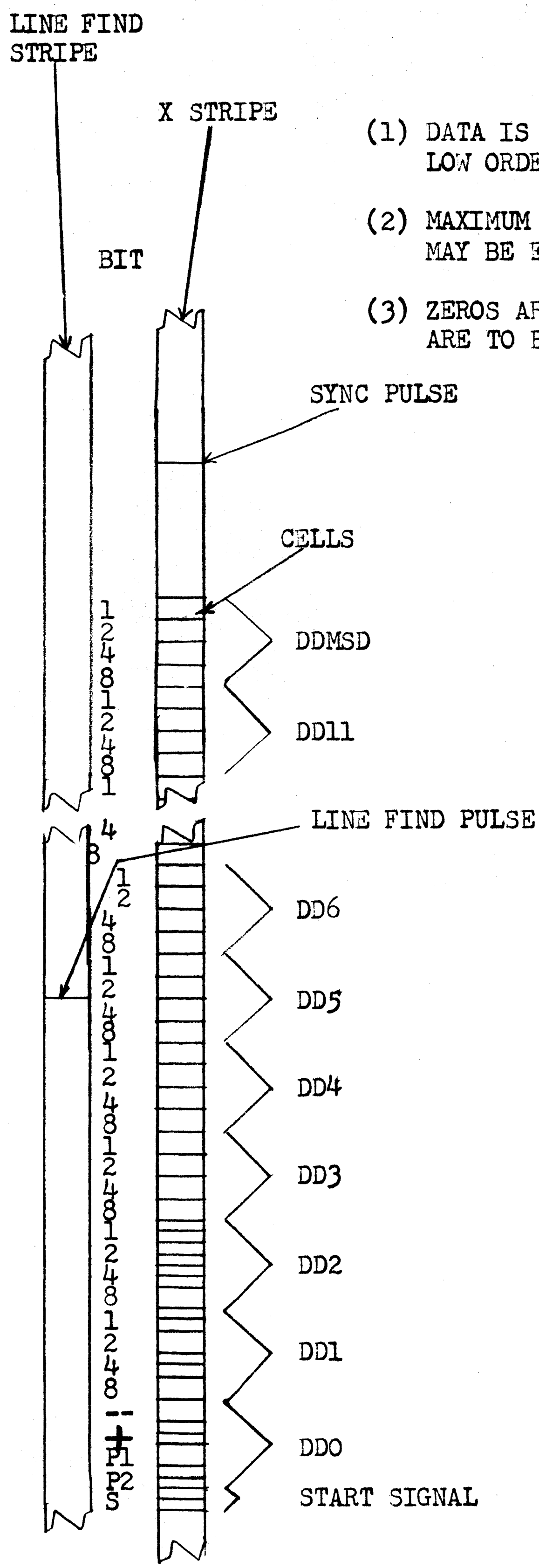
In a Dual Stripe (DS) machine, a maximum of ten, twelve-digit words of data with signs and parity can be stored in each of the X and Y stripes or a total of twenty words can be stored. If the DS machine is constructed with the Type To and From Memory feature, the X and Y stripes are used together to store the seven bits of the alpha code. A maximum of 120 alpha characters can be stored on the stripes.

Any number of words (10 or less) can be stored on the stripes. This is controlled by programming. The units of the highest memory address to be written on the stripes must be pinned in the WL position. Data stored in the stripes is always read from the 20-29 (SS) word group or 20-29 and 30-39 (DS) in the memory during the WL operation and written into this same word group during a RL operation. If 6 words are to be written on a SS machine, the data will be written from 25 down thru 20. This would require programming the memory address units 5 in the WL position. On a DS, the same could be done, however, locations 35 down thru 30 would be written on the Y stripe and not available for other operations. Another method would be to write 22 thru 20 on the X stripe and 32 thru 30 on the Y stripe. In this way 23 thru 29 and 33 thru 39 are available for other use.

ENCODING THE STRIPES

Data is written onto the stripe in a combination of data and complement pulses. Each pulse consist of a single reversal of the direction of magnetism of the stripe. This reversal of magnetic polarity is produced by a reversal of current through the head winding during the write operation. The complement pulses are written at regular evenly spaced intervals on the stripe and divide the stripe into cells. There are 90 cells per inch on the stripe. The data pulse consists of a reversal of magnetic polarity between the complement pulses. If no data is to be written (zero, or the bit positions not encoded), there is no reversal of polarity between complement pulses. Since the complements pulses are evenly spaced, they provide a means of timing for the read or write cycle and ensure that the data bits are given proper value. That is, a four bit is recognized as a four bit and is stored as such in the machine.

With ninety complement pulses or cells to the inch, the writing rate when data is being written is 180 bits per inch. This is a pulse approximately every .0056 inch. Four cells are required to record each digit (1, 2, 4 and 8 bits).



(1) DATA IS WRITTEN --HIGH ORDER WORD, HIGH ORDER DIGIT, LOW ORDER BIT

(2) MAXIMUM OF TEN TWELVE-DIGIT WORDS PLUS SIGN MAY BE ENCODED PER STRIPE

(3) ZEROS ARE WRITTEN WHERE NO SIGNIFICANT DIGITS ARE TO BE ENCODED

(4) PARITY CHECK IS FOR THE ENTIRE WORD

(5) SIGNS ARE ALWAYS WRITTEN IN DDO
A 1 BIT = MINUS
A 2 BIT = PLUS

(6) THE STRIPE AT LEFT SHOWS 75+ ENCODED IN THE X STRIPE WITH A SYNC PULSE ABOVE THE DATA.

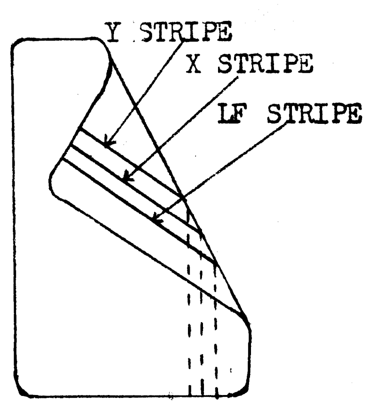


Figure I-1

The total number of bits for ten words (12 digits and sign) is 4 x 13 x 10 or 520 cells. At 90 cells per inch, this will extend approximately 5.8" on the stripe. With fewer words written, the distance encoded on the stripe will be correspondingly reduced.

WRITE DATA

When data is to be written on the stripe, the selected memory address and the DDREVFF select the MSD of the highest memory location to be written. Data is written from MSD downward toward DDO as the form is fed out of the machine. Zeros (no data pulses) are written in all digit positions which do not contain significant data. As the DD steps through DDO, a sign data digit is written, a one bit if the sign is minus and a two bit if the sign is plus. The four and eight bit positions of DDO are used to encode parity information for the word. The MARUFF's are stepped down to select the next lower numbered memory address and the writing process is repeated for that address. After DDO of memory address 20 has been written, an extra data bit and complement bit is written. This is the Start Read signal for the Read operation.

MACHINE STYLES

The E2150 number denotes the group or family of striped ledger machines and does not refer to a specific machine. The styles of machines that have been released to date are shown in the following chart.

STYLE	CONSOLE	PROCESSOR	MEMORY				STRIPES		TTM&TFN
			100	80	40	30	1(SS)	2(DS)	
E2154	F1E23	E2060			O		X		O
E2158	F1E23	E2060		O			X		O
E2160	F1E23	E2060	X				X		O
E2178	F1E24	E2080		O				X	
E2180	F1E24	E2080	X					X	
E2188	F1E23	E2090		O				X	X
E2190	F1E23	E2090	X					X	X

X - denotes standard construction - O - denotes options available on order

PARITY

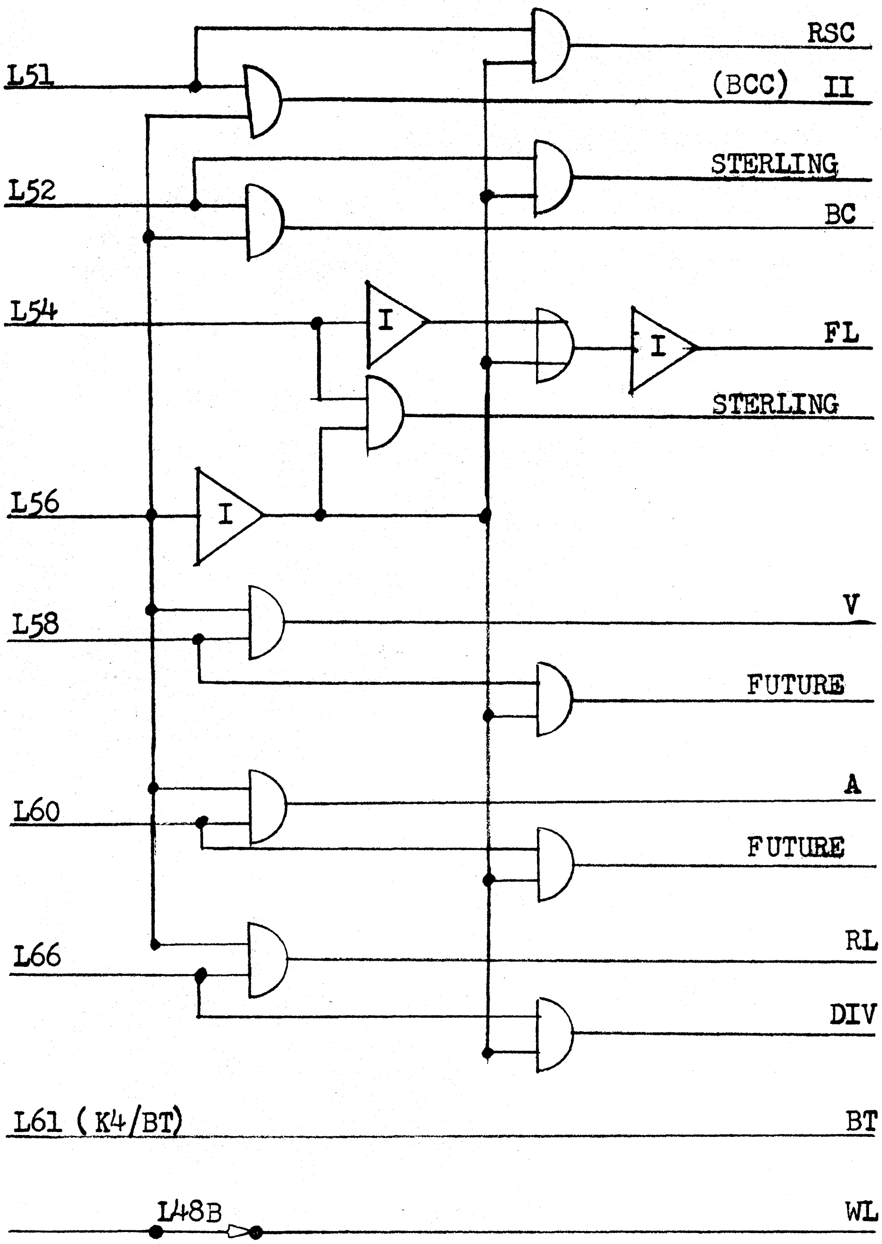
The parity check for the E2150 machines is a word parity. All data bits written on the stripes for each word are counted in multiples of four by the Parity FFs. The complement of this sum is written in the 4 and 8 bit positions of DDO of each word. During the read operation, this information is used to set the parity FF at DDO then the data bits read are used to count the FFs. At the end of each word, both Parity FFs must be set to indicate an acceptacle read operation. Parity is discussed further in the Write logic operation.

STRIPED LEDGER CONTROL LANES

In order to obtain the maximum use of the control lanes of the panel, most of the striped ledger lanes are gated with lane 56 to produce the SL signals. This means that to obtain a striped ledger signal lane 56 and another lane must both be programmed. This system is some times referred to as multiplexing. Figure I-2 shows the lanes used for the stripes ledger operation. The chart at the bottom of the figure shows the lanes that must be programmed for each operation.

LOWER ELECTRONIC GATE

The Striped Ledger electronic gate is mounted below the E2100 gate and adjacent to the power supply. The gate contains 140 card positions, with the pins toward the inside of the machine. The gate pivots through approximately 120 degrees so that the pins are accessable for servicing. 32 neon lights are provided so that the condition of various FFs can be determined during servicing. A fan provides ventilation for the cards.



Lane	48B	51	52	54	56	58	60	61	66
II (Initial Installation)		X	X		X				
BC (Blank Card)			X		X				
FL (Feed Ledger)				X	X				
V (Verify)					X	X			
A (Align)					X		X		
RL (Read Ledger)					X				X
WC (Write Correction)			X		X		X		
WL (Write Ledger)	X								
BT (BLOCK TRANSFER)					X			X	

Figure I-2
For Form 3738

BASIC LEDGER OPERATIONS

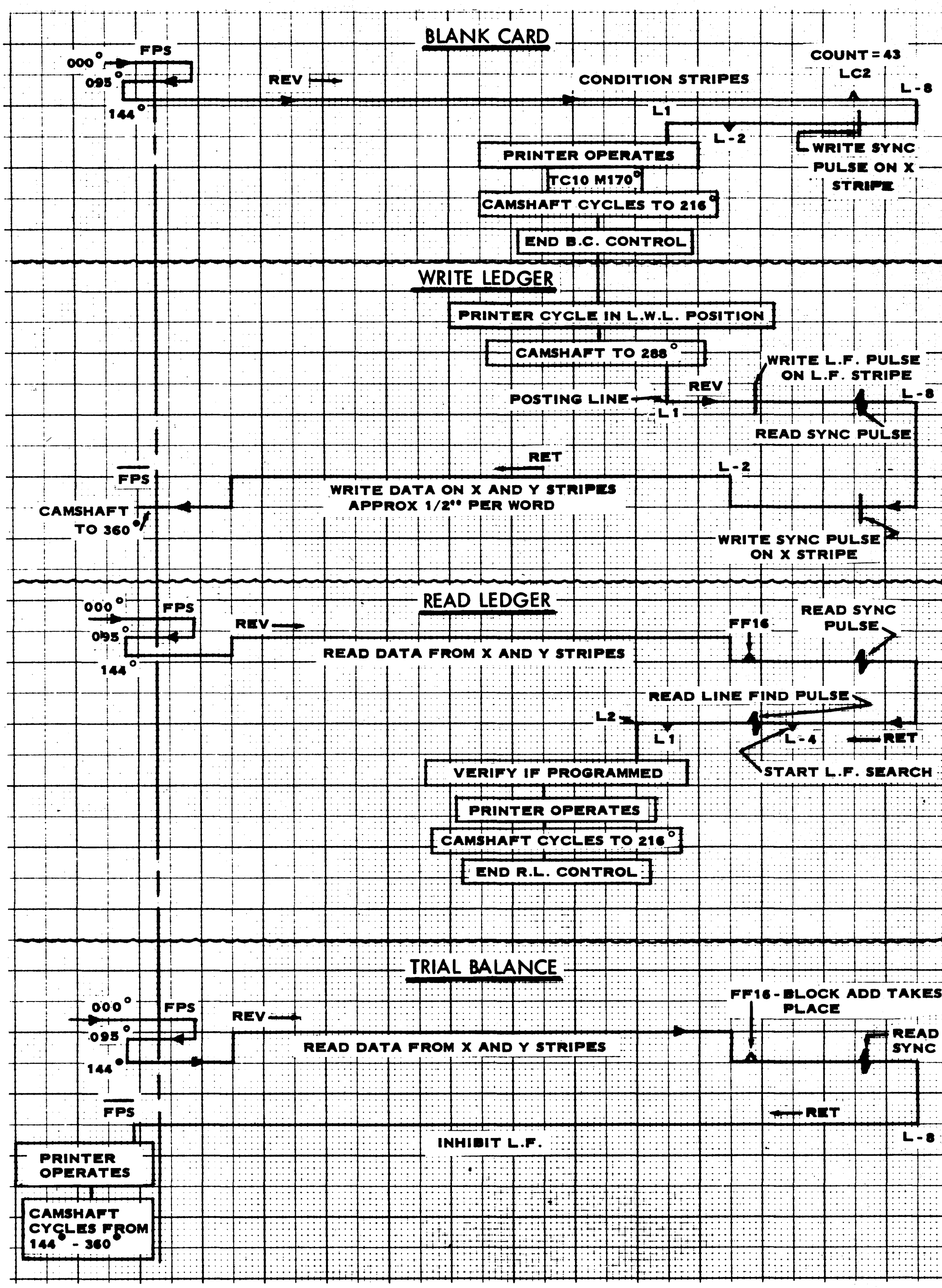


FIGURE I-3

MACHINE PROGRAMMING CHANGES

EKA-RKA

Beginning with machine F160058 diode C2J TB770 (page 507) was removed to provide additional flexibility of the EKA-RKA function.

With the diode removed lane 53 does not cause a combination of the keyboard M.A. keys with those pinned in the panel. If lane 53 is programmed, it now only enforces an operator depression of a keyboard M.A. key.

The lane 65 function has not been changed, therefore, if programmed, a combination of pinned and indexed keys without key enforcement is obtained.

When both key enforcement and binary combination is desired lanes 53 and 65 must be pinned.

An example use of this new programming could be as follows:

Lane 53 is pinned on an IEC position to enforce an operator memory selection to be used in the following AEC position. It is not desirable to alter the address on the IEC position. During the following EC positions pinned & indexed M.A. are combined by merely programming lane 65.

(BA) BLOCK ADD - (BTF) BLOCK TRANSFER

Beginning with Serial #F161884P, the Block Add-Block Transfer function has been separated from the automatic function of the Read Ledger Non-Align command. The new construction permits programming either of these functions with RLA or RLN. Block Add now requires a pin in lane 53 along with the RLN (56-66) or RLA (56-66-60). Block transfer now requires a pin in lanes 53 and 51 along with the RLN (56-66) or RLA (56-66-60).

Reference: Section I, Page 6

FORM HEADING STYLE 1

Beginning with Serial #F161884P, machines are wired to accept this feature. Form heading style 1 permits automatic alignment of striped ledgers to line -3 when the check limit switch is in the forward position. This allows "heading" alignment without turning the platen rearward. The form must be advanced to line #1 or higher to encode a usable line find pulse.

The check limit fingers are only active with the switch in the rearward position where normal Blank Card operations align the form to line #1.

Logic card "A" may have to be installed in position D5D to activate the feature.

Reference: Section I, Page 6

ONE WORD "WRITE"

Programming a one word "write" should be avoided on all machines that step the counter Flip Flops with the BOLP signal. Due to the non synchronous (without USMV) stepping of these counters, FF3X may set prior to stepping the DD's in sequence A, resulting in a non detected short "write".

Reference: Section I, Page 2

FEED LEDGER

Beginning with Serial #F161884P, programming Feed Ledger has been interlocked to permit passing over FL pins in other schedules during tabulation and return or Type From Memory.

The programming of FL now requires that a FL (Feed Ledger) pin or a RPT be programmed in the printer cycle preceding the desired Feed Ledger Stop position. The first feed after turning on the machines requires the depression of a motor bar.

Reference: Section VII, Page 40

AUTO LANE 29 INDEX WITH TFM

Beginning with Serial #F158459P, an automatic typewriter key 2 operation is indexed during type from memory whenever the capacity of the decade is reached on all E2190 systems.

Reference: Section VI (Temporary), Page 55.

CARRIAGE TRAY

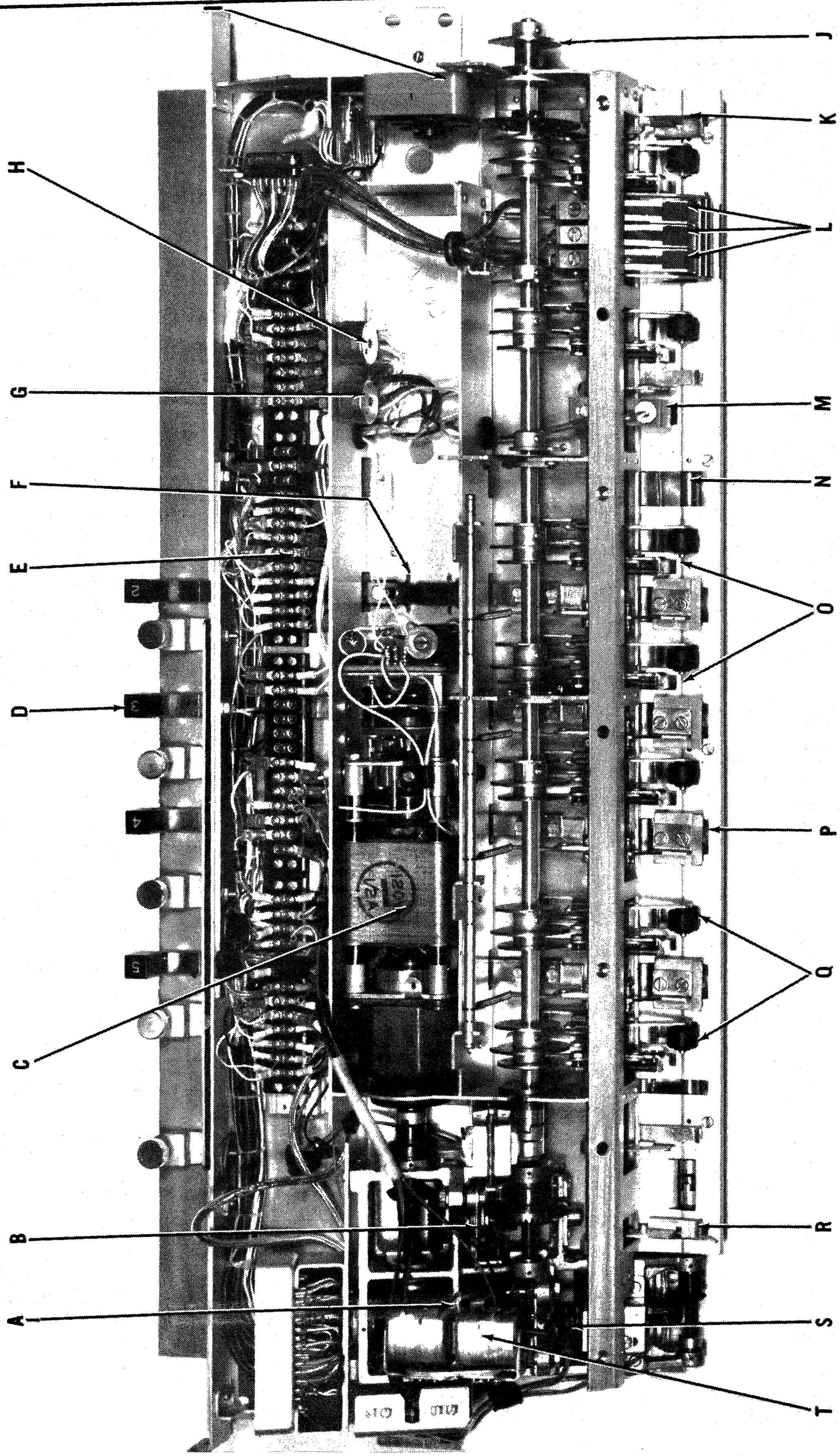
The carriage tray contains the mechanisms necessary to provide the automatic handling of the ledger after the initial insertion of the form into the carriage. These mechanisms are located on the tray which is built within the carriage.

The carriage tray (Figure II-1) contains the front paper switch (FPS) M, pusher fingers O, pressure rolls Q, drive rolls under pressure rolls, and drive shaft N, magnetic heads L, form guides K, manually retractable form guides P, program camshaft J, carriage timing switches I, carriage motor C, carriage gear box and program camshaft clutch assembly B, paper drive clutch assembly T, reverse clutch assembly A, terminal board E, timing disk unit BOL S, potentiometer R2001 H, potentiometer R2002 G.

The principal functions of the carriage tray are to square the form, feed the form into and out of the carriage, align the form to the proper printing line, read and write the data on the magnetic stripes, provide electrical timing signals and space the journal.

TRAY OPERATION DURING ONE COMPLETE SEQUENCE

The initial insertion of the form is done by the operator, inserting the form into the carriage throat far enough to interrupt the beam of light FPS. Once the beam of light is broken the machine takes control of the form from the operator. When the beam of light is broken, circuits are completed to start the carriage motor and trip the program camshaft by picking the prog. camshaft solenoid. The program camshaft clutch couples the carriage motor to the program camshaft through reduction gears.


H
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T

As the program camshaft is rotated, several functions are performed. First a set of cams make the pusher fingers advance in order to move the form upward. This movement is designed to position the form in the carriage and ensures that the form is not skewed and will drive straight into the carriage.

Now the stripes being aligned properly with the magnetic heads and the program camshaft continuing to turn, will cause at around 75° the release of the pressure rolls and grip the form against the driver rolls. By now the magnetic heads will also be lowered through the control of a cam on the program camshaft and the pusher fingers will retract and be lifted.

At approximately 95° of the program camshaft, CC2 switch is high, which in turn will cause the REV solenoid to be energized. This will engage the REV clutch and give the proper direction of turn to the PD clutch so to be able to feed the form into the tray. CC2 CC3 will also trigger a 100 ms. delay multivibrator which when timed out will cause the PD solenoid to be energized. As it takes 2.25 ms. for each degree turned of the program camshaft, by the time the PD clutch is coupled and the drive shaft is turning, the program camshaft clutch will be in its detent position of 144° and disengaged.

Now the form travels in and data is being read by the magnetic heads, the machine performing logic operations to store this information in the memory unit at the same time. When the X head reads the sync. pulse, the logic will enter the routine of stopping the inward travel of the form. The timing disk unit S, see Fig. II-1, in the paper drive gear box assembly will now give the electronic section the indication when to disengage the PD clutch.

Through a DMV the RET clutch solenoid is energized when the PD clutch has been practically disengaged, avoiding by this delay any wrong stopping of the PD clutch assembly due to bouncing in the REV clutch. As soon as the RET solenoid is energized the 100 ms. DMV is triggered, allowing the PD clutch to be tripped again, when it times out. As the RET clutch is now coupled, the form will move outwards and the logic in the electronic section will be in the line find routine. When the line find head reads the line find signal, the logic will enter the routine of stopping the outward travel of the form. The disk unit will now give again the electronic section the indication when to proceed to disengage the PD clutch, assuring in this manner a good line find.

If the check form limits were required, switch S2001 active, Fig. II-21,the check stop solenoid would pick turning the limits into active position. The printer would cycle now and during the cycling the prog. camshaft solenoid is picked tripping the program camshaft clutch and the program cams turn to 216°. The magnetic head will then be lifted as well as the pressure rolls and the carriage motor stopped.

The posting operations are now performed and the program camshaft remains at 216°. The carriage tray will not come into action again until a write ledger operation is programed. When this should be the case the carriage motor will start turning and the program camshaft clutch be tripped. The program camshaft will turn to 288°, the magnetic heads and pressure rolls being lowered during this interval. At approximately 250° of the camshaft C2 is high and will trigger the 100 ms. multivibrator which when times out and NOT TAB causes the PD solenoid to be energized. By the time the PD clutch is coupled, the program camshaft clutch will be in its detent position of 288° and disengaged.

The form is driven back into the carriage, the line find head is conditioned to write the new line find position on the stripe. When the sync pulse is read the electronic section and the tray mechanisms will go into the routine of changing the form travel by reversing the movement of the ledger in a similar manner as already explained during the read operation. As the form is driven out of the machine the new data is written on the stripes. At this time the timing disk unit BOL in conjunction with the electronic section checks the speed of the motor. Herewith the machine controls the speed at which the form travels outward (15 in/sec) and therefore the packing density of pulses on the stripe. When the form is completely driven out of the tray it will not interrupt the beam of light FPS any more, causing the program camshaft solenoid to be picked, which in turn will trip the program camshaft clutch. At approximately 320° CC2 will indicate the logic to energize stop paper drive solenoid, stop the carriage motor, lift the magnetic head, lift the pressure rolls, lower the pusher fingers and space the journal. The program camshaft continues to cycle until it stops in its detent position at 360°.

BEAM OF LIGHT FORM SENSING FPS

The front paper switch FPS form sensing unit, located on the front of the carriage tray, consists of a lamp holder enclosing a bulb which produces the beam of light and a solar cell unit, held by an independent bracket, see Fig. II-2. The lampholder A is supported by bracket B and the solar cell F is supported by bracket G to the tray.

The beam of light is aimed at the solar cell and there is a small opening on the support bracket of the cell so the beam cam reach the cell. As light shines on the solar cell it will produce a voltage at its terminals of around 200 mv.

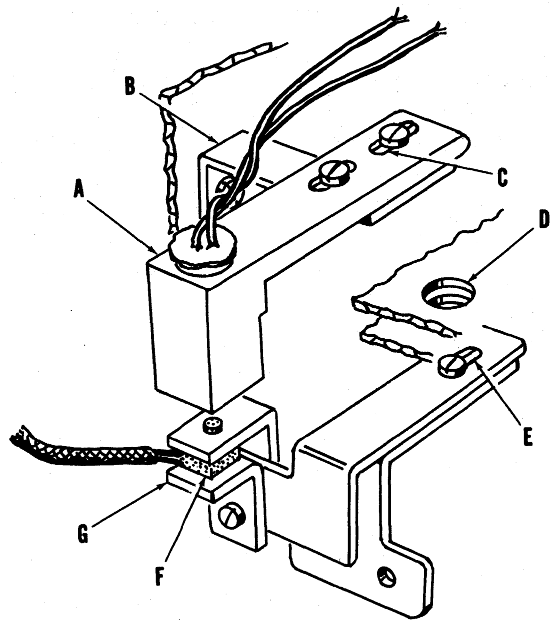


Figure II-2

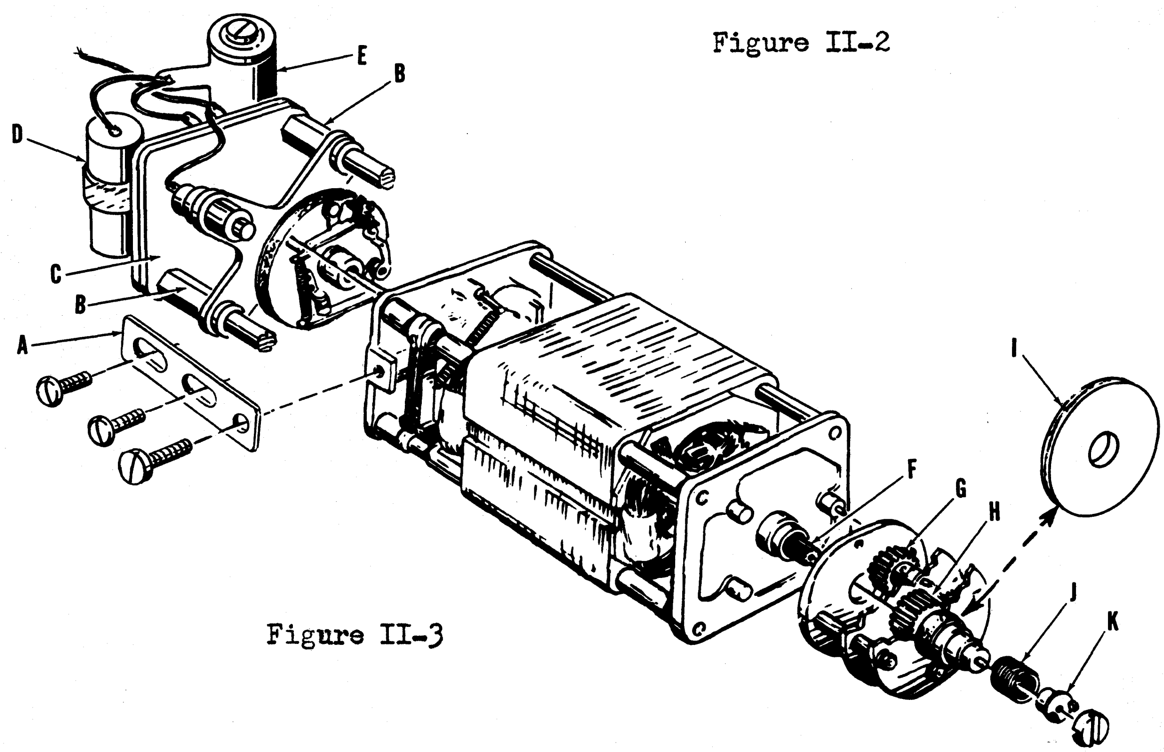


Figure II-3

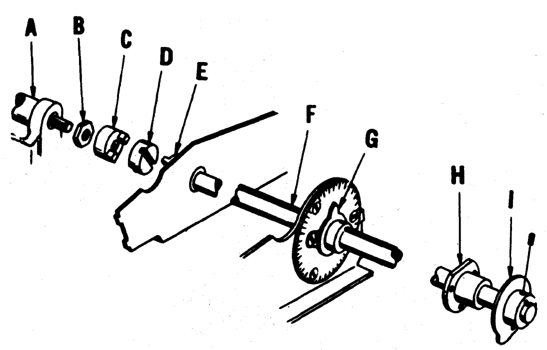


Figure II-4

This voltage is fed into the electronic section. The work of the solar cell in this application is one of a switch but without any mechanical wearout problems nor intermittent contact conditions. The intensity of the beam of light can be adjusted by potentiometer R2001 F, see Fig. II-1. The distance between the lamp and the solar cell unit is about the same as the tray throat opening were the form enters. Now, when a ledger is introduced, the paper will block the light from reaching the cell and in such a way give a front paper switch signal.

CARRIAGE MOTOR

The E2150 carriage motor is a universal type motor which will operate on either direct current or alternating current within the voltage limits specified on the motor rating plate. The carriage motor speed is maintained by a centrifugal governor and checked by the timing disk BOL unit in conjunction with the electronic section. It should be around (6400 rpm).

The motor is located in the center of the carriage and is mounted to the carriage at three points. The governor end is held in place by two screws through rubber bushings in the front and rear carriage partition plates. The screw through the rear partition is held by an adjustable mounting bracket A which can be positioned for proper mesh of the coupler between reduction gear box shaft and paper drive unit. The reduction gear box is mounted to the carriage partition plate by a rubber mounting grommet I. A capacitor D and a resistor E are mounted on a terminal board C which is secured to the end of the motor by posts B. The capacitor supresses arcing when the motor switch contacts open. The resistor serves to limit the charging voltage of the capacitor when the governor contacts are open and prevents high current flow through the contacts when they close.

Motor power is transmitted to the paper drive unit through a 11.75:. reduction gears F, G and H, the spring clutch J and a universal coupler element K.

PROGRAM CAMSHAFT

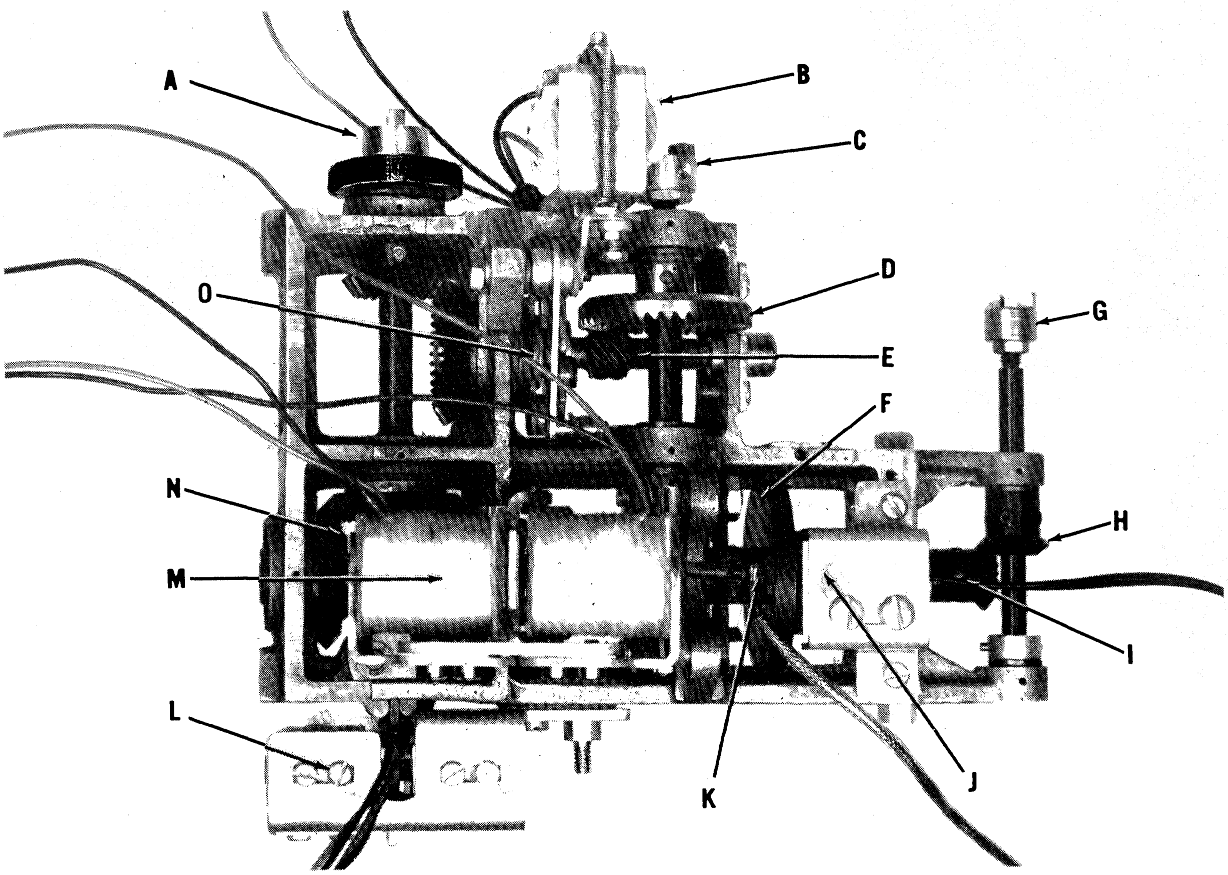
The program camshaft F, see Fig. II-4, located in front of the carriage motor, is positioned laterally across the carriage. It contains the cams which operate the pusher fingers, magnetic heads, pressure rolls, spaces the platen and turns the gears of the electrical timing switches. The shaft is coupled to the program cam clutch through a universal coupler element which is driven by an adjustable coupler at the carriage gear box. A degree indicator G which indicates the position of the shaft, is mounted on the program camshaft near the center of the carriage.

GEAR BOX ASSEMBLY

The gear box assembly, see Fig. II-5, is located on the left end of the carriage tray and basically consists of the program clutch unit O, reverse clutch unit N-L, paper drive clutch unit M and BOL disk unit F-J-K.

PROGRAM CLUTCH

The program cam clutch, see Fig. II-6, couples the power shaft N to the program camshaft. When the program cam solenoid S is energized, its armature is lifted, causing the armature latch R to rock clear of the lip of the clutch pawl J. This permits the torsion spring P to rock the clutch pawl upward. The clutch pawl dog K then engages the ratchet wheel L which couples the level gear H and the spiroid gear G. This causes the program camshaft to start its cycle. The detent pawl Q prevents overthrow and backlash of the program camshaft. One complete rotation of the program cam clutch turns the program camshaft 72 degrees at a rate of approximately 1 degree per 2.25 milliseconds.


A
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O
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F
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H
M
I
L
K
J

When the solenoid is de-energized, the armature latch is restored to normal and is rocked into the path of clutch pawl to disengage the clutch.

REVERSE CLUTCH

The reverse clutch, see Fig. II-7, located in the carriage paper drive unit provides the means for reversing the direction of the paper drive clutch, for driving the form into or out of the machine. The reverse clutch driving gears F, L are driven by the bevel gear on the end of power shaft A. The clutch driving gears are in constant mesh with the bevel gear and are driven in opposite directions. When the form is to be fed into the machine, solenoid G is energized attracting clapper I. Clutch actuator J pivots on post K causing clutch member B to be moved into engagement with rear gear L, thereby coupling shaft A to drive shaft C in the clockwise direction. When the form is to be fed out of the machine, solenoid H is energized to cause clutch member B to move forward to engage forward gear F, thereby driving shaft C counter clockwise.

PAPER DRIVE CLUTCH

The paper drive clutch couples the reverse clutch assembly to the driving pressure rolls, which drive the form into or out of the carriage.

When the paper drive solenoids A, see Fig. II-8, is energized the stop paper drive solenoid L is de-energized, the clapper K lifts out of the path of detent lugs H on the detent drum E and raises the clutch pawls F and J out of the path of the detent lugs. A compression spring inside the casing forces the detent drum clutch member E rearward to mesh with the driving clutch member C.

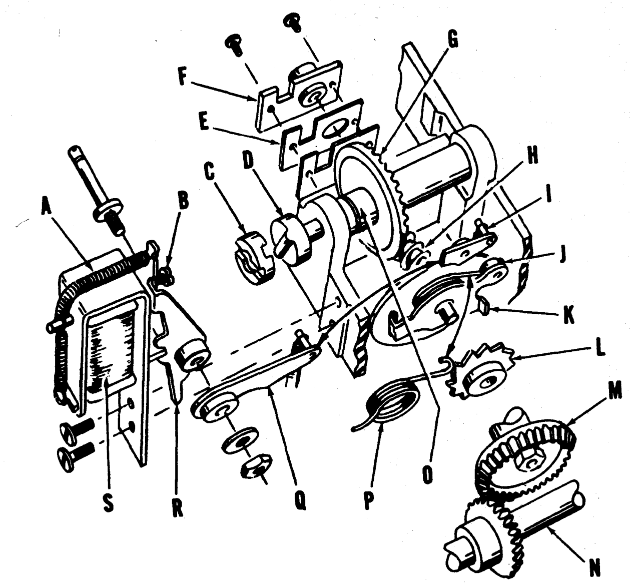


Figure II-6

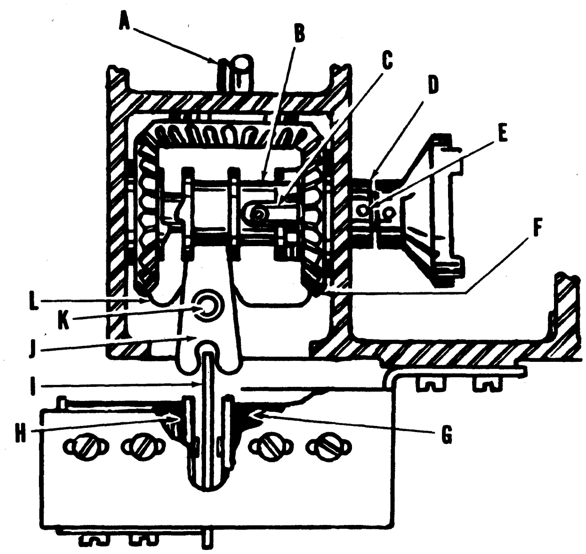


Figure II-7

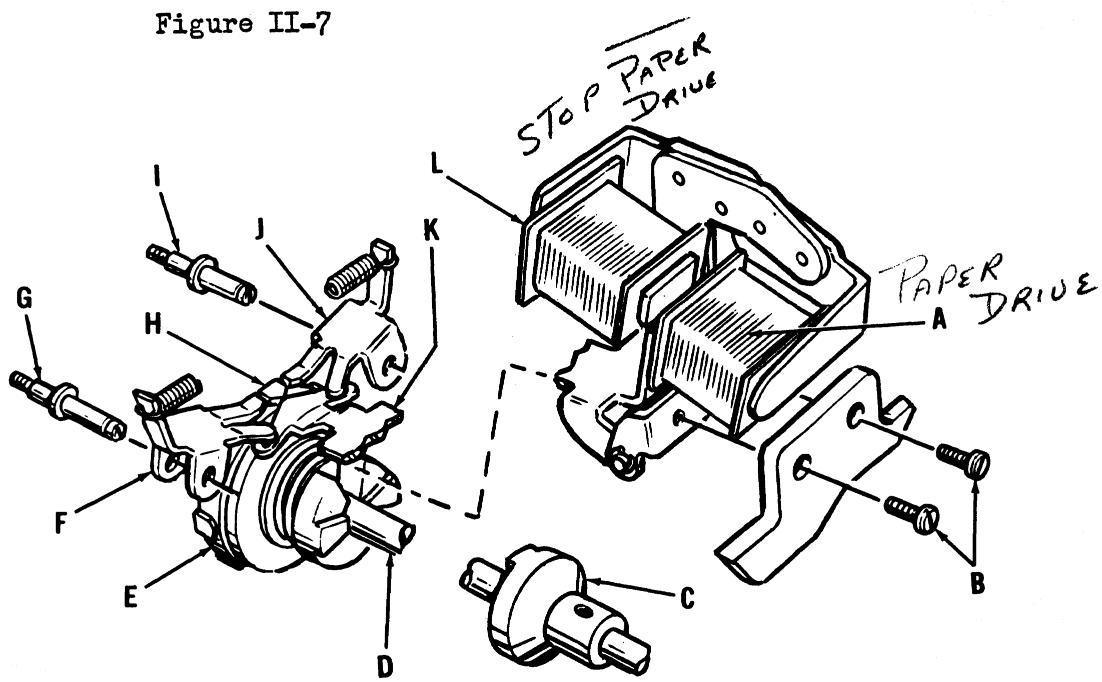


Figure II-8

The driving clutch member, which is rotated by the reverse clutch, causes shaft D, which is internal to and concentric with the casing, to rotate through the detent drum clutch member, and drive the clutch bevel gear E. The clutch bevel gear E, see Fig. II-9, is meshed with the geared pressure roll bevel gear B.

When the stop paper drive solenoid is energized the paper drive solenoid is not energized and the clapper and clutch pawls are positioned in the path of the detent lugs. This disengages the detent drum clutch member from the driving clutch member, which stops the feeding of the form. The BOL disk B, Fig. II-10, adds inertia to the detent drum to ensure the detenting of the lug in the clutch pawls.

BOL DISK UNIT

The BOL disk unit is located in the paper drive assembly, see Fig. II-10, and the disk itself is mounted on the shaft coupled to the paper drive clutch. The disk rotates between a solar cell and a lampholder in which there is located the light.

The solar cell G is held by a bracket and flat spring. The lampholder A is held on the paper drive unit be bracket I. The unit is assembled in such a way that the beam of light is aimed at the solar cell bracket opening, behind which is located the solar cell.

The timing disk B has ten openings equally spaced on its outer part and as the timing disk rotates between cell and light bulb, the beam of light will only reach the solar cell when a disk opening is exactly in line with them.

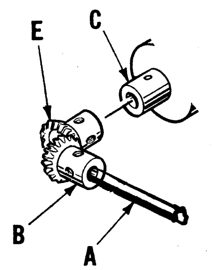


FIGURE II-9

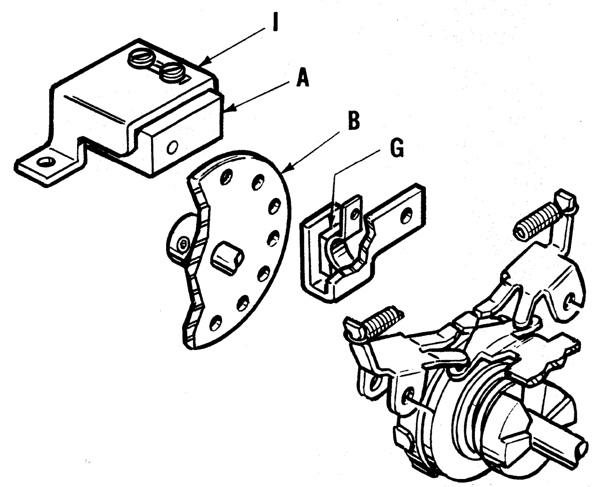


FIGURE II-10

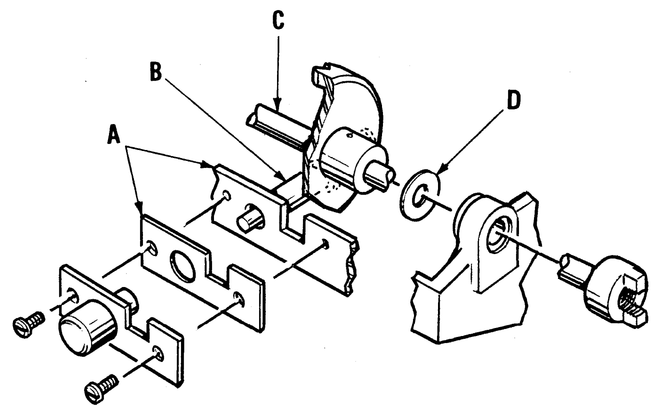


FIGURE II-11

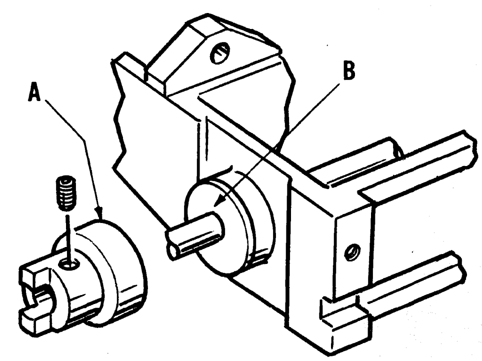


FIGURE II-12

The unit provides a means of controlling the time when the stop paper drive solenoid should be energized in order to disengage the paper drive clutch and get good alignment of the form. During the write operation it provides a means of checking the speed of the motor and therefore the distance between pulses on the outcoming ledger.

1) End play in shaft A should not exceed .003".

TO ADJUST: Remove excess play of shaft A toward the left, and position gear B as required. Tighten screw on flat sides of shaft. See Fig. II-9.

REASON: To maintain proper alignment and prevent excessive play in mesh of gears.

2) With the play of using C removed toward the front, clearance between gear E and bearing D should not exceed .003". See Fig. II-9.

TO ADJUST: Place .002" gauge between gear E and bearing D, move gear E to gauge and tighten screws.

REASON: To maintain proper alignment and freedom of parts and prevent a binding condition in mesh of gears.

3) End play in worm shaft B should not exceed .003". See Fig. II-11.

TO ADJUST: Add or remove shim A as required.

REASON: To maintain alignment of parts and prevent excessive play in mesh of gears.

4) End play in spiroid gear shaft C should not exceed .005". See Fig. II-11.

TO ADJUST: Add or remove shim D as required.

REASON: To maintain alignment of parts and prevent excessive play in mesh of gears.

5) With the end play of shaft C removed toward the right, clearance between coupling A and bearing B should not exceed .003". See Fig. II-12.

TO ADJUST: Place a .002" gauge between coupling A and bearing B, move coupling A to gauge and tighten screws.

REASON: To maintain proper alignment of gears and freedom of parts.

6) With all play of shaft D taken up toward the front of the unit, clearance between set collar E and shoulder of bevel gear C should not exceed .005". See Fig. II-13.

TO ADJUST: Position set collar E as required.

REASON: To eliminate excessive end play of shaft D.

7) Clapper C should pivot freely and have no more than .005" side play between the formed ears of bracket A and washers B. See Fig. II-14.

TO ADJUST: Add or remove washers B as required to both sides of clapper C.

REASON: To ensure minimum side play of clapper C when it detents clutch D.

8) With clapper C normal and a projection of clutch D located between clutch pawls B and E, there should be .003" to .005" side clearance between each projection G and clutch pawls B and E, when the clutch pawls are rotated. See Fig. II-15.

TO ADJUST: Starting with the low side of eccentrics A and F upward, rotate eccentrics inward, symmetrically as required.

REASON: To maintain porper alignment of each projection G and clapper C.

9) With solenoid L energized and any projection H of clutch E located between clutch pawls F and J, the point of clapper K should align centrally with the point of projection H. See Fig. II-8.

TO ADJUST: Loosen screws B and move solenoid assembly to right or left as required.

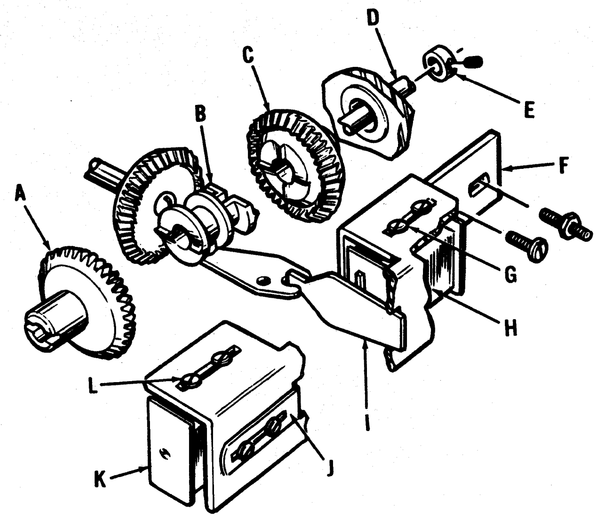


Figure II-13

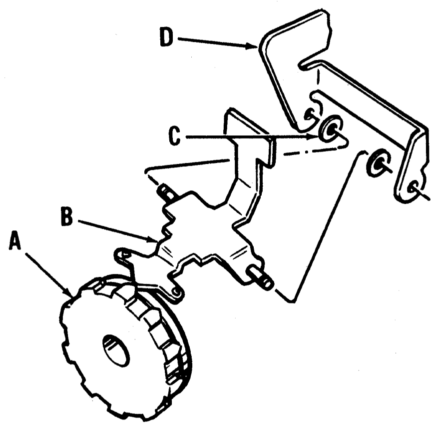


Figure II-14

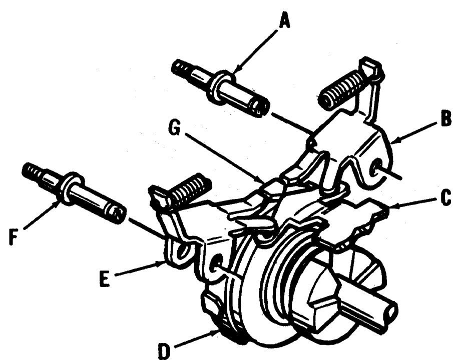


Figure II-15

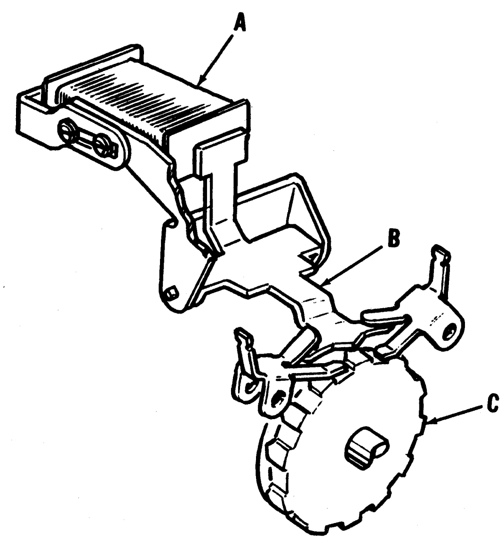


Figure II-16

REASON: To establish the normal position of clapper K and ensure disabling of clutch E.

10) With solenoid A energized, there should be .006" to .008" clearance between the lower side of clapper B and the upper surface of each projection on clutch C. See Fig. II-16.

TO ADJUST: Loosen screws holding solenoid A and move solenoid as required.

REASON: To ensure engagement of clutch C when clapper B is raised.

11) With solenoid L energized and any projection H of clutch E located between clutch pawls F and J, there should be .001" to .003" clearance between the pads on clapper K and projections of clutch pawls F and J. See Fig. II-8.

TO ADJUST: Bend projections on clutch pawls F and J as required.

NOTE: If excessive bending of clutch pawls F and J is required to make above adjustment, reset eccentric posts G and I (one at a time) to lower clutch pawls F and J, maintaining .003" to .005" side clearance between projection H and clutch pawls F and J. (See Test No. 7)

REASON: To ensure that clutch pawls F and J have a full hold on projections H and releasing clearance over projections H when solenoid A is energized.

12) With solenoid L energized, and any projection H positioned by clutch pawls F and J to limit on the point of clapper K, all play of shaft D should be taken up toward the front of the unit, and there should be from .005" to .008" clearance between the high surface of the teeth of clutch driver C and clutch E at their closest possible point. See Fig. II-8.

TO ADJUST: Position and tighten clutch driver C as required.

REASON: To ensure correct clearance between clutch members C and E and prevent an early disengagement of clutch members, resulting in the 1/10 clutch E not being driven to its normal position between clutch pawls F and J.

13) With any projection D of clutch F located between clutch pawls E and G any hole of disk B must align with hole in bracket C and there must be .025" to .035" clearance between bracket C and disk B. See Fig. II-10.

TO ADJUST: Loosen set screw I and position disk B as required.

REASON: To establish the normal position of disk B.

14) With any projection D of clutch F located between clutch pawls E and G, the hole in lamp holding block A must align with the hole in disk B and there must be .025" to .035" clearance between disk B and lamp holding block A. See Fig. II-10.

TO ADJUST: Loosen two screws and position lamp holding block J as required.

REASON: To ensure that the light of lamp block A will reach solar cell H at the time that a projection of clutch F is located between pawls E and G.

15) <u>NOTE:</u> Prior to Test, solenoids H and K should be centralized in slots G and L or mounting bracket F. With solenoid H energized, the teeth of clutch member B should have a full hold with the teeth of gear A. See Fig. II-13.

TO ADJUST: Loosen screws holding solenoid bracket F and shift bracket forward or rearward as required.

REASON: To ensure rotation of paper feed rolls and proper form insertion.

16) With solenoid K energized the teeth of clutch member B should have a full hold with the teeth on gear C. See Fig. II-13.

TO ADJUST: Loosen screws holding solenoid K and position the solenoid as required.

REASON: To ensure rotation of paper feed rolls and proper form ejection.

17) With solenoids H and K de-energized, there should be .003" to .005" clearance between limit J and clapper I, see Fig. II-13.

TO ADJUST: Loosen screws holding limit J and position as required.

REASON: To ensure proper function of clapper.

18) With solenoid A energized, there should be .008" to .012" clearance between latch E and lip C of clutch throw-out arm. See Fig. II-17.

TO ADJUST: With clapper B of solenoid A held against the core,slide solenoid A up or down as required.

REASON: To ensure passing clearance for lip C of clutch throw-out arm and full engagement of clutch pawl.

19) With solenoid A at normal, latch E should have .005" to .010" overlap on lip C of clutch throw-out arm. See Fig. II-17.

TO ADJUST: Turn screw D as required and secure with lock nut.

REASON: To ensure full hold of latch E on lip C and disengagement of clutch members.

CARRIAGE TIMING SWITCHES

The carriage timing switches, see Fig. II-18, are located in a very compact package on the right end of the tray. They are coupled directly to the program camshaft through a pair of gears (A) with a 1:1 ration.

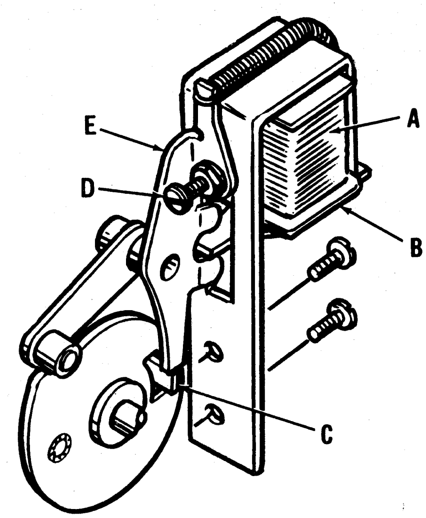


Figure II-17

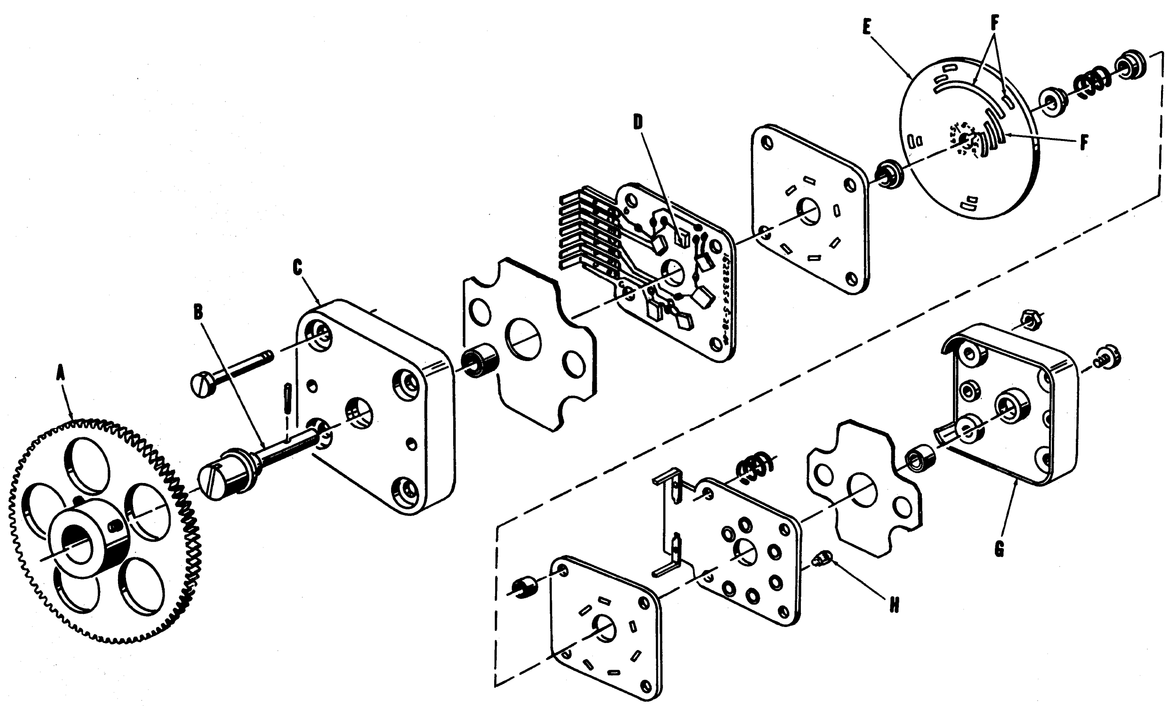


Figure II-18

There are six timing switches contained in the package and each switch consists of a solar cell D activated independently during different time intervals by its corresponding beam of light H through a rotating disk E. This disk is made of darkened plexiglass in which there are slots F, each set of slots being spaced at six different diameters around the disk. The plexiglass in the slots is transparent. As the disk rotates between the solar cells and the light bulbs each set of slots on one diameter will control one of the switches.

Refer to timing chart, Fig. II-19, for information concerning the making and braking of each one of these switches.

PUSHER FINGERS AND PRESSURE ROLLS

The pusher fingers and pressure rolls are controlled by cams on the program camshaft, see Fig. II-20. As the program camshaft turns, the pusher cam C drives the pusher cam follower B. This causes pusher finger T to be driven forward to contact the form, which is then squared and forced out to the proper starting position. The pusher fingers move forward from 10° to 50° of the program camshaft. At 75° the pressure rolls are lowered very rapidly against the driving roll, because the pressure cam arm H comes off the high point of the pressure roll cam G and is tensioned by spring F. Also, from 75° to 80° of the program camshaft, have the pusher fingers retracted completely. From 80° to 100° of the program camshaft the pusher finger lift cam D actuates pusher finger lift bail E to lift the pusher finger clear off the form. Now at 144° the program camshaft with the form in the proper starting position, the driving rolls drive the form into the machine. Once the form is properly positioned the program camshaft will turn again and the pressure rolls stay down until 195° of the program camshaft.

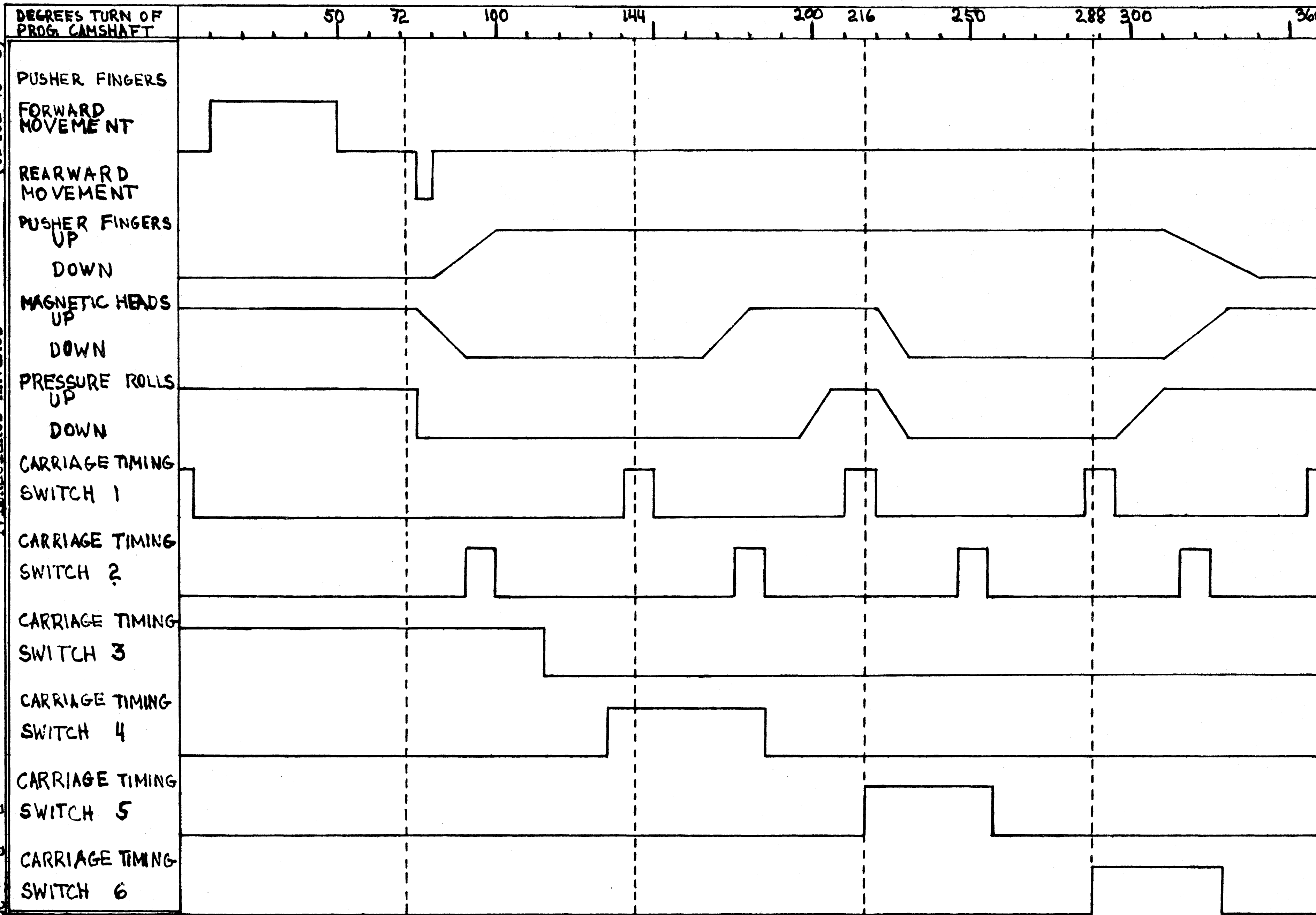

DEGREES TURN OF PROG. CAMSHAFT
50
72
100
144
200
216
250
288
300
360
PUSHER FINGERS
FORWARD MOVEMENT
REARWARD MOVEMENT
PUSHER FINGERS UP
DOWN
MAGNETIC HEADS UP
DOWN
PRESSURE ROLLS UP
DOWN
CARRIAGE TIMING SWITCH 1
CARRIAGE TIMING SWITCH 2
CARRIAGE TIMING SWITCH 3
CARRIAGE TIMING SWITCH 4
CARRIAGE TIMING SWITCH 5
CARRIAGE TIMING SWITCH 6

FIG. II-19

At 195° they start to lift and are fully raised at 205°. They stay up during posting, 216°, and are lowered again when the machine is driven into the writing routine. The pressure rolls begin to lower then at 220° and are down at 230°. This allows the form to be driven in and out to write the new data on. As the writing occurs at 288° of the program camshaft, the pressure rolls are down but when this is completed, the pressure rolls go up to 300° and are fully raised at 315°. The pusher fingers move down at 315° and they are completely lowered at 340°.

MAGNETIC HEAD ASSEMBLY

The magnetic head assembly, see Fig. II-20, located on the right side of the carriage, has three independent heads O. One head is for the line find system, the other two heads are for the X and Y stripes respectively. With these heads it is possible to read, erase or write data during different portions of the program camshaft cycle.

The magnetic head is a device which contains basically a laminated core and a winding. The winding is around one part of the core leaving the rest of the core free. This core has a horseshoe form separating one end from the other by a silver plate. The open end is located directly opposite to the magnetic stripe. This arrangement will force part of the magnetic flux in the laminated core to bridge through the air at the gap filled by the silver plate. As the stripe is sliding under the head the magnetic flux which leaves the core will find a path through the stripe back to the core on the other side of the gap. The stripe is of magnetizable material which will orient magnetically depending on the flux direction.

MAGNETIC HEAD ASSEMBLY - continued

Now the direction of the flux through the core will depend on the direction of current flow through the winding, this being controlled by the write amplifier circuit and the electronic section. The reversal of magnetic orientation on the stripe will cause during a read operation an induced voltage or read signal in the winding around the laminated core. Each magnetic head is mounted on a holder M which pivots on shaft S and has post L which through spring K will tension the magnetic head drum on the driver roll. Bracket N will rock head assembly up if cam I lowers the cam follower arm J. Bracket N pivots on shaft S. There is also an idler P mounted on a frame Q in front of the head assembly and its purpose is to keep the form against the tray through spring tension R, straightening out the form before the stripes slide under the heads.

The magnetic head assembly will be lowered at 75° and be completely down at 90° of the program camshaft. It will not lift until 165° so that during read 144°, the heads are down. At 165° the head assembly starts to lift off the form and is completely up at 180°. During posting, 216°, the head assembly will be up. If the machine enters after posting a writing routine, the heads will lower and be completely down at 320°. When writing is performed at 288°, the heads are down and after it is performed and the program camshaft cycles into home position they will start to raise at 295° being up at 310°.

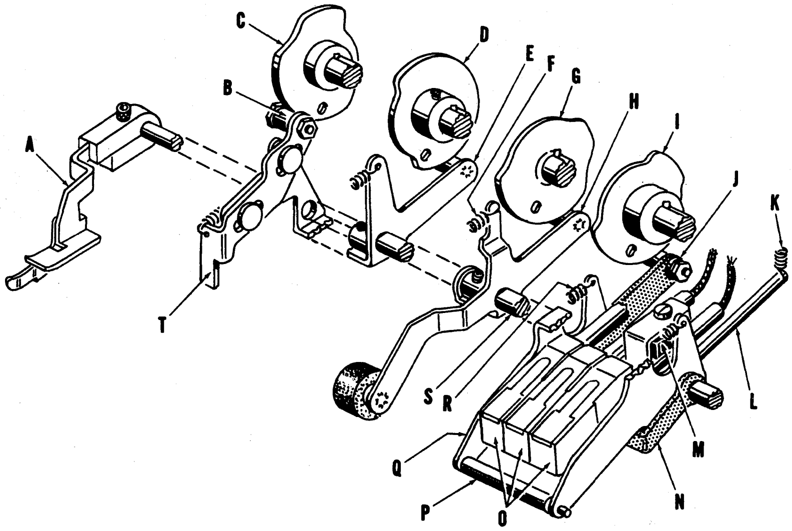


Figure II-20

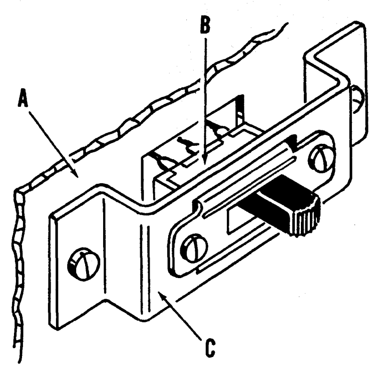


Figure II-21

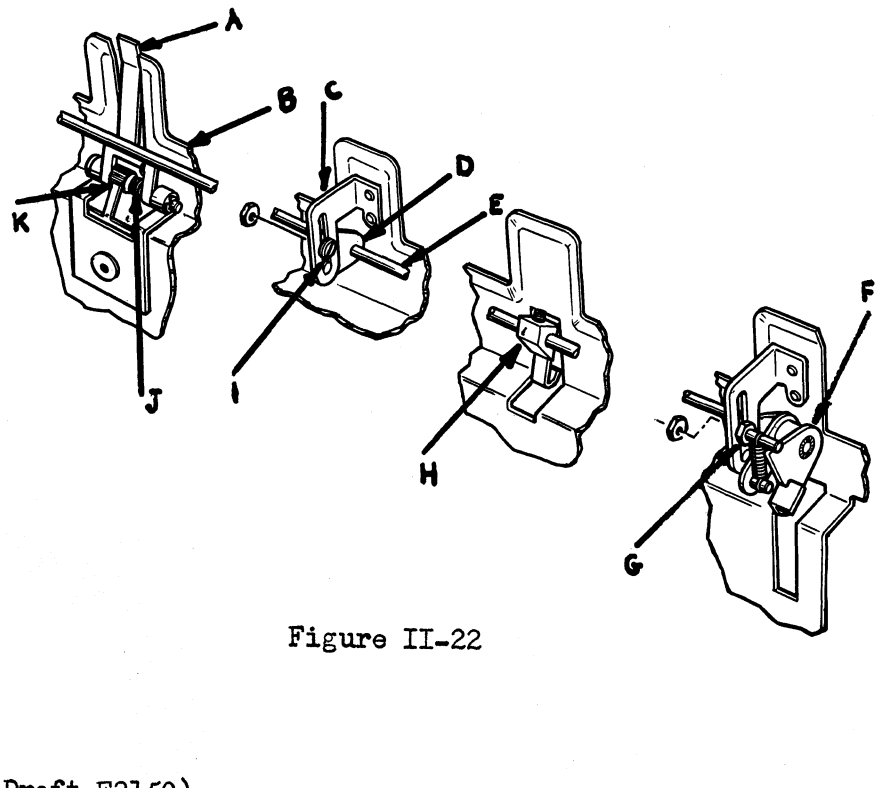


Figure II-22

INNER FORM GUIDES AND MANUALLY RETRACTIBLE FORM GUIDES

There are two fixed form guides A on the tray, one on the outer right and the other on the left end, see Fig. II-20. They can only be repositioned by loosening their mounting brackets. The fixed form guide on the right has a definite relation with respect to the magnetic stripe on the form and the magnetic head. The fixed form guide on the left can be positioned for forms of 16 1/2" or 19" width. There are also five manually retractible form guides D, see Fig. II-1, which serve as a limit for the left edge of the form and when active take over the function of the fixed form guide on the far left. If any one of these guides are pushed forward by a knob on the back part of the tray, the corresponding form guide will lower on the front part. The form guide will be held up or down by means of a flat spring detent F limiting in a knotch on the slide which goes from the rear part of the tray to the front. This slide is connected on its front part to the tail of the mounting bracket holding the guide.

These manually retractible form guides are numbered from one to five for different forms as shown below.

Manual Retractible Form Guide	Meant For Forms of the Following Width
No. 1	6"
No. 2	8"
No. 3	10"
No. 4	12"
No. 5	14 1/2"

CHECK LIMIT ASSEMBLY (FORM LIMITS STYLE 10)

The check limits H are on shaft E which is held by support plates D and support bracket C under ledger pan B, see Fig. II-22. These form limits, 5 in total, when active provide a limit and support for forms as a check for example, so that they are easily inserted and retain an aligned position for printing. The limits pivot on shaft E and when inactive are below ledger pan B. When the limits are required, shaft E is turned so that limits H pass their lower bend portion through a slot in ledger pan B and limit any incoming form. The turning of shaft E so that limits H get in active position, is controlled by solenoid A, and moving link C, refer to Fig. II-23. Link C got as its front end round nut D, which will rock actuator F, Fig. II-22, and so turn shaft E with limit H. Solenoid plunger and link C return to normal position by spring tension as well as the check limits.

Check stop solenoid is energized after the ledger has been read and positioned through line find. The energizing of this solenoid is conditional with switch S 2001, see Fig. II-21. In order to be able to insert an additional form after the ledger has been read, the printer must be prevented from tripping and cycling. This is done by the NOW AUTO KEY, which prevents MB#2 solenoid to be energized.

Test and Adjustments -

1) For 1 1/2" statement printing line, locate support plates D on shaft E to front of slot in support brackets C of the statement and ledger pan B. See Fig. II-22. For 1 3/4" statement printing line, locate support plates D on shaft E to rear of slot in support brackets C of the statement and ledger pan B.

   TO ADJUST: Loosen nuts holding screws I and spring post G and locate support plates D as required.

   REASON: To establish the correct printing line.

   NOTE: When the printing line is not specified, use the 1 3/4" position.

2) For 1 1/2" printing line locate round nut D in forward hole of link C. For 1 3/4" printing line locate round nut D in rear hold of link C. See Fig. II-23.

TO ADJUST: Locate round nut D as required.

REASON: To establish the correct printing line.

NOTE: When the printing line is not specified, use the 1 3/4" position.

3) With pivot arm F limiting against post G, all form limits H should be below the top surface of the statement and ledger pan B by .025" to .030". See Fig. II-22.

TO ADJUST: Loosen set screw in form limits H and rotate as required.

REASON: To ensure that form limits H do not interfer with form insertion.

4) With the carriage open and solenoid A energized, the horizontal and vertical corners of form limits F should align with the surface of the statement and ledger pan E as shown in the insert. See Fig. II-23.

TO ADJUST: Position solenoid bracket B as required.

REASON: To ensure correct position of form limits F when solenoid A is energized.

5) With pressure fingers A and torsion springs J assembled to ledger and statement pan B, a pressure of 30 $\pm$ 3 grams should completely deflect the pressure fingers A until level with ledger and statement pan B. See Fig. II-22.

TO ADJUST: Rotate knurled spring tensioner K as required.

NOTE: The above Test and Adjustment should be made prior to assembly of the statement and ledger pan B into carriage.

REASON: To provide retaining pressure required for the manually aligned form.

6) With the feature, "Form-Dual Independent Alignment" and machine completely assembled, insert the manually aligned form into the carriage until the lowest line of the form heading aligns with the line on form table B for the first printing line, and to the bottom of the last printer line for each succeeding line thereafter.

6) (continued) This should provide for six (6) lines of printing per inch, with good visible spacing. See Fig. II-24.

TO ADJUST: Loosen screws holding form table B to brackets A and move table B up or down as required.

REASON: To provide optimum form alignment.

PLATEN SPACING

Platen spacing for the journal roll is actuated by a cam B, Fig. II- , mounted on program camshaft at the right end of the tray. The high portion of the cam contacts roll on screw F, Fig. II-25, to provide one space of the platen at 330° of the program camshaft rotation. The lower part of G is moved forward which moves pawl D rearward to turn ratchet E and the platen one space. Pawl D is returned to normal by spring tension.

Test and Adjustments -

1) Platen A should be free to turn and have no more than .012" side play between end plates M. See Fig. II-26.

   TO ADJUST: Use space washer J between end plate M and clip D on all non-split platens.

   REASON: To aid in maintaining vertical alignment of type print.

2) Split and normal platens A should be free to turn, and:

   a) Platens A should have no more than .012" side play between end plates M.

   b) The clearance between platens should not exceed .031". See Fig. II-26.

   TO ADJUST: a) Use space washers J between end plates M and clips D as required.

   b) Use space washers N between platens A and end plates M as required.

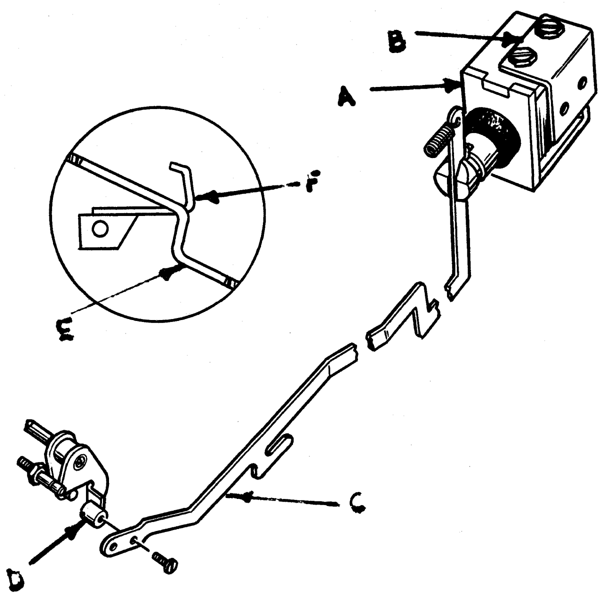


Figure II-23

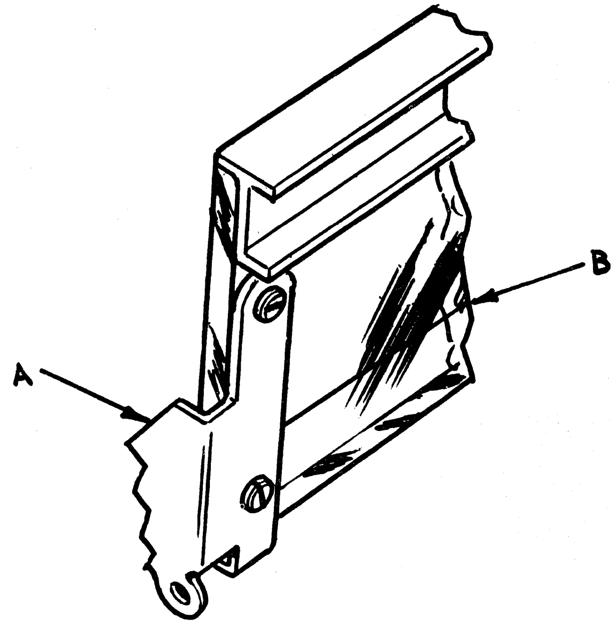


Figure II-24

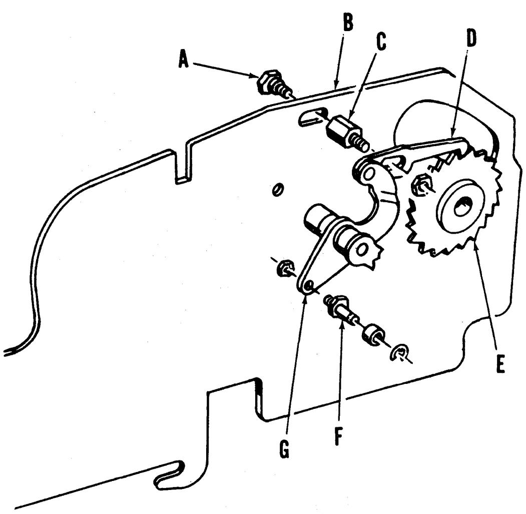


Figure II-25

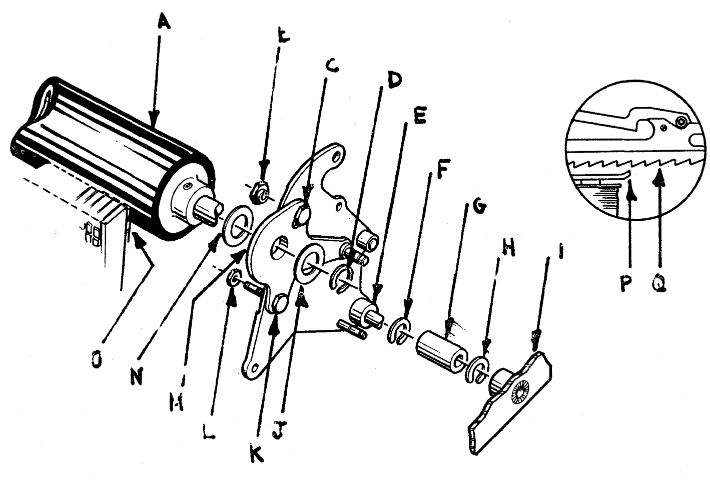


Figure II-26

3) With carriage open, paper fingers I should contact platen C evenly, and have at least .005" clearance under lower edge of aligning bail J. See Fig. II-27.

TO ADJUST: Bend paper fingers I as required.

REASON: To retain forms with carriage in its open position. To aid in maintaining vertical alignment of type print.

4) With the carriage in its closed position, rollers I on right and left support arms C should have a full hold without bind on hook arms H of carriage open and close shaft. See Fig. II-28.

TO ADJUST: Bend hook arms H as required.

REASON: To ensure positioning upper paper table E in open and close operations.

5) With a full keyboard indexed, type impression should be uniformly dense at top and bottom, in center and end positions of platen. See Fig. II-26.

TO ADJUST: Loosen screws C and K. Raise or lower platen A as required and tighten screws K with nuts L. Starting with the dot on eccentrics B at 12 o'clock, adjust eccentrics B as required for correct horizontal alignment of platen A, and lock eccentrics B with screws C.

NOTE: On unit assembly, place carriage on fixture J12922 and adjust eccentrics B for correct indicator read in.

REASON: To establish correct position of platen in relation to type.

6) The open and close bail A and space bail B must be parallel to the bearing surfaces of the raceways in casting within .010" from end to end. See Fig. II-29.

TO ADJUST: Weave open and close bail A and space bail B as required.

REASON: To provide uniform movement of bails with carriage in center and end positions.

7) The inner carriage shaft assembly E should have clearance not to exceed .008" between carriage sideframes I. See Fig. II-26.

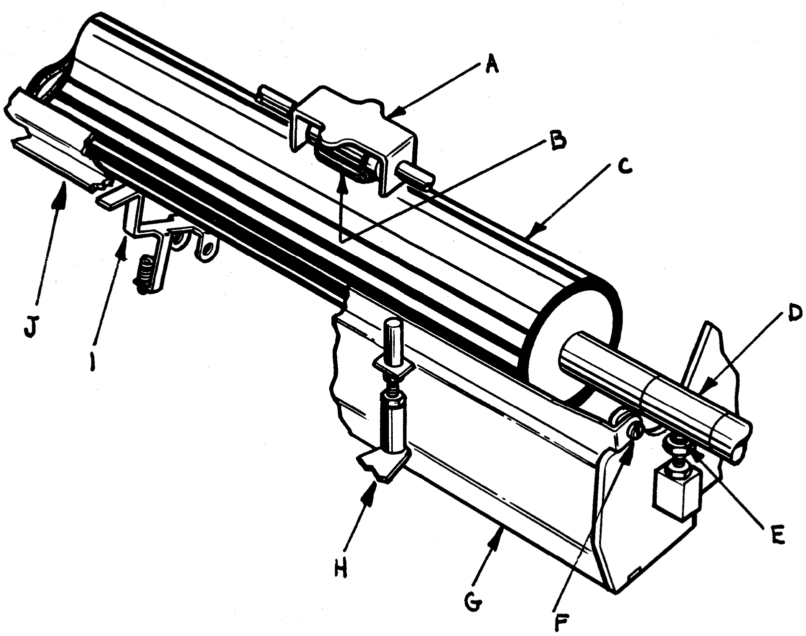


Figure II-27

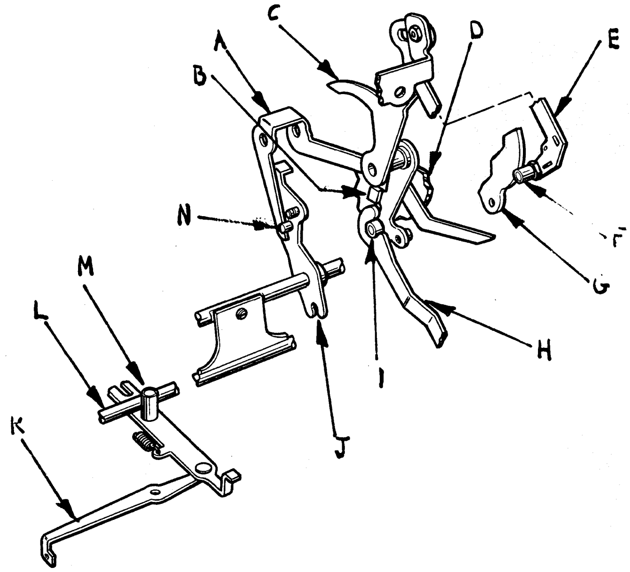


Figure II-28

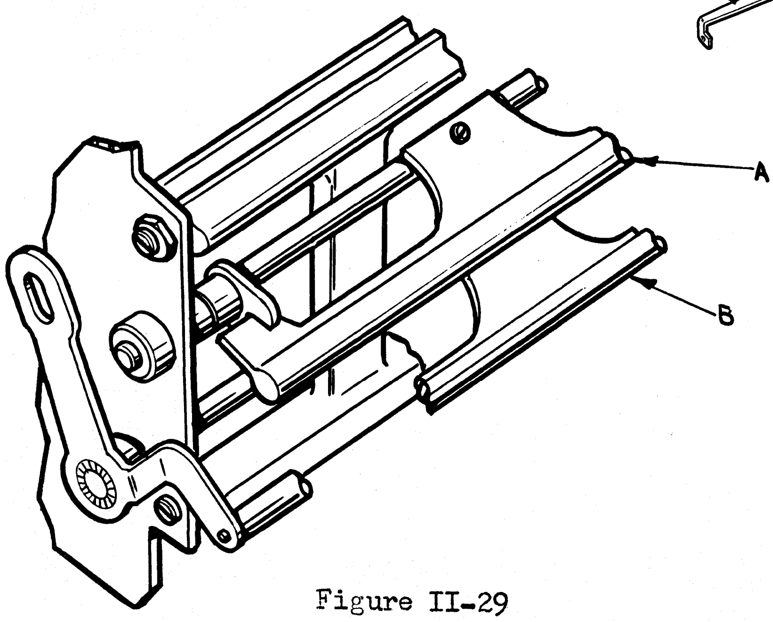


Figure II-29

TO ADJUST: Insert one shim H between sleeves G and R & L carriage sideframes I if required. If necessary, insert additional shims F between sleeve G and R & L inner carriage shaft assembly E as required.

REASON: To ensure clear type impression.

8) All pressure rolls B between R & L end rolls on upper pressure roll assembly should contact platen C with equal tension. See Fig. II-27.

TO ADJUST: Bend the front ear on support brackets A as required.

REASON: To prevent journal from slipping when carriage is open.

9) With the carriage in the open position, the lower arm of pressure roll release lever A should have a full hold on the stud H in lever B. See Fig. II-30.

TO ADJUST: Bend lower arm of the pressure roll release lever A as required.

REASON: To permit insertion and alignment of journal paper.

10) With carriage closed there should be no less than .020" clearance between platen C and form support G at both ends and center of platen and the form support should not contact ribbon guides H. On series F4000, F5000 and F6000 recheck the test after ribbon cover is installed to ribbon posts. See Fig. II-27.

TO ADJUST: With screws F loose, relocate form support G as required.

REASON: To provide clearance for correct feeding of forms.

11) With the carriage in its central position, there should be equal clearance between rollers C and end of enclosed cam B when carriage is in the open and closed positions. See Fig. II-31.

TO ADJUST: Turn eccentric D as required.

REASON: To ensure correct timing of carriage closing in relation to printing.

12) With inner carriage A in both open and closed positions, open and close bail G should be free to move forward and rearward between rollers E in slide F along the length of the bail. See Fig. II-31.

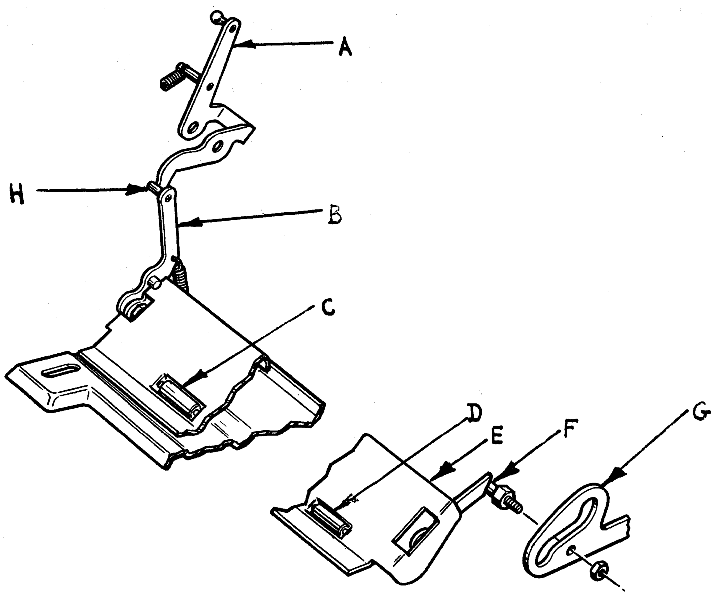


Figure II-30

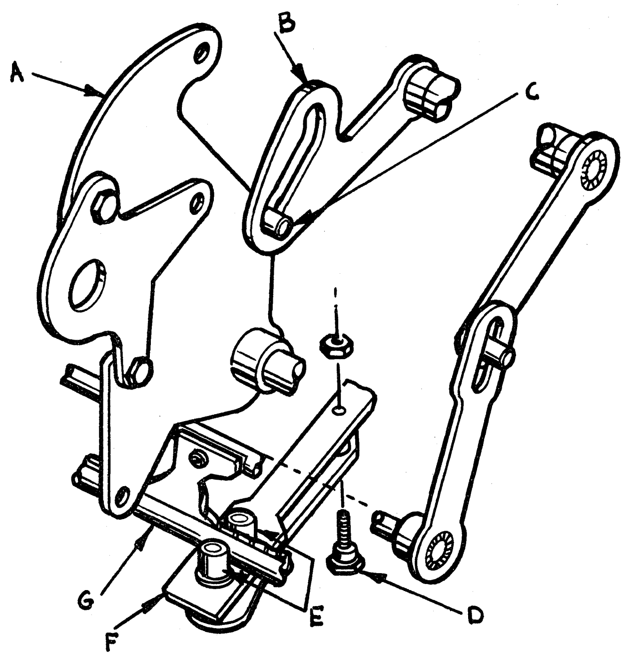


Figure II-31

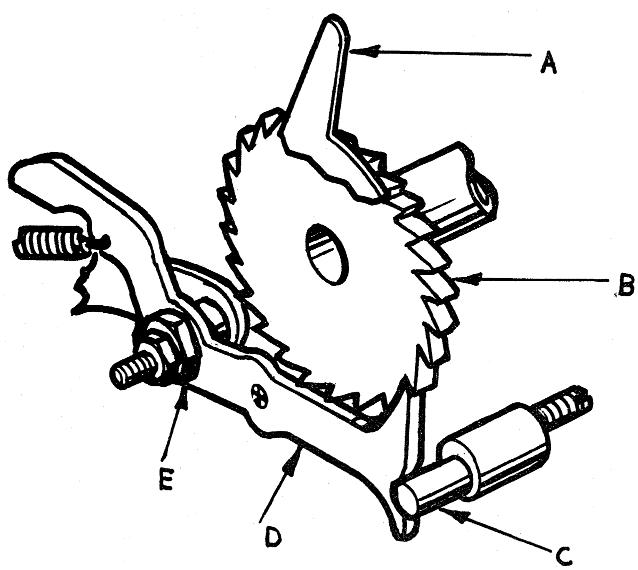


Figure II-32

TO ADJUST: Recheck Adjustments No. 6 and No. 11.

REASON: To ensure that bail G does not prevent the carriage from moving freely during tab and return.

13) With a full keyboard of fives indexed, cycle machine to 150°. There should be .137" to .142" clearance between platen A and type O at both right and left ends of platen. Cycle the machine and permit clappers P of the read-in unit to limit add racks Q in the No. 5 position. Continue to cycle the machine to 150°. There should be .137" to .142" clearance between platen A and type O at both right and left ends of platen. See Fig. II-26.

TO ADJUST: With screws K just snug enough to retain platen height, loosen screws C and adjust eccentrics B as required. Retighten screws K and C.

REASON: To provide correct relation between platen, type and hammer section.

14) a) With the carriage closed manually check the arm of bail A not to bind against stud N in the Platen Feed Shaft Assembly J.

b) With the carriage open and paper table E rearward there should be clearance between roll M on interlock assembly K and the entire length of the platen feed bail L. See Fig. II-28.

TO ADJUST: Weave bail A as required.

REASON: a) To allow the feed shaft assembly J to limit against roller M.

b) To permit unrestricted movement of interlock K with paper table E rearward.

15) With carriage closed, high side of eccentric stud C forward, and space pawl D moved to its extreme forward position against ratchet gear B, the platen should be spaced in multiplier of 1/6" spacing as indicated by space selector A. See Fig. II-32.

TO ADJUST: Turn eccentric E as required, starting with high side down.

REASON: To ensure uniform spacing of platen.

16) With space pawl D in its extreme forward position without binding, and adjusted in accordance with Adjustment No. 15, there should be no more than .006" clearance between space pawl D and eccentric post C. See Fig. II-32.

TO ADJUST: Turn eccentric post C as required, and determine clearance visually.

REASON: To prevent over space of the platen.

NOTE: Carriages with split and normal platens, Adjustments No. 15 and No. 16, should be performed on left side also.

17) With the carriage closed and centrally located on the carriage rails, apply slight pressure rearward to center of platen C to remove play. There should be clearance not to exceed .003" between pads E and the closest position of spacer sleeves D, determined by rotating platen shaft. See Fig. II-27.

TO ADJUST: Raise or lower pads E as required.

REASON: To provide an overthrow limit for platen C in the closed position to improve alignment of print.

18) With the carriage open and the right and left support arms C limiting on square studs B in carriage end D, eccentric rollers F should limit upper paper table E evenly on bearing plates G. See Fig. II-28.

TO ADJUST: Turn eccentrics F as required.

REASON: To establish normal open clearance between aligning bail and platen.

19) With carriage in its open position, set high side of eccentric stud C at approximately 9 o'clock, set high side of eccentric screw D at approximately 9 o'clock and against forward end of the elongated hole in E. Rotate program camshaft until highest point of space cam B is in contact with eccentric stud C (approximately 330°) at this point platen ratchet F should have spaced one tooth. See Fig. II-33.

TO ADJUST: Turn eccentric stud C as required.

REASON: To ensure form spacing.

20) With carriage in its open position, rotate program camshaft until highest point of space cam F is in contact with roller A on eccentric stud C (approximately 330°). Space pawl G should fully drive ratchet gear F into its detented position without a bind. See Fig. II-33.

TO ADJUST: Re-check Adjustment No. 19.

REASON: To prevent platen over spacing.

21) With the carriage in its open position, slowly rotate program camshaft from 330° until space pawl G and tooth of ratchet F are aligned point to point, as illustrated. Manually raise space pawl G, there should be .050" to .060" clearance between space pawl G and tooth of ratchet F. See Fig. II-33.

TO ADJUST: Turn or move eccentric screw D as required.

REASON: To ensure return of space pawl G to its normal position, and manual back spacing of platen.

INDEPENDENT PLATEN SPACING

Independent platen spacing on the E2000 is controlled by allowing pawl A or P, see Fig. II-34, to space the left or right platen. Pawl A can space the left platen if left indexing arm B permits A to engage on the left ratchet gear of the platen shaft, by raising arm B. Indexing arm B has at its rear end a stud D, that runs in enclosed cam C. Enclosed cam C is on the bail fastened to the left end of shaft F, which is held by the side frames on either end of the carriage. On this shaft are skids G and J which control the movement of indexing arms B and O respectively. Bracket H and I are fastened to the second carriage rail counted from the front with their projection pointing to the back of the machine.

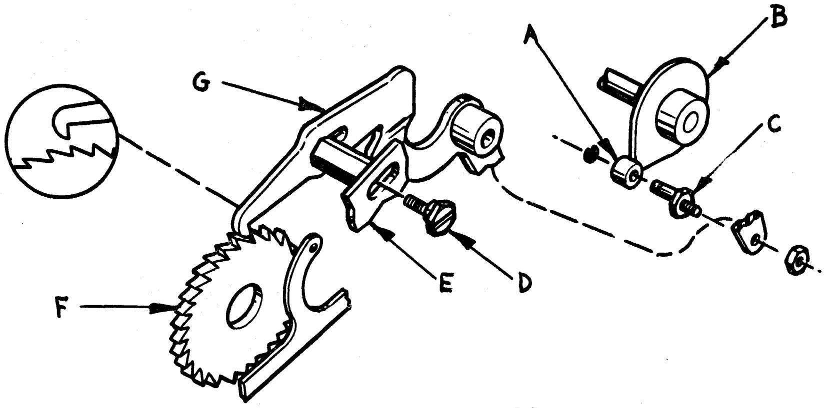


Figure II-33

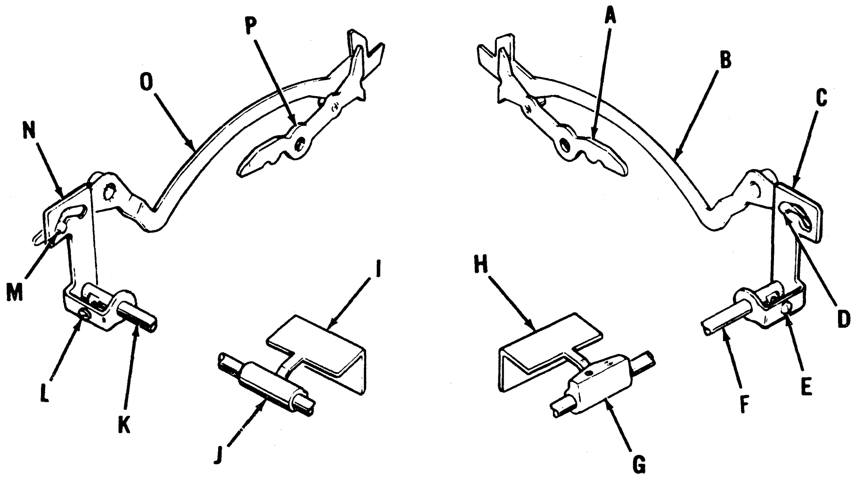


Figure II-34

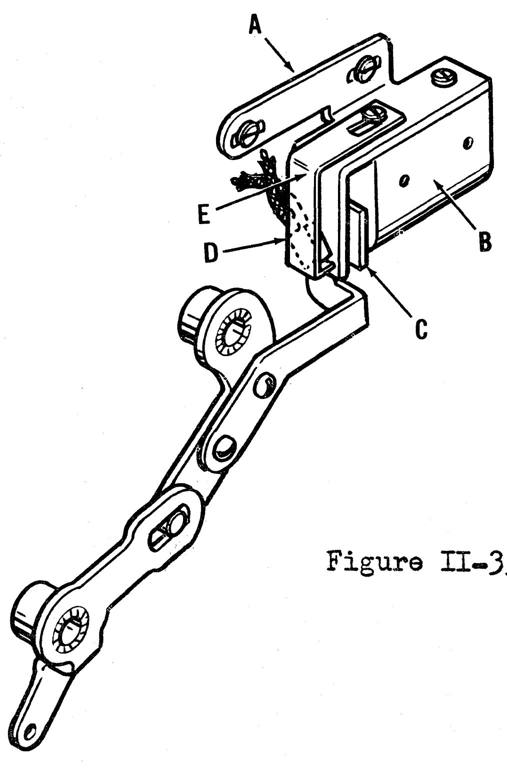


Figure II-35

Now, as the carriage moves from one side to the other for example, indexing skid G will pass over the projection of bracket H rocking E around and positioning C and D as shown on Fig. II-34. Indexing arm B is raised and allows pawl A to space only the left platen when indexed. The carriage will continue moving and at another position (depending on the programation of the machine and location of skids G and J will index skid J by passing under bracket I and rock the shaft in the opposite direction. This will cause N and M to be positioned, raise indexing arm O and permit pawl P to space only the right platen, when the spacing occurs.

Tests and Adjustments -

1) With cams C and N indexed by skids G and J studs D and M in the right and left indexing arms B and O should seat in detents of cams C and N. See Fig. II-34.

TO ADJUST: Position skids G and J as required.

REASON: To properly locate studs D and M in enclosed cams C and N.

2) a) With the high portion of indexing skid G positioned over the projection of plate H, the front end of left indexing arm B should be in a raised position, allowing pawl A to space the left platen. See Fig. II-34.

b) With the high portion of indexing skid J positioned under the projection of plate I, the front end of right indexing arm O should be in a raised position, allowing pawl P to space the right platen.

TO ADJUST: a) Loosen bristo screws and position indexing skid G as required.

b) Loosen bristo screws and position indexing skid J as required.

REASON: To ensure positive indexing from skids G and J and permit independent vertical spacing of two forms.

CARRIAGE OPEN SOLAR CELL

The carriage open solar cell assembly is located on the left carriage sideframe and is actuated by the carriage open mechanism. The whole assembly consists of a lampholder, see Fig. II-35B, enclosing a light bulb, which produces the beam of light. The lampholder is fixed by bracket A to the carriage left sideframe. The solar cell is mounted on an independent bracket E attached to the lampholder in such a way, that the solar cell is in front of the outcoming beam of light. The carriage open mechanism actuates a shutter C which can move in and out of the space between outcoming beam of light from the lampholder and solar cell as the carriage open or closes respectively. Thus, when the carriage is open, the light shutter will interpose between beam of light and solar cell and when the carriage is closed, the shutter moves out allowing the beam of light to reach the solar cell.

Test and Adjustments -

1) With carriage in open position, light shutter C should align centrally between light block B and mounting bracket A of photo cell D. See Fig. II-35.

   TO ADJUST: Loosen screws in bracket A and shift bracket as required.

   REASON: To prevent interference with light shutter C and stationary parts when opening and closing the carriage.

2) With carriage open, paper fingers I should contact platen C evenly and have at least .005" clearance under lower edge of aligning bail J. See Fig. II-35.

   TO ADJUST: Bend paper fingers I as required.

   REASON: To retain forms with carriage in its open position.

MOTOR BAR TWO SOLENOID

The stripe ledger unit has a solenoid which when energized will trip motor bar 2 in order to cycle the printer.

When the machine is in a blank card or read operation, the printer is in its normal position at zero degrees. After the blank card operation has been performed or after an ordinary read operation, where the data has been read and the form located properly, the printer has to cycle. If an Auto operation is indexed, motor bar 2 would energize, trip the printer and start cycling. By doing this, the printer must go through a normal tripping routine, closing the carriage first which is open, then energize in sequence the tappet solenoid, start relay and machine trip solenoid.

If a Non Auto operation is indexed by having the Non Auto key depressed, motor bar 2 solenoid will be not energized, this allowing the insertion of some additional form after the ledger has been read.

The motor bar 2 solenoid is fixed to the inside of the right printer frame, under motor bar 2 slide A, see Fig. II-36. Solenoid plunger D is linked to slide A directly so that when solenoid E energizes and pulls plunger D inward, slide A will lower and rock drive trip arm C around. This will trip the printer mechanically.

Tests and Adjustments -

1) With Motor Bar 2 held fully depressed, plunger D of solenoid E should just contact the core of the solenoid. See Fig. II-36.

   TO ADJUST: Loosen screws F. If necessary, lower solenoid E to permit full depression of Motor Bar 2, then position solenoid E as required.

   REASON: To ensure maximum power from the solenoid to trip the drive.

2) With Motor Bar 2 in its normal position and drive trip arm C limiting against eccentric screw B, there should be .020" to .025" clearance between the stud in motor bar slide A and drive trip arm C. See Fig. II-36.

   TO ADJUST: Turn eccentric screw B as required.

   REASON: To establish pre-travel of Motor Bar slide A, ensuring the tripping of the drive.

CARRIAGE OPEN LOCK SOLENOID

In order to prevent the manual opening or closing of the printer carriage during a blank card, read, write or posting operation, the stripe ledger machine has a carriage open lock solenoid.

The carriage open lock solenoid is fixed to the outside of the right auxiliary side frame by bracket E, see Fig. II-37. Clapper G, when solenoid C is energized, will rock blocking arm B around, causing step on arm B to move behind stud A. This will prevent indexing a manual carriage opening or closing by key I.

Tests and Adjustments -

1) With clapper G contacting the core of solenoid C, there should be clearance not to exceed .010" between the vertical surface of the step in interlock B and the rear of stud A. See Fig. II-37.

   TO ADJUST: Turn eccentric H as required.

   REASON: To permit indexing interlock B.

2) a) With clapper G contacting the core of solenoid C, there should be clearance not to exceed .010" between the upper surface of interlock B and stud A.

   b) With clapper G limiting against clapper limit F, depress the carriage open and close key I. Stud A should have passing clearance over the top of interlock B. See Fig. II-37.

   TO ADJUST: a. Move solenoid bracket E forward or rearward as required.

   b. Loosen screws D and locate clapper limit F as required.

   REASON: a. To permit energizing of solenoid C.

   b. To permit depression of the carriage open and close key I.

ENFORCED USE OF MEMORY ADDRESS KEYS

When a pin is active in lane 53 or a manual key is depressed, the lock relay is energized to open the machine drive trip circuit.

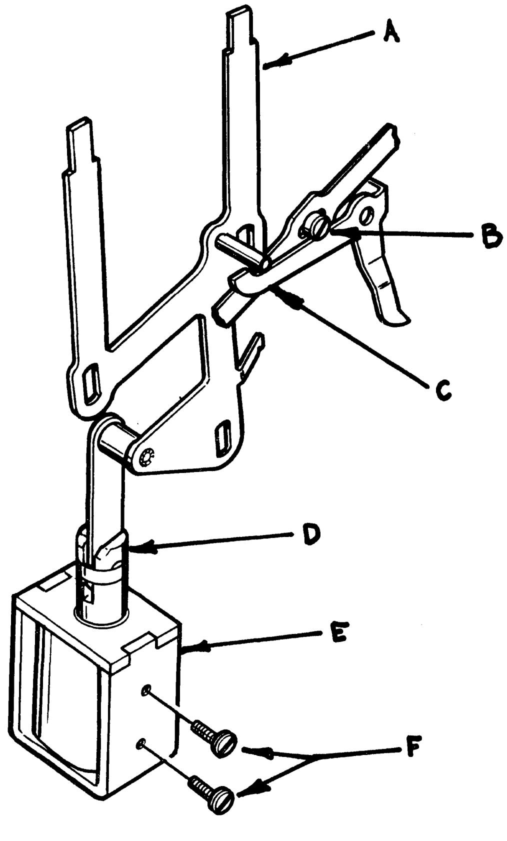


Figure II-36

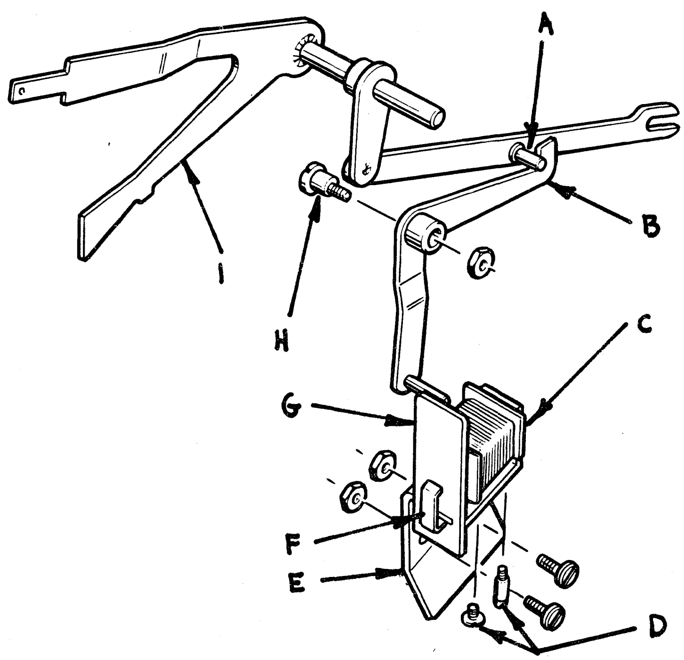


Figure II-37

This prevents the machine drive from tripping until a memory address has been indexed on the keyboard. Upon indexing a memory address on the keyboard, see Fig. II-38, switch H, is opened allowing the machine drive trip solenoid to be energized.

Depressing a memory address key cams slide A forward. Stud on slide A, contacts one of the fingers of bail B, rocking its bail arm forward. Bail arm of B has a stud attached to it, which when rocked forward will push projection of bail I to the front, turning arm of I away from switch H. This will allow switch H to restore, drop the lock relay and permit tripping the machine. With all memory address keys restored, both slides A are rearward and the ear on arm of bail I holds the plunger on switch H depressed through the tension of spring J.

Tests and Adjustments -

1) With no key in the memory address columns depressed and fingers of bail B limiting against the studs in slides A of the memory address columns, there should be .025" to .035" clearance between the ear of bail I and the body of switch H.

   TO ADJUST: Bend ear of bail I as required.

   REASON: To ensure transfer of switch contacts and maximum life of the switch.

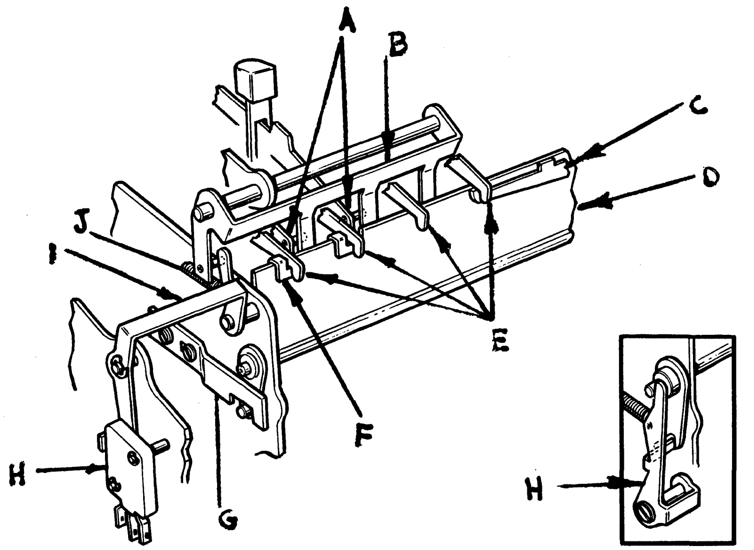


Figure II-38

READ-WRITE HEAD CIRCUITS

One read-write head is used for each stripe. A Read/Write head, Read Amplifier (RA), Write Amplifier (WA) and its control circuits are shown in Figure IV-1. During the write operation the head is controlled by the write Amplifier. CR1 and CR2 are reverse biased so that the write signals to the head are isolated from the Read Transformer. During a read operation CR1 and CR2 are forward biased so that the voltages induced in the head are inputs to the transformer. Pins 16 and 25 of the WA are wired to transistor collectors and are effectively an open circuit except during write ledger and BC operations. The two 1.6K resistors are across the head during a read ledger operation but the 3.2K combined resistance is so high compared to the head and read transformer that there is very little effect on the circuit.

Figure IV-2 shows the DC current path at static and during Read ledger. The AC voltage Pulses produced by the head during Read are also shown. Note that, the diodes are forward biased. This bias condition is produced by current from -100V through the 2.4K resistor, through two parallel circuits consisting of 1.6K resistors the halves of the primary transformer winding and the 10K resistor to ground.

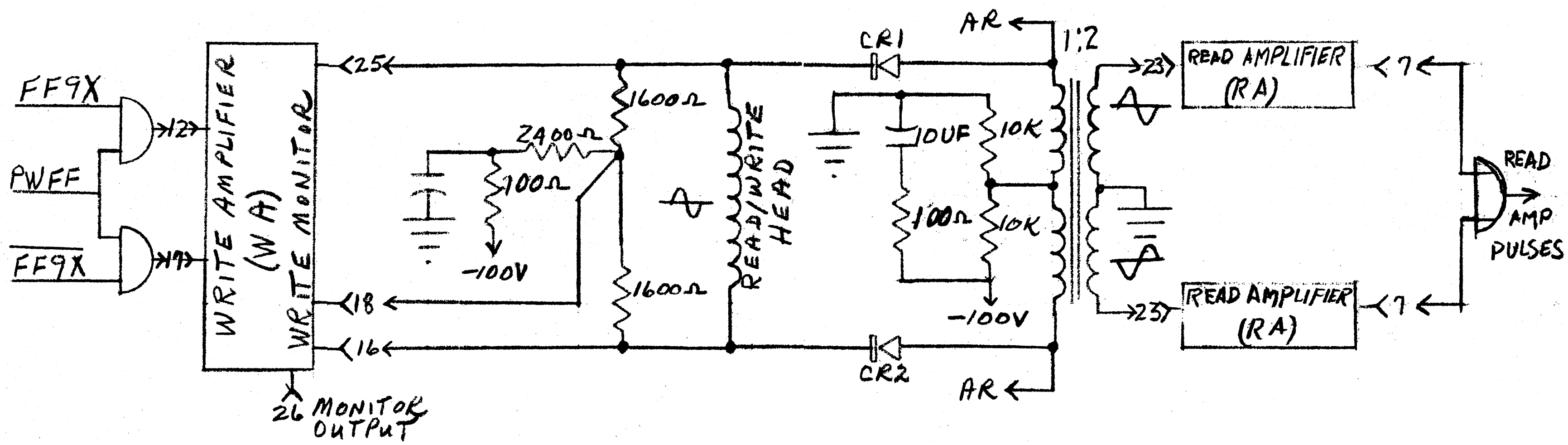


FIG. IV-1

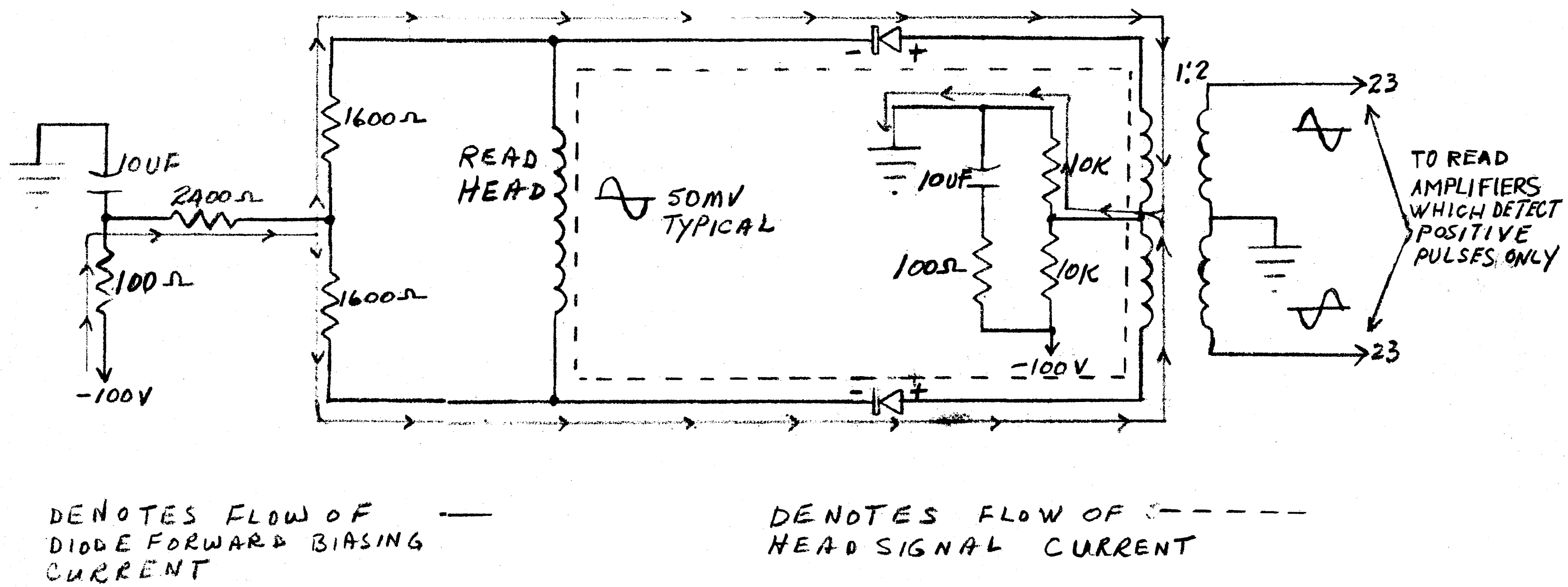


FIG IV-2

The voltages pulses induced in the head by changes of flux on the stripe will cause currents to flow in the primary winding of the transformer. The transformer is a 1 to 2 ratio transformer with the secondary center tap connected to ground. The secondary winding then, will produce two pulses that are identical in shape to the input. One of the secondary pulses will be 180° out of phase with the input. Each of these pulses will be applied to a read amplifier which will produce a READ AMP pulse for each positive peak of the input pulses. The outputs from the two read amplifiers are gated together through an OR gate to provide the read amp pulses from one stripe.

WRITE CURRENT

During the BC and write ledger operation the Permit Write FF (PWFF) will be set and the PWFF signal will be high. Either the 9XFF or NOT 9XFF signal will also be high. This will cause the inputs to the Write Amplifier at either pin 12 or 17 to be high. The WA circuit, which will be covered in detail later, will cause either pin 25 or 16 to go to ground. Figure IV-3 shows the current flow when FF9X}s set. Note the direction of current flow through the head and that the diodes are reverse biased to isolate the read transformer. Figure IV-4 shows the current flow when FF9X is reset. (NOT FF9X is high). Note the direction of current flow in the head and that the diodes are reverse biased to isolate the read transformer.

The reversal of current through the head, under these two condition, will produce the reversal of flux in the head necessary to write data on the stripe.

WRITE MONITOR PULSE

During the write operation the static voltage at the junction of the two 1.6K resistors is approximately -30V. This voltage results from the DC current flow as shown in Figures IV 3 and 4. Since the head contain a coil and magnetic material it is an inductive device. The impedence, inductance and resistance, of the head will appear as a large resistance during the changes of head current due to the setting and resetting of FF9X. Since the head is in series with one of the 1.6K resistors and this combination is in parallel with the other 1.6K resistor there will be a change in the voltage at the junction of the two 1.6K resistors. This voltage change is aided by the spike induced in the coil by the changing magnetic field of the head. The voltage change at the junction of the 1.6K resistors is approximately 15 volts (-30V to -45V). The duration of the voltage is the length of time required for the current in the head to reach maximum in the new direction.

WRITE AMP AND MONITOR CARD

Figure IV-5 shows a block diagram and pulse chart for the write amp and monitor card. The inputs at pins 12 and 17 of the Write Amp and monitor card are controlled by the PWFF and FF9X or NOT FF9X signals. Since FF9X controls pin 12 and NOT FF9X controls pin 17 one of these pins will be high, OV, and the other will be low, -4V, at any given time while PWFF is set.

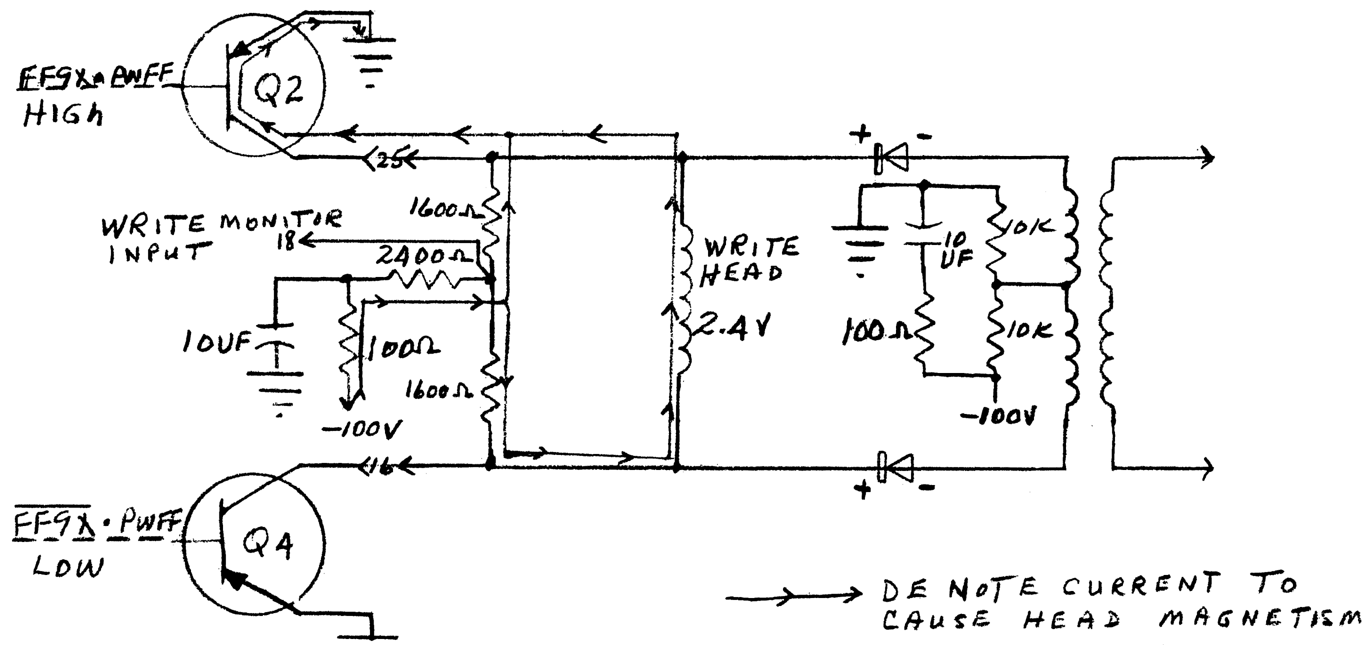


FIG IV-3

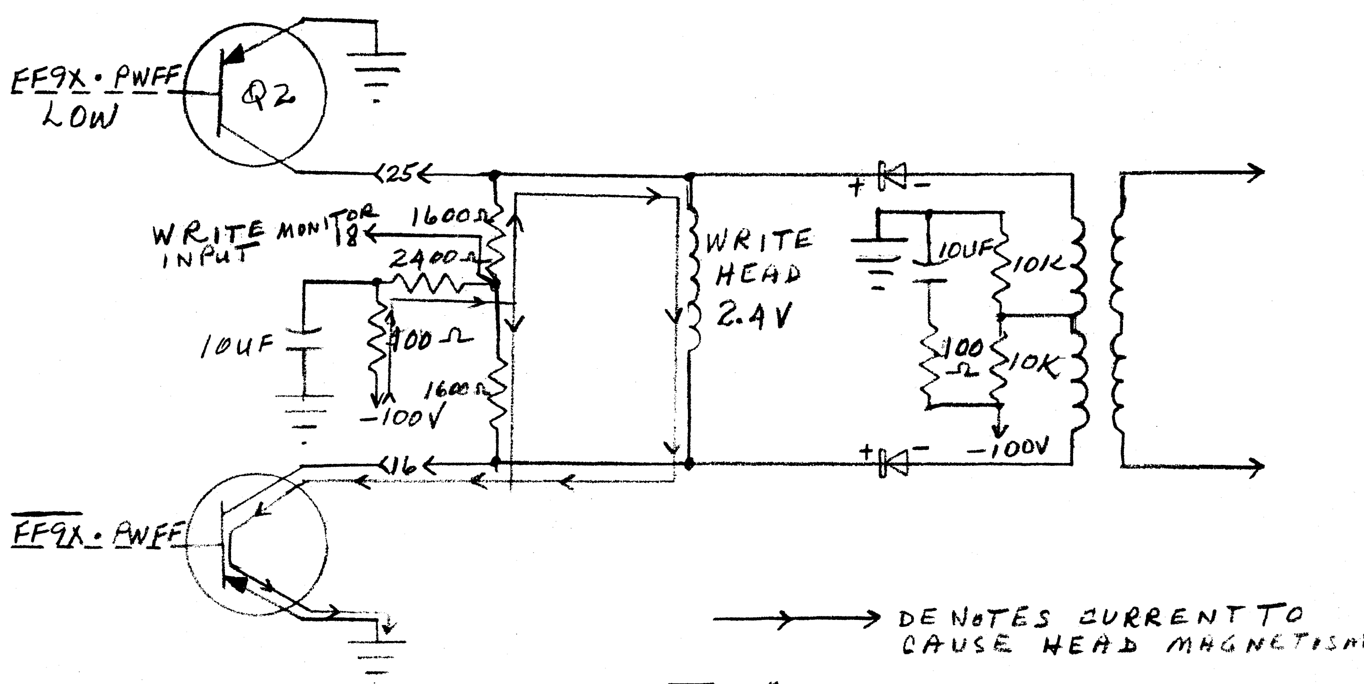
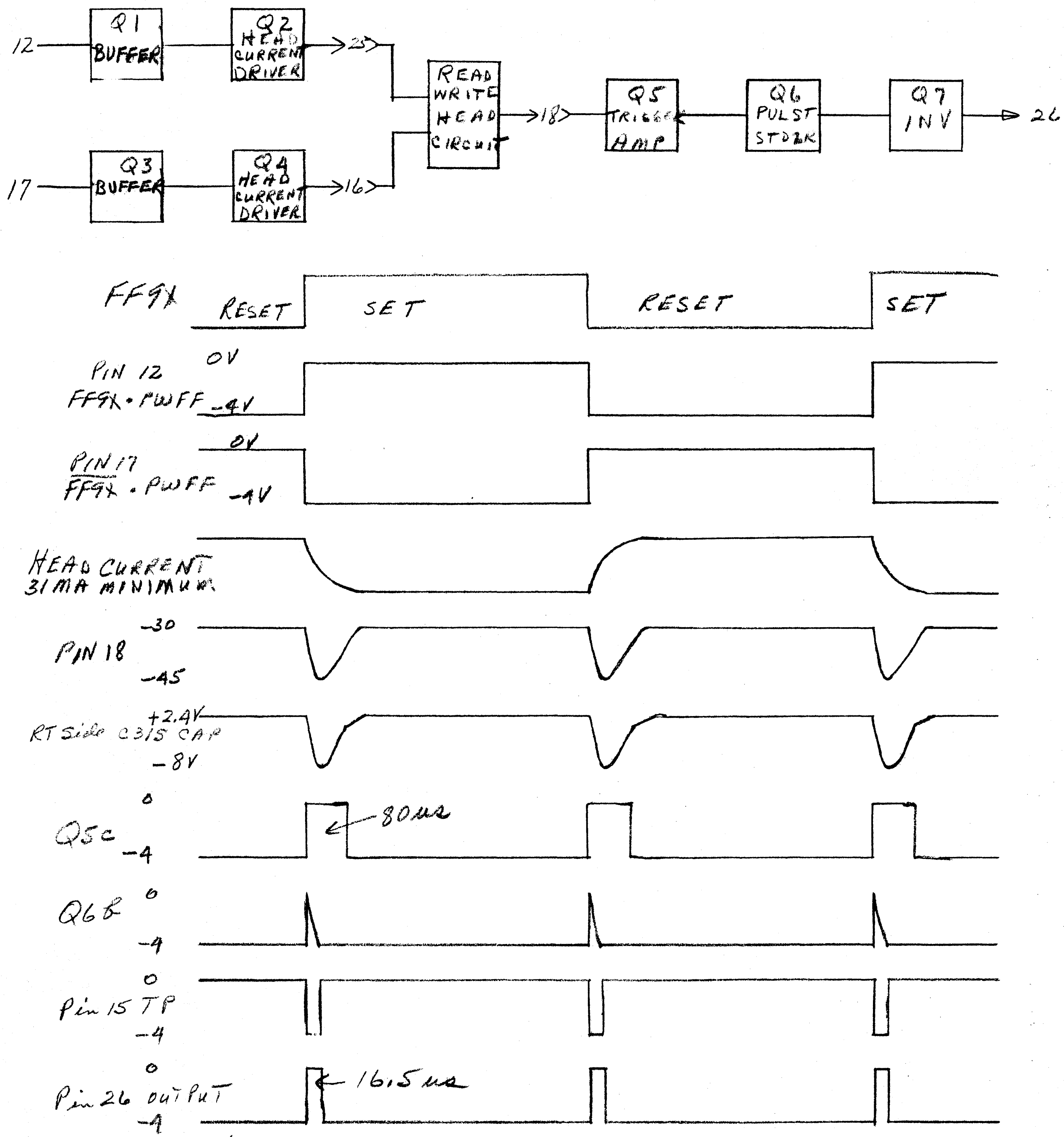


FIG IV-4



WRITE AMPLIFIER AND MONITOR BLOCK DIAG
AND SIGNAL CHART
FIG IV-5

The circuit diagram of the Write amplifier and monitor card is shown in Figure IV-6. Assume that FF9X is reset and pin 12 is at -4V. Current will flow from -4V of the input signal through resistors 10DD17 and LL16UU to +15V. Since these resistors have a 10 to 1 ratio a negative voltage appears at the base of Q1. Q1 will be on due to its emitter being at ground. Current will flow from ground through transistor Q1 and resistors S17Z and B13K to +15V establishing a positive voltage on the base of Q2. Q2 will be off since its emitter is at ground. Pin 25 is effectively an open circuit and no current flows through the head from this source.

With FF9X reset, NOT FF9X will be at 0V and cause pin 17 to be high, current will flow from ground at pin 17 through resistors CC37LL and LL35UU to +15V. The base of Q3 will be positive and Q3 will be off. The resistance network KK32TT, DD28MM and LL35UU establishes a negative voltage at the base of Q4. Q4 will be on. Current will flow from -100V through the 100 ohm, 2.4K resistors, a parallel circuit consisting of the lower 1.6K resistor and the upper 1.6K resistor and the head in series, pin 16, Q4 to ground. This circuit provides quantity and direction of current in the head to encode the stripe.

If the FF9X is now set the voltage at pins 12 and 17 will be reversed. Q3 will be on and Q4 off, which is effectively an open circuit at Q4. Q1 will be off and Q2 will be on providing a ground for the head circuit.

Current will now flow from -100V through the 100 ohm resistor, the 2.4K resistor the upper 1.6K resistor which is in parallel with the lower 1.6K resistor and the head in series, pin 25 and Q2 to ground. This circuit provides the quantity and direction of current in the head necessary to encode the stripe in the opposite direction to that discribed in the previous paragraph. Q1 and Q3 are buffer circuits that provide the driving current for the high voltage transistors Q2 and Q4. Q3 and Q4 provide the writing current for the head.

WRITE MONITOR CIRCUIT

The 15V pulse (-30V to -45V) developed by the head circuit when the current in the head is switched is applied to pin 18 of the write amplifier and monitor card. The duration of the pulse at pin 18 will be the length of time the current is changing in the head (80 to 100 usec.)

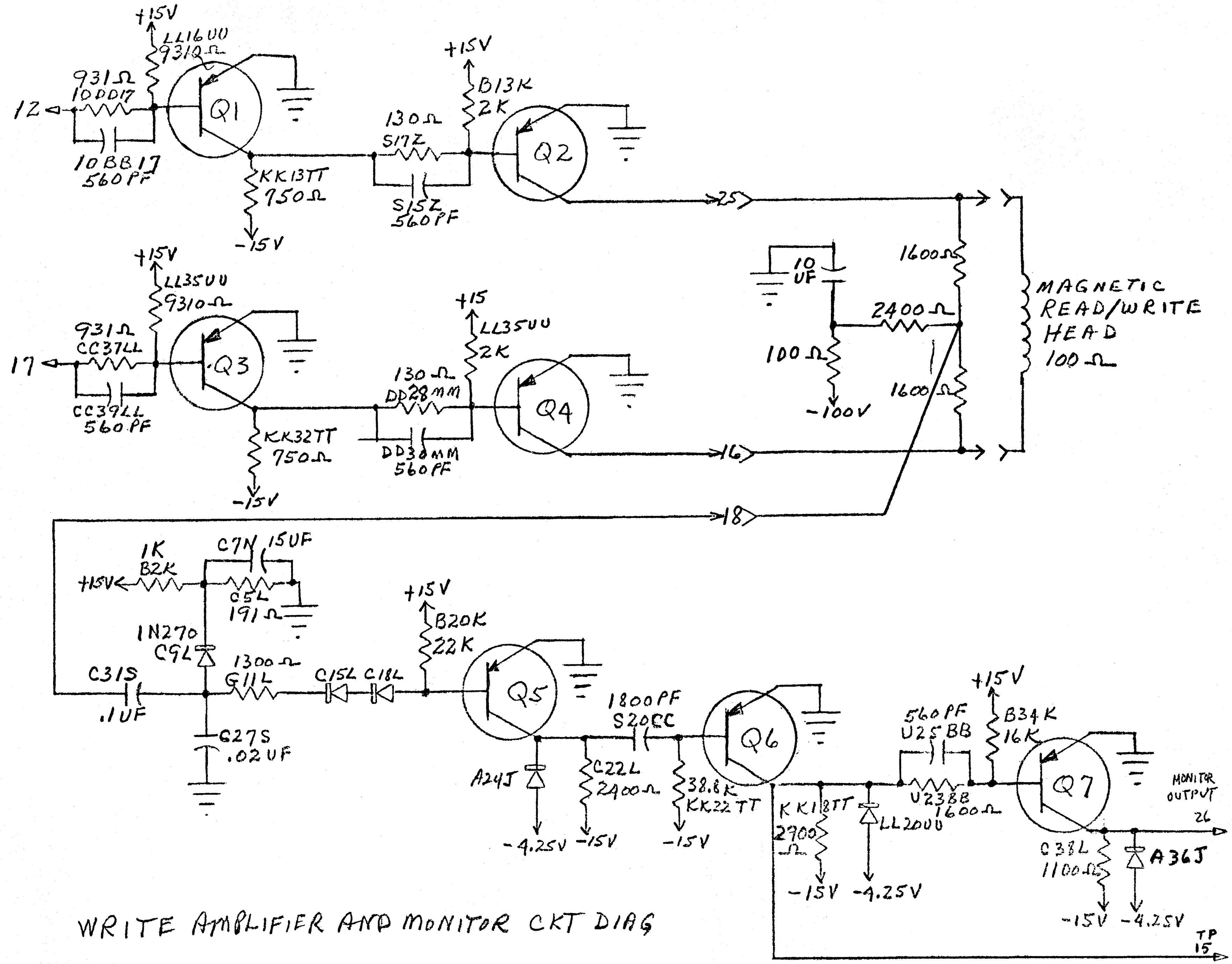
At static conditions the left side of capacitor C31S is approximately -30V. The right side of the capacitor is approximately +2.4V. The 2.4V is provided by the voltage divider network consisting of Resistors C5L, B2K, G11L and B20K and diodes C9L, C15L and C18L. Capacitor C7N stabilizes the voltage on the left side of capacitor C31S and prevents power supply variations affecting the circuit. The voltage divider network also provides approximately +3.6 at the base of Q5. This is a threshold voltage which must be overcome before an output pulse can be obtained. The circuit is immune to noise below approximately 3.6V. Since the head is an inductive device there is a tendency to ring during the switching of current.

Capacitor C27S suppresses this effect and improves the leading edge of the pulse to the base of Q5.

When the current in the head is switched in either direction a negative pulse from -30V to -45V will appear at the left plate of capacitor C31S. This will cause the right plate to go from +2.4V to -12.6V. The negative swing will cause Q5 to be turned on and the base will remain slightly below ground until capacitor C31S is discharged through resistor G11L, diodes C15L and C18L and Q5. During the pulse, diode C9L is reverse biased to prevent capacitor C31S discharging through the bias resistor circuit. Capacitor C31S and resistor G11L provide the RC time (approximately 80 us) that Q5 will be on. C15L and C18L are level shifting diodes.

The static voltages at capacitor S20CC are -4V on the left side and 0 on the right. The -4V is supplied by the clamp circuit, resistor C22L and diode A24J and the fact that Q5 is off. Q6 is on due to -15V through resistor KK22TT. The base of Q6 will be slightly below ground. Current flow from ground through Q6, resistor U23BB and resistor B34K to +15V, causes the base of Q7 to be positive and Q7 to be off. Clamp resistor C38L and diode A36J provides -4V at output at pin 26.

When the negative pulse from the head causes Q5 to turn on, the left side of capacitor S20CC will go from -4V to ground. The positive voltage swing on the right plate of the capacitor will cause Q6 to turn off.



WRITE AMPLIFIER AND MONITOR CKT DIAG

FIG IV-6

Q6 will remain off until capacitor S20CC discharges through resistor KK22TT to slightly below ground. This RC time is 16.5 us and determines the length of the pulse at pins 15 and 26. When Q6 is off - 4V from the resistor KK18TT and diode LL20UU through resistors U23BB and B34K provides a negative voltage at the base of Q7. Q7 will be turned on and ground through Q7 will be at pin 26.

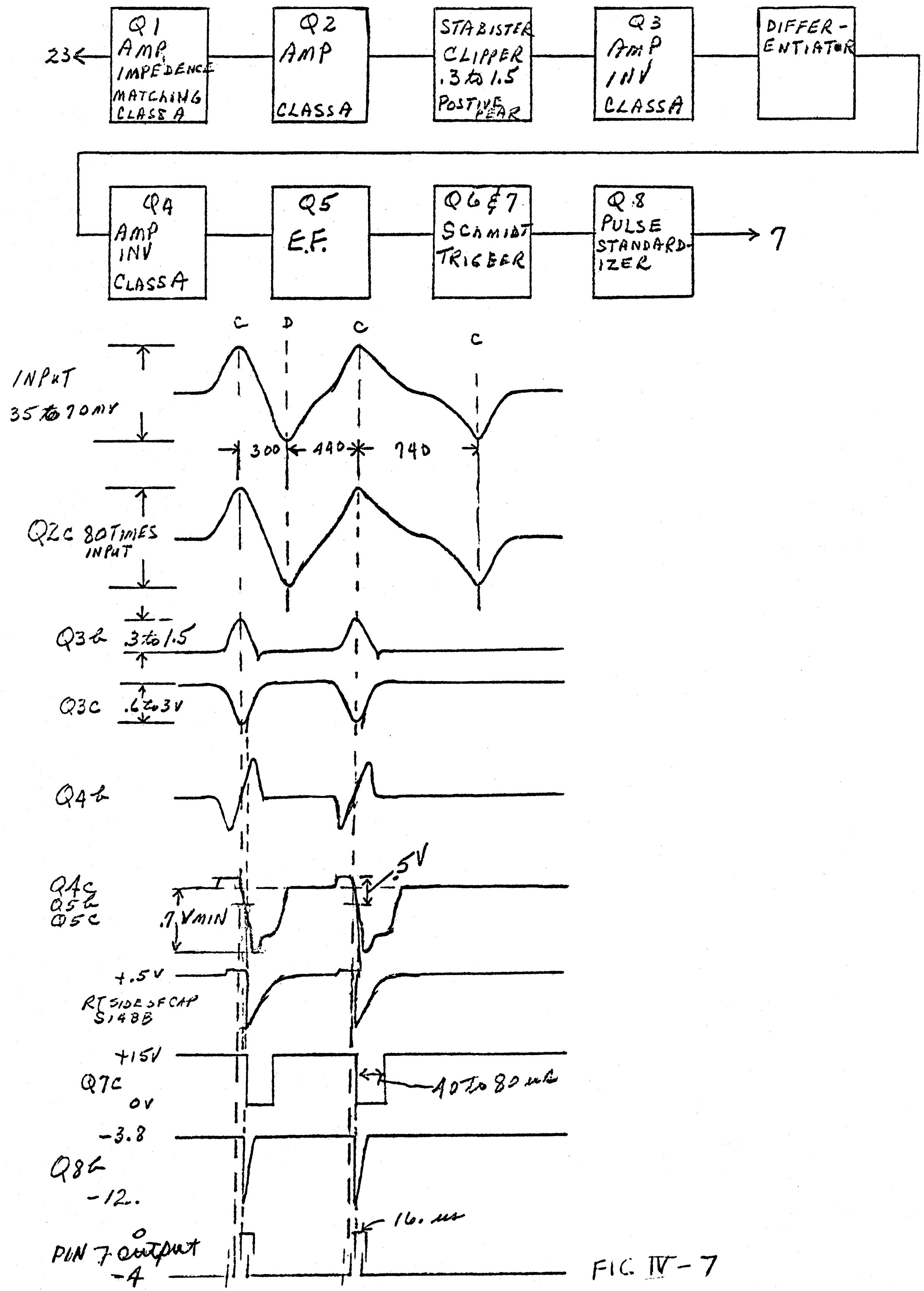
The output, at pin 26, will be a 16.5 us pulse from -4V to ground for each reversal of current through the head. The trailing edge of the monitor pulse occurs 16.5 us after the setting or resetting of FF9 which caused the change in head current. The use of the monitor pulse will be discussed in the monitor error circuits in Section V.

READ AMPLIFIER

The Read Amplifiers (one amplifier for positive pulses and one for negative pulses which are inverted by the transformer, from each head) operate on the frequency modulation principle for the detection of data and complement pulses. Figure IV-7 shows a block diagram of the amplifier and some of the wave forms associated with the amplifier. Figure IV-8 shows the circuit diagram of an amplifier. +13V and -13V are developed on these cards for use on the card by using a 51 ohm resistor and 13V zener diode. 15UF capacitors are used as filters with the +13V, -13V and -4 voltages. The 13V supplies are used here to remove any ripple or noise that may be on the 15V lines.

Quiescent DC Voltages

The first stage, Q1, is primarily an impedence matching stage.



23
Q1 AMP IMPEDENCE MATCHING CLASS A
Q2 AMP CLASS A
STABISTER CLIPPER .3 to 1.5 POSTIVE PEAK
Q3 AMP INV CLASS A
DIFFERENTIATOR
Q4 AMP INV CLASS A
Q5 E.F.
Q6 & 7 SCHMIDT TRIGGER
Q8 PULSE STANDARDIZER
7
C
D
C
C
INPUT 35 to 70 MV
300
440
740
Q2c 80 TIMES INPUT
Q3b .3 to 1.5
Q3c .6 to 3 V
Q4b
Q4c Q5b Q5c
.5 V
.7 V MIN
+.5 V
RT SIDE OF CAP S148B
+15 V
Q7c
0 V
40 to 80 us
-3.8
Q8b
-12.
16. us
PIN 7 output
-4

FIG. IV - 7

It operates as a class A amplifier and has a gain of approximately two. Resistors C24L and D31M provide a bias voltage of +4.3V for the stage. Base current through resistor D35M reduces the bias voltage to +1.1V at the base of Q1. Capacitor C26L is a noise filter. Capacitor D33M provides positive feedback for the circuit. Emitter resistor C22L provides the feedback voltage for capacitor D33M. The emitter DC voltage of Q1 is approximately +.4V and the collector DC voltage is approximately 4.4V.

Resistor FF19PP provides -3VDC bias at the base of Q2. Resistor 23NN30 provides shunt feedback for circuit stability. Adjustable resistor 34FF41 enables a class A gain of eighty in the first two stages.

NOTE: Resistor 34FF41 should never be turned to the ground position. If this is necessary to obtain a gain of eighty the resistor should be turned back at least 1/2 turn, sacraficing some gain. Capacitor 30KK39 provides signal bypass of the unused part of the adjustable resistor. Resistor EE21NN is the load resistor for Q2.

Capacitors CC28LL and 21N28 provide AC coupling for the clipper thyrector V28AA which clips .3 to 1.5V from the positive peaks of the signal. The AC coupling makes the clipper operate independently of DC voltage drifts in Q2 and Q3 due to temperature changes.

The thyrector was chosen for the clipper because of its .7V drop when forward biased. Its reverse biased operation is the some as any diode. Resistors 34W41, 34BB41 and C29L provide the clipping level. Resistor 34W41 provides for adjusting the clipping level, however, for machines of early construction this adjustment should be set for ground potential on the moveable contact.

When more sensitive heads are avilable an appropriate adjustment of resistor 34W41 will be necessary.

Stage Q3 is a class A invertor amplifier. The signal inversion is the primary function but a gain of two is also accomplished. Resistor C20L provides a bias voltage of -3.6V. Resistor R26Y provides shunt feedback for circuit stability. Resistors D18M and D14M are emitter resistors which provide emitter feedback. Capacitor E16R provides signal bypass of the D18M resistor. DC voltage at the emitter of Q3 is approximately -3.4V. DC voltage at the collector is approximately -9.6V. Resistor V20CC is the load resistor for Q3.

The DC voltage at the base of Q4 is -10.6V and the DC voltage on the emitter is -11V, therefore, Q4 will be on and biased for class A operation. -4.5VDC appears at the collector of Q4 and the base of Q5. Q5 is an emitter follower and the emitter will be slightly less negative than the base (approximately -4.3V). This is the static voltage on the left side of capacitor S14BB. The right side of capacitor S14BB is at approximately +.5V due to current through resistors A8J, B12K, Q6 and resistor D6M.

+.2V appear at the emitters of Q6 and Q7 and at the collector of Q6. Current from -15V through resistors B4K and 5R12 to .2V at the collector of Q6 provide +.03V for the base of Q7. Q7 will be off and +15V will be at the left plate of capacitor S2CC and at the lower plate of V11CC. Q8 will on since the base is positive with respect to the emitter. The base of Q8 and the left side of the capacitor S2CC will be at -3.8V. The output at pin 7 will be at -4V.

Signal Levels and Operation of the Read Amplifier

A head signal between 35 and 70 mv peak to peak is acceptable, however, a 50 mv signal is very desirable and will be assumed in this discussion. The signal from the head is applied to pin 23 and transmitted to the first stage, Q1, through capacitor D37P. Q1 has a gain of two and the signal at the collector of Q1 will be an exact replica of the input signal except it will be 100 mv peak to peak. This signal is applied to Q2 through capacitor X30HH. Q2 is a class A amplifier and has an adjustable gain of forty to one. The signal at the collector of Q2 is an exact replica of the input signal except that it is approximately eighty times as great or approximately 4V peak to peak. The 4V signal at the collector of Q2 is applied to the clipper thyrector V28AA through capacitor CC28LL. The right side of capacitor CC28LL is at ground and the thyrector will start to conduct when the voltage on its anode has reached +.7V.

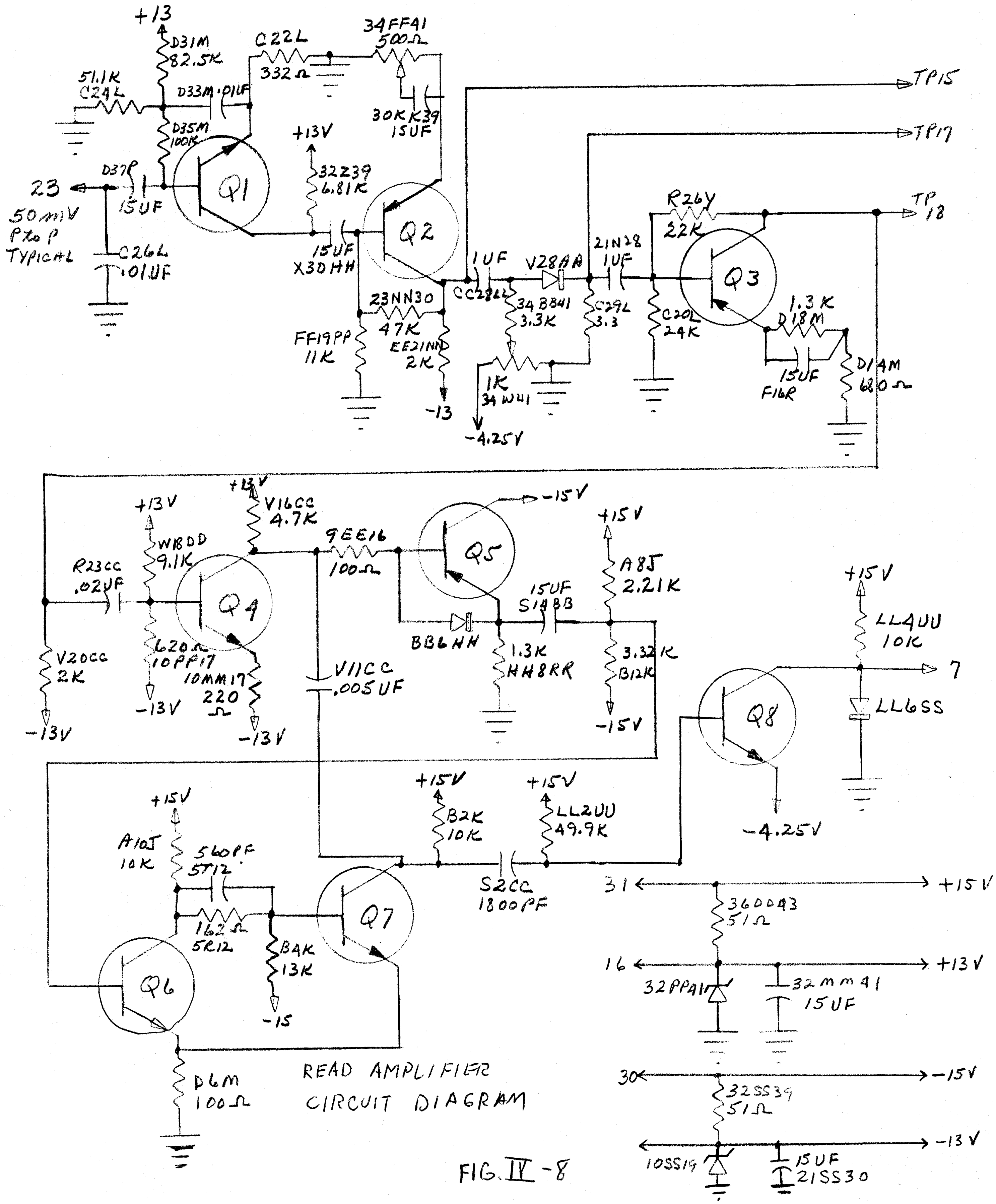
All of the positive signal above this voltage will appear through capacitor 21N28 at the base of Q3. If a 4 volt signal is applied, the clipped voltage at the base of Q3 will be 1.3V (2V less .7V). The signal at pin 17 should be an exact replica of the positive peaks of the input signal and should be between .3 and 1.5V in amplitude. If the signal at pin 17 is greater than 1.5V, resistor 34W41 should be adjusted. The reason for the 1.5V limit is to prevent distortion of the signal in Q3.

The signal at the collector of Q3 will be inverted in respect to the base signal and should be twice the amplitude (.6 to 3V).

The negative pulse at the Q3C Figure IV-8 is differentiated by capacitor R23CC and resistors W18DD and 10PP17. The values of these components are such that the signal on the base of Q4 is almost a sine wave. The signal passes through zero at the center of the input signal at TP18 or at the positive peak of the head signal. Q4 is a class A amplifier Inverter. The first half of the signal at the collector of Q4 is a true representation of the input signal on the base. The second half is distorted by the action of capacitor V11CC. Capacitor V11CC is a feedback circuit from the schmidt trigger (Q6 and Q7) and prevents double triggering the schmidt trigger from noise which might cause two output pulses at pin 7. Q5 is an emitter follower used to furnish driving current for the schmidt trigger. As the signal at the emitter of Q5 goes positive, the right side of capacitor S14BB is driven positive also.

Since Q6 is on, a low resistance path through resistor D6M discharges capacitor S14BB rapidly and the voltage on the right side of the capacitor rises very little above +.5V. On the second half of the signal the emitter signal swings negative. This negative voltage through capacitor S14BB causes Q6 to turn off and forces S14BB to discharge through resistors A8J and B12K. This RC time, which is 40 to 80 us, determines the length of the schmidt trigger pulse. When Q6 is turned off, current flow through resistors B4K, 5R12 and A10J will cause a positive voltage to appear on the base of Q7 which will turn Q7 on. The voltage at the collector of Q7 drops from +15V to very rear ground. This voltage change keeps Q5 low through capacitor V11CC and causes the right side of capacitor S2CC to go to approximately -11V. This turns Q8 off and allows resistor LL2UU and diode LL6SS to provide a high output at pin 7. The high output at pin 7 will last until capacitor S2CC discharges through resistor LL2UU this will be 16 us. When capacitor S14BB has discharged and the right side has become positive Q6 will again come on and will in turn cause Q7 to go off due to current through the voltage divider B4K and 5R12 to +.2V at Q6C.

One -4 to 0 pulse of 16 us duration has been produced whose leading edge concides with the positive peak of the head signal. The negative pulses produced by the head are inverted to positive pulses by the center tapped transformer secondary.



READ AMPLIFIER CIRCUIT DIAGRAM

FIG. IV-8

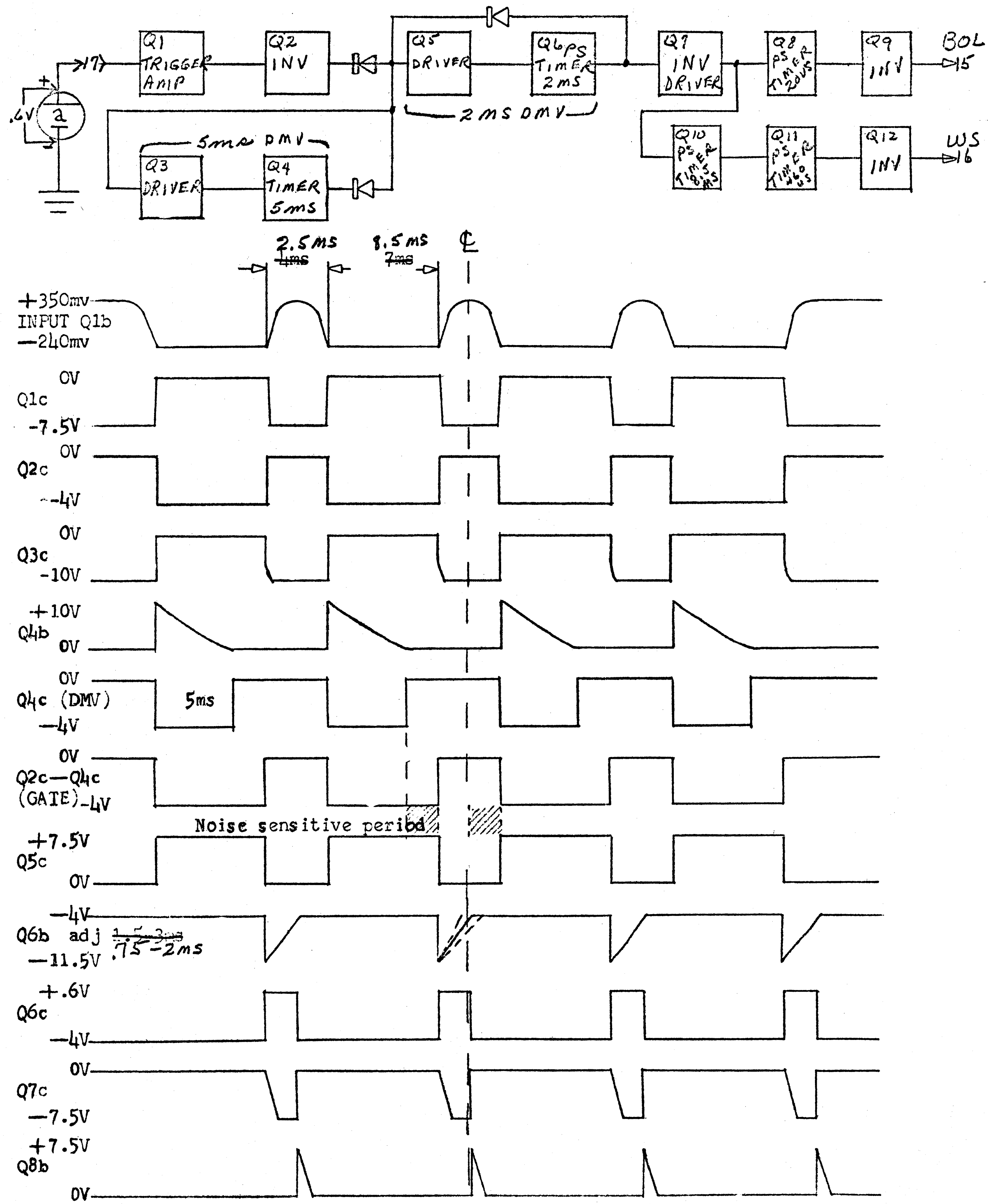
These pulses operate another Read amplifier. The outputs from the two amplifiers are gated together. The output from the gate is a 16 us pulse for each pulse, positive and negative, produced by the head.

Beam of Light (BOL) Line Counter

During paper handling operations some method of detecting the location of the form during its travel into and out of the carriage is needed. The method chosen was the counting of lines. To accomplish this a disc which contains evenly spaced holes is mounted on the paper drive shaft just in front of the paper drive clutch. The disc contains 10 holes and the distance between each hole and its adjacent holes corresponds to one line (1/6") of form travel. The disc is mounted between a solar cell and a light bulb. As the disc rotates the beam of light from the light bulb to the solar cell is interrupted by the disc. When the paper drive clutch is disengaged a hole in the disc is aligned with the bulb and solar cell. The signals generated by the solar cell, as the disc rotates, trigger an electronic circuit which indicate form movement and/or location of the form in the machine.

BOL Amplifier

The BOL amplifier is designed to produce two pulses from the leading edge of a hole in the disc. Since a hole in the disc is aligned with the solar cell at normal, the first pulse produced by the BOL amplifier will occur when the disc has moved to the next hole (1 space of the form).



Q1 TRIGGER AMP
Q2 INV
Q5 DRIVER
Q6 PS TIMER 2ms
Q7 INV DRIVER
Q8 PS TIMER 20us
Q9 INV
BOL 15
2ms DMV
5ms DMV
Q3 DRIVER
Q4 TIMER 5ms
Q10 PS TIMER 1.8ms
Q11 PS TIMER 460us
Q12 INV
WS 16
17
.6V
a
2.5ms
~~4ms~~
8.5ms
~~7ms~~
℄
+350mv
INPUT Q1b
—240mv
0V
Q1c
-7.5V
0V
Q2c
-4V
0V
Q3c
-10V
+10V
Q4b
0V
0V
Q4c (DMV)
5ms
—4V
0V
Q2c—Q4c
(GATE) -4V
Noise sensitive period
+7.5V
Q5c
0V
—4V
Q6b adj ~~1.5-3ms~~ .75-2ms
—11.5V
+.6V
Q6c
—4V
0V
Q7c
—7.5V
+7.5V
Q8b
0V

FIG ~~IV~~ -9A

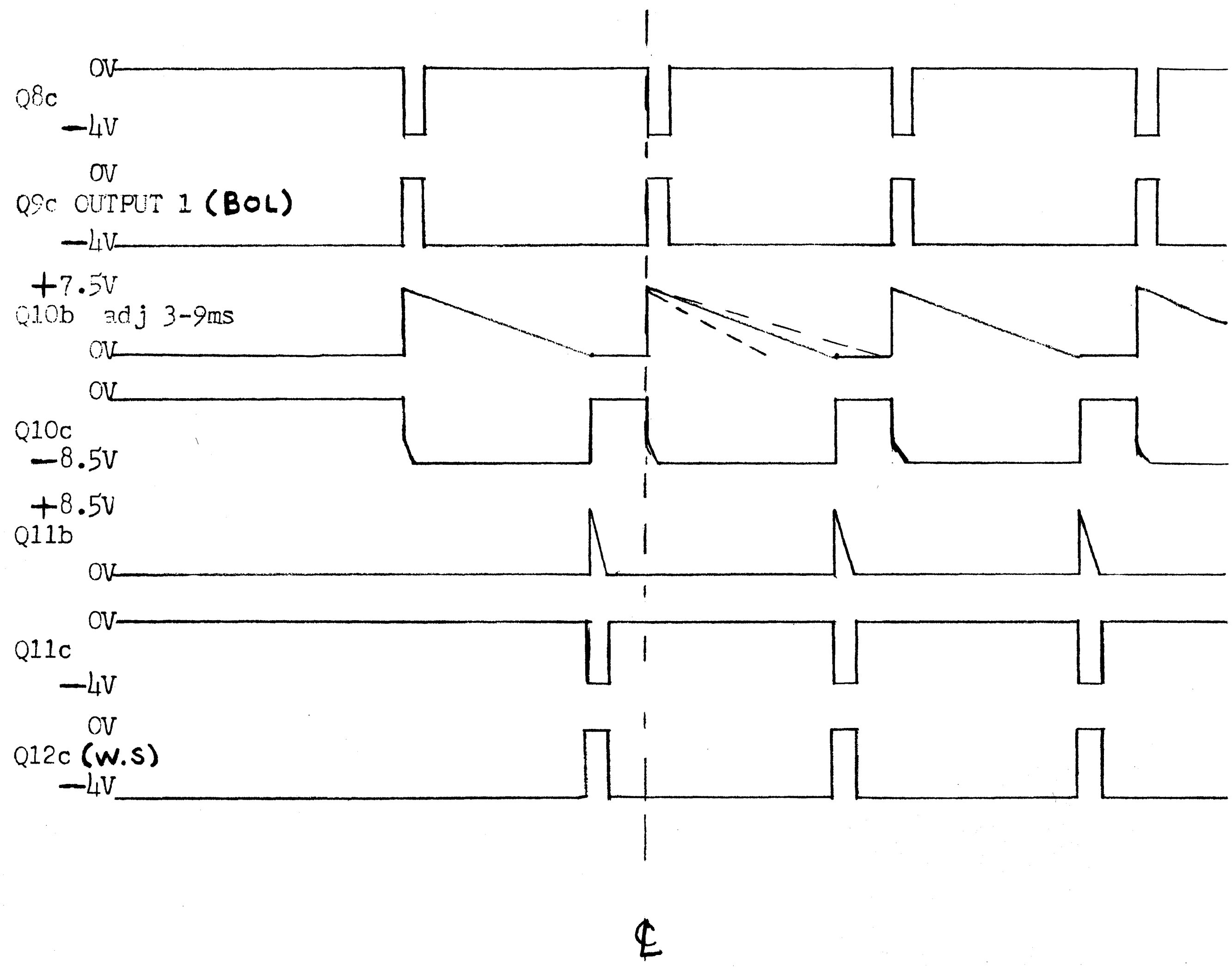

OV
Q8c
−4V
OV
Q9c OUTPUT 1 (BOL)
−4V
+7.5V
Q10b adj 3-9ms
OV
OV
Q10c
−8.5V
+8.5V
Q11b
OV
OV
Q11c
−4V
OV
Q12c (W.S)
−4V
℄

FIG. IV - 9B

Two separate pulses are produced by the BOL amplifier circuit. The BOL pulse is a 20 μs pulse which is timed to start at the center of the hole. The write Sync (WS) pulse is a 460 μs pulse which occurs 8.5 to 9 ms after the center of the hole. Each of these pulses occur at a frequency of 11.1 ms which is the time required to move the form one space. The holes in the disc are of such size that the light reaches the solar cell approximately 2.5 ms and the light is blocked approximately 8.5 ms. BOL and WS pulses are the standard -4V to 0 signals used throughout the machine.

BLOCK DIAGRAM AND PULSE CHART

Figure IV-9A and B shows a back diagram of the BOL Card and typical signal for various points on the card. Q1 is a trigger circuit for the BOL card. Q2 inverts the signal and furnishes driving current for Q3 and Q5. Q3 and Q4 form a 5 ms DMV. The purpose of this DMV is to guard against triggering a BOL and WS pulse due to the clutch bouncing as the teeth of the clutch engage to start the paper drive. This delay is initiated by the trailing edge of the hole. Q5 and Q6 form a 1.25 DMV. This DMV is initiated by the leading edge of the hole and its purpose is to provide a BOL pulse which starts in the center of the hole. Q7 is an inverter which drives pulse standardizers Q8 and Q10. Q8 provides the time duration for the BOL pulse. The 20 μs pulse will insure a good clock pulse for gating purposes. Q9 inverts the pulse and provides driving current for the BOL signal in the machine.

Q10 is a pulse standardizer which provides an 8.5 ms delay, from the center of the hole, for the start of the WS pulse. Q11 is a pulse standardizer which provides a 460 μs WS pulse. The 460 μs pulse will insure a good USMV pulse for gating. Q12 is an inverter and provides driving current for the WS signal in the machine.

BOL/WS Circuit Quiscent Conditions

The voltage established on the base of Q1 by the solar cell, resistor C3L and B5K is +.35V. This is positive in respect to the emitter and Q1 will be off. Resistors C1L, D8M and B12K will cause a negative voltage at the base of Q2. Q2 will be on and its base will be held very near ground. Resistors C1L and D8M will cause the collector of Q1 to be approximately -7.5V.

Current from ground through Q2, resistors V13LL and LL9UU to +15V will provide a positive voltage at the base of Q3. Since Q3 is PNP Q3 will be off. Current through resistors KK7TT and LL5UU provide approximately -10V for the left side of capacitor S10CC. The right side of 1BB11 will be near ground since Q4 will be on due to -15V through resistor LL3UU. Current from ground through Q2, resistor W15DD and JJ11SS to +15V will provide a positive voltage at the base of Q5. Since Q5 is NPN it will be on. The left side of capacitor T18DD will be near ground.

Current flow through Q6, resistors 32V39 and 35X42 will cause the base of Q6 and the right side of capacitor T18DD to be near -4V. -4V through Q6, resistors D2DM and A23L cause Q7 to be on. With Q7 on the voltage at the left side of capacitors S26CC and N22EE will be near ground. -15V through resistor KK29TT will cause Q8 to be on. The base of Q8 and the right side of capacitor S26CC will be near 0V. Current through Q8, resistors HH23RR and LL17UU to +15V will cause approximately +1.5V at the base of Q9 and Q9 will be off. Current through resistors KK21TT and diode NN19UU provide a -4V signal at pin 15 (BOL).

-15V through resistors 35MM42 and 33KK40 will cause Q10 to be on. The base of Q10 and the right side of capacitor N22EE will be near 0V. The left side of capacitor S30CC will also be near 0V. -15V through B31K will keep Q11 on. The base of Q11 and the right side of S30CC will be near 0V. Current through Q11, resistors 34P41 and D41M cause approximately +1.5V at the base of Q12. Q12 will be off and current from -15V through resistors C35L and diode A37F will provide a -4V signal at pin 16 (WS).

The BOL and WS Pulses

Approximately 1.25 ms after the driving member of the paper drive clutch has engaged the driven member the trailing edge of the hole in the disc will interrupt the light to the solar cell.

As the light to the solar cell is cut off the voltage developed by the cell will decrease. As the voltage on the base of Q1 goes negative Q1 is turned on at about -.17V. The base will continue in a negative direction to about -.24V. Current flow from ground through Q1, resistors D8M and B12K will cause +1.5V will appear at the base of Q2 turning Q2 off. -4V is established at the collector of Q2 by resistor B14K and diode E16L. Current flow -4V through diode M13T and resistors V13LL and LL9UU to +15V cause a negative voltage on the base of Q3 which turns Q3 on. The 4V positive swing at the collector of Q3 will appear through capacitor 1BB11 at the base of Q4. Q4 will be turned off by the +4V signal. With Q4 off, resistor JJ1SS and diode T8Y provide a -4V signal through diode T6Y, resistors V13LL and LL9UU to keep Q3 on. The 4V from Q4 through diodes T6Y and N15U, resistors D20M and A23L keep Q7 on to prevent any change in the BOL or WS signals. When Q2 was turned off the -4V from its collector clamp through diode M13T, resistors W15DD and JJ11SS to +15V caused a negative voltage at the base of Q5 to turn Q5 off. The voltage at the left plate of capacitor T18DD rises to +7.5V. A similar voltage change appears on the base of Q6 but since Q6 is already on no appreciable change takes place. The circuit remains in this state for 5 ms. this is the time required for capacitor 1BB11 to discharge through resistor LL3UU.

When the base of Q4 again becomes negative Q4 will turn on. The -4 clamp from resistor JJ1SS and diode T8Y is removed from Q3, Q5, and Q7. No changes occur since -4 from resistor B14K and diode E16L maintain the same state of Q3 and Q5 and -4 through Q6 maintains the state of Q7.

9 ms after the disc has started to rotate the leading edge of the first hole allows light to strike the solar cell again. As this occurs the voltage developed by the solar cell causes the voltage at the base of Q1 to again go positive. This will occur 2 ms before the form has moved 1 full space. (Spaces are measured from the center of one hole to the center of the next.) With Q1 on, current flow from ground through Q1, resistors D8M and B12K provide a positive voltage for the base of Q2 which turns Q2 on. Current now flows from ground through Q2, diode M13T, resistors V13LL and LL9UU to +15V. The positive voltage on the base of Q3 turns Q3 off. A 10 Volt negative swing occurs at the left side of capacitor 1BB11. This voltage also appears on the base of Q4 but since Q4 is already on no significant change occurs. Current from ground through Q2, diode M13T, resistors W15DD and JJ11SS to +15V provides a positive voltage on the base of Q5 to turn Q5 on. With Q5 on a negative 7.5V voltage swing appears on the left plate of capacitor T18DD. This 7.5V swing causes the voltage at the base Q6 to go to -11.5V which turn Q6 off.

With Q6 off current flows from ground through Q4, diodes T6Y and N15U, resistors D20M and A23L to +15V. This establishes approximately +.6 at the base of Q7. Q7 is turned off. Resistor C25L and B27K provide a 7.5V negative swing for capacitors S26CC and N22EE.

Resistor 35X42 should be adjusted so that capacitor T18DD discharges to -4V, through resistors 32V39 and 35X42, in 1.25 ms. At this time the form will have moved one full space and the center of the hole in the disc will be aligned with the solar cell. When the base of Q6 becomes positive in respect to the emitter of Q6, Q6 will turn on. Current then flows from -4.25V through Q6, resistors D20M and A23L to establish a negative voltage at the base of Q7. Q7 will turn on and current flows from ground through Q7 and resistor B27K to -15V. This causes a positive 7.5V swing on the left side of capacitors S26CC and N22EE. The positive change on the right plate of capacitor S26CC causes Q8 to turn off. Current flows from the -4V clamp made up of resistor KK27TT and diode NN31UU through resistors HH23RR and LL17UU establishing a negative voltage at the base of Q9. Q9 is turned on and ground through Q9 appears at pin 15 which is the leading edge of the BOL Pulse. The duration of the Pulse which is about 20 μs is determined by the discharge of capacitor S26CC through resistor KK29TT. When the right side of capacitor S26CC has become negative Q8 will again come on.

Current from ground through Q8, resistor HH23RR and LL17UU establishes a positive voltage on the base of Q9 which turns Q9 off. Clamp resistor KK21TT and diode NN19UU provides -4V at pin 15. This is the trailing edge of the BOL Pulse.

The positive 7.5V swing at capacitor N22EE causes Q10 to turn off. Current from -15V through resistors 35HH42 and 35EE42 causes an 8.5V negative swing on the base of Q11. Since Q11 is already on no appreciable change occurs. Resistor 35MM42 should be adjusted for 8.5 ms. discharge of capacitor N22EE through resistors 33NN40 and 35MM42. This provides the delay of the start of the WS pulse from the center of the hole. When the voltage on the base of Q10 becomes negative Q10 will turn on again. This will cause an 8.5V positive swing through capacitor S30CC. The positive swing turns Q11 off. Current from the -4V clamp resistor C33L and diode B39H through resistors 34P41 and D41M provides a negative voltage on the base of Q12 to turn Q12 on. Ground through Q12 appears at pin 16 and is the leading edge of the WS pulse. Capacitor S30CC will discharge through resistor B31K in approximately 460 μs. This is the duration of the WS Pulse.

When the base of Q11 becomes negative again Q11 will turn on. Current flow from ground through Q11, resistors 34P41 and D41M provides a positive voltage for the base of Q12.

Q12 turns off and the clamp resistor C35L and diode A37F provide -4V for pin 16. This is the trailing edge of the WS Pulse.

Capacitors N1W and D10M are noise filters, resistors C1L, B14K, LL13UU, B27K, KK7TT, JJ1SS, KK27TT, KK21TT, 35HH42, C33L and C35L are load resistors for this adjacent transistors as well as part of the clamp circuits already mentioned.

In review, then, the trailing edge of the hole in the disc has triggered a 5 ms guard period to protect against unwanted pulses due to chatter or bounce as the clutch is engaged. The leading edge of the hole has triggered a 20 µs BOL pulse whose leading edge coincides with the center of the hole. The trailing edge of the hole also triggers a 460 µs WS Pulse whose leading edge occurs 8.5 ms after the center of the hole.

B.O.L.A.

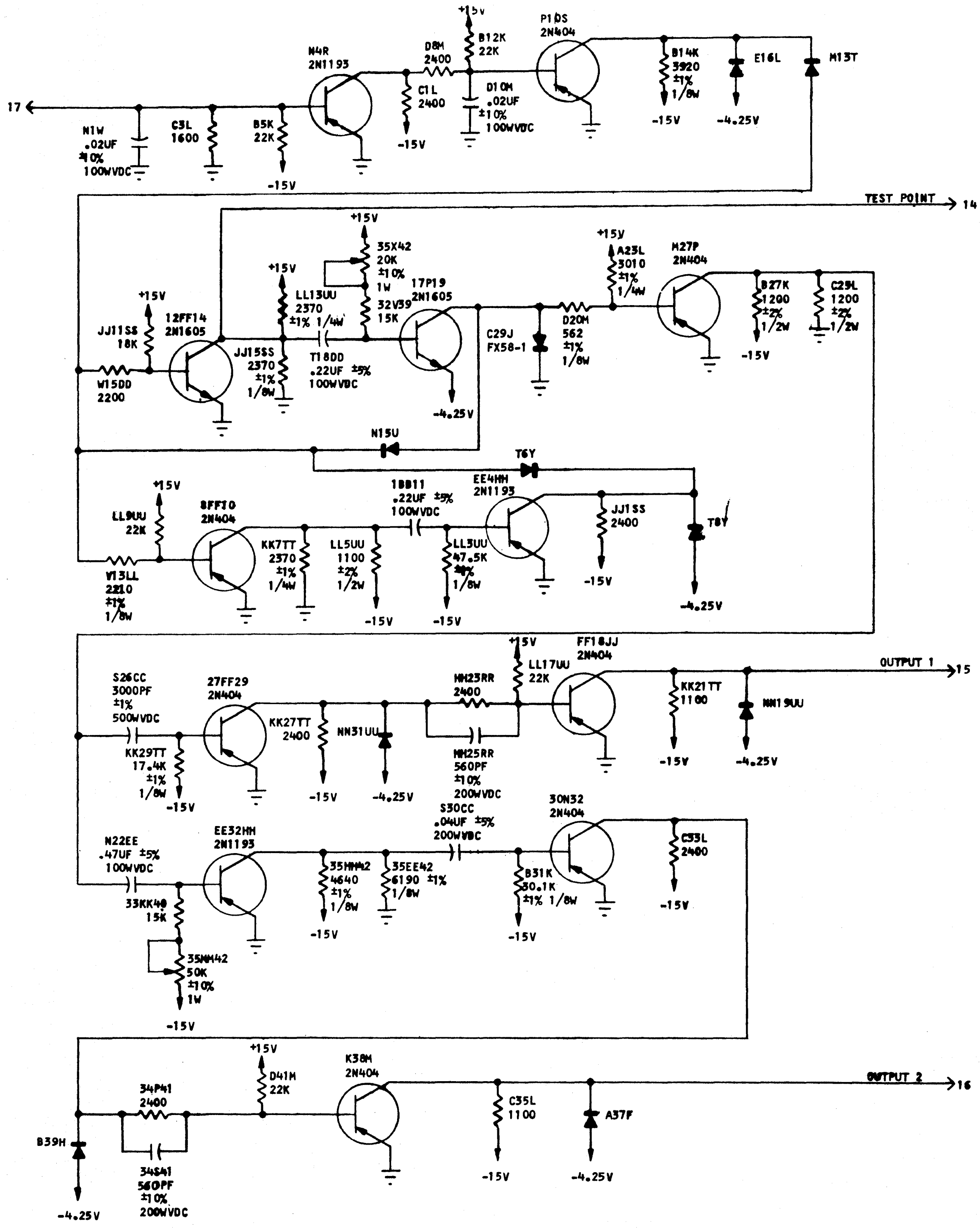


Fig. IV-10 # 1511 5108

PAPER DRIVE CLUTCH

The Paper Drive Clutch detent is moved to its engaged and disengaged positions by two solenoid coils. These coils are energized individually when the detent is to moved to its alternate position. The coils are picked with 120V to ensure positive movement of the detent. The 120V is applied for a period of approximately 30 ms. After that time the voltage is reduced to a hold voltage of 22V. These voltages are applied electronically by the circuits on the PDC card.

PDC Circuit

Figure IV-11 shows a block diagram and wave forms for the PDC circuit. Q1 is an emitter follower which furnishes driving current for Q2, Q4 and Q6. Q2 is an inverter which provides a 100V signal for Q3. Q3 is an power transistor used to energize and hold the PDC coil. Q4 is an inverter which controls Q5. Q5 is a 100V transistor which provides a shunt path around resistor P19AA when it is on. Q6 is the driver for the Pulse Standardizer. Q7 is a pulse standardizer which provides a 30 ms signal for Q8. Q8 is an emitter follower which provides driving current for Q2, Q4 and Q6 for 30 ms.

There are two of these circuits in the machine. One for the Paper Drive Solenoid and one for the Stop Paper Drive Solenoid. These circuits are controlled by the PDFF. One circuit being controlled by each output, PDFF and NOT PDFF. One of the solenoids will be energized at all times.

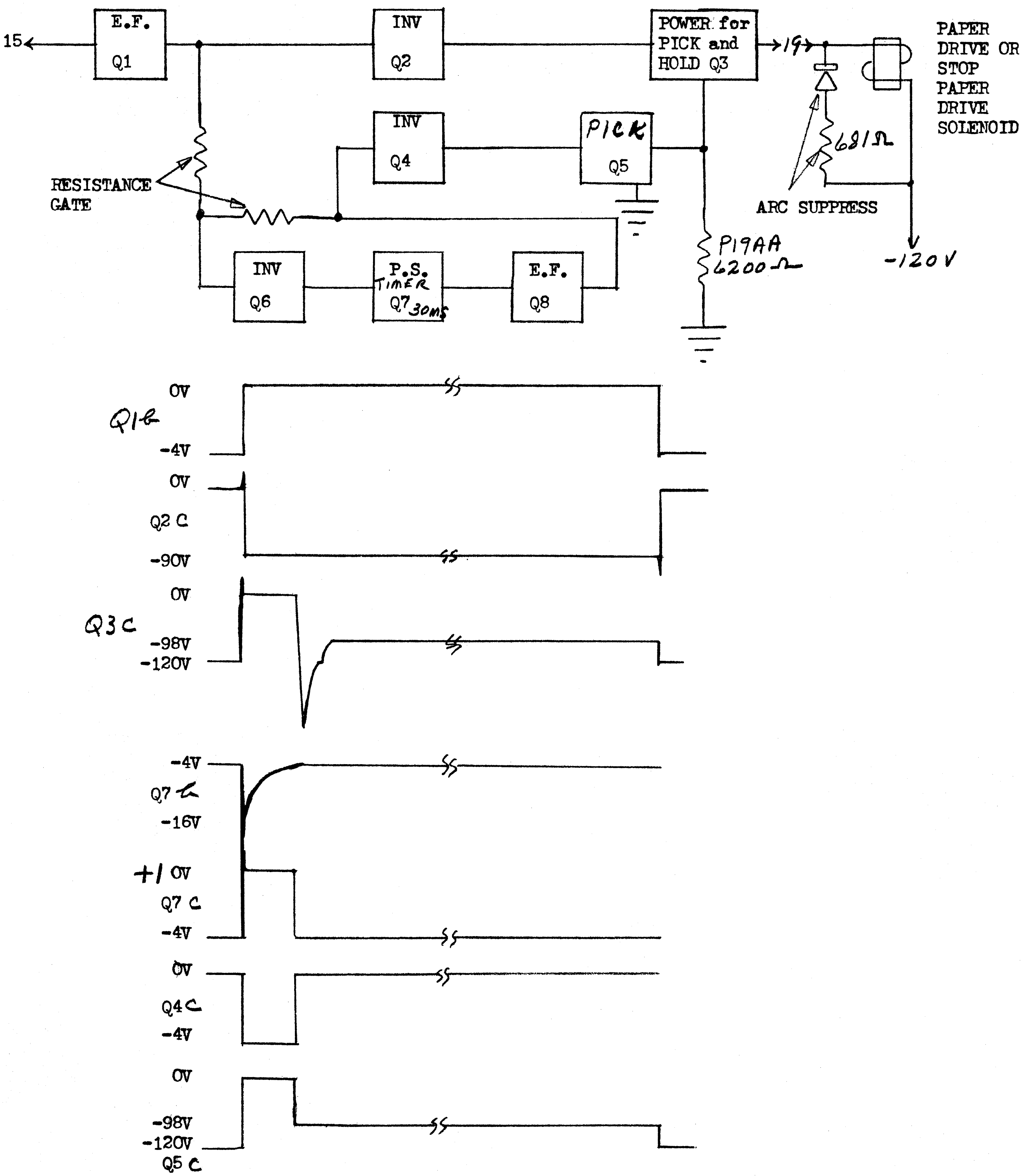

15
E.F.
Q1
INV
Q2
POWER for
PICK and
HOLD Q3
19
PAPER
DRIVE OR
STOP
PAPER
DRIVE
SOLENOID
INV
Q4
PICK
Q5
681Ω
RESISTANCE
GATE
ARC SUPPRESS
P19AA
6200Ω
-120V
INV
Q6
P.S.
TIMER
Q7
30MS
E.F.
Q8
0V
Q1 b
-4V
0V
Q2 C
-90V
0V
Q3 C
-98V
-120V
-4V
Q7 b
-16V
+1 0V
Q7 C
-4V
0V
Q4 C
-4V
0V
-98V
-120V
Q5 C

Figure IV-11

QUIESCENT STATE (Pin 15 low) Fig. IV-12

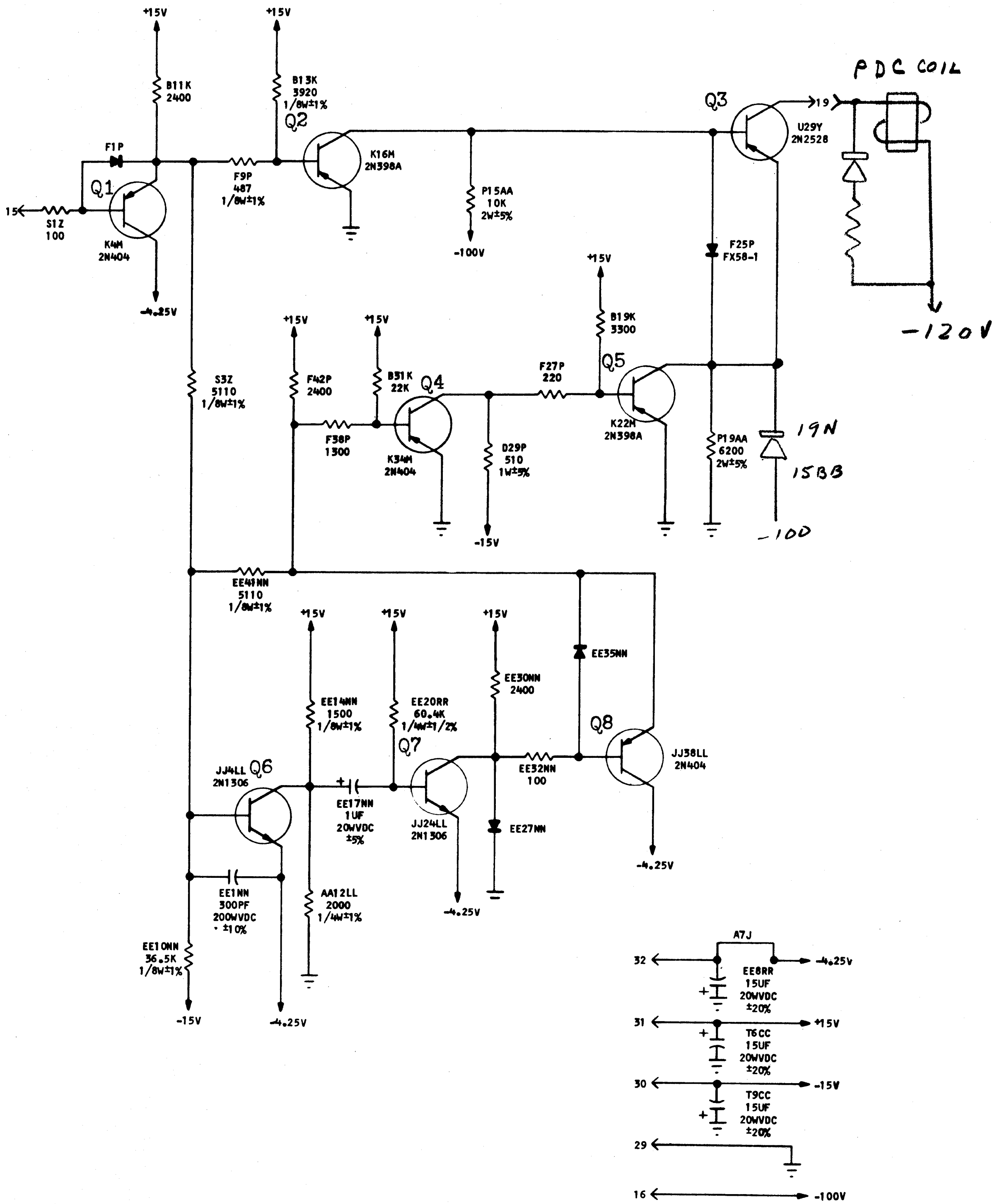
With the signal at pin 15 low the signal at the emitter of Q1 will also be low. Current flow from -4 through Q1, resistors F9P and B13K to +15V provides a negative voltage on the base of Q2. Q2 will be on and ground will be on the base of Q3. Current from -15V through resistors EE10NN and S3Z to -4V at the emitter of Q1 will provide a voltage something more negative than -4V at the base of Q6. Q6 will be off. Resistors AA12LL and EE14NN provide approximately +8.5V at the left plate of capacitor EE17NN. +15V through EE20RR will cause Q7 to be on. -4V will appear on the base of Q7 and the right plate of capacitor EE17NN. The base of Q8 is low and therefore the emitter will be low. Current from -4V through Q8, resistors F38P and B31K to +15V will provide a negative voltage for the base of Q4 which will turn on Q4. Current from ground through Q4, resistors F27P and B19K provides a positive voltage at the base of Q5 which keeps Q5 off. Q3 will also be off and the coil will not be energized.

When pin 15 becomes high the output at the emitter will also be high. Current flow from Pin 15 (ground through a transistor on the FF card), resistor S1Z, Q1, resistors F9P and B13K to +15V causing a positive voltage at the base of Q2 and Q2 will turn off. -100V will appear at the base of Q3.

Current from -15V through resistors EE10NN, S3Z, Q1, S1Z, and pin 15 to ground provides approximately -2V at the base of Q6. This turns Q6 on since its emitter is -4V. The voltage change at the left side of capacitor EE17NN is about 12V in the negative direction. The right side of the capacitor follows and Q7 is turned off. Ground through diode EE27NN and resistor EE32NN will cause the output from Q8 to become high. Current flow from ground through diode EE27NN, resistor EE32NN, Q8 resistors F38P and B31K to +15V provides a positive voltage at the base of Q4 to turn Q4 off. Current flow from -15V through resistors D29P, F27P and B19K provide a negative voltage at the base of Q5 to turn Q5 on. Current from ground, Q5, Q3, pin 19 and the PDC coil to -120V energizes the coil with pick current. The high signal from Q8 holdes Q6 on through resistor EE41NN.

After 30 ms, which is the discharge time of capacitor EE17NN through EE20RR, Q7 will be turned on. This will cause the output from Q7 to be low and subsequently the output from the emitter follower Q8 to be low. This low output through resistors F38P and B31K will turn Q4 on. Current flow from ground through Q4 and resistors F27P and B19K to +15V will cause a positive voltage at the base of Q5 and turn Q5 off. Current from ground through resistor P19AA, Q3, pin 19 and the PDC coil to -120V provides hold current for the coil. Voltage drop across P19AA is 98V therefore 22 volts will appear across the coil.

The low signal from Q8 through resistor EE41NN will turn Q6 off. With Q6 off the voltage on the left plate of capacitor will return to +8.5V. The positive voltage on the base of Q7 will have little effect since Q7 is already on. The diode and resistor across the coil provide arc suppression for the coil to limit the spike or overshoot of the coil due to current changes in the coil. Diode F25P prevents the base emitter junction of Q3 being damaged by the spikes induced by the coil. Diode 19N-15BB prevents excessive noise spikes at the collector of Q5.



NOTES:
FOR ASS'Y SEE 15115603

UNLESS OTHERWISE SPECIFIED:
RESISTANCE VALUES ARE IN OHMS ±5%, 1/2W
DIODES ARE BCX58-1

Figure IV-12

FRONT PAPER SWITCH

The Solar Cell and light bulb located in the throat of the carriage is known as the Front Paper Switch (FPS). When a ledger card is inserted into the Carriage, the Card interrupts the light to the solar cell. When the light illuminates the cell, the cell develops a voltage of about .2V. When the light is removed the voltage drops to OV.

Figure IV-13 shows a block diagram and waveforms for the circuit. Q1 is an inverter which provides driving current for the schmidt trigger, Q2 and Q3. Q4 is an emitter follower. Q7 is an emitter follower which provides driving current for the NOT FPS signal in the machine. Q5 is an inverter which provides the FPS signal. Q6 is an emitter follower which provides driving current for the FPS signal in the machine.

Figure IV-14 is the FPS circuit diagram.

When there is no form in the machine the light on the solar cell causes a voltage to be developed by the cell. This voltage through pin 9 and resistor FF1PP causes the base of Q1 to be negative which turns on Q1. Current flow from ground through Q1, resistors 2AA9 and LL5UU to +15V establishes approximately +3.5V at the base of Q2. Current from -15V through resistors KK7TT, 12AA19 and LL13UU to +15V establishes a negative voltage at the base of Q3. Q3 will be on and its emitter will be slightly positive (.5V) this will also be on the emitter of Q2 and Q2 will be off. With Q3 on its collector and the base of Q4 will be slightly positive. Q4 will be on and its emitter will be positive. This will turn Q7 on and ground thru Q7 to pin 18 will provide a high NOT FPS signal.

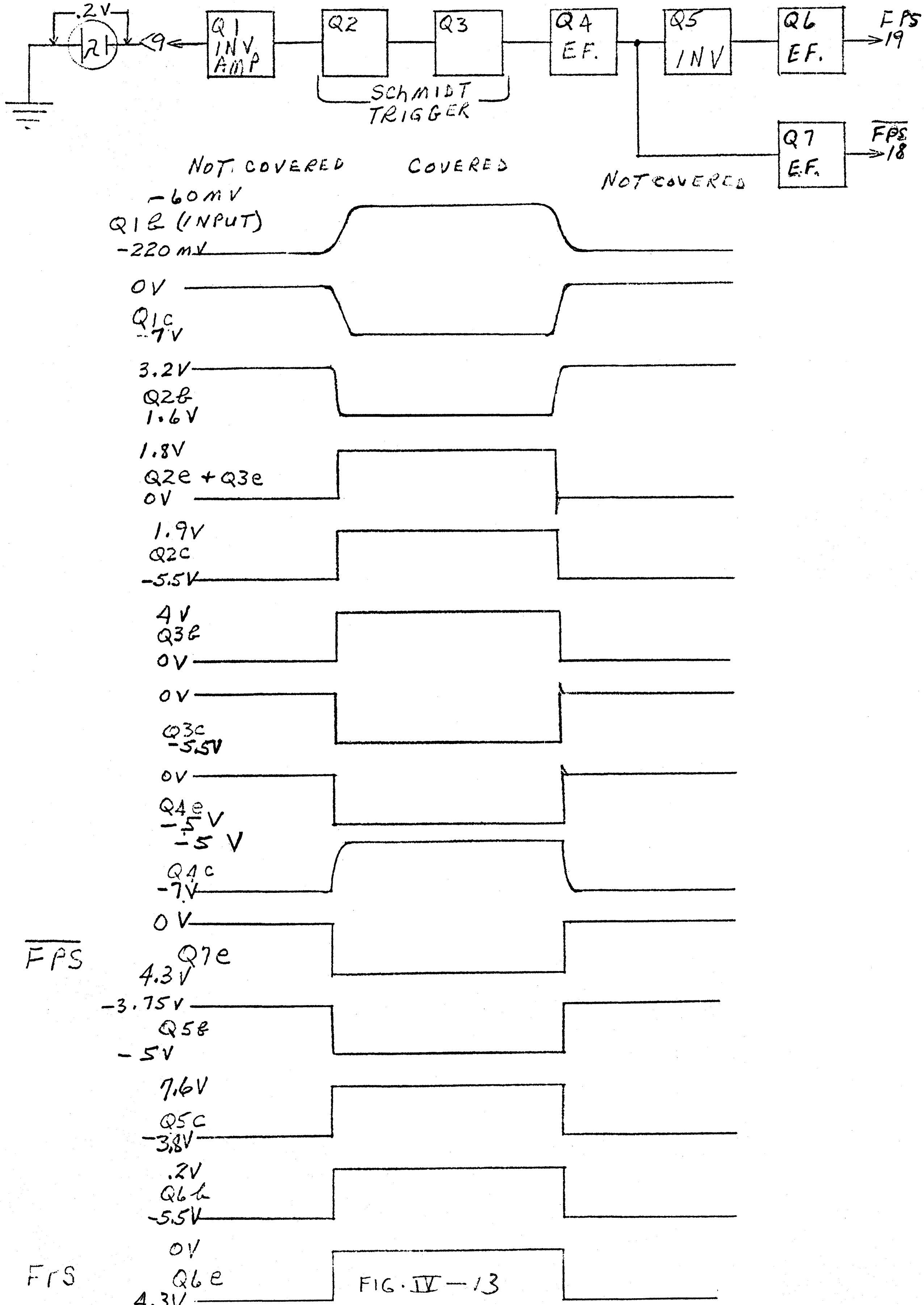
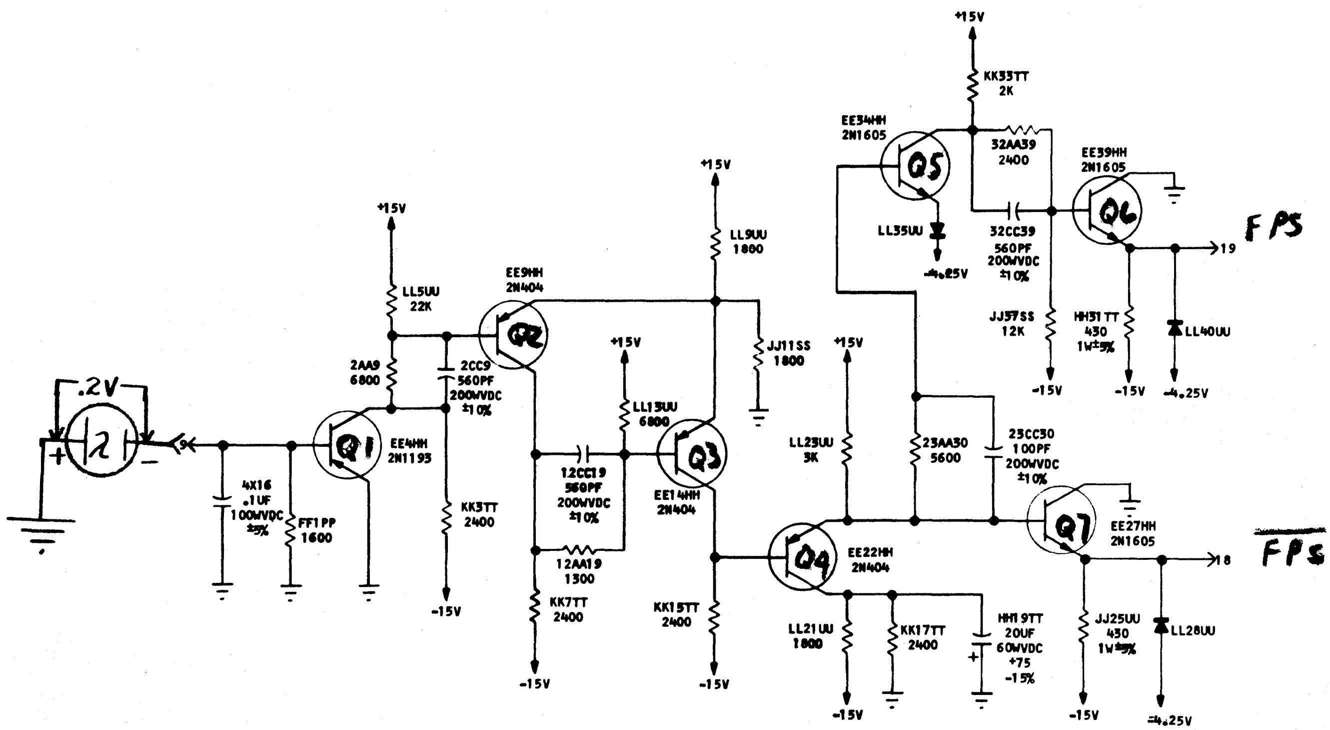

.2V
Q1 INV AMP
Q2
Q3
Q4 E.F.
Q5 INV
Q6 E.F.
FPS 19
SCHMIDT TRIGGER
Q7 E.F.
$\overline{FPS}$ 18
NOT COVERED
COVERED
NOT COVERED
-60mV
Q1e (INPUT)
-220mV
0V
Q1c
-7V
3.2V
Q2b
1.6V
1.8V
Q2e + Q3e
0V
1.9V
Q2c
-5.5V
4V
Q3e
0V
0V
Q3c
-5.5V
0V
Q4e
-5V
-5V
Q4c
-7V
0V
$\overline{FPS}$
Q7e
4.3V
-3.75V
Q5b
-5V
7.6V
Q5c
-3.8V
.2V
Q6b
-5.5V
0V
FPS
Q6e
4.3V

FIG. IV-13

The high signal from the emitter of Q4 will cause the base of Q5 to be positive in respect to its emitter. Q5 will be on current from -15V through resistors JJ37SS and 32AA39 to -4V at the collector of Q5 will provide a negative voltage at the base of Q6. Q6 will be off and current from -15V through resistor HH31TT and diode LL40UU to -4V will provide a low FPS signal at pin 19.

As a form is inserted or withdrawn from the machine the solar cell will be covered and uncovered gradually. This will cause a gradual voltage change from the solar cell. The Schmidt Trigger (Q2 and Q3) will provide a sharper leading and trailing edge for this signal.

When a form is inserted the solar cell voltage is removed from the base of Q1. Q1 will turn off. Current flow from -15V through resistors KK3TT, 2AA9 and LL5UU to +15V provides a negative voltage for the base of Q2. Since the emitter of Q2 is near ground Q2 will come on. When Q2 starts to come on the increased current through KK7TT causes a greater voltage drop and causes the base of Q3 to become more positive. Q3 conducts less reducing the current through resistor LL9UU and JJ11SS. This provides a more positive voltage for the emitter of Q2 and Q3. With the base of Q2 going negative and the emitter going positive Q2 will be turned on very rapidly. The current through resistor KK7TT and Q2 causes resistors 12AA19 and LL13UU to place a positive voltage on the base of Q3 turning Q3 off. -15V through KK15TT to the base of Q4 turns Q4 on and the emitter voltage goes to approximately -5.2V.



+15V
KK33TT
2K
EE34HH
2N1605
Q5
32AA39
2400
EE39HH
2N1605
Q6
LL35UU
-4.25V
32CC39
560PF
200WVDC
±10%
19
FPS
JJ37SS
12K
HH51TT
430
1W±5%
LL40UU
-15V
-15V
-4.25V
+15V
LL9UU
1800
+15V
LL5UU
22K
EE9HH
2N404
Q2
JJ11SS
1800
2AA9
6800
2CC9
560PF
200WVDC
±10%
+15V
+15V
.2V
Q1
EE4HH
2N1193
LL13UU
6800
Q3
LL23UU
3K
23AA30
5600
23CC30
100PF
200WVDC
±10%
4X16
.1UF
100WVDC
±5%
FF1PP
1600
KK3TT
2400
12CC19
560PF
200WVDC
±10%
EE14HH
2N404
Q4
EE22HH
2N404
Q7
EE27HH
2N1605
18
FPS
12AA19
1300
-15V
KK7TT
2400
KK15TT
2400
LL21UU
1800
KK17TT
2400
HH19TT
20UF
60WVDC
+75
-15%
JJ25UU
430
1W±5%
LL28UU
-15V
-15V
-15V
-15V
-4.25V

Fig. IV-14

This negative voltage turns Q7 off and current flow from -15V through resistor JJ25UU and diode LL28UU provide a -4V NOT FPS signal at pin 18. -5.2V at the base of Q5 turns Q5 off. Current flow from -15V through resistors JJ37SS, 32AA39 and KK33TT to +15V provides a positive voltage for the base of Q6. Q6 will be on and ground through Q6 to pin 19 provides a high FPS signal. If Q5 should have a high leakage current from base to emitter due to temperature changes the base of Q6 could become negative in respect to its emitter. This would be caused by increased current through KK33TT. Q6 may not be fully on to provide OV at pin 19.

A diode LL35UU which is reverse biased under these conditions, prevents this leakage current.

SOLAR CELL CAM AMPLIFIER

The Solar Cell Cam Amplifier (SCCA) is used to develop a 4V signal (-4 to 0) from the camshaft cam package in the tray. The circuit is also used with the carriage open indicator and with several conditions in the Auto Reader. The solar cell which controls this circuit develops a 220 mv signal when illuminated. When the solar cell is not illuminated the cell has no output signal. The positive side of the solar cell is connected to ground so that the output will be a negative signal.

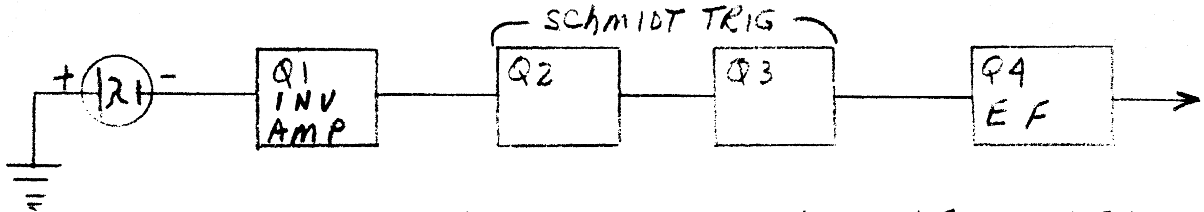
Figure IV-15 shows a block diagram, waveforms and a circuit diagram. Q1 is an inverter amplifier which Controls the Schmidt Trigger, Q2 and Q3. The Schmidt Trigger provides a square wave from the solar cell signal. The output from the solar cell is a rounded sloping curve due to the gradual covering and uncovering of the solar cell. Q4 is an Emitter Follower which provides driving current for the signal in the machine.

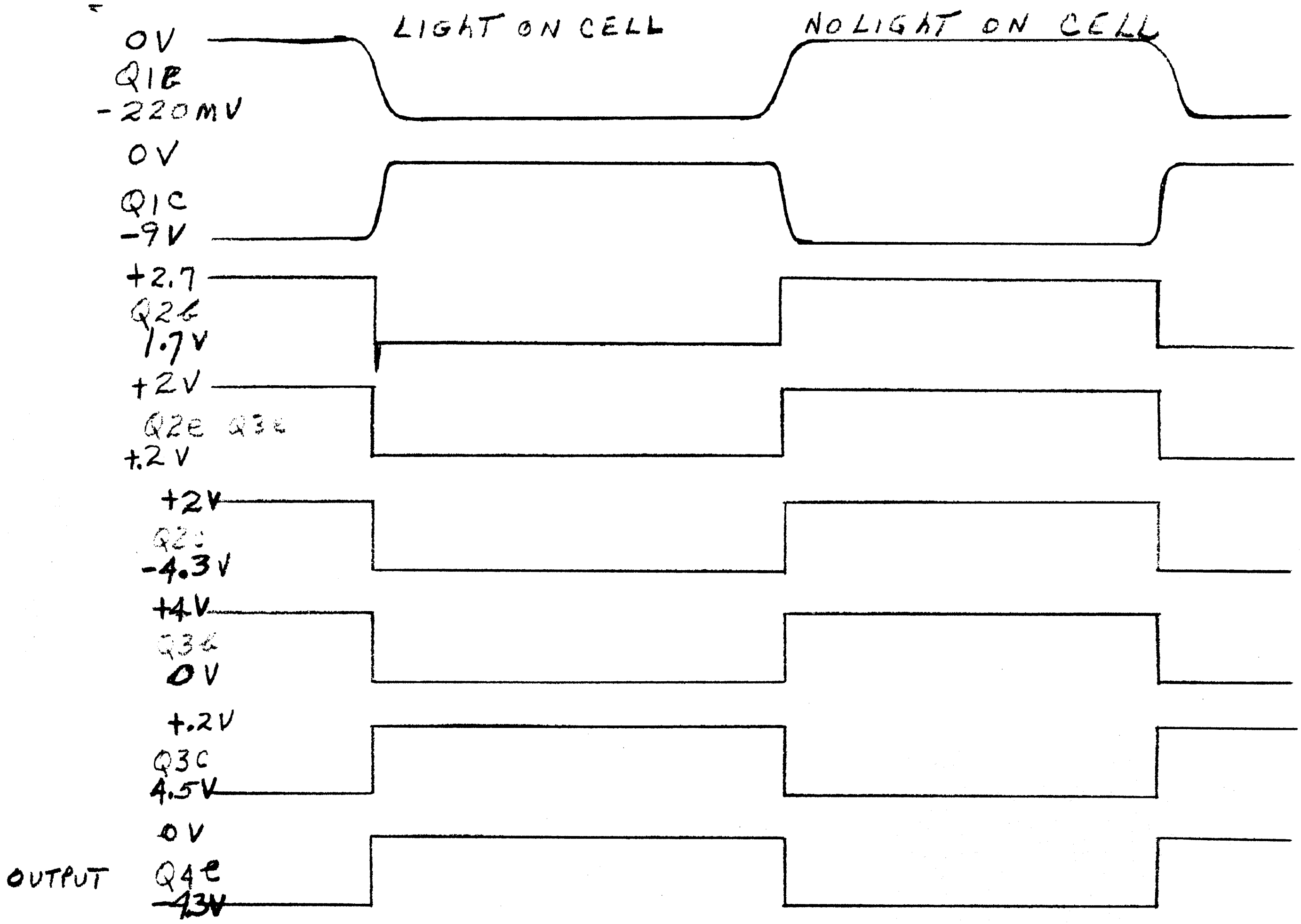
No Light on Cell

With no light on the cell the base and emitter of Q1 are both at ground and Q1 is off. Current from -15V through R2, R3 and R4 provide a negative voltage at the base of Q2, Q2 will be on and the base will then be driven positive by the emitter current. The voltage at the emitter of Q2 and Q3 will be at about +2V. Current flow from +2V at the collector of Q2 through R8 and R9 provides +4V for the base of Q3. The base emitter junction of Q3 will be reverse biased and Q3 will be off. -15V through R10 will keep Q4 off and current through the R11, CR3 diode will provide a low, -4V, signal at the output.

Light on Solar Cell

As the solar cell is illuminated the voltage at the base of Q1 becomes more negative. When the voltage reaches -170 mv, Q1 will turn on sufficiently for Current from ground through Q1, R3 and R4 provides a positive voltage at the base of Q2. Q2 will be turned off. As Q2 turns off the reduction of current flow through R5 will cause the emitter of Q2 and Q3 to become more positive. The clamp, R7 and CR1 will cause the collector of Q2 to go to -4V. Current flow from the clamp through R8 and R9 to +15V causes the voltage at the base of Q3 to become more negative. With the emitter of Q3 becoming more positive and the base becoming more negative Q3 will be switches on very rapidly, resulting in a square wave at the output. When Q3 is turned on the collector of Q3 is approximately 0V due to current flow from -15V through R10, Q3, R5 to +15V and and R6 to ground.


SCHMIDT TRIG
Q1 INV AMP
Q2
Q3
Q4 EF


LIGHT ON CELL
NO LIGHT ON CELL
0V
Q1B
-220MV
0V
Q1C
-9V
+2.7
1.7V
+2V
Q2E Q3E
+.2V
+2V
-4.3V
+4V
0V
+.2V
Q3C
4.5V
0V
OUTPUT
Q4E

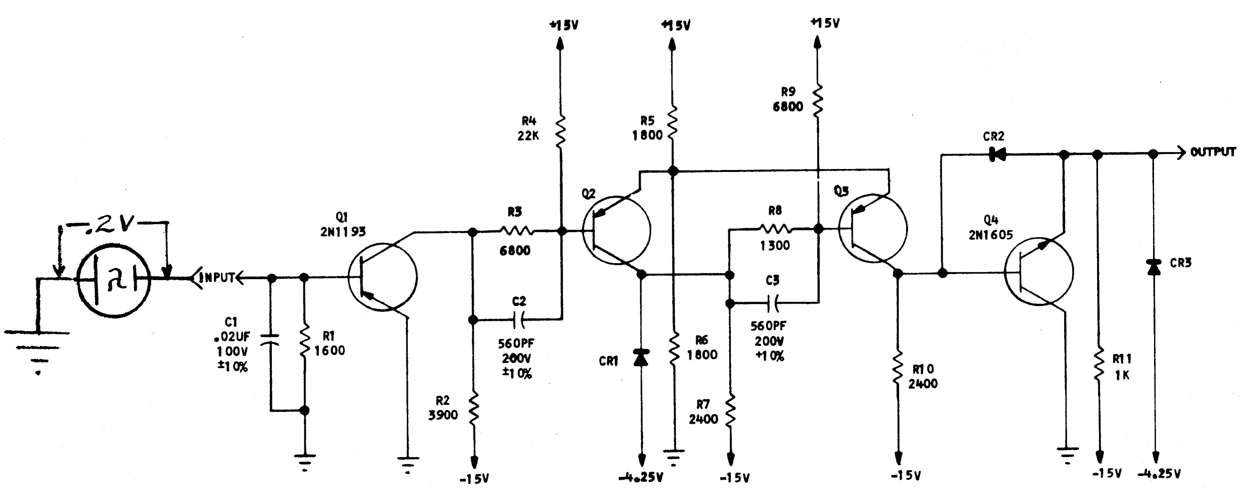

+15V
+15V
+15V
R4 22K
R5 1800
R9 6800
CR2
OUTPUT
Q1 2N1193
R3 6800
Q2
Q3
R8 1300
Q4 2N1605
-.2V
INPUT
C2 560PF 200V ±10%
C3 560PF 200V ±10%
CR3
C1 .02UF 100V ±10%
R1 1600
CR1
R6 1800
R10 2400
R11 1K
R2 3900
R7 2400
-15V
-4.25V
-15V
-15V
-15V
-4.25V

FIG. IV-15

With a high signal at the base of Q4 the emitter of Q4 and output will also be high.

When the cell is again covered the circuit will revert to its original state and the output will again by -4V. Q1 will be turned off when the voltage on its base becomes less negative than -170 mv. Q2 will be turned on again by the R2, R3 and R4 voltage divider. When Q2 turns on the base of Q3 becomes positive due to current flow through R6, Q2, R8 and R9 to +15V. Q3 is turned off. Q4 will be turned off by -15V through R10. With Q4 off, the R11, CR3 clamp provides -4V at the output.

6 ms RESETTABLE DELAY

As an encoded form is driven under the X read head, pulses from the stripe are gated to the 6 ms resettable delay circuit. Each pulse received, resets the circuit so that the RC time starts over again. When no pulses are read from the stripe for a period of 6 ms the delay will time out and a 16us pulse will be produced. This pulse indicates to the logic that all data from the X stripe has been read and that the next pulse received will be the sync pulse.

Figure IV-16 shows a block diagram and some wave forms for the circuit. Figure IV-17 shows the circuit diagram.

Q1 is an inverter which also converts the signal from a 4V signal to a 15V signal. Q2 is an E.F. used to charge the capacitor for the 6 ms delay. Q3 and Q4 form a schmidt trigger. The 6 ms discharge rate is a very flat curve and the schmidt trigger is needed to detect a voltage level on the curve and trigger from this voltage. Q5 provides charge current for the 16 us RC circuit. Q6 provides driving current for the output pulse in the machine.

Quiescient Conditions

-4V volts through pin 17, resistors U40BB and A36J to +15V provides a negative voltage at the base of Q1. Q1 will be on. Ground through Q1 will cause the base of Q2 to be near ground.

Q2 is an emitter follower and the cathode of diode V34CC will be slightly above ground. +15V through resistor LL32UU to the base of Q3 will cause Q3 to be on. The emitter of Q3 and Q4 will be +.5V due to current flow through resistor FF21PP. Since Q3 is on, the collector of Q3 will be at about +.5V. Current flow from -15V through resistors KK23TT and EE30NN to +.5V will provide +.3V at the base of Q4. Q4 will be off. Current flow from -15V through B28K, V28CC and LL25UU provides approximately -3.75V at the base of Q5. This is positive in respect to the emitter and Q5 will be on. Q5 being on will cause the left side of the capacitor C25P to be at -4V. +15V through resistor A21J to the base of Q6 will cause Q6 to be on and the output at pin 27 will be -4V.

Activated Conditions

When pin 17 goes high, due to a pulse on the X stripe, the base of Q1 will become positive and Q1 will turn off. The clamp circuit from -100V through resistor T37DD and diode B38K will provide -15V for the base of Q2. The emitter will also go to -15V. This voltage will forward bias the diode V34CC and current flow from -15V through Q2, diode V34CC, and resistors AA32JJ and LL32UU to +15V will cause capacitor V30CC to charge to approximately -15V.

The base of Q3 will also become negative and Q3 will turn off. With Q3 off, the voltage divider KK23TT, EE30NN, and LL34UU will provide a positive voltage at the base of Q4. Q4 will turn on and current from -15V through resisters B28K, V28CC, Q4 and resistor FF21PP will provide approximately -5V for the base of Q5. Q5 will turn off and current flow from ground through diode 24S31 and resistor A30J to +15V will cause a 4V positive swing at the left plate of capacitor C25P. The right side of the capacitor will also try to go positive, however, Q6 is already on and clamped to -4V. The out put at 27 will not change.

When the pulse from the read amplifier passes, -4V at pin 17 will cause Q1 to turn on. This will provide ground through Q1 to the base of Q2. The emitter of Q2 will also go to ground. This reverse biases diode V34CC. The discharge time of capacitor V30CC through resistors AA32JJ and LL32UU is very long (6ms). As additional pulses are received at pin 17 Q1 will turn off and on with each pulse. The base and emitter of Q2 will also go to near -15V on each pulse. As the voltage on the cathode of diode V34CC becomes negative with respect to the change on capacitor V30CC, the capacitor will be recharged to -15V. When no pulses have been received at pin 17 for 6 ms, capacitor V30CC will have discharged through resistors AA32JJ and LL32UU When the base of Q3 becomes positive in respect to the emitter Q3 will turn on. With Q3 on the collector of Q3 will again go to .5V. Current from -15V through resistors KK23TT and EE30NN to .5V at the collector of Q3 causes the base of Q4 to become negative in respect to its emitter. Q4 is turned off. Resistors B28K, V28CC and LL25UU between -15V and +15V provides -3.75V for the base of Q5. Q5 is turned on. -4V through Q5 will provide a 4V negative swing for the left side of capacitor C25P.

The right side of the capacitor will also have a 4V negative swing and goes to -8V. This is negative in respect to the emitter and Q6 is turned off. With Q6 off current from ground through diode D17M and resistor A19J provide a high signal at pin 27. The length of this high signal will be the RC time of capacitor C25P and resistor A21J. This will be approximately 16 us. When capacitor C25P has discharged enough for the base of Q6 to become positive with respect to its emitter, Q6 will turn over and -4V through Q6 to pin 27 provides a low signal. A 16 us pulse from -4 to ground has been produced at pin 27. The leading edge of the output pulse starts 6 ms after the last Read Amp pulse at pin 17.

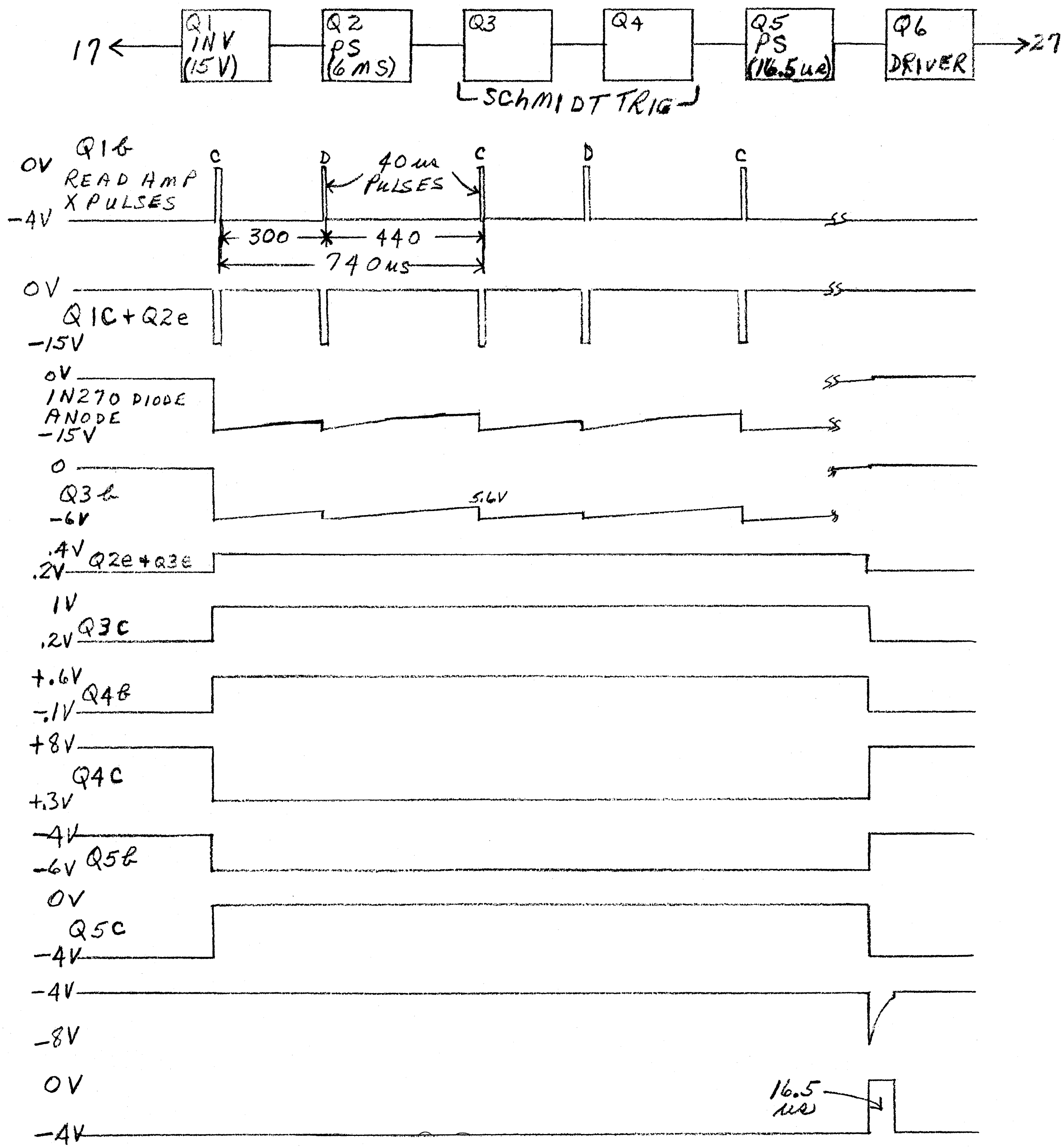

17
Q1 INV (15V)
Q2 PS (6 MS)
Q3
Q4
Q5 PS (16.5 us)
Q6 DRIVER
27
SCHMIDT TRIG
Q1b READ AMP X PULSES
0V
-4V
C D C D C
40 us PULSES
300
440
740 us
0V
Q1C + Q2e
-15V
0V
1N270 DIODE ANODE
-15V
0
Q3b
-6V
5.6V
.4V
.2V
Q2e + Q3e
1V
.2V
Q3C
+.6V
-.1V
Q4B
+8V
Q4C
+.3V
-4V
-6V
Q5b
0V
Q5C
-4V
-4V
-8V
0V
-4V
16.5 us

FIG. IV-16

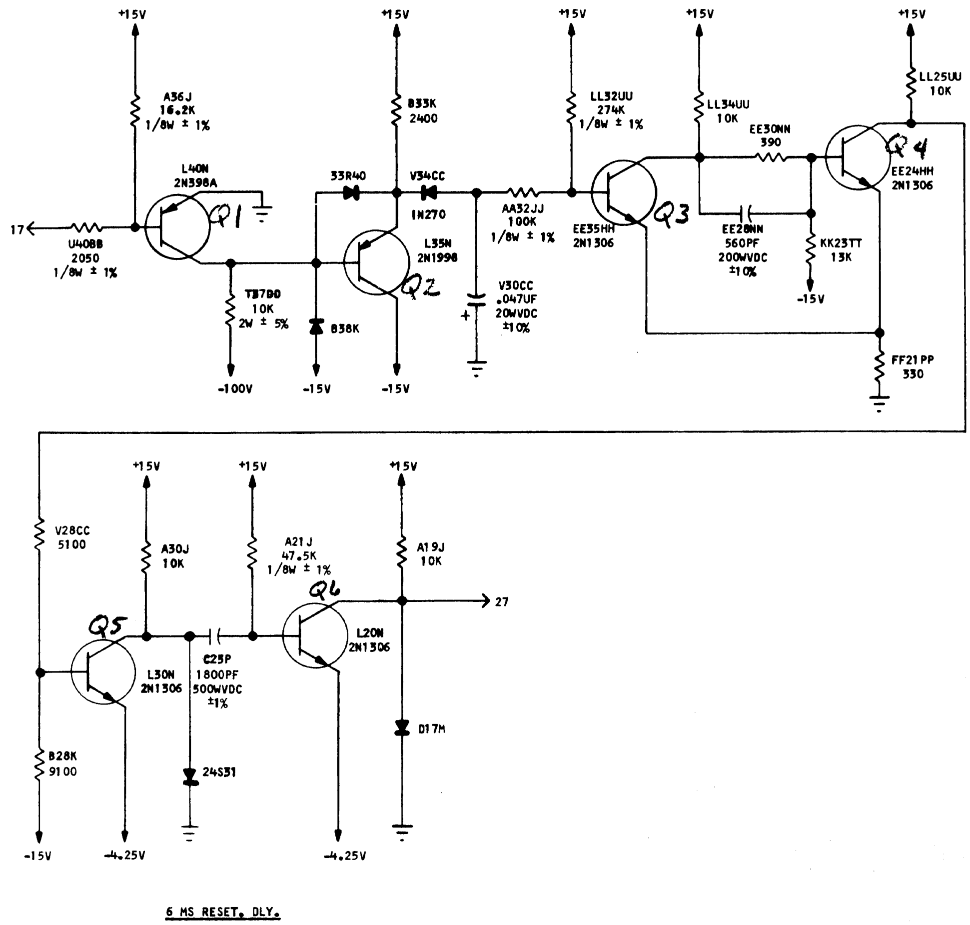

+15V
A36J
16.2K
1/8W ± 1%
L40N
2N398A
Q1
17
U408B
2050
1/8W ± 1%
T37DD
10K
2W ± 5%
-100V
B38K
-15V
B35K
2400
33R40
V34CC
1N270
L35N
2N1998
Q2
V30CC
.047UF
20WVDC
±10%
AA32JJ
100K
1/8W ± 1%
LL32UU
274K
1/8W ± 1%
EE35HH
2N1306
Q3
LL34UU
10K
EE30NN
390
EE28NN
560PF
200WVDC
±10%
KK23TT
13K
LL25UU
10K
Q4
EE24HH
2N1306
FF21PP
330
V28CC
5100
B28K
9100
Q5
A30J
10K
L30N
2N1306
C25P
1800PF
500WVDC
±1%
24S31
-4.25V
A21J
47.5K
1/8W ± 1%
Q6
L20N
2N1306
A19J
10K
27
D17M
6 MS RESET. DLY.

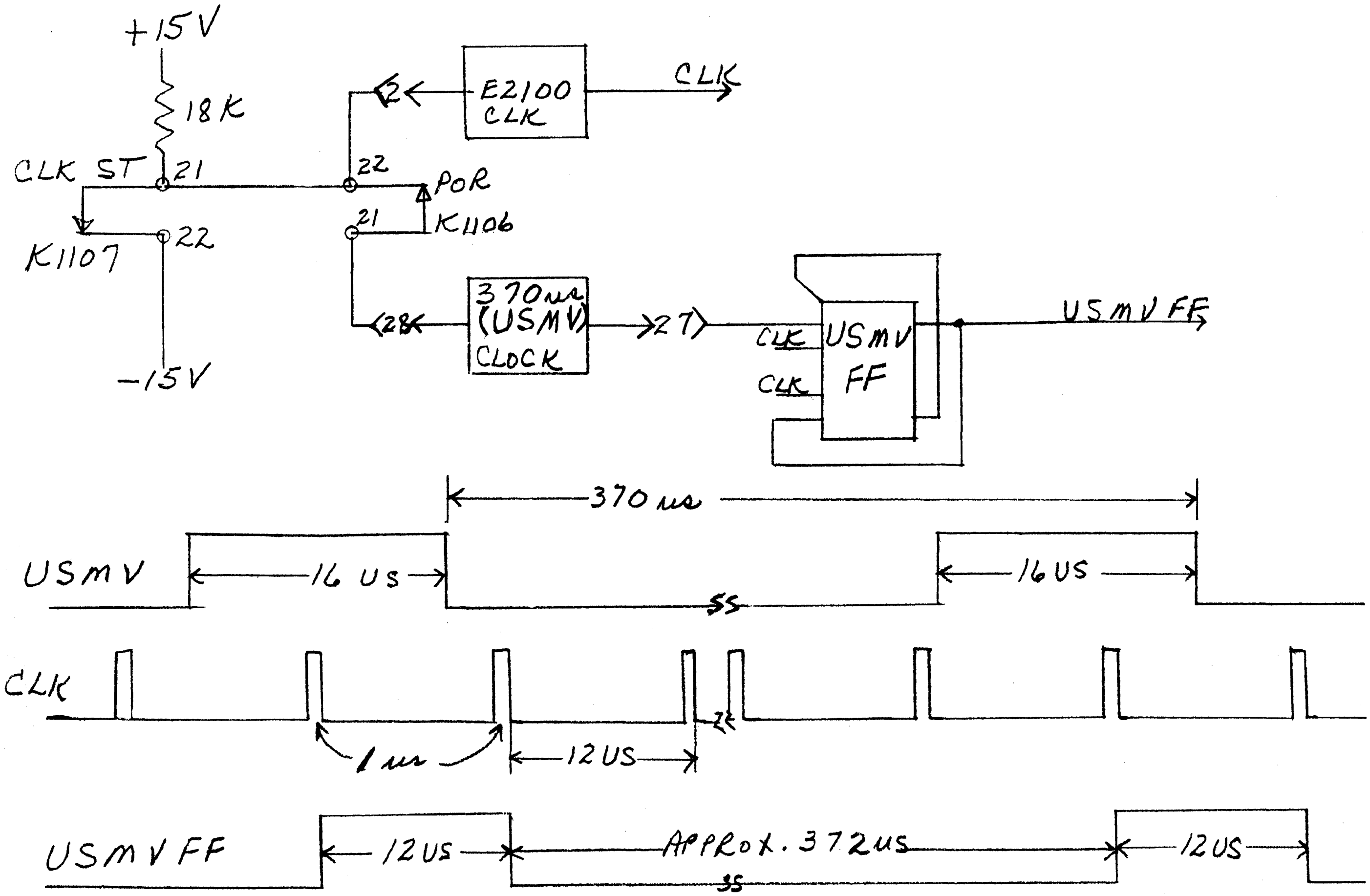
Fig. IV-17

UNSYNCHRONIZED MULTIVIBRATOR (USMV)

A free running multivibrator with a 16 μs pulse every 370 μs is used in addition to the E 2100 clock to control the Striped ledger operations. The 370 μs multivibrator uses the same circuit configuration as the E 2100 clock, only the RC components have different values. The circuit name comes from the fact that this circuit is not synchronized with the E 2100 clock. The 16 μs pulse provides enough time to ensure getting a complete clock pulse. The E 2100 clock and USMV signals are used to set the USMVFF. The USMVFF signal is used with the following clock pulse is used to reset the USMVFF. A 12 μs pulse every 370 μs is produced by the USMVFF. This pulse is synchronized with clock and is the signal used in the striped ledger logic.

Figure IV-18 shows a block diagram of the USMVFF signal circuit, some signals and a circuit diagram of the USMV.

Both the E 2100 clock and the USMV are triggered by the clock start relay to assure that pulses are generated. A set of POR contacts open the circuit between the two clocks after the starting trigger is received. This prevents the signals generated by one clock tending to trigger the other through the capacitor coupling of the clock start circuits.


+15V
18K
CLK ST
21
22
K1107
-15V
E2100
CLK
CLK
POR
K1106
370us
(USMV)
CLOCK
28
27
CLK
USMV
FF
CLK
USMV FF
370 us
USMV
16 us
16 US
CLK
1 us
12 US
USMV FF
12 US
APPROX. 372 US
12 US

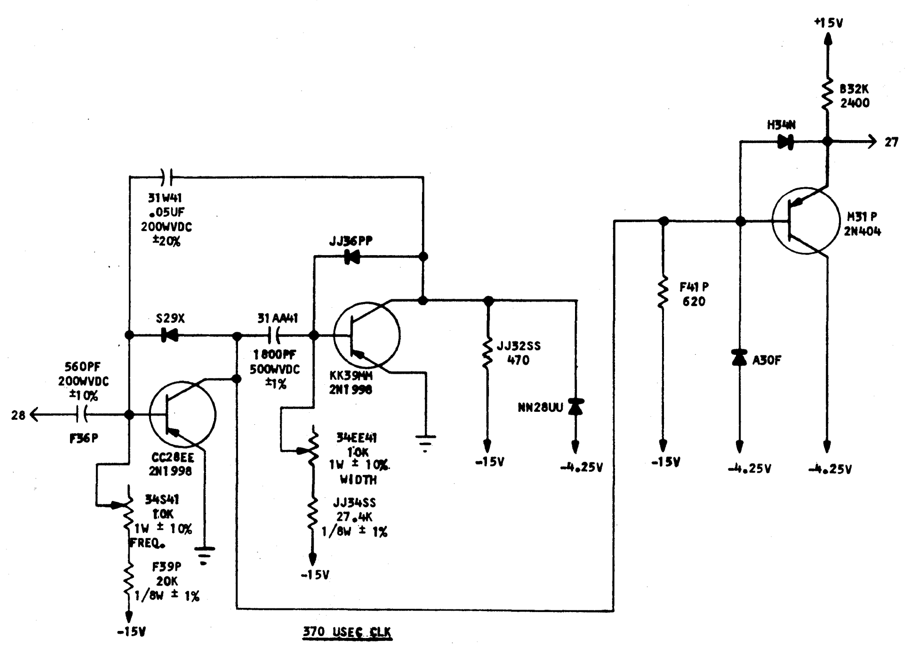

+15V
B32K
2400
H34N
27
M31 P
2N404
31W41
.05UF
200WVDC
±20%
JJ36PP
S29X
31 AA41
1800PF
500WVDC
±1%
KK39HH
2N1998
JJ32SS
470
F41 P
620
A30F
560PF
200WVDC
±10%
28
F36P
CC28EE
2N1998
NN28UU
-15V
-4.25V
34EE41
10K
1W ± 10%
WIDTH
JJ34SS
27.4K
1/8W ± 1%
34S41
10K
1W ± 10%
FREQ.
F39P
20K
1/8W ± 1%
-15V
370 USEC CLK

FIG. IV - 18

DELAY MULTIVIBRATOR (DMV) CIRCUITS

There are several DMV circuits used in the 2190 machines. All of these circuits are similar in their operation. Each consists of a driver circuit, an RC circuit, a feedback circuit and an output driver circuit. The first driver stage charges the capacitor of the RC circuit. The RC circuit provides the time period of the delay. The output driver provides current for the signal in the machine and to hold the capacitor driver on. The feedback circuit and the input circuit form a resistor or gate to control the first stage.

Some of the DMVS feed into a PS which provudes a pulse after the delay period.

The RC time of a circuit depends on three factors. These are (1) the size of the capacitor in farads, (2) the size of the Resistor in ohms, which the capacitor must discharge through and, (3) the charge in volts on the capacitor. In each circuit the RC time has been disigned to fall within certain specifications. If these specifications cannot be met by specifying tolerances for components an adjusting part is designed into the circuit.

MB2 Delay Multivibrator

Figure IV-19 shows the block diagram, wave forms and circuit diagram of the 100 ms DMV used in the MB2 solenoid circuit. This circuit will be discussed as a typical DMV.

Quiescent Conditions

Pin 15 is normally low (-4V). Current from -15V through resistors JJ24SS and 3Y10 to -4V causes the base of Q1 to be approximately -5V. This is negative with respect to the emitter and Q1 will be off. Current flow from ground through resistors HH19RR and KK17TT to +15V provides +5V for the left side of capacitor 15BB24. Ground through resistor EE12RR causes Q2 to be on and the collector of Q2 will be -15V. Clamp diode NN5UU clamps the base of Q3 at -4V. Since Q3 is an emitter follower the emitter and pin 12 will be at -4V or a low output. -4V is fed back to the base of Q1 through resistor 3AA10.

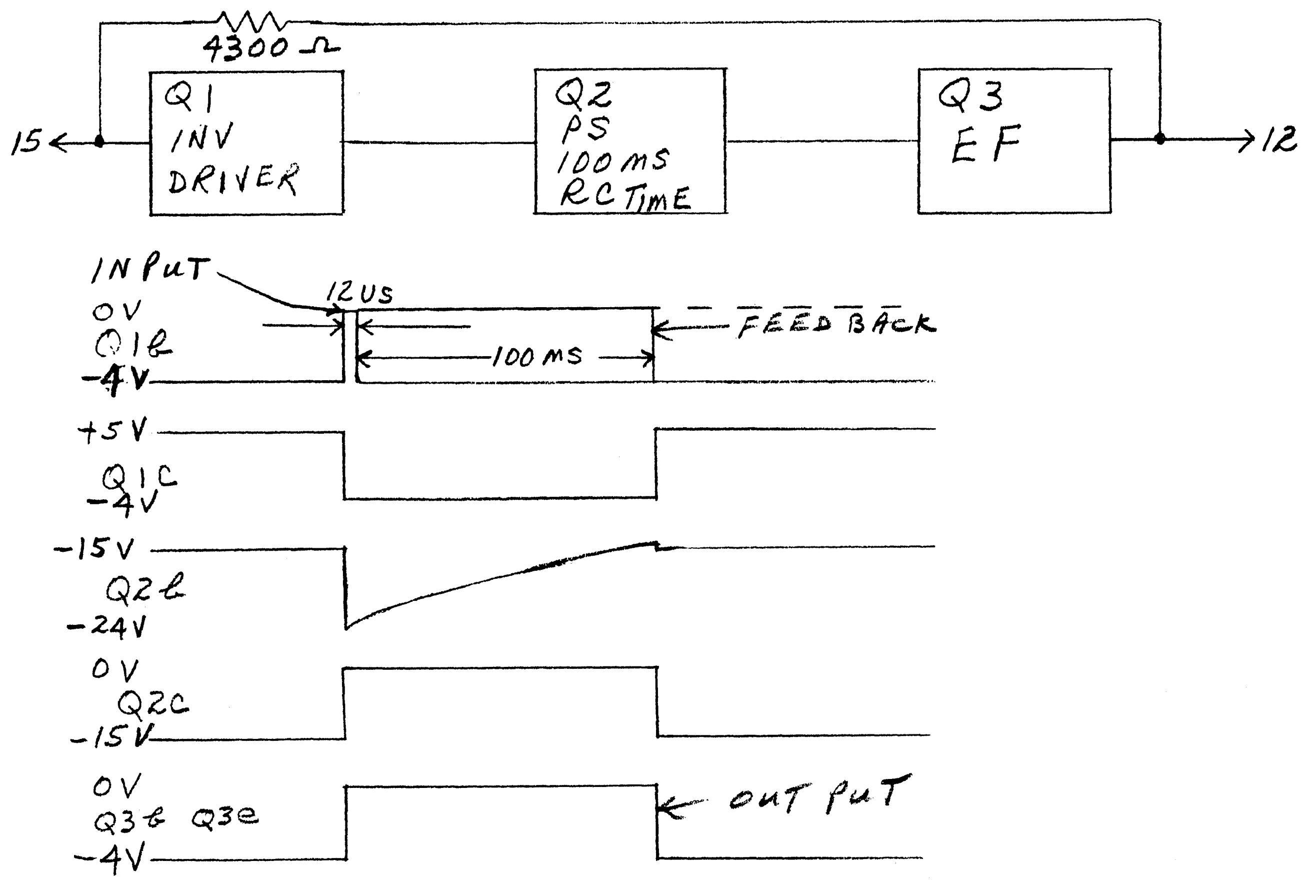
Once the DMV is triggered a pre-determined pulse is developed at pin 12. The pulse or signal at pin 12 is independent of the signal input. The only requirement of the input signal is to be of sufficient duration to trigger the DMV. The usual input to a DMV will be a 12 or 16 us pulse, however a pulse as short as 1 us will trigger the circuit. In some cases the input signal is longer than the output signal.

Activated Condition

When pin 15 becomes high, current flow from -15V through resistors JJ24SS and 3Y10 will provide approximately -2V at the base of Q1. Q1 will turn on and the base will go to -4V. The collector of Q1 and the left side of capacitor 15BB24 will go to -4V. This is a negative swing of 9V. The right side of the capacitor will be driven down 9V or to -24V. Q2 will be turned off. Current from ground through diode KK9RR and resistor KK7TT will provide a slightly positive voltage at the base of Q3.

The collector of Q3 and pin 12 will be high. The high output at pin 12 is applied to the base of Q1 through resistor 3AA10. This will hold Q1 on regardless of the input signal at pin 15. Pin 12 will remain high until capacitor 15BB24 discharges through resistor EE12RR. When the right side of capacitor 15BB24 and the base of Q2 becomes positive in respect to the -15V on the emitter, Q2 will again turn on. Current from -15V through Q2 resistor 6CC13 and diode NN5UU will cause the base and emitter to Q3 to go to -4V. The output at pin 12 will be low. The base of Q1 will become negative in respect to the emitter when both pin 15 and pin 12 become low. Assuming that this circuit was triggered by a 12 us pulse pin 15 will be low and when pin 12 goes low Q1 will turn off. With Q1 off the voltage divider resistors HH19RR and KK17TT provide +5V for the left side of capacitor 15BB24. The right side will also try to go positive which will turn Q2 on. Q2 is already on and no significient change occurs.

A 100 ms positive pulse has been produced at pin 12. The leading edge of the output pulse coincides with the leading edge of the input pulse.


4300 Ω
Q1
INV
DRIVER
Q2
PS
100 MS
RC TIME
Q3
EF
15
12
INPUT
12 US
0 V
Q1b
-4V
FEED BACK
100 MS
+5 V
Q1C
-4V
-15 V
Q2b
-24 V
0 V
Q2C
-15 V
0 V
Q3b Q3e
-4V
OUT PUT

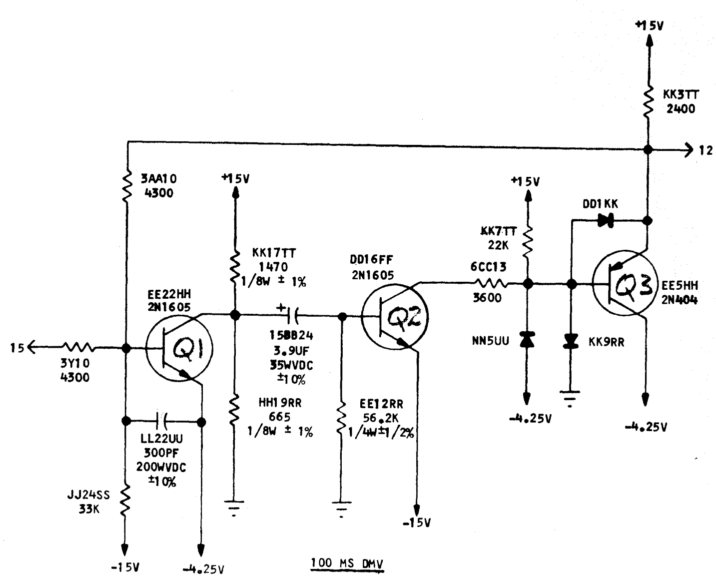

+15V
KK3TT
2400
12
3AA10
4300
+15V
+15V
DD1KK
KK7TT
22K
KK17TT
1470
1/8W ± 1%
DD16FF
2N1605
6CC13
3600
EE5HH
2N404
EE22HH
2N1605
158B24
3.9UF
35WVDC
±10%
NN5UU
KK9RR
15
3Y10
4300
HH19RR
665
1/8W ± 1%
EE12RR
56.2K
1/4W±1/2%
-4.25V
-4.25V
LL22UU
300PF
200WVDC
±10%
JJ24SS
33K
-15V
-15V
-4.25V
100 MS DMV

Fig. IV-19

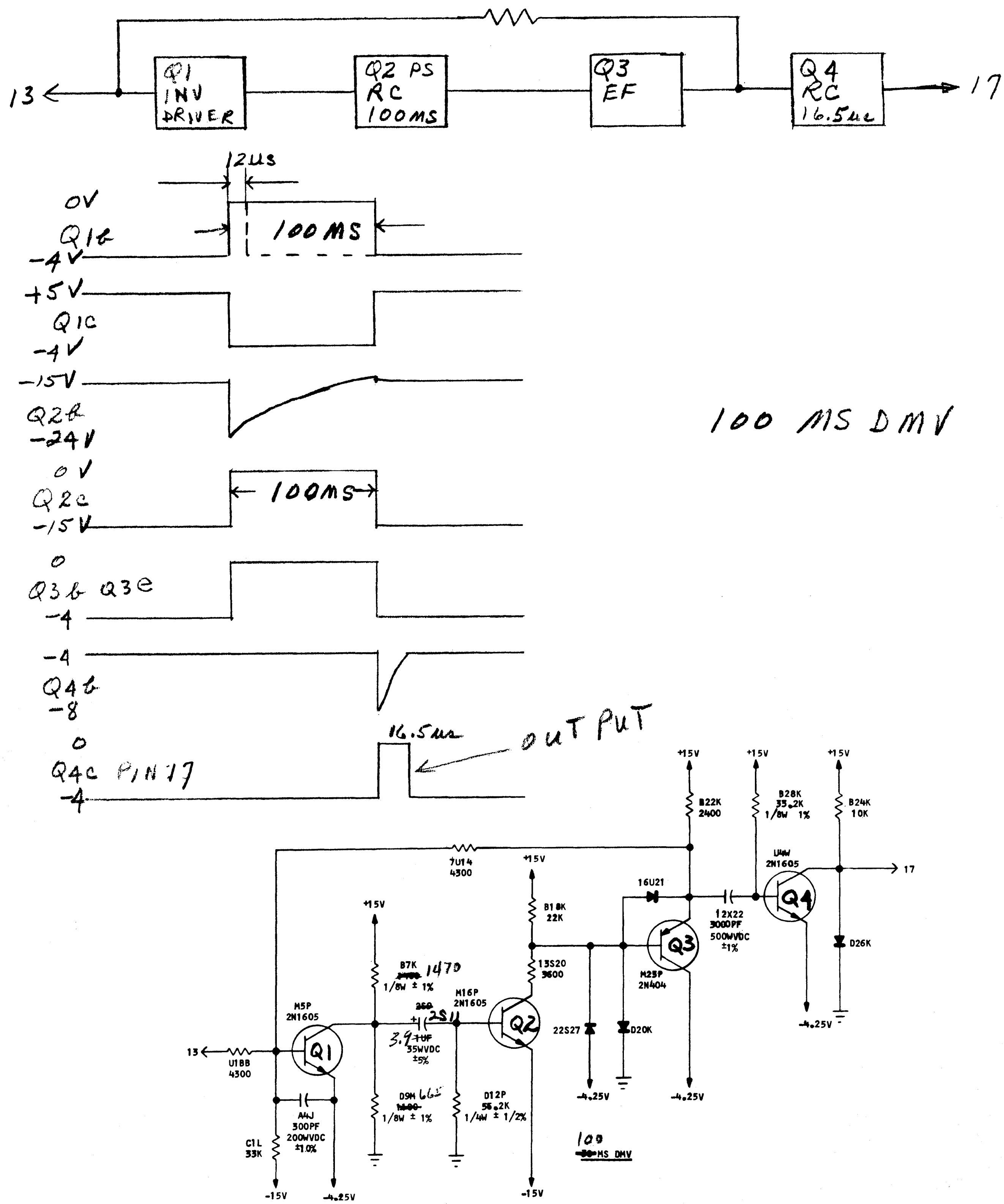
Paper Drive Clutch Delay Multivibrator

The DMV used with the Paper Drive Clutch is a 100 ms DMV and a Pulse Standardizer (PS) which produces a 16 us pulse after a 100 ms delay. The trailing edge or negative swing of the 100 ms signal is used to trigger a PS. The PS provides the 16 us pulse at the output.

Figure IV-20 shows the block diagram, wave forms and circuit diagram. The DMV is identical to the MB2 DMV.

16 us Output Pulse

+15V through B28K causes Q4 to be on. -4V through Q4 provides a low output at pin 17. Both sides of capacitor 12X22 are at -4V. When the emitter of Q3 becomes high, as the DMV is triggered, the right side of capacitor 12X22 will be driven positive. This will tend to turn on Q4. Since Q4 is already on no change occurs. On the trailing edge of the 100 ms DMV the emitter of Q3 will have a 4V negative swing. The right side of capacitor 12X22 will be driven to -8V. This will turn off Q4 and pin 17 will be made high due to current flow from ground through diode D26K and resistor B24K. When capacitor 12X22 discharges through resistor B28K sufficiently for the base of Q4 to becomes positive in respect to the emitter Q4 will turn on and pin 17 will again be low.



13
Q1 INV DRIVER
Q2 PS RC 100MS
Q3 EF
Q4 RC 16.5us
17
12us
0V
Q1b
-4V
100MS
+5V
Q1c
-4V
-15V
Q2b
-24V
0V
Q2c
-15V
100ms
0
Q3b Q3e
-4
-4
Q4b
-8
0
Q4c PIN 17
-4
16.5us
OUTPUT
100 MS DMV
+15V
B22K
2400
B28K
33.2K
1/8W 1%
B24K
10K
7U14
4300
U4W
2N1605
Q4
16U21
12X22
3000PF
500WVDC
±1%
D26K
B18K
22K
Q3
M23P
2N404
13S20
3600
B7K
1470
1/8W ± 1%
M16P
2N1605
Q2
M5P
2N1605
Q1
2S11
3.9
35WVDC
±5%
22S27
D20K
-4.25V
U1BB
4300
A4J
300PF
200WVDC
±10%
C1L
33K
D9M 665
1/8W ± 1%
D12P
56.2K
1/4W ± 1/2%
100
MS DMV
-15V

Fig. IV-20

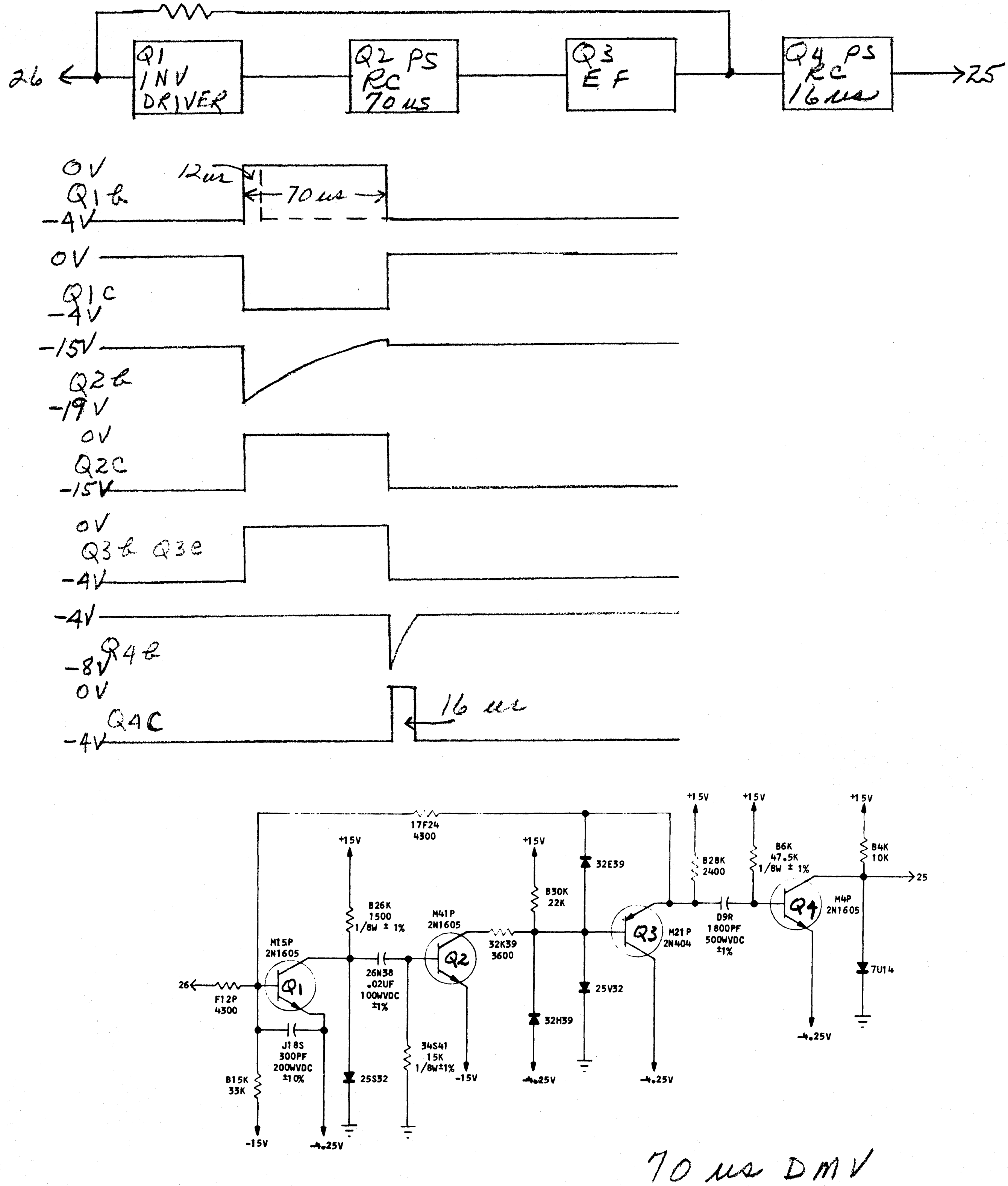

26
Q1 INV DRIVER
Q2 PS RC 70 us
Q3 EF
Q4 PS RC 16 us
25
0V
Q1b
-4V
12us
70 us
0V
Q1c
-4V
-15V
Q2b
-19V
0V
Q2C
-15V
0V
Q3b Q3e
-4V
-4V
Q4b
-8V
0V
Q4C
-4V
16 us
17F24
4300
+15V
B26K
1500
1/8W ± 1%
M15P
2N1605
Q1
F12P
4300
J18S
300PF
200WVDC
±10%
B15K
33K
-15V
-4.25V
26N38
.02UF
100WVDC
±1%
25S32
M41P
2N1605
Q2
34S41
15K
1/8W±1%
-15V
32K39
3600
B30K
22K
32E39
25V32
32H39
-4.25V
Q3
M21P
2N404
-4.25V
B28K
2400
D9R
1800PF
500WVDC
±1%
B6K
47.5K
1/8W ± 1%
Q4
M4P
2N1605
B4K
10K
7U14
-4.25V
70 us DMV

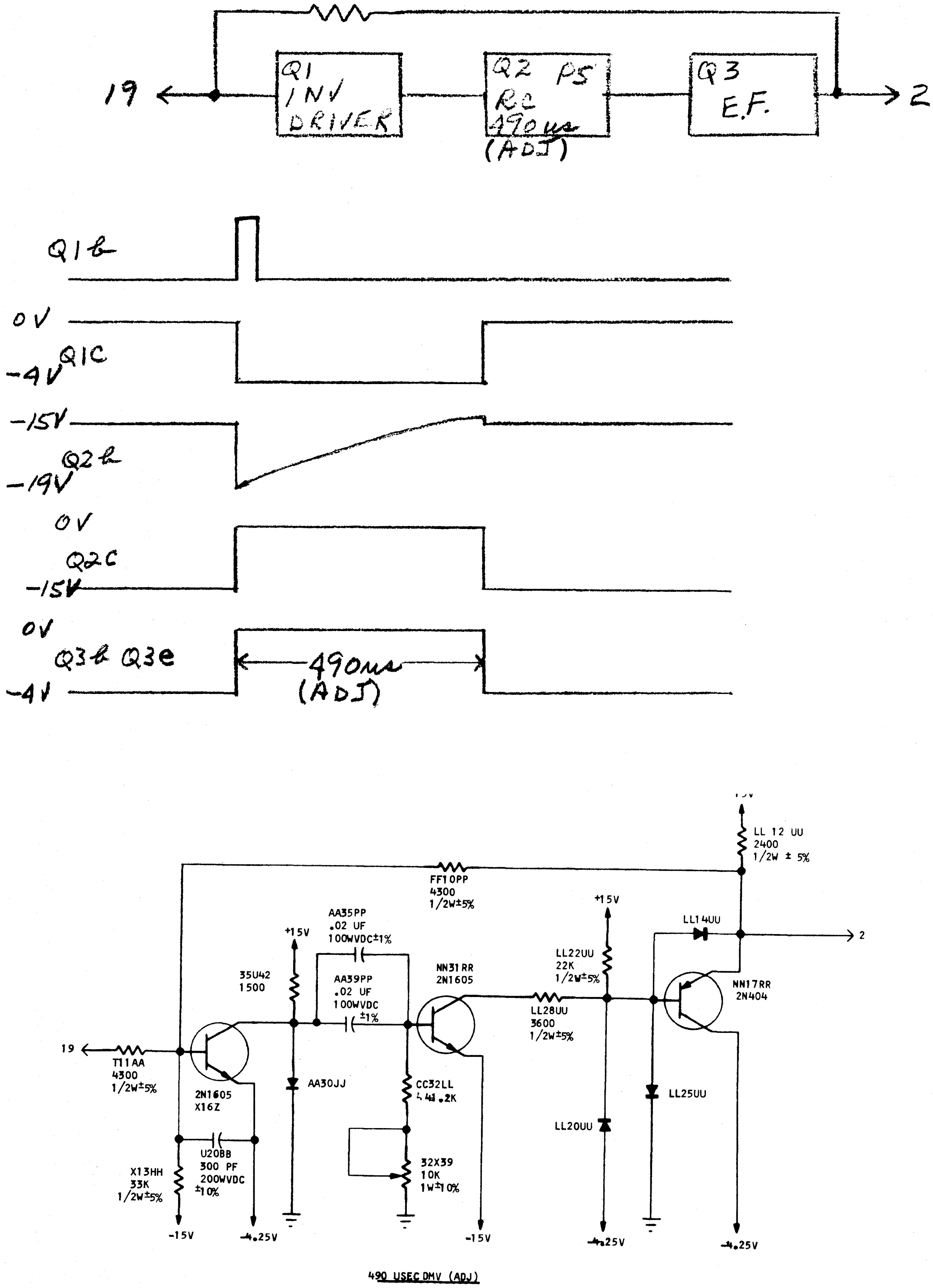
Fig. IV-21

70 us DMV

The Writing of data pulses on the stripes is delayed 70 us from the initiating USMVFF pulse. The 70 us DMV is very similar to the 100 ms DMV discussed in the previous subject. Only the capacitor and resistor sizes of the RC circuit and the applied voltage have been changed to provide the shorter delay. Figure IV-21 shows the block diagram, wave forms and circuit diagram.

490 us DMV

During the Read Ledger operation, each Complement pulse read from the stripes set the 490 us DMV. If another pulse is read from the stripe within the 490 us period it is recognized as a data pulse by the machine. The 490 us DMV must time out before the next complement pulse is read. The 490 us DMV is very similar to the 100 ms DMV which was discussed in detail. The RC components have been changed and an adjustable resistor is part of the RC circuit. This allows for precise adjustment of the output. Figure IV-22 shows the block diagram, wave forms and circuit diagram of the DMV.

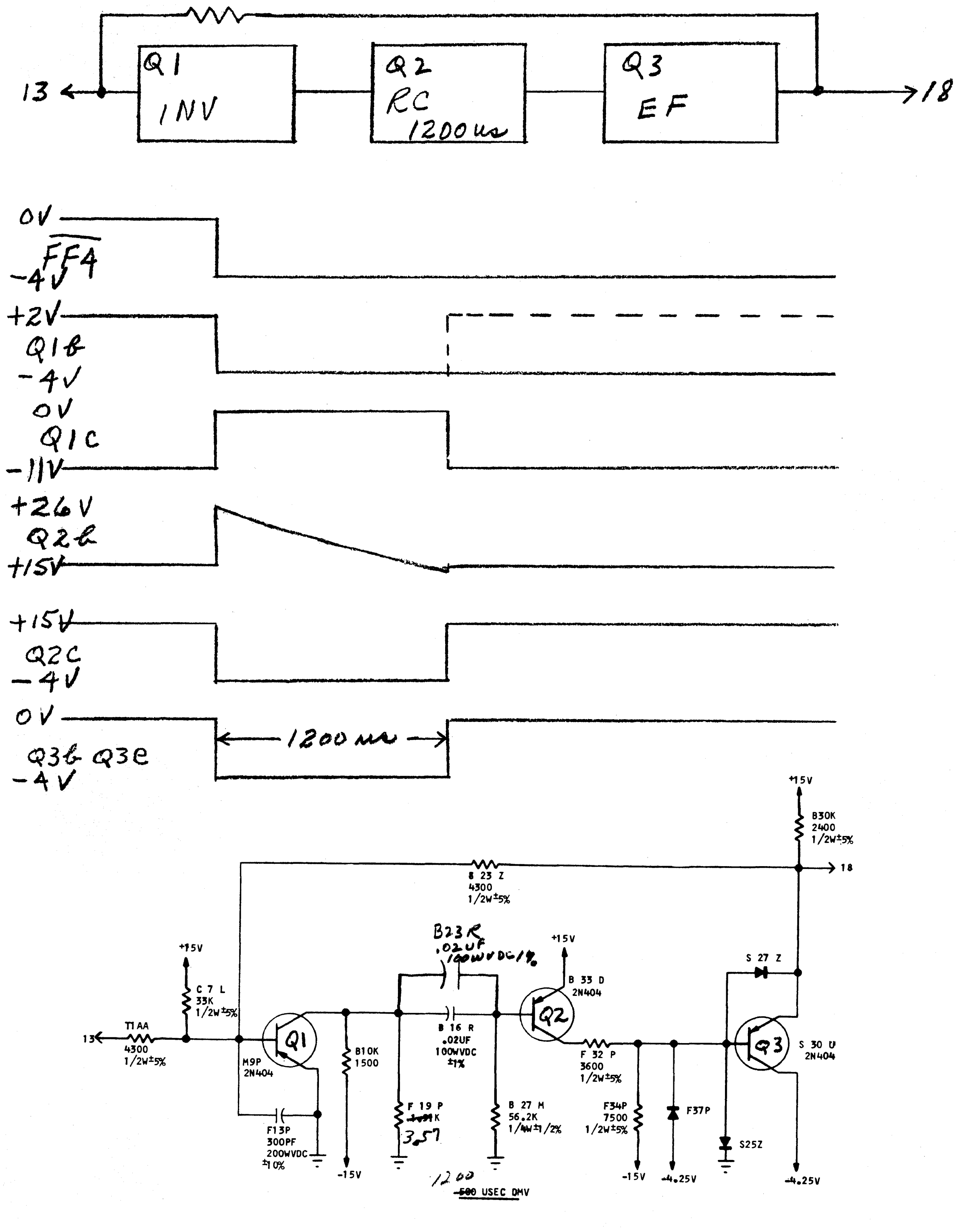


19
Q1 INV DRIVER
Q2 PS RC 490us (ADJ)
Q3 E.F.
2
Q1b
0V
Q1C
-4V
-15V
Q2b
-19V
0V
Q2C
-15V
0V
Q3b Q3e
-4V
490us (ADJ)
LL 12 UU 2400 1/2W ± 5%
FF10PP 4300 1/2W±5%
+15V
LL14UU
AA35PP .02 UF 100WVDC±1%
35U42 1500
AA39PP .02 UF 100WVDC ±1%
NN31RR 2N1605
LL22UU 22K 1/2W±5%
NN17RR 2N404
LL28UU 3600 1/2W±5%
T11AA 4300 1/2W±5%
2N1605 X16Z
AA30JJ
CC32LL
LL25UU
LL20UU
U20BB 300 PF 200WVDC ±10%
X13HH 33K 1/2W±5%
32X39 10K 1W±10%
-15V
-4.25V
490 USEC DMV (ADJ)

Fig. IV-22

1200 μs DMV

When the Line Find Information is written on the stripe by the line find head a disturbance is induced in the x head. To prevent this disturbance reaching the 6 ms resettable delay a 1200 μs DMV is used to inhibit the Read Amp X Pulses into the machine. The output of this DMV is normally high to make the gate permissive and is low for 1200 μs. The DMV is triggered by the NOT FF4 signal which is high and goes negative. The operation of this DMV is the same as the DMV's discussed previously. The type of transistors used (PNP) allows for the change in input and output signal levels, Figure IV-23 shows the block diagram wave forms and circuit diagram.



13
Q1
INV
Q2
RC
1200 us
Q3
EF
18
0V
FF4
-4V
+2V
Q1b
-4V
0V
Q1c
-11V
+26V
Q2b
+15V
+15V
Q2c
-4V
0V
1200 us
Q3b Q3e
-4V
+15V
B30K
2400
1/2W±5%
18
B 23 Z
4300
1/2W±5%
B23R
.02UF
100WVDC1%
+15V
+15V
C 7 L
33K
1/2W±5%
T1AA
4300
1/2W±5%
13
Q1
M9P
2N404
F13P
300PF
200WVDC
±10%
B10K
1500
-15V
B 16 R
.02UF
100WVDC
±1%
F 19 P
3.57
B 27 H
56.2K
1/4W±1/2%
1200
USEC DMV
Q2
B 33 D
2N404
F 32 P
3600
1/2W±5%
F34P
7500
1/2W±5%
-15V
F37P
-4.25V
S 27 Z
Q3
S 30 U
2N404
S25Z
-4.25V

Fig. IV-23

In the study of the Logic of the E2150 machines two types of flow charts will be used. There are paper handling flow charts and data flow charts. The paper handling flow charts describe the order of events in the machine which cause the ledger card to be fed into or out of the machine, the finding of the printing line etc. These flow charts appear only in the Instruction Book and are not found in the machine prints.

The data flow charts describe the method of reading and writing of data on the stripes and storage of data in Memory. These charts appear in the Instruction Book and also appear as part of the machine prints. The machine prints will always reflect the exact data flow for a specific machine.

Each data flow operation is performed while the paper is moving except the verify operation of items to be posted. This verify will be performed while the program camshaft is at 216°. Several signal timing charts are also used. These are presented as an aid to understanding the timing of events of certain operations.

BLANK CARD FORM TRAVEL

When new accounts are to be opened or as old forms are filled, forms must be handled which have no data encoded in the stripes. This operation is known as a Blank Card (BC) operation. The magnetic particles in the stripes of a new form either are not magnetized or are located in random directions. Since the form has no line find information, a counter is activated which will count the lines on the form and stop the form at 8 spaces above the first printing line. The direction of form travel will be reversed and the counter will stop the form at the first printing line. As the form is driven into the machine, the read-write heads are energized to orient or condition the stripes to receive data. The orientation is necessary since the line find data and sync pulses are single reversals of flux.

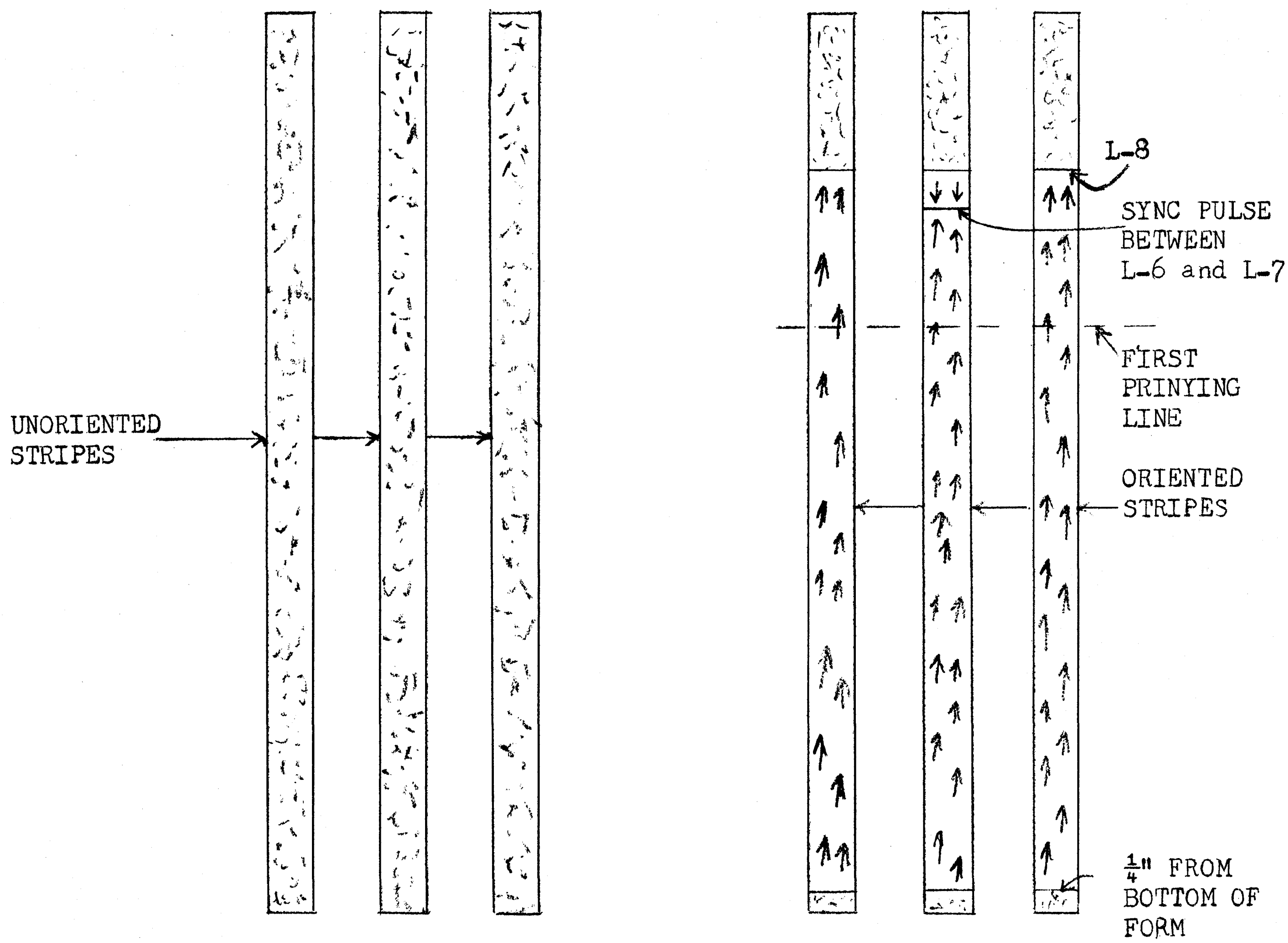

UNORIENTED
STRIPES
L-8
SYNC PULSE
BETWEEN
L-6 and L-7
FIRST
PRINYING
LINE
ORIENTED
STRIPES
$\frac{1}{4}$" FROM
BOTTOM OF
FORM

Figure V-1

The sync pulse is written in the data (center stripe between line minus six and line minus seven as the form moves from line minus eight to the first printing line. The sync pulse is used as a signal to stop the form at line minus eight as the form is driven into the machine on each subsequent read and write operation.

Figure V-2 is a single line drawing which represents paper movement during the Blank Card operation. When the card is inserted into the carriage, the program camshaft is at 0°. The form breaks the beam of light which starts the carriage motor and engages the program cam clutch. As the program cam rotates the form is pushed out of the carriage as the form is squared and aligned and the pressure rolls and read heads are lowered to the form. At 95° of the program camshaft cycle CC2 becomes high. The CC2 signal (1) drops the program camshaft clutch so that the program camshaft will detent at 144°. (2) causes a Reset pulse (R1) to prepare the electronic section for an operation. (3) triggers the paper drive circuits. A 100 ms DMV delays the paper feed signal until approximately 135°. (100 ms delay and camshaft rotating at 2 1/4 ms/degree).

The pick time of the paper drive solenoid must be added to the 135°. This will delay paper movement until the program camshaft is at 144°.

BLANK CARD FORM HANDLING LOGIC

The Blank Card operation is performed in a position programmed with lanes 56 (SL) and 52 (BC). Figure V-5 is a chart of events which control form handling during a BC operation. The initial conditions are as follows.

NOT TAB The NOT TAB signal is taken from the dropped condition of the TAB relay. The NOT TAB signal indicates that the carriage is in a stop position.

NOT TABFF A FF is used for the TAB and NOT TAB signals in the machine. The FF is set by the IN TAB SW and reset by the TAB relay. This provides noise immunity for the signal due to bouncing of the IN TAB SW during tabulation and stopping of the carriage.

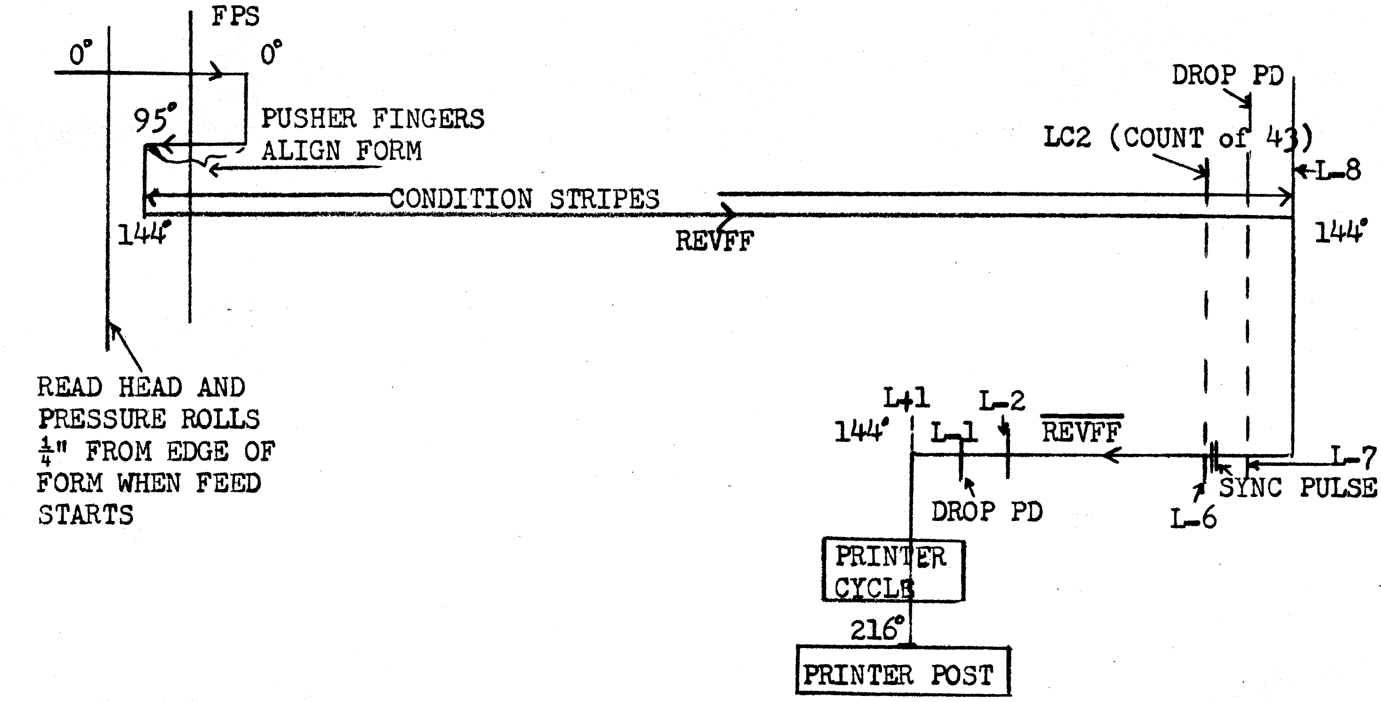


Figure V-2

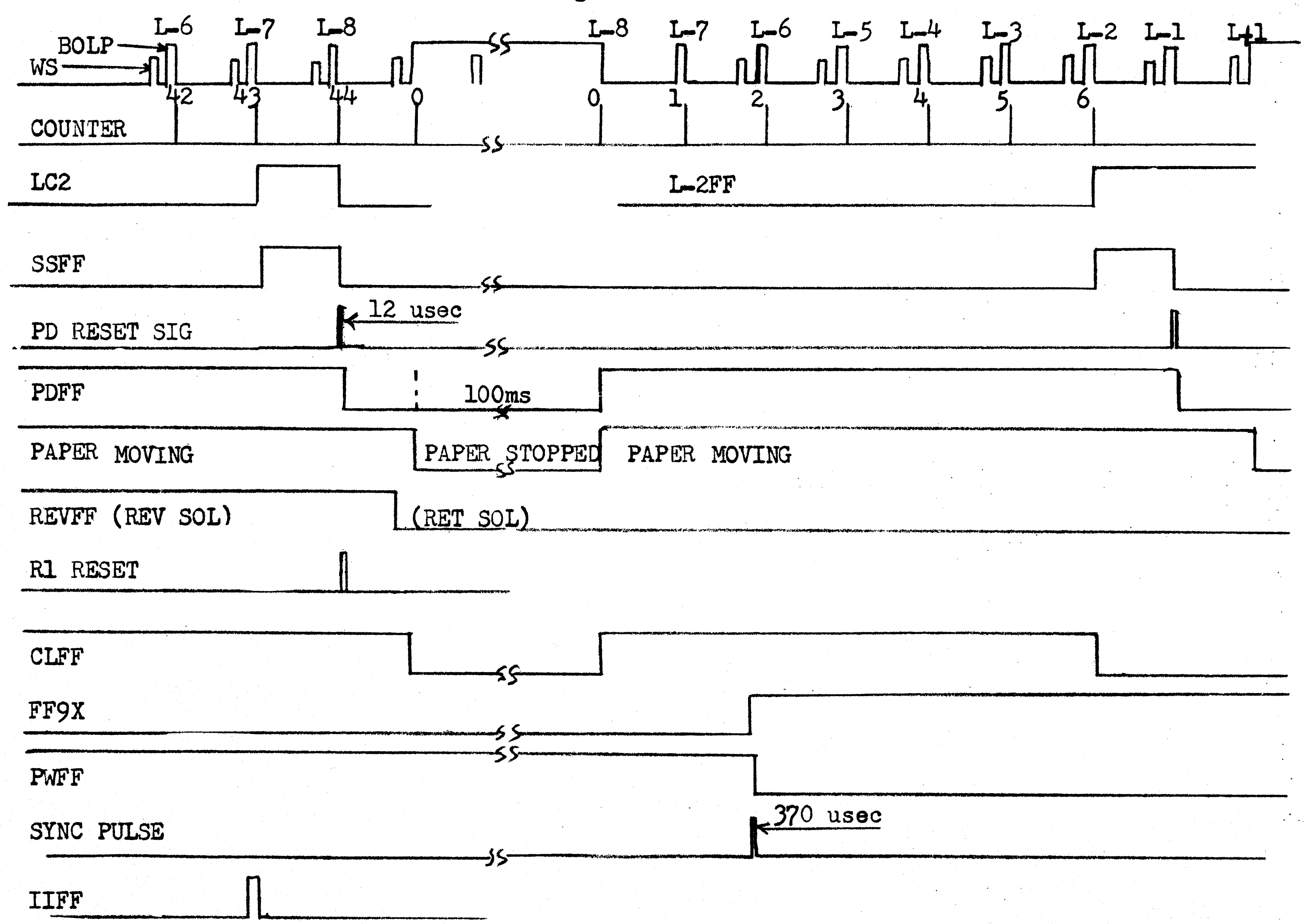


Figure V-4

NOT PDFF CC1 and CC3 provide a signal to reset the PDFF in the 0°, or home position.

STOP PD SOL The Stop PD Solenoid is energized by the NOT PDFF signal through a Paper Drive Clutch (PDC) circuit.

LBC The Lane Blank card signal is made when lanes 52 and 56 are programmed.

SL The Striped Ledger signal is made high by the LBC signal. This indicates that a Striped Ledger operation is to be performed.

LU SL The SL and NOT Printer Operate (POFF) causes the LOCK Relay to be picked. This forces the operator to insert a form in a BC position.

FPS The Front Paper Switch signal is made high when a form is inserted into the machine and breaks the beam of light.

SET BCFF The Blank Card FF is set by LBC.CC3.NOT ERFF.FPS

SET CRG MTRFF The carriage motor FF is set to allow the carriage motor to be started.

SET PROG CAM FF The PROG CAMFF is set by the NOT AR ON.SL.CC3.NOT ERFF.FPS.CC1. NOT LOCK signals. The NOT AR ON signal is high when the Auto Reader is not being used.

CRG LOCK SOL The Carriage Lock Solenoid will be energized by the FPS and NOT ECNC signal through a solenoid driver. This solenoid blocks the depression of the carriage open and close key to prevent the operator opening or closing the carriage and removing the form. This ensure the new information will be written into the stripes as the form is driven out of the carriage on the write operation.

PICK CRG MTR RELAY The Carriage Motor Relay K1109 is picked by the CRG MTR FF signal through a SD. The CRG MTR RELAY complete the circuit to start the carriage motor.

PROG CAM SOL The program cam solenoid is energized by the PROG CAM FF and a SD.

CC2 The Program Camshaft cycles to 95° and CC2 is made high. The basic purposes of CC2 is to provide on R1 reset pulse and reset the PROG CAM FF. The R1 Pulse resets a number of FF each time it is triggered. There is no time when all of these FF's are significient at once. At this time, the FF9X is significient.

RESET 9YFF The 9YFF is reset by the R1 pulse from the reset standardizer. This allows the right stripe to be oriented.

RESET 9XFF The 9XFF is reset by CC2.CK just prior to the start of form movement. This insures that the middle stripe is properly oriented.

SET REVFF The Reverse FF is set by CC3•CC2•NOT EJECT•CLK.

RESET COUNTERFF's A Reset Standardizer is triggered by CC2 which causes the Counter FF's to be reset. This is in preparation for counting the lines as the form is driven into the carriage.

100ms DMV CC2•CC3 triggers the 100ms DMV. This delay provides time for positioning the shuttle clutch.

RESET PROG CAMFF CC2•NOT•EJFF•CLK Resets the Program Cam FF and drops the Program Cam solenoid. The camshaft will detent at 144°.

DROP PROG CAM SOL Resetting PROG CAMFF drops PROG CAM SOL.

ENERGIZE REV SOL The Reverse solenoid is energized to shift the shuttle gear to drive the form into the carriage.

LF WRITE AMP The Line Find write amplifier is turned on by BCFF•REVFF•NOT WLFF • NOT ALIGN and orients the line find stripe.

SET PERMIT WRITE FF The Permit Write FF is set by BCFF•REVFF•CC3 and CLK. PWFF enables orienting the data stripes.

WRITE X AMP The X write amplifier is energized to orient the stripe by NOT FF9X• PWFF.

WRITE Y AMP The Y write amplifier is energized to orient the stripe by NOT FF9Y• PWFF.

SET PDFF Sig. When the 100ms DMV times out a SET PDFF signal is provided.

SET PDFF The Set PDFF signal and clock sets the PDFF. The cam shaft at this time is at 144°.

SET CLFF The Count Ledger FF is set in preparation for counting the lines as the form is driven into the carriage. It is set by SET PDFF•REVFF• BCFF•NOT LWLFF•CLK.

ENERGIZE PD SOL The paper drive solenoid is energized by the PDFF•CRG OPEN•NOT TAB signals through a paper drive clutch circuit. The CRG OPEN Signal is high when the carriage is open and prevents the paper drive pressure rolls being engaged if the carriage is closed. The paper drive clutch circuit operates at 120V and reduces the voltage to hold voltage (approx. 25V) after a predetermined time. (30ms)

COUNTER and COUNT PULSES (Figure V-3) the counter FF's count the lines on the form and signal the logic section when the form has reached certain points during various SL operations. In the BC operation, the counter must first signal the logic when sufficient length of the stripes has been oriented. The signal which causes the counter to advance is obtained from a solar cell activated from the 1/10 wheel disc. This signal must be timed and synchronized with the USMV pulses before it is used by the counter. The circuits and signals are shown below.

370 USEC DMV The 370 usec DMV provides a series of 16.5 usec pulses which are 370 usec from leading edge to leading edge.

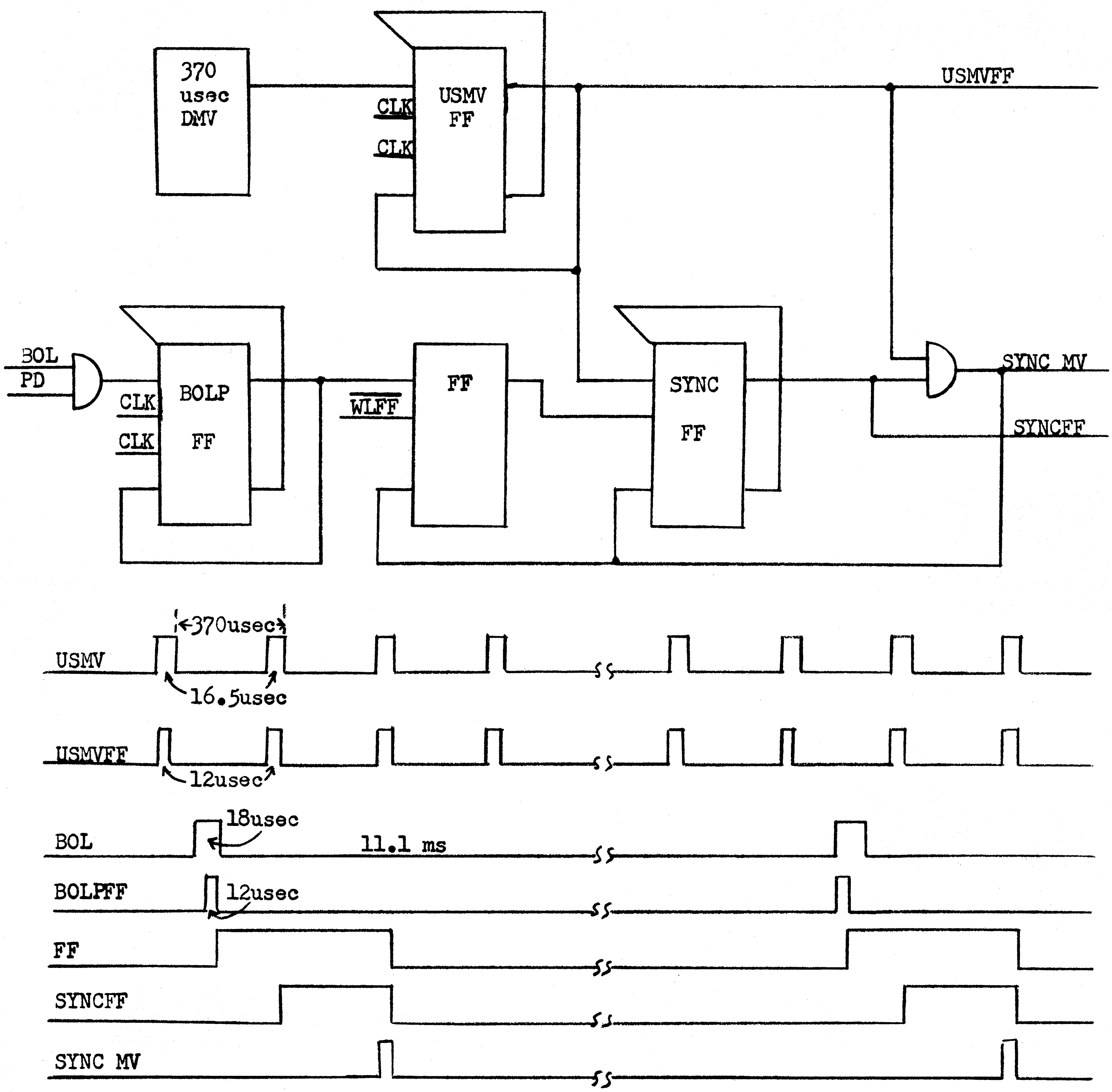

370
usec
DMV
USMV
FF
CLK
CLK
USMVFF
BOL
PD
CLK
CLK
BOLP
FF
WLFF
FF
SYNC
FF
SYNC MV
SYNCFF
370usec
USMV
16.5usec
USMVFF
12usec
18usec
BOL
11.1 ms
BOLPFF
12usec
FF
SYNCFF
SYNC MV

Figure V-3

USMVFF The USMVFF Synchronizes the USMV pulses with clock and provides a 12 usec pulse.

BOL The BOL pulse is an 18 us pulse generated by the solar cell and 1/10 wheel disc.

BOLP BOLP is a 12 usec pulse which is BOL synchronized with clock by the BOLPFF.

FF FF is set by BOLP•NOT WLFF FF. It will be on at least 370 and not more than 740 usec. The FF signal allows the BOLP and USMVFF to be synchronized by the SYNCFF FF is reset by SYNC MV.

SYNC FF The SYNC FF provides a 370 usec pulse to be gated with USMVFF to provide the SYNC MV Pulse. SYNC FF is reset by SYNC MV.

SYNC MV The SYNC MV Pulse is a 12 usec pulse which occurs every 11.1 ms. SYNC MV is used to count the counter FF's.

LC2 (Figure V-4) the ledger count 2 signal is made high by the CC4 and counter output 43 being high. (43 for 11" form or 61 for 14" form) This will occur at line minus 6, or 6 spaces above the first printing line.

R1 RESET The LC2 signal gates a R1 Pulse. The purpose of R1 at this time is to reset the CLFF.

SET SSFF The Stop Storage FF is set by the LC2 signal CLK and indicates that the paper drive is to be stopped.

RESET PDFF Signal SSFF BOLP causes the RESET PDFF signal to be high. This is controlled by BOLP and insures that the clapper will be dropped in the proper relation to the lugs on the clutch so that a positive line will be selected.

RESET SSFF RESET PDFF sig. CLK resets SSFF.

RESET PDFF The PDFF is reset by the RESET PDFF signal• NOT EJFF • CLK.

RESET COUNTERS The counter FF are reset by their Reset Standardizer. The RS is triggered by RESET PDFF signal REVFF.

ENERGIZE STOP PD SOL The NOT PDFF signal triggers the PDC circuit to energize the stop paper drive solenoid. The Stop paper drive solenoid moves the clapper into the path of a tooth on the 1/10" wheel. The PDC circuit operates at 120V and after a predetermined time (30ms) reduces the voltage to a hold voltage (25V).

RESET REVFF The REVFF is reset by WS•NOT PDFF•CLK.

ENERGIZES RET SOL The RET SOL is energized by NOT REVFF•CC1•CC4 through a SD. The RET SOL moves the shuttle clutch so that the form will be driven out when the PD clutch is again energized.

100ms DMV The 100ms DMV is triggered by RET•NOT PDFF•NOT L-2FF•NOT ERFF. The 100ms delay allows time for the shuttle gear to be positioned by the RET SOL. Form travel will stop with the form at L-8 and the machine waits for the 100ms DMV to time out.

SET PDFF Signal The 100 ms DMV provides the set PDFF signal.

SET PDFF The PDFF is set by PDFF signal and clock.

SET CLFF The count ledger FF is set by SET PDFF•RET•NOT L-2FF•CK, CLFF must be set so that a count can be made as the form moves from line minus 8 to the first printing line.

ENERGIZE PD SOL The paper drive solenoid is energized by PDFF•CRG OPEN•NOT TABFF through the PDC circuit. This will cause the form to be driven out. The counter FF are counted by the SYNC MV pulses. The generation of these pulses were discussed earlier. The counter counts lines as the form moves out from line minus 8.

SET FF9X FF9X which controls the direction of current flow through the head on the center stripe is set by USMVFF•PDFF•NOT REVFF•NOT L-2FF•NOT FF9X•WS•CK. The WS pulse is triggered by the BOL (V2010) circuit and is 400 to 700 usec long.

SET FF9X (continued) This ensures covering at least one USMVFF pulse. The WS pulse is initiated by the leading edge of the hole and will not be triggered by the hole at L-8. The WS pulse is delayed approximately 9 ms after the pulse is triggered. This causes the sync pulse to be written on the stripe between line minus 6 and line minus 7.

WRITE SYNC CC4•FF9X•USMVFF•CK resets the PWFF at the USMVFF pulse following the setting of FF9X. Thus the sync pulse written during a Blank Card operation consist of two reversals of flux written 370 usec apart. The PWFF is turned off at this time to prevent a flux reversal occuring when the form is stopped at the first printing line.

L-2FF When the form has been driven out six spaces, the counter will equal 6. RET•6•CLK sets L-2FF.

RESET CLFF The count ledger FF is reset by 6•L-2FF•CK. There is no more need to count pulses on the Blank Card operation.

SET SSFF The Stop Storage FF is set so that paper drive can be stopped. SSFF is set by BCFF•CC4•L-2FF•CLK.

LF SIG. The Line Find signal is made high by BCFF•CC4•L-2FF.

SET PRINTER OPERATE FF The POFF is set as an indication that the form handling is completed and the control console can be operated. LF•NOT REVFF triggers a PS whose output and NOT ERFF•CLK will set POFF.

RESET PDFF SIG. The SSFF and the following BOLP are gated together to produce the RESET PDFF SIG.

RESET SSFF RESET PDFF Sig CLK resets SSFF.

RESET PDFF The PDFF is reset by the RESET PDFF sig• NOT EJFF•CLK.

ENERGIZE STOP PD SOL The NOT PDFF triggers the PDC circuit to ENERGIZE the STOP PD SOL. This solenoid lowers the clapper into the path of the tooth on the clutch wheel.

ENERGIZE MB#2 SOL If an automatic cycle is to be made, the AUTO CYCLE signal from the keyboard key is high. The AUTO CYCLE•POFF•BCFF signals are gated with a 100ms pulse from a DMV (which is triggered by POFF) to activate Motor Bar 2 solenoid trips the drive in the same manner as the depression of Motor Bar 2.

RESET POFF The POFF is reset by TC10 and a clock pulse at 220° of the console cycle.

SET PROG CAM FF When TC10 is made at 220°, the CC1•CC4•TC10•CLK signal will set the program Cam FF.

PROGRAM CAM SOL The program cam solenoid is energized by the Program Cam FF through a SD. The program camshaft must be rotated to 216° for posting from media or for other arithmetic operations.

RESET PROG. CAMFF The program Cam FF is reset by CC2•NOT EJFF•CLK. CC2 is made briefly at 180° of the camshaft. When the PROG CAMFF is reset, the PROG CAM SOL will be dropped to allow the camshaft to detent at 216°.

RESET CRG MTRFF The Carriage Motor FF is reset by CC4•CC2•NOT•EJFF•CLK. This allows the carriage Motor relay to drop. The drop time of the relay and the coasting of the motor after the circuit opens turns the camshaft to 216°.

R1 RESET CC2 gates an R1 pulse which has no significance at this time. At this point the Blank Card operation is complete. The stripes have been oriented to receive data and line find information as the form is driven into the machine. The sync pulse has been written and the printing line has been found. The machine is now ready for posting or other arithmetic operations which are E2100 functions. The next form handling operation to be discussed will be the write ledger operation.

BLANK CARD PAPER HANDLING

R1 RESETS FFs

LFBFF	LFAFF
FF16	FF4
CLFF	FF
SYNCFF	VFF
PARITYFF	FF3Y
DISC XFF	DISC YFF
CPFF	FF9Y
FF1X	FF1Y
DATA XFF	DATA YFF
SRCXFFs	SRCYFFs

INITIAL CONDITIONS	
$\overline{\text{TABFF}}$	305
$\overline{\text{PDFF}}$	305
STOP PD SOL	305
LBC (L56 and L52)	135
SL	305
LU SL	319

Condition		Action	
INSERT FORM		FPS	323
FPS•LBC•CC3•$\overline{\text{ERFF}}$•CLK		SET BCFF	320
$\overline{\text{LOCK}}$•FPS•SL•CC3•$\overline{\text{ERFF}}$•CLK		SET CRG MTR FF	304
FPS•SL•CC3•CC1•$\overline{\text{ARON}}$•$\overline{\text{ERFF}}$•CLK		SET PROG CAM FF	304
$\overline{\text{ECNCFF}}$•FPS	SD	CARRIAGE LOCK SOL	513
CRG MTR FF	SD	PICK CRG MTR RELAY	102
PROG CAM FF	SD	PROG CAM SOL	322
CAMSHAFT CYCLES TO 95 DEGREES		CC2	303
CC2		R1 RESET	307
CC2•CLK		RESET FF9X	311
CC2•CC3•$\overline{\text{EJFF}}$•CLK		SET REVFF	305
CC2	SD	RESET COUNTER FFs	308
CC2•CC3		TRIGGER 100ms DMV	305
REVFF	SD	ENERGIZE REV SOL	322
REVFF•A•BCFF•$\overline{\text{LWLFF}}$		LF WRITE AMP	306
REVFF•BCFF•CC3•CLK		SET PWFF	310
PWFF•$\overline{\text{FF9X}}$		WRITE AMP X	316
PWFF•$\overline{\text{FF9Y}}$		WRITE AMP Y	316
100ms DMV times out		SET PDFF Sig	305

Figure V-5A

(Draft E2150)

SET•PDFF Sig•CLK		SET PDFF	305
SET PDFF Sig•REVFF•BCFF•$\overline{\text{LWLFF}}$•CLK		SET CLFF	307
PDFF•CGE OP•$\overline{\text{TAB}}$	PDC	PICK PAPER DRIVE SOL	322
PD•BOL		BOLP	323
$\overline{\text{WLFF}}$•BOLP		SET FF	308
FF•USMVFF		SET SYNCFF	308
SYNCFF•USMVFF		SYNC MV	308
SYNC MV•CLFF		ADVANCE COUNTER FFs	308
SYNC MV		RESET FF	308
		RESET SYNCFF	308
COUNT 43•CC4		LC2	307
LC2		R1 RESET	307
		RESET CLFF	307
LC2•CLK		SET SSFF	305
SSFF•BOLP		RESET PD Sig	305
RESET PDFF Sig•PD•$\overline{\text{EJFF}}$•CLK		RESET PDFF	305
RESET PDFF Sig•PD•REVFF	PS	RESET COUNTERFF s	308
$\overline{\text{PDFF}}$	PDC	PICK STOP PD SOL	305
WS•$\overline{\text{PDFF}}$•CLK		RESET REVFF	305
$\overline{\text{REVFF}}$•CC1•CC4	SD	PICK RET SOL	305
RET•$\overline{\text{PDFF}}$•$\overline{\text{L-2FF}}$•$\overline{\text{ERFF}}$		TRIGGER 100ms DMV	305
100ms DMV times out		SET PDFF Sig	305
SET PDFF Sig•CLK		SET PDFF	305
SET PDFF Sig•RET•$\overline{\text{L-2FF}}$•CLK		SET CLFF	307
PDFF•CRG OP•$\overline{\text{TAB}}$	PDC	PICK PAPER DRIVE SOL	322

Figure V-5B

$\overline{\text{WLFF}}$•BOLP	SET FF	308
FF•USMVFF	SET SYNCFF	308
SYNCFF•USMVFF	SYNC MV	308
SYNC MV	RESET FF	308
SYNC MV	RESET SYNCFF	308
SYNC MV•CLFF	ADVANCE COUNTERFFs	308
WS•USMVFF•PDFF•$\overline{\text{REVFF}}$•$\overline{\text{L-2FF}}$•$\overline{\text{FF9X}}$•CLK	SET FF9X	311
FF9X•PWFF	WRITE SYNC PULSE	316
USMVFF•FF9X•CC4•CLK	RESET PWFF	310
6•RET•CLK	SET L-2FF	306
6•L-2FF•CLK	RESET CLFF	307
L-2FF•BCFF•CC4•CLK	SET SSFF	305
L-2FF•BCFF•CC4	LF SIGNAL	305
LF•$\overline{\text{REVFF}}$ — PS — $\overline{\text{ERFF}}$•CLK	SET POFF	307
$\overline{\text{LU SL}}$	DROP LOCK RELAY	319
SSFF•BOLP	RESET PDFF Sig	305
RESET PDFF Sig•$\overline{\text{EJFF}}$•CLK	RESET PDFF	305
$\overline{\text{PDFF}}$ — PDC	PICK STOP PD SOL	305
POFF — 100ms DMV — AUTO CYCLE•BCFF•POFF	ENERGIZE MB2 SOL	307
TC10 (220)'• CLK	RESET POFF	307
TC10 (220)'• CC1•CC4•CLK	SET PROG CAMFF	304
PROG CAMFF — SD	PICK PROG CAM SOL	322
CAMSHAFT TURNS TO 216 DEGREES	CC2	303
CC2•$\overline{\text{EJFF}}$•CLK	RESET PROG CAMFF	322
CC2•CC4•$\overline{\text{EJFF}}$•CLK	RESET CRG MTRFF	304
CC2	R1 RESET	307

Figure V-5C

R1 RESET (continued) If the Initial Installation (II) operation is programmed (lanes 56, 52 and 51) the operation will be performed while the form is being fed into the machine. The operation will begin when the LC2 signal becomes high at a count of 43.

INITIAL INSTALLATION

In the initial installation, the balances must be manually entered on the keyboard and transferred to the stripe. This operation consists of a Blank Card operation, as described in the previous subject, and a logic operation which is initiated by pining lane 56 (Striped Ledger) 52 (Blank Card) and 51 (Initial Installation).

INITIAL INSTALLATION OPERATION

The logic operation begins when LC2 signal becomes high. LC2 is made up of CC4 and a counter output of 43. This occurs when the form is driven into line minus six. The purpose of the logic operation is to clear the active memory location prior to entering data from the keyboard.

Sequences A, B, C and 10 are used on this operation. During the logic operation, all 10 memory locations 20 through 29 are cleared Single Stripe (SS) and 20 memory locations 20 through 29 and 30 through 39 are cleared if the machine is Dual Stripe (DS).

In a SS machine, the DD is stepped in each SC as the data is read from succeeding digits. In a DS machine, the DD is stepped every other time SC is on because of the NOT FFZ signal. This allows the data to be read from any given DD in the 20's and 30's. MART1FF will be counted (Set or Reset) in SC to enable the DD of both memory locations to be read before the DD is stepped.

INITIAL CONDITIONS

BCFF — BCFF will be set from the BC operation.

IIFF — Initial Installation FF is set by L51, SET BCFF signal and CLK.

DDO — The R1 reset pulse reset all the DDFFs. This selects DDO.

FF6 — FF6 is set by clock and a pulse standardizer pulse produced by the change in LC2 when a count of 43 is reached. The PS allows the FF6 to be set only once due to the high LC2 signal. FF6 is reset by its own signal after one clock duration and provides a 12 usec pulse to initiate the logic sequence.

RESET FFZ (DS) — FFZ is used only on DS machines and is reset by FF6. On SS machines, FFZ is not installed.

SA — Sequence A in the E2150 machines (striped ledger) serves the same purpose as SO on the E2100 machine, that is, to set or reset control FF's for the operation.

RESET DDREV — Memory digits are to be read in the DDO to DDMSD order and DDREV must be reset.

2 → MART — The MART2FF is set to select the tens part of memory address 20.

0 → MARU — The MARUFF's are all reset. This selects the units part of memory address 20.

SET CAD — The "C" Memory Address is set so that C memory locations can be read in SB.

RESET MART 4 — MART 4 is reset to ensure that the operation does not start in memory address 60.

RESET COMPFF — All data is handled in true form during this operation and the COMPFF must be reset.

0 → WR — The WR is set to zero so that there will be no interference in the adder as the memory address units are counted in S10.

SB DDO through DDMSD

READ The selected digit of the active memory location is read into the MR. The memory location remains clear since the data is never written back into memory.

COMPLEMENT FFZ (DS) FFZ is complemented if the machine is dual stripe.

SD - DDO through DDMSD

SET SEQ B The logic returns to Seq B until the DD is stepped to DDMSD.

STEPDD Since NOT FFZ is floating on SS, the DD will be stepped each time SC is on. On a DS, the DD will be stepped every other time SC is on.

COUNT MART The MART is counted only on DS operations.

SEQ 10 When the DD has stepped to DDMSD, the logic goes to SEQ 10 rather than SEQ B. SEQ 10 provides a means of counting or stepping the memory address from 20 through 29.

SET CIFF The CIFF is set by DDMSD to provide a 1 input to the adder to count the memory location in SEQ 10.

S10 - DDO 0→MR The negative swing of the NOT S10 FF signal, as the S10 FF is set, triggers a reset or zero of the MR. This is an exception to the rule of action taking place at the end of a sequence and the MR is set to zero during the sequence.

RESET CiFF The carry in FF is reset by the first clock pulse after S10FF is set. CiFF is used to advance the MARU and to select the next sequence.

SET SEQ10 CiFF will be reset by the trailing edge of the first clock pulse during S10, therefore, S10FF will remain set for two clock durations.

GT MARU ADDER The output of the MARUFF's is gated to the adder through the T/C circuit.

GT ADDER MARU The adder output (The sum of the MARU and CiFF) is gated to the MARU by CiFF.

S10 - DDO (2nd clock duration) The fact that S10FF remains on two clock durations, is not significient for this operation but is necessary to make the operation compatable with future products.

0 →MR Not significient at this time.

RESET CiFF The CiFF was reset by the first clock pulse.

SEQ 10 SEQ 10 FF is not set again since CiFF is reset.

GT MARU ADDER Not significient at this time.

GT ADDER MARU CiFF is reset and the adder is not gated to the MARUFF's.

SEQ B NOT CiFF returns the logic to sequence B. Memory location 20 has been cleared and memory location 21 selected (SS). Memory 20 and 30 has been cleared on DS. This process is repeated for each memory location until 29 is reached. When the logic has reached S10 of memory location 29, the following gate ends the logic operation.

RESET IIFF The Initial Installation FF is reset by CiFF MARU-9 at the first clk during S10. At the second clock pulse of S10, CiFF and IIFF are both reset and no sequence FF is set which ends the operation. The Ending operation is the same for DS machines. Memory locations 20 through 29 and 30 through 39 will be cleared at the end of the operation.

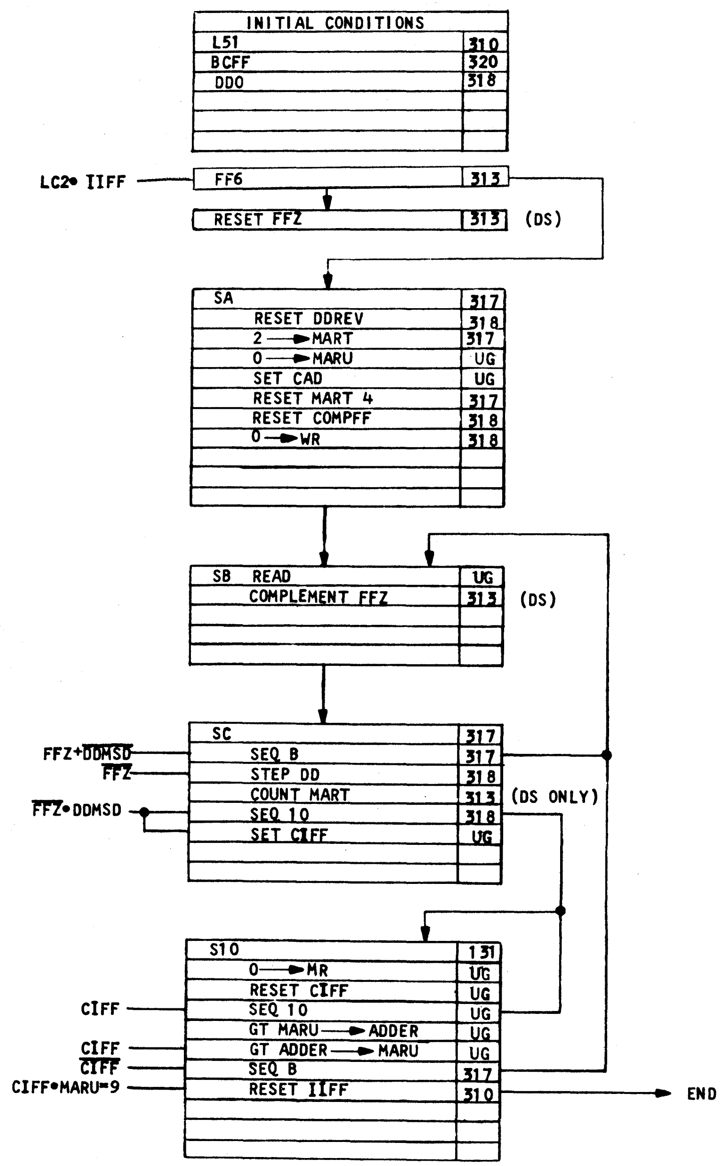


Figure V-6

NOTE:
"UG" REFERS TO UPPER GATE SCHEMATIC

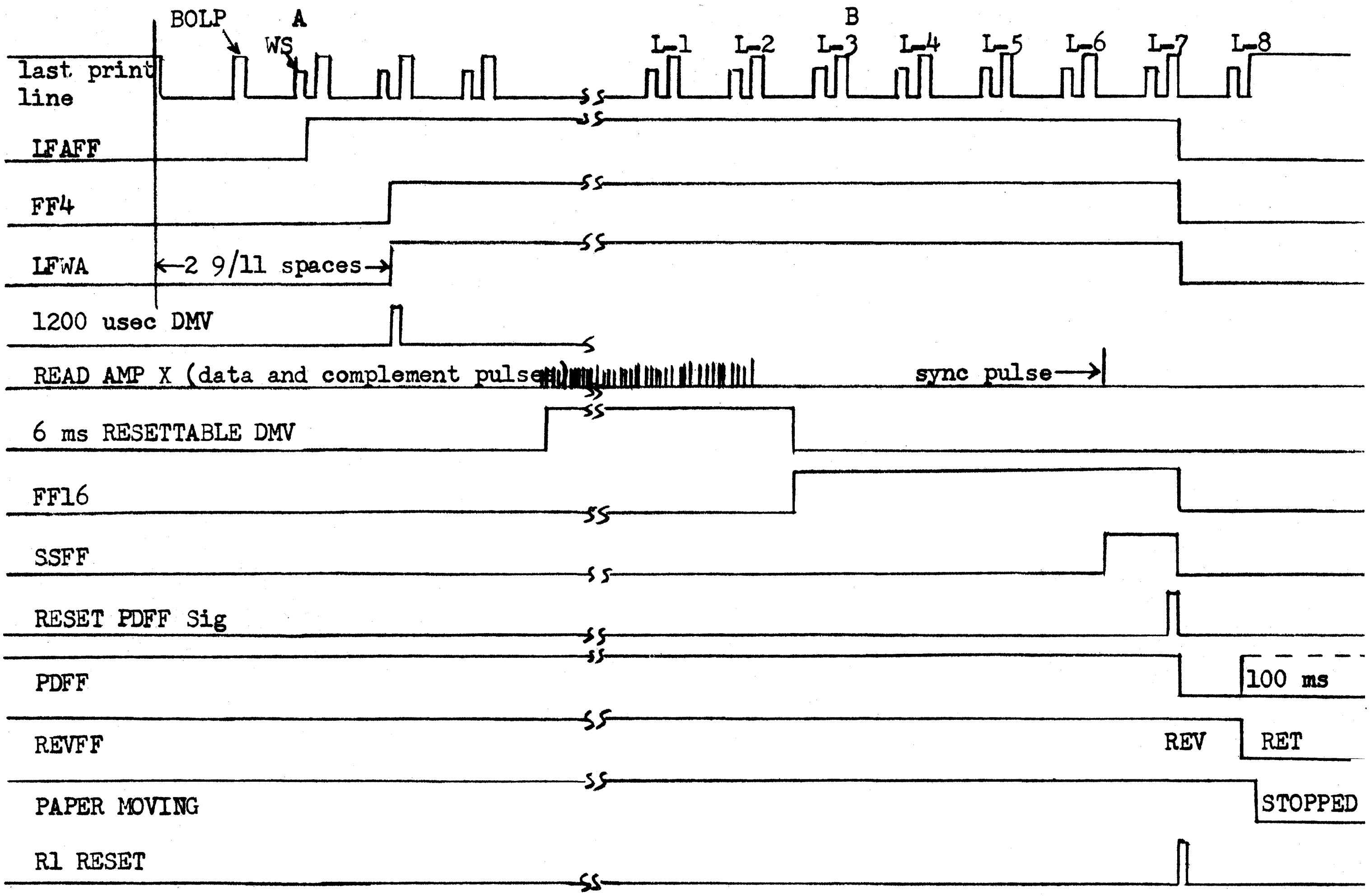
WRITE PAPER HANDLING

After posting and arithmetic has been completed by the operator, the results of the computations must be encoded on the stripes. The form travel during this operation is from the printing line where posting is completed into the machine to line minus eight and out until the form is completely out of the machine, see Figure V-7A. The line find information is encoded as the form is driven into line minus eight. Data is written in the stripes as the form is driven out of the machine. Data writing starts when the form has been driven out to the L-2 position. Writing continues until all programmed words have been written. If ten words are to be written, writing will continue for approximately 5.8" on the striper. If fewer words are to be written, the write on the stripes will be corresponding shorter. The letters A through F at the top of portions of the signal chart refer to areas as indicated on the line drawing of paper travel. For example, the signals under "A" refers to the writing of the line find pulse and occur at the start of form travel.

The Write Ledger Carriage position must be programmed with a Write Ledger pin. The units of memory address lanes must also be programmed with the highest memory location to be written on the stripes i. e. If four words are to be written, the units lanes must be programmed with a3. This will cause 23, 22, 21 and 20 to be written. A carriage open pin must also be programmed.

The paper handling operation will not start until the carriage has tabulated into the position following the write ledger position. The units of memory address and the Lane Write Ledger (LWL) flip flops must be set in the write ledger position before tabulation begins.

WRITE PAPER HANDLING



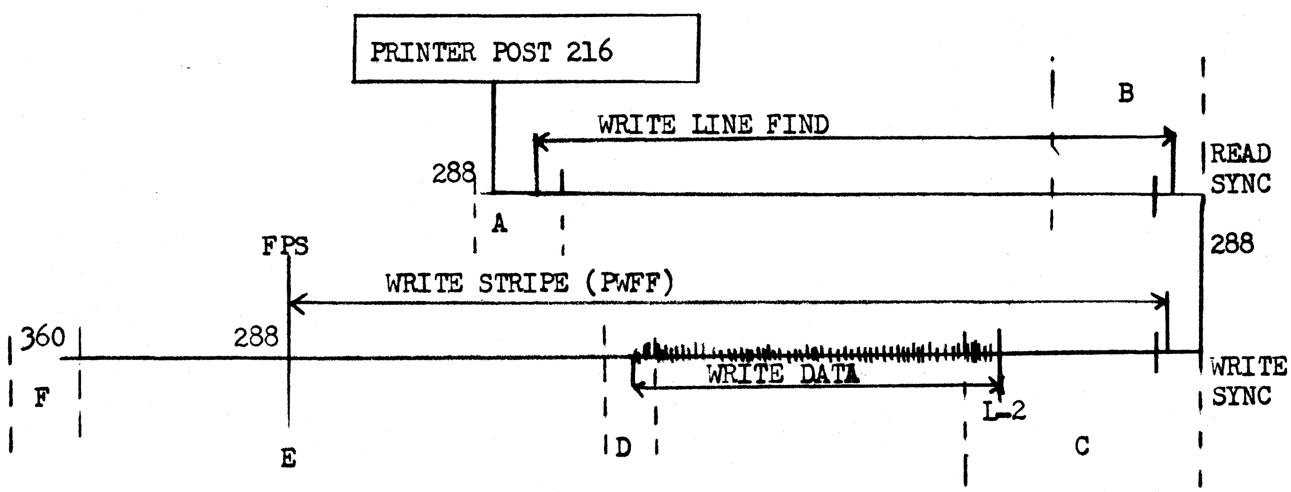


Figure V-7A

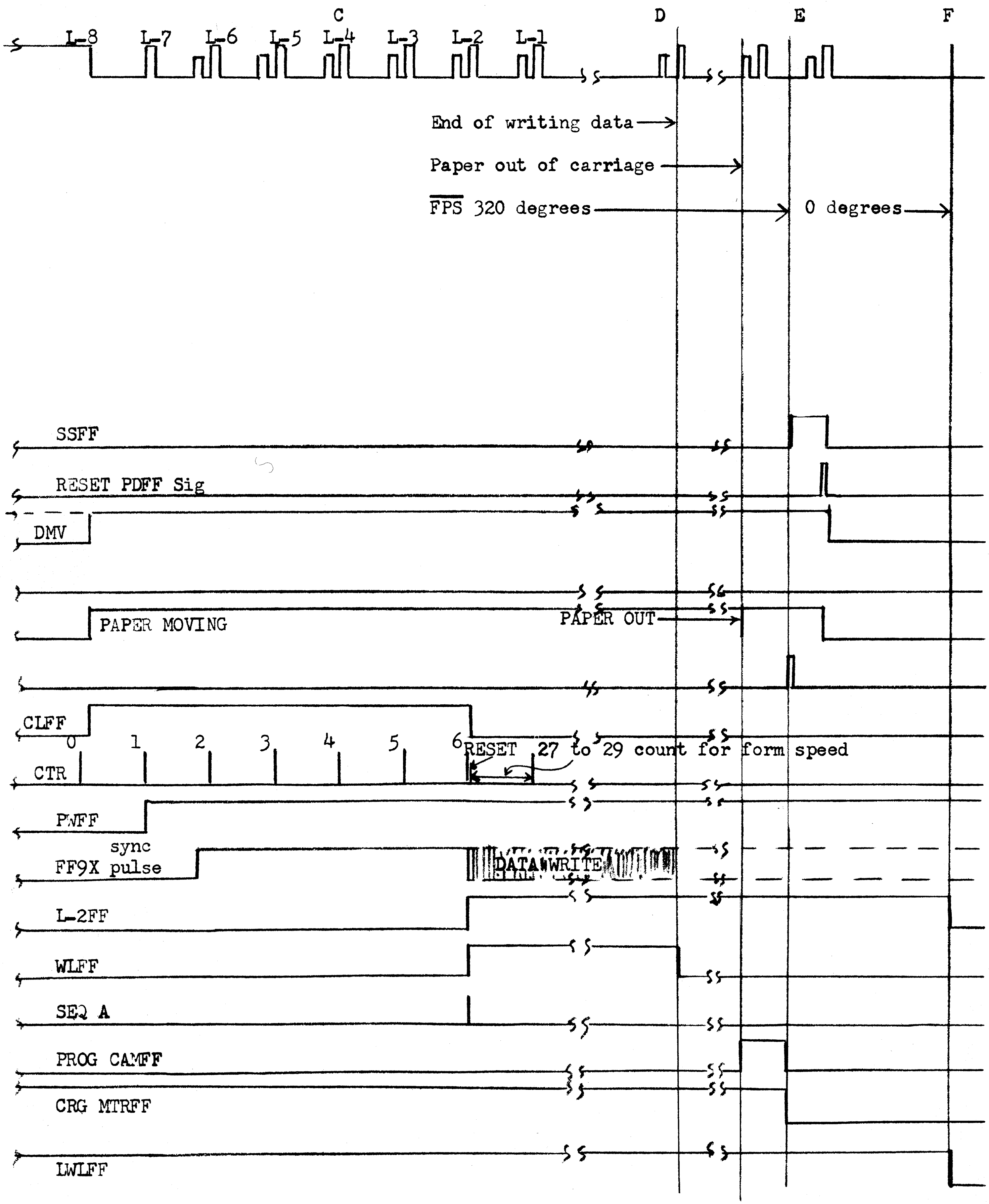

C
D
E
F
L-8
L-7
L-6
L-5
L-4
L-3
L-2
L-1
End of writing data
Paper out of carriage
$\overline{\text{FPS}}$ 320 degrees
0 degrees
SSFF
RESET PDFF Sig
DMV
PAPER MOVING
PAPER OUT
CLFF
0
1
2
3
4
5
6
RESET
27 to 29 count for form speed
CTR
PWFF
sync
FF9X pulse
DATA WRITE
L-2FF
WLFF
SEQ A
PROG CAMFF
CRG MTRFF
LWLFF

Figure V-7B

SET MARUFFs — See figure V-9. The MARU FFs will be set by delta MR at the start of the electronic cycle in the write ledger position.

SET LWLFF — The stop position where the write ledger is initiated must be pinned with a lane write ledger pin (LWL). The LWL•CC5•CLK signal sets the LWLFF.

SET CRG MTRFF — The LWL•CC5•CLK signal sets the CRG MTR FF.

ENERGIZE CRG MTR RELAY — The CRG MTRFF activates a SD to energize the CRG MTR RELAY which complete the circuit to the CRG MTR. The CRG MTR supplies power to drive the paper handler mechanism.

SET PROG CAM FF — The Prog Cam FF is set by LWLFF•TC10•NOT ERFF•CC1•CLK signals. The FF is set at 220° of the console cycle in the write ledger position.

ENERGIZES PROG CAM SOL — The Prog Cam SOL is energized by the Prog Cam FF signal and a SD. The program shaft will turn to 288°. This will lower the read/write heads to the stripes and allow the pressure rolls to grip the form. CC2 will become high for a short time at 250° of the Program camshaft cycle.

R1 RESET — CC2 provides a R1 reset at 250° of the camshaft cycle.

RESET COUNTER — CC2 and CLK resets the counter flip flops.

RESET FF9X — FF9X is reset by CC2•CLK•NOT FF9X if it is set, in preparation for writing the sync pulse.

RESET FF3X — FF3X is used to end the write operation and must be reset at the start of the operation.

RESET SRXFFs and SRYFFs — These flip flops are reset by CC2 as a safety precaution.

RESET PROG CAM FF — CC2•NOT EJFF•CLK will reset the prog. cam FF at 250° of the camshaft.

DROP PROG CAM SOL — The resetting of the PROG CAM FF allows the Prog Cam Sol to drop and detent the camshaft to detent at 288°.

100 MS DMV — CC2•CC5 triggers the 100 ms DMV. The 100 ms DMV provides time to position the shuttle gear.

SET REVFF — CC2•CC5•NOT EJFF•CLK will set the REVFF at 250°.

ENERGIZE REV SOL — The REV SOL is energized by REVFF and a SD. The REV SOL positions the shuttle clutch so that the form will be driven into the machine.

SET PDFF Signal — When the 100 ms DMV times out the SET PDFF Signal is made high. The PDFF is set by the SET PDFF signal and CLK.

ENERGIZE PDSOL — NOT TAB•CRG OPEN•PDFF activates the PDC circuit which energizes the paper drive sol and then drops the voltage to hold voltage. The NOT TAB signal prevents the write ledger paper handling operation starting until the carriage has reached the next stop position. CRG OPEN ensures the operation will not start with the CRG closed.

BOLP/WS — The BOL FF is set by PD•V2010 to generate a BOLP for each line (hole is the disc). A WS pulse is also produced by the BOL Circuit. The WS pulse occurs 9ms after the BOLP.

SET LFAFF — The Line Find A FF is set by WS REVFF CC6 when form feed is started. BOLP/WS pulses are produced by the first hole after paper drive has started.

SET FF4 — The LWLFF•LFAFF•WS signal sets FF4 9 ms after the second line. LFAFF and WS are used to delay the writing of the line find pulse two and nine elevenths lines above the last printing line. This allows the form to reach proper speed and the clutch vibration to settle before the line find pulse is written.

LF WRITE AMP FF4 REVFF turn on the write amplifier.

1200 usec DMV The trailing edge of the NOT FF4 signal triggers the 1200 usec DMV.

When the LF write amplifier is turned on, the current in the LF head is reversed. This reversal of current causes changes in the magnetism in the air around the head. These magnetic changes are large enough to be picked up by the X read head and cause setting of the 6 ms resettable DMV. If the LF pulse is written 6ms or more before the X head starts reading data pulses, this is indicates in the signals of Figure V-7, the first data pulse is recognized as the sync pulse and form reversal takes place. The purpose of the 1200 usec DMV is to prevent the disturbance in the X head, due to switching the LF head current, setting the 6ms DMV. Data in the X stripe must be read as an indication of the position of the form so that the sync pulse can stop from feed and reverse the form travel. Once reading has started, a lapse of 6ms between pulse indicates the end of data and the next pulse read will be the sync pulse. The 6ms DMV is a resettable DMV and is reset by each data pulse read. At the end of data, the 6ms DMV will time out and set FF16.

SET FF 16 FF4●REVFF●NOT FF16●AMPX reset 6ms DMV at each AMPX pulse. 6ms after the last pulse the 6ms DMV output will become high. This signal and a clock pulse sets FF16. FF16 is an indication that the next pulse will be the sync pulse.

SET SS FF READ AMPX●FF16●CLK Sets the SSFF. SSFF gates the BOLP to stop for travel. SSFF is reset by RESET PDFF sig.

RESET PDFF Sig. SSFF BOLP cause the reset PDFF signal to be high.

RESET SL (R1) RESET PDFF●REVFF triggers a PS to cause an R1 reset pulse. This signal resets the FF's used to stop the paper drive.

RESET COUNTERS The counter FF's are reset by Reset PDFF signal and REVFF. A count of lines to find L-2 must be made as the form is fed out.

RESET PDFF The PDFF is reset by the RESET PDFF sign. NOT EJFF•CLK.

ENERGIZE STOP PAPER DRIVE SOL NOT PDFF activates the PDC circuit to energize the STOP PD SOL and then drop the voltage to a hold voltage level.

RESET REVFF The REVFF is rest by the NOT PDFF•WS•CLK.

TRIGGER 100ms DMV RET•NOT PDFF•NOT L-2FF•NOT ERFF triggers the 100ms DMV. After 100ms, the PDFF is set to drive the form out of the machine.

ENERGIZE RET SOL NOT REVFF activates a SD to energize the RET SOL.

SET PDFF Sig. When the 100ms DMV times out, the Set PDFF signal is made high.

SET PDFF The PDFF is set by SET PDFF sig. CLK.

ENERGIZE PD SOL PDFF and a SD energize the PD Sol.

SET CLFF The CLFF is set by RET•NOT L-2FF•SET PDFF•CLK. The CLFF allows the counter FF's to count lines so that a starting point for writing dates can be found.

BOLP/WS BOLP and WS pulses are developed by PD and Solar Cell circuits.

SET PWFF The permit write FF is set by NOT REVFF•LWLFF•BOLP•CLK at line minus seven. The PWFF allows writing on the stripe.

SET FF The FF is set by the BOLP signal when the NOT WLFF signal is high.

SET SYNC FF The SYNC FF is set by USMVFF•NOT SYNC FF•FF. The SYNC FF allows the first USMVFF pulse after a BOLP to be gated out. The pulse which is gated out resets the FF and SYNC FF's so that only one USMVFF pulse will be gated out. This is the SYNC MV pulse.

SYNC MV The Sync MV pulse resets the FF and SYNC FF's and with CLFF advances the counters.

ADVANCE COUNTERS The SYNC MV will advance the counter FF's when the CLFF signal is high.

SET 9XFF — The 9XFF is set by USMVFF•PDFF•NOT REVFF•NOT L-2FF•NOT 9XFF•CLK•WS. The Write Sync pulse is developed from the BOL circuit and causes the sync pulse to be written 9ms after line minus seven.

WRITE SYNC PULSE — The setting of the 9XFF is gated to the write amplifier by PWFF. The reversal of write current through the head produces a flux change on the stripe which is the sync pulse.

SET L-2FF — The L-2FF is set by NOT WLFF•2•4•RET•CLK. The L-2FF's used here is prepared for writing data on the stripe.

RESET CLFF — NOT WLFF•2•4•RET•CLK resets the CLFF. The counters will be used for checking form speed.

SET WLFF — The WLFF is set by LWLFF•CLFF•L-2FF•NOT REVFF•CLK. The WLFF starts the write ledger logic.

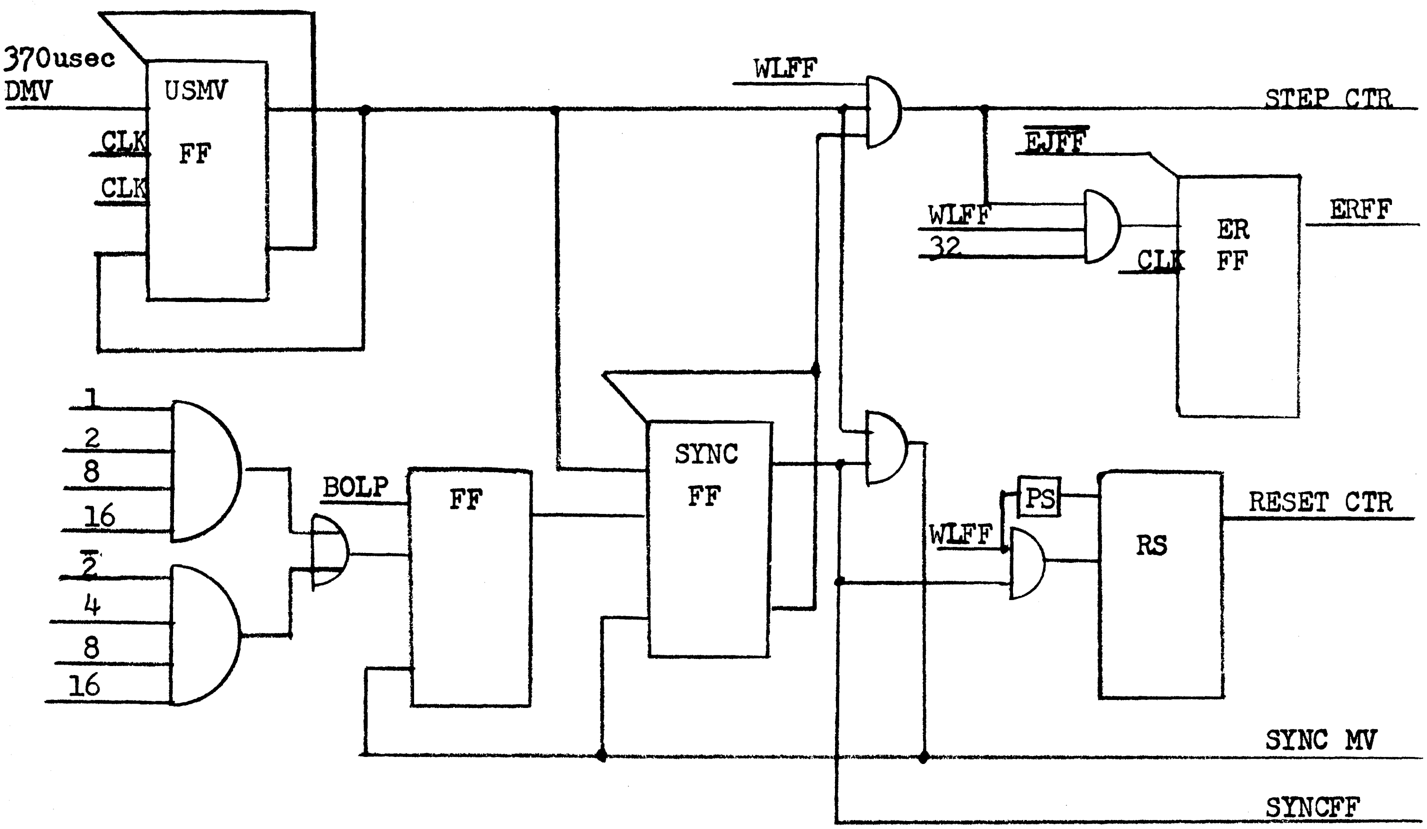
RESET COUNTERS — The counters are reset by WLFF, the change of WLFF through a PS.

SET SEQAFF — The SET WLFF sig• NOT SAFF•CLK sets SEQA FF. This starts the electronic operation for writing data on the stripe. This operation will be covered in detail following this subject. The form continues to be fed out as the data is written.

WRITE LEDGER LOGIC — The Write Ledger logic is controlled by USMVFF pulses. The speed of form movement during the Write Ledger operation is continuously checked during the write operation. The BOLP, which is developed by the paper drive mechanism, is compared to the USMVFF pulses, which control the writing of data on the form. Either 27, 28 or 29 USMVFF pulses must occur between any two BOLP's.

STEP CTR — Figure V-8, the Step counter signal is made high by USMVFF•WLFF• NOT SYNC FF. This produces a step counter pulse for each USMVFF pulse during writing except when the SYNC FF is set. These pulses advance the counter.

PAPER SPEED CHECK



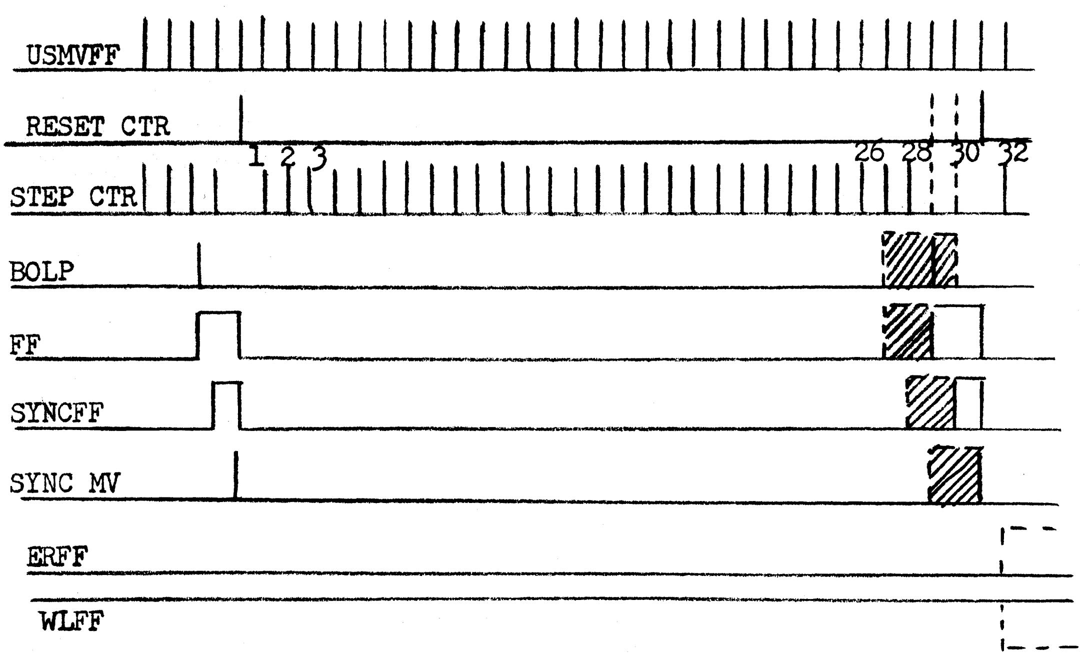


Figure V-8

SET FF — If a BOLP occurs while the counter is at 27, 28 or 29, the FF will be set. This indicates that the form is traveling at an acceptable speed.

SET SYNC FF — SYNC FF is set by FF•USMVFF•NOT SYNC FF being low inhibits the next STEP CTR pulse to prevent further counting.

SYNC MV — A SYNC MV pulse is gated out by SYNC FF being high.

RESET FF and SYNC FF — The SYNC MV pulse resets FF and SYNC FF.

RESET COUNTER — The counter FF's are reset by SYNC FF and WLFF.

An acceptable form speed has been recognized and the circuits reset for the count between the following BOLPs. If for some reason, the counter is not at 27, 28 or 29 when the BOLP occurs, it indicates that the form is not moving at the desired speed. It may be either too fast or too slow. If FF and SYNC FF are not set, the counters will continue to advance with each USMVFF pulse.

SET ERFF — A count of 32•STEP CTR•NOT EJFF•CLK sets the Error (ER) FF.

RESET WLFF — ERFF•CLK resets WLFF. This stops the writing of pulses on the stripes. Data remains in memory and another attempt to write can be made in the write error correction position. This operation will be discussed later. The write light will be on and the machine locked until the error correction procedure is followed.

RESET WLFF — The WLFF will be reset by the last complement pulse (CP) written on the ledger, the FF3X and CLK signal. FF3X is set by the logic to cause the start read data and complement pulses to be written.

SET PROG CAM FF — When the form is fed out of the carriage, the NOT FPS signal will be high. NOT FPS•CC6•L-2FF•CC1•CLK will set the PROG CAM FF.

ENERGIZE PROG CAM SOL	The Prog. Cam FF activates a SD to energize the PROG CAM SOL. The PROG CAM SOL will cause the program camshaft to rotate from 288° to 360°.
R1 RESET	CC2 gates an R1 pulse at 320° of the program camshaft cycle. This resets the control FF's after the write ledger operation is finished.
RESET FF9X	If FF9X is set, it is reset by CC2•NOT FF9X•CLK.
RESET FF3X	FF3X is reset by CC2•CLK after the write ledger operation is finished.
RESET PROG CAM FF	CC2•NOT EJFF•CLK resets the PROG CAM FF at 320°.
DROP PROG CAM SOL	The resetting of the PROG CAM FF drops the PROG CAM SOL so that the camshaft will detent at the 0° or home position.
RESET CRG MTRFF	The carriage motor FF is reset by CC2•CC6•NOT FPS at 320° of the cycle. The drop time of the relay and the speed of the motor will cause the camshaft to reach 0°.
DROP CRG MTR RELAY	The carriage motor relay is dropped when CRG MTRFF is reset.
SET SSFF	NOT FPS•CC2•CC6•CLK Sets SSFF. SSFF must be set so that the paper drive mechanism can be stopped. SSFF is reset by RESET PDFF Sig.
RESET PDFF sig.	SSFF BOLP produce a Reset PDFF signal.
RESET PDFF	The PDFF is reset by the RESET PD Sig• NOT EJFF•CLK.
ENERGIZE STOP PD SOL	NOT PDFF triggers the PDC circuit which energizes the STOP PD SOL.
RESET LWLFF	The Lane Write Ledger FF is reset by CC3•NOT ERFF•CLK when the camshaft reaches 0°. LWLFF must be reset to allow the operations pinned in the position to be performed. This is usually a Read Ledger (RL) position.

WRITE LEDGER PAPER HANDLING

R1 RESETS FFs

LFAFF	LFBFF
FF4	FF16
FF1X	FF1Y
FF3X	FF9Y
FF	SYNCFF
CLFF	VFF
PARITYFFs	CPFF
DISCXFF	DISCYFF
DATAXFF	DATAYFF
SRCXFFs	SRCYFFs

Condition		Action	Page
MARU LANES·ΔMR		SET MARUFFs	
LWL·CC5·CLK		SET LWLFF	306
		SET CRG MTRFF	304
CRG MTRFF	SD	ENERGIZE CRG MTR RELAY	304
LWLFF·TC10·$\overline{\text{LOCK}}$·CC1·CLK		SET PROG CAMFF	304
PROG CAMFF	SD	ENERGIZE PROG CAM SOL	322
CC2		R1 RESET	307

Condition		Action	Page
CC2·CLK		RESET COUNTERS	308
CC2·CLK·$\overline{\text{FF9X}}$		RESET FF9X	311
CC2·CLK		RESET FF3X	313
CC2		RESET SRXFFs	319
		RESET SRYFFs	315
CC2·$\overline{\text{EJFF}}$·CLK		RESET PROG CAMFF	304
RESET PROG CAMFF		DROP PROG CAM SOL	322
CC2·CC5		TRIGGER 100ms DMV	305
CC2·CC5·$\overline{\text{EJFF}}$·CLK		SET REVFF	305
REVFF	SD	ENERGIZE REV SOL	322

Condition		Action	Page
100ms DMV times out		SET PDFF Sig	305
SET PDFF Sig·CLK		SET PDFF	305
PDFF·$\overline{\text{TAB}}$·CRG OP	PDC	ENERGIZE PD SOL	322

Condition		Action	Page
PD·BOL·CLK/WS		BOLP/ WS	323
PD·WS·REVFF·CC6		SET LFAFF	305
LWLFF·LFAFF·WS·$\overline{\text{FF4}}$		SET FF4	306
FF4·REVFF		LFWA	306
$\overline{\text{FF4}}$		1200 us DMV	306

Condition		Action	Page
$\overline{\text{1200us DMV}}$·REVFF·$\overline{\text{SSFF}}$·$\overline{\text{PWFF}}$·PD·DATA X		READ AMP X	316

Condition		Action	Page
FF4·REVFF·$\overline{\text{FF16}}$·READ·AMP X		6 ms RESETTABLE DMV	306

Condition		Action	Page
6 ms DMV·REVFF·FF4·CLK		SET FF16	306
FF16·READ AMP X		SET SSFF	305
SSFF·BOLP		RESET PDFF Sig	305
RESET PDFF Sig·REVFF		R1 RESET	307
		RESET COUNTERS	308

Figure V-9-A

RESET PDFF Sig.$\overline{\mathrm{EJFF}}$•CLK		RESET PDFF	305
$\overline{\mathrm{PDFF}}$	PDC	ENERGIZE STOP PD SOL	305

$\overline{\mathrm{PDFF}}$•WS•CLK		RESET REVFF	305
RET•$\overline{\mathrm{PDFF}}$•$\overline{\mathrm{L\text{-}2FF}}$•$\overline{\mathrm{ERFF}}$		TRIGGER 100ms DMV	305
$\overline{\mathrm{REVFF}}$	SD	ENERGIZE RET SOL	305

100 ms DMV times out		SET PDFF Sig	305
SET PDFF Sig•CLK		SET PDFF	305
PDFF	PDC	ENERGIZE PD SOL	305
RET•L-2FF•SET PDFF Sig•CLK		SET CLFF	307
BOL•PD / WS		BOLP/WS	323
REVFF•LWLFF • BOLP•CLK		SET PWFF	323
BOLP•$\overline{\mathrm{WLFF}}$		SET FF	308
FF•USMVFF		SET SYNCFF	308
SYNCFF•USMVFF		SYNC MV	308
SYNC MV		RESET FF	308
		RESET SYNCFF	308
SYNC MV•CLK		ADVANCE COUNTERFFs	308

USMVFF•PDFF•$\overline{\mathrm{REVFF}}$•$\overline{\mathrm{L\text{-}2FF}}$•WS•CLK•$\overline{\mathrm{FF9X}}$	SET FF9X	311
PWFF•FF9X	WRITE SYNC PULSE	316

2•4•RET•$\overline{\mathrm{WLFF}}$•CLK		SET L-2FF	306
2•4•RET•$\overline{\mathrm{WLFF}}$•CLK		RESET CLFF	307
LWLFF•CLFF•L-2FF•$\overline{\mathrm{REVFF}}$•CLK		SET WLFF	310
WLFF	PS	RESET COUNTERFFs	308
SET WLFF•$\overline{\mathrm{SAFF}}$•CLK		SET SEQ A	317
USMVFF		WRITE LEDGER LOGIC	326
USMVFF•WLFF•$\overline{\mathrm{SYNCFF}}$		STEP COUNTERFFs	308
(27 + 28 + 29) BOLP		SET FF	308
FF•USMVFF		SET SYNCFF	308
USMVFF•SYNCFF		SYNC MV	308
SYNC MV		RESET FF	308
		RESET SYNCFF	308
SYNCFF•WLFF		RESET COUNTERFFs	308

Figure V-9B

32•STEP CTR•$\overline{\text{EJFF}}$•CLK	SET ERFF	321
ERFF•CLK	RESET WLFF	310
LAST CP ON WRITE•FF3X•CLK	RESET WLFF	310
$\overline{\text{FPS}}$•CC6•L-2FF•CC1•CLK	SET PROG CAMFF	304
PROG CAMFF — SD	ENERGIZE PROG CAM SOL	322
CC2	R1 RESET	307
CC2•$\overline{\text{FF9X}}$•CLK	RESET FF9X	311
CC2•CLK	RESET FF3X	313
CC2•$\overline{\text{EJFF}}$•CLK	RESET PROG CAMFF	304
RESET•PROG•CAMFF	DROP PROG CAM SOL	322
CC2•CC6•$\overline{\text{FPS}}$	RESET CRG MTRFF	304
RESET CRG MTRFF	DROP CRG MTR RELAY	304
$\overline{\text{FPS}}$•CC2•CC6•CLK	SET SSFF	305
SSFF•BOLP	RESET PDFF Sig	305
RESET PDFF Sig•$\overline{\text{EJFF}}$•CLK	RESET PDFF	305
$\overline{\text{PDFF}}$ — PDC	ENERGIZE STOP PD SOL	305
CC3•$\overline{\text{ERFF}}$•CLK	RESET LWLFF	306

Figure V-9C

WRITE LEDGER LOGIC

The encoding of information on the stripe is accomplished with a series of complement and data pulses. A complement pulse is written every 740 usec or every .011" on the stripe. This divides the stripe into "cells". If data is to be written, it is encoded as a flux reversal between the complement flux reversals. The complement pulses provide a means of timing and also a means of recognizing the bit value of a data pulse. Writing of data on the stripe starts with the MSD of the highest memory location to be encoded. This is the memory location whose units must be pinned in the panel in the write ledger position. Since writing is always from the twenties group of memories it is not necessary to program tens. For example, if five words are to be encoded, the first digit encoded will be MSD of memory location 24, the second digit will be DD1 of memory location 24. Each digit of each memory location will be written in descending order until DDO of memory location 20 is reached. This will be the last data digit written on the form and consequently the first read or a READ operation. One additional data and one complement pulse is written after the last data digit. This data and complement pulse is the start signal for the RL logic operation. The write amplifier will remain on until the form is driven out of the machine. This orients the stripe so that a false pulse will not appear due to the head current being turned off and will erase any data from a previous write.

DDO of each word contains the sign and the parity check of the word. A data bit is written in the one bit cell of DDO if the sign is minus. A data bit is written in the two bit cell of DDO if the sign is plus. The four bit and eight bit cell of DDO contains the parity check for the word. Two parity FF's are used as a four counter. Both P1FF and P2FF are reset at the start. The first data pulse sets P1FF. The second data pulse reset P1FF and sets P2FF.

The third data pulse sets P1FF again. The fourth data pulse resets both FF's and the cycle starts over again. These FF's are counted for each bit of data written until DDO is reached. When DDO is to be encoded, the status of P1FF and P2FF is transferred (in complementary form-from the O side of the FF) to the Shift register FF's. The zero side of the P1FF is transferred to SR2FF and the zero side of the P2FF is transferred to SR1FF. Since the data bits are always written from the SRX8 or SRY8FF's, the complement of P1FF will be written in the third cell (4 bit position) of DDO and the complement of P2FF will be written in the fourth cell (8 bit position). On the READ operation, these bit positions will be read and the P1FF and P2FF's set accordingly, then the data bits are read and will count the PFF's. When the MSD digit has been read, both PFF's are not high, the ERFF will be set and will stop the read.

Figure V-10 is a chart of the setting and resetting of the P1 and P2FF's during the RL and WL operations. The functions of the FF's are shown for no data pulses, 1, 2, 3 and 4 data pulses. A block is also included which indicates a missed pulse to shown how an error condition will be produced. The parity FF's are not counted in DDO. Thus the parity count is of DD1 thru DDMSO.

WRITE LEDGER LOGIC

Figure V-12 is the flow chart for the write ledger operation. SA is similar to SO of E2100 T time. SB and SC provide a means of reading data, transferring data to the Shift Registors FF's (SRFF's) and writing the data back to memory.

When data digits are transferred from the WR to the SR, WR1 is transferred to SR8, WR2 is transferred to SR4, WR4 is transferred to SR2 and WR8 is transferred to SR1. Since writing is always done from SR8 the order of writing on the form will be 1 bit, 2 bit, 4 bit and 8 bit. The first bit to be written on the form will be from the high order word, high order digit and low order bit.

PARITY

	WRITE	
CLEARED FOR WRITE	RESET P1FF	RESET P2FF
NO DATA PULSES	$\overline{\text{P1FF}}$	$\overline{\text{P2FF}}$
PARITY COMPLEMENT TO SR	SR2 = 1	SR1 = 2

	READ	
ON READ	SR4 = 1	SR8 = 1
TRANSFER TO PARITY FF	SET P1FF	SET P2FF
NO DATA PULSES	P1FF	P2FF
CORRECT PARITY CHECK	P1FF	P2FF

	WRITE	
CLEARED FOR WRITE	RESET P1FF	RESET P2FF
ONE DATA PULSE WRITTEN	SET P1FF	----------
PARITY FF COMPLEMENT TO SR	SR2 = 0	SR1 = 1

	READ	
ON READ	SR4 = 0	SR8 = 1
TRANSFER SR TO PARITY FF	$\overline{\text{P1FF}}$	P2FF
ONE DATA PULSE READ	SET P1FF	P2FF
CORRECT PARITY CHECK	P1FF	P2FF

	WRITE	
CLEARED FOR WRITE	RESET P1FF	RESET P2FF
FIRST DATA PULSE WRITTEN	SET P1FF	--------
SECOND DATA PULSE WRITTEN	RESET P1FF	SET P2FF
PARITY FF COMPLEMENT TO SR	SR2 = 1	SR1 = 0

	READ	
ON READ	SR4 = 1	SR8 = 0
TRANSFER SR TO PARITY FF	P1FF	$\overline{\text{P2FF}}$
FIRST DATA PULSE READ	RESET P1FF	RESET P2FF
SECOND DATA PULSE READ	SET P1FF	P2FF
CORRECT PARITY CHECK	P1FF	P2FF

Figure V-10A

WRITE

CLEARED FOR WRITE	RESET P1FF	RESET P2FF
FIRST DATA PULSE WRITTEN	SET P1FF	--------
SECOND DATA PULSE WRITTEN	RESET P1FF	SET P2FF
THIRD DATA PULSE WRITTEN	SET P1FF	P2FF
PARITY FF COMPLEMENT TO SR	SR2 = 0	SR1 = 0

READ

ON READ	SR4 = 0	SR8 = 0
TRANSFER SR TO PARITY FF	$\overline{\text{P1FF}}$	$\overline{\text{P2FF}}$
FIRST DATA PULSE READ	SET P1FF	--------
SECOND DATA PULSE READ	RESET P1FF	SET P2FF
THIRD DATA PULSE READ	SET P1FF	P2FF
CORRECT PARITY CHECK	P1FF	P2FF

WRITE

CLEARED FOR WRITE	RESET P1FF	RESET P2FF
FIRST DATA PULSE WRITTEN	SET P1FF	-------
SECOND DATA PULSE WRITTEN	RESET P1FF	SET P2FF
THIRD DATA PULSE WRITTEN	SET P1FF	P2FF
FOURTH DATA PULSE WRITTEN	RESET P1FF	RESET P2FF
PARITY FF COMPLEMENT TO SR	SR2 = 1	SR1 = 1

READ

ON READ	SR4 = 1	SR8 = 1
TRANSFER SR TO PARITY FF	P1FF	P2FF
FIRST DATA PULSE READ	RESET P1FF	RESET P2FF
SECOND DATA PULSE READ	SET P1FF	---------
THIRD DATA PULSE READ	RESET P1FF	SET P2FF
FOURTH DATA PULSE READ	SET P1FF	P2FF
CORRECT PARITY CHECK	P1FF	P2FF

Figure V-10B

	WRITE	
CLEARED FOR WRITE	RESET P1FF	RESET P2FF
FIRST DATA PULSE WRITTEN	SET P1FF	------
SECOND DATA PULSE WRITTEN	RESET P1FF	SET P2FF
THIRD DATA PULSE WRITTEN	SET P1FF	P2FF
FOURTH DATA PULSE WRITTEN	RESET P1FF	RESET P2FF
PARITY FF COMPLEMENT TO SR	SR4 = 1	SR8 = 1

	READ	
ON READ	SR4 = 1	SR8 = 1
TRANSFER SR TO PARITY FFs	P1FF	P2FF
FIRST DATA PULSE READ	RESET P1FF	RESET P2FF
SECOND DATA PULSE READ	SET P1FF	-------
FAILED TO READ THIRD DATA PULSE	P1FF	$\overline{\text{P2FF}}$
FOURTH DATA PULSE	RESET P1FF	SET P2FF
PARITY ERROR	$\overline{\text{P1FF}}$	P2FF

Figure V-10C

The logic blocks above SA on the chart are controlled by the USMVFF pulses and cause writing of the data and complement pulses on the stripe. When the last bit (the 8 bit) of each digit has been written on the stripes SB and SC read the following digit and transfer it to the Shift Registors. S10 provides a means of counting down memory locations.

Initial conditions

<u>PMA</u> The Pinned Memory Address indicates that a memory address (units) must be pinned in the Write Ledger Position. The units only need be pinned since writing always occurs from the 20 to 29 group. The highest units of memory to be written must be pinned.

<u>LWLFF</u> The Lane Write Ledger FF is set by a pin in the Write Ledger lane (48b) CC5 and a clock pulse. This indicates that the carriage is in a Write Ledger position. The LWLFF must be set since the carriage will move out of the write ledger position before the writing on the stripe takes place.

<u>DDO</u> The Digit Distributor must start from the DDO position and is made high by R1 Reset.

<u>NOT CiFF</u> The CiFF must be reset at the start of the operation.

<u>PWFF</u> The Permit Write FF must be set to permit encoding data in the stripe.

<u>NOT P1XFF, NOT P2XFF</u> The parity XFF's must be reset at the start of the operation. This ensures a correct parity count.

<u>NOT CPFF</u> The complement pulse FF must be reset at the start of the operation.

SRCX-O The Shift Register Counter must equal zero at the start of writing. This ensures writing all bits of the first digit.

FF4 FF4 must be reset since it is used in one of the write monitor circuits (see error conditions).

NOT FF1X, NOT FF1Y, NOT FF3X FFs 1X, 1Y and 3X must be reset at the start of the operation. These FF's insure that all of the data is written and causes a start signal (1 data and 1 comp pulse) to be written after DDO of memory location 20.

NOT P1YFF and NOT P2YFF (DS) The P1Y and P2YFFs are the parity counters for the second stripe of dual stripe operations. Certain blocks of the flow chart are designated by (DS). This indicates blocks that are involved only on dual stripe operations. On single stripe operations, these blocks should be ignored. In machines equipped for single stripe operation, the logic cards for DS are not installed and the signal lines for this logic except part of FFZ which is at -4V, are left floating.

FF3Y FF3Y is used in a write monitor circuit and must be reset (see error conditions).

FF9Y FF9Y must be reset at the start of the write ledger operation.

FF9X FF9X is set when the sync pulse is written.

Assume that the control console has cycled in the write ledger position, the carriage has moved to the next carriage position and the carriage is open. The paper handler will drive the form into the carriage and the line find information will be written. The sync pulse is read and will cause the form travel to be reversed, the sync pulse rewritten (FF9X is set) and when the form reaches the line minus 2 location, the CLFF•L-2FF•NOT REVFF•LWLFF signal will be high. This signal initiates the encoding of data on the stripes in the following manner.

SET WLFF — The write ledger FF is set to initiate and control the actual writing of the data on the stripes. The WLFF is set by the CLFF•L-2FF•NOT REVFF•LWLFF•CLK signal.

SET DDREV — The DDREV FF is set so that the High order digits can be written first. The DDREV FF is set by WLFF•CLK.

RESET FFZ (DS) — FFZ is used on the dual stripe to designate which word group and stripe is being processed. If FFZ is reset the 20-29 word group and the middle stripe are active. If FFZ is reset the 30-39 word group and the left stripe are being processed.

SA — The Sequence A FF is set by CLFF•L-2FF•NOT REVFF•LWLFF•CLK. Sequence A preconditions the Electronic Processor for the write operation.

SA of DDO SET CAD — The SA1, SA2 and SA3FFs are all reset at the end of sequence A to select CAD so that the MARUFFs, which were set to the units of memory address in the WL carriage position, will select the first word to be written.

2 → MART — The MART2FF is set, by sequence A, to select the 20-29 word group. MART1FF is reset by the same signal to ensure writing does not start from the 30-39 word group.

RESET MART4FF — MART4FF is reset to ensure that writing doessnottbegin in the 60-69 word group.

STEP DD — The DD is stepped to DD1. During the write ledger operation DDREV is set; therefore, DDMSD of the selected C address will be the first digit written.

0 → WR — The WR must be clear at the start of the operation.

MR→MEM The MR→MEMFF is set so that the data read from memory, to be written in the stripe, can be written back to memory.

RESET COMPFF The COMPFF is reset since all data is to be handled in true form.

SB of DD1 (20) READ DDMSD of the C address is read into the MR. (DD1 & DDREV are set).

MR→WR The WR is made equal to the MR.

COMPLEMENT FFZ (DS) In the dual stripe machine, FFZ will be complemented to prepare for reading from the 30-39 word group and writing in the left stripe.

SC of DD1 (20) WRITE Data is written from the MR back into the DDMSD of the C address.

COMPLEMENT MART1 (DS) The MART1FF is set in Dual Stripe machines to select word group 30-39.

WR→SRX Data in the WR (DDMSD of the C address) is transferred to the Shift Register XFFs. FFZ•NOT DDO cause the transfer. Data will be written from the SRX8 to the stripe.

STEP DD On a single stripe machine, the DD is stepped by NOT DDO.

SEQB In a Single Stripe machine FFZ will be low and no sequence will be set. The logic waits for a USMVFF signal. In a Dual Stripe machine, FFZ will be high and will return the logic to SB.

SB of DD1 (30) READ DDMSD of the 30-39 word group is read into the MR.

MR→WR The WR is made equal to the WR.

COMPLEMENT FFZ The FFZ is reset.

SC of DD1 (30) WRITE Data from the MR is written back into DDMSD of the 30-39 word group.

WR →SRY Data is transferred from the WR to the SRY. Data from the SRY will be written into the left stripe.

STEP DD NOT FFZ NOT DDO cause the DD to step to DD2.

No sequence is set and the logic waits for a USMVFF pulse. Data from the high order digit of the high order word is now in the SRX and SRY (DS). This data will be written into the stripes under the control of the USMVFF pulses.

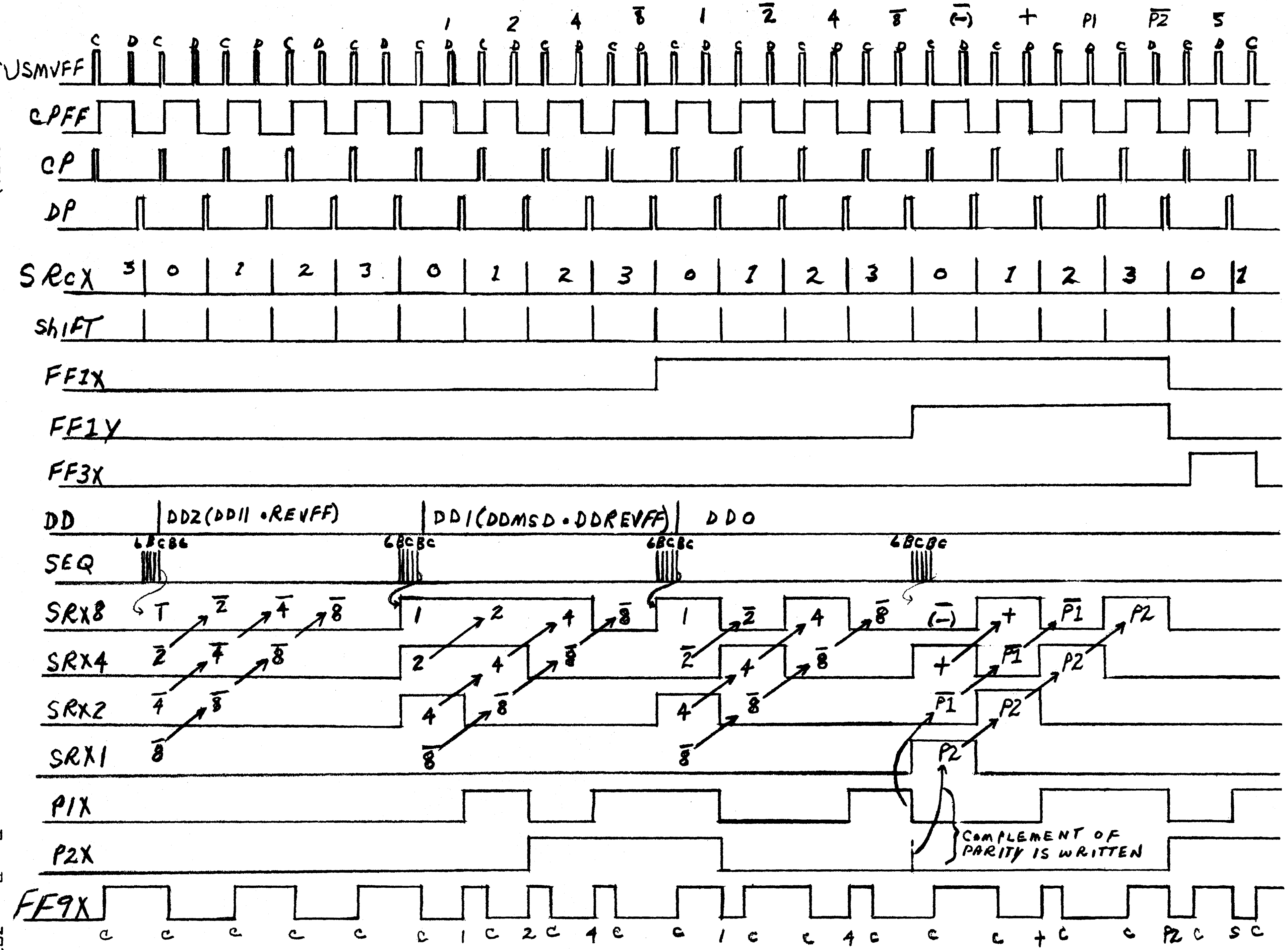
Figure V-11 shows the time relationship of some of the signals while writing the last two digits and sign of memory locations 20 and 30 (DS). The signals shown are for the writing of .75+. This signal chart may be used as an example while studying the logic flow chart.

COMPLEMENT CPFF Each USMVFF pulse is gated with WLFF to complement the COMPLEMENT PULSE FF. This occurs every 370 usec. The USMVFF pulse stays high for one clock duration (12 usec).

COMPLEMENT PULSE The NOT CPFF signal is high at the start of the operation. (Initial condition). The NOT CPFF is gated with USMVFF•WLFF. The output of this gate is the CP pulse and is high for one clock duration.

GATE 9XFF and 9YFF The trailing edge of the CP pulse complements the 9X and 9Y FFs. Complementing the 9X and 9Y FFS causes a reversal of head currents and writes a complement pulse in each stripe 12 usec after the start of the USMVFF pulse. 370 usec later, the second USMVFF pulse occurs.

COMPLEMENT CPFF The CPFF is complemented by the trailing edge of every USMVFF pulse during the WL operation.



WRITING 0.75+ IN MEMORY LOCATION 20   FIGURE V-11

<u>DATA WRITE</u> The CPFF and WLFF•USMVFF are gated together to produce the DATA WRITE signal. This signal triggers a 70 usec DMV. The output of the DMV is gated with WLFF and the resulting signal triggers a PS.

<u>FF6</u> The PS pulse• NOT FF6•CK sets FF6. The FF6•CK signal resets FF6 after one clock duration. The FF6 signal is a 12 usec pulse which is synchronized with clock.

<u>DATA PULSE</u> The DATA pulse is an inverted NOT FF6 signal.

<u>COUNT SRCX</u> The Shift Register counter X (and Y) consists of 2FFs each. These FFs are used to count 4 as follows: SRCX1 set - 1, SRCX2 set -2, SRCX1 and SRCX2 set - 3, SRCX1 and SRCX2 reset - 0 thus the count is 1, 2, 3 and 0 for a four count. Each DATA PULSE (DP) counts the SHIFT REGISTER COUNTER.

<u>COMPLEMENT FF9X and FF9Y (DS)</u> The DP is gated with SRX8. If this produces a high signal (if SRX8 contains data read from memory) the FF9X will be complemented. A complementation will produce a reversal of head current and thus write a data pulse (1 bit) on the stripe. The data pulse is, written 440 usec after the first complement pulse (370 + 70). The same conditions exist for FF9Y.

<u>COMPLEMENT PXFF and PYFF (DS)</u> The P1X and P2X FFS count data pulses written in a similar manner to the SRCXFFs. If SRX8 was high to cause a reversal of head current the SRX8•DP•NOT DD1•NOT P1XFF•CLK will complement or count the Parity FFs. The same conditions exist for the PYFF's.

<u>SHIFT SRX and SRY (DS)</u> Each DP causes data in the SRXFFs to shift one bit position. Writing on the stripe is always done from SR8X. After the first bit is written, the data that was in SR1, SR2 and SR4 is shifted into SR2, SR4 and SR8. The four bit data can then be written from SR8 on the next DP.

SHIFT SRX and SRY (DS) (continued) These are the shifts that are counted by the SRCXFFs. The SRYFF are shifted in a similar manner.

COMPLEMENT CPFF The CPFF is complemented by the following USMVFF pulse.

COMPLEMENT PULSE A 12 usec CP is produced by NOT CPFF•WLFF•USMVFF.

GATED FF9X and FF9Y (DS) The trailing edge of the CP complements the FF9X and FF9Y to cause a complement pulse to be written in the stripe. This pulse is written 300 usec (370-70) after the data pulse if data was written.

COMPLEMENT CPFF The following USMVFF pulse again complements the CPFF.

DATA WRITE The DATA WRITE signal is made high by WLFF•USMVFF•CPFF and triggers the 70 usec DMV. The DMV and WLFF triggers a PS. FF6 is set by the PS and CK to synchronize the operation with the clock.

DATA PULSE A DP is produced by FF6.

COMPLEMENT FF9X and PXFF The FF9X and PXFFs are complemented if SR8X is high (a two bit is to be written on the stripe).

COMPLEMENT FF9Y (DS) and PYFF (DS) The FF9Y and PYFFs are complemented if SRY8 is high.

COUNT SRCX The Shift Register Counter are counted by the DP. The SRCX now equals 2.

SHIFT SRX and SRY (DS) Data in the Shift Register is shifted one place.

COMPLEMENT CPFF The CPFF is complemented by a USMVFF pulse.

COMPLEMENT PULSE A CP pulse is produced by the NOT CPFF•WLFF•USMVFF.

GATED FF9X and FF9Y (DS) The CP complements the FF9X and FF9Y to write a pulse in the stripes.

<u>COMPLEMENT CPFF</u> The USMVFF complements the CPFF.

<u>DATA WRITE</u> A Data write signal is produced by WLFF•USMVFF•CPFF. The Data write and WLFF signals triggers the 70 usec DMV which in turn triggers a PS.

<u>SET FF6</u> FF6 is set by PS and CK to synchronize with clock.

<u>DATA PULSE</u> A DP is produced by FF6.

<u>COMPLEMENT FF9X and PXFF</u> If SR8X is high (a four bit is to be written) the 9X and PXFFs are complemented. This will write the data and count parity.

<u>COMPLEMENT FF9Y (DS) and PYFF (DS)</u> If SR8Y is high, the 9Y and PYFFs are complemented. This will write data on the stripe and count parity.

<u>SHIFT SRX and SRY (DS)</u> The 8 bit data is shifted into the SRX8 and SRY8FFS.

<u>COUNT SRCX</u> The DP counts the SRCXFF to 3.

<u>COMPLEMENT CPFF</u> The USMVFF complements the CPFF.

<u>COMPLEMENT PULSE</u> NOT CPFF•USMVFF•WLFF produce a CP.

<u>GATE FF9X and FF9Y (DS)</u> FFs 9X and 9Y are complemented to write a complement pulse on the stripes.

<u>COMPLEMENT CPFF</u> The USMVFF complements the CPFF.

<u>DATA WRITE</u> CPFF•USMVFF•WLFF produce the Data write signal which triggers the 70 usec DMV. The DMV and WLFF triggers a PS.

<u>SET FF6</u> FF6 produces the DP.

<u>COMPLEMENT FF9X and PXFF</u> If SRX8 is high (a 8 bit is to be written) the FF9X and PXFF are complemented.

<u>COMPLEMENT FF9Y (DS) and P9YFF (DS)</u> If SRY8 is high, the FF9Y and P9Y FF are complemented.

<u>SHIFT SRX and SRY (DS)</u> The DP causes the SRX and SRYFF to shift.

<u>COUNT SRCX</u> The DP causes the SRCX to advance. The SRCX is now equal to zero.

SEQB NOT FF1Y•SRCX-3•DP•CK sets SEQB. SRCX is still equal to three when the DP becomes high. With the setting of SEQB, the procedure up to this point is started over again. This procedure is repeated for each digit as the data is read from memory and written into the stripes. When DDO is high and SEQB has been set by NOT FF1Y•SRCX - 3•DP•CK the logic is as follows.

SB of DDO (20) READ The sign of the "C" address is read to the MR (MR1 indicates a minus sign).

MR → WR The WR is set equal to the MR.

COMPLEMENT FFZ (DS) FFZ is complemented.

SC of DDO (20) WRITE The sign if written back to memory.

COMPLEMENT MART1 (DS) MART1 is set to select the sign of the 30-39 word group.

NOTE: That the sign which is in the WR is not transferred to the SRX.

SEQB SB is set so that the sign of the selected word from the 30-39 group can be read.

8 → SRX8 If the sign in the MR is negative, MR1 will be high and the SRX8FF will be set. This will be written in the 1 bit position on the stripe.

4 → SRX4 If the sign in the MR is positive, the NOT MR1 will be high and the SRX4FF will be set. This will be written as a two bit in the stripe.

A bit is written for both a negative and a positive sign. Thus, the machine must account for the sign of a word and cannot have the sign change by loosing a bit.

GATE NOT P2XFF → SRX1 and GATE NOT P1XFF → SRX2 The complement of the parity count (from the zero side of the FF) is gated to the SRX, NOT P1XFF will be written as a 4 bit on the stripe and NOT P2XFF will be written as an 8 on the stripe.

SB of DDO (DS-30) READ — The sign of the selected 30-39 word is read into the MR.

MR ⟶ WR — The WR is set equal to the MR.

COMPLEMENT FFZ — FFZ is complemented.

SC of DDO (DS-30) WRITE — The sign is written back to memory.

COMPLEMENT MART1 — MART1FF is reset to count back to the 20-29 word group. Note the WR is not transferred to the SRY.

STEP DD — The DD is stepped by NOT•FFZ MARU $\neq$ 0.

8 → SRY8 (DS) — If the sign in the MR is negative, MR1 will be high and the SRY8FF will be set. This will be written as a 1 bit on the left stripe.

4 → SRY4 (DS) — If the sign in the MR is positive, the NOT MR1 will be high and SRY4FF will be set. This will be written as a 2 bit on the left stripe.

GATE NOT P2YFF → SRY1 and GATE NOT P1XFF → SRY2 — The complement of parity Y is transferred to the SRY. The zero side of PARITY 1 will be written as a 4 bit on the left stripe and the zero side of PARITY 2 will be written as an 8 bit on the left stripe. After the complement of the parity count is transferred to the SRX and SRY (DS) the parity FF are reset for the start of the parity count of the next word.

SEQ10, SET CiFF and 8 → WR — Each of these conditions is set by MARU $\neq$ 0•NOT FFZ DDQ·SEQ 10 is set so that the memory address units can be counted down. The CiFF and 8 in the WR provide a 9 input to the adder to enable a count down.

S10 0 → MR — The MR is cleared so that there is no unwanted input to the adder. The MR is cleared during the sequence.

GATE MARU ⟶ ADDER — The MARU FFs are an input to the adder.

GATE ADDER ⟶ MARU — The adder output, which the MARU FF plus 8 from the WR and 1 from CiFF, is gated to set the MARUFFS, by CiFF.

SEQ 10 — S10 is set again by CiFF. The fact that S10 stays on two clock pulses has no significience here but will be used in future machines.

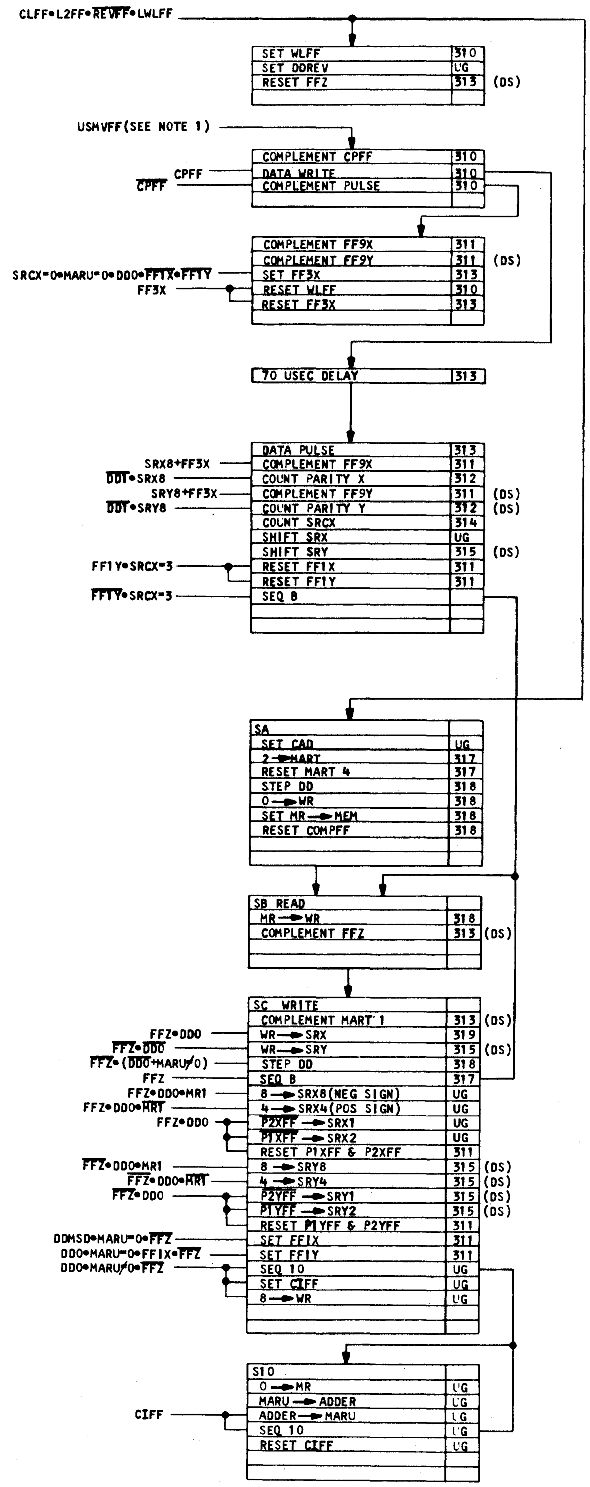
RESET CiFF — CiFF reset after S10. No logic sequence is set after S10 and the machine waits for a USMVFF pulse to write the data for DDO. This is written in the same way that data of the other digits is written on the stripes. When DDO is finished, DDMSD of the next word is read from memory and written on the stripes. This process continues until all digits of all words are written through DDO of memory location 20 and 30 (DS).

After the data for DDO is written on the stripe, a start read signal must be written on the stripes. This consists of one Data and one complement pulse after the DDO data is written. The writing of these pulses is controlled by the 1X, 1Y and 3X FFs.

Since the DD is not stepped out of DDO at the end of the write operation, DDO will be high during the writing of data for DD1 and DDO of word 20. FF1X and FF1Y are used as counters to count the digits written while DDO is high. FF1X is set by DDMSD•MARU = O•NOT FFZ•SC•WLFF•CK. This occurs when SRCX = O of DD1 (DDMSD and DDREV) is high. NOT FF1X is then low and prevents setting FF3X when the SRCX = O and a CP occurs, which will occur while writing DDMSD (DD1). FF1Y is set by DDO•MARU = O•FF1X•NOT FFZ•SC•WLFF•CK. This occurs when SRCX = O of DDO is high. NOT FF1X and NOT FF1Y both prevent setting FF3X when the SRCX = O and a CP which occurs while writing DDO. NOT FF1Y being low prevents SB being set to read DDO from memory again and transferring it to the SRX and SRY (DS).

FF1Y•SRCX = 3•WLFF resets FF1X and FF1Y. This allows the CLK to set FF3X when CP•SRCX = O•MARU = O•DDO•NOT FF1X•NOT FF1Y is high. FF3X will allow the next DP to write a pulse on the form. The next CP pulse will be written on the form and with FF3X. CK will reset FF3X and WLFF. The resetting of the WLFF prevents further CP or DP pulses which prevents complementing FF9X or FF9Y. PWFF remains set and the write amplifiers remain on to orient the reset of the data stripes as the form is fed out of the machines. This erases any previous data or noise from the stripes and prevents a possible unwanted pulse due to interrupting head current.

INITIAL CONDITIONS	
PMA	UG
LWLFF	306
DDO	318
$\overline{CIFF}$	UG
FF9X	311
PWFF	310
$\overline{P1XFF}$	312
$\overline{P2XFF}$	312
$\overline{CPFF}$	310
SRCX=0	314
$\overline{FF4}$	306
$\overline{FF1X}$	311
$\overline{FF1Y}$	311
$\overline{FF3X}$	313
$\overline{P1YFF}$	312
$\overline{P2YFF}$	312
$\overline{FF3Y}$	313
$\overline{FF9Y}$	311



NOTE:
1. WHENEVER NOT IN ANY SEQ, USMVFF CONTROLS THE LOGIC
2. "UG" REFERS TO UPPER GATE SCHEMATIC

Figure V-12

READ LEDGER OPERATION

The Read Ledger (RL) operation is initiated when the operator inserts a card into the throat of the carriage. The carriage must be located in a stop position programmed with lane 56 (SL) and lane 66 (RL). If the card is to be aligned at the printing line, the align, lane 60, (A) must also be pinned. If lane 60 (A) is not pinned, the card will be fed completely out of the carriage.

Paper travel, see Fig. V-13, during the RL operation is from the pusher fingers rearward as the pusher fingers align the form. At this position, the read heads and pressure rolls are lowered to the form and the form is driven into the machine. Data is read as the form moves under the head. At approximately L-2, the reading of data is finished and the sync pulse just after line minus six causes the form travel to be reversed. When the form is driven out to L-4, the search is started for the line find pulse. If the align lane is pinned, the line find pulse will cause the form to be stopped at the printing time. If the align lane is not pinned, the line find pulse will be ignored and the form will be fed out of the carriage.

Read Paper Handling Logic

The logic which controls the feeding and alignment of the form on the RL operation during a posting cycle is shown in Fig. V-14, and is as follows.

<u>RESET TABFF</u> The TAB FF is reset by NOT TAB•CK. NOT TAB comes from normally closed TAB Relay contacts and thus does not become high until the carriage bounce has stopped.

<u>RESET L-2FF</u> The L-2FF must be reset at the start of the operation and is reset by CC1•CC3•CK when the carriage camshaft is in the home position.

<u>RL Sig.</u> The Read Ledger signal is made high when the Read Ledger lane is pinned.

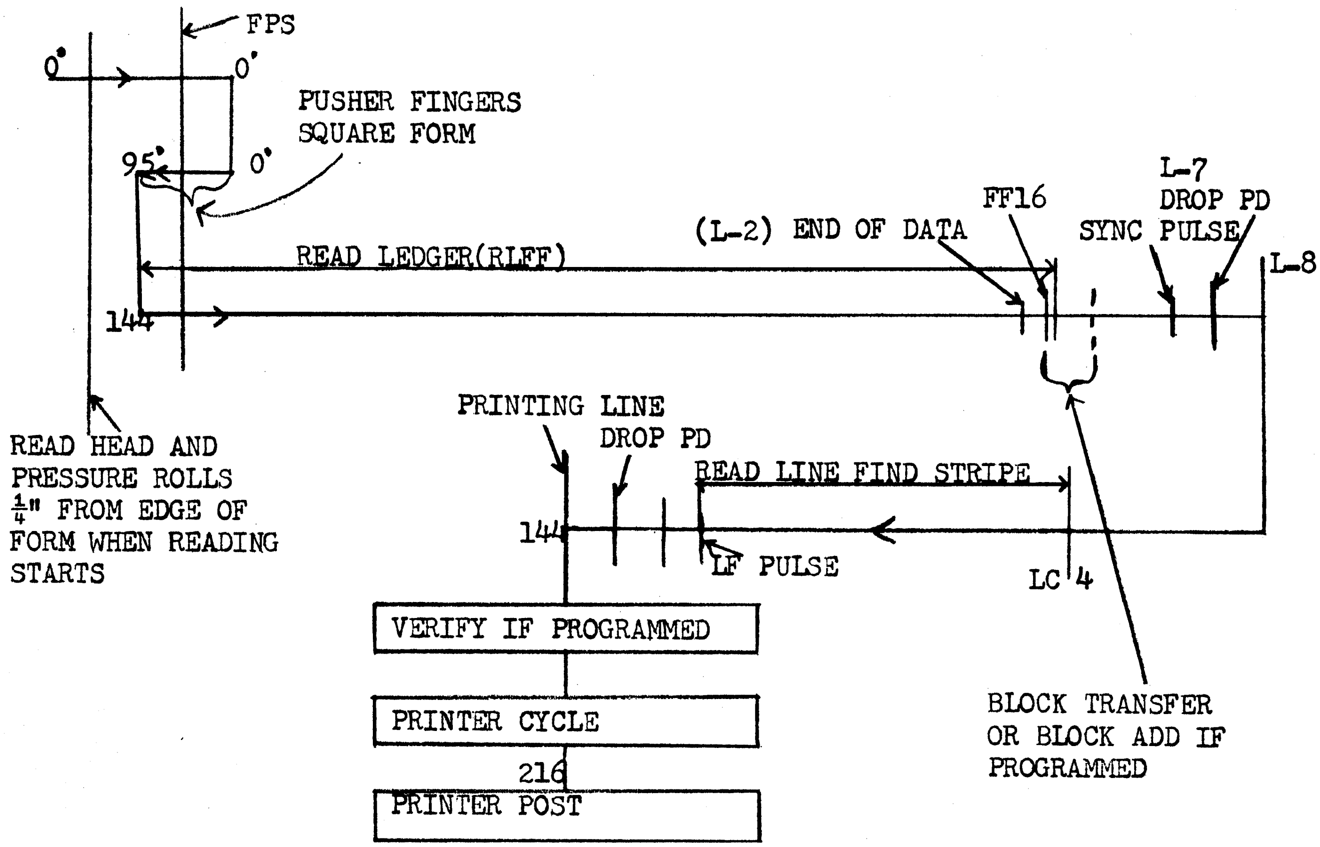

FPS
0°
0°
PUSHER FINGERS
SQUARE FORM
95°
0°
L-7
FF16
DROP PD
(L-2) END OF DATA
SYNC PULSE
READ LEDGER(RLFF)
L-8
144
PRINTING LINE
DROP PD
READ HEAD AND
PRESSURE ROLLS
¼" FROM EDGE OF
FORM WHEN READING
STARTS
READ LINE FIND STRIPE
144
LF PULSE
LC 4
VERIFY IF PROGRAMMED
PRINTER CYCLE
216
PRINTER POST
BLOCK TRANSFER
OR BLOCK ADD IF
PROGRAMMED

Figure V- 13

<u>SL Sig.</u> The striped Ledger signal is made high when any striped ledger operation is to be performed.

<u>ALIGN (A)</u> The ALIGN signal is made high if the align lane is pinned.

<u>SL LU</u> Striped Ledger Lock up causes the lock Relay to be picked and prevents a console cycle until the RL operation is finished and POFF is set.

<u>FPS</u> The FPS is made high when the form interrupts the light beam to the FPS solar cell.

<u>CRG OP LOCK SOL</u> The Carriage Open Lock Solenoid is energized by FPS•NOT ECNC through a solenoid driver. When the SOL is energized, the carriage open/close key cannot be indexed. This prevents the operator manually removing the form. However, the form must be removed if the machine has an ECNC lock.

<u>SET CRG MTRFF</u> The Carriage Motor FF is set by FPS•CC3•NOT ERFF•NOT LOCK•SL•CLK. This signal indicates that a form has been inserted, the camshaft is at home, the machine is not under an error or lock condition from some previous operation, and that a striped ledger operation is pinned.

<u>CRG MTR RELAY</u> (K1109) is energized by the CRG MTRFF signal and a Solenoid Driver. The relay contacts complete the circuit to the carriage motor.

<u>SET PROG CAM FF</u> The program Cam FF is set by CC3•FPS•NOT ERFF•NOT LOCK•SL•CC1•(NOT ARON + NOT FL)•CLK. This signal indicates that the program camshaft is at home, a form has been inserted, the machine is not under error or lock condition, a striped ledger operation is pinned, and that an Auto Reader operation is not indicated.

<u>PROGRAM CAM SOLENOID</u> The PROG CAM FF signal energizes the PROGRAM SOL through a solenoid Driver. The program cam solenoid couples the carriage motor to the Program Camshaft.

TRIGGER 100ms DMV	The 100ms DMV is triggered by CC2 at 95°, so that Paper Drive can be started. The 100ms DMV provides time for the shuttle gear to be positioned.
SET REV FF	When the program camshaft has turned to 95°, CC2 becomes high and the CC2•CC3•NOT EJFF•CK signal sets the Reverse FF.
REVERSE SOL	The REVFF signal energizes the Reverse Solenoid through a Solenoid Driver. The Reverse Solenoid positions the shuttle gear so that the form will be driven into the carriage.
RESET PROGRAM CAM FF	The Program Cam FF must be reset between 72° and 144° so that the camshaft can be stopped at 144°. CC2•NOT EJFF•CK resets the Prog Cam FF at 95°.
SET PDFF SIG.	The Paper Drive FF is made high when the 100ms DMV times out.
SET PDFF	The output of the 100ms DMV and CK sets the PDFF.
ENERGIZES PD SOL	The paper drive solenoid is energized by the PDFF•NOT TABFF• CRG OPEN through a PDC Circuit. The NOT TABFF•CRG OPEN signals are primarily for the WRITE operation, however, they are used on the read operation also. The PDC circuit energizes the solenoid from 120V and reduces the voltage to approximately 25V hold voltage after a predetermined length of time.
GATE BOLP	The PD signal gates the BOL signals from the BOLP circuit into the machine. The BOL pulses are generated from a solar cell and disc on the pressure roll drive shaft.
SET RLFF SIG	The SET READ LEDGER FF SIG is made high to allow the RLFF to be set, gate a R1 RESET pulse and set SA. FPS through a PS• PDFF•NOT LWLFF•REVFF makes the signal high. The PS triggered from the FPS is necessary to prevent continuously setting SA.
SET RLFF	The Read Ledger FF is set by the SET RLFF signal. RL•CLK. The RLFF maintains the read operation after the FPS - PS signal.

R1 RESET Various striped ledger FFs that are to be used during the Reading of Data must be reset before the reading begins. The R1 reset is triggered by the SET RLFF•NOT BCFF.

SET SA Sequence A prepares several FF in the E2100 portion of the machine to read data from the stripes. Sequence A is set by SET RLFF•RL•NOT SA•CK.

GATE READ AMPX The Read Amp X pulses are gated into the machine by REVFF•NOT FF4•NOT SSFF•NOT PWFF•PD.

GATE READ AMPY The Read Amp Y pulses are gated into the machine by RLFF•NOT BCFF.

SET FF3X FF3X is set by the start read signal which consists of a complement and a data pulse. FF3X allows the succeeding data to be stored in memory.

6MS RESETTABLE DMV The 6ms Resettable DMV is reset by each pulse read from the X stripe.

READ LOGIC The Read Logic is a separate subject and is discussed following this subject.

SET FF16 When the 6ms resettable DMV times out the 6ms DMV•FF3X•CK signal sets FF16. This indicates that all data pulses have been read and that the next pulse will be the sync pulse.

RESET RLFF The RLFF is reset by FF16•RLFF•DDO•CLK. This prevents the next pulse read being handled as a data pulse.

SET SSFF FF16 and the next Read amp X pulse sets the Stop Storage FF. Stop Storage FF is an indication that the form travel must be reversed.

RESET PDFF SIG. The RESET PDFF sig is made high by SSFF and the next BOLP pulse.

RESET COUNTERS The REVFF•RESET PDFF Sig. resets the counters for a count of lines as the form is driven out. A search for the line find pulse starts at a count of 4 or at L-4.

RESET PDFF — The PDFF is reset by the RESET PDFF Sig.•NOT EJFF•CLK so that the form travel will stop.

ENERGIZE STOP PD SOL — NOT PDFF and a PDC energizes the STOP PD SOL at L-7. Paper travel stops at L-8.

RESET REVFF — NOT PDFF•WS resets the REVFF 9ms after the L-7 BOLP.

ENERGIZE RET SOL — NOT REVFF energizes the RET Sol through a SD.

TRIGGER 100MS DMV — RET•NOT PDFF•NOT L-2FF•NOT ERFF triggers the 100ms DMV which provides time for the shuttle gear to be positioned before paper drive is started again.

SET PDFF SIG. — The SET PDFF Sig is made high when the 100ms DMV times out.

SET CLFF — The CLFF will allow the counter to be used to find the line minus four position where a search is started for the line find pulse. CLFF is set by RET•NOT L-2FF•SET PDFF•CK.

SET PDFF — The PDFF is set by the SET PDFF Sig.•CLK.

ENERGIZE PD SOL — The PDFF•NOT TABFF•CRG OPEN, triggers a PDC circuit to energize the PD SOL. The Sol is picked by 120V and then the voltage is reduced to hold voltage.

SET FF — NOT WLFF•BOLP sets FF. FF gates the USMVFF to the SYNC FF.

SET SYNC FF — FF•USMVFF•NOT SYNC sets SYNC FF. The SYNC FF pulse is a 370 usec pulse which starts at the next USMVFF pulse after a BOLP.

SYNC MV — The SYNC MV is made high by USMVFF•SYNC FF. SYNC MV pulse is a 12 usec pulse.

RESET FF & RESET SYNCFF — The FF and SYNC FFs are reset by the SYNC MV.

ADVANCE COUNTER — The SYNC MV•CLFF advances the counter.

SET L-2FF — The Line minus 2FF is set by a count of 6•RET•CK. The L-2FF is set so that the CLFF can be reset.

RESET CLFF — The CLFF is reset to block the SYNC MV pulses from the counter and allow the count 4FF of the counter to remain set until the LF pulse is read. (6•NOT WLFF)• L-2FF•CK resets the CLFF.

SET LFAFF — The Line Find AFF is set by a pulse from the Line Find Read amplifier the count 4FF•CC4•RET. The count of 4 prevents noise on the upper end of the stripe from being recognized as the line find pulse. LFAFF gates the following BOLP pulse to the LFBFF and thus synchronizes the line find pulse with a tooth on the clutch.

SET LFBFF — Line Find BFF is set by LFAFF•BOLP•CK.

LF SIG — The Line Find signal is made high by BOLP•LFBFF•ALIGN•CC4•CLK• L-2FF and is an indication that the form feed should be stopped.

SET SS FF & RESET LFAFF — A Stop Storage FF is set by the LF signal and clock. LFAFF is reset by the same signal. SSFF gates a BOLP pulse to RESET PDFF.

RESET PDFF Sig & RESET SSFF — SSFF BOLP make the RESET PDFF signal high and the next CLK Pulse resets the SSFF.

RESET PDFF — The RESET PDFF sig•NOT EJECT•CLK resets the PDFF to stop form travel.

ENERGIZE STOP PD SOL — The Stop paper drive solenoid is energized by NOT PDFF through the PDC circuit.

SET POFF — The Printer Operate FF is set by the LF sig•NOT REVFF•(through a PS) NOT ERFF•CLK. This indicates that the line has been found and that there was no error on the operation.

CHECK STOP SOL — This solenoid provides a limit in the carriage for a check or other short form. It is energized after the read is completed and before the drive is tripped by NOT PTFF•FPS•POFF through a SD.

MB2 SOL — The MB2 solenoid is energized by A•POFF•AUTO CYCLE•a PS which is triggered by POFF. The PS provides a 100ms pulse to energize the MB2 Sol if an automatic cycle is desired. The 100ms pulse prevents over heating of MB2 SOL. The Auto Cycle is a signal developed from the restored condition of a latch down key on the keyboard. It provides automatic operations after a feed ledger operation.

RESET POFF — Timing Cam 10 which is made from ~~220°~~ 170° to ~~260°~~ 210° and clock reset the printer operate FF, during the console cycle.

SET PROG CAM FF — The console cycle with the program camshaft at 144° causes the camshaft to advance to 216°. The setting signal is TC10•CC4•CC1•CLK.

PROG CAM SOL — The PROG CAM FF energizes the PROG CAM SOL through a SD.

RESET PROG CAM FF — The CC2•NOT EJFF•CLK signal resets the PROG CAM FF at 180° of the Program Camshaft.

RESET CRG MTR FF — The carriage Motor FF is reset at 180° of the camshaft by CC2• CC4•NOT EJFF•CLK. The drop time of K1109 and the coasting of the motor turns the camshaft to 216°.

RESET 3XFF — The 3XFF is reset by CC2•CLK.

R1 RESET & RESET COUNTER — CC2 resets the electronic control FFs and counter.

RESET 9XFF — If the 9XFF is set, it is reset by CC2•9XFF•CLK.

READ LEDGER LOGIC

In order to perform a read ledger operation certain predetermined conditions must be met. The carriage position must be programmed with Read Ledger and Striped Ledger pins and the following FFs must be reset. These FFs will be reset by the previous machine operation or the turn on sequence. ERFF, COMPFF, FF1X, FF1Y, FF3X, FF3Y, FF9X and FF9Y.

READ LEDGER PAPER HANDLING

R1 RESETS FFs

LFAFF	LFBFF
FF4	FF16
FF1X	FF1Y
FF3X	FF9X
FF	SYNCFF
CLFF	VFF
PARITYFFs	CPFF
DISCXFF	DISCYFF
DATAXFF	DATAYFF
SRCXFFs	SRCYFFs

Condition	Driver	Function	
$\overline{\text{TAB}}$•CLK		RESET TABFF	305
CC1•CC3•CLK		RESET L-2FF	306
LN 56•LN 66		RL Sig	304
RL		SL Sig	304
LN 56•LN 60		ALIGN (A)	304
SL•$\overline{\text{POFF}}$		SL LU	

Condition	Driver	Function	
FPS•SOLAR CELL		FPS	323
FPS•$\overline{\text{ECNC}}$	SD	CRG OPEN LOCK SOL	304
FPS•CC3•$\overline{\text{ERFF}}$•$\overline{\text{LOCK}}$•CLK•SL		SET CRG MTRFF	304
CRG MTRFF	SD	CRG MTR RELAY	304
CC3•FPS•$\overline{\text{ERFF}}$•$\overline{\text{LOCK}}$•SL•CC1•CLK•($\overline{\text{ARON+FL}}$)		SET PROG CAMFF	304
PROG CAMFF	SD	ENERGIZE PROG CAM SOL	322

Condition	Driver	Function	
CC2•CC3		TRIGGER 100ms DMV	305
CC2•CC3•$\overline{\text{EJFF}}$•CLK		SET REVFF	305
REVFF	SD	ENERGIZE REV SOL	305
CC2•$\overline{\text{EJFF}}$•CLK		RESET PROG CAMFF	304

Condition	Driver	Function	
100ms DMV TIMES OUT		SET PDFF Sig	305
SET PDFF Sig•CLK		SET PDFF	305
PDFF•$\overline{\text{TABFF}}$•CRG OPEN	PDC	ENERGIZE PD SOL	305
PD•BOL		BOLP	323
FPS → PS → PDFF•$\overline{\text{LWLFF}}$•REVFF		SET RLFF Sig	309
SET RLFF•RL•CLK		SET RLFF	309
SET RLFF•$\overline{\text{BCFF}}$		R1 RESET	307
SET RLFF•RL•$\overline{\text{SA}}$•CLK		SET SA	317
REVFF•$\overline{\text{FF4}}$•SSFF•$\overline{\text{PWFF}}$•PD		GATE READ AMP X	316
RLFF•$\overline{\text{BCFF}}$		GATE READ AMP Y	316

Condition	Function	
RLFF•START READ Sig	SET FF3X	313
RLFF•READ AMP X•FF3X	6ms RESETTABLE DMV	306
READ AMP PULSES	READ LOGIC	316

Condition	Function	
6ms DMV TIMES OUT•CLK•FF3X	FF16	306
FF16•RLFF•DDO•CLK	RESET RLFF	309

Figure V-14A

FF16•READ AMPX		SET SSFF	305

SSFF•BOLP		RESET PDFF Sig	305
REVFF•RESET PDFF Sig		RESET COUNTER	308
RESET PDFF Sig•$\overline{\text{EJFF}}$•CLK		RESET PDFF	305
$\overline{\text{PDFF}}$	PDC	ENERGIZE STOP PD SOL	305
$\overline{\text{PDFF}}$•WS		RESET REVFF	305
$\overline{\text{REVFF}}$	SD	ENERGIZE RET SOL	305
RET•$\overline{\text{PDFF}}$•$\overline{\text{L-2FF}}$•$\overline{\text{ERFF}}$		TRIGGER 100ms DMV	305

100ms DMV TIMES OUT		SET PDFF Sig	307
RET• SET PDFF•Sig•$\overline{\text{L-2FF}}$•CLK		CLFF	307
SET PDFF Sig.CLK		SET PDFF	305
PDFF•$\overline{\text{TABFF}}$•CRG OPEN	PDC	ENERGIZE PD SOL	308
$\overline{\text{WLFF}}$•BOLP		SET FF	308
FF•USMVFF•$\overline{\text{SYNCFF}}$		SET SYNCFF	308
USMVFF•SYNCFF		SYNC MV	308
SYNC MV		RESET FF	308
		RESET SYNCFF	308
SYNC MV•CLFF		ADVANCE COUNTERS	308

6•RET•CLK		SET L-2FF	306
6•L-2FF•CLK•$\overline{\text{WLFF}}$		RESET CLFF	307

LFRA•4•CC4•RET		SET LFAFF	307
LFAFF•BOLP•CLK		SET LFBFF	305
LFBFF•BOLP•A•CC4•L-2FF•CLK		LF Sig	305
LF Sig		RESET LFAFF	305
		SET SSFF	305

SSFF•BOLP		RESET PDFF Sig	305
SSFF•BOLP•CLK		RESET SSFF	305
RESET PDFF Sig•$\overline{\text{EJFF}}$•CLK		RESET PDFF	305
$\overline{\text{PDFF}}$	PDC	ENERGIZE STOP PD SOL	305

LF Sig•$\overline{\text{REVFF}}$ — PS — $\overline{\text{ERFF}}$•CLK		SET POFF	307
$\overline{\text{PTFF}}$•FPS•POFF	SD	CHECK STOP SOL	307

Figure V-14B

POFF A•POFF• $\boxed{\text{100ms DMV}}$ •AUTO CYCLE — SD	MB2 SOL	307
(TC10 M B)•CLK	RESET POFF	307
(TC10 M B)•CC1•CC4•CLK	SET PROG CAMFF	304
PROG CAMFF — SD	PROG CAM SOL	304
CC2•$\overline{\text{EJFF}}$•CLK	RESET PROG CAMFF	304
CC2•CC4•$\overline{\text{EJFF}}$•CLK	RESET CRG MTRFF	304
CC2•CLK	RESET FF3X	313
CC2	R1 RESET	307
CC2	RESET COUNTER	308
CC2•FF9X•CLK	RESET FF9X	311

Figure V-14C

The operator inserts the ledger card into the carriage for the read ledger operation. The form is pushed out slightly and squared in the carriage by the pusher fingers. The paper drive and reverse clutches are actuated to drive the form into the machine. The FPS triggers a PS whose output with PDFF•NOT LWLFF•REVFF will cause the RLFF to be set to prepare for reading pulses. The Set RLFF signal sets Seq. A (SA) FF, resets FFZ and gates the R1 reset pulse. R1 sets DDO signal high and resets the SRCX FFs, SRCYFFs, the parity X and Y FFs, the data X and Y FFs and the discriminator (DISC X and Y) FFs.

At the end of SA, the following conditions are active.

<u>SA</u>

(SET CAD)	The special address (SA) FFs cause the "C" address selected by the MART and MARU FF to be active.
(2⟶MART)	The MART2FF is set to select the 20 group of memory locations.
(0⟶MARU)	The MARU FFs are reset to select memory location 20.
(RESET MART 4)	MART 4 is reset to ensure that memory location 60 is not selected.
(0⟶WR)	The WR is cleared prior to the start of Reading pulses to ensure a true indication of the first digit read.
(WR⟶MEM)	The WR to MEM FF is set so that data read from the stripe and transferred to the WR can be written into memory.
(RESET DDREV)	Data was written on the stripe in descending order from DDMSD to DDO and must be read in ascending order, therefore DDREVFF must be reset.
(RESET COMPFF)	The COMPFF is reset so that all data will be handled in true form. At this point the logic waits for pulses to be read from the card as the card is fed into the machine. The program camshaft will be rotated to 144° before the form is started into the carriage.

If the machine is a DS machine, three reading conditions are possible. (1) Read AMPX pulses may occur before Read AMPY pulses. (2) Read AMPY pulses may occur before Read AMPX pulses or (3) both Read AMPX and READ AMPY pulses may occur simultaneously. There is no conflict here since two independent sets of shift Register FFs (SRX1-2-4-8 and SRY1-2-4-8) are provided. Data is read from the stripes into the SRX and SRY FFs. All data from SRXFFs and SRYFFs must be transferred to the WRFFs one digit at a time to be written into memory. The data from the stripe that is read first will be written into memory first.

If both stripes are read simultaneously, the left stripe (Y data) will take precedence and be written into memory first. The 1X and 1Y FFs control the order of writing digits (X or Y) into memory. If FF1X is set, the X data digits will be written into the 20's before the Y data digits are written into the 30's. If FF1Y is set, the Y data digits will be written into the 30's before the X data digits are written into the 20's. The 1X or 1Y FF that is set remains set for the entire read operation. Both FF1X and FF1Y can never remain set simultaneously during the Read Ledger operation.

A single stripe (SS) machine contains data on the X or middle stripe only and the FF1X will be set. No writing is done in the 30's memory locations due to the absence of several (DS) logic card in the machine.

(Fig. V-16 and V-17) assume now that the first pulse is read from the X stripe before the first pulse is read from the Y stripe.

(READ AMPX) The first read ampx pulse, (CP) RLFF and NOT DISC FF sets the DISC FF. The purpose of the DISC X FF and its associated circuits shown in Fig. V-15 is to recognize and separate the data pulses (DP) from the complement pulses (CP).

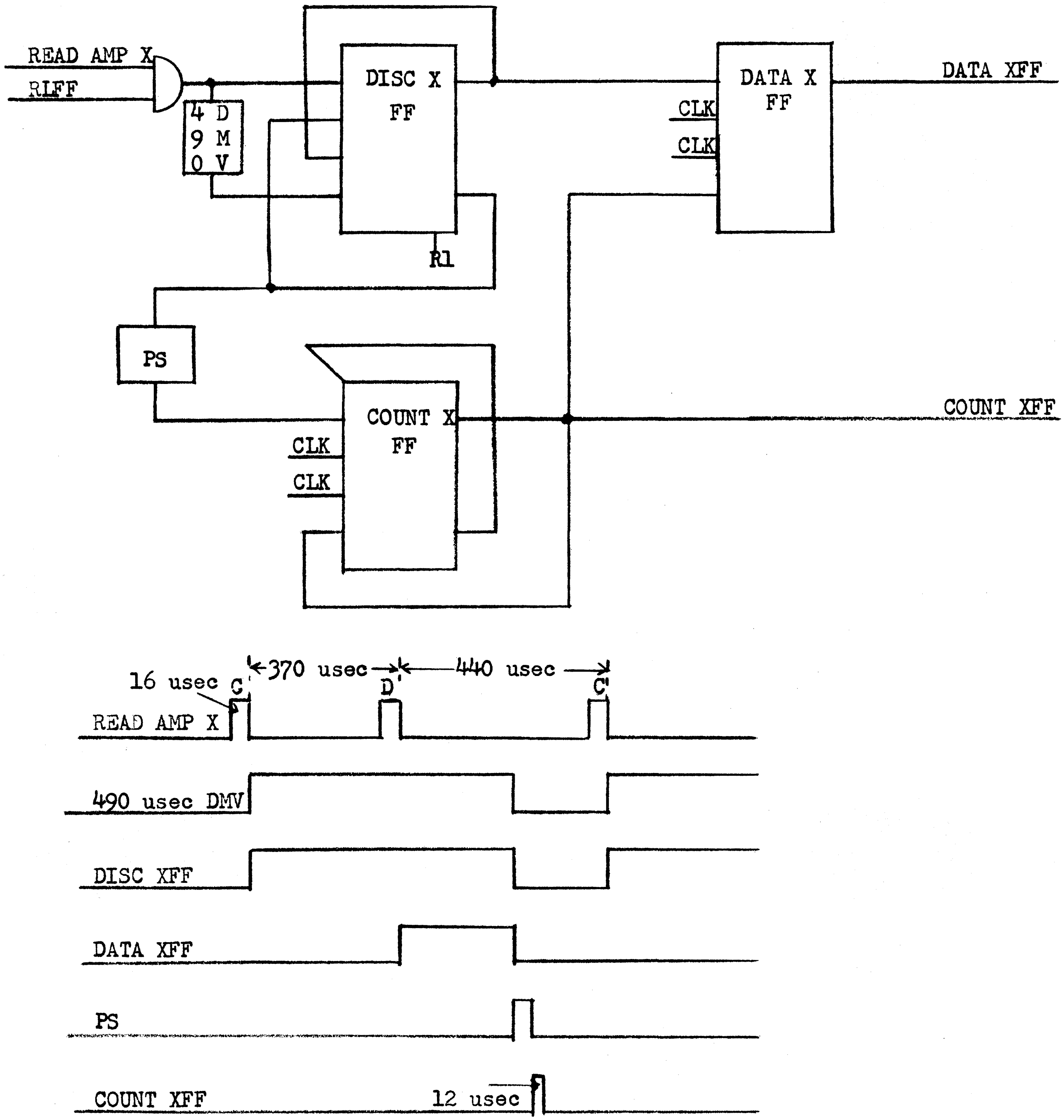

READ AMP X
RIFF
4 D
9 M
0 V
DISC X
FF
R1
DATA X
FF
CLK
CLK
DATA XFF
PS
COUNT X
FF
CLK
CLK
COUNT XFF
16 usec
C'
370 usec
D'
440 usec
C'
READ AMP X
490 usec DMV
DISC XFF
DATA XFF
PS
COUNT XFF
12 usec

Figure V-15

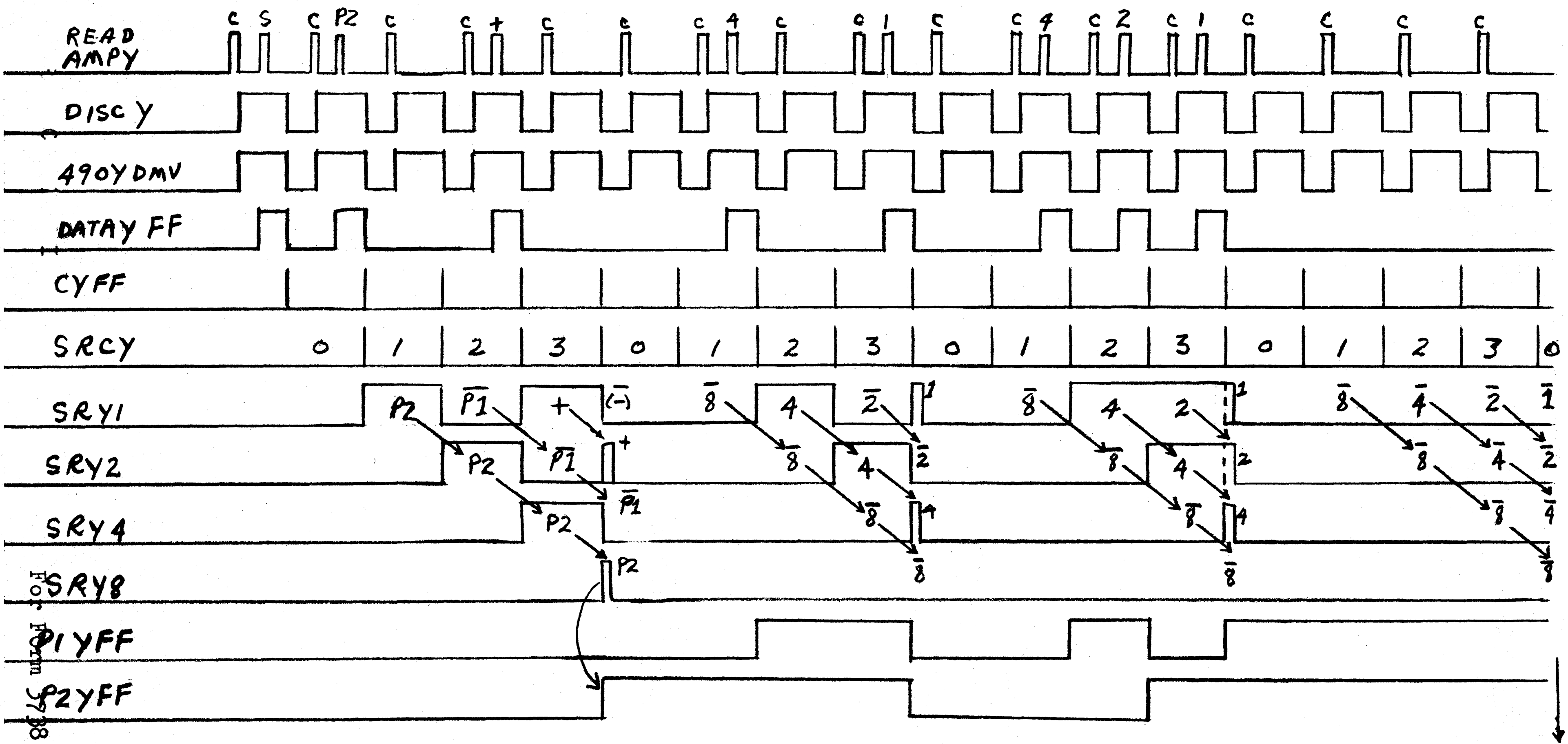

READ AMPY
DISCY
490YDMV
DATAY FF
CYFF
SRCY
SRY1
SRY2
SRY4
SRY8
P1YFF
P2YFF

FIGURE V-16A

(Draft E2150)

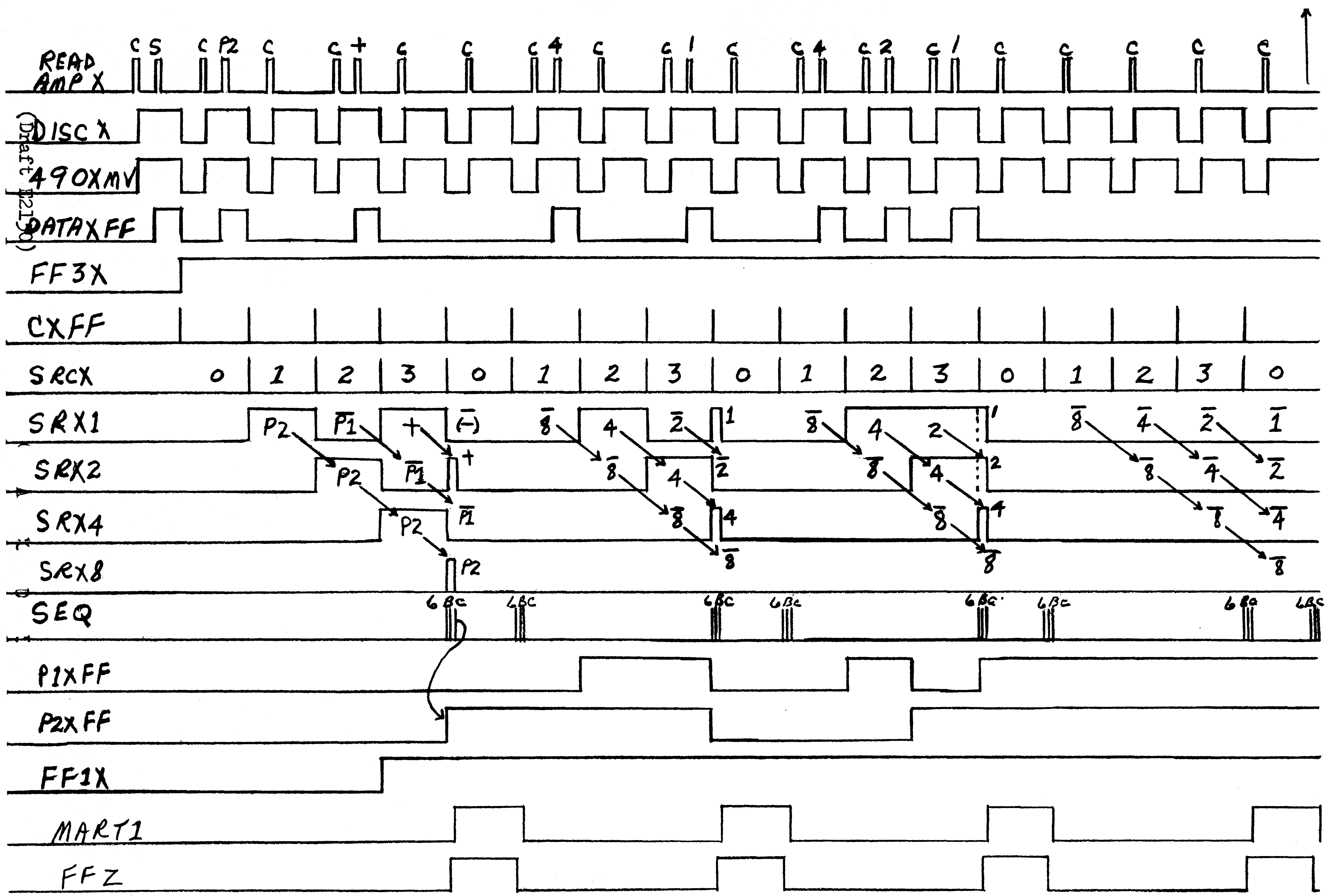


FIGURE V-16B

For Form 3738

(TRIGGER 490 usec DMV) The CP signal which set the DISC FF, triggers a 490 usec DMV. If another read AMPX pulse occurs within the 490 usec period, it will be recognized as a DP (normally a data pulse follows a CP by 440 usec). This results from the 370 usec USMVFF pulses and the 70 usec delay on the write operation).

(SET DATA X FF) The DATA X FF will be set by the Read AMPX (DP)•RLFF•DISC X FF•CLK signal. The DATA X FF will remain set from the time the Read AMPX (DP) signal until after the 490 usec DMV times out. A nominal time for DATA X FF to be on is 200 usec.

(RESET DISC X FF) The end of the 490 DMV pulse resets the DISC FF.

(SET COUNT X FF) The resetting of the DISC X FF causes the PS•CLK•NOT COUNT X FF to set the COUNT X FF. The following clock pulse and COUNT X FF pulse resets the COUNT X FF. The CXFF signal will be high for one clock duration each time the DISC FF is reset by the 490 usec DMV and will start at the clock pulse following the reset of the DISC FF.

(RESET DATA X FF) The DATA X FF is reset by the CXFF•CLK signal. The main function of the DATA X FF at this time (the first data pulse or start signal) is to Set FF3X. The setting of FF3X is a indication that the start read signal has been received and that the following pulses should be processed as pertinent information.

(SET DISC X FF) The third READ AMPX pulse sets the DISC FF again.

(490 usec DMV) The third READ AMPX pulse triggers the 490 usec DMV.

(6ms RESETTABLE) Since the 3XFF is now high, the FF3X•NOT FF16•READ AMPX signal triggers the 6 ms Resettable DMV. Every READ AMPX pulse will retrigger the 6 ms DMV. 6ms after the last data is read, the 6ms resettable DMV will become high and cause FF16 to be set. FF16 is an indication to the machine that the next READ AMPX pulse will be that of the sync pulse. The sync pulse is a signal to stop form travel.

(SET DATA X FF) If the next READ AMPX pulse occurs while the DISC FF is set (while the 490 usec DMV is set) the pulse will be recognized as a DATA X pulse and the DATA X FF will be set.

(490 usec MV times out)

(RESET DISC X FF) When the 490 usec MV times out the DISC FF is reset.

(SET COUNT X FF) The resetting of the DISC FF through a PS•NOT COUNT X FF•CLK sets COUNT X FF. The CXFF•FF3X causes the Shift Register Counter (SRCX) FFs to be advanced and gates the data X FF to the Shift Register X1FF (SRX1FF). The gating of the data X FF stores the data pulse read from the stripe in the SRX1FF.

(COUNT PARITY X) Since the machine is reading DDO the parity FFs will not be counted due to the NOT DDO signal being low.

The following complement and data pulses perform the same functions as above. A COUNTXFF pulse occurs as a result of each complement pulse read. The COUNT X FF pulse occurs approximately 490 usec after the complement pulse and allows time for data to be stored in the DATA FF if a data pulse is read. The COUNTXFF pulse will then (1) gate the output of DATA FF to SRX1FF (2) cause a shift of the SRX FFs (3) count the number of SRX shifts that have been made and (4) count the parity FFs except when DDO is high.

(SET FF1X) When the Shift Register Counter equals 2 (SRCX2) the SRCX2•CXFF•NOT FF1Y•CLK will set FF1X. NOT FF1Y will be high in a SS machine or if the X stripe is being read first in a DS machine. It should be remembered that in a DS machine the Y stripe is being read simultaneously with the X stripe with a completely independent set of circuits. If the SRCY2 becomes high before SRCX2, the FF1Y will be set and NOT FF1Y be low to prevent setting FF1X. In the same manner if SRCX2 becomes high before SRCY2 (as assumed here) the NOT FF1X will be low and prevent setting FF1Y. If both FF1X and FF1Y are set at the same clock pulse FF1X will be reset at the next clock pulse by the RLFF•FF1Y•CLK signal. With FF1X set, the data from the SRXFF will be transferred to the WR and written into the 20's of memory before the data from the SRYFF is transferred to the WR and written into the 30's of memory.

(SET FF6) When SRCX=3 the next CXFF pulse will gate the last bit of the digit being read to the SRX FF and the 1, 2, 4 and 8 bits of the digit will be shifted into respective SRXFFs. The SRCX=3•NOT FF1Y•CXFF will trigger a PS. The PS output• NOT FF6•CLK will set FF6. The purpose of FF6 is to synchronize the RL operation with the E2100 operation. FF6 is reset on the following clock pulse by FF6•CLK. FF6•RLFF•CLK sets sequence B.

SB

(READ) DDO of MA 20 will be read (MA 20 was selected in SA). The purpose of the read is to clear the old data from the location.

(COMPLEMENT FFZ) (DS) FFZ is complemented. In this case, it is set since it was reset by the R1 signal. FFZ controls the transferring the data from the SRX and SRY into the WR.

(SRX⟶WR) Since FFZ is reset until after this sequence the data in the SRX is transferred to the WR. In DDO the only bit which is important to Memory is the one bit which is the sign of the word.

SRX4—>P1XFF & SRX8—>P2XFF) The 4 and 8 bit positions of DDO contain the parity count (which was written in complementry form during WL) for the word. DDO•NOT FFZ transfers the parity count to the parity FFS.

SC

(WRITE) The data in the WR is written into DDO of memory location 20.

(COMPLEMENT MART) (DS) The MART1FF is complemented. In this case it is set to select memory location 30.

(O—>SRX) The SRX is set to zero. This is not significient at this time.

(STEP DD) (SS) The DD will be stepped at the end of SC in a single strip machine but not until after the data from both stripes is written on a DS machine.

On a Single Strip Machine the logic waits, as reading of the strip continues, until the SRCX3 is again high, which would again set FF6. On a Dual Stripe Machine, FF6 will be set when SRCY=O•FFZ•FF1X•CLK is high. It is possible for FF6 to set by the same clock which reset SC, or it may occur at some time later whenever SRCY=O become high. FF6 will be reset after one clock duration and will set Sequence B.

SB (DS)

(READ) DDO of memory address 30 is read to clear the old information.

(COMPLEMENT FFZ) FFZ is complemented, in this case reset.

(SRCY—>WR) The data in the SRCY (from the Y stripe) is transferred to the WR. Only the one bit is important to memory.

(SRY4—>P1YFF & SRY8—>P2YFF) DDO•FFZ gates the parity count (in complementary form) for the first word on the Y stripe to the parity FFs.

SC (DS)

(WRITE) The sign of the first word on the Y stripe is written from the WR into DDO of memory address 30.

(COMPLEMENT MART) MART1FF is reset to select memory address 20 again.

(O—>SRY) NOT FFZ causes the SRY FFs to be reset. This is not significient at this time.

(STEP DD) The DD is stepped to DD1.

Reading of the stripes continues and when SRCX3 is high with CXFF•NOT FF1Y•CLK the DD1 data read from the stripes will be written into DD1 of the memory locations during SB and SC. In the same manner each digit is written into Memory. When DDMSD is reached, the MARU FFs must be counted so that data can be written into memory locations 21 and 31. Assume now that DDMSD is high with SC and the memory address is 30.

(WRITE) DDMSD data is written in memory location 30.

(COMPLEMENT MART) MART1FF is reset to select memory location 20.

(STEP DD) The Digit Distributor is stepped to DD0.

(0⟶WR) DDMSD•FF1X•NOT FFZ sets the WR to zero. The WR is an input to the adder and must be clear.

(SET CiFF) The CiFF is set by DDMSD•FF1X•NOT FFZ so that the MARU can be advanced one location.

(SEQ 10) S10 is set by DDMSD•FF1X•NOT FFZ.

<u>S10</u>

(0⟶MR) The MR must be cleared since it is an input to the adder. The MR is cleared between clock pulses and will be clear before the end of the sequence.

(GATE MARU⟶ADDER) The MARUFFs and CiFF are inputs to the adder.

(GATE ADDER⟶MARU) The MARUFFs are set to the adder output by CiFF. Thus the MARU is advanced by one.

(S10) Sequence 10 FF is set by CiFF and the Sequence stays on for two clock durations. This has no significance on this operation but is necessary for future equipment.

(RESET CiFF) The CiFF is reset after the first clock pulse. The CiFF being low will prevent gating the ADDER to the MARU the second time and reset S10 after the second clock duration.

Reading of data continues until all data is read and transferred to the memory. 6ms after the last data is read, the 6 ms resettable DMV times out.

(FF16) FF16 is set by the 6MS DMV•FF3X•CLK. FF16 indicates to the logic that all data has been read and that the next READ AMPX Pulse will be that of the sync pulse on the stripe.

(RESET RLFF) FF16•RLFF•DDO•CLK resets the RLFF.

(RESET FF1X + FF1Y) FF16•RLFF•DDO•CLK resets the 1X or 1Y FF that was set while reading DDO of the first words (20 and 30). When FF16 is set, the Read Ledger Handling Logic takes over and proceeds to align the form at the printing line as already discussed.

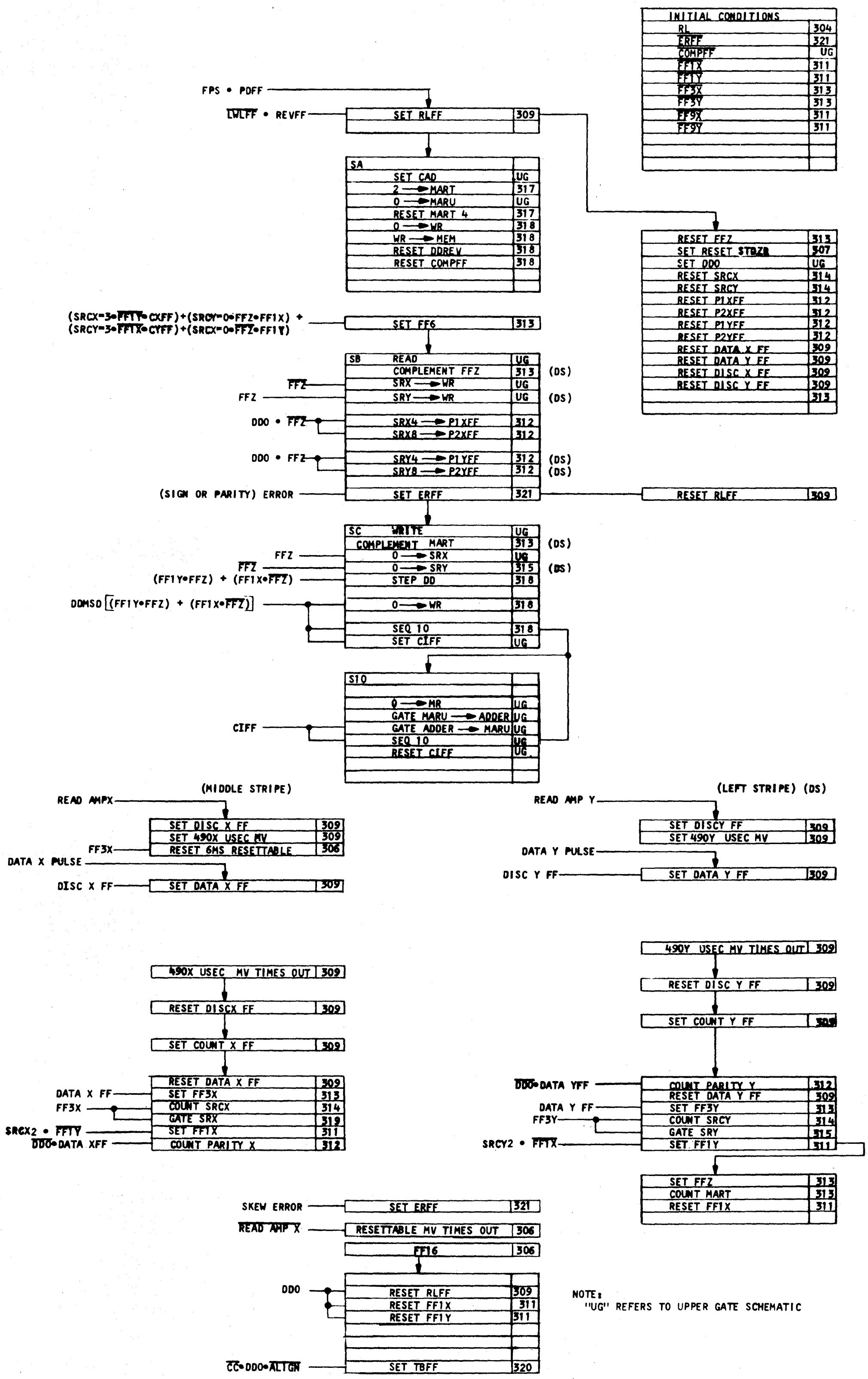

INITIAL CONDITIONS
RL 304
ERFF 321
COMPFF UG
FF1X 311
FF1Y 311
FF3X 313
FF3Y 313
FF9X 311
FF9Y 311
FPS • PDFF
LWLFF • REVFF
SET RLFF 309
SA
SET CAD UG
2 → MART 317
0 → MARU UG
RESET MART 4 317
0 → WR 318
WR → MEM 318
RESET DDREV 318
RESET COMPFF 318
RESET FFZ 313
SET RESET STBZB 307
SET DDO UG
RESET SRCX 314
RESET SRCY 314
RESET P1XFF 312
RESET P2XFF 312
RESET P1YFF 312
RESET P2YFF 312
RESET DATA X FF 309
RESET DATA Y FF 309
RESET DISC X FF 309
RESET DISC Y FF 309
313
(SRCX=3•FF1Y•CXFF)+(SRCY=0•FFZ•FF1X) +
(SRCY=3•FF1X•CYFF)+(SRCX=0•FFZ•FF1Y)
SET FF6 313
SB READ UG
COMPLEMENT FFZ 313 (DS)
FFZ
SRX → WR UG
FFZ
SRY → WR UG (DS)
DDO • FFZ
SRX4 → P1XFF 312
SRX8 → P2XFF 312
DDO • FFZ
SRY4 → P1YFF 312 (DS)
SRY8 → P2YFF 312 (DS)
(SIGN OR PARITY) ERROR
SET ERFF 321
RESET RLFF 309
SC WRITE UG
COMPLEMENT MART 313 (DS)
FFZ
0 → SRX UG
FFZ
0 → SRY 315 (DS)
(FF1Y•FFZ) + (FF1X•FFZ)
STEP DD 318
DDMSD [(FF1Y•FFZ) + (FF1X•FFZ)]
0 → WR 318
SEQ 10 318
SET CIFF UG
S10
0 → MR UG
GATE MARU → ADDER UG
CIFF
GATE ADDER → MARU UG
SEQ 10 UG
RESET CIFF UG
(MIDDLE STRIPE)
READ AMPX
SET DISC X FF 309
SET 490X USEC MV 309
FF3X
RESET 6MS RESETTABLE 306
DATA X PULSE
DISC X FF
SET DATA X FF 309
(LEFT STRIPE) (DS)
READ AMP Y
SET DISCY FF 309
SET 490Y USEC MV 309
DATA Y PULSE
DISC Y FF
SET DATA Y FF 309
490X USEC MV TIMES OUT 309
RESET DISCX FF 309
SET COUNT X FF 309
RESET DATA X FF 309
DATA X FF
SET FF3X 313
FF3X
COUNT SRCX 314
GATE SRX 319
SRCX2 • FF1Y
SET FF1X 311
DDO•DATA XFF
COUNT PARITY X 312
490Y USEC MV TIMES OUT 309
RESET DISC Y FF 309
SET COUNT Y FF 309
DDO•DATA YFF
COUNT PARITY Y 312
RESET DATA Y FF 309
DATA Y FF
SET FF3Y 313
FF3Y
COUNT SRCY 314
GATE SRY 315
SRCY2 • FF1X
SET FF1Y 311
SET FFZ 313
COUNT MART 313
RESET FF1X 311
SKEW ERROR
SET ERFF 321
READ AMP X
RESETTABLE MV TIMES OUT 306
FF16 306
DDO
RESET RLFF 309
RESET FF1X 311
RESET FF1Y 311
CC•DDO•ALTGN
SET TBFF 320
NOTE:
"UG" REFERS TO UPPER GATE SCHEMATIC

Figure V-17

VERIFICATION

The data in memory location 20 can be verified against data on the keyboard. The entire 12 digits of the keyboard is verified against the 12 digits of the memory location. Since the keyboard has no representation of the sign, the sign cannot be verified. Verification can be obtained in any position where programmed except where a machine repeat is used to get into the stop position. If verification is programmed with a striped ledger Read operation, the verification occurs while the program camshaft is at 144°. The operation will be performed after the read operation is finished and the line has been found. The logic is initiated by the PTFF just prior to the console cycle. If items are to be verified during posting, the verification occurs while the program camshaft is at 216° and is triggered by the PTFF just prior to each posting cycle. When the carriage stops in a position pinned for verification and CC5 is high or when set POFF Sig. is high after a Read ledger, the verify flip flop (VFF) is set by clock. The VFF causes the striped ledger lock up signal LUSL to be high which picks the LOCK relay to prevent a machine cycle. When a verification is completed, the VFF will be reset and releases the machine for operation. The verification must be completed before the printer cycle is initiated. The keyboard data must be read before the start relay is picked to remove the +35 wetting voltage from the contacts. This is accomplished by inserting a set of printer trip relay contacts in the wetting voltage circuit.

As in the E2100 print operation, the criterion for recognizing digits is the SUM = 9 signal from the adder. In the verification operation, the SUM = 9 adder output is obtained by entering the keyboard digit into the adder through the WR and entering the memory digit into the adder in complementary form from the MR. The CiFF must remain reset to obtain a nines complement. If the MR and WR contain the same digit, the SUM = 9 signal will be high to indicate verification.

SET VFF — If verification is programmed after a RL operation (lane 58), V•NOT ERFF•SET POFF•SIG•CK signal will set VFF. If verification is programmed during posting (lane 58), V•CC5•NOT PTFF•NOT EJFF•CK will set VFF.

FF6 — FF6 is used for synchronization of the control console or SL operation with the E2100 clock. If verification follows a RL operation, the POFF•PTFF•VFF signal triggers a PS. The PS•NOT FF6•CK sets FF6. If the verification is during posting, the CC5•PTFF•VFF signal triggers the PS. The PS•NOT FF6•CK sets FF6. FF6 is a complementing FF and is reset at the next clock pulse.

RESET FFZ (DS) — FFZ is reset in a Dual Stripe machine.

SAFF — The SAFF is set by VFF•FF6•NOT SAFF•CK. Sequence A performs its usual function of setting or resetting the control for the verify operation.

SA

(RESET DDREVFF) — The DDREVFF is reset so that digits will be handled from DD1 through DDMSD.

STEP DD — The sign position is not verified and the DD1 is stepped to DD1.

SET COMPFF — The COMPFF is set so that the memory digit will enter the adder in complementary form.

0 → WR — The WR must be cleared prior to gating data from the keyboard.

(0 → MARU and 2 → MART) — The MARU is set to zero and MART is set to 2 so that memory location 20 will be verified.

SET CAD — The C address is set so that memory address 20 will be active.

RESET MART4 — The MART 4 FF is reset to ensure that memory address 60 is not selected.

SB

READ C — DD1 of the C address (20) is read into the MR.

GATE KB→WR — DD1 of the keyboard is gated into the WR.

COMPLEMENT FFZ (DS) — The complementing of FFZ is a normal and necessary function of SB on the RL and WL operations. The complementing of FFZ on this operation is not necessary but to prevent the complementing would have required additional logic circuitry. The result of complementing FFZ is that both SB and SC are on twice for each digit verified. This lengthens the verify time by approximately 288 usec. This additional time poses no timing problems. On a SS machine, there is no FFZ and only one read and one write of each digit is performed.

SET MR→MEM — The MR to memory FF is set so that the data can be written back into memory.

SC

WRITE C — Data from the MR is written into memory.

SEQB — SB is always set by SC except when DDMSD is high. This occurs after each digit has been handled for verification.

STEP DD — The DD is stepped every SC on a SS machine and every alternate SC on a DS machine.

RESET COMPFF and VFF — When each of the 12 digits have been verified, the NOT FFZ• SUM = 9•NOT ERFF•DDMSD•CK signal resets COMPFF and VFF. The resetting of VFF allows the LUSL signal to go low and release the lock of the machine.

SET ERFF — If at any time that SC is on the SUM = 9 signal is high, the ERFF will be set. The ERFF prevents a machine cycle however, the verifying process continues until VFF is reset in the usual manner.

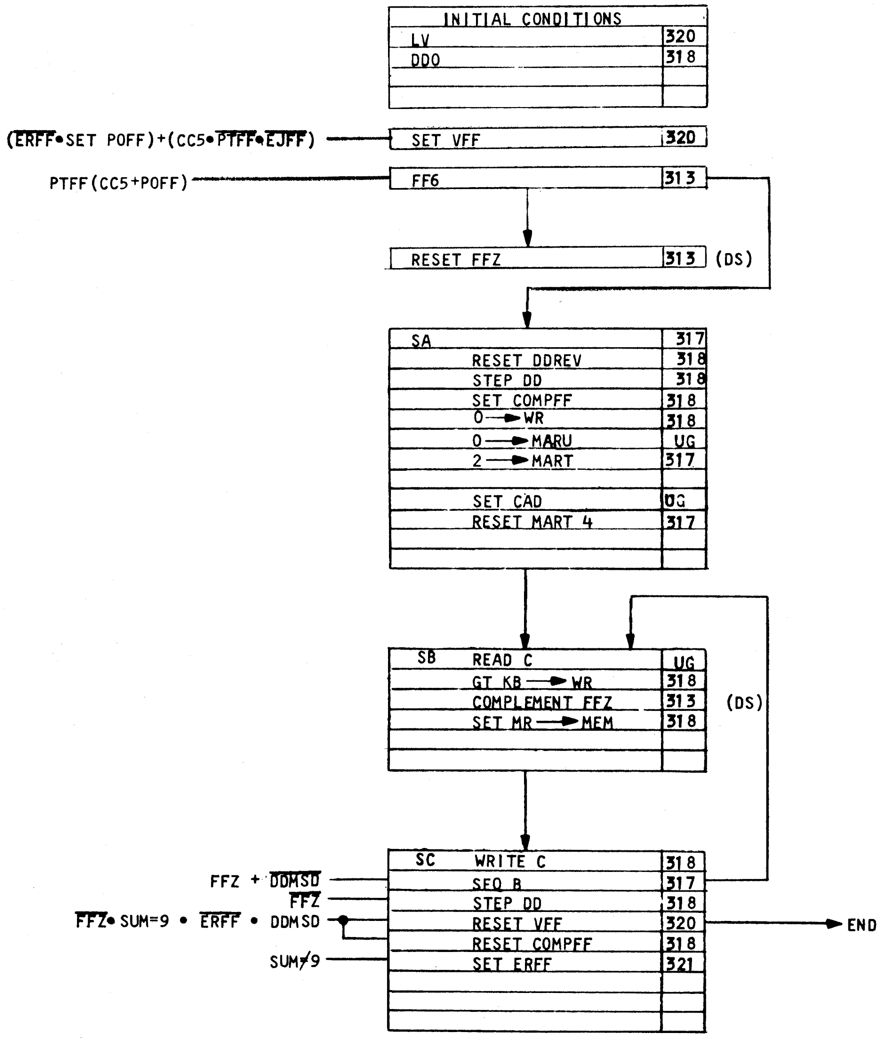


Figure V-18

NOTE:
"UG" REFERS TO UPPER GATE SCHEMATIC

TRIAL BALANCE AND BLOCK TRANSFER

The Trial Balance and Block Transfer operation is essentially a Read Ledger operation followed by an E2100 add or transfer clear operation. The operation is performed for each of the 20s memory locations where data is read from the stripe on SS and for each 20s and each 30s memory location where Dual Stripe is read.

In the Trial Balance operation, data read from each form is accumulated to provide a grand total of all forms read. The programming for this operation is RL and NOT ALIGN.

In the Block Transfer operation, data read from the form is transferred too but not accumulated in other memory locations. This operation is comparable to the E2100 Transfer Clear operation.

This allows data from the stripes on two forms to be entered into the machine for use during updating accounts. Programming for this operation consists of RL (lanes 56 and 66), the absence of align (lane 60) and Block Transfer (lane 61).

The RL part of this operation is the same as any other RL operation and will not be discussed here. References will be made to conditions during or at the end of the RL operation.

In a SS machine, only the memory locations from which data was read are active during the add part of the operation. If data is read from six locations (20 through 25), the additions begin with the highest location (25) and progress downward to 20. These additions are made to 35 down to 30 respectively. Since only memory locations where data is read from the stripe are involved, forms with varying amounts of data encoded can be handled on the same trial balance run. That is to say, forms with 4, 6 or 8 words encoded can be mixed on the Trial Balance.

Data is read from the stripe into the 20s and block added into the corresponding 30s.

In a DS machine, the additions start with the highest location read from the stripe and are added to the corresponding 60s locations. When 20 is reached, the MART1FF is set to select the 30s group and the MARU is counted down from 0 to 9 so that the additions continues from 20 - 60 to 39 - 79. Additions continue as the MARU is counted down to 30. The entire 30s group is added regardless of the number of words read from the stripe. This would result in incorrect accumulation of data in the upper 70s locations if forms with varying amounts of data are read on the TB operation. For DS BT then, all forms for a given run must contain the same number of words of data.

The Trial Balance or Block Transfer operation can be started as soon as the signal is received that all data has been read from the stripe. This signal is the timing out of the 6ms DMV which sets FF16. This will occur when the form is at approximately L-2 1/2 as the form is driven into the machine on the RL operation. The addition of 20 memory locations will require approximately 12.5 ms if no re-complementation is involved. The Trial Balance additions or Block Transfer will, in most cases, be completed before the form reaches L-4.

TRIAL BALANCE LOGIC

The initial conditions for the Trial Balance Logic are the conditions that exist at the end of the RL operations. Those that are important to the Trial Balance are as follows:

DDO — DDO is a normal ending condition of the RL operation. The DD is stepped to DDO in SC of the RL logic when DDMSD of the last word is written into memory.

RLFF — The RLFF is used to control the Read Ledger operation and is used to initiate the Trial Balance operation. RLFF is reset at the start of the TB operation.

MART 2 — MART 2 is set so that the stripe will be read into the 20s and 30s.

NOT ERFF — NOT ERFF indicates that a correct read has been performed.

NOT ALIGN — NOT ALIGN is a normal function and is the absence of a pin in the align lane. NOT ALIGN must be high so that the form will be driven out of the machine.

The Trial Balance operation is initiated by the NOT CC, which is an indication that the SRCX has counted properly. The NOT ALIGN (RL NOT ALIGN indicates a Trial Balance) and EORD which is an indication that all data on the stripe has been read. The following conditions are set up by the above signal.

RESET MART1FF — To ensure operating in the 20s first.

SET TBFF — TBFF controls the operation similar to a T time.

RESET FFZ — To correspond with the 20s M.A.

SET CiFF and 8 → WR — To count down MARU.

SET S1OFF — To count down MARU. A S10 function was performed at the end of the RL operation. This is a normal result of DDMSD. As a result of the S10 operation, the MARU is one higher than the last memory location read from the stripe. If 28 is the last word read, the MARU will be at 9 and must be counted back to 28 before additions begin.

S10

0 → MR — The MR is reset to prevent interference with the adder.

RESET CiFF — The CiFF will be reset after one clock duration of S10.

SET S10 — CiFF causes S10 to stay on for two clock durations.

GT MARU → ADDER — The MARU is made an input to the adder.

GT ADDER → MARU — The MARU is set equal to the adder (MARU + WR8 + CiFF). This counts the MARU down one memory location.

RESET SC FF — The SCFF is used for recomplementations control on the add operation and must be reset at the end of each word of the addition.

SEQO — TBFF and NOT CiFF returns the logic to SO after the second clock duration of S10. The additions of the 20s memory locations to the 30s on SS or of 20s and 30s to the 60s and 70s on DS is very similar to the standards E2100 TX additions. The main difference being the addition of one C location to another C location without the use of P memory location. The addition of C to C is accomplished by maintaining the CAD set and setting and resetting MART1FF and MART4FF as required.

SO — SO has the same function on the Trial Balance as with the normal E2100 add cycle which is to reset the control FFs (CiFF, COMPFF and SCFF) and select the C address where the data is to be accumulated.

S1 — The basic function of S1 is to read the data from the 30s (SS), 60s or 70s (DS) and select the corresponding location that is to be added.

S2 — The basic function of S2 is to read the data to be added and to set MR →MEM so that the data read in S2 can be written back in S3.

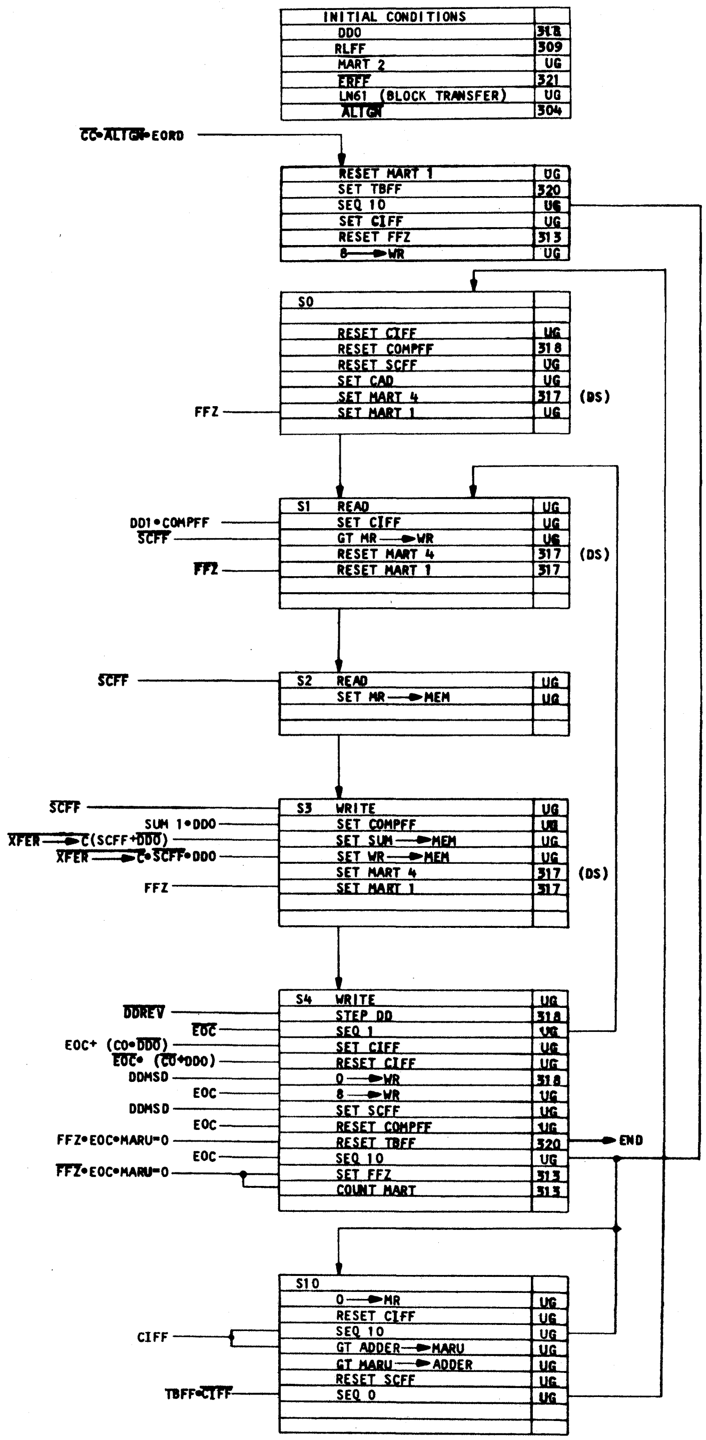
S3 — In S3 the data to be added is written back into the 20s (SS) or 20s and 30s (DS). At the end of S3, the SUM →MEMFF must be set if a Balance Transfer is being performed. This requires that the NOT XFER →C signal is high. The NOT XFER→C signal is an inversion of the NOT T5, NOT T4, NOT T3, NOT TC, and the K4 (lane 61) signals.

S3

K4 is the controlling signal of this group and is the Block Transfer lane during a SL operation. If lane 61 is not programmed (on a Trial Balance operation, it will not be programmed) the RW output will be inverted and become NOT XFER→C. If lane 61 is programmed, NOT XFER →C will be low and SUM →MEMFF cannot be set at the end of S3. In this case, MR →MEMFF will remain set and the data that is in the 20s (SS) or 20s and 30s (DS) will be written into the 30s (SS) or 60s and 70s (DS). This is a comparative operation to the TC operation of the E2100.

S4

In S4, data is written into the 30s (SS) or 60s and 70s (DS). The DD is stepped and the logic returns to S1 if NOT EOC is high. If EOC is high, the logic will go to S10 where the operation described above will be repeated. When memory location 20 (SS) or 30 (DS) has been added or transferred to 30 (SS) or 70 (DS) as the case may be, the FFZ EOC MARU = 0 signal will be high and the TBFF will be reset to end the operation.



NOTE:
1. XFER → C = TBFF•BT
2. $\overline{\text{XFER}}$ → C = TBFF•$\overline{\text{BT}}$
3. FFZ MUST FLOAT ON SINGLE STRIPE
4. "UG" REFERS TO UPPER GATE SCHEMATIC

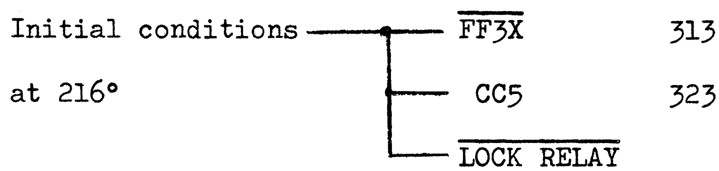
Figure V-19

FILLED SHEET AND EJECT OPERATION

There are two different modes in getting the machine into the filled sheet routine. One is during the posting operation (multiple posting), when the form has 37 lines printed and is spaced up to the 38th line.

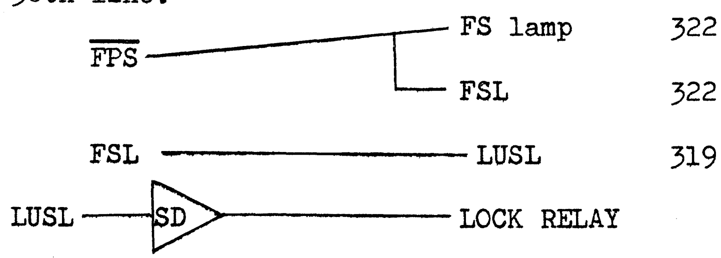
The other mode can occur during the read operation, when a sheet is fed into the machine which has 37 or 38 lines posted.

The filled sheet light will come up during posting, when the form is spaced up to the 38th line. At the 38th line, the beam of light on the front paper switch is not obstructed by the form any more and NOT FPS signal comes high. This starts a sequence of steps to indicate to the operator that the form has reached the last posting line.



Space up to the

38th line.



The LOCK RELAY is energized, the printer will not cycle and the FS lamp is on. In order to be able to post the 38th line and write the new data on the form, the FS light should be depressed which will close NO contacts of FSL SW.

FSL SW ———————	FS SW	313
$\overline{FFP}$ • CC5 • FSSW • CLK ———	Set FF3X	313
$\overline{FFP}$ • CC5 • FF3X ———	$\overline{FS\ LAMP}$	322
	$\overline{FSL}$	322
FSL ———————	LUSL (reset LOCK RELAY)	319

The Printer is cycled now.

The last line is now posted and the machine tabulates into the LWL position. As FF3X is still high, the machine can be cycled and start the write operation. At 250° of the program camshaft, CC2 comes high. CC2 and CLK will reset FF3X, which is one of the initial conditions for the write logic.

With LWLFF, CC2 comes high.

CC2 • CLK ——————— Reset FF3X 313

It should be noted that if FSL SW has been depressed in order to write the 38th line, the operator could go on posting the form out of the carriage. Therefore, after the FS light has come up, the last line should be posted. The write logic and the paper handler sequence will be performed in the same manner as on a not filled sheet operation.

If a form is read which has 37 or 38 lines posted, the read logic will advance as usual prior to the line find routine. In the case when the form has 37 lines posted, the line find pulse is between the 34 and 35 line. If the form has 38 lines posted, the line find pulse is between the 35th and 36th line. The routine explained in the following lines will be done taking a form with 37 lines posted, because it is more critical than the case with 38 lines.

As the line find pulse is between the 34th and 35th line, 2ms from the 34th line, the printer will get locked before tripped by MB2, avoiding the operation on the 38th line.

The information has been read into the memory, where it is stored and the FS light will be on. See Figure No. V-20 and refer to the paper handler logic in the read routine.

The LOCK RELAY prevents cycling the printer, the carriagemotor continues running, REVFF is reset and the program camshaft is at 144°. Depressing the FSL SW (filled sheet light switch) will turn high FS SW signal, which in turn causes EJFF to be set.

Initial Conditions

FSL	322
CC4	323
LOCK REL.	
$\overline{\text{REVFF}}$	305

Depressing FSL SW ——	FS SW	313
FSSW•CC4•FSL•CLK ——	Set EJFF	320
EJFF • CLK ——	CRG MOTOR FF (already set)	304
$\overline{\text{FPS}}$•CC1•EJFF•CLK ——	SET PROG CAM FF	304
EJFF • CLK ——	Reset PRINTER OPERATE FF	307

CRG MOTOR FF —— SD ——	ENERGIZE CRG MOTOR RELAY	
PROG CAMFF —— SD ——	ENERGIZE PROG CAM SOL	322
EJFF---100ms Delay ——	PDFF	305
PDFF•CRG OPEN•$\overline{\text{TAB}}$ ——	PDSOL	322

The program camshaft turns

CC2 ——	Reset	307
	Reset SL (R1)	307
CC1•CC5•CLK ——	Reset L-2FF	306

CC2•CC6•CLK	Reset EJFF	320
CC2•CC6•$\overline{\text{FPS}}$•CLK	Reset CRG MOTOR FF	304
CC2•CC6•$\overline{\text{FPS}}$•CLK	Set SSFF	305
CC2•EJFF•CLK	Reset PROG CAMFF	304
$\overline{\text{CRG MOTOR FF}}$ — SD	STOP CRG MOTOR	
$\overline{\text{PROG CAM FF}}$ — SD	DROP PROG CAM SOL	322
SSFF • BOLP	Reset PDFF SIG	305
Reset PDFF Sig•EJFF•CLK	Reset PDFF	305
$\overline{\text{PDFF}}$ — PDC	Energize Stop PD SOL	305

EJFF signal high will assure that the carriage motor stays on during the eject routine, will set the Program Cam FF, reset Printer Operate FF and trigger the 100ms DMV, which when timed out, set PDFF.

As soon as the program clutch solenoid is energized, the program clutch will trip and the program camshaft turn. Similarly, when the paper drive solenoid is energized, the paper drive clutch is tripped. As the REVFF is reset the form is driven out of the carriage. At 180° of the program camshaft, CC2 comes high causing a RESET and a RESET SL (R1) pulse.

CC1• CC5 will reset L-2FF and when CC2 • CC5 comes high, RLFF is reset. At approximately 320° of the program camshaft CC2 • CC6 comes high resetting EJFF and CRG MOTOR FF. NOT EJFF and CC2 reset PROG CAM FF. CRG MOTOR RELAY de-energizes and cuts the carriage motor power off.

As SSFF is set, the next BOLP gives a Reset PDFF SIG causing with NOT EJFF the resetting of PDFF. NOT PDFF energizes STOP PD SOL decoupling the paper drive clutch.

The program camshaft stops at 360° having performed logically the previous steps as well as restoring mechanically the paper handler tray.

FILLED SHEET OPERATION

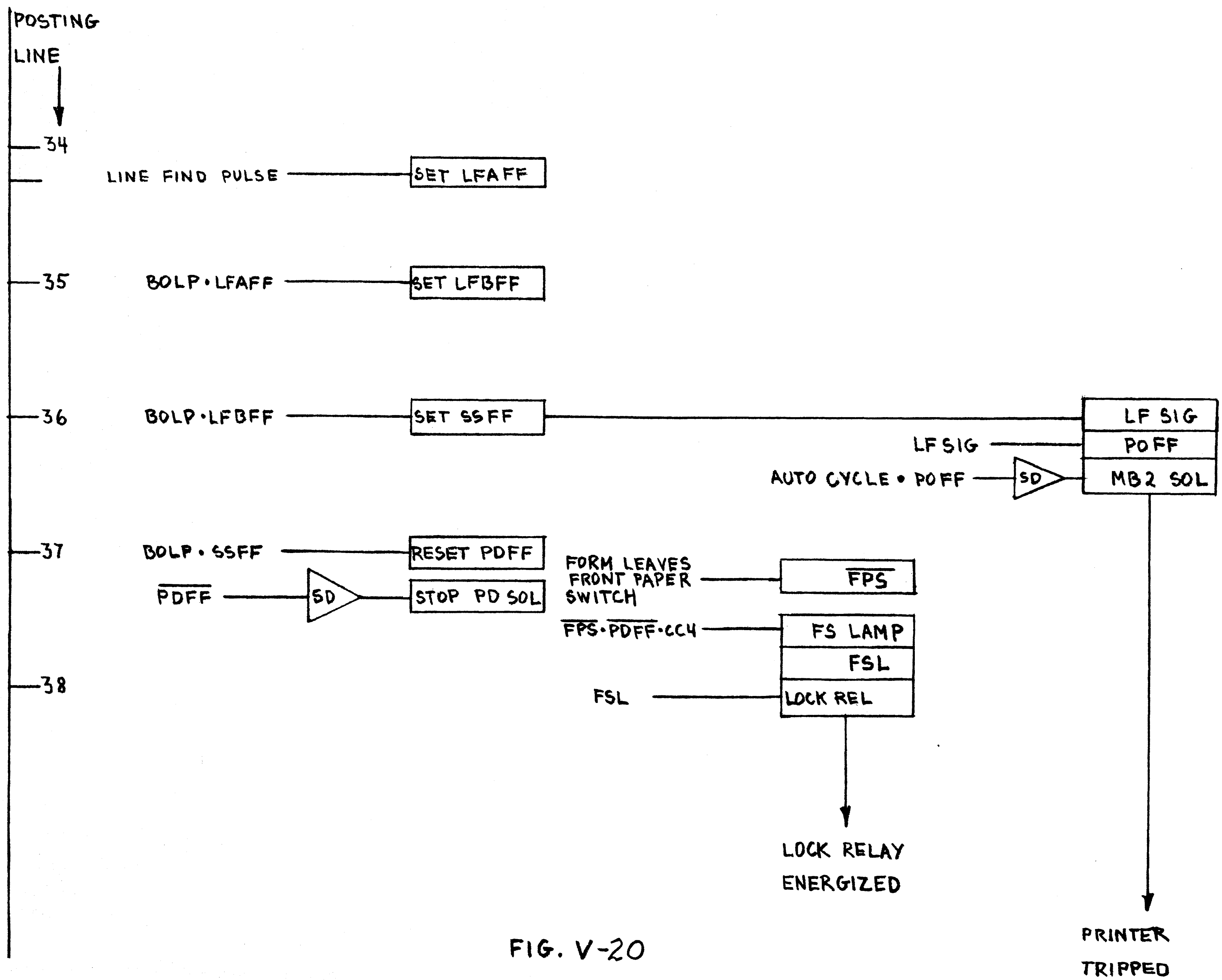


FIG. V-20

ERROR DETECTION GATING

The purpose of the ERROR FF and the gating that controls it, is to have in the E2150 a means of checking the read and write operation of the magnetic stripes on the form.

During the read operation, the read ledger logic follows a sequence which allows checking each word for parity, see gates No. 11, 14 and Fig. V-21, for its sign, gates No. 9, 10 and 12, 13, as well as form skew during the inward travel, gates No. 6 and 7. When all the cells of an incoming form have been read, the end of message check is performed, gates No. 15, 16 and 18.

The steps to test each of the previously named conditions are not performed at the same time during a read operation, but separately and at different points in the logic.

The parity check is performed at the end of each word that has been read from a form and stored in memory. Refer to the read ledger logic. Therefore, this check is performed in DDMSD as many times as words are written on the form. There are two parity counter FFs (P1 and P2) for the X stripe and two PFFs (P1 and P2) for the Y stripe. It is required at the end of each word that has been read, to have both parity FF set. This implies that the correct number of data pulses for a word have been picked up by the head and recorded by the electronic section. Data pulses, as they are read in, count up the parity counters. In order to fulfill the required parity condition at the end of each word, the initial setting of P1 and P2 for a word has to be in accordance with the data pertaining to the word. The reason which can cause that the parity FF do not fulfill the required condition of both being set at the end of a word, could be caused by information not being read from the card.

Not reading information can be due to the fact that it was not written on the form, is too weak to be picked up or was originally written on the form but the magnetic stripe is damaged and the information is therefore lost. This would cause the parity counter to be out of step with the rest of the logic and set the ERROR FF in DDMSD (Parity errors are detected by gate No. 11, Fig. V-21) for the X stripe and gate No. 14 controls parity for the Y stripe.

During DDO of each word, that is, at the read start of a word, logic checks if a sign, plus or minus has been read. It is possible to get an error condition due to having read two signs, see gates No. 9, 12 and Fig. V-21 or no sign, gates No. 10 and 13. Therefore, a sign for each word has to be written and also read back.

In the case where the numerical information stored on the form is all zeros, there will be two parity pulses and a sign pulse in DDO per word. The information has to be read back into the electronic section in order to set the parity flip flops. This assures that the machine is writing and reading the information correctly, even if the numerical data is zero.

The end of message check, gates No. 15, 16, 17 and Fig. V-21, tests if the counter FF (SRCX and SRCY) were stepped up correctly when all the information has been read from the form. As an example, it could happen that one or several complement pulses are not read during the last word. This would cause that the electronic section to fail to step uo to DDMSD and check parity. As it does not get into the routine of checking parity, it cannot detect the error by this means. The end of message gating checks if the counter flip flops (SRCX and SRCY) were counted up to one. If the logic has stepped through correctly, SRCX and SRCY were counted up from zero to one on the last complement pulse in DDMSD of the last word. When complement or complement and data pulses are missing in the last word, the end of message gating would detect this error.

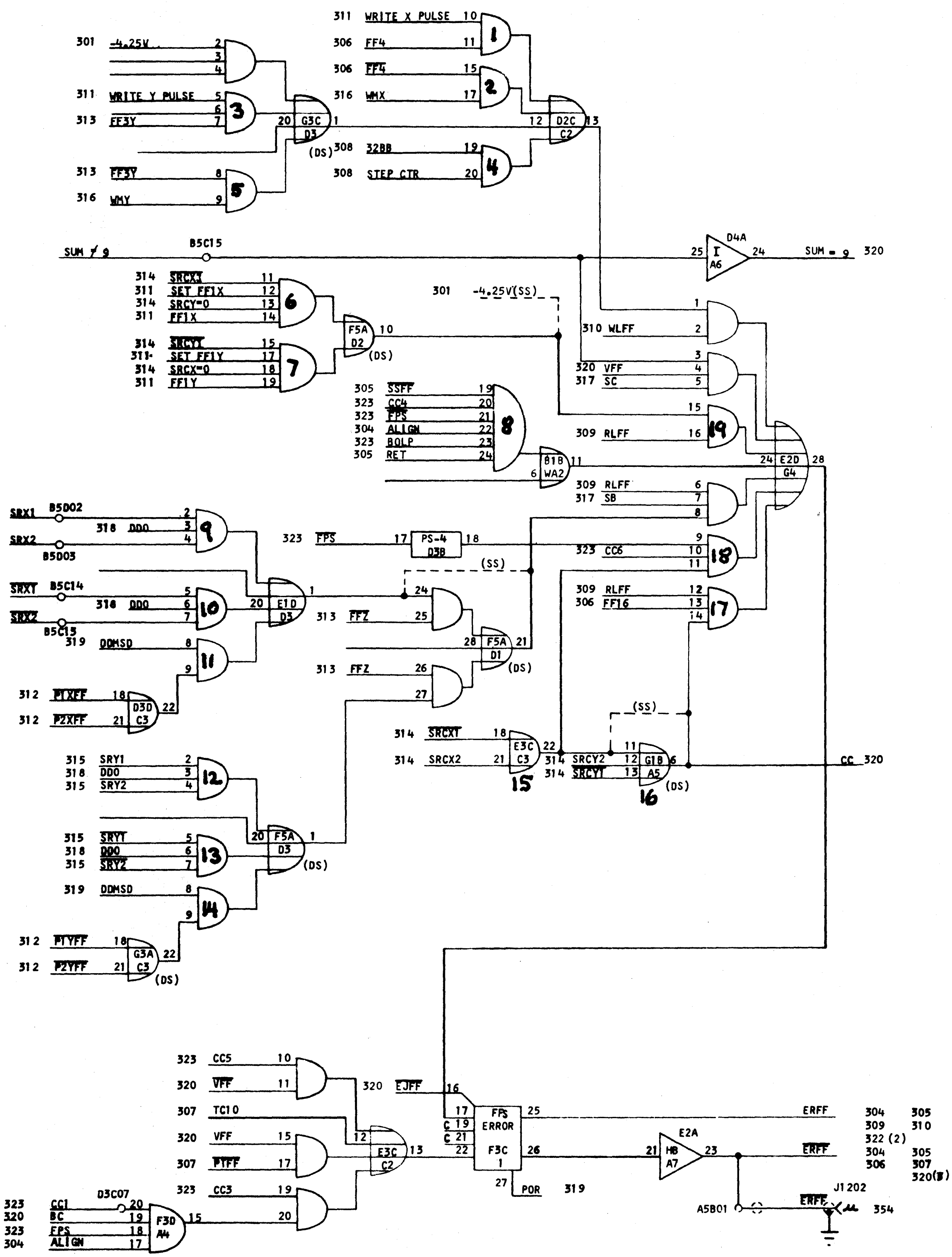

311 WRITE X PULSE
306 FF4
316 WMX
308 32BB
308 STEP CTR
301 -4.25V
311 WRITE Y PULSE
313 FF3Y
316 WMY
SUM ≠ 9
B5C15
SUM = 9 320
D4A
314 SRCX1
311 SET FF1X
314 SRCY=0
311 FF1X
314 SRCY1
311 SET FF1Y
314 SRCX=0
311 FF1Y
301 -4.25V(SS)
310 WLFF
320 VFF
317 SC
305 SSFF
323 CC4
323 FPS
304 ALIGN
323 BOLP
305 RET
309 RLFF
317 SB
323 CC6
306 FF16
SRX1 B5D02
318 DDO
SRX2 B5D03
SRXT B5C14
B5C13
319 DDMSD
312 P1XFF
312 P2XFF
323 FPS
PS-4
313 FFZ
314 SRCXT
314 SRCX2
314 SRCY2
314 SRCYT
CC 320
315 SRY1
318 DDO
315 SRY2
315 SRYT
319 DDMSD
312 P1YFF
312 P2YFF
323 CC5
320 VFF
307 TC10
307 P1FF
323 CC3
320 EJFF
FPS ERROR
F3C
27 POR 319
ERFF
304 305
309 310
322 (2)
304 305
306 307
320
J1202
A5B01
354
323 CC1
320 BC
323 FPS
304 ALIGN
D3C07

Figure V-21

The machine can get into an error condition if the form should skew. As can be recalled from the read ledger logic, FF1X or FF1Y can be set, depending on which of the pulses on stripes X or Y, will count up first the shift register counters to the third complement pulse in DDO of the first word. The setting of FF1X or FF1Y at this point determines for the rest of the reading operation of a form, if the X or Y side respectively will enter first for each digit into the memory storage logic. Taking an example, it will be supposed that FF1Y was set first during the reading of a form. Then FF1Y is set and FF1X is reset. The logic for storing the information into memory, which consists of FF6, SB and SC will then always wait to store the Y data for a particular digit first, before the X data can do the same. At the end of the X data storage in memory, the DDFF are stepped and the logic waits again for Y. Now, if due to skew the 4 X cells of a digit are read prior to the corresponding Y digit (4 Y cells), even though at the start of the reading FF1Y was high first, the logic waits until the 4 Y cells have been read from the stripe. When it is through with reading the 4 Y cells, the logic goes into the routine of storing the Y digit into memory. Once this is performed, the corresponding X digit, which was waiting the moment SRCX counted to zero, is stored in memory.

Suppose the delay the X digit (4 X cells) and Y digit (4 Y cells) under this situation is over 740 usec. (one cell). Signals on gate No. 7, Fig. V- 21 SRCX - 0, NOT SRCY - 1 and FF1Y will be high. When discriminator Y, set at the start of the third cell, times out, signal SET FF1Y comes high with the second CLK pulse thereafter, indicating that the skew is over 740 usec. and ERFF is set through gate No. 7, 19. See also timing Fig. V-21.

At this point, it should be recalled that data and complement information is written from the head in exact time intervals. The actual spot where it is recorded on the stripes during the write operation, depends on the form travel and the relative position between the magnetic heads.

Therefore, the physical intervals between data and complement pulses on a stripe will have certain variations from one cell to the other and also a cell on one stripe with its corresponding cell on the other stripe. During read, the time interval between the magnetic recorded complement and data information as it passes under the heads, where it is sensed, is again subject to form travel as well as its location on the stripe. Therefore, when a form is read, data and complement pulses are actually received by the electronic section in a time range around the original timing intervals given during the write operation. This time range is around 70 usec.

Now taking this into consideration, suppose a form gets, due to skew, into a timing difference of around 740 usec. between the X digit leading the Y digit with FF1Y set. Because of the range in which the pulses are read, on some occasions the timing difference between digits will be under 740 usec. and on others above. The first time the conditions at gate No. 7 and fulfilled, will set ERFF as shown in timing Fig. No. V-22 and the reading operation is stopped.

The form can also skew in the other direction, that is, if for example FF1Y is set at the beginning of a read operation and the cells on the Y stripe for each digit are always read ahead of its corresponding X cells. The limits in regards to the logic in this case, before ERFF is set, are wider than in the previous case. It could also be possible to get into a situation as just described, without skew, but due to the fact that the X head is positioned ahead of the Y head and the form so written, is read on another machine with the magnetic heads correctly set. Under this situation, the Y cells for a digit could be read up to 1480 usec. (two cells) minus one clock pulse ahead of its corresponding X cells without setting ERFF. Again, due to the range in which the recorded information is read in, a form which has around two cells timing difference between the Y and Y cells, Y leading Y with FF1Y set, set ERFF as soon as the required conditions on Gate No. 7, Fig. No. V- 21 are fulfilled. Also refer to timing Fig. V-23.

(Draft E2150)

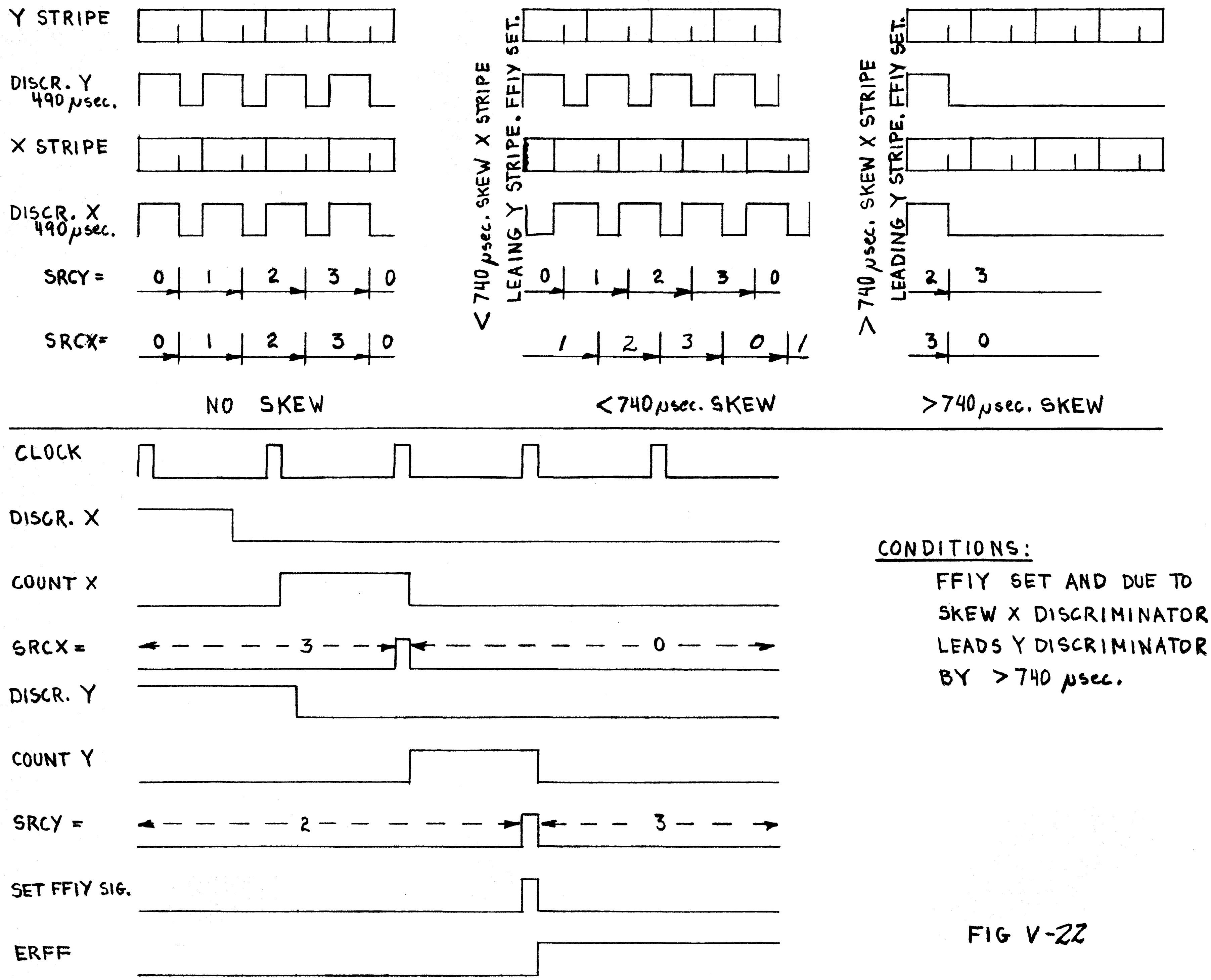
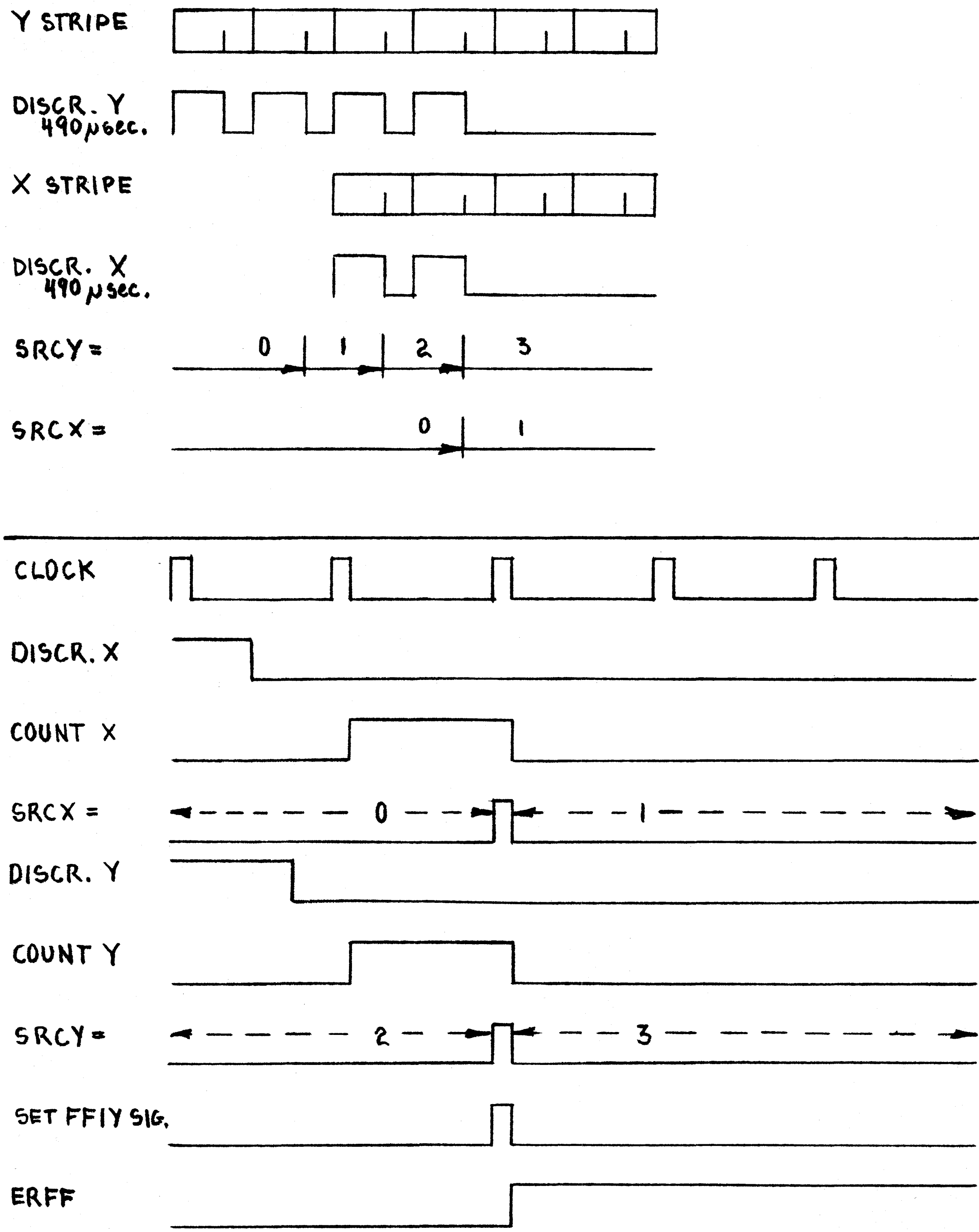


FIG V-22

(Draft E2150)



CONDITIONS:

FFIY SET AND DUE TO SKEW Y DISCRIMINATOR LEADS X DISCRIMINATOR BY 2×740 μsec.

FIG V-23

TYPICAL EXAMPLE OF X SKEW ERROR WHEN Y WAS LEADING

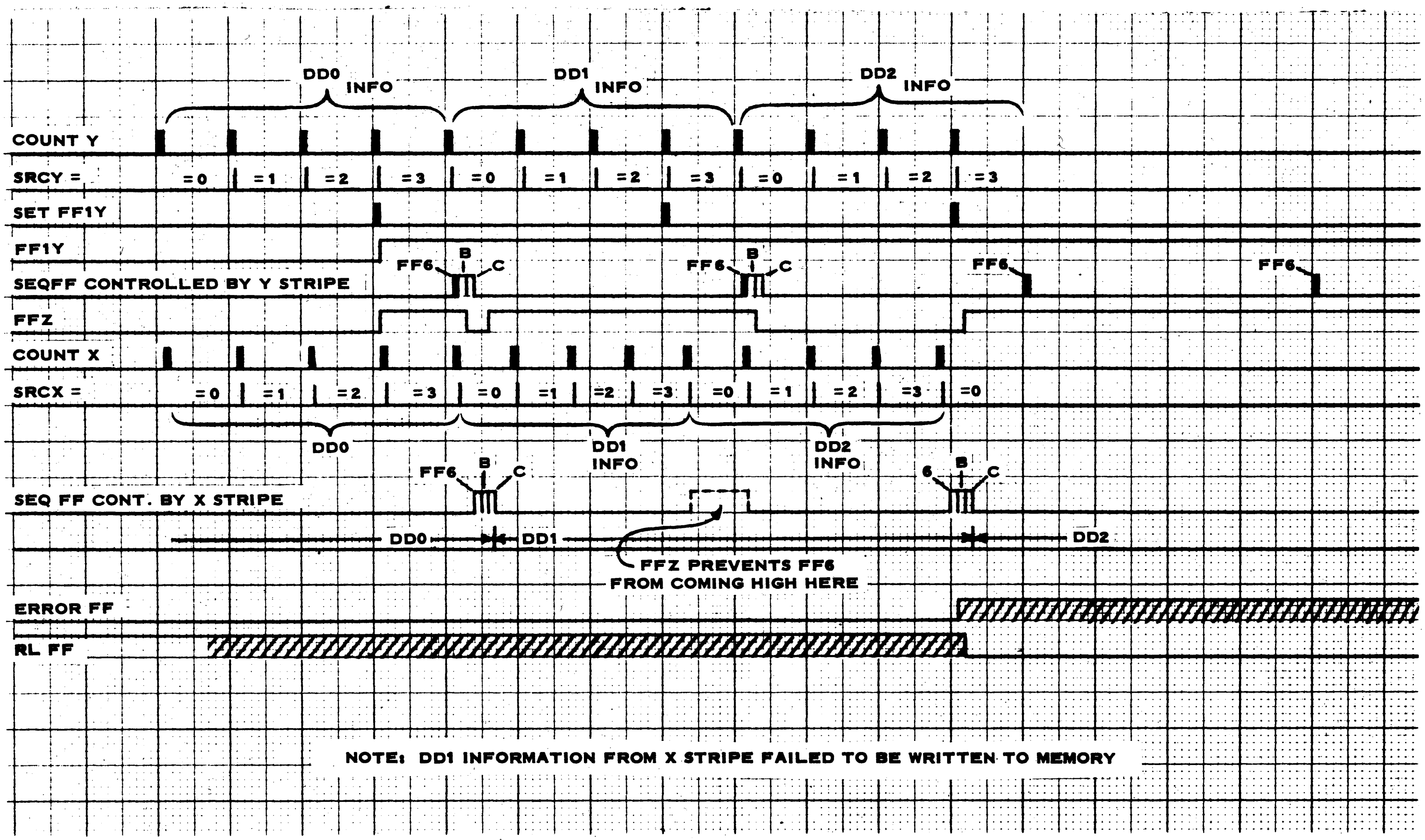


FIGURE V-23-1

When an error should occur during the reading of a form, one of the previously mentioned conditions sets ERFF. ERFF in turn resets RLFF, resets CRG MOTOR FF, the form stops traveling and the read lamp on the right of the keyboard remains lit.

Error Condition $\overline{\text{EJFF}} \cdot \text{CLK}$	Set ERFF	321
$\overline{\text{LWLFF}} \cdot \overline{\text{VFF}} \cdot \text{ERFF}$	Read Light	322
SD	Read Lamp	
$\text{ERFF} \cdot \text{RLFF} \cdot \text{CLK}$	Reset CRG MOTOR FF	304
$\text{ERFF} \cdot \text{CLK}$	Reset RLFF	309
$\text{ERFF} \cdot \overline{\text{EJFF}} \cdot \text{CC4} \cdot \text{CLK}$	Set SSFF	305
$\overline{\text{CRG MOTOR FF}}$ — SD	Stop CRG MOTOR	
$\text{SSFF} \cdot \text{BOLP}$	Reset PDFF SIG	305
Reset PDFF SIG $\cdot$ REVFF	RESET	307
	RESET SL (R1)	307
Reset PDFF SIG $\cdot$ $\overline{\text{EJFF}}$ $\cdot$ CLK	Reset PDFF	305
$\overline{\text{PDFF}}$ — PDC	ENERGIZE STOP PD SOL	322
$\overline{\text{PDFF}} \cdot \text{WS}$	Reset REVFF	305
$\overline{\text{REVFF}}$ — SD	ENERGIZE RET SOL	322

When the Read Lamp on the keyboard is depressed, it closes normally open contacts of Read Light Switch and EJ KEY signal comes high. EJ KEY signal together with Read Light signal sets EJFF and once EJFF is set, the eject routine starts as follows.

Initial Conditions	Read Light	322
	CC4	
	ERFF	321
	$\overline{\text{RLFF}}$	309
	$\overline{\text{CRG MOTOR FF}}$	304

	$\overline{\text{REVFF}}$	305
Depressing Read Light SW	EJ KEY SIG	
EJ KEY SIG • READ LIGHT • CLK	Set EJFF	320
EJFF • CLK	Set CRG MOTOR FF	304
CRG MOTOR FF — SD	ENERGIZE CRG MOTOR RELAY	
EJFF - - 100ms delay	PDFF	305
PDFF • CRG OPEN • $\overline{\text{TAB}}$ — PDC	ENERGIZE PD SOL	322

The form travels outward until it leaves the pressure rolls and NOT FPS signal comes high.

$\overline{\text{FPS}}$ • CC1 • EJFF • CLK	Set PROG CAM FF	304
PROG CAM FF — SD	ENERGIZE PROG CAM SOL	322

The program camshaft starts turning.

CC2	Reset	307
	Reset SL (R1)	307
CC1 • CC5 • CLK	Reset L-2FF	306
CC5 • $\overline{\text{VFF}}$ • CLK	Reset ERFF	321
$\overline{\text{ERFF}}$	$\overline{\text{Read Light}}$	322
CC2 • CC6 • CLK	Reset EJFF	320
CC2 • CC6 • $\overline{\text{FPS}}$ • CLK	Reset CRG MOTOR FF	304
CC2 • CC6 • $\overline{\text{FPS}}$ • CLK	Set SS FF	305
CC2 • $\overline{\text{EJFF}}$ • CLK	Reset PROG CAMFF	304
SSFF • BOLP	Reset PDFF SIG	305
Reset PDFF SIG • EJFF • CLK	Reset PDFF	305
$\overline{\text{CRG MOTOR FF}}$ — SD	STOP CRG MOTOR	

$\overline{\text{PROG CAM FF}}$	SD	DE-ENERGIZE PROG CAM SOL	322
$\overline{\text{PDFF}}$	PDC	ENERGIZE STOP PD SOL	322

EJFF signal high sets CRG MOTOR FF, triggers the 100ms DMV which when timed out, sets PDFF. As REVFF is reset, the form is driven out of the carriage.

The form travels outward until it leaves the pressure rolls, NOT FPS signal coming high. NOT FPS sets PROG CAM FF and as soon as the program clutch solenoid is energized, the program clutch will trip and the program camshaft turn. At 180° of the program camshaft, CC2 comes high causing a RESET and a RESET SL (R1) pulse.

CC5 at 216° of the program camshaft resets ERFF, L-2FF and the Read Light is turned out. At approximately 320° of the program camshaft, CC2 • CC6 comes high resetting EJFF and CRG MOTOR FF. Also with CC2 • CC6, SSFF is set and NOT EJFF and CC2 resets PROG CAM FF.

As SSFF is set, the next BOLP gives a Reset PDFF SIG causing the NOT EJFF the resetting of PDFF. NOT PDFF energizes STOP PD SOL decoupling the paper drive clutch.

The program camshaft stops at 360° in its clutch detent, the carriage motor stops, the form is out of the carriage tray and the electronic section is ready to start a new read operation.

At the end of a read operation, an error condition may arise by not reading the Line Find pulse. When this happens, the form travels outward until the pressure rolls have no grip on the form any more. NOT FPS signal comes high and gate No. 8 detects this case allowing to set ERFF with the next CLK. Once ERFF is set, the electronic section performs a series of logic steps as follows:

Error Condition • $\overline{\text{EJFF}}$ • CLK		Set ERFF	321
ERFF • $\overline{\text{EJFF}}$ • CC4 • CLK		Set SSFF	305
ERFF • $\overline{\text{LWLFF}}$ • $\overline{\text{VFF}}$	SD	READ LAMP	321
		READ LIGHT	321

SSFF • BOLP——Reset PDFF SIG 305

Reset PDFF SIG • EJFF • CLK——Reset PDFF 305

$\overline{\text{PDFF}}$ —— PDC ——ENERGIZE STOP PD SOL 322

$\overline{\text{PDFF}}$ • CC4 • $\overline{\text{FPS}}$ —— SD —— FS LAMP 321

—— FSL 321

When ERFF is set, the READ LAMP and READ LIGHT signal come high and SSFF is set. With the next BOLP and SSFF set a Reset PDFF SIG is obtained resetting PDFF and stop PD SOL is energized. With NOT PDFF at 144° of the program camshaft and NOT FPS puts FS LAMP and FSL signal high.

The carriage motor continues running and the program camshaft stays at 144°.

Depressing the READ LAMP SW or the FS LAMP SW sets EJFF and a normal eject routine is done as already explained, restoring the electronic section as well as the carriage tray.

Depressing FSL SW——FS SW 313

FS SW • CC4 • FSL • CLK——Set EJFF 320

or

Depressing READ LAMP SW——EJ KEY 513

EJ KEY • READ LIGHT • CLK——Set EJFF 320

With EJFF set at 144° of program camshaft, a normal eject routine is performed.

ERROR CONDITIONS DURING WRITE

The E2150 has, for the write on stripe operation, several error detection gates which can come high under certain conditions during write and set ERFF. This is to assure that the information recorded on the magnetic stripes is as required for a subsequent read of a form.

During the write operation, it is checked if there was a failure to write data or complement pulses, if information was written on the stripe when it was not supposed to be written, if the carriage motor speed is in the range for the proper packing density of pulses on a stripe and if the end of message check is correct.

An error by failing to write data or complements pulses, would be detected by gate No. 1 for the X stripe and gate No. 3 for the Y stripe. The inputs at gate No. 3 (Y stripe) require for an error condition a WRITE Y PULSE and FF3Y set. WRITE Y PULSE is obtained with each complement pulse or each time a data pulse is written. FF3Y is reset by WMY pulse. The write monitor circuit sends out a WMY pulse each time a current reversal takes place in the corresponding magnetic head. WMY is emitted only if the inductance of the magnetic head is the correct one (number of active turns) and the current through the head winding was strong enough to saturate the stripe. At the end (trailing edge) of the WMY pulse, which has a length of around 16.5 usec. FF3Y is reset. If due to no current reversal or a faulty situation in the head, no WMY pulse is emitted and FF3Y stays set. When the next pulse is going to be written, WRITE Y PULSE comes high for 12 usec. as well as gate No. 3 and with CLK, ERFF is set. A similar procedure is followed by gate No. 1 for the X stripe.

Gate No. 2 (X stripe) and gate No. 5 (Y stripe) detects if data pulses are written by the magnetic heads on the X or Y stripes respectively, when there was no indication from the logic to do so. This means that there is a current reversal in the winding of the Y head for example, and a WMY pulse emitted from the write monitor circuit with no WRITE Y PULSE present. WRITE Y PULSE, which is controlled by logic, sets at its trailing edge FF3Y. A situation as just mentioned could be caused by reversing the state of FF9Y due to noise on its input gates, a breakdown in components on the input gating or wrong input signals due to machine malfunction.

The result would be a reversal in the head current, writing a pulse on the stripe, without indication from the logic. Gate No. 5 gets high with NOT FF3Y and WMY and with CLK sets ERFF.

The packing density of the pulses written on the magnetic stripes will depend on the velocity with which the form passes under the magnetic head and the US MVFF frequency, which is fixed. Therefore, the packing density basically depends on the carriage motor speed. The motor speed is adjustable and is checked for the proper R.P.M. by counting the USMVFF pulses between the BOLP. The counting operation has been explained in the write paper handling logic and it should be referred to at this point.

Gate No. 4 detects when the speed of the carriage motor is too slow or too fast. In both cases, the counter FF are not reset when they have been counted up to 27, 28 ~~or~~ 29, 30 or 31. This puts gate No. 4 high because the counter FF will step up to 32, setting with CLK the ERFF.

The end of message check, gate No. 15 tests if the counter FF (SRCX) were stepped up correctly when all the information has been written on the form. The SRCX are stepped up during write with the DP. After the last digit of the last word has been written on the stripes, the write ledger logic goes into a routine for writing the read start message. The read start message as can be recalled, consists of a data pulse ~~between two~~ AND complement pulses. As the SRCX counter resets to 0 after the last DP in DDO of the last digit, it is stepped up to one with the read start data pulse. When the form stops interrupting the beam of light at the front paper switch, signal $\overline{FPS}$ comes high. Gate No. 18 checks with the $\overline{FPS}$ high on the write operation if the SRCX counter fulfill the required condition of having been counted up to one by this time. Not to fulfill this condition at the end of a write operation is caused when the write ledger logic gets out of step.

SRCX not counted up to one makes gate No. 15 high which together with CC6 and NOT FPS put gate No. 18 high. This in turn together with CLK sets ERFF.

Error Condition • $\overline{\text{EJFF}}$ • CLK	Set ERFF	321
ERFF • CLK	Reset WLFF	310
$\overline{\text{WLFF}}$	Stops the write ledger logic, no further information is written on the stripes but the form continues traveling outward. When the form does not interrupt the beam of light any more, $\overline{\text{FPS}}$ comes high.	
$\overline{\text{FPS}}$ • CC6 • L-2FF • CC1 CLK	Set PROG CAM FF	304
PROG CAM FF — SD	ENERGIZE PROG CAM SOL	322

The program camshaft cycles

CC2	RESET	307
	RESET SL (R1)	307
CC2 • $\overline{\text{EJFF}}$ • CLK	Reset PROG CAM FF	304
CC2 • CC6 • $\overline{\text{FPS}}$ • CLK	Reset CRG MOTOR FF	304
CC2 • CC6 • $\overline{\text{FPS}}$ • CLK	Set SSFF	305
$\overline{\text{CRG MOTOR FF}}$ — SD	STOP CRG MOTOR	
SSFF • BOLP	Reset PDFF SIG	305
Reset PDFF SIG • $\overline{\text{EJFF}}$ • CLK	Reset PDFF	305
$\overline{\text{PDFF}}$ — PDC	ENERGIZE STOP PD SOL	322
CC1 • CC3 • CLK	Reset L-2FF	306
CC1 • CC3 • CLK	Reset PWFF	310
LWL FF — SD	WRT LAMP	322

LWL FF remains set, the program camshaft is in its detent position at 0°, ERFF is set and the WRT LAMP is on. This indicates that one of the previously mentioned error possibilities during a write operation has occurred and the operator seeing the WRT LAMP on, moves the carriage into the WC (write correction) position and writes again the information on the form.

The WC position is essentially a BC position which is also programmed for NOT ALIGN. The NOT ALIGN signal prevents the LF write amplifier coming on to erase the line find pulse. The form is aligned at the first printing line, the console is cycled with the hammer block active and the carriage moves to a write ledger position for another write ledger operation.

When a paper handler write logic is started and a malfunction occurs in such a way that PDFF and REVFF are not reset, the form is not reversed in its travel and would come out of the back part of the carriage tray. This situation could be caused for example; by not reading the sync pulse on the X stripe during a write operation. As the form continues moving inward NOT FPS signal comes high, CC6 is high, the counter FF (SRCX) are reset and gate No. 15 and 18 set ERFF with the next CLK. Due to this, WRT LAMP is lit, PDFF and REVFF remain set, the carriage motor continues turning and the program camshaft is at 288°. As L-2FF is still reset at this point PROG CAMFF cannot be set when NOT FPS comes high and cycle the program camshaft.

Depressing the WRT LAMP puts high WRT L SW signal. WRT L SW • LWL FF • CC6 • CLK set EJFF which in turn is going to start the eject routine at 288°.

LWLFF • ERFF —— SD ——	WRT LAMP	321
Depressing WRT LAMP SW ——	WRT L SW signal	513
WRT L SW • LWLFF • CC6•CLK ——	Set EJFF	320
EJFF • $\overline{\text{FPS}}$ • CC1 • CLK ——	Set PROG CAM FF	304
PROG CAM FF —— SD ——	PROG CAM SOL.	322

CC2		RESET	307
		RESET SL	307
CC2 • CC6 • CLK		Reset EJECT FF	320
CC2 • CC6 • $\overline{\text{FPS}}$ • CLK		Reset CRG MOTOR FF	304
CC2 • CC6 • $\overline{\text{FPS}}$ • CLK		Set SSFF	305
CC2 • $\overline{\text{EJFF}}$ • CLK		Reset PROG CAM FF	304
$\overline{\text{CRG MOTOR FF}}$	SD	STOP CRG MOTOR	
SSFF • BOLP		Reset PDFF SIG	305
Reset PDFF SIG • $\overline{\text{EJFF}}$ • CLK		Reset PDFF	305
$\overline{\text{PDFF}}$	PDC	STOP PD SOL	322
$\overline{\text{PDFF}}$ • WS • CLK		Reset REVFF	305
LWLFF • ERFF	SD	WRT LAMP	321

With EJFF set the PROG CAM FF is set and the program camshaft clutch tripped causing the program camshaft to turn. At approximately 320° of the program camshaft, CC2 and CC6 come high resetting EJFF, CRG MOTOR FF and SSFF. NOT EJFF and CC2 resets PROG CAM FF.

As SSFF is set, the next BOLP gives a Reset PDFF SIG causing with NOT EJFF the reseting of PDFF. NOT PDFF energizes STOP PD SOL decoupling the paper drive clutch and NOT PDFF•WS and CLK reset REVFF.

The program camshaft stops at 360° in its clutch detent and the carriage motor stops turning. As LWLFF and ERFF remain set the WRT LAMP is on. The operator has to take the carriage into a WC (write correction position) and attempt to write again the information on the form.

TYPE TO AND FROM MEMORY FEATURE - USING UPPER AND LOWER CASE KEYS

The Type To Memory portion of this feature allows alphanumeric data entered into the typewriter keyboard to be stored in memory. The Type From Memory portion allows the typewriter to be operated from data stored in memory. When this feature is incorporated in the striped ledger machine, alphanumeric data, stored in memory, can be read from and written onto the stripes. The main application of Type To and From Memory will be in conjunction with striped ledger, however, the feature is independent and the striped ledger will not be discussed further here. The Type To Memory portion of the feature will be covered first.

TYPEWRITER CODING

The Typewriter incorporates seven coding slides to provide the vertical and lateral limits for the type box. An eighth (Shift slide-SH) to indicate upper or lower case type and as an end of message control when the TAB or RET keys are used. As the typewriter camshaft cycles, various combinations of the coding slides are allowed to move rearward depending upon which key on the keyboard has been depressed. The two positions of the coding slide, normal and rearward, provide a binary condition which can be designated as 0 and 1. The normal position is the 0 condition and the rearward or indexed position is the 1 condition. The type arrangement and coding charts are shown in the flow chart section of the prints. Slides 1, 2 and 3 position the type box in its horizontal row while slides 4, 5 and 6 position the box in its vertical row. Slide 7 is used to indicate that a typewriter tab, return or space key has been used. Slide SH is controlled by the shift key and indicates that the shift key has been depressed. The RET 3 key is the normal carriage return key used when typing into memory and does not signify an end of alphanumeric condition to the logic. The RET 1, RET 2, and TAB 4 keys normally signify an end of alphanumeric to the logic, however, these keys may be used without ending alphanumeric, if the SHIFT key is held down while they are depressed. The end of alphanumeric code consists of slides 3 and 7. When the shift key is depressed, slide 3 signal is gated out and only the 7 slide of the end alpha code is written.

One of the Vertical columns of the type box can be selected by encoding two slide combinations in memory (slide 5 or slide 5 and 6). Two of the lateral rows of the type box can be selected by encoding two slide combinations (slide 1 or slides 1 and 3) (slide 2 or slides 2 and 3).

ELECTRICAL SIGNALS

The position of each of the eight slides is converted into electrical signals by reed contact magnetic switches, which are actuated when the slides move rearward see Fig. VI-1. Each slide is equipped with a thin strip of metal or "flag" which is interposed between the reed switch and its magnet, when the slide is at normal. In this position, the flag acts as a shield to prevent the magnetic field reaching the switch. When the slides are indexed, the flags are removed from the shielding position between the magnet and switch and the magnetic field causes the switch contacts to transfer.

Each switch is wired to a relay wetter circuit, which provides a -4V or low signal, when the slides are normal and a ground or high signal when the slides are indexed. The low and high signals represent zeros and ones to the electronic logic. On each typewriter cycle, eight bits of binary information are provided for the electronic section logic.

DATA STORAGE IN MEMORY

The memory consists of a four bit digit, therefore, more than one digit position is required for storage of a eight bit typewriter character. The bits from slides 4, 5, 6 and SH are stored in an even tens digit memory location (20-29, 40-49, 60-69, etc.). These bits are referred to as the numeral or N bits. The bits from slides 1, 2, 3 and 7 are stored in an odd tens digit memory location (30-39, 50-59, 70-79, etc.).

These bits are referred to as the zone or Z bits. The Z bits of a character are always stored in a memory location which is ten higher than that where the N bits are stored. This permits the selection of the N and Z bit memory locations by setting and resetting the MART1FF. For example, if the N bits of a character are stored in DD3 of memory location 21, the Z bits will be stored in DD3 of memory location 31.

TEMPORARY STORAGE

Since eight bits are to be gated into the electronic section simultaneously, additional temporary storage and working elements were necessary. Four flip flops similar to the WR were added. These flip flops are known as the SRX1FF, SRX2FF, SRX4FF and SRX8FF. In addition, to use as a storage and working register on the Type To and From Memory feature, these flip flops are used as a Shift Register (data is read in serial form) on other features. The X is an identification from other shift registers used with the striped ledger.

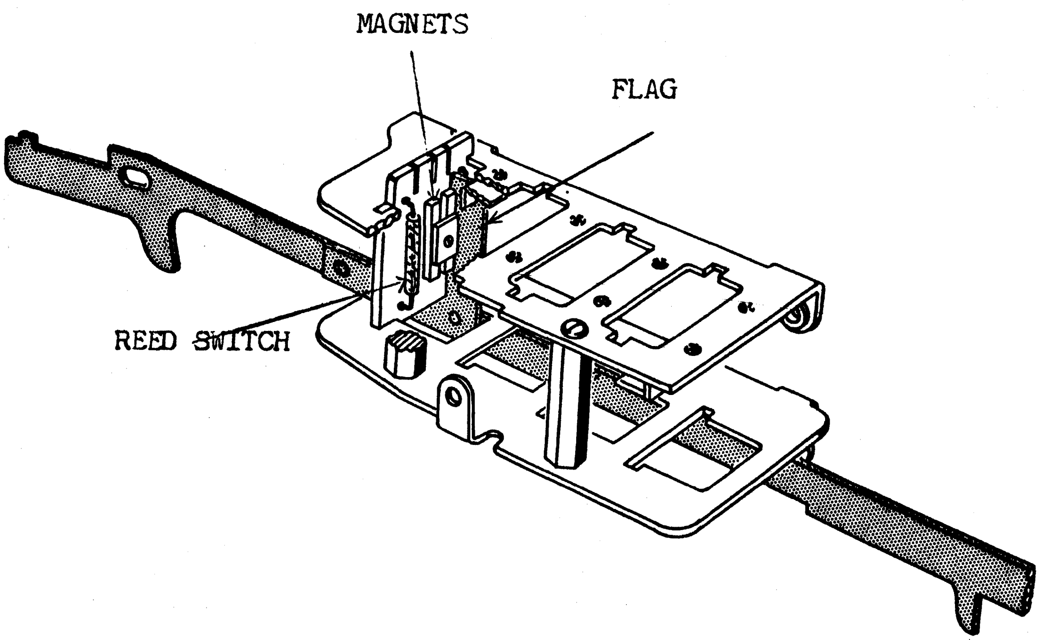


Figure VI-1

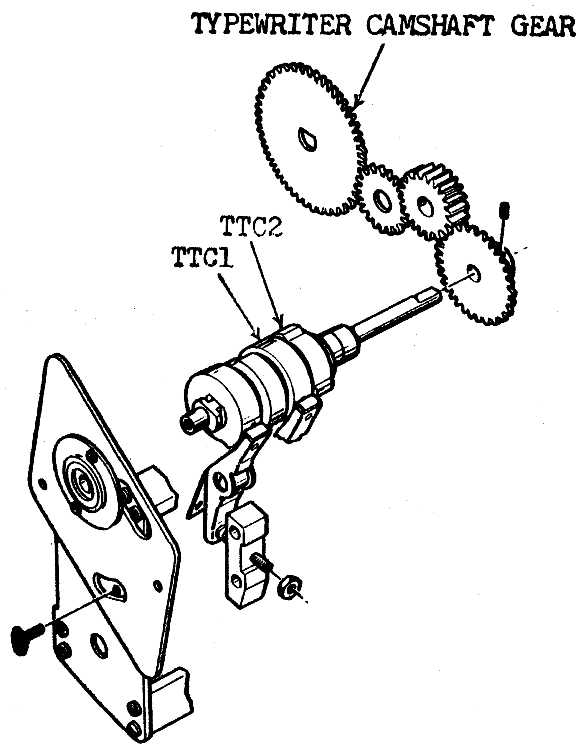


Figure VI-2

When the eight bits are gated to the electronic section, bits from slides 4, 5, 6 and SH (N bits) are gated into the WR and bits from slides 1, 2, 3 and 7 (Z bits) are gated to the SRX.

WRITING DATA INTO MEMORY

Alphanumeric data storage in memory must start in an even tens digit memory location for the N bits and the next higher (odd) tens digit for the Z bits. Data is stored from the MSD digit downward to DD1. Data is not stored in the DDO position. After twelve characters (1 word) are stored, the next higher memory location is selected and storage again starts in the MSD. When 120 characters (ten words of memory) have been stored, another even tens digit Memory location must be selected. If less than 120 characters are to be stored, the Memory locations beyond the last alphanumeric storage can be used for regular keyboard entries. For example, if a maximum of 60 characters are to be stored and the storage is to start in memory locations 40 and 50, the alphanumeric characters will not extend beyond memory locations 44 and 54. In this case, memory locations 45 thru 49 and 55 thru 59 could be used for regular storage of data.

ADVANCING MEMORY ADDRESS

To provide a means of selecting and advancing the units of memory address while typing to memory, four flip flops have been added. These are the Memory Address Register Units (MARU) flip flops MARU1, MARU2, MARU4 and MARU8. These FF's are used as a register or storage location for the units of memory address. the MAU1, MAU2, MAU4 and MAU8 data from the wetter encoder is gated to the set input of the respective FF by the ΔMR. An inversion of the data is also fed into the reset side of the flip flops. The $\triangle$MR signal also makes a third leg of the MARU's high so that the MARU's can be set by the clock.

The output of the MARU's is gated into the adder during each sequence Z of the TIM or TOM operation. the CiFF is set by the Not DDO signal soon after the start of the operation. The output of the adder will then be equal to the MARU's plus 1, The adder output is gated to the MARU input by the SZ and DDO signals which will also make the third leg of each MARU set and reset gate high so that the MARU's can be set equal to the adder by a clock pulse. the MARU1 and MARU8 signals are gated together to produce the MARU=9 signal when both are high.

The $\triangle$MR signal causes the MARUFF's to be set by the MAU signal at the start of each console cycle and the SZ, DDO and CiFF signals cause the MARU digit to be increased by one.

The MARU signals are used in the selection of a memory address in much the same manner as the MART signals are used in the arithmetic logic.

The MART4, MART8 and MARH1FF's have been added to enable selecting a memory address up to 199.

PROGRAMMING REQUIRED FOR TYPING TO MEMORY

The Type To Memory (TTM) lane 45D must be programmed in the last printer position before typing to memory is to begin. This lane provides the signal for setting the Type Into Memory (TIM) flip flop, which is equivalent to a T time flip flop in the arithmetic logic.

TYPEWRITER TIMING CAMS

The Typewriter Timing Cam 1 (TTC1) see Fig VI-2 which is closed from

COUNTING MARUS WITH ADDER AND CIFF

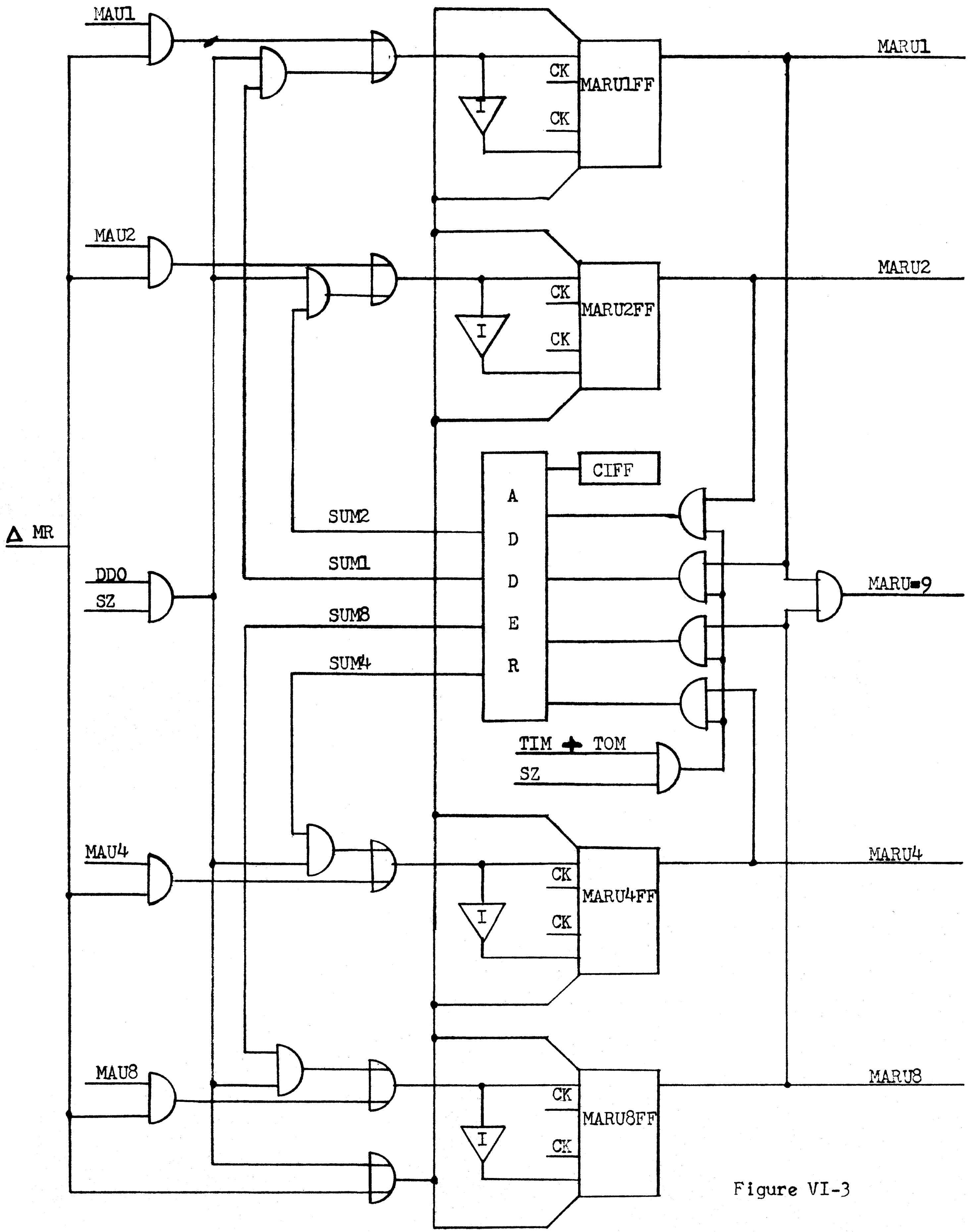


Figure VI-3

50° to 70° of the typewriter camshaft cycle, provides the signal to the logic to cause the slide position information to be written into the memory, by setting the TTCFF. The TTCFF·CLK signal sets the Bounce Eater (BEFF). TTC1 is an ignition type switch which is mounted at the lower center of the left auxiliary sideframe and is driven from the typewriter camshaft through a gear arrangement. TTC2 is mounted adjacent to TTC1 and is made from 200° to 300° of the camshaft cycle. TTC2 resets the flip flops which were set by TTC1 and resets the Type Into Memory (TIMFF) at the end of the operation.

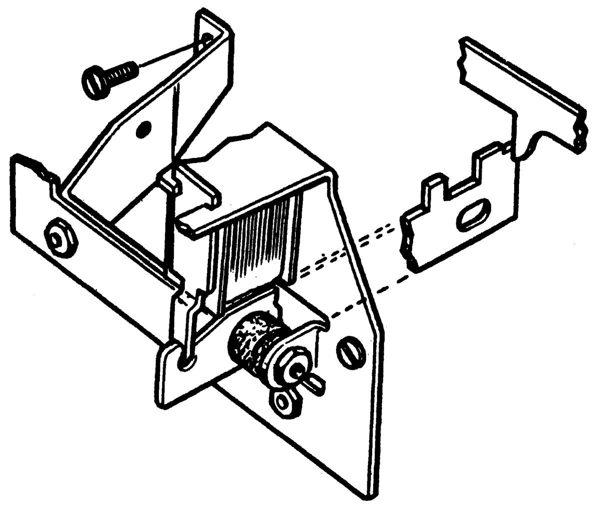
SLIDE LIMIT SOLENOIDS

Eight solenoids see Fig. VI-4. mounted on the auxiliary left sideframe near the machine trip solenoid, provide limits for the slides during the TFM operation. The solenoid for the SH slide is energized by the shift key and is used during the Type To Memory operation. Solenoids 1 thru 7 must be energized to block coding slides 1 thru 7. Solenoid 8 must be energized to release the SH slide.

TYPE TO MEMORY BLOCK DIAGRAM

In the block diagram, Fig. VI-5. the typewriter keyboard is shown with four outputs. One is to position the type box. This is the normal mechanical function and is very similar to the standard typewriter. The second output is shown feeding the card to tape punch encoder from keyboard switches. These switches are the normal outputs for the P and PA series of machines and are shown here to indicate compatability.

The third and fourth, the prime outputs for this discussion, are the coding slide switches. The information from these switches is gated into the SRX and WR during the TTM logic.



For Form VI-4

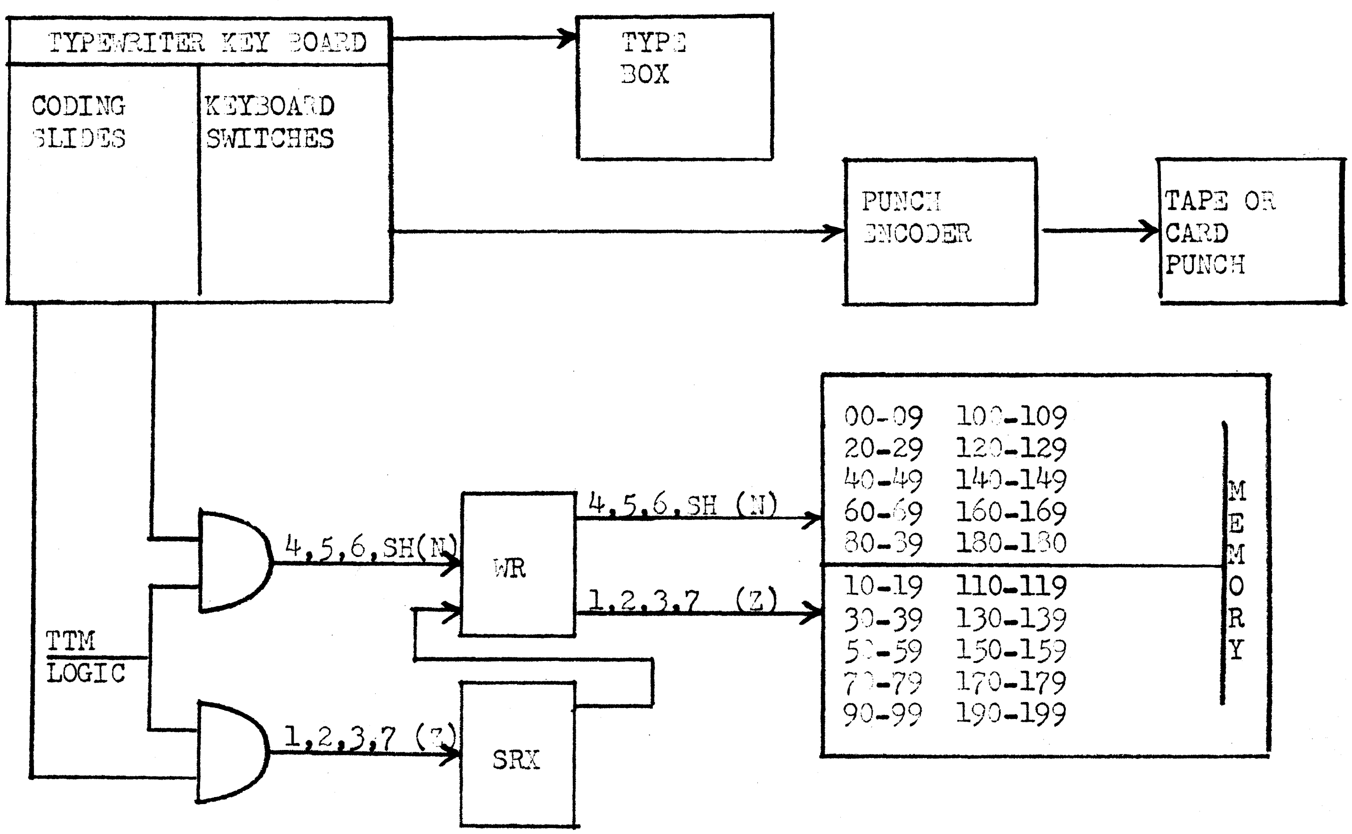


Figure VI-5

The data in the WR (N) is then written into the selected memory location. The data (Z) in the SRX is transferred to the WR, the MART FF's are counted and the Z bits are then written into the higher memory location.

TYPE TO MEMORY CONTROL CIRCUITS

When the printer cycles in the last stop position, before Type To Memory begins, the TTM lane switch and its RW will cause the Type Into Memory (TIM) flip flop to be set at the end of T6, see Fig. VI-7. The TIMFF provides logic signals to allow writing into memory and provides a signal to pick the KYBD Lock Solenoid if a lock condition has occurred on the initiating cycle. The KYBD Lock Solenoid locks the typewriter keyboard. The TIMFF remains set until one of three conditions is met. 1. If an Invalid Memory Address has been selected, the MAFF signal would cause the LOCK signal to be high and pick the KYBD•LOCK SOL. TIMFF will be reset by the MAFF Reset signal. 2. When the SRX8 and SRX1 signals (from slides 7 and 3) are high simultaneously an end of message is indicated. the SRX8•SRX1•TTC2 signals reset the TIMFF after the last character is written into memory.
3. When DDO and MARU=9 signals are high simultaneously, the group of memory addresses selected at the start of the type to memory operation have been filled. The DDO•MARU=9•TTC2 signals reset the TIMFF to halt the type to memory operation. If more typing to memory is desired, another printer cycle must be made to select a new group of memory locations and re-initiate the type to memory operation.

The signal which triggers the electronic section into operation to receive and write data from the typewriter keyboard to memory is the TTC1 switch, see Figure VI-2.

As with any switch, a certain amount of electrical noise is generated by contact bounce. The phase flip flop (PHFF), Typewriter Timing Cam flip flop (TTCFF) and Bounce Eater flip flop (BEFF) minimize this noise and synchronize the TTC1 and TTC2 signals with clock. PHFF is a complementing FF and produces 12 us pulses, PH1 and PH2, these pulses are 180 out of phase. PH1 is wired to the set and reset side of TTCFF. PH2 is wired directly to the reset side of BEFF and through an AND Gate to the set side of BEFF. If a high frequency noise pulse appears from TTC1 or if TTC1 makes during the latter part of a clock pulse which PH1 is high, a short pulse will appear at the set side of the TTCFF. This pulse may do one of two things (a) Set TTC or (b) Appear at TTCFF output without setting TTC. If TTC is set, its output with PH2·TIM+TOM·CLK will set BEFF. If the short pulse did not set TTCFF but appeared at its output, PH2 inhibits the gate and BEFF cannot be set. BEFF can never be set unless TTCFF has been set. BEFF controls the sequences for reading data from or writing data into memory.

END OF MESSAGE AND CARRIAGE MOVEMENT CODES

The End of Message code is a nine in the odd tens memory decade. This appears as a SRX1·SRX8 during type to memory and as an MR1·MR8 during type out of memory. This code is normally entered by the 3 and 7 coding slides when the RET 1, RET 2 or TAB 4 keys are used. RET 3 does not allow slide 3 to be indexed and does not produce the end of message code. If the shift key is held depressed while RET 1, RET 2, or TAB 4 are used, the SRX1FF is not set and the end of message code is not produced. When the shift key is indexed, a circuit to pick the Shift slide solenoid (L858) is energized, see Figure 7.

The shift slide solenoid positions the blocking slide so that the Shift coding slide (SH) is indexed during the operation. The signals from the 7 and SH coding slide switches are gated together with an AND gate and inverted to produce the NOT SH SL•NOT SL7 signal. If this signal is low, slide 3 cannot set SRX1 and the end of message code is not encoded. The SRX8 code alone causes the typewriter carriage skip or return mechanisms to become active. The typewriter lane of control during the skip or return is encoded in the even tens decade of memory by slides 4, 5 and 6. Decoding for lane of control will be covered in Type From Memory.

If the operator does not properly index the space bar, incorrect coding may result. The incorrect codes which can be produced in this way, are gated by an OR gate and the output is inverted. This signal, when high, inhibits setting the SRX1, 2 and 4 and WR 1, 2 and 4 FFs. Slide 7 is encoded which produces a space instead of wrong carriage skip or return.

TYPE UPPER CASE CHARACTERS

Upper case characters may be encoded in memory by depressing the shift key with the desired character. The SH slide solenoid is picked and the SH slide is allowed to index. The SH slide will cause switch S858 to transfer which sets WR8FF and encodes an 8, in addition to the normal character codes, in the odd tens decade of memory. The SH slide also mechanically positions the type box to the left to print the upper case characters.

TYPE TO MEMORY DATA FLOW CHART - Initial Conditions, see Prints

The initial conditions are those at the end of the initiating printer cycle.

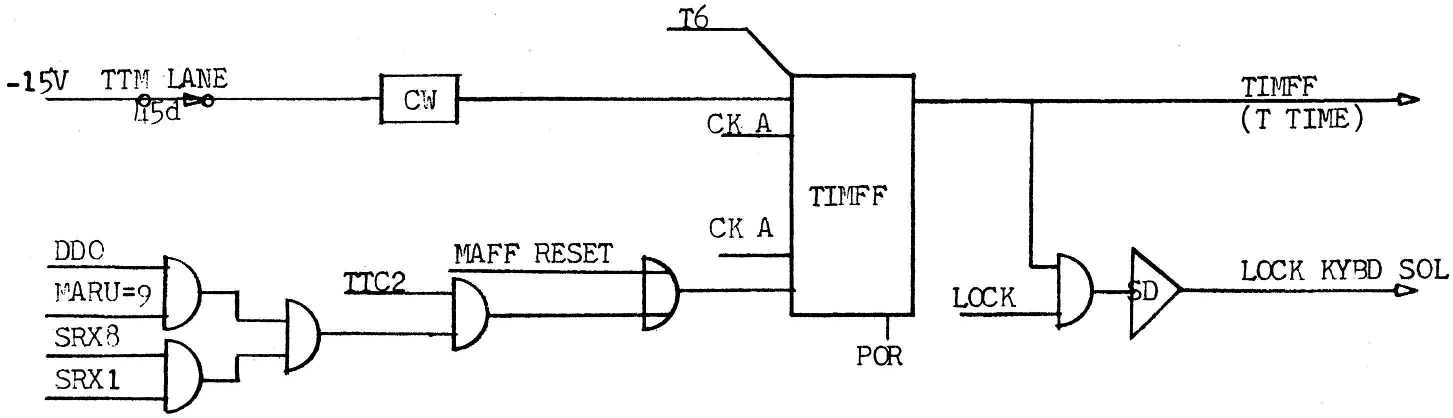


Figure VI-6

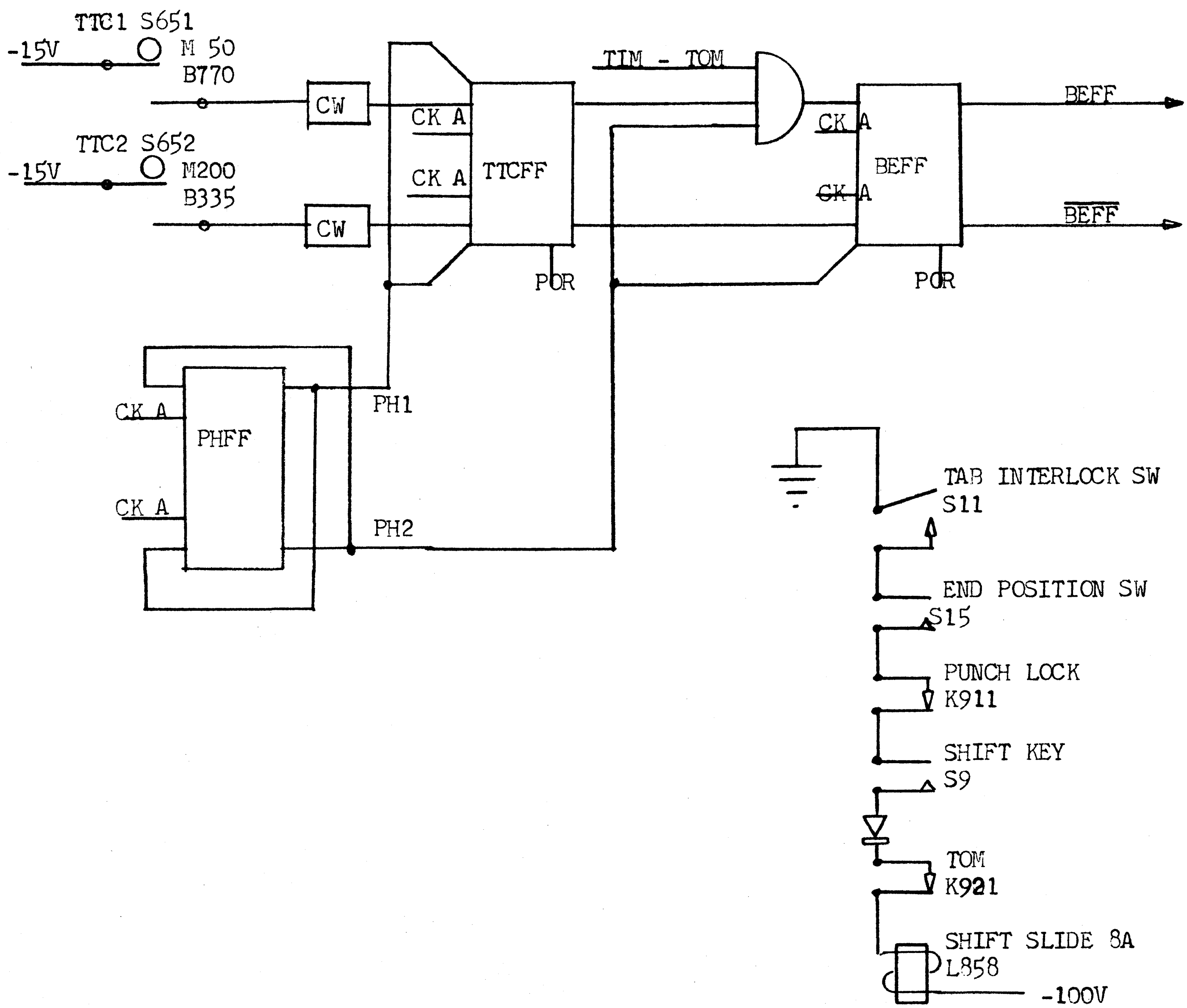


Figure VI-7

(DDO) The DDO FF is set at the end of each printer cycle.

(CiFF) The CiFF is reset at the end of each printer cycle.

(COMPFF) The COMPFF is reset at the end of each printer cycle.

(CAD) The Memory address where alphanumeric storage is to start is set in the MART and MARU flip flops on the initiating printer cycle.

(TIMFF) The TTM lane switch and RW causes the TIMFF to be set. The TIMFF is equivalent to a T time in the arithmetic operation.

(PICK LOCK REL) The TIMFF Picks the lock relay to prevent starting a printer cycle during the type to memory operation.

(PICK KYBD LOCK SOL) When the TIMFF and LOCK signals are high, the KYBD LOCK SOL picks to lock the typewriter keyboard. The Lock signal will be high when a lock condition such as Invalid Address or ECNC occurs.

(TTCFF) TTCFF is set by TTC1·PH1·CK at 50° of the TYPEWRITER CYCLE.

(BEFF) The BEFF is set by TTC·PH2·CK when TIMFF is set. BEFF sets the electronic sequence W by the trailing edge of the NOT BEFF signal. Now the logic for writing a character into memory has started.

The Sequences used for the Type To and From Memory feature are controlled by flip flops the same as on the arithmetic operations.

MEMORY ADDRESS

When the memory address is designated as CAD, PAD, AAD, BAD or DAD, on the flow charts, the address is selected by a combined output from three flip flops see Figure 8. These are the Special Address 1, 2 and 3 flip flops (SA1, SA2 and SA3). The SA1 and SA2 signals are taken from the reset output of the flip flops while the SA3 signal is taken from the set output of its flip flop. The flip flops are reset by the POR signal when the machine is turned on. The SA1 and SA2 signals will then be high and are gated together to produce the CAD signal. The not Cad signal is the CAD signal through an inverter.

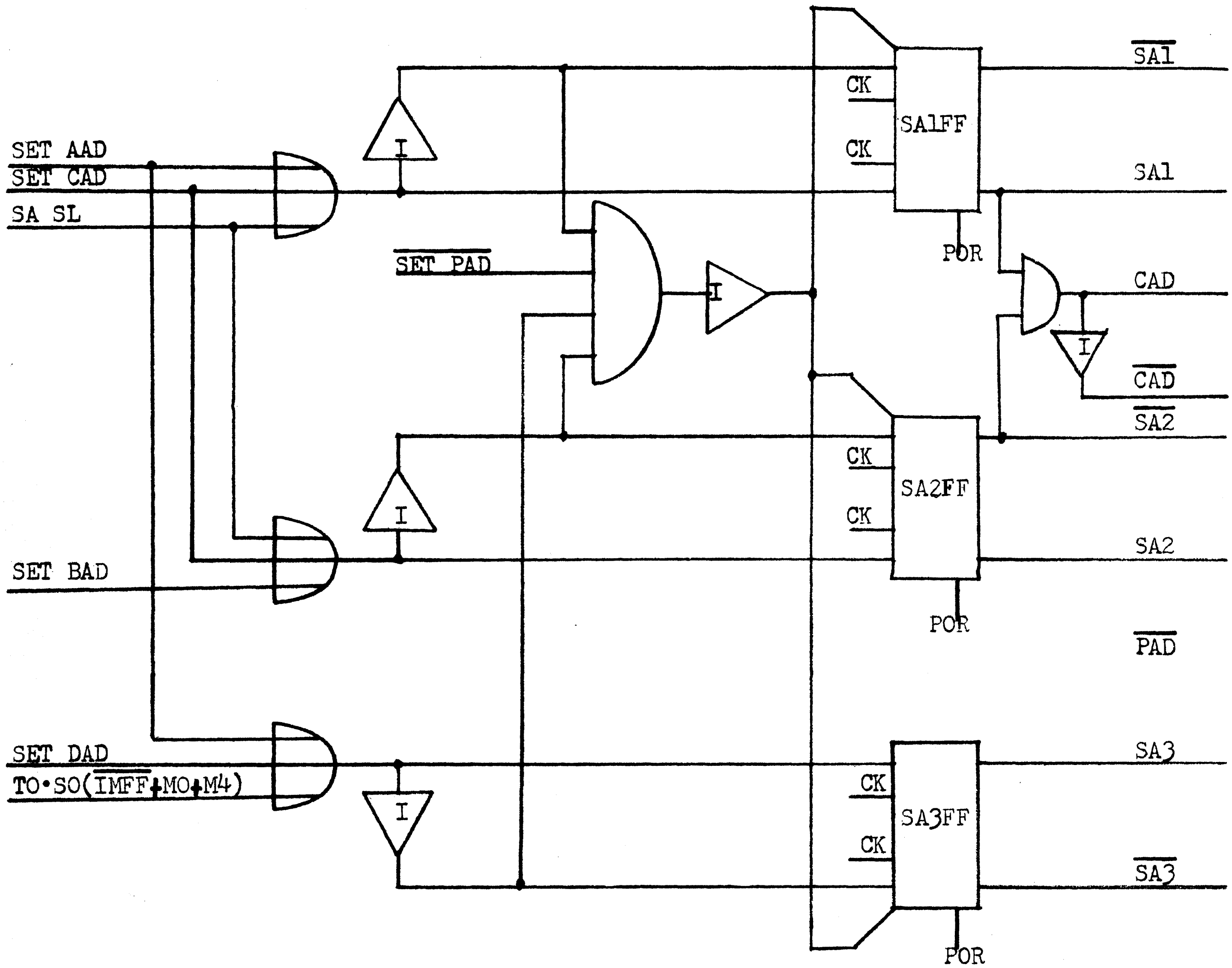
The following chart shows the conditions necessary to select a special address, see Fig. VI-8

The ones and zeros of the chart refer to the high or low condition of the signals SA1, SA2 and SA3 and do not represent a set or reset condition of the flip flops, or refer to the one or zero output. For example, to select B, the SA1 and SA3 signals must be low and the SA2 signal must be high. These conditions will exist when SA1FF is set, SA2FF is reset and SA3FF is reset. Whenever a special address signal (SET PAD etc.) is made high by the logic, all three flip flops are set or reset as needed to select the desired address. Assume that CAD was the last address selected (all three flip flops are reset and SA1 and SA2 are high with SA3 low) and the signal set DAD is made high by the logic. The high DAD signal will allow the SA3FF to be set by a clock pulse. The inverted DAD signal makes the reset of SA3FF low and also makes the four legged AND gate output low. The AND gate signal is inverted to make a high signal which is wired to the reset gate of SA3FF and the set gate of the SA1FF and SA2FF. Since the inverted output feeding the SA1FF and SA2FF is high, they will both be set by a clock pulse. Each of the flip flops has been changed to agree with the chart. In a similar manner, any special address signal will control all three flip flops.

For identification purposes, the sequences of type to and from memory are designated as W, X, Y and Z.

From 6° to 19° of the typewriter camshaft cycle, the coding slides are positioned to correspond to the code for the key depressed on the keyboard. The TIMFF is set and BEFF is reset. At 50° of the cycle, the TTC1·PH1·CK

SPECIAL ADDRESS FF's



MEMORY ADDRESS	A	D(K)	C	P(O)	B
HI or LOW STATE OF SA1 SIG.	1	0	1	0	0
HI or LOW STATE OF SA2 SIG.	0	0	1	0	1
HI or LOW STATE OF SA3 SIG.	1	1	0	0	0

Figure VI-8

signal sets the TTCFF. TTCFF·CLK·PH2·TIM sets BEFF. As the not BEFF signal goes low, the negative swing of the not BEFF and TIM signals sets Sequence W flip flop (SW).

Assume now that JOHN DOE and Social Security number 333 22 0000 is to be typed on two lines and written into CAD 20.

SW DDO of the pinned CAD (20)

READ No Read takes place since not DDO is low. The sign positions are not used hence no Read or Write in DDO is performed on this feature.

GT SLIDES 4, 5, 6, SH→ WR The GATE SLIDES (GTS) signal allows slides 4, 5 and 6 to be gated to the WR. The SH slide is always entered into WR8 when the shift key has been used to energize the shift solenoid. If the operator does not fully index the space bar, it is possible for various slides to be released in addition to slide 7. To prevent these faulty codes being written into memory, slide 7 and these codes are inverted to make up the GTS signal. When GTS is low, only slide 7 or 7 and SH can be gated to the WR and SRXFFs. For the letter J, a 1 bit is gated to the WR (see code chart).

GT SLIDES 1, 2, 3, 7→SRX The J will cause a 1 bit to be gated to the SRX. NOT SL7·NOT SHIFT SLIDE will be high since neither the space bar nor RET 1, 2, 3 or TAB 4 were used.

SET WR→MEM When TIM is set, data is written from the WR into Memory.

SET DDREV The DDREV FF is set so that writing to memory starts in the MSD of the CAD (20).

SX - DDO of 20

WRITE No Write takes place in the sign position. Not DDO is low.

SET MART 1 MART 1 is set to select the next higher tens CAD (30).

GT SRX—>WR TIM causes the data in the SRX to be transferred to the WR. Data in the SRX cannot be written directly into memory.

SY - DDO of 30

READ No Read takes place in DDO.

SET CiFF The CiFF is not set in DDO.

0—>MR The MR is set to zero so that the MARU can be advanced by the Adder in SZ.

0—>WR The WR is set to zero so that the MARU can be advanced by the Adder to SZ.

SZ DDO of 30

WRITE No Write takes place in DDO.

RESET MART 1 MART 1FF is reset to return the CAD to 20.

STEP DD The DD is stepped to DD1.

GT MARU—>ADDER SZ gates the MARU to the adder so that the memory address may be advanced by one, after a word has been filled. Since nothing has been written and CiFF is not set, the memory address is not advanced at this time.

GT ADDER—>MARU DDO causes the MARU flip flops to be set equal to the adder.

SET SW TIM and DDO returns the logic to SW.

Basically, the only thing accomplished in the above sequences is the stepping of the DD.

SW - DD1 of 20

READ DDMSD (DD1 is high with DDREVFF set) is read to clear any data from a previous operation.

GT SLIDES 4, 5, 6, SH→WR A 1 is again gated to the WR.

GT SLIDES 1, 2, 3, 7→ SRX A 1 is again gated to the SRX.

SET WR→ MEM The WR to Memory is already set.

SET DDREV The DDREVFF is already set.

SX - DD1 of 20

WRITE A 1 is written into MSD of CAD 20.

SET MART 1 MART 1 is set to select CAD 30.

GT SRX→WR The data in the SRX (1) is transferred to the WR so that it can be written into memory in SZ.

SY - DD1 of 30

READ MSD of CAD 30 is read to clear the location.

SET CiFF The CiFF is set by not DDO.

The CiFF will not be used until the DD has stepped to DD0 again. At the completion of the first word, the CiFF will be an input to the adder to advance the MARU and select CAD 21.

SZ - DD1 of 30

WRITE The data from the WR is written into the MSD of CAD 30.

RESET MART 1 MART 1 is reset to return the CAD 20.

STEP DD The DD is stepped to DD2.

One character (j) has been written into memory. No sequence is set and the logic waits for TTC2 to make at 200° of the typewriter camshaft cycle. At 200°, TTC2 makes and provides a signal with PH1·CK to reset the TTCFF. The TTCFF·PH2·CK resets the BEFF. The logic now waits for 50° of the next typewriter cycle.

When the operator depresses the next key (a 0 in the example), the slides will be positioned according to the code chart by 19° of the camshaft. At 50°, TTC1·PH1·CK again sets the TTCFF which enables PH2·CK to set the BEFF. The negative swing of the not BEFF signal sets SW and the code for 0 is written into the memory during SX and SZ in the same manner as the J was written. Assume now that the operator has typed JOHN DOE and depresses the RET 3 key so that the social security number can be printed under the name.

When the operator depresses the RET 3 key, the code slides are positioned during the cycle as shown in the code chart to the right of RET 3 and not shift. Note that an 8 bit is written into the odd tens CAD (30). This bit denotes carriage movement when read on the Type From Memory operation.

Typing of the social security number continues and after twelve characters have been written into CAD's 20 and 30, the logic will count the MARU so that writing will continue in the MSD of 21 and 31. This occurs in SY and SZ when DDO is high.

<u>SY - DDO of 30</u>

<u>READ</u>	No read occurs in DDO.
<u>SET CiFF</u>	The CiFF was set in the first DD1 and has never been reset.
<u>0→MR</u>	The MR is cleared to prevent interference with counting the MARU.
<u>0→WR</u>	The WR is cleared to prevent interference with counting the MARU.

<u>SZ - DDO of 30</u>

<u>WRITE</u>	No write occurs in DDO.
<u>RESET MART 1</u>	MART 1 is reset to select CAD 20.
<u>STEP DD</u>	The DD is stepped to DD1.

GT MARU—▷ADDER The MARU (0) becomes an input to the adder. CiFF (1) is also an input to the adder.

GT ADDER—▷MARU The MARU is set equal to the adder (1).

The TIM and DDO signals set the SW FF where the writing of data continues in CAD 21 and 31.

Typing could continue until the MARU has been counted to 9 and the DD has been stepped to DDO. If this condition occurs, the TTC2, DDO and MARU=9 signals will all be high. When the TTC2 closes at 200°, DDO·MARU=9·TTC2·CK will reset TlMFF and halt the Type To Memory operation. In the example used here, the MARU=9 will not be reached before the Social Security number is finished. When the operator types the last digit of the number, a carriage tab or return key must be used. Assume the TAB 4 key is used. Setting the BEFF gates the slide data to the WR and SRX. The SRX8 and SRX1 are set by slides 7 and 3 respectively. This is the end of message code and will allow TTC2·SRX1·SRX8·CK to reset the TIMFF to end the Type To Memory operation.

TYPE FROM MEMORY

The Type From Memory operation reads data stored in memory and utilizes the data to control the typewriter. In order to initiate a Type From Memory operation, the TFM lane 43D must be programmed along with the CAD where the start of the typing data is stored. As with the TTM operation, the TFM must be initiated by a printer cycle.

TYPE FROM MEMORY BLOCK DIAGRAM

The first block shown in Fig. VI-9 is the memory with two groups of CAD's, the even tens or N data and the odd tens or Z data. These are the memory locations discussed in the TTM operation.

When the operation is initiated, the N data is read from the MSD of the pinned CAD into the MR. This data is transferred to the WR and the Z data is read from the corresponding odd tens CAD to the MR. The MR and WR signals are then fed to gating for the carriage movement decoder and to solenoid drivers. If the data read is alphanumeric (MR8 - Slide 7 is not high) the data will cause the SD's for the code slide block solenoids 1 thru 7 to position the blocking slides to limit the coding slides for the character to be printed. The coding slides will result in the mechanical positioning of the type box.

If the data read contains an MR8, the carriage control data decoder will cause SD's to pick the prpper carriage control solenoids to cause a tab, return and/or space to take place. The Space solenoid can be wired to pick on any or all carriage operations. The alphanumeric and carriage control data is fed into a punch decoder if the machine has punch equipment. The punch decoder converts the data from the typewriter code to the regular card or tape code so that punching can be obtained from alphanumeric data stored in memory.

SLIDE BLOCKING SOLENOIDS

The slide blocking solenoids are mounted on the outside of the left auxiliary sideframe, see Fig. VI-4. The solenoids move blocking slides at right angles to the code slides which provides limits for projections on the code slides. The construction of the assembly is such that the solenoids 1 thru 7 must be picked to cause blocking of the code slides. The Shift slide solenoid must be picked to release the SH slide. Thus, the solenoids must be picked to represent a 0 and not picked to represent a 1 of the code slide.

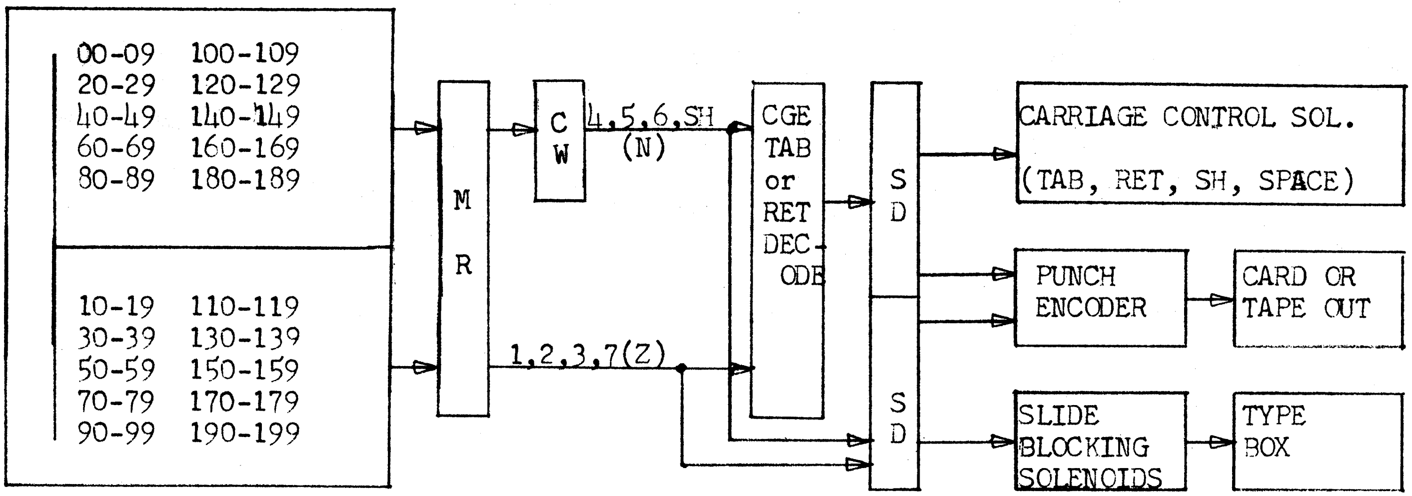


Figure VI-9

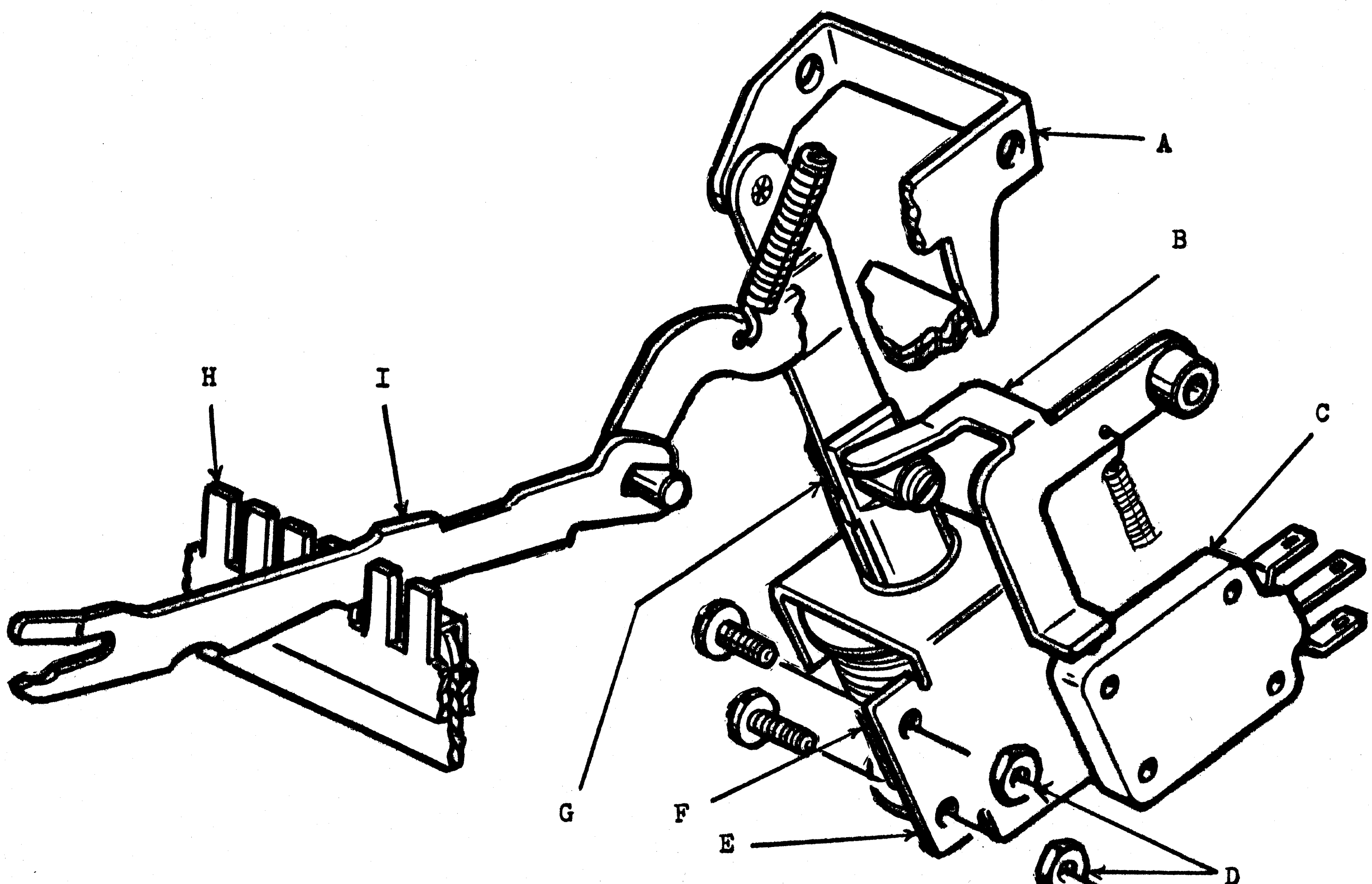


Figure VI-10

This is an inversion of the way in which data was written into the memory. For this reason, the Not MR1, Not MR2, Not MR4, Not MR8, Not WR1, Not WR2 and Not WR4 signals are used for the 0 or 1 condition to energize solenoids 1 thru 7 during the TFM operation. The WR8 signal is used to energize the shift slide solenoids.

TYPE OUT OF MEMORY FF

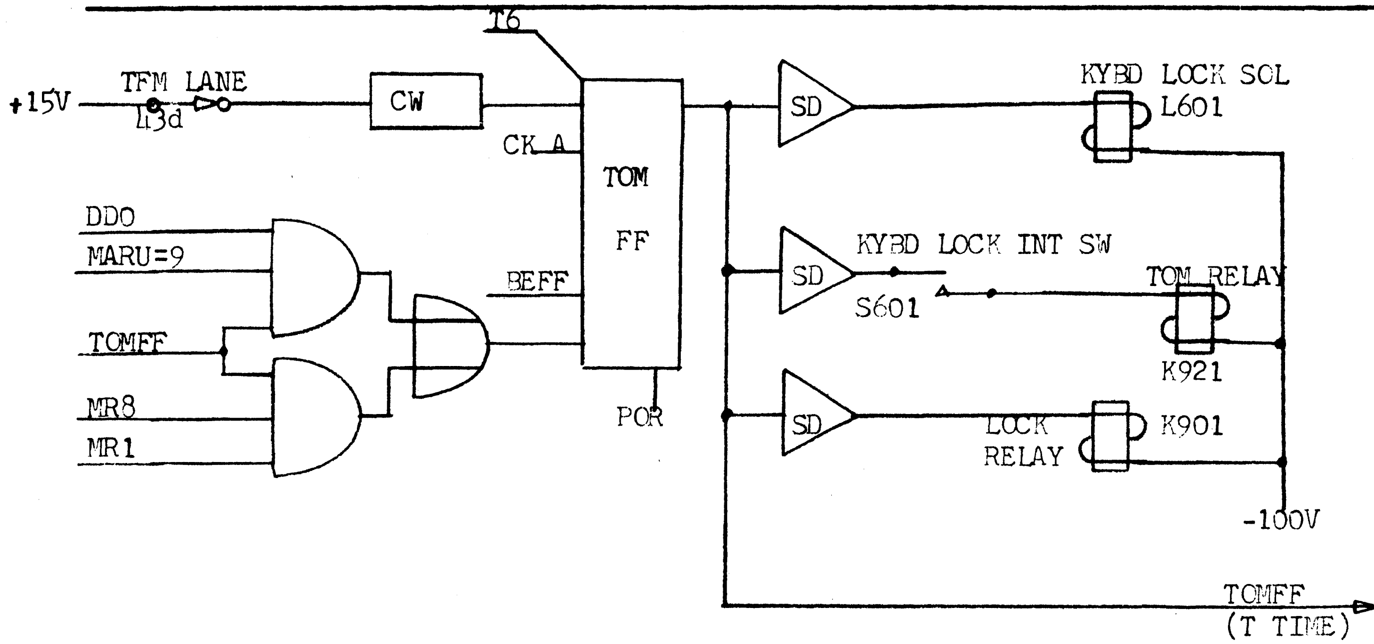
When the TFM lane switch is made during the initiating printer cycle, the Type Out of Memory flip flop (TOMFF) is set. The TOMFF provides a signal to pick the KYBD LOCK SOL. through a SD. The KYBD LOCK SOL. (see Fig. VI-10) locks the typewriter keyboard by moving an arm into the interlocks in the same manner as one key prevents the depression of any other key. By the same mechanism, if the operator holds a typewriter key indexed, the KYBD LOCK SOL. cannot pick to complete the start of the TFM operation. When the KYBD LOCK SOL. picks, an arm B operates as a switch C (Keyboard Lock Interlock Switch) which is mounted on the solenoid bracket. The keyboard lock int. sw. closes a circuit to allow the TOMFF to pick the TOM relay (K921) through a S.D. The TOMFF also picks the LOCK relay to disable the printer. The TFM operation will continue as long as the TOMFF remains set. The TOMFF is, then equivalent to a T time.

The TOMFF will be reset by the reset of the BEFF when one of two conditions is met. These conditions are: (1) When the MR8 and MR1 signals are high at the same time. This is the end of message code written at the end of the TTM operation. (2) When the MARU=9 and DDO signals are high at the same time. This is a signal that the end of the selected memory group has been reached.

TOM RELAY

The TOM relay, see Fig. VI -11, which is picked by the TOMFF and keyboard, lock int. sw., provides the following circuits to allow the data in memory to control the operation.

1. A set of TOM contacts provide full power to the hysteresis clutch in machines not equipped with the permanent magnetic clutch so that the carriage will move properly when escapement is indexed.
2. A set of TOM contacts transfers the SH slide solenoid from the shift key circuit used on the TTM operation to the WR8FF circuit. The SH slide solenoid is the only slide solenoid used on the TTM operation.
3. A set of TOM relay contacts prepares the circuit to energize the typewriter clutch solenoid L6, see Fig VI-12. This solenoid is energized for each character to be typed by the typewriter interlock switch (S774). The pick circuit is from -100V through TC8, the solenoid, typewriter interlock switch, tappet switch C, TAB relay contacts, TOM relay contacts, Shift switch (S9) contacts, the End Position Switch (S15) and In Tab Switch to ground.
4. Two sets of TOM relay contacts are involved in the L1, L2, L3 and L4 carriage movement solenoids circuits. A normally closed set of contacts is opened to remove the ground used on the regular typewriter operation. During the TFM operation, the ground will be supplied as data from the memory by the set or reset condition of the MR and WR flip flops. A set of normally open TOM contacts provides the -100V supply for the L1 and L4 solenoids. These solenoids must have a voltage source during the TFM operation so that the grounds from the data in memory can pick the solenoids. Data in memory triggers SD's.


T6
+15V
TFM LANE
43d
CW
CK A
TOM
FF
BEFF
POR
DDO
MARU=9
TOMFF
MR8
MR1
SD
KYBD LOCK SOL
L601
KYBD LOCK INT SW
S601
TOM RELAY
K921
LOCK
RELAY
K901
-100V
TOMFF
(T TIME)

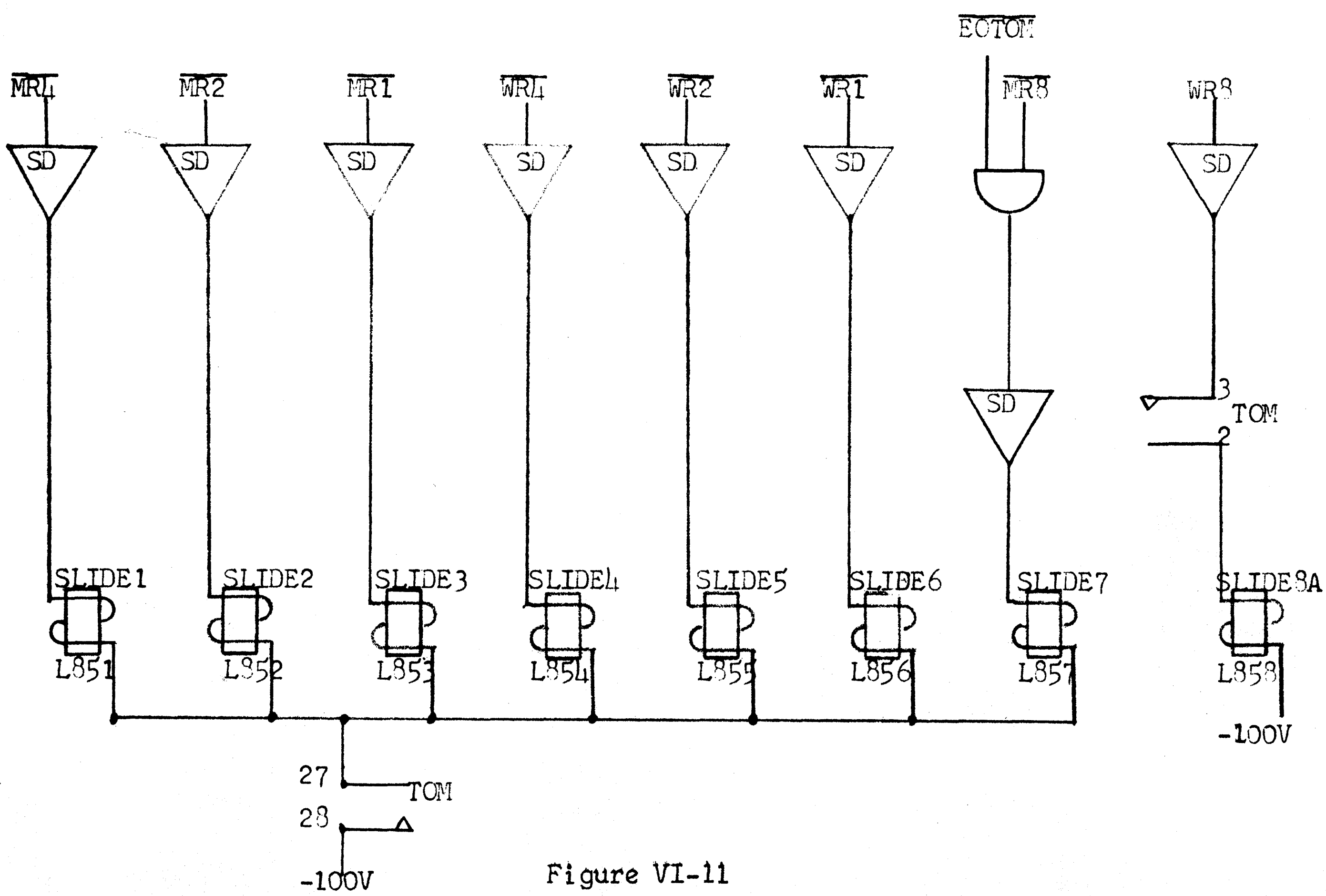

EOTOM
MR4
MR2
MR1
WR4
WR2
WR1
MR8
WR8
SD
3
TOM
2
SLIDE1
SLIDE2
SLIDE3
SLIDE4
SLIDE5
SLIDE6
SLIDE7
SLIDE8A
L851
L852
L853
L854
L855
L856
L857
L858
-100V
27
TOM
28
-100V

Figure VI-11

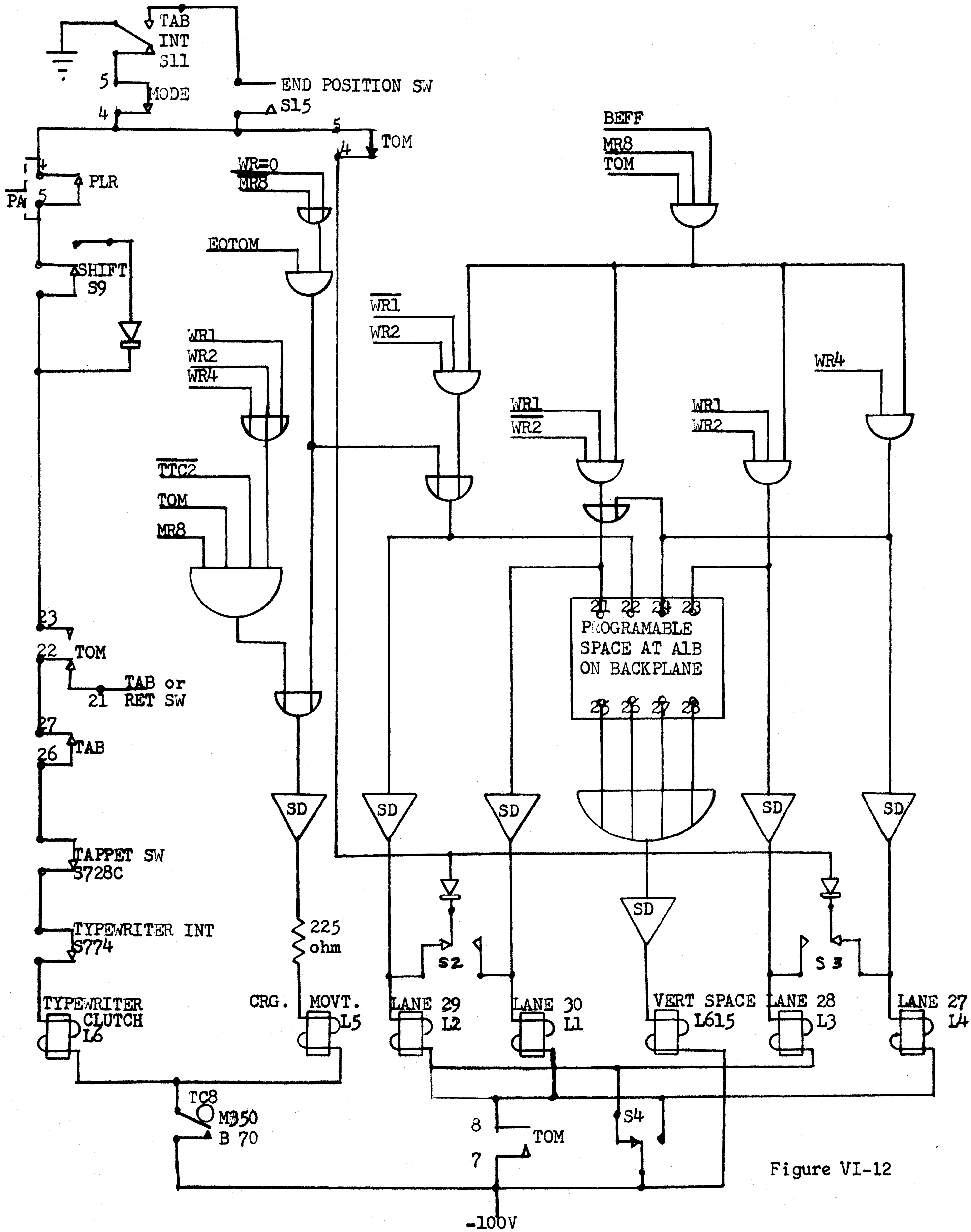

TAB
INT
S11
5
MODE
4
END POSITION SW
S15
5
4
TOM
PLR
PA
SHIFT
S9
WR=0
MR8
EOTOM
BEFF
MR8
TOM
WR1
WR2
WR1
WR2
WR4
WR4
WR1
WR2
WR1
WR2
TTC2
TOM
MR8
23
22 TOM
TAB or
21 RET SW
27
TAB
26
21 22 24 23
PROGRAMABLE
SPACE AT A1B
ON BACKPLANE
25 26 27 28
SD
TAPPET SW
S728C
TYPEWRITER INT
S774
225
ohm
S2
S3
TYPEWRITER
CLUTCH
L6
CRG. MOVT.
L5
LANE 29
L2
LANE 30
L1
VERT SPACE
L615
LANE 28
L3
LANE 27
L4
TC8
M350
B 70
8
TOM
7
S4
-100V

Figure VI-12

5. A set of TOM contacts remove -100V from the slide blocking solenoids except the SH solenoid that the solenoids will not pick from data in the MR and WR except during the TFM operation.

The diodes shown above S2 and S3 are isolation diodes and prevent a ground on the L1 solenoid circuit being fed back through the S2 and S3 switches to pick L4 and Vise Versa.

The space solenoid is mounted just to the rear of the typewriter tab and return keys and below the typewriter keyboard. This solenoid, see Figure 13, (L615) when picked, indexes the space mechanism and can be wired to pick from any or all data information that would pick L1, L2, L3 or L4.

The carriage movement solenoid L5 is picked directly from data in memory.

TYPE FROM MEMORY FLOW CHARTS, SEE PRINTS

The initial conditions for TFM are the same as those for TTM since TFM will always be set up by a printer cycle.

DDO The DD will be in DDO at the end of the initiating cycle.

NOT CiFF The CiFF will be reset at the end of the initiating cycle.

NOT COMPFF The COMPFF will be reset at the end of the initiating cycle.

CAD The C Memory location where TFM is to start must be programmed in the last printer cycle position.

Assume the same data and memory location used in the TTM flow chart discussion (JOHN DOE 333 22 0000 in CAD20).

SET TOMFF The TOMFF will be set when T6 is high in the initiating printer cycle. CAD 20 is also pinned.

PICK LOCK RELAY The TOMFF signal picks the LOCK relay to prevent printer

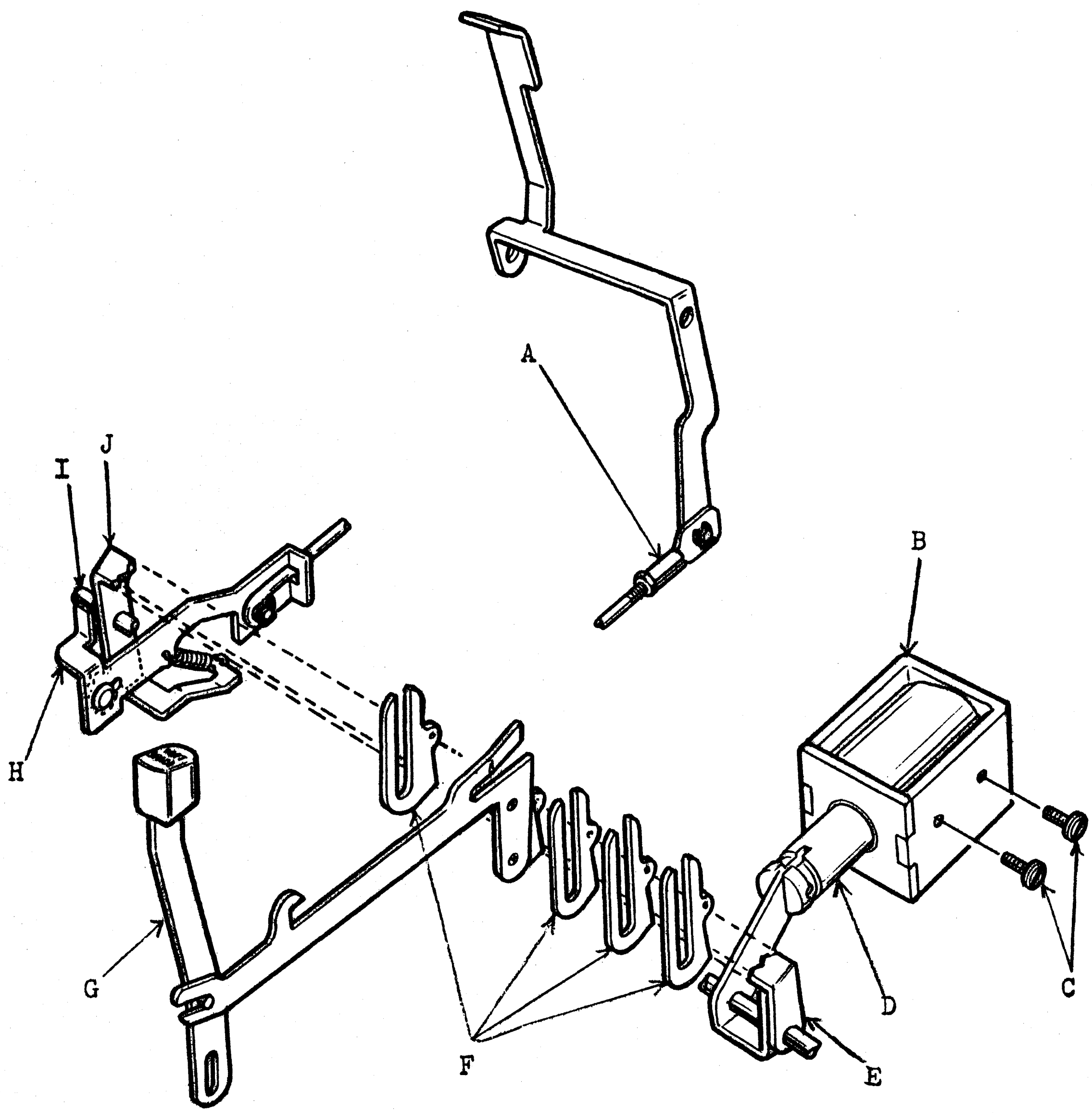


Figure VI-13

cycles during the TFM operation.

PICK KYBD LOCK SOL. The KYBD LOCK SOL. is picked by the TOMFF to prevent depression of typewriter keys during the TFM operation.

PICK TOM RELAY The TOM relay is picked by the TOMFF signal and the KYBD LOCK INTERLOCK SWITCH. The KYBD. LOCK INT. SW. is transferred by the KYBD LOCK SOL. The TOM relay prepares circuits so that the data read from memory can be used to pick the slide solenoids and carriage control solenoids.

The limits for the slides must be set up prior to 6° of each camshaft cycle because the slides start to move to the indexed position at 6°. It follows, then, that the data read from memory during each camshaft cycle will be used to provide limits for the slides on the following cycle. In order to have data available to pick the solenoids for the first cycle a read of data must be made during the latter part of the initiating printer cycle. The signals which trigger this read are the TOMFF and END OP. The first read of data occurs just after the end of the arithmetic cycle. TOMFF and the trailing edge of END OP sets SW.

SW - DDO of CAD 20

READ No read takes place in DDO. Not DDO is low.

SET MR→MEM The MR to MEM is set so that data can be written back to Memory in SX.

SET DDREV The DDREVFF is set so that reading will begin in the MSD of CAD 20.

SX - DDO of CAD 20

WRITE No write is performed in DDO.

SET MART1) MART 1 is set to select CAD 30.

GT MR—▷WR   TOM causes a transfer of data from the MR to the WR.

SY - DDO of CAD 30

READ   No read is made in DDO.

CiFF   The CiFF is not set in DDO.

0—▷WR   The WR is set to zero.

0—▷MR   The MR is set to zero.

SZ - DDO of CAD 30

WRITE   No write takes place in DDO.

RESET MART1   MART1 is reset to return the CAD to 20.

STEP DD   The DD is stepped to DD1.

SW   TOM and DDO returns the logic to SW.

GT MARU—▷ADDER   The units of CAD 30 (0) is gated to the adder.

GT ADDER—▷MARU   The units of CAD 30 is made equal to the adder. WR=0, MR=0. CiFF is reset and MARU=0. The adder is equal to zero and the units of the CAD is not counted at this time.

The net results of the above sequence is the stepping of the DD.

SW DD1 of CAD 20

READ   The N code of the J (1) is read into the MR from the MSD of CAD 20.

SET MR—▷MEM   The MR to MEM FF is already set.

SET DDREV   The DDREVFF is already set.

SX - DD1 of CAD 20

WRITE   The data in the MR (1) is written back into the MSD of CAD20.

SET MART 1 MART1FF is set to select CAD 30.

GT MR→WR The data in the MR (N code of J) is transferred to the WR.

SY - DD1 of CAD 30

READ The Z data of J (1) is read from the MSD of CAD 30.

SET CiFF The CiFF is set to provide an input to the adder so that the MARU can be counted at the end of each word of memory.

0→MR The MR is not set to zero. DDO is low.

0→WR The WR is not set to zero. DD0 is low.

SZ - DD1 of CAD 30

WRITE The Z data of J (1) is written back into the MSD of CAD 30.

RESET MART1 MART1FF is reset to return to CAD 20.

STEP DD The DD is stepped to DD2.

GT MARU→ADDER The MARU is gated to the ADDER.

GT ADDER→MARU The ADDER is not gated to the MARU. DDO is low.

SW Sequence W is not set. DDO is low.

At this point, the following things have occurred. The logic has been triggered by the END OP signal, the DD is stepped to DD1, the N bits of J have been read from memory, gated into the WR and written back into memory. The MART was counted and the Z bits of J have been read into MR and written back to memory. The CiFF has been set to count the MARU and the MART1 reset.

With the N data in the WR and the Z data in the MR, the MR1FF and WR1FF will be set and the MR2, MR4, MR8, WR2, WR4 and WR8 will be reset. The not MR4, not MR2, not WR4, not WR2 and not MR8 signals will be high and will pick the 1, 2, 4, 5 and 7 solenoids respectively. With these solenoids picked, limits are provided for all slides except 3 and 6. These are the slides necessary to position the type box to print the character J.

The LOCK relay, KYBD. LOCK SOL. and TOM relays have been picked and the machine cycle continues. TC8 makes at 350° and completes a circuit to pick the typewriter clutch solenoid. The typewriter camshaft starts to rotate and all code slides are limited except 3 and 6 which will select J. At 50° of the camshaft TTC1·PH1·CK sets the TTCFF which will cause BEFF to set. At 200°, TTC2·PH2·CK resets the TTCFF which causes BEFF to reset. The negative swing of the BEFF signal when TOM and not EOTOM signals are high will set the SW flip flop to trigger the read of the next character from memory, a 0 in the example. The reading of character data into the MR and WR and the limiting of the code slides by the data continues as described above until the data is read for returning the carriage after the E in JOHN DOE is typed, Fig. VI-14. The data in the WR is 3 and in the MR is 8. The not MR8 signal will be low which allows slide 7 to be indexed to disable positioning the type box. The WR1, WR2 and MR8 signals are high. These signals will cause the L5 solenoid to be energized to provide a carriage return and L3 to be picked to enable the lane return latch. With the proper jumper installed, the space up solenoid will also be picked.

Typing continues until the end of the social security number is reached. At this point, the TAB 4 code is read, a 9 in the MR and a 4 in the WR. The not MR8 is low and slide 7 will be indexed to disable positioning the type box. The TOM, MR8 and WR4 signals pick the L1 and L4 solenoids to enable a carriage tabulation latch. L5 solenoid is also picked to cause carriage movement to be indexed. The space up solenoid will also be picked if programmed with a jumper. The MR1, MR8 and BEFF signals will cause the TOM FF to be reset when BEFF is reset by the TTCFF·PH2·CK·TOM at 200° of the cycle. The resetting of TOMFF drops the LOCK, and TOM relays the KYBD LOCK SOL. to release the machine for regular posting or other operations.

TERMS USED WITH THE TYPE TO AND TYPE FROM MEMORY FEATURE

TTM	Type To Memory. Panel layout designation for programming the type to memory feature.
TFM	Type From Memory. Panel layout designation for programming the type from memory feature.
TIMFF	Type Into Memory Flip Flop. A flip flop which controls the TTM feature in the same way the T time flip flops control the arithmetic cycle.
TOMFF	Type Out of Memory Flip Flop. A flip flop which controls the TFM feature in the same way the T time flip flops control the arithmetic cycle.
TOM RELAY (K 921)	A relay which is picked during the TFM operation to transfer the control of the carriage movement solenoids to the data circuits. TOM also picks the typewriter clutch solenoid.
BEFF	Bounce Eater Flip Flop. The BEFF is picked and dropped by TTCFF. BEFF provides a noise free signal that coincides with TTC1 and TTC2.
TTCFF	Typewriter Timing Cam FF. Set by TTC1 and RESET by TTC2.
TTC1 (S 651)	Typewriter Timing Cam Switch One. TTC1 is made from 50° to 70° of the typewriter camshaft cycle. TTC1 provides timing for writing data to memory during the TTM operation.
TTC2 (S 652)	Typewriter Timing Cam Switch Two. TTC2 is made from 200° to

to 300^{o} of the typewriter camshaft cycle. TTC2 provides timing for reading data from memory during the TFM operation.

BLOCKING SOLENOIDS (L671 - L678) Solenoids which position blocking slides to limit the coding slides during the TFM operation.

BLOCKING SLIDES Slides which provide a limit for projections on the coding slides.

CODING SLIDE SWITCHES Reed (Magnetic) switches which provide electrical signals that represent the position of the coding slides.

KYBD. LOCK SOL. Keyboard Lock Solenoid. A solenoid which locks the typewriter keyboard and transfers the keyboard lock int. sw.

KYBD LOCK INT. SW Keyboard Lock Interlock Switch. The keyboard lock int. sw. picks the TOM relay to complete the start of the TFM operation.

CAD "C" Memory address. A memory location selected by the lane switches.

SRX (1,2,4,8) Shift Register X. Four flip flops used for temporary storage of data.

MARU (1,2,4,8) Memory address register units. Flip flops used to retain the units of the selected memory address.

SPACE SOLENOID (L 615) When picked, the space solenoid indexes the platen space mechanism.

PHFF Phase FF. Prevents noise getting through TTCFF to set BEFF.

TEST & ADJUSTMENTS

1. See Fig VI-13 , lower all driver F into the patch of trigger bail E. With trigger bail E limiting on the rear most driver F and formed ear of trigger latch H limiting on post I, there should be .010" to .035"

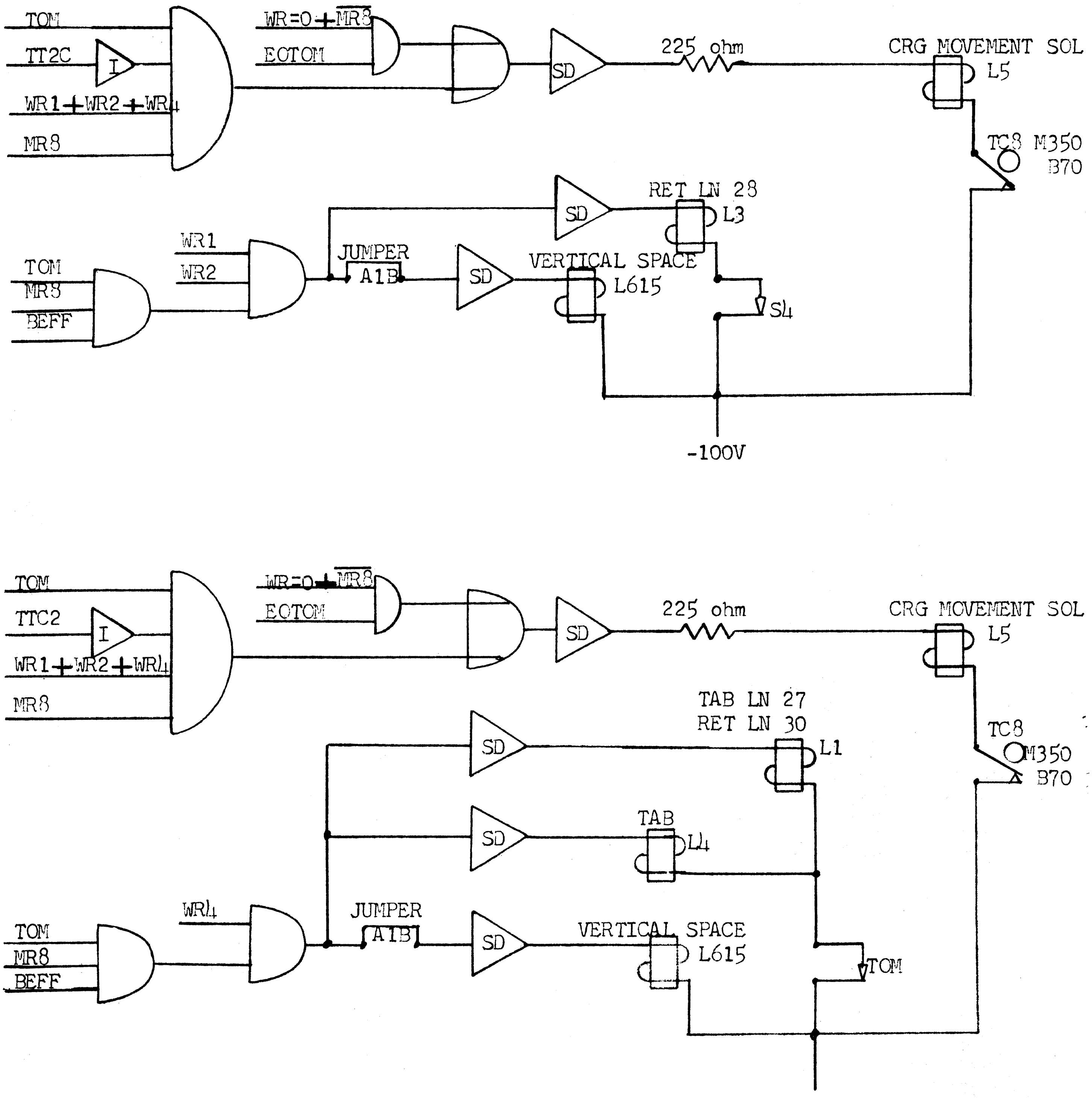

TOM
TT2C
I
WR1+WR2+WR4
MR8
WR=0+$\overline{MR8}$
EOTOM
SD
225 ohm
CRG MOVEMENT SOL
L5
TC8 M350
B70
RET LN 28
L3
WR1
WR2
TOM
MR8
BEFF
JUMPER
A1B
SD
VERTICAL SPACE
L615
S4
-100V
TOM
TTC2
I
WR1+WR2+WR4
MR8
WR=0+$\overline{MR8}$
EOTOM
SD
225 ohm
CRG MOVEMENT SOL
L5
TAB LN 27
RET LN 30
L1
TC8
M350
B70
TAB
L4
WR4
JUMPER
A1B
VERTICAL SPACE
L615
TOM
TOM
MR8
BEFF
-100V

Figure VI-14

clearance between the driving edge of trigger bail E and trigger latch H.

TO ADJUST: Bend formed ear of trigger latch H at point of contact with post I as required.

REASON: To ensure sufficient throw of space mechanism and reset of trigger bail E beyond trigger latch I, when the vertical space key G and the four carriage movement keys are depressed and released.

2. When the vertical space key G and the four carriage movement keys are slowly depressed individually, the vertical space clutch in the gear box should engage just prior to release of trigger latch E from trigger bail H.

TO ADJUST: Turn turnbuckle A as required.

REASON: To ensure engagement of vertical cpace clutch, just prior to release of trigger latch H from trigger bail E.

3. When plunger D of solenoid B is manually bottomed against the core of the solenoid, the vertical space clutch in the gear box should engage just prior to release of trigger latch H from tirgger bail E.

TO ADJUST: Loosen screws C and move solenoid B as required.

REASON: To ensure engagement of vertical space clutch just prior to bottoming of plunger D against the core of solenoid B.

4. See Fig VI-10 with plunger G of solenoid F seated against the core of the solenoid, all keys in the typewriter keyboard should be interlocked against depression.

TO ADJUST: (a) Loosen nuts D freeing solenoid bracket E.

(b) Manually rock bail A until interlock I limits in the keyboard interlock assembly H, and hold bail A in this position.

(c) Manually position solenoid bracket E to seat core of solenoid F against plunger G and tighten nuts D.

REASON: To prevent depression of keys in the typewriter keyboard when solenoid F is energized.

5. With the plunger of solenoid F seated against the core of the solenoid, there should be .025" to .030" clearance between the ear of switch actuator B and the body of switch C.

   TO ADJUST: Bend the upper ear of switch actuator B as required.

   REASON: To ensure transfer of switch contacts and maximum life of switch C.

INTRODUCTION

APPLICATION AND OPERATION

The Style A4002 Auto Reader is used as an adjunct to the Direct Accounting Computer, Series E2150. If provides, (1) an automatic trial balance of the ledger on a listing tape, and (2) transfer of balance to new ledger accounts with an accumulated total and tape listing as desired.

The A4002 consists of a single movable unit containing an automatic form feed, form transport, heads for reading the magnetic stripes, and a receiving hopper. There is no provision for writing on the form which in the A4002. All writing, adding and printing is performed by the E2150. A panel of control switches and indicator lamps is located in the A4002. The A4002 is connected by a plug-in cable to the E2150 and all power for the Auto Reader is supplied through this cable.

Control Switches and Indicator Lamps

The control panel located on the front of the A4002 and above the receiving hopper consists of a series of five switches and four lamps. In rotation from right to left the switches, indicator lamps and markings are as follows:

ON-OFF switch with Indicator Lamp - This switch, makred ON and OFF in green is used to turn the power to the Reader on or off. The E2150 power must be on for the Auto Reader to operate. The indicator lamp is illuminated when the power is on both machines.

AUTO FEED switch - The depression of this switch, marked AUTO-FEED in green, causes forms to be fed and processed until stopped from some other source.

SINGLE FEED switch - Depression of this switch, marked SINGLE-FEED in green, causes a single form only to be fed and processed.

STOP FEED switch with Indicator Lamp - This switch, marked STOP-FEED in red, permits the operator to interrupt the automatic operation of the machine. After the processing of the active form is completed the machine will stop and the lamp will be illuminated. A SINGLE FEED or AUTO FEED switch will restart the form feed and turn off the indicator lamp.

DOUBLE FORM switch with Indicator Lamp - This lamp and switch is marked DOUBLE FORM in red. Whenever the adjustable double document mechanism senses a thickness greater than one form, the feed is stopped and the DOUBLE FORM lamp is illuminated. A misoperation may be caused by feeding two forms or perhaps by sensing the extra thinkness of a multilated form. The depression of the DOUBLE FORM switch will complete the transport cycle and stack the form or forms involved in the receiving stacker. No form reading or printing will occur. After the information from the form or forms in question is entered manually,

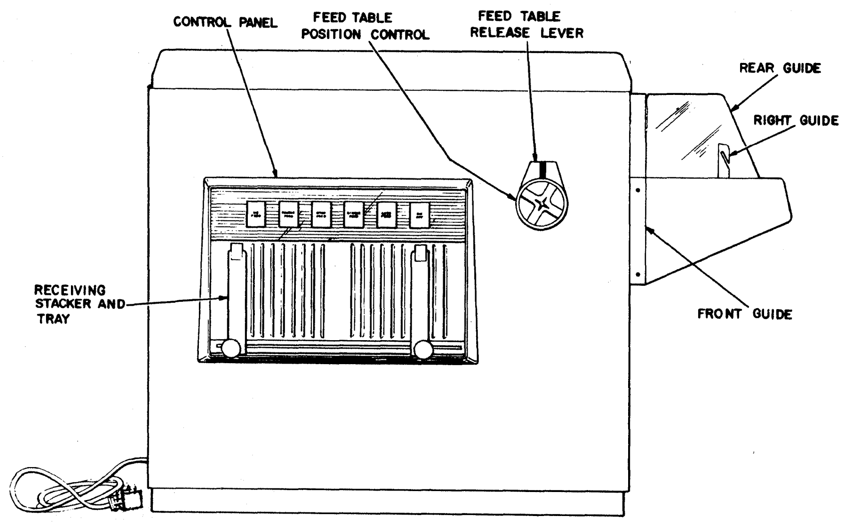

CONTROL PANEL
FEED TABLE
POSITION CONTROL
FEED TABLE
RELEASE LEVER
REAR GUIDE
RIGHT GUIDE
RECEIVING
STACKER AND
TRAY
FRONT GUIDE

Figure VII-1

or the form or forms returned to the feeder for automatic handling, the SINGLE FEED or AUTO FEED switch is used to restart the feeder and turn off the DOUBLE FORM lamp.

NO FEED Indication Lamp - This lamp, marked NO FEED in red, indicates the machine is unable to feed a form. In the event the feeder fails to feed a form on two consecutive attempts, the A4002 stops and the NO FEED lamp is illuminated. The lamp remains on until the SINGLE FEED or AUTO FEED switch is used. Whenever the machine is unable to read the magnetic stripe it is stopped by the Error circuit and the RD lamp on the E2150 is illuminated. The ERFF immediately stops any further form feeding. The form on which the error was detected continues to feed and stack in the hopper.

A4002 is basically set to take a trail balance. Lane 54 and LN 56 (Feed Ledger) is specifically required for the A4002 trial balance operation.

For Specifications

Width - The A4002 can handle forms from 3" to 14½" in width.

Height - A. Forms varying in height from 10 1/6 to 11 inches may be used. Only one form height may be used on any one machine.
B. A fixed form limit is used in the A4002. The center stripe must be 2" from the right edge of all forms.

FEED TABLE

The Feed Table is located on the right side of the A4002 accessible to a seated operator. The maximum capacity of the Feed Table is a stack of forms 4 1/2" thick, which is approximately 500 accounts. To accomodate stacks of varying heights a feed table elevating knob is provided on the front of the A4002 to raise the table to the prescribed height. A thumb release just above the feed table elevating knob lowers the feed table. An adjustable form limit post is located at the center of the feed table. This post limits the forms and assists in their separation. After the forms have been loaded on the feeder table, the form limit post should be brought up to the back of the forms and the feed table elevated until the top form is level with the upper level indicator.

Output Stacker

The output stacker is located in the front of the machine under the control panel. The receiving tray located in the output stacker can be partially pulled out to facilitate the removal of a small stack of forms, or it can be pulled completely out for use as a tray to transport a large stack of forms.

Operation

The A4002 should be located at the operator's right when seated at the E2150 console. The forms are placed in the feed table, face up, with the right edge toward the machine. The adjustable form limit post is brought up against the rear of the forms. The ON-OFF keys must be in the ON position on both the A4002 and the E2150.

The A4002 is started by either the AUTO FEED or the SINGLE FEED switch. The forms are picked up and transported past the rear heads to the output stacker face down, with the bottom of the forms toward the operator. The A4002 may be connected to the E2150 without interfering with the normal posting run provided the ON-OFF switch of the A4002 is set to OFF.

Trial Balance Operation

Routine

1. Clear the E2150 memory.

2. Position the E2150 carriage in a trial balance programmed position (as indicated on the form layout).

3. Load the feed table with a stack of forms with the top edge of the forms nearest the operator. Position the feed table so as the top form is level with the form height indicator.

4. With both the E2150 and A4002 turned on depress either the SINGLE FEED or AUTO FEED switch. Single Feed allows only one form to be fed and read. Auto Feed causes a continuous cycle of feeding and reading forms at the rate of approximately 48 forms per minute until the feed table is emptied.

Each form is fed into the Ready Station and then past the read heads and stacked in the output stacker. The data encoded on the form stripes is accumulated in the E2150 memory. A programmed print operation of at least one data word is performed by the E2150. Any number of these words may be programmed to print.

In the event of a Read Error the operation will stop and the E2150 will indicate to the operator that an error has occurred on the top form of the output stacker. This form should be removed. Depression of the Read Light switch on the E2150 will restart the Auto cycle and eliminate any accumulative addition of the data from the misread form. After all forms from the feed table have been read, the misread form can be inserted and read. It should then be reinserted in its proper sequencial order in the stack.

BALANCE TRANSFER OPERATION

Routine

1. Clear the E2150 memory.

2. Position the E2150 carriage in a Balance Transfer programmed position.

3. With both the A4002 and E2150 turned on and a stack of forms loaded to the correct height in the feed table, depress the Auto Feed switch. This will cause a form to feed into the A4002 Ready Station where it will wait until a blank form is placed into the E2150 carriage throat.

4. Both forms will feed at the same time. The blank form will position at line #1. The form in the Auto Reader will feed from the Ready Station and be read. The data is transferred to the E2150 memory where it is block added for accumulated totals.

5. As the blank form is being fed, the printed account number from the blank form should be indexed on the keyboard. This will allow verification of the form read and the form being transferred to. Twelve digits or less may be programmed to verify. Normally, three or four are used. The verify cycle begins as the blank form positions itself at line #1. Verify is a programable feature and may be omitted if so desired.

6. After a correct Verify, the printer will cycle and the carriage will move to a Write Ledger position. An auto cycle will be performed and the carriage will move to the starting Balance Transfer position. The carriage will open and the form will be written, encoding the data from the programmed memory of the E2150. During these printer cycles the auto reader was automatically feeding another form to the Ready Station. It will wait as before, until the next blank form is inserted in the E2150 carriage.

In the event of a read error, the top form from the output stacker should be removed. The Read Error lamp is depressed causing the blank card to eject from the carriage. Both cards should be set aside and handled at the end of the Balance Transfer Operation. Depression of the Read lamp cycles the carriage camshaft to its starting postion and prevents any accumulated arithmetic operations.

In the event of a write error on the blank card, the carriage must be positioned in a Write Correction Stop. In this stop the form with the encoded write error is reinserted into the carriage. It will position at line #1. A printer cycle will cause the carriage to move to an alternate write ledger position where an auto cycle takes place. During this cycle the carriage will move to the starting Balance Transfer position where the carriage opens and the form is written as before.

MECHANISMS AND ADJUSTMENTS

TRANSMISSION ASSEMBLY - Figure VII-2

The transmission assembly is used to furnish power to the feeder and transport system and is made up of four sections; Reduction and Right Angle Drive Gear Assembly, Feed Cam Clutch Assembly, Drum Driver Assembly and the Drive Belt and Pulley Assembly.

Pulley V is fastened on the motor drive shaft and is coupled to shaft S by V belt W and pulley Y. Shaft S contains geared pulley T which drives the high speed rolls through a Gilmer belt. Shaft S also contains worm gear M which turns gear K to provide a speed reduction of 7.5 to 1. Shaft O, which is driven by gear K, supplies power directly to the feeder clutch and contains geared pulley R which drives the feed rolls through a Gilmer belt. Shaft O also contains gear I which turns gear J mounted on shaft AB and supplies power to the Drum Drive through shaft AB, geared pulley AG, Gilmer belt AH, and geared pulley AK. The Feed Cam Clutch is a spring coupled clutch controlled by a solenoid and supplies power to the feed cam through geared pulleys and Gilmer belts. The drum is constantly running and receives its power from a gear and Gilmer belt assembly driven by gear AK.

The vacuum release valve C is operated by cam D and removes the vacuum from the feeder after the form has entered the feed rolls. This prevents the form being held against and dragged across the vacuum yoke as it is feeding into the machine. The vacuum pump is driven by the motor through one section of pulley V, belt Z and pulley AJ which is mounted on the pump shaft. The pump is an off center vane type pump and both the intake and exhaust are filtered to prevent wear or damage to the graphite vances by dirt.

DRIVE BELT AND PULLEY ASSEMBLY - Figure VII-3

Tests and Adjustments

1. To provide correct alignment of the motor with the transmission --

   With a straight edge extended across the transmission side of transmission pulley B, the fact of pulley D on the motor should be parallel to and in contact with the straight edge.

   To adjust, square motor and move pulley D on motor shaft as required. Snug motor mounting bolts.

2. To ensure positive drive of the transmission without escessive tension --

   The tension of belt C between the motor and transmission should be just sufficient to prevent slippage.

   To adjust, move motor, maintaining test 1, as required.

3. To provide correct alignment of the pump with the motor --

   With a straight edge extended from the motor side of motor pulley D, the pump side of pump pulley H should be parallel to, and in contact with the straight edge.

   To adjust, square pump and move pulley on pump shaft as required.

4. To ensure positive drive of the pump without excessive tension --

   The tension of belt E between the motor and pump should be just sufficient to prevent slippage.

   To adjust, move pump, maintaining test 3 as required.

REDUCTION AND RIGHT ANGLE DRIVE GEAR ASSEMBLY - Figure VII-4

Tests and Adjustments - Figure VII-4

Before making adjustments 1 through 3, loosen the set screws in parts E, G, I,

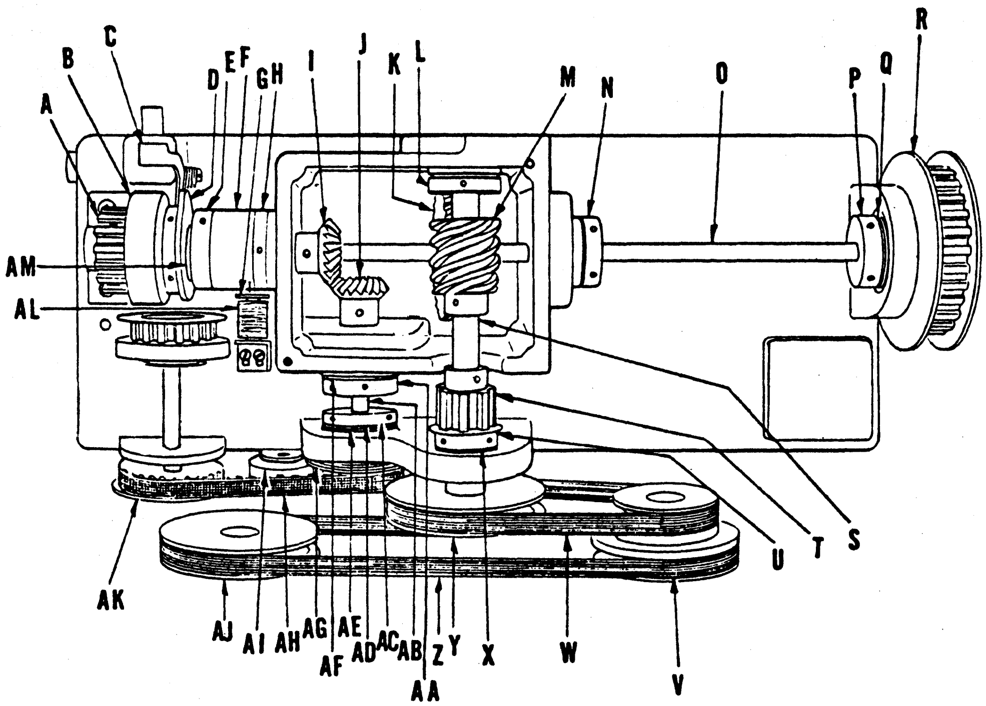


Figure VII-2

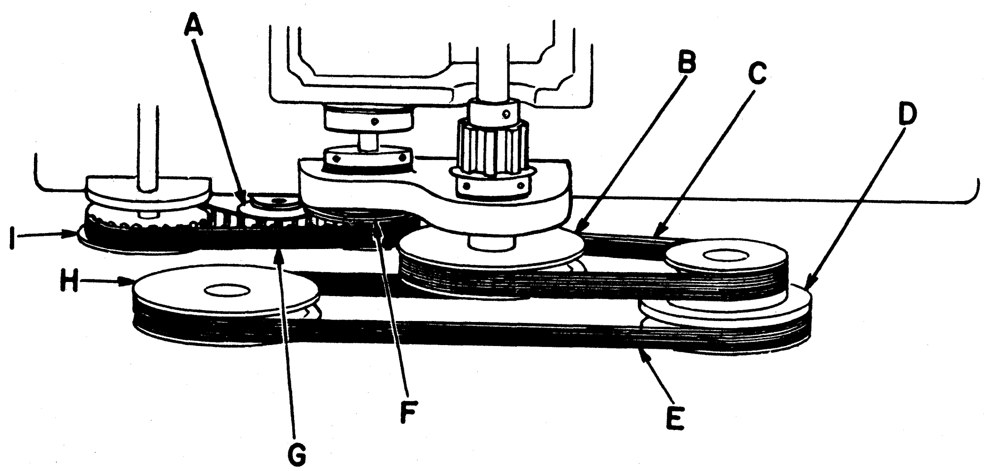


Figure VII-3

N, P and T.

1. To ensure free running clearance of gears B and C --

With the major outside diameter of the teeth on gears B and C flush, collar I and thrust bearing J should be located against the front bearing support and there should be .005" to .007" clearance between collar G and the gear box casting.

To adjust, position collars G and I as necessary.

2. To ensure free running clearance of gears B and C --

With the major outside diameter of the teeth of gears B and C flush, collar P and bearing R should be located against the bearing in the casting and there should be .005" to .007" clearance between collar T and its thrust bearing.

To adjust, position collars P and T.

3. To ensure free running clearance of gears D and E --

With the right end of shaft L flush with the right end of sleeve E and sleeve E against the bearing in the casting, there should be .005" to .007" clearance between collar N and thrust bearing O when O is against the casting.

To adjust, position sleeve E and collar N.

4. To ensure positive drive of the high speed rolls without excessive tension --

The tension of the high speed roll drive belt should be just sufficeint to remove the excessive whip of the belt.

To adjust, move the idler pulley as required.

5. To ensure positive drive of the feed rolls without excessive tension --

The tension of the feed roll drive belt should be just sufficient to remove the escessive whip of the belt.

To adjust, move the idler pulley as required.

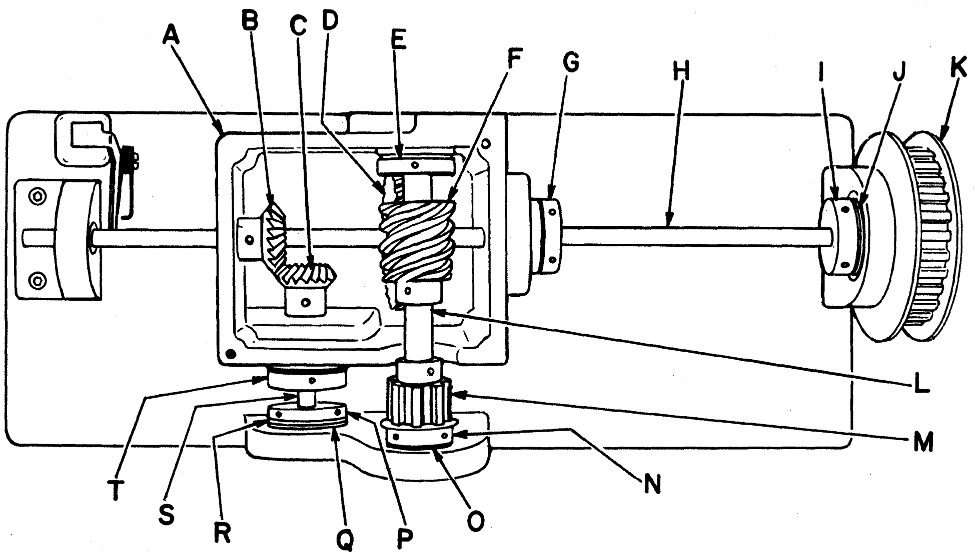


Figure VII- 4

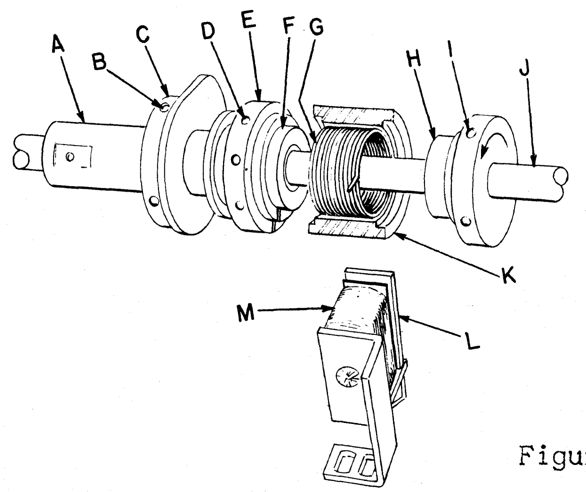


Figure VII-5

FEED CAM CLUTCH - Figure VII-5

Shaft J passes through the complete clutch and furnishes support for the clutch assembly. Shaft J is rotated by the main drive gears in the gear box and will rotate collar H which is fastened to it by screws I. As shaft J rotates, the friction between it and spring G causes the turned lip on spring G to contact clapper L of the control solenoid. This tends to uncoil spring G and allow collar H to slip within spring G. When clapper L is pulled from beneath the lip of spring G, the spring will contract around collar H. This will cause spring G to rotate which will allow spring G to tighten around collar F and cause it to turn also. Collar F is a part of hollow shaft A. Therefore, hollow shaft A will rotate and cause the drive pulley fastened to it to turn until clapper L is allowed to limit the lip of spring G again.

The removal of the feed clutch may be accomplished as follows. Remove the geared pulley from the end of shaft A and remove the screws holding the bearing housing. Remove the bearing housing and while holding shaft A, uncoil spring G slightly and pull shaft A and spring G off shaft J. Cam C and collars E and H may be removed by loosening screws B, D and I respectively. To assemble the clutch, place collar H on shaft J and tighten screws I securely into the dog point holes in shaft J. Slide collar E on collar G of shaft A, with the spring retaining slot out. Place spring G inside sleeve K with the turned lip of spring G projecting through the cut in sleeve K. Place the spring and sleeve on collar F while rotating the spring and sleeve clockwise until the horizontal lip of spring G slips into the spring slot of collar E. Slip the assembled shaft A, collar E, spring G and sleeve K over shaft J, until spring G limits on collar H. Uncoil spring G slightly and allow it to slip on collar H. Replace the bearing housing and geared pulley on shaft A.

Tests and Adjustments

1. To ensure proper position of collar H --

The pointed ends of screws I must be located in the dog point holes of shaft J.

To adjust, position collar H and tighten screws I.

2. To ensure non-binding clearance of clutch members with sleeve K --

Clutch member F should have .005" to .007" end play but maintain a maximum clearance of .014" between clutch members.

To adjust, with collar H secured on shaft J (test 1) and the play of shaft J held against the clutch, force clutch member F against collar H and position cam C as necessary.

3. To ensure proper timing of cam C --

With the lip of clutch spring G limited on the clapper of control solenoid and the movement of cam C taken up in the direction of rotation, the drop surface of cam C should be in alignment with the left radial surface of the roll on the vacuum control valve.

To adjust, reposition cam C using care to maintain Test 2.

4. To ensure positive release of feed clutch spring --

With clapper L held against the core of solenoid M, there should be .020" to .025" clearance between the face of the clapper and the end of the feed clutch spring.

To adjust, move solenoid bracket as required.

5. To ensure positive limiting of feed clutch spring --

With clapper L in its normal position, the end of the clutch spring should have

.010" less than a flush hold on the clapper.

To adjust, weave the limiting tails on clapper L as required.

6. To maintain correct timing between the feeder and the transmission --

With a six pound outward pressure exerted on the belt from the feed clutch 6" down from the idler gear, the horizontal distance between the tips of the teeth at this point should be 2-11/16" to 2-3/4".

To adjust, move idler gear as required.

FEEDER - Figure VII-6

The feeder is used to separate the forms stacked in the feed hopper and feed them singly to the Ready Station as the feed clutch is picked. It uses a vacuum type form picker which is lowered to pick up the top form then lifted and rocked toward the feed rolls to feed the form.

The front guide C keeps the top forms against the plastic guide T and guide A keeps the top forms against the plates O containing the separators Q. The air from the riffler tubes D and R helps separate the top forms and causes the top form to rise and minit against the separator fingers Q. As the vacuum yoke G picks up the top form, it will pull it by the separator fingers Q which will prevent the second form from sticking to it and causing a double feed.

Indicator S is used to indicate to the operator a definite position for the top form when elevating the feed table after the forms are stacked in the feeder.

The feed pressure rolls K hold the form in contact with the feed roll N. The pressure roll shaft assembly may be raised and lowered by screw F on each side of the feeder.

The Double Document and Drop count switch assemblies J and L have actuating arms and rollers over the feed roll N to sense the forms feed into the machine.

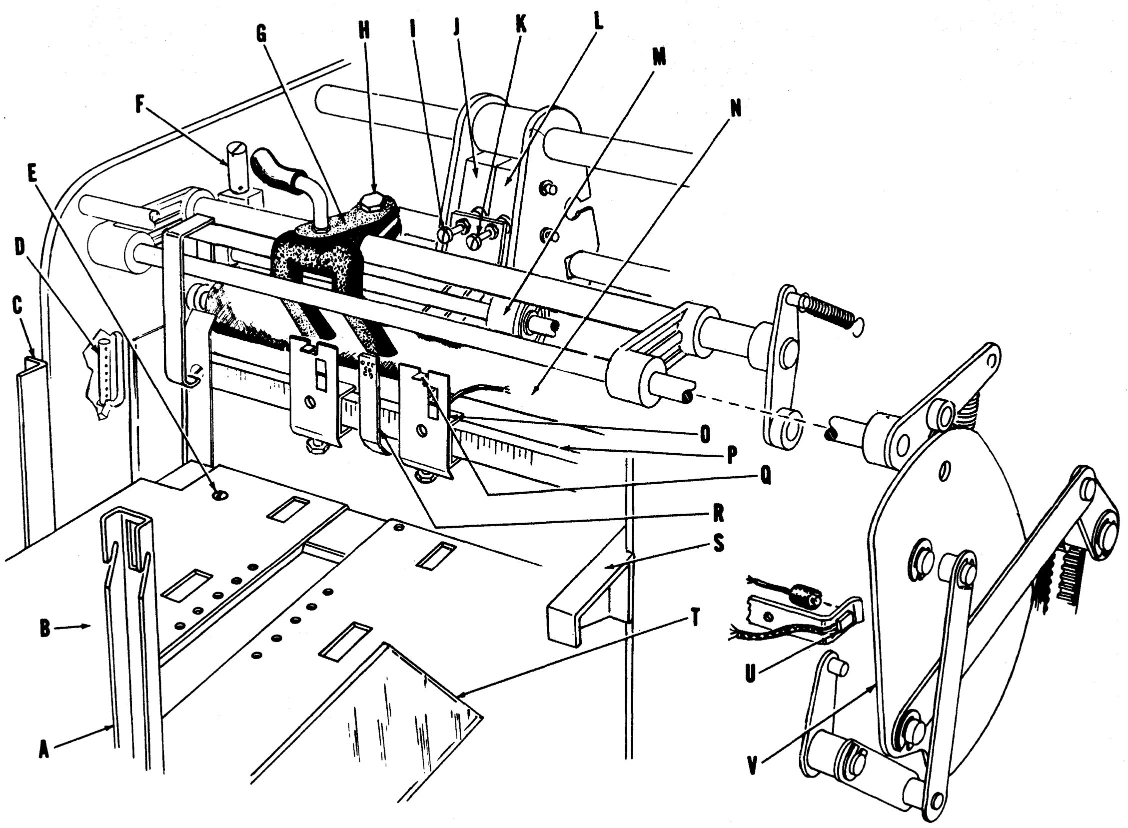


Figure VII-6

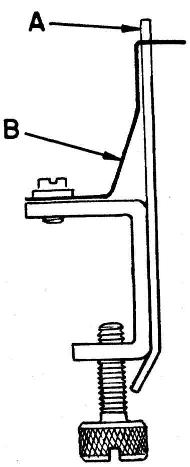


Figure VII-7

The Double Document switch J will sense the extra thickness of the forms if the feeder should try to feed two or more. The Drop Count switch L will sense the thickness of one form to indicate that a form has been fed.

SOLAR CELL ASSEMBLY - Figure VII-6

A solar cell and light assembly (u) is mounted to the side frame. It is used to detect the oscillations of the feed cam (V). Each feed attempt will cause the cam to block the solar cell from its light source. This will signal the electronic logic that a feed attempt is being made.

Tests and Adjustments

1. To obtain maximum efficiency of riffler tubes --

a.) the tip of the center riffler should have clearance with the feed roll not to exceed .031".

b.) the top hole in the center riffler tube R should align with a scale splaced against the under side of the lips of stripper fingers Q.

To adjust, a) Remove riffler tube from mounting bracket and form as required with parallel pliers.

b) position riffler tube as required. Reched step (a).

2. With the feed table level with the bottom of the cut outs in the seperator clip brackets and a .050 guage placed on top of the table: the bottom of the 3rd hole from the top of the side rifflers should align with the top of the guage and the holes should point to the closest suction foot.

To adjust, position as required.

3. To provide a correct initial position of the feeder table --

The top of the form position indicator S should be even with the top of the feed table when the table is manually raised to 1/8" below the cut outs in the form seperator assemblies.

To adjust, loosen mounting screw in indicator S and position as required.

4. To provide correct relationship of feeder parts --

a) both the vacuum foot and detection switch should be centrally located on their respection mounting shafts.

b) the left transport idler roll should align with the belt and the feed pressure rolls K should be just outside each suction foot.

To adjust, reposition as necessary.

5. To provide positive sensing of the double document switch J --

The DD should "make" when two forms are fed but should not "make" when a single form is fed.

To adjust, turn adjusting screw I until switch "makes" and then turn screw in opposite direction one turn.

6. To provide positive sensing of the Drop Count Switch (L) --

The DCT switch should "break" when a form is fed to the transport mechanism.

To adjust, turn adjusting screw until switch "breaks" and then turn screw in opposite direction 3/8" of a turn.

7. To ensure that the forms enter the feed rollers squarely --

The feed table should be square with the knurled feed roller N.

To adjust, loosen the four mounting screws E and position the table as necessary.

STRIPPER PLATE ASSEMBLY - Figure VII-7

There are two stripper plate assemblies mounted on the feeder scale bar and each contain one stripper finger. The stripper fingers prevent feeding more than one form.

Tests and Adjustments

1. To provide maximum efficiency of the stripper finger --

a) The horizontal projection of the finger (B) should be 1/32" above the top window slot in the bracket (A).

b) The forward vertical surface of the finger should contact and be parallel to the bracket and the horizontal projection should be perpendicular to the bracket.

To adjust, a) loosen screw and position finger as required. b) weave seperator finger as required.

2. To prevent double feeding of forms and to allow the center of the form to "float" --

The stripper assemblies should be located on the scale bar with their edges aligned with 24 and 64 respectively.

To adjust, position as necessary.

VACUUM YOKE ACTUATING MECHANISM - Figure VII-8

The feed clutch engages when the clutch solenoid is picked. When the driven member of the clutch rotates, it rotates the geared pulley which drives belt N to turn crankshaft M. This causes crankshaft M to rotate 360°. As crankshaft M rotates, it drives link K which in turn drives cam J causing it to pivot on a stud in the feeder sideframe.

As crankshaft M rotates from 0 to 90 degress, it causes cam J to rock counter-clockwise and roll I on arm H will be pulled down by the slot in the cam. As arm H is lowered, it causes the vacuum yoke B to be lowered to contact the top form in the hopper.

As the crankshaft M rotates from 90 to 180 degrees, link K causes cam J to rock clockwise to its normal position. As cam J rocks, roll I on arm H is lifted by the slot in the cam. As arm H is lifted, it rotates shaft D and causes arms E to lift the vacuum yoke shaft assembly C. As the vacuum yoke B is lifted, it picks up the top form.

As the crankshaft rotates from 180 to 270 degress, cam J continues to rock clockwise. Cam S, being fastened to cam J, oscillates also and will cam roll G and cause arm F to rotate shaft C and rock the vacuum yoke toward the feed rolls. As the yoke moves the form horizontally, it inserts the form into the feed rolls which feed it into the machine.

As the crankshaft rotates from 270 to 360 degrees, the cams are rocked counter-clockwise to their home position. As cam S rocks, it allows the vacuum yoke to be rocked away from the feed rolls to its normal position.

Tests and Adjustments

1. To provide immediate movement of feed cam when the feed clutch is engaged --

With the feed clutch held disengaged by the clapper of the clutch solenoid and the spring removed from the detent R on cam J, the cam should be manually rocked counter-clockwise until it is limited by the feed clutch spring. In this position, the upper right projection of detent R should be directly beneath the center of roll I.

To adjust, mesh belt N with crank pulley M to bring cam J into approximate position, then move link K through screw L as required.

2. To provide positive insertion of form into feed rolls --

With crankshaft M rotated 90 degrees, there should be 1/2" between the lower edge of the vacuum yoke and the separator plate assembly.

To adjust, loosen screw A and position yoke as necessary.

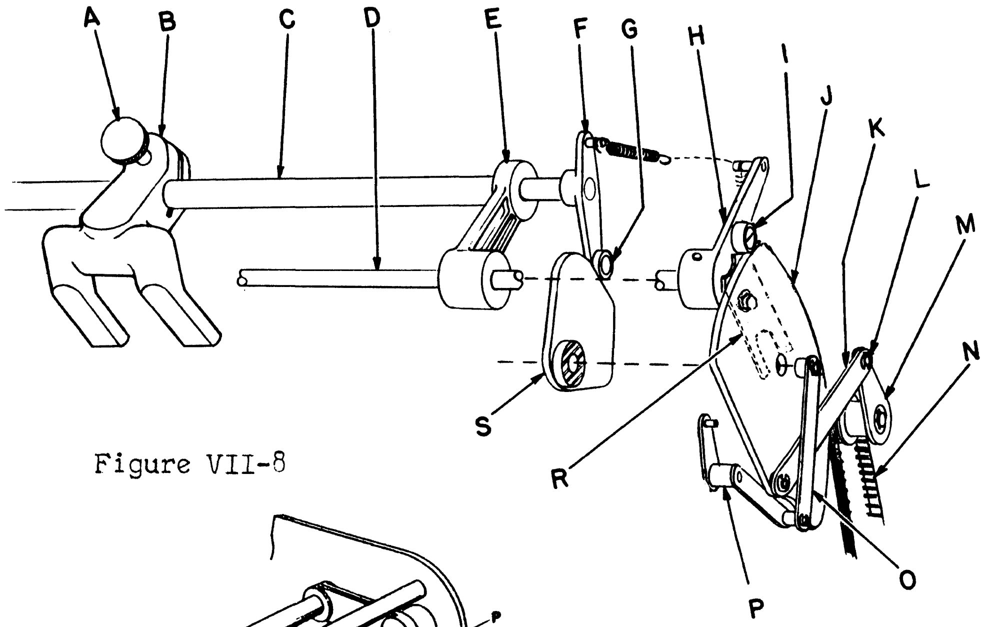
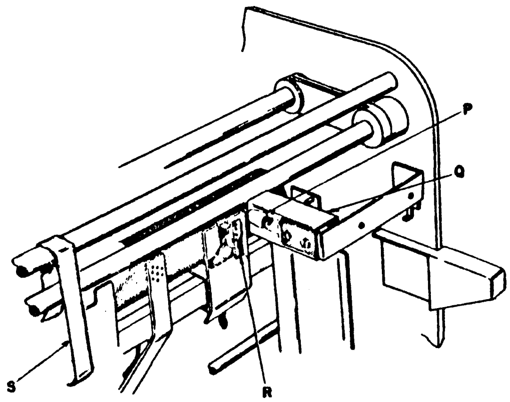


Figure VII-8



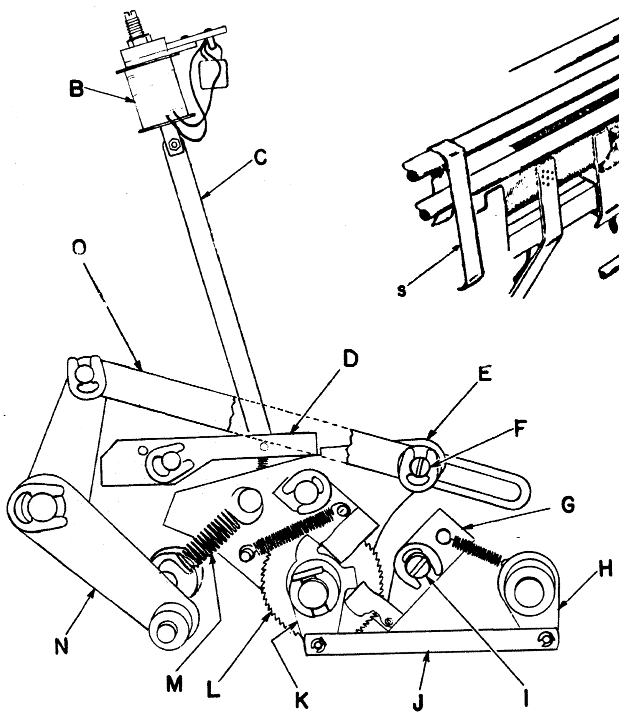


Figure VII-9

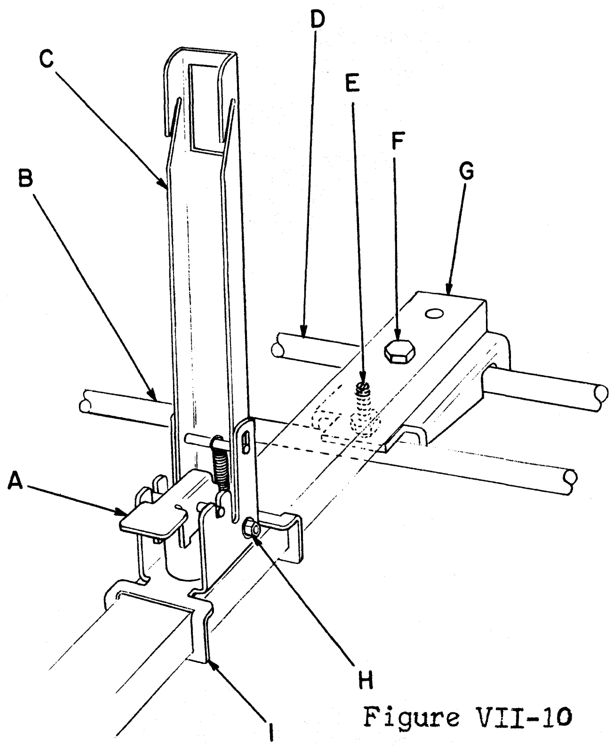


Figure VII-10

FEED HOPPER ELEVATING ASSEMBLY - Figure VII-9

The feed hopper elevating assembly elevates the feed hoppe 1/16" when the top form in the stack is sensed at pre-determined level. The sensing mechanism consists of lamp P, light sensitive photo cell R to control the circuit which picks solenoid B. The table lifting mechanism is actuated by the feed cam through a link from the feed cam to bellcrank N.

If the solenoid is energized, it actuates pawl D which allows spring M to rock ratchet pawl assembly E counter-clockwise one tooth space of ratchet L.

As the crankshaft rotates from 90 to 270 degrees, solenoid B is dropped which allows pawl D to drop back to its normal position in order to detent ratchet pawl assembly E after it is actuated. The large feed cam actuates bellcrank N through a link. As the bellcrank rocks clockwise, it drives link O which rocks ratchet pawl assembly E one tooth space of the ratchet. Detent pawl G drops into the next tooth space to hold the ratchet. Pawl D drops behind the step in the ratchet assembly.

As the crankshaft rotates from 270 to 360 degrees, the cams rock counter-clockwise to their normal position.

When the feed table release lever is operated, it rocks arm H clockwise which, through link J, rocks arm K and its projections release the pawls holding the ratchet and allow the table to drop.

Clip S stabilizes narrow forms (Stubs) on machines with photo cell sensing and prevents forms raising above the stripper fingers as the yoke picks up the top form.

Tests and Adjustments

1. To allow pawl D to restore properly --

With the latch disc E in its extreme driven position, there should be .008" to .012" clearance between the end of pawl D and the step of latch disc E.

To adjust, turn eccentric F as required keeping high side of bearing up.

2. To allow pawl G to latch ratchet L --

With latch disc E in its extreme driven position, there should be .010" clearance between the face of the detenting tooth of ratchet L.

To adjust, adjust eccentric I as required keeping the high side down.

RIGHT FORM SUPPORT AND GUIDE - Figure VII-10

The right form support and guide assembly slides on bar G which is mounted on two cross braces of the feeder frame with bolt F. Guide C may be moved horizontally by lifting detent lever A which allows the guide to slide on bar G. Guide C may be lifted slightly and tilted away from the feeder to allow easier insertion of forms in the feeder. After placing forms in the feeder, the operator should raise the feed table until the top form is level with the form level indicator, then the guide should be moved until there is minimum clearance between it and the top form in the feeder.

Tests and Adjustments

1. To locate bar G in relation to feeder table --

Bar G should be level with and centrally located between the cutout in the feed table support bracket.

To adjust, loosen bolt F and shift bar G horizontally. Turn screw E up or down to level bar G. Tighten bolt F.

2. To allow clearance of forms with lower portion of guide C --

With a square placed on bar G and against guide C, there should be 3/16" clearance between the square and the bottom of guide C.

To adjust, move stud H in bracket I as necessary.

IDLER AND DRUM CONTROL ASSEMBLY - Figure VII-11

The idler rolls, drum and high speed rolls are used to transport the form from the Ready Station to the Receiving Stacker. When the form is in the Ready Station, its lower edge is approximately 1/4" beneath the idler rolls.

When solenoid F is energized, its plunger pulls link H forward tripping cam E which releases arm assembly C. Spring B pulls idler assembly forward causing rollers A to limit on the drive drum Q.

The formed lower arm K of the idler assembly releases the tip of spring J which allows the spring to uncoil and tighten around the inner clutch members. This will cause the complete clutch assembly L to rotate with the drive drum.

As the idler assembly is lowered, the lower formed ear N interrupts the solar cell M light source This is used as a signal to the electronic logic that a form is starting to be fed from the Ready Station.

After the form has traveled approximately six inches, cam I contacts a roller on the idler assembly and raises it which allows spring D to rock the cam E under the raised assembly. As the drum continues revolving the lower arm K contacts the spring clutch ear disengaging the clutch which prevents the clutch assembly from rotating with the drum.

Tests and Adjustments

1. To retain the idler, drum and high speed roll shafts in the machine --

The bearings for the idler down shaft, the drum roll shaft and the high speed shaft should be securely held in place when the hooks such as P, on the end of the idler down shaft and the left end of the drum roll and high speed roll shafts,

are wedged 1/2 to 3/4 the length of their camming surfaces over them.
To adjust, turn the eccentric in the hook.

2. To eliminate the effect of residual magnetism in the idler down solenoid --
The collar G should limit the plunger of the idler down solenoid .010" before the plunger bottoms in the solenoid.
To adjust, loosen the set screw in the collar G and manually bottom the plunger. Move the collar to limit against the solenoid bracket and snug the set screw. Pull the plunger out slightly and place a .010" gauge between the collar and bracket and push plunger in until it limits on the gauge. While holding plunger securely, remove gauge and loosen set screw. Then move collar on the plunger until it limits on the bracket and tighten the set screw.

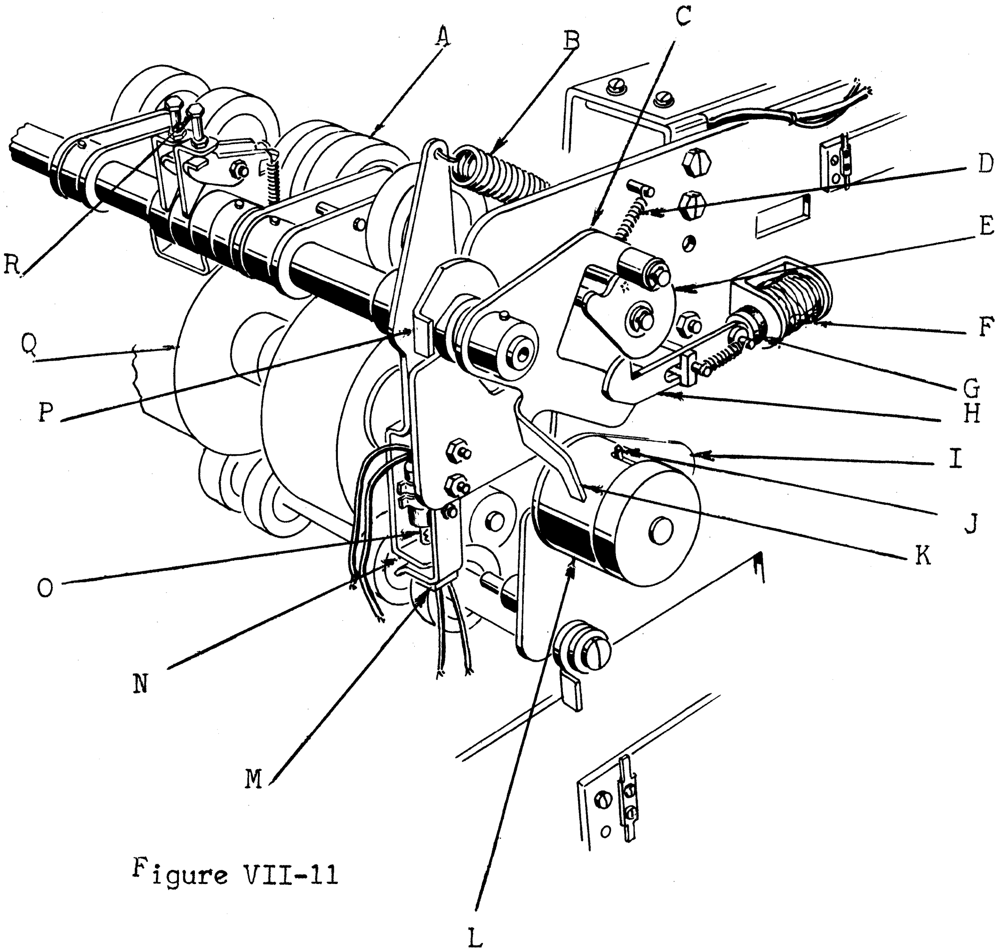


Figure VII-11

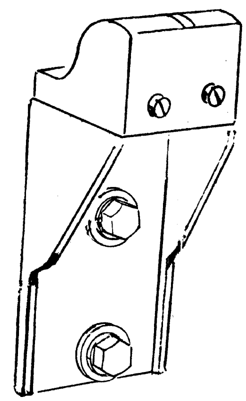


Figure VII-12

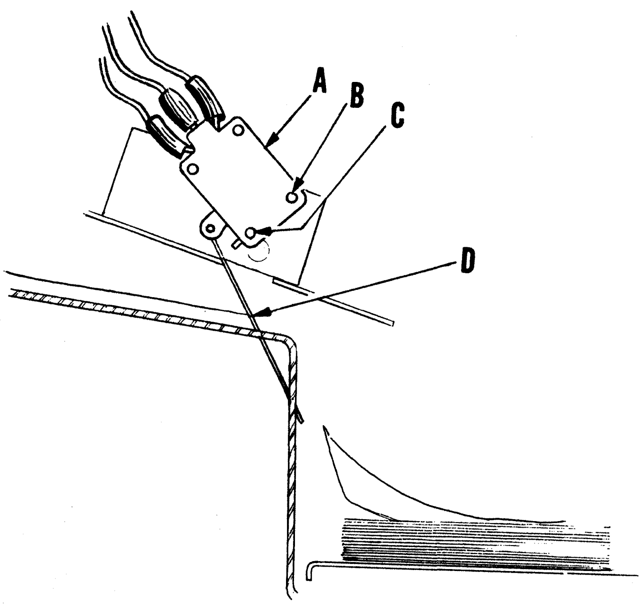


Figure VII-13

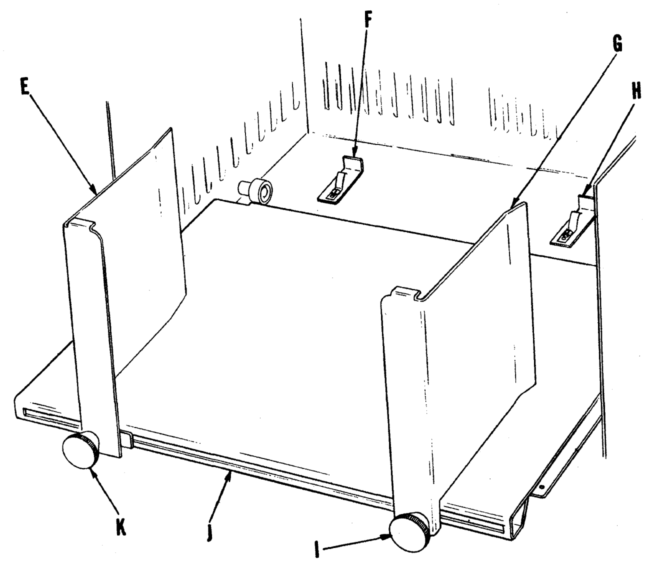


Figure VII-14

READ HEAD - Figure VII-12

The read head is used to read the forms only and is mounted between the two sections of the drum. As the form leaves the ready station it passes over the read head which reads the magnetic data and transfers this to the Auto Reader Read Amplifiers.

RECEIVING STACKER - Figure VII-14

The receiving stacker is the receptacle for the forms after they have been read. As the form leaves the high speed rolls and passes through the stacking chute to the tray in the stacker, it actuates the bin jam switch. If the form does not clear the chute, it keeps the bin jam switch transferred and prevents any further operations.

As the form leaves the chute, it should strike the front of the receiving stacker and settle to the bottom of the bin without interference.

Test and Adjustments

1. To provide an indication of a form jam in the stacking chute --
The bin jam switch "A" should "make" before a form moves its actuating arm D out of the slot in the rear of the stacking bin.
To adjust, loosen screws B and C and position switch A as necessary.

2. To provide proper clearance for the forms in the stacking bin --
With the receiving tray J latched in the detents F and H, there should be 1/32" to 1/16" play between the form and the back of the bin.
To adjust, snug detents F and H in their forward position, insert receiving tray and force detents to rear as required. Remove receiving tray and tighten detents.

3. To prevent interference by the stacking guides as the forms enter the stacking bin --
The form should enter the stacking bin squarely without interference by stacking guides E and G and all forms but 3" stubs should have 1/32" side play between the guide when lying in the bottom of the tray. Three inch stubs may have as much as 1/4" side play.
To adjust, loosen screws I and K and move guides as necessary.

POWER SECTION - Figure VII-15

Electrical power for the A4002 is upplied by the E2150 Electronic Bookkeeping Machine. 107 to 127 VAC, 60 cycles, is required to run the motor.

Mechanical power is furnished by the 1/3 H.P. inductive type motor which is coupled to a transmission by a V belt. The transmission furnishes power to the feed rolls, conveyor assembly, and high speed drive rolls continually through geared pulleys and Gilmer belts. The transmission also furnishes power through a solenoid-controlled spring clutch to the feeder. The clutch is coupled to the feeder by geared pulleys and Gilmer belts. The transmisson also furnished power to rotate the drive drum at a constant speed by geared pulleys and a Gilmer blet.

The vacuum pump is coupled to the motor by a V belt, and operates any time the motor is running, the pump is a rotary vance type protected from dirt by two filters, one on the intake and one on the exhaust. Both the intake (vacuum) and the exhaust are used in the feeder to assist feeding the forms.

THE FEEDER - Figure VII-16

The feeder is operated by a large cam which is caused to oscillate by a crank shaft which is coupled to it by a connecting rod. The crank shaft is coupled through a Gilmer belt to the feed clutch on the transmission assembly. As the cam oscillates, it causes the vacuum feed yoke to be lowered and its feet to contact the top form in the feeder. The vacuum then holds the form against the feet of the yoke when the yoke is lifted. As the cam completes its oscillation, the vacuum feed yoke will lift the top form and advance it to the feed rolls. The yoke will then return to its normal position.

A table elevation photo cell senses the level of the top form in the feeder, prior to the lowering of the vacuum yoke. If the level of the top form is low, a solenoid is energized which allows the feed table elevating mechanism to raise the table 1/8" during the feed operation.

The exhaust from the vacuum pump is directed between the forms from each side and the front by three tubes containing holes to direct the air. This causes the forms to riffle and aids in their separation during feeding.

CONVEYOR SYSTEM - Figure VII-17

After the form is fed into the feed rolls, they advance it into the conveyor system. The conveyor is comprised of two belts driven by the feed rolls and moving over the top of a steel table. There is a row of steel balls held loosely on each belt, and as the form enters the conveyor, it is held against the conveyor belts by the steel balls. The form then advances on to the Ready Station, where it is held by a metal limit and the belts slip beneath it. When in the Ready Station, the form covers two solar cells which allow the idler rolls

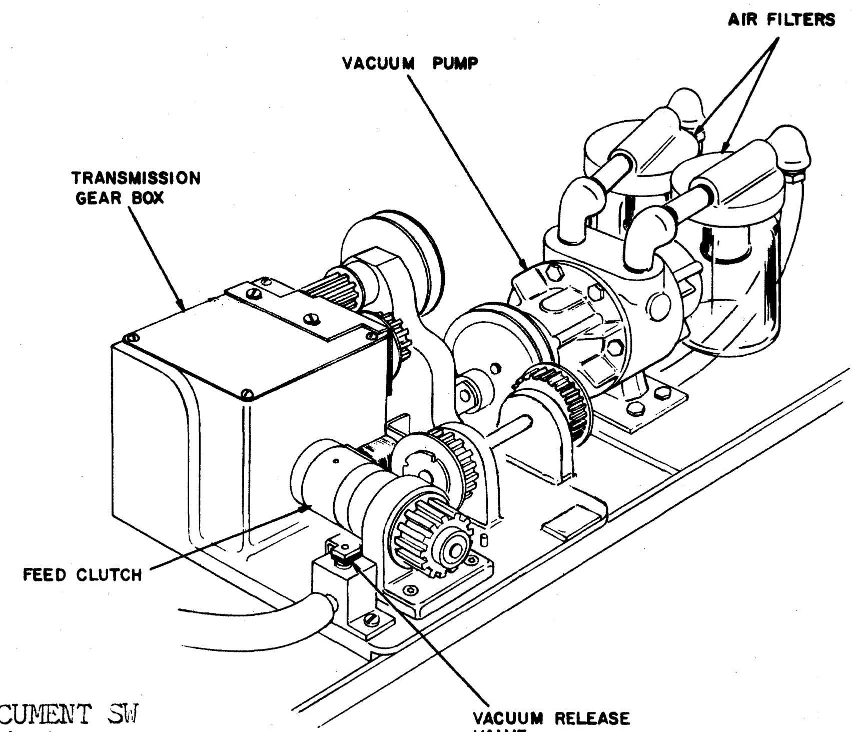


Figure VII-15

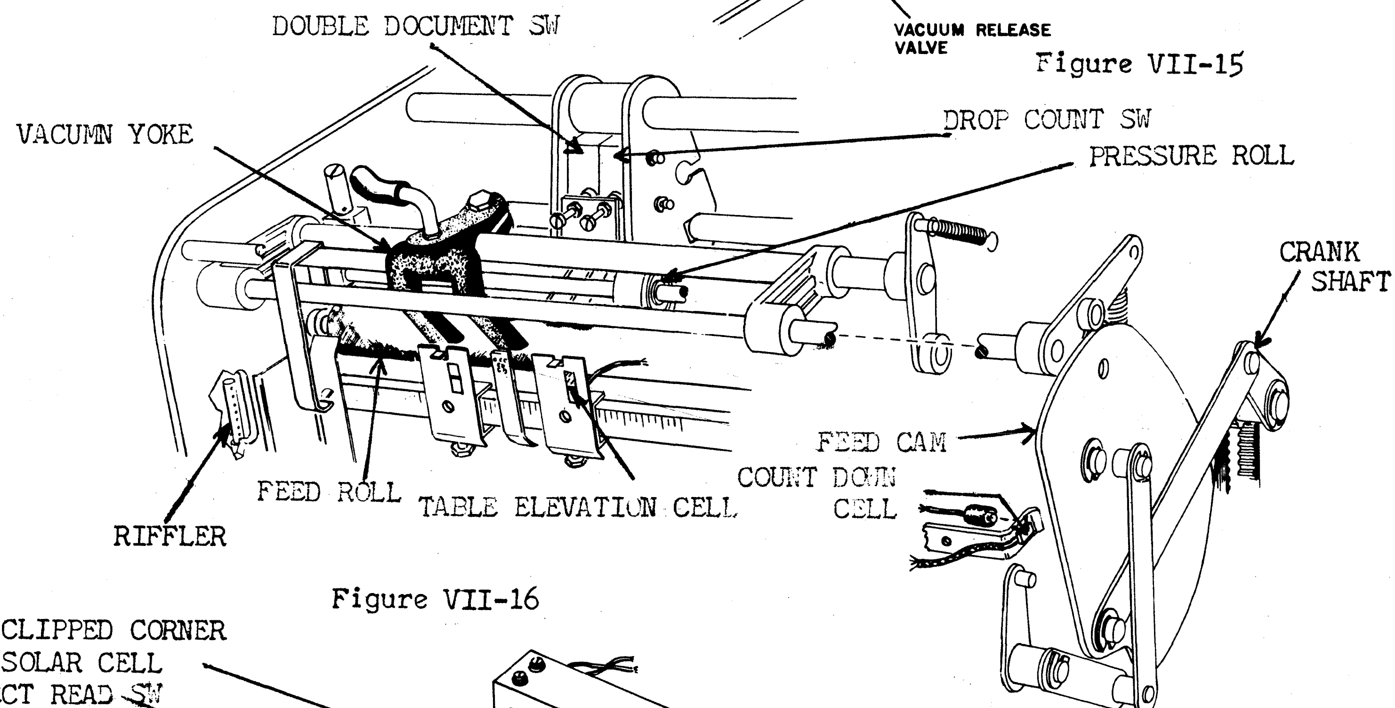


Figure VII-16

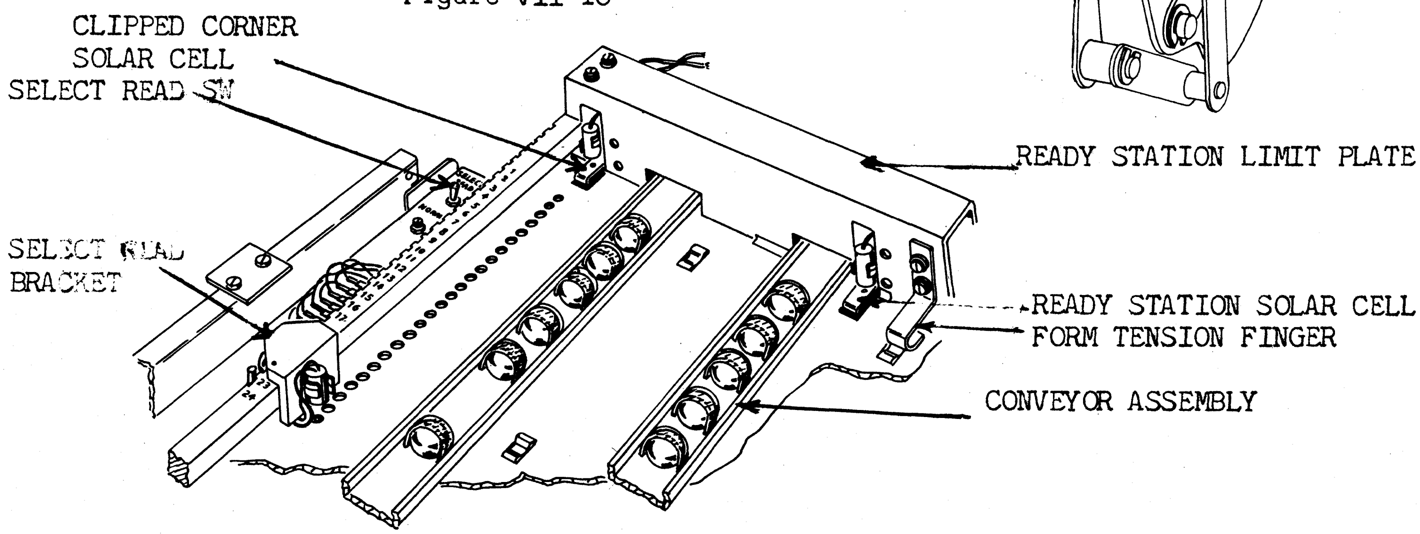


Figure VII-17

to drop. The lowering of the idler rolls causes the form to start into the drive drum assembly and also causes the feed clutch to pick and start another feed operation.

READY STATION - Figure VII-17

As the form comes into the Ready Station, it contacts the form limit plates to align the magnetic stripes with the read heads. The form squares itself as it contacts this limit and also covers two solar cells. It always closes the Ready Station Align cell which given the signal that a form is in the Ready Station and ready to be read. If the form covers the clipped corner cell, it indicates it is to be read and activates a signal to start read after the form moves $\frac{1}{4}$" over the read heads. If the form has the upper right corner clipped off, it does not cover the clipped corner solar cell, indicating the form should not be read as it passes over the read heads.

While in the Ready Station, the form is $\frac{1}{4}$" over the drive durm and read head and also $\frac{1}{4}$" under the idler rolls.

IDLER ROLLS - Figure VII-18

The idler rolls are used to cause a form to feed from the Ready Station into the high speed rolls and then to the receiving hopper.

As the Ready Station signals a form ready, the Idler down solenoid picks and drops the idler rolls. These rolls hold the form against the drum and read heads and are raised by a rotating cam on the end of the drive drum shaft.

The idler down assembly, when lowered, blocks a sp;ar ce;; wjocj caises a delayed pulse to pick the feed clutch. This starts another form into the ready station as the drive drum is feeding the active one out.

DRIVE DRUM ASSEMBLY - Figure VII-19

The drive drum assembly is comprised of a split, rubber covered metal drum with a spiral spring type clutch attached to the end of the shaft. This drum clutch is controlled by the idler down solenoid. When the solenoid is energized the idler rolls are lowered to the form. The solenoid also trips a clutch which causes a idler reset cam to revolve with the drum. This cam resets the idler down roller assembly after the form has been driven over the read heads. The read heads are located between the two sections of the drum.

When the idler rolls are lowered, the form in the Ready Station is driven over the read heads approximately "$\frac{1}{4}$", at which time the start read signal is made high by the CC/ST RD solar cell. The form is read and passes around the drum into the high speed rolls. The sync pulse on the form controls the stopping of the read in the same manner as the E2150.

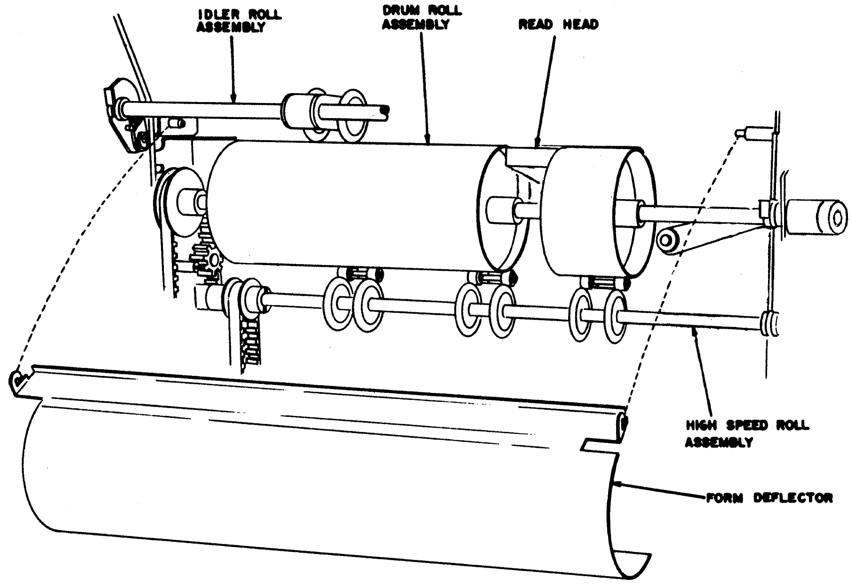


Figure VII-19

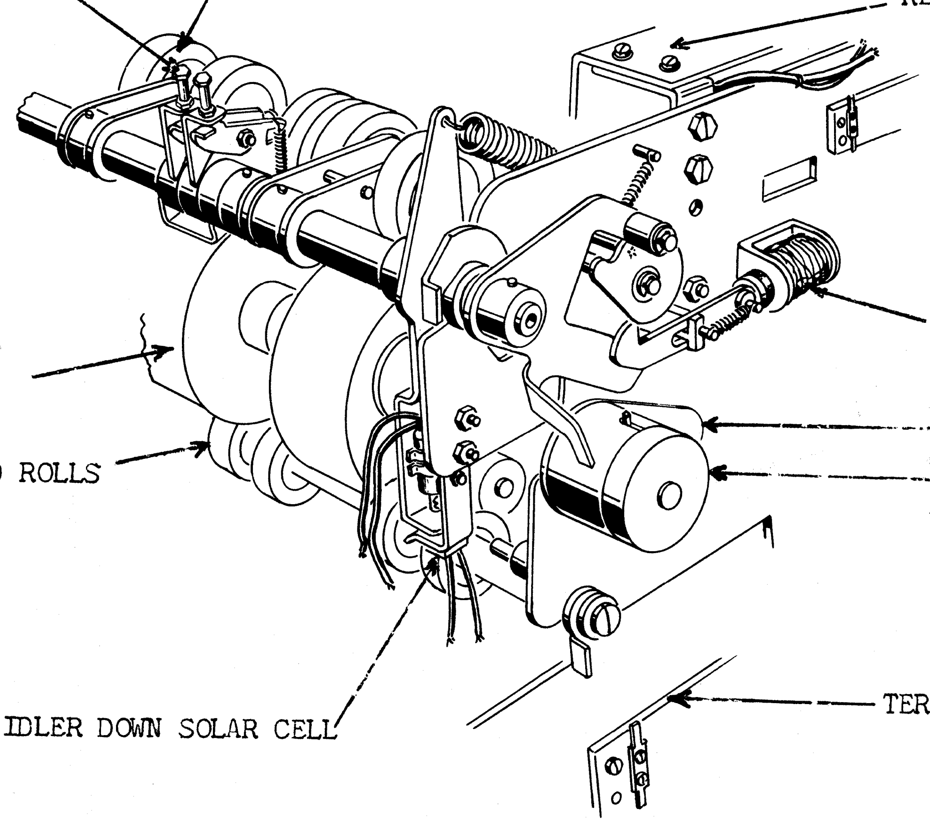


Figure VII-18

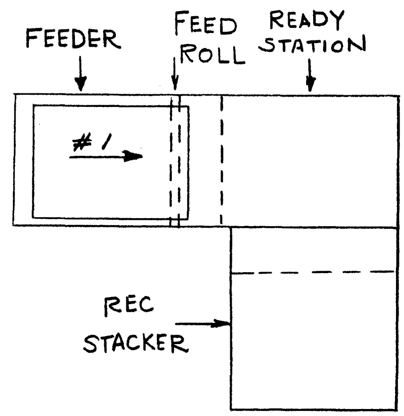
HIGH SPEED ROLLS - Figure VII-19

The high speed rolls are directly beneath the drive drum and consist of eight rolls on a shaft driven continually by the transmission. Each of the driven rolls has a pressure roll above it to hold the form against it.

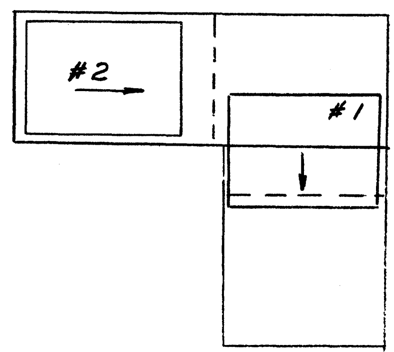
The form enters the high speed rolls before the idler rolls are lifted, therefore, the high speed rolls must slip on the form until the idlers are lifted. As the idlers are lifted, the high speed rolls take over and increase the speed of the form from 15" per second to approximately 62" per second.

As the form leaves the high speed rolls, its momentum carries it into the output stacker where it strikes the front of the receiving tray and settle before the next form enters.

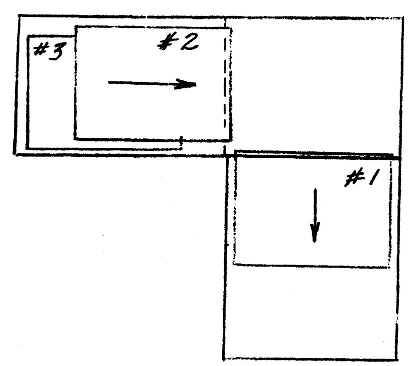
BASIC FORM TRAVEL AND TIMING



When a start feed switch is depressed, the top form (#1) in the feeder is picked up and inserted into the feed rolls where it actuates the drop count switch to stop the feeder. After passing through the feed rolls, the form is conveyed to the Ready Station where it is aligned for reading and actuates the Ready Station solar cell and the Clipped Corner solar cell.



As form #1 starts out of the Ready Station, the feeder begins another feed operation to feed the next form (#2) to the Ready Station. The Start Read solar cell is actuated and begins the Read operation as the form moves approximately $\frac{1}{4}$" out of the Ready Station. When form #1 is half out of the Ready Station, form #2 is just passing into the feed rolls.



When the form #2 is approximately 1" under the feed rolls, form #1 has moved approximately $6\frac{1}{2}$" out of the Ready Station. The high speed rolls take control of the form and drive it into the Receiving Stacker. As form #1 completely clears the Ready Station, form #2 is just entering it and continues on to the Ready Station.

POWER ON AND OFF SEQUENCE

The auto reader receives its entire power from the cable connected E2150. The safety switch S4106, actuated by the case lid, must be closed to allow the Auto Reader to be started.

Depression of the S4101 On-Off push button switch supplies -100 volts to pick the Control Relay K4201, thru N.C. POR contacts 21-22. The On-Off Switch is a latch-type switch. A second depression is necessary to release it.

The Control Relay has the following functions:

1. Contacts 2-3 supply the 115 V.A.C. to operate the fan.
2. Contacts 4-5 are not used.
3. Contacts 6-7 supply ground to the ground buss.
4. Contacts 8-9 supply the +15 V.D.C. to the back plane distribution buss.
5. Contacts 21-22 supply a hold circuit to the control relay from the -56V. This hold circuit thru POR contacts 25-26 will hold the control relay until after the POR has had a chance to drop out during the Off sequence. The -100 is thus removed ahead of the bias voltages, and the AR Power On signal is low before any other logic signals change. Stray turn off noises and false signals are gated out of the E2150 with the AR Power On signal.
6. Contacts 23-24 supply the -100 volts to pick the Motor Relay K4202, and the POR Relay K4203. The Motor Relay supplies the A.C. voltage to operate the motor.
7. Contacts 25-26 supply the -4.25 V lamp voltage to Selective Read and Table Elevation lamps.

8. Contacts 27-28 supply the -15 V.D.C. to the back plane distribution buss.
9. Contacts 29-30 supply the -4.25 V.D.C. to the back plane distribution buss.

Picking of the POR Relay has the following functions:

1. Contacts 2-3 cause the POR reset pulse to go to ground. This allows logic to control the Flip Flops.
2. Contacts 4-5 supply +15 V to four solar cell lamps.
3. Contacts 6-7 supply -100 V to the solenoid coils and back plane.
4. Contacts 21-22 open the pick path to the control relay.
5. Contacts 25-26 supply the hold circuit to the -56 V. (Refer to #5 of Control Relay Functions.)
6. Contacts 27-28 allow the AR Power On signal to come high. This signal is gated to the E2150 to suppress the setting of the Prog Cam FF during an Auto Reader Trial Balance.

CLOCK

The A4002 contains its own independent clock. It is the same type clock as used in the E2150, and is used for logic control of the Auto Reader circuits.

AR READY SIGNAL

The Auto Reader ready signal consists of the output of either the Start Read (ST RD) or Count Down (CT DN) solar cell amplifiers. One of these signals is always high, therefore, the AR Ready signal will be high as long as there is power to the solar cell lamps.

The AR ready signal is fed to the set gates of the Single Feed (SF) and Auto Feed (AF) Flip Flops. These Flip Flops control the Feed Flip Flops, therefore, until the solar cell lamps have had time to illuminate, and gain control of their amplifier, no form feed can take place.

SINGLE FEED

This is to describe a normal single feed operation with no form in the ready station.

Depression of the Single Feed Switch (S4103) will cause a relay wetter output to go to ground. This high signal is gated with NOT AFFF·NOT DDFF·AR Ready to set the SFFF with the next clock pulse. The SF signal will also reset the Stop FF if it had previously been set. See Figure VII-21.

Setting the SFFF causes the following events to occur:

1. The next clock pulse sets the Feed FF through the AND Gate: NOT STOPFF· $\overline{\text{C2FF}}\cdot\overline{\text{RSTAFF}}\cdot$SFFF.
2. The Feed Solenoid driver energizes the Feed solenoid which releases the Feed Clutch.
3. The Feed Clutch causes the Feed Cam to oscillate and pick up a form from the table.
4. Oscillation of the cam assembly causes the Count Down (CT DN) solar cell to be blocked. The CT DN SCA output goes to -4. This inverted signal will set the Count One (C1) Flip Flop when the cam arm starts its return stroke.
5. Further oscillation of the cam assembly causes the form to be injected into the feed platen and on into the ready station.

6. As a single form enters the ready station, being driven by the feed platen, it closes the roller actuated Drop Count (DCT) switch.
7. The DCT switch and clock will reset the Feed FF which causes the Feed Solenoid to de-energize and disengage the spring clutch after one complete revolution.
8. The DCT and SFFF and clock will set the Stop FF. Setting the Stop FF inhibits the set AND gate to the Feed FF. This prevents feeding a second form while the first one is traveling to the ready station. The Stop FF will be reset by a 15 usec pulse when the form reaches the ready station limit, and the Ready Station Align FF sets. Stop is reset at this time to prevent the Stop Feed lamp from illuminating. When the RSTAFF comes high, it will inhibit the set Feed AND Gate before the Stop FF resets.

   The DCT Signal and clock also reset the C1FF. See Figure VII-21.
9. See Figure VII-22. As the form reaches the Ready Station limit, it blocks the RSTA and clipped corner (CC) solar cells. The SCA outputs go from ground to -4 V as the form blocks them.

   The RSTA SCA output is inverted and the next clock pulse sets the RSTAFF. The CCFF will not set due to the NOT SEL+CC signal being low at this time. NOT SEL+CC is low because ST RD is low from the CC SCA output.
10. See Figure VII-23. With RSTAFF high the form is now ready to be fed around the drum and be read by the read heads.

    An Auto Reader Control (AR Control) signal is needed from the E2150 before the form can be fed from the Ready Station. AR Control is a signal indicating the E2150 is ready to accept information. It is comprised of: NOT BC·NOT PDFF·CC3·(ARP ON·FL).

11. The NOT IDN·RSTAFF·SFFF· (NOT ERFF·NOT LOCK·AR CONTROL) bring the Drop I signal high. This signal causes a solenoid driver to energize the Drop I solenoid.

12. Energizing the Drop I solenoid causes the idler roller assembly to be unlatched. A spring then lowers the assembly and Idler rolls to limit on the form. When the assembly is lowered, an arm blocks the IDN solar cell making its SCA go to -4 V. The IDN signal is the inverted SCA output. See Figure VII-22.

    The Drop I solenoid also causes a spring clutch to be released which allows a restoring cam to rotate with the drum assembly. This cam will raise the idler assembly and a latch will latch it in its raised position. The latch is controlled by the solenoid plunger. The solenoid will be de-energized at this time due to the low NOT IDN signal inhibiting the Drop I signal AND Gate.

13. The IDN·RSTAFF signals will cause the SFFF to reset with the next clock pulse.(FIG 21)

14. With the idler rolls on the form, the form starts moving around the drum, over the read heads. After the form has moved $\frac{1}{4}$", the CC ST/RD solar cell is unblocked. This causes the SCA output to go from -4 V to ground bringing the ST RD signal high.

15. See Figure VII-23. The high ST RD·IDN·NOT CCFF signals are fed into a pulse standardizer to produce a positive pulse 15 usec in width. The

output of this gate called Start Read, is gated to the E2150 to set the Read Ledger (RL) FF if the carriage is in a Read Ledger programmed position.

16. See Figure VII-24. The ST RD·RSTAFF·NOT CCFF signals are gated with the output of the X and Y Read Amplifiers. The information received from the Auto Reader Data X and Data Y read amplifiers, is handled by the E2150 in the same manner as information received from its own Read heads. Reading of pulses will continue until FF16 sets, the same as E2150 logic. At this time, the RLFF will reset.

17. See Figure VII-22. As the form continues to feed around the drum, it will unblock the RSTA solar cell. When this happens, the SCA output goes from -4 to ground. This signal and the next clock pulse will reset the RSTA FF. Resetting the RSTA FF inhibits the data X and data Y read gates.

18. The form travel continues into the high speed rolls where its speed is increased and it is ejected into the receiving tray ending a Single Feed Operation.

AUTO FEED OPERATION

This is to describe a normal auto feed operation, starting with no form in the Ready Station.

Depression of the Auto Feed switch S4102 will cause a relay wetter output to go to ground. See Figure VII-21. This high signal called AF will cause:

The AFFF to set by the AF·AR READY·NOT STOPPFF·NOT DDFF and CLK.

The SFFF to set by the AF·NOT AFFF·NOT DDFF·AR READY and CLK.

The SFFF is set to cause the first form to feed. Thereafter, form feed will occur from a delayed I DN signal.

The STOP FF to be reset if it had been previously set.

Setting the AFF and SFF causes the following events to occur:

1. The next clk pulse sets the Feed FF through the AND GATE: NOT STOPFF· NOT C2FF·SFFF·NOT RSTAFF.

2. The Feed Solenoid driver energizes the Feed solenoid which releases the Feed Clutch.

3. The Feed Clutch causes the Feed Cam to oscillate and pick up a form from the table.

4. See Figure VII-22. Oscillation of the cam assembly causes the count down (CT DN) solar cell to be blocked. The inverted output of the SCA and the Feed FF signal will cause the CIFF to set as the arm starts its return stroke.

5. See Figure VII-21. The AFFF and CIFF signals are gated together to reset the SFFF with the next clk pulse following setting of the CIFF. Resetting SFFF at this time prevents setting the STOP FF on this first cycle of Auto Feed.

6. Further oscillation of the Cam assembly causes the form to be injected into the feed platen and on into the Ready Station. As a single form enters the Ready Station, being driven by the feed platen, it closes the roller actuated Drop Count Switch.

7. The DCT switch and clk will reset the Feed FF which causes the Feed solenoid to de-energize and disengage the spring clutch after one complete revolution.

See Figure VII-22. The DCT switch and clk will reset the CIFF.

8. As the form reaches the Ready Station limit, it covers the RSTA and CC solar cells. The low RSTA SCA output is inverted and the next clk pulse sets the RSTAFF.

The CC FF will not set due to the NOT SEL + CC signal being low at this time.

9. With RSTA FF high, the form is ready to be fed around the drum and be read by the read heads.

See Figure VII-23. AR control is a signal indicating the E2150 is ready to accept information.

10. The NOT IDN·RSAFF·AFFF· (NOT ERFF·NOT LOCK·AR CONTROL) bring the Drop I signal high. This signal causes a solenoid driver to energize the Drop I Solenoid.

11. The Idler assembly is dropped in the same manner as single feed and causes the IDN solar cell AMP to produce, through an inverter, a high I DN signal.

12. The low IDN signal causes the Drop I signal to return to -4 allowing the Idler solenoid to de-energize. This will allow the Idler assembly to be latched up as the drum completes one cycle.

13. See Figure VII-21. The IDN signal is fed into a DMV. This DMV will produce a 15 usec positive pulse after an 80 ms delay. This delayed pulse together with AFFF·RSTAFF will set the Feed FF. Thus, another form is starting to be fed as the active form is being fed around the drum on its way to the receiving hopper.

14. The Start Read signal and subsequent reading of the information from the form stripes is the same as explained in Single Form Feed.

15. See Figure VII-22. As the form thats being read clears the paper pan, the RSTA SCA is unblocked. This high signal and clk will reset the RSTA FF.

The idlers reset after this occurs and the Drop I signal must wait for a new form to set the RSAFF. Once this happens, idlers drop and the cycle continues as before.

16. Automatic feeding and reading of forms will continues until the AFFF is reset.

BALANCE TRANSFER OPERATION

This operation using both the E2150 and the A4002 requires the following special programming.

Lane 56 and 52 (BC) are programmed for the Blank Card control of the E2150.

Lane 54 (FL) is programmed for the Feed Ledger control of the Auto Reader.

Lane 66 (RL) is programmed for the Read Ledger control of the E2150.

The E2150 is used to accept a blank form where the transferred amounts are printed on the Balance Forward line.

The A4002 is used to read the encoded amounts from the existing forms and place this information into the E2150 memory storage.

Operation: Figure VII 20.

There are two basic functions, one dependent on the other, that must occur on this operation.

One is the reading of the forms in the Auto Reader. The read takes place as the form feeds from the Ready Station, therefore, a Drop I signal must be received to initiate form movement from the Ready Station. The Drop I signal is inhibited until the E2150 carriage cam shaft reaches 95° and sets the REV and Paper Drive FF's.

The other function is the Blank Card form handling in the E2150. This is controlled by the Program Cam Shaft, which is inhibited until the Prog FF sets.

The Prog FF is in turn inhibited until a form is in the Ready Station of the Auto Reader, making the Ledger Ready signal high.

With the carriage in a proper programmed stop and the Auto Reader turned on, the Auto Feed switch is depressed. A basic feed takes place until a form is fed into the Ready Station. At this time, the Drop I signal cannot come high because the AR control signal is low. The AR control signal is waiting for the Reverse and Paper Drive FF's to set. The Auto Reader will remain in this condition until a form is fed into the E2150.

Next a form is inserted into the E2150 carriage throat. The (FPS·CC3·NOT ERFF·NOT LOCK) and Ledger Ready sets the Program Cam and Blank Card FF's and a Blank Card procedure is started.

At 95^{o} of the Prog Camshaft cycle, the CC2 will set the Rev FF. 100ms later, the PDFF will set allowing the AR control signal to come high. This in turn brings the Drop I signal high, causing the idlers to be lowered and the form in the Auto Reader Ready Station to be read. Both forms are now moving at the same time.

The form in the Auto Reader is read with its information placed into the E2150 memory. Data that was read is now in MA 20/30, and accumulated data due to block add is in MA 30/60·70. 80ms after the idlers drop another Auto Reader feed cycle begins, feeding another form into the Ready Station. This form will not be fed from the Ready Station until the next time the REV FF is set at 95^{o} of the Program Cam Shaft.

The form in the E2150 is fed to line -8 and out again to line #1. At this time, all form travel has stopped and the Printer Operate FF is set. A 100ms pulse, triggered from POFF will cause the MB #2 solenoid to pick. The drive trip shaft then closes switch S770 to pick the Printer Trip Relay K914. Contacts 4 and 6 supply a high signal to set the Printer Trip FF. Contacts 1 and 2 remove the +35V from the keyboard wetting circuit. Contacts 1 and 3 supply the hold circuit for the +35 sense relay K1102.

If Verify is not programmed, the tappets will fire and the printer will operate and print the desired number of balances on the form. The printer will then cycle into a write ledger mode where the form will be written using the E2150 memory data.

If Verify had been programmed by pinning lane 58, the firing of the tappets would have been held up until after the verification logic finished. This would be accomplished by the Verify signal. NOT ERFF·SET POFF signal setting the Verify FF. Verify FF in turn causes the lock solenoid to pick opening the tappet pick circuit. The Motor Bar 2 solenoid would pick causing the drive trip shaft to close switch S770. This in turn picks PT relay (K914) and contacts 4-6 set the PTFF·(PTFF·VFF·POFF) cause FF6 to set and the Verification logic begins. 600 usec later, if a good verification was received, the VFF resets. This is turn resets lock and the tappets can fire.

The cycle will start again when a ledger is placed in the E2150 carriage throat.

At the end of the Balance transfer operation, the accumulated totals can be printed from MA30 on single stripe and MA60 and 70 on Dual Stripe machines.

TRIAL BALANCE

This operation using both the E2150 and A4002 requires the following special programming: Lane 56 and 54 (FL) are programmed for the Feed Ledger

Control of the Auto Reader.

Lane 66 (RL) is programmed for the Read Ledger Control of the E2150.

The E2150 is used to accept and store information received from the A4002 read amplifiers.

The A4002 is used to read the encoded amounts from the existing forms and gate this information into the E2150 memory storage.

OPERATION (FIG 20)

There are two functions to this operation. One is the feeding and reading of the forms in the Auto Reader. The automatic operation of the Auto Reader is dependent on the CC3, FL and NOT POFF signals from the E2150. FL is controlled by a programmed stop position. The NOT POFF signal is high when the printer is in a static condition. CC3 is high between 355° and 115° of the Printer cycle.

The other function is the printing of as many balances as programmed. Normally, this is only one. The printer cycle is controlled by the Trial Balance FF.

With the carriage in a proper programmed stop and the Auto Reader turned on, the Auto Feed switch is depressed. A basic feed takes place until a form is fed to the Ready Station. At this time, the NOT POFF and CC3 and NOT BC allow the AR control signal along with RSTAFF and AFFF to bring high the Drop I signal, which causes the idlers to drop.

After the form moves $\frac{1}{4}$", the Start Read signal sets the RLFF. The form passes over the Read heads and a normal read takes place. The information from the Data X and Data Y Read Amplifiers is gated to the E2150 with the ARP

ON·FL signals. This information is handled in the same manner as if it were received from the E2150 Read Amplifiers.

The Trial Balance FF will be set at the end of a good read and the E2150 proceeds into a normal Trial Balance, block adding the amounts from 20 and 30 to 60 and 70 on a dual stripe machine, or 20 to 30 on single stripe machines.

The reset Trial Balance FF signal then causes the Printer Operate FF to set to begin a normal printing operation.

During this time, another form has been in the process of feeding into the Ready Station. If only one printer cycle was programmed, the operational speed of the two units is such that the printer is now waiting for another Auto Reader cycle. Thus, as a form causes the RSTAFF to set, the drop I signal becomes high and another Read cycle is started. If more than one balance was programmed to print, the form would more than likely position into the Ready Station before the printer reached another FL position. In this case, the Drop I signal is delayed until both FL and CC3 are high at 355° of the printer cycle.

All forms are read with the accumulated data being stored in MA 30 on Single Stripe, or MA 60 and 70's on Dual Stripe.

STOP FEED OPERATION

The Stop Feed Operation provides a means for the operator to stop the A4002 without disturbing a feeding or reading operation already in progress. When the Stop Feed switch S4104 is depressed, it causes a relay wetter output to set the Stop FF with the next clk pulse. See Figure VII-21.

The STOP FF signal will cause the Stop Feed lamp to illuminate and the AF + SF FF's to reset with the next clk pulse.

Depression of the Stop Feed Switch during an AF at the time of form movement from the Ready Station, will still allow a new feed to take place. However, the Drop I signal cannot come high as the form limits in the Ready Station because the AFFF is reset. The operation will cease with a form in the Ready Station.

The following five methods are used to set the STOP FF:

1. By the Stop Feed Switch as discussed above.

2. During a Single Feed Operation by the DCT switch. It is set at this time to prevent feeding a second form while the first one is traveling to the Ready Station.

3. By improper stacking of forms in the receiving hopper causing the bin jam switch to close. The Stop FF will set the next time a form sets the RSTAFF and produces a Drop I Signal.

4. 500ms, after the count down has reached two. The delay is necessary because a form could be picked up on the second feed attempt. If so, we do not want to stop the operation and the set AND gate would be blocked by the AFFF signal before the 500ms DMV times out.

5. See Figure VII-24. During a Double Document Clearing Operation. It is set at this time to reset the Double Document FF when the I DN assembly restores. The Stop FF also causes the STOP feed light to come on during D.D. clearing.

DOUBLE DOCUMENT OPERATION

The Double Document Operation consists of two parts:

A. The Detection Operation.

It consists of a roller actuated switch located on top of the Feed platen. It is adjusted to allow one form thickness to pass without the switch making contact.

See Figure VII-24. If this switch (S4108) is closed during a feed operation, the next clk pulse will set the DD FF. The outputs of this FF function are as follows:

1. The DDFF signal will cause a Sol Driver to illuminate the DD light.

2. The NOT DDFF signal inhibits the illumination of the STOP FEED light at the time of DD detection.

3. The DDFF signal and clk, resets either or both the SF and AF FF's.

4. The NOT DDFF signals inhibit the AND gates to prevent setting the AF or SF FF's if their push button control switches are used. This signal also inhibits the Ledger Ready signal to prevent feeding a form in the E2150 while a DD condition exists. (FIG 20).

B. The Clearing Operation

This consists of a method to cycle the forms from the Ready Station without reading them.

Depression of the DD front panel switch (S4105) will cause two relay wetter outputs to go high.

One such wetter allows the DD CLR signal to make the Drop I signal high, which in turn causes the Idler assembly to drop. This will cause the forms to be fed from the Ready Station into the receiving hopper. (FIG 23)

The other output of this DD clr wetter will allow the next clk pulse to set the CCFF. This is done to inhibit the Start Read Signal and inhibit the outputs of the Data X and Data Y signals. the NOT DDFF signal is used to inhibit the reset AND gate to the CCFF. This is to prevent resetting the CCFF which is inhibiting the read. (FIG 22)

The other relay wetter output called DD, is used to set the Stop FF on Double Doc clearing. Stop FF will remain set until the next initiation of an AF or SF.

Setting of this FF will allow the DDFF to reset as the Idler assembly is being restored.

CLIPPED CORNER

The Clipped corner FF allows a form to be fed through the A4002 without being read. See Figure VII-25. If the CCFF is set, the Start Read signal will be low as the form is fed from the Ready Station, and the form is not read as it travels to the receiving hopper.

The normal method of picking CCFF is for the CC solar cell output to be high as a form limits on the Ready Station limit plate. (assuming the form is clipped.) The ST RD signal being high at this time will cause NOT SEL + CC to be high. This gated with NOT IDN and the high RSTA will allow the next clk pulse to set the CCFF. The not CCFF signal inhibits the Start Read signal and the form is not read.

The CCFF is normally reset as the RSTA solar cell is unblocked and the NOT IDN signal goes high.

The other reset gate functions as follows:

If a form enters the Ready Station slightly skewed, its possible for the RSTAFF to set prior to the blocking of the clipped corner solar cell. When this happens, the CCFF will set and remain set until the form squares itself against the limit plate.

The inverted NOT SEL + CC signal, along with CCFF·NOT DDFF·NOT IDN will reset the CCFF with the first clock pulse following the blocking of the CC solar cell. A normal read then takes place.

COUNT DOWN OPERATION - Figure VII-22.

The count down operation consists of a method of stopping the feed cycle if a form is not picked up in two attempts.

There are two Flip Flops used to detect the number of attempted feeds.

The Count One (C1) Flip Flop is controlled by the inverted output of the CT DN SCA. The C1FF will set as the Feed Cam Arm starts to restore after the first form pickup try. If a form is picked up and injected into the feed platen, the DCT signal will reset the C1FF with the next clk pulse. DCT also resets Feed FF and no further attempts are made.

If a form failed to get picked up, the Feed Clutch cycles again. As the Cam Arm starts to restore during this second attempt the C2FF will set. Setting the C2FF controls logic to stop the operation.

COUNT DOWN OPERATION - AUTO FEED - Figure VII-22.

As the Cam Arm starts to restore on the first attempted pickup, the C1FF will set due to the SCA inverted output going from ground to -4V.

Setting of the C1FF will cause the SFFF to be reset with the next clk pulse.

See Figure VII-22. As the cam arm starts to restore on the second feed attempt, the C2FF will set. Setting the S2FF at this time will allow:

1. The AFFF and Feed FF to reset with the next clk pulse. See Figure VII-21.

2. The table elevation solenoid to pick causing the raise pawl to become active. The table will raise on the next attempted feed.

3. A multivibrator to trigger, and afeter a 500ms delay, will produce a 15 usec pulse. This pulse gated with C2FF·NOT AFFF will set the Stop FF. This will stop the cycle, and illuminate the NO FEED lamp.

If a form was picked up on the second try, it would be injected into the DCT switch before the 500ms DMV times out. When this happens, the AFFF will be set again through DCT·C2FF·NOT SFFF. The setting of AFFF will prevent the DMV pulse from setting the STOP FF by inhibiting the set AND GATE with the AFFF signal.

Drop Count resets C1FF, therefore when AFFF sets again, C2FF will be reset with the next clk pulse. Thus, the Automatic Cycle of feeding forms remains unbroken as the cycle continues.

COUNT DOWN OPERATION - SINGLE FEED

The operation is exactly the same as Auto Feed except for the method of resetting the SFFF when form pickup fails.

An AND gate with C2FF and the 500ms DMV pulse will reset the SFFF if form pickup fails. If a pickup is made on either try, the SFFF is reset in the normal manner by the IDN·RSTAFF signals. The C1FF in this case is reset by the DCT signal and NOT C1FF·SFFF·CLK reset the C2FF.

BIN JAM LOGIC - Figure VII-23.

The Bin Jam switch (S4109) is located above the receiving hopper. This switch controls the Drop Idler solenoid circuit, preventing Idler drop if improper form stacking occurs.

The Bin Jam signal is high only during the time the Drop I signal is high and a jam is holding the switch transferred.

If the switch transfers, it has no effect on the next feed until the form reaches the Ready Station limit. At this time, the RSTAFF signal brings the Drop I signal high and through a relay wetter the Bin Jam signal comes high. The idler solenoid is not energized at this time because of the transferred Bin Jam switch.

See Figure VII-21 . The Bin Jam signal will set the Stop FF with the next clk pulse. This in turn will reset the AFFF, causing the DROP I signal to go low.

If the SF push button is now depressed with a jam still present, and a form in the Ready Station, the SFFF will set bringing high the Drop I. Drop I brings high Bin Jam. Bin Jam sets the STOPFF and the two reset the SFFF with the next clk pulse. This allows the operator to clear the Bin Jam without the Idlers dropping and sending another form into the receiving hopper during the clearing.

TABLE ELEVATION CONTROL - Figure VII-26.

The Table Elevation Control is a mechanism to control the automatic raising of the form table during a machine cycle. The correct table height will be maintained at all times. This insures proper form pickup during the feed cycle.

The Electrical part consists of a Photo Cell, Light source, and logic circuit to control the solenoid driver that energizes the Table Elevation Solenoid.

During an AF or SF operation, the light source to the photo cell is normally blocked. A darkened cell presents a high resistance to its circuit somewhere over 1 MEG OHMS resistance. This causes the base of the Inverter transistor to be reversed biased and cut off. With the inverter output at -4V, the solenoid is not being energized.

When the level of the forms has diminished to a point where light from the lamp strikes the photo-cell, its resistance changes to a low value. This low value allows the Inverter transistor to be forward biased and the collector output to go to ground. The solenoid driver conducts and the elevation solenoid picks dropping the pawl into the ratchet. The next feed attempt will cause the elevator to raise one step.

The CT DN signal on the AND gate is used to disregard a high signal from the inverter at a time when the forms are being pushed down by the suction foot. This insures that only during normal form riffling will the sense circuit function.

Table Elevation will also be initiated if the count down reaches two, regardless of whether light is seen on the photo-cell. In most cases, light would be seen by the photo cell on the count of 2, and elevation would be initiated in the regular manner.

SELECTIVE READ - Figure VII-25.

The selective read feature of the Auto Reader provides for automatic selection of accounts by category, for obtaining a trial balance without the necessity of removing and refilling the accounts.

A hole, located at one of 24 positions along the top of the form, is used to select the form to be read by the Auto Reader.

A solar cell, located on a sliding bracket, is used to change the category of which hole position will be read. Only the forms punched in the corresponding position, that aligns with the photo cell, will be read. The read operation is by-passed on the other forms, but they are fed through the Auto Reader to maintain their correct sequencial order.

A toggle switch, Figure VII-25 mounted on top of the control switch panel bracket must be set to the "Select Read" position for this operation. When set at "normal" position, regular operations are performed, reading all the ledgers except those with cut corners.

The holes in the ledger are to be located and punched according to the following specifications:

1. $\frac{1}{4}$" in diameter.
2. Round, punch by a standard hand punch.
3. The first hole center is 1 $\frac{1}{2}$" ($\pm$ 1/32) from the right edge. The hole positions are numbered from right to left.
4. Holes are 3/8" ($\pm$ 1/32) apart, center to center, but this tolerance is not cumulative.
5. The center of the hole is $\frac{1}{4}$" ($\pm$ 1/32) below top of form.
6. There must be at least $\frac{1}{4}$" space between the last hole and the left edge of the form.

Sel Read Operation

See Figure VII-25. As a form enters the Ready Station, the first solar cell to be blocked will be the Select Read. Its SCA output goes to -4V. This iverted signal, and the Select RD toggle switch output will cause the NOT SEL + CC signal to go to ground. If a punched hole does not align with the Select

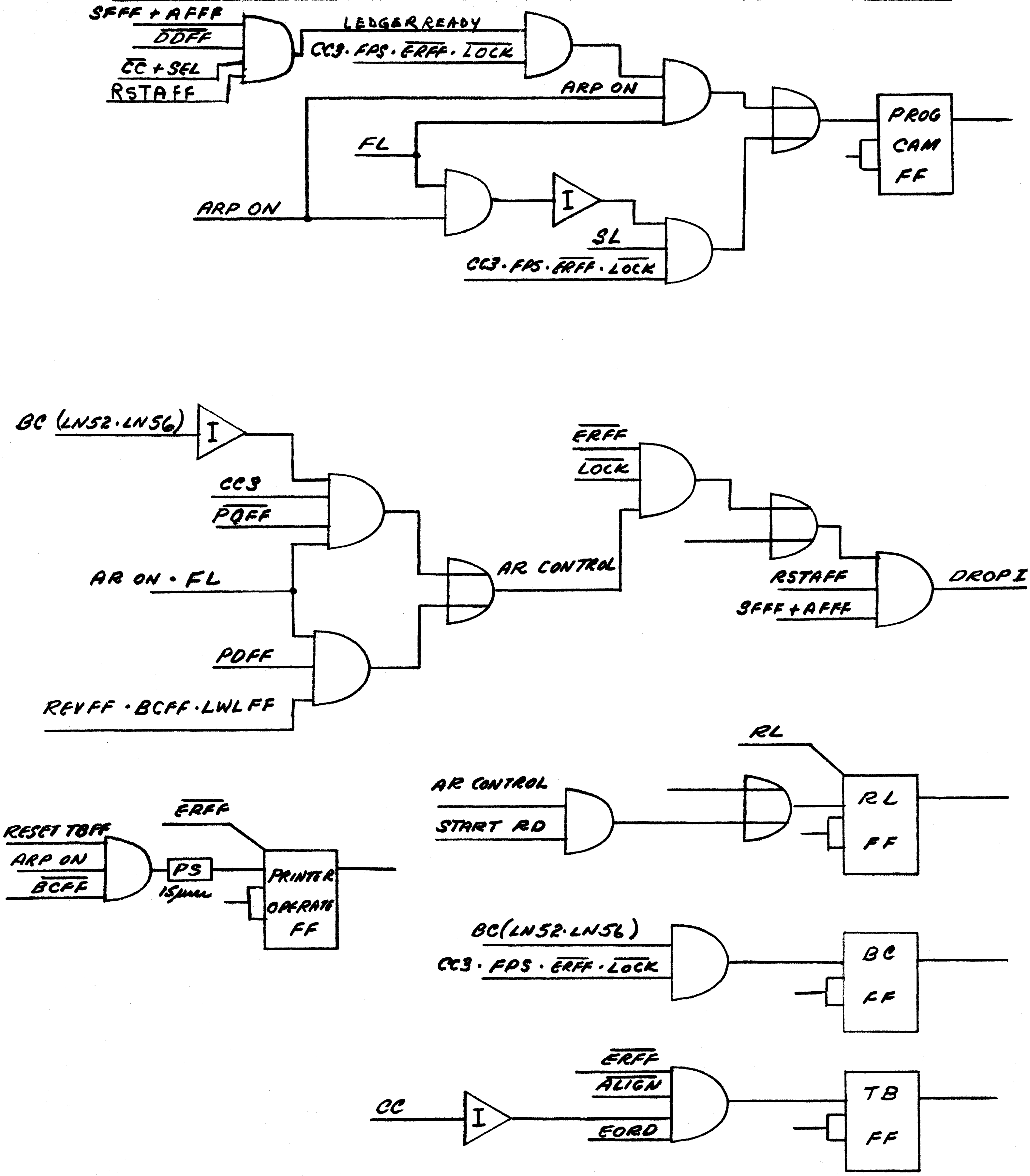


FIGURE VII - 20

(Draft E2150)
For Form 3738

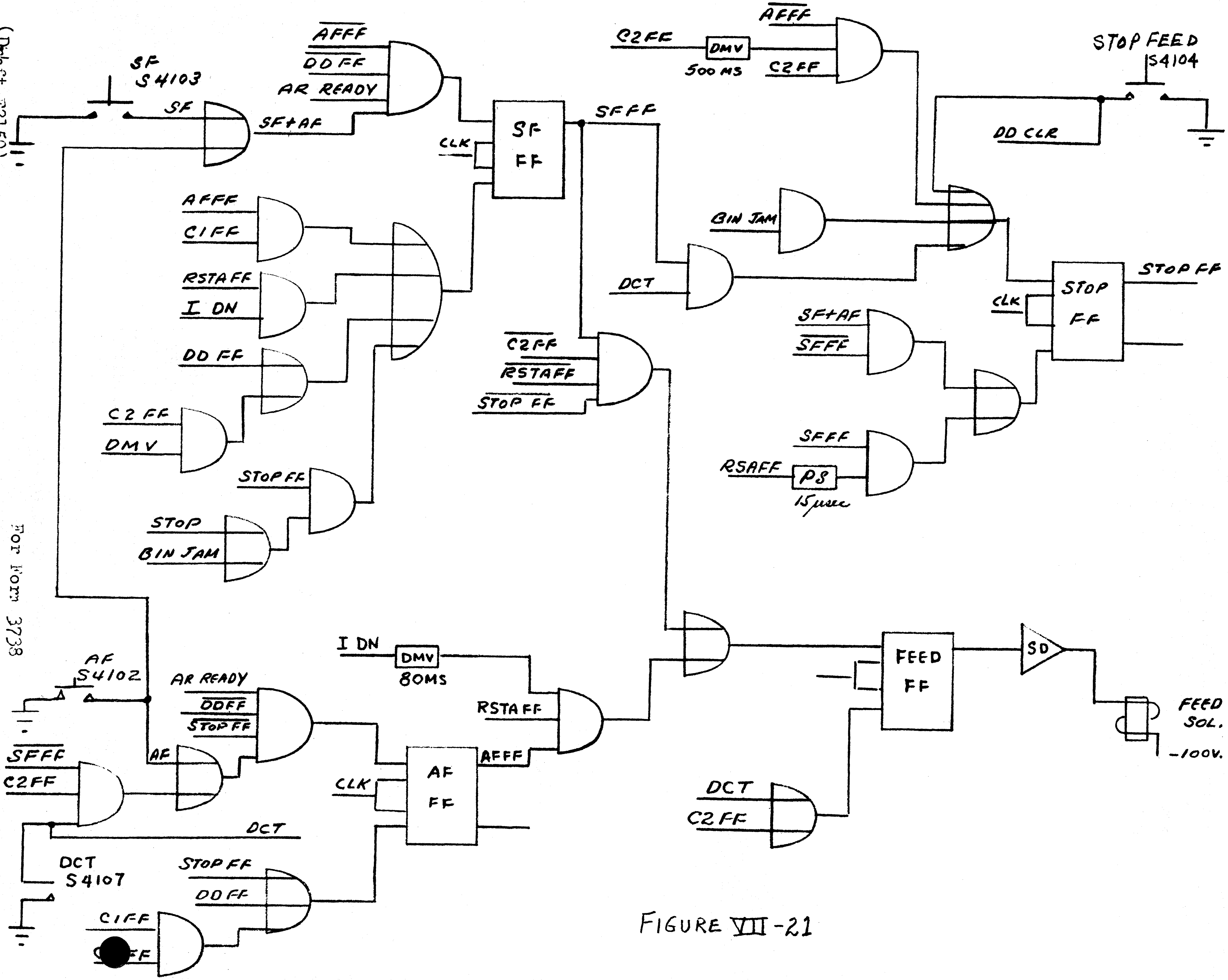


FIGURE VII-21

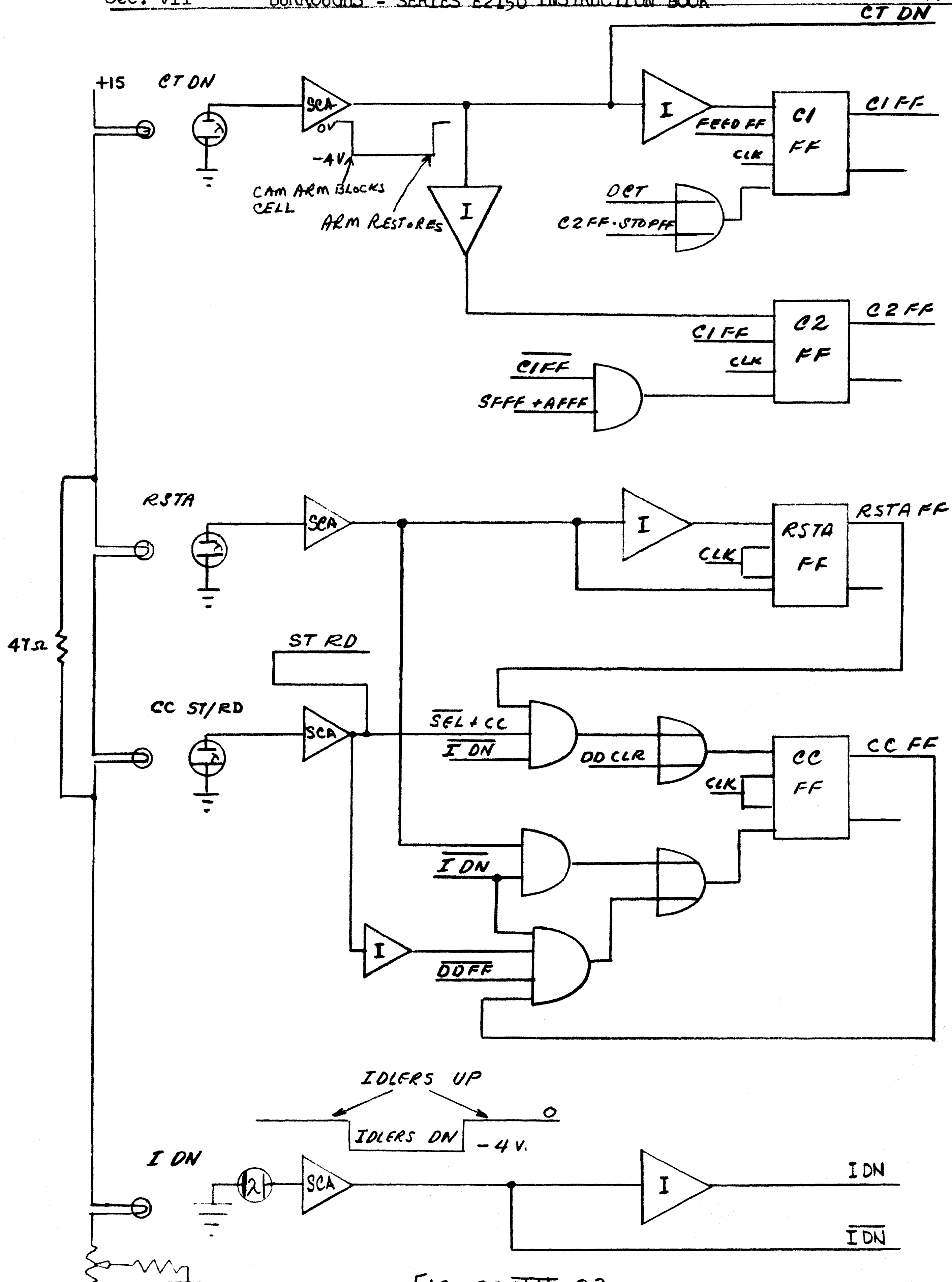


FIGURE VII-22

(Draft E2150)

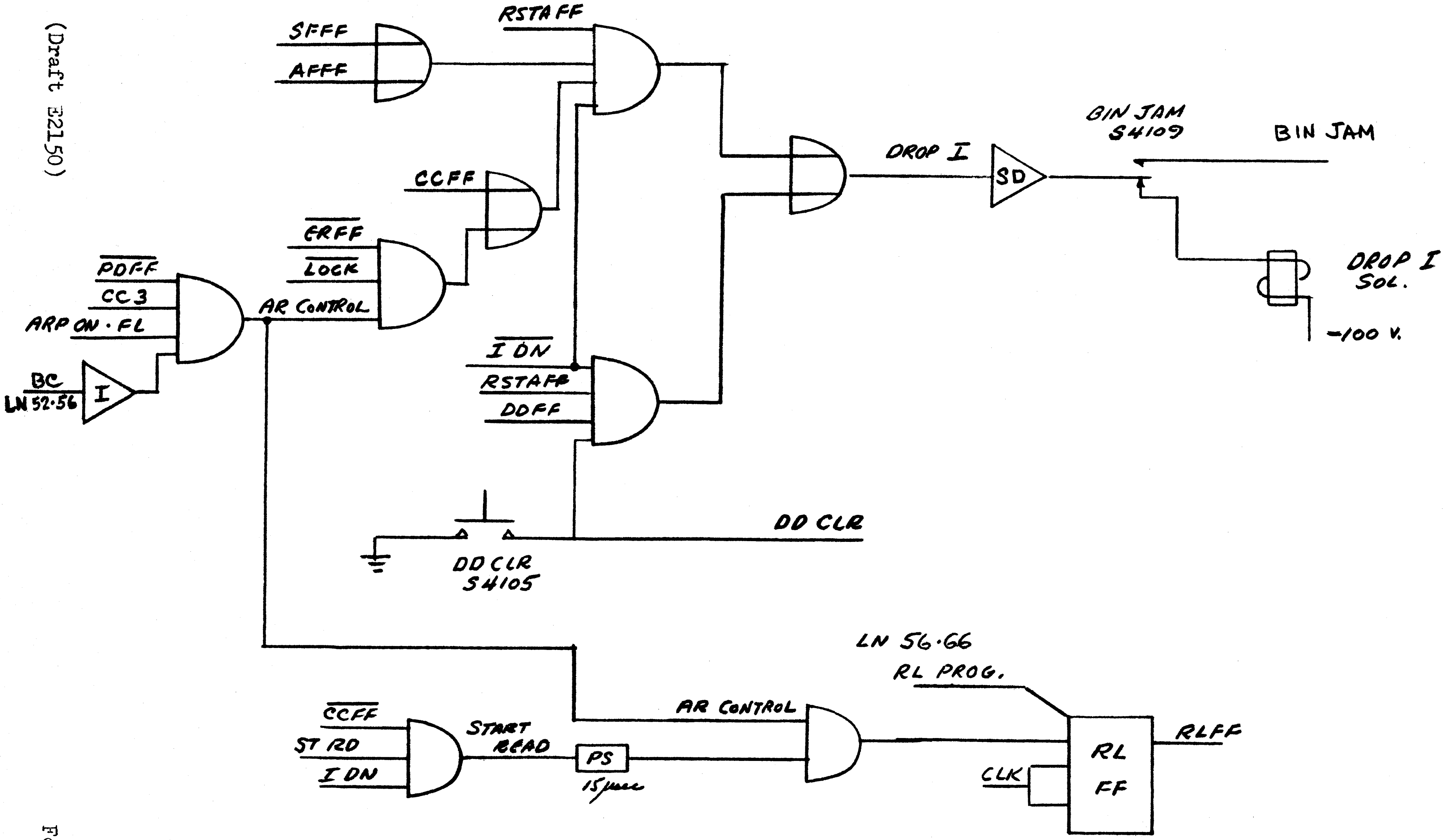


FIGURE VII-23

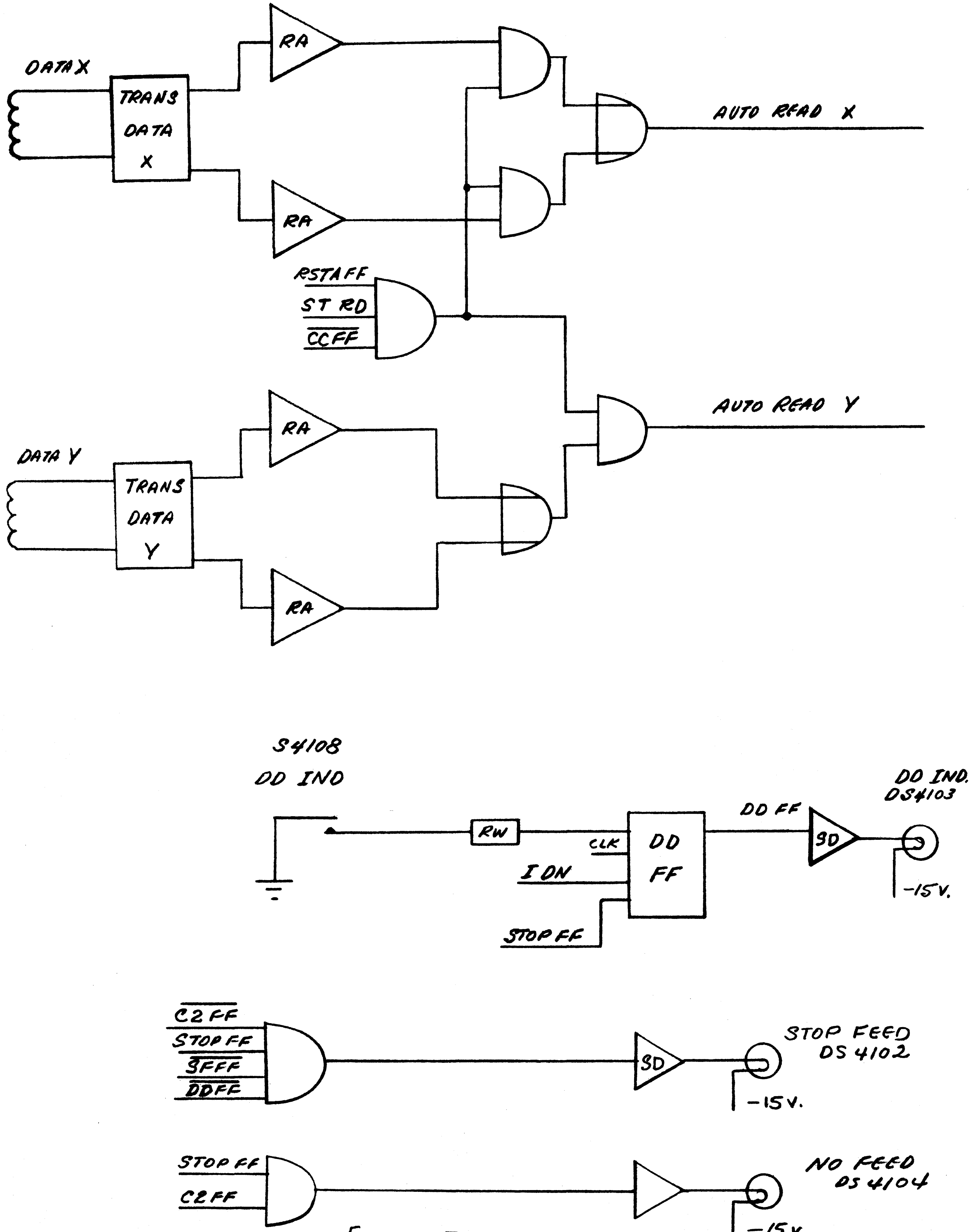


FIGURE VII-24

(Draft E2150)

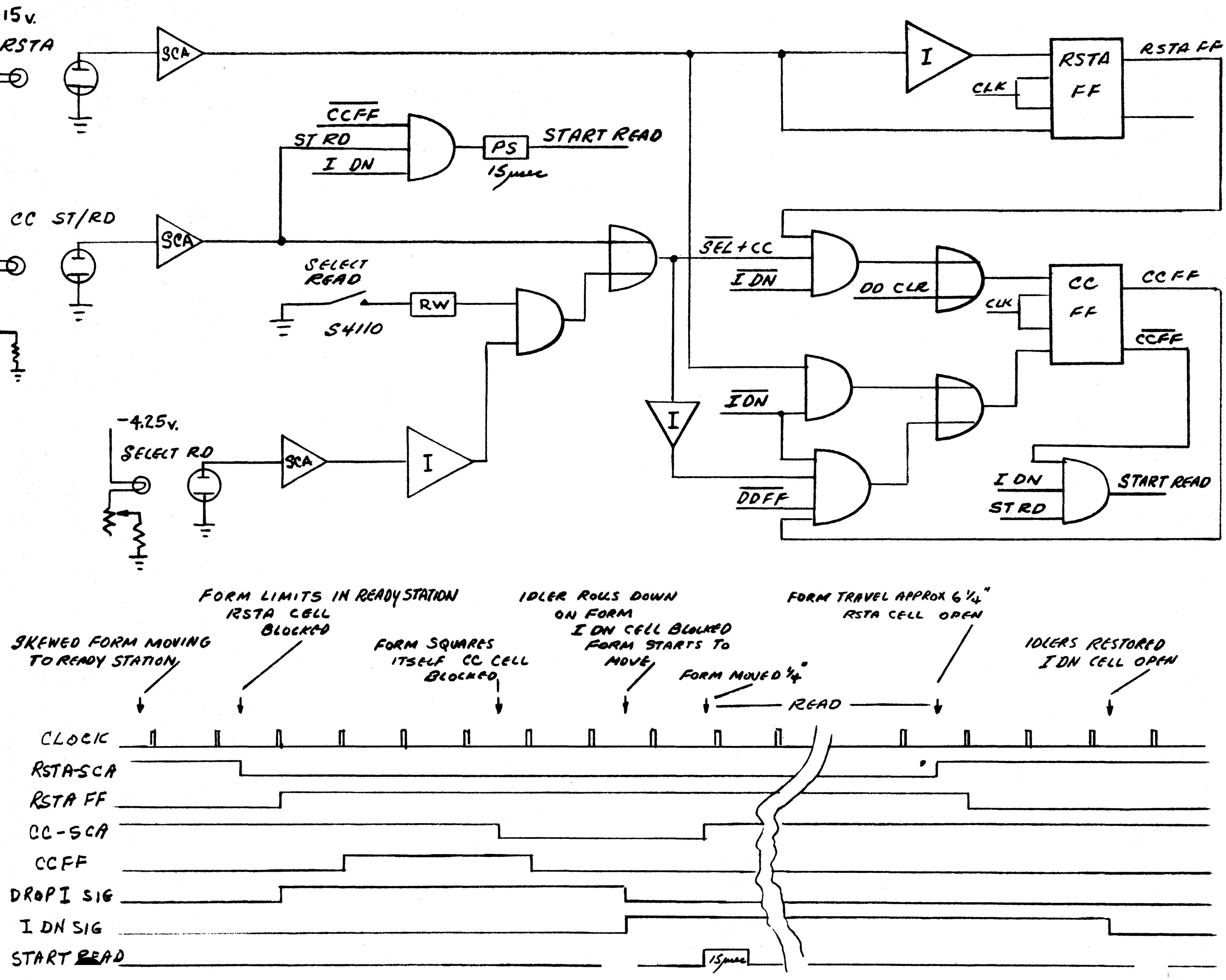


FIGURE VII-25

For Form 3738

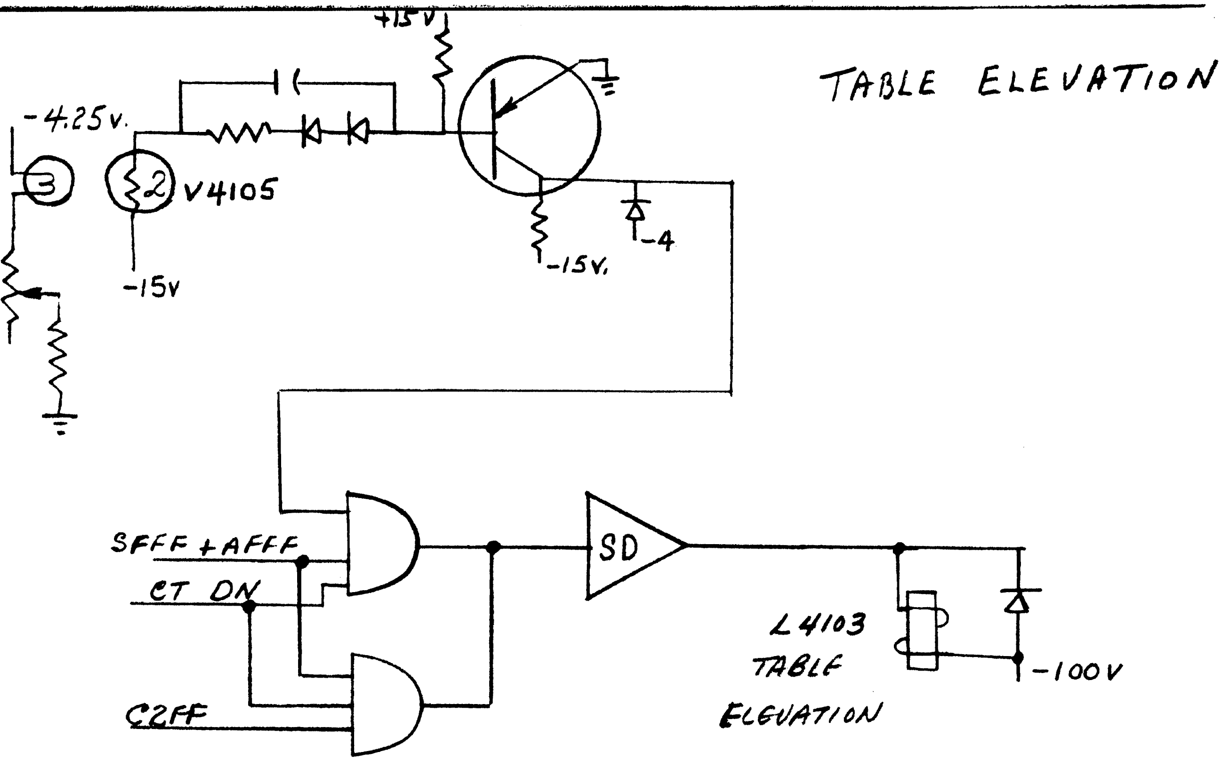


FIGURE VII-26

GATE VIEW FROM OUTSIDE

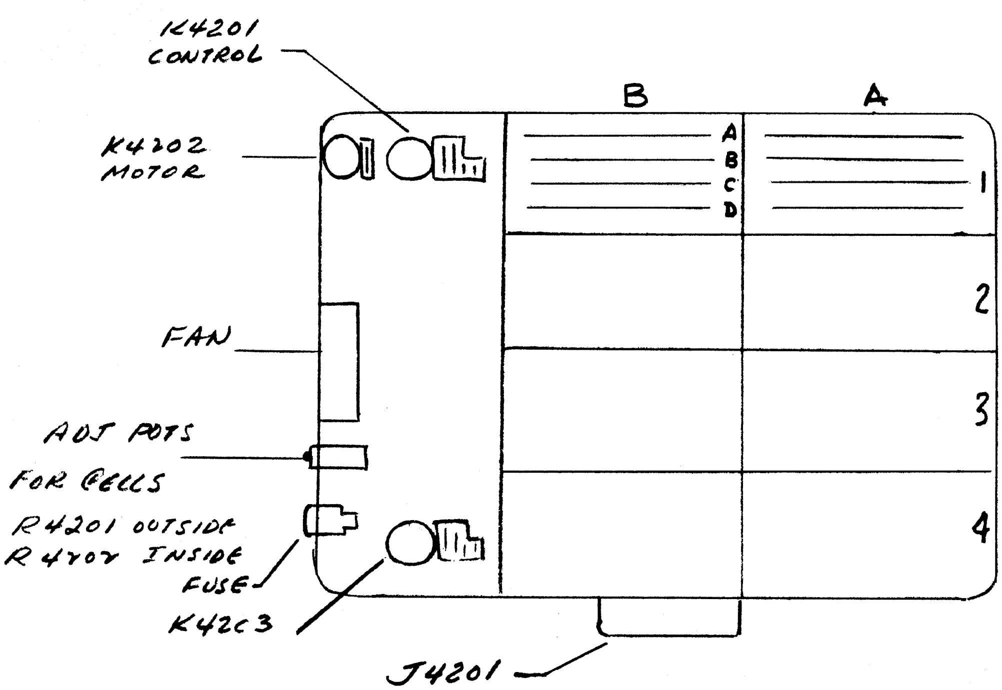


FIGURE VII-27

RD cell as the form limits in the Ready Station, the CCFF will set. Setting the CCFF results in the form passing out of the Ready Station without being read by inhibiting the Start Read Signal.

If a punched hole aligns with the SEL RD solar cell as the form limits, the SCA output will go to ground. The inverted signal now inhibits the NOT SEL + CC AND gate and the NOT SEL + CC signal is low. The CCFF is not set and normal reading takes place. All forms are passed through the machine and only those forms with a hole punched that corresponds to the selected setting of the solar cell are read.

SIGNALS AND TERMS

AF — Auto Feed. A signal developed from the AF front panel switch, that sets the SF and AF FF's.

AR CONTROL — Auto Reader Control. A signal developed in the E2150 used to allow a form to feed from the Ready Station.

AR READY — Auto Reader Ready. A signal developed by the CT DN or CC solar cells that prevents starting an operation until the Solar Cell amplifiers have gained control of the logic.

AUTO READ X + Y — Auto Read X + Y. The X and Y outputs of the Auto Reader X and Y Read Amplifiers.

AR POWER ON — Auto Reader Power On is a signal generated by the picking of the Power On Relay that conditions the logic control of the E2150.

BIN JAM — Bin Jam is a signal developed from the closing the Bin Jam switch located in the receiving hoppe.

CT DN — Count Down. A signal developed each time the feed cam oscillates.

DCT — Drop Count. A signal developed from the closing of the DCT switch as a form enters the Ready Station.

DD Clr Double Document Clear. A signal developed from the closing of the Front Panel DD switch which is used to clear forms from the Ready Station without reading them.

DMV Delay Multivibrator. A signal taken from the 500ms DMV used to reset the SFFF.

DROP I Drop Idlers is a signal used to energize the Idlers solenoid and cause a form to be read.

I DN Idler Down. A signal indicating whether the idler rolls are in a raised or lowered position.

LEDGER READY Ledger Ready is a signal indicating to theE2150 that a form is in a position to be read.

POR Power On Reset is a signal used to reset all A4002 FF's as the power comes on.

SCA Solar Cell Amplifier is the electronic card used in conjunction with the solar cells.

SEL + CC Select or Clipped Corner is a signal developed by solar cells to control whether a form should be read.

SF Single Feed is a signal developed from the depression of the Front panel SF switch used to feed a single form.

ST RD ST RD is a signal from the ST/RD + CC solar cell indicating the form has moved $\frac{1}{4}$ over the read heads.

START READ Start Read is a signal from the A4002 to the E2150 to set the RL FF and allow information to be processed.

STOP Stop is a signal developed from the depression of the Front Panel Stop or DD switches.

FLIP FLOP IDENTIFICATION

Standard E2100 Flip Flops are used in this machine.

DESIGNATION	NAME	FUNCTION
AF	Auto Feed	Controls Automatic feed of forms.
CC	Clipped Corner	A control FF that determines if a form is to be read.
C1 C2	Count One Count Two	Count down FF's used to detect the number of feed attempts.
DD	Double Document	A control FF to stop the operation if double feed occurs.
FEED	Feed	Used to cause the Feed solenoid to energize.
RSTA	Read Station Align	A Flip Flop used to signal the logic that a form is in the ready station.
SF	Single Feed	Controls single feeding of forms.
STOP	Stop	A control FF used to stop the operation.

SOLAR CELLS

Five solar cells of the type used in the E2150 are used in this machine.

The solar cell works on the principle of developing a voltage and current inside the cell when an external light is applied to it.

DESIGNATION	NAME	FUNCTION
CC ST/RD	Clipped Corner Start Read	Used to detect forms with corners clipped and provides ST RD when form moves $\frac{1}{4}$" out of ready station.
CT DN	Count Down	Used to detect when a feed is being attempted.
I DN	Idlers Down	Used to detect when the idler roll assembly is lowered.
RSTA	Ready Station Align	Used to detect presence of a form in the ready station.

DESIGNATION	NAME	FUNCTION
SELECT READ		A solar cell used on the feature Select Read, that controls reading certain forms.

PHOTO CELLS

One photo cell is used in this machine. It works on the principly of varying its resistance when an external light is applied. The cells resistance drops when light is applied.

NAME	FUNCTION
TABLE ELEVATION	Used to detect low table height which causes the table to raise.

RELAY IDENTIFICATION

NUMBER	NAME	FUNCTION
K4201	Control	Used to supply voltages to the A4002.
K4202	Motor	Used to run the motor.
K4203	Power On Reset	Used for voltage controls after Control Relay is picked.

SOLENOID IDENTIFICATION

NUMBER	NAME	FUNCTION
L4101	Drop Idlers	Causes the idler rolls to be lowered onto the form.
L4102	Feed	Allows the feed clutch to cycle to pick up forms from the table.
L4103	Table Elevation	Controls a mechanical pawl, which when active will raise the elevator on a feed attempt.

SWITCH IDENTIFICATION

NUMBER	NAME	FUNCTION
S4101	On-Off	Turns D.C. On-Off to Auto Reader.

SWITCH IDENTIFICATION - continued

NUMBER	NAME	FUNCTION
S4102	Auto Feed	Auto Feed control
S4103	Single Feed	Single Feed control
S4104	Stop Feed	Signals that the feed operation has stopped.
S4105	Double Document	Allows clearing a double form from the ready station.
S4106	Safety	Turns off power to Auto Reader when lid is raised.
S4107	Drop Count	Signals that a form is being fed into the ready station.
S4108	Double Document Indication	Signals that more than one form is being fed into the ready station.
S4109	Bin Jam	Signals that the forms are not stacking properly in the receiving hopper.
S4110	Select Read	A switch controlling the use of the Select Read Feature.

(Draft E2150)

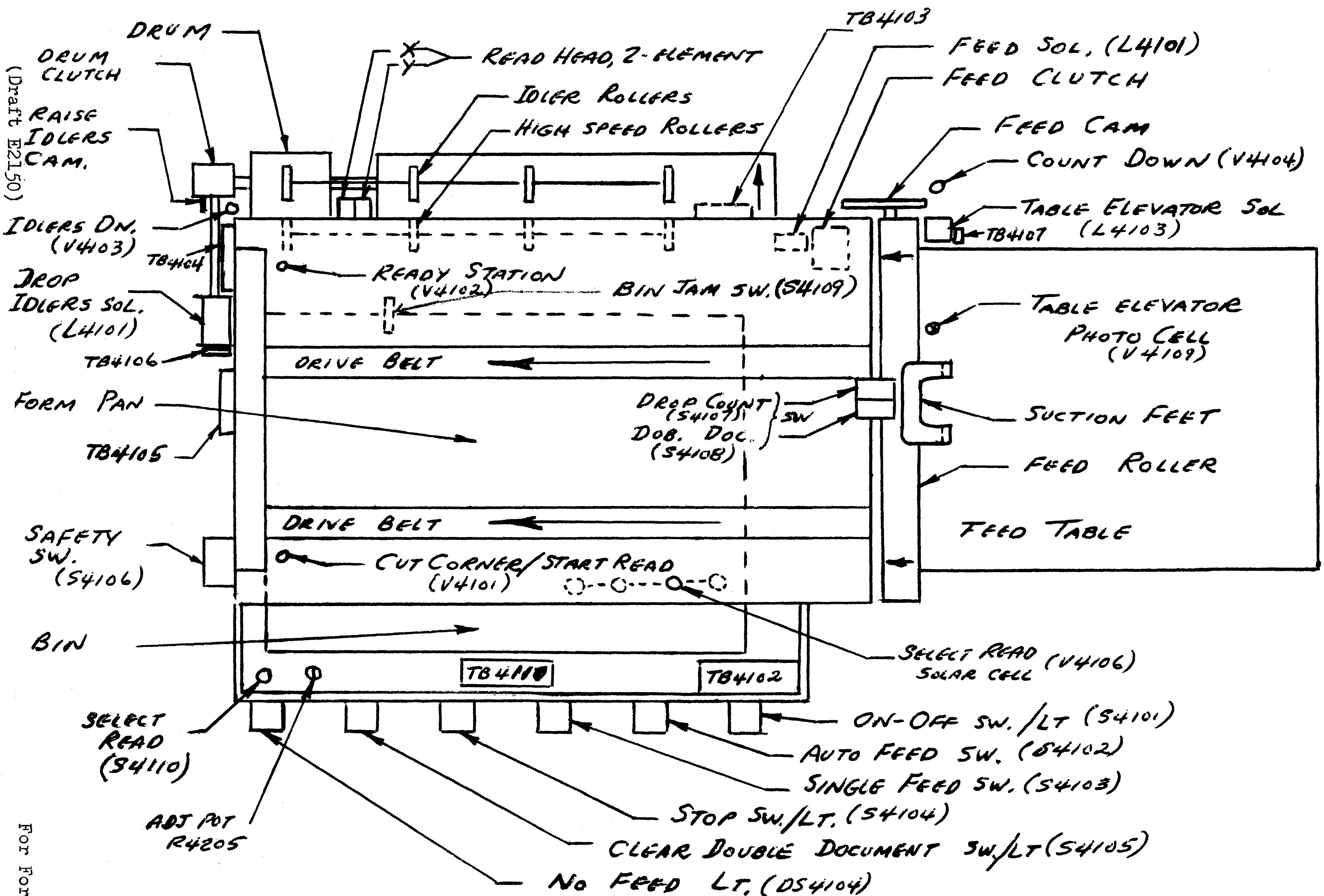


FIGURE VII - 28

INDEX REGISTER FEATURE

The Index Register Feature (IR) is a programable method of indexing the Memory Address to which data is to be computed by coding the data word with the address to be acted upon. This feature may be used on E 2150 style systems after Serial #E3107.

The use of this feature allows a categoric distribution of data during a routine trial balance operation. It enables amounts transferred to P during T1 time to be added during T5 time to the Memory Address indexed by columns 11 and 12 of P.

PROGRAMING

Two lanes of programing are involved with this feature. Lane 56 (SL) must be programed when either of these control lanes are to be active.

Lane 58 Memory Address C Arithmetic (MAC)

When lanes 58-56 are pinned the MAC signal will cause the MART and MARU FF's to be set equal to the decimal digit of columns 11 and 12 of P. Setting of these Flip Flops occurs during the 9 search of T2 time. The MAC signal will also cause a P to C algebraic addition to take place during T5 time.

Lane 60 Ten Digit Arithmetic (TDA). When lanes 60-56 are pinned the TDA signal will cause columns 11 and 12 of P to be cleared during T2 time so that only columns 1 thru 10 will contain data to be used in all other T times.

Two examples of programing are listed below explaining applications of this feature.

EXAMPLE #1.

In this example the type of loan is coded in columns 12 and 11 along with the amount of the loan in the 1st ten digits of the same word. This word is encoded on the ledger stripe along with the other information. During the machine cycle, after reading the ledger, a transfer of this word is made to P. The register (M.A.) is selected during T2 and the 1st ten digits of the word accumulated in the selected memory. Thus at the end of a trial balance a complete breakdown of each type of loan has been made along with a grand total of all loans.

EXAMPLE #2.

In this example a more complete analysis of a trial balance is desired. This example might be on a mortgage accounting application where the desired results are to produce, as a by-product of the trial, any one or more of several categories concerning the mortgage loan accounts.

Each loan account will have encoded on the stripe one word into which all pertinent information about the account is stored in two digit codes. During the trial balance several stop positions are used to isolate and select the desired code. The total of the account is then accumulated into the selected code resulting in a grand total of all accounts containing such a code. Different codes (categories) may be selected during the trial balance by changing a predetermined factor such as 1,000.00 or 10,000.00. In this way any number of categories may be selected during the trial balance operation. Each category selection during the trial requires a different set of carriage positions to obtain the desired results.

In the example below the 2 digit codes are encoded in MA21 on the ledger card. The loan balance of $10,000.00 is encoded in MA25. The desired result is a total of all outstanding loans at 5 1/4% (code #45 encoded in digits 4 and 3 of word 21). The constant (CFM) to be used to cause a left hand shift in this case is 1,000,000.00.

MA25 = $10,000.00

MA21 =

CAT.				G.L.	I.R.	T.L.
COL.	12-11	10-9	8-7	6-5	4-3	2-1
CODE				56	45	82

CATEGORY	T.L. = TYPE OF LOAN	I.R. = INTEREST RATE	G.L. = GEOGRAPHIC LOCATION
CODES	80 = G.I. 81 = F.H.A. 82 = Conventional	43 = 4% 44 = 4 1/2% 45 = 5 1/4%	55 = North 56 = N.W. 57 = N.E.

Six carriage positions are needed on this application to isolate the one category desired during the trial balance operation. Stops #5 and 6 are for credit amounts.

STOP #	1	2	3	4	5	6
LN 3			S			
LN 5				<		<
A	N	N	A	N	T	N
B	A	R	A	T	S	T
C	R	S	R	N	S	N
MA	21	10	25		10	
	RLN FL. RPT CFM M	TDA RPT	AM3 RPT DSR	MAC TDA RPT SP CNT		MAC TDA RPT SP CNT RE

A stop by stop analysis of the operation is as follows:

Stop #1: Read ledger in Auto Reader. Block Add to 60's and 70's.

Sub Total MA21, Add B.

Multiply by constant MA 02.

B now = 4,582,000,000.00

Stop #2: Read 10 digits of B, Subtract C10

B now = 4,500,000,000.00

Stop #3: Read MA25, Add B and A

Check for status of A, if + basic tab to #4

if - skip to stop #5.

B now = 4,500,010,000.00

Stop #4: Total B add to MA45 using the MAC to select MA45. Also use TDA to add only columns 1 thru 10.

CNT in col 10 keeps a total of the number of loans.

Ret in lane 5 reads next ledger.

CREDIT ROUTINE: STARTING AT STOP #3

Stop #3: Read M25 Add B and A

Check for Status of A. If Minus skip to #5.

Assuming the loan was 10,000.00 -

B would now equal 4,499,990,000.00

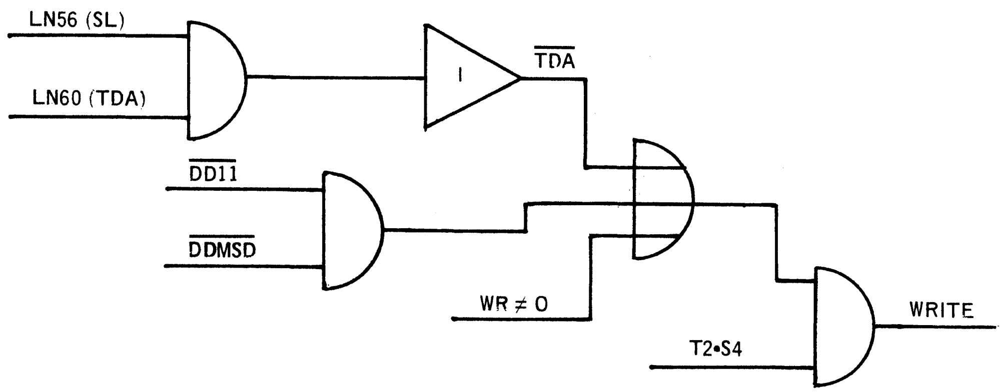
Stop #5:	Total A (10,000.00-)	4,499,990,000.00+
	Subtract B	10,000.00+
		4,500,000,000.00+
	Subtract C10	10,000.00+
	B now equal to:	4,500,010,000.00+
Stop #6:	Total B	
	MAC (Add to MA45)	4,500,010,000.00
	TDA (Add 10 digits only)	10,000.00-
	CNT (Count number of loans)	10,010,000.00-
	RE (Reverse Entry so as to Credit Amount)	
	MA45 =	10,010,000.00-

INDEX REGISTER LOGIC

There are three changes of 2100 logic when the Index Register feature is programed. Two of these are active during T2 time, the other during T5 time.

Ten Digit Arithmetic (TDA) (LN 60)

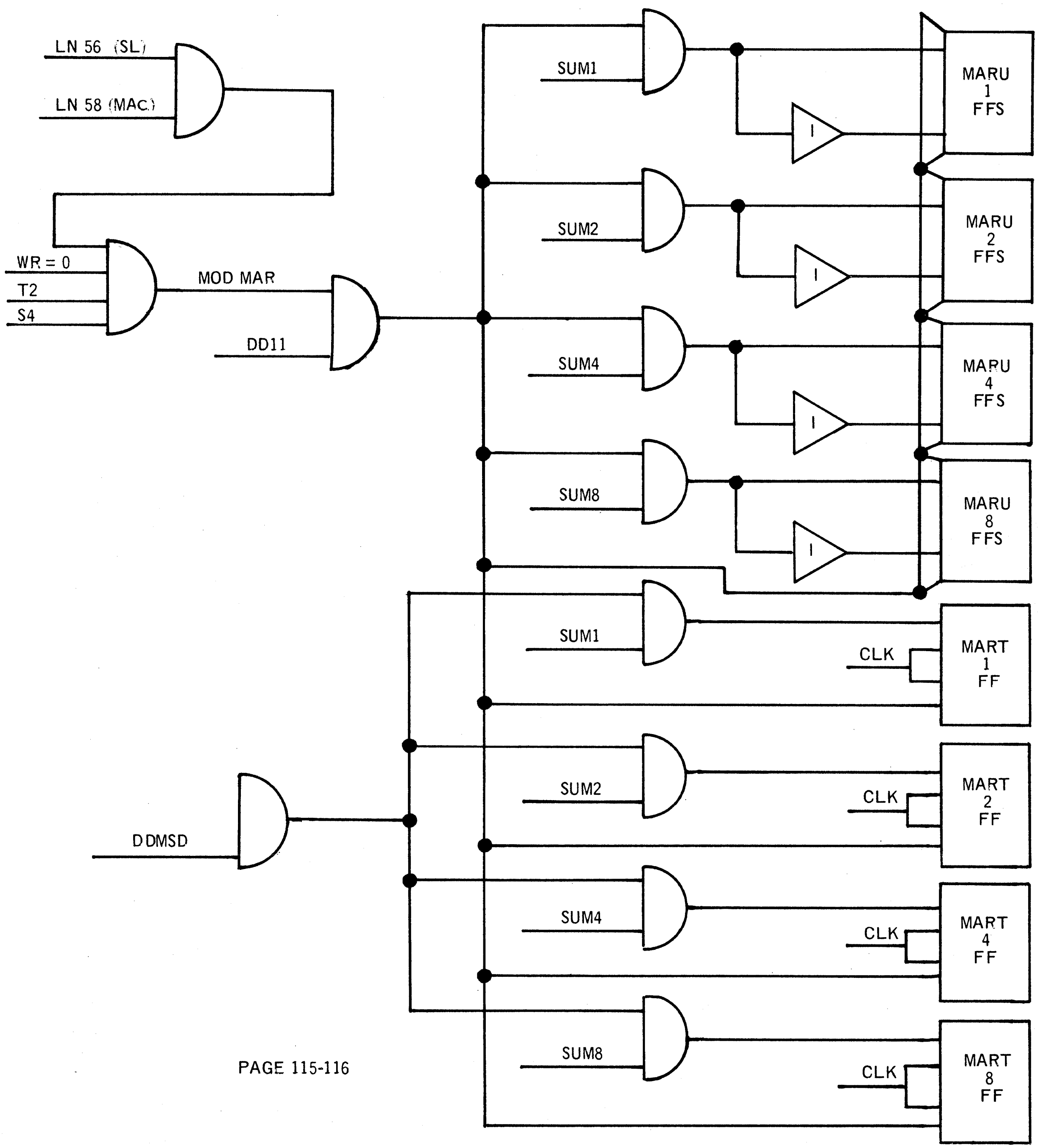
The TDA signal controls the "write" signal during T2-S4 when P is being written from the MR's during the search for the 9 print position. If the TDA lane 60 and SL lane 56 are pinned, no "write" will be made to "P" during DD11 or DDMSD. Thus P will contain 10 digits of data for the rest of the electronic cycle.



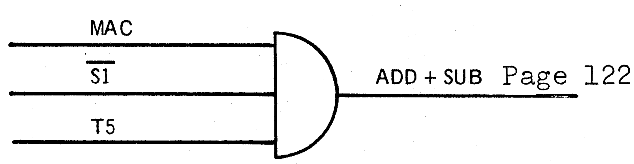
PAGE 113

Memory Address C Arithmetic (MAC) (LN58)

The MAC signal controls setting the address Flip Flops during T2•S4 when the WRFF's are equal to zero. The MARU FF's will be set during DD11 and the MART FF's during DDMSD, thus columns 11 and 12 control the address to which amounts in the other columns will be added to during T5 time.



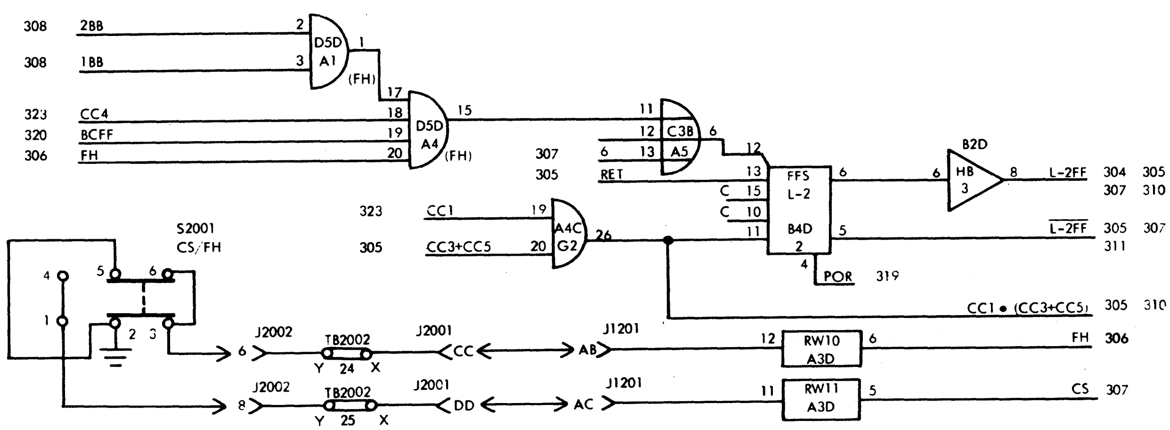
Addition during T5 time is controlled by the ADD + SUB signal in S2•S3. The Add + Sub signal is made high by the MAC • $\overline{S1}$ • T5 as shown below. The $\overline{S1}$ is on the gate to prevent setting the CiFF.



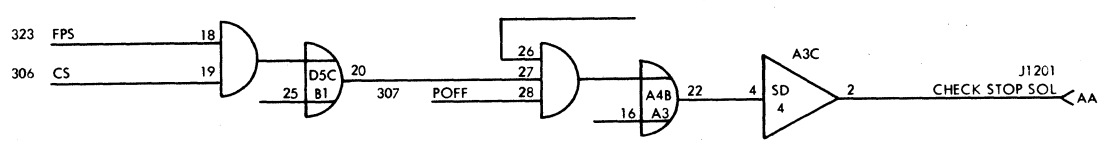
AUTOMATIC FORM HEADING ALIGNMENT

Form Heading permits automatic alignment of striped ledgers to line -3 and is under control of the check stop switch S2001.

With the switch in the forward position, Form Heading is active and check limits inactive. When a striped ledger is inserted in a Blank Card or Blank Card and Clear position, L-2FF will be set when count reaches 3, to automatically align the form to line -3. This permits end-run filled sheet operations and Initial Installation without having to turn the platen back manually. It is still necessary to have the ledger spaced up to line 1 or better prior to writing, to encode a usable line find pulse.



With the switch in the rearward position, Form Heading is inactive and check limits are active. When a ledger card is inserted in a BC or BCC position, it will automatically align to line 1. Heading information is not printed on the new ledger at this time.



AMOUNT PROTECTION FEATURES

Beginning with approximately Serial #F162368P-E4768P, striped ledger machines are wired to accept amount protection features AP1, AP2, or AP3. The standard amount protection of one dollar sign to the left of the MSD is active without one of these features being wired.

STYLE 1 allows 2 characters to print from RACKS 5 thru 13.

STYLE 2 allows 2 characters to print from RACKS 4 thru 13.

STYLE 3 allows a print of a $ from RACK 13 followed by asterisks in RACKS 12 thru 5.

AP STYLE 1

This feature allows for a print of a character ($ or *) in two columns to the left of the most significant digit. Type bar columns 5 thru 13 (amount columns 4 thru 12) are active when the AP lane switch is programmed. Two logic cards are needed for this feature: LCB at E2A and LCE at E2B.

OPERATION (See Fig. VII-29)

A regular $ search is made as on a standard machine. On the "zero" search, the CIFF is made to set from the column 6 Rack Stop FF that was set for the $ sign. The CIFF signal gated to the adder inhibits the sum = 9 signal for the next column to the left (column 7). Thus the Rack Stop FF for this column does not set to allow the clapper to drop. The CIFF is only high for the one column search. During the subsequent print searches (WR = 8-7-6, etc.), a sum = 9 signal will never be received for column 7, therefore, the type bar will travel to its maximum position (12) where an appropriate symbol will print (in this case an *).

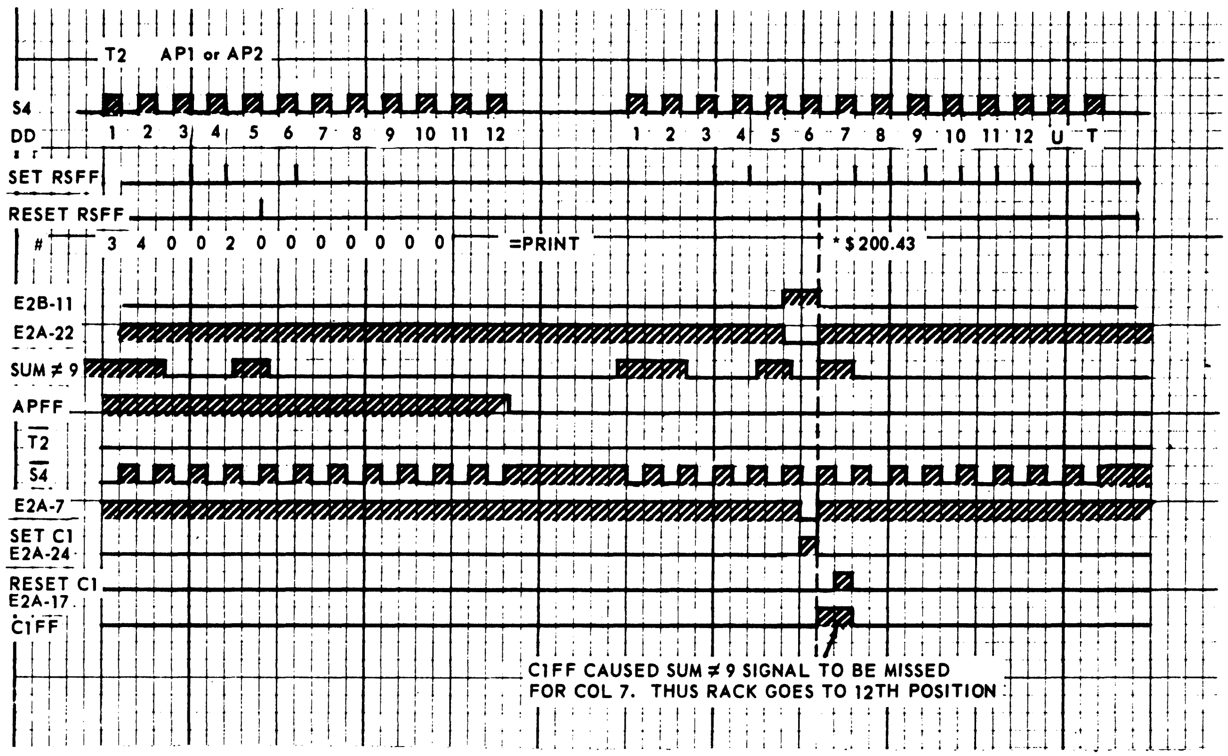


Fig. VII-29

The set CIFF signal (refer to Logic Page 125) is inhibited whenever any one input signal to OR gate E2A is high. ($\overline{T2}$ during any other T time, or APFF during $ search, or $\overline{S4}$.) The only time CIFF may be set is when the FF (and DD) that was set on the $ sign search causes Inverter E2A-22 to go low. The sum ≠ 9 will be low at this time because another zero has been read.

The -4.25V on pin 2 of gate E2B will prevent setting CIFF if column 3 had been set on the $ sign search. If not inhibited and a zero were in column 3 and 4, the CI signal would be added to the column 4 zero during the "zero" search and that rack would go to the 12th position.

EXAMPLE

# in memory	0	0	0	0	0	6	5	0	0	0	0
$ search				This Rack	$				0	0	0
0 search	0	0	0	Goes To Type Posi- tion #12	(CIFF)			0			

OR gate E2A-17 causes the CIFF to be reset after CI has been high for a one column search.

NOTE: The level 2 jumper wires from E2A04 to E2A05 and E2A26 to E2A27 (page 125) must be removed when this feature is activated.

AP STYLE 2

The logic for AP Style 2 is identical to Style 1 except for two points:

1. The -4.25V is removed from E2B-2 to allow a double character print from columns 3 and 4. Column 3 contains a $ sign in its top type position instead of a zero as on standard construction.
2. $\overline{\text{RSFF3}}$ is added to B2B-27 to prevent setting any more insignificant columns FF's during $ sign search if Rack Stop 3 sets.

AP STYLE 3

This feature allows a $ sign in amount column 12 to print, when programmed, along with * in all insignificant columns 11 thru 4.

It is activated by removing the wire from B2C-22 to B2B-28 (page 125).

Removal of this wire allows the set of rack stop FF's for all columns containing a zero during $ sign search. A RSFF reset is still made of all set FF's if a significant digit is detected, the same as a basic $ sign search.

AUTOMATIC ITEM INPUT STYLE 2

The Automatic Item Input Style 2 (AI) feature allows the auto reader to be used to enter data into the E2000 after a ledger sheet has been read in the carriage. The carriage camshaft will be at 216° of its cycle at this time. A separate stop is required for each data sheet read in the auto reader. The only limitation as to the number of data sheets used in the auto reader with each account is the number of stops that can be programmed into the panel. The same number of data sheets must be used with every account posted. If no data is to be entered in certain stops on various accounts, data sheets containing all zeroes must be read by the auto reader in these positions.

LOGIC OPERATION

A ledger sheet will feed from the auto reader when the carriage camshaft is at 216° under the following conditions:

1. The carriage must enter a stop position under RPT or a motor bar must be depressed in the stop position.
2. A ledger must be in the ready station of the auto reader.
3. FL and RL must be programmed.
4. The auto reader must be on and auto feed switch depressed.

PTFF·FL·CLK ———	Set FLFF	305
RL·ARP ON·FL·FLFF ———	FEED	305
FEED·$\overline{\text{BC}}$·$\overline{\text{POFF}}$ ———	AR CONTROL	319
$\overline{\text{POFF}}$·ARP ON·FL ———	LU SL	319
LU SL ———	LOCK RELAY	133
$\overline{\text{IND}}$·$\overline{\text{ERFF}}$·$\overline{\text{LOCK}}$·AR CONTROL·RSTAFF·AFFF ———	DROP I	354
IDN SOLAR CELL ———	I DN signal	354
ST/RD SOLAR CELL ———	ST RD signal	354
RSTAFF·ST RD·$\overline{\text{CCFF}}$·IDN·AFFF---PS ———	START READ	353
START READ·AR CONTROL ———	SET RL	309
$\overline{\text{RLFF}}$·RL·SET RL·CLK ———	SET RLBFF	309
RLBFF·CLK ———	Set RLFF	309
RLBFF·CC5·$\overline{\text{ERFF}}$ ———	RESET·RESET SL	307

Read Amp Pulses•RSTAFF•ST RD•$\overline{\text{CCFF}}$	Auto Reader READ AMP X and Y	356
Read Amp X•$\overline{\text{FF16}}$•FF3X	TRIGGER 6 ms DMV	306
FF3X•6 ms DMV times out	Set FF16	306
FF16•RLBFF•DDO	Reset RLFF EORD	309 309

When TB is programed

EORD•$\overline{\text{ERFF}}$•$\overline{\text{CC}}$•LANE 53	Set TBFF	320
Reset TBFF•FEED•CC5	PRESET	307
PRESET•$\overline{\text{ERFF}}$•CLK	Set POFF	307
$\overline{\text{POFF}}$•ARP ON•FL	Drop LU SL signal	319
$\overline{\text{LU SL}}$ signal	Drop LOCK RELAY to allow machine cycle	133

When TB not programed

EORD•$\overline{\text{LN53}}$•FEED•CC5	PRESET	307
PRESET•$\overline{\text{ERFF}}$•CLK	Sets POFF	307
$\overline{\text{POFF}}$•ARP ON•FL	Drop LU SL signal	319
$\overline{\text{LU SL}}$•signal	Drop LOCK RELAY to allow machine cycle	133

ERROR ROUTINES

A read error when detected will set ERFF. If AFFF is set, there will be a ledger in the Ready Station of the Auto Reader. Depression of the Read Light switch will reset ERFF, set STOP FF and CCFF and the ledger in the Read Station will be fed into the receiving hopper, without reading the ledger. The LU SL signal will remain high and the printer will not cycle. Both ledgers may be replaced in the Feed Table in proper sequence and another read attempted.

This is accomplished under control of the following logic:

Carriage camshaft at 216° - ERFF - $\overline{\text{CRG OPEN}}$ - FPS

ERFF•CLK	RESET RLFF	309
ERFF•$\overline{\text{RLFF}}$•$\overline{\text{VFF}}$	Read Light	322

ERFF•AR Control•$\overline{\text{IDN}}$•CLK	Set DDFF	355
Depress Read Light Switch	EJ KEY signal	513
EJ KEY•READ LIGHT•CRG OPEN	EJFF doesn't set as carriage is closed	320
$\overline{\text{FPS}}$•EJFF	Program Cam FF doesn't set	304
EJ KEY•CC5 READ LIGHT•CLK	Reset ERFF	321
EJ KEY•DDFF	DD CLR	354
DD CLR•CLK	Set CC FF	354
	Set STOP FF	355
STOP FF•CLK	Reset AFFF	353
$\overline{\text{IDN}}$•DDFF•EJ KEY	DROP I	354
IDN•STOP FF	Reset DDFF	355

When a ledger fails to read in the Auto Reader it may be necessary to remove the ledger from the carriage tray and the associated ledgers in the Auto Reader. The operator could then continue with the next set of ledgers. This is accomplished in the following manner. While the read light is on, open the carriage. When the carriage is open remove the ledger sheet, then depress the read light switch and the camshaft will then go to 0°:

Carriage camshaft at 216° - Read light - FPS

READ LIGHT — I — $\overline{\text{LOCK}}$•FPS	Drop Carriage Lock Solenoid	304

Manually open carriage and remove ledger.

Depress the read light switch.

READ LIGHT•EJ KEY•CRG OPEN•CLK	Set EJFF	320
EJFF•CLK	Set CGE MOTOR FF	304
EJFF - 100 ms DMV•CLK	Set PDFF	305
EJFF•$\overline{\text{FPS}}$•CC1•CLK	Set PROG.CAMFF	304

The camshaft then cycles home.

VERIFICATION LIGHTS

Failure to verify causes the Verification Lamp to illuminate. The machine will not cycle and the Auto Reader stops. By visually comparing the number on the input ledger, now in the receiving hopper of the Auto Reader, with the number indexed on the Keyboard, the type of error may be determined.

Failure to verify can be caused by either having the wrong number indexed on the Keyboard or reading the wrong input ledger in the Auto Reader. In either case the error correction routine is the same when the Verify Light switch is depressed. When the Verify Light switch is depressed, the ledger in the Auto Reader Ready Station will be fed into the receiving hopper. Both ledgers (the ledger that caused the Verify Light and the ledger fed when the Verify Lamp switch was depressed) are then replaced in order in the Auto Reader Feed Table and the operation is repeated with the correct number indexed on the keyboard for the ledger being read in the Auto Reader.

Failure to verify will cause ERFF to set. ERFF will prevent POFF from setting and Lock Relay will remain picked blocking a machine cycle.

Logic Operation

VFF	LU SL	319
SUM$\neq$9.VFF•SC•$\overline{\text{EJFF}}$•CLK	Set ERFF	321
ERFF•AR CONTROL.$\overline{\text{IDN}}$.CLK	Sets DDFF	355
Depress Verify Lamp Switch	EJ KEY	513

EJ KEY will cause the ledger in the ready station to be fed, using the same logic as the read error correction routine.

VFF will be reset when the next ledger is read in the Auto Reader by:

RLBFF•CC5	Reset SL	307
Reset SL	R1	106A-B
R1	Resets VFF	320

FLIP-FLOP INDEX

Designation	Schematic Page	Name	Functions
AFFF	353	Auto Feed	Controls automatic feed for forms from A4002 auto reader.
ALFF	138	--	Card future use.
ALIGN FF	304	Align	Controls line find when programed.
AMFF	135	Automatic Mode	Provides control signal during AEC operations.
APFF ($)	125	Amount Protection	Controls search for dollar signs.
BCFF	320	Blank Card	Controls blank card operation.
BEFF	140	Bounce Eater	Eliminates electronic noise when typing to or from memory.
BOLPFF	323	Beam of light pulse	Converts 18 usec BOL solar cell signals into 12 usec clock duration pulses when paper drive clutch is engaged.
CCFF	354	Clipped corner	A control that determines if a form is not to read from A4002 auto reader.
CFMFF	119	Change factor mode	Permits selection of memory location 02 instead of 00 during multiply or divide when lane 46D is programed.
CHARFF	126	Character	The character flip-flop controls the release of the rack stop clapper for the character column.
CIFF	122	Carry in	Provides a means of carrying from one digit to another on an arithmetic operation and as a control or storage flip-flop on other operations.
CLFF	307	Count Ledger	Permits the counter to be advanced by the step counter signals.
CMATFF 1,2,4,8	134	Count Memory Address tens	CMAU and CMAT flip-flops select the memory address on an all total operation. The flip-flops are counted consecutively from 00 to 29 (39) (79) (99) by the END OP signal.

FLIP-FLOP (Cont'd)

Designation	Schematic Page	Name	Functions
CMAUFF 1,2,4,8	134	Count Memory Address Units	CMAU and CMAT flip-flops select the memory address on all total operation. The flip-flops are counted consecutively from 00 to 29 (39) (79) (99) by the END OP signal.
COMPFF	123	Complement	Controls the addition of complements on arithmetic operations and is used as a control flip-flop on other operations.
CPFF	310	Complement Pulse	Permits every alternate USMVFF pulse to be written as a complement pulse on the stripe during the WL operation.
CRGMOTORFF	304	Carriage	Permits carriage motor relay K1109 to be picked or dropped to control the carriage motor.
COUNT XFF	309	Count X	1. Permits the SRCX FF to be counted each time a complement pulse is read from the stripe. 2. Permits the data in the SRXFF's to be shifted. 3. Permits parity to be counted if data has been read after the last pulse. 4. Triggers writing of data to memory when all bits of a digit have been read.
COUNT YFF	309	Count Y	Same as CXFF except for Y stripe.
C1 FF C2 FF	354 354	Count One Count Two	Count down FF's used to detect the number of feed attempts on A4002 auto reader.
DATA XFF	309	Data X	Temporary storage for data bits read from the X stripe.
DATA YFF	309	Data Y	Same as data XFF except for Y stripe.
DDFF	355	Double Document	A control to stop the operation if double feed occurs on A4002 auto reader.
DDREVFF	117	Digit Distributer Reverse	The Digit Distributer Reverse flip-flop is used during the shift and multiply operation to reverse the order of selection of data digits by the DDFF's from the memory.
DDOFF thru DDMSDFF DDUFF and DDTFF	107 108	Digit Distributor Zero thru MSD Units & Tens of Memory	The digit distributor flip-flops select the active digit from memory, or the keyboard column on a keyboard entry.

FLIP-FLOP INDEX (Cont'd)

Designation	Schematic Page	Name	Functions
DMSDFF	108	Most Sifnificant Digit	The most significant data digit (col. 12)
DISCRIMXFF	309	Discriminator X	Separates the complement X and data X pulses read from the X stripe.
DISCRIMYFF	309	Discriminator Y	Same as discrimnator X only for Y stripe.
DVFF	129	Divide	Provides signal for divide operation.
ECNCFF	133	Electronic Cycle Not Complete	Locks machine if the electronic unit does not complete the required T times.
EJECTFF	320	Eject	Provides the necessary control circuits for restoring the machine to normal when an error condition occurs.
EOWFF	138	End of Word	Card, future use.
ERROR FF	321	Error	Provide lock circuits and light circuits when various stripe ledger errors occur.
ED FF	356	Feed Form	Used to cause the feed solenoid to energize on A4002 auto reader.
FF	308	Flip Flop	Provides control circuits for the counter flip-flops.
FF1X	311	Flip Flop One X	1. During RL operation, permits X data to be written to memory first, if X stripe is leading. 2. During WL operation used as counter to write start signal on the stripe.
FF1Y	311	Flip Flop One Y	1. During RL operation, permits Y data to be written to memory first if Y stripe is leading, or if both stripes are read simultaneous. 2. During WL operation used as counter to write the start signal on the stripe
FF3X	313	Flip Flop 3X	1. Set by start signal on RL operation and permits the X data to be written to memory. 2. Controls writing of the start signal on WL operation.

FLIP-FLOP INDEX (Cont'd)

Designation	Schematic Page	Name	Functions
FF3Y	313	Flip Flop 3Y	1. Set by start signal on RL operation and permits the Y data to be written to memory. 2. During WL operation is used as Y stripe write monitor FF.
FF4	306	Flip Flop 4	1. During WL is used as the X stripe write monitor FF and the line find write FF.
FF6	313	Flip Flop 6	Synchronizes the stripe ledger operations with the E2100 clock.
FF9X	311	Flip Flop 9X	Controls the direction of X head current during WL operation.
FF9Y	311	Flip Flop 9Y	Controls the direction of Y head current during WL operation.
FF16	306	Flip Flop 16	1. During RL the 6MSDMV will set FF16 indicating the end of data on the X stripe. 2. Permit sync pulse to stop the form at L-8.
FFZ	313	Flip Flop Z	Control flip-flop used during RL and WL to determine the active X or Y logic.
IIFF	310	Initial Installation	Controls the initial installation logic.
KBFF	138	Keyboard	Card, future use.
KIFF	138	Card In	Card, future use.
L-2	306	Line Minus 2	Indicates the position of the form as it is being driven out of the carriage.
1,2,4,8,16, 32FF's	308	Ledger Count	Used to count lines as the form is driven in during BC, and out from L-8 during RL and WL. Also used for speed check during WL.
LFAFF	305	Line Find A	1. Permits a one line delay on line find write. 2. Used as a counter on line find read.
LFBFF	305	Line Find B-	1. Used only on RL. LFA and LFB count 2 lines after the line find pulse. The clapper for the PD clutch is then activated.
LN3FF	135	Lane 3	Permits indexing of lane 3 carriage controls from status of A or B.
LWLFF	306	Lane Write Ledger	Retains the write ledger instruction after the carriage has moved out the WL position

FLIP FLOP INDEX (Cont'd)

Designation	Schematic Page	Name	Functions
MAFF	133	Memory Address	Signifies invalid memory address.
MART1FF MART2FF MART4FF MART8FF	115	Memory Address Register Tens	Used to alter programmed memory addressed.
MARU1FF MARU2FF MARU4FF MARU8FF	116	Memory Address Register Units	Contains the units of memory address for the RL and WL operations.
MR → MEMFF	112	Memory Register to Memory	Permits the data in the MRFF's to be written into memory.
MR1FF MR2FF MR4FF MR8FF	121	Memory Register 1,2,4,8, Bits	Special flip-flop which receives data read from memory.
NZFF	128	Non-Zero	1. Indicates clear or non clear condition of A or B during C arithmetic time. 2. Also used as a control flip-flop.
PAFF	133	Print Alarm	Indicates that the proper number of pulses were not received during print (T2) and that the print should be verified.
PDFF	305	Paper Drive	Permits the form to be moved during RL or WL operations.
PRINTER OPERATE FF	307	Printer Operate	A control used to indicate an acceptable RL has been performed.
PROGCAMFF	304	Program Cam	A control that permits the program camshaft to be rotated.
PRINTER TRIP FF	307	Printer Trip	1. Indicates when a motor bar is depressed or MB2 solenoid is energized. 2. Initials verify operation if programed.
PERMIT WRITE	310	Permit Write	Permits write amplifier current to flow thru the heads.
P1X FF P2X FF	312	Parity X	Counts data X pulses during a RL or WL operation.
P1Y FF P2Y FF	312	Parity Y	Counts data Y pulses during a RL or WL operation.
REVFF	305	Reverse	1. Permits forms to be moved into the carriage. 2. Reset condition permits forms to be moved out of the carriage.

FLIP-FLOP INDEX (Cont'd)

Designation	Schematic Page	Name	Functions
RLFF	309	Read Ledger	Controls the RL operation and is comparable to a "T" time.
RLBFF RSFF RSTA	309 125 354	Read Ledger B Rack Stop Ready Station Align	Prevents a partial clock pulse from starting RL logic control the release of the rack stop clappers used to signal the logic that a form is in the ready station A4002 auto reader.
SFF	132	Sign	1. Indicates the sign of A or B during C arithmetic. 2. Also used as a control FF.
SA1FF SA2FF SA3FF	128	Special Address	Permits memory addressing during logic operation.
SCFF	132	Special Control	Used for various control purposes.
S0FF S1FF S2FF S3FF S4FF S5FF S6FF S7FF S8FF S9FF	130 131	Sequence Zero thru 9	Sequence flip-flop to control the logic progression during each T time.
S10FF	131	Sequence 10	A logic sequence in which the memory address is counted up or down between words.
SAFF SBFF SCFF	317	Sequence A,B,C	Logic control sequences during RL and WL operations.
SQFF SSFF STFF SUFF	138 139 139 139	Sequence Q,S,T,U	Card, future use.
SWFF SXFF SYFF SZFF	139 139 139 139	Sequence W,X,Y,Z	Control logic sequence for TIM and TOM.
SFFF	353	Single Feed	Controls single feed of forms in the A4002 auto reader.
SRCX1FF SRCX2FF	314	Shifter Register Counter	Counts the number of shift of the X shift register.

FLIP-FLOP INDEX (Cont'd)

Designation	Schematic Page	Name	Functions
SRCY1FF SRCY2FF	314	Shift Register Counter	Counts the number of shifts of the Y shift register.
SRX1FF SRX2FF SRX4FF SRX8FF	109	Shift Register	Used for temporary storage for the X data on the RL and WL operations.
SRY1FF SRY2FF SRY4FF SRY8FF	315	Shift Register	Used for temporary storage for the Y data on the RL and WL operations.
STOP FF	355	Stop	A auto reader control FF used to stop the operation.
STOP STORAGE FF	305	Stop Storage	Indicates that the paper drive clutch should be dropped at the next BOLP signal.
SUM → MEMFF	112	Sum to Memory	Indicates that the adder output is to be written into memory.
SYMFF	126	Symbol	Controls the release of the rack stop clapper for the symbol column.
SYNCFF	308	Sync	Synchronizes the USMVFF signal with the BOLP signal for use in the counter circuit for counting lines of paper movement and form speed check during the WL operation.
TABFF	305	Tab	Provides a noise free signal that stays high until the carriage bounce has settled. The TAB FF is set by the IN TAB switch and reset when the TAB relay drops.
TBFF	320	Trial Balance	Controls Block Add or Block Transfer operation in the same manner as the T5FF does in the E2100. FBFF is set at the end of reading data if no error is encountered and Align is not pinned TBFF is reset when all the data has been added or transferred.
TOFF thru T7FF	129	Time	The time flip-flop controls the various operations of the arithmetic and memory unit. TO - Shift & round. T1 - Transfer T2 - Print. T3 - A arithmetic. T4 - B arithmetic. T5 - C arithmetic. T6 - Clear. T7 - Multiply or divide.

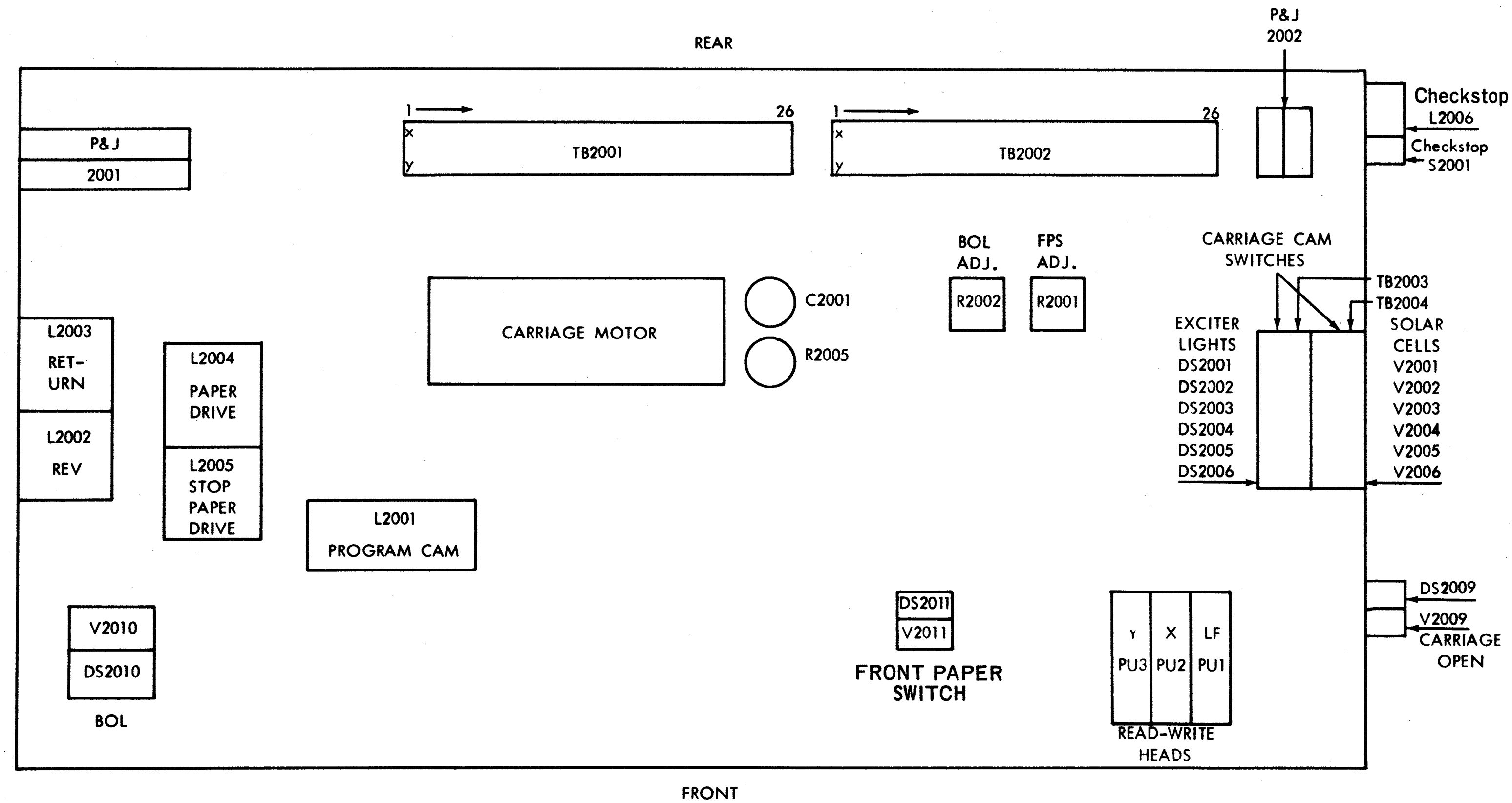
FLIP-FLOP INDEX (Cont'd)

Designation	Schematic Page	Name	Functions
TIM FF	140	Type into Memory	Controls typing into memory.
TOM FF	140	Type out of Memory	Controls typing out of memory.
TTC FF	140	Typewriter Timing Cam	Noise isolation to prevent double search of memory for digit.
USMVFF	308	Unsyncronized multi vibrator	Provides a 12 us pulse that is synchronized with clock.
VFF	320	Verify	Controls the verify operation similar to a "T" time.
WLFF	310	Write Ledger	Controls the writing of data on the stripes. It is equivalent to a "T" time.
WR1FF WR2FF WR4FF WR8FF	111	Working Register 1,2,4 & 8 bit	The Working Register flip-flop provides storage location for data as an operation progresses. WR is always a input to the adder.

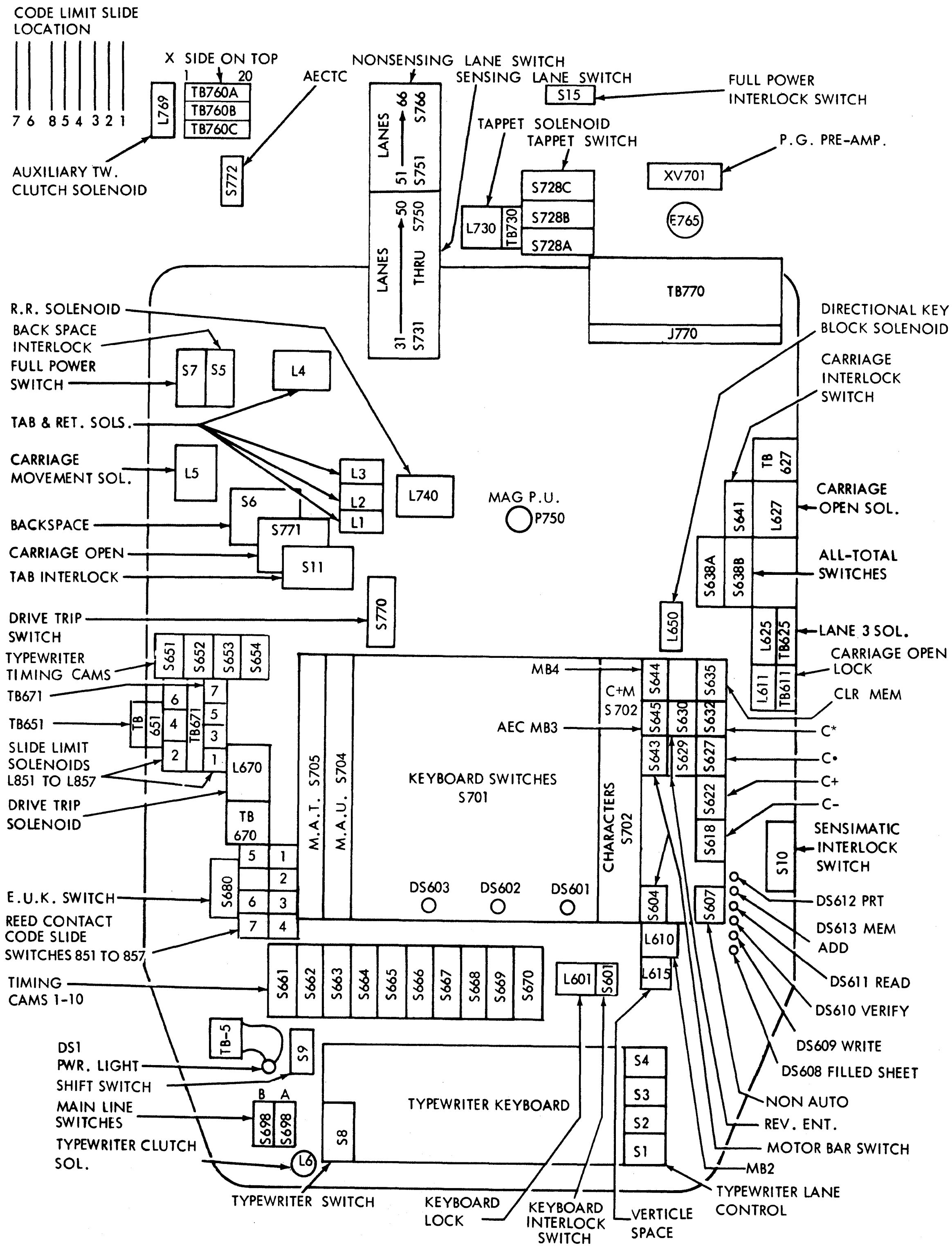
COMPONENT INDEX

INDEX	PAGE NUMBER UPPER GATE E2150 100 PRINTS	LOWER GATE E2150 300 PRINTS	KEYBOARD PRINTER E2150 500 PRINTS
CARRIAGE TIMING CAMS		323	
CARRIAGE TRAY, SOLENOIDS & COMP.		330	
CARD LOCATION CHART	149-150-151	329-330-358	
ERROR GATING		321	
FUSES	154		502
LOGIC FLOW CHARTS			
1. T1 thru T7	141 thru 147		
2. TIM	147		
3. TOM	147		
4. II, V, WL, RL, TB, BT		324 thru 328	
P. & J CONNECTOR INDEX	155	333	333
RELAYS	154		517
SOLAR CELLS		330	
SOLENOIDS		330	516
SWITCHES	154	330	516
SIGNALS BETWEEN UPPER AND LOWER GATE	156		
TB770 COMPONENTS			516
TB901 COMPONENTS			516

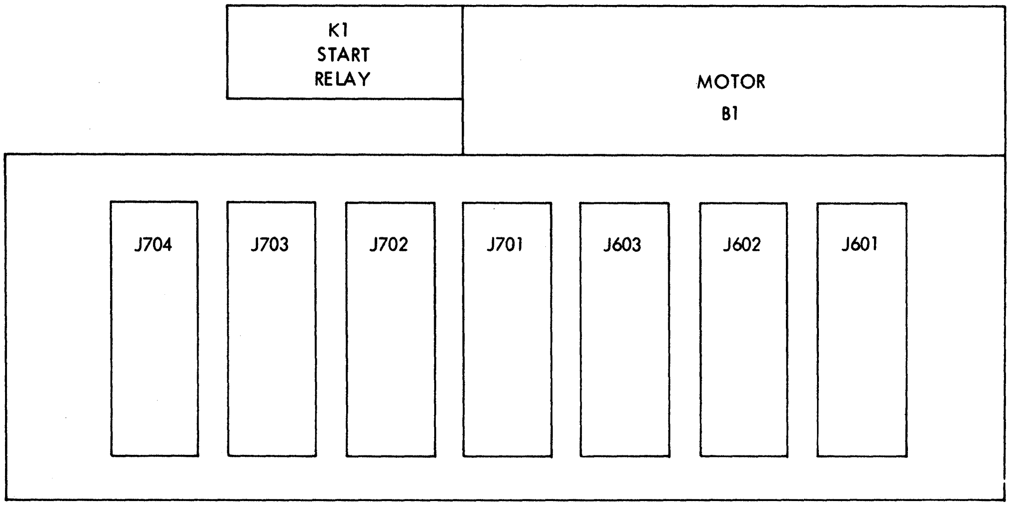
CARRIAGE PAPER DRIVE UNIT COMPONENT LOCATIONS (TOP VIEW)

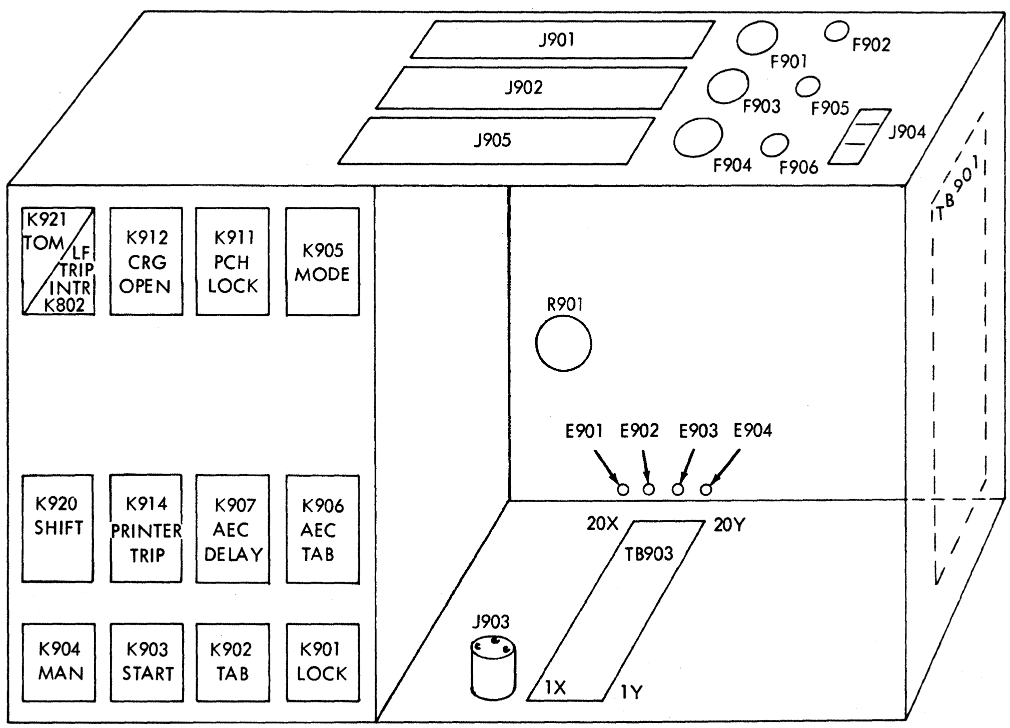


KEYBOARD - PRINTER COMPONENT LOCATIONS

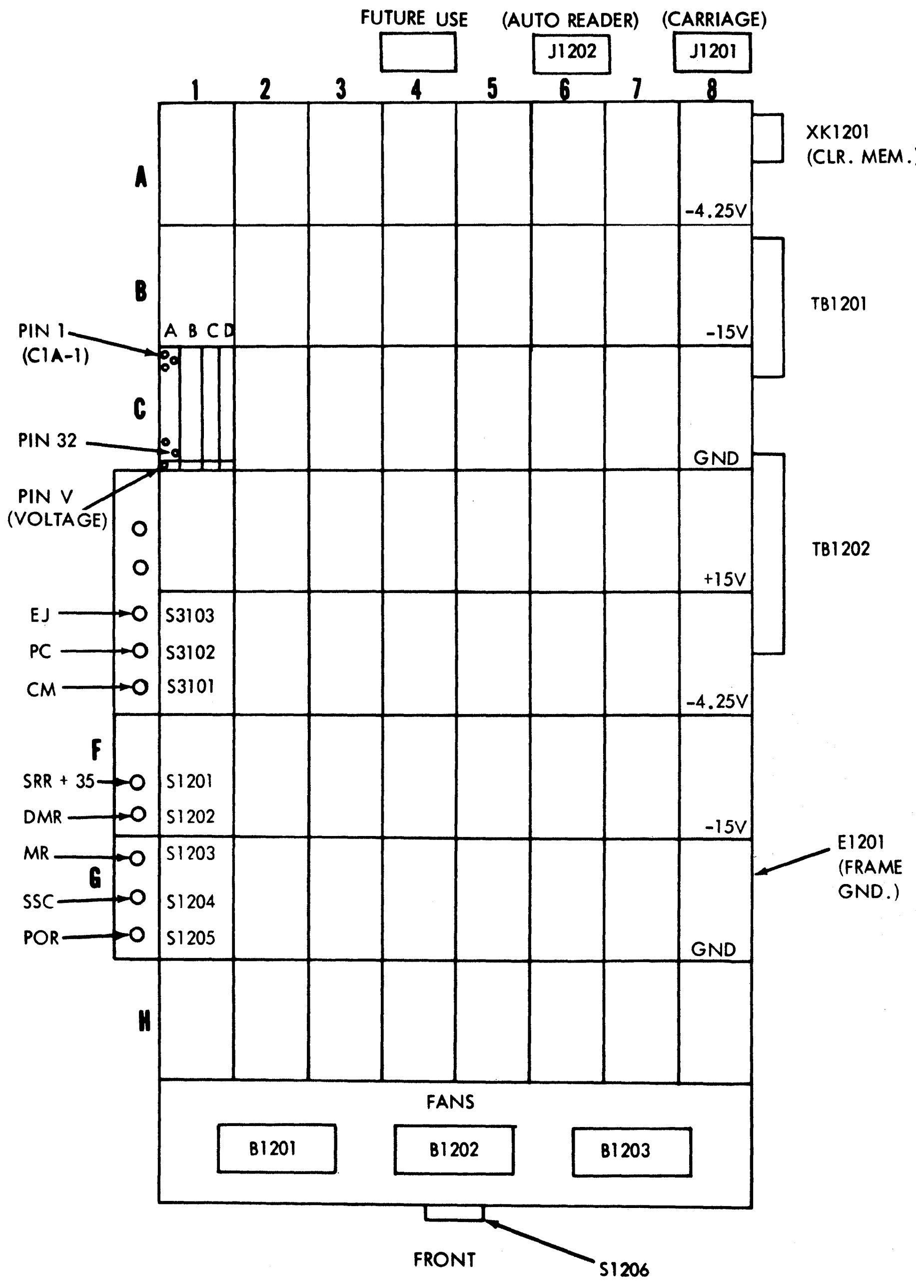


REAR VIEW - PRINTER CONNECTORS





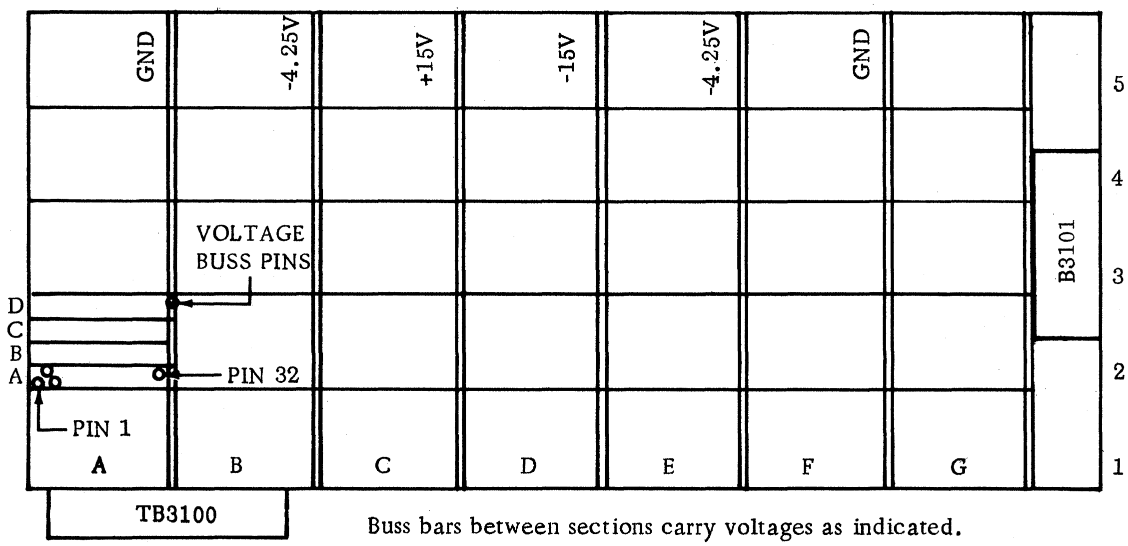
E2150 PROCESSOR UPPER GATE WHEN TILTED



BUSS BARS BETWEEN SECTIONS CARRY VOLTAGES AS MARKED

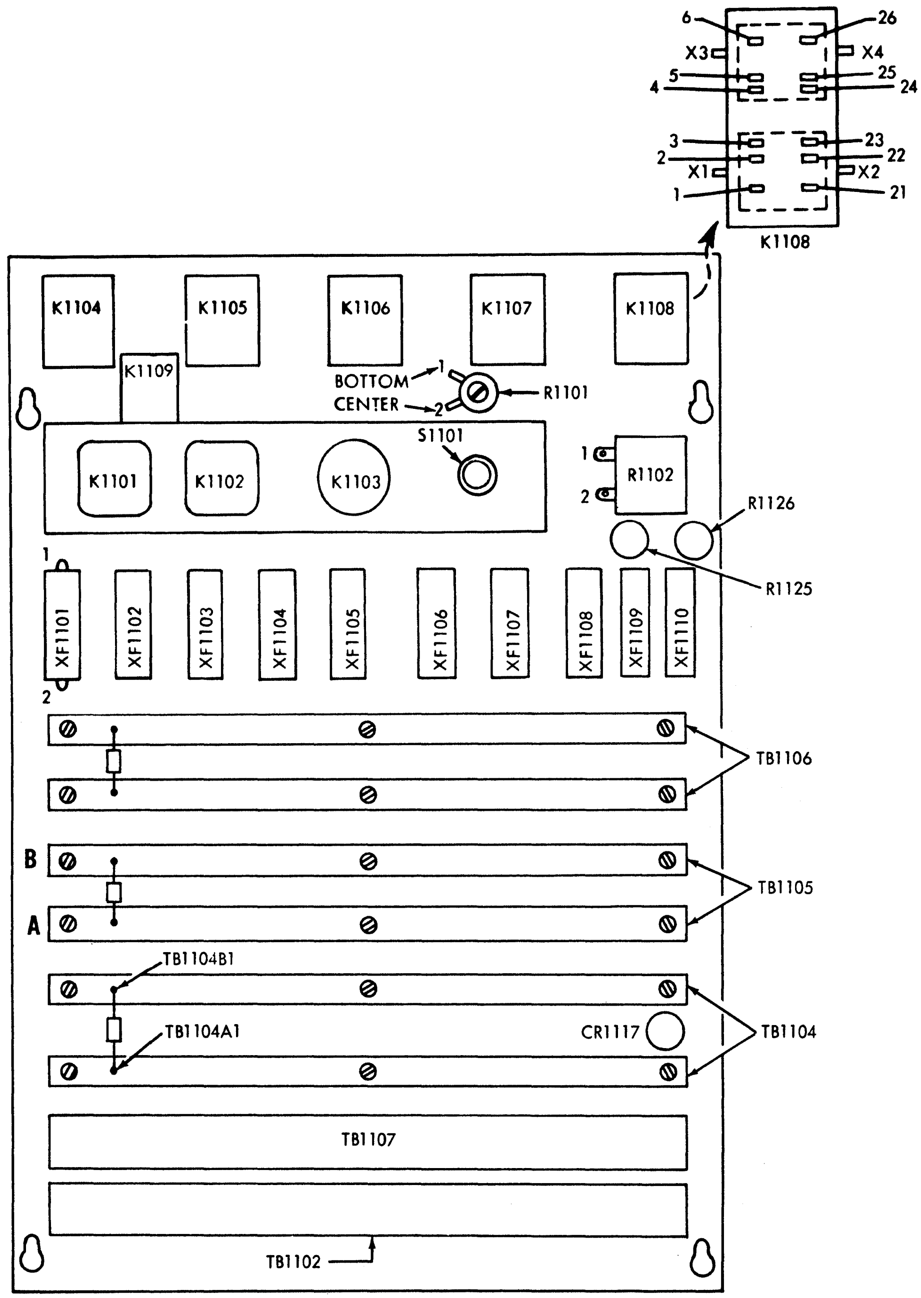
LOWER GATE E 2150

LEFT SIDE VIEW TILTED DOWN

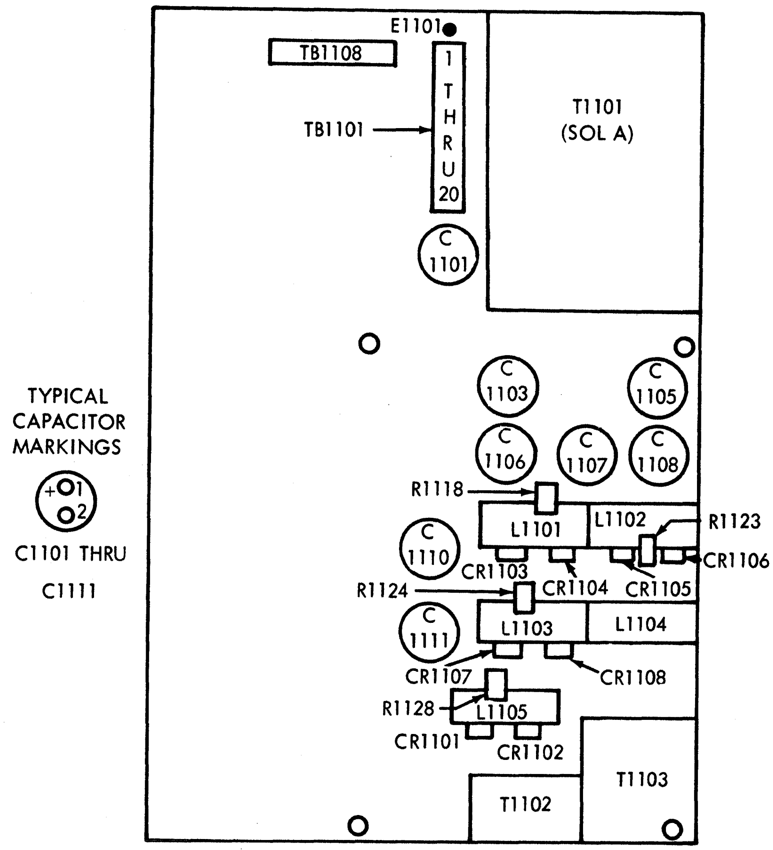


Buss bars between sections carry voltages as indicated.

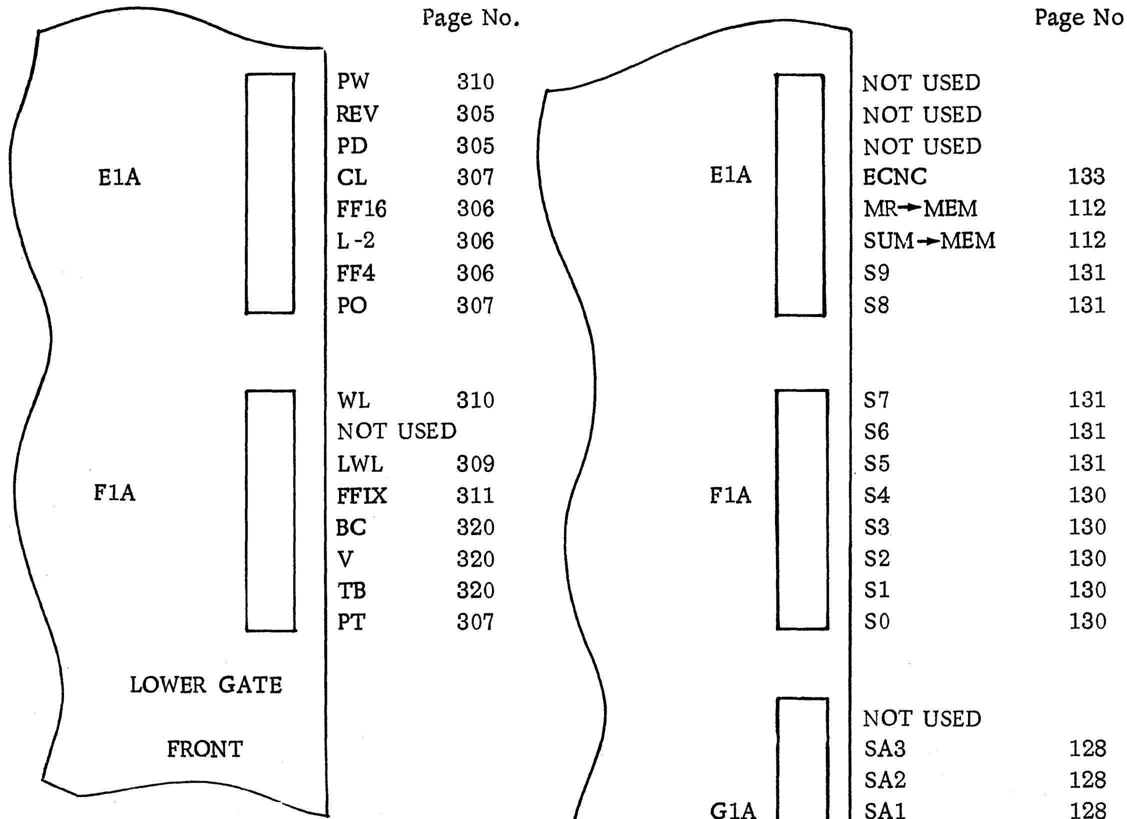
E2150 PROCESSOR POWER SUPPLY COMPONENTS AND RELAYS



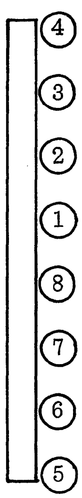
E2150 PROCESSOR POWER SUPPLY TRANSFORMERS,
CHOKES & CAPACITORS



INDICATOR LIGHT LOCATION CHART E2150



Back plane
pin location
for indicators



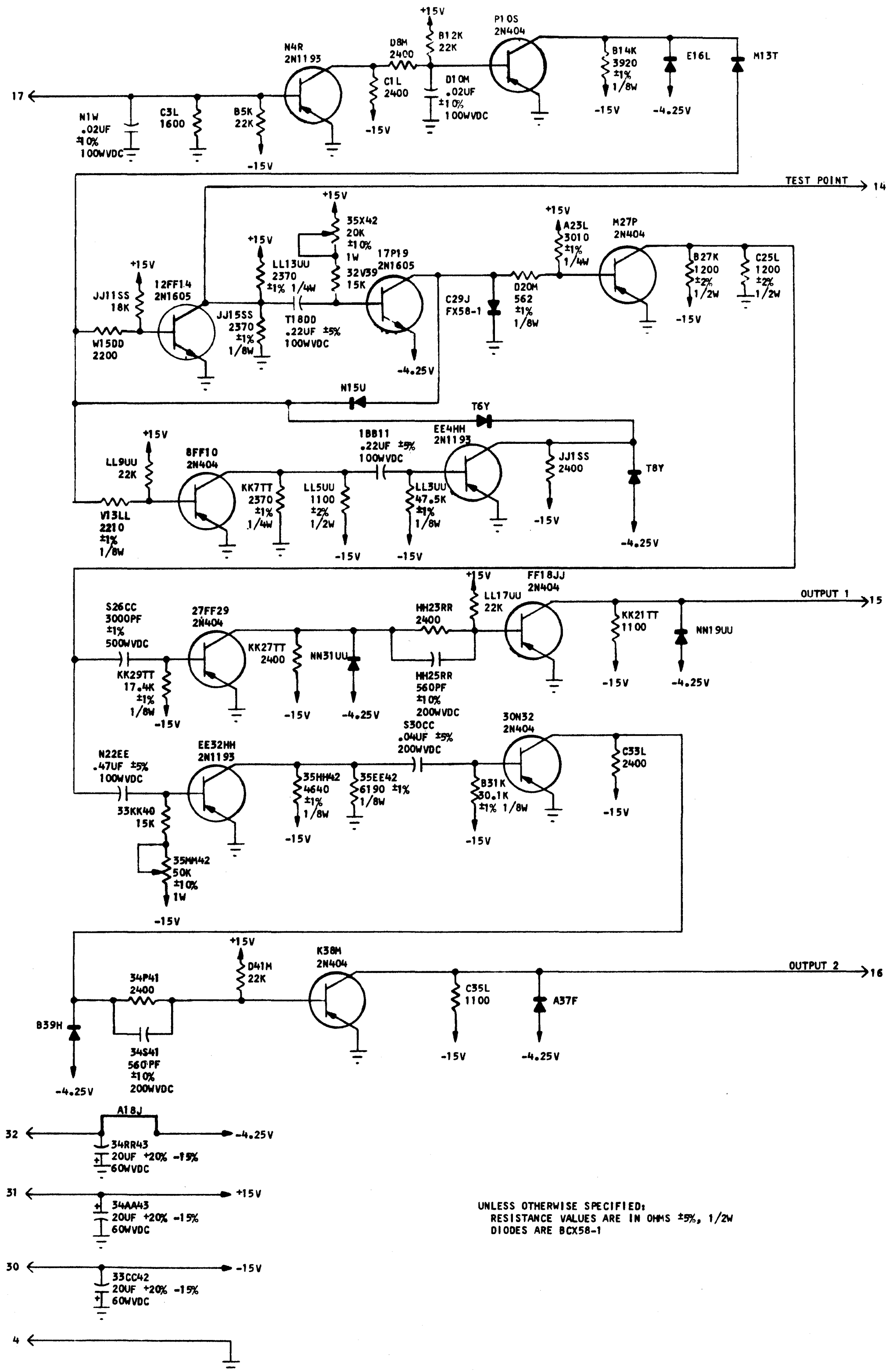
(SIGNALS AND TERMS E2150)
(Refer to E2100 Instruction Book Section VIII
for all E2110 Signals and Terms)

Auto Cycle	307	A signal developed from the restored condition of a latch down key on the keyboard. It provides automatic operations after a feed ledger operation.
A S R X	319	Allow shift Register X.
B O L	323	Beam of light - an 18 ms pulse generated by the solar cell and 1/10 wheel.
B O L P	323	A 12 us pulse generated by B O L and clock.
CC1 CC2 CC3 CC4 CC5 CC6	323	Carriage control cams used to control paper handling logic.
Check Stop Sol	307	Activates the check stop limits on Style 10 carriage.
Clock	106	A free running multivibrator used for timing electronic logic.
Crg Lock Sol	307	A Solenoid that block the depression of the carriage open close key during stripe ledger operations.
Crg Open	323	Indicates the carriage is open.
DMV		Delay multivibrator used to control electronic logic.
6 MS	106	
70 US	313	
100 MS	305	
100 MS	307	
370 US	308	
490 US	309	
1200 US	316	
D P	313	A inverted $\overline{FF6}$ signal.
E O R D	309	End of read.
F P S	323	Front paper switch. A solar cell and light to detect the presence of a form in the carriage.
F S lamp	322	A signal to indicate a filled sheet.

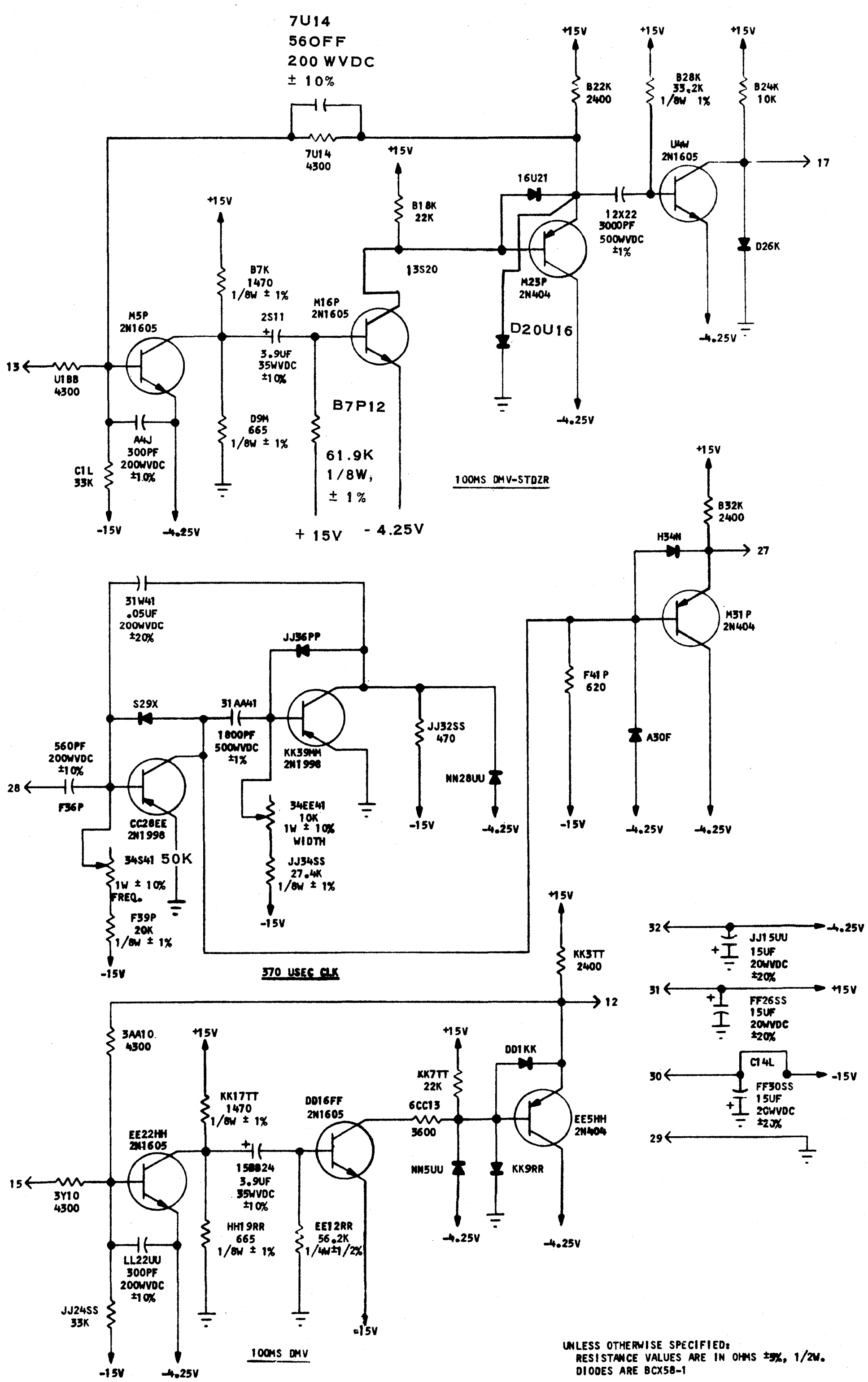
GT SR → WR	110	A signal to control the gating of information in the SRXFF's to the WRFF's.
GT SRY 1,2,4,8 → WR	319	Controls gating information from SRYFF's to the WRFF's.
GT WR → SRX SL	319 (109)	Gating control signal for transfer of information from the WRFF's into the temporary storage SRXFF's.
LC2	307	Ledger count 2. A signal that comes high at line minus 6 during a Blank Card operation.
L F R A	306	Line find read amplifier. A signal used to control setting of LFA FF.
L F Write Amp	306	Write amplifier for line find.
L U S L	319	Lock up striped ledger. Causes a lock condition of the keyboard printer.
M A C	135	Memory address C. A feature to permit memory address selection from column 11 and 12.
M A R U 1,2,4,8	116	Memory address register units.
MB-2	307	A solenoid that activates motor Bar 2.
MOD MAR	115	A signal used in conjunction with MAC for resetting of the MART and MARU FF's.
READ AMP X READ AMP Y	316 316	An amplified pulse read from the stripe.
READ LAMP	322	A signal to indicate a read error.
RESET SL	307	Produces R1 pulse to reset Flip Flops during striped ledger operations.
RS	106	Reset standardizer. Produces R1, R2, and delay MR pulses which are used for resetting flip-flops.
SET AAD SET BAD SET CAD SET PAD SET DAD	127 127 127 127 127	Special address signals used for memory selection of A,B,C, P or D.
SET FF1X SET FF1Y	311 311	Signals used for skew error detection.
SHIFT RELAY	510	A control to prevent resetting of TIM FF when K4 is depressed.

Slide 1	140	A signal from the solenoid drivers to the code slides solenoid.
Slide 2	140	
Slide 3	140	
Slide 4	140	
Slide 5	140	
Slide 6	140	
Slide 7	140	
SL	304	Striped Ledger - A signal produced by programming. Indicates a striped ledger operation.
Step Ctr	308	Step Counters. A signal used to advance the form speed check counter.
TC 10	307	Timing Cam 10. A control used for form travel.
TDA	135	Ten digit arithmetic.
TTC 1 and 2	140	Typewriter timing cam 1 and 2 controls digit selection during type into and from memory.
VER LAMP	322	Indicates invalid verification.
VERT SPACE SOL	140	A vertical space control read from the strip.
WMX and Y	316	Write monitor X and Y. A pulse emited when the correct current flows thru the head used for write error detection.
WRITE X and Y AMP	311	Causes current to flow in the heads during a write operation.
WRT LAMP	322	Write lamp indicates a write error.
W S	323	Write sync - a pulse used to control the writing of a sync pulse between line minus 6 and line minus 7 of the X stripe.

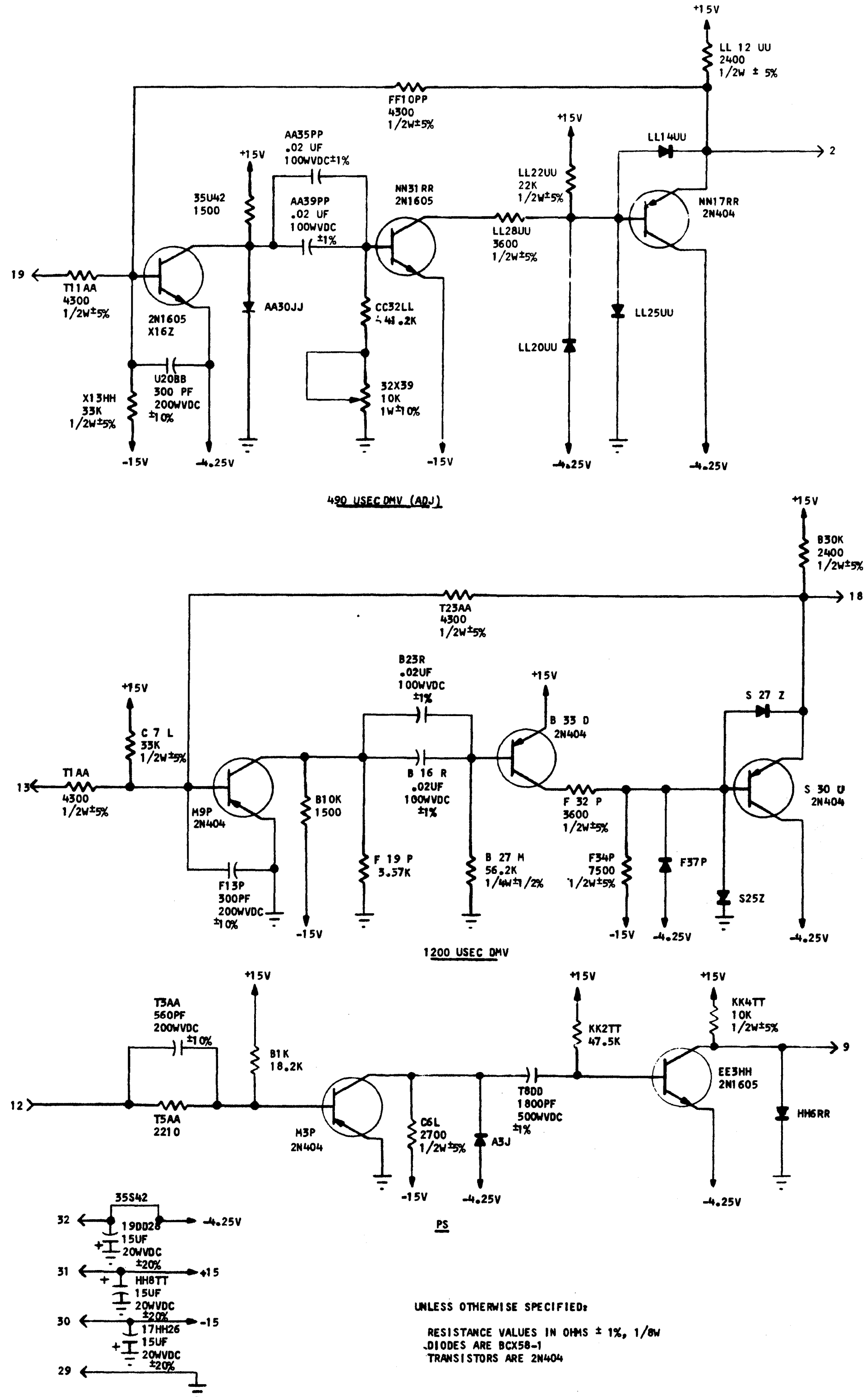
B.O.L.A.


+15V
B12K
22K
P10S
2N404
N4R
2N1193
D8H
2400
C1L
2400
D10H
.02UF
±10%
100WVDC
B14K
3920
±1%
1/8W
E16L
M13T
-15V
-4.25V
17
N1W
.02UF
±10%
100WVDC
C3L
1600
B5K
22K
TEST POINT
14
35X42
20K
±10%
1W
17P19
2N1605
32V39
15K
LL13UU
2370
±1% 1/4W
T18DD
.22UF ±5%
100WVDC
JJ11SS
18K
12FF14
2N1605
JJ15SS
2370
±1%
1/8W
W15DD
2200
C29J
FX58-1
D20H
562
±1%
1/8W
A23L
3010
±1%
1/4W
M27P
2N404
B27K
1200
±2%
1/2W
C25L
1200
±2%
1/2W
N15U
T6Y
18B11
.22UF ±5%
100WVDC
EE4HH
2N1193
LL9UU
22K
8FF10
2N404
V13LL
2210
±1%
1/8W
KK7TT
2370
±1%
1/4W
LL5UU
1100
±2%
1/2W
LL3UU
47.5K
±1%
1/8W
JJ1SS
2400
T8Y
S26CC
3000PF
±1%
500WVDC
KK29TT
17.4K
±1%
1/8W
27FF29
2N404
KK27TT
2400
NN31UU
HH23RR
2400
HH25RR
560PF
±10%
200WVDC
LL17UU
22K
FF18JJ
2N404
KK21TT
1100
NN19UU
OUTPUT 1
15
N22EE
.47UF ±5%
100WVDC
33KK40
15K
EE32HH
2N1193
35HH42
4640
±1%
1/8W
35EE42
6190 ±1%
1/8W
S30CC
.04UF ±5%
200WVDC
B31K
30.1K
±1% 1/8W
30N32
2N404
C33L
2400
35HH42
50K
±10%
1W
D41H
22K
K38H
2N404
34P41
2400
34S41
560PF
±10%
200WVDC
B39H
C35L
1100
A37F
OUTPUT 2
16
A18J
32
34RR43
20UF +20% -15%
60WVDC
31
34AA43
20UF +20% -15%
60WVDC
30
33CC42
20UF +20% -15%
60WVDC
4
UNLESS OTHERWISE SPECIFIED:
RESISTANCE VALUES ARE IN OHMS ±5%, 1/2W
DIODES ARE BCX58-1

DMV - A

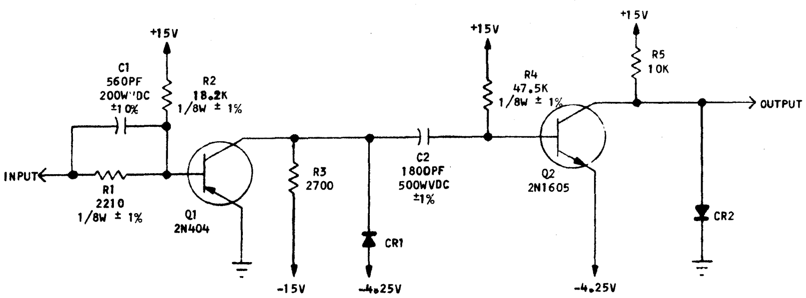

7U14
560FF
200 WVDC
± 10%
7U14
4300
+15V
B22K
2400
B28K
33.2K
1/8W 1%
B24K
10K
U4W
2N1605
17
16U21
12X22
3000PF
500WVDC
±1%
D26K
B18K
22K
13S20
M23P
2N404
D20U16
B7K
1470
1/8W ± 1%
M5P
2N1605
2S11
3.9UF
35WVDC
±10%
M16P
2N1605
13
U18B
4300
A4J
300PF
200WVDC
±10%
C1L
33K
D9M
665
1/8W ± 1%
B7P12
61.9K
1/8W,
± 1%
-15V
-4.25V
+ 15V
- 4.25V
100HS DMV-STDZR
B32K
2400
H34N
27
M31P
2N404
31W41
.05UF
200WVDC
±20%
JJ36PP
S29X
31AA41
1800PF
500WVDC
±1%
KK39MM
2N1998
JJ32SS
470
F41P
620
A30F
NN28UU
560PF
200WVDC
±10%
28
F36P
CC28EE
2N1998
34EE41
10K
1W ± 10%
WIDTH
34S41 50K
1W ± 10%
FREQ.
F39P
20K
1/8W ± 1%
JJ34SS
27.4K
1/8W ± 1%
370 USEC CLK
KK3TT
2400
12
32
JJ15UU
15UF
20WVDC
±20%
31
FF26SS
15UF
20WVDC
±20%
30
C14L
FF30SS
15UF
20WVDC
±20%
29
3AA10
4300
KK17TT
1470
1/8W ± 1%
DD16FF
2N1605
KK7TT
22K
6CC13
3600
DD1KK
EE5HH
2N404
EE22HH
2N1605
15
3Y10
4300
15B824
3.9UF
35WVDC
±10%
NN5UU
KK9RR
HH19RR
665
1/8W ± 1%
EE12RR
56.2K
1/4W±1/2%
LL22UU
300PF
200WVDC
±10%
JJ24SS
33K
100HS DMV
UNLESS OTHERWISE SPECIFIED:
RESISTANCE VALUES ARE IN OHMS ±5%, 1/2W.
DIODES ARE BCX58-1

DMV-B

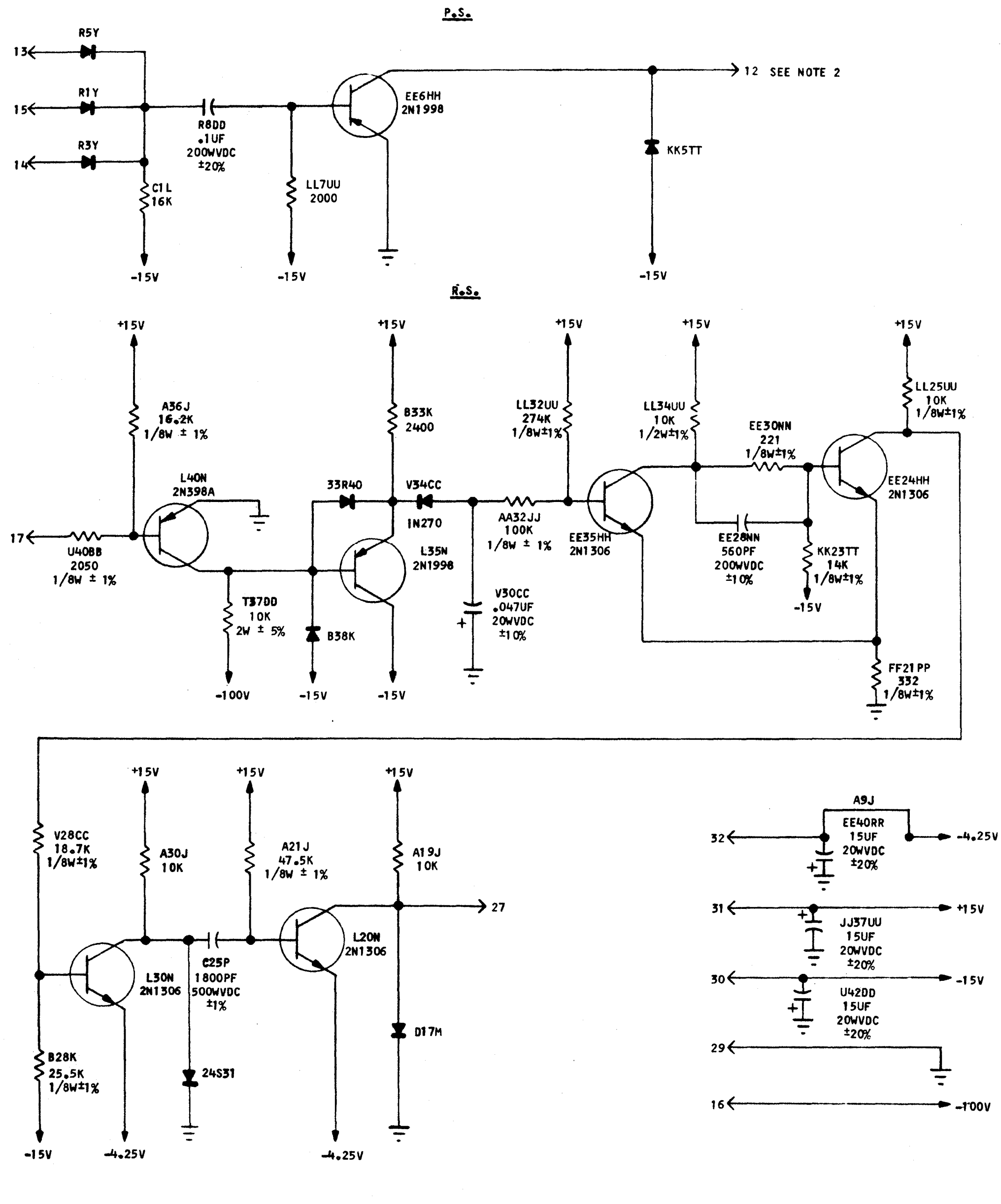


+15V
LL 12 UU
2400
1/2W ± 5%
FF10PP
4300
1/2W±5%
+15V
LL14UU
2
AA35PP
.02 UF
100WVDC±1%
+15V
35U42
1500
AA39PP
.02 UF
100WVDC
±1%
NN31RR
2N1605
LL22UU
22K
1/2W±5%
LL28UU
3600
1/2W±5%
NN17RR
2N404
19
T11AA
4300
1/2W±5%
2N1605
X16Z
AA30JJ
CC32LL
41.2K
LL25UU
LL20UU
U20BB
300 PF
200WVDC
±10%
X13HH
33K
1/2W±5%
32X39
10K
1W±10%
-15V
-4.25V
-15V
-4.25V
-4.25V
490 USEC DMV (ADJ)
+15V
B30K
2400
1/2W±5%
T23AA
4300
1/2W±5%
18
B23R
.02UF
100WVDC
±1%
+15V
B 33 D
2N404
S 27 Z
+15V
C 7 L
33K
1/2W±5%
13
T1AA
4300
1/2W±5%
M9P
2N404
B10K
1500
B 16 R
.02UF
100WVDC
±1%
F 32 P
3600
1/2W±5%
S 30 U
2N404
F13P
300PF
200WVDC
±10%
F 19 P
3.57K
B 27 M
56.2K
1/4W±1/2%
F34P
7500
1/2W±5%
F37P
S25Z
-15V
-15V
-4.25V
-4.25V
1200 USEC DMV
+15V
+15V
+15V
T3AA
560PF
200WVDC
±10%
B1K
18.2K
KK2TT
47.5K
KK4TT
10K
1/2W±5%
9
12
T5AA
2210
M3P
2N404
C6L
2700
1/2W±5%
A3J
T8DD
1800PF
500WVDC
±1%
EE3HH
2N1605
HH6RR
-15V
-4.25V
-4.25V
35S42
32
19DD28
15UF
20WVDC
±20%
-4.25V
31
HH8TT
15UF
20WVDC
±20%
+15
30
17HH26
15UF
20WVDC
±20%
-15
29
PS
UNLESS OTHERWISE SPECIFIED:
RESISTANCE VALUES IN OHMS ± 1%, 1/8W
DIODES ARE BCX58-1
TRANSISTORS ARE 2N404

DMV-C

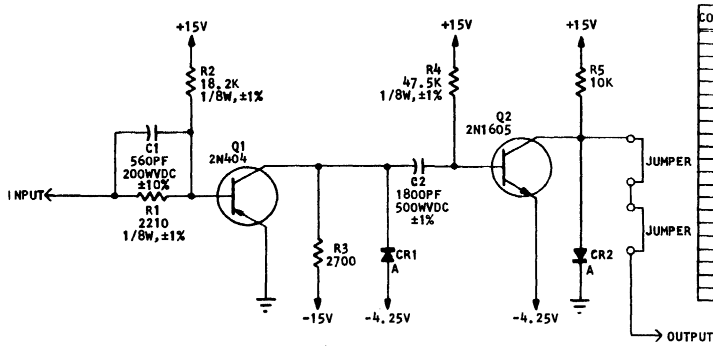


COMPS.	CKT. 1	CKT. 2
R1	V24CC	U18BB
R2	KK19TT	KK13TT
R3	KK15TT	KK9TT
R4	A15J	A7J
R5	A13J	A5J
C1	V26CC	U16BB
C2	S21CC	R12BB
CR1	LL17UU	LL11UU
CR2	D11M	D3M
Q1	EE16HH	EE11HH
Q2	L14N	L6N
INPUT	20	21
OUTPUT	26	25

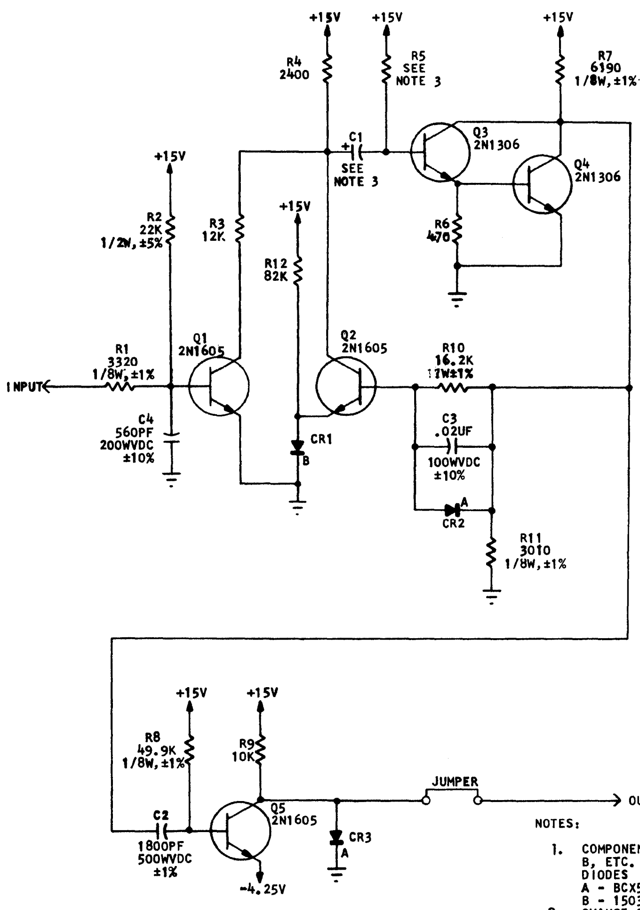


UNLESS OTHERWISE SPECIFIED:
RESISTANCE VALUES ARE IN OHMS ±5%, 1/2W.
DIODES ARE BCX58-1

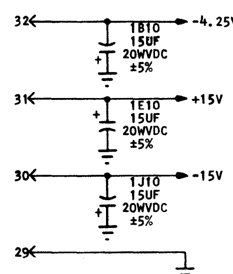
DMV-D



COMPONENTS	CKT1	CKT2
R1	M1V	M5V
R2	A12J	B30K
R3	B14K	A32J
R4	A22J	A40J
R5	E24N	36S43
C1	L3U	M7V
C2	A19M	A37M
CR1	A16F	A34F
CR2	A28F	38P43
Q1	L12N	M29P
Q2	A25C	K42M
JUMPER	J26S	32V39
JUMPER	P10X	M9V
INPUT	17	16
OUTPUT	14	15



COMPONENTS	500MS DMV STD	80MS DMV STD
	CKT1	CKT2
R1	ST2Z	Z1HH
R2	CC5LL	6JJ13
R3	5UUT2	6FF13
R4	17FF24	19DD26
R5	15RR22	N22Y
R6	35NN42	U24BB
R7	18LL25	26FF33
R8	35FF42	33Z40
R9	KK1TT	K34T
R10	LL30UU	S16Z
R11	17NN24	S30Z
R12	20JJ27	DD15MM
C1	14TT23	15BB22
C2	32KK42	29CC39
C3	LL28UU	S18Z
C4	S14Z	CC3LL
CR1	7MM12	3Z8
CR2	NN26UU	U20Z
CR3	NN3UU	M32T
Q1	PP7SS	BB8DD
Q2	PP11SS	BB12DD
Q3	RR34TT	Z27BB
Q4	RR39TT	V27X
Q5	AA42CC	V42X
JUMPER	NONE	32X39
INPUT	20	18
OUTPUT	13	19



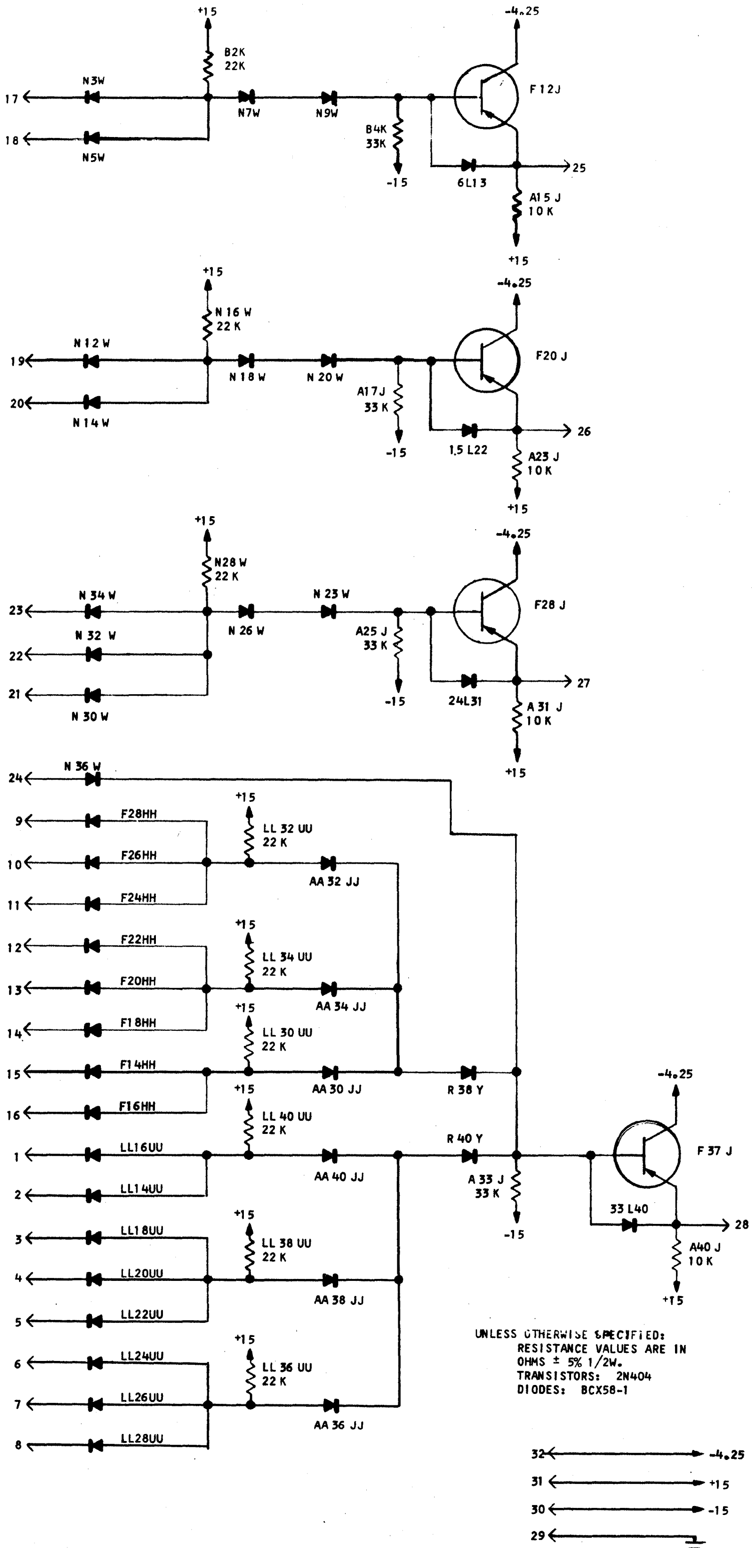
NOTES:

1. COMPONENTS IDENTIFIED BY LETTERS A, B, ETC. INDICATE PART NUMBERS AS FOLLOWS:
   DIODES
   A - BCX58-1
   B - 15039472
2. CHANGE COMPONENT VALUES AS INDICATED BELOW

COMPONENTS	500MS CKT1	80MS CKT2
R5	54.9K 1/8W,±1%	60.4K 1/4W,±1/2%
C1	15UF 20WVDC ±5%	2.2UF 20WVDC ±5%

UNLESS OTHERWISE SPECIFIED:
RESISTANCE VALUES ARE IN OHMS ±5%, 1/2W

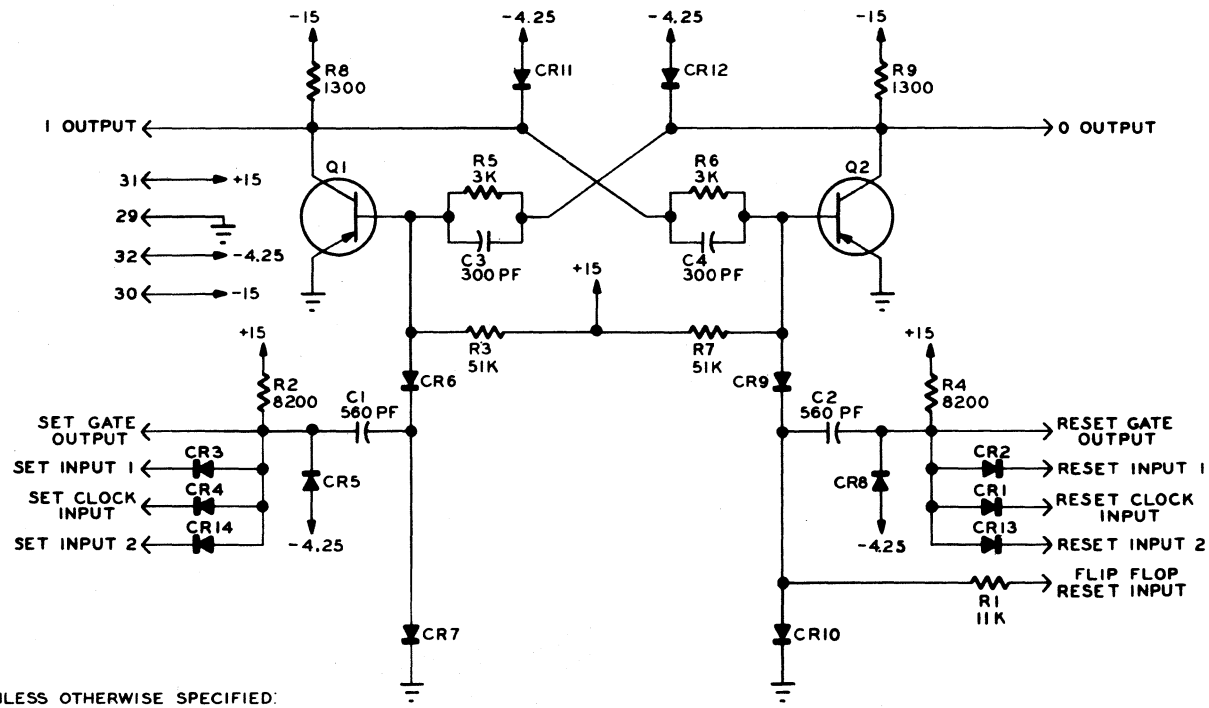
LOGIC CARD "G"


+15
B2K
22K
-4.25
F12J
N3W
N7W
N9W
N5W
B4K
33K
-15
6L13
A15 J
10 K
N16 W
22 K
F20 J
N12 W
N18 W
N20 W
N14 W
A17J
33 K
1.5 L22
A23 J
N28 W
F28 J
N34 W
N26 W
N23 W
N32 W
N30 W
A25 J
24L31
A31 J
N36 W
F28HH
F26HH
F24HH
F22HH
F20HH
F18HH
F14HH
F16HH
LL 32 UU
LL 34 UU
LL 30 UU
LL 40 UU
LL 38 UU
LL 36 UU
AA 32 JJ
AA 34 JJ
AA 30 JJ
AA 40 JJ
AA 38 JJ
AA 36 JJ
LL16UU
LL14UU
LL18UU
LL20UU
LL22UU
LL24UU
LL26UU
LL28UU
R 38 Y
R 40 Y
A 33 J
33 K
F 37 J
33 L40
A40 J
10 K
UNLESS OTHERWISE SPECIFIED:
RESISTANCE VALUES ARE IN
OHMS ± 5% 1/2W.
TRANSISTORS: 2N404
DIODES: BCX58-1

FLIP FLOP SPECIAL
(2 ELEMENT)

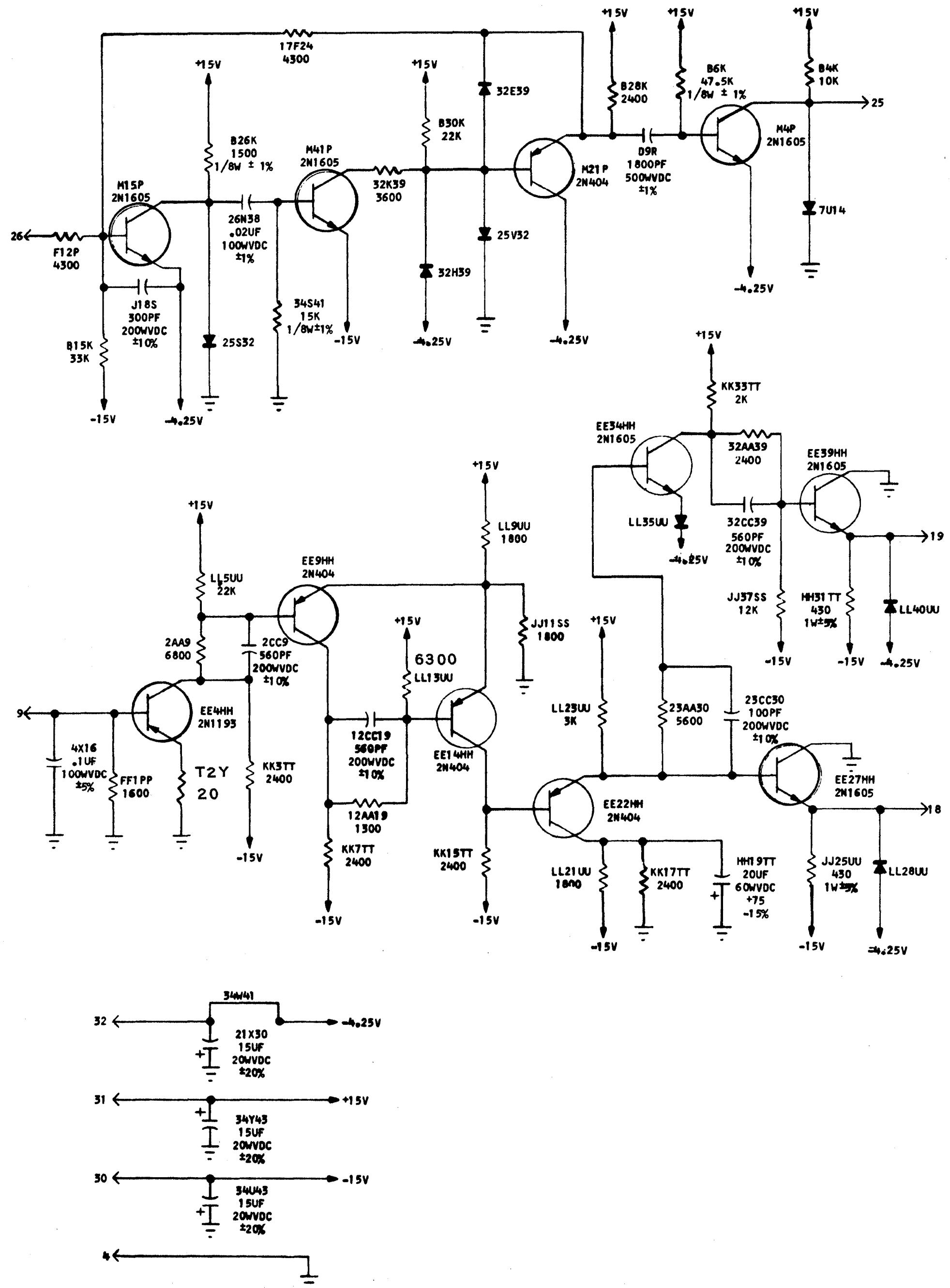
COMPONENT	CKT 1	CKT 2
RESET GATE OUT.	23	3
SET INPUT 2	16	12
RESET INPUT 2	20	9
Q1	N10R	EE10HH
Q2	N31R	EE31HH

COMPONENT	CKT 1	CKT 2
C1	K5B	KK5TT
C2	B35K	TT35KK
C3	15P22	15EE22
C4	15H22	15MM22
CR1	M37V	Z37HH
CR2	M39V	Z35HH
CR3	M3V	Z3HH
CR4	M1V	Z1HH
CR5	K3B	KK3TT
CR6	K11B	KK11TT
CR7	B7K	TT9KK
CR8	B37K	KK37TT
CR9	K28B	KK28TT
CR10	B30K	TT31KK
CR11	B9K	TT7KK
CR12	B26K	TT26KK
CR13	M35V	Z39HH
CR14	M5V	Z5HH
R1	B32K	TT33KK
R2	B1K	TT1KK
R3	K13B	KK13TT
R4	B39K	TT39KK
R5	15M22	15HH22
R6	15K22	15KK22
R7	B24K	TT24KK
R8	N7W	Y7FF
R9	M26V	Z26HH
SET INP[illegible]	17	13
RESET INPUT 1	22	11
FLIP FLOP RESET	27	4
SET CLOCK IN.	19	15
RESET CLOCK IN.	21	10
"1" OUTPUT	25	6
"0" OUTPUT	26	5
SET GATE OUT.	24	8



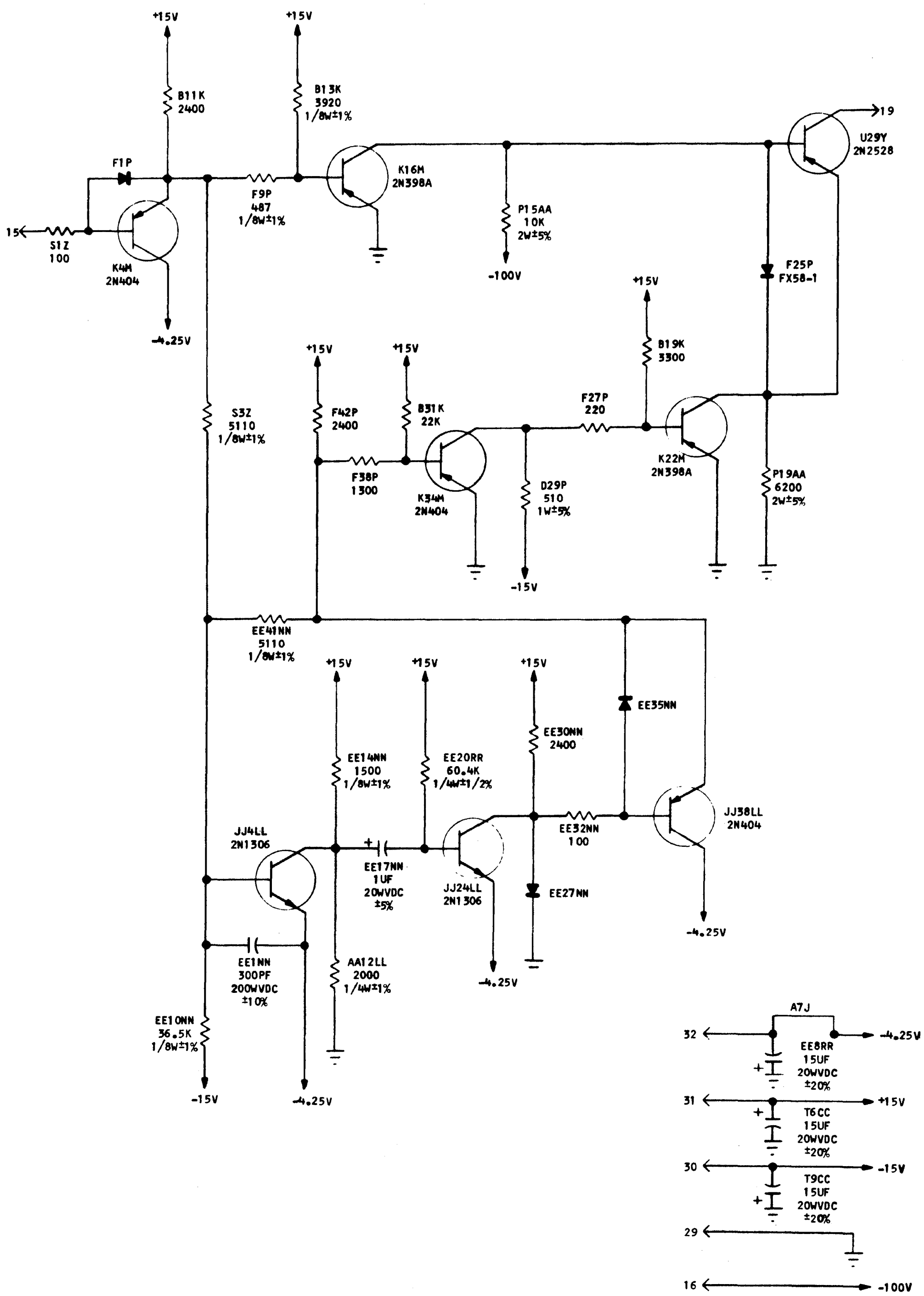
UNLESS OTHERWISE SPECIFIED:
RESISTANCES ARE IN OHMS, 5%, 1/2W.
TRANSISTORS 2N404.
DIODES BCX 58-1
CAPACITANCES ARE ± 10% 500WVDC

FRONT PAPER SWITCH



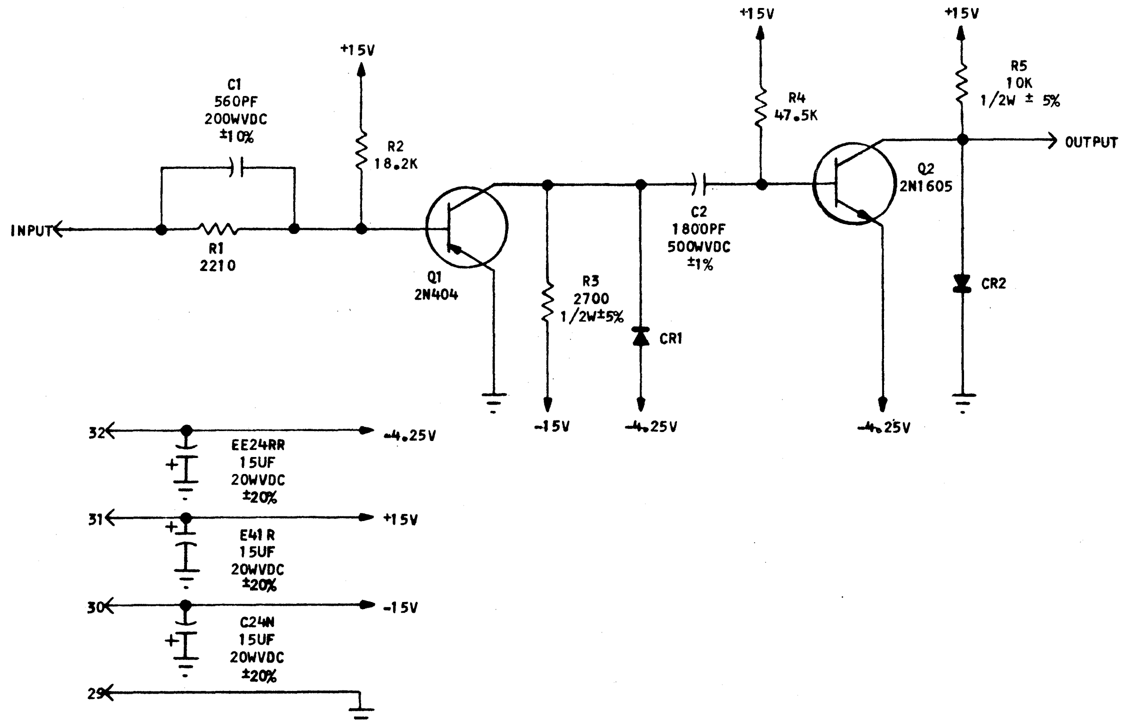
. UNLESS OTHERWISE SPECIFIED:
RESISTANCE VALUES ARE IN OHMS ±5%, 1/2W
DIODES ARE BCX58-1

P.D.C. SOL. DR.



UNLESS OTHERWISE SPECIFIED:
RESISTANCE VALUES ARE IN OHMS ±5%, 1/2W
DIODES ARE BCX58-1

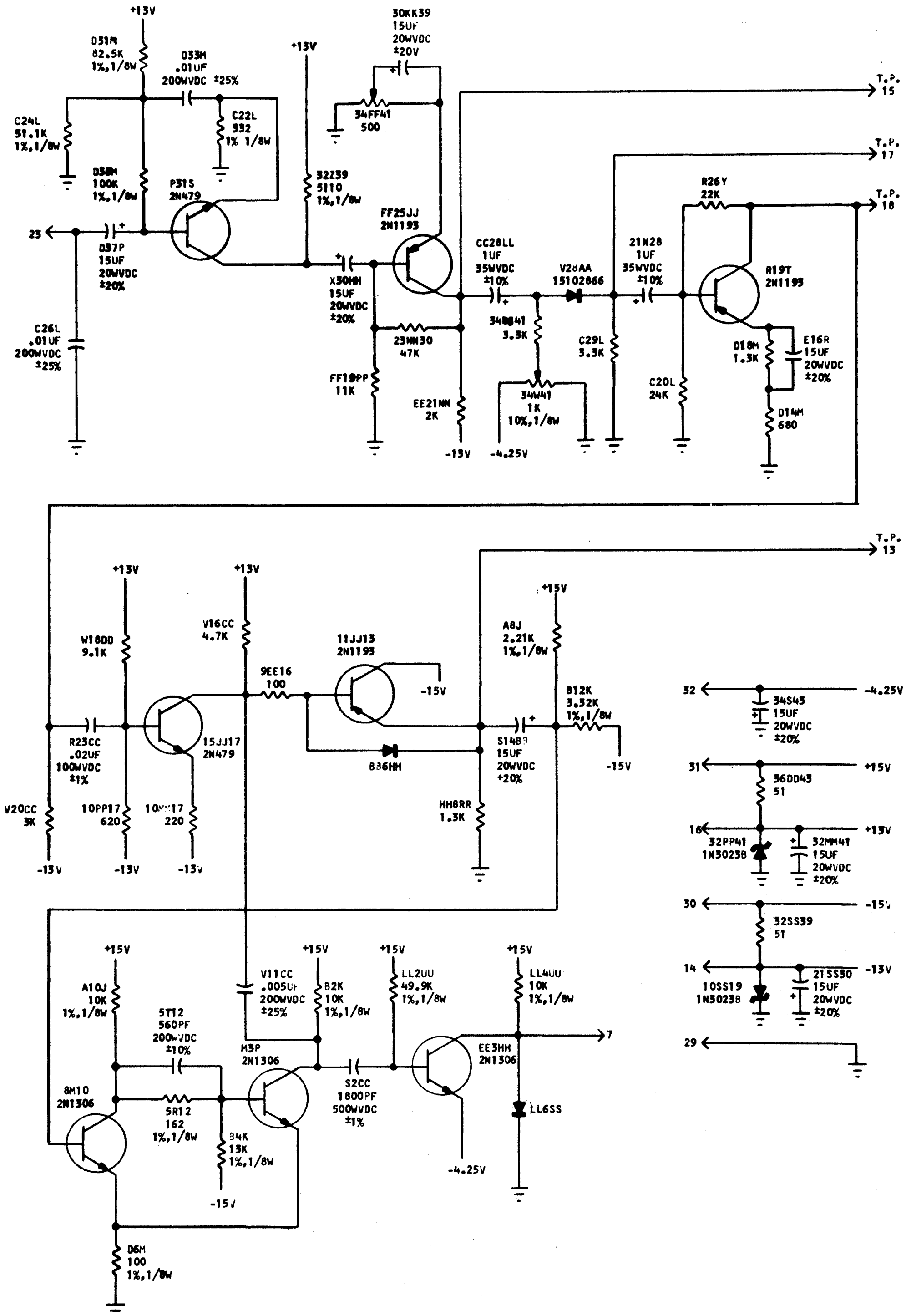
PULSE STANDARDIZER



COMPONENTS	CKT. 1	CKT. 2	CKT. 3	CKT. 4	CKT. 5
R1	U9BB	T3AA	U18BB	U27BB	U36BB
R2	B2K	B11K	B17K	B27K	B33K
R3	C8L	C15L	C21K	C31L	C38L
R4	KK7TT	KK14TT	KK21TT	KK31TT	KK39TT
R5	KK4TT	KK11TT	KK18TT	KK28TT	KK36TT
C1	U11BB	T1AA	U20BB	U29BB	U38BB
C2	S6CC	S15CC	S24CC	S33CC	T42DD
CR1	A6J	A13J	A19J	A29J	A36J
CR2	HH1RR	HH9RR	HH16RR	JJ26SS	HH33RR
Q1	M4P	M12P	M19P	M28P	M36P
Q2	EE4HH	EE12HH	EE19HH	EE28HH	EE36HH
INPUT	12	13	15	17	19
OUTPUT	11	14	16	18	20

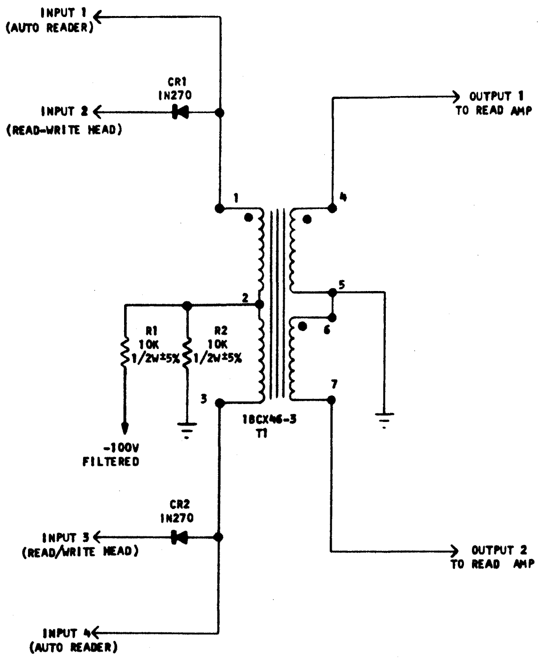
UNLESS OTHERWISE SPECIFIED:
RESISTANCE VALUES ARE IN OHMS ±1%, 1/8W
DIODES ARE BCX58-1

READ AMP

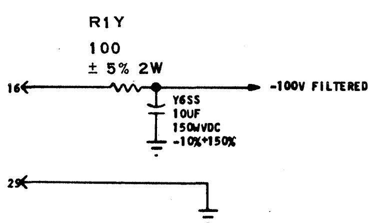


UNLESS OTHERWISE SPECIFIED:
RESISTANCE VALUES ARE IN OHMS 1/2W, 5%
DIODES ARE BCX58-1

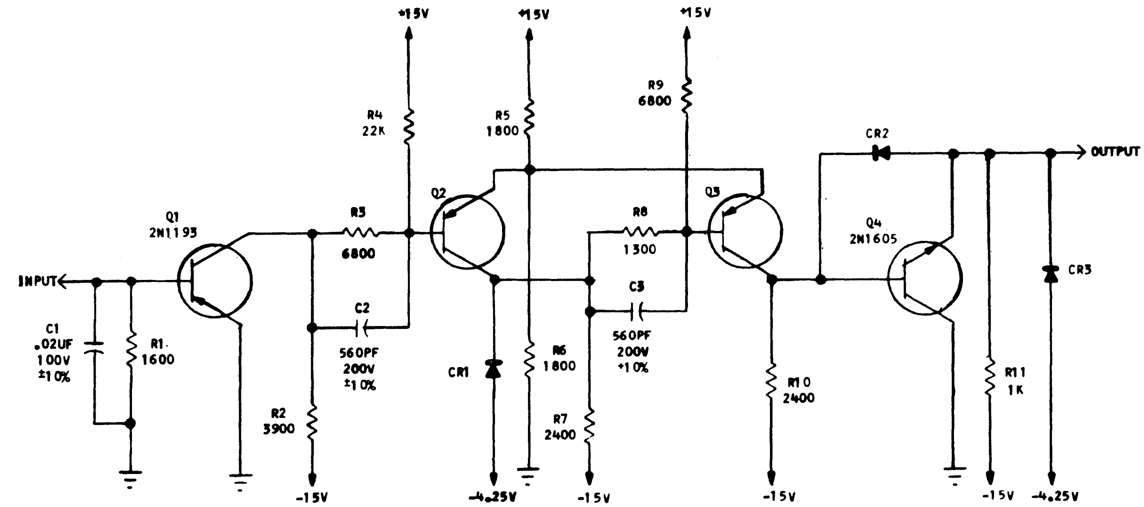
READ TRANSFORMER



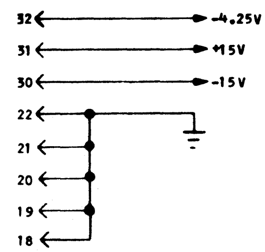
COMPONENTS	DATA 1	DATA 2	DATA 3
R1	N6W	8W15	AA1JJ
R2	C5L	11BB18	LL1UU
CR1	H8R	U21BB	KK11TT
CR2	H10R	U23BB	KK13TT
T1	L17	X30	MM20
INPUT 1	28	14	6
INPUT 2	26	9	2
INPUT 3	25	10	3
INPUT 4	27	13	7
OUTPUT 1	24	11	5
OUTPUT 2	23	12	4



SOLAR CELL CAM AMPLIFIER

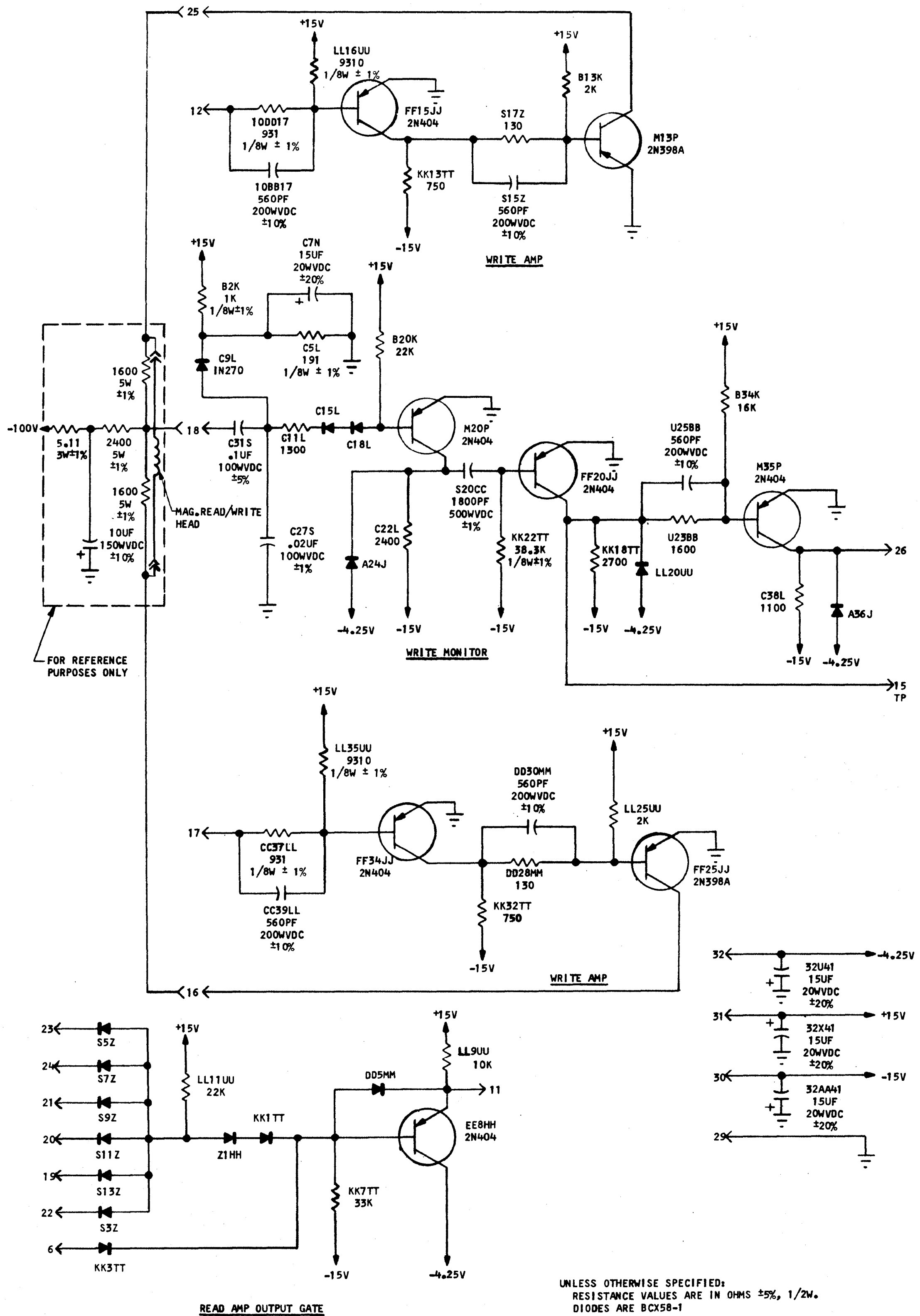


COMPONENT	CKT. 1	CKT. 2	CKT. 3	CKT. 4
R1	R5Y	S22Z	5X12	V24CC
R2	B4K	B25K	LL4UU	KK27TT
R3	5R12	24R31	2BB9	W30DD
R4	A6J	A23J	LL5UU	LL29UU
R5	A2J	A31J	LL9UU	LL25UU
R6	5V12	R34Y	BB11KK	W32DD
R7	B10K	B29K	LL3UU	KK33TT
R8	R16Y	R38Y	14BB21	34AA41
R9	A12J	A36J	LL13UU	LL35UU
R10	B16K	B34K	KK19TT	KK37TT
R11	B20K	B38K	KK23TT	KK39TT
C1	R1Y	S20Z	5Z12	V26CC
C2	5T12	24T31	2DD9	V28CC
C3	R14Y	R36Y	14DD21	34CC41
CR1	A8F	A27F	NN7UU	NN31UU
CR2	E18L	R40W	HH17NN	JJ41PP
CR3	A14F	A40F	NN15UU	NN21UU
Q1	L2N	L27N	FF2JJ	24HH26
Q2	L7N	L32N	FF7JJ	FF31JJ
Q3	L13N	L36N	FF14JJ	34FF36
Q4	L22N	L41N	FF21JJ	EE39HH
INPUT	24	27	9	4
OUTPUT	26	28	5	3

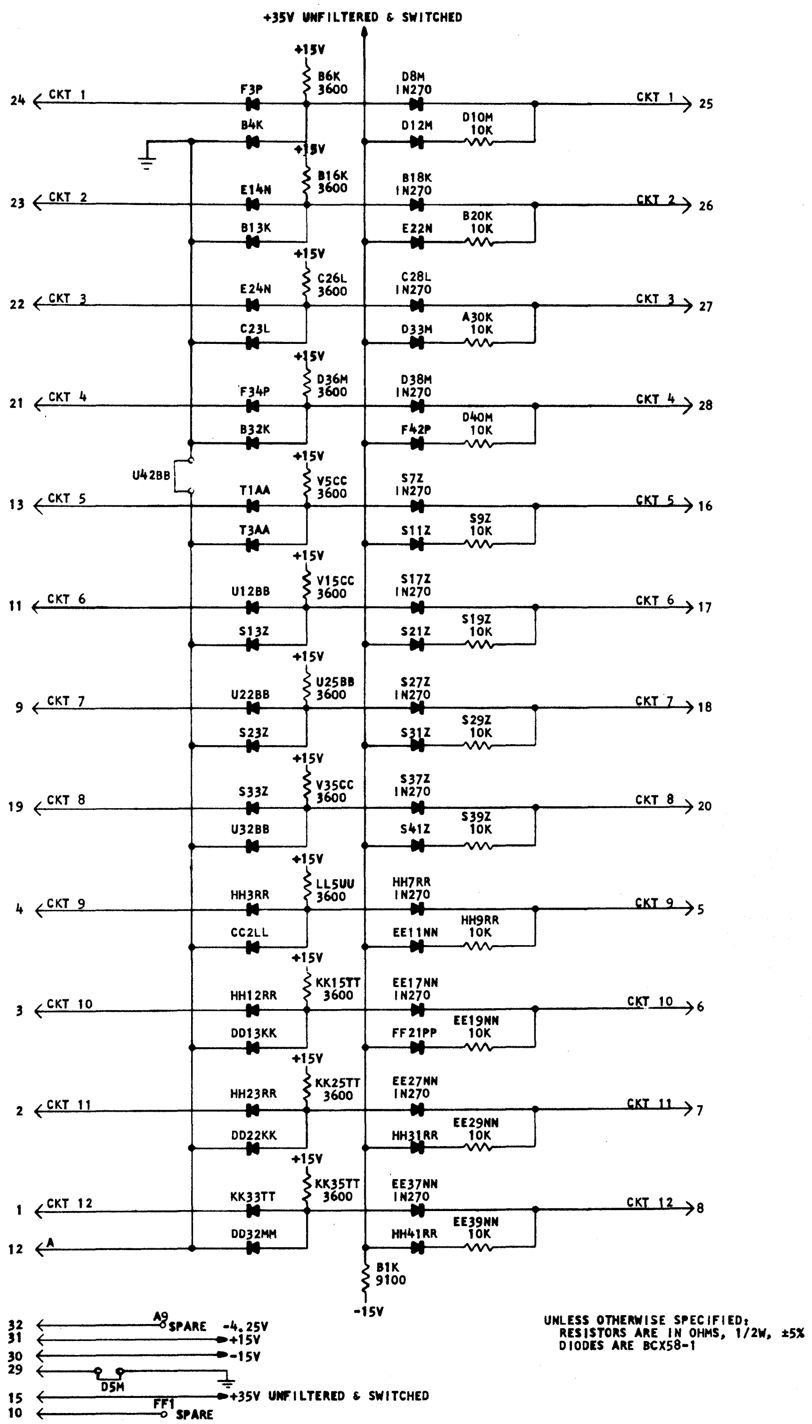


UNLESS OTHERWISE SPECIFIED:
RESISTANCE VALUES IN OHMS ±5%, 1/2W
TRANSISTORS 2N404
DIODES BCX58-1

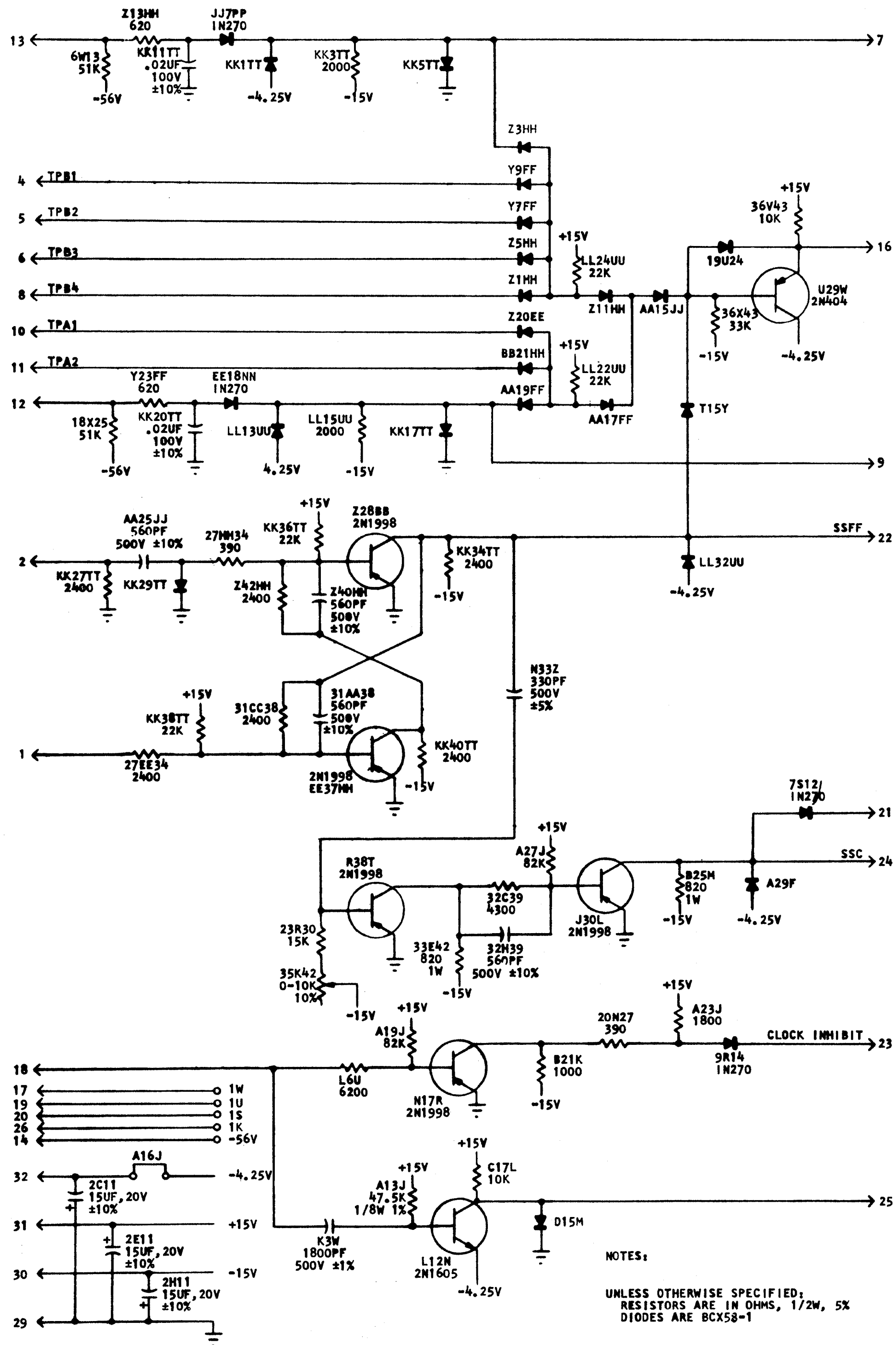
WRITE AMP & MONITOR



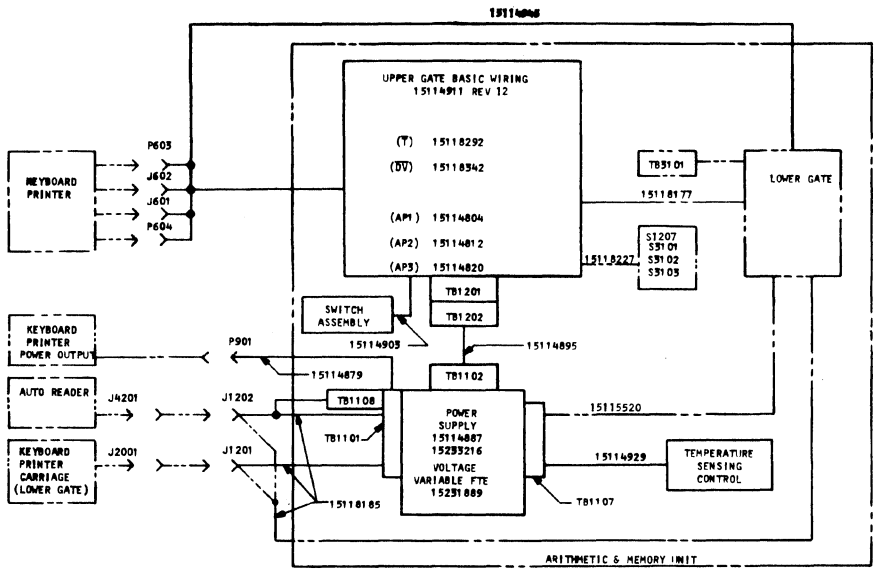
KEYBOARD WETTER



✓SINGLE SHOT CLOCK (P)



✓Changes or additions since last issue



PAGE	DESCRIPTION	E.R.DATE	REV
100	ARITHMETIC & MEMORY UNIT INDEX	04-02-66	P
101	POWER SUPPLY	04-02-66	P
102A-B	POWER SUPPLY, MER RELAY, MR SW, +35 SENSING	12-7-64	C
102B-B	POWER SUPPLY, VOLTAGE & FREQUENCY VARIABLES	04-02-66	P
103	VOLTAGE ROUTING +15V, -4.25V, -2.5V	03-22-65	P
104	VOLT. ROUTING -15V,-15M,-56V,-100V,-100UNDELAYED	12-24-65	L
105	VOLTAGE ROUTING GRD	03-22-65	P
106A-B	POR, RESET STANDARDIZER	03-22-65	P
106B-B	SINGLE SHOT CLOCK PERMANENT (SSCP) CLOCK	12-24-65	L
107	DIGIT DISTRIBUTOR, DD0-DD5, STEP DD	12-24-65	L
108	DIGIT DISTRIBUTOR, DD6-DD11, DDMSD, DDU, DOT	12-24-65	L
109	KEYBOARD, SRX'S	12-25-65	N
110	GT→WR	12-24-65	L
111	WR'S	12-24-65	L
112	MR→MEM, SUM →MEM, WR→MEM, ~~XFER→C~~	12-24-65	L
113	WRITE	8-14-65	G
114	READ, MTA, MTB	12-24-65	L
115	DECIMAL TO BINARY ENCODER & VOLTAGE WETTER, MART	12-24-65	L
116	DECIMAL TO BINARY ENCODER & VOLTAGE WETTER, MARU	12-24-65	L
117	DJREW, MEMORY DECODING - X DRIVERS	12-24-65	L
118	MEMORY DECODING - X DRIVERS	2-4-66	M
119	MEMORY DECODING - Y DRIVERS	2-4-66	M
120	INHIBIT DRIVERS, CLR MEM		
121	MEMORY, MR.	2-4-66	M
122	ADD, SUB, CIFF	12-24-65	L
123	COMPFF, T/C'S	12-24-65	L
124	ADDER, DECIMAL CORRECTOR	7-16-65	G
125	APFF, RACK STOP DRIVERS	12-24-65	L
126	SYMFF & CHAR FF	12-24-65	L
127	SET SPECIAL ADDRESS	7-16-65	G
128	SPECIAL ADDRESS FF'S, NZFF	12-24-65	L
129	TO-T7, DVFF	12-25-65	N

PAGE	DESCRIPTION	E.R.DATE	REV
130	S0 - S4, PC	12-24-65	L
131	S5 - S10	12-24-65	L
132	SCFF, SFF	12-24-65	L
133	EOC, EOCA, ECNC, LOCK, END OP, PAFF, MAFF	12-25-65	N
134	ALL TOTALS, AT LU	2-4-66	M
135	LANES, AMFF, LN3FF, RED RIBBON SOL, AEC LOCK	12-24-65	L
136	NOT USED		
137	NOT USED		
138	NOT USED		
139	SW, SX, SY, SZ	12-24-65	L
140	TIM, TOM, BEFF, KBD LOCK SOL, CRG RET,SLIDE 1-7	12-25-65	N
141	TO - SHIFT RIGHT OR SHIFT RIGHT AND ROUND LOGIC		
142	T1 - TRANSFER LOGIC		
143	T2 - PRINT LOGIC	12-24-65	L
144	T3, 4 & 5 - ADD OR SUB (A,B,OR C) LOGIC	7-16-65	G
145	T6 - CLEAR LOGIC	7-16-65	G
146	T7 - MULTIPLY LOGIC	7-16-65	G
147	T7 - DIVIDE LOGIC	11-20-64	C
148	TYPEWRITER IN AND OUT FEATURE LOGIC	11-27-65	H
149	CARD LOCATION & TIE POINT CHART	12-25-65	N
150	CARD LOCATION & TIE POINT CHART	12-25-65	N
151	CARD LOCATION & TIE POINT CHART	2-4-66	M
152	CARD ELEMENTS & COMPONENTS		
153	CARD ELEMENTS & COMPONENTS	12-24-65	L
154	COMPONENT INDEX	12-24-65	L
155	CONNECTOR INDEX	10-23-65	
156	SIGNAL INDEX LOWER & UPPER GATE	12-25-65	N
157	TERMINAL BOARD INDEX	12-24-65	L

NOTES:
1. WIRING SHOWN IN DASHED LINES (------) INDICATES OPTIONAL FEATURES.
2. CHARACTERS IN PARENTHESIS ON WIRING INDICATES NAME OF OPTIONAL FEATURE REQUIRING WIRING.
3. CHARACTERS IN PARENTHESIS LOCATED NEAR CARD ELEMENT INDICATES OPTIONAL FEATURE REQUIRING THAT CARD.
4. PART NUMBERS ON INPUT SIGNALS INDICATE PAGE OF ORIGIN.
5. EXCEPT FOR VOLTAGE AND FF ELEMENT PINS, ALL ELEMENT PINS ARE SHOWN. PINS 10, 15, 19, 21, IF SHOWN ON FF ELEMENTS, ARE CLOCK (A, B, B1, OR C) INPUTS. ALL OTHER ELEMENT PINS SHOWN WITHOUT SIGNAL ARE NOT WIRED.
6. PAGES 100 THRU 299 DESIGNATE A & M UPPER GATE SCHEMATIC 15115009.
7. PAGES 300 THRU 349 DESIGNATE A & M LOWER GATE AND KBD. PTR. CRG. SCHEMATIC 15118300.
8. PAGES 350 THRU 358 DESIGNATE AUTO READER SCHEMATIC 15227440.
9. PAGES 500 THRU 549 DESIGNATE KEYBOARD PRINTER SCHEMATIC 15117997.
10. CAPACITORS C1102, C1104, C1109, ARE ADDED WHEN A.C. VOLTAGE SOURCE IS 50 CYCLES PER SECOND.
11. "ME" INDICATES SIGNAL WHICH REQUIRED CONSIDERATION OF MUTUAL EXCLUSIVENESS IN THE DETERMINATION OF ITS LOAD.

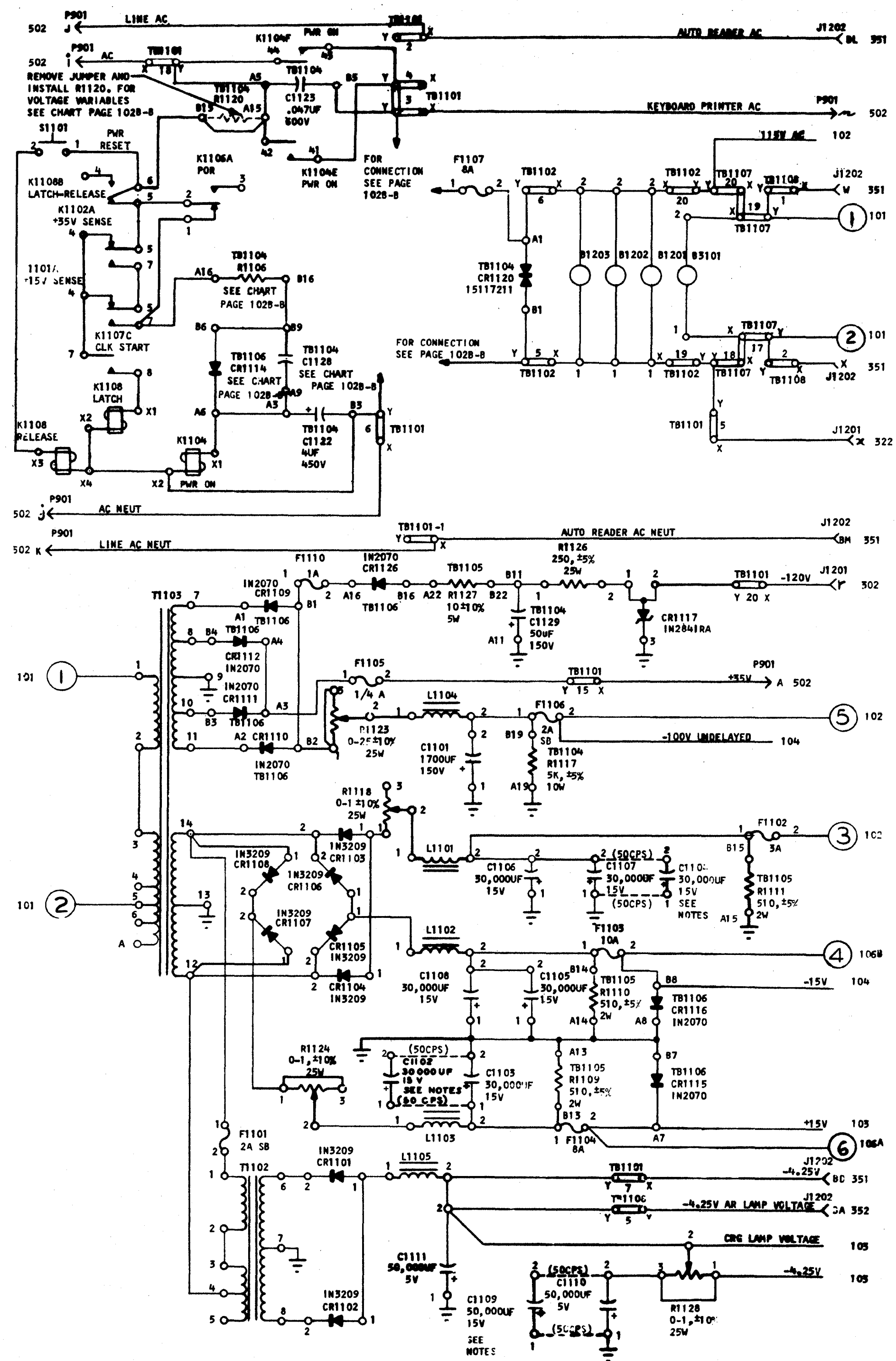
UNLESS OTHERWISE SPECIFIED:
ALL CAPACITORS ARE 5UF, 25 WVDC
ALL DIODES ARE BCX58-1
ALL RESISTANCES ARE IN OHMS

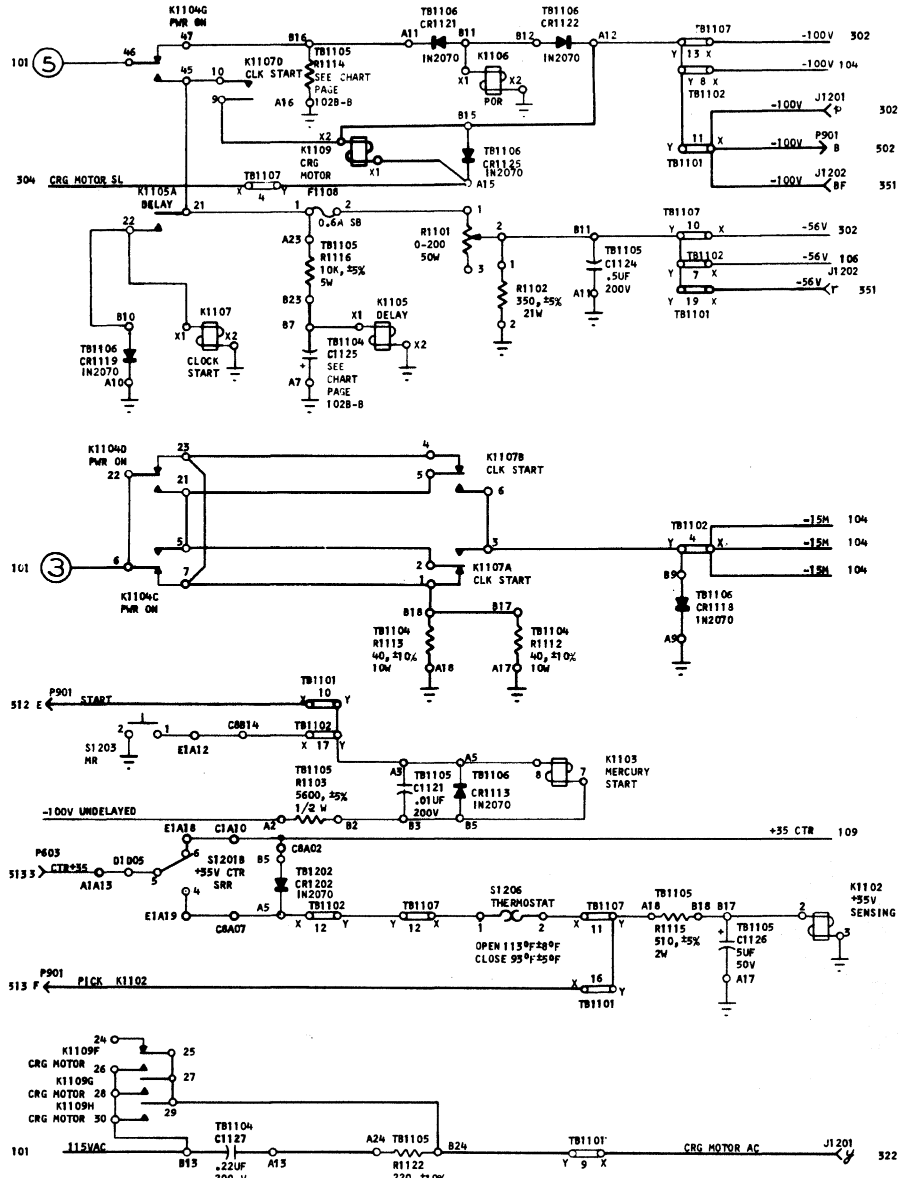
OPTIONAL FEATURES
ABBREVIATIONS:
(4M) 40 WORD MEMORY

(1M) 100 WORD MEMORY
(T) TYPE TO/FROM MEMORY
($\overline{T}$) TYPE TO/FROM MEMORY,INACT.
(DV) DIVIDE
($\overline{DV}$) DIVIDE INACTIVE
(R) RESERVED FOR FUTURE

(AP1) DOUBLE CHARACTER AMOUNT PROTECTION RACKS 5-13
($\overline{AP1}$) DOUBLE CHARACTER AMOUNT PROTECTION RACKS 5-13 INACTIVE
(AP2) DOUBLE CHARACTER AMOUNT PROTECTION RACKS 4-13
($\overline{AP2}$) DOUBLE CHARACTER AMOUNT PROTECTION RACKS 4-13 INACTIVE
(AP3) FULL AMOUNT PROTECTION
($\overline{AP3}$) FULL AMOUNT PROTECTION INACTIVE

Ref. Page 100


LINE AC
AUTO READER AC
REMOVE JUMPER AND INSTALL R1120. FOR VOLTAGE VARIABLES SEE CHART PAGE 102B-B
KEYBOARD PRINTER AC
PWR RESET
LATCH-RELEASE
+35V SENSE
CLK START
FOR CONNECTION SEE PAGE 102B-B
SEE CHART PAGE 102B-B
AC NEUT
LINE AC NEUT
AUTO READER AC NEUT
-120V
-100V UNDELAYED
-15V
+15V
-4.25V AR LAMP VOLTAGE
CRG LAMP VOLTAGE
-4.25V
SEE NOTES

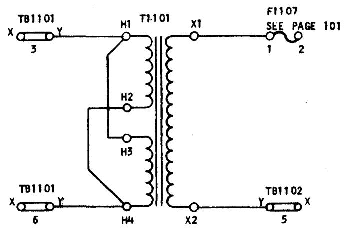


REF INFORMATION		
SUPPLY (VOLTS)	TOLERANCE *	MAXIMUM CURRENT (AMPS)
+15	± 5%	6.5
-15	± 5%	7.5
-15 MEM	± 3%	2.7
-4.25	± 5%	8.0
-100	± 5%	1.8
-56	±10%	0.3
+35UF	± 5%	0.1
-4.12	± 5%	2.0
-120	± 10%	0.12

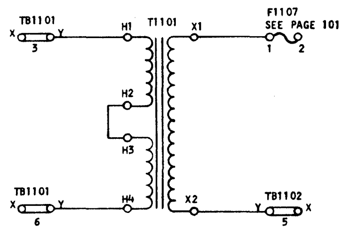
* INCLUDES RIPPLE TOLERANCE

Ref. Page 102A-B

T1101 CONNECTIONS FOR ANY 60 CPS ±1% OR 50 CPS ±1% VOLTAGE SOURCE WHOSE MINIMUM OUTPUT IS NOT LESS THAN 88 VOLTS AND WHOSE MAXIMUM OUTPUT IS NOT GREATER THAN 134 VOLTS.



T1101 CONNECTIONS FOR ANY 60 CPS ±1% OR 50 CPS ±1% VOLTAGE SOURCE WHOSE MINIMUM OUTPUT IS NOT LESS THAN 176 VOLTS AND WHOSE MAXIMUM OUTPUT IS NOT GREATER THAN 267 VOLTS.

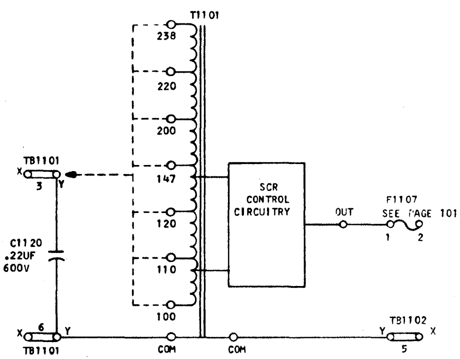


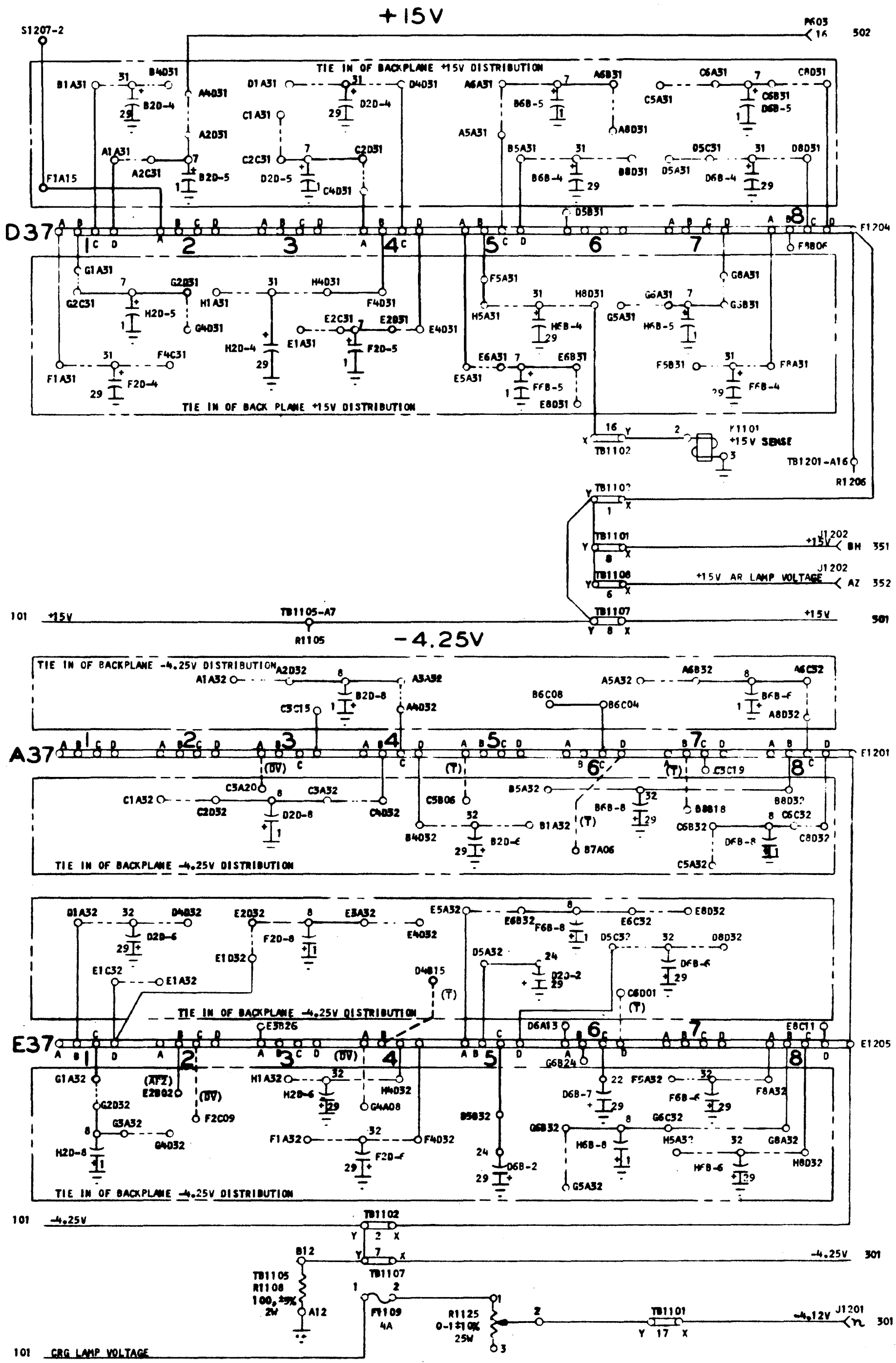
T1101 CONNECTIONS FOR ANY 46 THRU 64 CPS VOLTAGE SOURCE WHOSE MINIMUM AND MAXIMUM OUTPUTS ARE WITHIN ONE OF THE RANGES LISTED.

A.C. VOLTAGE SOURCE			TAP CONNECTED
MIN. VOLTS	NOM. VOLTS	MAX VOLTS	TO TB1101-Y3
88	100	112	100
97	110/115	123	110
106	120/127	134	120
129	150	165	147
176	200/210	224	200
194	220/230	246	220
209	240/250	267	238

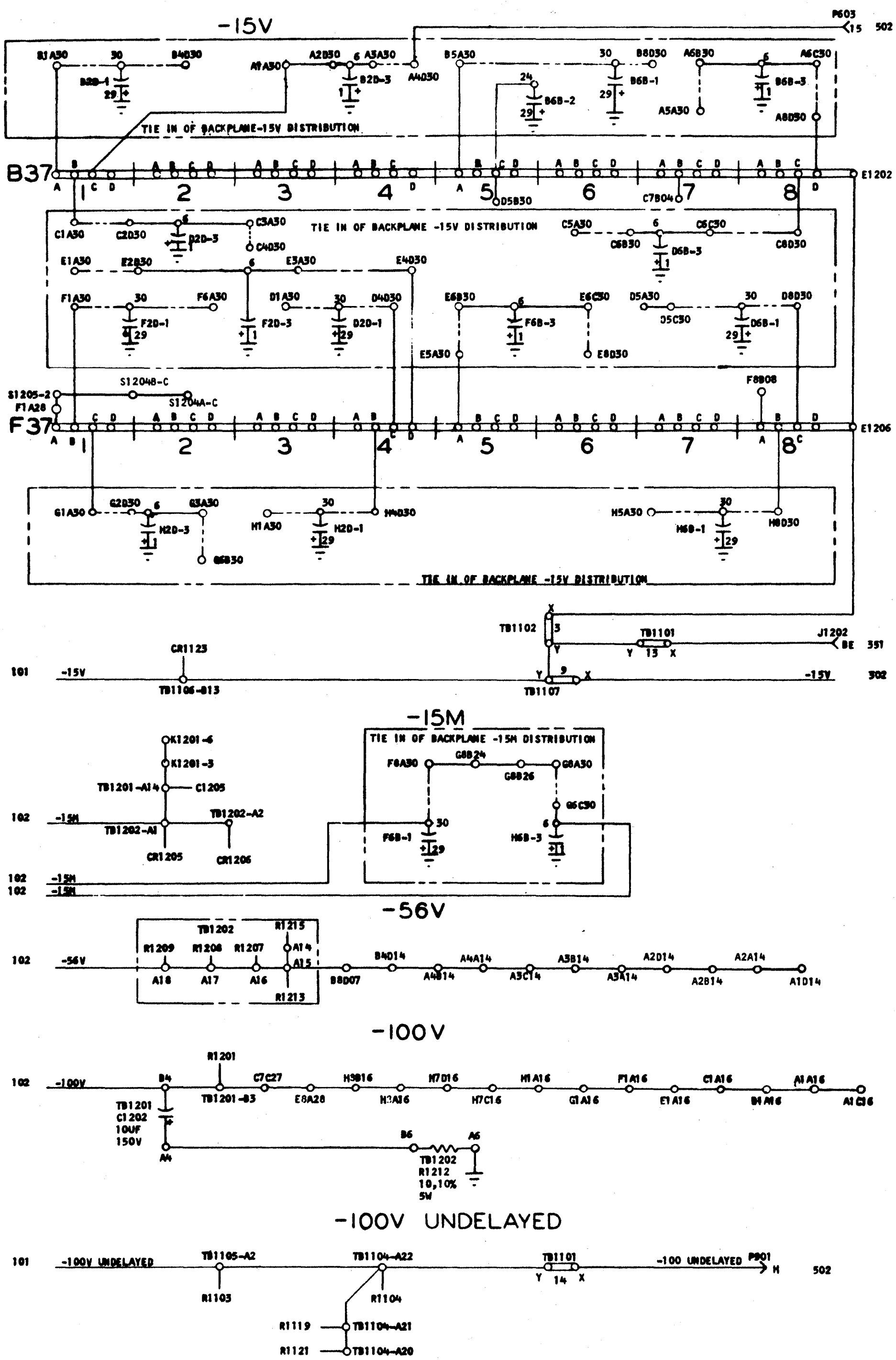
T1101 - A.C. LINE REGULATOR				
PART NO.	INPUT VOLTAGES	FREQUENCY	C1125	R1114
1BRX46-2	88-134/176-267	60CPS±1%	150UF 150V	510 5% 2W
15005093	88-134/176-267	50CPS±1%	150UF 150V	510 5% 2W
15231236	88-112/97-123/106-134/129-165/176-224/194-246/209-267	46-64CPS	500UF 50V	5K 5% 5W

LINE VOLTAGE	R1106	R1120	C1128	CR1114
88-134	250 5% 10W	JUMPER	.22UF 400V	1N2070
129-165	500 5% 10W	500 5% 10W	.22UF 600V	1N2071
176-267	1200 5% 10W	1200 5% 10W	.22UF 600V	1N2071

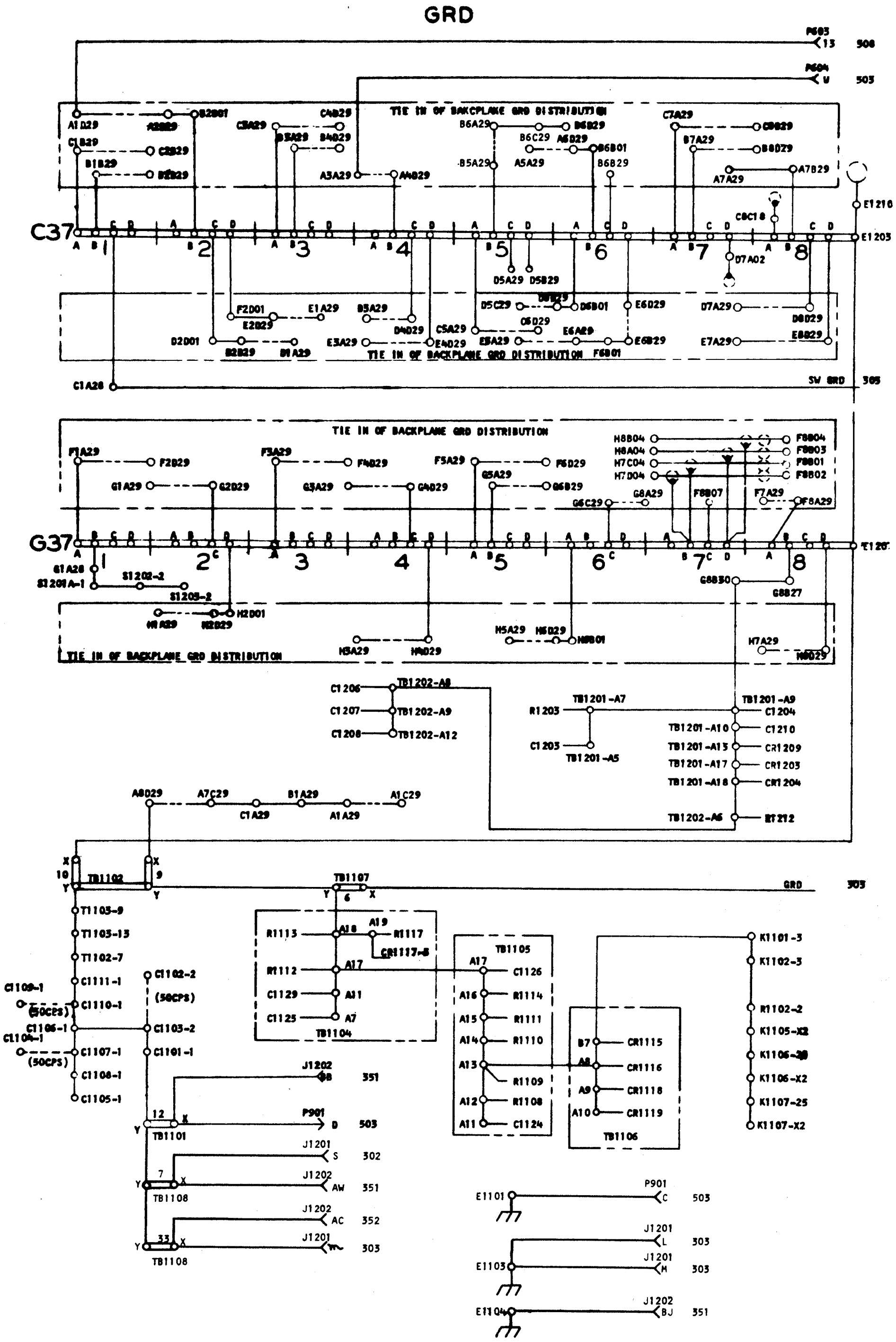



+15V
TIE IN OF BACKPLANE +15V DISTRIBUTION
D37
TIE IN OF BACK PLANE +15V DISTRIBUTION
+15V SENSE
+15V AR LAMP VOLTAGE
-4.25V
TIE IN OF BACKPLANE -4.25V DISTRIBUTION
A37
E37
CRG LAMP VOLTAGE

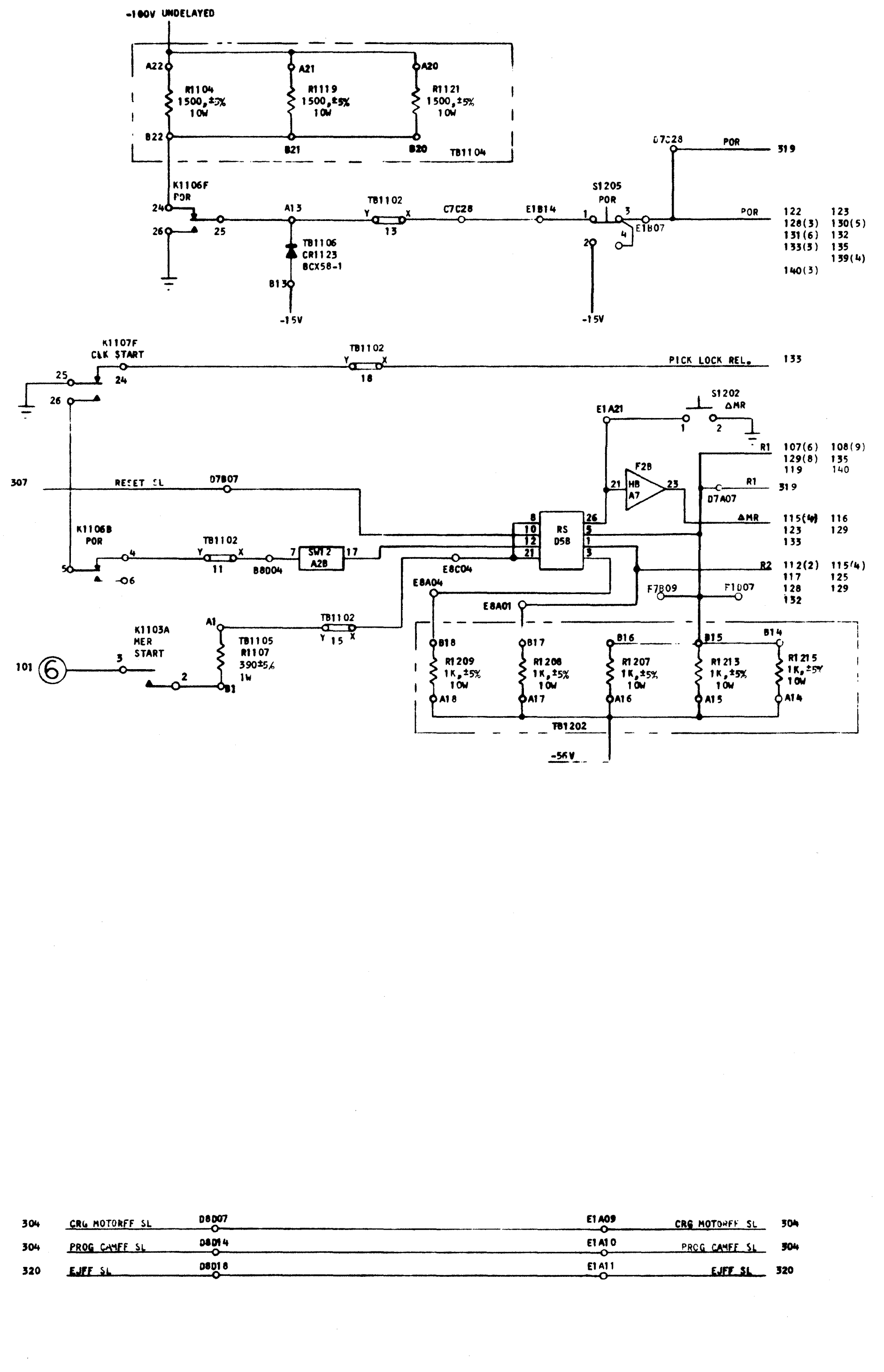
Ref. Page 103


-15V
TIE IN OF BACKPLANE-15V DISTRIBUTION
B37
F37
-15M
TIE IN OF BACKPLANE -15M DISTRIBUTION
-56V
-100V
-100V UNDELAYED

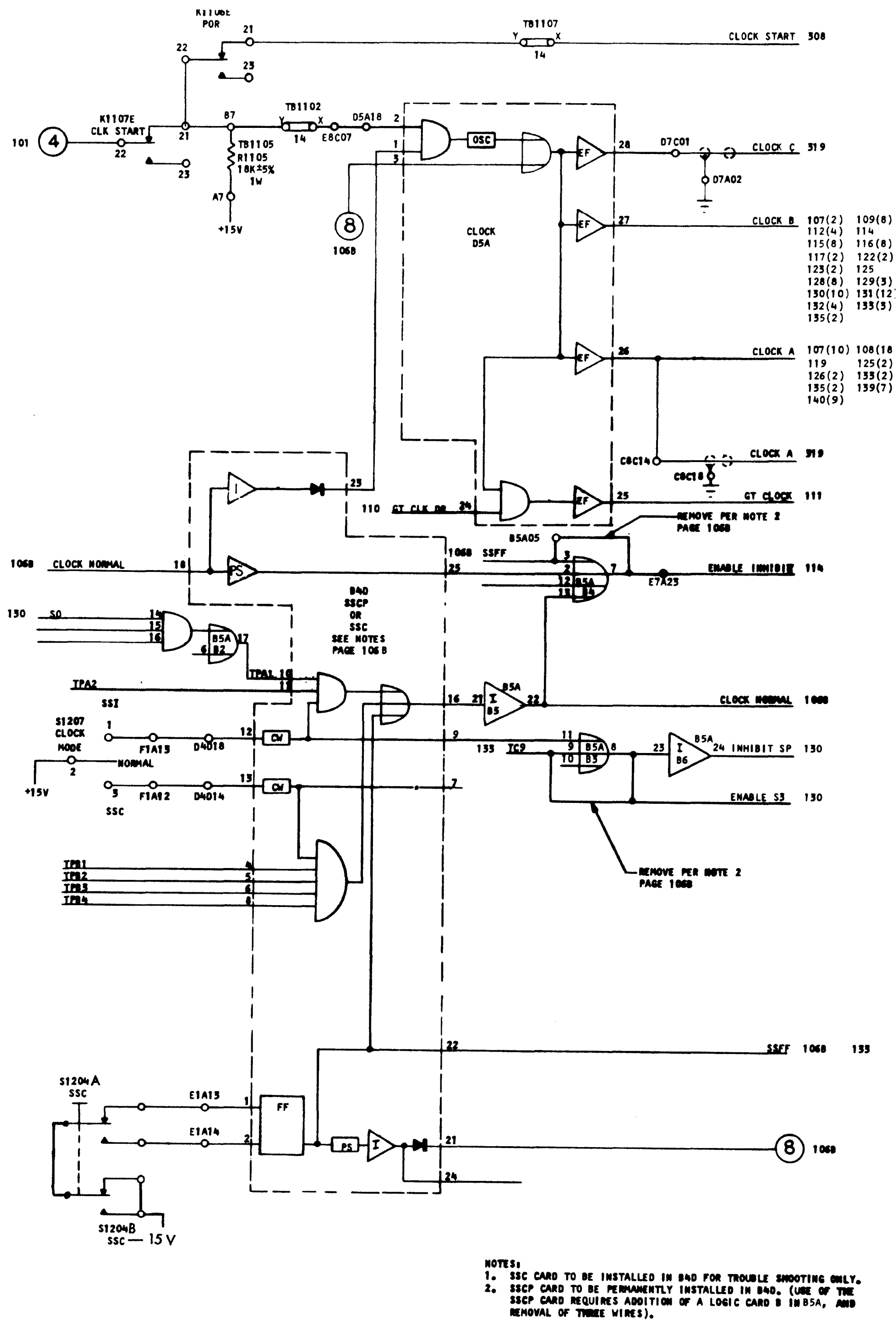
Ref. Page 104


GRD
TIE IN OF BACKPLANE GRD DISTRIBUTION
C37
G37
SW GRD
TB1101
TB1104
TB1105
TB1106
TB1107
TB1108
GRD

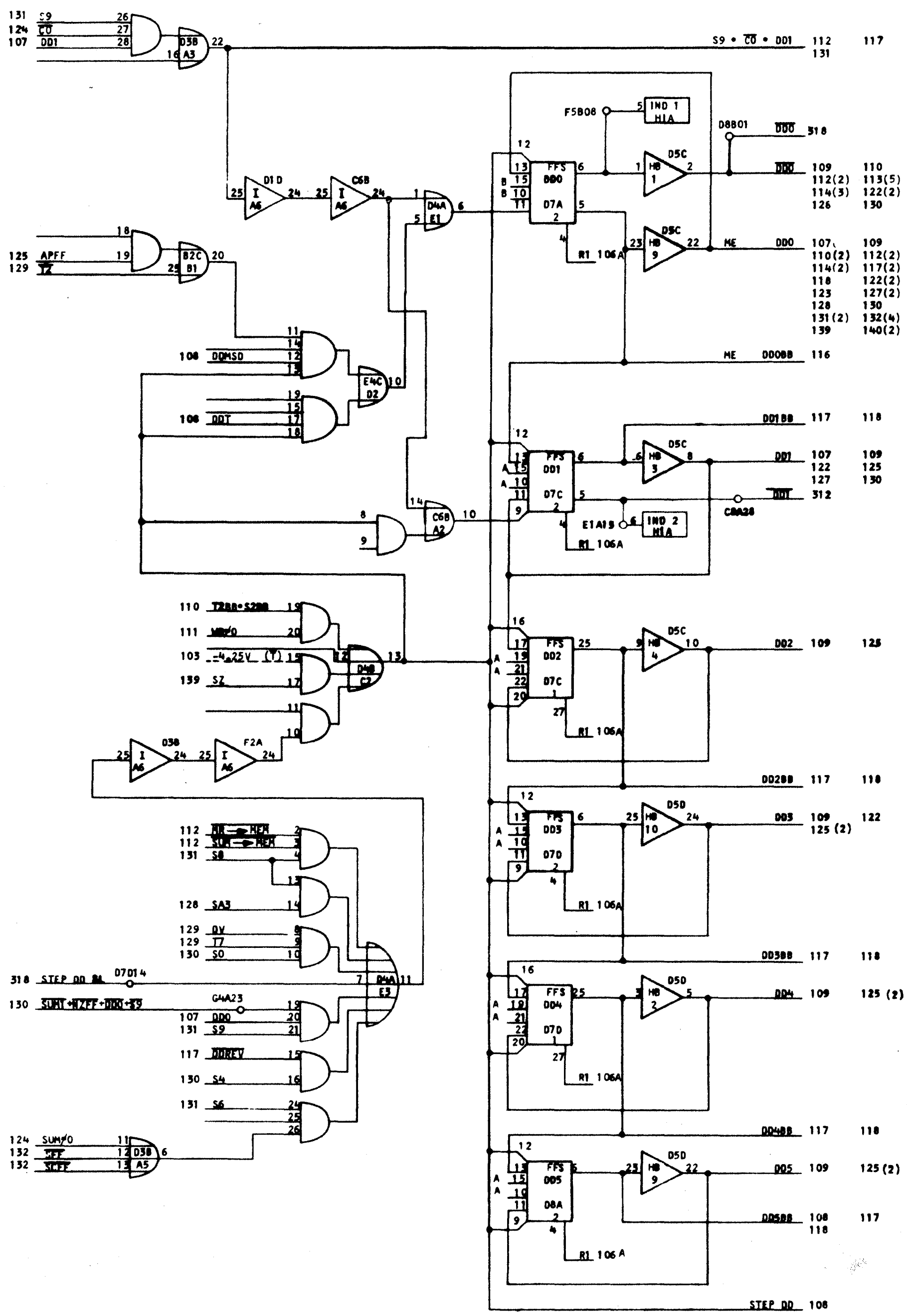
Ref. Page 105



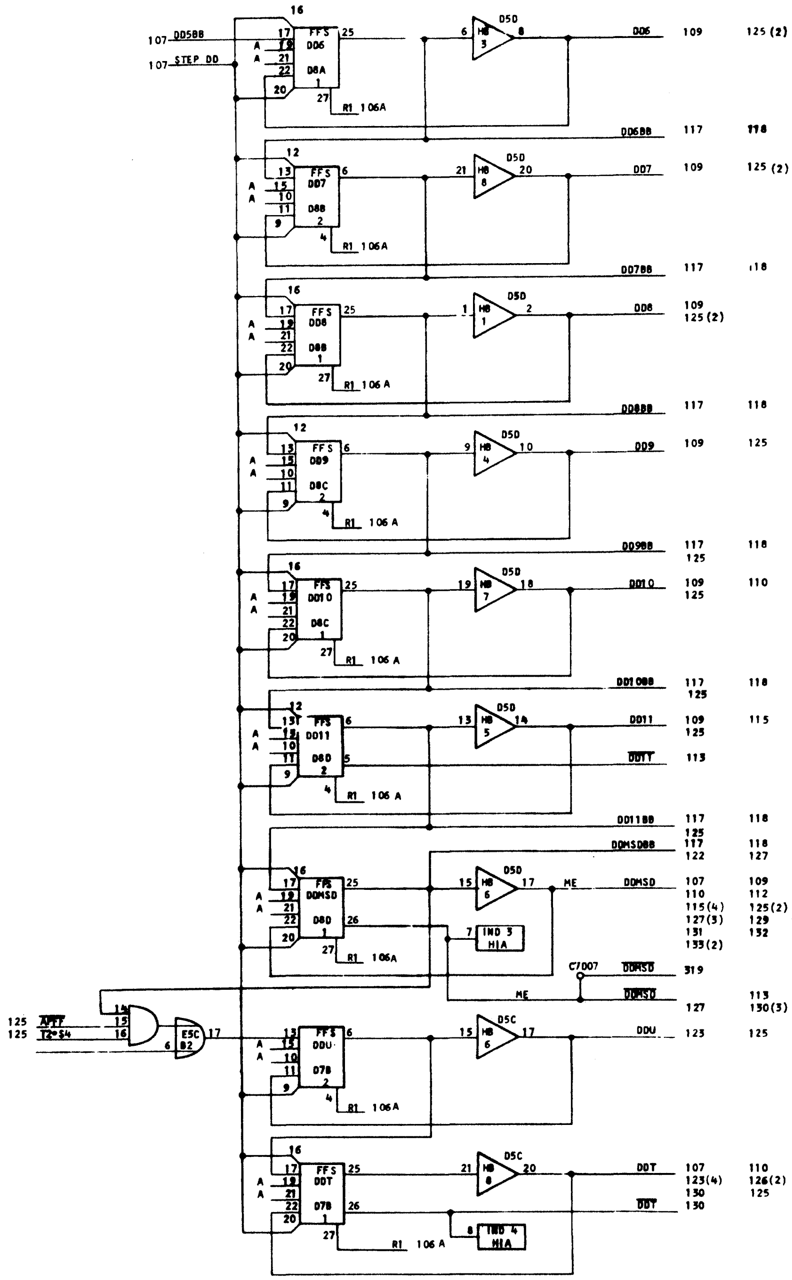
Ref. Page 106A -B



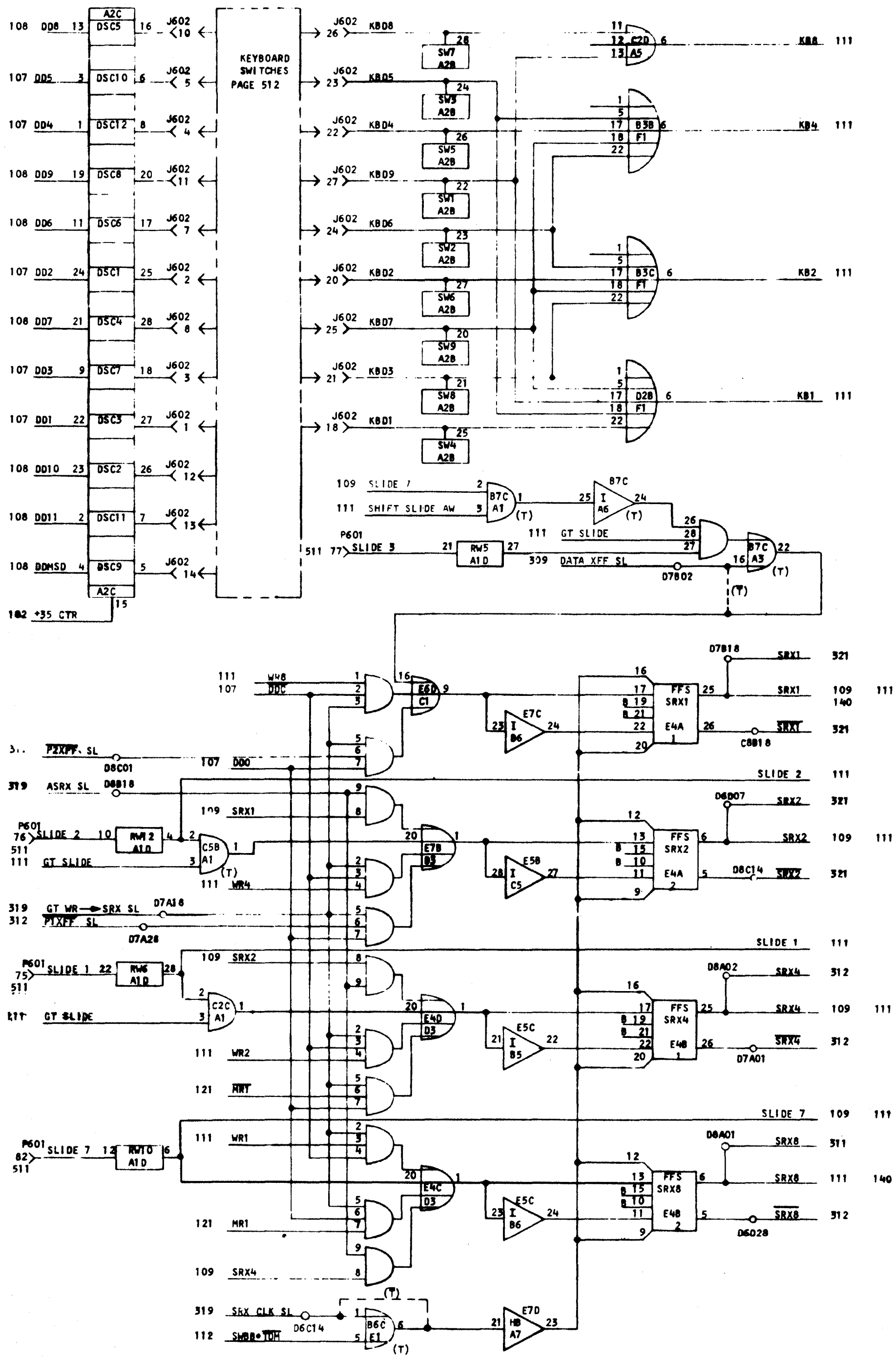
Ref. Page 106B -B



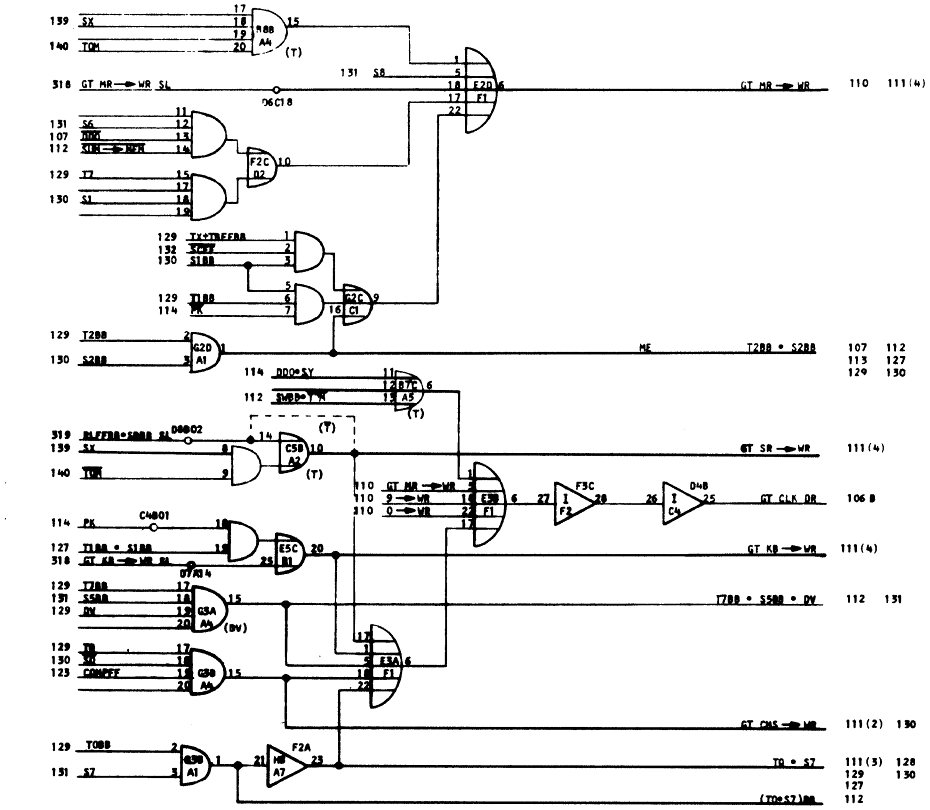
Ref. Page 107

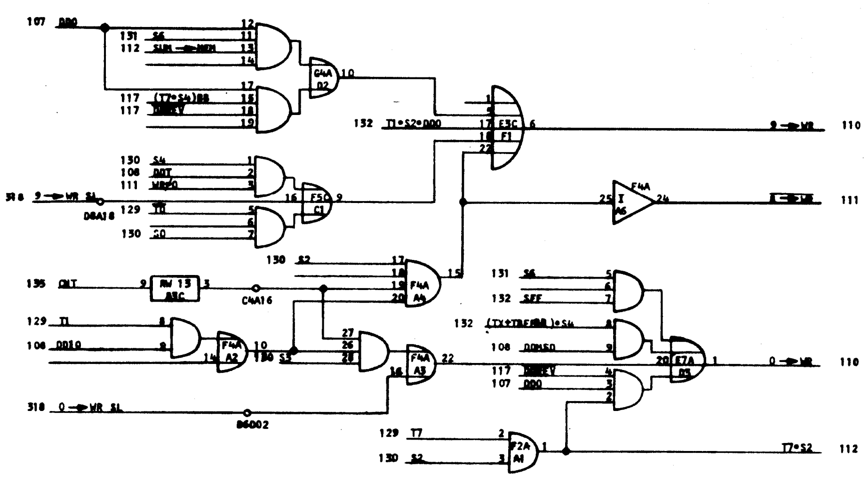


Ref. Page 108

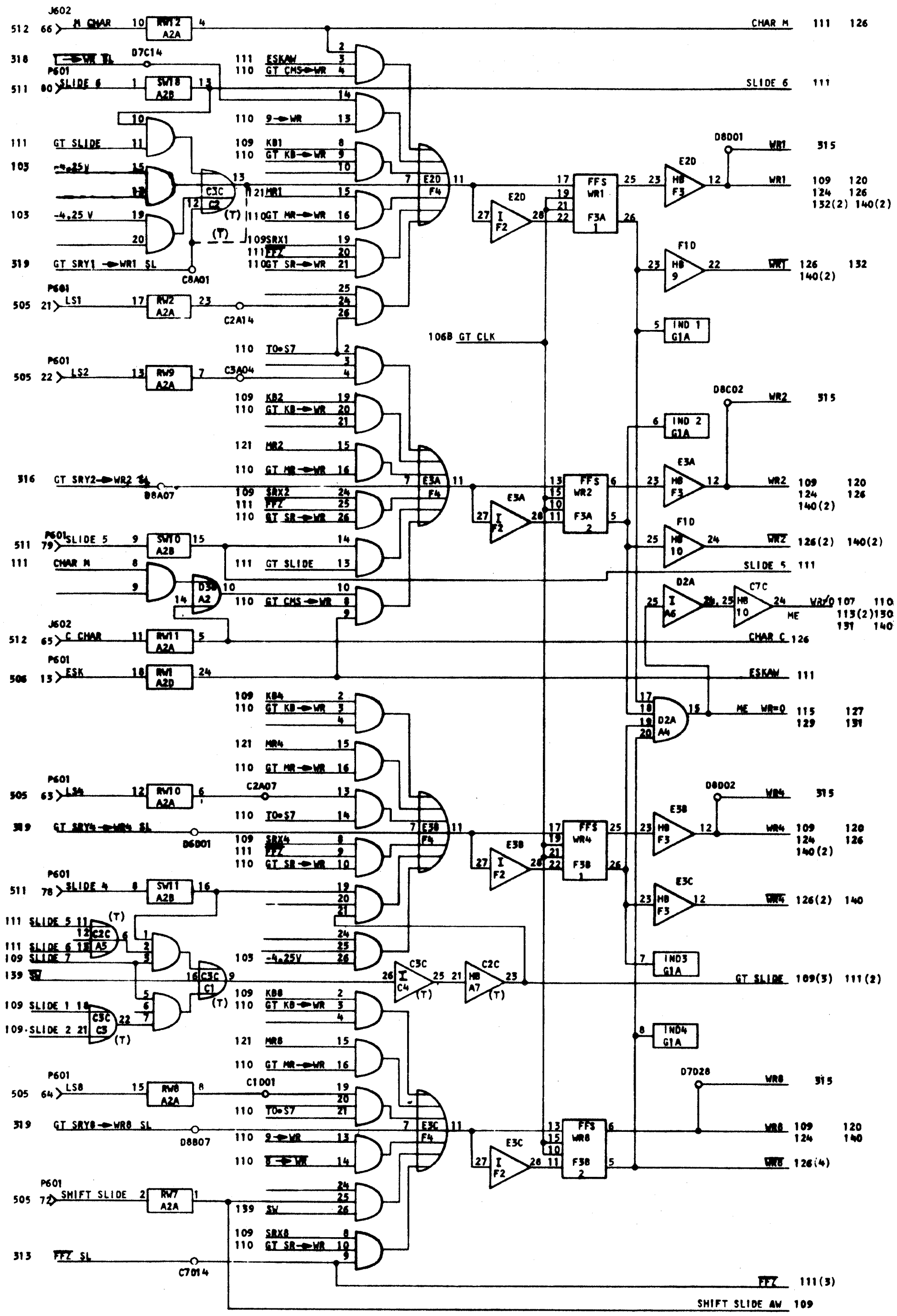

KEYBOARD SWITCHES PAGE 512
J602
KBD8
KBD5
KBD4
KBD9
KBD6
KBD2
KBD7
KBD3
KBD1
KB8
KB4
KB2
KB1
SLIDE 7
SHIFT SLIDE AW
GT SLIDE
SLIDE 3
DATA XFF SL
SLIDE 2
SLIDE 1
ASRX SL
GT WR→SRX SL
SRX CLK SL
FFS
SRX1
SRX2
SRX4
SRX8
+35 CTR

Ref. Page 109

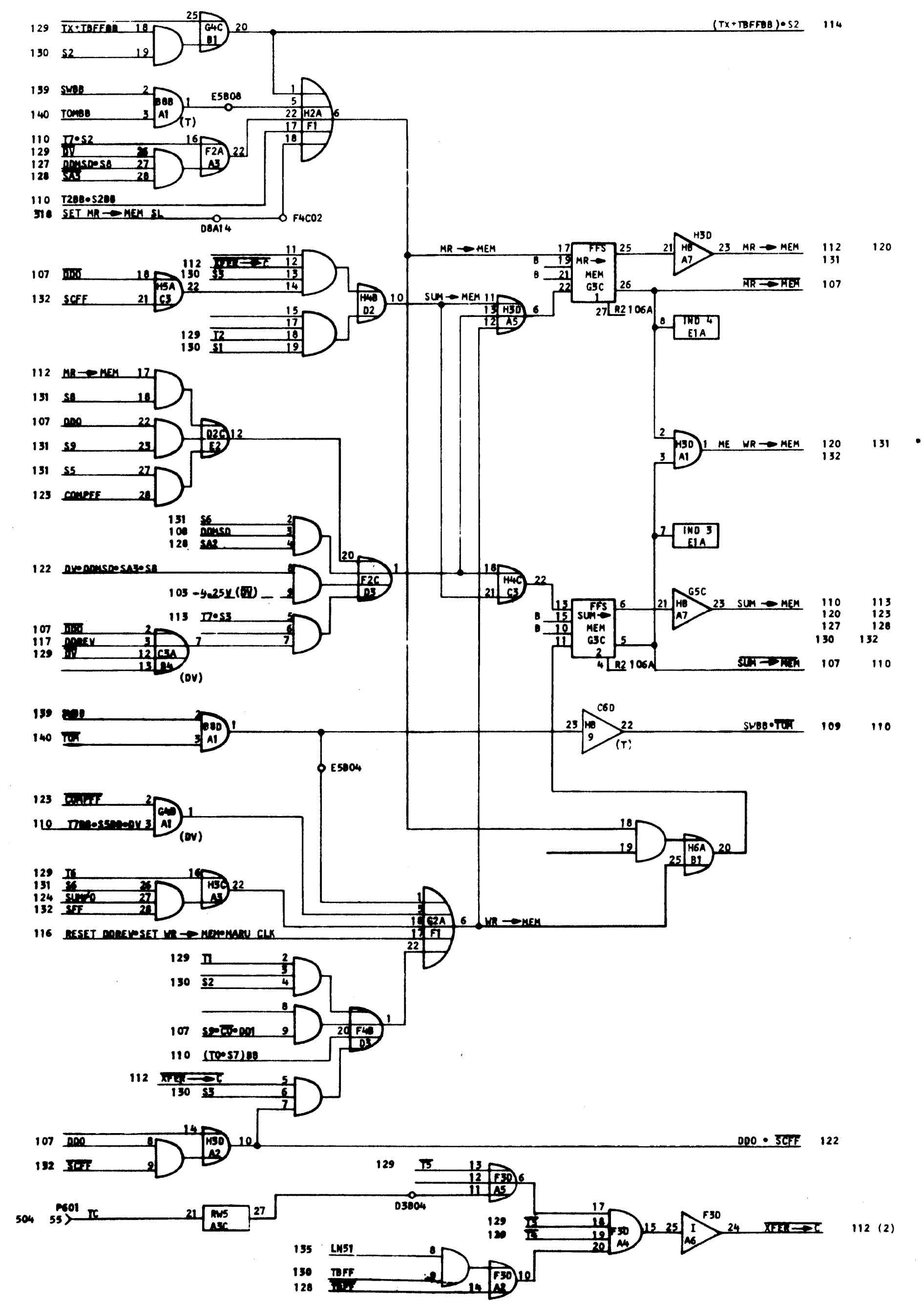

GT MR → WR
T2BB • S2BB
GT SR → WR
GT CLK DR
GT KB → WR
T7BB • S5BB • DV
GT CNS → WR
TO • S7
(TO•S7)BB


9 → WR
0 → WR
T7•S2

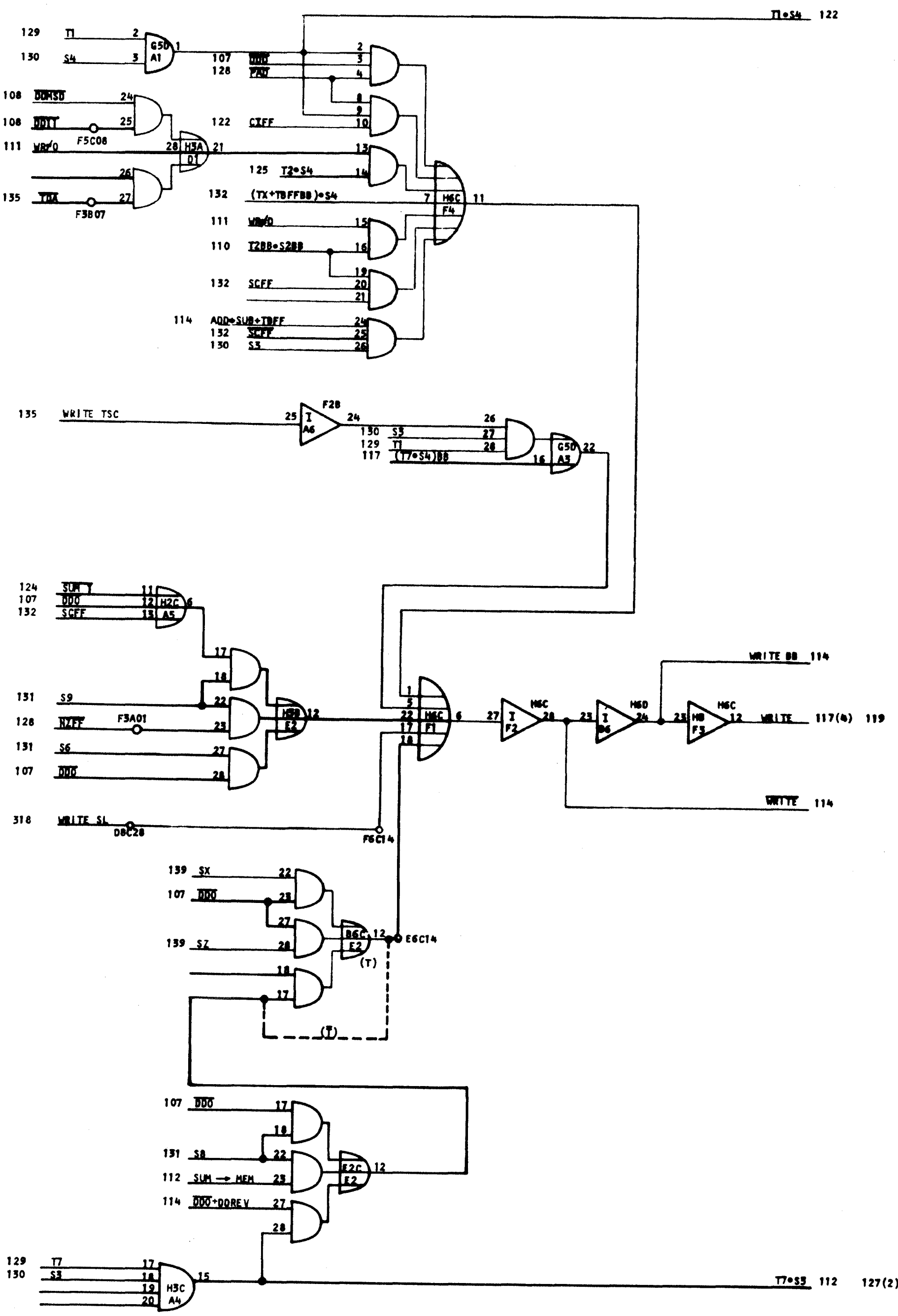
Ref. Page 110



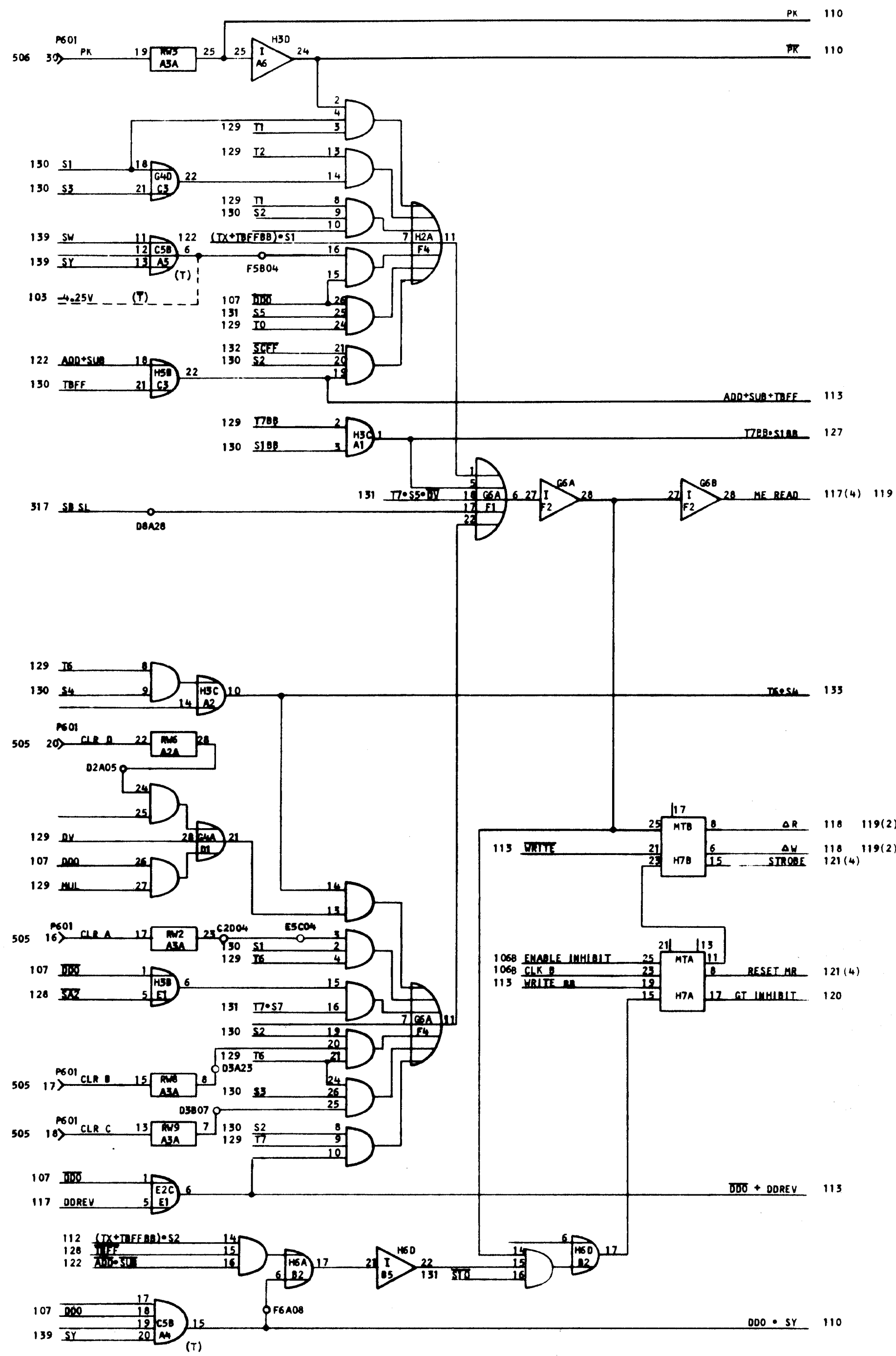
Ref. Page 111


(TX+TBFFBB)•S2
MR → MEM
SUM → MEM
WR → MEM
SWBB•TOM
DDO • SCFF
XFER → C
IND 4
IND 3
E5B08
E5B04
F4C02
D8A14
D3B04
SET MR → MEM SL
RESET DDREV•SET WR → MEM•MARU CLK

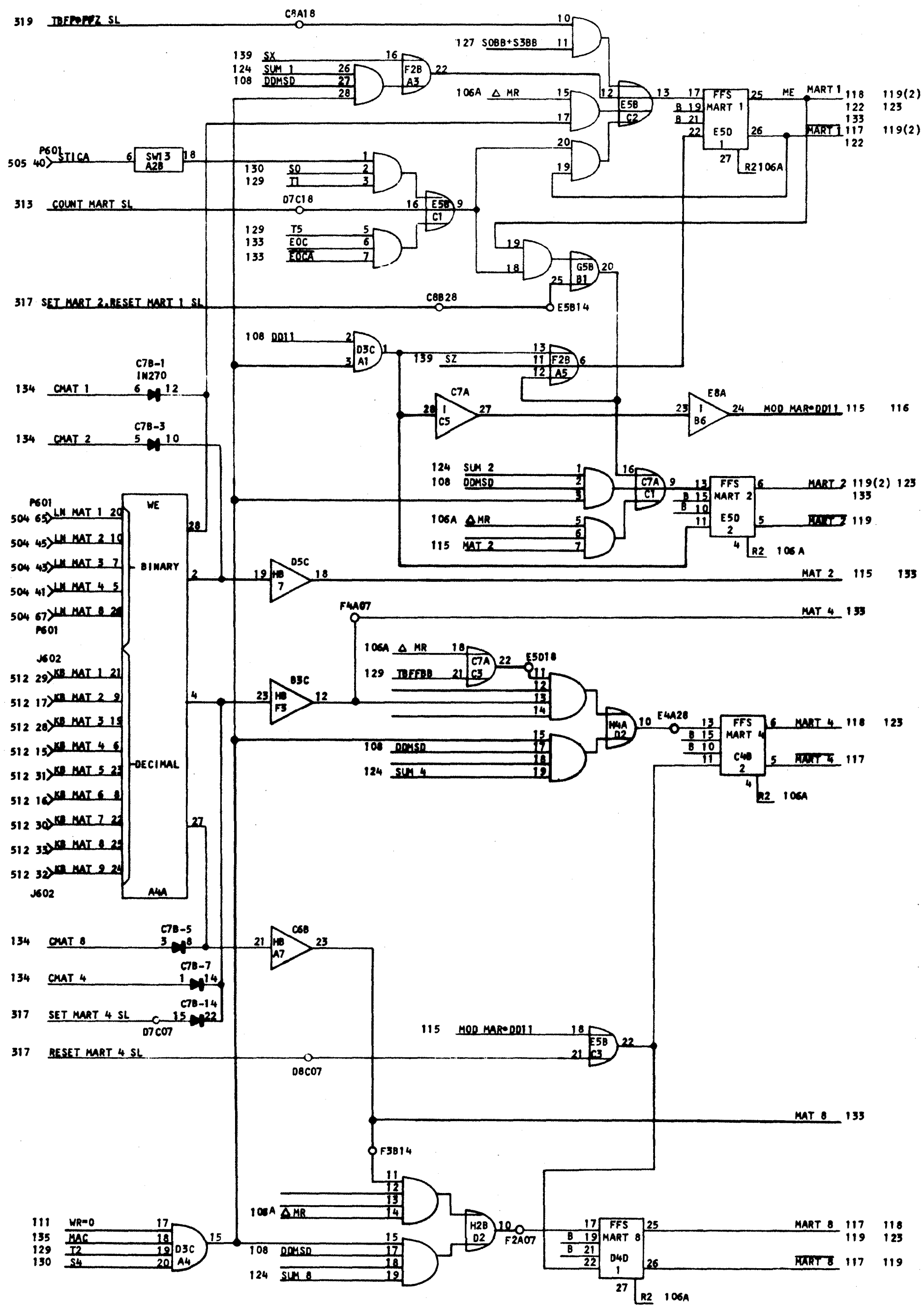
Ref. Page 112


T1•S4 122
WRITE BB 114
WRITE 117(4) 119
WRITE 114
T7•S3 112 127(2)
WRITE TSC
WRITE SL
SUM → MEM

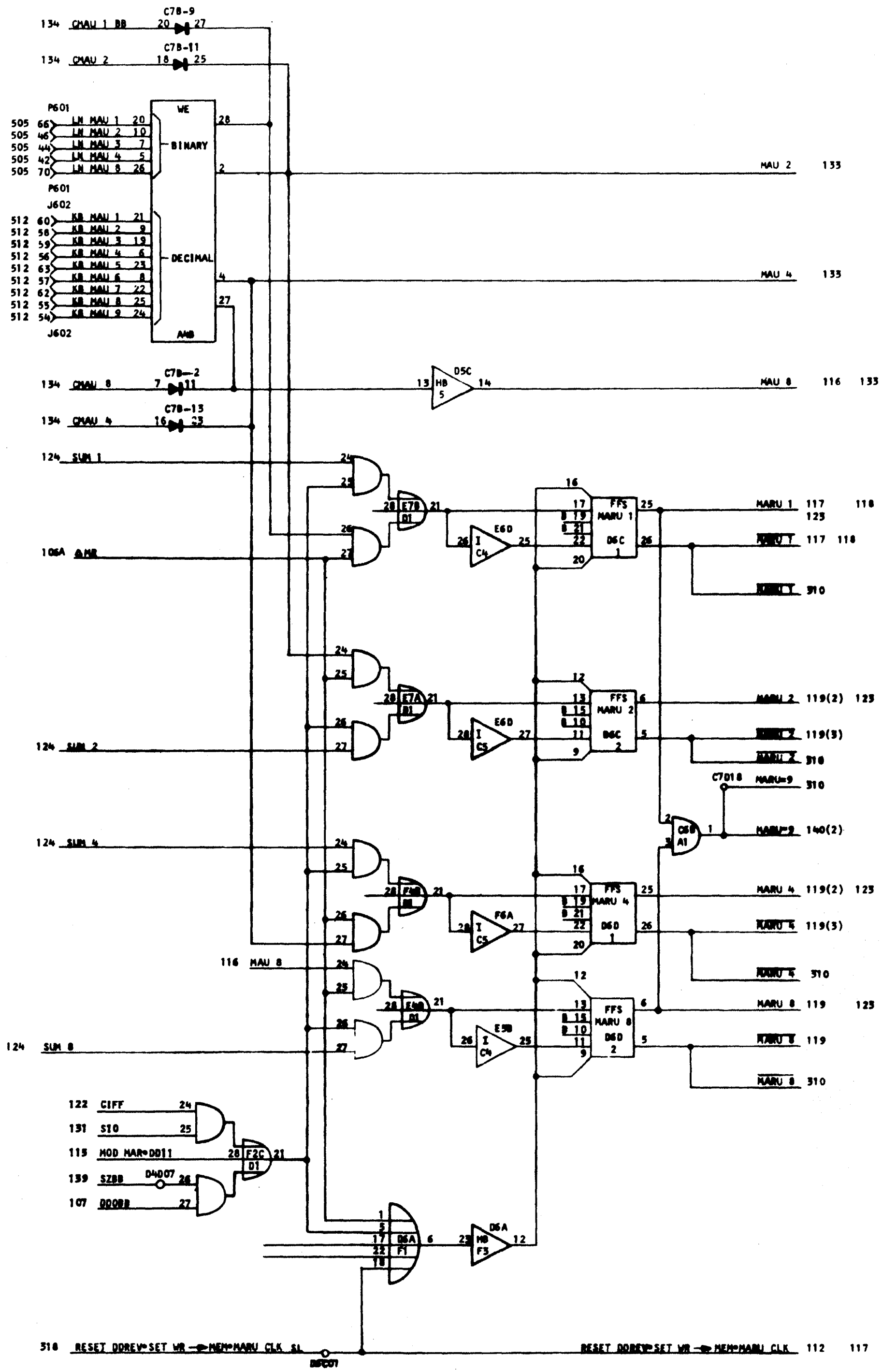
Ref. Page 113



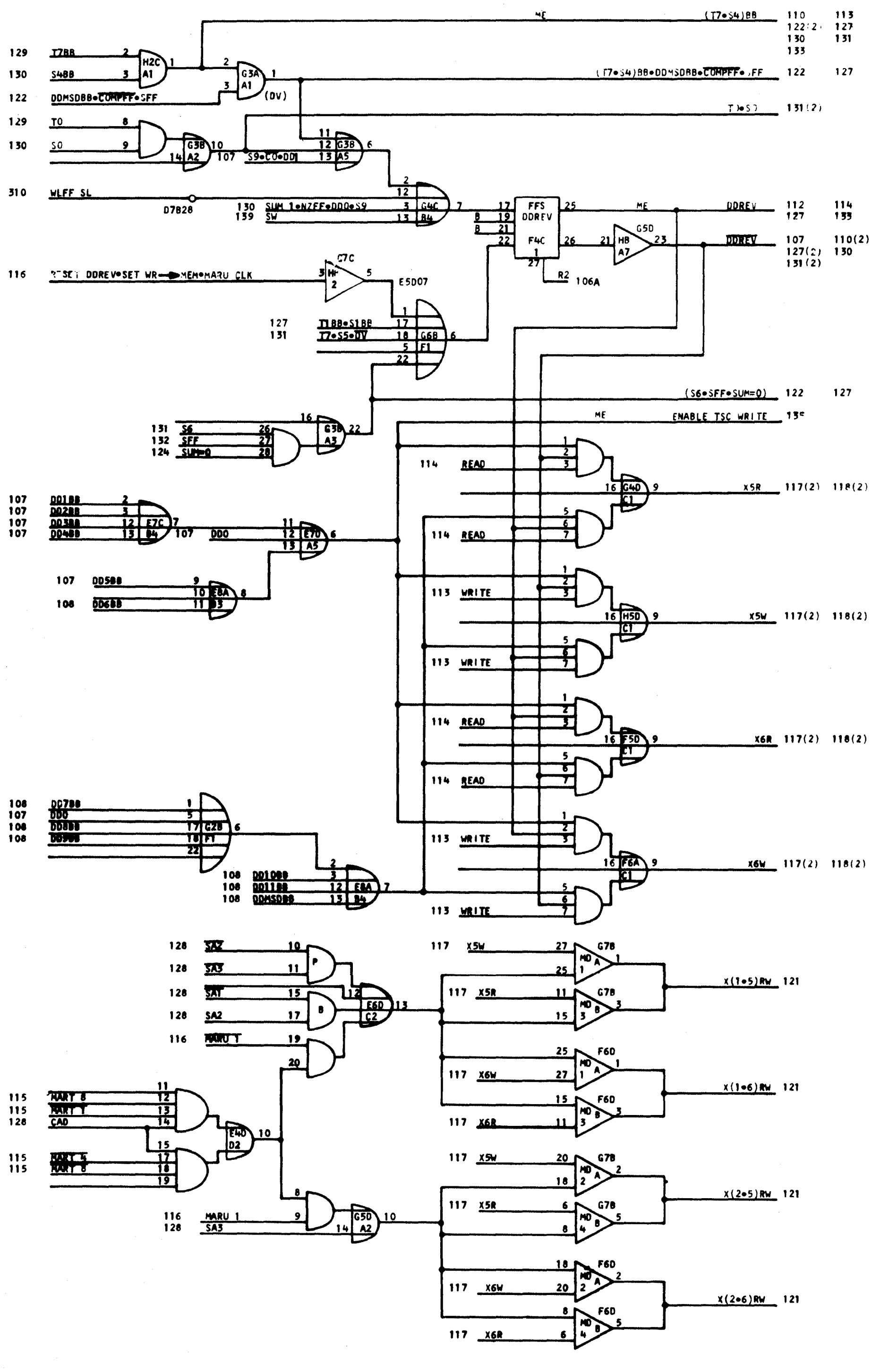
Ref. Page 114


319 TBFP•PPZ SL
127 S0BB+S3BB
139 SX
124 SUM 1
108 DDMSD
106A △ MR
FFS
MART 1
E5D
ME
MART 1
MART 1
505 40 STICA
SW13 A28
130 S0
129 T1
313 COUNT MART SL
129 T5
133 EOC
133 EOCA
317 SET MART 2.RESET MART 1 SL
108 DD11
139 SZ
134 CMAT 1
134 CMAT 2
MOD MAR•DD11
124 SUM 2
108 DDMSD
106A △MR
115 MAT 2
FFS
MART 2
E5D
MART 2
MART 2
LN MAT 1
LN MAT 2
LN MAT 3
LN MAT 4
LN MAT 8
BINARY
KB MAT 1
KB MAT 2
KB MAT 3
KB MAT 4
KB MAT 5
KB MAT 6
KB MAT 7
KB MAT 8
KB MAT 9
DECIMAL
MAT 2
MAT 4
106A △ MR
129 TBFFBB
108 DDMSD
124 SUM 4
FFS
MART 4
MART 4
MART 4
134 CMAT 8
134 CMAT 4
317 SET MART 4 SL
317 RESET MART 4 SL
115 MOD MAR•DD11
MAT 8
111 WR=0
135 MAC
129 T2
130 S4
106A △MR
108 DDMSD
124 SUM 8
FFS
MART 8
MART 8
MART 8

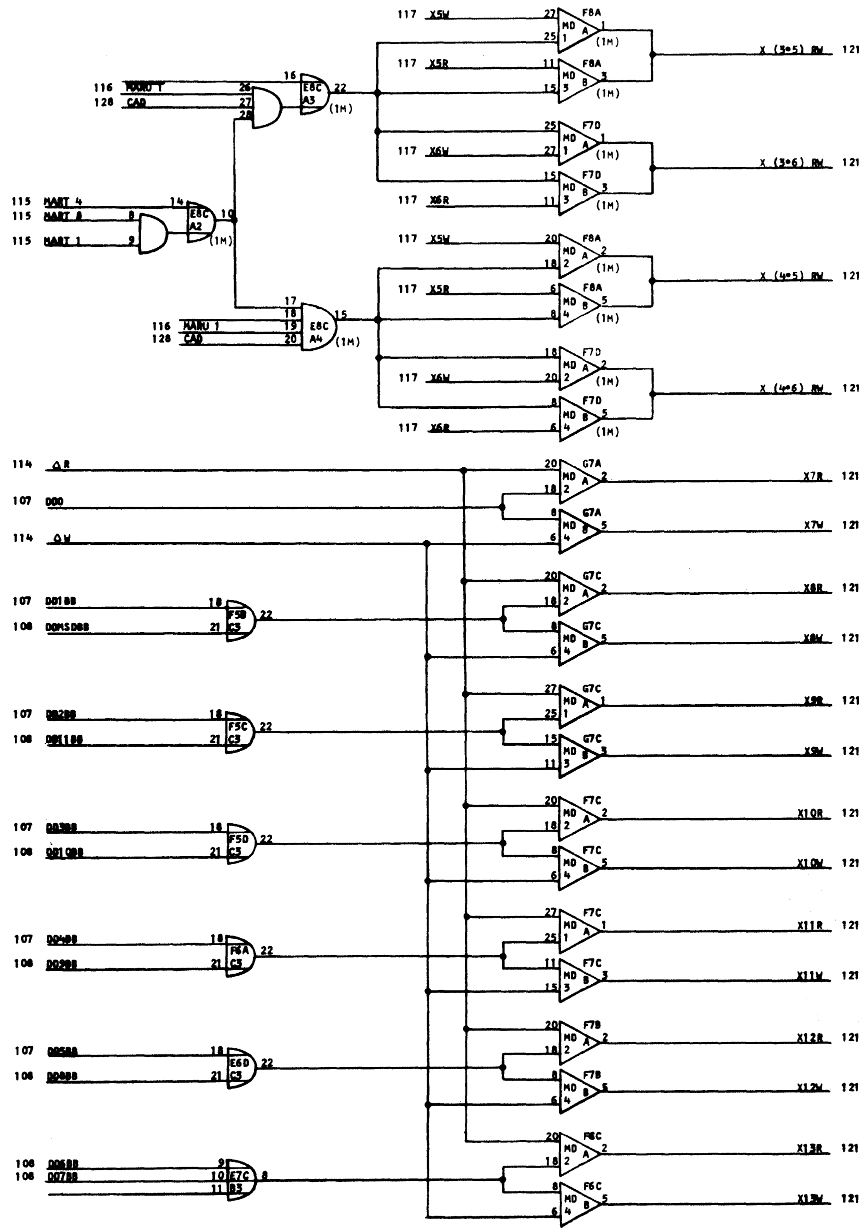
Ref. Page 115


CMAU 1 BB
CMAU 2
CMAU 8
CMAU 4
BINARY
DECIMAL
SUM 1
SUM 2
SUM 4
SUM 8
MAU 2
MAU 4
MAU 8
MARU 1
MARU 2
MARU 4
MARU 8
CIFF
S10
MOD MAR=D011
SZBB
D00BB
RESET DDREV=SET WR → MEM=MARU CLK SL

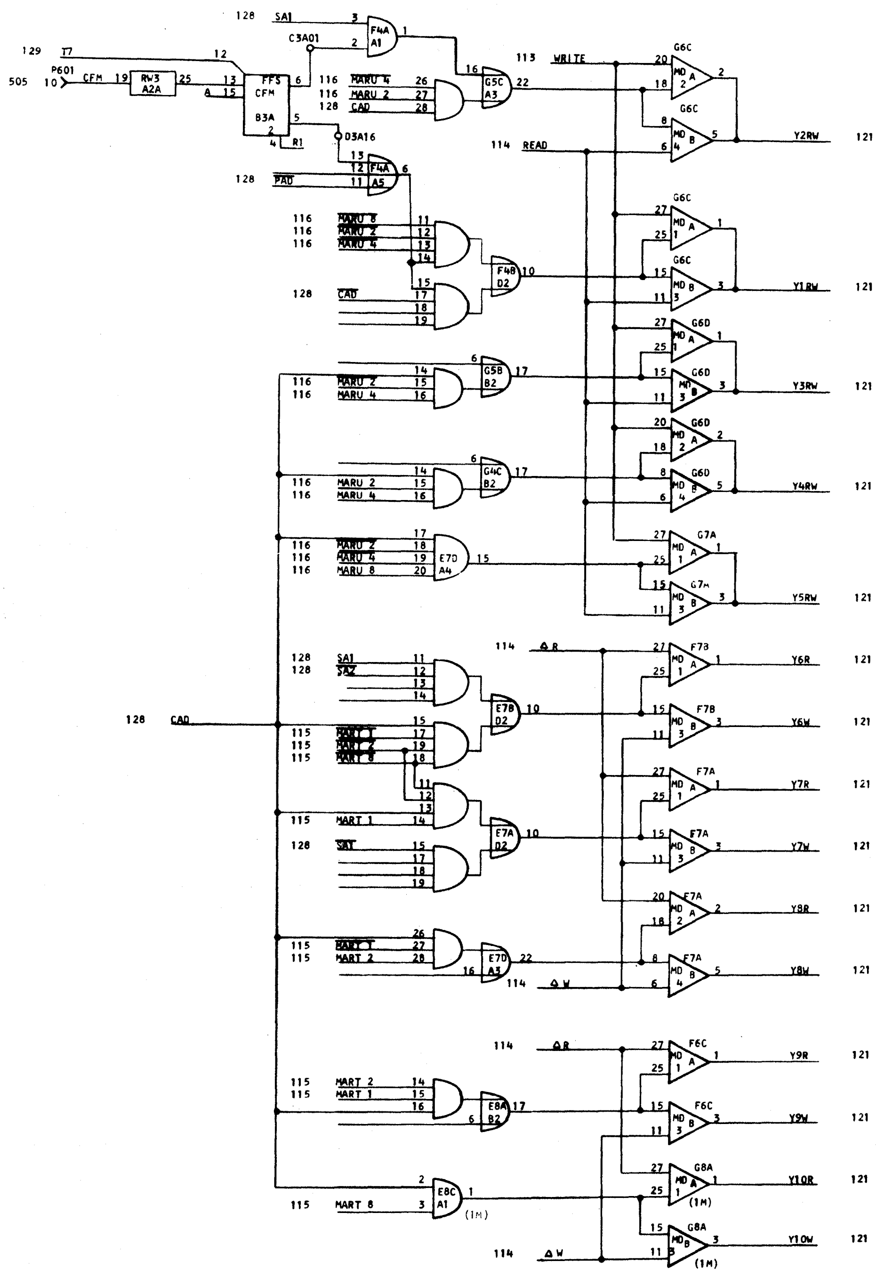
Ref. Page 116



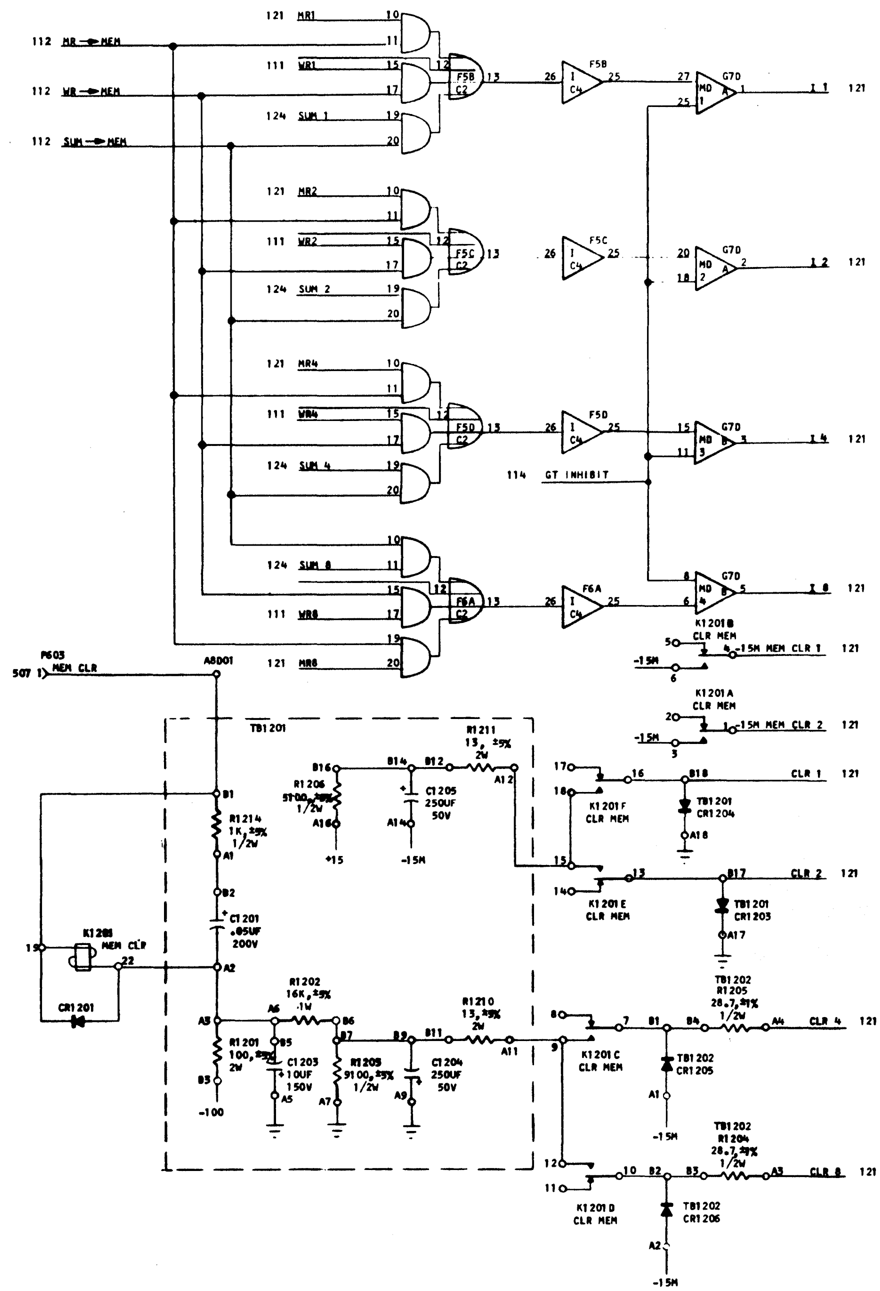
Ref. Page 117


117 X5W
117 X5R
117 X6W
117 X6R
X (3•5) RW 121
X (3•6) RW 121
X (4•5) RW 121
X (4•6) RW 121
115 MART 4
115 MART 8
115 MART 1
116 MARU 1
128 CAD
114 ΔR
107 DD0
114 ΔW
X7R 121
X7W 121
X8R 121
X8W 121
X9R 121
X9W 121
X10R 121
X10W 121
X11R 121
X11W 121
X12R 121
X12W 121
X13R 121
X13W 121

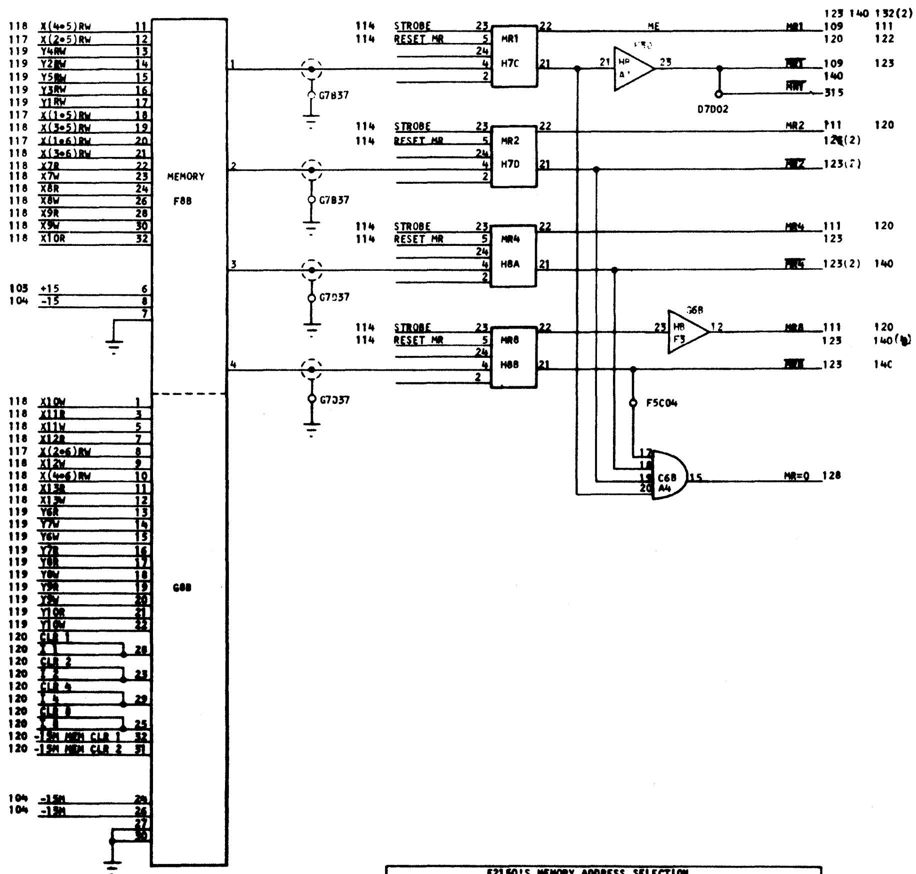
Ref. Page 118



Ref. Page 119



Ref. Page 120



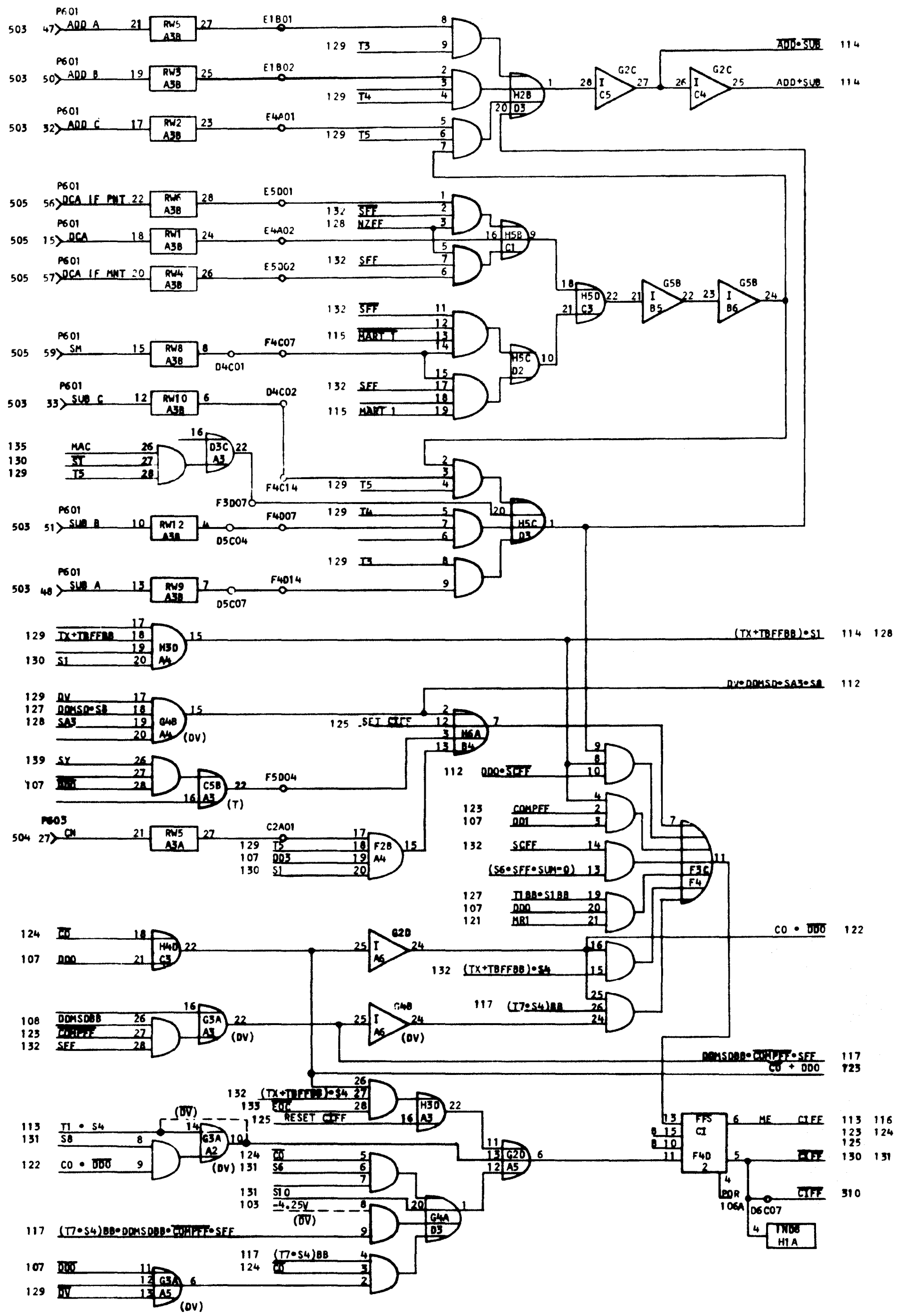
MEMORY SIZE	MEMORY LOCATIONS
40 WORD	00-39
100 WORD	00-99

DIGIT POSITION	12 X
0	7.5
1	8.5
2	9.5
3	10.5
4	11.5
5	12.5
6	13.5
7	13.6
8	12.6
9	11.6
10	10.6
11	9.6
12	8.6

E2150'S MEMORY ADDRESS SELECTION

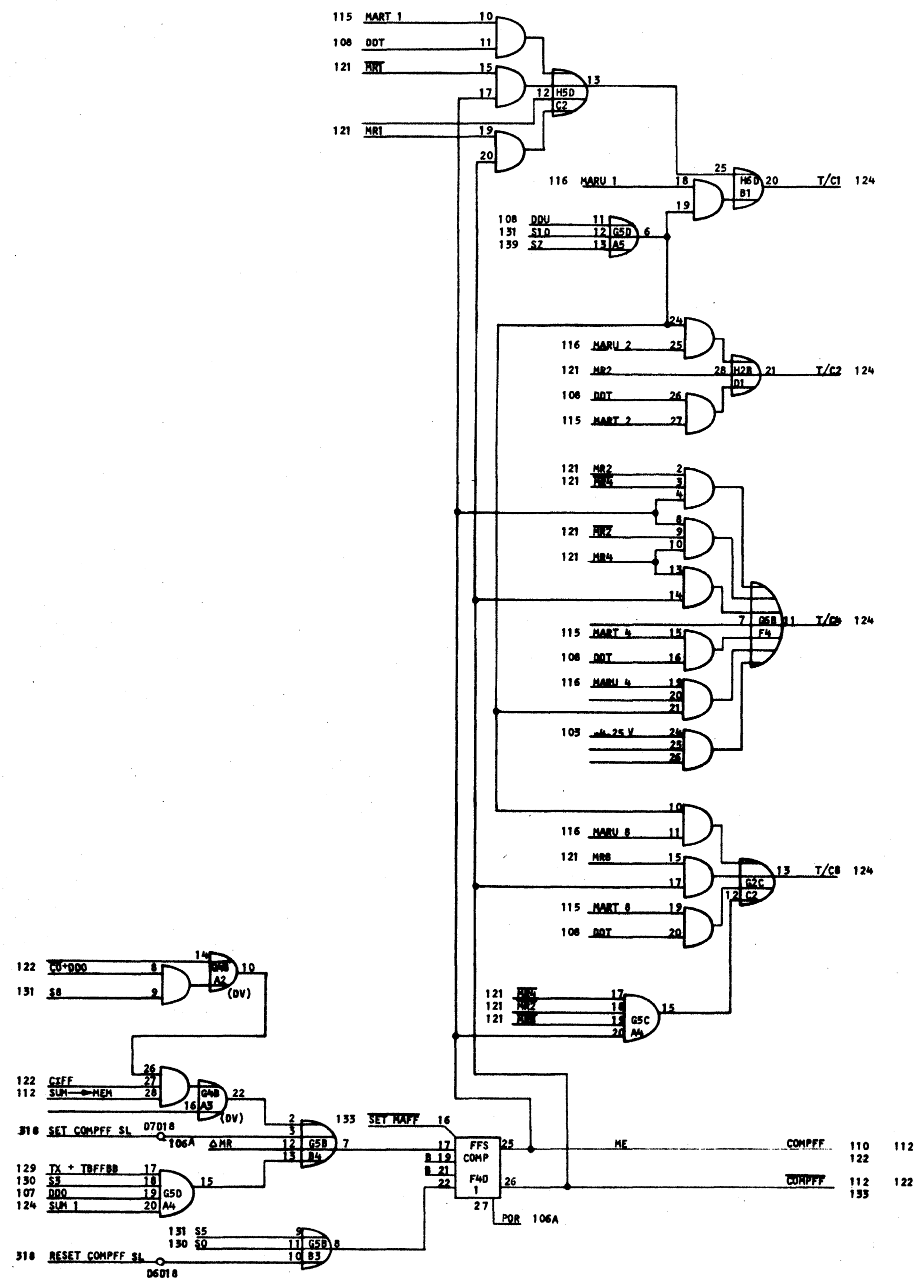
SPEC ADR	MEMORY LOCATION	X	Y	MEMORY LOCATION	X	Y	MEMORY LOCATION	X	Y
P	00	1	1.6	34	1	3.9	68	3	5.8
A	01	2	1.6	35	2	3.9	69	4	5.8
CFM	02	1	2.6	36	1	4.9	70	3	1.9
	03	2	2.6	37	2	4.9	71	4	1.9
	04	1	3.6	38	1	5.9	72	3	2.9
	05	2	3.6	39	2	5.9	73	4	2.9
	06	1	4.6	40	3	1.6	74	3	3.9
O	07	2	4.6	41	4	1.6	75	4	3.9
	08	1	5.6	42	3	2.6	76	3	4.9
	09	2	5.6	43	4	2.6	77	4	4.9
B	10	1	1.7	44	3	3.6	78	3	5.9
D	11	2	1.7	45	4	3.6	79	4	5.9
	12	1	2.7	46	3	4.6	80	1	1.10
	13	2	2.7	47	4	4.6	81	2	1.10
	14	1	3.7	48	3	5.6	82	1	2.10
	15	2	3.7	49	4	5.6	83	2	2.10
	16	1	4.7	50	3	1.7	84	1	3.10
	17	2	4.7	51	4	1.7	85	2	3.10
	18	1	5.7	52	3	2.7	86	1	4.10
	19	2	5.7	53	4	2.7	87	2	4.10
	20	1	1.8	54	3	3.7	88	1	5.10
	21	2	1.8	55	4	3.7	89	2	5.10
	22	1	2.8	56	3	4.7	90	3	1.10
	23	2	2.8	57	4	4.7	91	4	1.10
	24	1	3.8	58	3	5.7	92	3	2.10
	25	2	3.8	59	4	5.7	93	4	2.10
	26	1	4.8	60	3	1.8	94	3	3.10
	27	2	4.8	61	4	1.8	95	4	3.10
	28	1	5.8	62	3	2.8	96	3	4.10
	29	2	5.8	63	4	2.8	97	4	4.10
	30	1	1.9	64	3	3.8	98	3	5.10
	31	2	1.9	65	4	3.8	99	4	5.10
	32	1	2.9	66	3	4.8			
	33	2	2.9	67	4	4.8			

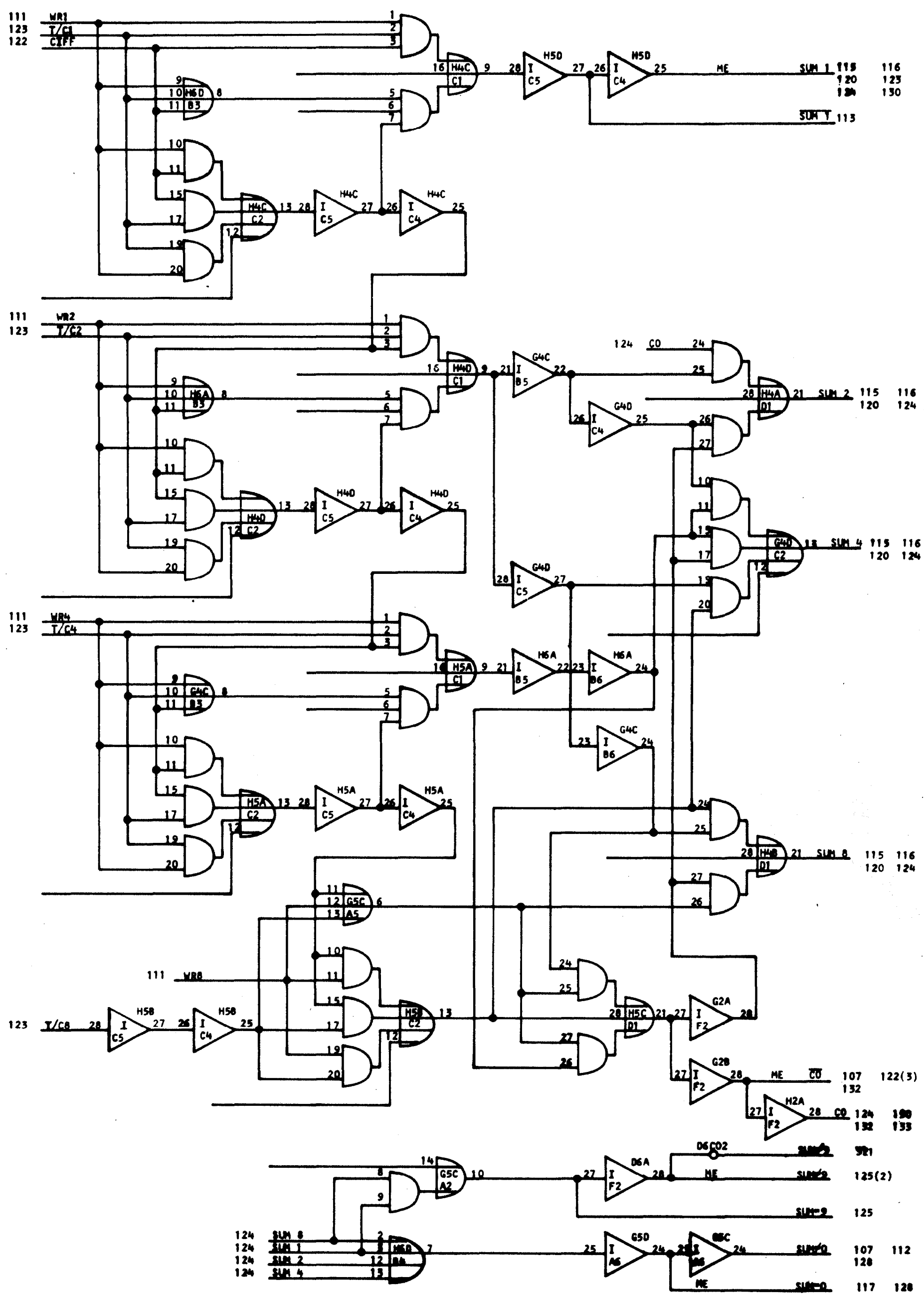
Ref. Page 121



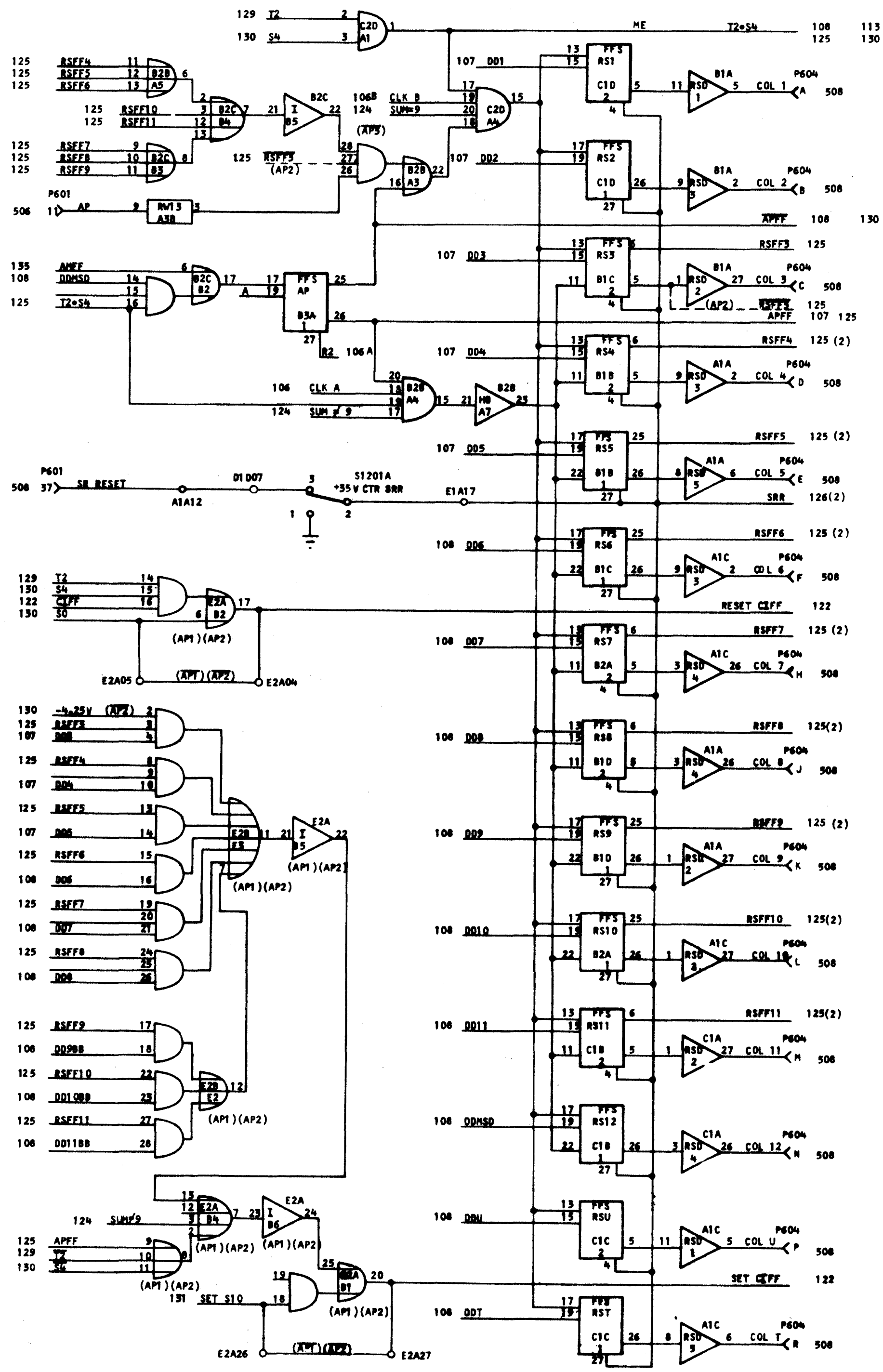
P601
ADD A
ADD B
ADD C
DCA IF MNT
DCA
SM
SUB C
SUB B
SUB A
MAC
T5
T4
T3
SFF
NZFF
H2B
H5B
H5D
H5C
G2C
G5B
ADD+SUB
CO • DDO
RESET CIFF
DDMSDBB
COMPFF
SCFF
F3C
F4D
106A
D6C07
H1A

Ref. Page 122

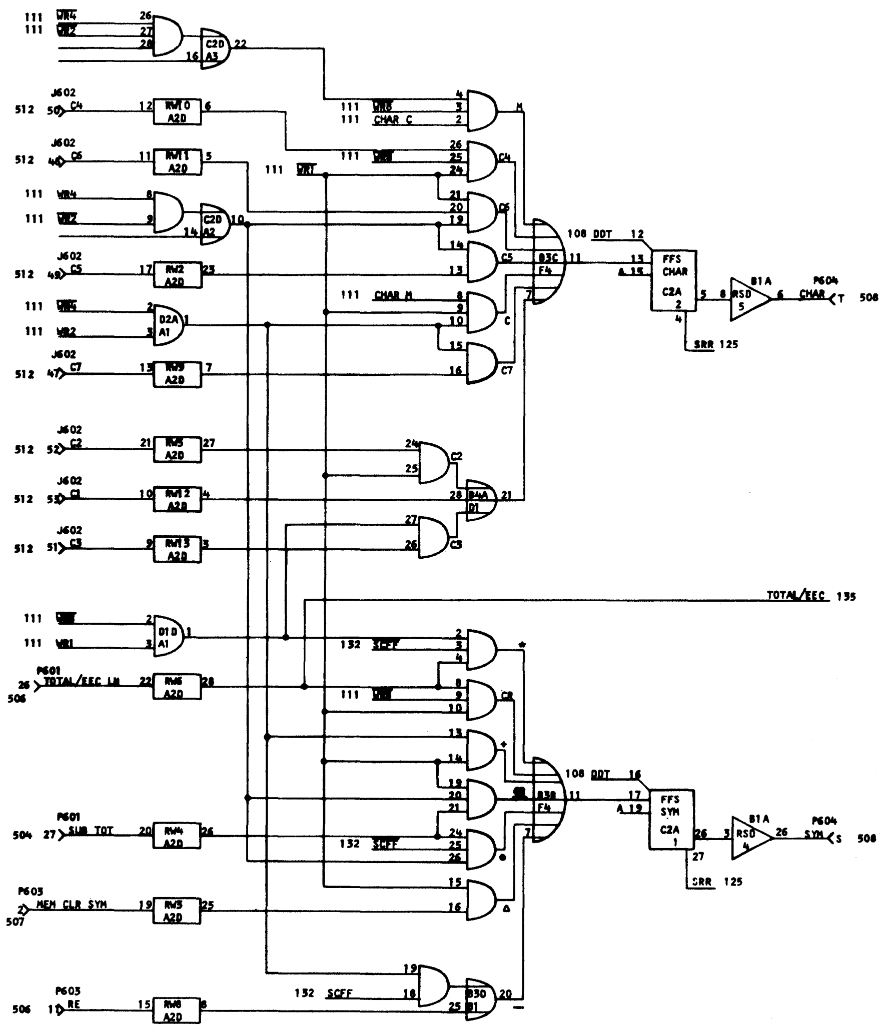




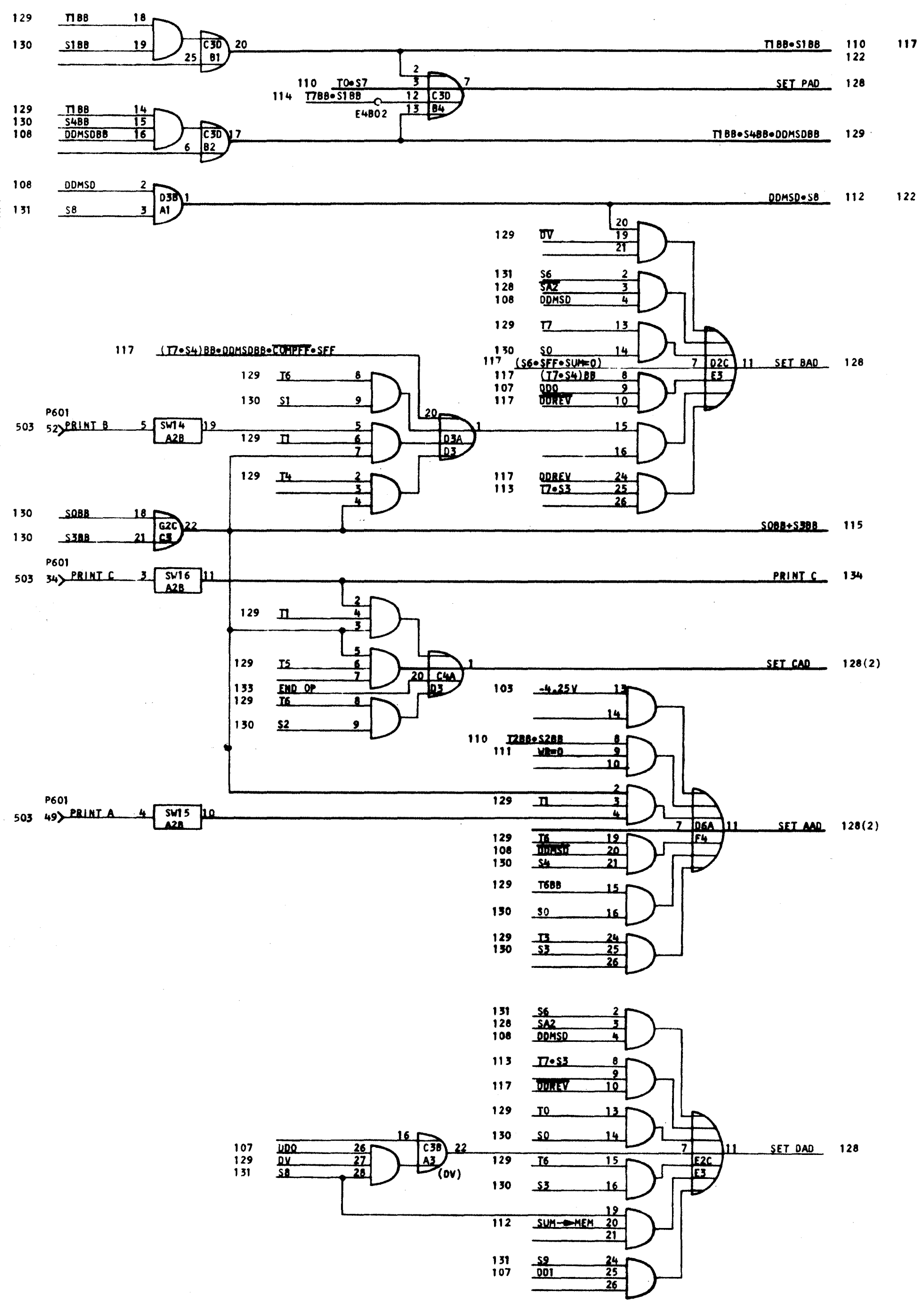
Ref. Page 124



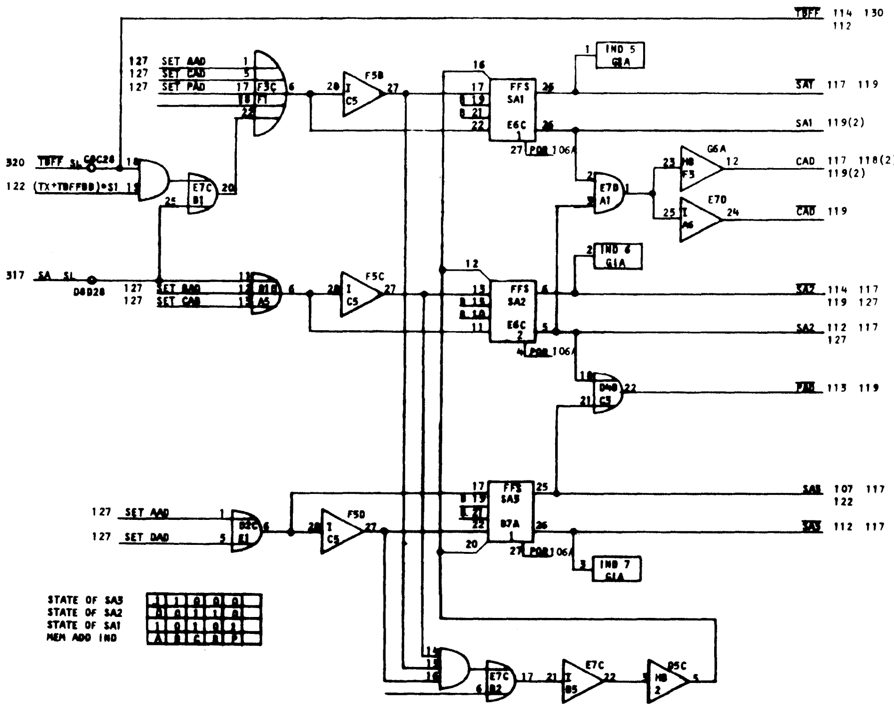
Ref. Page 125

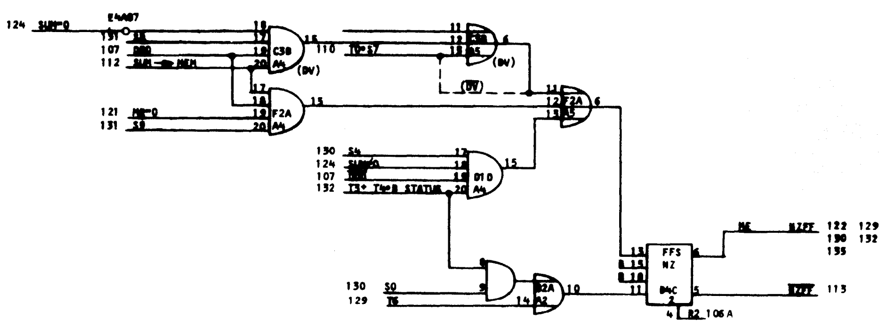

TOTAL/EEC 135
108 DDT
FFS
CHAR
FFS
SYM
SRR 125
CHAR C
CHAR M
MEM CLR SYM
SUB TOT
TOTAL/EEC LN
SCFF

Ref. Page 126

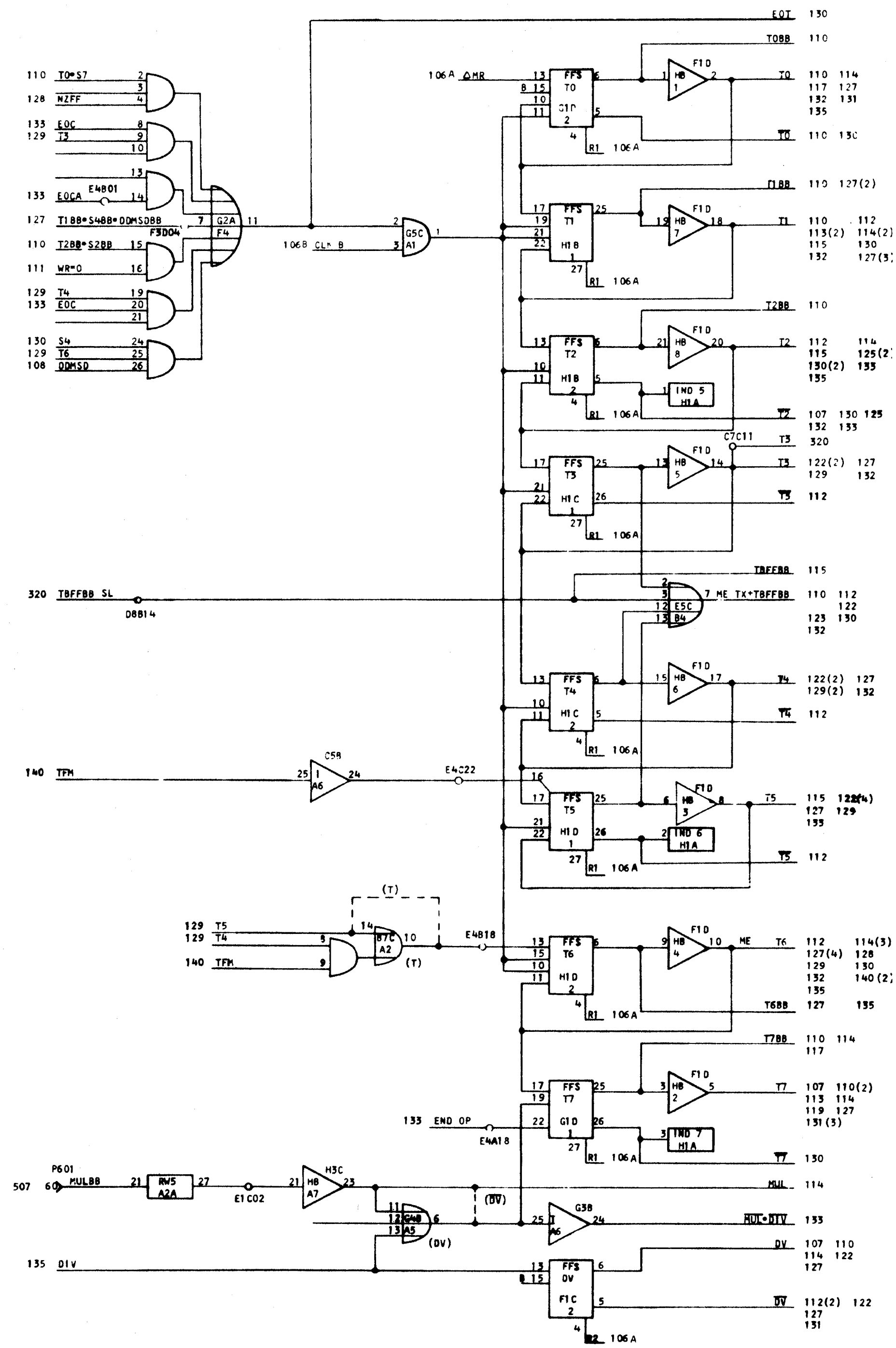


Ref. Page 127

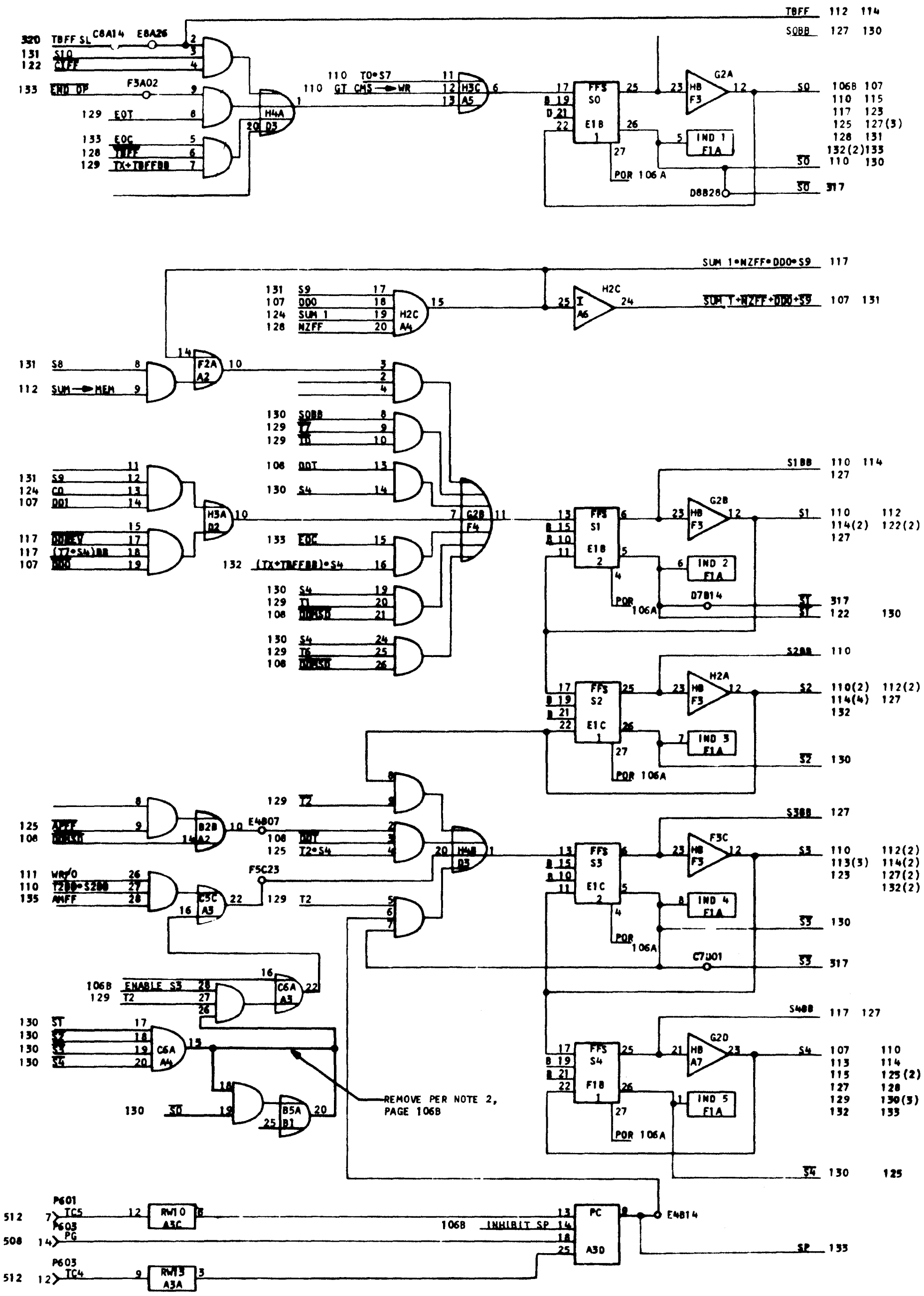

127 SET AAD
127 SET CAD
127 SET PAD
320
122
317
127 SET DAD
STATE OF SA3
STATE OF SA2
STATE OF SA1
MEM ADD IND
114 130
112
117 119
SA1 119(2)
CAD 117 118(2)
119(2)
119
114 117
119 127
112 117
127
113 119
107 117
122
112 117


124
107
112
121
131
130
124
107
132
130
129
122 129
190 132
135
113
106A

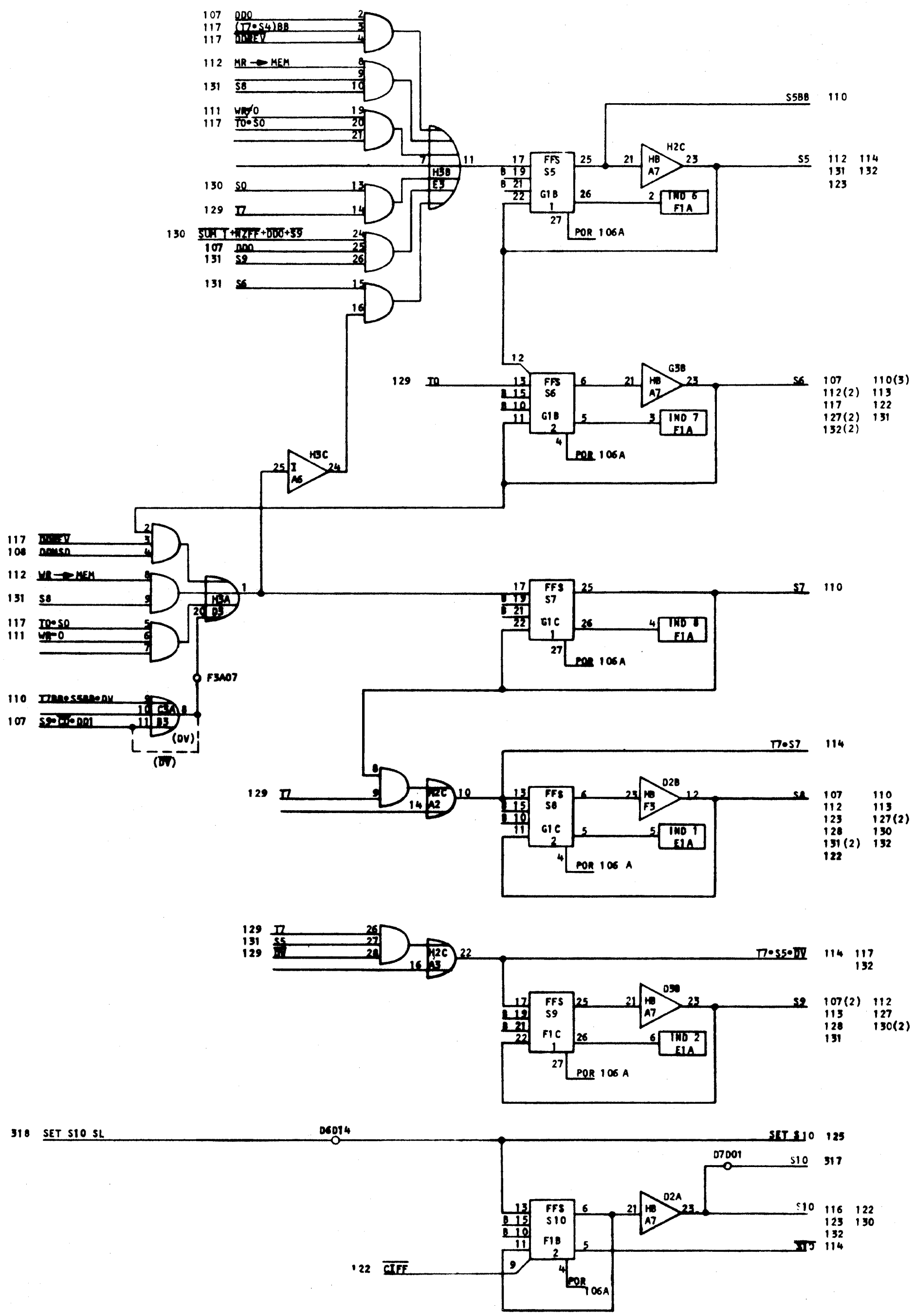
Ref. Page 128



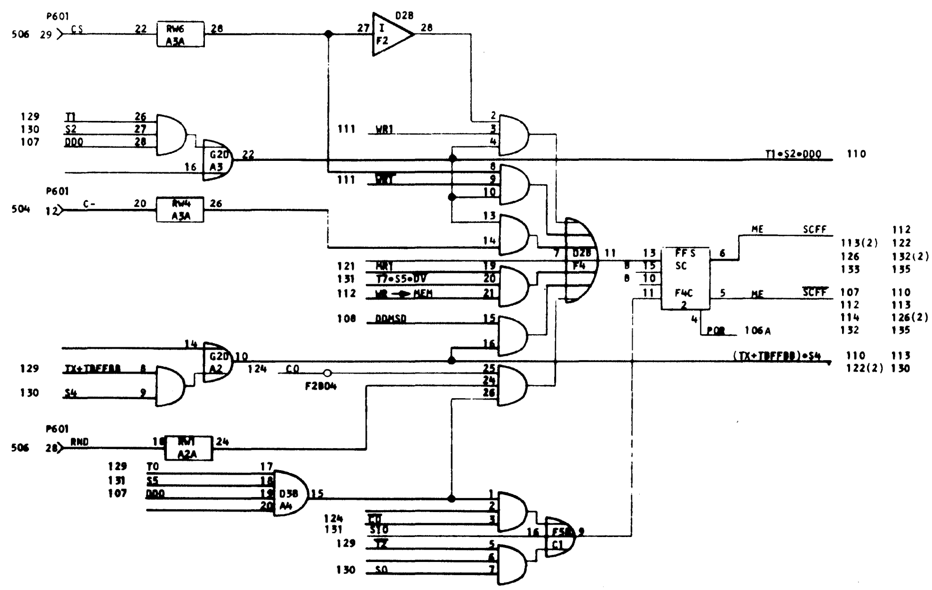
Ref. Page 129

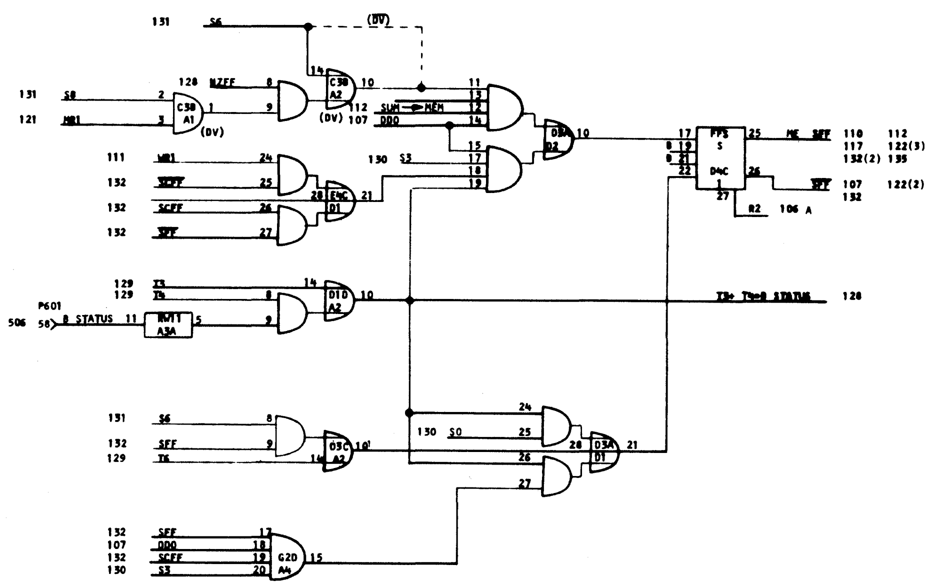


Ref. Page 130

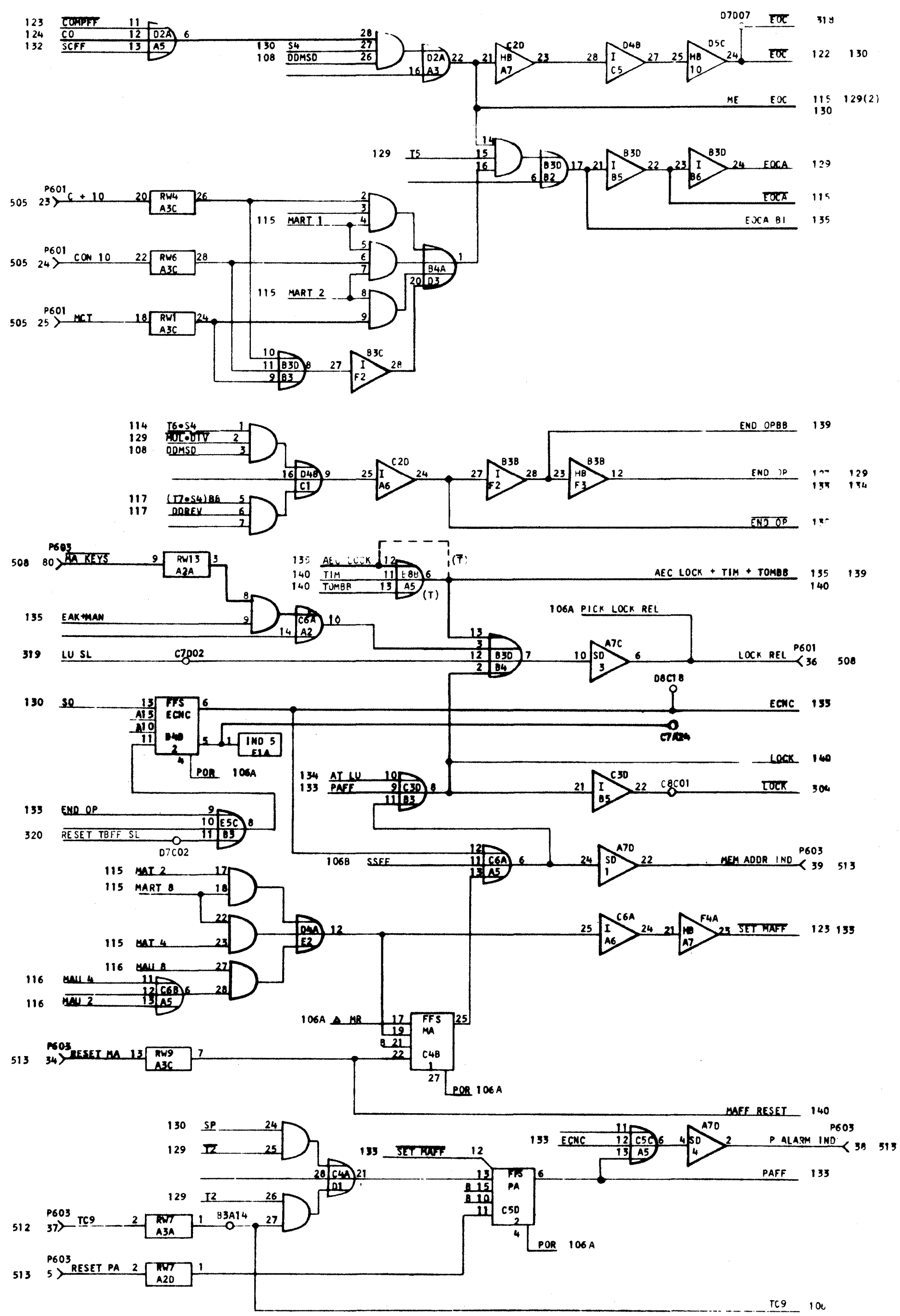


Ref. Page 131

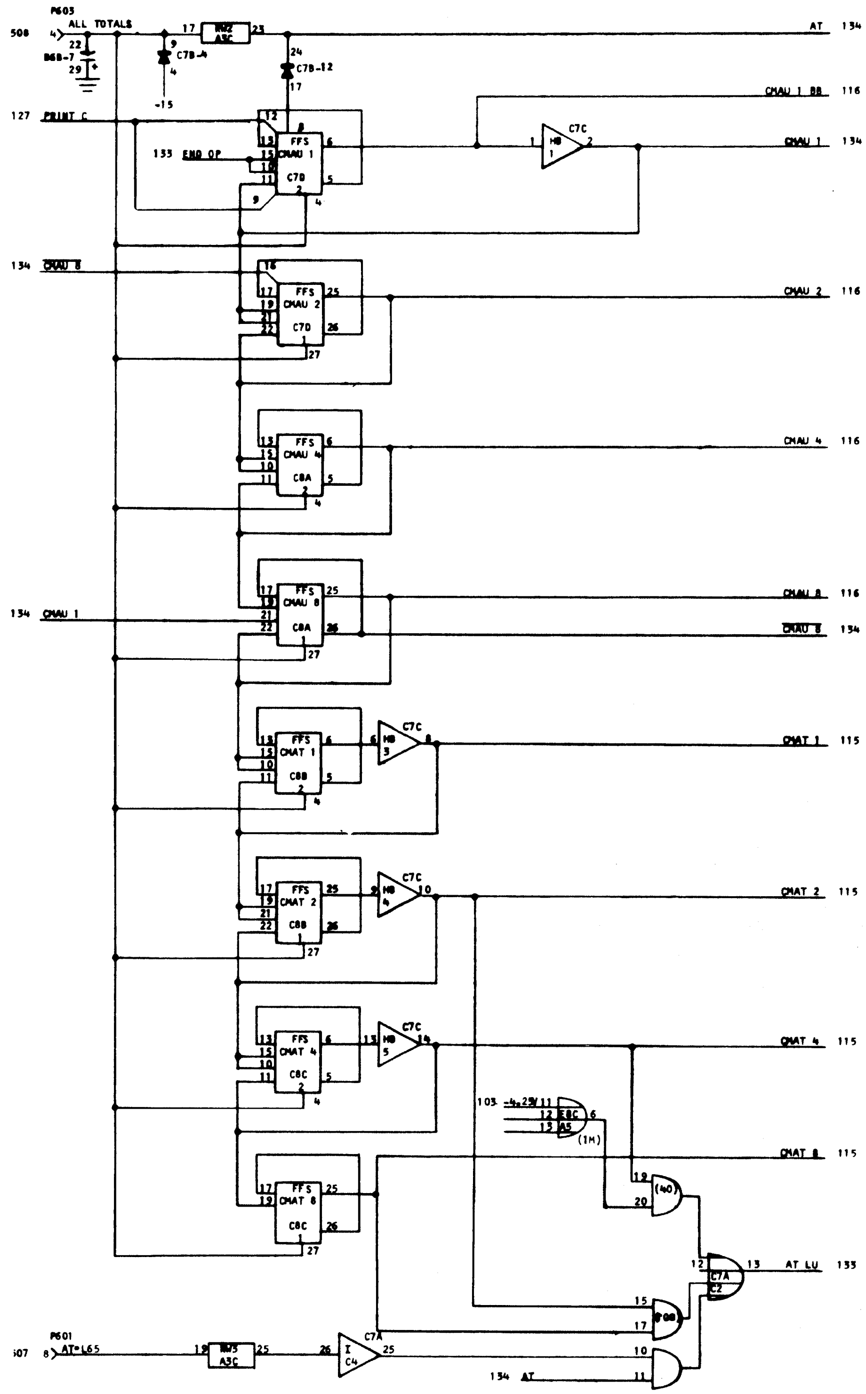




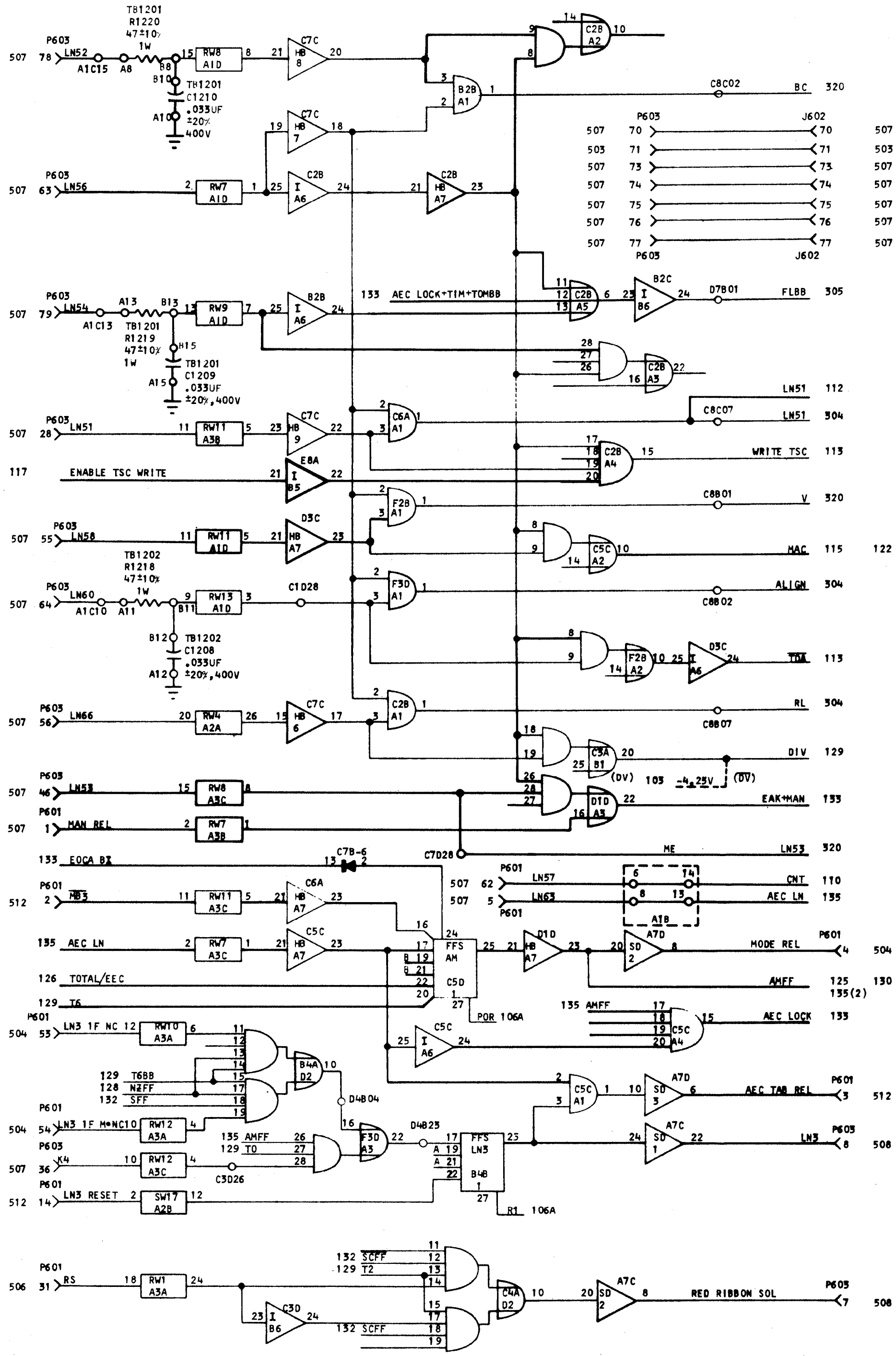
Ref. Page 132



Ref. Page 133



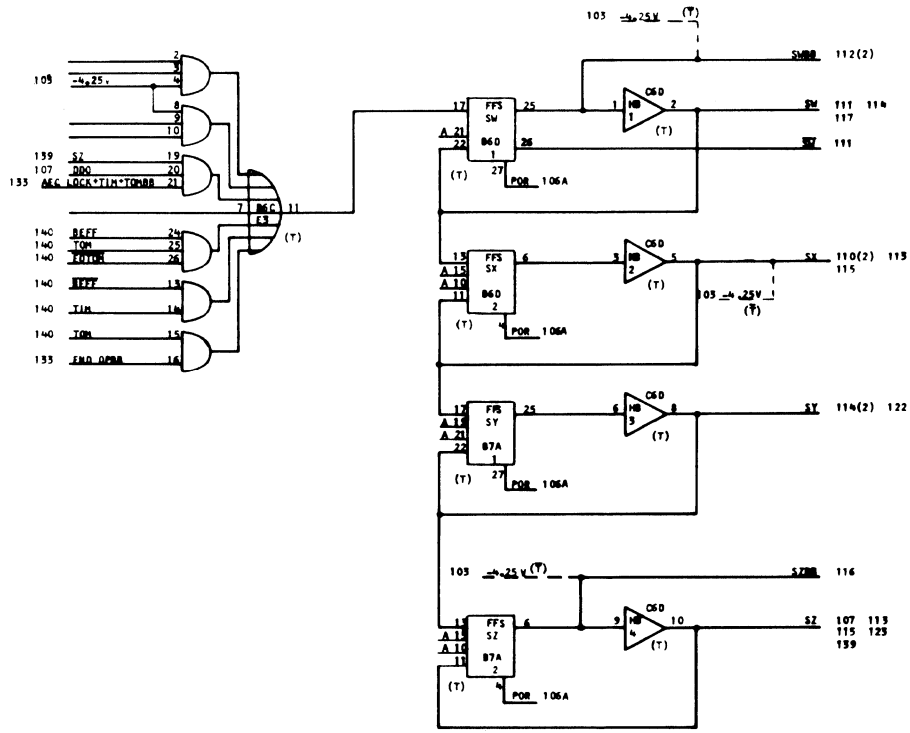
Ref. Page 134



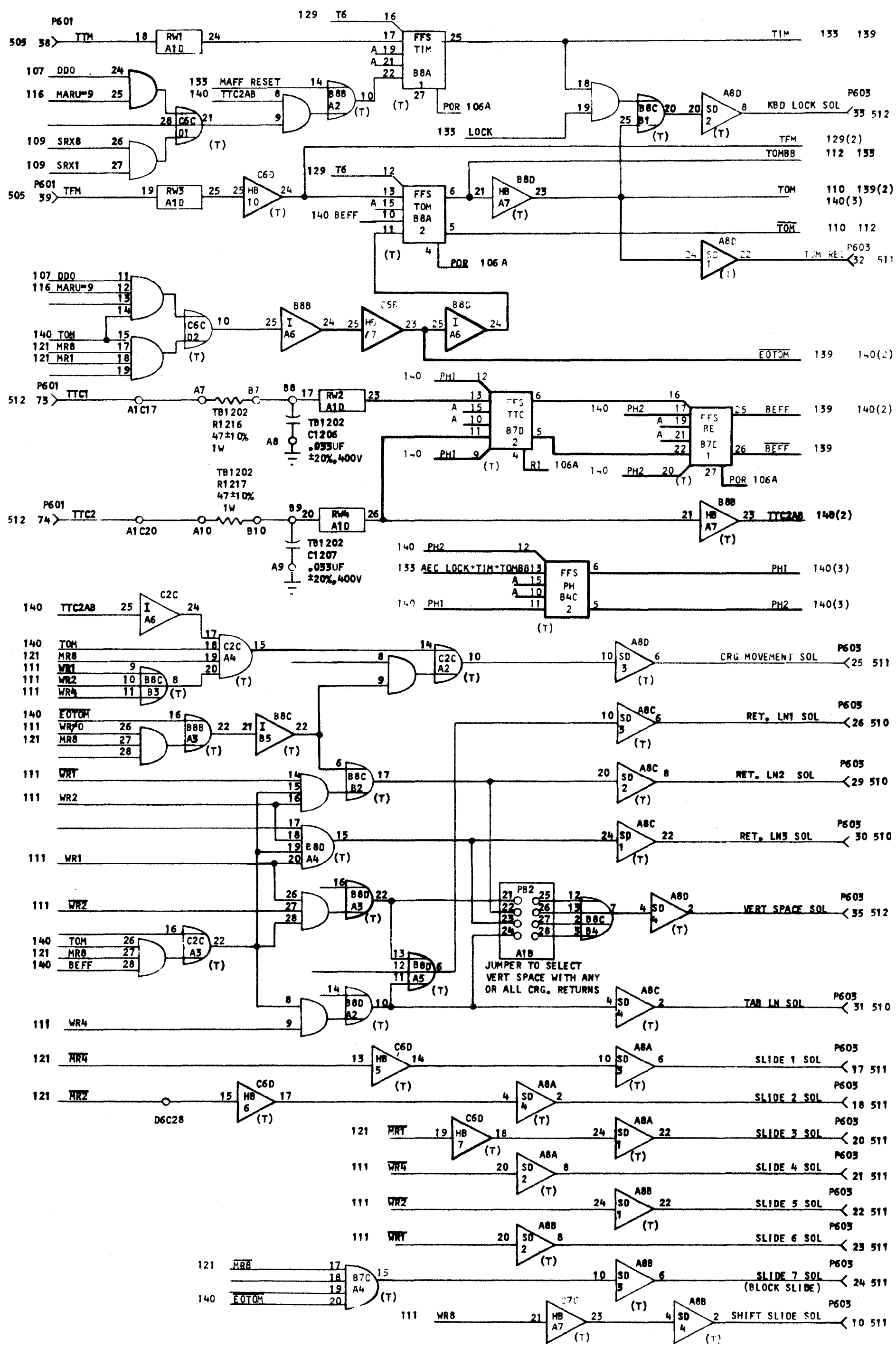
Ref. Page 135

Note:

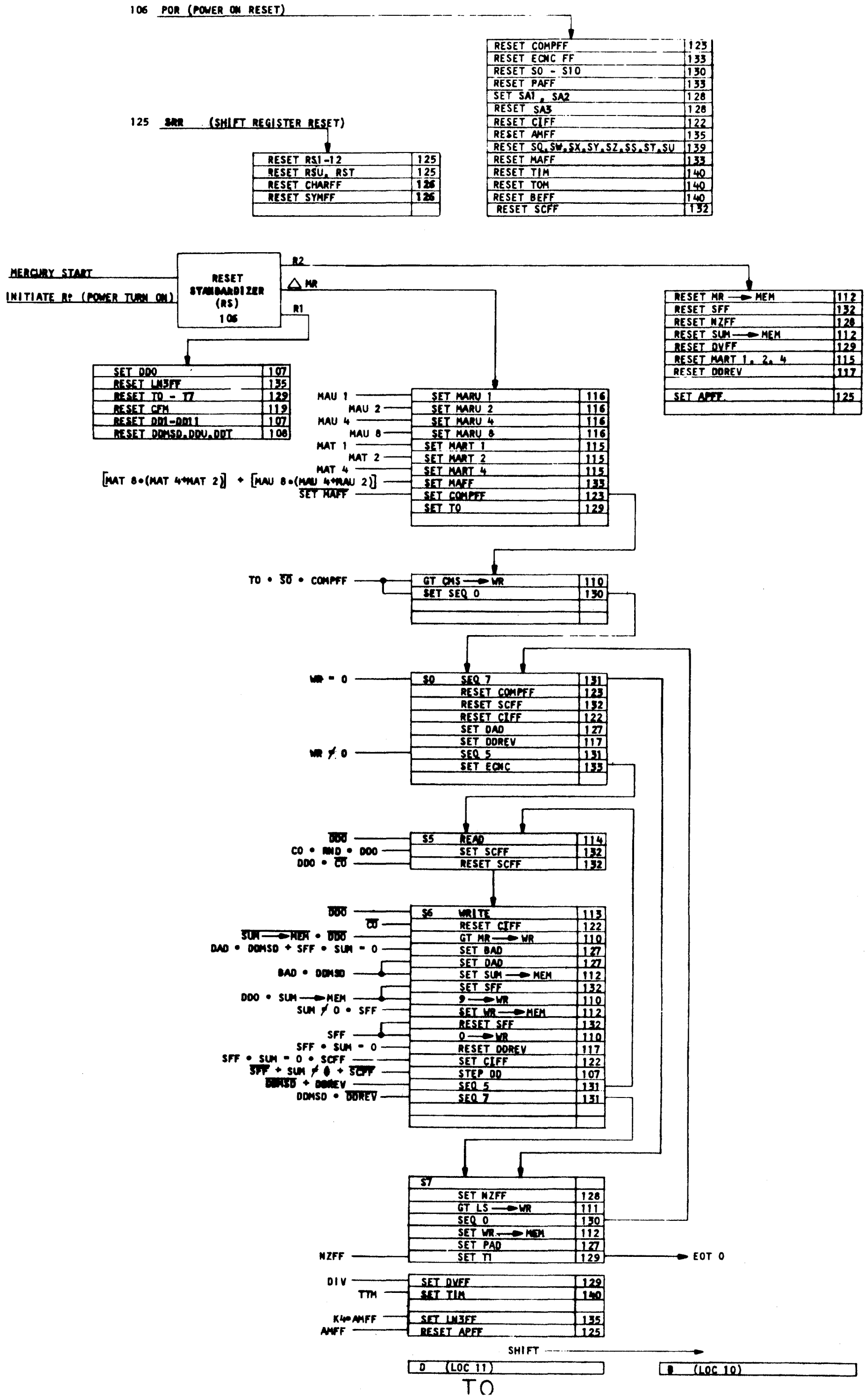
Reference pages 136, 137, & 138 not included



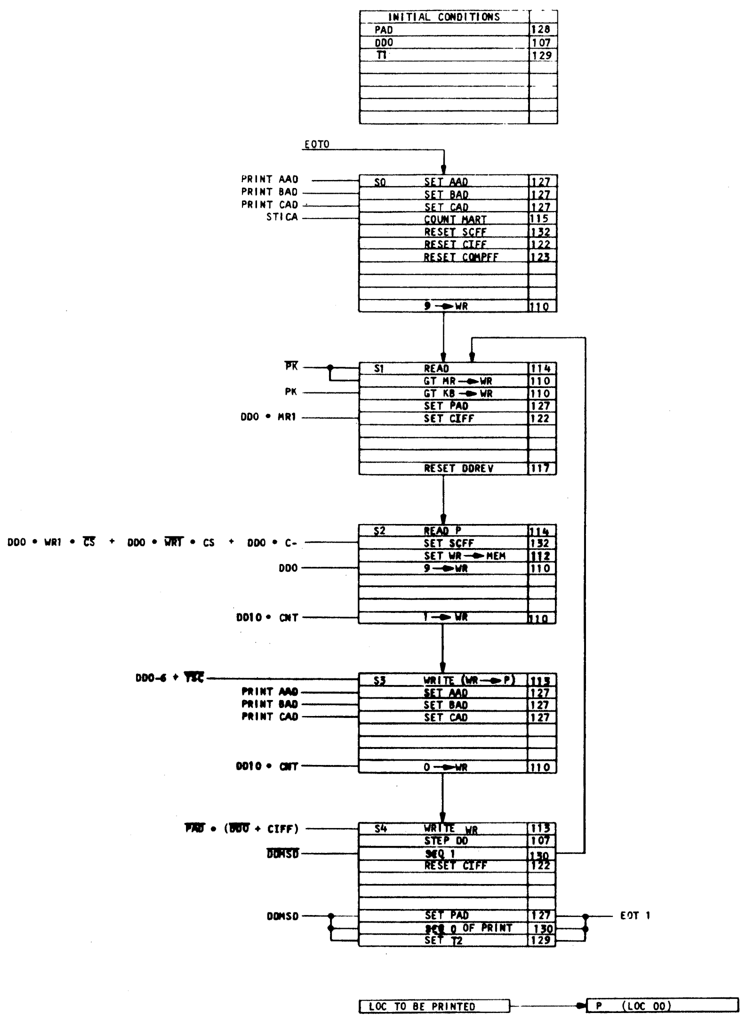
Ref. Page 139


P601
KBD LOCK SOL
TIM
TFM
TOMBB
TOM
MAFF RESET
LOCK
BEFF
EOTOM
CRG MOVEMENT SOL
RET. LN1 SOL
RET. LN2 SOL
RET. LN3 SOL
VERT SPACE SOL
JUMPER TO SELECT
VERT SPACE WITH ANY
OR ALL CRG. RETURNS
TAB LN SOL
SLIDE 1 SOL
SLIDE 2 SOL
SLIDE 3 SOL
SLIDE 4 SOL
SLIDE 5 SOL
SLIDE 6 SOL
SLIDE 7 SOL
(BLOCK SLIDE)
SHIFT SLIDE SOL
P603

Ref. Page 140

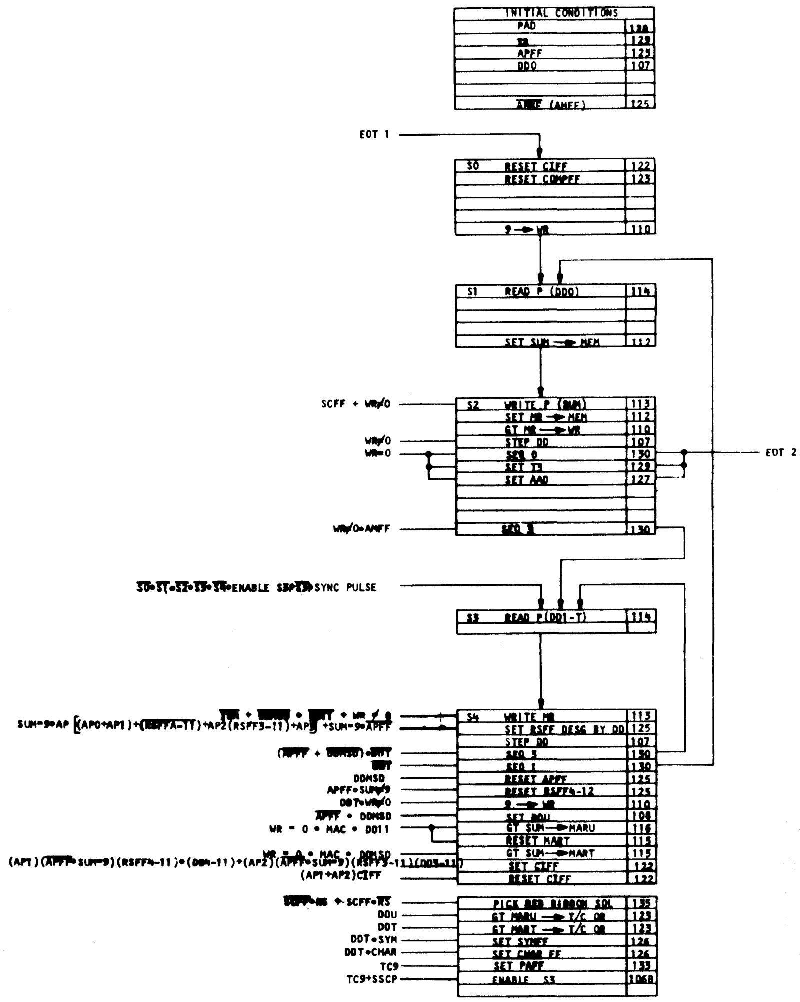

106 POR (POWER ON RESET)
125 SRR (SHIFT REGISTER RESET)
MERCURY START
INITIATE Rt (POWER TURN ON)
RESET STANDARDIZER (RS) 106
EOT 0
SHIFT
(LOC 11)
(LOC 10)
TO

Ref. Page 141



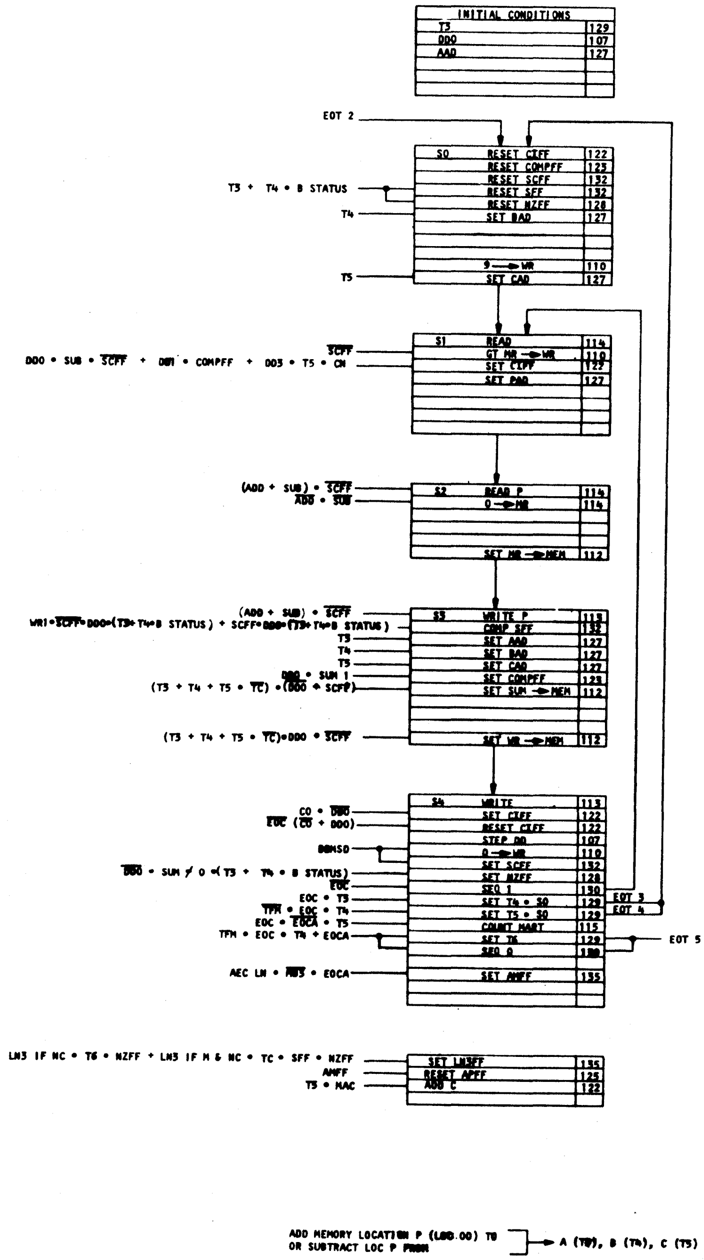
T1

Ref. Page 142



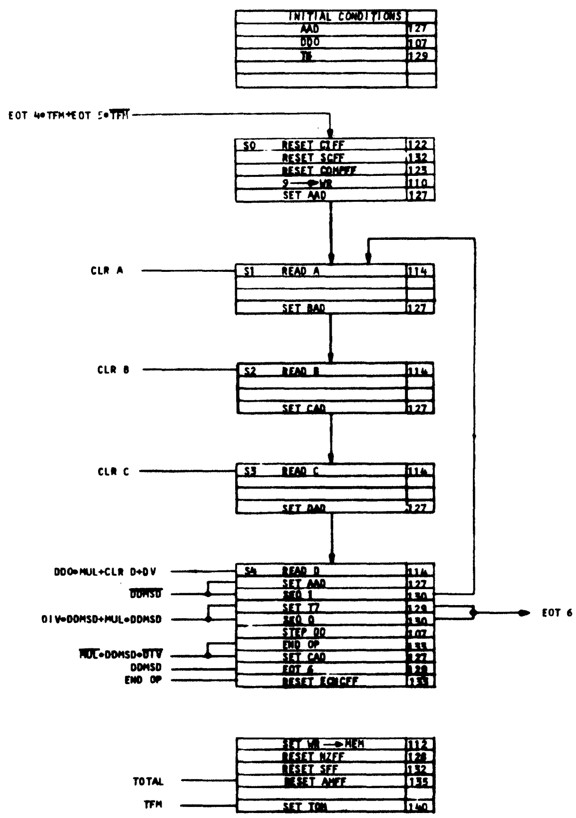
T2 PRINT P (LOC 00)

Ref. Page 143



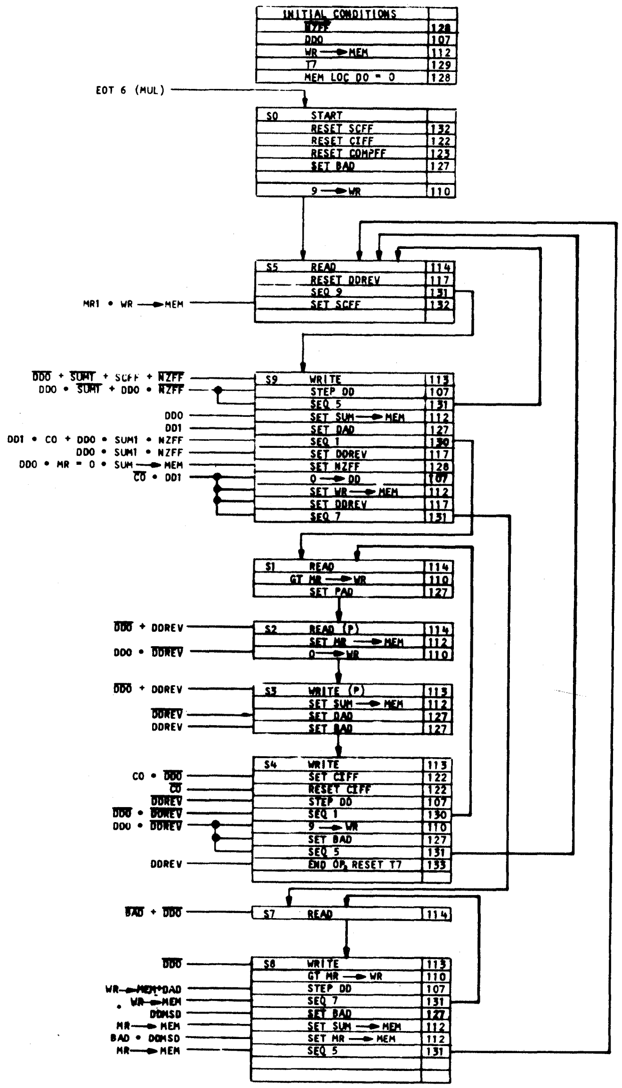
TX = T3 + T4 + T5

Ref. Page 144



T6 CLEAR A, B, C, D

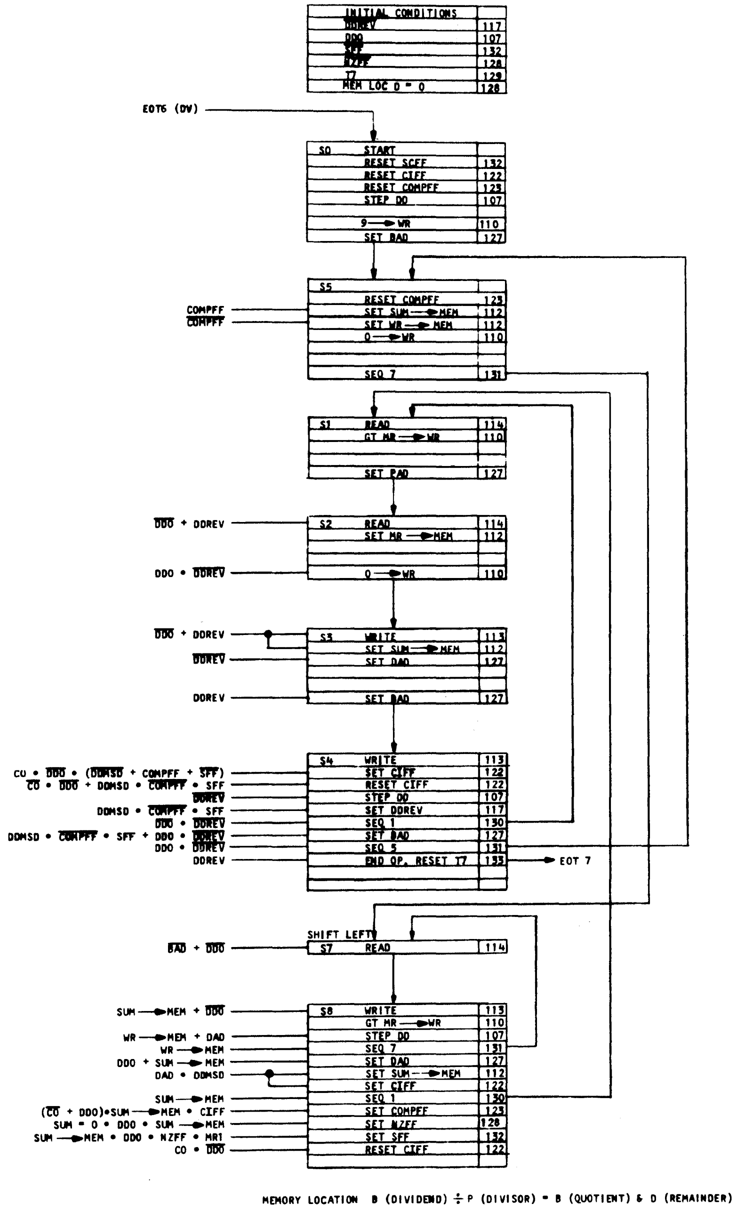
Ref. Page 145



MEMORY LOCATION P(MULTIPLICAND) X B(MULTIPLIER) = D(MAJOR PRODUCT) & B(MINOR PRODUCT)

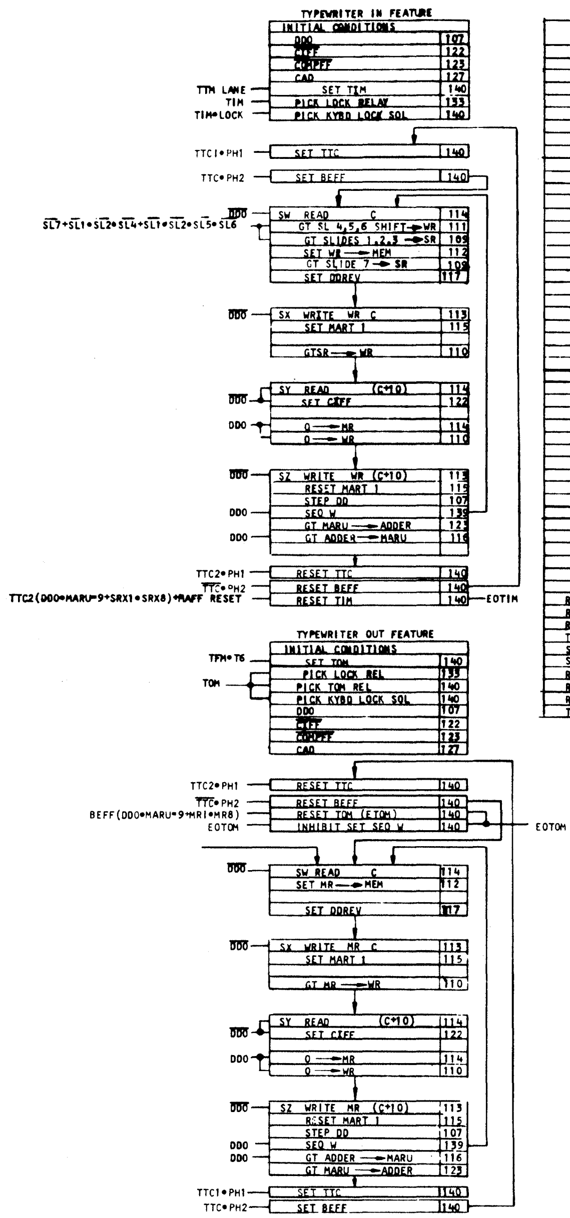
T7 MULTIPLY

Ref. Page 146



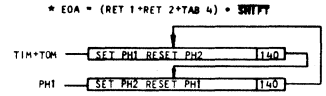
T7 DIVIDE

Ref. Page 147



CHAR	MEM LOC / REG / SLIDE / MEM	ODD TENS SR 7 / 8	ODD TENS IN→MR 1 / 4	ODD TENS IN→MR 2 / 2	ODD TENS OUT 3 / 1	EVEN TENS WR / 8	EVEN TENS WR 4 / 4	EVEN TENS WR 5 / 2	EVEN TENS WR 6 / 1
A		0	0	1	0	0	0	0	1
B		0	0	1	0	0	0	1	0
C		0	1	1	0	0	0	0	0
D		0	0	1	0	0	1	0	0
E		0	0	1	0	0	1	0	1
F		0	0	1	0	0	1	1	0
G		0	0	1	0	0	1	1	1
H		0	1	1	1	0	0	1	0
I		0	1	1	1	0	1	1	0
J		0	0	0	1	0	0	0	1
K		0	0	0	1	0	0	1	0
L		0	1	1	0	0	1	0	0
M		0	0	0	1	0	1	0	0
N		0	0	0	1	0	1	0	1
O		0	0	0	1	0	1	1	0
P		0	0	0	1	0	1	1	1
Q		0	1	1	1	0	1	0	0
R		0	1	1	1	0	1	0	1
S		0	1	0	0	0	0	1	0
T		0	1	1	0	0	0	0	1
U		0	1	0	0	0	1	0	0
V		0	1	0	0	0	1	0	1
W		0	1	0	0	0	1	1	0
X		0	1	0	0	0	1	1	1
Y		0	1	1	1	0	0	0	0
Z		0	1	1	1	0	1	1	1
1		0	0	0	0	0	0	0	1
2		0	0	0	0	0	0	1	0
3		0	1	1	0	0	0	1	1
4		0	0	0	0	0	1	0	0
5		0	0	0	0	0	1	0	1
6		0	0	0	0	0	1	1	0
7		0	0	0	0	0	1	1	1
8		0	0	1	0	0	0	0	0
9		0	1	1	1	0	0	[illegible]	1
0		0	1	0	0	0	[illegible]	[illegible]	0
@		0	0	0	0	0	0	[illegible]	[illegible]
-		0	0	0	1	0	0	0	[illegible]
:		0	1	1	0	0	1	0	1
.		0	1	1	0	0	1	1	0
,		0	1	1	0	0	1	1	1
/		0	1	0	0	0	0	0	1
RET 1 • $\overline{\text{SHIFT}}$	*	1	0	0	1	0	0	0	1
RET 2 • $\overline{\text{SHIFT}}$	*	1	0	0	1	0	0	1	0
RET 3 • $\overline{\text{SHIFT}}$		1	0	0	0	0	0	1	1
TAB 4 • $\overline{\text{SHIFT}}$	*	1	0	0	1	0	1	0	0
SPACE		1	0	0	0	0	0	0	0
SHIFT						1			
RET 1 • SHIFT		1	0	0	0	0	0	0	1
RET 2 • SHIFT		1	0	0	0	0	0	1	0
RET 3 • SHIFT		1	0	0	0	0	0	1	1
TAB 4 • SHIFT		1	0	0	0	0	1	0	0

* EOA = (RET 1+RET 2+TAB 4) • $\overline{\text{SHIFT}}$



TYPEWRITER MAGAZINE
1 = SLIDE INDEXED
0 = SLIDE BLOCKED

SLIDE 123 \ SLIDE 456	111	110	101	100	011 010	001	000
000	7	6	5	4	2	1	@
001	P	O	N	M	K	J	-
011 010	G	F	E	D	B	A	8
101 100	X	W	V	U	S	/	ZERO
110	,	.	;	L	3	T	C
111	Z	I	R	Q	H	9	Y

TTM - SLIDE SWITCHES → WR → MEMORY LOCATIONS WITH EVEN TENS DIGIT
→ SRX → WR → MEMORY LOCATIONS WITH ODD TENS DIGIT

TFM - MEMORY LOCATIONS WITH EVEN TENS DIGIT → MR → WR
MEMORY LOCATIONS WITH ODD TENS DIGIT → MR
→ TYPEWRITER CARRIAGE CONTROL AND SLIDE BLOCKING SOLENOIDS

Ref. Page 148

CARD LOC	CARD	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	FEATURE	TIE POINTS PIN/PAGE					
A1A	RSD		125	125	125	125															12/125	13/102				
A1B	—	135	140	PINS USED FOR LANE AND VERT SPACE-CRG RETURN SELECTION																						
A1C	RSD	125	125	125	125	125																				
A1D	RW	140	140	140	140	109	109	135	135	135	109	135	109	135												
A2A	RW	132	111	119	135	129	114	111	111	111	111	111	111	133												
A2B	SW	109	109	109	109	109	109	109	109	109	111	111	106A	115	127	127	127	135	111							
A2C	DSC	109	109	109	109	109	109	109	109	109	109	109	109													
A2D	RW	111	126	126	126	126	126	133	126	126	126	126	126	126												
A3A	RW	135	114	114	132	122	132	133	114	114	135	132	135	130												
A3B	RW	122	122	122	122	122	122	135	122	122	122	135	122	125												
A3C	RW	133	134	134	133	112	133	135	135	133	130	135	135	110												
A3D	PC	130																								
A4A	WE	115																								
A4B	WE	116																								
A4C																										
A4D																										
A5A																										
A5B																										
A5C																										
A5D																										
A6A																										
A6B																										
A6C																										
A6D																										
A7A																										
A7B																										
A7C	SD	135	135	133																						
A7D	SD	133	135	135	133																					
A8A	SD	140	140	140	140															(T)						
A8B	SD	140	140	140																(T)						
A8C	SD	140	140	140	140															(T)						
A8D	SD	140	140	140	140															(T)	1/120					
B1A	RSD	125	125	125	126	126																				
B1B	FFS	125	125																							
B1C	FFS	125	125																							
B1D	FFS	125	125																							
B2A	FFS	125	125																							
B2B	A	135	130	125	125	125	135	125																		
B2C	B	107	125	125	125	125	135																			
B2D	DC	104		104	103	103	103		103																	
B3A	FFS	125	119																		14/133					
B3B	F	109	133	133	126																					
B3C	F	109	133	115	126																					
B3D	B	126	133	133	133	133	133																			
B4A	D	126	135	133																						
B4B	FFS	135	133																							
B4C	FFS		140																	(T)						
B4D	SSCP	106B																		SEE NOTE 1, PAGE 106B						
	SSC	106B																		SEE NOTE 2, PAGE 106B						
B5A	B	130	106B	106B	106B	106B	106B													SEE NOTE 2, PAGE 106B				5/106B		
B5B																										
B5C																										
B5D																										
B6A																										
B6B	DC	104	104	104	103	103	103	134	103																	
B6C	E	109	113	139																(T)						
B6D	FFS	139	139																	(T)						
B7A	FFS	139	139																	(T)						
B7B																				(T)						
B7C	A	109	129	109	140	110	109	140												(T)						
B7D	FFS	140	140																	(T)						
B8A	FFS	140	140																	(T)						
B8B	A	112	140	140	110	133	140	140												(T)						
B8C	B	140	140	140	140	140														(T)						
B8D	A	112	140	140	140	140	140	140												(T)	7/104	4/106A				
C1A	RSD		125		125																10/102	28/105				
C1B	FFS	125	125																							
C1C	FFS	125	125																							
C1D	FFS	125	125																		1/111					28/135
C2A	FFS	126	126																			7/111		1/122	14/111	
C2B	A	135	135	135	135	135	135	135																		
C2C	A	109	140	140	140	111	140	111												(T)						
C2D	A	125	126	126	125	109	133	133														4/114				
C3A	B	135		131	112															(DV)	1/119	4/111				
C3B	A	132	132	127	128	128														(DV)						
C3C	C	111	111	111	111															(T)						
C3D	B	127	127	133	127	133	135														26/135					
C4A	D	133	135	127																	16/110					
C4B	FFS	133	115																		1/110					
C4C																										
C4D																										
C5A																										
C5B	A	109	110	122	114	114	129	140												(T)						
C5C	A	135	135	130	135	133	135	135																		
C5D	FFS	135	133																							
LOC	TYPE CARD	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	FEATURE	PIN/PAGE TIE POINTS					

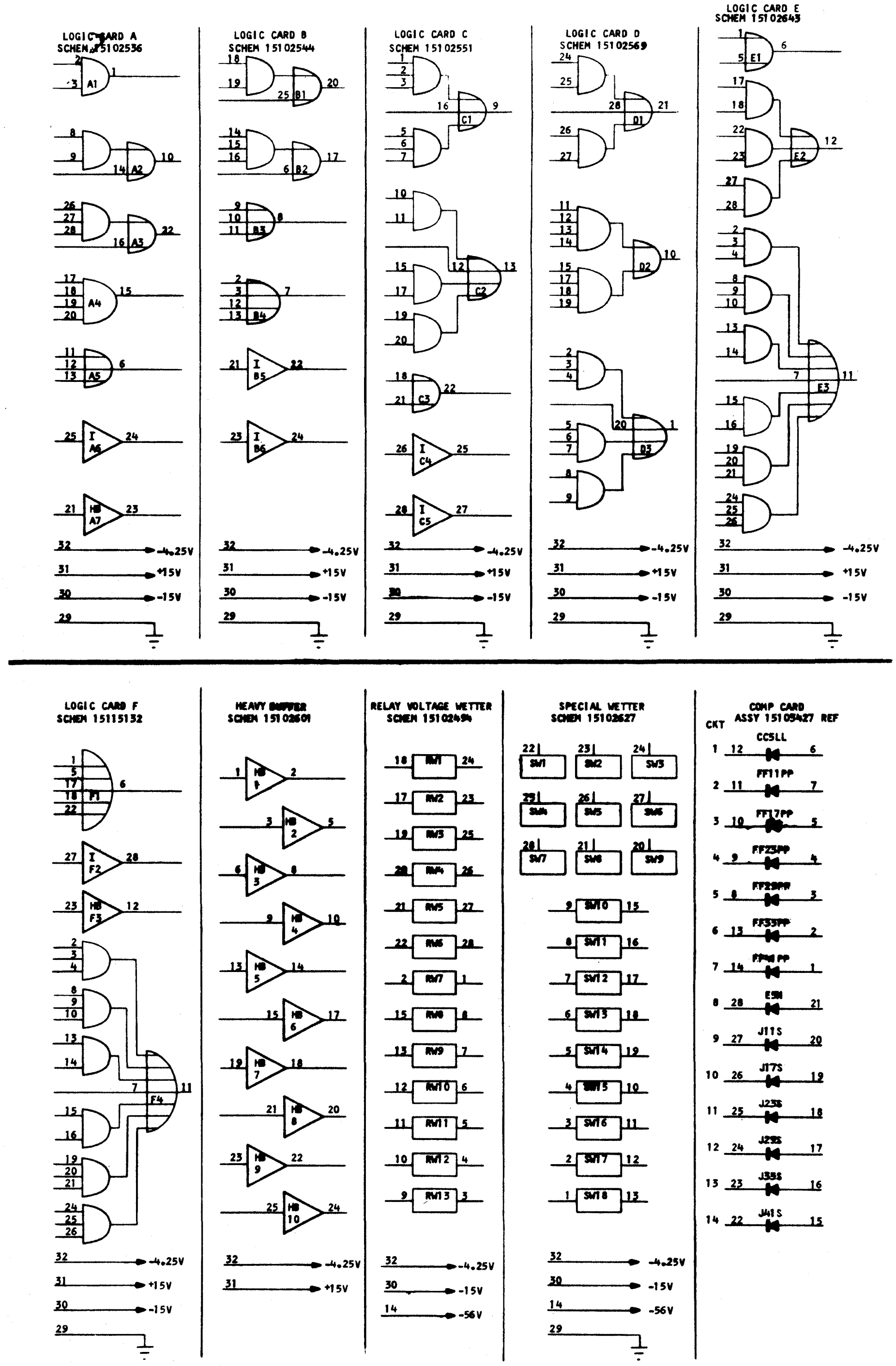
Ref. Page 149

CARD LOC	CARD TYPE	CIRCUIT/PAGE 1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	FEATURE	TIE POINTS PIN/PAGE					
C6A	A	135	133	130	130	133	132																			
C6B	A	116	107		121	133	107	115																		
C6C	D	140	140																	(T)						
C6D	HB	139	139	139	139	140	140	140	140	112	140									(T)						
C7A	C	115	134	115	134	115																				24/133
C7B	COMP	115	116	115	134	115	135	115		116		116	134	116	115											
C7C	HB	134	117	134	134	134	135	135	135	135	111													11/129	27/104	28/106A
C7D	FFS	134	134																		1/130	2/133	7/108	14/111	18/116	28/135
C8A	FFS	134	134																		1/111	2/102	7/102	14/130	18/115	28/107
C8B	FFS	134	134																		1/135	2/135	7/135	14/102	18/109	28/115
C8C	FFS	134	134																		1/133	2/135	7/135	14/106B	18/106B	28/128
C8D																										
D1A																										
D1B																										
D1C																										
D1D	A	126	132	135	128	128	107	135													7/125	5/102				
D2A	A	126	128	133	111	133	111	131													5/114					
D2B	F	109	132	131	132																					
D2C	E	128	112	127																						
D2D	DC	104	103	104	103	103	103		103																	
D3A	D	132	132	127																	23/114	16/119				
D3B	A	127	111	107	132	107	107	131													7/114		4/112			
D3C	A	115	132	122	115		135	135																		
D3D																										
D4A	E	107	133	107																						
D4B	C	133	107	128	110	133															4/135	23/135				
D4C	FFS	132	128																		1/122	2/122				
D4D	FFS	115																			14/106B	18/106B	7/116			
D5A	CLK	106B																			13/106B					
D5B	RS	106A																								
D5C	HB	107	128	107	107	116	108	115	108	107	133										4/122	7/122				
D5D	HB	108	107	108	108	108	108	108	108	107	107															
D6A	F	116	124	116	127																					
D6B	DC	104	103	104	103	103	103	103	103																	
D6C	FFS	116	116																		1/116	2/124	7/122	14/109	18/110	28/140
D6D	FFS	116	116																		1/111	2/110	7/109	14/131	18/123	28/109
D7A	FFS	128	107																		1/103	2/106B	7/106A	14/110	18/109	28/109
D7B	FFS	108	108																		1/135	2/129	7/106A	14/130	18/109	28/117
D7C	FFS	107	107																		1/106B	2/133	7/115	14/111	18/115	28/106A
D7D	FFS	107	107																		1/131	2/121	7/133	14/107	18/123	28/111
D8A	FFS	108	107																		1/109	2/109	7/111	14/112	18/110	28/114
D8B	FFS	108	108																		1/107	2/110	7/111	14/129	18/109	28/130
D8C	FFS	108	108																		1/109	2/111	7/115	14/109	18/133	28/113
D8D	FFS	108	108																		1/111	2/111	7/106A	14/106A	18/106A	28/128
																					2/106A	10/106A	11/106A	12/102	13/106B	14/106B
E1A	IND	131	131	112	112	133															15/107	17/125	18/102	19/102		21/106A
E1B	FFS	130	130																		1/122	2/122	7/106A	14/106A	21/106B	28/103
E1C	FFS	130	130																			2/129				
E1D																										
E2A	B	125	125	125	125	125	125													AP1,AP2	4/125	5/125	26/125	27/125	28/130	
E2B	E		125	125																AP1,AP2						
E2C	E	114	113	127																						
E2D	F	110	111	111	111																					
E3A	F	110	111	111	111																					
E3B	F	110	111	111	111																					
E3C	F	110	111	111	111																					
E3D																										
E4A	FFS	109	109																		1/122	2/122		7/128	18/129	
E4B	FFS	109	109																		1/129	2/127	7/130	14/130	18/129	28/115
E4C	D	132	107	109																		22/129				
E4D	C	116	117	109																						
E5A																										
E5B	C	115	115	115	116	109															8/112	4/112	14/115			
E5C	B	110	108	133	129	109	109															4/114				
E5D	FFS	115	115																		1/122	2/122	7/117		18/115	
E6A																										
E6B																										
E6C	FFS	128	128																		14/113					
E6D	C	109	117	118	116	116																				
E7A	D	116	119	110																	23/106B					
E7B	D	116	119	109																						
E7C	B	128	128	118	117	128	109																			
E7D	A	128		119	119	117	128	109																		
E8A	B		119	117	117	135	115														26/130	28/104	1/106A	4/106A		
E8B																										
E8C	A	119	118	118	118	134														(1M)	4/106A	7/106B				
E8D																										
F1A	IND	130	130	130	130	130	131	131	131												12/106B	13/106B	15/103			28/104
F1B	FFS	130	131																							
F1C	FFS	131	129																							
F1D	HB	129	129	129	129	129	129	129	129	111	111										7/106A					
F2A	A	110	130	112	128	128	107	110														7/115				
F2B	A	135	135	115	122	115	113	106A													4/132					
F2C	D	116	110	112																						
F2D	DC	104		104	103	103	103		103																	
F3A	FFS	111	111																		1/113		7/131	2/130		
F3B	FFS	111	111																				7/113	4/115		
LOC	TYPE	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	FEATURE	PIN/PAGE					
CARD		CIRCUIT/P																			TIE POINTS					

Ref. Page 150

CARD LOC	TYPE	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	FEATURE	TIE POINT PIN/PAGE					
F3C	F	128	110	130	122																					
F3D	A	135	112	135	112	112	112	121													4/129		7/122			
F4A	A	119	110	110	110	119	110	133															7/115			
F4B	D	116	119	112																						
F4C	FFS	117	132																		2/112	7/122	14/122			
F4D	FFS	123	122																		7/122	14/122				
F5A																										
F5B	C	132	120	118	120	128															8/107	4/114				
F5C	C	110	120	118	120	128															4/121	23/130				
F5D	C	117	120	118	120	128															4/122	8/[illegible]13				
F6A	C	117	120	118	120	11[illegible]															8/114					
F6B	DC	104		104	103	103	103		103																	
F6C	MD	119	118	119	118																14/113					
F6D	MD	117	117	117	117																					
F7A	MD	119	119	119	119																					
F7B	MD	119	118	119	118																	9/106A				
F7C	MD	118	118	118	118																					
F7D	MD	118	118	118	118															(1M)						
F8A	MD	118	118	118	118															(1M)						
F8B	MEM	121																								
F8C																										
F8D																										
G1A	IND	111	111	111	111	128	128	128																		28/105
G1B	FFS	131	131																							
G1C	FFS	131	131																							
G1D	FFS	129	129																							
G2A	F	112	124	130	129																					
G2B	F	117	124	130	130																					
G2C	C	110	123	127	122	122																				
G2D	A	110	132	132	132	122	122	130																		
G3A	A	117	122	122	110	122														(DV)						
G3B	A	110	117	117	110	117	129	131																		
G3C	FFS	112	112																							
G3D																										
G4A	D	114	110	122																	23/107					
G4B	A	112	123	123	122	129	122													(DV)						
G4C	B	112	119	124	117	124	124																			
G4D	C	117	124	114	124	124																				
G5A																										
G5B	B	115	119	123	123	122	122																			
G5C	A	120	124	119	123	124	124	112																		
G5D	A	113	117	113	123	123	124	117																		
G6A	F	114	114	128	114																					
G6B	F	117	114	121	123																					
G6C	MD	119	119	119	119																					
G6D	MD	119	119	119	119																					
G7A	MD	119	118	119	118																					
G7B	MD	117	117	117	117																					
G7C	MD	118	118	118	118																					
G7D	MD	120	120	120	120																					
G8A	MD	119		119																(1M)						
G8B	MEM	121																								
G8C																										
G8D																										
H1A	IND	107	107	108	108	129	129	129	122																	
H1B	FFS	129	129																							
H1C	FFS	129	129																							
H1D	FFS	129	129																							
H2A	F	112	124	130	114																					
H2B	D	123	115	122																						
H2C	A	117	131	131	130	113	130	131																		
H2D	DC	104		104	103	103	103		103																	
H3A	D	113	130	131																						
H3B	E	114	113	131																						
H3C	A	114	114	112	113	130	131	129																		
H3D	A	112	112	122	122	112	114	112																		
H4A	D	124	115	130																						
H4B	D	124	112	130																						
H4C	C	124	124	112	124	124																				
H4D	C	124	124	122	124	124																				
H5A	C	124	124	112	124	124																				
H5B	C	122	124	114	124	124																				
H5C	D	124	122	122																						
H5D	C	117	123	122	124	124																				
H6A	B	112	114	124	122	124	124																			
H6B	DC	104		104	103	103	103		103																	
H6C	F	113	113	113	113																					
H6D	B	123	114	124	124	114	113																			
H7A	MTA	114																								
H7B	MTB	114																								
H7C	MR	121																								
H7D	MR	121																								
H8A	MR	121																								
H8B	MR	121																								
H8C																										
H8D																										
LOC CARD	TYPE	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	FEATURE	PIN/PAGE TIE POINTS					

Ref. Page 151


LOGIC CARD A
SCHEM 15102536
LOGIC CARD B
SCHEM 15102544
LOGIC CARD C
SCHEM 15102551
LOGIC CARD D
SCHEM 15102569
LOGIC CARD E
SCHEM 15102643
LOGIC CARD F
SCHEM 15115132
HEAVY BUFFER
SCHEM 15102601
RELAY VOLTAGE WETTER
SCHEM 15102494
SPECIAL WETTER
SCHEM 15102627
COMP CARD
ASSY 15105427 REF
CKT
-4.25V
+15V
-15V
-56V

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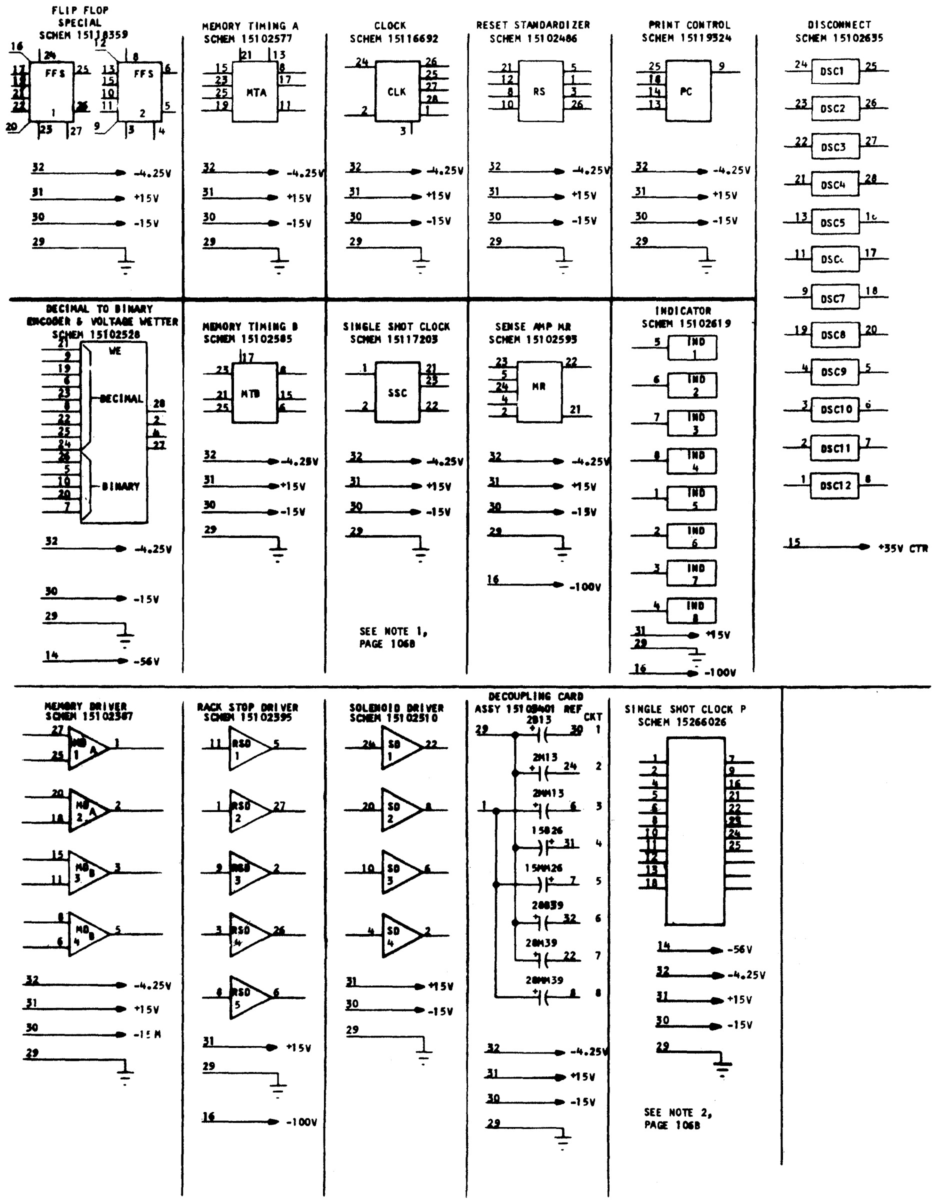
FLIP FLOP SPECIAL SCHEM 15118359
MEMORY TIMING A SCHEM 15102577
CLOCK SCHEM 15116692
RESET STANDARDIZER SCHEM 15102486
PRINT CONTROL SCHEM 15119524
DISCONNECT SCHEM 15102635
DECIMAL TO BINARY ENCODER & VOLTAGE WETTER SCHEM 15102528
MEMORY TIMING B SCHEM 15102585
SINGLE SHOT CLOCK SCHEM 15117203
SENSE AMP MR SCHEM 15102593
INDICATOR SCHEM 15102619
SEE NOTE 1, PAGE 106B
MEMORY DRIVER SCHEM 15102387
RACK STOP DRIVER SCHEM 15102395
SOLENOID DRIVER SCHEM 15102510
DECOUPLING CARD ASSY 15108401 REF
SINGLE SHOT CLOCK P SCHEM 15266026
SEE NOTE 2, PAGE 106B
+35V CTR

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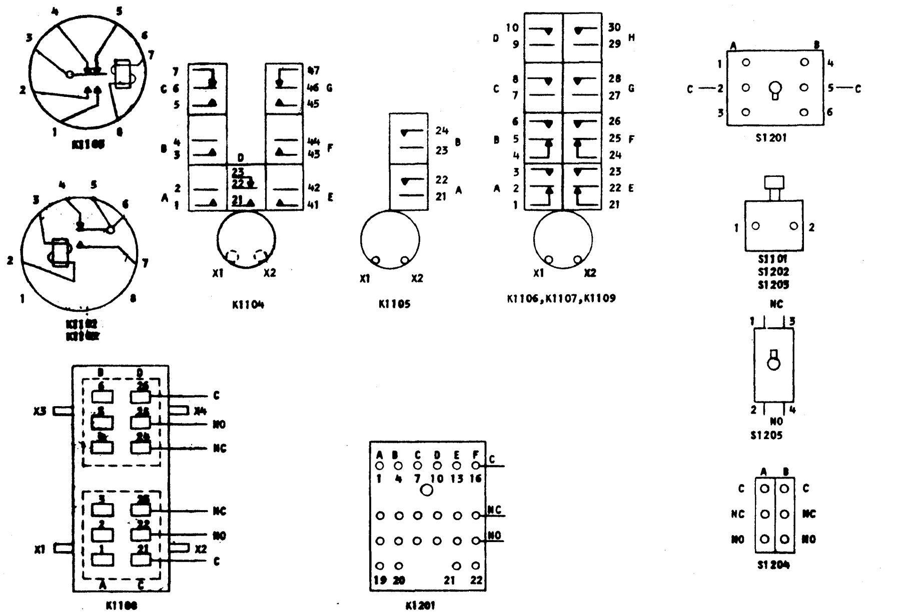

RELAYS	NAME	PAGE								
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K1104	POWER ON	101	102A-B		102A-B	102A-B	101	101	102A-B	
K1105	DELAY	102A-B	102A-B							
K1106	POR	102A-B	101	106A				106A		
K1107	CLOCK START	102A-B	102A-B	102A-B	101	102A-B	106B	106A		
K1108	LATCH, RELEASE	101,101		101						
K1201	MEMORY CLEAR	120	120	120	120	120	120	120		
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S1203	MR	102A-B
S1204A	SSC	106B
S1204B	SSC	106
S1205	POR	106
S1206	THERMOSTAT	102A-B
S1207	CLOCK MODE	106B

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R1103	102A-B	R1128	101	C1103	101	C1128	101	CR1103	101		
R1104	106A			C1104	101	C1129	101	CR1104	101		
R1105	106B			C1105	101			CR1105	101		
R1106	101			C1106	101			CR1106	101		
R1107	106A	R1201	120	C1107	101			CR1107	101		
[illegible]	103	R1202	120	C1108	101			CR1108	101		
[illegible]	101	R1203	120	C1109	101			CR1109	101		
R1110	101	R1204	120	C1110	101	C1201	120	CR1110	101	CR1201	120
R1111	101	R1205	120	C1111	101	C1202	104	CR1111	101	CR1202	102A-B
R1112	102A-B	R1206	120			C1203	120	CR1112	101	CR1203	120
R1113	102A-B	R1207	106A			C1204	120	CR1113	102A-B	CR1204	120
R1114	102A-B	R1208	106A			C1205	120	CR1114	101	CR1205	120
R1115	102A-B	R1209	106A			C1206	140	CR1115	101	CR1206	120
R1116	102A-B	R1210	120			C1207	140	CR1116	101		
R1117	101	R1211	120			C1208	135	CR1117	101		
R1118	101	R1212	104			C1209	135	CR1118	102A-B		
R1119	106A	R1213	106A			C1210	135	CR1119	102A-B		
R1120	101	R1214	120	C1120	102A-B			CR1120	101		
R1121	106A	R1215	106A	C1121	102A-B			CR1121	102A-B		
R1122	102A-B	R1216	140	C1122	101			CR1122	102A-B		
R1123	101	R1217	140	C1123	101			CR1123	106A		
R1124	101	R1218	135	C1124	102A-B						
R1125	103	R1219	135	C1125	102A-B			CR1125	102A-B		
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E1101	CHASSIS GRD	105
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E1103	CHASSIS GRD	105
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E1203	GRD DISTRIBUTION BUSS	105
E1204	+15V VOLTAGE DISTRIBUTION BUSS	103
E1205	-4.25V VOLTAGE DISTRIBUTION BUSS	103
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E1207	GRD DISTRIBUTION BUSS	105
E1208	SHIELD TERMINATION	303
E1209	SHIELD TERMINATION	303
E1210	SHIELD TERMINATION	105

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2	135	2	109	2	126	B	125	B	102	B		B	
3	135	3	109	3	102	C	125	C	105	C		C	
4	135	4	109	4	134	D	125	D	105	D		D	
5	135	5	109	5	133	E	125	E	102	E		E	
7	130	7	109	7	135	F	125	F	102	F		F	
8	134	8	109	8	135	H	125	H	104	H		H	
10	119	10	109	10		J	125	J	101	J		J	
11	125	11	109	11	126	K	125	K	101	K		K	
12	132	12	109	12	130	L	125	L		L	105	L	
13	141	13	109	13	105	M	125	M		M	105	M	
14	135	14	109	14	130	N	125	N		N		N	
15	122	15	115	15	104	P	125	P		P		P	
16	114	16	115	16	103	R	125	R		R		R	
17	114	17	115	17	140	S	126	S		S	105	S	
18	114	18	109	18	140	T	126	T		T		T	
20	114	20	109	20	140	U	105	U		U		U	
21	111	21	109	21	140	V		V		V		V	
22	111	22	109	22	140	W		W		W		W	101
23	135	23	109	23	140	X		X		X		X	101
24	133	24	109	24	140	Y		Y		Y		Y	
25	133	25	109	25	140	Z		Z		Z		Z	
26	126	26	109	26	140	a		a		a		a	
27	126	27	109	27	122	b		b		b		b	
28	132	28	115	28	135	c		c		c		c	
29	132	29	115	29	140	d		d		d		d	
30	114	30	115	30	140	e		e		e		e	
31	135	31	115	31	140	g		g		g		g	
32	122	32	115	32	140	h		h		h		h	
33	122	33	115	33	140	i		i	101	i		i	
34	127	34		34	133	j		j	101	j		j	
35		35		35	140	k		k		k		k	
36	133	36		36	135	m		m		m	105	m	
37	125	37		37	133	n		n	101	n	103	n	
38	140	38		38	133					p	102	p	
39	140	39		39	133					q		q	
40	115	40		40						r	101	r	102
41	115	41		41						s		s	
42	116	42		42						t		t	
43	115	43		43						u		u	
44	116	44		44						v		v	
45	115	45		45						w		w	
46	116	46		46	135					x	101	x	
47	122	47	126	47						y	102	y	
48	122	48	126	48						z		z	
49	127	49	126	49						AA		AA	
50	122	50	126	50						AB		AB	
51	122	51	126	51						AC		AC	105
52	127	52	126	52						AD		AD	
53	135	53	126	53						AE		AE	
54	135	54	116	54						AF		AF	
55	112	55	116	55	135					AH		AH	
56	122	56	116	56	135					AJ		AJ	
57	122	57	116	57						AK		AK	
58	132	58	116	58						AL		AL	
59	122	59	116	59						AM		AM	
60	129	60	116	60						AN		AN	
62	135	62	116	62						AP		AP	
63	111	63	116	63	135					AR		AR	
64	111	64		64	135					AS		AS	
65	115	65	111	65						AT		AT	
66	116	66	111	66						AU		AU	
67	115	67		67						AV		AV	
70	116	70	135	70	135					AW		AW	
71		71	135	71	135					AX		AX	
72		72		72						AY		AY	
73	140	73	135	73	135					AZ		AZ	103
74	140	74	135	74	135					BA		BA	101
75	109	75	135	75	135					BB		BB	105
76	109	76	135	76	135					BC		BC	
77	109	77	135	77	135					BD		BD	101
78	111	78		78	135					BE		BE	104
79	111	79		79	135					BF		BF	102
80	111	80		80	133					BH		BH	103
82	109	82		82						BJ		BJ	105
										BK		BK	
										BL		BL	101
										BM		BM	101

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* INDICATES SOURCE

SIGNAL INDEX - LOWER GATE, UPPER GATE

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304	ALIGN	*135	310	$\overline{\text{MARU 7}}$	*116	311	SRX8	*109
*319	ASRX SL	109						
320	BC	*135	310	$\overline{\text{MARU 8}}$	*116	312	$\overline{\text{SRX8}}$	*109
310	$\overline{\text{CIFF}}$	*122						
319	CLK A	*106B	310	MARU = 9	*116	*318	STEP DD SL	107
			315	$\overline{\text{MRT}}$	*121			
319	CLK C	*106B				321	SUM ≠ 9	*124
308	CLOCK START	*106B	319	POR	*106A	317	$\overline{\text{S0}}$	*130
			* 304	PROG CAMFF SL	106 A			
*313	COUNT MART SL	115	*312	$\overline{\text{P1XFF}}$ SL	109	317	$\overline{\text{ST}}$	*130
*304	CRG MOTORFF SL	106 A	*312	$\overline{\text{P2XFF}}$ SL	109	317	$\overline{\text{S3}}$	*130
*304	CRG MOTOR SL	102	319	R1	*106A	317	S10	*131
			307	RESET SL	106A	320	T3 •	*129
*309	DATA XFF SL	109	304	RL	*135	*320	TBFF SL	130
319	$\overline{\text{DDMSD}}$	*108	*317	SET MART 2, RESET MART 1	115	*320	$\overline{\text{TBFF}}$ SL	128
318	$\overline{\text{DDO}}$	*107	*317	RESET MART 4 SL	115	*320	TBFFBB SL	129
312	$\overline{\text{DDT}}$	*107	*318	RESET COMPFF SL	123	*319	TBFF • FFZ SL	115
						320	V	*135
			*318	RESET DDREV • SET WR → MEM • MARU CLK SL	116	*310	WLFF SL	117
318	$\overline{\text{EOC}}$	*133						
*320	EJFF SL	106A				*318	WRITE SL	113
*313	$\overline{\text{FFZ}}$ SL	111						
304	FLBB	*135	*320	RESET TBFF SL	133	315	WR1	*111
*318	GT KB → WR SL	110	*319	RLFFBB•SBBB SL	110			
*318	GT MR → WR SL	110	*317	SA SL	128	315	WR2	*111
			*317	SB SL	114	315	WR4	*111
*319	GT SRY1 → WR1 SL	111	*318	SET COMPFF SL	123	315	WR8	*111
*319	GT SRY2 → WR2 SL	111	*317	SET MART 4 SL	115	*318	0 → WR SL	110
*319	GT SRY4 → WR4 SL	111	*318	SET MR → MEM SL	112	*318	$\overline{\text{1 → WR}}$ SL	111
*319	GT SRY8 → WR8 SL	111	*318	SET S10 SL	131	*318	9 → WR SL	110
*319	GT WR → SRX SL	109				301	+15V	*103
			*319	SRX CLK SL	109	301	-4.25V	*103
304	$\overline{\text{LOCK}}$	*133	321	SRX1	*109	302	-15V	*104
310	LN51	*135						
*319	LU SL	133	321	$\overline{\text{SRX1}}$	*109	302	-56V	*102
310	$\overline{\text{MARU 1}}$	116	321	SRX2	*109	302	-100V	*102
310	$\overline{\text{MARU 2}}$	*116	321	$\overline{\text{SRX2}}$	*109	303	GRD	*105
320	LN53	*135	312	SRX4	*109	303	SW GRD	*105
			312	$\overline{\text{SRX4}}$	*109			

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1	101	1	103	A1	101	A1	106A	A1	101	1		1	101			A1	120	A1	120				
2	101	2	103	A2		A2	102A	A2	101	2		2	101			A2	120	A2	120				
3	101	3	104	A3	101	A3	102A	A3	101	3		3	105			A3	120	A3	120				
4	101	4	102A	A4		A4		A4	101	4	102A	4	R			A4	104	A4	120				
5	101	5	101	A5	101	A5		A5	102A	5		5	101			A5	120	A5	102A				
6	101	6	101	A6		A6		A6	101	6	105	6	103			A6	120	A6	104				
7	101	7	102A	A7	102A	A7	106B	A7	101	7	103	7	105			A7	120	A7	140				
8	103	8	102A	A8		A8		A8	101	8	103	8				A8	135	A8	140				
9	102A	9	105	A9	101	A9		A9	102A	9	104	9	102A			A9	120	A9	140				
10	102A	10	105	A10		A10		A10	102A	10	102A	10	102A			A10	135	A10	140				
11	102A	11	106A	A11	101	A11	102A	A11	102A	11	102A	11	102A			A11	120	A11	135				
12	105	12	102A	A12		A12	103	A12	102A	12	102A	12	R			A12	120	A12	135				
13	104	13	106A	A13	102A	A13	101	A13	106A	13	102A					A13	135	A13					
14	104	14	106B	A14		A14	101	A14		14	106B					A14	120	A14	106A				
15	101	15	106A	A15	101	A15	101	A15	102A	15						A15	135	A15	106A				
16	102A	16	103	A16	101	A16	102A	A16	101	16						A16	120	A16	106A				
17	103	17	102A	A17	102A	A17	102A	A17		17	101					A17	120	A17	106A				
18	101	18	106A	A18	102A	A18	102A	A18		18	101					A18	120	A18	106A				
19	102A	19	101	A19	101	A19		A19		19	101												
20	101	20	101	A20	106A	A20		A20		20	101												
				A21	106A	A21		A21															
				A22	106A	A22	101	A22															
				A23	N.A.	A23	102A	A23															
				A24	N.A.	A24	102A	A24															
				B1	101	B1	106A	B1	101							B1	120	B1	120				
				B2		B2	102A	B2	101							B2	120	B2	120				
				B3	101	B3	102A	B3	101							B3	120	B3	120				
				B4		B4		B4	101							B4	104	B4	120				
				B5	101	B5		B5	102A							B5	120	B5	102A				
				B6		B6		B6	101							B6	120	B6	104				
				B7	102A	B7	106B	B7	101							B7	120	B7	140				
				B8		B8		B8	101							B8	135	B8	140				
				B9	101	B9		B9	102A							B9	120	B9	140				
				B10		B10		B10	102A							B10	135	B10	140				
				B11	101	B11	102A	B11	102A							B11	120	B11	135				
				B12		B12	103	B12	102A							B12	120	B12	135				
				B13	102A	B13	101	B13	106A							B13	135	B13					
				B14		B14	101	B14								B14	120	B14	106A				
				B15	101	B15	101	B15	102A							B15	135	B15	106A				
				B16	101	B16	102A	B16	101							B16	120	B16	106A				
				B17	102A	B17	102A	B17								B17	120	B17	106A				
				B18	102A	B18	102A	B18								B18	120	B18	106A				
				B19	101	B19		B19															
				B20	106A	B20		B20															
				B21	106A	B21		B21															
				B22	106A	B22	101	B22															
				B23	N.A.	B23	102A	B23															
				B24	N.A.	B24	102A	B24															

R INDICATES RESERVED POINTS
N.A. INDICATES NOT AVAILIABLE

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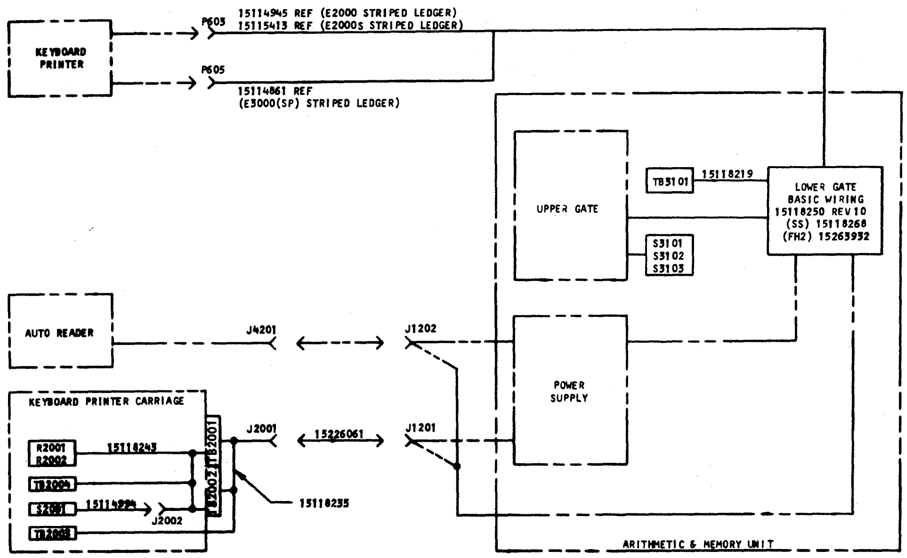


PAGE.	DESCRIPTION	ER DATE	REV
300	ARITHMETIC & MEMORY UNIT	3-11-66	J
301	VOLTAGE ROUTING +15V, -4.12V, -4.25V	7-16-65	E
302	VOLTAGE ROUTING -15V, -56V, -100V, -120V	10-23-65	G
303	GROUND ROUTING	12-29-65	H
304	ALIGNFF, SL, RL, CRG MOTOR SL, PROG CAM, ARP ON•FL, CRG LOCK SOL.	12-25-65	J
305	REVFF, TABFF, PDFF, STOP STORAGE FF	12-25-65	J
306	LF READ AMP, LF WRITE AMP, FF4, LWLFF, L-2FF, FF16	2-26-66	J
307	POFF, PTFF, CLFF, RESET SL, LC2	2-26-66	J
308	COUNTERS; SYNCFF, USMVFF	10-23-65	G
309	RLFF, DISCRIMINATOR XFF, DISCRIMINATOR YFF, COUNT XFF, COUNT YFF, DATA XFF, DATA YFF RLBFF	12-29-65	H
310	WLFF, MARU/0, CPFF, PWFF, 11FF, $\overline{\text{CTFF}}$	12-29-65	H
311	FF9X, FF9Y, FF1X, FF1Y, SRX8	12-29-65	H
312	P1XFF, P1YFF, P2XFF, P2YFF, $\overline{\text{DDT}}$	5-10-65	D
313	FF3X, FF3Y, FFZ, FF6, DP	12-29-65	H
314	SRCX1, SRCX2, SRCY1, SRCY2, SRCX=3, SRCX=0, SRCY=3, SRCY=0	5-10-65	D
315	SRY1, SRY2, SRY4, SRY8, WLFFBB•SCBB•DDO•$\overline{\text{FFZ}}$	5-10-65	D
316	READ AMP X, READ AMP Y, WRITE AMP X, WRITE AMP Y	12-25-65	J
317	SA; SB; SC; SET MART 4; RESET MART 4; SET MART 2, RESET MART 1	12-29-65	H
318	EOC, SET COMPFF SL, SET S10 SL, 9→WR SL, DDO, 0→WR SL, STEP DD SL, SET MR→MEM SL, RESET DDREV• SET WR→MEM•MARU CLK SL, GT KB→WR SL, GT MR→WR SL, WRITE SL	12-29-65	H

PAGE	DESCRIPTION	ER DATE	REV
319	LU SL, AR CONTROL, RLFFBB•SCBB, ASRX, WLFF+ RLFF, SRX CLK SL, GT WR→SRX SL, WLFFBB•SCBB• FFZBB, DDMSD, GT SRY→WR SL, CLK A CLK C, R1 POR	3-11-66	J
320	BCFF, VFF, TBFF, EJFF, BC, RLN•CC4, RESET TBFF	2-26-66	J
321	ERFF, SUM=9, CC	12-25-65	J
322	VER LAMP, READ LAMP, FS LAMP, WRT LAMP, CRG MOTOR & CRG SOLENOIDS	7-16-65	E
323	FPC, BOLP, CRG OPEN, CRG CAMS 1-6	12-29-65	H
324	INITIAL INSTALLATION LOGIC ONE/TWO DATA STRIPES	10-2-64	A
325	VERIFICATION LOGIC, ONE/TWO DATA STRIPES	10-2-64	A
326	WRITE LEDGER LOGIC ONE/TWO DATA STRIPES	11-16-64	A
327	READ LEDGER LOGIC ONE/TWO DATA STRIPES	7-16-65	E
328	TRIAL BALANCE & BLOCK TRANSFER(LANE 61)LOGIC ONE/TWO DATA STRIPES	7-16-65	E
329	CARD LOCATION CHART & TIE POINT CHART	3-11-66	J
330	CARD LOCATION CHART, TIE POINT CHART & COMPONENT CHART	12-25-65	J
331	CARD ELEMENTS & COMPONENTS	9-30-65	F
332	CARD ELEMENTS & COMPONENTS	10-2-64	A
333	CONNECTOR INDEX	10-23-65	G
334	TERMINAL BOARD INDEX	10-23-65	G

NOTES:

1. WIRING SHOWN IN DASHED LINES (— — — — — — —) INDICATES OPTIONAL FEATURES.
2. CHARACTERS IN PARENTHESIS ON WIRING INDICATES NAME OF OPTIONAL FEATURE REQUIRING WIRING.
3. CHARACTERS IN PARENTHESIS LOCATED NEAR CARD ELEMENT INDICATES OPTIONAL FEATURE REQUIRING THAT CARD.

*4. INSERT LOGIC CARD "A" INTO CARD SLOT C1B FOR 11 INCH LEDGER OR C1C FOR 14 INCH LEDGER.

5. EXCEPT FOR VOLTAGE AND FF ELEMENT PINS, ALL ELEMENT PINS ARE SHOWN. PINS 10, 15, 19 & 21, IF SHOWN ON FF ELEMENT, ARE CLOCK (A, B OR C) INPUTS. ALL OTHER ELEMENT PINS SHOWN WITHOUT SIGNAL ARE NOT WIRED.
6. WIRING SHOWN IN PHANTOM LINES (——— — — ———) FOR REF ONLY.
7. PAGE NUMBERS ON INPUT SIGNALS INDICATE PAGE OF ORIGIN.
8. PAGES 100 THRU 299 DESIGNATE A & M UPPER GATE SCHEMATIC.
9. PAGES 300 THRU 349 DESIGNATE A & M LOWER GATE SCHEMATIC 15118300.
10. PAGES 350 THRU 358 DESIGNATE AUTO READER SCHEMATIC 15227440.
11. PAGES 500 THRU 549 DESIGNATE KEYBOARD PRINTER SCHEMATIC.
12. WHEN PAGE NUMBER DOES NOT APPEAR ON INPUT OR OUTPUT, REFER TO SIGNAL INDEX CHART ON APPLICABLE UPPER GATE SCHEMATIC TO DETERMINE WHERE SIGNALS ENTER OR LEAVE.
13. P605 REPLACES P603 FOR SUPPLEMENTARY PROGRAMMING MACHINES (SP), SERIES E3000
14. LOGIC CARD "CW" REPLACES LOGIC CARD "RW" FOR SUPPLEMENTARY PROGRAMMING MACHINES (SP), SERIES E3000

UNLESS OTHERWISE SPECIFIED:
ALL CAPACITORS ARE 5UF, 25 WVDC
ALL DIODES ARE BCX58-1
ALL RESISTANCES ARE IN OHMS

OPTIONAL FEATURES
ABBREVIATIONS

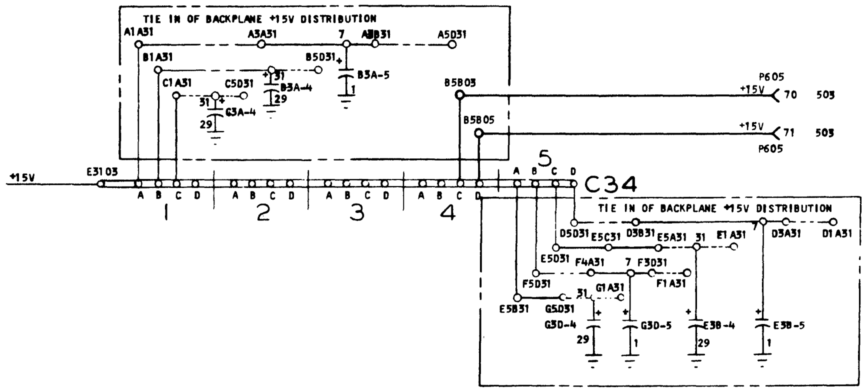
(SS) SINGLE STRIPE

(DS) DUAL STRIPE

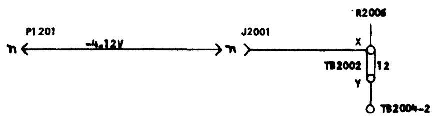
(AR) AUTO READER

(FH2) FORM HEADING ALIGNMENT, STYLE 2

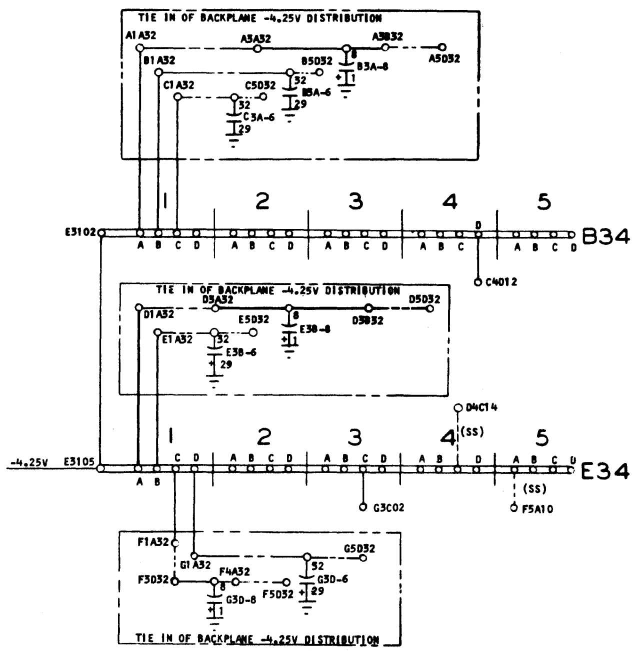
+15V



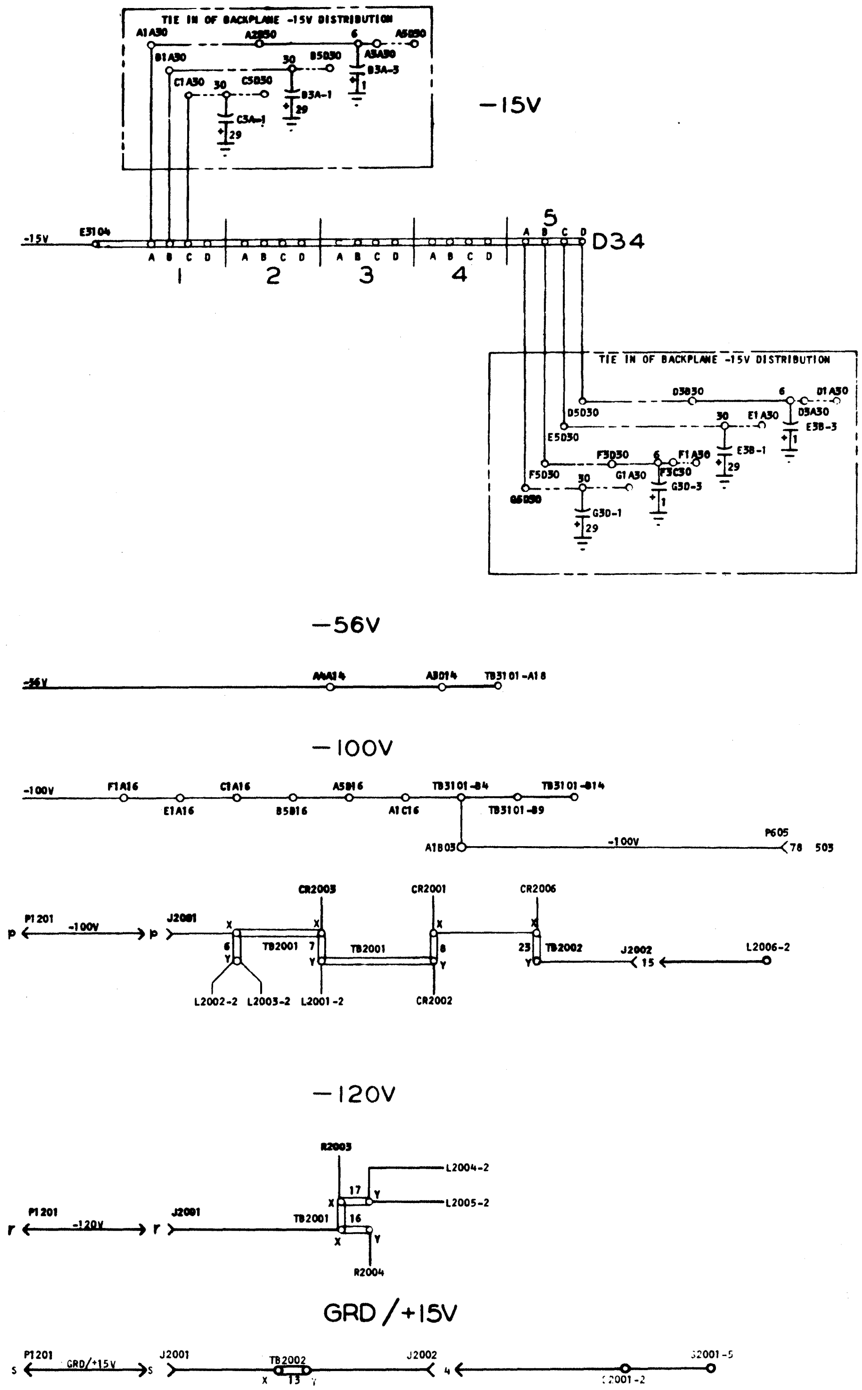
−4.12V



−4.25V

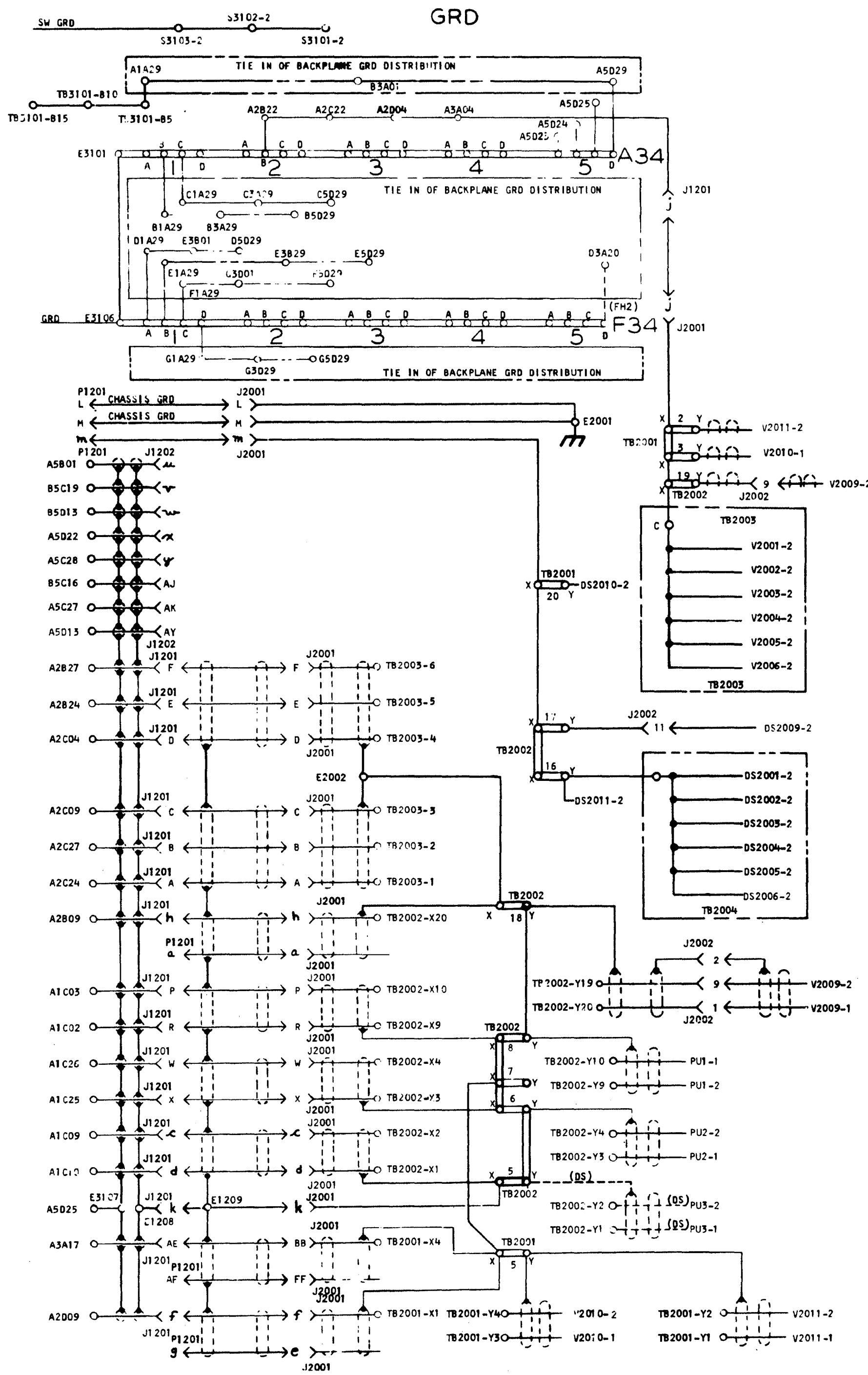


Ref. Page 301

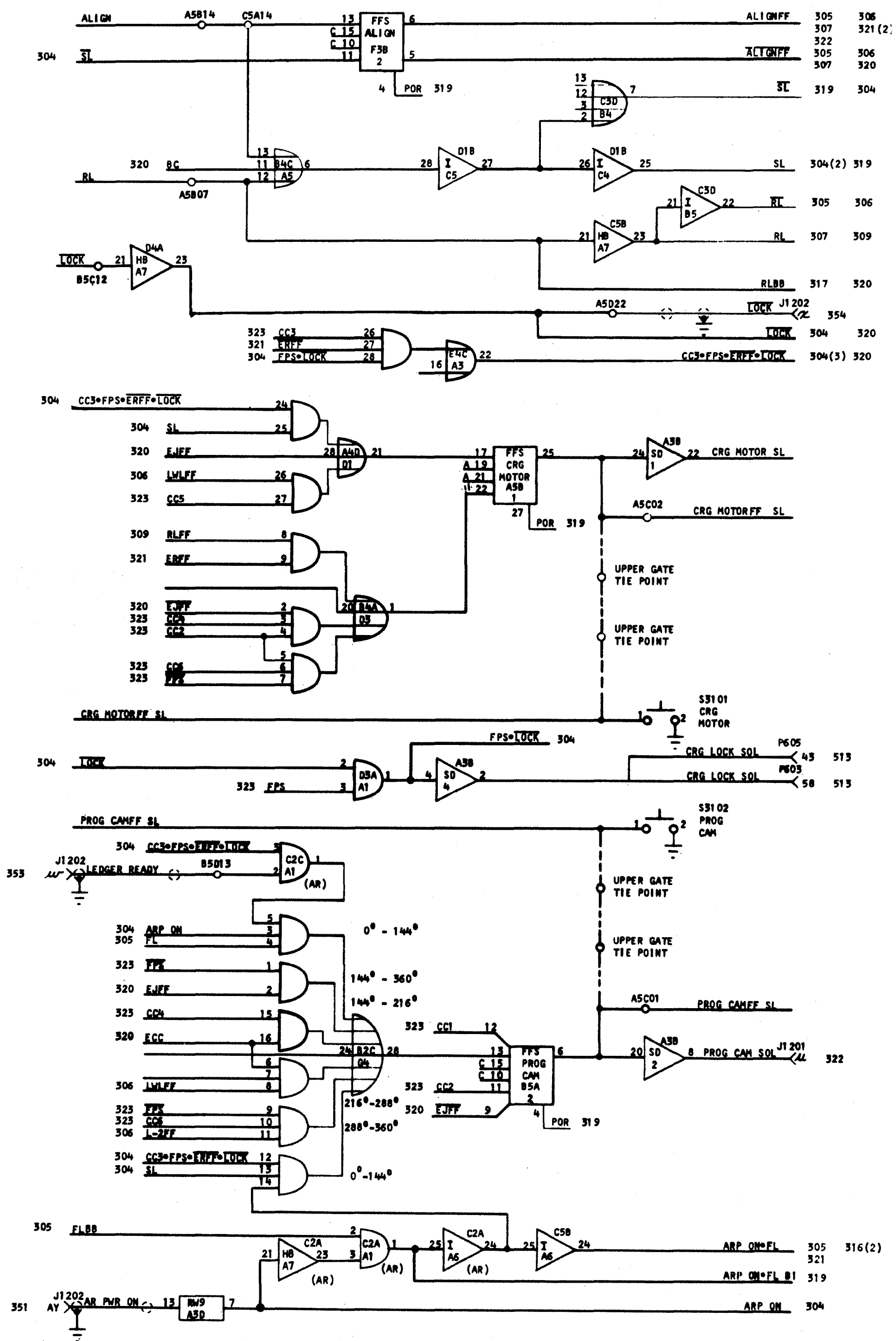


TIE IN OF BACKPLANE -15V DISTRIBUTION
−15V
D34
TIE IN OF BACKPLANE -15V DISTRIBUTION
−56V
−100V
−120V
GRD / +15V

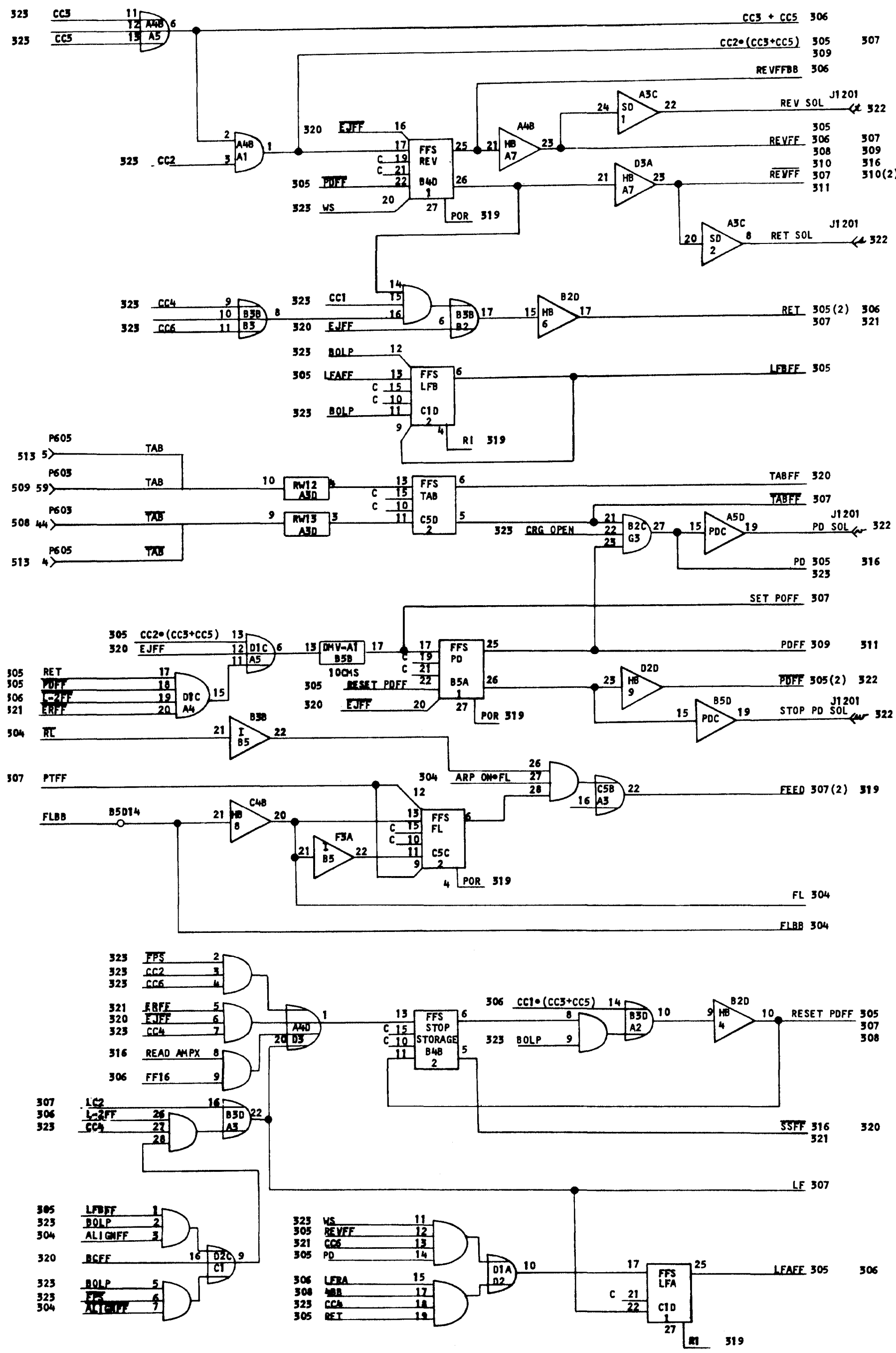
Ref. Page 302


GRD
SW GRD
S3102-2
S3103-2
S3101-2
TIE IN OF BACKPLANE GRD DISTRIBUTION
A1A29
A5D29
B3A01
TB3101-B10
TB3101-B15
TB3101-B5
A5D25
A2B22
A2C22
A2D04
A3A04
E3101
A34
J1201
J2001
F34
GRD E3106
E2001
CHASSIS GRD
TB2001
TB2002
TB2003
TB2004
J2002
V2011-2
V2010-1
V2009-2
V2009-1
DS2010-2
DS2009-2
DS2011-2
PU1-1
PU1-2
PU2-2
PU2-1
PU3-2
PU3-1
V2011-1
V2010-2

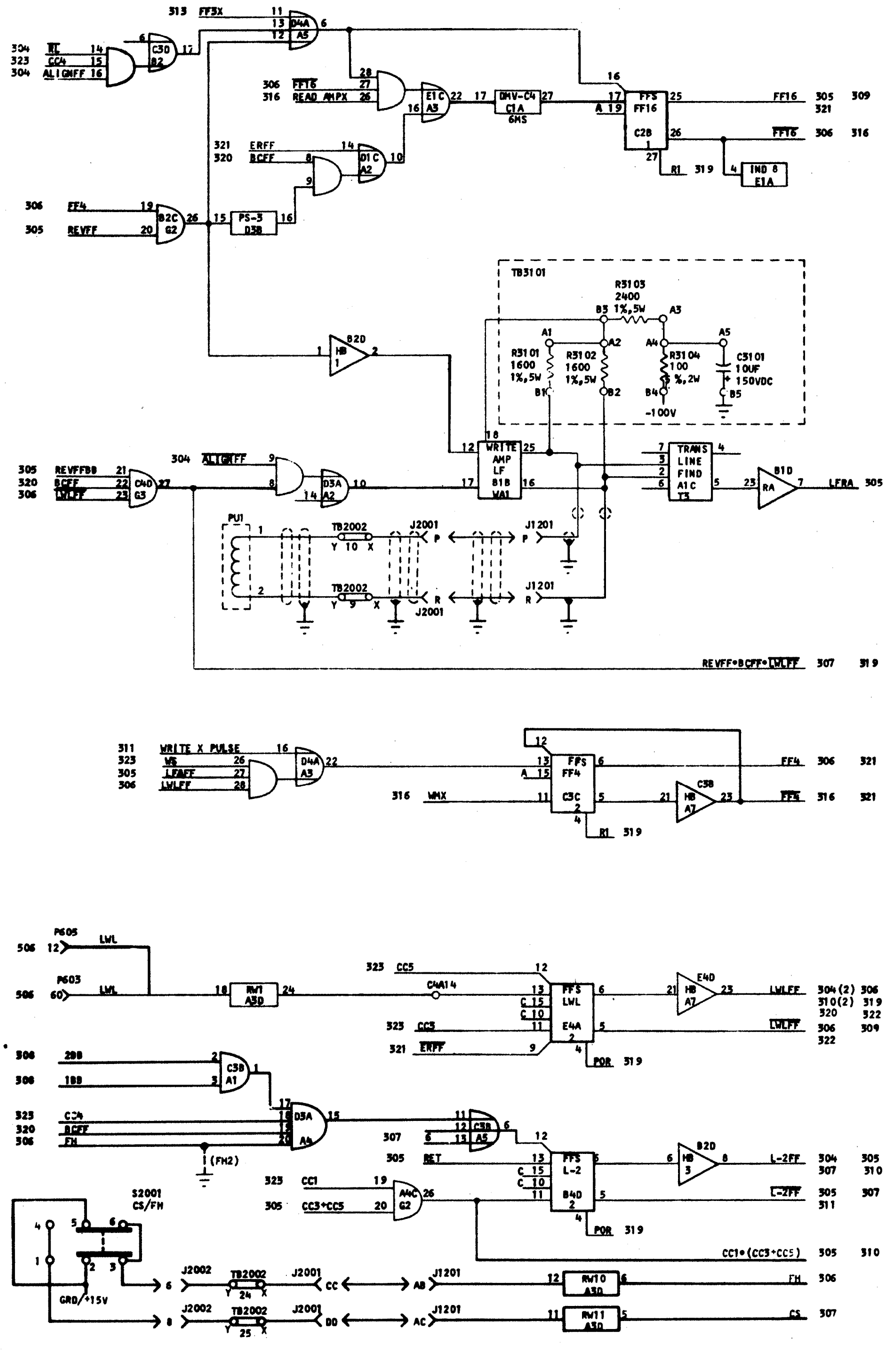
Ref. Page 303

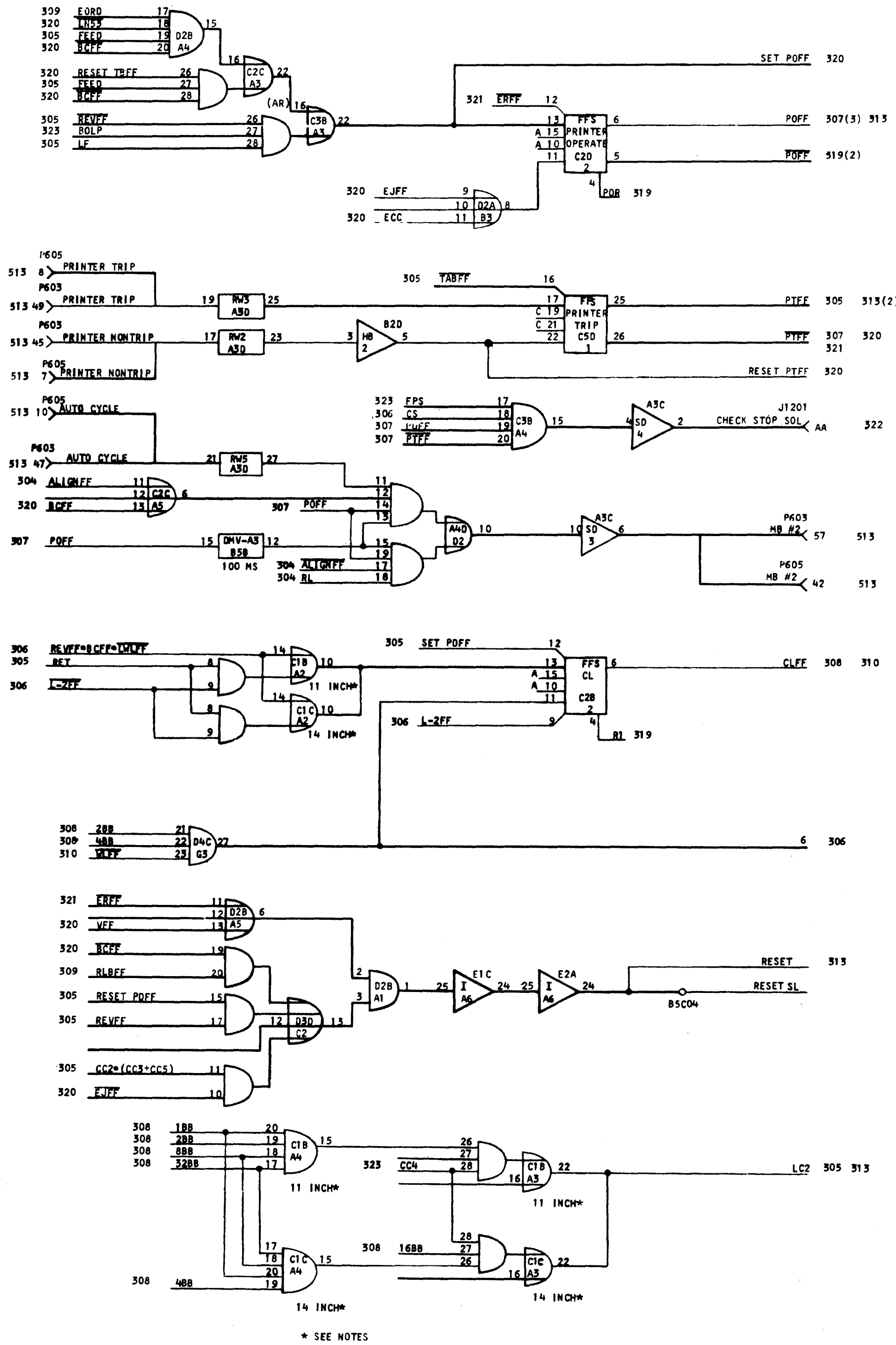

ALIGN
ALIGNFF
SL
RL
LOCK
CC3•FPS•ERFF•LOCK
CRG MOTOR SL
CRG MOTORFF SL
UPPER GATE TIE POINT
CRG LOCK SOL
PROG CAMFF SL
LEDGER READY
PROG CAM SOL
ARP ON•FL
ARP ON
AR PWR ON
FLBB
POR

Ref. Page 304

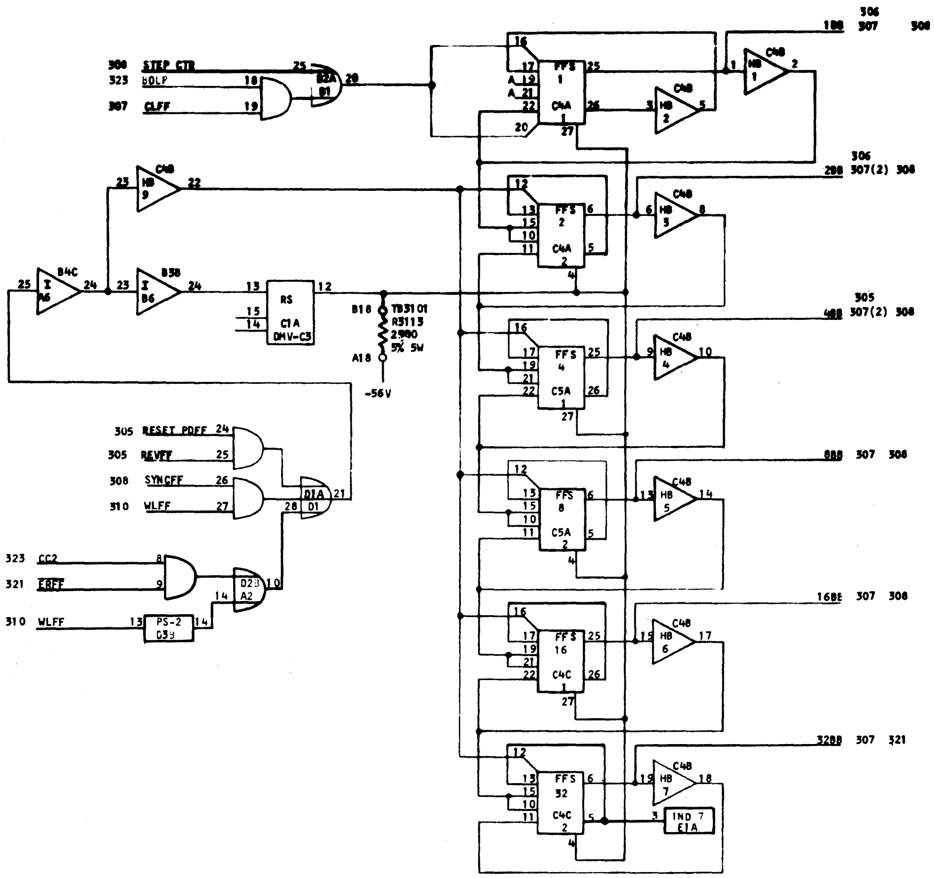


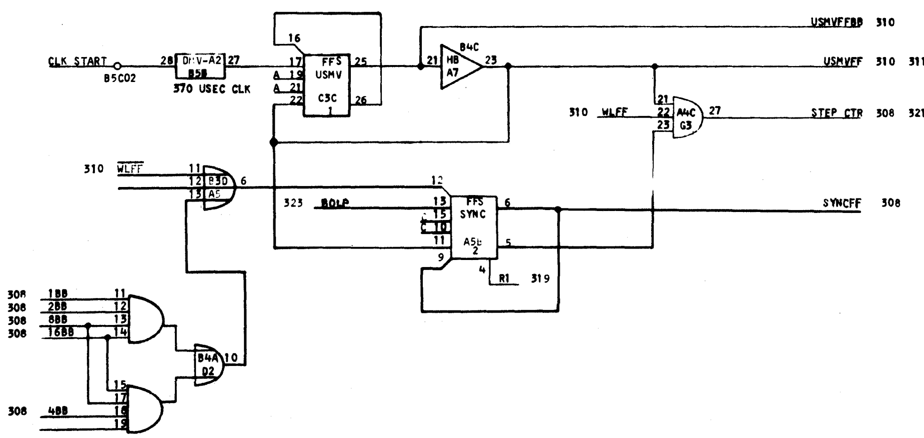
Ref. Page 305


FF3X
RL
CC4
ALIGNFF
FF16
READ AMPX
ERFF
BCFF
FF4
REVFF
PS-3
DMV-C4
6MS
FFS
FF16
IND 8
TB3101
R3103
2400
R3101
1600
R3102
1600
R3104
100
C3101
10UF
150VDC
-100V
WRITE AMP LF
TRANS LINE FIND
LFRA
REVFFBB
LWLFF
PU1
TB2002
J2001
J1201
REVFF•BCFF•LWLFF
WRITE X PULSE
WS
LFAFF
WMX
FFS
FF4
FF4
LWL
CC5
CC3
ERFF
FFS LWL
LWLFF
POR
29B
19B
CC4
BCFF
FH
RET
CC1
CC3+CC5
FFS L-2
L-2FF
CC1•(CC3+CC5)
S2001
CS/FH
GRD/+15V
J2002
RW10
RW11
FH
CS

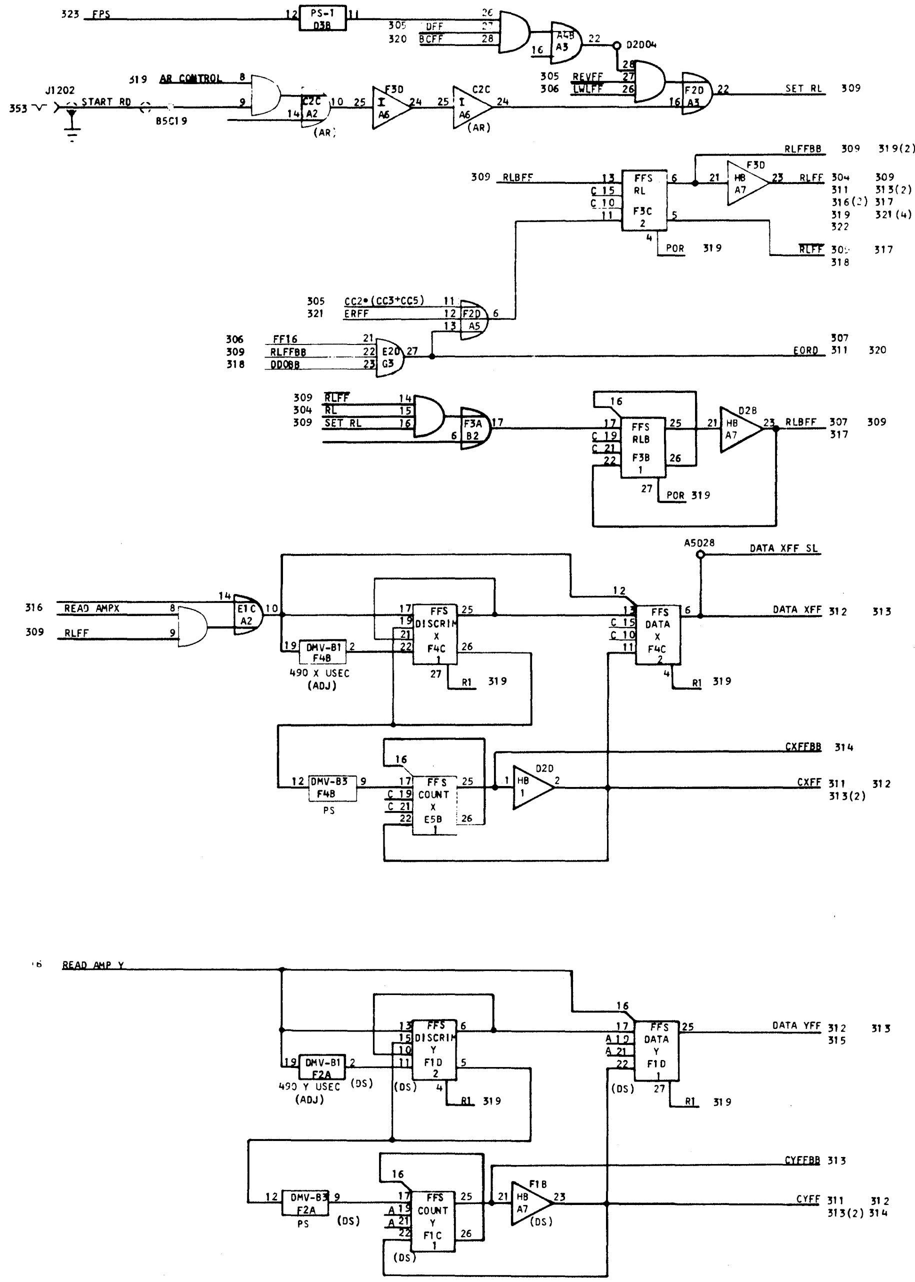

SET POFF
POFF
PRINTER OPERATE
EJFF
ECC
PRINTER TRIP
PRINTER NONTRIP
PTFF
RESET PTFF
AUTO CYCLE
CHECK STOP SOL
ALIGNFF
BCFF
100 MS
SET POFF
CLFF
L-2FF
RESET
RESET SL
LC2
11 INCH*
14 INCH*
* SEE NOTES

Ref. Page 307


STEP CTR
BOLP
CLFF
RESET PDFF
REVFF
SYNCFF
WLFF
CC2
ERFF
-56V

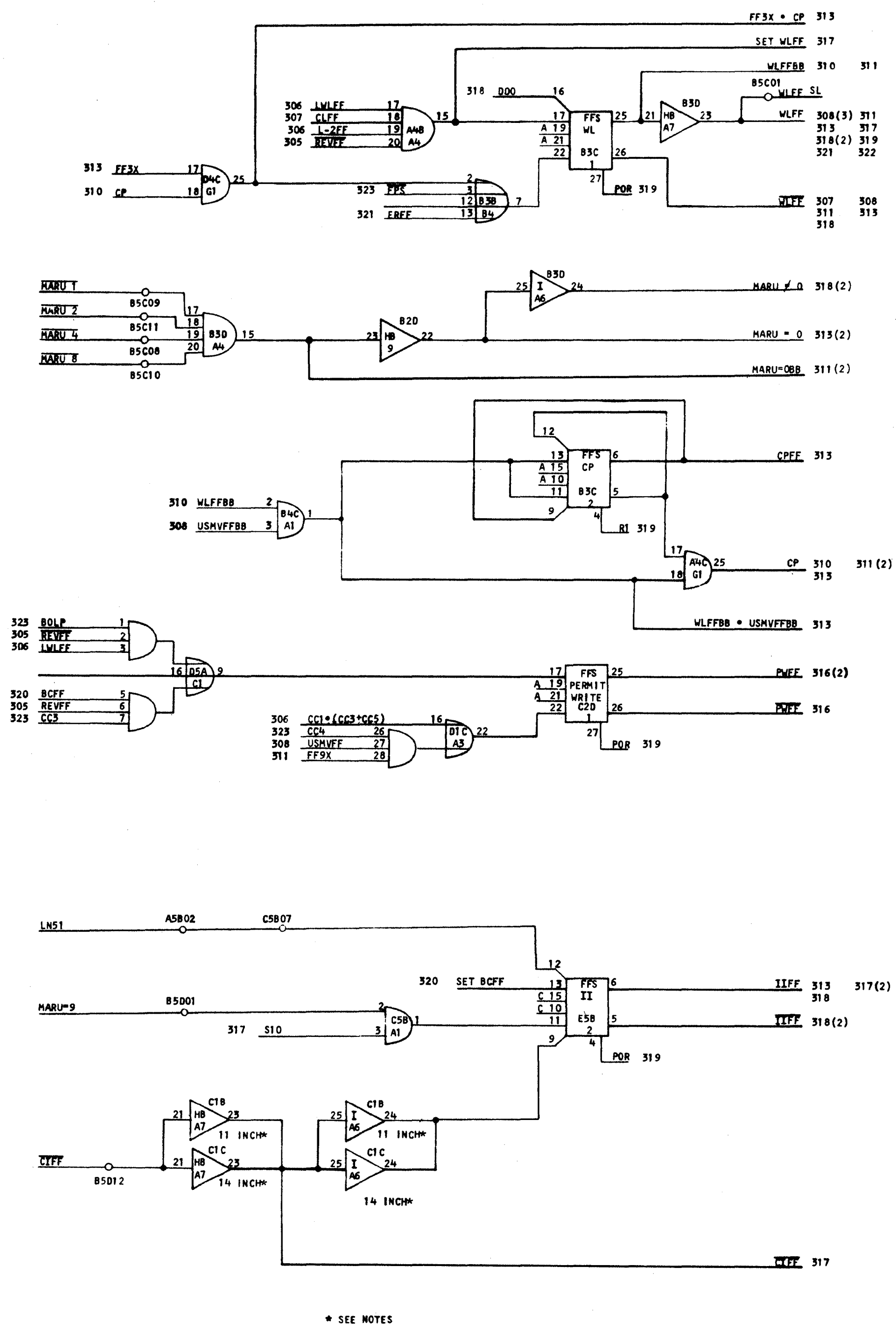

CLK START
370 USEC CLK
USMVFFBB
USMVFF
WLFF
STEP CTR
BOLP
SYNCFF

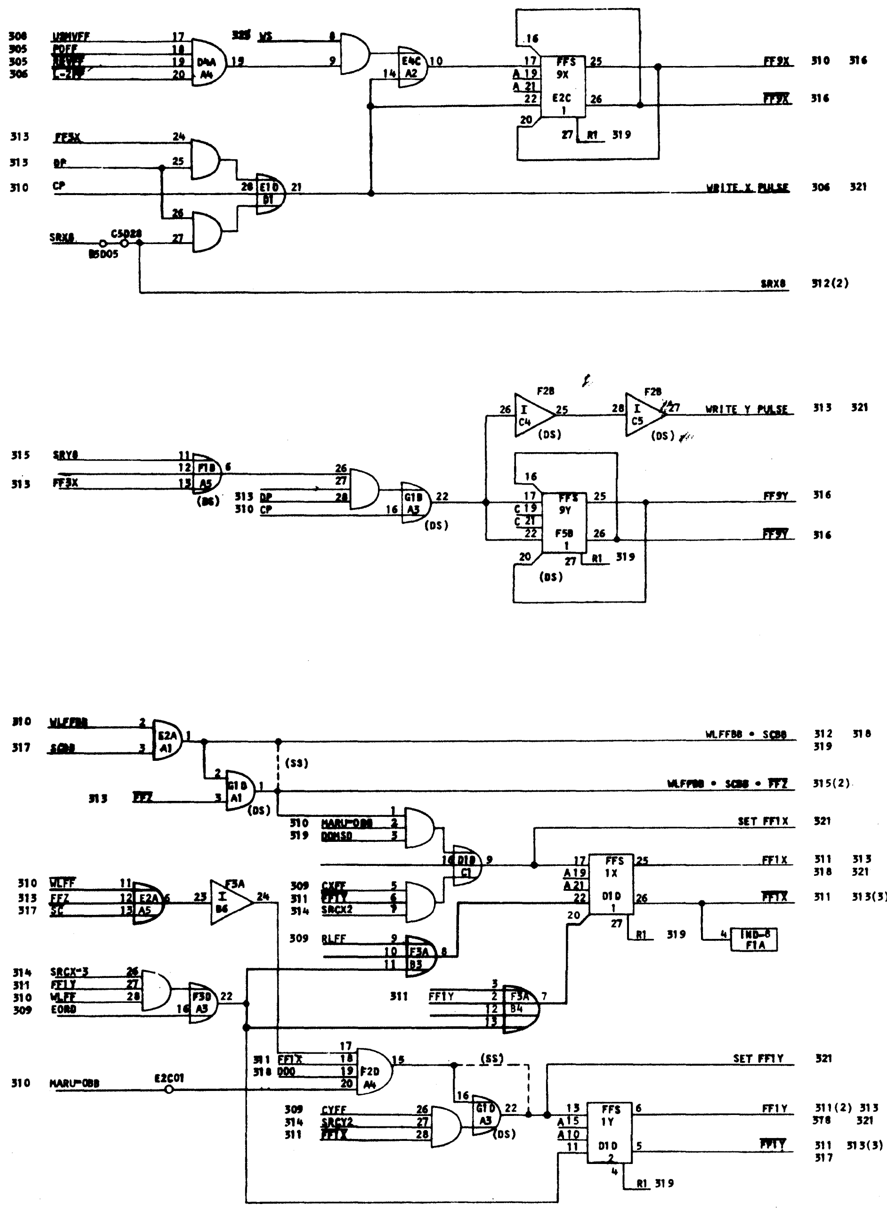
Ref. Page 308



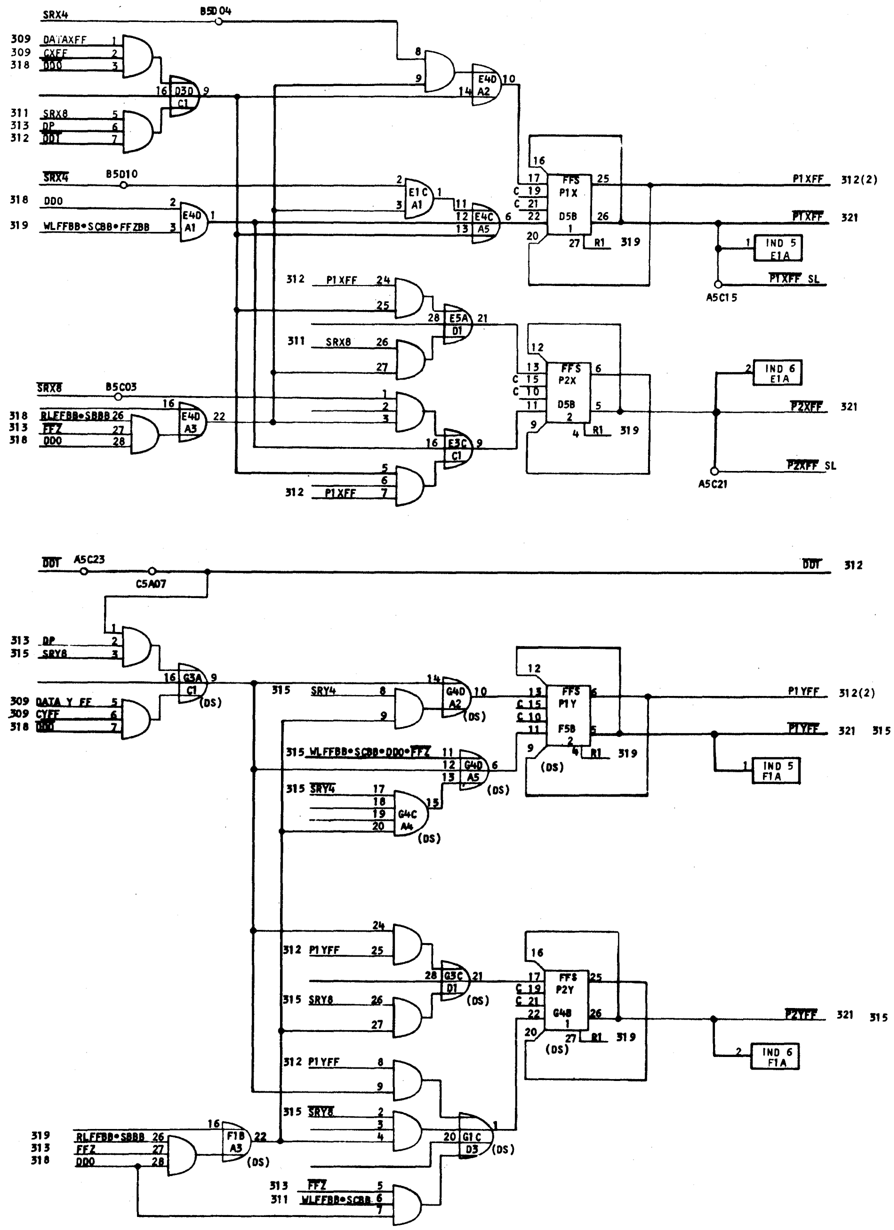
FPS
PS-1
SET RL
RLFF
RLBFF
POR
EORD
DATA XFF SL
DATA XFF
READ AMPX
DISCRIM
490 X USEC
(ADJ)
CXFFBB
CXFF
COUNT
READ AMP Y
DATA YFF
490 Y USEC
CYFFBB
CYFF

Ref. Page 309

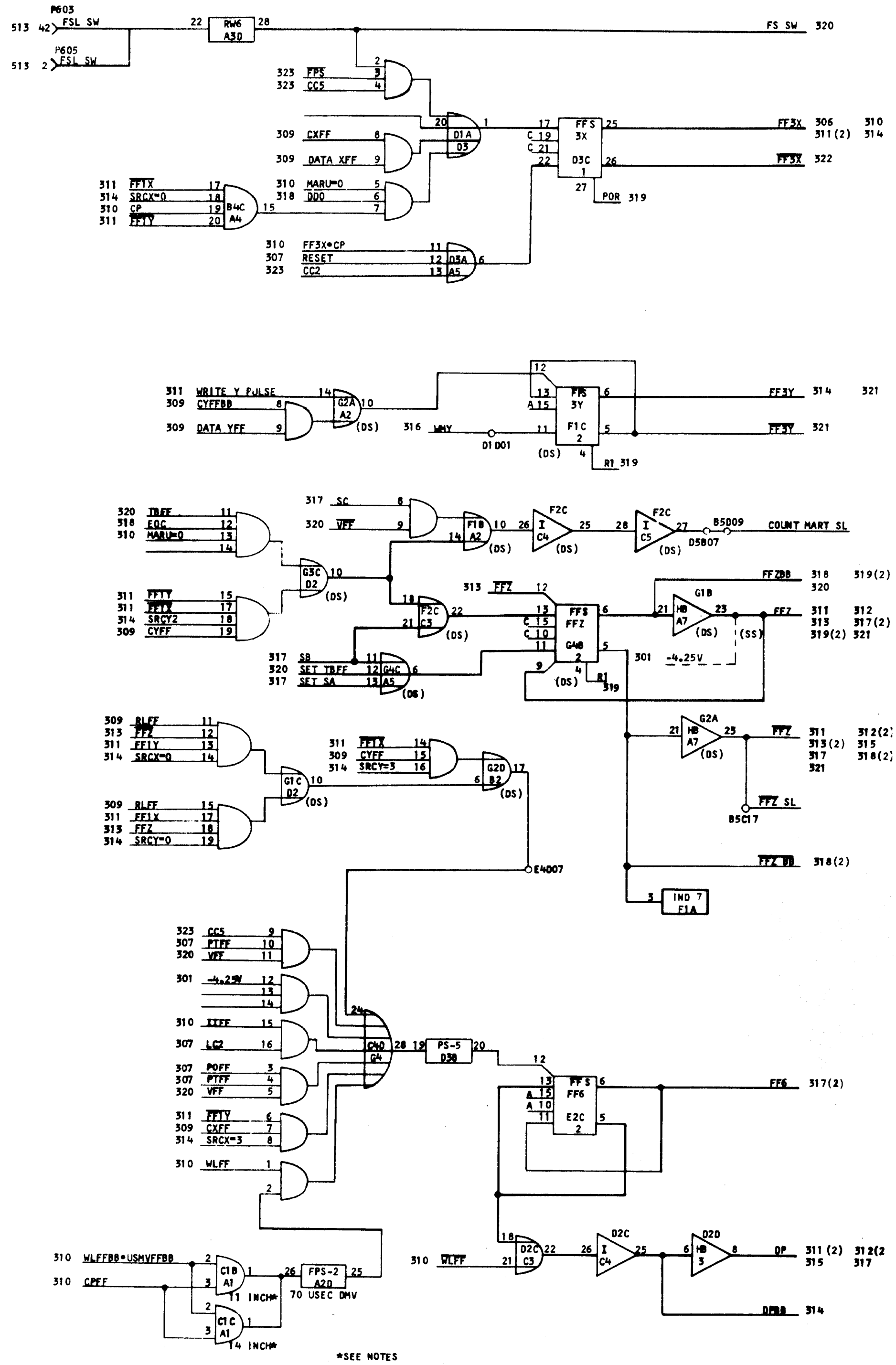

FF3X • CP 313
SET WLFF 317
WLFFBB 310 311
B5C01
WLFF SL
WLFF 308(3) 311 313 317 318(2) 319 321 322
WLFF 307 308 311 313 318
FFS WL B3C
POR 319
306 LWLFF
307 CLFF
306 L-2FF
305 REVFF
318 DOO
313 FF3X
310 CP
323 FFS
321 ERFF
MARU 1
MARU 2
MARU 4
MARU 8
B5C09
B5C11
B5C08
B5C10
MARU ≠ 0 318(2)
MARU = 0 313(2)
MARU=0BB 311(2)
FFS CP B3C
CPFF 313
310 WLFFBB
308 USMVFFBB
R1 319
CP 310 311(2) 313
WLFFBB • USMVFFBB 313
323 BOLP
305 REVFF
306 LWLFF
320 BCFF
305 REVFF
323 CC3
FFS PERMIT WRITE C2D
PWFF 316(2)
PWFF 316
306 CC1•(CC3+CC5)
323 CC4
308 USMVFF
311 FF9X
POR 319
LN51
A5B02
C5B07
320 SET BCFF
MARU=9
B5D01
317 S10
FFS II E5B
IIFF 313 317(2) 318
IIFF 318(2)
POR 319
CIFF
B5D12
11 INCH*
14 INCH*
CIFF 317
* SEE NOTES



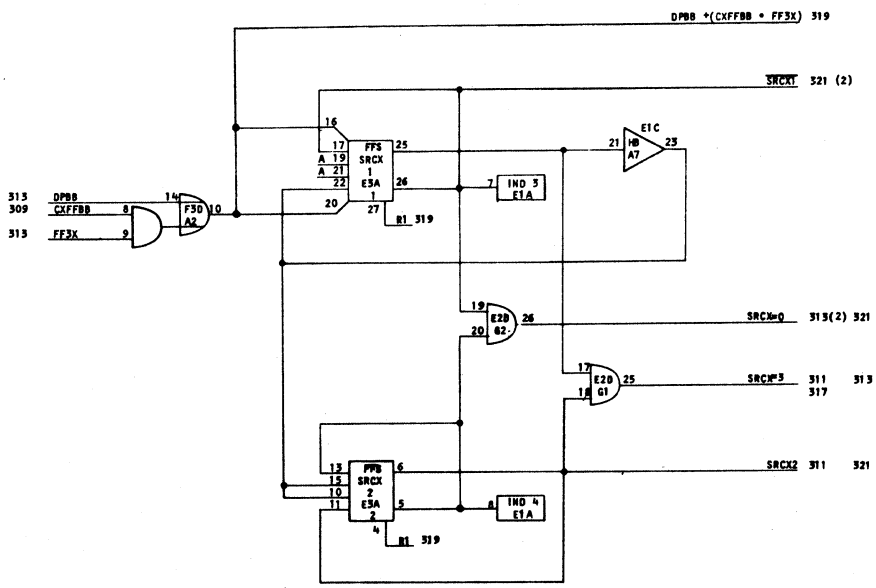
Ref. Page 311

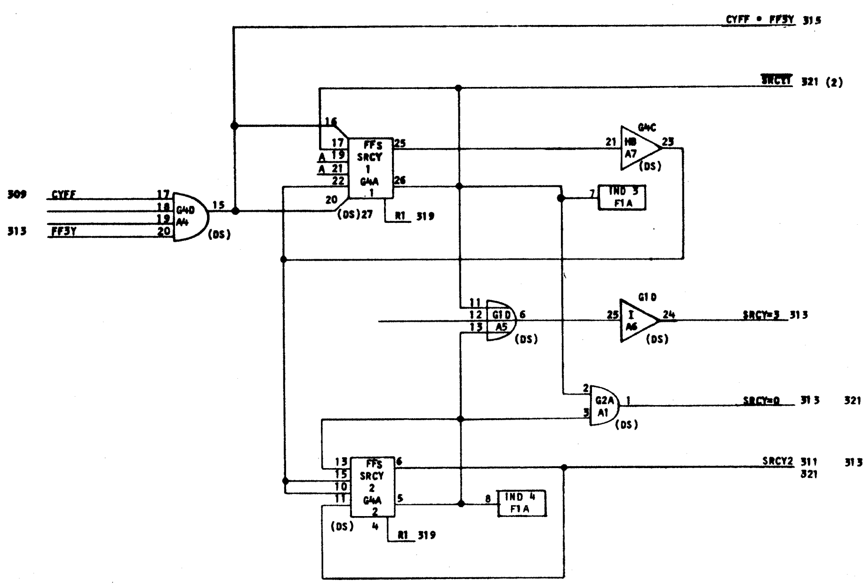


Ref. Page 312

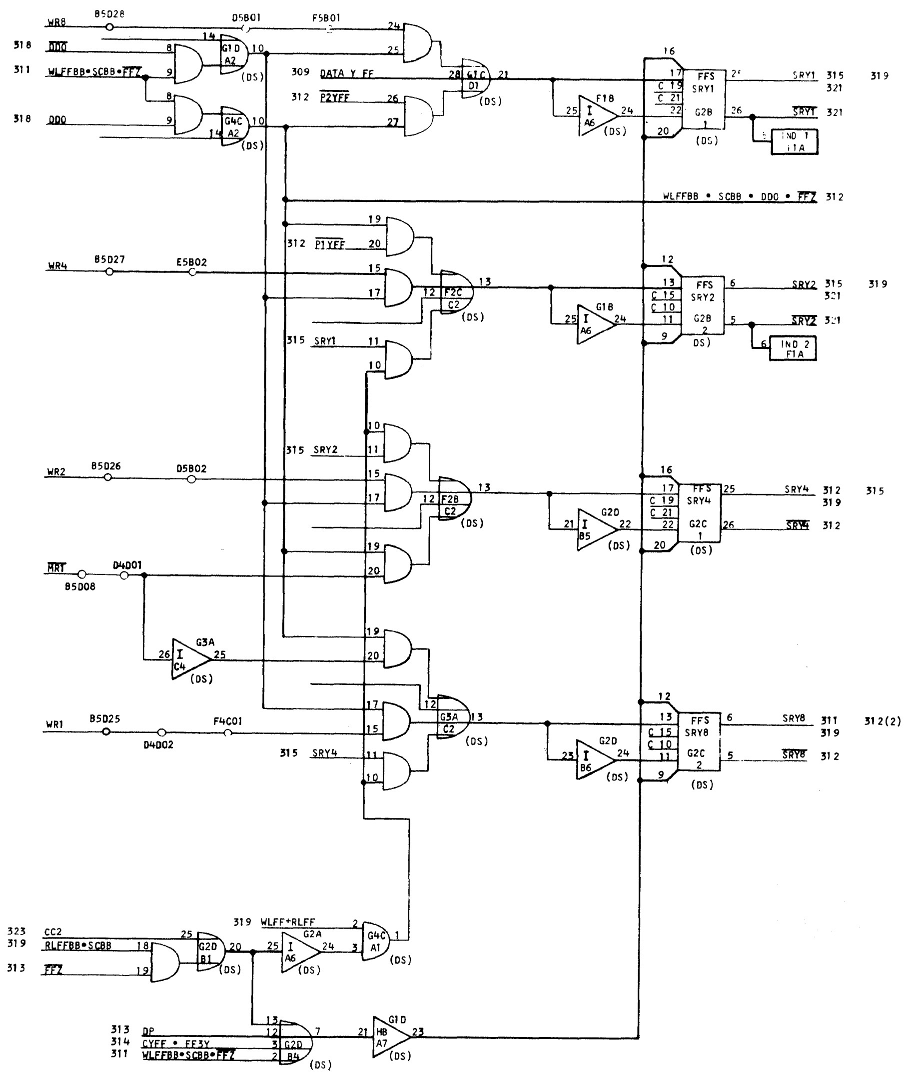

FSL SW
FS SW 320
FF3X
FF3Y
COUNT MART SL
FFZBB
FFZ
FFZ SL
IND 7 F1A
FF6 317(2)
DP
DPBB 314
70 USEC DMV
*SEE NOTES

Ref. Page 313

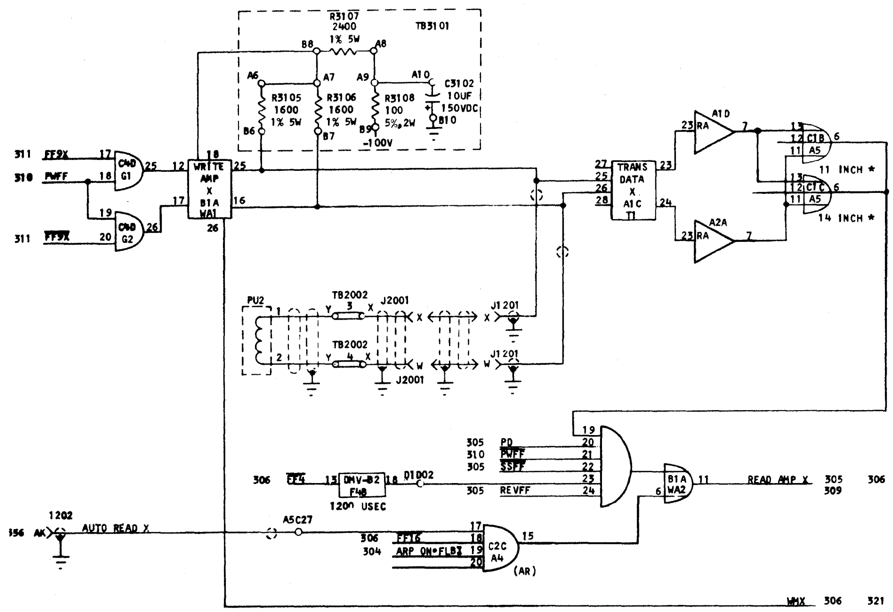

DPBB +(CXFFBB • FF3X) 319
SRCX1 321 (2)
313 DPBB
309 CXFFBB
313 FF3X
F3D A2
FFS SRCX 1 E3A
R1 319
E1C HB A7
IND 3 E1A
E2D B2
SRCX=0 313(2) 321
E2D G1
SRCX=3 311 313 317
FFS SRCX 2 E3A
SRCX2 311 321
IND 4 E1A
R1 319

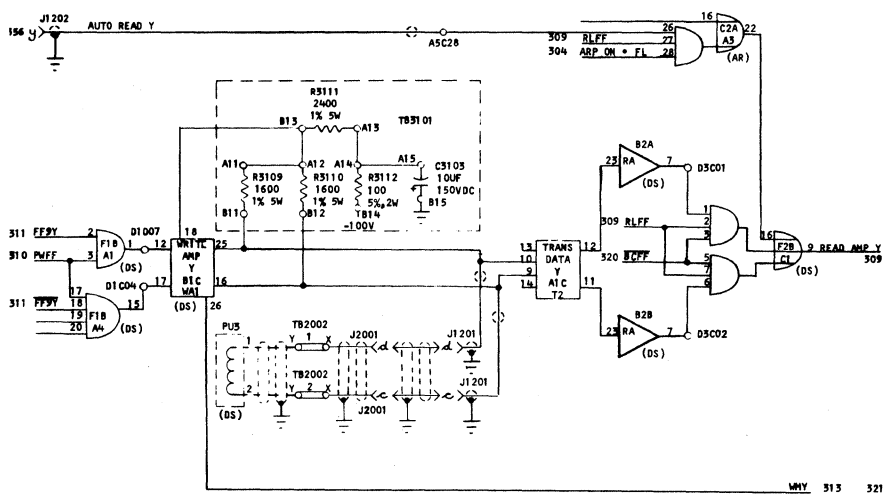

CYFF • FF3Y 315
SRCY1 321 (2)
309 CYFF
313 FF3Y
G4D A4
(DS)
FFS SRCY 1 G4A
R1 319
G4C HB A7
IND 3 F1A
G1D A5
G1D I A6
SRCY=3 313
G2A A1
SRCY=0 313 321
FFS SRCY 2 G4A
SRCY2 311 313 321
IND 4 F1A
R1 319

Ref. Page 314

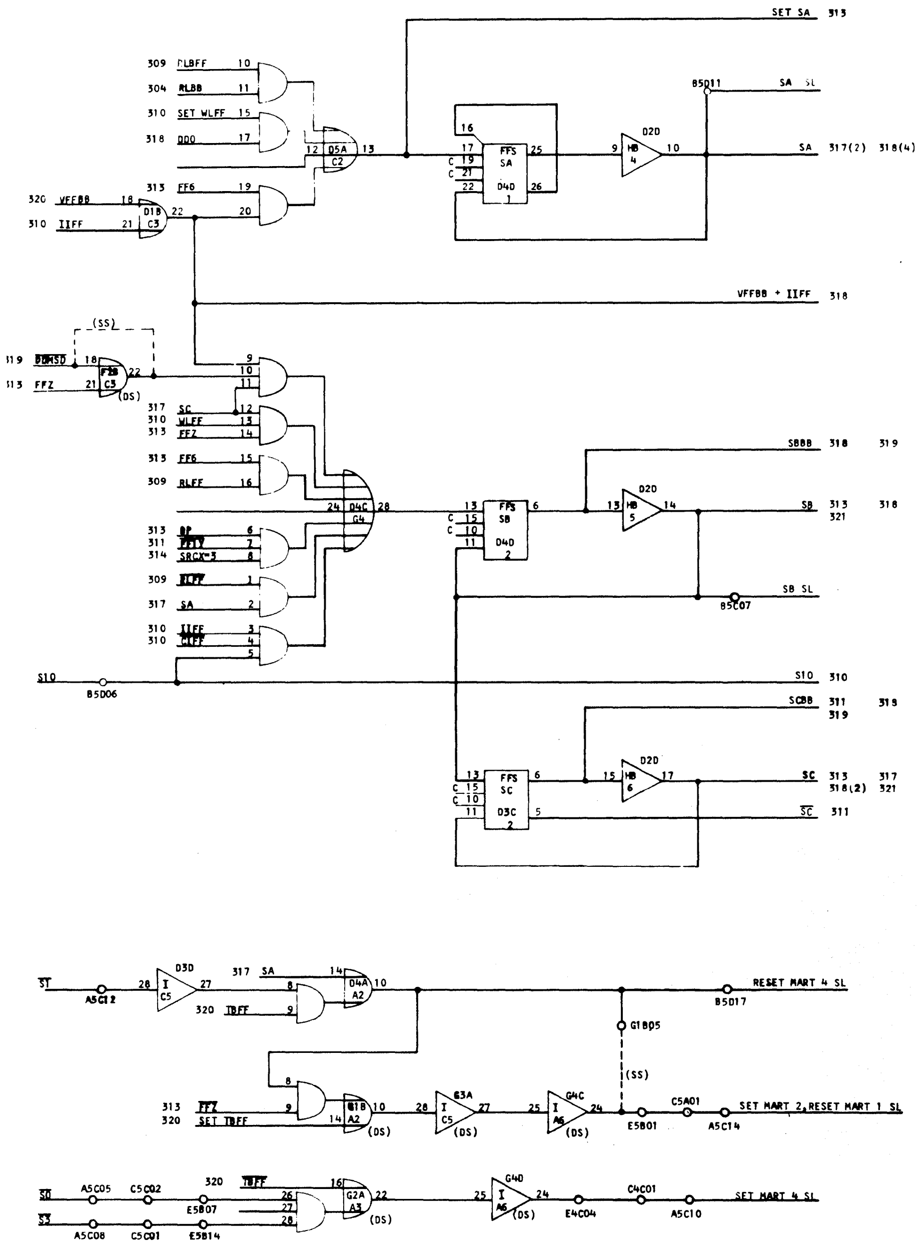

WR8
85D28
D5B01
F5B01
318 DDO
311 WLFFBB•SCBB•FFZ
318 DDO
309 DATA Y FF
312 P2YFF
FFS SRY1
SRY1 315 321 319
SRY1 321
IND 1 F1A
WLFFBB • SCBB • DDO • FFZ 312
312 P1YFF
WR4
85D27
E5B02
FFS SRY2
SRY2 315 321 319
SRY2 321
IND 2 F1A
315 SRY1
315 SRY2
WR2
85D26
D5B02
FFS SRY4
SRY4 312 319 315
SRY4 312
MRT
D4D01
85D08
WR1
85D25
D4D02
F4C01
315 SRY4
FFS SRY8
SRY8 311 319 312(2)
SRY8 312
323 CC2
319 RLFFBB•SCBB
313 FFZ
319 WLFF+RLFF
313 DP
314 CYFF • FF3Y
311 WLFFBB•SCBB•FFZ

Ref. Page 315

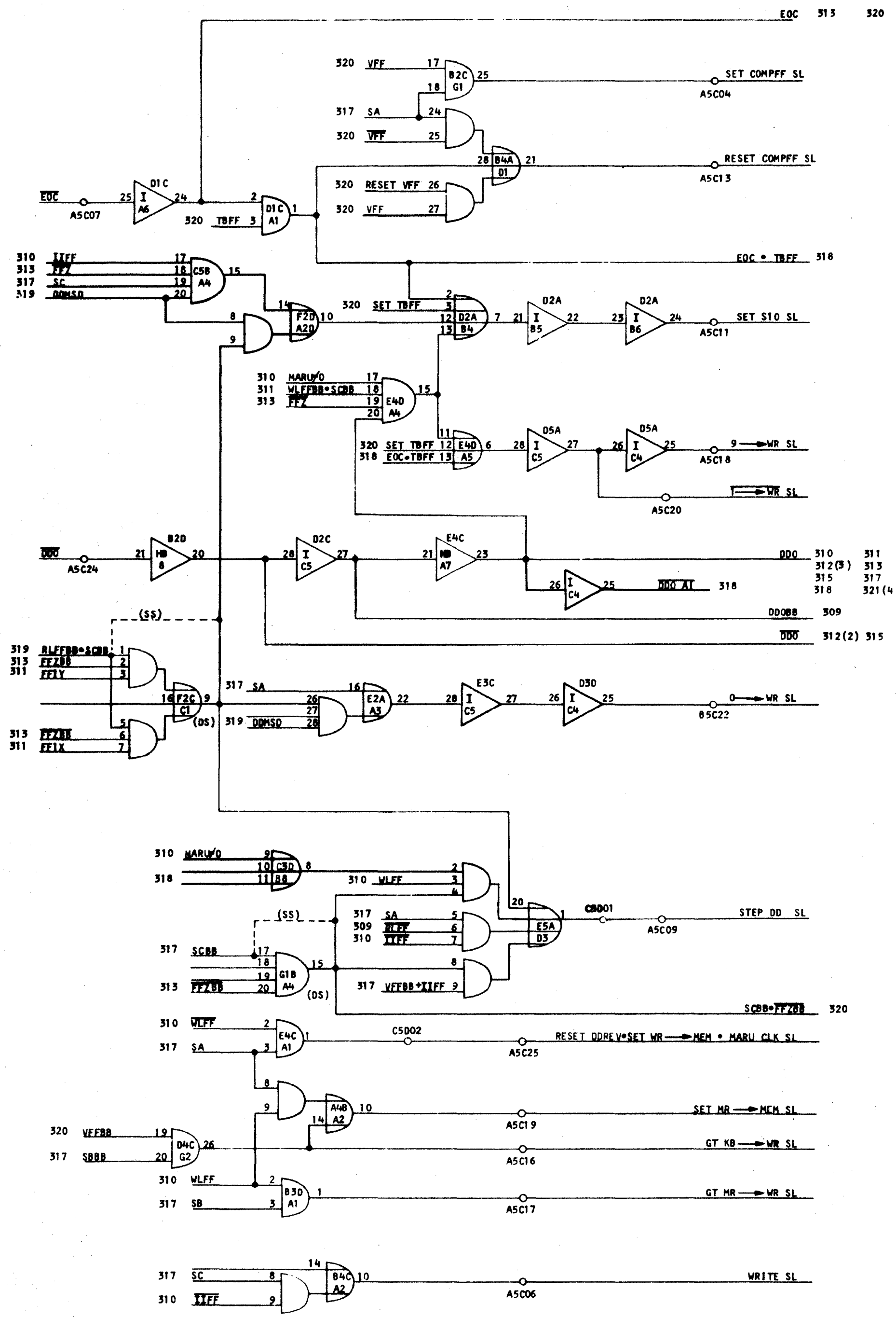

R3107
2400
1% 5W
TB3101
C3102
10UF
150VDC
R3105
1600
1% 5W
R3106
1600
1% 5W
R3108
100
-100V
WRITE AMP X
B1A
WA1
TRANS DATA X
A1C
T1
11 INCH *
14 INCH *
PU2
TB2002
J2001
J1201
READ AMP X
AUTO READ X
REVFF
1200 USEC
ARP ON•FLB3
(AR)
WHX


J1202
AUTO READ Y
A5C28
RLFF
ARP ON • FL
(AR)
R3111
2400
1% 5W
TB3101
C3103
10UF
150VDC
R3109
1600
1% 5W
R3110
1600
1% 5W
R3112
100
-100V
WRITE AMP Y
B1C
WA1
(DS)
TRANS DATA Y
A1C
T2
D3C01
D3C02
READ AMP Y
PU3
TB2002
J2001
J1201
WHY

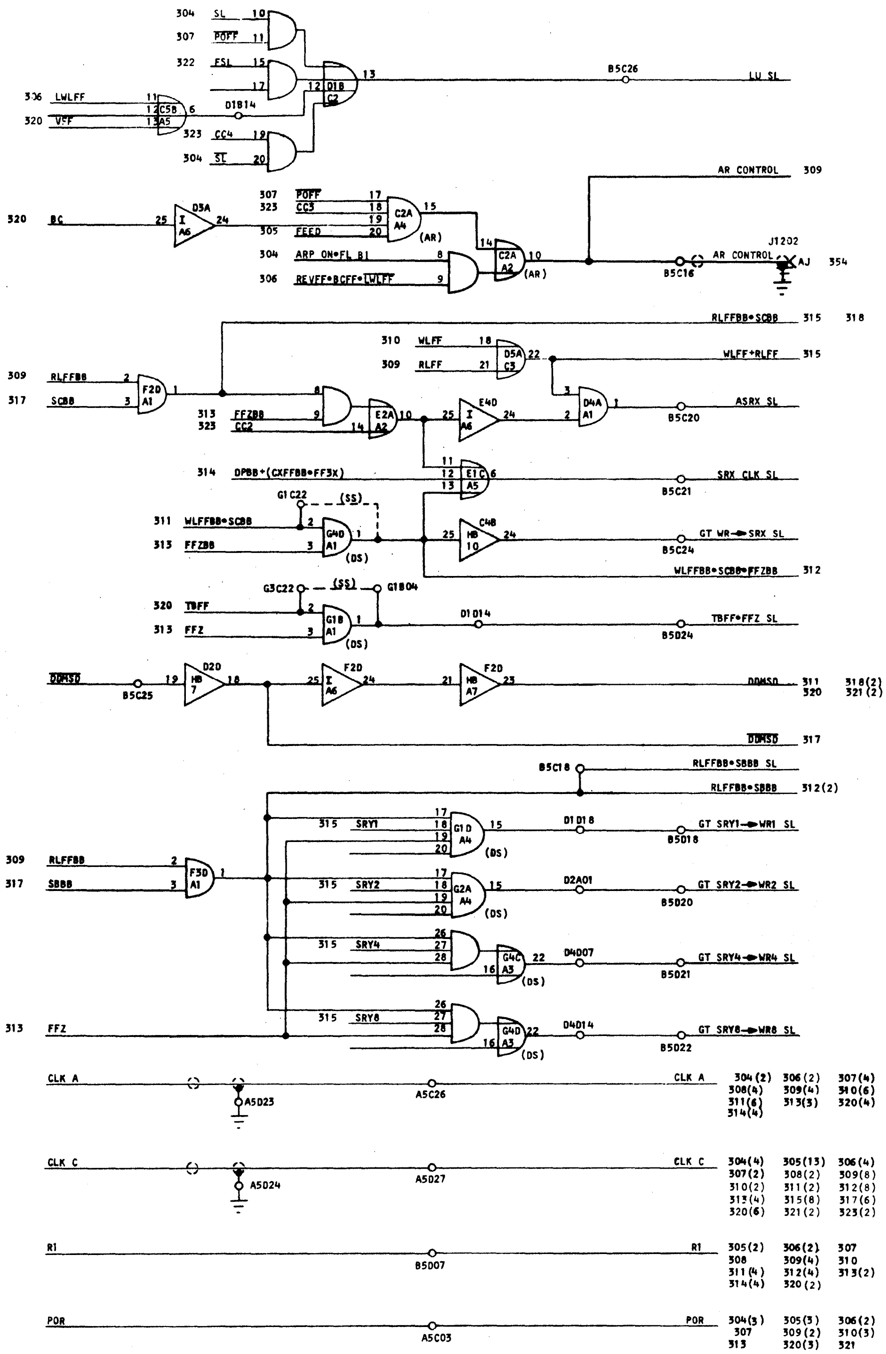
Ref. Page 316


SET SA 313
309 RLBFF
304 RLBB
310 SET WLFF
318 DDO
313 FF6
320 VFFBB
310 IIFF
D5A C2
D1B C3
FFS SA D4D 1
D2D
B5D11
SA SL
SA 317(2) 318(4)
VFFBB + IIFF 318
(SS)
119
113 FFZ
(DS)
317 SC
310 WLFF
313 FFZ
313 FF6
309 RLFF
313
311
314 SRCX=3
309
317 SA
310 IIFF
310
D4C G4
FFS SB D4D 2
SBBB 318 319
SB 313 321 318
SB SL
B5C07
S10
B5D06
S10 310
SCBB 311 319 319
FFS SC D3C 2
SC 313 318(2) 317 321
SC 311
ST
A5C12
D3D
I C5
317 SA
320 TBFF
D4A A2
RESET MART 4 SL
B5D17
G1B05
(SS)
313 FFZ
320 SET TBFF
G1B A2
G3A I C5
G4C I A6
E5B01
C5A01
A5C14
SET MART 2, RESET MART 1 SL
SD
S3
A5C05
C5C02
A5C08
C5C01
320 TBFF
E5B07
E5B14
G2A A3
G4D I A6
E4C04
C4C01
A5C10
SET MART 4 SL

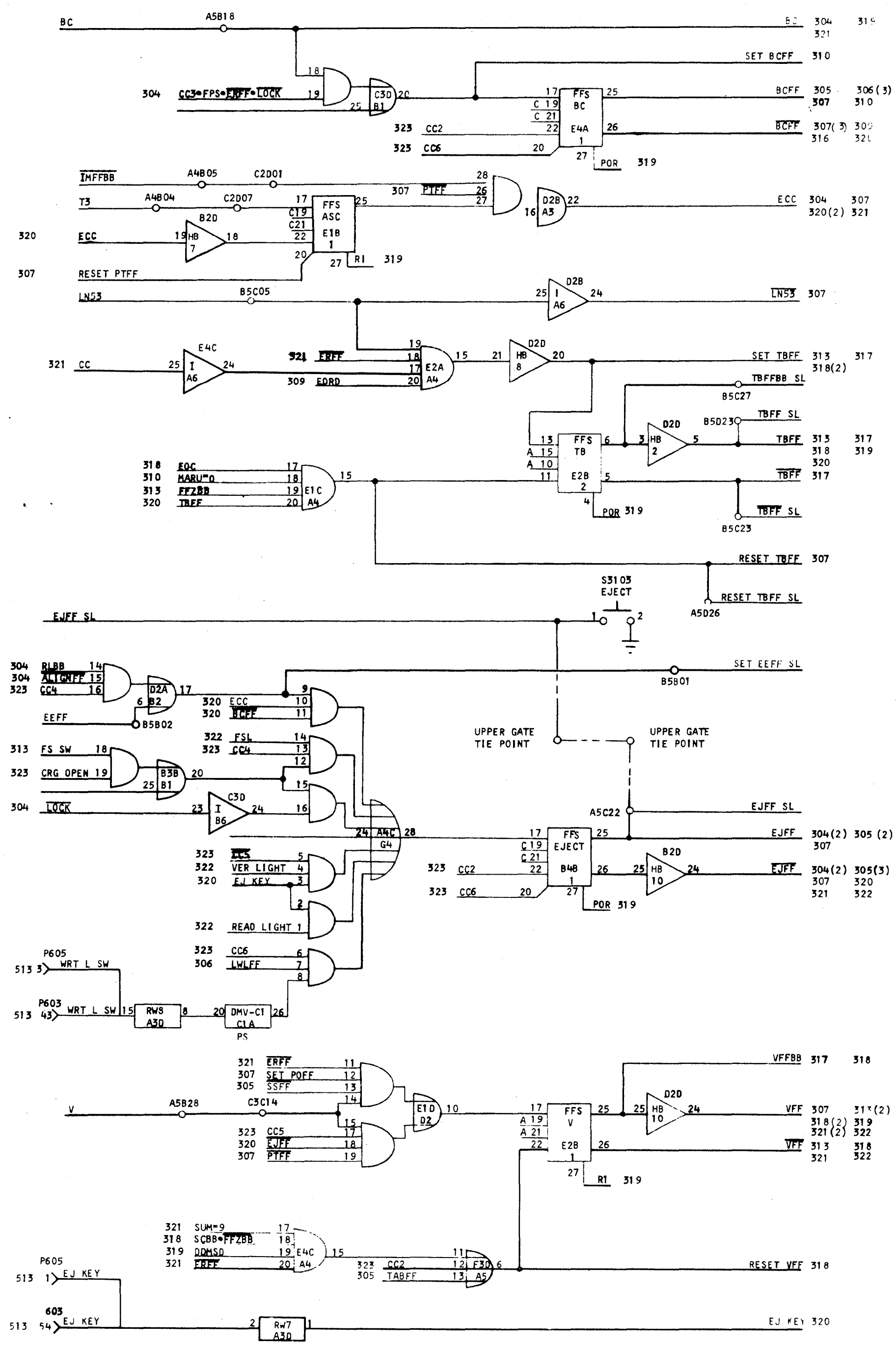
Ref. Page 317


EOC 313 320
SET COMPFF SL
RESET COMPFF SL
EOC • TBFF 318
SET S10 SL
9 → WR SL
1 → WR SL
DDO 310 311 312(3) 313 315 317 318 321(4
DDO A1 318
DDOBB 309
DDO 312(2) 315
0 → WR SL
STEP DD SL
SCBB•FFZBB 320
RESET DDREV•SET WR → MEM • MARU CLK SL
SET MR → MEM SL
GT KB → WR SL
GT MR → WR SL
WRITE SL

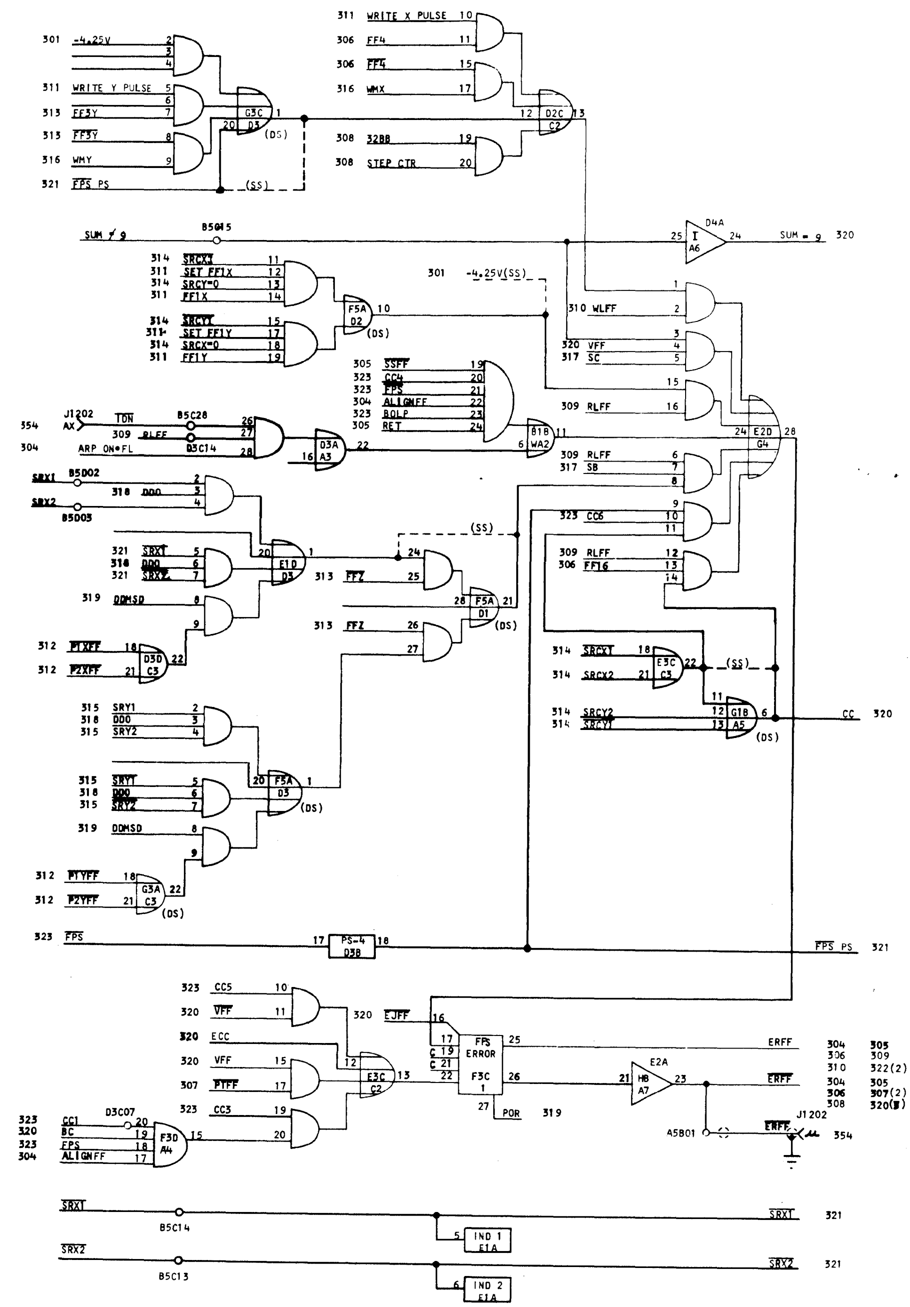
Ref. Page 318


LU SL
AR CONTROL 309
AR CONTROL
J1202
RLFFBB•SCBB 315 318
WLFF+RLFF 315
ASRX SL
SRX CLK SL
GT WR→SRX SL
WLFFBB•SCBB•FFZBB 312
TBFF•FFZ SL
DDMSD 311 320 318(2) 321(2)
DDMSD 317
RLFFBB•SBBB SL
RLFFBB•SBBB 312(2)
GT SRY1→WR1 SL
GT SRY2→WR2 SL
GT SRY4→WR4 SL
GT SRY8→WR8 SL
CLK A
CLK C
R1
POR

Ref. Page 319

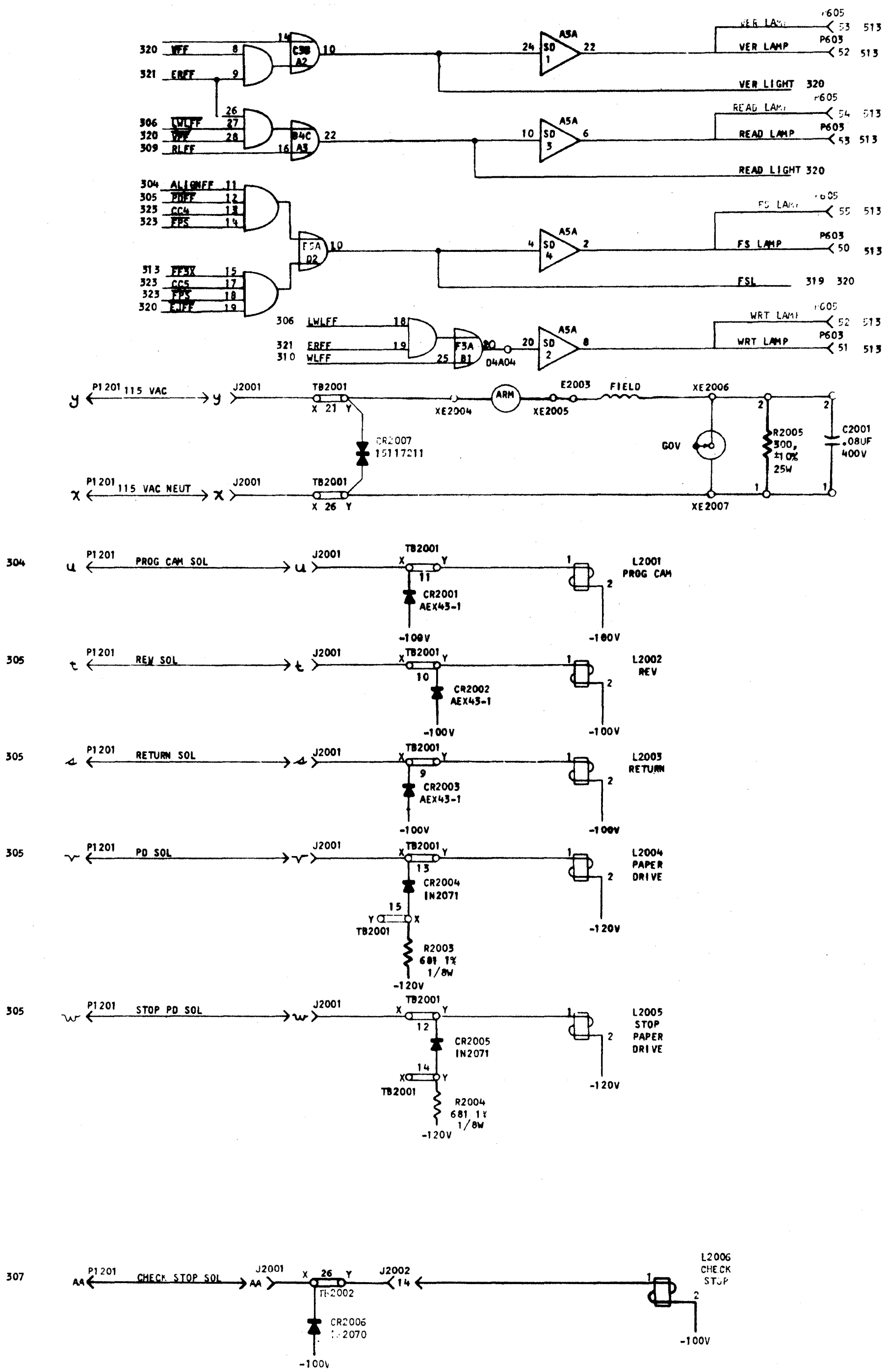


Ref. Page 320

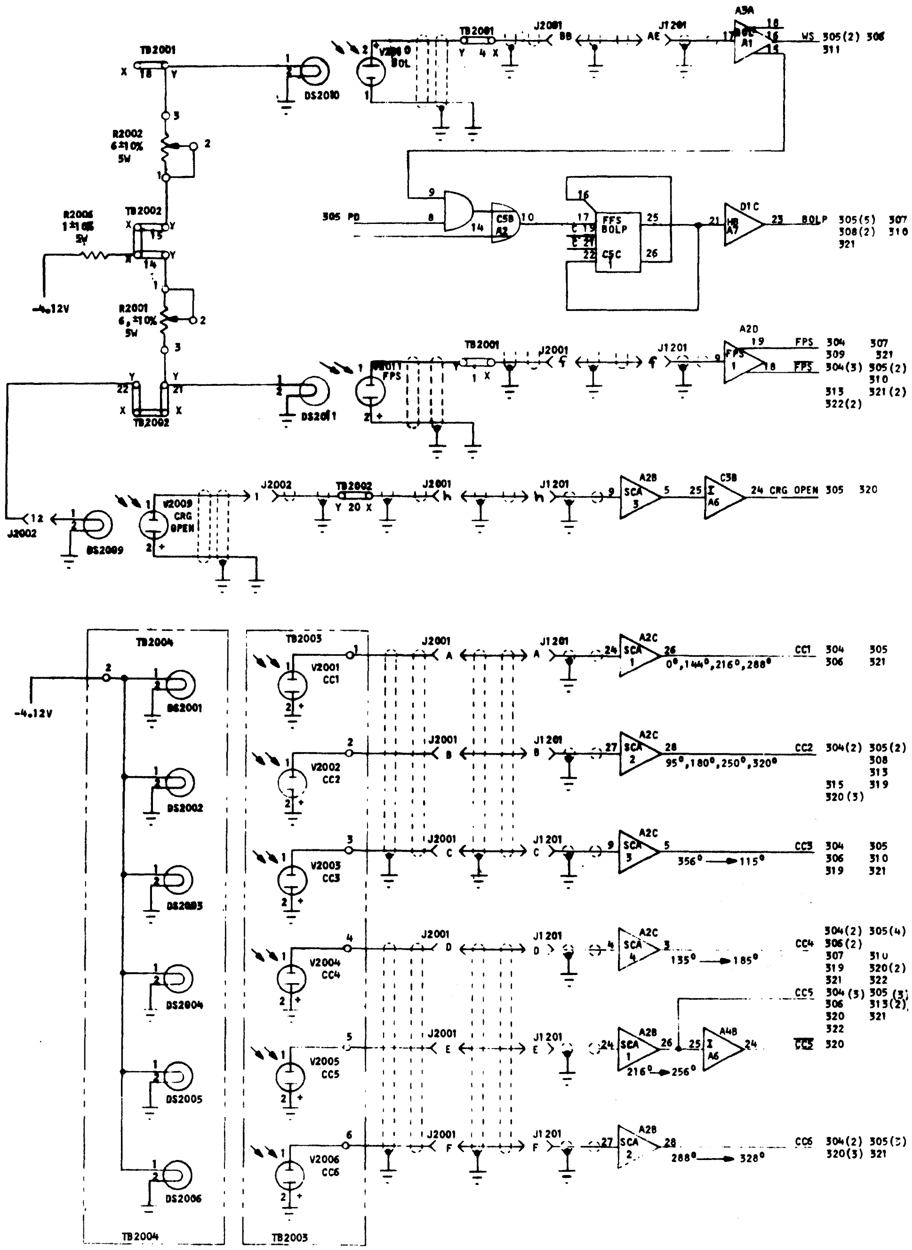


WRITE X PULSE
WRITE Y PULSE
FF3Y
WMY
FPS PS
FF4
WMX
32BB
STEP CTR
SUM ≠ 9
SUM = 9
SRCY=0
SET FF1X
FF1X
SET FF1Y
SRCX=0
FF1Y
SSFF
ALIGNFF
BOLP
RET
TDN
ARP ON•FL
WLFF
VFF
SC
RLFF
SB
CC6
FF16
DDO
DDMSD
SRY1
SRY2
SRXT
SRX2
FFZ
SRCX2
SRCY2
CC
FPS
FPS ERROR
ERFF
EJFF
ECC
PTFF
CC5
CC3
CC1
BC
POR
IND 1
IND 2

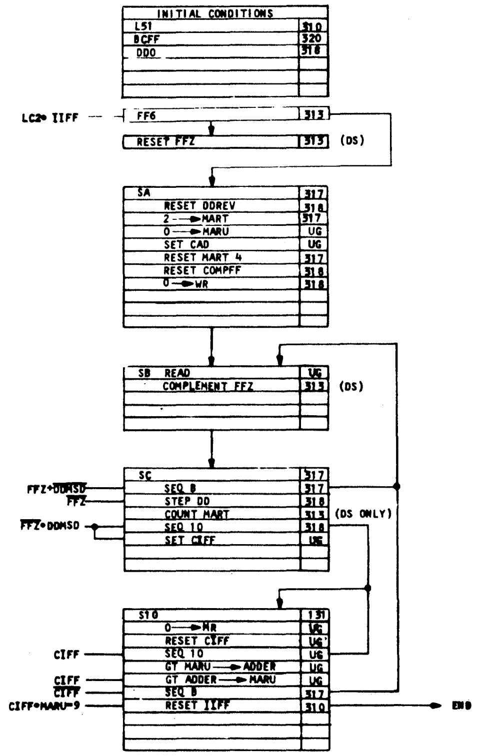
Ref. Page 321


VER LAMP
VER LIGHT 320
READ LAMP
READ LIGHT 320
FS LAMP
FSL 319 320
WRT LAMP
P603
P1201 115 VAC
P1201 115 VAC NEUT
J2001
TB2001
ARM
E2003
FIELD
XE2004
XE2005
XE2006
XE2007
CR2007
GOV
R2005
C2001 .08UF 400V
PROG CAM SOL
L2001 PROG CAM
CR2001 AEX43-1
-100V
REV SOL
L2002 REV
CR2002 AEX43-1
RETURN SOL
L2003 RETURN
CR2003 AEX43-1
PD SOL
L2004 PAPER DRIVE
CR2004 IN2071
R2003 681 1% 1/8W
-120V
STOP PD SOL
L2005 STOP PAPER DRIVE
CR2005 IN2071
R2004 681 1% 1/8W
CHECK STOP SOL
J2002
L2006 CHECK STOP
CR2006

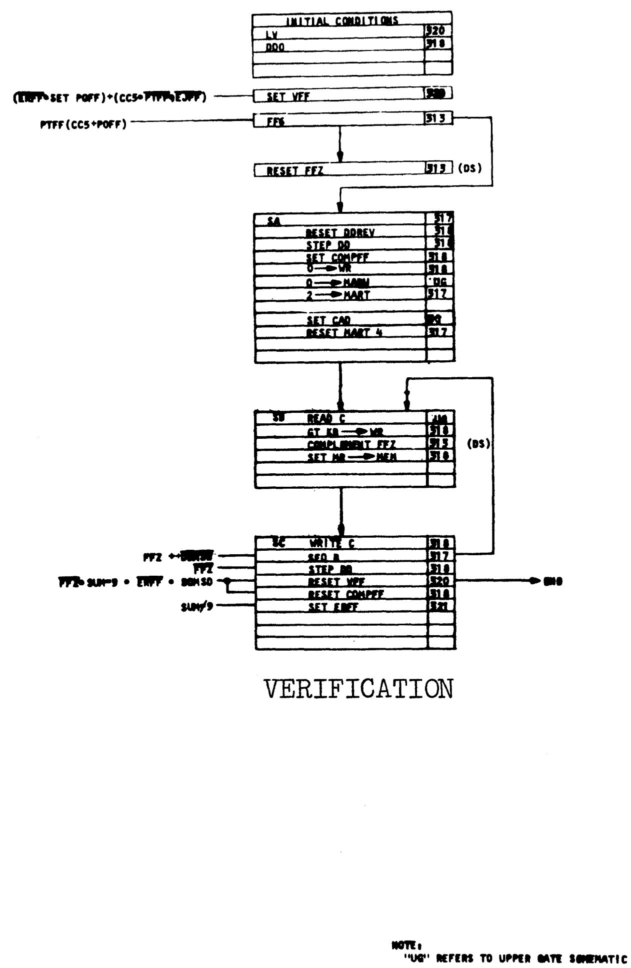
Ref. Page 322



Ref. Page 323



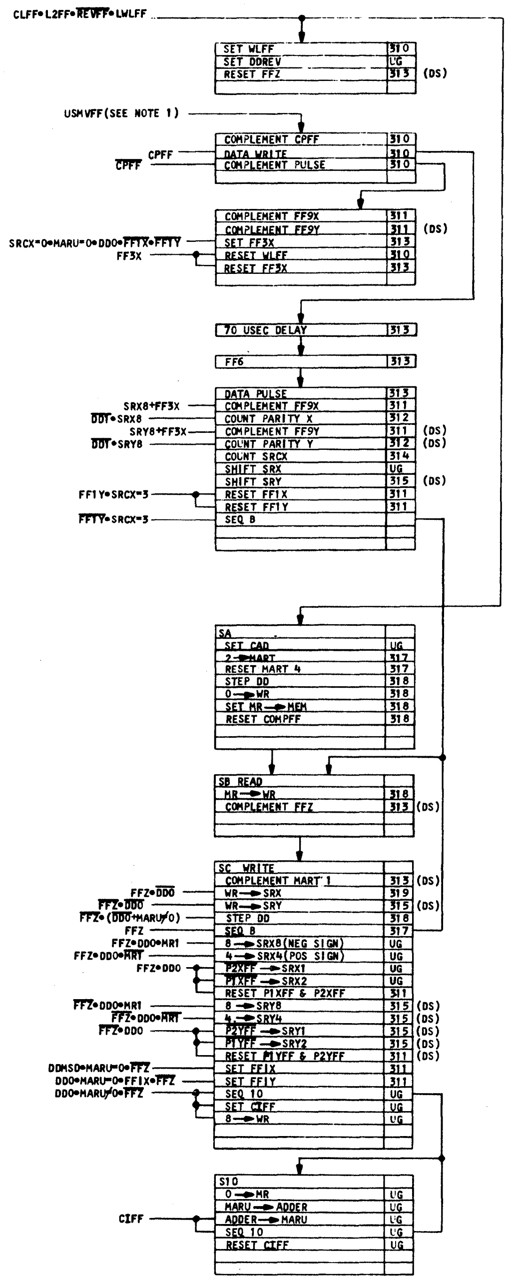
INITIAL INSTALLATION



VERIFICATION

Ref. Page 325

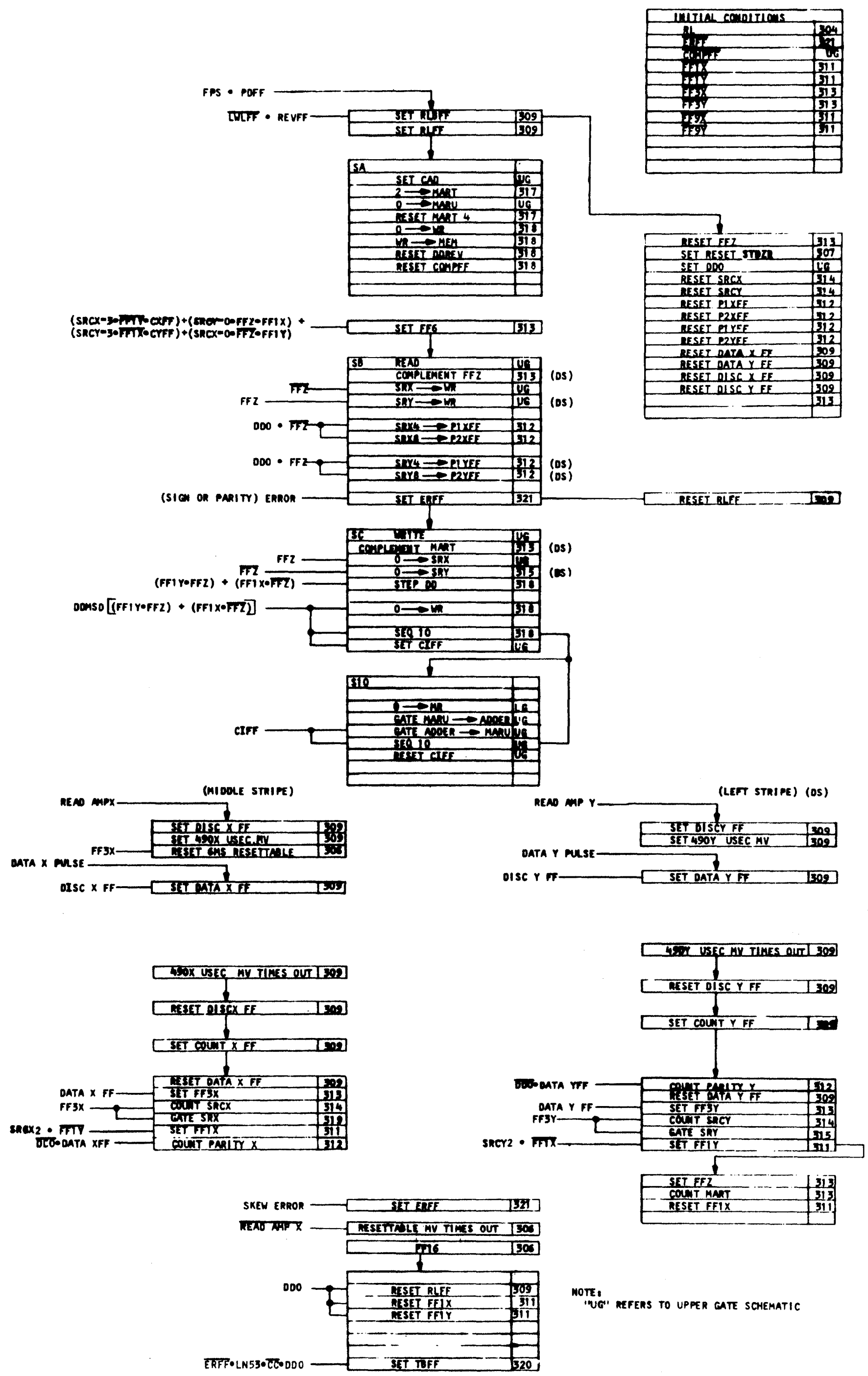
INITIAL CONDITIONS	
PMA	UG
LWLFF	306
DDO	318
$\overline{CIFF}$	UG
FF9X	311
PWFF	310
$\overline{P1XFF}$	312
$\overline{P2XFF}$	312
$\overline{CPFF}$	310
SRCX=0	314
$\overline{FF4}$	306
$\overline{FF1X}$	311
$\overline{FF1Y}$	311
$\overline{FF3X}$	313
$\overline{P1YFF}$	312
$\overline{P2YFF}$	312
$\overline{FF3Y}$	313
$\overline{FF9Y}$	311



WRITE LEDGER

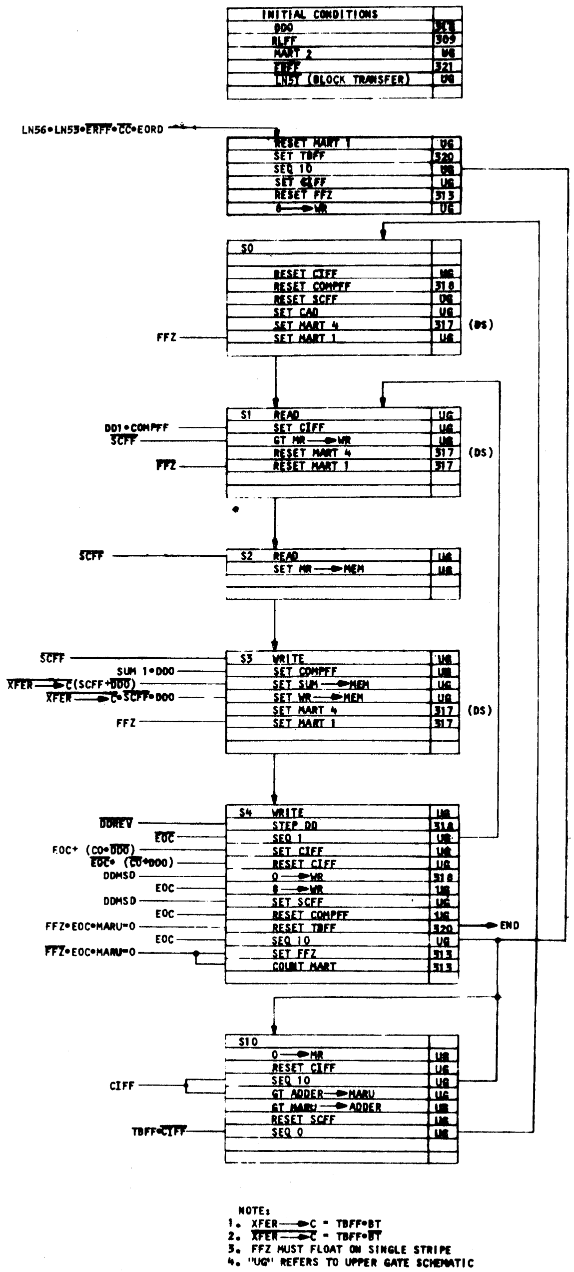
NOTE:
1. WHENEVER NOT IN ANY SEQ, USMVFF CONTROLS THE LOGIC
2. "UG" REFERS TO UPPER GATE SCHEMATIC

Ref. Page 326



READ LEDGER

Ref. Page 327



TRIAL BALANCE & BLOCK TRANSFER

Ref. Page 328

CARD LOC	CARD TYPE	CIRCUIT/PAGE 1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	FEATURE	TIE POINTS PIN/PAGE					
A1A	--																									
A1B	--																					3/302				
A1C	TRANS	316	316	306																						
A1D	RA	316																								
A2A	RA	316																								
A2B	SCA	323	323	323																						
A2C	SCA	323	323	323	323																					
A2D	FPS	323	313																							
A3A	BOLA	323																								
A3B	SD	304	304		304																					
A3C	SD	305	305	307	307																					
A3D	RW/ CW(S)	306	307	307		307	313	320	320	304	306	305	305													
A4A																										
A4B	A	305	318	307	310	305	323	305															4/320	5/320		
A4C	G	310	306	308	320																					
A4D	D	304	307	305																						
A5A	SD	322	322	322	322																					
A5B	FFS	304	308																		1/321	2/310	7/304	14/304	18/320	28/320
A5C INTERCONN PINS																					1/304	2/304	3/319	4/318	5/317	6/318
																					7/318	8/317	9/318	10/317	11/318	12/317
																					13/318	14/317	15/312	16/318	17/318	18/318
																					19/318	20/318	21/312	22/320	23/312	24/318
																					25/318	26/319	27/316	28/316	-	-
A5D	PDC	305																			23/319	24/319	25/305	26/320	27/319	28/309
																						22/304				
B1A	WA	316	316																							
B1B	WA	306	321																							
B1C	WA	316																		(DS)						
B1D	RA	306																								
B2A	RA	316																		(DS)						
B2B	RA	316																		(DS)						
B2C	G	318	306	305	304																					
B2D	HB	306	307	306	305	304	305	320	318	310	320															
B3A	DC	302		302	301	301	301		301																	
B3B	B	320	305	305	310	305	308																			
B3C	FFS	310	310																							
B3D	A	318	305	305	310	308	310	310																		
B4A	D	318	308	304																						
B4B	FFS	320	305																							
B4C	A	310	318	322	313	304	308	308																		
B4D	FFS	305	306																							
B5A	FFS	305	304																							
B5B	DMVA	305	308	307																	1/320	2/320	3/301		5/301	
B5C INTERCONN PINS																					1/310	2/308	3/312	4/307	5/320	
																					7/317	8/310	9/310	10/310	11/310	12/304
																					13/321	14/321	15/321	16/319	17/313	18/319
																					19/309	20/319	21/319	22/318	23/320	24/319
																					25/319	26/319	27/320	28/321	-	-
B5D INTERCONN PINS	PDC	305																			1/310	2/321	3/321	4/312	5/311	6/317
																					7/319	8/315	9/313	10/312	11/317	12/310
																					13/304	14/305	17/317	18/319	20/319	21/319
																					22/319	23/320	24/319	25/315	26/315	27/315
																					28/315	-	-	-	-	-
C1A	DMVC	320		308	306																					
C1B	A	313	307	307	307	316	310	310												*						
C1C	A	313	307	307	307	316	310	310												*						
C1D	FFS	305	305																							
C2A	A	304	319	316	319		304	304												(AR)						
C2B	FFS	306	307																							
C2C	A	304	309	307	316	307	309													(AR)						
C2D	FFS	310	307																		1/320		7/320			
C3A	DC	302			301		301																			
C3B	A	306	322	307	307	306	323	306																		
C3C	FFS	308	306																					14/320		
C3D	B	320	306	318	304	304	320																			
C4A	FFS	308	308																					14/306		
C4B	HB	308	308	308	308	308	308	308	305	308	319															
C4C	FFS	308	308																		1/317					
C4D	G	316	316	306	313																					
C5A	FFS	308	308																		1/317		7/312	14/304		
C5B	A	310	323	305	318	319	304	304															7/310			
C5C	FFS	323	305																		1/317	2/317				
C5D	FFS	307	305																		1/318	2/318			28/311	
D1A	D	308	305	313																						
D1B	C	311	319	317	304	304																	14/319			
D1C	A	318	306	310	305	305	318	323														4/316				
D1D	FFS	311	311																		1/313	2/316	7/316	14/319	18/319	
D2A	B	308	320	307	318	318	318														1/319					
D2B	A	307	308	320	307	307	320	309																		
D2C	C	305	321	313	313	318																				
D2D	HB	309	320	313	317	317	317	319	320	305	320											4/309				
D3A	A	304	306	321		313	319	305																		
D3B	PS	309	308	306	321	313																				
D3C	FFS	313	317																		1/316	2/316	7/321	14/321		
D3D	C	312	307	321	318	317																				
D4A	A	319	317	306	311	306	321	304														4/322				
D4B																										
D4C	G	310	318	307	317																					
D4D	FFS	317	317																		1/315	2/315	7/319	14/319		
LOC CARD	TYPE	1	2	3	4	5	6	7	8	9	10 CIRCUIT/PAGE	11	12	13	14	15	16	17	18	FEATURE	PIN/PAGE TIE POINTS					

Ref. Page 329

CARD LOC	CARD PAGE	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	FEATURE	TIE POINTS PIN/PAGE					
D5A	C	310	317	319	318	318																				
D5B	FFS	312	312																		1/315	2/315		7/313		
D5C																										
D5D																										
E1A	IND	321	321	314	314	312	312	308	306																	
E1B	FFS	320																								
E1C	A	312	309	306	320	319	307	314																		
E1D	D	311	320	321																						
E2A	A	311	319	318	320	311	307	321																		
E2B	FFS	320	320																							
E2C	FFS	311	313																		1/311					
E2D	G	314	314	306	321																					
E3A	FFS	314	314																							
E3B	DC	302		302	301	301	301		301																	
E3C	C	312	321	321	318	318																				
E3D																										
E4A	FFS	320	306																							
E4B																										
E4C	A	318	311	304	320	312	320	318															4/317			
E4D	A	312	312	312	318	318	319	306																7/313		
E5A	D	312	322	318																						
E5B	FFS	309	310																			1/317	2/315	7/317	14/317	
E5C																										
E5D																										
F1A	IND	315	315	314	314	312	312	313	313	311																
F1B	A	316	313	312	316	311	315	309												(DS)						
F1C	FFS	309	313																	(DS)						
F1D	FFS	309	309																	(DS)						
F2A	DMVB	309		309																(DS)						
F2B	C	316	315	317	311	311														(DS)						
F2C	C	318	315	313	313	313														(DS)						
F2D	A	319	318	309	311	309	319	319																		
F3A	B	322	309	311	311	305	311																			
F3B	FFS	309	304																							
F3C	FFS	321	309																							
F3D	A	319	314	311	321	320	309	309																		
F4A																										
F4B	DMVB	309	316	309																						
F4C	FFS	309	309																		1/315					
F4D																										
F5A	D	321	321	321																(DS)						
F5B	FFS	311	312																	(DS)	1/315					
F5C																										
F5D																										
G1A																										
G1B	A	319	317	311	318	321	315	313												(DS)			4/319	5/317		
G1C	D	315	313	312																(DS)					22/319	
G1D	A	311	315	311	319	314	314	315												(DS)						
G2A	A	314	313	317	319		315	313												(DS)						
G2B	FFS	315	315																	(DS)						
G2C	FFS	315	315																	(DS)						
G2D	B	315	313		315	315	315													(DS)						
G3A	C	312	315	321	315	317														(DS)						
G3B																										
G3C	D	312	313	321																(DS)					22/312	
G3D	DC	302		302	301	301	301		301																	
G4A	FFS	314	314																	(DS)						
G4B	FFS	312	313																	(DS)						
G4C	A	315	315	319	312	313	317	314												(DS)						
G4D	A	319	312	319	314	312	317													(DS)						
G5A																										
G5B																										
G5C																										
G5D																										
LOC CARD	TYPE	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	FEATURE	PIN/PAGE TIE POINTS					

CIRCUIT/PAGE

SOLENOID	NAME	PAGE
L2001	PROG CAM	322
L2002	REV	322
L2003	RETURN	322
L2004	PAPER DRIVE	322
L2005	STOP PAPER DRIVE	322
L2006	CHECK STOP	322

LIGHTS	NAME	PAGE
DS2001	CC1	323
DS2002	CC2	323
DS2003	CC3	323
DS2004	CC4	323
DS2005	CC5	323
DS2006	CC6	323
DS2009	CRG OPEN	323
DS2010	BOL	323
DS2011	FPS	323

DIODES	PAGE
CR2001	322
CR2002	322
CR2003	322
CR2004	322
CR2005	322
CR2006	322
CR2007	322

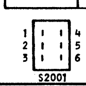
CAPACITORS	PAGE
C2001	322
C3101	306
C3102	316
C3103	316

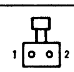
RESISTORS	PAGE
R2001	323
R2002	323
R2003	322
R2004	322
R2005	322
R3101	306
R3102	306
R3103	306
R3104	306
R3105	316
R3106	316
R3107	316
R3108	316
R3109	316
R3110	316
R3111	316
R3112	316
R3113	308

MAGNETIC HEADS	PAGE
PU1	306
PU2	316
PU3 (DS)	316

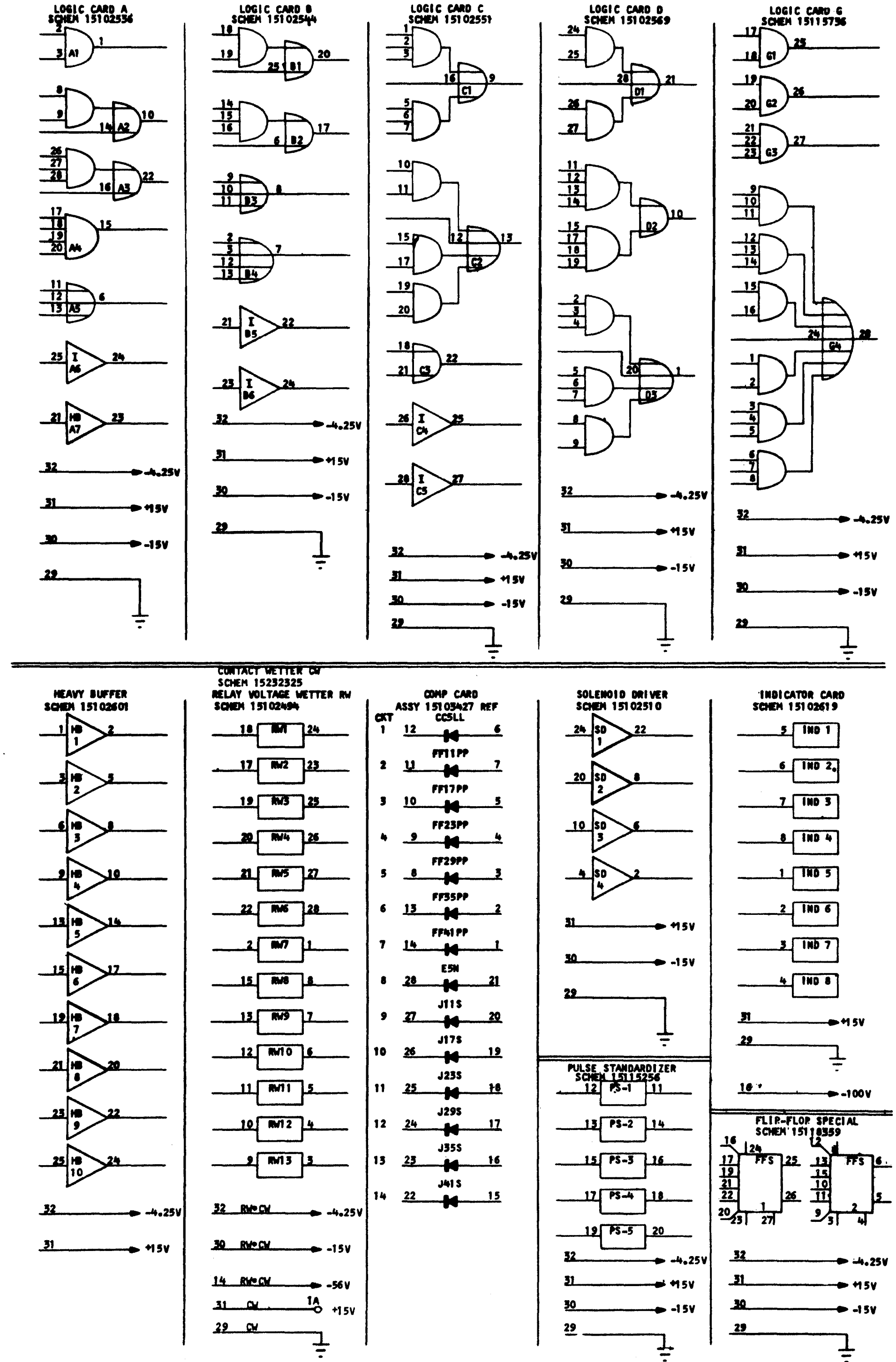
SOLAR CELLS	NAME	PAGE
V2001	CC1	323
V2002	CC2	323
V2003	CC3	323
V2004	CC4	323
V2005	CC5	323
V2006	CC6	323
V2009	CRG OPEN	323
V2010	BOL	323
V2011	FPS	323

SWITCHES	NAME	PAGE
S2001	CHECK STOP FOR. HEADING	306
S3101	CRG MOTOR	304
S3102	PROG CAM	304
S3103	EJECT	320

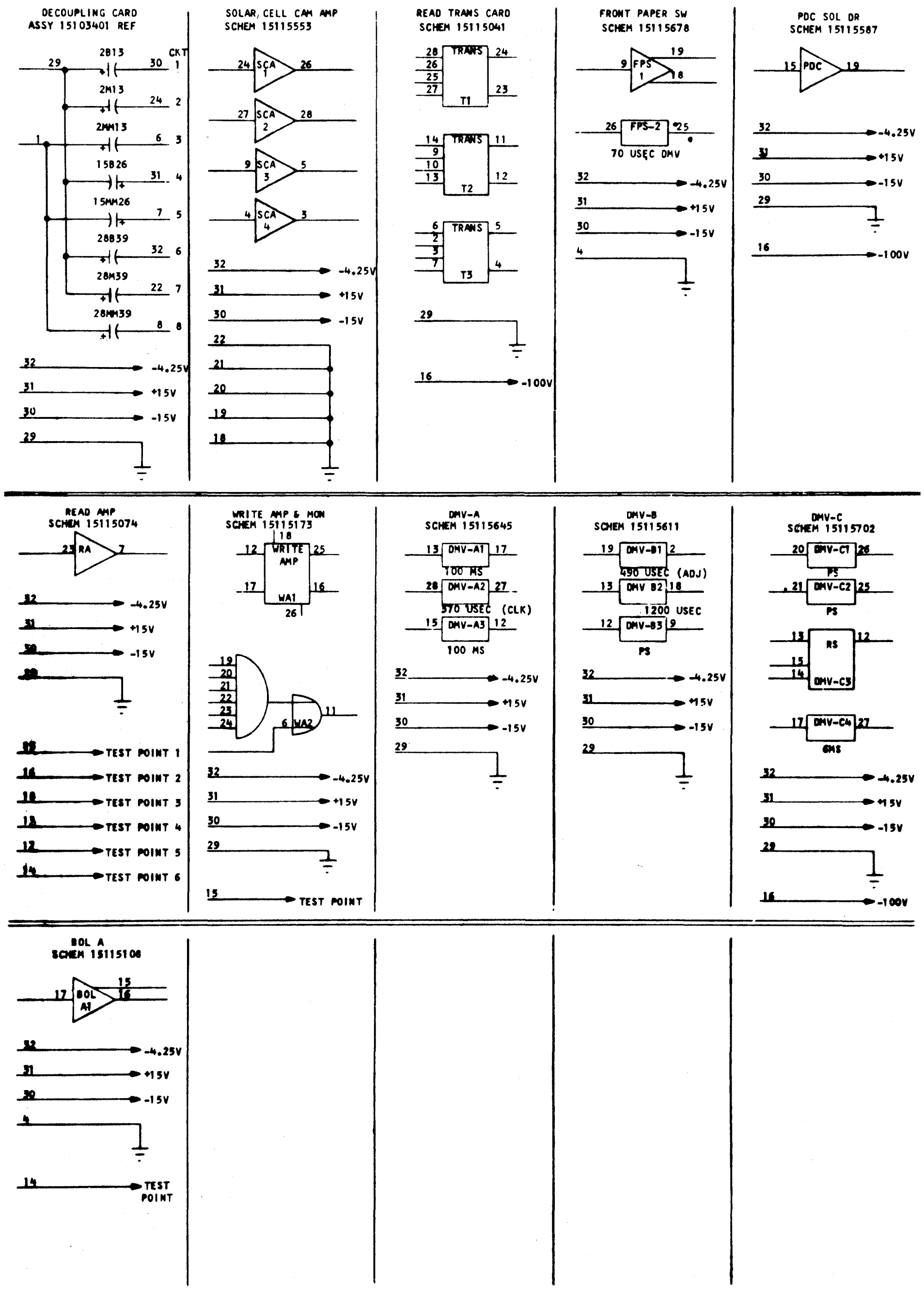




Ref. Page 330



Ref. Page 331


DECOUPLING CARD
ASSY 15103401 REF
SOLAR CELL CAM AMP
SCHEM 15115553
READ TRANS CARD
SCHEM 15115041
FRONT PAPER SW
SCHEM 15115678
PDC SOL DR
SCHEM 15115587
READ AMP
SCHEM 15115074
WRITE AMP & MON
SCHEM 15115173
DMV-A
SCHEM 15115645
DMV-B
SCHEM 15115611
DMV-C
SCHEM 15115702
SOL A
SCHEM 15115108
70 USEC DMV
100 MS
370 USEC (CLK)
490 USEC (ADJ)
1200 USEC
TEST POINT

Ref. Page 332

CONNECTOR INDEX

P603		P60[illegible]		J2001		J2002		J1201		J1202	
PIN	PAGE	PIN	PAGE	PIN	PAGE	PIN	PAGE	PIN	PAGE	PIN	PAGE
1		1	320	A	323	1	323	A	323	A	
2		2	313	B	323	2	303	B	323	B	
3		3	320	C	323	3		C	323	C	
4		4	305	D	323	4	30[illegible]	D	323	D	
5		5	305	E	323	5		E	323	E	
7		7	307	F	323	6	306	F	323	F	
8		8	307	H		7		H		H	
10		10	307	J		8	306	J		J	
11		11		K		9	303	K		K	
12		12	306	L	303	10		L		L	
13		13		M	303	11	303	M		M	
14		14		N		12	323	N		N	
15		15		P	306	13		P	306	P	
16		16		R	306	14	322	R	306	R	
17		17		S	302	15	302	S	302	S	
18		18		T				T		T	
20		20		U				U		U	
21		21		V				V		V	
22		22		W	316			W	316	W	
23		23		X	316			X	316	X	
24		24		Y				Y		Y	
25		25		Z				Z		Z	
26		26		a	303			a	303	a	
27		27		b				b		b	
28		28		c	316			c	316	c	
29		29		d	316			d	316	d	
30		30		e	303			f	323	f	
31		31		f	323			g	303	g	
32		32		h	323			h	323	h	
33		33		j	303			i		i	
34		34		k	303			j	303	j	
35		35		m	303			k	303	k	
36		36		n	301			m		m	
37		37		p	302			n		n	
38		38		r	302			p		p	
39		39		s	322			q		q	
40		40		t	322			r		r	
41		41		u	322			s	305	s	
42	313	42	307	v	322			t	305	t	
43	320	43	304	w	322			u	304	u	321
44	305	44		x	322			v	305	v	309
45	307	45		y	322			w	305	w	304
46		46		z				x		x	304
47	307	47		AA	322			y		y	316
48		48		BB	323			z		z	
49	307	49		CC	306			AA	307	AA	
50	322	50		DD	306			AB	306	AB	
51	322	51		EE				AC	306	AC	
52	322	52	322	FF	303			AD		AD	
53	322	53	322	HH				AE	323	AE	
54	320	54	322					AF	303	AF	
55		55	322					AH		AH	
56		56						AJ		AJ	319
57	307	57						AK		AK	316
58	304	58						AL		AL	
59	305	59						AM		AM	
60	306	60						AN		AN	
62		62						AP		AP	
63		63						AR		AR	
64		64						AS		AS	
65		65						AT		AT	
66		66						AU		AU	
67		67						AV		AV	
70		70	301					AW		AW	
71		71	301					AX		AX	321
72		72						AY		AY	304
73		73						AZ		AZ	
74		74						BA		BA	
75		75						BB		BB	
76		76						BC		BC	
77		77						BD		BD	
78		78	302					BE		BE	
79		79						BF		BF	
80		80						BH		BH	
82		82						BJ		BJ	
								BK		BK	
								BL		BL	
								BM		BM	

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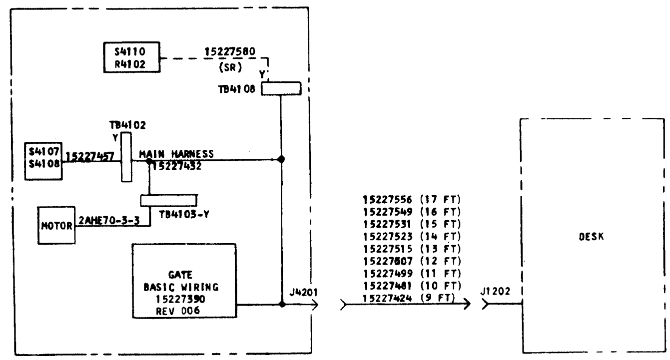
TERMINAL BOARD INDEX

TB2001		TB2002		TB2003		TB2004		TB3101															
TERM	PAGE	TERM	PAGE	TERM	PAGE	TERM	PAGE	TERM	PAGE	TERM	PAGE	TERM	PAGE	TERM	PAGE	TERM	PAGE	TERM	PAGE	TERM	PAGE	TERM	PAGE
X1	323	X1	316	1	323	1	303	A1	306														
X2	303	X2	316	2	323	2	323	A2	306														
X3	303	X3	316	3	323	3		A3	306														
X4	323	X4	316	4	323	4		A4	306														
X5	303	X5	303	5	323			A5	306														
X6	302	X6	303	6	323			A6	316														
X7	302	X7	303					A7	316														
X8	302	X8	303					A8	316														
X9	322	X9	306					A9	316														
X10	322	X10	306					A10	316														
X11	322	X11						A11	316														
X12	322	X12	301					A12	316														
X13	322	X13	302					A13	316														
X14	322	X14	323					A14	316														
X15	322	X15	323					A15	316														
X16	302	X16	303					A16															
X17	302	X17	303					A17															
X18		X18	303					A18	308														
X19		X19	303																				
X20	303	X20	323					B1	306														
X21	322	X21	323					B2	306														
X22	323	X22	323					B3	306														
X23	323	X23	302					B4	306														
X24		X24	306					B5	306														
X25		X25	306					B6	316														
X26	322	X26	322					B7	316														
Y1	323	Y1	316					B8	316														
Y2	303	Y2	316					B9	316														
Y3	303	Y3	316					B10	316														
Y4	323	Y4	316					B11	316														
Y5	303	Y5	303					B12	316														
Y6	302	Y6	303					B13	316														
Y7	302	Y7	303					B14	316														
Y8	302	Y8	303					B15	316														
Y9	322	Y9	306					B16															
Y10	322	Y10	306					B17															
Y11	322	Y11						B18	308														
Y12	322	Y12	301																				
Y13	322	Y13	302																				
Y14	322	Y14	323																				
Y15	322	Y15	323																				
Y16	302	Y16	303																				
Y17	302	Y17	303																				
Y18	323	Y18	303																				
Y19		Y19	303																				
Y20	303	Y20	323																				
Y21	322	Y21	323																				
Y22	323	Y22	323																				
Y23	323	Y23	302																				
Y24		Y24	306																				
Y25		Y25	306																				
Y26	322	Y26	322																				

Ref. Page 334

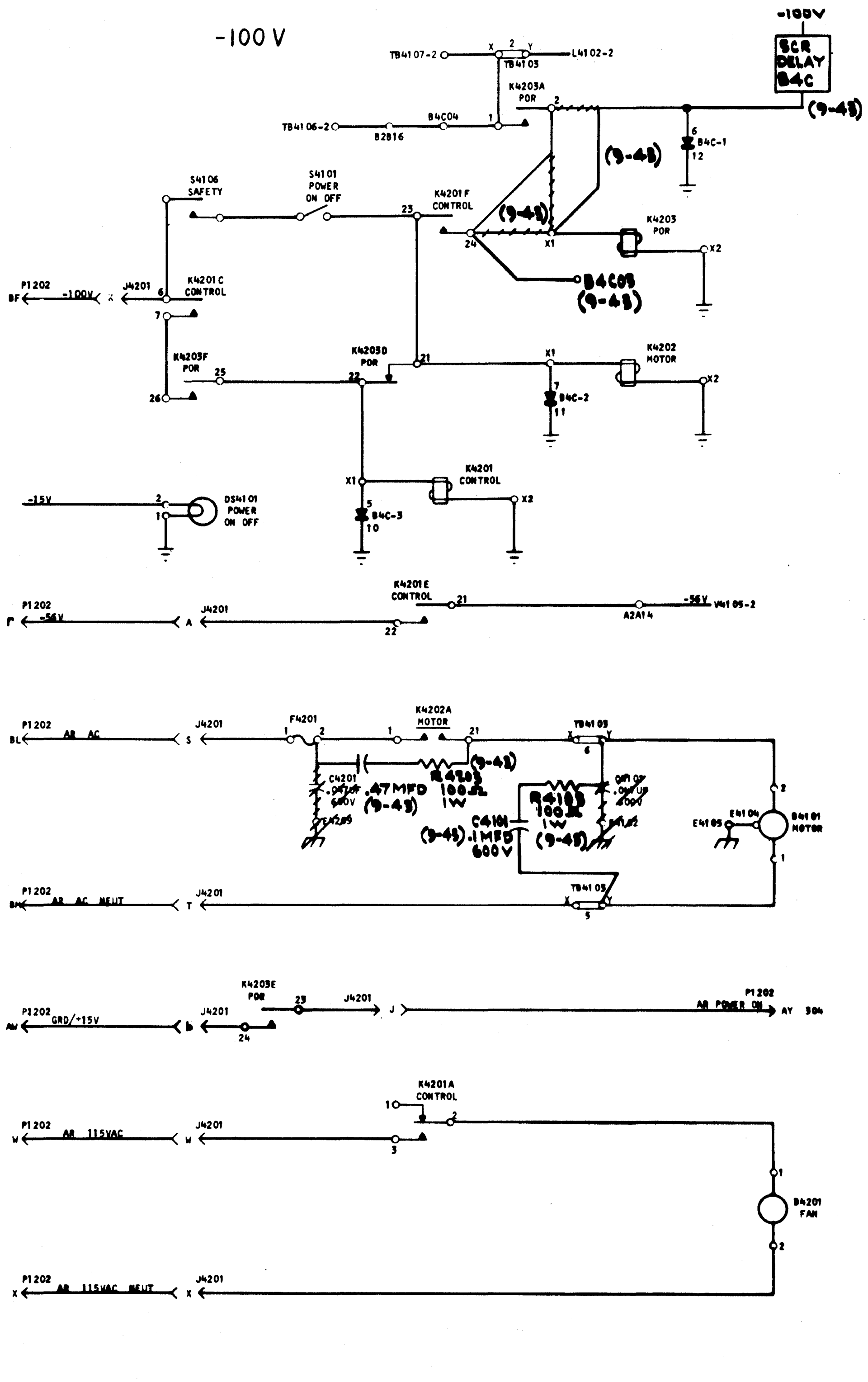


PAGE	DESCRIPTION	ER DATE	REV LETTER
350	AUTOREADER INDEX	10-23-65	E
351	RELAYS, VOLTAGE CONTROL	7-16-65	D
352	ROUTING +15V, GRD -4.25V, -15V,POR; -4.25V & +15V LAMP VOLTAGES	10-23-65	E
353	CLK, AFFF & SFFF	10-23-65	E
354	C1FF, C2FF, CCFF, RSTAFF, I ON, DROP I, DDCLR	10-23-65	E
355	STOPFF & DDFF, INDICATOR LIGHTS	4-22-65	C
356	DROP I, FEED, TABLE ELEV. SOLS & READ AMPS	10-23-65	E
357	SELECTIVE READING FEATURE	11-6-64	A
358	CARD LOCATION & TIE POINT CHART, COMPONENTS	10-23-65	F
359	CARD ELEMENTS & COMPONENTS	11-6-64	A

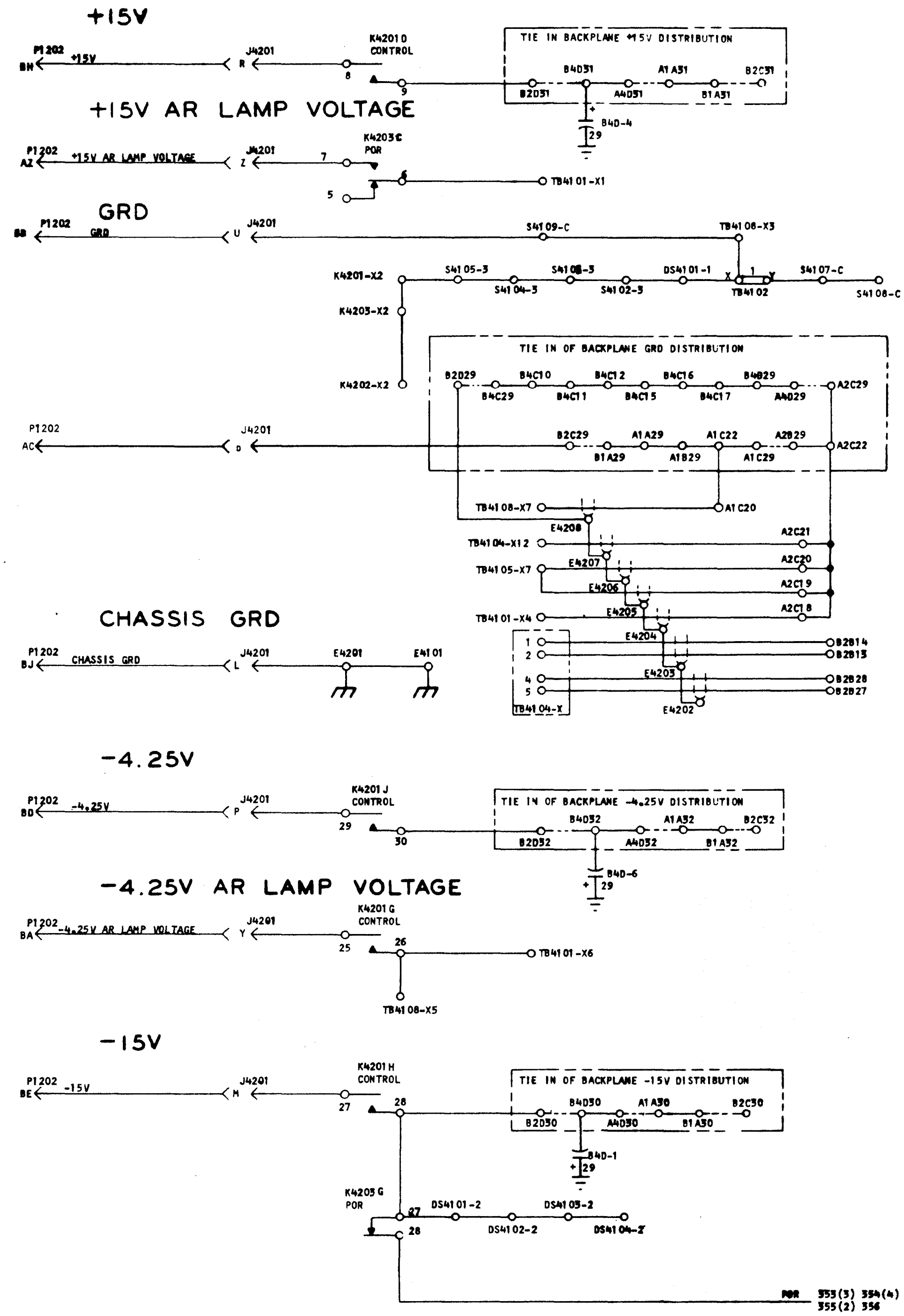
NOTES:

1. STANDARD CONSTRUCTION HANDLES SINGLE & DUAL STRIPE FORMS.
2. PAGE NUMBER ON INPUT SIGNALS INDICATE PAGE OF ORIGIN.
3. ALL ELEMENT PINS (OTHER THAN VOLTAGE) ARE SHOWN EXCEPT ON FF ELEMENTS. PINS 1[illegible], 15, 19 & 21, IF SHOWN ON FF ELEMENTS, ARE CLOCK INPUTS. ALL ELEMENT PINS SHOWN WITHOUT SIGNAL ARE NOT WIRED.
4. WHEN PAGE NUMBER DOES NOT APPEAR ON INPUT OR OUTPUT, REFER TO SIGNAL INDEX CHART ON UPPER GATE SCHEMATIC TO DETERMINE WHERE SIGNALS ENTER OR LEAVE.
5. PAGES 300 THRU 349 DESIGNATE A & M LOWER GATE SCHEMATIC 15118300.
6. (SR) INDICATES SELECTIVE READING FEATURE.
7. WIRING SHOWN IN DASHED LINES (-) INDICATES OPTIONAL FEATURES.
8. CHARACTERS IN PARENTHESES ON FEATURE WIRING INDICATE NAME OF OPTIONAL FEATURE REQUIRING THAT WIRING.
9. CHARACTERS IN PARENTHESES LOCATED NEAR CARD ELEMENTS OR COMPONENTS, INDICATE NAME OF OPTIONAL FEATURE REQUIRING THAT CARD OR COMPONENT.

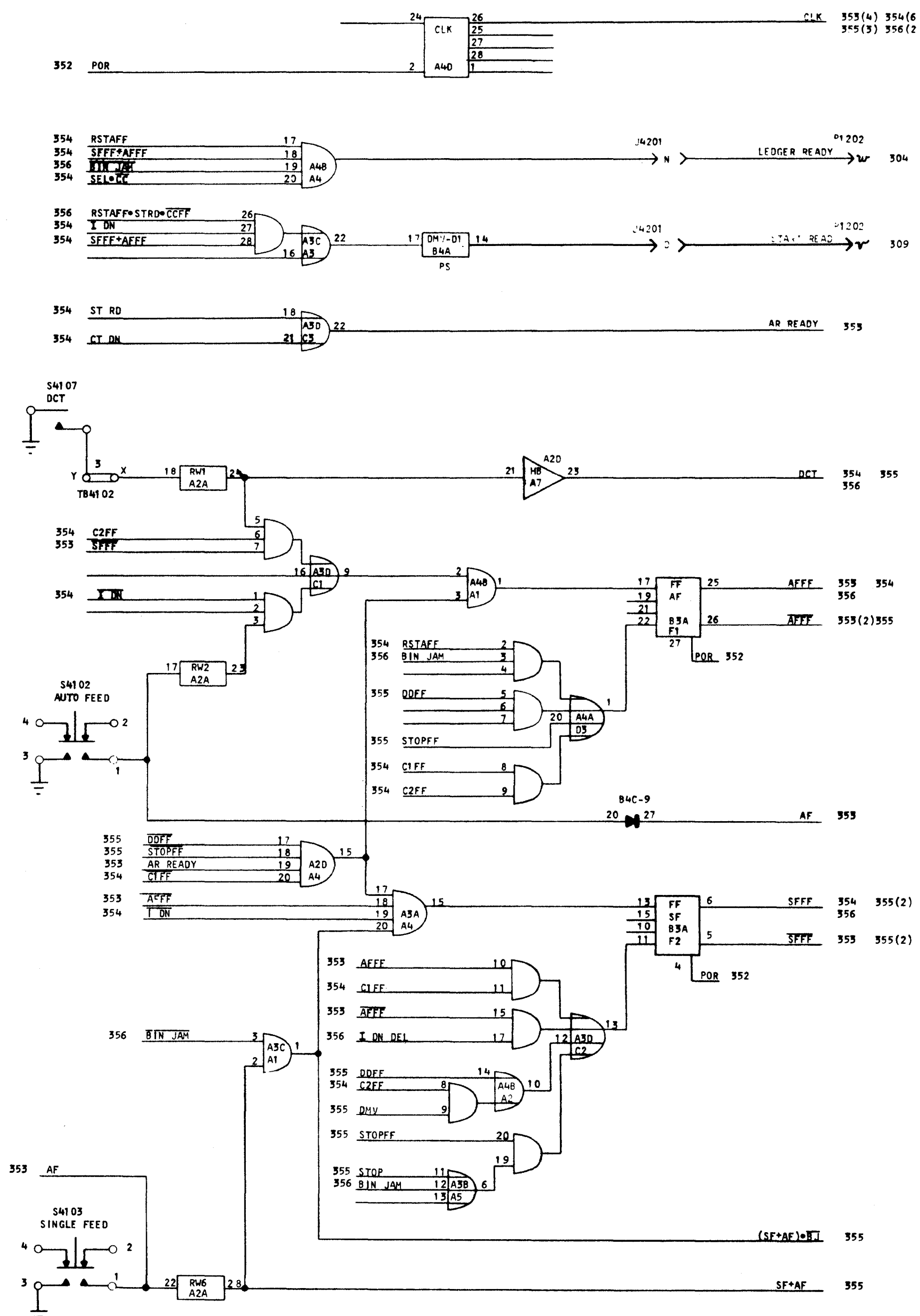
Ref. Page 350



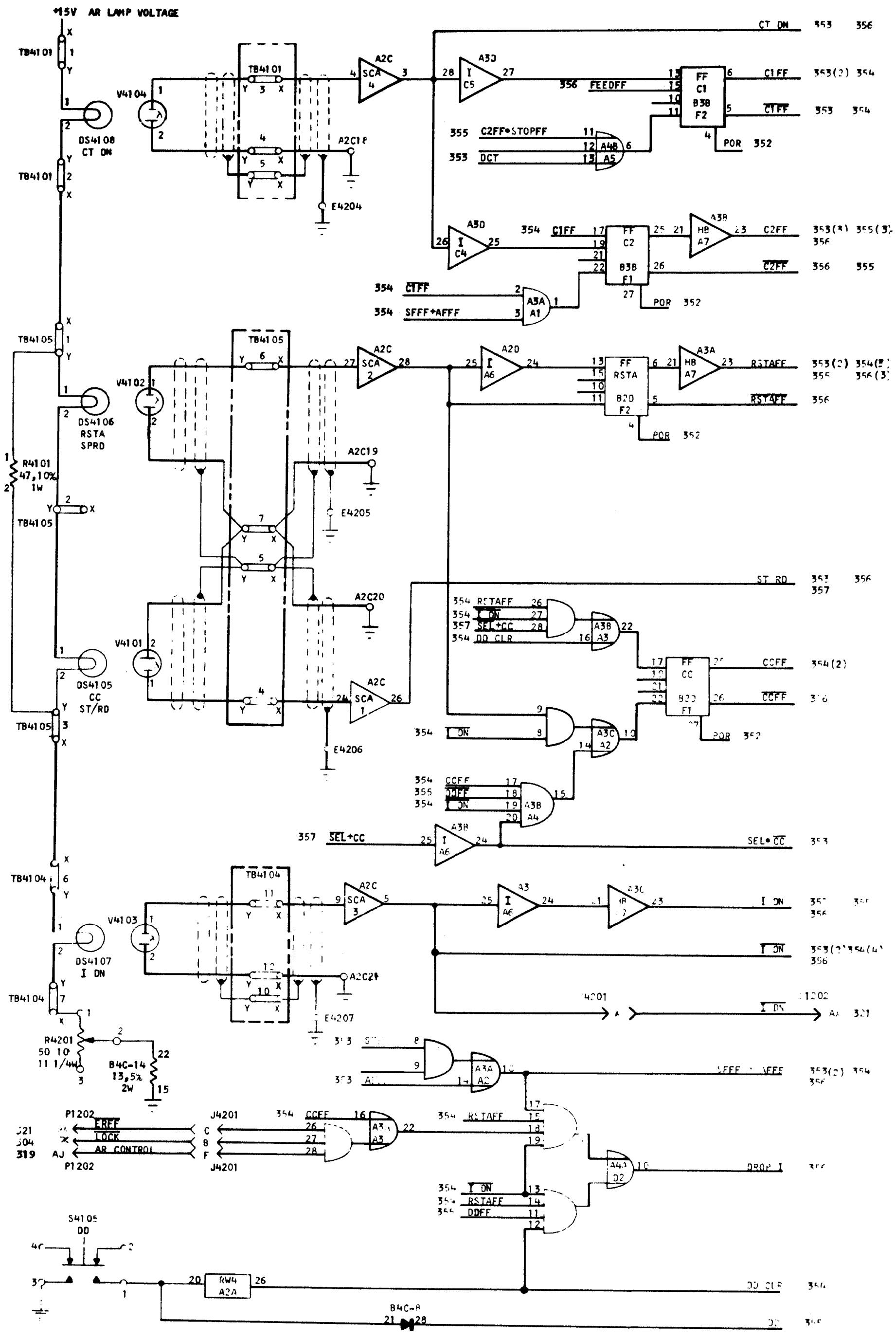
Ref. Page 351


+15V
+15V AR LAMP VOLTAGE
GRD
CHASSIS GRD
-4.25V
-4.25V AR LAMP VOLTAGE
-15V
TIE IN BACKPLANE +15V DISTRIBUTION
TIE IN OF BACKPLANE GRD DISTRIBUTION
TIE IN OF BACKPLANE -4.25V DISTRIBUTION
TIE IN OF BACKPLANE -15V DISTRIBUTION

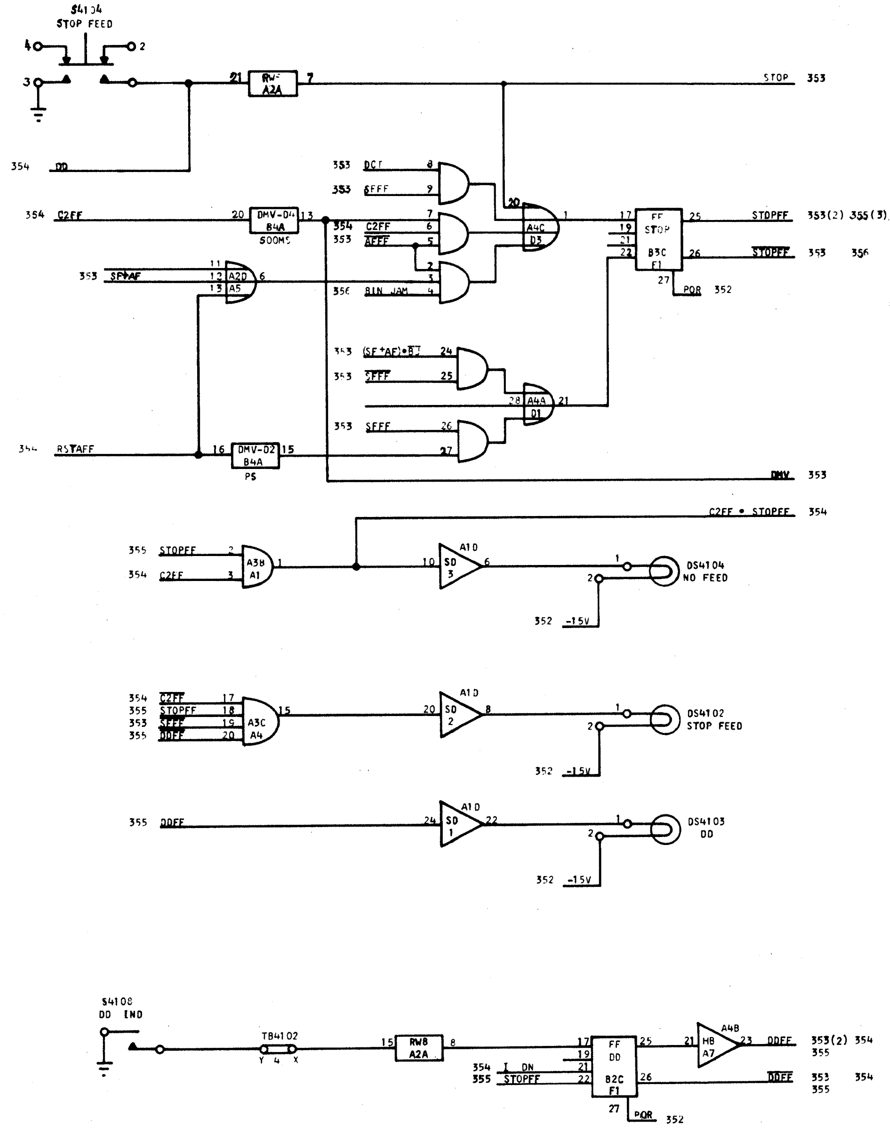
Ref. Page 352



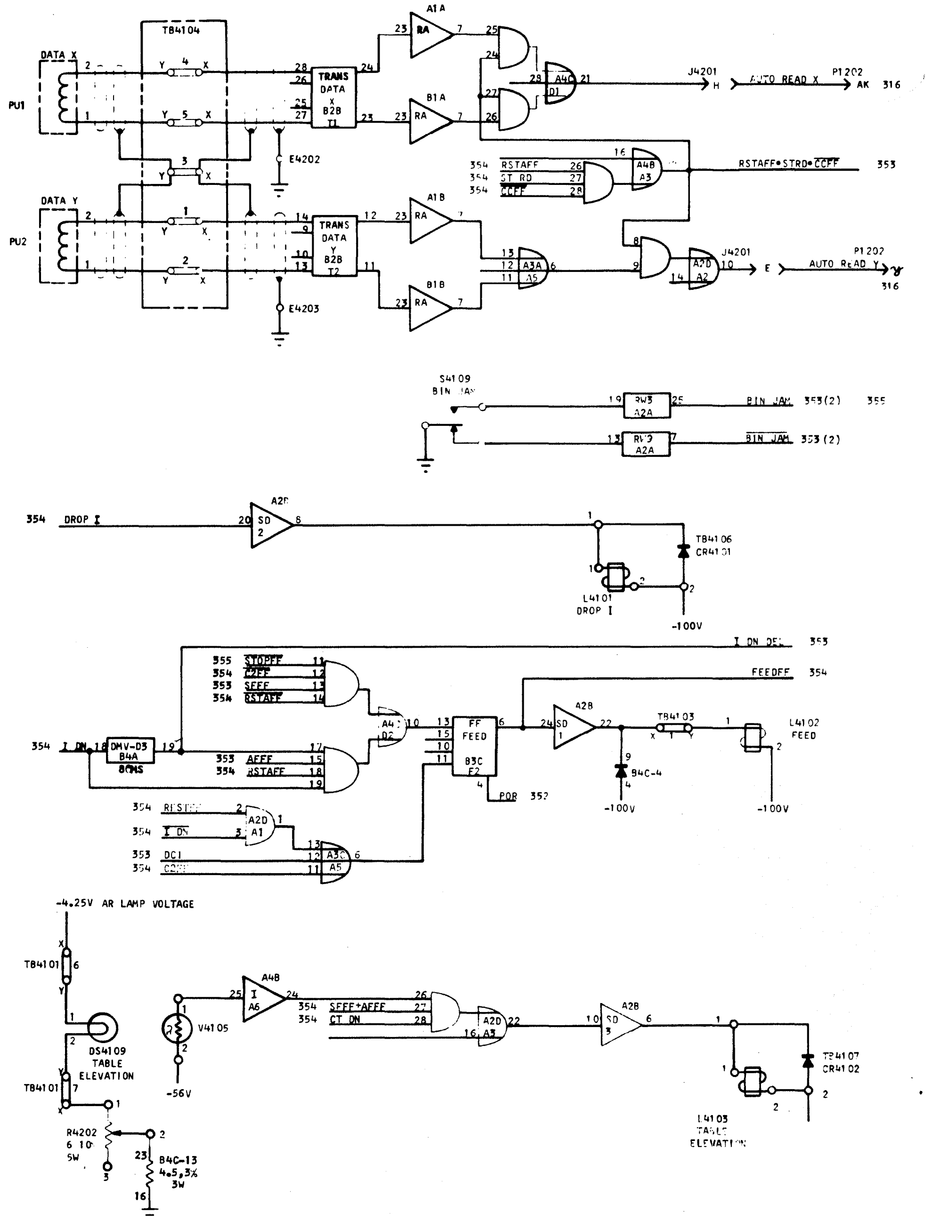
Ref. Page 353



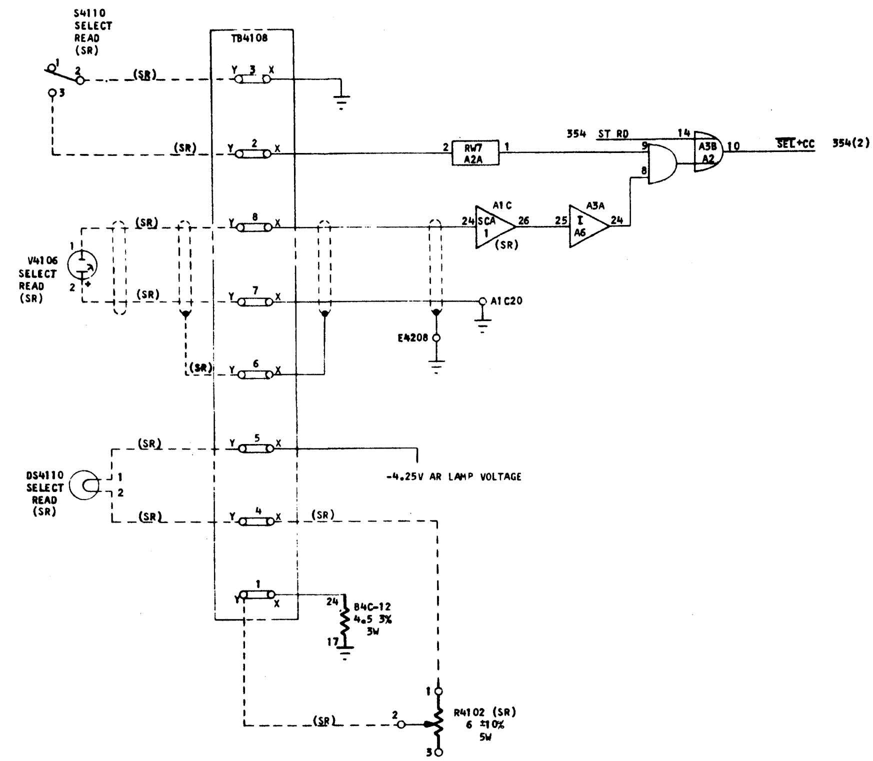
Ref. Page 354


S4104
STOP FEED
STOP 353
STOPFF 353(2) 355(3)
POR 352
DMV 353
C2FF • STOPFF 354
DS4104
NO FEED
DS4102
STOP FEED
DS4103
DD
S4108
DD END
TB4102
DDFF 353(2) 354 355

Ref. Page 355

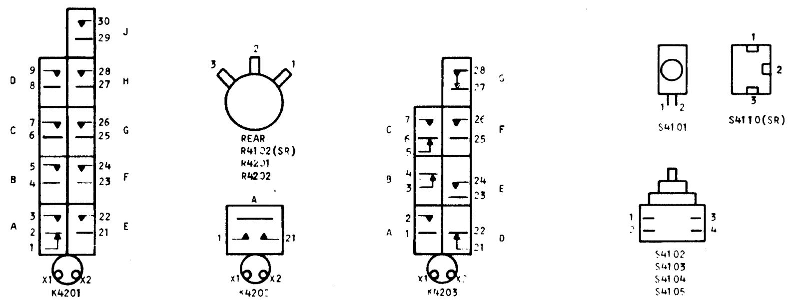

TB4104
DATA X
PU1
DATA Y
PU2
TRANS DATA X B2B
TRANS DATA Y B2B
E4202
E4203
A1A
B1A
A1B
B1B
J4201
AUTO READ X
P1202
AK 316
RSTAFF•STRD•CCFF
353
RSTAFF
ST RD
CCFF
AUTO READ Y
S4109
BIN JAM
353 (2)
DROP I
TB4106
CR4101
L4101
DROP I
-100V
I DN DEL
FEEDFF
STOPFF
SFFF
DMV-D3
B4A
AFFF
FF FEED
B3C
POR
TB4103
L4102
FEED
B4C-4
-4.25V AR LAMP VOLTAGE
TB4101
DS4109
TABLE ELEVATION
R4202
B4C-13
V4105
-56V
SFFF+AFFF
CT DN
CR4102
L4103

Ref. Page 356


S4110
SELECT
READ
(SR)
TB4108
354 ST RD
RW7
A2A
A3B
A2
SEL+CC 354(2)
A1C
SCA
A3A
A6
V4106
SELECT
READ
(SR)
A1C20
E4208
-4.25V AR LAMP VOLTAGE
DS4110
SELECT
READ
(SR)
B4C-12
4.5 3%
5W
R4102 (SR)
6 ±10%
5W

Ref. Page 357

CARD LOC	CARD TYPE	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	FEATURE	TIE POINTS PIN/PAGE
A1A	RA	356																			
A1B	RA	356																			
A1C	SCA	357																		(SR)	
A1D	SD	355	355	355																	
A2A	RW	353	353	356	354	355	353	357	355	356											
A2B	SD	356	356	356																	
A2C	SCA	354	354	354	354																
A2D	A	356	356	356	353	355	354	353													
A3A	A	354	354	354	353	356	357	354													
A3B	A	355	357	354	354	353	354	354													
A3C	A	353	354	353	355	356	354	354													
A3D	C	353	353	353	354	354															
A4A	D	355	354	353																	
A4B	A	353	353	356	353	354	356	355													
A4C	D	356	356	355																	
A4D	CLK	353																			
B1A	RA	356																			
B1B	RA	356																			
B1C																					
B1D																					
B2A																					
B2B	TRAN	356	356																		
B2C	FF	355																			
B2D	FF	354	354																		
B3A	FF	353	353																		
B3B	FF	354	354																		
B3C	FF	355	356																		
B3D																					
B4A	DMVD	353	355	356	355																
B4B																					
B4C	COMP	351	351	351	356				354	353			357	356	354						
B4D	DC	352			352		352														



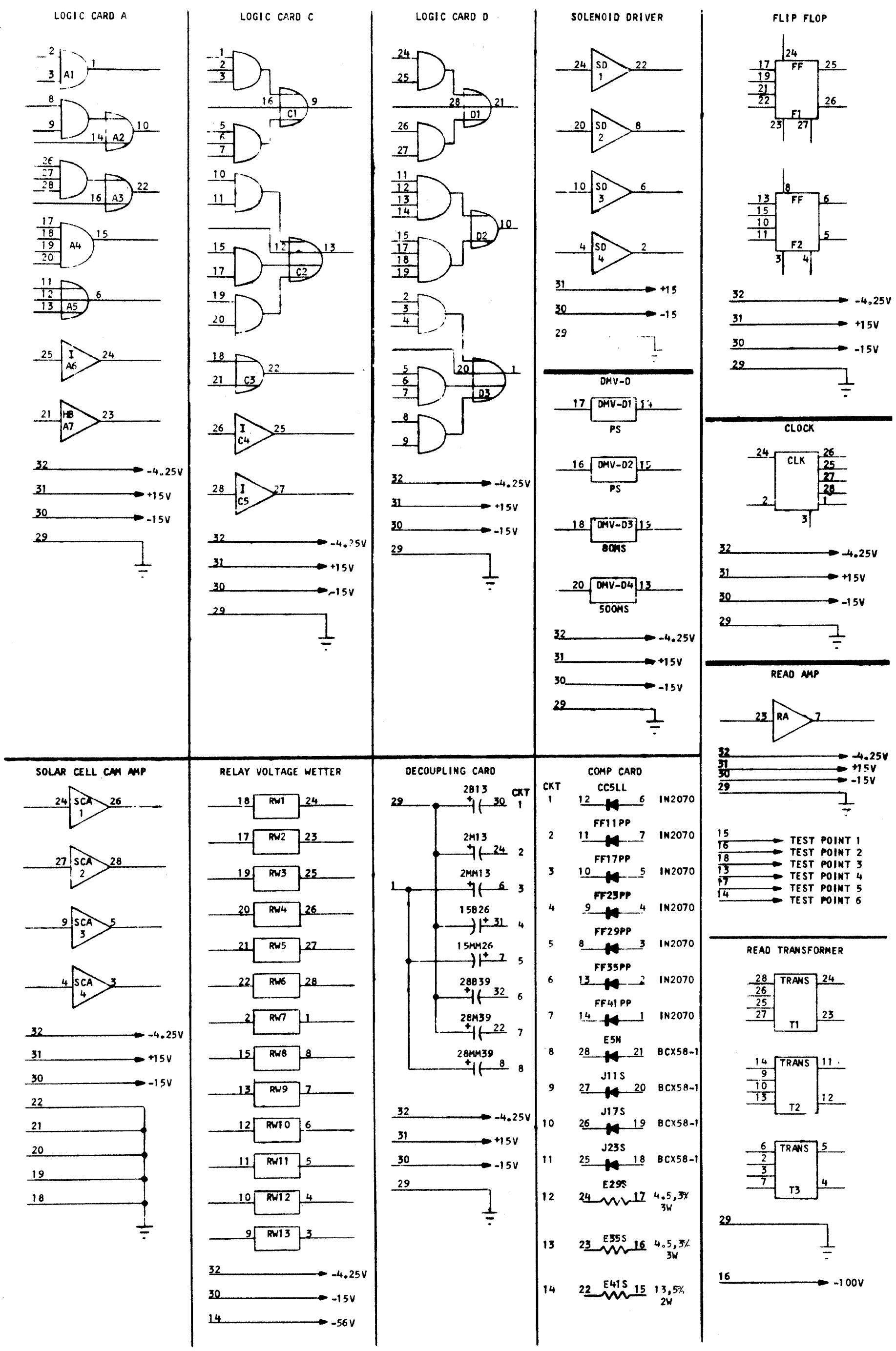
RELAYS	NAME	PAGE COIL	A	B	C	D	E	F	G	H	J
K4201	CONTROL	351	351		351	352	351	351	352	352	352
K4202	MOTOR	351	351								
K4203	POR	351	351	352	352	351	351	351	352		

SWITCHES	NAME	PAGE
S4101	POWER ON-OFF	351
S4102	AUTO FEED	353
S4103	SINGLE FEED	353
S4104	STOP FEED	355
S4105	DD	354
S4106	SAFETY	351
S4107	DCT	353
S4108	DD IND	355
S4109	BIN JAM	356
S4110(SR)	SELECT READ	357

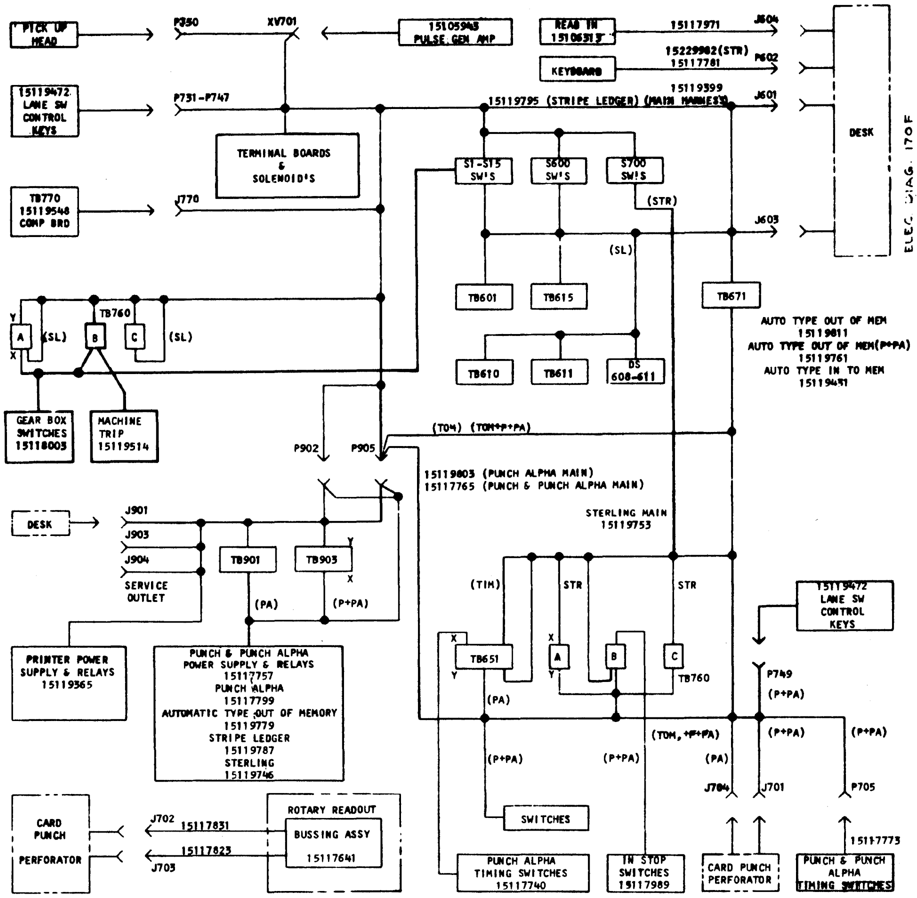
RESISTORS	PAGE
R4101	354
R4102(SR)	357
R4201	354
R4202	356

CAPACITORS	PAGE
C4101	351
C4201	351

Ref. Page 358


LOGIC CARD A
LOGIC CARD C
LOGIC CARD D
SOLENOID DRIVER
FLIP FLOP
DMV-D
CLOCK
READ AMP
SOLAR CELL CAM AMP
RELAY VOLTAGE WETTER
DECOUPLING CARD
COMP CARD
READ TRANSFORMER
TEST POINT 1
TEST POINT 2
TEST POINT 3
TEST POINT 4
TEST POINT 5
TEST POINT 6
-4.25V
+15V
-15V
-56V
-100V

Ref. Page 359



PAGE	DESCRIPTION	ER DATE	REV LETTER
501	PRINTER INDEX	7-14-65	K
502	AC INPUT AND DC VOLTAGE ROUTING	7-14-65	K
503	GROUND ROUTING AND LANES 31 THRU 33	7-16-65	E
504	LANE COMM, MANUAL KEYS, MANUAL RELAY, MODE RELAY AND LANES 34 THRU 36	9-27-65	H
505	LANES 37 THRU 44		
506	LANES 45 THRU 48 AND RE KEY		
507	LANES 51 THRU 55, 57, 59, 61, 63, 65, 66, CLEAR MEMORY KEY AND DECIMAL LIGHTS	5-24-65	G
508	LOCK RY, LANE 3, SRR, ALL TOTAL, PG AMP, RED RIBBON, RACK STOP COILS, AND AEC DELAY	7-16-65	E
509	PRINTER CONTROLS	9-27-65	H
510	TYPEWRITER CONTROLS	7-14-65	K
511	TYPE IN AND OUT OF MEMORY *	7-14-65	K
512	MEMORY ADDRESS, KYBD SWITCHES, TIMING CAM 4, 5, 9, MB3, AEC TAB, STERLING INTLK	3-1-65	C
513	STRIPE LEDGER, PRINT ALARM AND MEMORY ADDRESS	7-16-65	E
514	PUNCH ALPHA FEATURE WIRING AND TOM RELAYS	1-20-65	
515	PUNCH AND PUNCH ALPHA FEATURE WIRING	12-22-64	
516	NOT USED		
517	NOT USED		
518	KEYBOARD CONSTRUCTION FOR STANDARD AND STERLING FARTHING	2-22-65	B
519	KEYBOARD CONSTRUCTION FOR STERLING DECIMAL PENNY AND WHOLE PENNY	2-22-65	B
520	COMPONENT LISTING	7-14-65	K
521	RELAY CONFIGURATION AND SIGNAL ROUTING	7-14-65	K
522	CONNECTOR AND TERMINAL BOARD INDEX	9-27-65	H

NOTES:

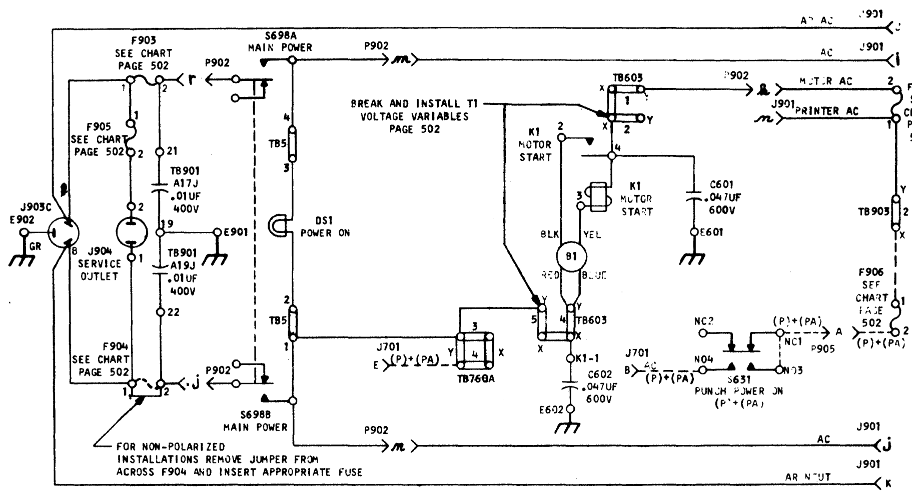
1. WIRING SHOWN IN DASHED LINES INDICATES FEATURES (-----)
2. DESK WIRING SHOWN IN PHANTOM LINES FOR REF PURPOSE ONLY (—— - - ——)
3. * INDICATES SOURCE OF SIGNAL
4. PAGE NUMBERS ON INPUT SIGNALS INDICATE PAGE OR ORIGIN
5. WHEN PAGE NUMBER DOES NOT APPEAR ON INPUT OR OUTPUT REFER TO CONNECTOR INDEX CHART ON APPLICABLE SCHEMATIC TO DETERMINE WHERE SIGNALS ENTER OR LEAVE.

OPTIONAL FEATURES ABBREVIATIONS

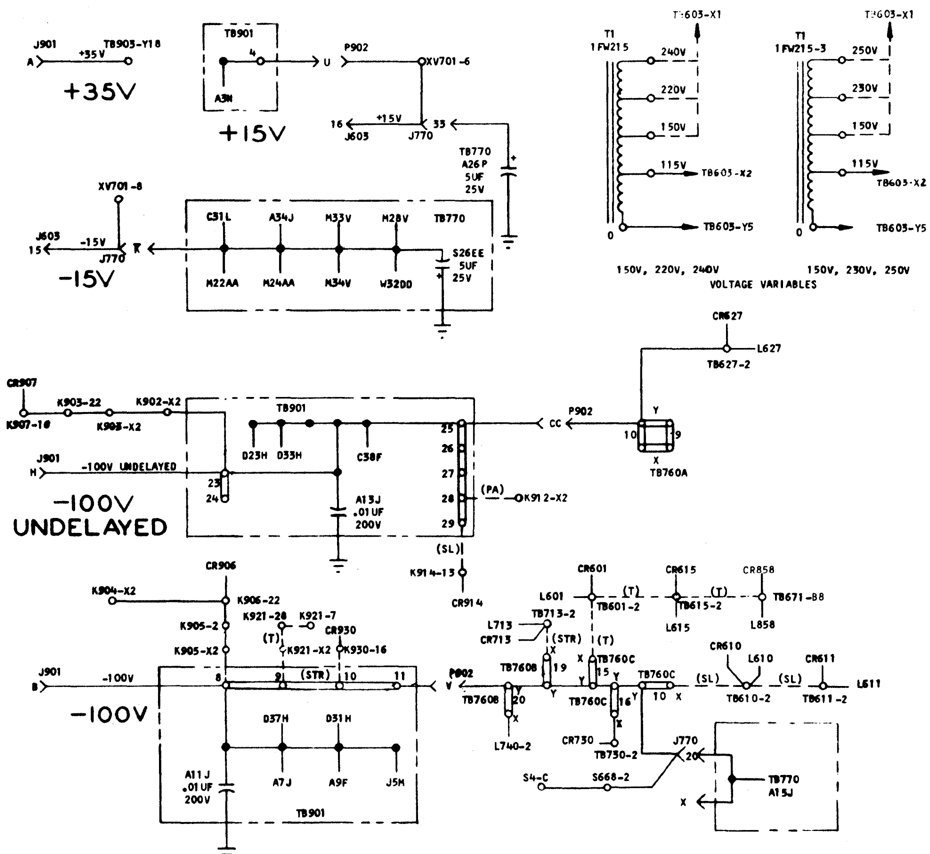
(PA) INDICATES PUNCH ALPHA
(P+PA) INDICATES PUNCH AND PUNCH ALPHA
(STR) INDICATES STERLING
(T) INDICATES TYPE IN & OUT OF MEMORY
(SL) INDICATES STRIPE LEDGER
(F) INDICATES FARTHING

UNLESS OTHERWISE SPECIFIED:
ALL DIODES ARE IN270
ALL RESISTANCES ARE IN OHMS

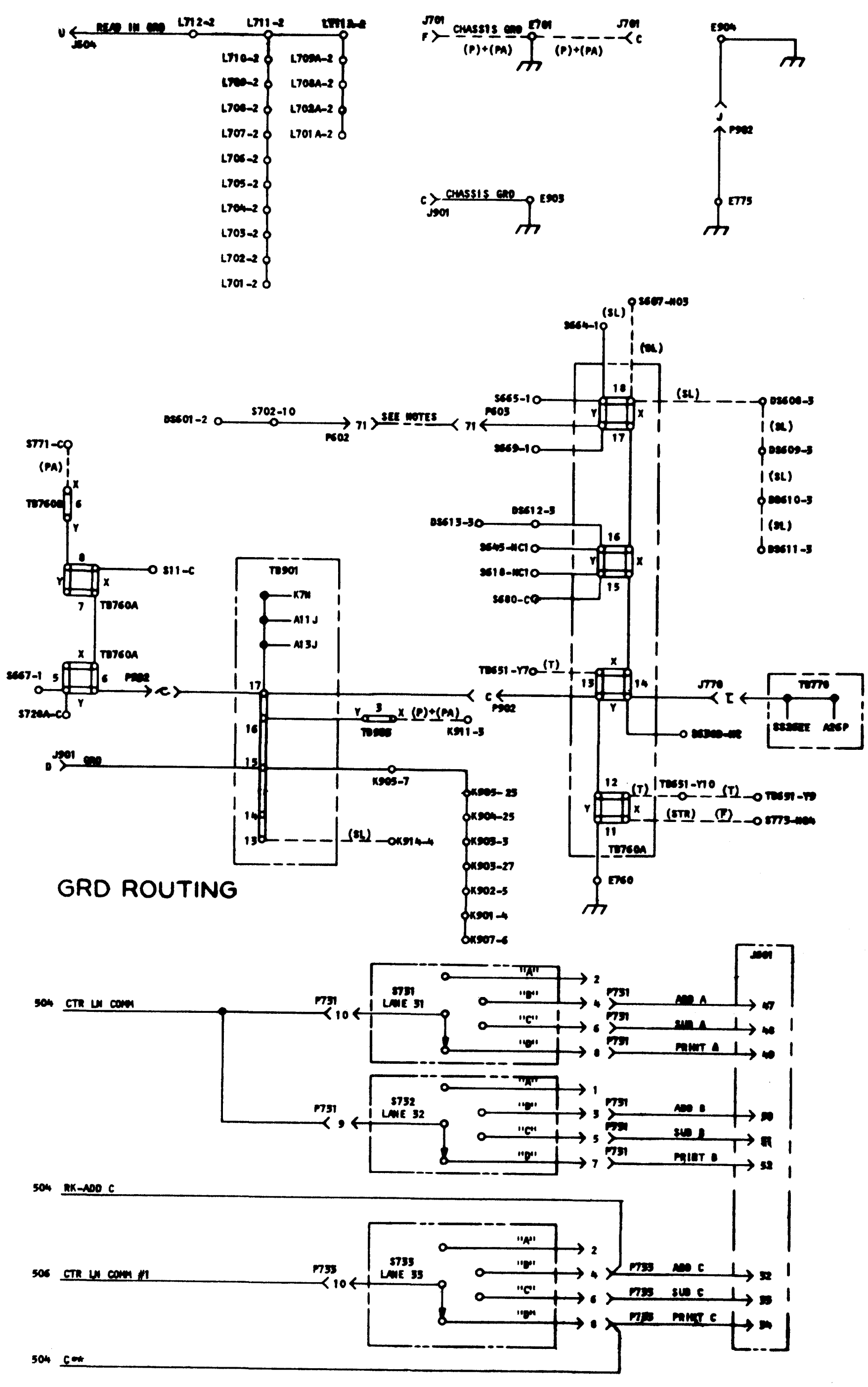
Ref. Page 501



LINE VOLTAGE	F901	F903	F904	F905	F906	DS1
120	3.2A 125V	8.0A SB 250V	8.0A SB 250V	7A SB 125V	1.5A SB 125V	1FX417
150	2A 250V	6.25A SB 250V	6.25A SB 250V	2A 250V	1.25A SB 250V	1FX48-4
220-250	2A 250V	6.25A SB 250V	6.25A SB 250V	2A 250V	0.8A SB 250V	1FX48-4

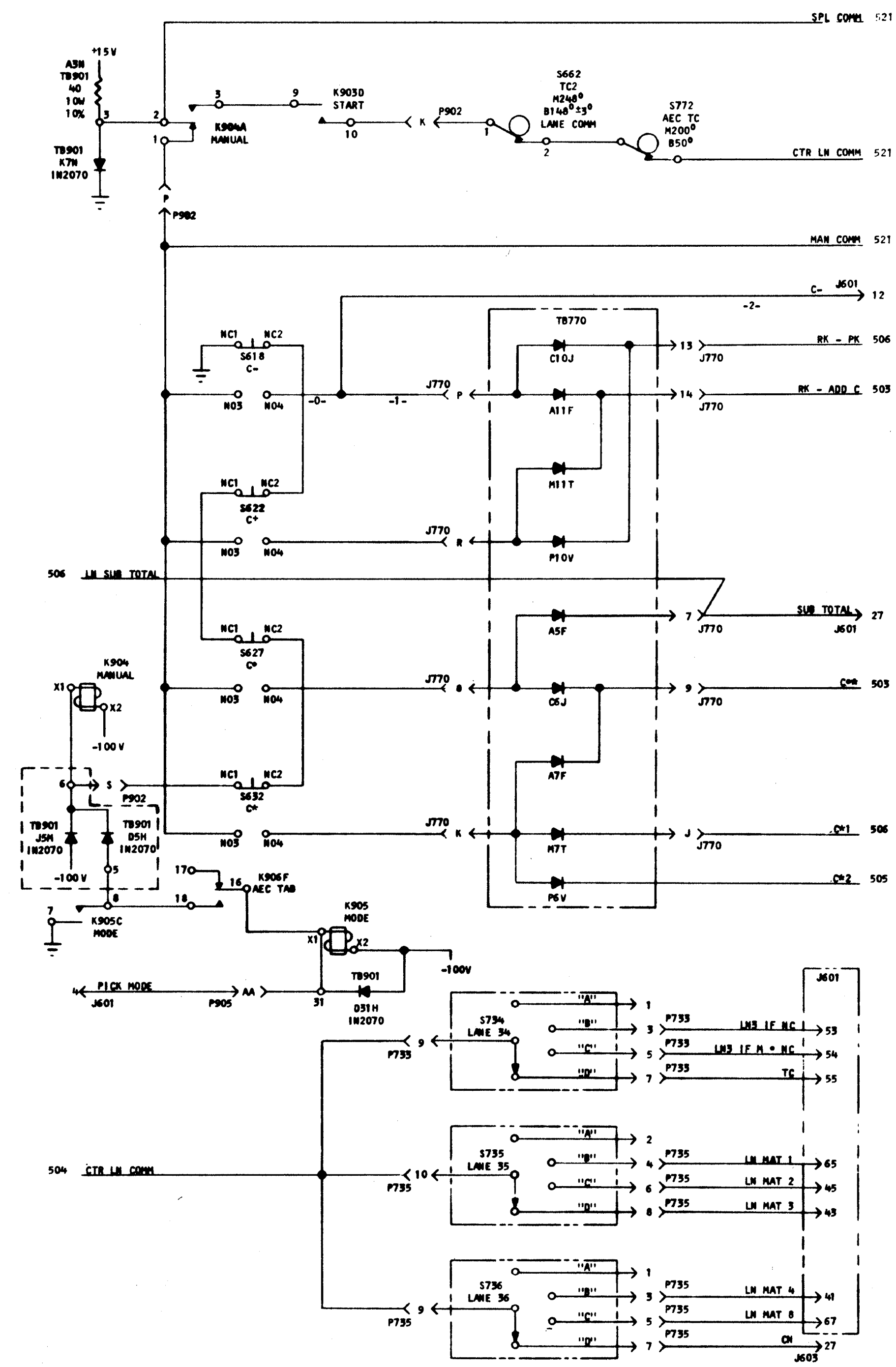


Ref. Page 502

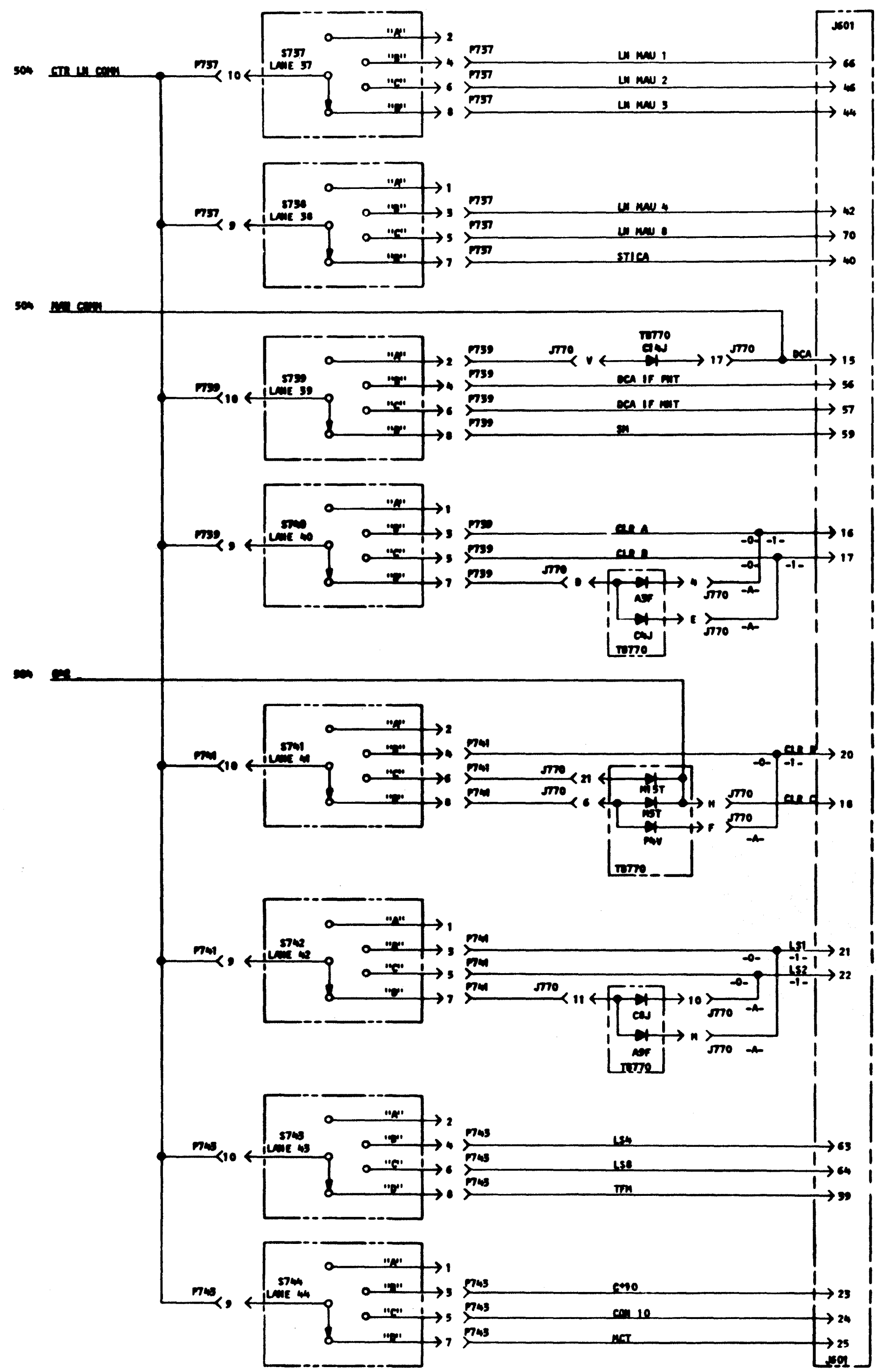


GRD ROUTING

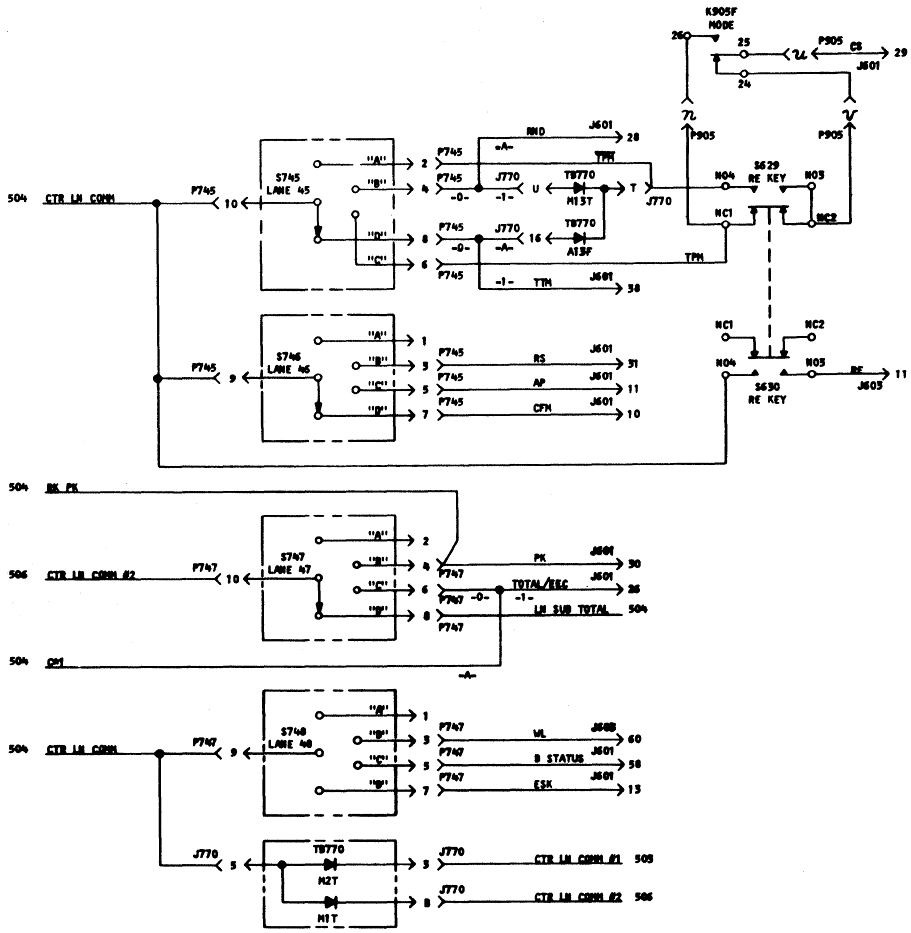
Ref. Page 503



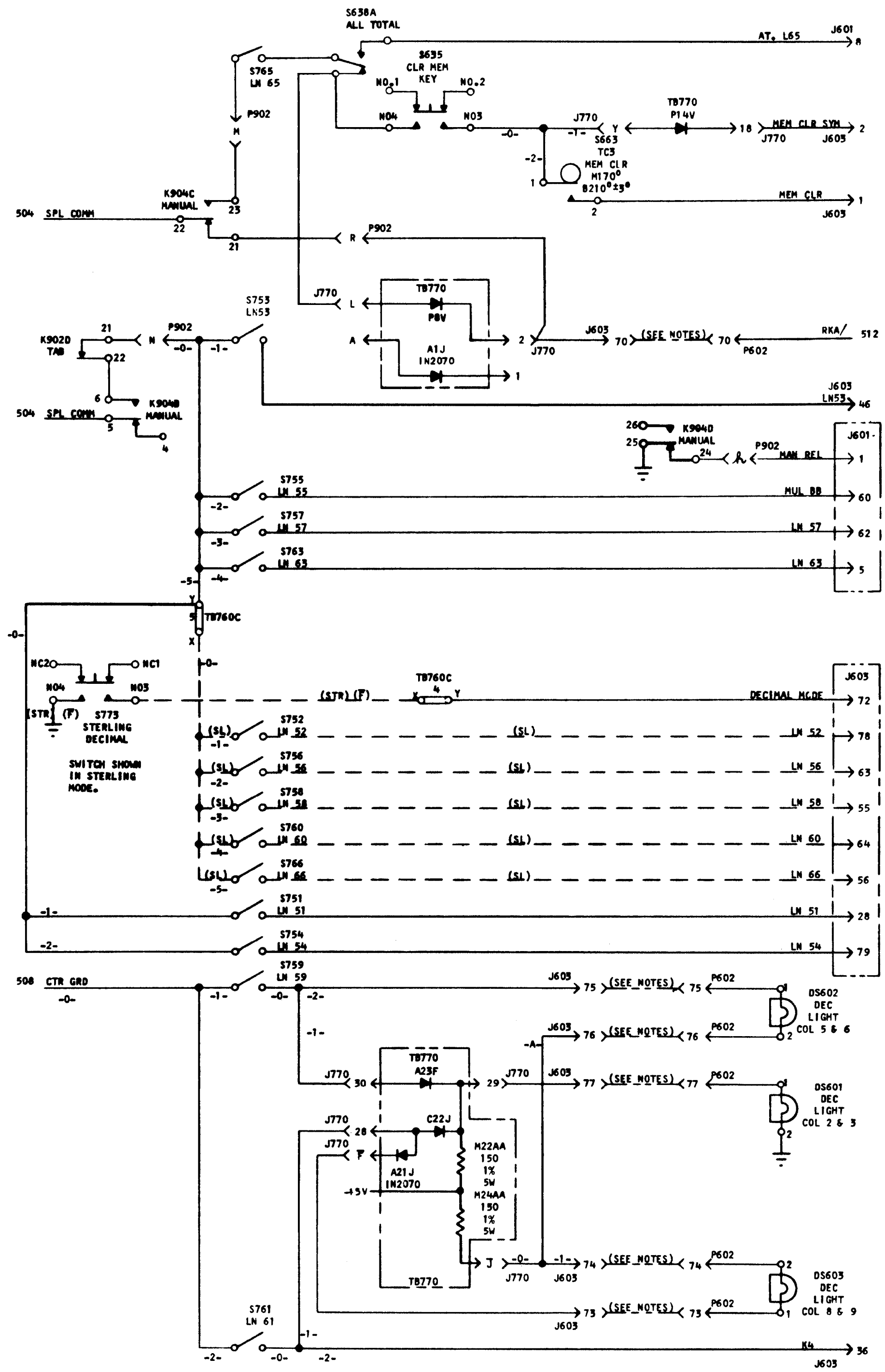
Ref. Page 504


J601
504 CTR LN COMM
S737
LANE 37
P737
LN MAU 1
LN MAU 2
LN MAU 3
S738
LANE 38
LN MAU 4
LN MAU 8
STICA
504 MAN COMM
S739
LANE 39
P739
J770
TB770
DCA
DCA IF PNT
DCA IF MNT
SM
S740
LANE 40
CLR A
CLR B
ASF
CAJ
S741
LANE 41
P741
MST
TB770
S742
LANE 42
LS1
LS2
CBJ
S743
LANE 43
P743
LS4
LS8
TFM
S744
LANE 44
COM 10
MCT

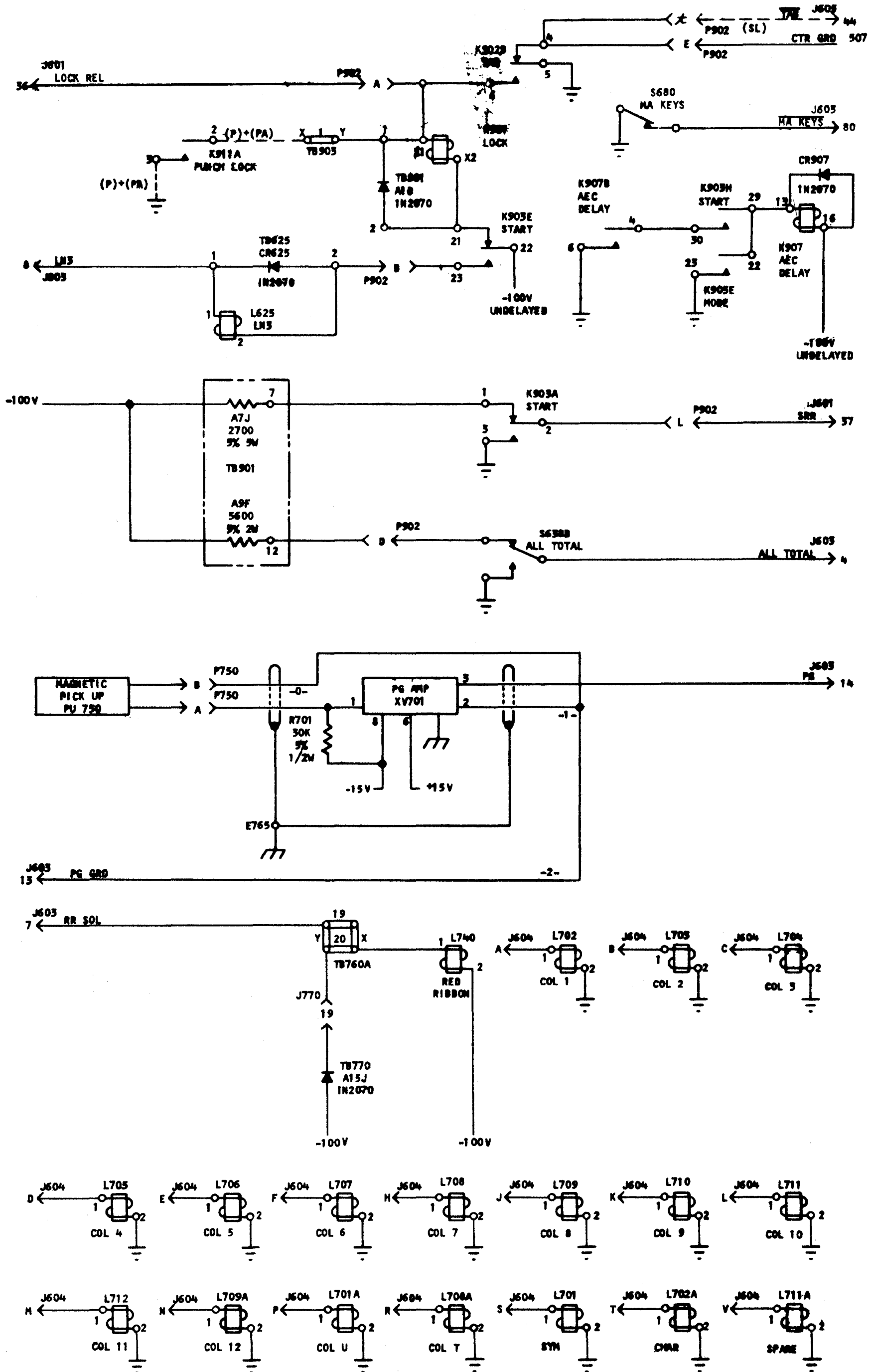
Ref. Page 505



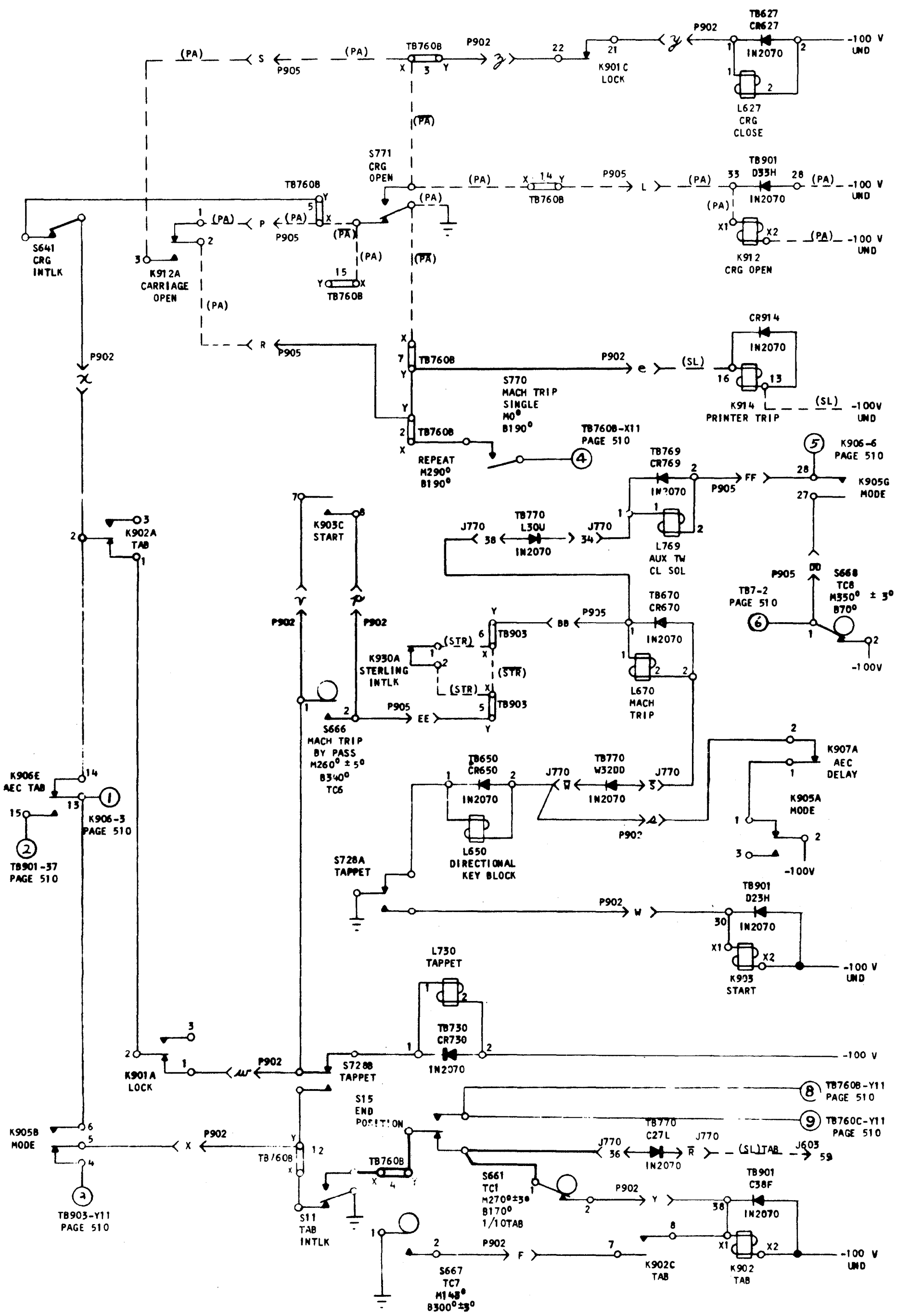
Ref. Page 506


S638A
ALL TOTAL
AT. L65
J601
S635
CLR MEM
KEY
S765
LN 65
P902
K904C
MANUAL
504 SPL COMM
MEM CLR SYN
MEM CLR
TB770
P14V
J770
J603
S663
TC3
MEM CLR
S753
LN53
K902D
TAB
K904B
MANUAL
RKA/ 512
P602
K904D
MANUAL
MAN REL
S755
LN 55
MUL BB
S757
LN 57
S763
LN 63
TB760C
S773
STERLING
DECIMAL
SWITCH SHOWN
IN STERLING
MODE.
DECIMAL MODE
S752
LN 52
S756
LN 56
S758
LN 58
S760
LN 60
S766
LN 66
S751
LN 51
S754
LN 54
S759
LN 59
508 CTR GRD
(SEE NOTES)
DS602
DEC
LIGHT
COL 5 & 6
DS601
DEC
LIGHT
COL 2 & 3
DS603
DEC
LIGHT
COL 8 & 9
S761
LN 61

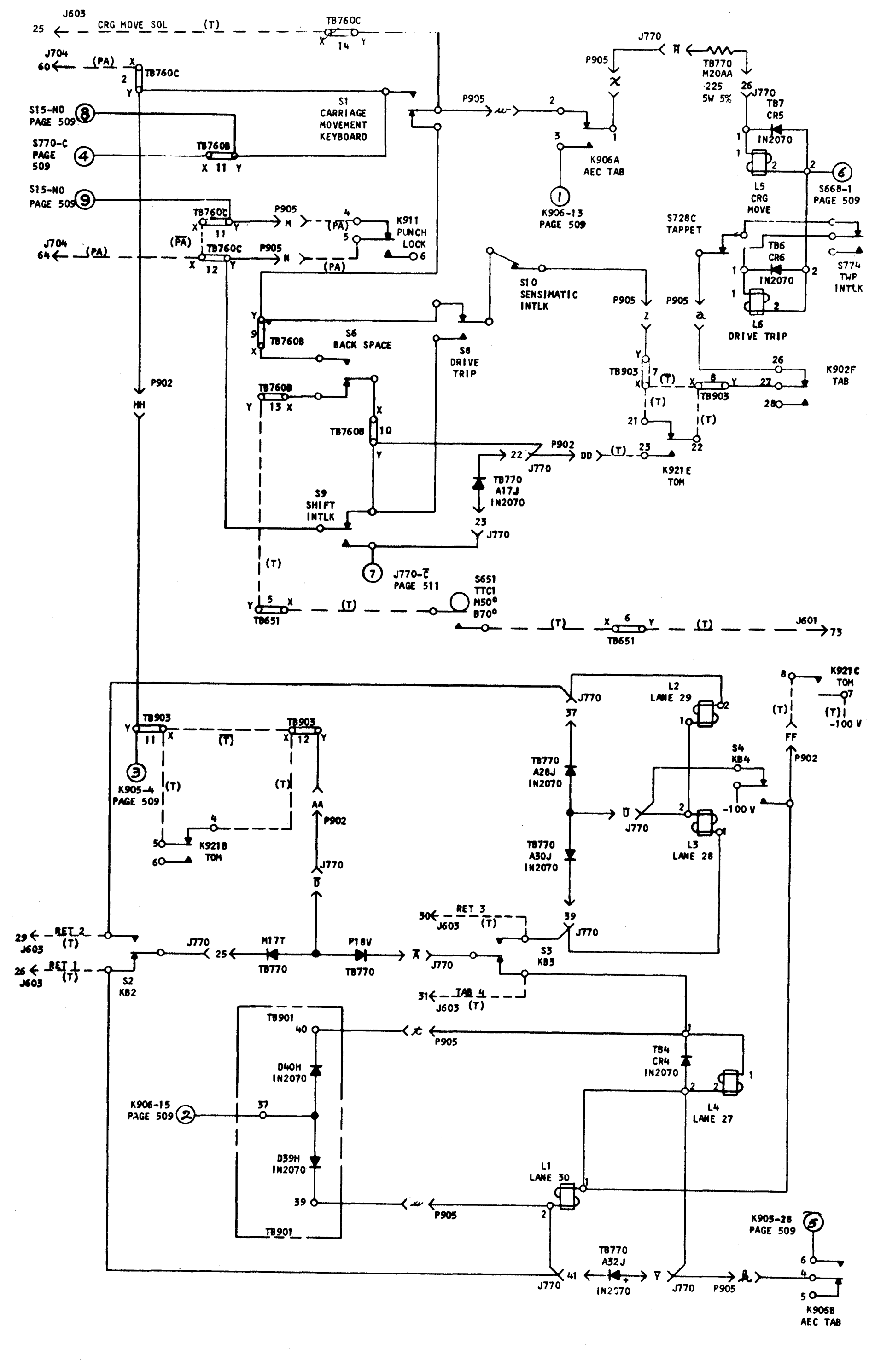
Ref. Page 507


J601
LOCK REL
P902
S680
MA KEYS
J603
MA KEYS
K911A
PUNCH LOCK
(P)+(PA)
TB905
CR907
1N2070
K907B
AEC
DELAY
K903H
START
K903E
START
K907
AEC
DELAY
TB625
CR625
1N2070
LN3
J603
L625
LN3
-100V
UNDELAYED
K905E
MODE
-100V
A7J
2700
5% 5W
TB901
A9F
5600
5% 2W
K903A
START
SRR
S638B
ALL TOTAL
J603
ALL TOTAL
MAGNETIC
PICK UP
PU 750
P750
PG AMP
XV701
R701
50K
5%
1/2W
-15V
+15V
E765
J603
PG
PG GRD
RR SOL
TB760A
J770
L740
RED
RIBBON
TB770
A15J
1N2070
-100V
-100V
J604
L702
COL 1
L703
COL 2
L704
COL 3
L705
COL 4
L706
COL 5
L707
COL 6
L708
COL 7
L709
COL 8
L710
COL 9
L711
COL 10
L712
COL 11
L709A
COL 12
L701A
COL U
L708A
COL T
L701
SYM
L702A
CHAR
L711A
SPARE

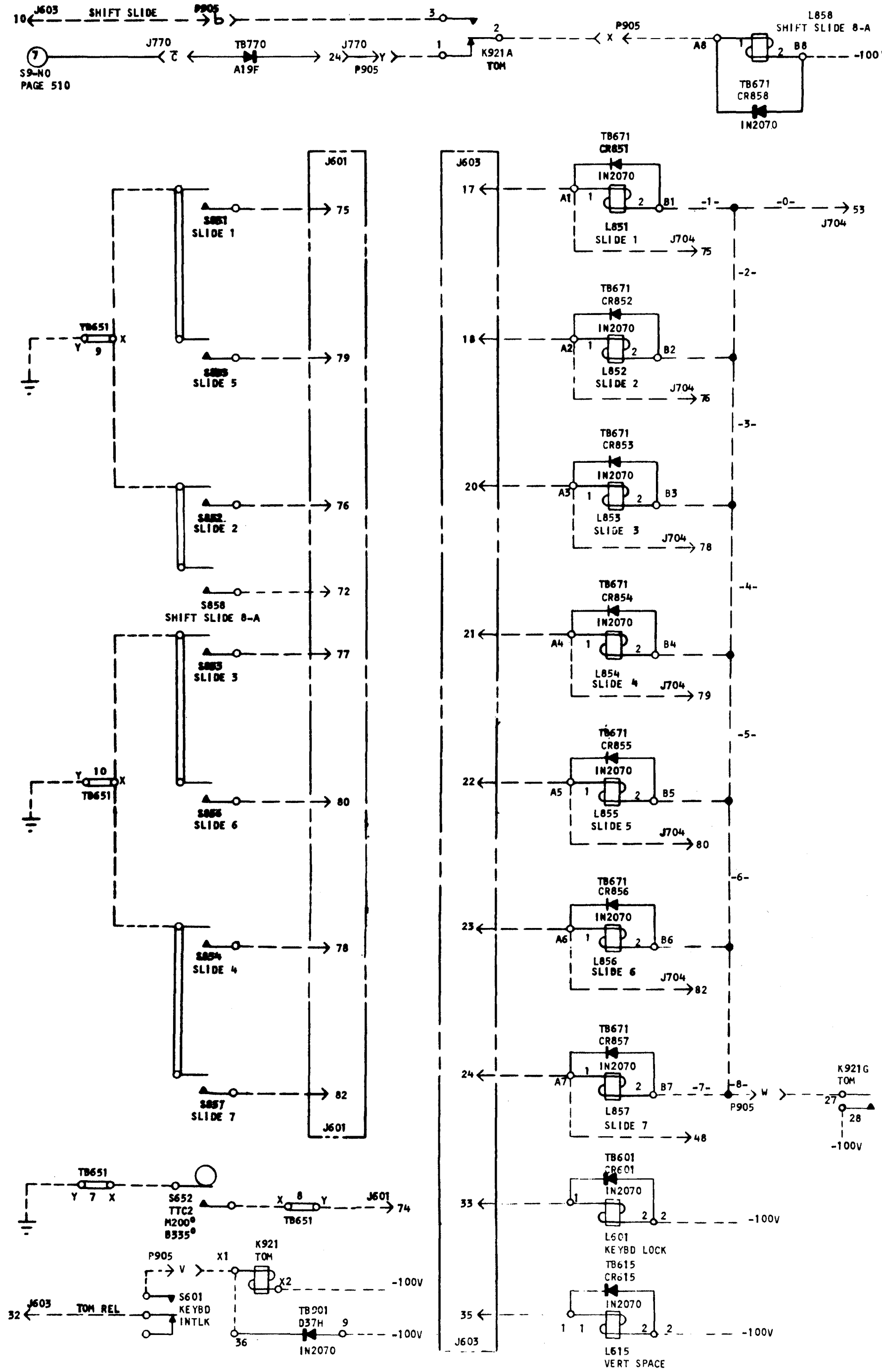
Ref. Page 508


TB627
CR627
1N2070
-100 V
UND
P902
K901C
LOCK
L627
CRG
CLOSE
TB7608
P905
S771
CRG
OPEN
TB901
D33H
1N2070
K912
CRG OPEN
S641
CRG
INTLK
K912A
CARRIAGE
OPEN
CR914
K914
PRINTER TRIP
S770
MACH TRIP
SINGLE
REPEAT
TB7608-X11
PAGE 510
TB769
CR769
K906-6
PAGE 510
K905G
MODE
TB770
L30U
J770
L769
AUX TW
CL SOL
K902A
TAB
K903C
START
TB670
CR670
TB7-2
PAGE 510
S668
TC8
K930A
STERLING
INTLK
TB903
L670
MACH
TRIP
S666
MACH TRIP
BY PASS
TC6
K906E
AEC TAB
K906-3
PAGE 510
TB901-37
PAGE 510
TB650
CR650
L650
DIRECTIONAL
KEY BLOCK
W32DD
K907A
AEC
DELAY
K905A
MODE
S728A
TAPPET
TB901
D23H
K903
START
L730
TAPPET
TB730
CR730
K901A
LOCK
S728B
TAPPET
S15
END
POSITION
TB7608-Y11
PAGE 510
TB760C-Y11
PAGE 510
K905B
MODE
TB903-Y11
PAGE 510
S11
TAB
INTLK
S661
TC1
C27L
J603
TB901
C38F
S667
TC7
K902C
TAB
K902
TAB

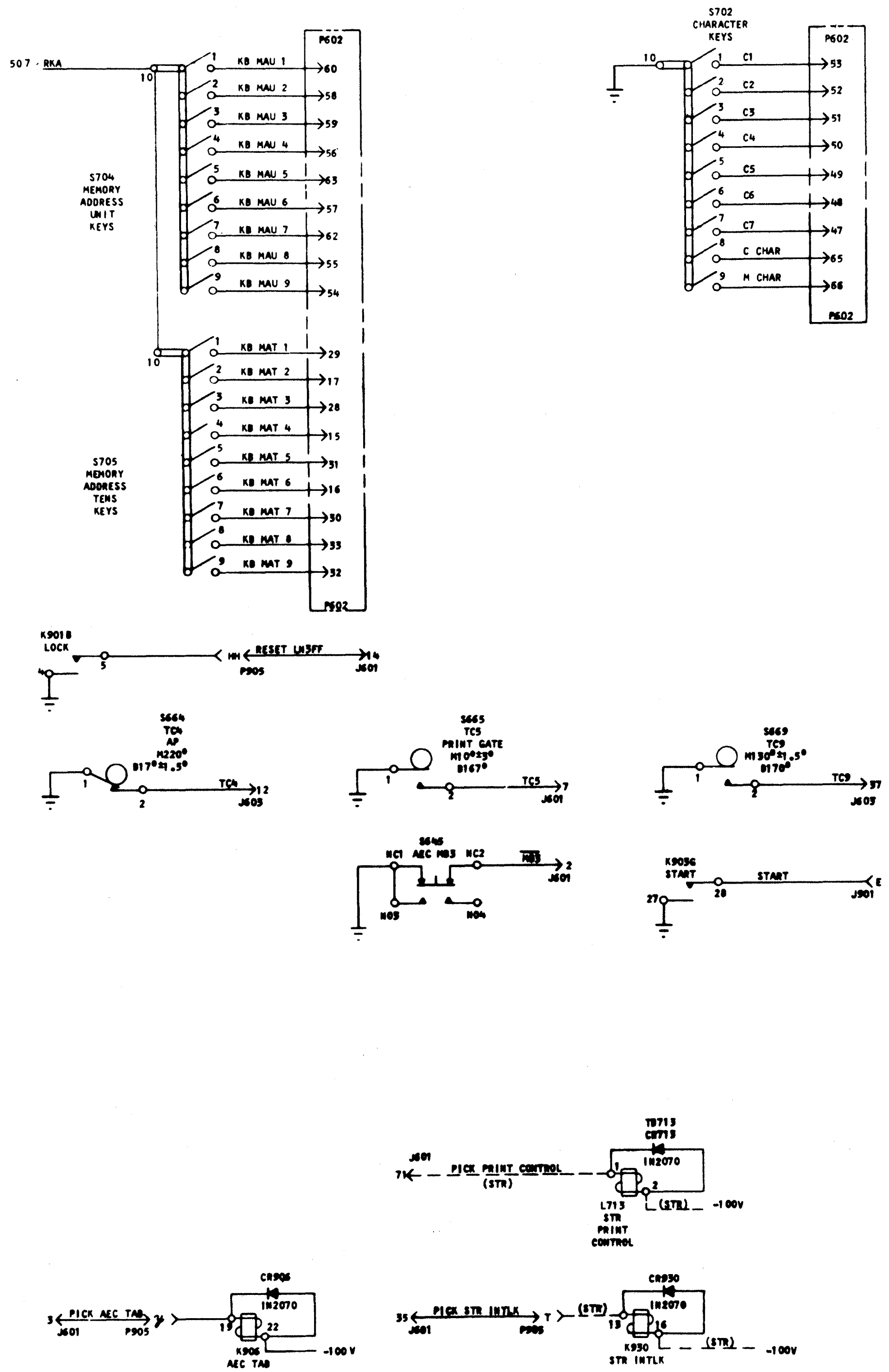
Ref. Page 509



Ref. Page 510

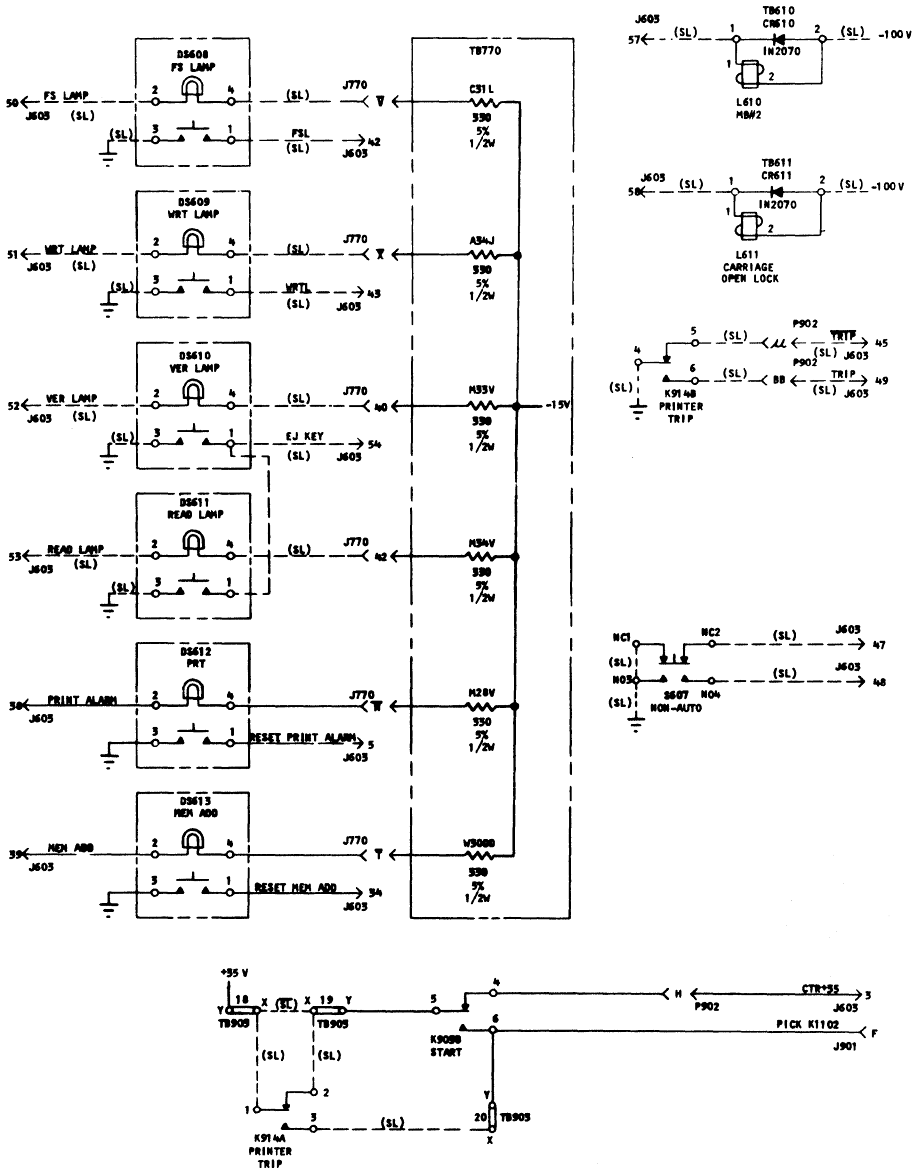

SHIFT SLIDE
S9-NO
PAGE 510
K921A
TOM
L858
SHIFT SLIDE 8-A
-100V
J601
J603
SLIDE 1
SLIDE 5
SLIDE 2
S858
SHIFT SLIDE 8-A
SLIDE 3
SLIDE 6
SLIDE 4
SLIDE 7
L851
L852
L853
L854
L855
L856
L857
K921G
TOM
L601
KEYBD LOCK
L615
VERT SPACE
S601
KEYBD
INTLK
TOM REL

Ref. Page 511

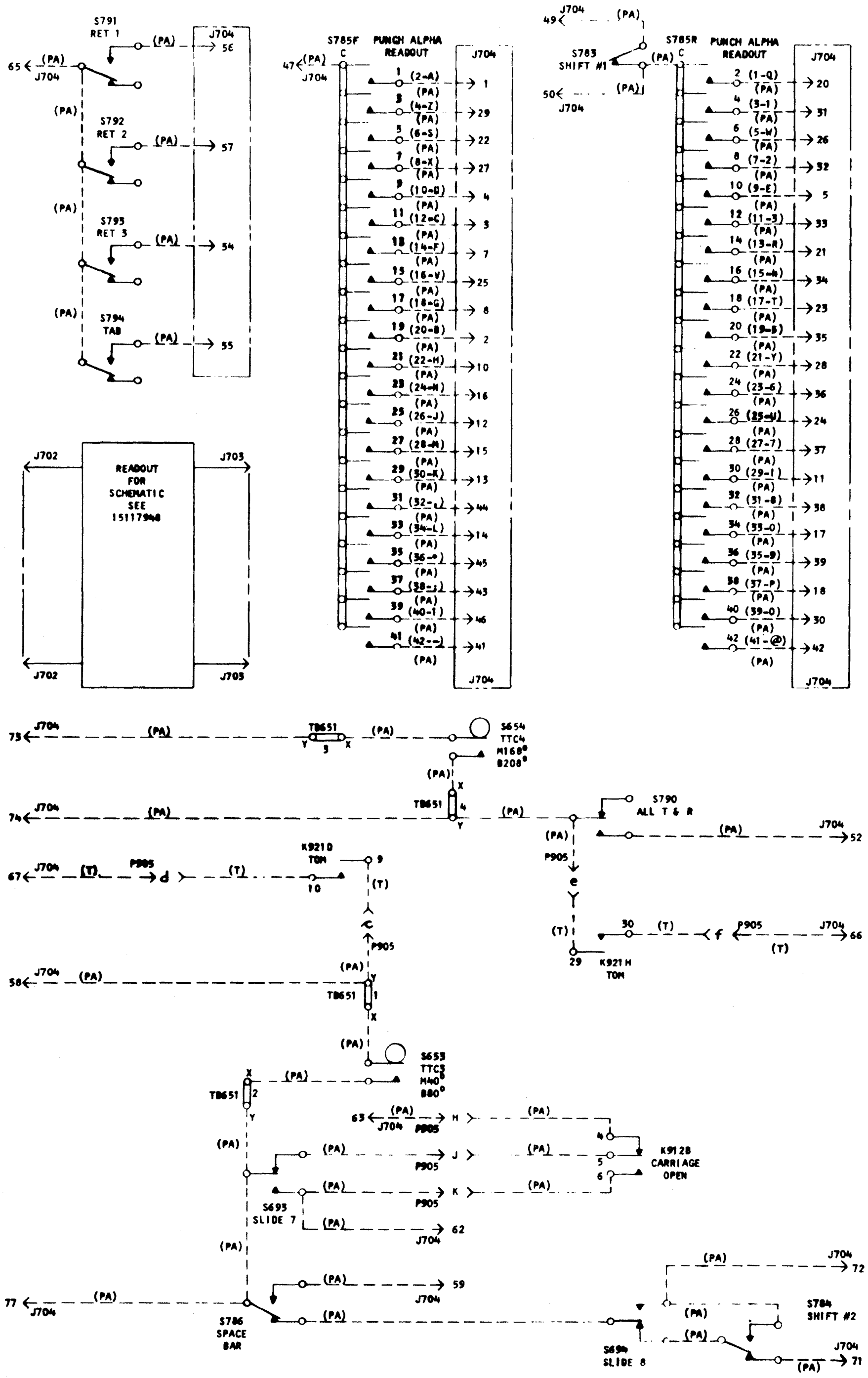


507 - RKA
S704 MEMORY ADDRESS UNIT KEYS
KB MAU 1
KB MAU 2
KB MAU 3
KB MAU 4
KB MAU 5
KB MAU 6
KB MAU 7
KB MAU 8
KB MAU 9
P602
S705 MEMORY ADDRESS TENS KEYS
KB MAT 1
KB MAT 2
KB MAT 3
KB MAT 4
KB MAT 5
KB MAT 6
KB MAT 7
KB MAT 8
KB MAT 9
S702 CHARACTER KEYS
C1
C2
C3
C4
C5
C6
C7
C CHAR
M CHAR
K901B LOCK
RESET LNSFF
P905
J601
S664 TC4 AP
TC4
J603
S665 TC5 PRINT GATE
TC5
S669 TC9
TC9
S646 AEC MB3
START
J901
PICK PRINT CONTROL (STR)
1N2070
L713 STR PRINT CONTROL
-100V
PICK AEC TAB
CR906
K906 AEC TAB
PICK STR INTLK
CR930
K930 STR INTLK

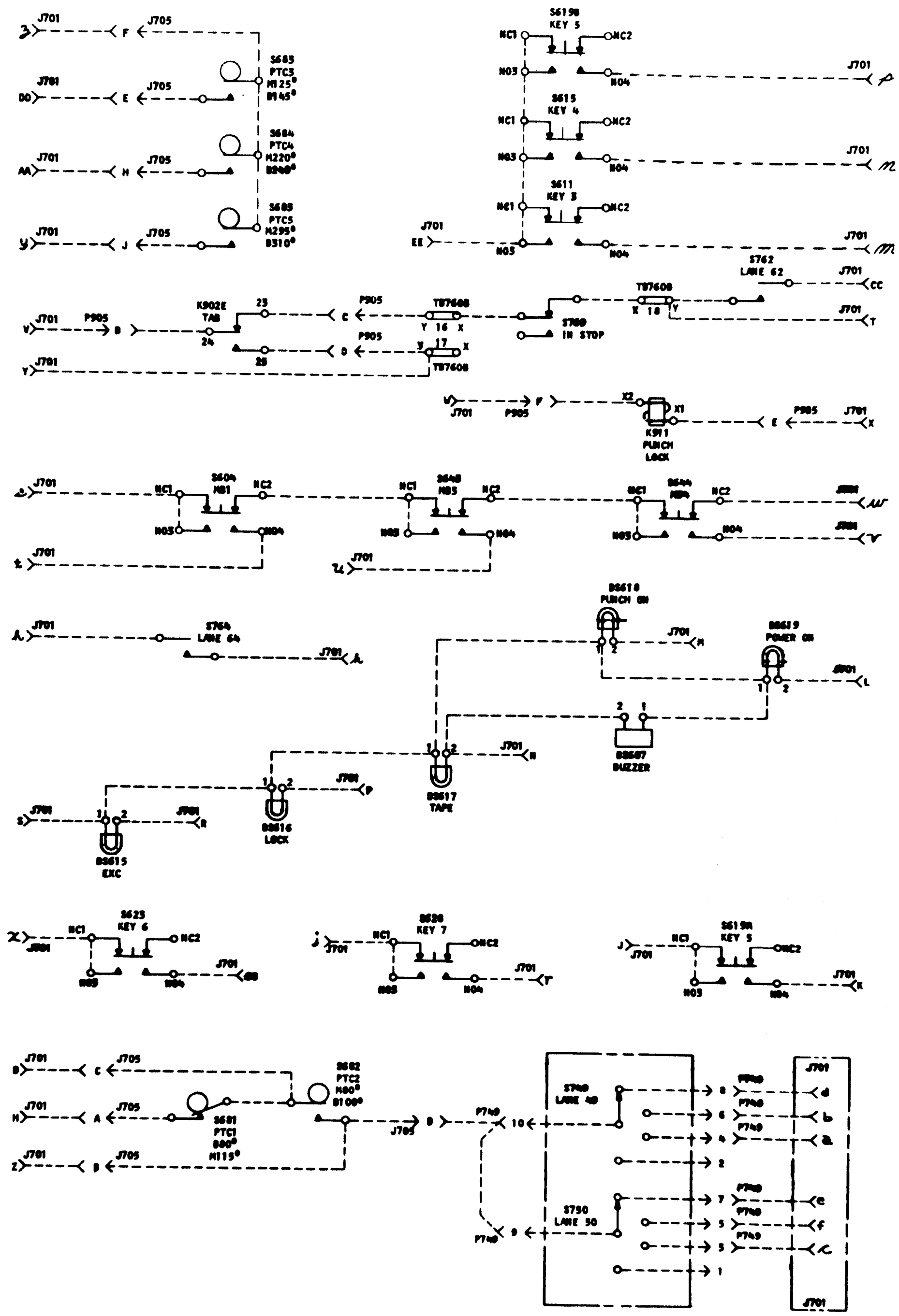
Ref. Page 512



Ref. Page 513



Ref. Page 514



Ref. Page 515

CARD	RESISTORS	PAGE	CAPACITORS	PAGE	DIODES	PAGE
TB770	M20AA	510				
TB770	M22AA	507	A26P	502		
TB770	M24AA	507	S26EE	502	M1T	506
TB770	M28V	513				
TB770	W300D	513			M2T	506
TB770	C31L	513			A3F	505
TB770	M33V	513			C4J	505
TB770	M34V	513			P4V	505
TB770	A34J	513			A5F	504
TB770					M5T	505
TB770					C6J	504
TB770					P6V	504
TB770					A7F	504
TB770					M7T	504
TB770					C8J	505
TB770					P8V	507
TB770					A9F	505
TB770					C10J	504
TB770					P10V	504
TB770					A11F	504
TB770					M11T	504
TB770					A13F	506
TB770					M13T	506
TB770					C14J	505
TB770					P14V	507
TB770					C27L	509
TB770					A19F	511

CARD	RESISTORS	PAGE	CAPACITORS	PAGE	DIODES	PAGE
TB770					A15J	508
TB770					M15T	505
TB770					A17J	510
TB770					M17T	510
TB770					P19V	510
TB770					A21J	507
TB770					C22J	507
TB770					A23F	507
TB770					A28J	510
TB770					A30J	510
TB770					A32J	510
TB770					W320D	509
TB770					L30U	509
TB770					C27L	509
TB901	A7J	508	A13J	502	D5H	504
TB901	A9F	508	A17J	502	J5M	504
TB901	A3N	504	A19J	502	K7N	504
TB901			A11J	502	D23H	509
TB901					D31H	504
TB901					D33H	509
TB901					D37H	511
TB901					C38F	509
TB901					D39H	510
TB901					D40H	510
TB901					A1D	508

SOLENOID	NAME	PAGE
L1	LANE 30	510
L2	LANE 29	510
L3	LANE 28	510
L4	LANE 27	510
L5	CARRIAGE MOVE	510
L6	DRIVE TRIP	510
L601	KEYBD LOCK	511
L610	MB #2 (SL)	513
L611	CARRIAGE OPEN LOCK (SL)	513
L615	VERT SPACE (T)	511
L625	LANE 3	508
L627	CARRIAGE CLOSE	509
L650	DIR KEY BLOCK	509
L670	MACH TRIP	509
L701	SYM	508
L701A	COL U	508
L702	COL 1	508
L702A	CHAR	508
L703	COL 2	508
L704	COL 3	508
L705	COL 4	508
L706	COL 5	508
L707	COL 6	508
L708	COL 7	508
L708A	COL T	508
L709	COL 8	508
L709A	COL 12	508
L710	COL 9	508
L711	COL 10	508
L711A	SPARE	508
L712	COL 11	508
L730	TAPPET	509
L740	RED RIBBON	508
L769	AUX TW CL SOL	509
L851	SLIDE 1 (T)	511
L852	SLIDE 2 (T)	511
L853	SLIDE 3 (T)	511
L854	SLIDE 4 (T)	511
L855	SLIDE 5 (T)	511
L856	SLIDE 6 (T)	511
L857	SLIDE 7 (T)	511
L713	STR PRINT CONTROL(STR)	512
L858	SHIFT SLIDE 8-A	511

SWITCHES	NAME	PAGE
S1	CRG MOVEMENT KEYBD	510
S2	KEYBD 2	510
S3	KEYBD 3	510
S4	KEYBD 4	510
S6	BACK SPACE	510
S8	DRIVE TRIP	510
S9	SHIFT INTLK	510
S10	SENSIMATIC INTLK	510
S11	TAB INTLK	509
S15	END POSITION	509
S601	KEYBD INTLK (T)	511
S604	MB1 (P+PA)	515
S607	NON-AUTO (SL)	513
S611	KEY 3 (P+PA)	515
S615	KEY 4 (P+PA)	515
S618	C-	504
S619A	KEY 5 (P+PA)	515
S619B	KEY 5 (P+PA)	515
S622	C+	504
S623	KEY 6 (P+PA)	515
S627	C•	504
S628	KEY 7 (P+PA)	515
S629	RE KEY	506
S630	RE KEY	506
S631	PUNCH POWER ON (P+PA)	502
S632	C*	504
S635	CLR MEM KEY	507
S638A	ALL TOTAL	507
S638B	ALL TOTAL	508
S641	CRG INTLK	509
S643	MB3 (P+PA)	515
S644	MB4 (P+PA)	515
S645	AEC MB3	512
S651	TTC1 (T)	510
S652	TTC2 (T)	511
S653	TTC3 (PA)	514
S654	TTC4 (PA)	514
S661	TC1	509
S662	TC2	504
S663	TC3	507
S664	TC4	512
S665	TC5	512
S666	TC6	509
S667	TC7	509
S668	TC8	509
S669	TC9	512
S680	MA KEYS	508
S681	PTC 1(P+PA)	515
S682	PTC 2(P+PA)	515
S683	PTC 3(P+PA)	515
S684	PTC 4(P+PA)	515
S685	PTC 5(P+PA)	515
S693	SLIDE 7 (PA)	514
S694	SLIDE 8 (PA)	514
S698A	MAIN POWER	502
S698B	MAIN POWER	502
S701	PRINTER KEYBD SWITCHES	512
S702	C, M & CHARACTER KEYS	512
S704	MEM ADDRESS UNITS KEYS	512
S705	MEM ADDRESS TENS KEYS	512

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S728A	TAPPET	509
S728B	TAPPET	509
S728C	TAPPET	510
S731	LANE 31	503
S732	LANE 32	503
S733	LANE 33	503
S734	LANE 34	504
S735	LANE 35	504
S736	LANE 36	504
S737	LANE 37	505
S738	LANE 38	505
S739	LANE 39	505
S740	LANE 40	505
S741	LANE 41	505
S742	LANE 42	505
S743	LANE 43	505
S744	LANE 44	505
S745	LANE 45	506
S746	LANE 46	506
S747	LANE 47	506
S748	LANE 48	506
S749	LANE 49 (P+PA)	515
S750	LANE 50 (P+PA)	515
S751	LANE 51	507
S752	LANE 52 (SL)	507
S753	LANE 53	507
S754	LANE 54	507
S755	LANE 55	507
S756	LANE 56 (SL)	507
S757	LANE 57	507
S758	LANE 58 (SL)	507
S759	LANE 59	507
S760	LANE 60 (SL)	507
S761	LANE 61	507
S762	LANE 62 (P+PA)	515
S763	LANE 63	507
S764	LANE 64 (P+PA)	515
S765	LANE 65	507
S766	LANE 66 (SL)	507
S769	IN STOP (P+PA)	515
S770	MACH TRIP	509
S771	CRG OPEN	509
S772	AEC TC	504
S773	STERLING DECIMAL	507
S783	SHIFT #1	514
S784	SHIFT #2	514
S785F	PUNCH ALPHA READOUT	514
S785R	PUNCH ALPHA READOUT	514
S786	SPACE BAR (PA)	514
S790	ALL T & R (PA)	514
S791	RET #1 (PA)	514
S792	RET #2 (PA)	514
S793	RET #3 (PA)	514
S794	TAB (PA)	514
S851	SLIDE 1(T)	511
S852	SLIDE 2(T)	511
S853	SLIDE 3(T)	511
S854	SLIDE 4(T)	511
S855	SLIDE 5(T)	511
S856	SLIDE 6(T)	511
S857	SLIDE 7(T)	511
S774	TWP INTLK	510
S858	SHIFT SLIDE 8-A	511

DIODES	PAGE
CR4	510
CR5	510
CR6	510
CR601	511
CR610	513
CR611	513
CR615	511
CR625	508
CR627	509
CR650	509
CR670	509
CR713	512
CR730	509

DIODES	PAGE
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CR851	511
CR852	511
CR853	511
CR854	511
CR855	511
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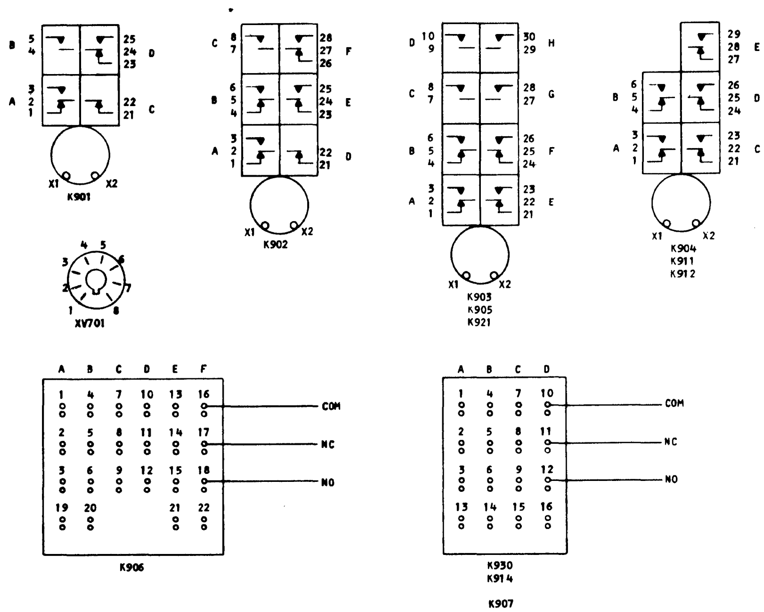
CR857	511
CR906	512
CR907	508
CR914	509
CR858	511
CR930	508

RESISTORS	PAGE
R701	508

CAPACITORS	PAGE
C601	502
C602	502



RELAYS	NAME	PAGE								
		COIL	A	B	C	D	E	F	G	H
K1	MOTOR START	502								
K901	LOCK	508	509	512	509					
K902	TAB	509	509	508	509	507	515	509		
K903	START	509	508	513	509	504	508		512	508
K904	MANUAL	504	504	507	507	507				
K905 (AEC)	MODE	504	509	509	504		508	506	509	
K906 (AEC)	AEC TAB	512	510	510			509	504		
K907	AEC DELAY	508	509	508						
K911 (P)+(PA)	PUNCH LOCK	515	508	510						
K912 (PA)	CARRIAGE OPEN	509	509	514						
K914 (SL)	PRINTER TRIP	509	513	513						
K921 (T)	TOM	511	511	510	510	514	510		511	514
K930 (STR)	STERLING INTLK	512	509							

CTR LN COMM	PAGE
*S772-NO	504
P731-10	503
P731-9	503
P733-9	504
P735-10	504
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P737-10	505
P737-9	505
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P743-9	505
P745-10	506
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P747-9	506
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S630-N04	506

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K904-2	504
K904-5	507
K904-22	507

MAN COMM	PAGE
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S618-N03	504
S622-N03	504
S627-N03	504
S632-N03	504
J770-17	505
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COMPONENT	NAME	PAGE
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DS601	DEC LIGHT COL 2 & 3	507
DS602	DEC LIGHT COL 5 & 6	507
DS603	DEC LIGHT COL 8 & 9	507
DS607	BUZZER (TAPE)	515
DS608	FS LAMP (SL)	513
DS609	WRT LAMP (SL)	513
DS610	VER LAMP (SL)	513
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DS616	LOCK (TAPE)	515
DS617	(TAPE)	515
DS618	PUNCH ON	515
DS619	POWER ON (TAPE)	515
XV701	PG AMP SOCKET	508

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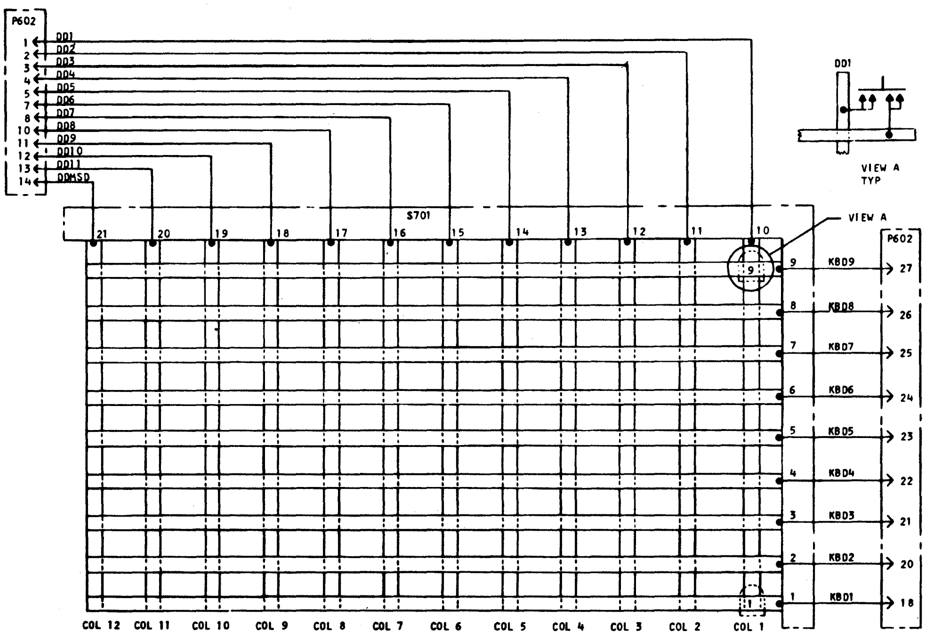
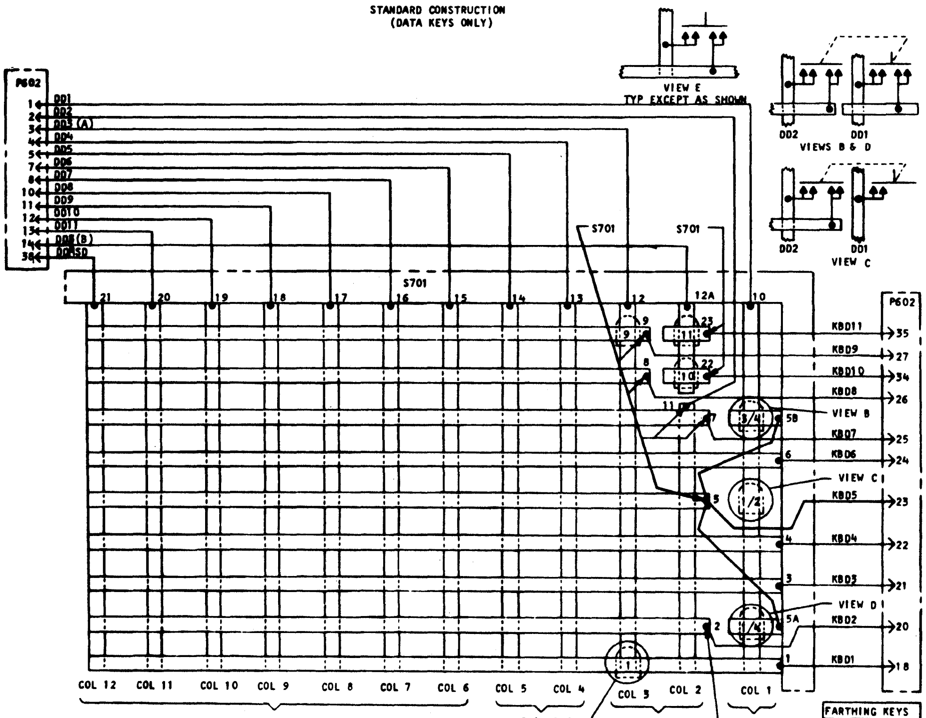


STANDARD CONSTRUCTION
(DATA KEYS ONLY)



FARTHING CONSTRUCTION
(DATA KEYS ONLY)

FARTHING KEYS		
KEY	DD2	DD1
1/4	2	5
1/2	5	0
3/4	7	5

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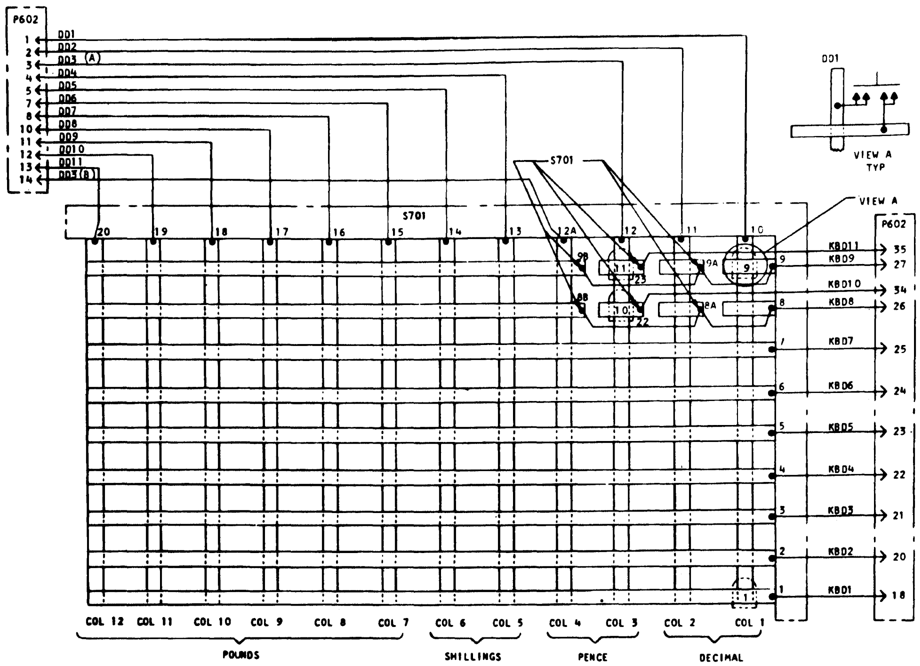
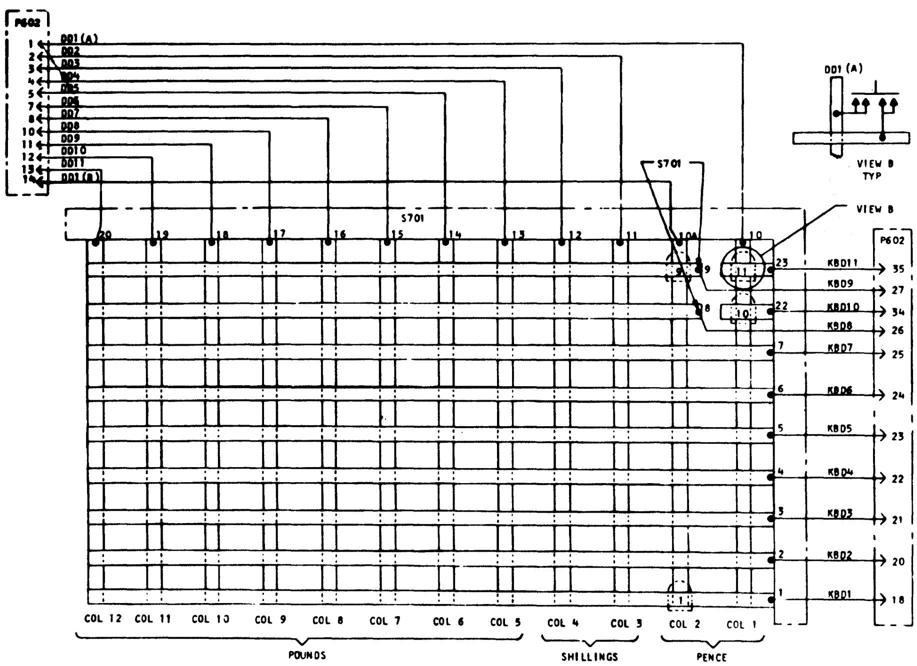


DECIMAL PENNY CONSTRUCTION
(DATA KEYS ONLY)



WHOLE PENNY CONSTRUCTION
(DATA KEYS ONLY)

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J601		J603		J604				J701		J704		J901		P602		P705		P902		P905	
PIN	PAGE	PIN	PAGE	PIN	PAGE	PIN	PAGE	PIN	PAGE	PIN	PAGE	PIN	PAGE	PIN	PAGE	PIN	PAGE	PIN	PAGE	PIN	PAGE
1	507	1	507	A	508	1		A		1	514	A	502	1	518	A	515	A	508	A	502
2	512	2	507	B	508	2		B	502	2	514	B	502	2	518	B	515	B	508	B	515
3	512	3	513	C	508	3		C	503	3	514	C	503	3	518	C	515	C	503	C	515
4	504	4	508	D	508	4		D	515	4	514	D	503	4	518	D	515	D	508	D	515
5	507	5	513	E	508	5		E	502	5	514	E	512	5	518	E	515	E	508	E	515
7	512	7	508	F	508	7		F	503	7	514	F	513	7	518	F	515	F	509	F	515
8	507	8	508	H	508	8		H	515	8	514	H	502	8	518	H	515	H	513	H	514
10	506	10	511	J	508	10		J	515	10	514	J	502	10	518	J	515	J	503	J	514
11	506	11		K	508	11		K	515	11	514	K	502	11	518	K		K	504	K	514
12	504	12	512	L	508	12		L	515	12	514	L		12	518	L		L	508	L	509
13	506	13	508	M	508	13		M	515	13	514	M		13	518	M		M	507	M	510
14	512	14	508	N	508	14		N	515	14	514	N		14	518	N		N	507	N	510
15	505	15	502	P	508	15		P	515	15	514	P		15	512	P		P	504	P	509
16	505	16	502	R	508	16		R	515	16	514	R		16	512	R		R	507	R	509
17	505	17	511	S	508	17		S	515	17	514	S		17	512			S	504	S	509
18	505	18	511	T	508	18		T	515	18	514	T		18	518			T		T	512
20	505	20	511	U	505	20		U		20	514	U		20	518			U	502	U	
21	505	21	511	V	508	21		V	515	21	514	V		21	518			V	502	V	511
22	505	22	511	W		22		W	515	22	514	W		22	518			W	509	W	511
23	505	23	511	X		23		X	515	23	514	X		23	518			X	509	X	511
24	505	24	511	Y		24		Y	515	24	514	Y		24	518			Y	509	Y	511
25	505	25	510	Z		25		Z	515	25	514	Z		25	518			Z		Z	510
26	506	26	510	a		26		a	515	26	514	a		26	518			a		a	510
27	504	27	504	b		27		b	515	27	514	b		27	518			b		b	511
28	506	28	507	c		28		c	515	28	514	c	(TC)*	28	512			c	503	c	514
29	506	29	510	d		29		d	515	29	514	d		29	512			d		d	514
30	506	30	510	f		30		e	515	30	514	f		30	512			e	509	e	514
31	506	31	510	g		31		f	515	31	514	g		31	512			f		f	514
32	503	32	511	h		32		h	515	32	514	h		32	512			h	507	h	
33	503	33	511	i		33		j	515	33	514	i	502	33	512			j	502	j	
34	503	34	513	j		34		k	515	34	514		502	34	518			k	502	k	510
35	512	35	511	k		35		m	515	35	514	k		35	518			m	502	m	
36	508	36	507	m		36		n	515	36	514	m		36				n	502	n	506
37	508	37	512	n		37		p	515	37	514	n	502	37				p	509	p	
38	506	38	513			38		r	515	38	514			38	518			r	502	r	
39	505	39	513			39		s	515	39	514			39				s	509	s	510
40	505	40				40		t	515	40				40				t	508	t	510
41	504	41				41		u	515	41	514			41				u	513	u	506
42	505	42	513			42		v	515	42	514			42				v	509	v	506
43	504	43	513			43		w	515	43	514			43				w	509	w	510
44	505	44				44		x	515	44	514			44				x	509	x	510
45	504	45	513			45		y	515	45	514			45				y	509	y	512
46	505	46	507			46		z	515	46	514			46				z	509	z	
47	503	47	513			47		AA	515	47	514			47	512			AA	510	AA	504
48	503	48	513			48		BB	515	48	511			48	512			BB	513	BB	509
49	503	49	513			49		CC	515	49	514			49	512			CC	502	CC	
50	503	50	513			50		DD	515	50	514			50	512			DD	510	DD	509
51	503	51	513			51		EE	515	51				51	512			EE	(TC)*	EE	509
52	503	52	513			52		FF		52	514			52	512			FF	510	FF	509
53	504	53	513			53		HH		53	511			53	512			HH	510	HH	512
54	504	54	513			54				54	514			54	512						
55	504	55	507			55				55	514			55	512						
56	505	56	507			56				56	514			56	512						
57	505	57	513			57				57	514			57	512						
58	506	58	513			58				58	514			58	512						
59	505	59	509			59				59	514			59	512						
60	507	60	506			60				60	510			60	512						
62	507	62				62				62	514			62	512						
63	505	63	507			63				63	514			63	512						
64	505	64	507			64				64	510			64							
65		65				65				65	514			65	512						
66	505	66				66				66	514			66	512						
67	504	67				67				67	514			67							
70	505	70	507			70				70				70	507						
71	512	71	503			71				71	514			71	503						
72	511	72	507			72				72	514			72							
73	510	73	507			73				73	514			73	507						
74	511	74	507			74				74	514			74	507						
75	511	75	507			75				75	511			75	507						
76	511	76	507			76				76	511			76	507						
77	511	77	507			77				77	514			77	507						
78	511	78	507			78				78	511			78							
79	511	79	507			79				79	511			79							
80	511	80	508			80				80	511			80							
82	511	82				82				82	511			82							

* NOTE: FEATURE ABBREVIATIONS IN PAGE COLUMN INDICATES PIN IS RESERVED, AND FOUND ON APPROPRIATE SCHEMATIC

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TERMINAL BOARD INDEX

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TERM	PAGE	TERM	PAGE	TERM	PAGE	TERM	PAGE	TERM	PAGE
1		1		1		1		1	508
2		2	509	2	510	2		2	502
3		3	509	3		3		3	502
4	502	4	509	4	502	4		4	
5	502	5	509	5	507	5		5	509
6	502	6	502	6		6		6	509
7	502	7	509	7	509	7		7	510
8	502	8		8		8		8	510
9	502	9	510	9		9		9	
10	502	10	510	10	502	10		10	
11	502	11	510	11	510	11		11	510
12	502	12	509	12	510	12		12	510
13	502	13	510	13		13		13	
14	502	14	509	14	510	14		14	509
15	502	15	509	15	502	15		15	
16	502	16	515	16	502	16		16	
17	502	17	515	17		17		17	513
18	502	18	515	18		18		18	513
19	508	19	502	19		19		19	513
20	508	20	502	20		20		20	513

Servicing Procedures

INDEX

SERVICING PROCEDURES

Servicing Procedures provides a guide in servicing the system. One of the most important things to remember when servicing the system is, "Do not do anything to the system without giving prior thought to its effect." Always gather as much information as possible about a problem before changing the status of the machine. Once the power is turned off or a halt or lock is released, the entire status of the logic may change. This may make it impossible to determine the problem or its cause unless the condition reoccurs.

CARD SUBSTITUTION

Card substitution may be used in servicing the machine. However, the second stage amplifier of each MRFF card is critically matched with the corresponding sense pre-amplifier on the memory card.

UNDER NO CIRCUMSTANCES SHOULD MRFF CARDS BE INTERCHANGED, EXCEPT TEMPORARILY WHILE TROUBLESHOOTING. SHOULD REPLACEMENT OF AN MRFF CARD OR THE MEMORY CARD BECOME NECESSARY, ALL FOUR MRFF CARDS AND THE MEMORY CARD MUST BE REPLACED AS A MATCHED SET OR ERRATIC READING MAY RESULT.

To avoid possible damage to components, always turn off the power before removing or inserting cards.

SINGLE SHOT CLOCK OPERATION

The arithmetic cycle can be performed in single clock pulse increments by using the single shot clock. To prepare for single shot clock operation the power must be turned off and the following changes made.

1. Insert the single shot clock card in location B4D. This disables the automatic clock card and makes the SSC switch active.

2. Remove the PC card from location A3D. This is necessary to prevent damage to the PC card when simulating sync pulses.

3. Place a jumper wire from the output of the PC card, (A3D pin 9) to -4 volts (A3D pin 32). This simulates a low output from the PC card until simulated sync pulses are desired.

4. Turn the power on.

The single shot clock is primarily designed for use with a manual operation. This means that the desired memory location, data input, and manual program should be indexed on the keyboard. If it should be necessary to program commands which are normally provided by the sensing switches but not available at the keyboard, the appropriate wetter inputs may be jumpered to ground in the arithmetic unit after removing the connection between the switch and the wetter. Failure to remove the circuit between the wetter and switch will result in back circuits, which cause incorrect commands to the arithmetic unit.

When the machine has been readied for single shot operation and the proper program indexed, a machine cycle may be initiated in the following manner:

1. Transfer the SRR/35 switch. This removes the 35 volt keyboard wetting and provides a Start Relay Reset signal to reset the rack stop flip-flops.

2. Depress and release the POR switch button. This initiates the Power On Reset signal.

3. Depress and release the MR switch button. This initiates the machine reset signals.

4. Depress and hold the DMR switch button.

5. While holding the DMR button depressed, depress and release the SSC switch button. After releasing the SSC button, release the DMR button. This initiates the Delay Machine Reset signal.

The electronic cycle has now been initiated and may be progressed by repetitively depressing the SSC button. Each depression of the SSC button now generates a single clock pulse.

Repetitive depression of the SSC button will progress the logic to S3 of T2 where a PC sync pulse is required in order to set S3. The sync pulse is simulated by removing one end of the jumper holding the pin at A3D pin 9 to -4 volts. With the jumper removed from A3D pin 9 to the signal level at pin 9 goes to ground and simulates a high signal from the PC card, thus simulating a sync pulse. With the jumper removed, depress and release the SSC button and S3 will set. Then replace the jumper between A3D pin 9 and A3D pin 32. This procedure is necessary each time a sync pulse is required to set S3 in T2.

The electronic cycle may be terminated at any time and a new cycle begun by repeating steps two through five of the initiating procedure. The cycle may be terminated at any time and the machine returned to standard operating condition by turning the power off, transferring the SRR.35 switch back to normal, removing the SSC card, replacing the PC card, removing the jumper from A3D pin 9 to A3D pin 32 and removing any other jumpers which may have been used.

JAMMING LOGIC ELEMENTS

The output of certain logic elements may be jammed in a high state to assist in analysis of troubles. Under no condition should an attempt be made to jam the input of any element other than a voltage wetter.

Jamming an input will cause destruction of diodes or transistors in preceeding elements of the logic. The output of certain elements may be jammed by installing a jumper between the output terminal and ground. The circuit and the output terminal should be double checked prior to installing the jumper. <u>Grounding of the incorrect terminal can cause serious trouble.</u>

JAMMING FLIP-FLOPS

When a flip-flop is jammed in the above manner a signal spike will be obtained from its reset or set output. For example, if in desiring to jam a flip-flop in its reset state a jumper is connected from the reset output to ground, the set input signals will attempt to set the flip-flop and at this time a positive going spike will appear at its set output. The flip-flop, however, will not set. If this spike cannot be tolerated, connect the annode of a BCX58-1 diode to the set gate output to prevent the flip-flop from being set. Connect the cathode (marked end) of the diode to -4.25 volts. Connecting the annode of the diode to the reset gate output will prevent the flip-flop from being reset unless the direct reset input is being used.

JAMMING GATES

Gates cannot be jammed. If the output of a gate is clamped to ground and a negative signal is applied at its input, the transistor will be destroyed due to the excessive current flow between the emitter and collector. If the output is clamped to -4 and a ground signal is applied to one of the OR inputs, one of the diodes between the transistor emitter and the input will be destroyed.

JAMMING HEAVY BUFFERS

The heavy buffer circuit output cannot be jammed under any conditions. If a heavy buffer is jammed, either the transistor or the diode in parallel with its emitter-base junction will be destroyed due to excessive current flow.

JAMMING INVERTERS

An inverter output can be clamped to ground by placing a jumper wire from its output terminal to ground. It cannot be clamped to -4 or the transistor will be destroyed when a negative signal is applied at its input terminal.

JAMMING RELAY WETTERS

Relay or switch contact wetters may be jammed in a high state at their input terminals by placing a jumper between the appropriate terminal and ground. When the input to a wetter is jumpered to ground, the circuit between the wetter and the switch contact should be opened to prevent a possible feedback loop to the switch common and other switches. Failure to open the circuit could cause incorrect signals at the inputs of their wetters. Relay wetters should not be clamped to ground at their outputs with contacts closed at their inputs may be as high as + .6 volts.

TROUBLESHOOTING ELECTRONIC LOGIC PROBLEMS

The electronic section can be cycled independently of the printer, while troubleshooting electronic problems. The electronic section can be cycled under three methods of control. These are: (1) Manual Control - A keyboard operation is performed for each depression of the MR switch. (2) Panel Control - A panel controlled operation is performed for each depression of an external switch. (3) Continuous Electronic Cycles - A continuous operation of the electronic processor under keyboard or panel control.

T times 0, 1, 3, 4, 5, and 6 may be caused to repeat continuously when using methods 1 and 2.

The pin locations mentioned in these methods should be verified by the prints with the machine under service.

MANUAL CONTROL

To initiate electronic cycles under manual control the following steps must be performed.

1. Install a jumper wire from the input of the TC9 Relay Wetter (A3A2) to ground. (Page 133)

2. Index DATA, MEMORY ADDRESS, and A Control Key (plus, minus, subtotal, or total).

3. Place the 35V switch (S1201) in the off position (Rear).

4. Depress the MR switch (S1203) on the electronic gate to initiate electronic cycles.

Any signal that normally occurs in T0 through T6 of a manual operation can be observed by this method. It must be realized that there is no writing for sync pulses in T2 and T2 will be shorted accordingly to 331 clock pulses.

PANEL CONTROL

To obtain electronic cycles under panel control the following steps must be performed:

1. Locate carriage in the stop position containing the desired programming and turn machine off.

2. Install a jumper wire from the input of the TC9 Relay Wetter (A3A2) to ground (Page 133).

3. Remove pin from TB903-6X (Page 509). This prevents the machine trip solenoid picking.

4. Remove the taper tab from the common (center terminal) of tappet switch "A" (S728A, Page 509). Attach a normally open switch between the taper tab and the common of tappet SW "A".

5. Release the tappets. If the carriage position contains a stop dog, the tappets can be released by the depression of the motor bar. If the position does not contain a stop dog, manually release the tappets.

6. Turn machine on. An electronic cycle will be obtained from each depression of the switch.

NOTE: If the RKS or EKS lanes are pinned a keyboard memory address must be indexed. If the RK lane is pinned, data as desired may be entered from the keyboard data keys.

TO REPEAT A T TIME

A T time may be repeated automatically be opening certain circuits in the machine. T2 and T7 cannot be repeated. Circuits may be opened by removing the cards, applying a small piece of scotch tape at the contacts and reinserting the card.

To repeat TO tape G1D11 and H1B19. (Page 129)

To repeat T1 tape H1B21. (Page 129)

To repeat T3 tape H1C21. (Page 129)

To repeat T4 tape H1C10. (Page 129)

To repeat T5 tape H1D21. (Page 129)

To repeat T6 tape H1D10. (Page 129)

NOTE: T6 can be repeated only if MUL or DV is programmed. SO can be used as a trigger point to view signals starting at the beginning of each T time.

CAUTION: Cards should be inspected for residue when tape is removed.

CONTINUOUS ELECTRONIC CYCLES

The electronic section can be made to repeat continuously by performing the steps listed below. This operation can be used with a manual operation, an existing magazine location or with a special magazine. When checking a multiply or divide operation with this method it is necessary that the same factors (02X10) are used during each operation. This is the operation programmed in the special magazine. This magazine may be installed in any open space in the panel, preferably near the right end. A stop is not necessary in the position. The programming of the special magazine is as follows: Add A, add B, add C, @, MA10, Clear A, Clear 11, SX, CFM, RK, ESK, and M or DV.

To initiate the cycles perform the following steps:

1. If the special magazine is to be used, load one of the multiplication or division factors into Memory Address 02.

2. Move carriage into the position to be used during the operation.

3. Turn machine off and manually release tappets.

4. Remove pin from TB903-6X (Page 509). This opens the machine trip solenoid circuit.

5. Place the +35V switch (S1201) in the off position.

6. Remove the mercury start relay (K1103).

7. If the RK, RKA, EKA signals are to be active, index the proper data or MA keys.

8. Install a jumper from the input of TC9 Relay Wetter (A3A2, page 133, to ground).

9. Install a jumper from the ECNCFF to a spare inverter input. (B4B6 to E8A21).

10. Turn machine on.

11. Install a jumper from the inverter output to the Reset Standardizer input (E8A22 to D5B21).

The ECNC signal will trigger the RS at the end of each cycle. The RS will start an electronic cycle and the electronic processor will cycle continuously. Care must be used to select trigger points that occur in the T times or portions of the T times to be observed. For example, the SCFF can be observed during T1 by triggering at G2D22 (T1.S2.DDO - Page 132).

ELECTRONIC TEST AND ADJUSTMENT
370 us Clock (USMV)

1. (a) Set oscilloscope for internal, positive, AC mode with 2 usec/div.

(b) Observe 370 usec Clock pulses at (B5B-27). The clock pulse width should be as shown below.

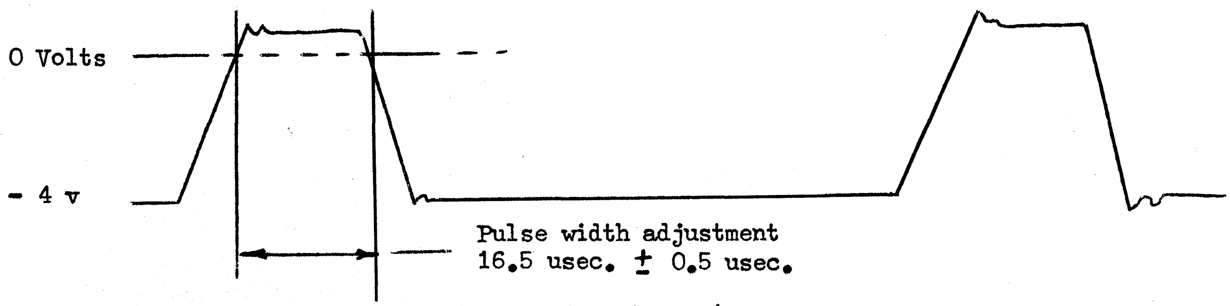


Fig. X-1

TO ADJUST: Turn potentiometer at 34EE41 of the USMV Card as required.

(c) Set oscilloscope for 50 us/division.

(d) Observe USMV FF output at C3C-25. The output should be as shown below. Adjustment should be made on the latest pulse.

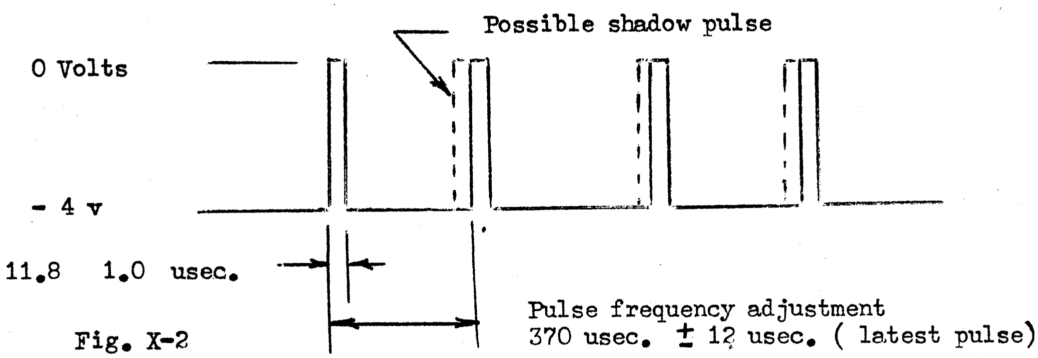


Fig. X-2

TO ADJUST: Turn potentiometer at 34S41 of the clock card.

NOTE: Recheck pulse width and readjust if necessary.

REASON: To ensure correct 370 usec clock pulse and stable USMV FF synchronization.

BOL

2. (a) Check for 2V across BOL lamp. This can be checked between TB2001-18 and TB2001-20 (ground). Set the scope to free run, 2V per division.

TO ADJUST: Turn R2002 as required. When standing at the back of the machine R2002 is the right potentiometer in the tray.

(b) With the 1/10 clutch F latched in position, observe the input to the BOL Card (A3A-17). The BOL input should remain above +150 mv when the clutch is moved slightly between pawls E & G. Set the scope to free run, .05V per division. (Fig. X-4)

TO ADJUST: (1) Loosen screw I in disc B and position as required. There must be a minimum clearance of .015 between disc B and bracket C and disc B and block A. (2) Readjust bulb voltage to provide the proper amplitude signal (R2002).

(c) Set the scope on EXT trigger, positive, AC fast 2 ms/division and .05V/division. Place external trigger on the WS output, A3A16. The input at A3A-17 should appear as below with the carriage motor running and the paper drive solenoid energized.

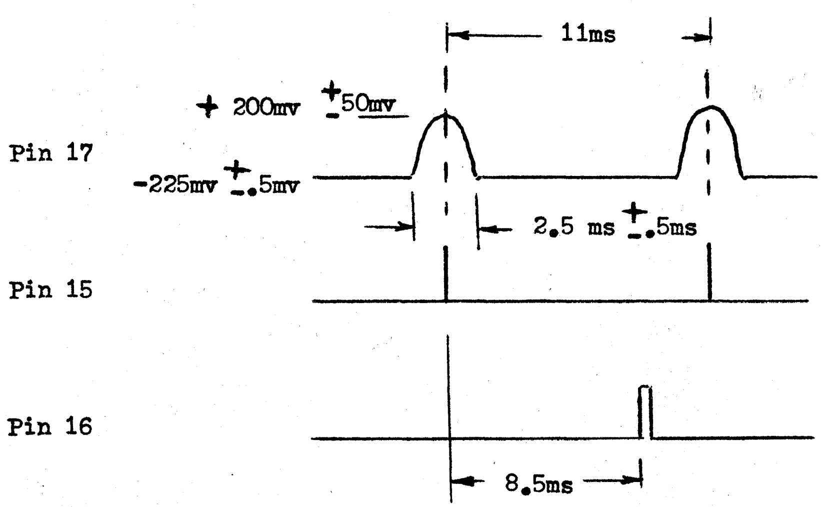


Fig. X-3

Pulse widths should be consistent within .4 ms. (With the carriage located in a RL Position, use a small piece of paper to break the FPS Beam of Light).

TO ADJUST: Adjust screw on carriage motor governor for 11 ms between pulses. This adjustment must be refined in the write speed check adjustment.

(d) With the scope triggered as in test C, check to see that the BOL output at A3A15 starts at the center of the BOL input pulse at A3A17.

TO ADJUST: Turn potentiometer at 35 K.K. 42 of the BOL card.

(e) With the scope set the same as in test C, move the trigger to BOLA output, A3A15, check that the WS pulse, A3A16, occurs 8.5 ± .5 ms after the BOLA pulse.

TO ADJUST: Turn potentiometer at 35MM42 on the BOL card.

REASON: To provide line-find operation and indicate form position.

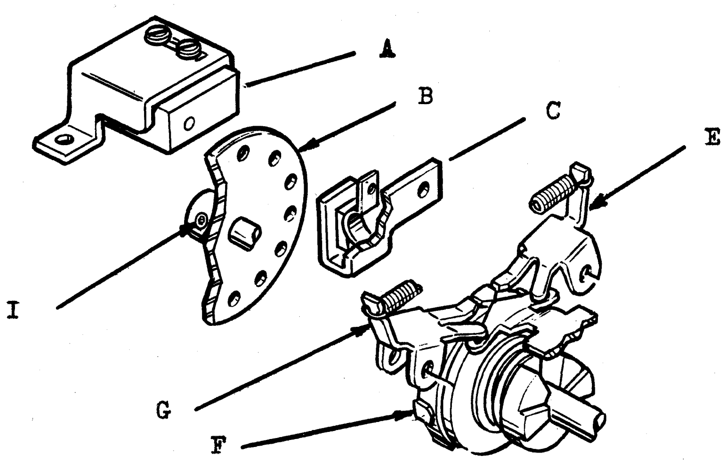


Fig. X-4

ADJUSTMENT OF CARRIAGE MOTOR SPEED

Before making this adjustment the 370 usec DMV should be checked for proper adjustment.

Using the output of OR gate B4A-10 (page 308) for an external trigger observe the relative position of the BOLB pulses during a W.L. operation (A5B-13) (page 308). You will notice some jitter indicating differences of motor speed. This should not be excessive. The governor spring on the carriage motor should be adjusted so the BOLP pulses appear 925 usec from the trigger of 27 (+ or - minus the jitter). Use time base of 20 usec/div.

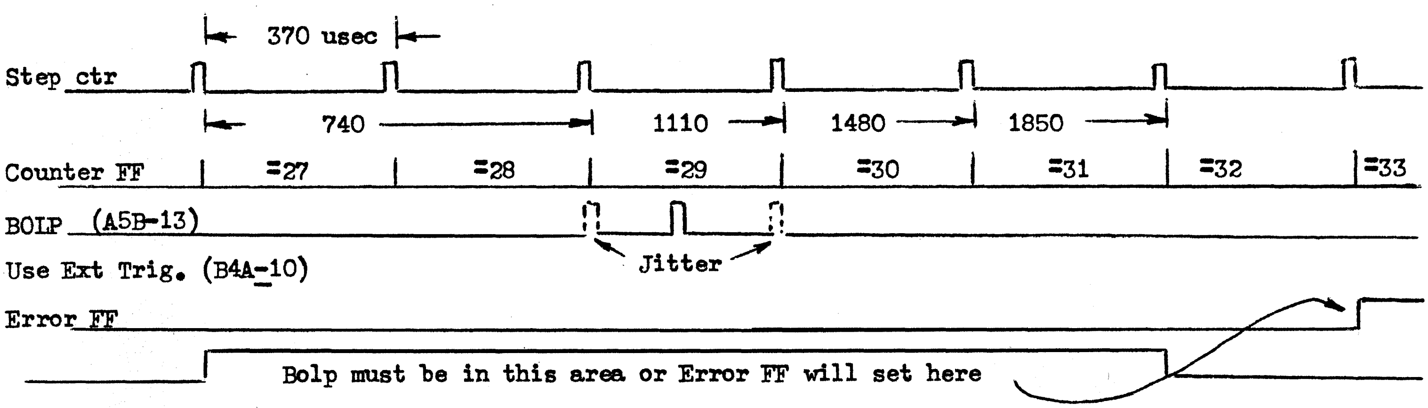


Fig. X-5

Speed check may be observed using a Write Ledger Operation or if so desired a continuous writer ledger may be jammed as follows:

Place a jumper from B3C-25 (page 310) and ground. This will jam WL high. Use the carriage motor and program camshaft service switches to place the camshaft at 288°. The motor and paper drive mechanism should now be running and the speed check can be observed. If governor adjustment is required, turn off the power, make the adjustment, resume power, and recycle the camshaft to 288°.

DATA DISCRIMINATOR X AND Y TIMING (490 us DMV). (FIG. X-6)

PREPARATION: (1) Obtain a form with good data encoded in the X and Y stripe. (2) If error FF is being set, connect the anode of a BCX58-1 to F3C-24 and the cathode (Red Band) to F3C-32 (04V). This will prevent setting the ERROR FF. (3) Set the scope trigger controls for external positive, AC mode. (4) Set time control to 50 us/division. (a) Trigger from set output of the discriminator FF (F4C-25 for X; F1D-6 for Y). (Page 309). (b) Observe the trigger signal and adjust the horizontal position control until the trailing edge of the pulse is at the center of the screen, FIG. X-6. (c) Observe the input to the DISC FF's Read AMP outputs. Place probe at F4B-19 for X or F2A-19 for Y. (d) With the carriage in a RL position, insert the form into the carriage. The data pulses will appear to the left of the center of the screen and the complement pulses will appear to the right of the center of the screen. The latest data pulse and the earliest complement pulse should equidistant from the center of the screen. (e) If pulses observed in D are not properly spaced, note position of pulses, return probe to the output of the discriminator FF.

TO ADJUST: Turn potentiometer at 32 X 39 on F4B for X or F2Y for Y to position the trailing edge of the discriminator pulse equidistant between the pulses mentioned in D. Remove diode installed in 2 above and read several ledger cards to check setting of the discriminator control.

If a dual trace scope is available both discriminator pulse and read amp pulse may be observed simultaneously by setting the pre amp display mode to chopped.

REASON: To insure optimum setting of data discriminator timing and minimize read errors due to read pulse timing variations.

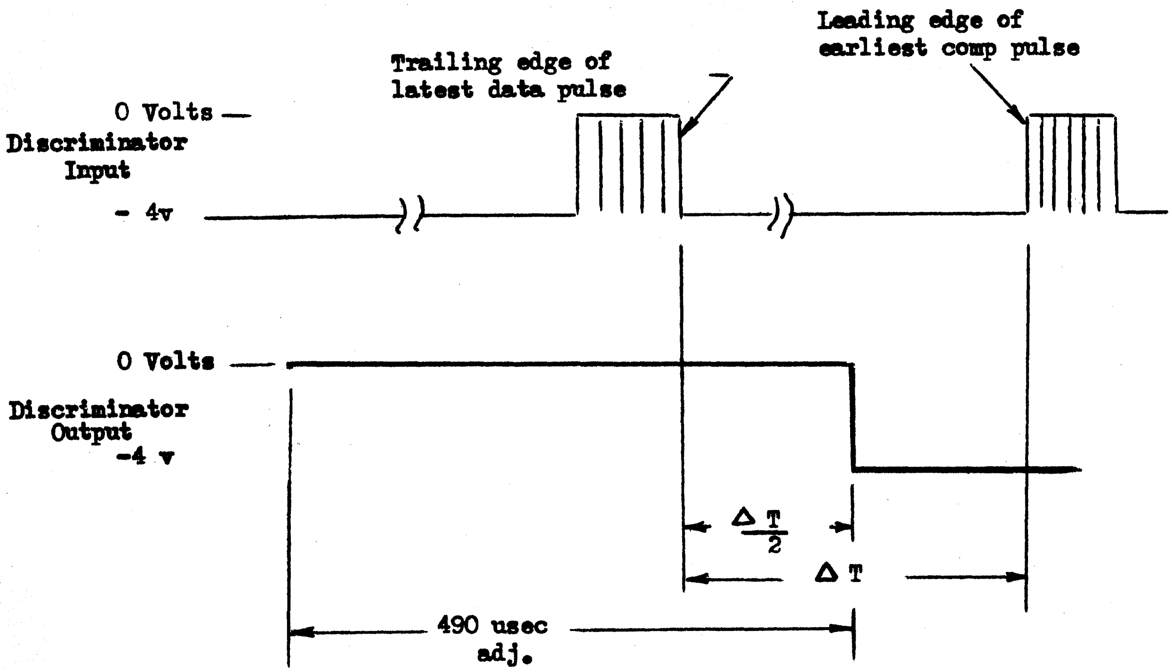


Fig. X-6

CARRIAGE OPEN

The voltage measured between TB2002-22 and TB2002-16 (Page 323) should be -4.12V.

With the carriage open the input to the carriage open switch amplifier (A2B-9) should be -50 MV ± 50 MV and the output (A2B-5) should be low, -4.4 ± .2V. With the carriage closed, the input to the amplifier should be -190 MV minimum and the amp output should be 0 $^{0}_{\pm}$ .2V.

REASON: To ensure proper lamp voltage and amplifier output for the carriage open signal.

MAGNETIC HEADS & READ AMPLIFIER ADJUSTMENTS (FIG. X-7)

The Form Guides must be set to cause the form to feed straight into the carriage and the stripes must be aligned with the heads before the following adjustments are made.

Place a diode between F3C24 and -4V. with the cathode at -4V. This prevents setting the ERFF.

A. Using a ledger card with several words of data encoded in the stripe, observe the head signal at the output of Read Transformer X. Set the scope for positive external trigger, .02V/div and 5 ms/div. Trigger on FF3X (D3C25) and probe the Read Transformer (A1C23 and A1C24). The signals should average 45 to 55 MV peak to peak with no individual pulses below 20 mv.

TO ADJUST: Loosen head clamp screw and move head forward or rearward as required.

B. Using a head alignment reference ledger card (Kit 1623 8230 - $.12) adjust the read heads for coincidental read.

To aid in alignment mark the initial position of the heads with a scribe mark across the top surface of the heads. Establish which pulse is being read earliest by using the scope as follows: Trigger on positive external, 2V/div and 20 us/div. Trigger at Read Amp X (B1A-11) (Page 316) and probe Read Amp Y (F2B-9). If no pulse is seen on the trace, this indicates that Y is leading X, and that the probe & trigger leads should be reversed. If no pulse is observed, repeat above with the sweep speed reduced.

TO ADJUST: When the lagging pulse is displayed on the scope, the other head should be adjusted forward or rearward so that the pulse starts within 50 us of the trigger signal.

C. The Read transformer outputs from both heads should now produce 45 to 50 mv average signals with no pulses less than 20 mv.

NOTE: If these amplitudes cannot be obtained, a sheet of soft pencil carbon paper should be folded over the form and inserted into the carriage. The impression left by the carbon will show whether the heads are tilted in relation to the form.

TO ADJUST: Loosen clamp screw and set head flat on the form. Do not move heads forward or rearward.

D. The line find pulse should produce a positive 25 MV signal.

To Observe: Use + ext trigger, 5 ms, 5MV/div. Trigger on the count of 4 and probe on B1D23 (page 306) using a ledger with one line of posting.

TO ADJUST: Loosen screw in the head clamp and move head forward or rearward as required. Be sure head is setting flat on the form.

The Read Amplifier Card (Page 316) should produce a -4 to OV pulse of approximately 45 us duration for each pulse encoded on the stripe.

Connect the anode of a BCX58-1 diode to F3C-24 and the cathode to F3C32 (-4V). Set scope for Ext. Trigger on FF3X, .02V per division, 2 ms per division. While reading a previously encoded form observe the inputs to the X Read amplifier at pin 23. This should be approximately 50 mv. Note the amplitude of the input signals. Change the scope to 2V per division and move probe to pin 15. The amplitude of the signal should be 60 times the input voltage (1.2 to 4.2).

TO ADJUST: Turn potentiometer at 35EE42 as required.

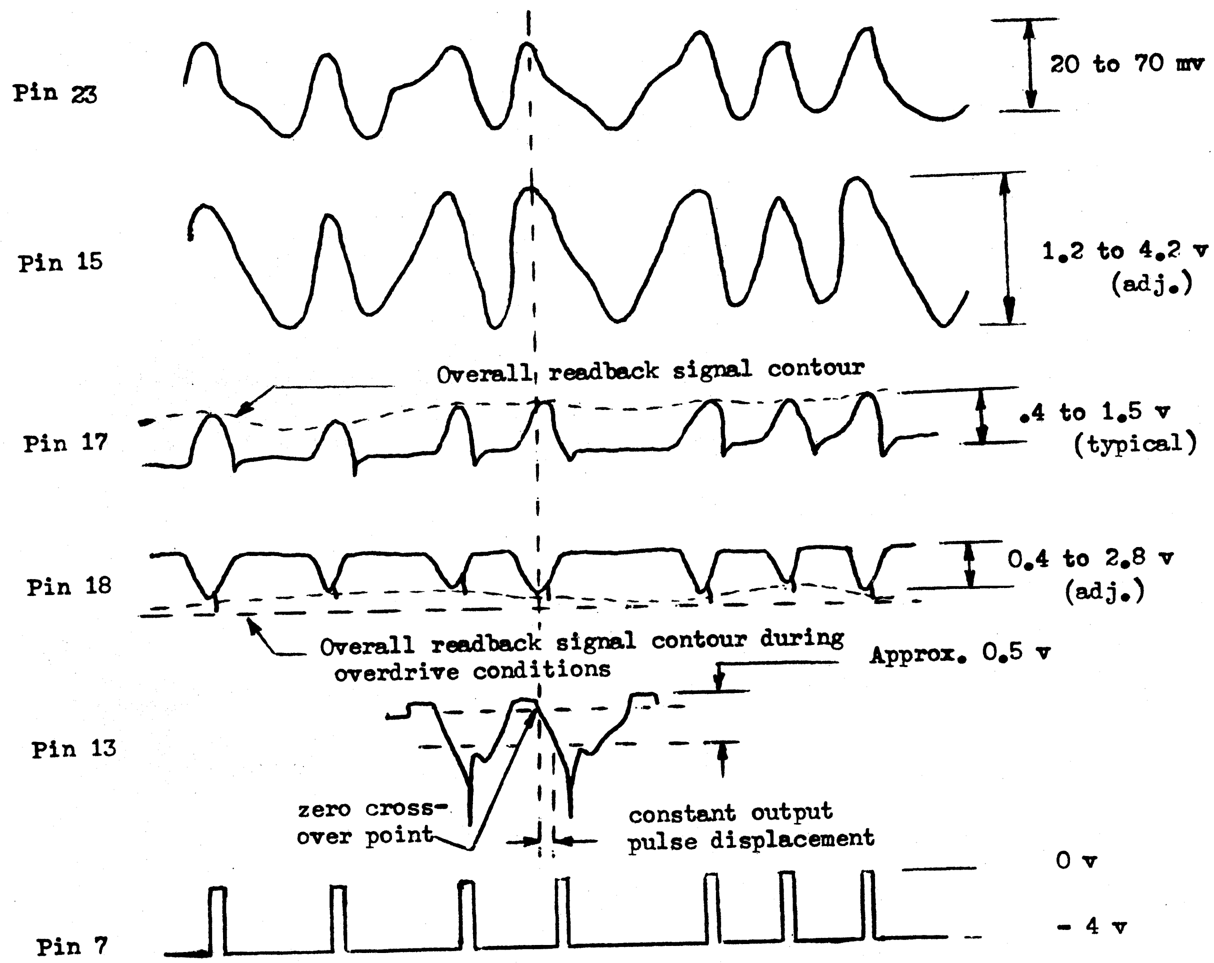
Move the probe to pin 17 of the amplifier being looked at. Positive pulses from .4 to 1.5V should be observed. No pulses should be less than .4 nor more than 1.5V. Observe the variation in amplitude of the various pulses.

Move the probe to pin 18. Negative pulses from -0.4 to -2.8 should be observed. They should be 2/3 of the amplitude of pin 15. Observe the variation in amplitude of pulses, the variation should be the same as in the previsous test. If the variations are not the same over amplification is indicated and potentiometer 35BB42 should readjusted.

Move probe to pin 7. A 4V, 40 to 45 us pulse for each pulse at pin 18 should be observed. The pulse at pin 7 should start at about the center of the pulse at pin 18. Any displacement of the pulse at pin 7 from the center of the pulse at pin 18 should remain constant for all pulses.

Perform the same test for the other 3 amplifiers.

REASON: To ensure optimum gain and threshold settings of read amplifiers and minimize read errors due to readback signal variations.



LINE COUNTERS DURING B C

During the Blank Card operation the counter FF's are advanced by the BOLP FF Pulses. When the counter has reached 43, per an eleven inch form, the SSFF will be set. The following BOLP, which is 12 us long, will reset the CLFF and trigger a RS pulse which resets the counter flip flops.

Fig. X-8 shows the wave forms for the counter FF's. These can be observed by triggering external on BOLP (D1C23) (Page 323), 2V per division, and 50 ms per division.

The counter FF Pattern will be the same for the speed check during the write ledger operation but will be stepped at the rate of the USMVFF frequency of 370 usec. It should never reach 32 on W.L. because the BOLP pulse will occur between the count of 27 to 31 to reset the counters.

A typical wave form chart of these counter FF's is shown below.

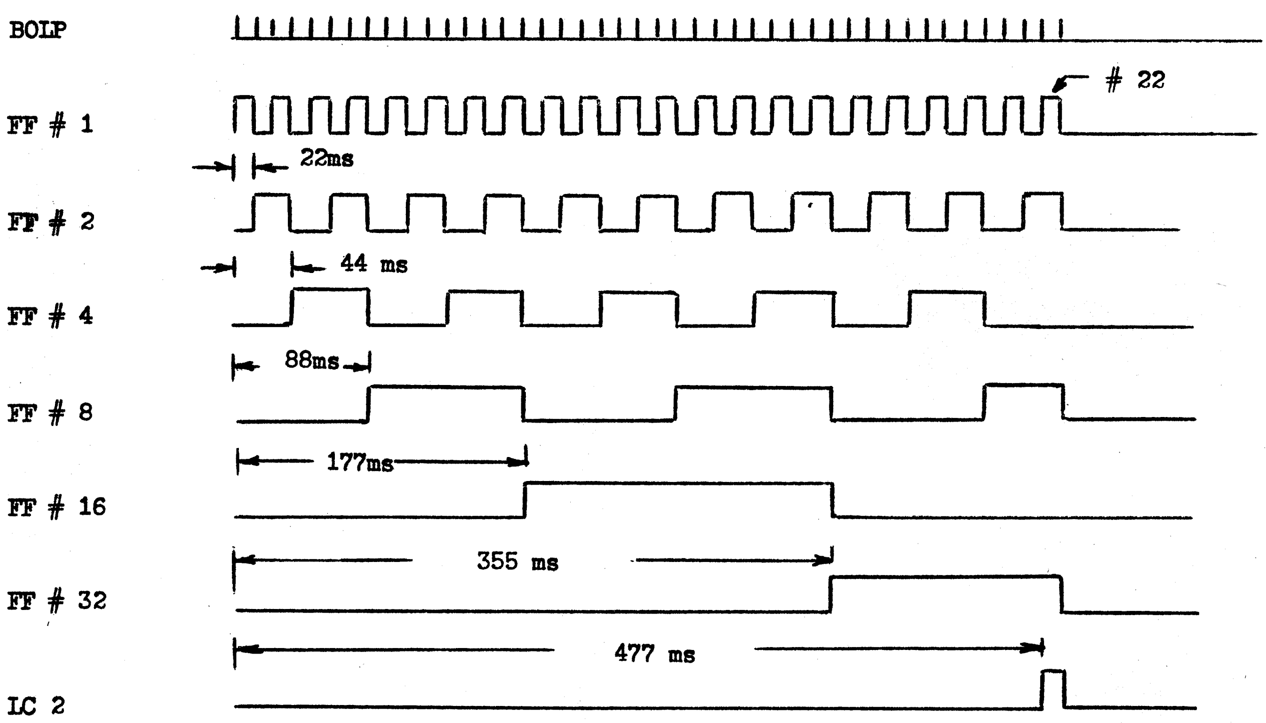


Fig. X-8

ALPHA TIMING ADJUSTMENTS

The typewriter timing camshaft speed is 296 usec/degree. One complete cycle is 107 ms.

The normal opening clearance of cams L, M, N, O should be .057" to .063".

The hole in the surface of cam L is a reference mark for the normal position of the section. The top edge of the hole should be aligned with the upper edge of follower arm F. Plate J may be rotated for fine adjustments of this section.

Screws G may be adjusted to obtain:

	MAKE	BREAK	PULSE LENGTH	OCCURENCE LIMITS
Cam L	40^o	80^o	$40^o \pm 3^o$	$\pm 3^o$ ON MAKE
Cam M	168^o	208^o	$40^o \pm 5^o$	$\pm 5^o$ ON MAKE
Cam N	50^o	70^o	$20^o \pm 3^o$	$\pm 5^o$ ON MAKE
Cam O	200^o	335^o	$135^o \pm 5^o$	$\pm 5^o$ ON MAKE

Kit 440 (timing dial guage) may be adapted to this unit by modifying the Kit 440-1 screw or substituting a FX60-213 screw to fit the threads of shaft E.

The screw (Kit 440-1) may be modified by placing a short piece of spaghetti (FX415-1) onto its threads.

The FX60-213 screw may be substituted for the Kit 440-1 if a 46 nut is placed all the way onto its threads.

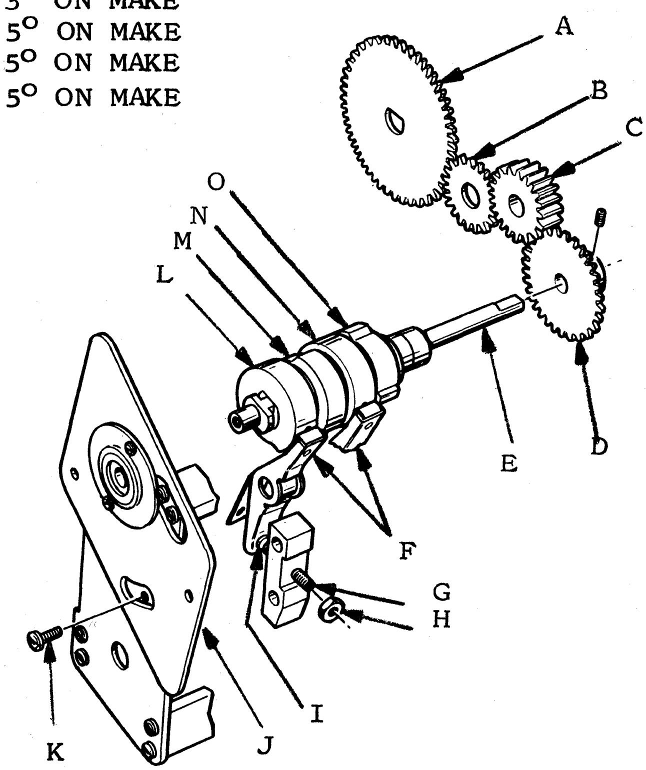


Fig. X-8-1

Timing cams L and M should be refined within their tolerances for a minimum of 37 ms and maximum of 41 ms from the make of Cam L to the make of Cam M. (This is critical on A520 five channel punching.)

TROUBLESHOOTING TYPE-OUT-OF-MEMORY

1. Remove wire from TB903-X8 (Page 510).

2. Cycle the printer in T.O.M. programmed position. Printer should now be locked with T.O.M. Relay Picked.

3. At this time the typewriter solenoids, MRFF's and WRFF's may be observed to check their correct functioning from reading DD1 of the desired memory.

4. Each subsequent cycle may be initiated by releasing the clapper of L6 (Typewriter Trip Solenoid) manually.

5. At the end of each typewriter cycle all pertinent functions may be observed and checked with a 310 meter.

CAUTION: A machine print of the numeric information stored in memory for typewriter coding may not be the same as the binary bit information. EXAMPLE: A digit in an odd memory contains a 2-4 and 8 bit. This digit causes a tab 4 during a type-out-of-memory operation. However, the first numeric print out of this digit is "zero". The second print out is 4.

Examination of each digit in memory using the above single cycling of type-out-of-memory is the only true way of detecting the stored binary information.

OBSERVATION OF TYPE-OUT-OF-MEMORY SIGNALS

Figure X-9 shows typical signals that may be observed during T.O.M. These signals are typical and should not be used as adjustment reference. (NOTE: These signals are from a positive escapement carriage type machine.)

PROCEDURE:

1. Externally sync the oscilloscope on BEFF (Page 140) using 20 ms/div.

2. With each digit of the memory loaded with the same binary information observe the signals shown during type-out-of-memory.

3. Closer observation of leading edge signals may be observed using INT triggering.

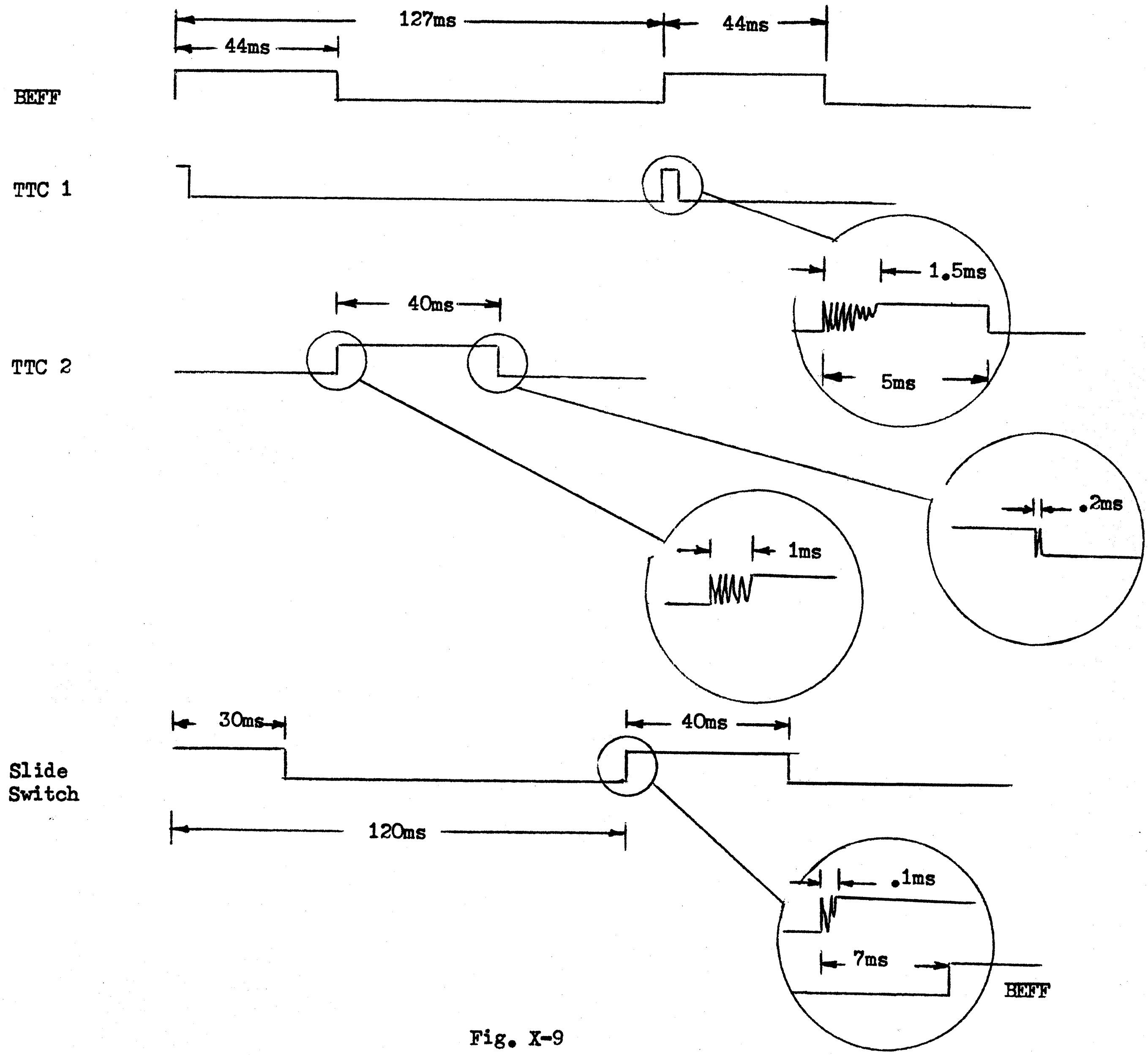


Fig. X-9

CONTINUOUS "WRITE LEDGER" OPERATION

The Write Ledger Operation can be made to write continuously from one machine cycle. The Write Operation can be a one word write, except word 20, or a 10 word write. To initiate the continuous writing of one word perform the following:

1. Locate the carriage in a Write Ledger position (A #7 pin in lane 48).

2. Remove the acrobat connection at A5C-20 (L.G.) $\overline{1 \rightarrow WR}$ SL (Page 318).

3. Depress MB2 and as the form comes out insert a narrow piece of paper to keep from dropping FPS. The Memory Address programmed in the panel will be written continuously.

4. Place a jumper wire from B3C-25 (WLFF) to ground. This will allow power to be turned off and on without losing the operation.

SRCX=0 is a convenient sync point to trigger on to observe W.L. functions.

To initiate the continous writing of 10 words perform the following:

1. Locate the carriage in a WL position.

2. Remove the acrobat connection from B5C09 (Page 310).

3. Place a jumper wire from B5C09 to -4 (Pin 32). This will prevent the MARU=0 signal from coming high to set FF1X or FF1Y.

4. Depress MB2 and as the form comes out insert a narrow piece of paper to keep FPS high.

A convenient sync point to observe all 10 words is B3D-20 (Page 310). This will start with MARU=8.

ONE WORD NORMAL WRITE

It may be desirable to cause a normal one word write without changing the magazine in the control unit.

One word writes simplify the numer of signals used. ONE CAUTION: One word writes will not detect parity problems such as parity flip-flops setting during writing of the DDO pulses on each word except word 20.

PROCEDURE:

Attach a jumper wire from D6A-17 (Page 116) to D1D-11 (Page 128). This will cause the MARU Flip-Flops to reset during sequence A of WL.

OBSERVATION OF MONITOR PULSES

Monitor pulses during W.L. may best be observed by jamming the machine into a continuous W.L. mode and observing the typical pulses shown in Figure X-10.

PROCEDURE:

1. Place machine in a continuous W.L. mode.

2. EXT sync the scope on either write X (E1D-21) page 311 or write Y (F2B-27) page 311 and observed the appropriate pulse as shown. Head current change may be seen on either write amplifier at pin 18.

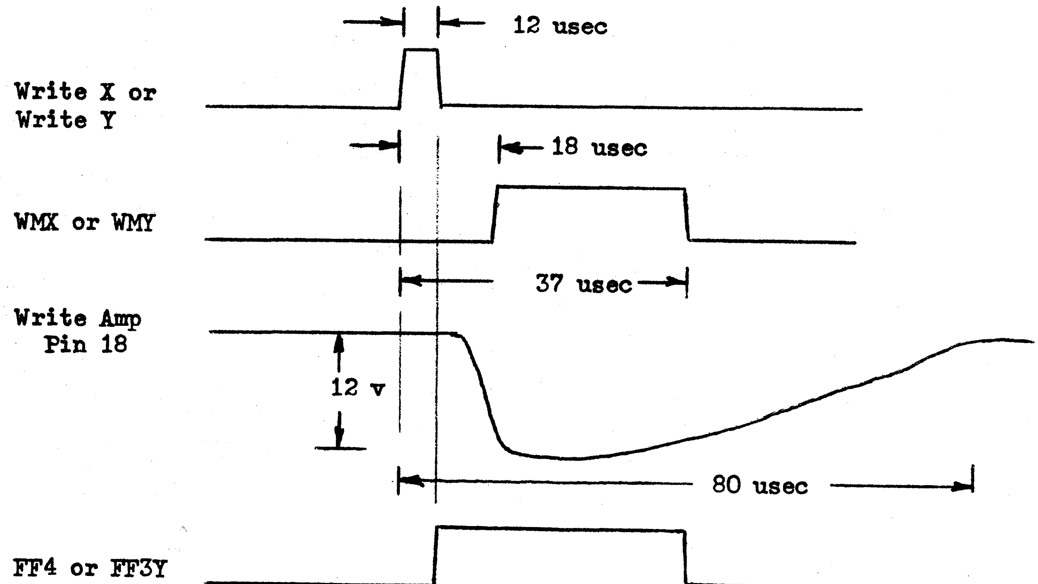


Fig. X-10

STRIPED LEDGER TIMING CHARTS

The following three timing charts contain the majority of the signals used during Read and Write of forms. These charts are what you should expect to see when scoping these signals except for the condensation of certain signals that was necessary to keep these in a usable size.

The first chart Figure X-11 deals with the start of Write Ledger as the counter flip-flops are changing from 5 to 6. It must be remembered that the start of Write Ledger is not synchronous with the USMV flip-flop, therefore, some pulse displacement will be seen when using WLFF for a sync pulse.

The second chart Figure X-12 deals with the end of Write Ledger starting with DD11. A good sync point to use to observe the end of W.L. is FF1X, FF1Y, or FF3X. Before using these they should be checked to see if they are timed correctly with the start of W.L.

The third chart Figure X-13 deals with Read Ledger. The RLFF is a good sync point to observe many signals during read, however, it must be remembered the paper will have to move about 3/4" before pulses will actually be read.

START OF WRITE LEDGER

WRITING A 9 IN COL. 12 OF MA 29 AND WRITING A 6 IN COL 12 OF MA 39.

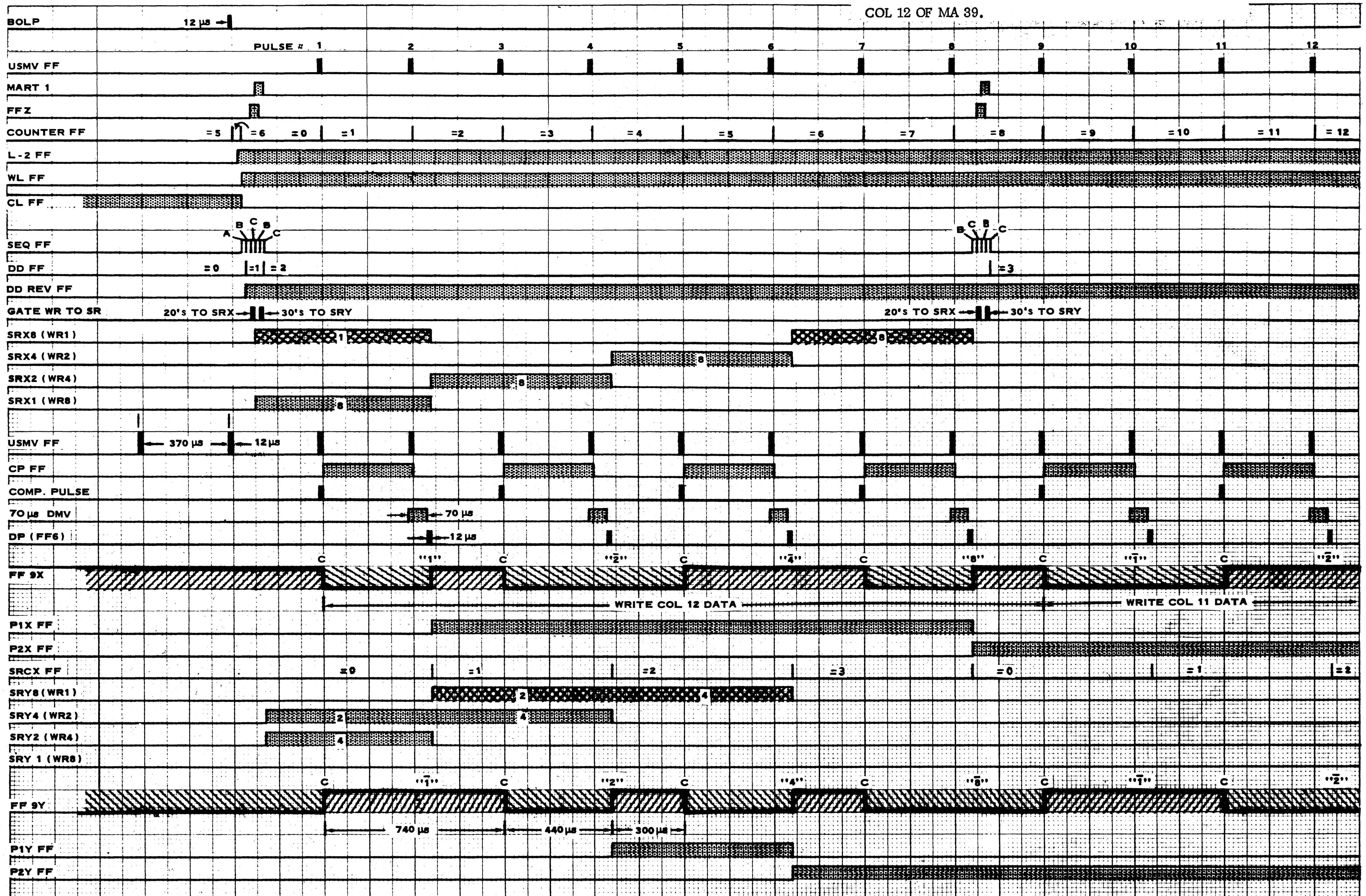


Fig. X-11

END OF WRITE LEDGER

OPERATION STARTS IN DD11 WITH REV FF HIGH.
MA20 = .75+
MA30 = .30-

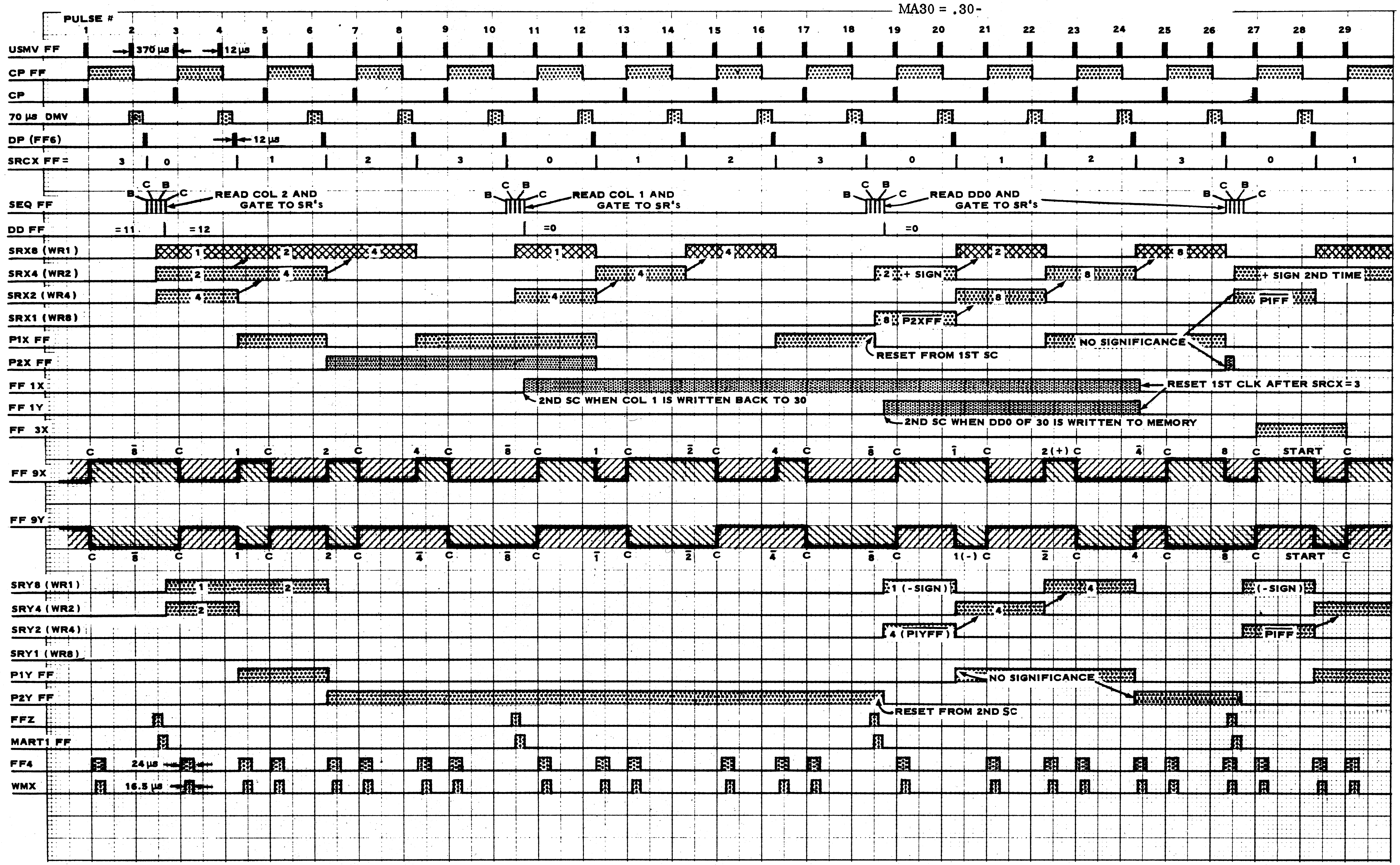


Fig. X-12

READ LEDGER

FORM ENCODED TO READ .75+ TO MA20 AND .30- TO MA30.

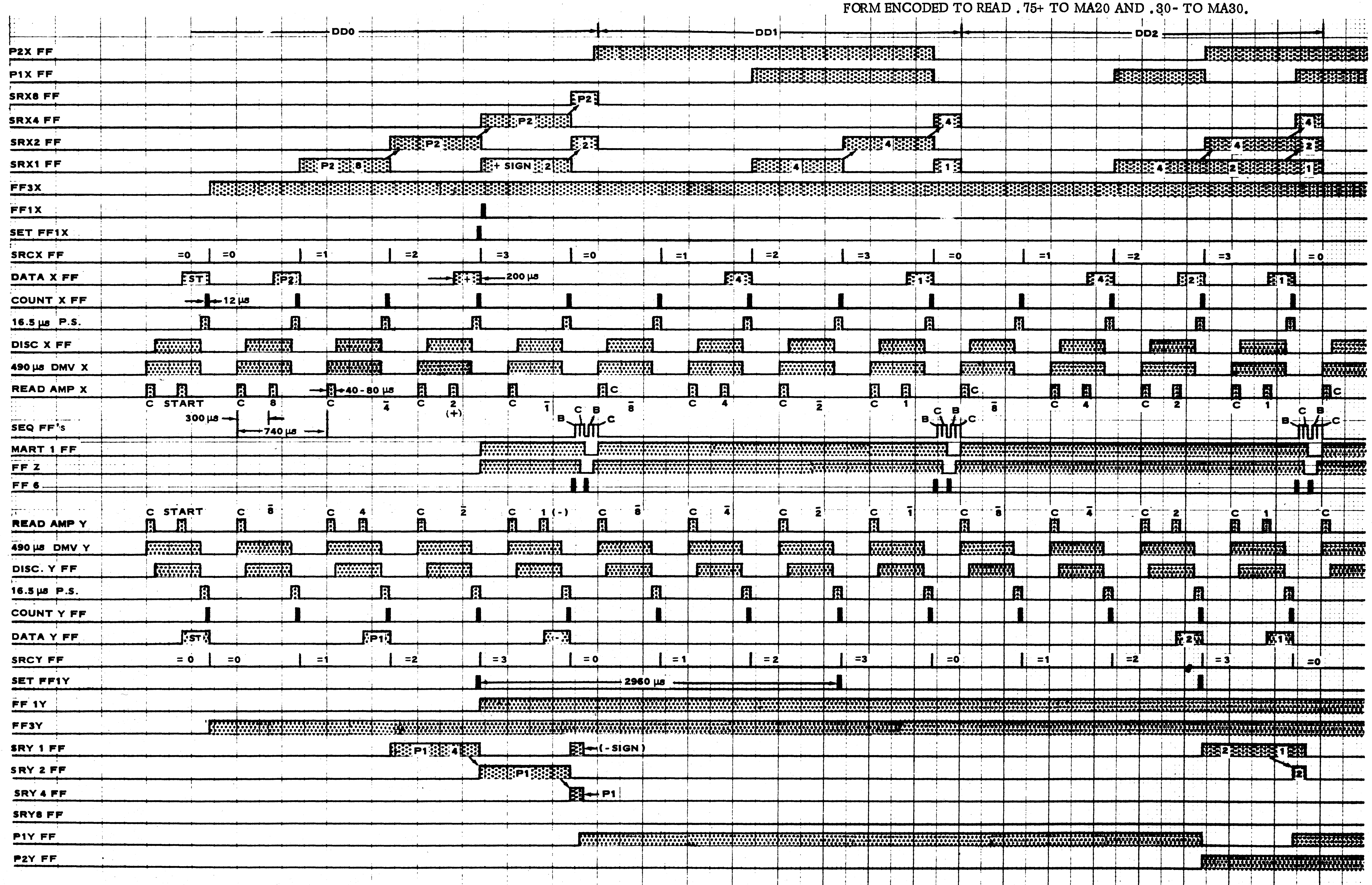


Fig. X-13

TROUBLESHOOTING LINE FIND

Line find problems may be caused from a faulty write of the pulse or a wrong drop of the paper drive after reading the pulse. The largest share of problems are due to screws coming loose in the paper drive mechanism.

The pin catcher tray should be removed and all screws in the BOL disc and pressure roll shaft gears should be thoroughly tightened. The 1/10" wheel contains two screws, one on top of the other. The top one must be removed to tighten the lower one on the shaft. (See Adj. Page 11)

Figure X-14 shows the relative positions of the first print line, sync pulse and line find pulse as should be written on a W.L. following a blank card operation

The first print line as shown in Figure X-14 may be adjusted by positioning the carriage tray forward or rearward as required. To adjust, loosen the 5 screws in the top front of the tray, the four screws located in the side mounting blocks and the two screws at the rear corners.

Extreme care must be taken to keep the tray square with the form. This should be checked against a printed line near the bottom of the form when the form is limiting on the pusher fingers. Pushers fingers should never be adjusted.

NOTE: When removing a tray for service work always remove the lower four screws from the front of the pan. This will allow dowel rod positioning on reinsertion thus eliminating any change of first line print adjustment.

Determination of a correctly written line find pulse must be made by dusting the card. Scoping may be done to determine the possibility of extroneous WS pulses prior to moving the form.

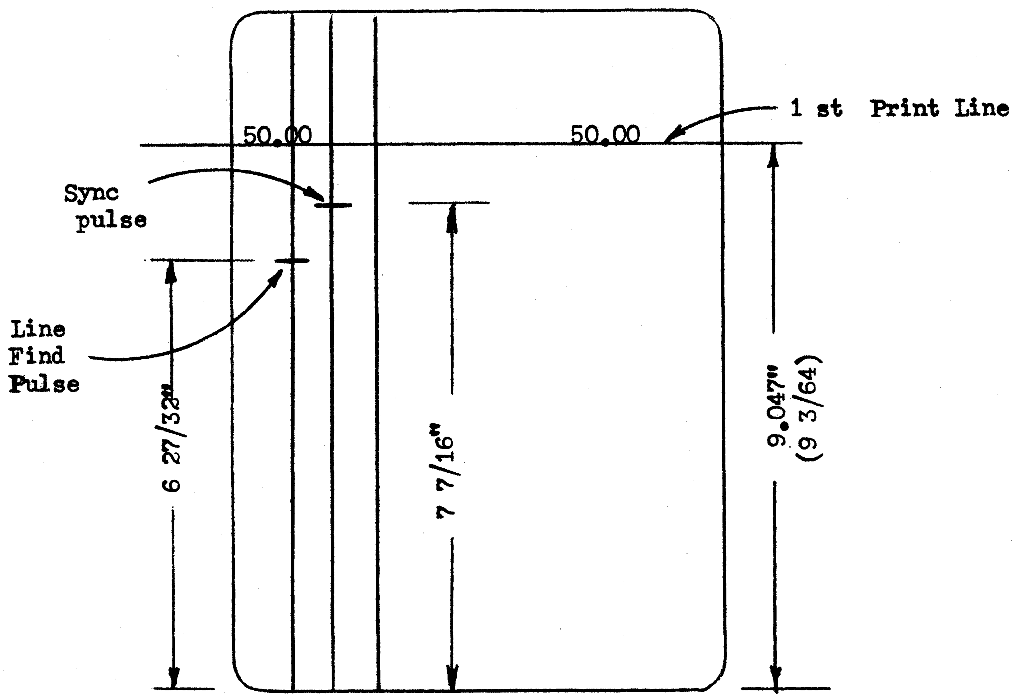


Fig. X-14

The exciter lamp for the BOL disc must have the filament placed in a horizontal plane to prevent the possibility of WS pulses as the carriage is overthrowing and rebounding in a WL stop position. These lamps (1522 4710) are marked with a red dot to indicate the horizontal position of the filament. The lamp should be positioned with the red dot at the top.

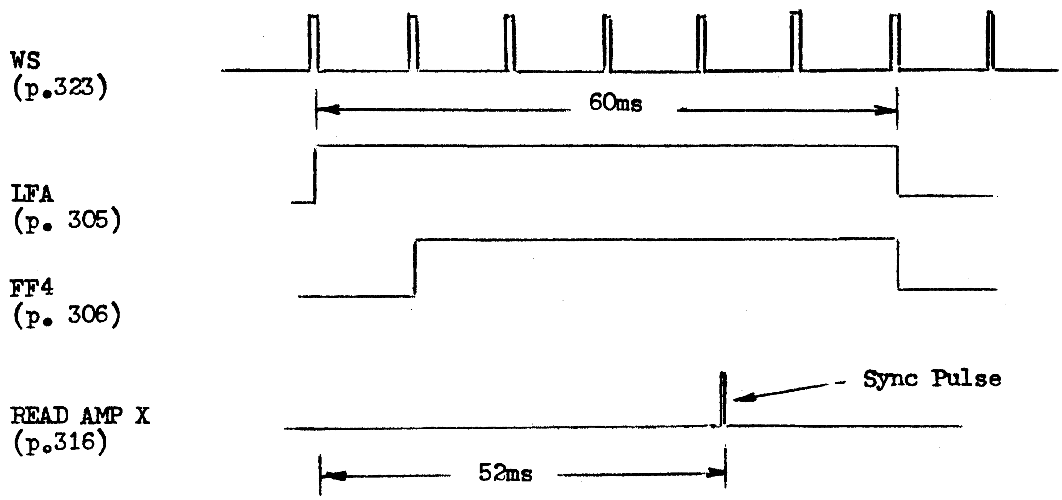
Relative timing of the Line Find Operation is shown in Figure X-15.

The top sequence of signals shows the relative time involved to set LFA, FF4, and the reading of the sync pulse using the first WS pulse on W.L. as the external scope sync.

If the first WS pulse is produced after the form moves 1 9/11 lines, the sync pulse should be read at approximately 52 ms as shown. (Starting at line #1.)

STARTING AT LINE # 1

WS (A3A-16) as EXT. SYNC



STARTING AT LINE #2

READ AMP X as EXT. SYNC

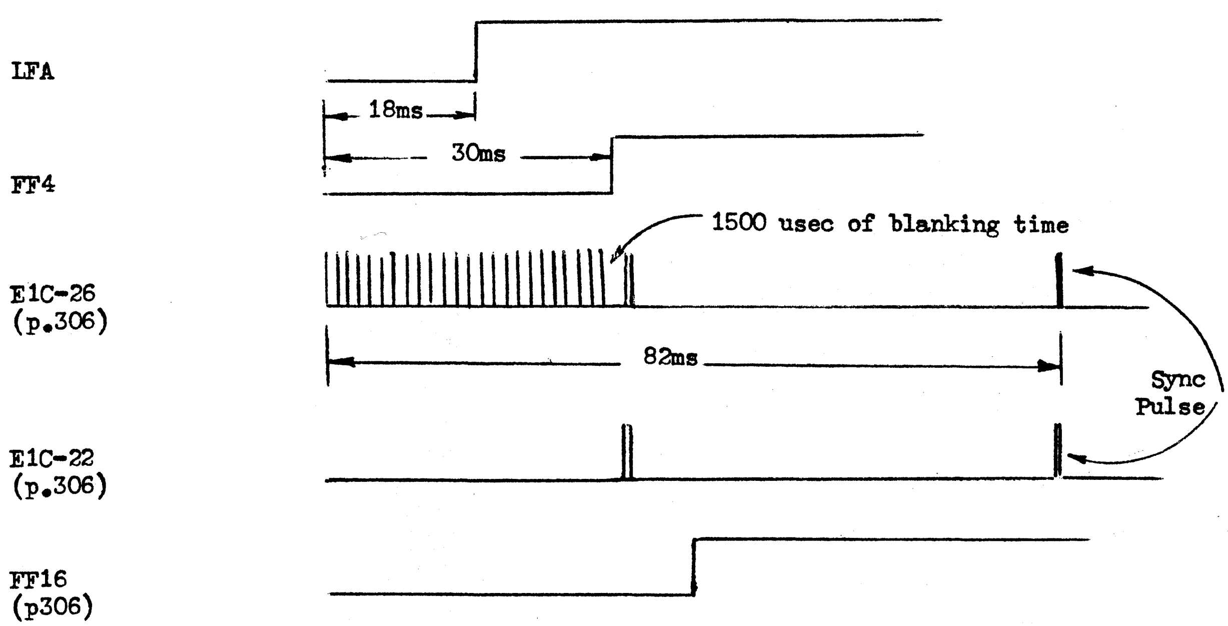


Fig. X-15

The lower sequence of signals on Figure X-15 shows the relative time involved to set LFA, FF4, and the reading of the sync pulse starting at line #2, and using the first Read Amp X as an external scope sync. The relative settings of LFA and FF4 could be observed this way starting at any line. This method should detect an early setting of LFA due to a premature WS pulse.

Note the narrow margin of safety when writing a ledger from this second line. This is due to the fact the form must move 2 9/11 lines before FF4 sets which controls the gate E1C-22. A late WS pulse or an operator variable form realignment at line #2 could cause a delayed setting of FF16 (6 ms after reading the sync pulse). This would cause the form to drive to line minus 10 and all data writing would now start higher on the form. Once such written, the form will continue to drive to line -10. This does not create a problem in the E2150; however, if the form is used in the A4002, the high speed rollers will increase the sheet speed before reading is finished and a "Read Light" may develop on the last word being read from the form.

INDICATOR LIGHTS ON STRIPED LEDGER STYLES

There are six indicator cards in each E2150 style system. Four in the upper gate and two in the lower. The two cards in the lower gate may be wired one of two ways. The early style systems are wired as per the drawing on page 17 of Sec. VIII.

Starting with serial E4136 the lower gate was modified to indicate certain flip-flops to be used in analysis of Read and Write Errors. Along with this two logic changes were made to prevent resetting these key flip-flops as the paper drive resets on Read, or the camshaft cycles home on write errors. These changes are shown below. The change on page 307 prevents the R1 reset signal once the Error FF is set. The change of page 308 prevents resetting the counter FF's during W.L. if ERROR is set. Thus a speed check may be observed.

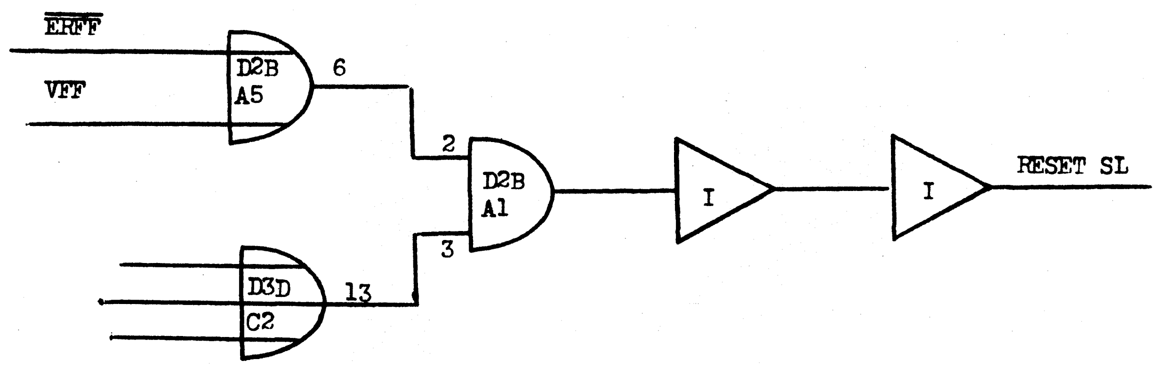


Fig. X-16 Page 307

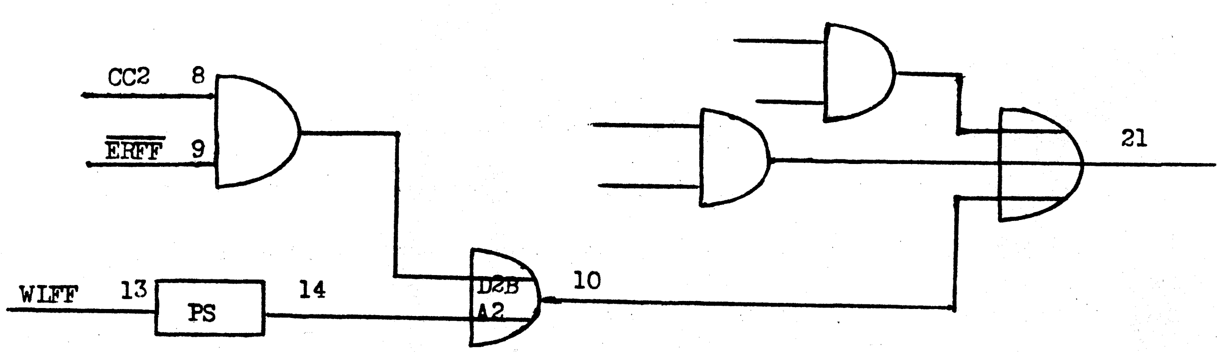


Fig. X-17 Page 308

The indicator cards at E1A and F1A on the lower gate are now wired as shown:

Ind.	E1A	Pin #1	F1A
8	FF16		FF1X
7	32		FFZ
6	P2X		P2Y
5	P1X		P1Y
4	SRCX 2		SRCY 2
3	SRCX 1		SRCY 1
2	SRX 2		SRY 2
1	SRX 1		SRY 1
		32	

Certain formulas have been worked out to help analyze problems without the aid of an oscilloscope. These are to be used in conjunction with other means of determining the source of problems. Do not over look the importance of some of the upper gate indicators.

WRITE LIGHTS

There are three possible write indications:

1. FF32 = SPEED CK.
2. SRCX ≠1 = COUNT PROBLEM
3. X or Y MONITOR PROBLEMS

1. Counter flip-flop 32 high indicates a speed check. (page 308)

The form might be dusted in this case to determine if the error occurred early in the 1st WD. (½ inch/wd.) If so, there's a possibility the counters were not reset at the beginning of Write Ledger.

Speed Check lights are caused by improper motor speed, improper governor control, loose BOL disc, loose paper drive members, or 370 ms DMV.

Governor problems are mostly caused by a binding fly weight arm. The spring should be removed and the following items should be checked:

a. The copper "keeper" should not exert pressure on the hub of the arm.

b. The fly weight arm ear (that extends into a hole in the insulated disc) should not bottom or rub on the edge of the hole.

c. The contacts should meet squarely.

d. If a relatively stable speed cannot be obtained, remove the reduction gear assembly, disassemble, and check for freedom of the gear drive and bearings.

e. Check all gears and bearings in paper drive for freedom and lubrication.

2. SRCX $\neq$ 1 when the form leaves FPS.

This error may happen one of two ways. The first is a failure to read the sync pulse and the form ejects out the rear of the tray. The second is an actual failure of the counter flip-flops to end up with the count equal to one at the end of Write Ledger.

CAUTION: A monitor problem could also leave the SRCX counter not equal to one. If this is suspected block the FPS with a small piece of paper as the ledger is returning on W.L. If the error light does not go out and the counter is not equal to one, it is a monitor problem. (SRCX $\neq$ 1 can only set ERFF with $\overline{\text{FPS}}$.) Do not overlook the possibility of losing FPS during write.

3. Monitor Problems:

These will be the most difficult to pin point without the use of a scope. One such method is present in Fig. X-18.

Attach a jumper from one of the two monitor OR gates D2C-13 or G3C-1 on page 321 to a spare flip-flop as in illustration A of Figure X-18. Once the detection is made as to the X or Y stripe the spare FF may be used to determine which two signals are coincidental as in illustration B.

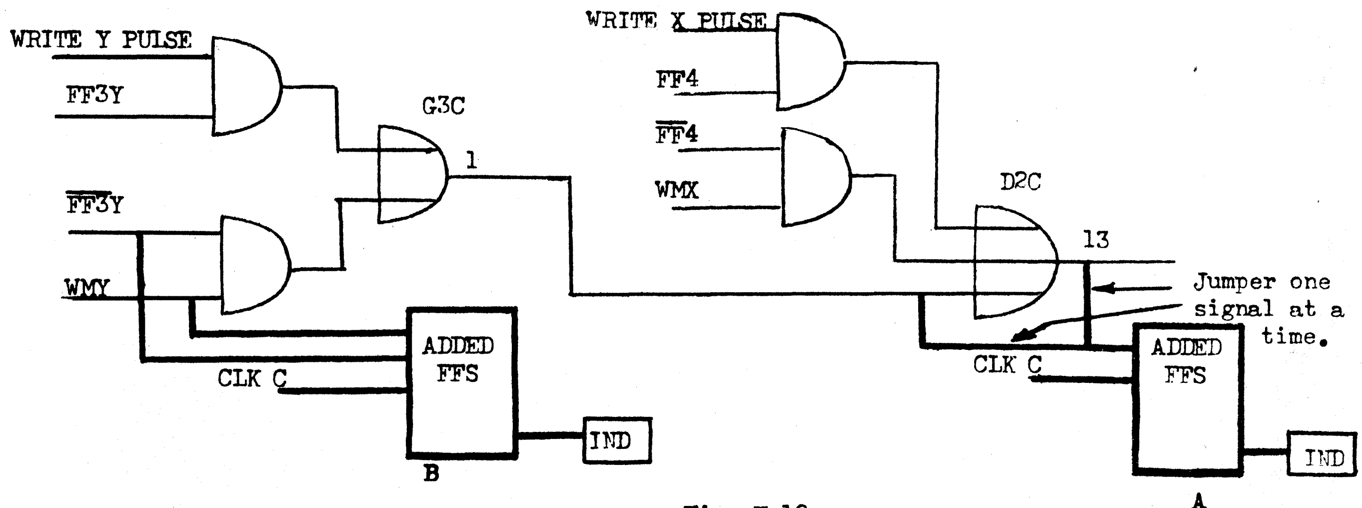


Fig. X-18

Monitor or count problems may best be solved by jamming the logic into a continuous "write" mode. Tapping and moving the gate or carriage tray connection may prove beneficial at this time.

READ LIGHTS:

There are 7 possible Logic Read indications.

1. $FF16 \cdot (SRCX + SRCY \neq 1) =$ Count Problem.
2. $FFZ \left[(FF1X \cdot DDMSD) + (\overline{FF1X} \cdot DDO) \right] \cdot \left[(\overline{P1X} + \overline{P2X}) \right] =$ X PARITY.
3. $\overline{FFZ} \left[(\overline{FF1X} \cdot DDMSD) + (FF1X \cdot DDO) \right] \cdot \left[(\overline{P1Y} + \overline{P2Y}) \right] =$ Y PARITY.
4. $FFZ \left[(FF1X \cdot DDO) + (\overline{FF1X} \cdot DD1) \right] \cdot \left[(SRX1 \cdot SRX2) + (\overline{SRX1} \cdot \overline{SRX2}) \right] =$ X SIGN.
5. $\overline{FFZ} \left[(\overline{FF1X} \cdot DDO) + (FF1X \cdot DD1) \right] \cdot \left[(SRY1 \cdot SRY2) + (\overline{SRY1} \cdot \overline{SRY2}) \right] =$ Y SIGN.
6. $\overline{FFZ} \cdot FF1X \cdot SRCX1 \cdot SRCX2 \cdot SRCY{=}0$ = SKEW WHEN X WAS LEADING Y.
7. $FFZ \cdot \overline{FF1X} \cdot SRCY1 \cdot SRCY2 \cdot SRCX{=}0$ = SKEW WHEN Y WAS LEADING X.

A number of variables may cause the Read Error to illuminate during Read. Low amplifier amplitude or pulse spacing may occur at any given time; therefore the formulas as stated may not always indicate a positive condition.

EXAMPLE: A misadjusted amplifier or worn Read Head may cause a loss of a data pulse on one read showing up in the sign area. The same form on another attempt may for the same reason on another pulse, show up as a parity error.

These variations must be considered when analyzing "Read Lights".

1. Count Problems

FF16·SRC COUNTERS NOT EQUAL TO ONE.

This indicates that the cell counter Flip Flops did not end up in their correct relation at the End of Read.

A change in logic (Fig. X-19) prevents FF16 from setting on other read errors as the form is being stopped.

After all pulses have stopped coming thru the amplifiers and FF16 is allowed to set, a check of the X and Y counter FF's is made.

2. X Parity

$$FFZ \left[(FF1X \cdot DDMSD) + (\overline{FF1X} \cdot DDO) \right] \cdot \left[(\overline{P1X} + \overline{P2X}) \right] = X\ PARITY$$

X Parity errors may occur on the leading or lagging word being read from the stripe. If X were leading Y, FF1X will be illuminated. If so, logic sequence B to set Error will be reached in DDMSD with $\overline{FFZ}$. If both Parity FF's are not high during sequence B, Error will set. At the end of sequence B $\overline{FFZ}$ will be complemented. The DD's will not step out of MSD because this is the leading word. If X were lagging Y, $\overline{FF1X}$ will be true, therefore, as Error is being set at the end of Sequence B a Sequence C is also set which will step the DD's to DDO.

3. Y Parity

$$\overline{FFZ} \left[(\overline{FF1X} \cdot DDMSD) + (FF1X \cdot DDO) \right] \cdot \left[(\overline{P1Y} + \overline{P2Y}) \right] = Y\ PARITY$$

The logic for Y parity errors is the same for X parity errors.

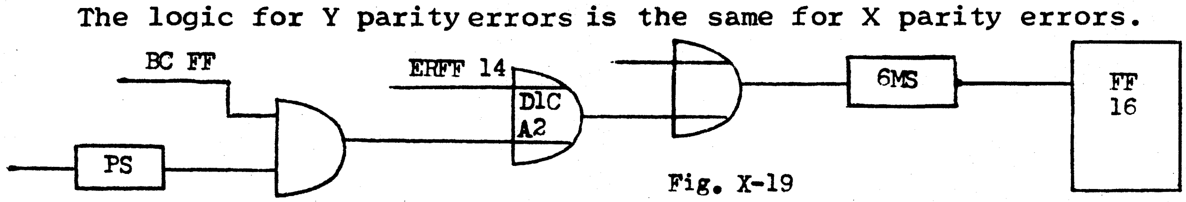


Fig. X-19

4. X Sign

$$FFZ\left[(FF1X\cdot DD0)+(\overline{FF1X}\cdot DD1)\right]\cdot\left[(SRX1\cdot SRX2)+(\overline{SRX1}\cdot\overline{SRX2})\right] = X\ SIGN$$

X sign errors may occur on the leading or lagging word the same as parity errors.

The logic for stepping the DD's is the same. If the X stripe is leading, the DD will not step out of DD0. $\overline{FFZ}$ will again be complemented at the end of sequence B. (FFZ indicates the X stripe is being handled first.)

If the X stripe is being handled last, the DD's will again step to DD1 from the automatic sequence C as Error is setting.

5. Y Sign

$$\overline{FFZ}\left[(\overline{FF1X}\cdot DD0)+(FF1X\cdot DD1)\right]\cdot\left[(SRY1\cdot SRY2)+(\overline{SRY1}\cdot\overline{SRY2})\right] = Y\ SIGN$$

The logic for Y sign errors is the same for X sign errors.

6. Skew when the X stripe was leading the Y stripe.

$$\overline{FFZ}\cdot FF1X\cdot SRCX1\cdot SRCX2\cdot SRCY{=}0 \quad = \quad SKEW\ WHEN\ X\ WAS\ LEADING\ Y$$

FF1X indicates the X stripe was being handled first. $\overline{FFZ}$ will be true due to the fact that the original lagging signal will be setting FF6 and sequence B before the Error FF is being set to drop RL as shown in Fig. X-20.

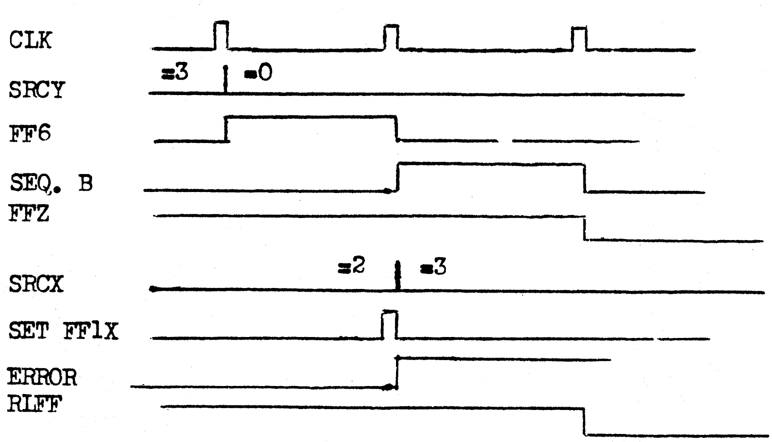


Fig. X-20

SRCX = 1·2 because the set FF1X signal counts the counter to 3.

SRCY=0 because the Y stripe was accelerated two cells earlier than the X stripe after determination was made that the X stripe was the earliest.

7. FFZ·FF1X·SRCY1·SRCY2·SRCX=0 = SKEW WHEN Y WAS LEADING X

The logic for Skew errors when the Y stripe was leading the X is the same as for X leading Y.

Skew errors should be handled in the following manner:

a. Clean the pressure rolls and heads with platen restorer.

b. Lubricate the pressure roll shaft bearings.

c. Adjust, if necessary, the upper pressure rolls for straight tracking of the form in the guides.

d. Using the head alignment ledger card follow the procedure as outlined in Sec. X, page 16.

e. Align plastic form guides with form guides on tray.

SERVICING THE HYSTERESIS CARRIAGE CLUTCH

The hysteresis clutch is a non frictional contact clutch. It is composed of 3 non oriented ceramic rings that are permanently magnetized into eight segments. Each ring is separated by a vicalloy disc with a .008" to .015" air gap. The vicalloy disc has the magnetic ability to maintain its position in the segmented field. Positioning of the center ring magnet determines the clutch output torque. Output torque is also determined by air gap between the vicalloy disc and rings.

It is very important that the disc and magnetic rings are free of dirt before assembly. Equally important is a proper air gap. The air gap is a built in factor, however, it may be destroyed if screws C, Fig. X-21, are not torqued down evenly after an adjustment.

Clutch output torque is precisely adjusted at the factory. Barring any problems with the ball bearings, the output torque will remain constant at all temperatures for an indefinite time. The clutch should require no maintenance.

To check the output torque:

1. Remove all horizontal chains or belts from the left driving sprockets.
2. Loop a string around one of the nuts on screws C and rotate the clutch until 2 or 3 wraps have been made around the outer circumference as shown in Fig. X-21.
3. Block the movement of the clutch output chain at A.
4. Attach a 0-32 oz. scale (1623 0609) and pull the scale as evenly as possible towards the rear of the machine. The output torque should be 18 to 19 oz. for side insertion machines. The output torque should never be adjusted to exceed 19 oz.

If necessary, adjustment is made by positioning the center ring D. The direction of movement depends on orientation of the magnetic fields during assembly. The amount of movement depends on the air gap and the magnetic strength of center ring B.

Service replacement clutches will have an arrow denoting the directional movement of ring B for more output torque.

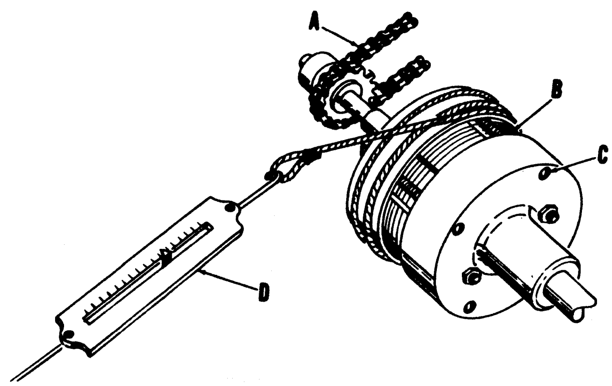


Fig. X-21

PROGRAM DEBUGGING

A method is presented here to assist initial program debugging on E2100 systems. This may be installed temporarily or permanently as an analysis aid.

1. The first requirement is to be able to operate the printer in any of the 220 carriage positions.

PROCEDURE: Attach a wire from the open contact of MB#3 switch to the common of a double throw double pole toggle switch as shown below. Attach the normally open of this switch contact to TB760B-X2. This will parallel switch S770 and will allow a printer operation in any position including AEC positions.

2. The second requirement is to block the LN3 set ups which, if allowed, will cause a double operation when using bar 3 with repeat programmed.

PROCEDURE: Remove one wire from the lane 3 solenoid and attach to the common of the other switch pole. Attach a wire from the normally closed switch contact to the open terminal of the lane 3 solenoid.

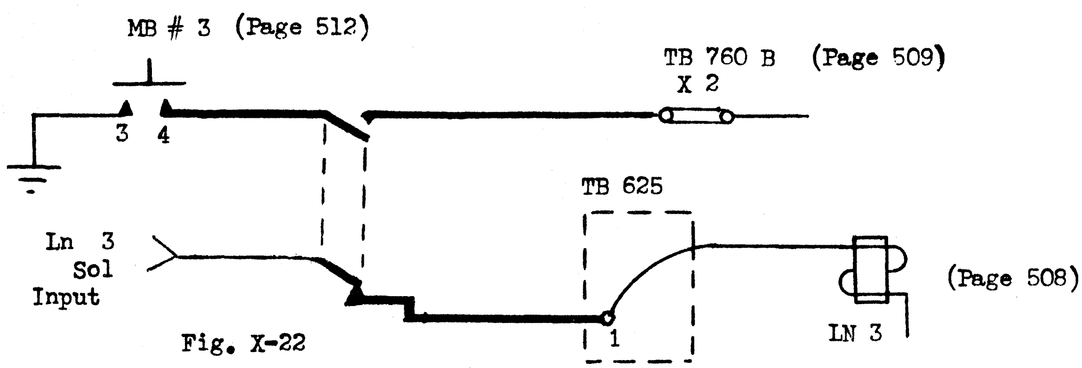


Fig. X-22

3. The third requirement is to print each operation.

PROCEDURE: Open up the hammer block to allow a full print.

OPERATION: With the toggle switch in the transferred position a printer operation may be obtained in any carriage position. The manual tab and return keys or typewriter space bar should be used to position the carriage in each succeeding programmed position.

Manual testing of computations may be done after any operation.

On striped ledger styles it is most desirable to use one set of encoded balances for all program routines. This may best be accomplished by reading the form, allowing the first machine operation after read, manually opening the carriage, cycling the program camshaft home with the FS switch, carriage open, and AT switch rearward and printing on a 22" roll of paper.

One more control that may become useful is to control the firing of the tappets by a manual switch.

This will allow dynamic operations from each carriage position.

PROCEDURE: Remove one wire from the tappet coil and attach a jumper wire from it to a normally open contact of any plunger micro switch. Attach another jumper wire from the switch common to the tappet coil.

Each machine operation, including AEC will require a depression of this switch.

The above methods are not intended to be the only way to debug programs. They may help increase your efficiency in this checkout work.

TROUBLESHOOTING POWER SUPPLY PROBLEMS

The most important single item to be used in this area is an accurate volt-ohm meter. Of particular importance on power supply "short" problems is an accurate X1 scale in the ohm meter section. The meter batteries must have sufficient power to "zero in" on this scale. A back circuit thru the power supply will read as low as 4 ohms, therefore, the X-1 scale must be capable of distinguishing between 0 and 4 ohms.

This scale may be checked on any meter by measuring the 28.7 ohm resistors on a Memory Driver Card. Do not attempt to run down "short" problems with a faulty meter.

"SHORTS"

The -15M is a very delicately fused circuit. A loss of the -15V or -4 source in the system or any other condition that arises that allows uncontrollable run away of the Memory Drivers will cause this fuse to open. Always check for a loss of another voltage source when this fuse is open.

If a "short" is experienced, check the resistance from both sides of the open fuse to ground or to another source voltage. If zero ohms is detected, a systematic isolation of this circuit should be made until the source of the short is located.

Starting at the beginning short reading, isolate this portion of the circuit by removing the next terminal board connection. Recheck the original point. If the short reading has disappeared, move to the next leg of the circuit. Isolate upper and lower gates and the printer in this manner.

If the short is in one of the gates, each distribution bus should be removed. Next, the decoupling cards should be pulled one at a time and finally one logic card at a time until the problem is localized.

Changes or additions since last issue.

Back plane shorts between pins, caused by a small piece of foreign material such as wire between pins, occur rarely. These may best be localized by placing the system in a continuous "Electronic Cycle" to determine the improperly working circuit. Once this has been done, visually inspect very carefully each pin connection of the faulty circuit with the adjacent pins on the back plane.

REMEMBER: Certain lower gate signals that are normally at -4 are transmitted to pins on the upper gate.

"CONNECTIONS"

Good solid connections in the power supply often mean the difference between a solid system and one with intermittent malfunctions.

Each connection and distribution point should be visually inspected for proper and tight connections. Crimped ring tongues should be inspected to assure that the wires put far enough into the opening to secure each wire tightly. <u>Pulling on these wires is a good test.</u> Also assure that the wires were not put too far into the opening so as to crimp the plastic wire cover rather than the bare wire.

Another important area to check are the connections <u>inside the solar transformer</u>. Check for all connections to be tight and to see if the wires were behind the screws when tightened. All terminal board screws must be securely tightened.

All relay taper tab connections must be tight, particularly in the -100 volt circuits.

CASE AND LOGIC GROUND

Case and logic ground should only be connected at E760 on the printer. This connection is located under the P.G. module as shown on page 503. Any other connection, such as a shielded cable touching the frame, will cause noise in the logic resulting in intermittent logic malfunctions, ie., read-write lights, type-out-of-memory, set or reset of flip-flops.

To check for a proper connection from J901-D (page 503) to E760 through the sensing plate to E775 (under the hysteresis clutch) then to E904 (page 503), a near zero ohms should be read from a buss bar ground to the case. It is very important that the chain of connections from logic ground J901-D to case ground E904 are solid.

Equally important is an unwanted short between the two in another place in the system. The following procedure may be used to check this:

1. Remove the wires from TB901-15 (page 503).
2. Approximately 100 ohms resistance should be read to the machine frame using the wires removed as the common meter lead. Approximately 90 ohms should be read with the leads reversed.
3. Next remove the following plugs in order and observe the readings. Do not reinsert the plugs until finished.

J902 - 180 ohms common to the removed wires.
140 ohms leads reversed.

J905 - Same Readings

J602 - 2K ohms common to the wires.
500 ohms leads reversed.

J603 - 2K ohms common to the wires.
5K ohms leads reversed.

Do not overlook the possibility of the short occurring during a printer or program cam shaft cycle. Visually check the printer wires for non-rubbing clearances.

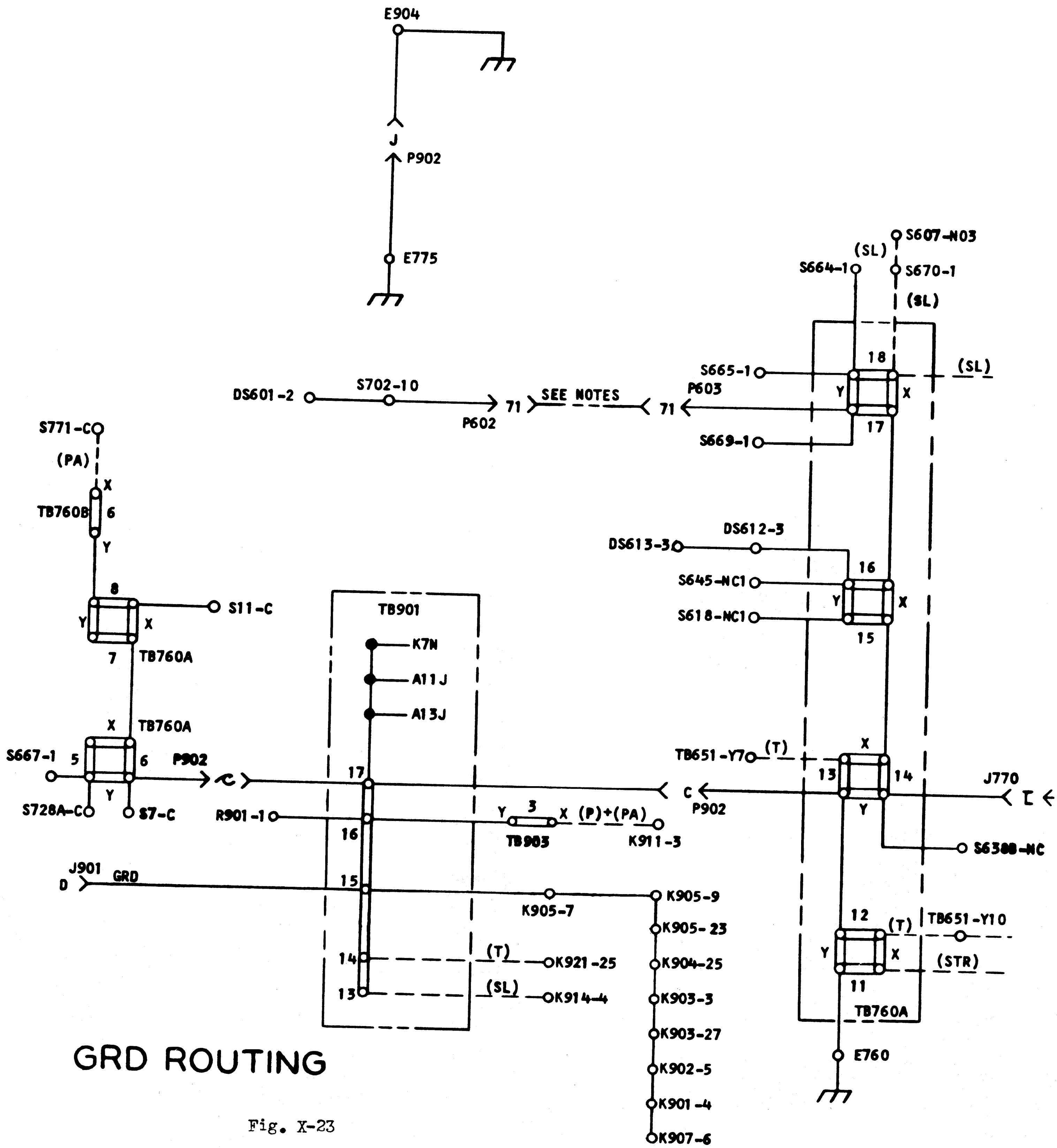


Fig. X-23

"METER ACCURACY"

Power supply adjustments at the factory are made using a digital voltmeter that has an accuracy of ± 0.2%.

Meters used in the Field do not approach this accuracy. Scopes are ±6% accurate on voltage readings. The 310 Triplett is ± 3%. The 625 Tripplett is ± 0.5%.

Meter accuracy is generally specified as percentage of full scale deflection. When measuring small deflections on large scales, the per cent of accuracy is greatly reduced.

EXAMPLE: The adjustment for the -15 volt supply in E2190 is -15.25 to -15.45. This is about a 1% tolerance.

Using the most expensive and best meter available in the Field, which is 0.5%, it appears an accurate adjustment could be made on the -15 supply. However, the range needed to read 15.45 exceeds the 0-15 and the next higher range, which is 0-90 volts, must be selected.

Calculating the accuracy of this scale, we find (90 volts x .005) = 0.45 volts. This means the meter is perfectly within its labeled accuracy if any reading on the 0-90 volt scale is within 0.45 volts of the true value.

Next, we must calculate the per cent of accuracy when reading the desired voltage (-15.45) using this scale. (0.45 volts ÷ 15.45 volts) = .029 or 2.9%. As can be seen this exceeds the Engineering specifications for the adjustment of this voltage using the best meter available.

Calculating the same readings when using the Triplett 310 (accuracy of ± 3%) we see: The 0-60 volt scale must be used. (60 volt x 3%) = 1.8 volts.

Next, the percentage of accuracy when measuring the 15.45 volts is calculated as: (1.8 volts ÷ 15.45) = <u>11.6%</u>.

The above examples merely point out why factory adjusted power supplies should be left intact if at all possible.

"CONSTANT VOLTAGE TRANSFORMERS"

Each constant voltage transformer has its own characteristic which affects the output voltage. These transformers will regulate to a certain degree A.C. line input variations. It takes about ½ cycle before any regulation is accomplished. However, frequency changes cause a drastic change in their output. The output of these transformers may vary 1% as temperature goes up. The outputs from individual transformers are between 110 and 120 volts. If one must be replaced in a system, a complete check of the voltages will be necessary due to the characteristic differences of individual transformers.

Other power supply components also have their own characteristics. Some are compensated for by adjustments and these too should be considered when being replaced.

BUCK OR BOOST TRANSFORMERS

T1103 and T1102 are Buck or Boost transformers. These are necessary to make the compensating adjustments of the power supply due to the characteristics of components. These transformers also have their individual characteristics, therefore, the primary concern in adjustments lies in the final output voltages. All necessary voltages have individual resistor adjustments except the -15 volts. This is the basic voltage adjustment in the power supply and is attained by altering the input hookup to the Buck or Boost transformer T1103.

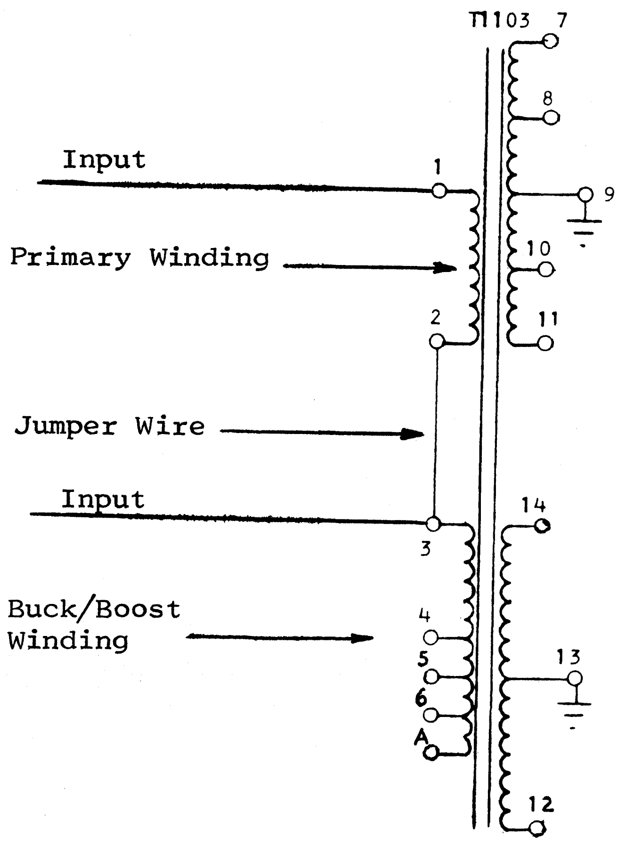


Fig. X-24

The input to T1103 contains a primary winding (terminals 1 and 2) along with additional primary windings that may be used by means of a jumper wire to "buck" or "boost" the primary. Any amount up to 12 volts may be used by different terminal connections of the jumper wire. Each succeeding portion will "buck" or "boost" the output voltage approximately .9%. The standard hookup (no buck or boost) would be terminals 1 and 3 for input and the jumper wire between 2 and 3. As shown in Fig. X-24.

If the output voltage needed to be boosted by .9% the input would then be terminals 1 and 3 with the jumper between 2 and 4.

VOLTAGE ADJUSTMENTS

Factory adjusted power supplies should not be changed unless absolutely necessary. Before attempting to change any factory adjustments, record all readings and terminal hookups on the panel next to the filter. Review "Meter Accuracies".

Step A: Use E1207 (ground buss) as the ground reference point. Measure the -15 voltage at E1202 and E1206 (-15 busses) with all adjuncts turned on. The voltage must be between -15.10 and -15.45 volts when the system temperature is normal.

TO ADJUST: Use the table in Fig. X-25 to alter the -15 voltage in the direction necessary.

NOTE: The approximate voltage change as shown is from the initial connections (no buck or boost wired).

Jumper Between	Input to	Approximate Voltage Change in -15 supply	
2 and A	1 and 3	-1.56 (Volts)	
2 and A	1 and 4	-1.43	↑
2 and A	1 and 5	-1.17	
2 and 6	1 and 3	-0.91	
2 and 6	1 and 4	-0.78	
2 and A	1 and 6	-0.65	Boost Output
2 and 6	1 and 5	-0.52	
2 and 5	1 and 3	-0.39	
2 and 5	1 and 4	-0.27	
2 and 4	1 and 3	-0.13	
2 and 3	1 and 3	initial connections	
2 and 3	1 and 4	+0.13	
2 and 4	1 and 5	+0.27	
2 and 3	1 and 5	+0.39	
2 and 5	1 and 6	+0.52	
2 and 6	1 and A	+0.65	Buck Output
2 and 4	1 and 6	+0.78	
2 and 3	1 and 6	+0.91	
2 and 5	1 and A	+1.17	
2 and 4	1 and A	+1.43	↓
2 and 3	1 and A	+1.56	

Fig. X-25

Step B: Position the center tap of R1124 so that the +15 voltage measured at E1204 is between +15.45 and +15.10. At times it may be necessary to jumper resistor R1124.

Step C: Position the center tap of R1123 so that the -100 voltage measured at TB1201-B3 is between -102 and -98.

Step D: Position the center tap of R1118 so that the -15 Memory Voltage measured at F8A-30 is between -15.20 and -15.12.

Step E: Measure the -4.25 voltage at TB1101-X7. The voltage must be between -5.05 and -4.75. If -4 transformer (T1102) is connected with the jumper between 2 and 3 and the input to 1 and 3 (initial connections), the output voltage will be changed as shown in Figure X-26 when connections are changed. Select -4 transformer (T1102) connections so that the -4.25 voltage measured at TB1101-X7 is between -5.05 and -4.75.

Jumper Between	Input to	Approximate Voltage Change in -4.25 supply
2 and 5	1 and 3	-.37 Volts
2 and 5	1 and 4	-0.25
2 and 4	1 and 3	-0.12
2 and 3	1 and 3	initial connections
2 and 3	1 and 4	+0.12
2 and 4	1 and 5	+0.25
2 and 3	1 and 5	+0.37

Fig. X-26

Step F: Position the center tap of R1128 so that the -4.25 voltage measured at E1201 and E1205 is between -4.35 and -4.20.

Step G: Position the center tap of R1101 so that the -56 voltage measured at TB1202-A14 is between -58.5 and -54.5.

Step H: Measure the +35 unfiltered voltage at TB1202-B5 for -38 to -32.5 volts.

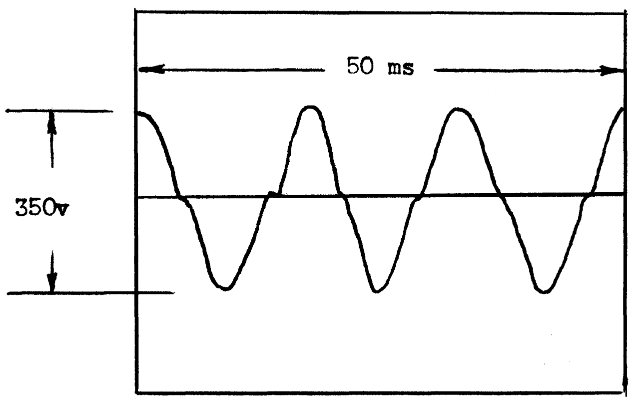
Step I: Relocate the voltmeter ground to TB2002-16 (cge. tray). Measure the -4.12 voltage at TB2002-12. The voltage must be between -4.16 and -4.10. To obtain the required voltage, loosen locking nut of resistor R1124 and rotate adjusting screw. Tighten locking nut.

Step J: Measure the -120 voltage at TB2001-16. The voltage must be between -140 and -108.

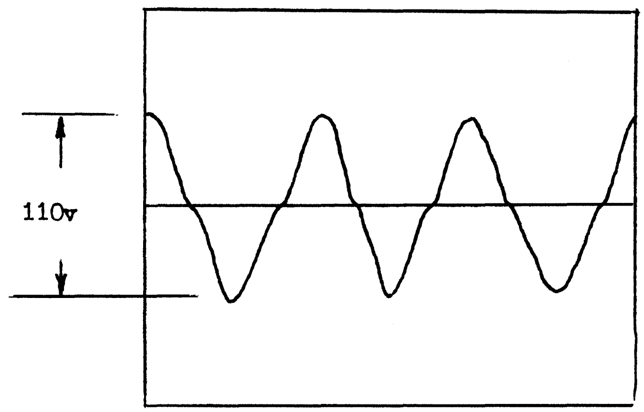
Voltage	Ripple Checked At:	Ripple (Max Mv) Peak to Peak
-15	E1202 and E1206	150
+15	E1204	150
-100	TB1201-B3	1000
-15 Memory	F8A30 (non-sterling system)	75
-4.25	E1201 and E1205	43
-56	TB1202-A14	560
-120	TB2001-16	1200

POWER SUPPLY WAVEFORMS

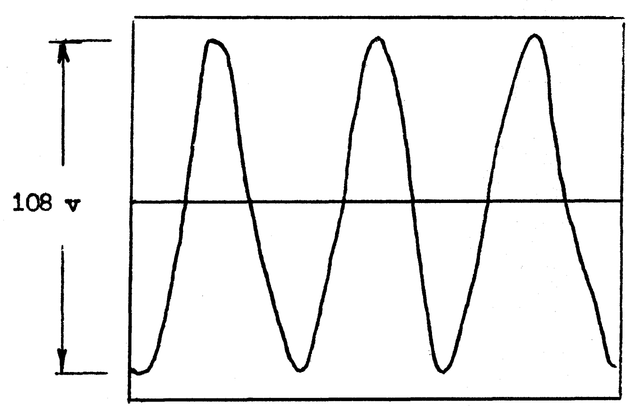
The following diagrams show typical power supply waveforms and approximate meter readings. These are only typical and are under no circumstances to be used for making any adjustments to the power supply. Refer to "Voltage Adjustments" for exact settings of the power supply.



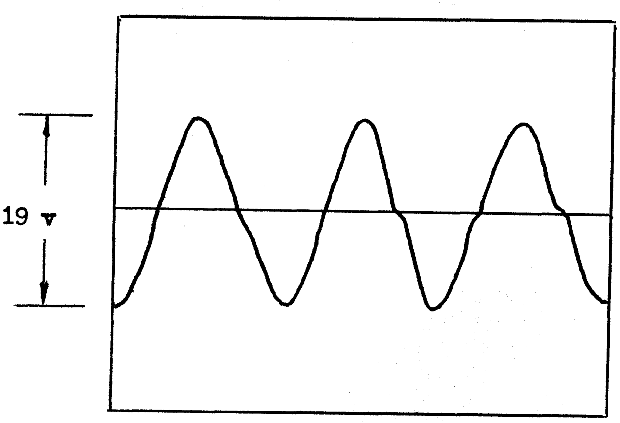
T 1103 -7 or -11
Meter = 125 v ac
Grd. T1103 -9



T 1103 -8 or -10
Meter = 40 v ac
Grd. T1103-9

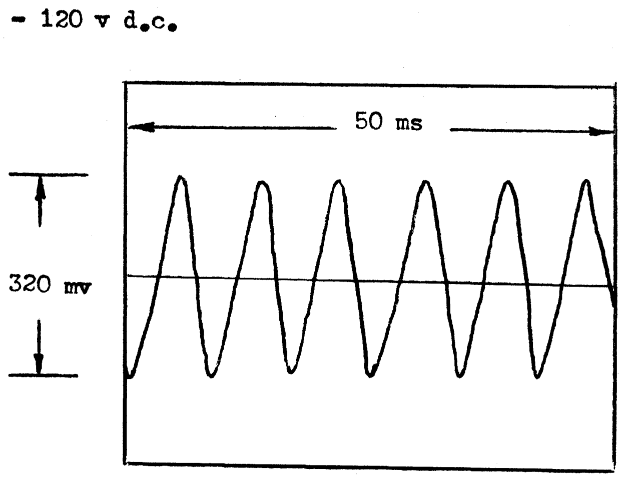


Scope across
T 1103 -12 to 14
Meter = 38.5 v ac

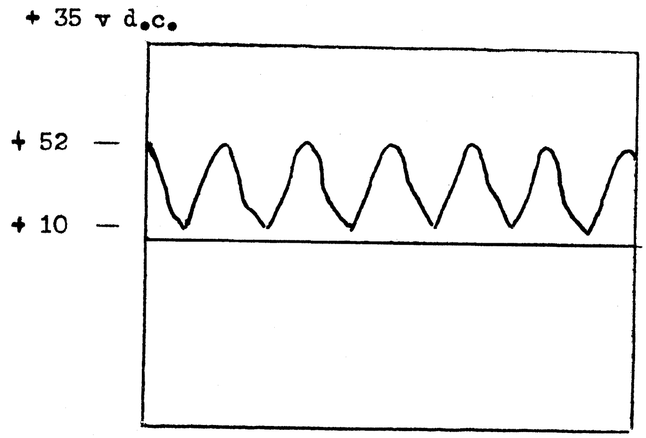


T 1102 -6 or -8
Meter = 33.5 v ac
Ground at T 1102 -7

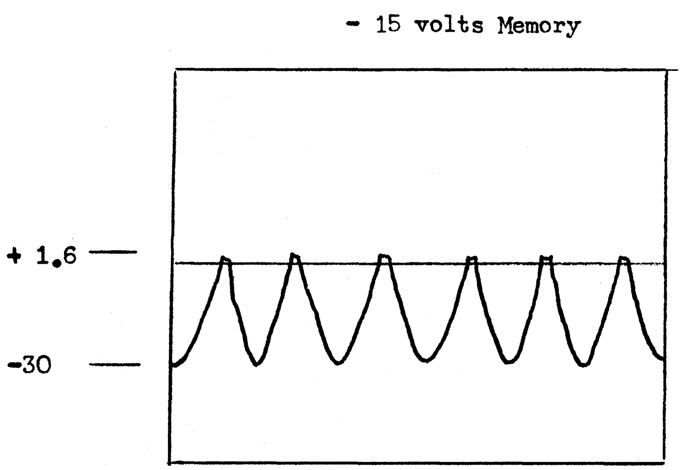
Fig. X-27



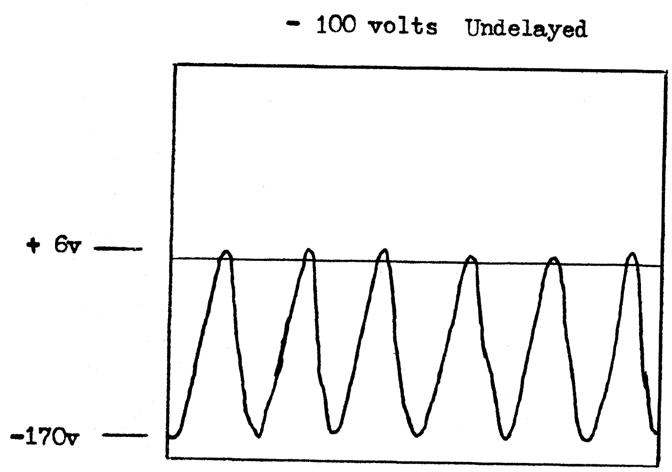
CR 1117 - 1
Meter = -120 vdc
Grd. at T1103-9
Scope input AC



F 1105 -2
Meter = -36 vdc



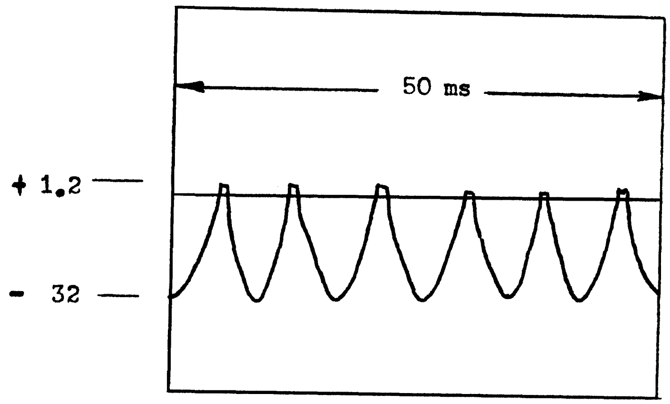
L 1101 -1
Meter = -15.5 vdc
Grd. at T1103 -13



L 1104 -1
Meter = - 100 vdc
Grd at T1103 -9

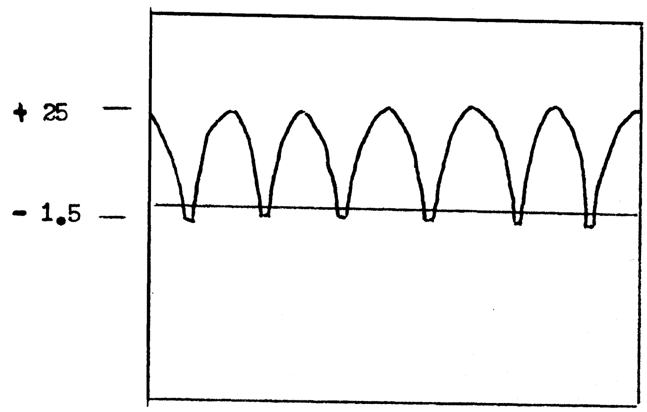
Fig. X-28

- 15 volts



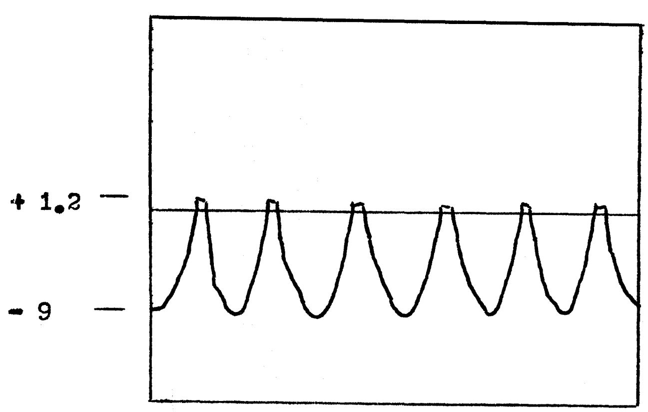
L 1102 -1
Meter = 16 vdc
Grd at T 1103 -13

+ 15 Volts



L 1103 -1
Meter = + 15 vdc
Grd at T1103 -13

- 4.25 volts



L1105 -1
Meter = 5 vdc
Grd at T1103 - 13

Fig. X-29

TROUBLESHOOTING SOLAR CELLS

The standard solar cell as used in the 2100 equipment will produce approximately .8 to 1 milli amp of current when light is applied to the cell. A meter may be placed in series with the cell to check its output. Current flow is in a direction away from the negative lead. This lead should be attached to the common of a triplett 310 meter. The red wire attached to a cell is normally the positive lead.

Resistance readings thru cell will be approximately 100 ohms in one direction and 50-150 K ohms in the other.

Some of the common problems that have developed with solar cells are as follows:

1. A cracked projection on the end of the molded package. This tip is sometimes damaged when inserting the package into its mounting hole if the tip is too large a diameter.

Extreme care must be taken in removing these from their mounting as once the tip is broken the cell will no longer function satisfactorily.

2. Glue sometimes runs between the solar cell and the plastic package during manufacture covering part of the cell.

3. Occassionally the cell is not positioned directly beneath the projection when the package is molded.

4. A short sometimes develops between the cell wires and the shielded wire. This generally happens as the wires are snaked through the shielding.

5. A poor electrical connection may develop inside the cell package. Along these same lines a proper ground connection is extremely important to the cell.

6. The exciter lamps occassionally will be found containing a dark center ring that reduces the foot candle output. Exciter lamps have also been known to allow their filaments to sag, when hot, causing the focus of the lamp to change.

TROUBLESHOOTING FLIP FLOPS

The following procedure may be used to check Flip Flops that may be suspected as being marginal or faulty.

Step #1 - Place the desired Flip Flop in an empty card position that has pins 29-30-31-32 wired for the proper voltages.

Step #2 - Complement the Flip Flop Circuits by connecting the "1" outputs to the reset inputs and the "0" outputs to the set inputs as shown in Fig. X-30.

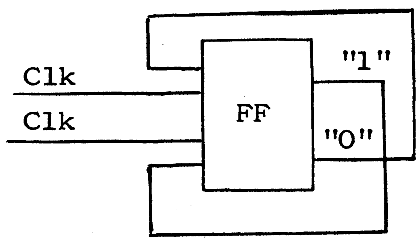


Fig. X-30

Step #3 - Scope the outputs of the Flip Flops for the switching times as shown in Fig. X-31. Pulse time measurements refer to 10% and 90% points.

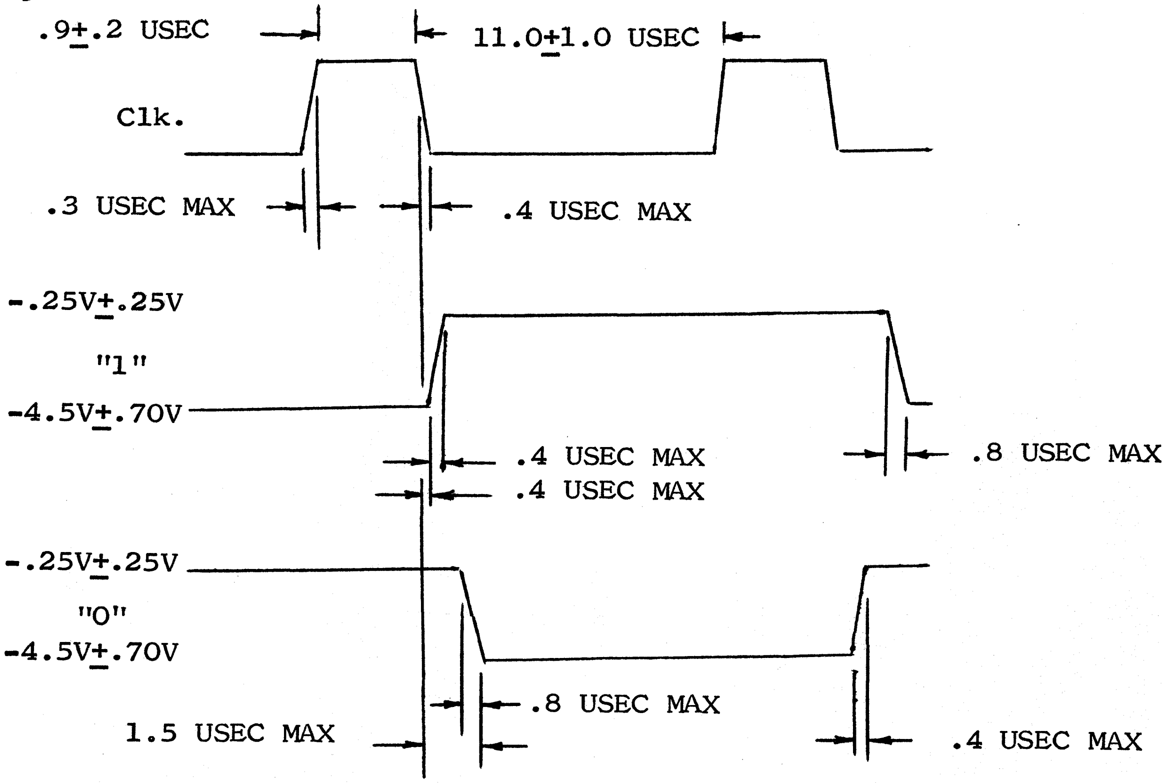


Fig. X-31

Step #4 - Connect alternately to one leg of each input gate a 2K resistor to -15.0 volts as in Fig. X-32. Measure the output of the input gate. It should be at -4.5 volts ± .6 volts.

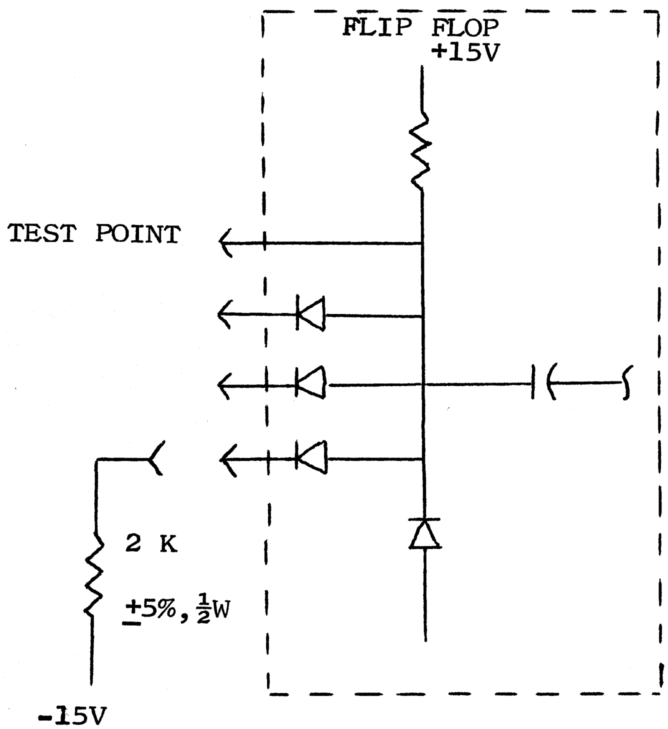


Fig. X-32

METHOD OF ADJUSTING BEAM OF LIGHT ON SERIES A4002

1. Position lamps DS4105 (CC ST/RD), DS4106 (RSTA), DS4107 (I DN), and DS4108 (CT DN) .250" ± .025" from the solar cells.
2. Ground oscilloscope on A2C20. (Do not use 3 wire AC plug to the scope.)
3. With lamps illuminated the input voltage level to the following solar cell amplifiers should be -200 MV. ± 10 MV.

CTDN	Pin No.	A2C4
RSTA		A2C27
CC		A2C24
IDN		A2C9

4. Adjust potentiometer R4201 as required. It may be necessary to re-position an individual lamp or two to obtain desired amplifier input level.
5. For machines with Selective Read:
   a. Ground oscilloscope on pin No. A1C20.
   b. With lamp illuminated the input voltage level to the solar cell amplifier (A1C24) should be -200 MV. ± 10 MV.
   c. With a form between the lamp and solar cell the amplifier (A1C24) voltage level should be -60 MV. ± 50 MV.
   d. Adjust potentiometer R4102 as required.

METHOD OF ADJUSTING PHOTO-CELL BEAM OF LIGHT ON SERIES A4002

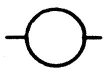
1. The filament of lamp DS4109 should be vertical since the weight of the filament will cause it to sag when hot thereby causing the adjustment to change.
2. With the Auto Reader ON and the form table in its lowered position, adjust potentiometer R4202 for minimum intensity of lamp DS4109.
3. Cover all except the upper .125" of light reflector and depress the Auto Feed button. The form table should move up on the first machine cycle.
4. To adjust, increase the light intensity of lamp DS4109 by adjusting potentiometer R4202.

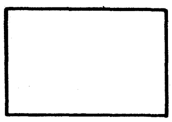
✓ E 2150 DESCRIPTIVE FLOW CHARTS

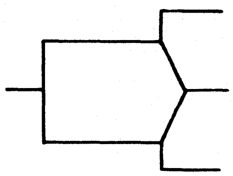
The following simplified flow charts help explain the E 2150 operational flow charts.

They may be used as:
1. Instruction Aids
2. Study Aids
3. Handy Reference Aids

The flow charts are a pictorial representation of the step by step progress through the operation. Three symbols are used:

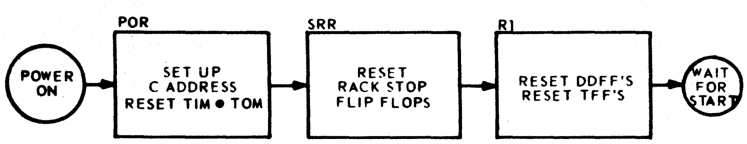
1.  Symbolizes the beginning, end, or continuation of the operation.

2.  Symbolizes the operation to be performed.

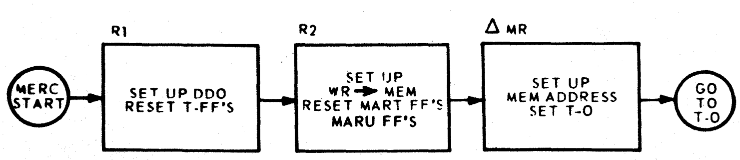
3.  Symbolizes a decision making operation. A question is asked, and a path is chosen according to the answer.

The flow chart is a series of these symbols outlining a sequential chain of events.

POWER UP SEQUENCE

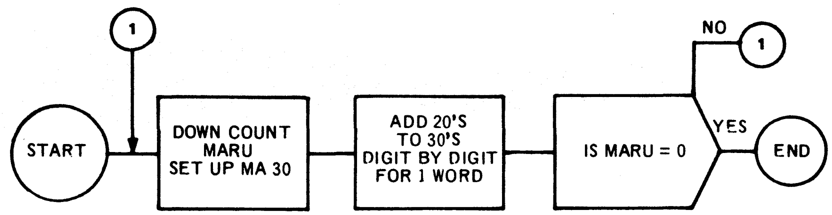


START RESET LOGIC

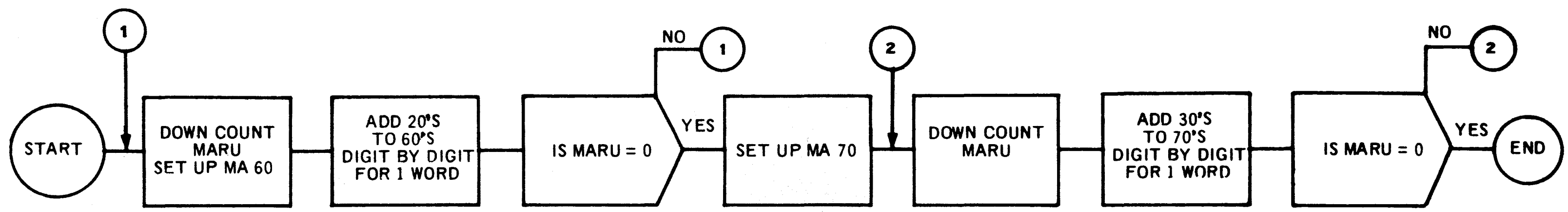


✓ Changes or additions since last issue

TB TRIAL BALANCE (BASIC)

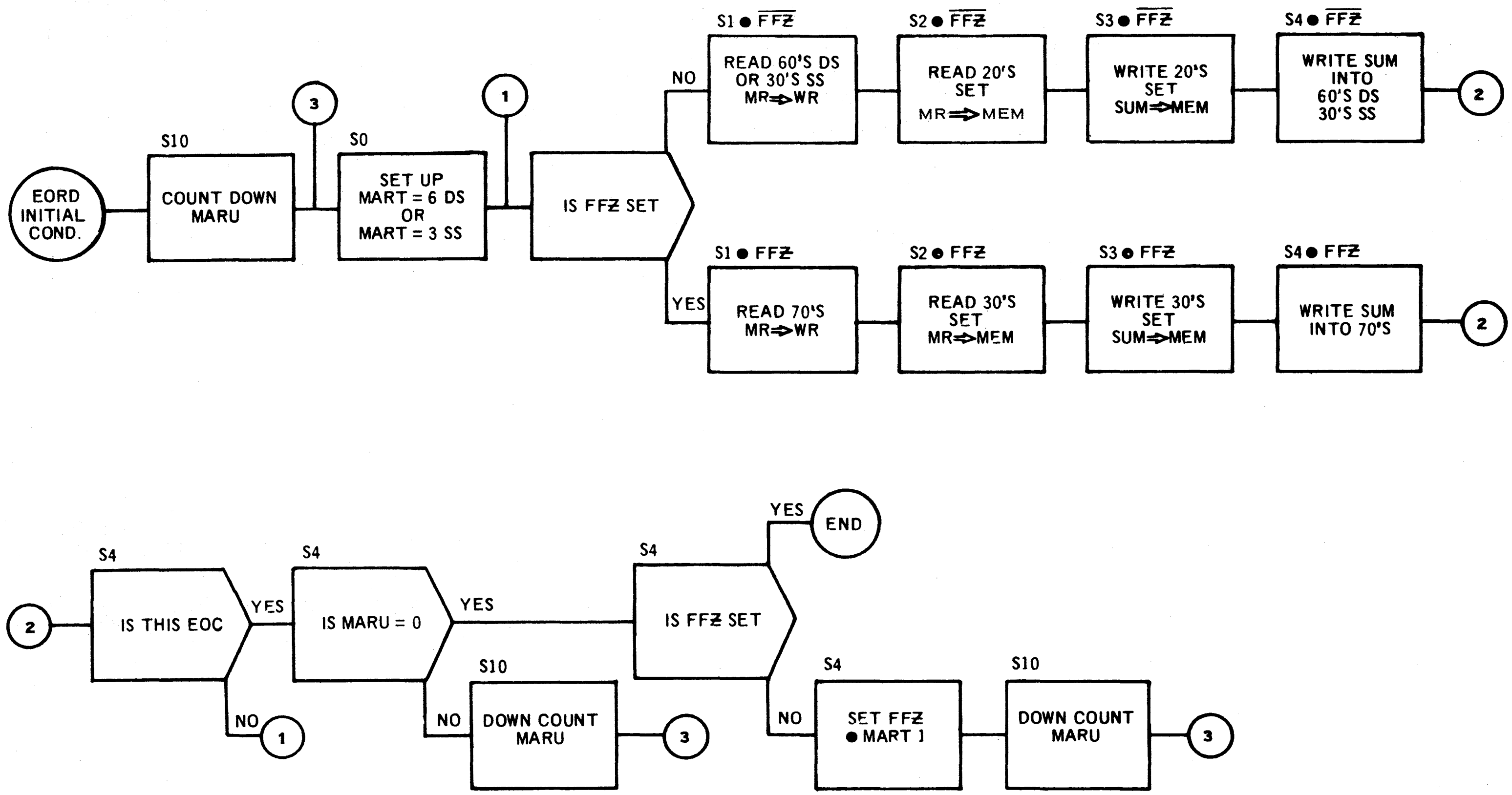


SINGLE STRIPE LOGIC

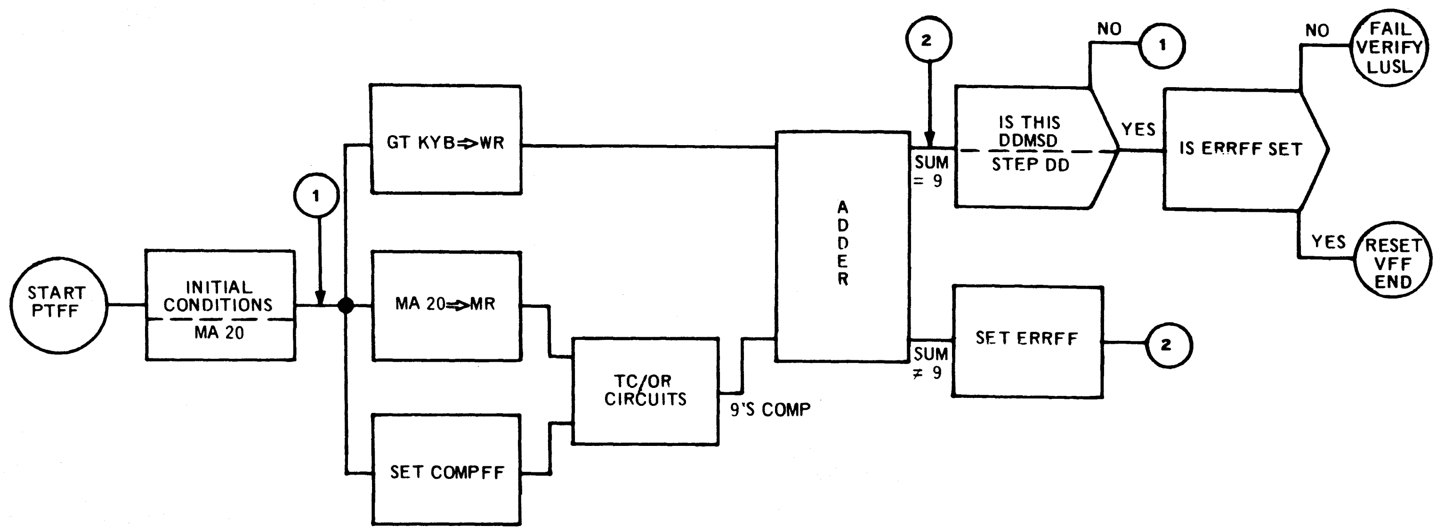


DUAL STRIPE LOGIC

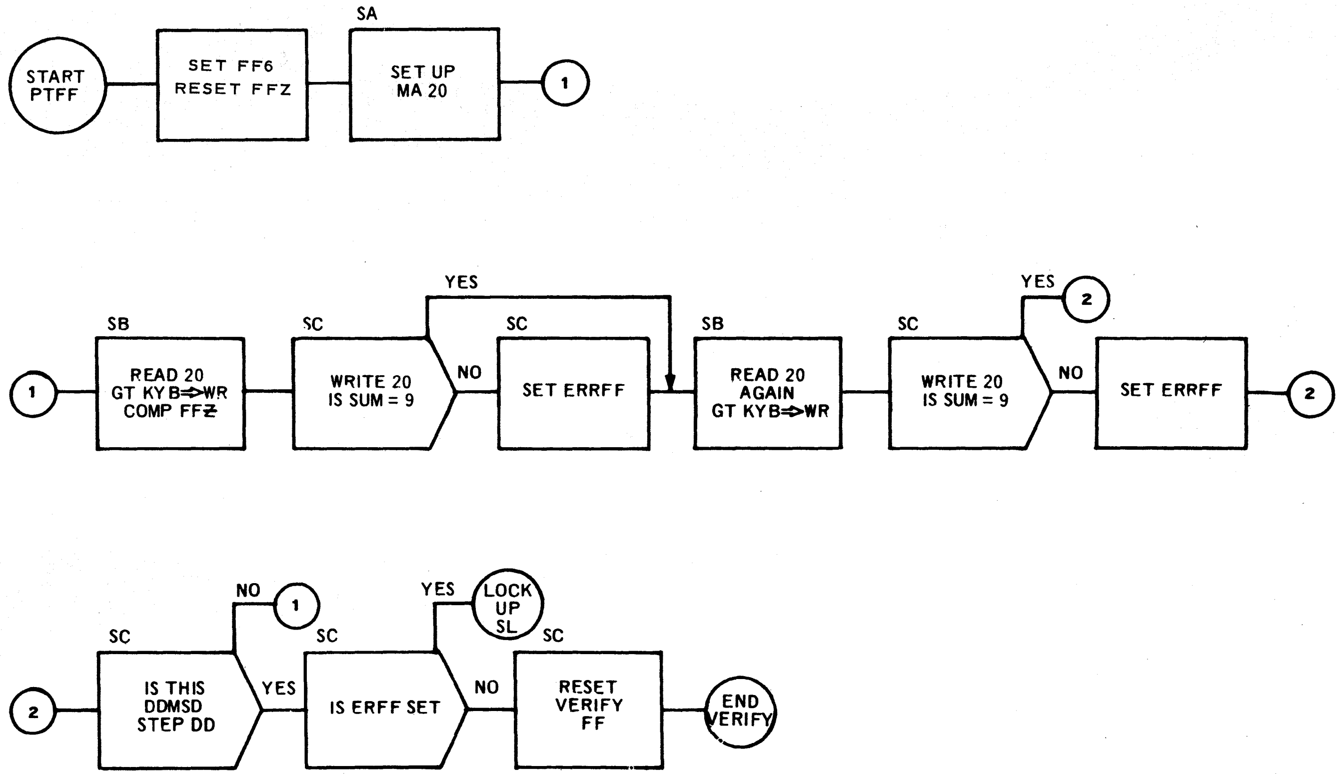
TB TRIAL BALANCE (DETAILED)



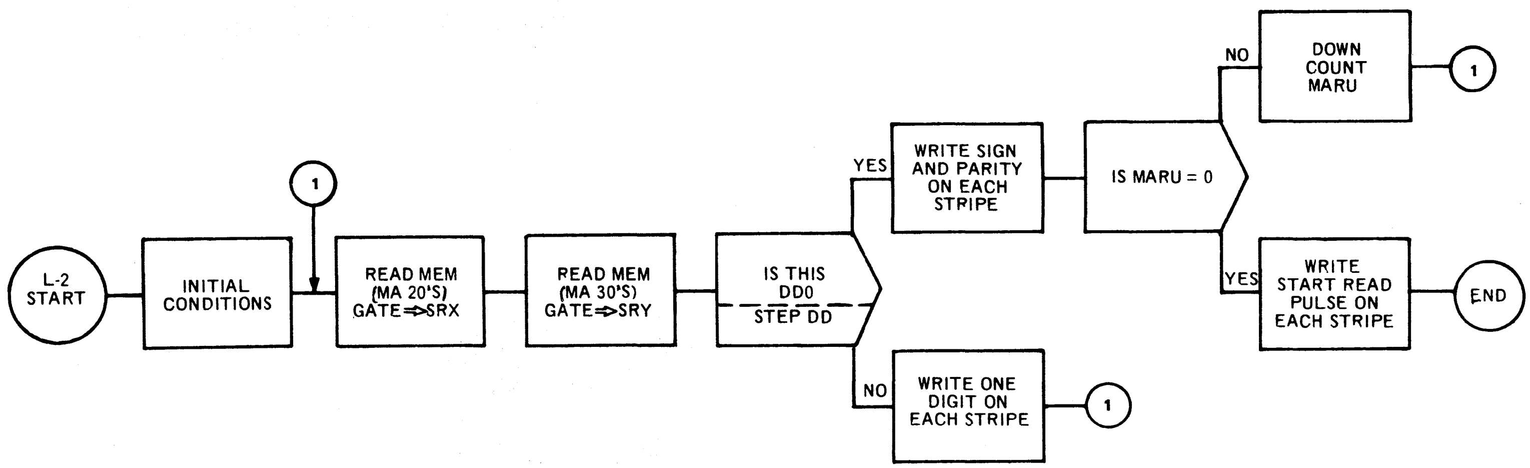
V VERIFY (BASIC)



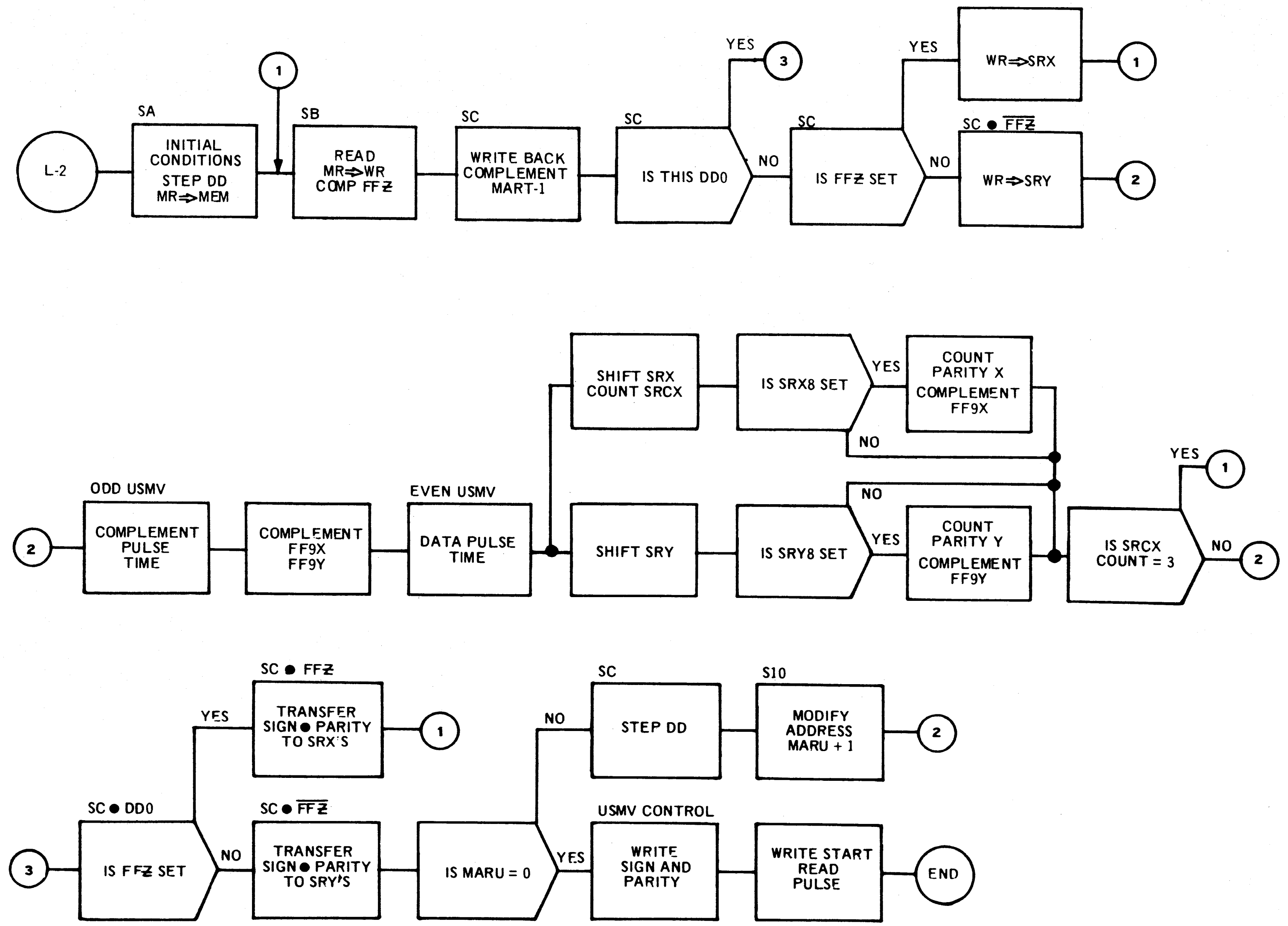
V VERIFY (DETAILED)



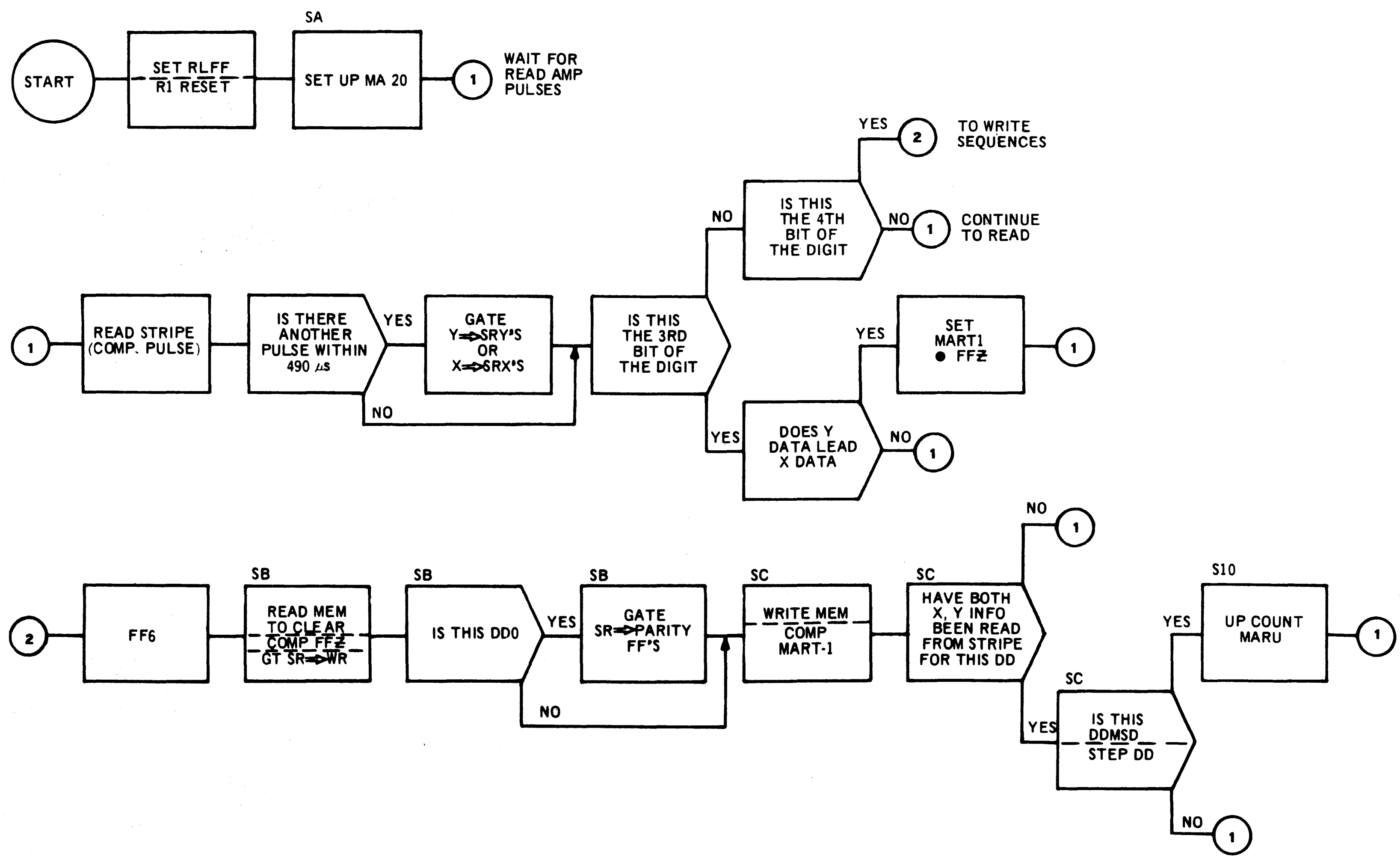
WL WRITE LEDGER



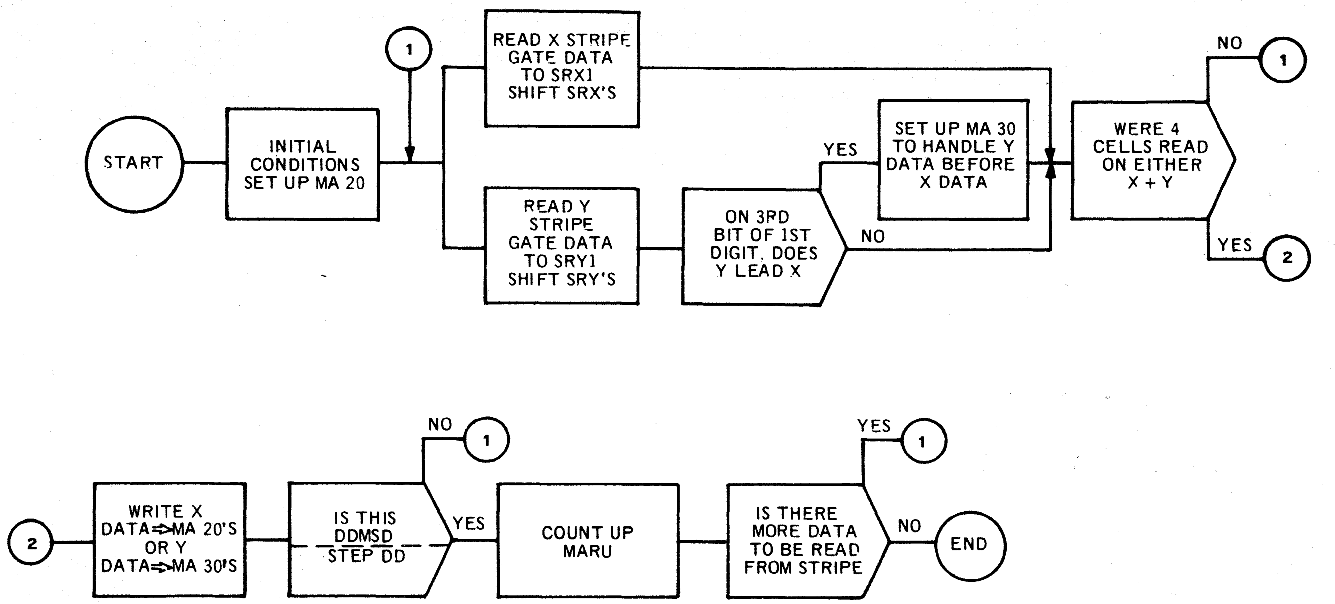
WL WRITE LEDGER (DETAILED)



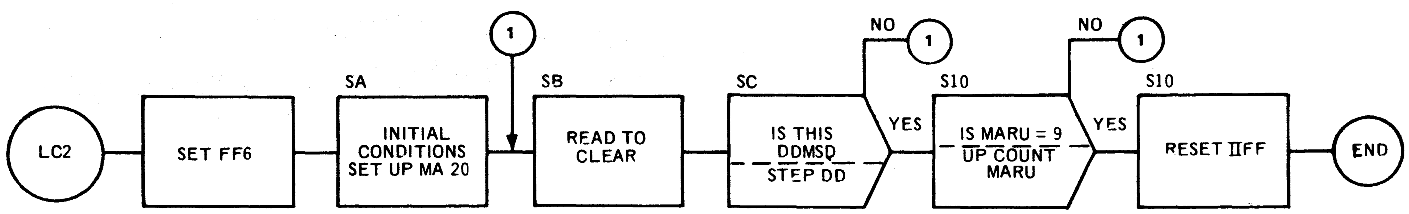
RL READ LEDGER (DETAILED)



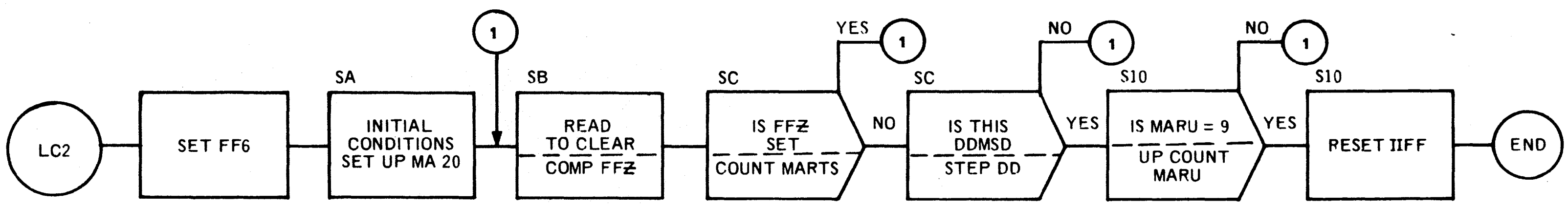
RL READ LEDGER (BASIC)



II INITIAL INSTALLATION

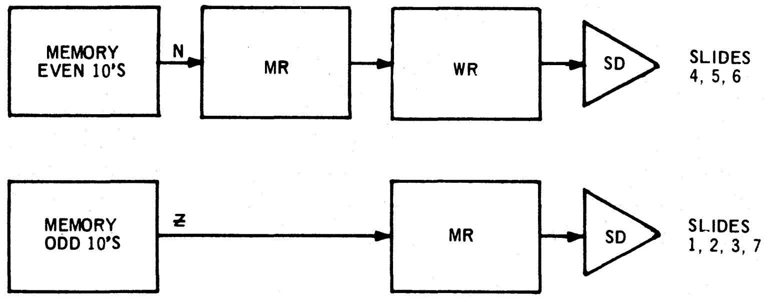


SINGLE STRIPE LOGIC

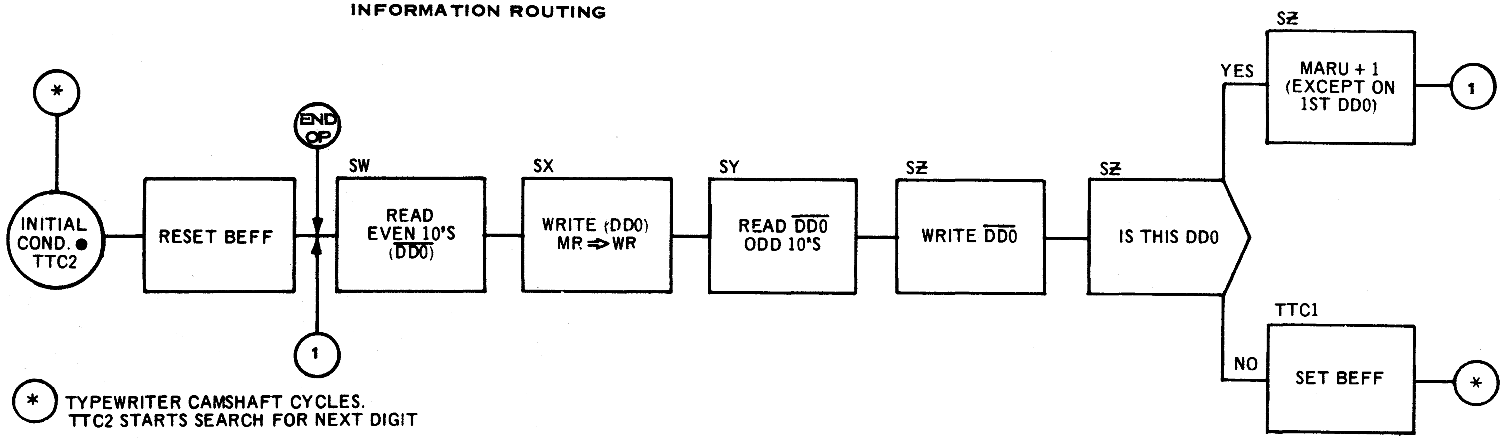


DUAL STRIPE LOGIC

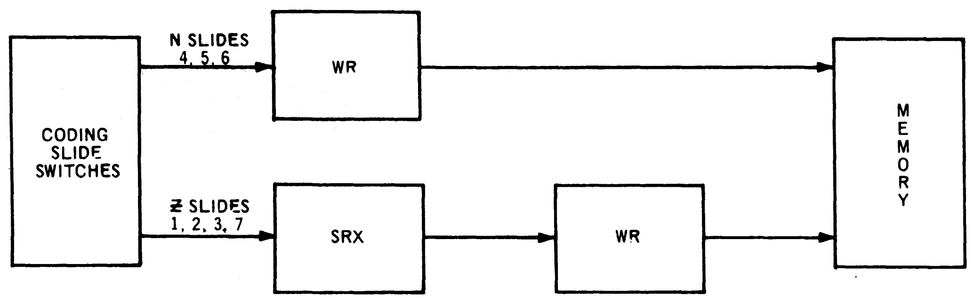
TOM TYPE OUT OF MEMORY



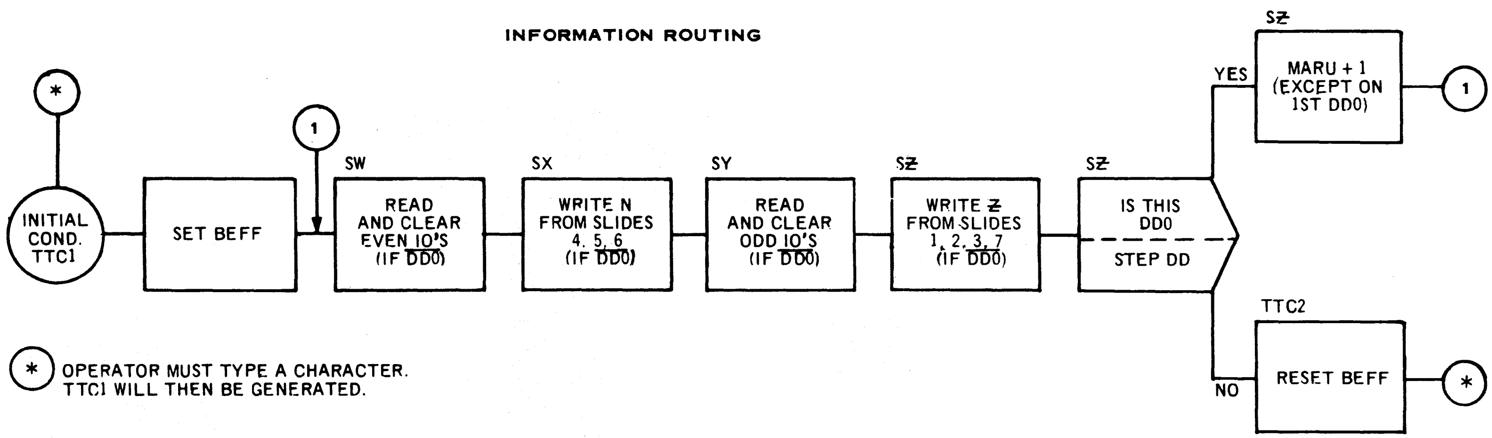
INFORMATION ROUTING



TIM TYPE INTO MEMORY



INFORMATION ROUTING



(*) OPERATOR MUST TYPE A CHARACTER.
TTC1 WILL THEN BE GENERATED.

✓ SINGLE SHOT CLOCK PERMANENT
(Above Serial No. E5745)

A new single shot clock card (SSCP) has been designed to be permanently installed in the upper gate of the processor. Associated logic circuits have also been added to make the SSC routine a more effective service aid. A CLOCK MODE SWITCH S1207 has been installed to stop the electronics in Sequence 0 of the desired T time where the single shot operation is to be performed. It also allows stopping of the logic when a predetermined signal occurs. A single shot operation can be performed without picking the start relay. This operation merely steps through the T times with no arithmetic performed. To accomplish this operation, install a jumper from B4D7 to B5A10 to enable S3 during T2. Set the Clock Mode switch in the SSC position. The POR switch is depressed and released. The MR switch is depressed and released. The DMR switch is depressed and held while the SSC switch is depressed and released, then the DMR switch is released. At this time T0 and S0 will be set, which is the first sequence of the shift operation. One clock pulse will now be obtained for each depression of the SSC switch. The logic can be stepped through the T times to the end of T6.

A manual operation can be performed by removing the pin from TB903-6X, which opens the pick circuit to the machine trip solenoid. Index the desired keys (control, data, MA) on the keyboard, depress the motor bar and proceed as described above.

A panel operation can be performed by locating the carriage in the desired position, removing Pin TB903-6X, indexing keys as desired, depressing the motor bar and proceeding as above.

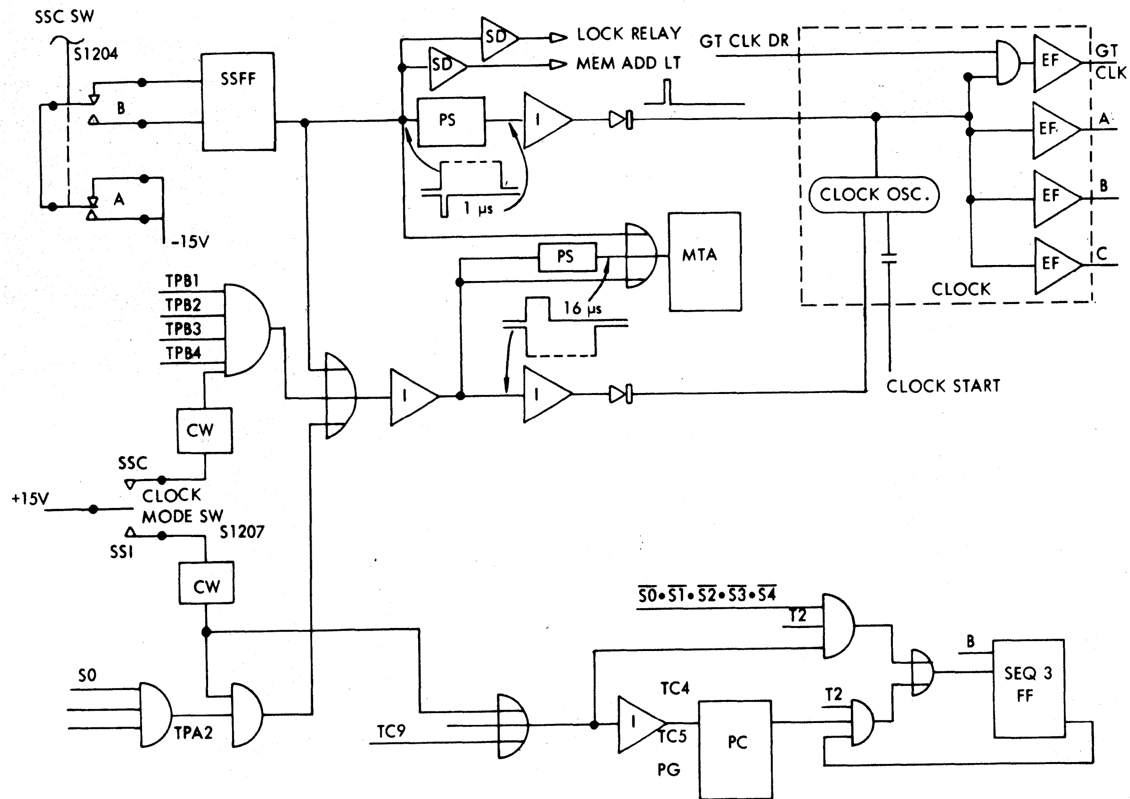
✓Changes or additions since last issue.

The machine must be turned off and on between each cycle in order to obtain a reset signal (R1, R2, R3, and Delay Reset), otherwise some FF's are not reset. If the DD FF's step from DD0 to DD1 on the first depression of the SSC switch, it will be necessary to remove the Step DD SL signal from D7D14 (Reference Page 107) on the upper gate. When the Clock Mode switch is in the SSI position, the logic will stop when S0 is high. Each depression of the SSC switch will advance the logic until S0 comes high again, thus stopping the logic at the beginning of each T time. The operation can be transferred to the single shot operation in S0 of any T time by holding the SSC switch depressed and transferring the Clock Mode switch to the SSC position.

The logic can be stopped at any pre-determined T time by placing a jumper from TPA2 (B4D11) to set side of the TFF desired and placing the Clock Mode switch in the SSI position. The logic will stop with S0 and the selected T time high. The operation can be changed to single shot clock by holding the SSC switch depressed and transferring the Clock Mode switch to the SSC position.

If it is suspected that a given signal is becoming high erroneously, that signal can be jumpered to TPB1 (B4D4) and switch S1207 placed in the SSC position. The logic will halt when this signal becomes high. The indicator lights can be analyzed to determine if the signal became high at the proper time. The SSC switch will step the logic one clock pulse at a time until the signal under question goes low. The logic will then proceed at clock frequency until the signal under question again becomes high. The signal under question can be further defined. For example, if it is suspected that the NZFF is being set during T1 time, NZFF can be jumpered to TPB1 and T1FF signal jumpered to TPB2. The logic now will stop if NZFF is set during T1, but not when it is set during any other T time such as T0.

LOGIC OPERATION



Single Instruction (T Time)

When the Clock Mode switch is placed in the SSI position, the Contact Wetter (CW) output goes from -4V to ground. This enables an AND gate with SO. The output of this gate will become high at the start of each T time. This high signal through a double inverter inhibits the clock oscillator. Thus the logic stops before a clock pulse is produced to step out of SO. No other action takes place until the SSC switch is depressed. The depression of SSC will cause the SSFF to be reset. This signal will remain high as long as the SSC switch is depressed and will accomplish several things. A PS will be triggered by the leading edge (positive swing) of the SSFF signal. The output of the PS is a negative going 1 usec pulse which is inverted and fed into the clock card. This signal through the emitter followers on the clock card becomes clock A, B, C, and Gated Clock, if the Gated Clock Driver signal is high.

The clock pulse produced will cause SO to go low. The clock oscillator cannot produce pulses again because the SSFF signal is still holding the clock oscillator inhibited. When the SSC switch is released, the inhibit is removed from the clock oscillator and the logic proceeds at clock frequency until the SO signal again becomes high at the start of the next T time. When T2 is reached under the SSI operation, the high signal from the CW of Clock Mode switch is inverted and wired to the PC card to inhibit PC pulses. The CW signal from the SSI switch is also gated with T2 and $\overline{S0}$, $\overline{S1}$, $\overline{S2}$, $\overline{S3}$, and $\overline{S4}$ to enable setting S3. This operation will step through the logic one T time at a time. Another method of getting to the desired T times is to place a jumper from the desired T time flip flop to the gate with SO. This will cause the logic to stop with SO and the T signal high.

SINGLE SHOT CLOCK

If the Clock Mode switch is transferred to the SSC position while the SSC switch is held depressed, the high signal from the CW from the SSC side of the Clock Mode switch will cause the clock to be inhibited. A depression of the SSC switch will cause the PS to generate a pulse for the clock, but the clock inhibit will not be removed. The logic is stepped one clock pulse at a time. The operation can be transferred back to the SSI operation at any time by transferring the Clock Mode switch while the SSC switch is held depressed. When the SSC switch is now released, the logic will continue at clock frequency. The SSFF signal also picks LOCK relay and turns on the MEM ADD light. This LOCK relay circuit holds up the following machine cycle as long as the SSC switch is held depressed.

With the Clock Mode switch in the SSC position and a signal jumpered to one of the TPB points, the logic will stop when the signal at the TPB point becomes high. This signal is inverted and wired to a PS which is in turn wired to the enable inhibit circuit of the MTA card. The PS provides a 16 to 18 usec pulse which permits writing the correct digits to memory if the logic stops with the write signal high. The PS is necessary to allow a write operation, yet prevent the inhibit drivers from staying on, which would cause overheating of resistors in the inhibit circuit. The SSC switch steps the logic one clock pulse at a time until the signal at TPB goes low. At this time, the logic will again operate at clock frequency.