

B 1700

FIELD CARD TESTER

Burroughs

FIELD ENGINEERING

**TECHNICAL
MANUAL**



FIELD ENGINEERING PROPRIETARY DATA

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SECTION 1

INTRODUCTION AND OPERATION

GENERAL INFORMATION

MAINTENANCE PHILOSOPHY

The maintenance philosophy of the Burroughs B1700 computer is based upon the on-site use of a portable Field Card Tester, referred to as an FCT.

Central system faults, either on processor cards or input-output cards, may be confirmed by exercising a suite of MTR/Diagnostic test routines. These test routines are supplied with each system. Each test routine is encoded on a 0.25 inch wide magnetic tape enclosed in a plastic cassette.

The tape drive and its electronic control unit is a plug-in module mounted on the front console. The tape drive control logic interfaces directly with the processor and is independent of all other input-output controls. These test routines may be executed directly from cassette or entered into main memory prior to execution. All test routines are supported by documentation containing loading procedures, error halts, options and console key instructions. Error halts are signalled by observing the console lamp display or the Console Printer (SPO). For each processor error halt, the supporting test documents will advise the Field Engineer (FE) of the failing logic card. Some complex logic functions are located on more than one card. In this case, the error halts will define a small group of cards rather than one logic card. The suggested group of logic cards are then tested in the FCT, one by one, to identify the failing card. With the diagnostic ability of the FCT, the FE can isolate the failing circuit or chip. After replacing the faulty circuit, the card must be tested again by the FCT to ensure that the fault has been repaired. Also, the MTR/Diagnostic test routines must be repeated to ensure that the overall system is functioning correctly.

MEMORY CARDS

The dynamic S-memory and M-string memory cards are not test-compatible with the FCT.

CAUTION

NEVER INSERT MEMORY CARDS INTO THE FIELD CARD TESTER.

Fault diagnosis of memory problems are determined by executing special memory test routines that assist the FE in isolating the failure to a component or a small group of components. Fault location is simplified by memory logic design and that memory cards are interchangeable.

FIELD CARD TESTER

The Burroughs B1700 FCT as shown in Figure 1-1, is designed for field service and operated by FE's trained in its use. The B1700 maintenance philosophy states that logic cards must be repaired on-site. The FCT is specifically designed to be used as the primary diagnostic tool to detect and isolate defective logic components. The FCT electronics and metal case surrounding it, weighs approximately 27 pounds (13 Kg) and measures 19 x 14 x 7 inches (49 x 36 x 18 cm) overall. Storage space for tester accessories are included within the case.

The basic areas of the FCT are as follows:

1. Logic Power
2. Main Test Logic
3. Operating Panel
4. Lamp Display
5. Card Connectors.

Logic Power

The four logic voltages +4.75, -2, (+12, -12) volts and mains A.C. power are obtained from the processor via a flexible cable. A cable socket on the processor mainframe (card side), allows the FCT to be operated on the SPO table.

IO cards use

Main Test Logic

The test logic is mounted on seven logic cards. All logic I.C. chips and discrete components are common B1700 parts, mounted on three quarter sized B1700 double edge connector cards. The wire wrapped logic cards on early FCT's have been superseded and replaced by etched cards. The FCT circuits and logic functions are identical for wire-wrap or etched FCT cards. Only the chip locations are different. Section 2 of this manual will refer to etched card chip locations for explanation purposes.

Introduction and Operation

CAUTION

CARD INSERTED WITH LOGIC
CHIPS FACING OPERATING PANEL

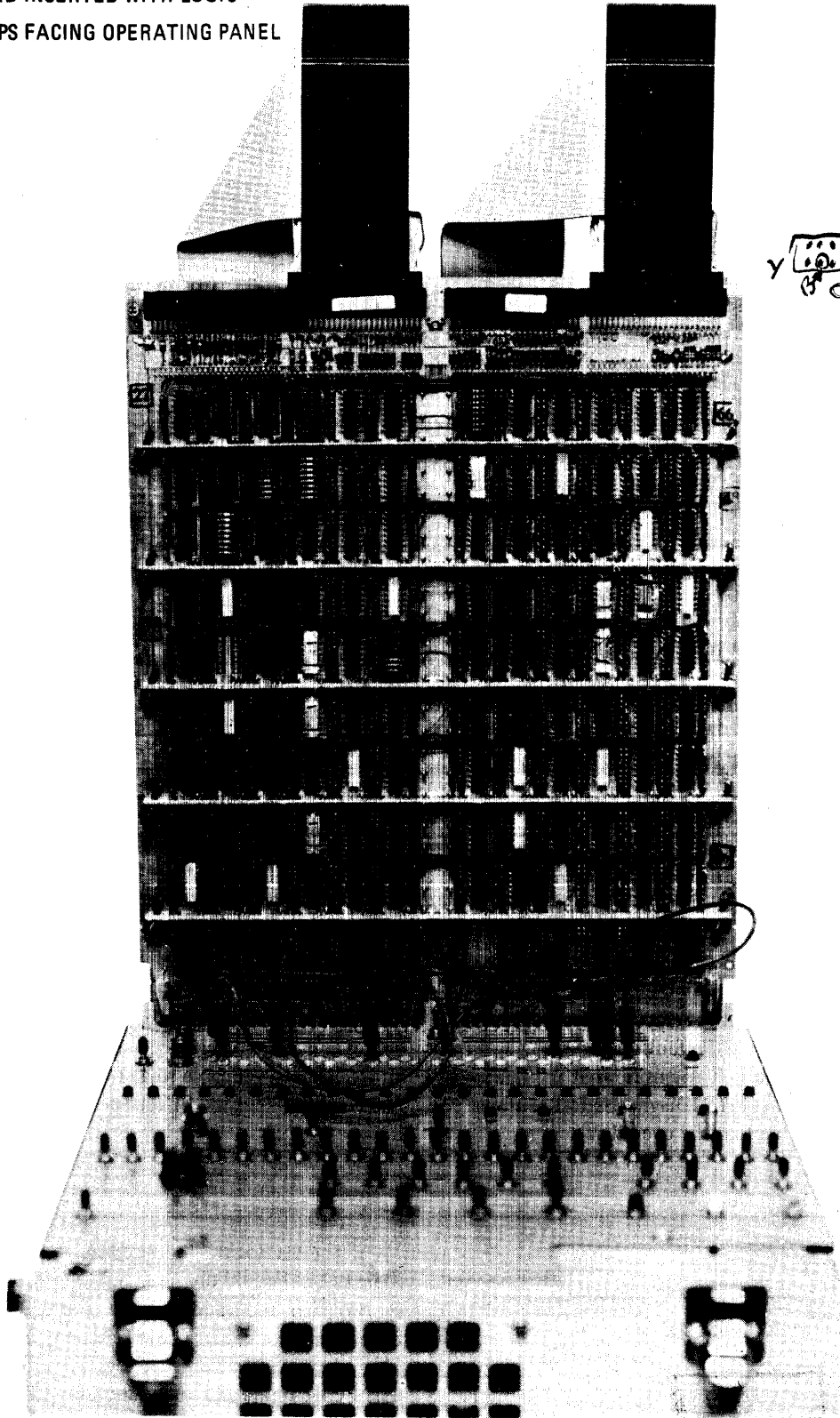


Figure 1-1. Typical B1700 Logic Card Prepared for Testing.

Introduction and Operation

PULSE COUNTING PROBE
CONNECTED TO PCP JACK

FRONTPLANE CONNECTOR
USED FOR CHIP CLIP
(EITHER F0 OR F1)

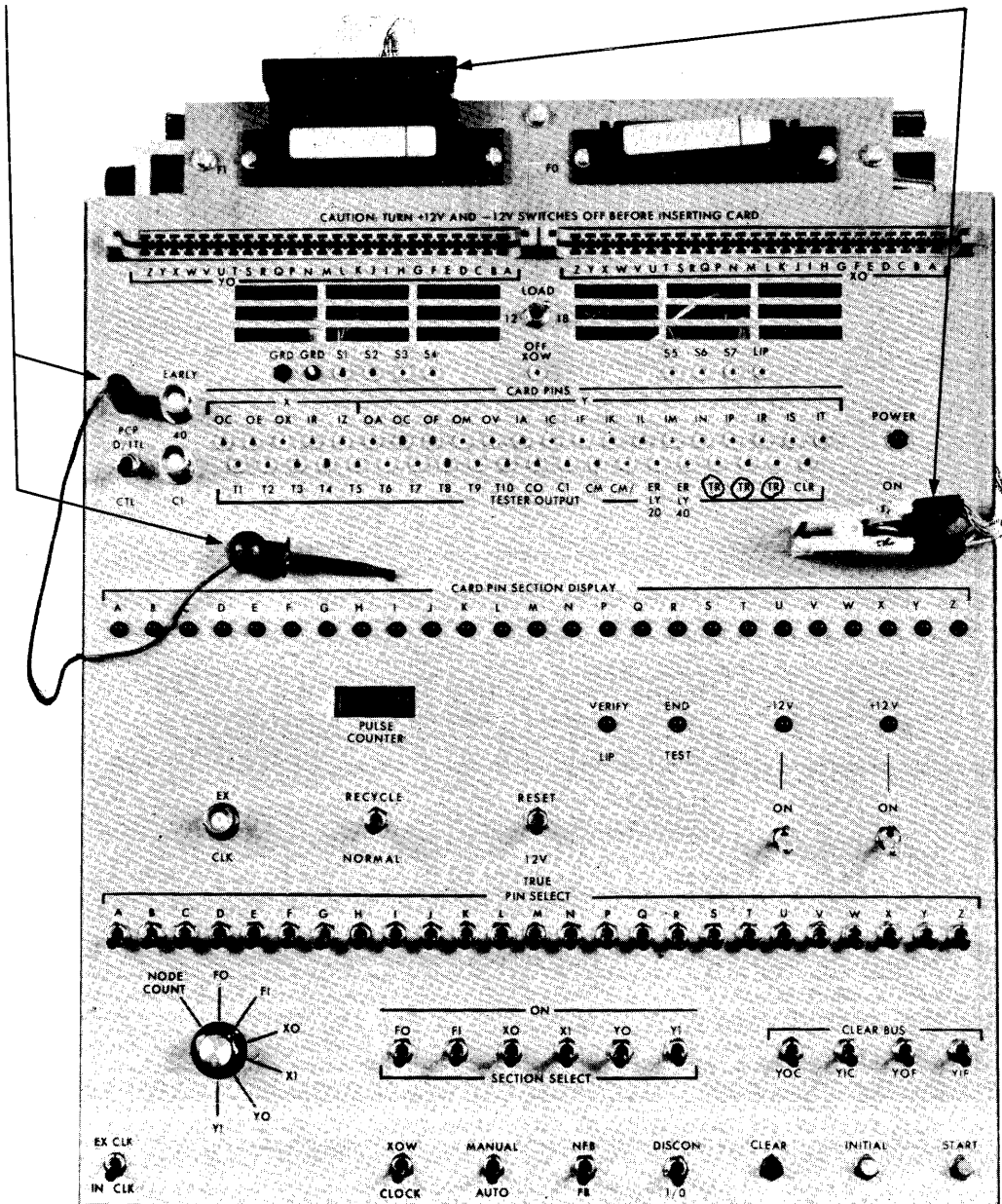


Figure 1-2. Field Card Tester

Introduction and Operation

Operating Panel

The operator's switch panel comprises 43 switches, providing sufficient flexibility to diagnose and locate logic card faults. The main function of the switch panel is to precondition the FCT logic via the Section Select, Pin Select and DISCON-1/0 switches. Panel controls will also select the front plane or backplane connector pins or Node Count for display purposes. Special loading resistor networks for internal clock and type of logic under test are switchable. Remaining switches include Manual/Auto, Feedback/No Feedback, Internal/External Clock, ± 12 volts and Master Power on/off.

Lamp Display

The lamp display is composed of 30 light emitting diodes (LED's). The display is divided into a 25 card pin display, a 4 digit LED octal pulse counter display and other indicators for power, end of test, ± 12 volts etc. The LED's are illuminated by true logic voltage levels from each card pin selected by the rotary selector switch.

Card Connectors

The FCT includes two 50 socket backplane connectors marked X0, X1, Y0, Y1 and two 50 pin frontplane connectors marked F0, F1. Three 50 way flat ribbon cables are provided with the accessories to connect and test all card frontplane connectors.

SIGNATURE

The true complete signature for any B1700 test-compatible logic card is contained in the 25 pin card pin display at the end of the Test Sequence. A quick visual check of a card signature is displayed by the Pulse Counter. This four digit readout is a partial signature, obtained by sampling 12 logic levels of a card pin connector at the end of a Test sequence. Each card that is test-compatible with the FCT, will exhibit its own unique signature. The signatures of good, correctly functioning cards are recorded in the Card Test Documents which are distributed with each FCT. Therefore the signature of any card under test is compared to the correct signature indicated in the Card Test Documents. If the signatures do not compare, then the FCT has correctly identified the faulty logic card. An incorrect signature however, will not indicate the cause or location of the fault on that card.

NODE COUNT

Faulty components are located by a supplementary test procedure known as the Node Count. In this test, points within the logic circuit are checked and displayed on the Pulse Counter. The card test documents provide detailed instructions for Node Count procedures and lists the correct Node Count values expected for logic signals on the card.

The Node Count is displayed at the end of the Test Sequence with no feedback. By starting with a correct node count it is possible to follow and check each count along any logic signal path. By this signal path count method, the incorrect count will be associated with the faulty component.

TEST CYCLE THEORY

The test cycle will generate a repeatable series of logic signals or bit patterns to a logic card at a clock speed of 1 Megahertz. Higher clock speeds may be employed using an external clock generator connected to the FCT. These bit patterns are referred to as words, which are applied to the card via the backplane and frontplane connector pins. The complete test cycle is divided into 2 phases, beginning with the Clear phase and ending with the Test phase.

CONNECTOR PINS

The total number of card connector pins varies from a maximum of 200 to a minimum of 100. The FCT is designed to test 138 connector pins at a time which includes the complete backplane and 2 frontplane connectors. Also, the card test procedures are divided into sequential steps where each step will test the additional frontplane connectors.

WORD REGISTER

Each FCT connector pin is connected to one stage of a word generator register, therefore making a total of 138 stages. The word register is split into 6 sections for logical reasons and will generate bit patterns or words and apply them to the card. Each section is composed of a shift register with the last stage output connected to the first stage input. One stage in each section includes a logical Exclusive-Or element which will modify the next word in sequence.

CLEAR PHASE

The Clear phase ensures that both the FCT Logic and card under test are cleared to a known state before the Test phase.

TEST PHASE

During the Test phase, the word generator register automatically generates the first word by INLQ. Each word and clock pulse are applied sequentially to the card to logically activate the logic chips and discrete components. The activated logic chip outputs are connected as feedback to the word register inputs to generate the next word in sequence. This process of generating bit patterns or words by the method of the Exclusive-or element and feedback, continues throughout the Test phase. Any logic malfunction however small will modify the final signature, due to the feedback principle.

Introduction and Operation

CLOCK CONTROL

An exact number of clock pulses are issued for each Clear and Test phase, controlled by a pulse counter. One word is generated for each clock pulse. The precise number of words applied to a card during the Test phase will be 1,048,576. The complete test cycle duration is 2.1 seconds when operating at a clock speed of 1 Megahertz.

DISPLAY

The logical state of each connector pin may be displayed on the operating panel. At completion of the Test phase, the card pin lamp display pattern is known as the complete Card Signature. A sample of the card pin display is decoded and displayed on a 4 digit octal readout. A value can be displayed for each FCT connector, enabling the FE to quickly determine that the card is functioning correctly.

SELF CHECK FEATURE

Since the FCT is to be used as the primary tool for testing and locating logic faults, the FCT itself must be tested. Therefore a self check feature is incorporated into the FCT logic that enables the FE to verify the FCT is operating correctly. The internal logic is subjected to the same Clear and Test phases and number of words as generated for any B1700 card under test. The final card pin display signature and octal readout display value is compared to the correct values contained in the Card Test Documents.

CARD DESCRIPTION

This card contains:

1. Parity Check.
2. ML Register
3. 1/2 Rotator Control
4. Rotator Control Translator.
5. MEX to Rotator
6. Memory Read Data to MIR.
7. Rotator.

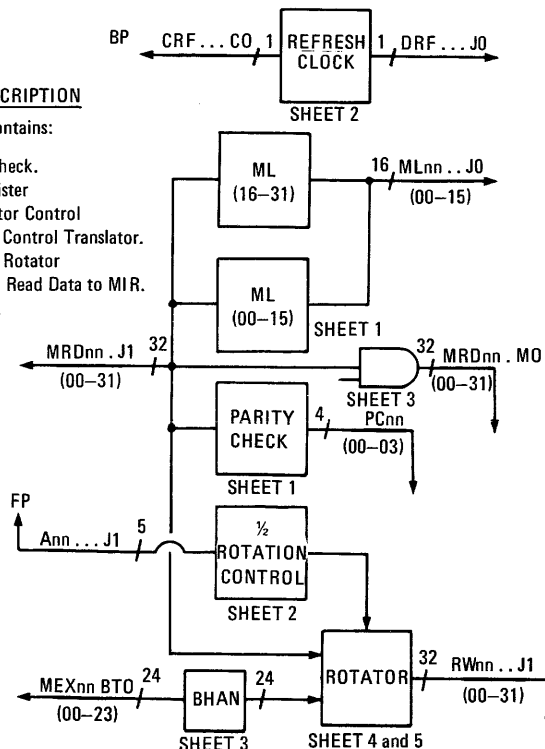


Figure 1-3. Card Block Diagram (Card J).

CARD TEST DOCUMENTS

Card test data documents are provided for all B1700 logic cards that are test-compatible with the FCT. For each card the information contained in these documents is as follows.

Revision History Sheet

The history sheet lists a description of the revision, its revision suffix, revision date and lists the EI/ECN's relevant to that card.

Card Description

Briefly describes the logic and control function contained on that card, as shown in Figure 1-3.

Test Flow Diagram

Indicates, step by step as shown in Figure 1-4, the fault procedure to be followed to isolate the faulty logic component on the card.

Card Block Diagram

Illustrates a simplified logic block diagram showing important logic signals. The block diagrams are partitioned and relate the logic schematic page number to the block diagram, also shown in Figure 1-3.

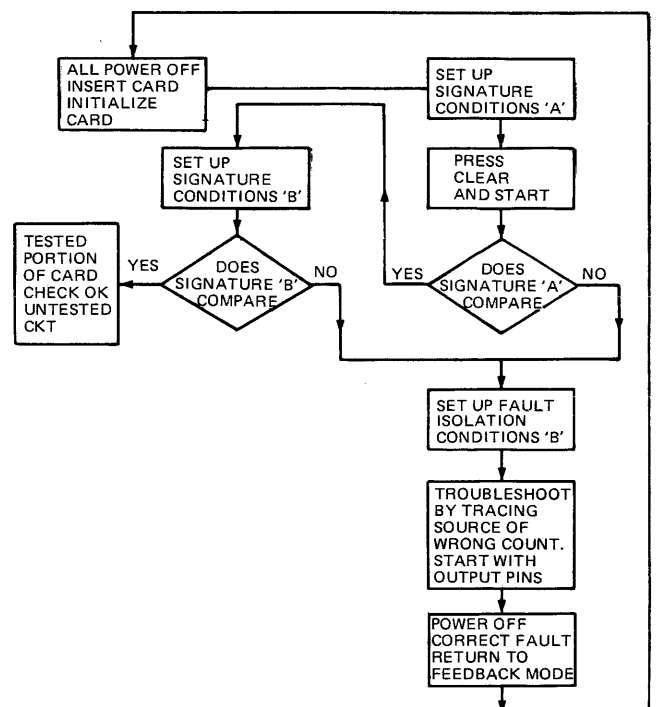


Figure 1-4. Card Test Flow Diagram.

Introduction and Operation

Operating Instructions and Signature

Provides operating instructions necessary to precondition the FCT. A typical signature and card pin lamp display is shown in Figure 1-5.

Node Count

Provides additional instructions for FCT preconditioning for Node Counting, and lists untested circuits. A typical Node Count listing is shown in Figure 1-6.

Node Count Values

Lists in alphabetical order all logic signals, pin location and correct Node Count values.

Early node count listings were alphabetic only. Recent editions are composed of the following:

1. A chip pin-sort list.
2. Input-output card pin list.
3. Alphabetic signal name listing.

CARD HISTORY SHEET

Before beginning a signature or node count test, the FE must ensure that the card under test and card test data documents correspond. The card history sheet must be used to check that card and test documents are related. Each logic card has its own history sheet as shown in Figure 1-7, which records the following information:

1. Engineering changes.
2. Card Order Number.
3. Card Test Data.
4. Logic Card Schematics.
5. Card Circuit Lists.

Card order numbers are changed to show engineering changes and are stamped on the solder side of the card in black eight digit numbers. Caution: the smaller eight digit number, also stamped in black, represents the card assembly number. Each page of the card test documents also shows an eight digit document number. By reference to the card history sheet, the FE can quickly check that the card order number and its related card test document package, do correspond.

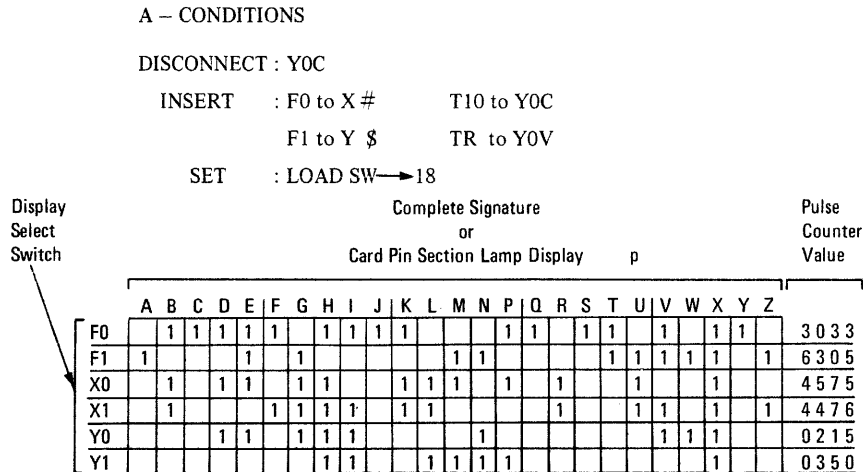


Figure 1-5. FCT Conditions Lamp and Signature Display (For Card J)

CIRCUIT	PIN	COUNT
M E X 2 2 B T O	0 U Y	0 6 2 6
M E X 2 3 . J .	K 9 P	7 7 2 1
M F E T C H F O	1 A Y	6 3 2 2
M L C O N / J .	F 8 D	0 4 3 5
M L C O N T H O	1 C Y	7 3 4 3

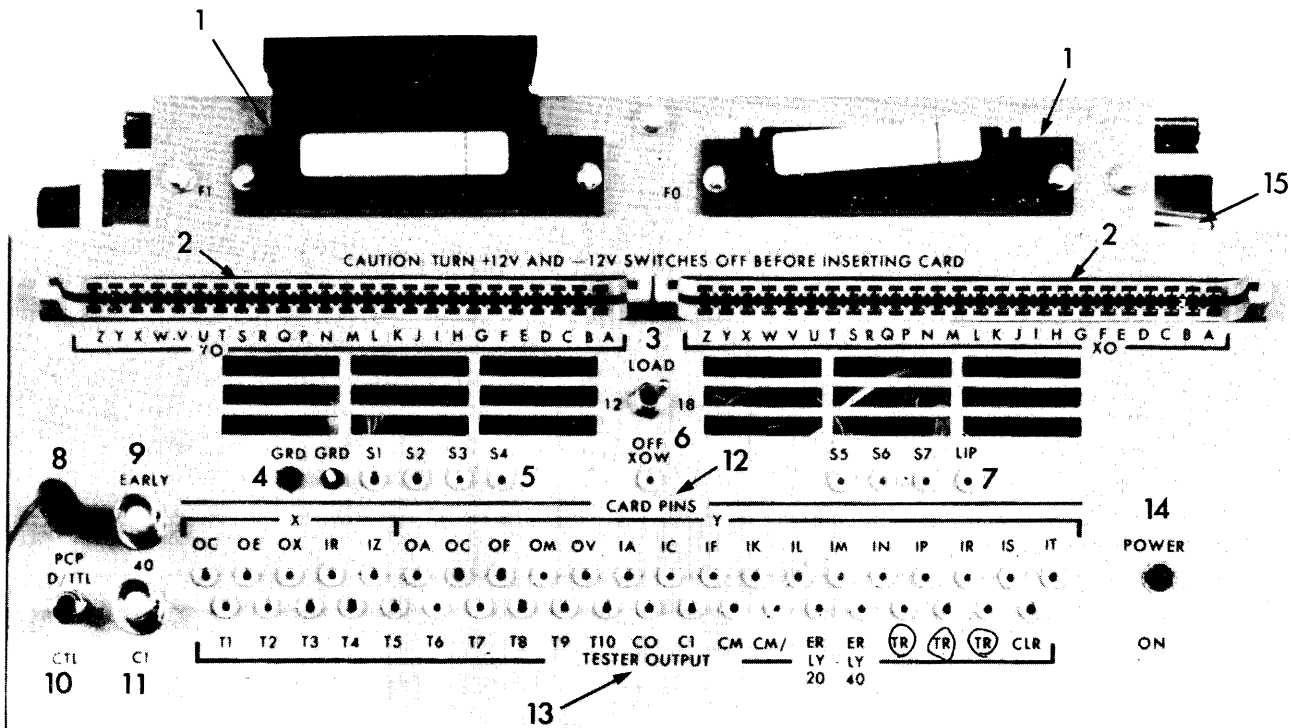
Figure 1-6. Typical Node Count Listing (This list has been shortened for space reasons).

Introduction and Operation

CHG CONTROL DOC NO.	ORDER NUMBER (O N)	CIRCUIT LIST	REV	SCHEMATIC	REV	CARD TEST DATA	REV	REMARKS OR RELATED B P & CARD CHANGES	MFG DASH
ECN 1925 A	2214 2871	T-2203 9325	AI	D-2200 3644	B	B-2207 1757	C	INCORPORATED PIORR EI'S EXCEPT SPCL ASSY INSTR.	
EI 1900 A	2214 2889	T-2203 9325	AJ					TO REDUCE RC NETWORK INDUCTANCE.	
ECN 2077 A								UPDATED SPCL ASSY INSTR COORD WITH ECN 1925.	
EI 2052 A	2214 2897	T-2203 9325	AK					WIRE CHANGE REQUIRE IF CARDS W/W WITH CD DECK AH.	
ECN 3089 A		T-2203 9325	AK	D-2200 3644	B	B-2209 7588	A	INCORPORATED EI'S CHANGED P/N CD TEST DATA.	
EI 3447 A	2214 2905							ADDED (116) 16 PIN SOCKETS TO CD ASSY.	
EI 3375 A	2214 2913							CHANGE CAP VALUE AND QUANTITY.	
EI 3377 A	2214 2921							CHANGE CAP VALUE AND QUANTITY.	
ECN 3673 A		T-2203 9325	AK	D-2200 3644	B	B-2209 7588	A	INCORPORATED EI's.	
ECN 3669		DELETED WIRE WRAPPED CARD AND					REPLACED		
		WITH ETCHED		CARD, P/N		2208 0972,	CD	J ASSY-S PROG.	
EI 3699 A	2214 2921	T-2203 9325	AK	D-2200 3644	B	B-2209 7588	A	RLSD HISTORY SHEET	
EI 4448 A 1-3-74						B-2209 7588	B	ADDED ADDITIONAL INCOMPATIBLE NODE COUNTS.	

Figure 1-7. Logic Card History Sheet (Example Only)

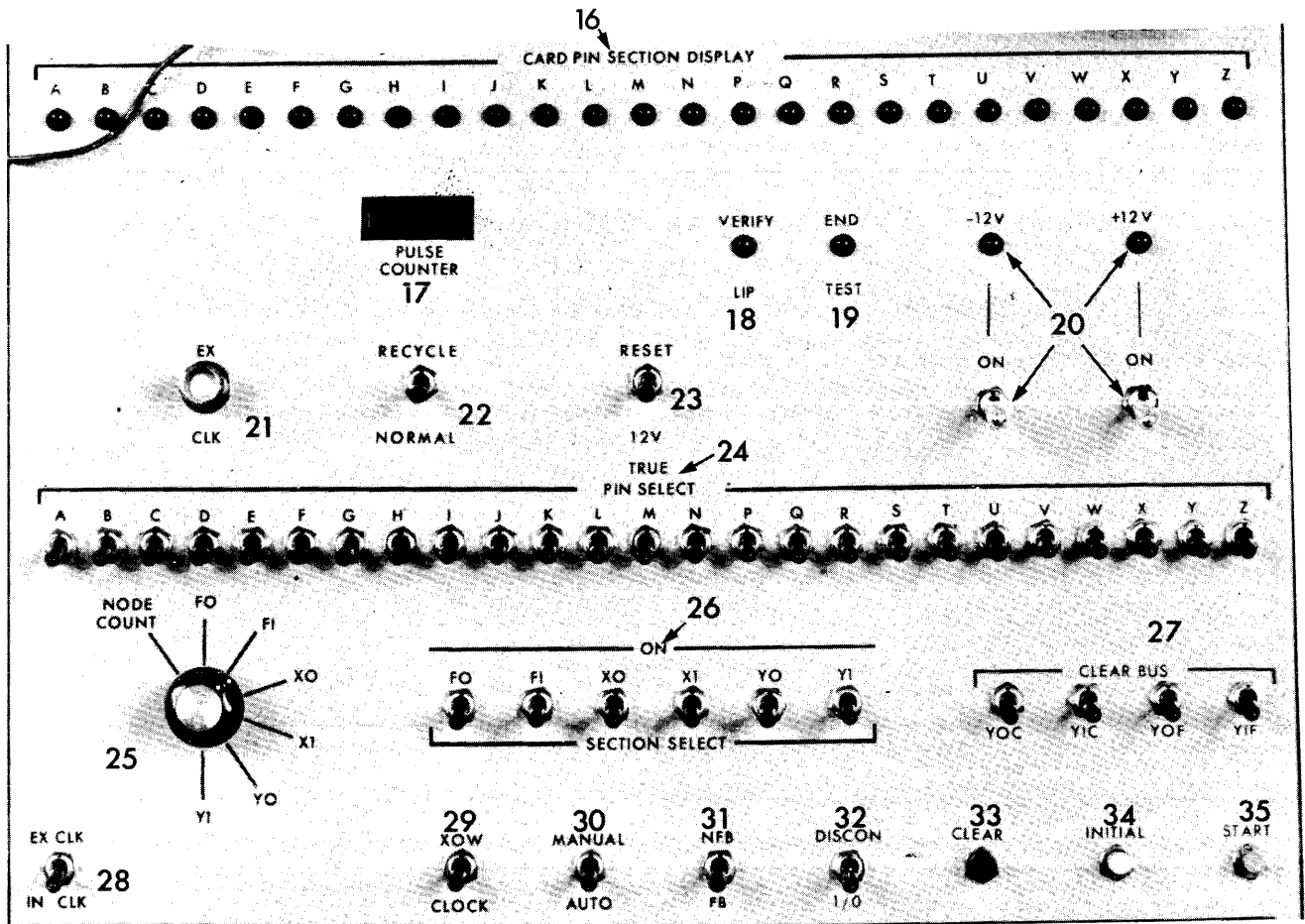
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1. Frontplane cable connectors F0, F1.
2. Backplane connectors.
3. Load Switch.
4. Auxiliary logic grounding.
5. Test Jacks S7 = 11N32KPO
S1 through S6 not used.
6. XOW Clock Jack.
7. Logic Input Probe Jack (LIP).
8. Pulse Count Probe Jack (PCP).
9. Coaxial Clock Output.
10. Logic Load Switch D/TTL-CTL.
11. Coaxial FCT Clock Output.
12. Card Pin Jacks (X and Y).
13. Tester Output Jacks.
14. Power on Indicator (+4.75v).
15. Main Power on/off switch.

Figure 1-8. Upper Operating Panel Detail.

Introduction and Operation



16. Card Pin Section Display
17. Pulse Counter
18. Verify LIP Indicator
19. End of Test Indicator
20. $\pm 12v$ Switches and LED's
21. External Clock Coaxial Connector
22. Recycle/Normal Switch
23. Reset Switch for $\pm 12v$ Relay.
24. Pin Select Switches.
25. Rotary Display Switch.
26. Section Select Switches.
27. Clear Bus Switches.
28. External/Internal Switch.
29. XOW/CLOCK Switch.
30. MANUAL/AUTO Switch.
31. NO FEEDBACK/FEEDBACK Switch.
32. DISCONNECT/1-0 Switch.
33. Clear Pushbutton.
34. Initial Pushbutton.
35. Start Pushbutton.

Figure 1-9. Lower Operating Panel Detail.

Introduction and Operation

OPERATING PANEL DETAILS

The upper and lower operating panel details are shown in Figure 1-8 and Figure 1-9 respectively.

MASTER POWER ON/OFF

This switch controls the application of the +4.75v and -2.00v logic voltage supply from the processor to the FCT. The power on indicator (LED) is illuminated by +4.75 volts supplied through this switch.

FRONT PLANE CONNECTOR

Two 25 pin connectors, labelled F0 and F1, are used to connect and test logic cards fitted with frontplane connectors. Flat ribbon cables are provided with the FCT accessories for mating the frontplane connectors to the FCT. For cards with more than two frontplane connectors, then the card test instructions will specify more than one test sequence. Each test sequence will use a different frontplane connector configuration to test all connectors.

BACKPLANE CONNECTOR

Two 50 pin backplane connectors are provided, into which the card under test is inserted.

CAUTION

The card must be inserted with the logic chips facing the operating panel, as shown in Figure 1-1. Failure to observe this precaution will severely damage the card.

The usual device, ensuring correct card insertion has been removed to allow the FCT cover to fit. Connector designations and card pin identities as shown on the operating panel corresponding to the processor backplane.

LOAD SWITCH

A three position switch for selecting the correct loading resistor network for the clock line. Manually set according to instructions contained in the card test data for that card under test. The clock resistor network provides for:-

1. 12 clock loads.
2. No clock loading.
3. 18 clock loads.

CARD PIN SOCKETS

These sockets are directly connected to card pins on the backplane connector of the FCT. All 21 card pin sockets are designated by connector (X or Y) and by card pin location (OC thru' IT). Patch cards are inserted into these sockets during a Signature or Node Count test sequence, according to card test data instructions.

TESTER OUTPUT SOCKETS

The FCT logic generates special signals which are distributed from these tester output sockets through patch cards to the card pin sockets. Cards which require special signals for logic clearing purposes, must use these sockets. Signals generated and distributed from the tester output sockets are described in the following text.

T1 thru T10.

These signals are clock signals, active only during the clear phase. Signal T1 frequency is 500 KHZ if the internal clock is used or half the external clock rate. Signals T2 thru' T10, are generated by a series of divide-by-two circuits, using T1 as the basic input signal. These signals switch on the trailing edge of the clock signal at XOW.

TRUE

A true signal, shown as TR, provides a constant true logic level. There are three sockets that distribute a true (TR) signal.

CLEAR

A clear signal, shown as CLR, provides a constant logical true output during the clear phase only of a test cycle. The clear (CLR) socket completes the series of tester output sockets.

LOGIC INPUT PROBE

The logic input probe is inserted into the socket marked LIP and in conjunction with its LED indicator, are used to indicate the logic state of any card signal. The LIP indicator will be ON for a true and be OFF for a false logic level.

PULSE COUNT PROBE

The pulse count probe is inserted into the socket marked PCP, when checking node counts on a logic card. The PCP socket is connected to the pulse counter logic which will display the card pin node count at the end of the test sequence.

D/TTL - CTL switch

Selects the correct loading network to match the type of logic being checked by the node count method. The switch position will vary according to instructions contained in the card test documents.

CLK 0 (Clock 0)

This signal is essentially the FCT system clock. When the internal FCT clock is used then CLK 0 will have a frequency of one megacycle, with a mark to space ratio of

Introduction and Operation

710 nanoseconds to 420 nanoseconds. This clock signal is active at all times even when the FCT is in the manual mode. The socket CLK 0 provides a convenient external point for checking the FCT clock pulse wave form and frequency.

CLK 1 (XOW CLOCK)

This clock signal output is identical to that distributed at XOW when the switch XOW/CLOCK is in the clock position. However, CLK 1 is generated independently to the setting of this XOW/CLOCK switch. Also connected to a coaxial connector.

CM and CM/ (Write Enable)

These two clock signals occur slightly earlier than the FCT clock and are used for writing into and reading from 64 bit RFCN's and 256 bit RFDN memory chips. Both CM and CM/ are active for the complete period between start button release and end of the test cycle.

EARLY 20/40 CLOCKS

These signals, abbreviated to ERLY, are similar to the XOW clock signal, except that they occur 20 or 40 nanoseconds earlier. These signals are active for the complete period between start button action and end of the test cycle. Early 40 is also connected to the coaxial connector.

CARD PIN DISPLAY

The card pin section display is composed of 25 light emitting diodes (LED's), marked A thru' Z, except O. Each LED displays the logic state (true or false) of its corresponding card pin of the card connector selected by the rotary Section Display Selector. For design reasons, the outputs of the card under test and the FCT word generator output buffer stages are strapped together, effectively making an OR-GATE. Therefore the card pin display LED's are illuminated by either (or both) of the following conditions:

1. The card under test supplies a positive voltage to that pin.
2. The corresponding word generator buffer stage is set and its Disconnect Latch was not set.

Due to this OR-GATE the pin display LED's will indicate the state of the word generator and card if the following conditions are followed. Display the word generator by either (or both) of the following conditions:

- 1) Disconnect Latches not set.
- 2) No card inserted into FCT.

Display the card outputs only if:—

- 1) The corresponding word generator stage was set to zero.
- 2) The corresponding Disconnect Latch was set.

Some backplane pins are permanently reserved for distributing +4.75 and -2.00 volts and logic ground to the card. Therefore the corresponding LED's will not illuminate when selected for display. These reserved backplane pins are shown in Figure 1-10.

+ 4.75v	-2.00v	GROUND
XOA	YOZ	XID
XIA	YIZ	XIJ
		XIW
		XIQ
		YID
		YIJ
		YIW

Figure 1-10. Reserved Backplane Pins.

To supply ± 12 volts to specific logic cards, three backplane pins are used, designated YIA, YIL and XOZ.

PULSE COUNTER DISPLAY

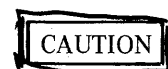
The display is composed of a four digit LED read out, counting in octal from 0000 to 7777. When tracing and locating logic faults the pulse counter displays the node count of the logic pin being tested. When the start push-button is released the display remains at a value of 0000 during the Clear phase and counts during the Test phase. The final count is then compared with the correct node count shown in the Card Test Documentation. For convenience, a selected portion of the card pin display bit patterns are also displayed by the pulse counter for quickly checking the overall logic condition of a card.

END OF TEST INDICATOR

Indicates completion of test. Goes off when the start pushbutton is pressed, and is illuminated at the end of the Test Phase.

 ± 12 v SWITCH AND INDICATORS

Two LED indicators, one marked +12 volts and the other marked -12 volts are illuminated when their respective switch is ON. The switches fitted below each voltage indicator distribute ± 12 volts to specific FCT backplane pins. The -12v feeds pins YIA and XOZ, whilst +12v feeds pin YIL. Some B1700 logic cards do not require ± 12 volts for testing purposes. Therefore, FE's must conform to Card Test Data instructions regarding the ± 12 volt application to the card under test.



INCORRECT APPLICATION OF ± 12 VOLTS WILL DAMAGE THE LOGIC CARD.

Introduction and Operation

12v/RESET SWITCH

This spring return switch (S6) and associated relay (K1) is fitted to recent FCT models to prevent ± 12 volts being applied by mistake, to the card. Relay K1 will energise when a card is inserted and the 12v/Reset Switch selected towards the reset position. The required ± 12 v may then be applied by selecting the appropriate ± 12 v switch.

NORMAL/RECYCLE SWITCH

In the normal position, this switch permits one complete test sequence to occur. Normally used for Signature testing. Whilst the recycle position will permit an automatic repetition of complete test sequences to occur. The recycle function is used during node count testing.

PIN SELECT SWITCHES

There are 25 pin select switches marked A thru' Z, except O. Each switch position corresponds to one stage of the word generator section as determined by the Section Select switches. The pin select switches are used to set a stage or to set a Disconnect Latch of any stage and in any section of the word generator register. The type of operation on the word generator depends upon the DISCON/1-0 switch position.

EXT: CLOCK CONNECTOR

The coaxial connector, marked EX CLK, provides the possibility of connecting the FCT to an external clock signal.

SECTION DISPLAY SELECTOR

This display selector is a seven position rotary switch which controls the card pin section display and pulse counter. The switch positions are marked as follows: (1) Node Count (2) FO (3) F1 (4) XO (5) X1 (6) Y0 (7) Y1. Functions of the display selector are as follows:

1. Node Count – In this position the pulse counter displays the node count value obtained by circuit sampling, using the pulse counter probe.
2. Switch positions FO thru Y1 – From any one of these six positions the FCT will display the complete bit pattern (or signature) on the card pin section display. The switch also decodes a selected portion of the bit patterns into a four digit octal readout for pulse counter display.
3. Frontplane Connector FO, F1. – The chip clip may also be inserted into either of these two connectors when testing individual chips or small circuit strings.

SECTION SELECT SWITCHES

There are six section select switches, marked (1) X0,

(2) X1, (3) Y0, (4) Y1, (5) F0, (6) F1. These switches select the required section of the FCT word generator. These switches are selected in combination with the Pin Select and Discon/1-0 switches to modify the word generator register, according to Card Test Data instructions.

CLEAR BUS SWITCHES

Four switches, marked Y0C, Y1C, Y0F and Y1F are logically connected to their corresponding pins on the backplane connector. Early in the test cycle, automatic clear signals are applied to these four pins regardless of clear switch settings. Normally the clear bus switches are OFF during the test cycle unless instructed otherwise in the Card Test Documents. Any clear bus switch in the ON position, logically disconnects the pin from the word generator and the pin remains at zero throughout the test cycle. This will reduce the effectiveness of the FCT diagnostic ability.

INTERNAL/EXTERNAL CLOCK

This switch, marked in CLK/EX CLK, selects the required clock for the FCT electronics and the card under test.

XOW/CLOCK

This switch selects the signal to be connected to pin XOW of the card under test. Certain B1700 logic cards use pin XOW as a clock input, whilst others use XOW as a normal logic signal. In the XOW position, the word generator stage is connected to pin XOW. When in the CLOCK position the clock signal is connected to pin XOW. No feedback will occur from pin XOW, in the CLOCK position, even though the corresponding word generator remains active.

MANUAL/AUTO SWITCH

When in MANUAL, one clock pulse will occur for each start pushbutton action. While in AUTO the FCT will perform the complete card test sequence for each Start pushbutton action. The complete card test sequence begins with the Clear cycle automatically followed by the Test cycle. During each cycle 2^{20} clock pulses will occur. The duration of each cycle is controlled by a clock counter, which indicates the end of the Clear cycle by the signal T21 and the end of Test cycle by T22.

FEEDBACK/NO FEEDBACK

This switch, marked FB (feedback) and NFB (no feedback), determines whether the card outputs are to be used as feedback to the word generator register. Feedback from the card outputs are used to contribute in the determination of the next bit pattern in the word generator. This switch is

Introduction and Operation

set to feedback (FB) for card signature (GO/NO GO) testing. The no feedback (NFB) position is used for fault location and node counting. No feedback must be used for fault location. Because a faulty logic circuit in one logic area will modify the node count of its adjacent logic circuit that is functioning correctly, therefore making fault location impossible. Instructions specifying the required switch position will be found in the Card Test Data.

DISCON-1/0 SWITCH

This switch marked DISCON and 1/0, determines the type of operation performed by the Pin Select switches. The DISCON-1/0 switch is used in conjunction with the following switches:

1. Pin Select switches
2. Section Select switches
3. Initialize pushbutton

These switches are used to pre-condition or initialize the FCT. Complete instructions for these switch positions are contained in the Card Test Data documents.

DISCON

This position will set a DISCONNECT Latch of the word generator stage if the corresponding Pin Select switch is in the ON position. The choice and number of Disconnect Latches to be set depends upon the Pin Select switches that are selected. A Disconnect Latch when set, will logically disconnect a word generator stage output from the card pin under test. The Card outputs of disconnected stages are connected to word generator inputs as feedback in the usual way, if the Feedback switch is switched to FB. A Disconnect Latch can only be reset by the following procedure:

1. Set Pin Select switch to OFF.
2. Set DISCON-1/0 to DISCON.
3. Depress the Initialize pushbutton.

1/0

This position is marked 1/0 representing one/zero, will store the Pin Select switch positions into the corresponding stage of the word generator register during the clear phase. The Pin Select switches in the ON position will store a one (1) whilst in the OFF position stores a zero (0). The patterns of 1's and 0's are referred to as a word, which will vary according to the card under test. The contents of the word register are changed during the Test phase therefore this Initialization process of pre-conditioning the FCT must be repeated for each test. Those cards that are completely cleared by a single pulse on pins Y0F, Y1F, Y0C and Y1C can use any word because the card is cleared early in the Test phase.

CLEAR SWITCH

When actuated, the clear pushbutton will clear all FCT registers to zero.

INITIALIZE SWITCH

When actuated, the initialize pushbutton will perform the operation indicated by the DISCON-1/0 switch on the word generator register stages selected by the Section Select and Pin Select switches. Used to load the selected word into the word generators register or to set the Disconnect Latches.

START PUSHBUTTON

The release of the Start pushbutton will start the complete test sequence. The test sequence begins with the Clear phase followed automatically by the Test phase. A counter controls the duration of each phase with the signal T21 terminating the Clear and signal T22 terminating the Test phase. In the manual mode, one clock pulse is generated for each Start pushbutton release.

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FCT OPERATING PROCEDURES

An example of FCT operating procedures (page 1) is reproduced in Figure 1-11 and 1-12. Information contained on page 1, shows the precautions and preliminary checks to be followed before card insertion. The FCT self-checking test sequence and signature is outlined in Figure

1-12, step 12.

It is impractical to provide complete FCT operating instructions in this manual for all B1700 FCT compatible logic cards. Therefore, the FE must read and conform to the operating instructions detailed in the Card Test Documents.

THE NORMAL POSITION OF ALL SWITCHES WILL BE DOWN OR OFF UNLESS OTHERWISE SPECIFIED.

CHECK FOR:

- MAIN POWER OFF
- 12v SW OFF
- + 12v SW OFF

CAUTION - ± 12V APPLIED IMPROPERLY CAN RESULT IN DAMAGED PLUG-IN CARDS. MODELS WITH THE 12V RESET SW HAVE THESE VOLTAGES INTERLOCKED.

IF OPERATING CONDITION OF THE TESTER IS IN DOUBT. CONSULT THE SELF-CHECKING FEATURE INSTRUCTIONS ITEM 12.

1. INSERT CARD

THIS COMPLETES THE GND TO THE 12V INTERLOCK AND ACTIVATES THE 12V RESET SWITCH. WHEN + OR -12V IS CALLED FOR IN THE CARD TEST INSTRUCTIONS, THE APPROPRIATE SW MUST BE ACTIVATED FOLLOWED BY "RESET" BEFORE THE VOLTAGE WILL BE PRESENT

2. MAIN POWER ON

3. INITIALIZE TESTER

- DEPRESS CLEAR SWITCH
- PIN SELECT SWITCHES DOWN (A→Z)
- SECTION SELECT SWITCHES UP (F0→Y1)
- I/O SWITCH TO DISCONNECT
- DEPRESS INITIAL SWITCH
- SECTION SELECT SWITCHES DOWN (F0→Y1)

4. CONSULT INDIVIDUAL CARD TEST INSTRUCTIONS

5. TO DISCONNECT A PIN OR GROUP OF PINS

- I/O SWITCH TO DISCONNECT
- MOVE THE APPROPRIATE SECTION SELECT SW UP (ON)
- MOVE THE APPROPRIATE PIN SELECT SW OR SWITCHES UP (TRUE)
- DEPRESS INITIAL SWITCH
- (ANY PIN SELECT SWITCHES LEFT IN THE DOWN POSITION DURING THIS OPERATION ARE CONNECTED)

6. INSERTION OF SIGNALS IS ACCOMPLISHED THROUGH USE OF THE JUMPER WIRES AND CARD PIN JACKS AND TESTER OUTPUT PIN JACKS.

7. THE LOGIC INPUT PROBE (LIP) IS USED IN VERIFYING LOGIC LEVELS. LOGIC LEVELS ARE VISUALLY DISPLAYED IN THE "VERIFY LIP" INDICATOR.

8. THE LOAD SWITCH (THREE POSITIONS) PROVIDES NO LOAD. 12 LOADS OR 18 LOADS AT THE CLOCK LINE XOW.

9. THE SIGNATURE IS OBTAINED AFTER THE SET-UP DESCRIBED FOR THE INDIVIDUAL CARD, BY DEPRESSING CLEAR AND START. THE COMPLETE SIGNATURE IS IN THE BIT PATTERNS OF THE CARD PIN SECTION DISPLAY AS THE SELECTOR IS ROTATED THROUGH THE DESIGNATED POSITIONS.

A SELECTED PORTION OF THE BIT PATTERNS ARE DISPLAYED IN THE PULSE COUNTER DISPLAY FOR CONVENIENCE.

check card

11 card self check

*CL
all sw down
F0→Y1 & I/O sw. up
initial sw
F0→Y1 down
clear start*

*0125
0125
7777
2330
1400
7577*

*card data (A-K)
Test Book*

*To step 12
check manual*

Figure 1-11. Card Test Data Page 1

Introduction and Operation

10. THE NODE COUNTS ARE OBTAINED BY INSERTING THE TEST PROBE INTO JACK PCP AND CONNECTING TO THE APPROPRIATE PIN. THE SELECTOR SWITCH MUST BE SET TO OFF OR NODE COUNT AND THE PB SWITCH TO NO/FB. CLEAR AND START WILL RESULT IN A DISPLAY OF THE NODE COUNT NUMBER IN THE PULSE COUNTER DISPLAY. (SEE NOTE 1) THE RECYCLE SW ALLOWS CONTINUOUS CYCLES.
 11. TO FACILITATE STATIC TESTING OF INDIVIDUAL CHIPS OR SMALL CIRCUIT STRINGS, A CHIP CLIP IS PROVIDED. THE CLIP CABLE IS PLUGGED INTO F0 OR F1 OF THE TESTER AND THE SELECTOR SWITCHED TO THE SAME POSITION. IF THE CLIP IS THEN ATTACHED TO A CHIP, THE STATE OF EACH CHIP PIN (EXCEPT E, M AND L) WILL BE DISPLAYED IN THE CORRESPONDING CARD PIN DISPLAY INDICATOR. IN ADDITION, A TRUE LEVEL CAN BE PLACED ON EACH PIN BY MOVING THE APPROPRIATE PIN SELECT SWITCH TO TRUE (UP) AND DEPRESSING THE INITIAL SWITCH. (THE CHIP CLIP MUST BE ORIENTATED WITH THE CABLE EXITING DOWNWARD.)
3. THE TESTER SELF-CHECKING FEATURE IS PERFORMED WITH NO CARD INSERTED, ALL SWITCHES IN NORMAL, CLEAR AND START SHOULD RESULT IN THE SIGNATURE DISPLAYED BELOW IF THE TESTER HAS BEEN PROPERLY INITIALIZED AS DESCRIBED IN ITEM 3. (THIS TEST IS DONE IN THE FB MODE).

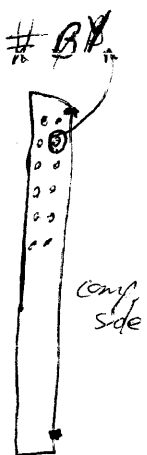


Figure 1-11. Card Test Data Page 1 (cont'd).

	A	B	C	D	E	F	G	H	I	J	K	L	M	N	P	Q	R	S	T	U	V	W	X	Y	Z		
FO					1					1																	0725
F1						1																					0725
X0		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	7777
X1		1																									2330
Y0		1	1	1																							2400
Y1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	7577

* THE TESTER MUST HAVE BEEN INITIALIZED AND CLEARED. IF THE NODE COUNTER IS HOLDING INFORMATION THIS MUST BE CLEARED BY REMOVING THE NODE COUNT PROBE FROM ANY CIRCUITRY AND CYCLING THE TESTER.

NOTE 1. ZERO COUNTS ON THE NODE COUNT LISTINGS CAN BE EXPRESSED IN SEVERAL WAYS AS FOLLOWS:

- [TRUE] ZERO COUNT RESULTING FROM A CONSTANT TRUE [CTR. CYCLES DURING TEST] **9888**
- [FALSE] ZERO COUNT RESULTING FROM A CONSTANT FALSE [CTR. DOES NOT CYCLE] **0000**
- [CLOCK] ZERO COUNT RESULTING FROM A CLOCK SIGNAL OR SYNCHRONISM BETWEEN THE FALSE GOING SIGNAL AND THE TESTER CLOCK.
- [0000] ZERO COUNT RESULTING FROM AN EVEN MULTIPLE OF 7777 (OCTAL) + 1.
- [INCOM] ZERO COUNT RESULTING FROM INCOMPATIBLE LOGIC LEVELS.

NOTE: WHERE MULTIPLE NODE COUNTS ARE LISTED, ZEROS ARE NOT SIGNIFICANT.

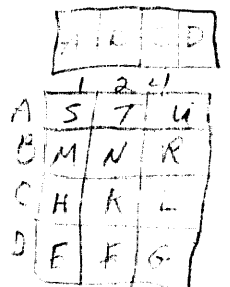


Figure 1-12. Card Test Data

Introduction and Operation

ACCESSORIES

DESCRIPTION and USE

All FCT accessories as shown in Figure 1–13, are identified by a number which is referenced to the following text.

1. Frontplane Cables
 PN 2207 5402 Quantity: 3.
 These flat ribbon cables are used to connect the FCT frontplane connectors F0, F1 to any card frontplane connector.
2. Chip Clip
 PN 2207 7689 Quantity: 1.
 The chip clip can be used to statically test any logic chip soldered to the card. The clip is connected to the chip required and the cable end inserted into either frontplane connector F0, F1. Various logic levels can be applied to the chip thru the operating panel. The card pin section display will indicate the logic state of each chip pin.
3. Coaxial Clock Cable
 PN 2206 5197 Quantity: 1.
 Used to connect the FCT to an external clock generator.
4. Tester to Card Jumpers
 PN 2207 7713 Quantity: 3.
 Used in special cases to apply a true level or signal from the tester output jacks to specific card pins. Alternatively connected to the PCP jack and used as a card pin probe whilst Node Counting any card pin.
5. Insulated Jumper Pins
 PN 2207 7747 Quantity: 6.
 These are used to connect card pins with two wire wrap levels to standard point to point card pin jumpers.
6. Point to Point Card Jumpers
 PN 2207 7705 Quantity: 8.
 Specifically used to re-route logic signals between card pins when locating logic faults.
7. Point to Point Jumpers
 PN 2206 0644 Quantity: 10.
 Commonly used to connect card pin jacks and tester output jacks together according to Card Test Data instructions.
8. Pulse Counting Probe
 PN 2206 9116 Quantity: 1.
 Specifically used when node counting, to connect any logic point to the PCP jack. The probe is composed of spring loaded expanding clip to connect to any logic pin or discrete component.
9. Plastic Cover.
 PN 2207 7754 Quantity: 1
 A waterproof plastic cover is provided to protect the FCT electronics from water during transportation in bad weather.
10. Jumper Chip
 PN 2210 7437 Quantity: 1
 A standard 16 pin jumper chip.
11. DIP Switch
 PN 2210 1778 Quantity: 5
 These dual-in-line package switches (DIP) are inserted into specific DIP sockets on logic cards during the testing procedure.
12. Check List
 This check list is not an accessory. The “out of box” check list is applicable to new Liege manufactured FCT’s. Details of transportation damage and FCT self checking tests must be reported on this list and returned using the pre-addressed envelope.

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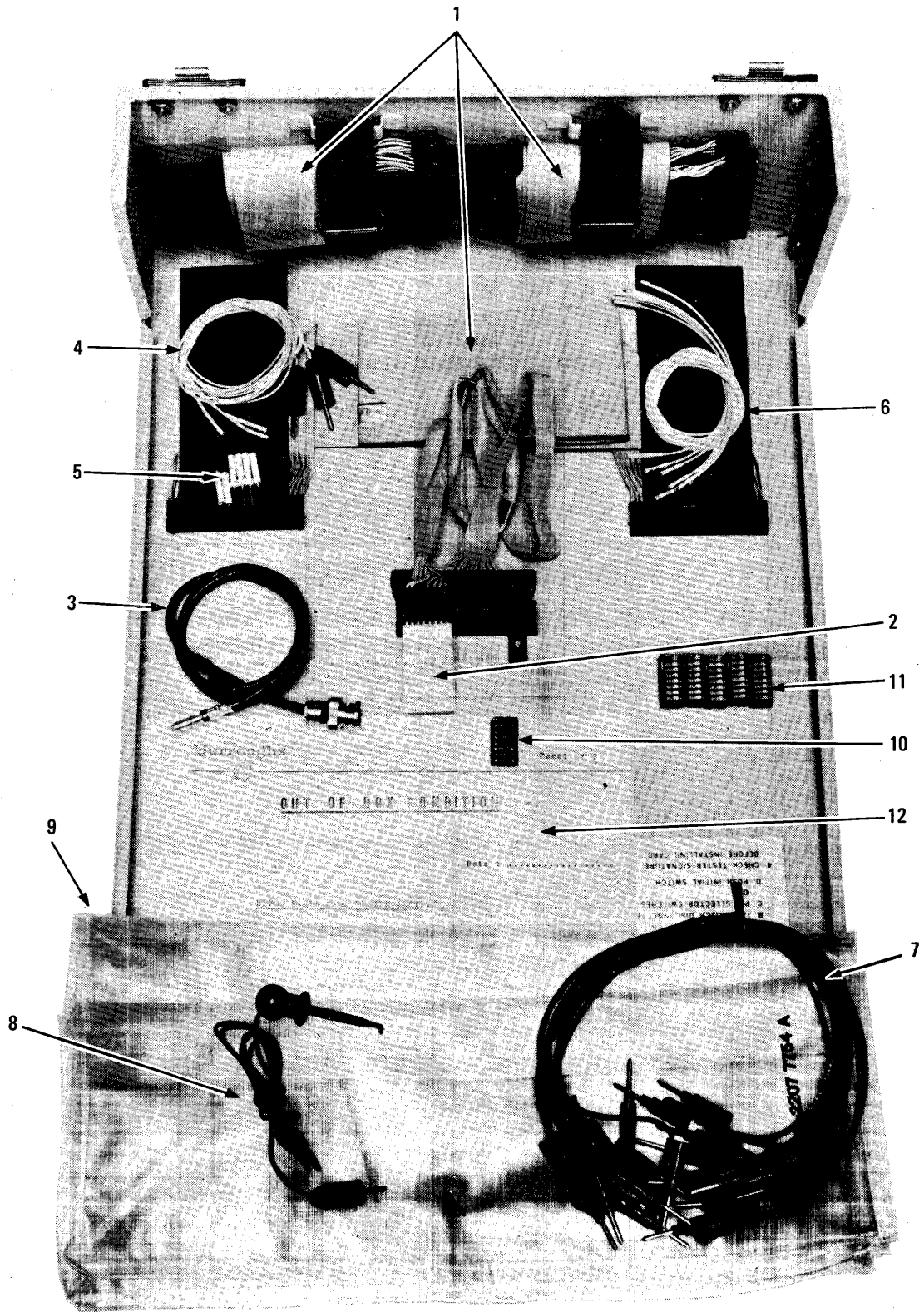


Figure 1-13. Field Card Tester Accessories.

Introduction and Operation

LOGIC SIGNAL GLOSSARY

CL Card.

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LOGIC FUNCTION AND LOCATION	LOGIC SIGNAL, INPUT/OUTPUT PIN(S).
CLEAR ALL SECTION REGISTERS F0,F1,X0,X1,Y0,Y1	Output term CLEARQ → CLRQ/1 . .
CLEAR CLOCK COUNTER	CLEAR A . . True during Start Sequence
CLEAR PULSE COUNTER	CLRNDCT → CLR3 . . . True during Start Sequence. FRERUN/ or True during FRERUN . 0.and T20
CLEAR WORD GENERATOR CLOCK	CLRQT . .
CLOCK COUNTER 8 RFAN's	T-STATES; T01 thru' T22 T21 → End of Clear Phase T22 → End of Test Phase
CLEAR LATCH	CLRN
CLOCK PULSE for clock counter	CLK2
CLEAR PUSHBUTTON (normally open) Operating panel S41 → XAOE	Cross coupled inverter Input OEX → CLRN/0.0
CLEAR PUSHBUTTON (normally closed) Operating panel S41 → XAOJ	Input OJX → CLRN/C.0
COUNT PULSE + 1 to pulse counter from D/TTL and CTL (S3) position.	COUNT . . . Input to RFAN
DISCONNECT LATCH CLOCK	QTINL . . .
EARLY 20 CLOCK marked C1 Operating panel coaxial output and Tester Output jack. J5 → J50 → XAOB → (OBX)	CLK1 . . . 0 Output OBX
EARLY 40 CLOCK Operating panel coaxial output and Tester Output jack. J4 → J50 → YAIL → (ILY)	ERLY 40 . 0 Output 1LY
ENABLE DISCONNECT LATCH INPUT ENABLE INPUT TO WORD GEN:	QTON
END OF TEST LED Operating panel E16	ENGLIG TO Output OIX
FORCE CLEAR TO RESERVED BACKPLANE PINS Y0C,Y1C,Y0F,Y1F.	Output term F5 0 Output 1GX to card Y0 pin 1XY
FORCE START BIT into word generator	INLQ . . . 0 Output 1IY
F0 SECTION SELECT SWITCH Operating panel S26 → XA1T	Input 1TX → F0 0
F1 SECTION SELECT SWITCH Operating panel S27 → XA1E	Input 1EX → F1 0

Introduction and Operation

CL Card

Page 2 of 3.

LOGIC FUNCTION and LOCATION	LOGIC SIGNAL, INPUT/OUTPUT PIN(S)
INHIBIT FEEDBACK DURING CLEAR PHASE	Output term F4/ 0 Output pin 1BX distributed to cards F0/F1 input pins 1XY-0XY X0-X1 input pins 1YY-0YY Y0-Y1 input pins 1YY-0YY.
INITIAL LATCH	INLN Cross coupled inverter
INTERNAL CLOCK	CLK . . . 0 Output 1FX
INITIAL PUSHBUTTON (normally open) Operating panel S42 → YA1V	Input 1VY → INLN/0 . 0
INITIAL PUSHBUTTON (normally closed) Operating panel S42 → YA1U	Input 1UY → INLN/C.0
INITIAL PUSHBUTTON LOGIC	QT1,QT1/,QT2,QT2/
PULSE COUNTER 4 RFAN's	COUNT 1.0 thru' COUNT 12.0 Outputs 1TY thru' 0DY
PULSE COUNTER CLOCK	CLKC1 . . . → CLK2 . . . True during Test Phase (T21 to T22) or True during FRERUN . 0 and T20 to clear RFAN's to zero
PULSE COUNTER PROBE (PCP) J7 operating panel S3 in D/TTL position.	YAOU → Input OUY → COUNT TT.0
PULSE COUNTER PROBE (PCP) J7 operating panel S3 in CTL position.	XAOQ → Input OQX → COUNT CT0 YA0Y → Input OYY → CNTC/T.0
RECYCLE FUNCTION Operating panel S5 contacts 1 2 connects XAOK → XAOT (OKX → OTX)	Input OTX → FRERUN . 0 Output OKX → RECTRU . 0
RECYCLE SWITCH Operating panel S5 → XAOT	Input OTX → FRERUN . 0
SIMULATE START PUSHBUTTON LOGIC during Recycle 2 RFBN's and buffers.	SO2X SO1X
START LATCH	SO1Y,SO2Y Cross-coupled inverter
START PUSHBUTTON (normally open) Operating panel S43 → XA1Y	Input 1YX → SO2 0
START PUSHBUTTON (normally closed) Operating panel S43 → XA0Y	Input OYX → SO1 0
START SEQUENCE FLIP-FLOPS	Output terms F1 thru F5
TESTER OUTPUT JACK Operating panel CLR	Output 1ZX → TRU5 . . 0 → J58 → CLR
TESTER OUTPUT JACK Operating panel S7	Output ODX → 1IN32KP0 → J16 → S7

Introduction and Operation

CL Card
Page 3 of 3

LOGIC FUNCTION and LOCATION	LOGIC SIGNAL, INPUT/OUTPUT PIN(S)
TESTER OUTPUT JACKS Operating panel T1 thru' T10	TEX01 . . 0 thru TEX10 . . 0 Output ORY → TEX01 . . 0 → J39 → T1
TESTER OUTPUT JACK CM/ Operating panel J52 → YA1P	CLKM/ . . 0 Output 1PY
TESTER OUTPUT JACK CM Operating panel J51 → YA1H	CLKMO . . 0 Output 1HY.
XO DISCON : LATCH AND SECTION GENERATOR INPUT ENABLE	XOON . . . 0 (4) Output ORX
XO DISCONNECT LATCH CLOCK	XO1NL . . 0 (3) Output OFX
XO SECTION CLEAR	CLR . . 0 (2) Output 1CX
XO SECTION CLOCK	XOCLK . . 0 (1) Output OCX
<p>NOTE</p> <p>The terms CLK, CLR, INL and ON, as indicated by the Nos. 1, 2, 3 and 4 above, are identical to the 5 remaining sections X1, F0, F1, Y0 and Y1 on this schematic. The logic generating these terms is also identical, therefore these signals are not shown in this glossary.</p>	
X0 SECTION SELECT SWITCH Operating panel S28 → XA1H	Input 1HX → X0 0
X1 SECTION SELECT SWITCH Operating panel S29 → XA1L	Input 1LX → X1 0
Y0 SECTION SELECT SWITCH Operating panel S30 → XA1K	Input 1KX → Y0 0
Y1 SECTION SELECT SWITCH Operating panel S31 → XA1M	Input 1MX → Y1 0
WORD GENERATOR CLOCK	QRCLK . . .

Introduction and Operation

Y0 CARD

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LOGIC FUNCTION and LOCATION	LOGIC SIGNAL, INPUT/OUTPUT PIN(S)
CARD PIN BUFFER OUTPUT	P-CONDITIONS Output term P61 0 Output OAY
CARD PIN FEEDBACK LOGIC enabled if terms P61 0 and NOFEDYO are both true	Output term P61
CARD PIN LAMP DISPLAY LOGIC for Lamp A. Illuminated if Card Pin OAY (P61 0) and YO Section Select (YOREAD . 0) are both True.	Output term LA61 . . . 0 Output pin 1BX
CLEAR BUS SWITCH – YOC Operating panel E32 → YB1K	Input 1KY → YOCCON . 0
CLEAR BUS SWITCH – YOF Operating panel S34 → YB1L	Input 1LY → YOFCON . 0
DISCONNECT CLEAR BUS SWITCH during Clear phase	Input 1XY → F5 0
DISCONNECT LATCHES	4 LFAN's
DISCONNECT SWITCH Operating panel S40 → YC1U	Input 1UY → DISCOT . 0
EXCLUSIVE – OR LOGIC	2 input AFAN
FORCE BIT (Start Sequence)	Input 1MY → INLQ . . . 0
INHIBIT FEEDBACK during Clear phase	Input 1YY → F4/ 0
INPUT CONDITIONS TO CARD PIN BUFFER AND SUM/SHIFT AFAN	Q-CONDITIONS Output term Q61
1/0 INITIAL SWITCH Operating panel S40 → YC1S	Input 1SY → 1/0 INL . 0
NO FEEDBACK SWITCH Operating panel S3 0 → YC1R	Input 1RY → NOFED . . 0
OUTPUT OF DISCONNECT LATCH feeding card pin buffer	Output term LAT 61 . . . of LFAN
PIN SELECT SWITCH – PINA Operating panel S1 → XC1C (Pins B thru L are similar)	Input 1CX → A 0
SET WORD GEN : STAGE RFBN by either of the following conditions: 1) Pin select switch A 0 and 1/0 INYO 2) Sum and shift	S-CONDITIONS Input term S61
SET DISCONNECT LATCH STAGE by Pin Select Switch A 0 and DISCNYO.	Input term LAT611 . . to LFAN

 Introduction and Operation

YO CARD

Page 2 of 2

LOGIC FUNCTION and LOCATION	LOGIC SIGNAL, INPUT/OUTPUT PIN(S)
SUM AND SHIFT LOGIC	3 input AFAN's
YO CLEAR SECTION GENERATOR PULSE	Input 1CY → CLRYO . . 0
YO DISPLAY SELECTOR SWITCH Operating panel S2-6 → YB1V	Input 1VY → YOREAD . 0
YO INITIAL CLOCK PULSE	Input 1FY → YOINL . . 0
YO INPUT ENABLE TO DISCONNECT LATCH AND SECTION GEN:	Input 1PY → YOON . . 0
YO SECTION CLOCK	Input OWX → YOCLK . 0

NOTE

The remaining stages of the YO section register are identical to that described in this glossary. Therefore the remaining logic terms for these stages will not be identified. Furthermore, the logic schematic diagrams for Y1, X0, X1, F0 and F1 are also identical to the YO register glossary. Therefore the FE must identify logic terms and components using the YO card schematic and this glossary and relate to the Y1, X0, X1, F0 and F1 logic schematics.

SECTION 2 FUNCTIONAL DETAIL

BASIC TEST METHOD

The method of testing a B1700 logic card is to generate a repeatable sequence of bit patterns or words. A precise number of generated words are applied to the card under test with each word modified by card feedback. The final logical state of all card pins are displayed and known as the signature for the card. The FCT logic block diagram, as shown in Figure 2-1, indicates major logic areas, signal flows and display indicators when testing a logic card.

A word is 138 bits long divided into 5 Sections X0, X1, Y0, F0 and F1 with one bit corresponding to each card

pin. These words are applied to all backplane and frontplane card pins regardless of which pins are input or output. The logical state of each card connector pin is determined by a backplane wired-or function.

A card input pin will be true if the FCT drives it true. But a card output pin will be true if the FCT output is true or if the logic card output signal is true.

The next word generated in sequence is determined from the present word or bit pattern and feedback signals from the card under test. The 138 stage word generator is basically a shift register divided into 5 Sections X0, X1, Y0,

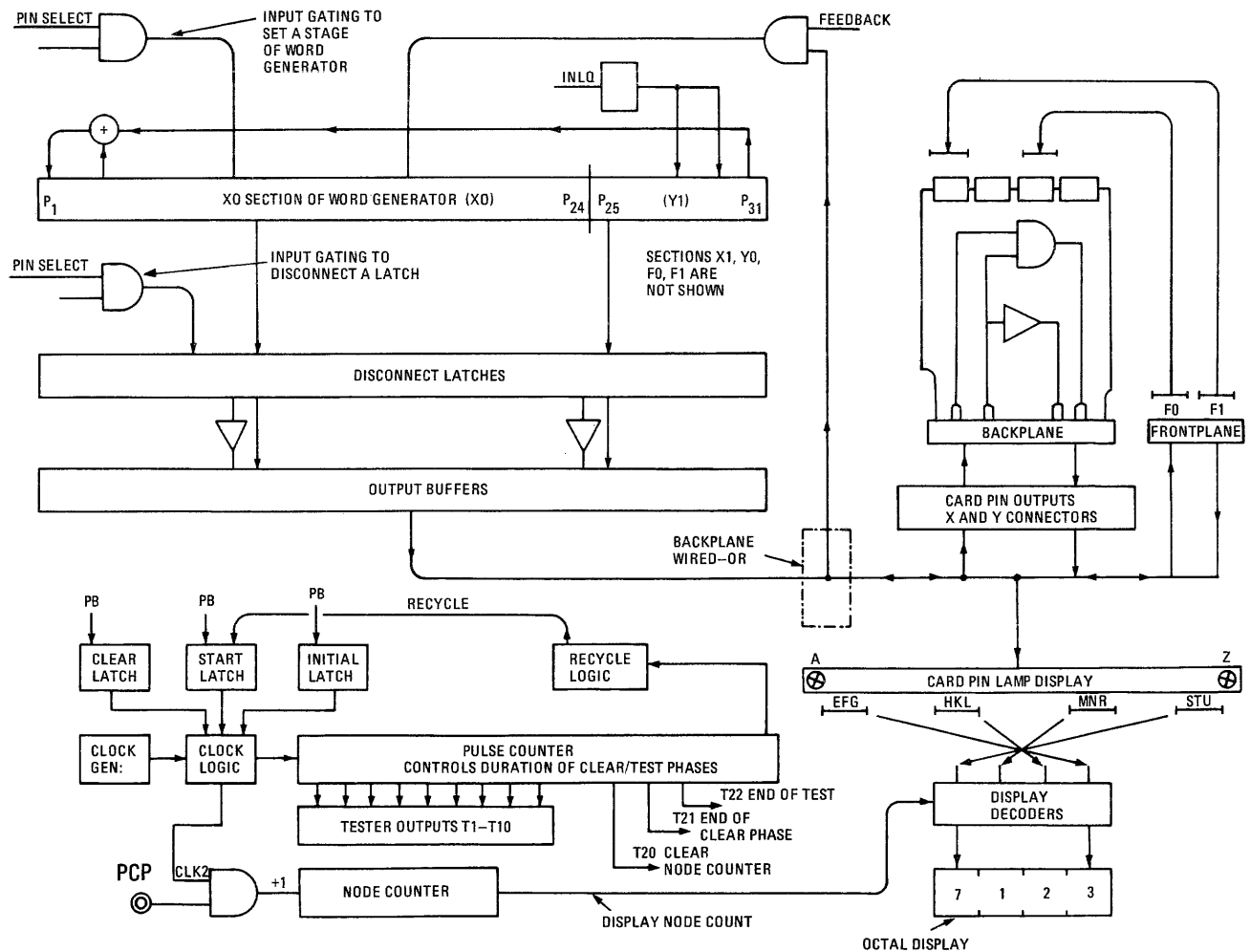


Figure 2-1. FCT Logic Block Diagram

Functional Detail

F0 and F1. Logic within each section includes one exclusive-or, sum and shift logic and a start bit.

Both the card and FCT must be in the initialized condition before starting the word generation sequence. The precise number of words (1,048,576) applied to the card is controlled by a pulse counter. This pulse counter also determines the duration of the Clear and Test Phases of the complete test sequence.

SIGNATURE

The complete card signature is indicated by the card pin section display, at the end of the test sequence. A correct signature is obtained by testing a properly functioning logic card on a FCT, and recording the signature values in the Card Test Data documentation.

In general, the sequentially generated bit pattern or word, modified by exclusive-or and card feedback will not be known. If one bit of a word generated during the test phase is incorrect then the following words will be incorrect. By the shift, exclusive-or, and feedback logic the following words in sequence will be modified and the final card signature will also be incorrect.

SIMPLE SHIFT REGISTER

An introduction to bit pattern generator theory begins with an example of a 4 stage shift register as shown in Figure 2-2. The actual word generator in the FCT will be related to this simple 4 stage shift register, later in this section.

Consider a 4 stage shift register A thru D as shown in Figure 2-2. The signal !NLQ inserts a bit into the B stage for the first word of the Test sequence. Each stage output is connected to the following stage input. Exclusive-or gate (E) obtains its inputs from the shift register outputs C and D. Input to stage 1, is obtained from the exclusive-or gate output. All shift register stages A through D transfers the bit pattern to the next stage at clock time.

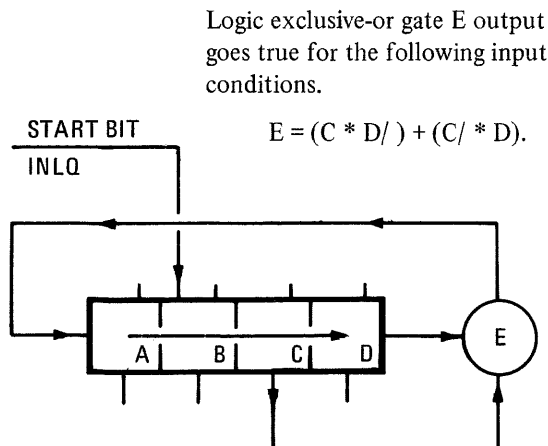


Figure 2-2. Simple Shift Register.

BIT PATTERN GENERATOR

Figure 2-3 shows the bit patterns generated in sequence from the shift register, as shown in Figure 2-2. Start bit !NLQ begins the sequence by forcing stage B to hexadecimal 4. Clock 1 shifts this bit into stage C giving a value of hexadecimal 2. The exclusive-or gate E goes true to enable the stage A input on the next clock pulse. Clock 2 sets stage A by the true exclusive-or condition, and shifts the start bit !NLQ into stage C. At the end of clock 2 the register value equals hexadecimal 9. This sequence continues as shown in Figure 2-3, until Clock 15, where the series of hexadecimal bit patterns are repeated.

Therefore after the reset condition and 15 clocks the register has generated the following values and series:

1. All hexadecimal values generated 0 through F.
2. A non-sequential series of hexadecimal values.
3. Repeats the series of hexadecimal values.

FEEDBACK PRINCIPLE

The principle of applying feedback from activated card logic is to modify each word in the shift register. Each word generated by the shift register is applied to the logic

CLOCK Q	STAGE				EX-OR CD	EX-OR RESULT	HEX DEC
	A	B	C	D			
RESET	0	0	0	0			0
!NLQ	0	1	0	0			4
1	0	0	1	0	TRUE	SET A → 1	2
2	1	0	0	1	TRUE	SET A → 1	9
3	1	1	0	0			C
4	0	1	1	0	TRUE	SET A → 1	6
5	1	0	1	1			B
6	0	1	0	1	TRUE	SET A → 1	5
7	1	0	1	0	TRUE	SET A → 1	A
8	1	1	0	1	TRUE	SET A → 1	D
9	1	1	1	0	TRUE	SET A → 1	E
10	1	1	1	1			F
11	0	1	1	1			7
12	0	0	1	1			3
13	0	0	0	1	TRUE	SET A → 1	1
14	1	0	0	0			8
15	0	1	0	0			4
16	0	0	1	0	TRUE	SET A → 1	2
ETC	1	0	0	1	TRUE	SET A → 1	9

Figure 2-3. Self Generate Bit Pattern

Functional Detail

card as shown in Figure 2-4. Shift register outputs are buffered as indicated by J through M. The backplane wired-or connection of the FCT provides the following functions:

1. Transfers buffer outputs to the logic card inputs.
2. Transfers activated card logic outputs as feedback to the shift register input.

The process of card feedback to the shift register is used to develop each successive bit pattern in addition to the exclusive-or element. Feedback continues for each clock pulse throughout the Test Phase of 1,048,576 clocks. The final bit pattern displayed at the end of the Test Phase will be determined by the following conditions:

1. Logic card design changes by EI/ECN's.
2. The exclusive-or element in the shift register.
3. Type and density of logic elements used i.e. AFAN's, RFBN's, LFAN's or simple gating elements.

Therefore the final signature will be unique for each logic card because of these conditions. If one activated logic

element fails to switch during the Test Phase then the feedback feature will modify the final signature.

SIGNATURE/NODE COUNT

General

Six examples as shown in Figure 2-5, illustrate the effect of faulty logic elements, on the generated shift register bit pattern, over 8 clock pulses. These examples are developed from the simple 4 bit register with feedback as shown in Figure 2-4.

During the Test Phase, however, the FCT applies a total of 1,048,576 clock pulses to the logic card under test.

Therefore, it would be practically impossible to determine each bit pattern during the Test Phase, due to logic complexity and number of clocks. Only the good, final Signature and Node Counts are valuable, and these are listed in the Card Test Documents.

The term shift register, has been used to describe a simple 4 stage shift register as shown in Figures 2-2 and 2-4. But for the large 138 stage version, it is known as a word generator.

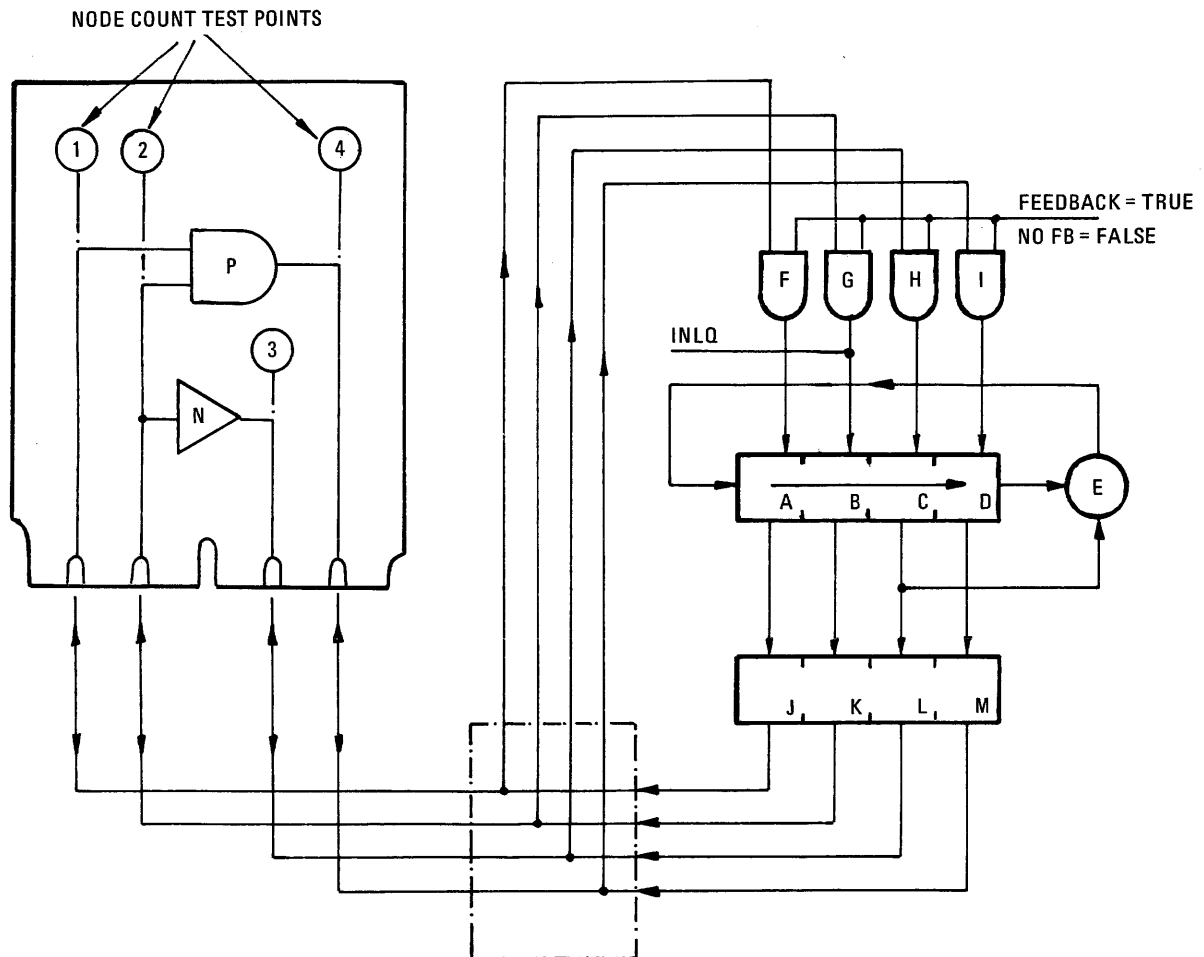


Figure 2-4. Feed Back Principle

Functional Detail

Good Signature
(With Feedback)

This example as shown in Figure 2-5, indicates the And gate (P) and Invertor (N) switching correctly when their logical inputs are activated. Logic card feedback modifies the self generated bit pattern sequence at clock 4 where the hexadecimal value C is modified to 5. Refer to the self generated bit pattern in Figure 2-3, which shows the hexadecimal series as 4, 2, 9, C, 6, B, 5 and A. Both logic elements P and N are switched once during the 8 clock sequence, producing a signature of hexadecimal 7.

Bad Signature
(Fault P with FB)

The And-gate is faulty and fails to switch true when activated. Failure to switch true produces a signature of F after 8 clocks. The expected good signature should be 7.

Bad Signature
(Fault N with FB)

Here the Invertor (N) is faulty and fails to switch true when activated. The result of the Invertor (N) failing modifies the bit pattern and activates the And-gate twice, at clocks 4 and 5, during the 8 clock sequence. A faulty invertor in this example produces a signature of 1 when the expected good signature should be 7.

Good Node Count
(No feedback)

In the NO FEEDBACK mode the shift register is not modified by feedback from activated card logic. The self generated bit pattern series from the shift register shown in Table 2-1, follows the sequence of 4, 2, 9, C, 6, B, 5. This sequence is constant. Node count test points numbered 1 through 4 as shown in Figure 2-4, enable the FE to check

GOOD SIGNATURE WITH FEEDBACK						
HEX DEC	SR				FB	
	A	B	C	D	1	2 3 4
4	0	1	0	0	0	1 0 0
2	0	0	1	0	0	0 1 0
9	1	0	0	1	1	0 1 1
5	0	1	0	1	0	1 0 1
A	1	0	1	0	1	0 1 0
D	1	1	0	1	1	1 0 1
E	1	1	1	0	1	1 1 1
7	0	1	1	1	✓	✓ ✓ ✓ ✓
NODE COUNT =					4	4 4 4 4
SIGNATURE =					7	

- ①
- ②
- ③
- ④

BAD SIGNATURE FAULT (P) WITH FB						
HEX DEC	SR				FB	
	A	B	C	D	1	2 3 4
4	0	1	0	0	0	1 0 0
2	0	0	1	0	0	0 1 0
9	1	0	0	1	1	0 1 1
5	0	1	0	1	0	1 0 1
A	1	0	1	0	1	0 1 0
D	1	1	0	1	1	1 0 1
E	1	1	1	0	1	1 1 0
F	1	1	1	1	✓	✓ ✓ x
NODE COUNT =					4	4 4 3
SIGNATURE =					F	

- ⑤

BAD SIGNATURE FAULT (N) WITH FB						
HEX DEC	SR				FB	
	A	B	C	D	1	2 3 4
4	0	1	0	0	0	1 0 0
2	0	0	1	0	0	0 1 0
9	1	0	0	1	1	0 0 1
C	1	1	0	0	1	1 0 1
E	1	1	1	0	1	1 1 1
7	0	1	1	1	0	1 1 1
3	0	0	1	1	0	0 1 1
1	0	0	0	1	x	✓ ✓ x
NODE COUNT =					3	4 4 5
SIGNATURE =					1	

- ⑥
- ④
- ④
- ①

GOOD NODE COUNT NO FEEDBACK						
HEX DEC	SR				FB	
	A	B	C	D	1	2 3 4
4	0	1	0	0	0	1 0 0
2	0	0	1	0	0	0 1 0
9	1	0	0	1	1	0 1 1
C	1	1	0	0	1	1 0 1
6	0	1	1	0	0	1 1 0
B	1	0	1	1	1	0 1 1
5	0	1	0	1	✓	✓ ✓ ✓ ✓
NODE COUNT =					3	3 4 3
SIGNATURE =					5	

- ②
- ④

BAD NODE COUNT FAULT (P) AND NO FB						
HEX DEC	SR				FB	
	A	B	C	D	1	2 3 4
4	0	1	0	0	0	1 0 0
2	0	0	1	0	0	0 1 0
9	1	0	0	1	1	0 1 1
C	1	1	0	0	1	1 0 0
6	0	1	1	0	0	1 1 0
B	1	0	1	1	1	0 1 1
5	0	1	0	1	✓	✓ ✓ x
NODE COUNT =					3	3 4 2
SIGNATURE =					5	

- ②
- ⑤

BAD NODE COUNT FAULT (N) AND NO FB						
HEX DEC	SR				FB	
	A	B	C	D	1	2 3 4
4	0	1	0	0	0	1 0 0
2	0	0	1	0	0	0 1 0
9	1	0	0	1	1	0 0 1
C	1	1	0	0	1	1 0 1
6	0	1	1	0	0	1 1 0
B	1	0	1	1	1	0 1 1
5	0	1	0	1	✓	✓ x ✓
NODE COUNT =					3	3 3 3
SIGNATURE =					5	

- ⑥
- ④

Notes:

1. Attempt to set C by Invertor N but already true from SR.
2. Set C to 1 by invertor N.
3. Attempt to set D by And gate P but already true from SR.
4. Set D to 1 by And gate P.
5. Faulty And gate P fails to switch to 1.
6. Faulty Invertor N fails to switch.

Figure 2-5. Signature/Node Count Examples.

Functional Detail

each node count using the node count probe and pulse counter. Therefore, Invertor (N) will count thru 4 whilst And-gate (P) counts 3 during the 8 clock sequence. These counts are known as node counts.

Bad Node Count
(Fault P and no FB)

This example shows the result of a faulty And-gate (P) that fails to switch true at clock 4. At clock 8, the node counter will indicate 2 for test point 4, instead of 3. All test points 1 thru 3 will be correct.

Fault isolation is achieved by simply referring to the logic schematics and checking for good input node counts. If both input counts are good to activate And-gate (P) but its output count is bad, then clearly And-gate (P) is faulty.

The shift register is not modified by logic card feedback when node counting.

Bad Node Count
(Fault N and no FB)

The effect of a faulty Invertor (N) will produce a node count value of 3 at test point 3, after 8 clock pulses. If the input node count of the Invertor (N) at test point 2 is good then the invertor has failed to switch true and is faulty.

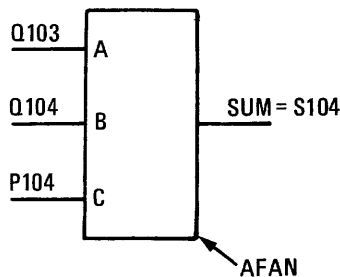
Whenever node counting a logic card, the FE must ensure that the FEEDBACK/NO FB switch is in the NO FB position.

SUM/SHIFT LOGIC

Logical AFAN elements with 3 inputs provide the sum and shift function in the word register. A typical AFAN as shown in Figure 2-6, produces the arithmetic sum from the following inputs:

- A. Adjacent RFBN stage output Q103.
- B. Same RFBN stage output Q104.
- C. Feedback P104.

Five 3 input AFAN's (3) are also shown in Figure 2-8.



$$SUM = C (\bar{A}\bar{B} + AB) + \bar{C} (\bar{A}B + A\bar{B})$$

Figure 2-6. Sum/Shift AFAN Element

The shift element is introduced by summing the output from the adjacent RFBN stage output into the next AFAN input.

EXCLUSIVE-OR AND RETURN LOOP

The exclusive-or logic element is a 2 input AFAN as shown in Figure 2-7. There are 5 exclusive-or logic elements in the word generator, one each for X0, X1, Y0, F0 and F1 sections. A typical AFAN as Figure 2-7, will produce an exclusive-or function from 2 inputs as follows:

- A. Return loop RFBN output stage Q125.
- B. Same RFBN stage output Q103.

An example of a 2 input AFAN (2) is shown in Figure 2-8.

The exclusive-or function is obtained from a typical AFAN by ignoring the feedback input (C) from the logical sum equation from a 3 input AFAN element. Outputs from 2 input AFAN's connected in this way will switch true for logic input conditions of $\bar{A}B$ and AB .

Since 1 input to each AFAN is connected to the adjacent RFBN stage output, then a return loop must be considered. This 2 input AFAN element therefore provides the dual function of an exclusive-or element and return loop conditions.

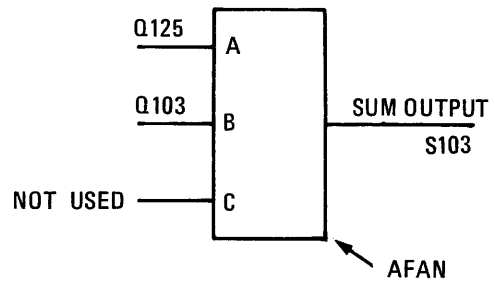
REGISTER STORAGE LOGIC

The four bit storage RFBN (1) as shown in Figure 2-8, stores the following logical input conditions:

- 1. Pin Select switch settings, S1 thru' S4.
- 2. Sum outputs from AFAN's, S101 thru' S104.
- 3. Start bit signal INLQ.

Output RFBN terms Q101 thru' Q104 are distributed to:

- 4. AFAN inputs to contribute to the next word.
- 5. Output buffer (4) inputs to activate the card connect-or pins.



$$EX-OR = \bar{C} (\bar{A}B + AB)$$

Figure 2-7. Exclusive-OR AFAN

Functional Detail

OUTPUT BUFFER LOGIC

The four output buffers (4) as shown in Figure 2-8, activate the card logic by the terms P101 thru' P104. The P terms are true when Q and LAT/input conditions are both true.

BACKPLANE WIRED-OR CONNECTION

The feedback principle depends on the backplane connection (5) as shown in Figure 2-8, by distributing card pin logic levels to the following elements:

1. Feedback And-gates (6).
2. Card Pin Section Display And-gates (7).

FEEDBACK GATING

The And-gates (6) as shown in Figure 2-8, when enabled will distribute the feedback logic levels back to the AFAN sum logic (3).

Feedback is disabled throughout the Clear Phase by F4/ from the start switch logic at inverter (10).

For two clocks at the beginning of the Test phase feedback is also disabled. This allows the start bit INLQ to set the RFBN stages of the word generator.

Feedback is disabled by FOINL during the disconnect latch sequence. This occurs when the output buffers (4) are disabled by a LAT/ from an LFAN latch.

LED DISPLAY GATING

The output terms LA (xxx) thru' LZ (xxx) from the And-gates (7) as shown in Figure 2-8, are connected to the Card Pin Section Display LED's. These gates are enabled by the following logic conditions:

1. Card connector pin terms P (yyy) ... 0, where (yyy) represents and buffer output (8) term.
2. Section selector switch S2 that produces the term (zz) READ, where (zz) represents any section F0, F1, X0, X1, Y0 and Y1.

The 25 LED's labelled A thru' Z (except O) on the operating panel will indicate the corresponding logic card levels for each word generator section. Switch S2 logic terms (zz) READ selects the appropriate section LED display for gating.

START BIT LOGIC

The start bit term INLQ from buffer (8) as shown in Figure 2-8, directly sets the RFBN stage during the Test phase for two clock pulses. The RFBN input terms are preset to a fixed bit pattern for the first word of the Test phase. This allows the self generate and feedback circuits of

the word generator to start functioning. Seven RFBN stages are preset by INLQ at the following locations:

1. F0 at S102.
2. F1 at S102.
3. X0 at S27 and S29.
4. X1 at S55.
5. Y0 at S63 and S67.

DISCONNECT INPUT GATING

The disconnect latch input And gates (7) as shown in Figure 2-9, are enabled when the following conditions are true:

1. Pin Select switch term A thru Z 0
2. Section Select switch term F00N.
3. Switch S40 in the DISCON position.
4. Initialize pushbutton terms QTON and QTINL.

The logic signal QTON has a duration of 4 clock pulses and occurs during the Initialize pushbutton sequence. The And gates (1) and buffer (2) are enabled by QTON to latch the input Pin Select switch levels into the LFAN.

Logical equation to enable And gates (1) is:

$$\text{DISCNF0} = \text{F00N} * \text{QTON} * \text{DISCOT}$$

LFAN CLOCK LOGIC

All true input terms LAT 101 I thru LAT 104 I are latched into the 4 stage LFAN (5) as shown in Figure 2-9, by FOINL. The LFAN clock is enabled by the following conditions:

1. Section Select switch S26 true.
2. Inverter (3) term 1/0 F0/ false.
3. A one clock QTINL pulse has been generated by the Initialize pushbutton logic.

LFAN clock buffer equation is:

$$\text{FOINL} = 1/0 \text{ F0/} * \text{QTINL} * \text{F0} \dots \dots 0$$

DISCONNECT LATCH LOGIC

The 4 stage LFAN (5) is permanently wired in the D-set mode as shown in Figure 2-9. True input terms LAT 101 I thru LAT 104 I are latched into the LFAN by clock pulse FOINL. The corresponding true LFAN outputs are inverted (6) to disable the output buffers (7). Therefore the word generator stage output is logically disconnected from the card connector pins OAY thru' ODY by the output buffers (7).

Word generator function, feedback and card pin display gating logic is not effected by the disconnect logic.

Do below

Functional Detail

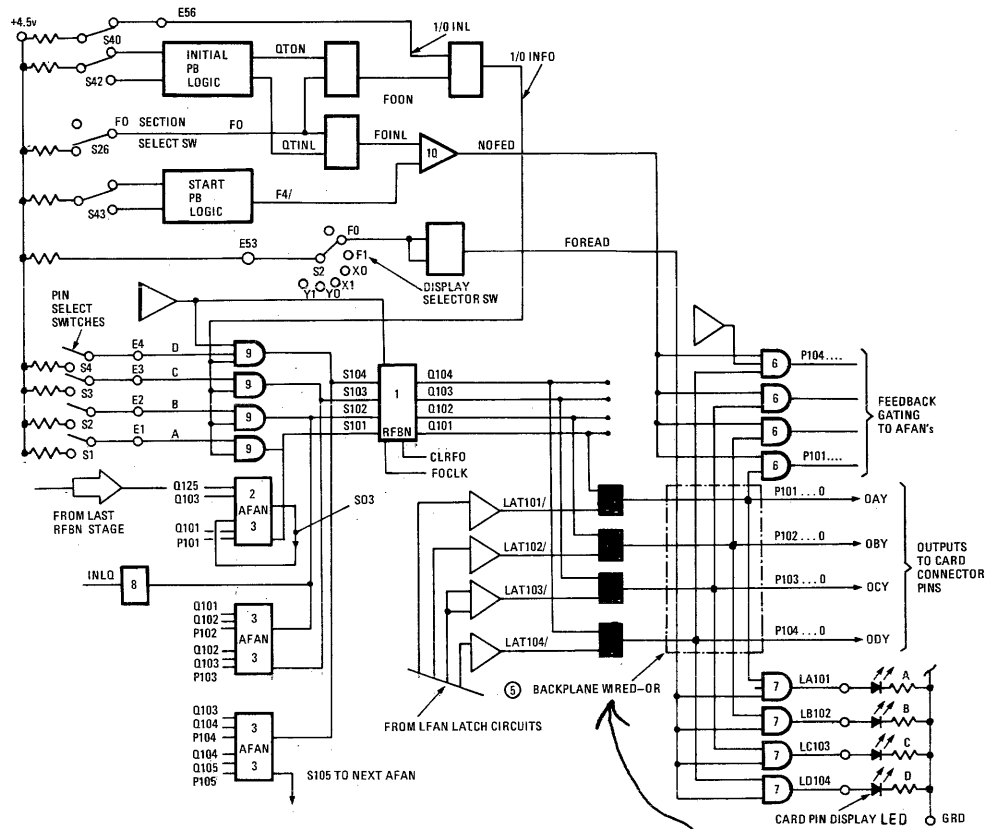


Figure 2-8. Sum/Shift/Display Logic

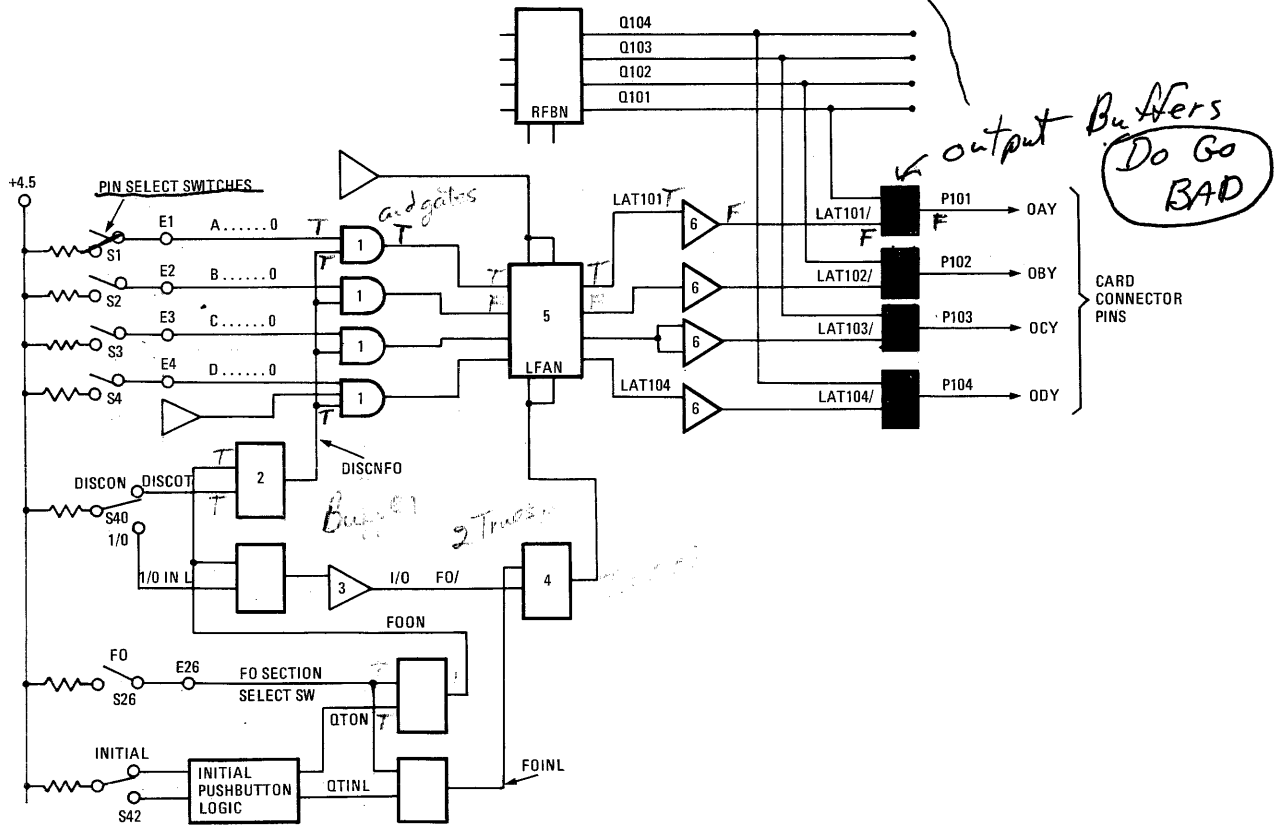


Figure 2-9. Disconnect Logic

Functional Detail

PIN DISCONNECT PROCEDURE

The procedure to disconnect a pin or a group of pins is as follows:

1. 1/0 switch positioned to DISCONNECT.
 2. Select the designated section select switches UP.
 3. Select the designated Pin Select switch UP.
- All switches must be up together.
4. Press the Initialize pushbutton.

During this operation any pin select switch(es) in the down or off position will connect the word generated stage output to the card pins.

PIN SELECT PROCEDURE

For static chip testing, a true level may be applied to a logic chip using the chip clip accessory. The chip clip is plugged into either F0 or F1 frontplane connector. The procedure for applying a true level is as follows:

1. Select the Section Select switch UP.
2. Select the required Pin Select switch UP.
3. Press the Initialize pushbutton.

START PUSHBUTTON LOGIC

The start pushbutton and associated logic is shown in Figure 2-10, and logic elements are numbered and referenced to the text for explanation purposes.

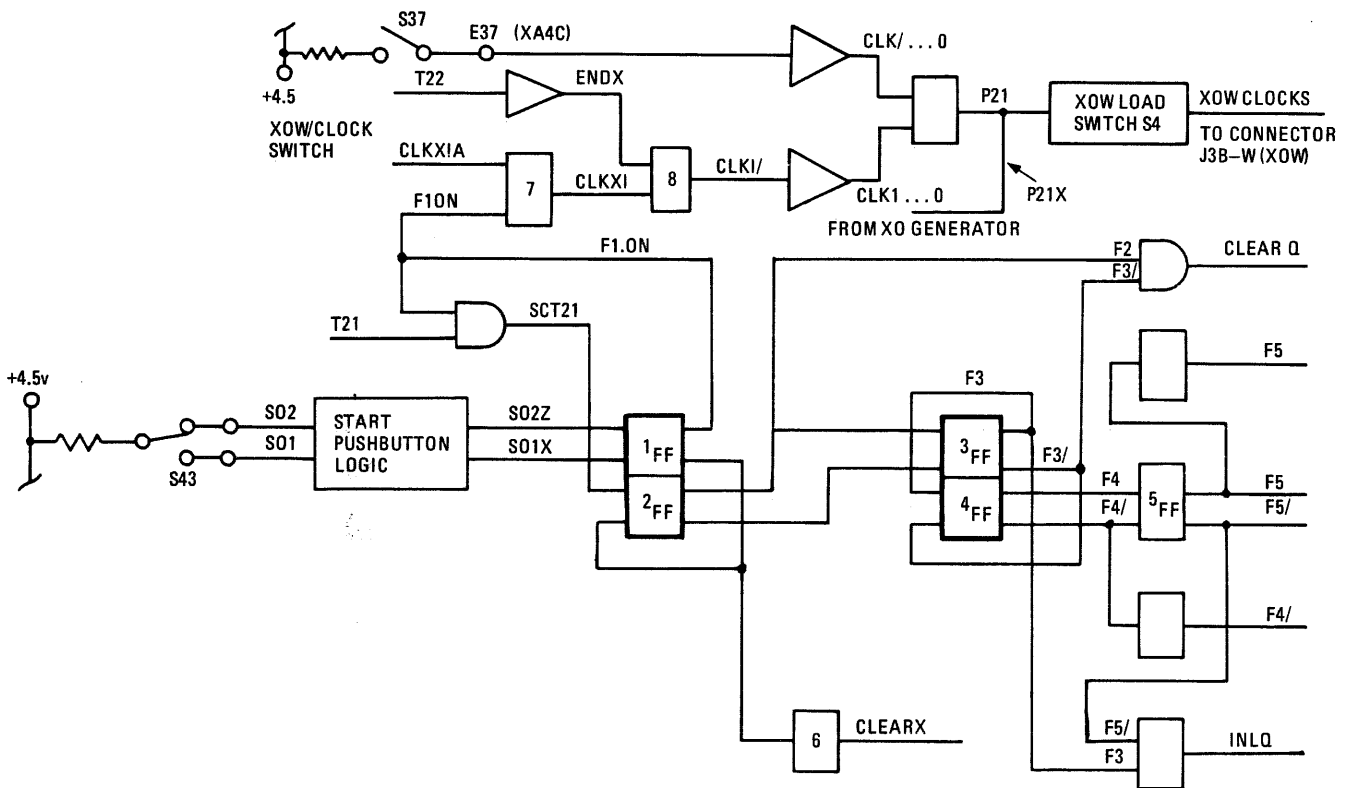


Figure 2-10. START Pushbutton Logic

Functional Detail

A true signal S01X from the start pushbutton logic resets flip flop FF1 on the trailing edge of clock S1. In the reset state FF1 provides a true signal CLEAR to clear the pulse and node counters, Signal CLEARX enables the clock pulse logic when switch S37 is in the manual position.

Referring to the start pushbutton timing diagram as shown in Figure 2-11, each clock pulse S2 thru' S5 resets flip flops FF1 thru' FF5 as shown. All flip flops remain reset after clock pulse S5 until the start pushbutton is released.

When the start pushbutton is released, signal S01Z goes true and sets FF1 on clock S9.

With FF1 being set the CLEAR signal goes false (buffer 6) and allows the pulse and node counters to begin counting on each CLK2 clock pulse. Buffer (7) is enabled

by F10N and CLKX1A from the DLCN clock delay element to allow CLK1 . . . 0 clock through to the load switch S4. Test phase signal T22 is false during the start pushbutton sequence and clear phase. Output signal P21 is connected to the XOW load switch S4 to provide the required resistor loading to the XOW clock line.

The CLR tester output jack (J58) as shown on Figure 2-14, is normally jumpered to one of the following reserved card pins; Y0F, Y1F, Y0C and Y1C. Therefore, the card under test will be cleared by the CLR signal and XOW clock pulses. Pulse counter logic sends 1,048,576 clocks during the clear phase to ensure that all card logic elements are reset.

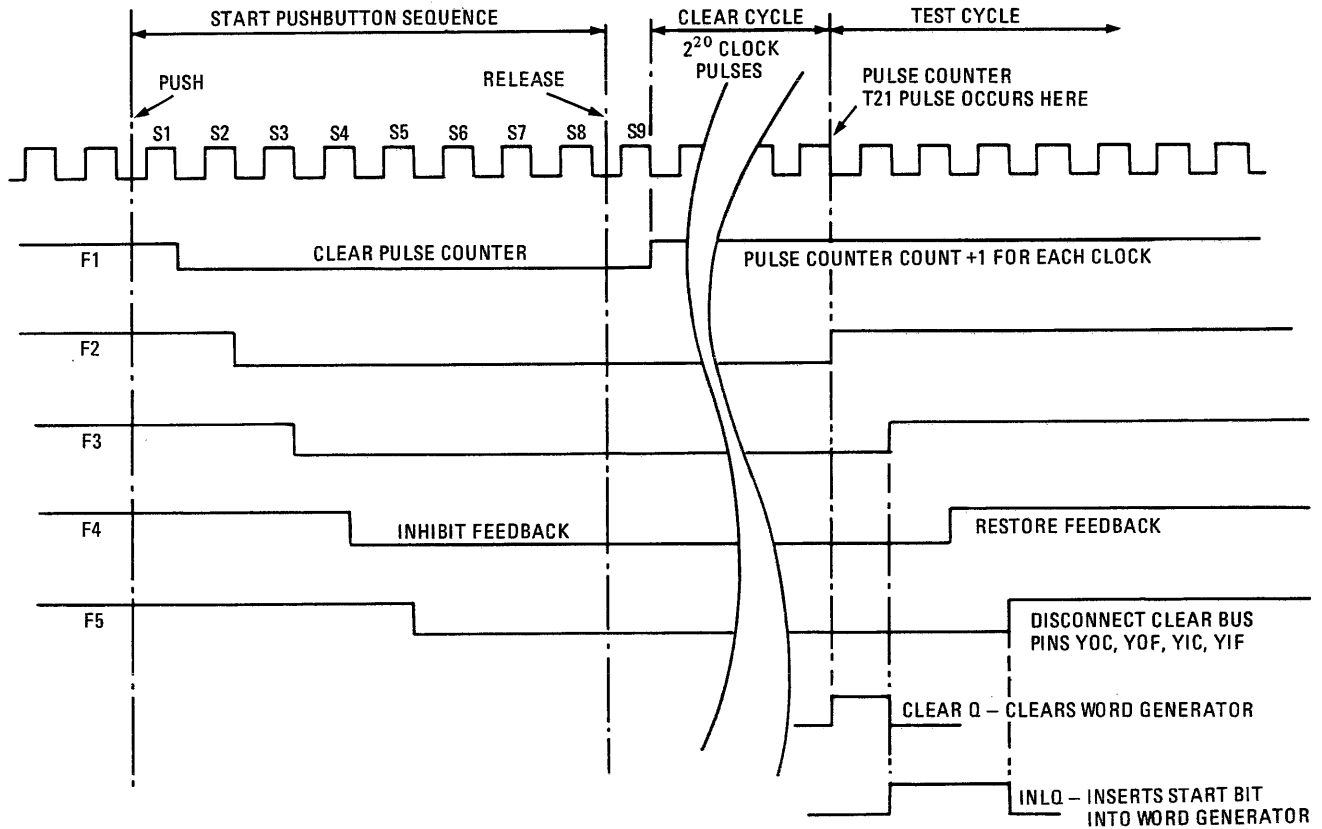


Figure 2-11. START Pushbutton Logic Timing

Functional Detail

INITIAL PUSHBUTTON LOGIC

Figure 2-12 shows the pushbutton logic and its associated timing diagram in Figure 2-13. For explanation purposes Figure 2-12 indicates pushbutton logic connected to the X1 section of the word generator. Similar logic circuitry exists for the other F0, F1, X0, Y0 and Y1 sections as shown on card schematic CL, page 3 of 3.

Two flip flops FF1 and FF2 converts the pushbutton latch output into 4 signals QT1, QT1/, QT2 and QT2/. These signals are connected to buffers 3 thru' 7, to produce the following signals:

1. QTCLK from QT1 * QT2/
2. CLRQT from QT1/ * QT2
3. QTINL from QT1 * QT2/
4. QTON from QT2/

With X1 section selector switch S29 selected, buffers 10, 11, 13 and gate 14 will be enabled to provide the following signals:

1. Generate X1CLK thru buffer 10, to set a RFBN stage. Only the second clock is useful since it must coincide with X1ON to enable the pin select switch input gating.
2. Generate CLRX1 thru buffer 11 to clear the RFBN's in this section.
3. Generate X1INL thru buffer 13 to the LFAN latch clock input.
4. Generate X1ON thru gate 14 to enable pin select input gating to set either the RFBN or LFAN stage.

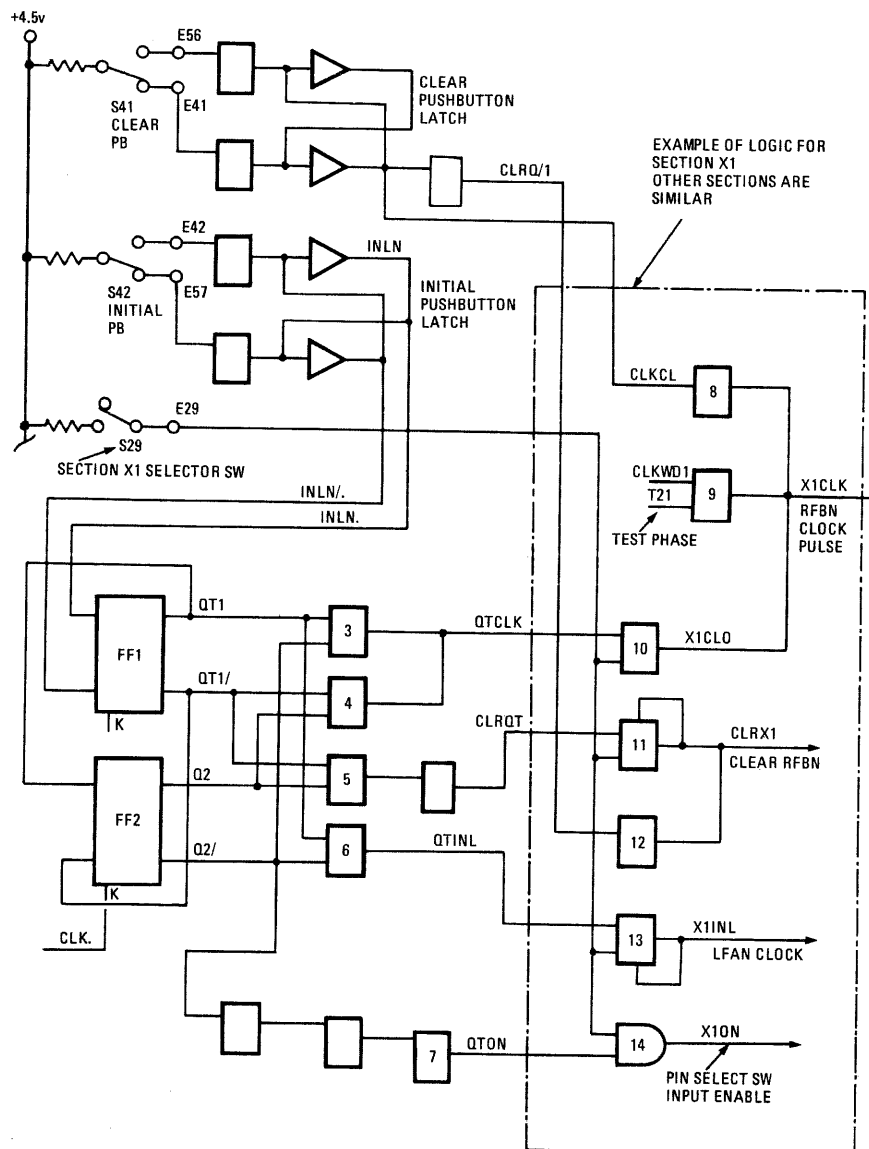


Figure 2-12. INITIAL Pushbutton Logic

Functional Detail

When the clear pushbutton is pressed the following conditions occur:

1. Buffer 8 provides a continuous true level to X1CLK
2. Buffer 12 provides a continuous true level to CLRX1 to clear all RFBN's of the word generator.

WORD SECTION GENERATOR

The complete 138 stage word generator is logically divided into 5 sections, as shown in Figure 2-14, and each section is referred to as X0, X1, Y0, F0 and F1. Logic for these 5 section generators are distributed over 6 logic cards at locations X0, X1, Y0, Y1, F0 and F1. Logic on card Y1 is shared by 3 section generators at X0, X1 and Y0.

The number of stages in each section is as follows:

1. X0 has 31 stages P1 thru' P31.
2. X1 has 29 stages P32 thru' P60.
3. Y0 has 28 stages P61 thru' P88.
4. F0 and F1 have 28 stages.

Each stage of F0 and F1 begins with P101 thru' to P125. No stages exist from P89 thru' to P100.

WORD GENERATOR BLOCK DIAGRAM

Figure 2-15 shows an example of F0 section

generator, which shows logic signal distribution, return loop logic and exclusive-or gate AFAN element. For simplicity only 4 stages of this section generator have been shown.

PULSE COUNTER PROBE LOGIC

The COUNTCTO input to the 4 RFAN node counter is derived from the load switch (S3) and PCP input (J7). Figure 2-16, shows the PCP logic, S3 and J7 and associated logic.

With S3 in the CTL position, CNTC/T.0 is connected to +4.5v. Any logic pulse to PCP (J7) makes COUNTCTO true to enable buffer 1. Alternatively when S3 is in the D/TTL position, the CNTC/T.0 term effectively goes false and all PCP logic pulses are connected to IHCN chip (2).

The DTL hex inverter chip IHCN (2) is a diode transistor inverter and will invert any COUNTT.0 signal. Inverter (3) will invert again and restore COUNTT.0 to allow COUNTC to switch true.

The timing diagram as shown in Figure 2-17, illustrates the result of load switch (S3) on the node counter +1 signal COUNTC. Refer to the Card Tester Timing diagram for the relationship between PCP logic pulses and the node counter clock pulses (CLK2).

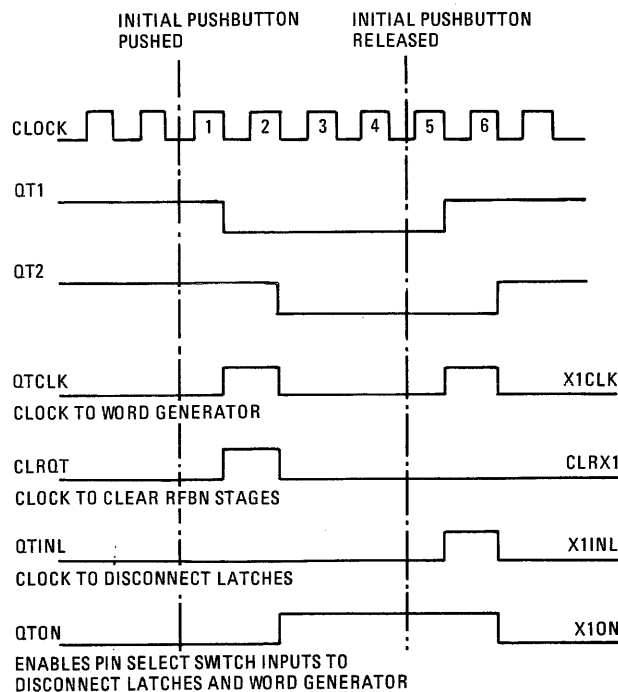


Figure 2-13. INITIAL Pushbutton Timing Diagram

Functional Detail

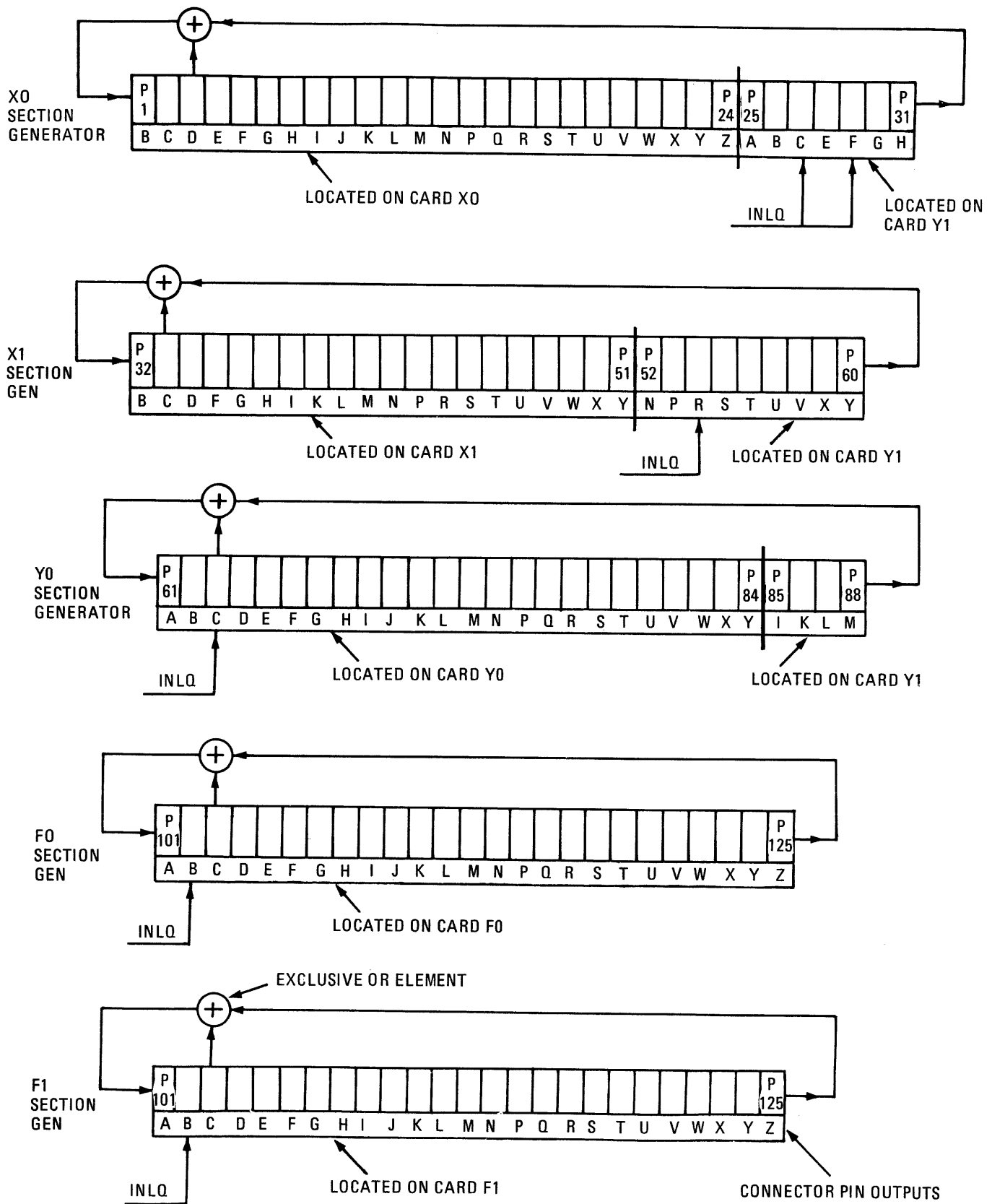


Figure 2-14. Word Generator Sections

Functional Detail

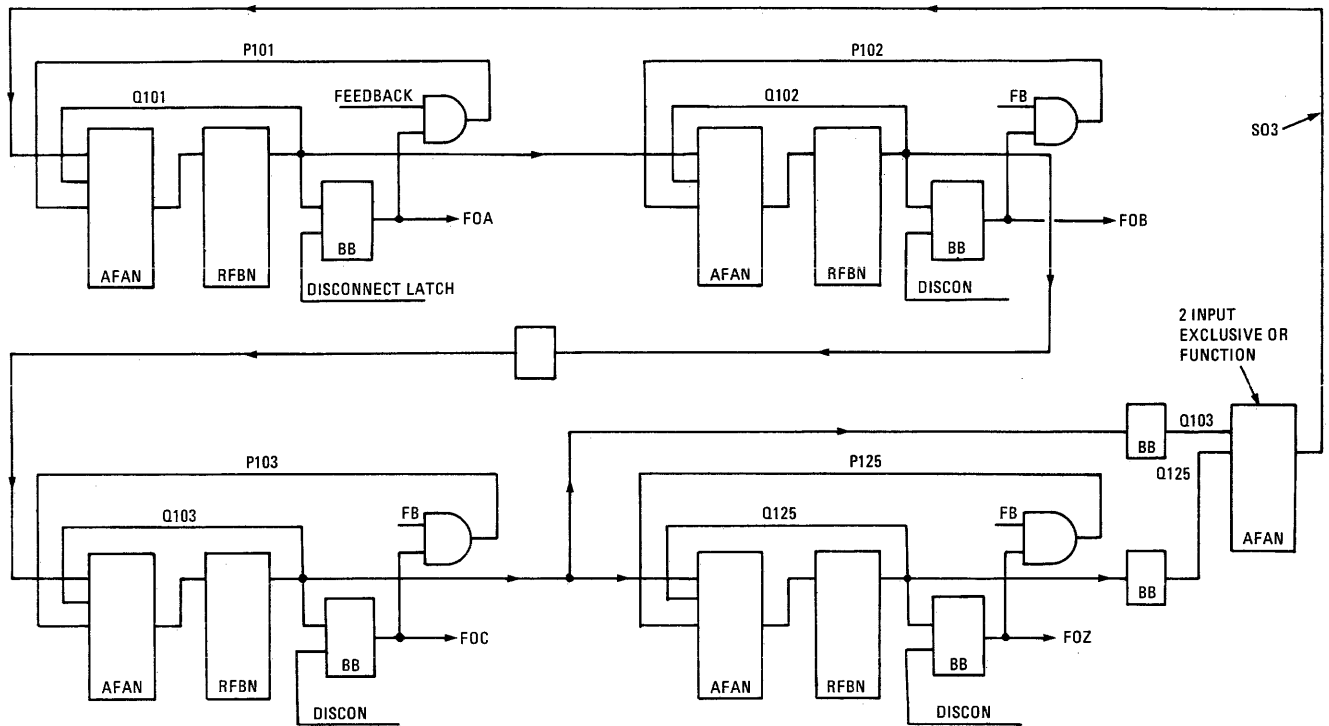


Figure 2-15. FO Word Generator Block Diagram

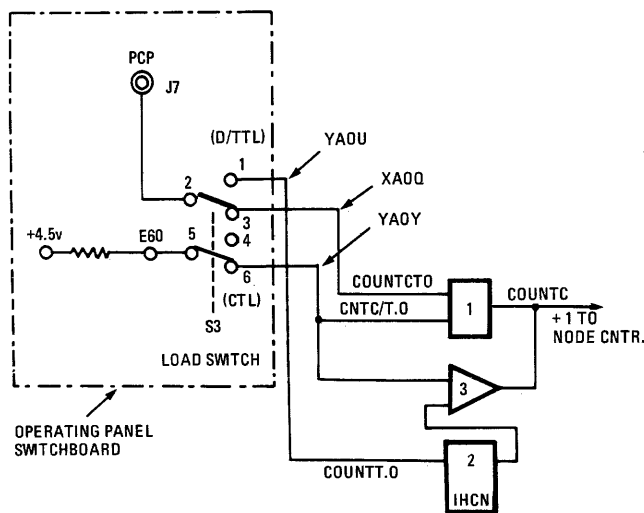


Figure 2-16. Pulse Counter Probe Logic

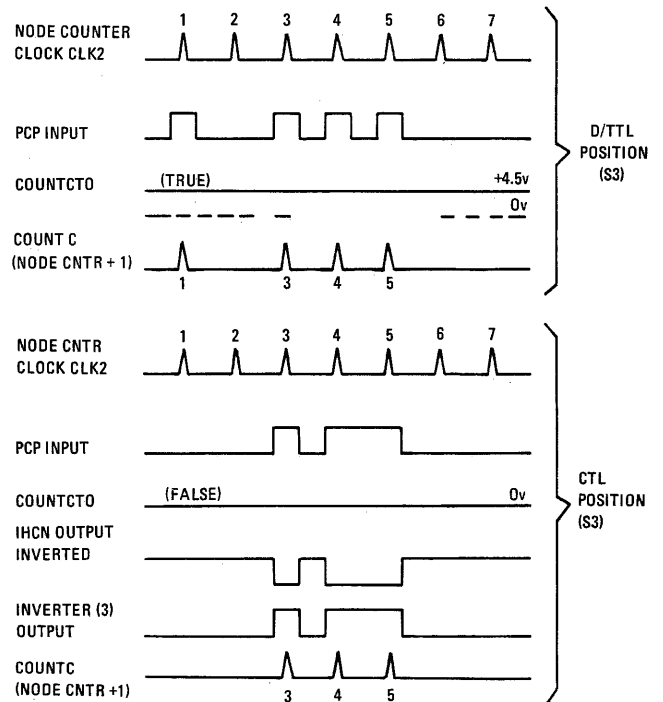


Figure 2-17. PCP Logic Timing Diagram

Functional Detail

NODE COUNTER LOGIC

This counter as shown in Figure 2-18, is composed of 4 RFAN's, connected in series and permanently set in the shift up mode. Input from the PCP logic is connected to the lower RFAN input. Twelve RFAN outputs, termed COUNT 1 thru' 12 are connected to the lamp board terminals E1 thru' 12 as shown.

thru' E12 as shown.

The node counter is cleared by CLRNDCT during 6 start pushbutton sequence clocks S1 thru' S6. The counter remains reset until the Test Phase begins as signalled by T21 and will count +1 whenever the PCP input term COUNTC is true at CLK2 time.

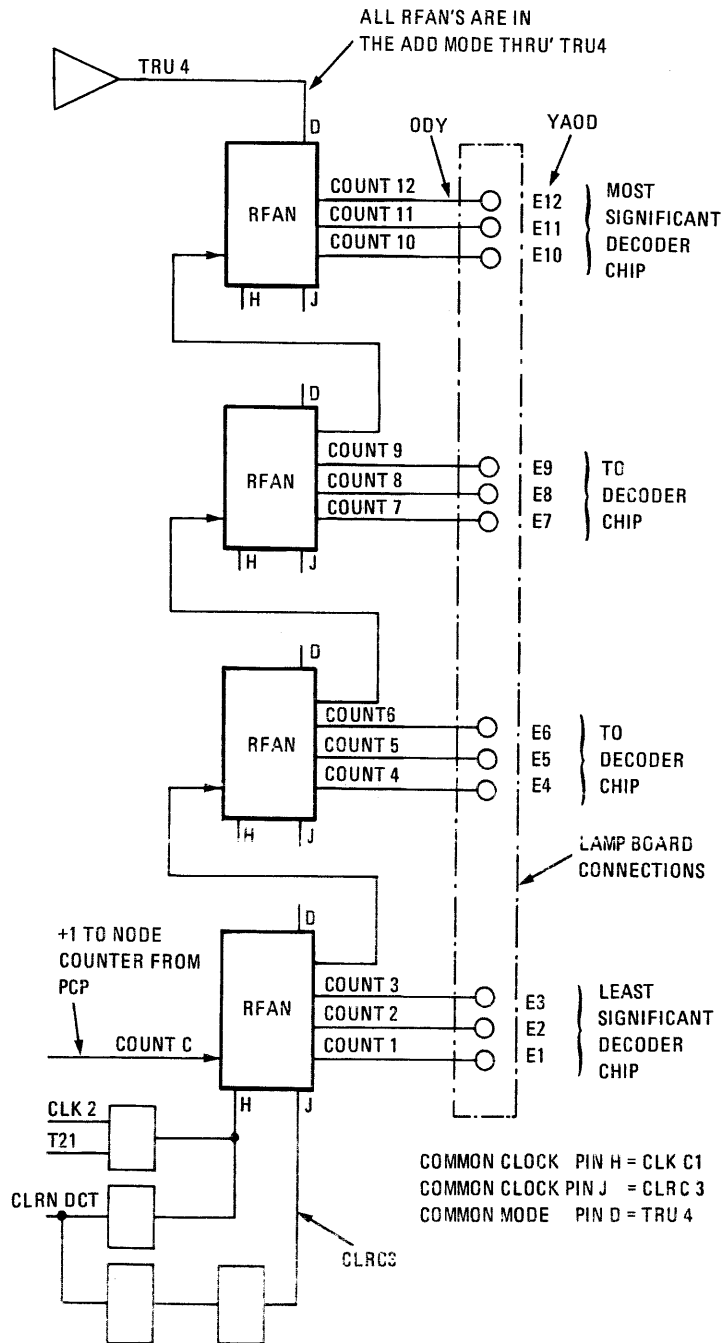


Figure 2-18. Node Counter Logic.

Functional Detail

PULSE COUNTER LOGIC

Eight RFAN's as shown in Figure 2-19, are serially connected and logically forced into the add mode. The function of the pulse counter is to determine precisely the duration of both Clear and Test phases by counting the number of clock pulses CLK2. Ten RFAN outputs T1 thru T10 are buffered and connected to Tester Output jacks T1 thru T10 on the operating panel. Two more tester outputs are generated by the pulse counter logic. Output signal 1IN32KO from RFAN 5 is buffered and connected to S7. Whilst the combined logic outputs of T21/ * T22/ from RFAN's 7 and 8 are buffered and connected to the CLR tester output jack (J58).

For convenience the 8 RFAN binary count output sequence is also shown in Figure 2-19. This shows

8 x 4 = 32 stages of the RFAN node counter. Cross latched stages represent outputs not used or as carry outputs to the next stage.

PULSE COUNTER DECODER LOGIC

A DFBN decoder chip as shown in Figure 2-20, accepts 4 bit BCD 8421 input codes and produces appropriate outputs to drive a seven segment LED matrix display.

Input BCD codes are applied to the DFBN chip address lines A0 thru A3. Outputs for the LED display segment selection ZA thru' ZG are activated as shown in the following truth table, Figure 2-21.

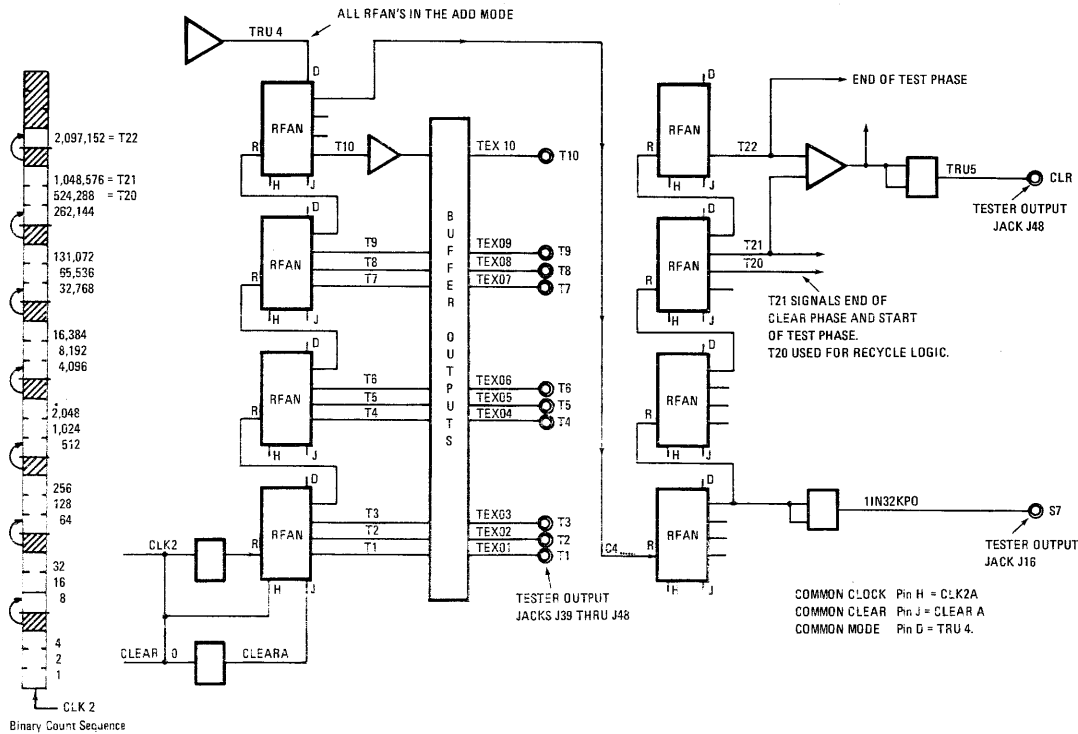


Figure 2-19. Pulse Counter Logic

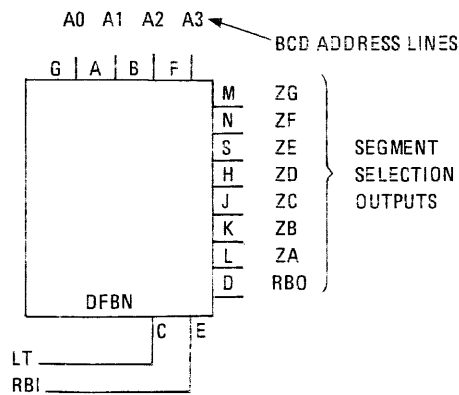


Figure 2-20. Seven Segment Decoder

LT	RBI	INPUTS				OUTPUTS							No.	
		A3	A2	A1	A0	ZA	ZB	ZC	ZD	ZE	ZF	ZG		RBO
1	1	0	0	0	0	1	1	1	1	1	1	0	1	0
1	X	0	0	0	1	0	1	1	0	0	0	0	1	1
1	X	0	0	1	0	1	1	0	1	1	0	1	1	2
1	X	0	0	1	1	1	1	1	1	0	0	1	1	3
1	X	0	1	0	0	0	1	1	0	0	1	1	1	4
1	X	0	1	0	1	1	0	1	1	0	1	1	1	5
1	X	0	1	1	0	1	0	1	1	1	1	1	1	6
1	X	0	1	1	1	1	1	1	0	0	0	0	1	7

Figure 2-21. DFBN Truth Table.

Functional Detail

As shown in Figure 2-22, the decoder inputs are connected to the following lampboard pins E1 thru E3.

1. Node Counter output signals COUNT 1 thru COUNT 12 as shown by E1 = YA1T = 1TY = COUNT 1.
2. To input pins of the Card Pin Section display LED's at pins EFG, HKL, MNR and STU. These 12 pins are used to sample the complete card pin section signature and generate the partial 4 digit octal signature.

NUMERIC DISPLAY LOGIC

The pulse counter is composed of 4 numeric display elements. Each display element has 7 bar lines activated by the decoder outputs ZA thru ZG, as shown in Figure 2-23. Corresponding display chip leg numbers are shown in brackets ().

Figure 2-24, shows the plan pin view of a numeric display element with the marker positioned on the right hand side.

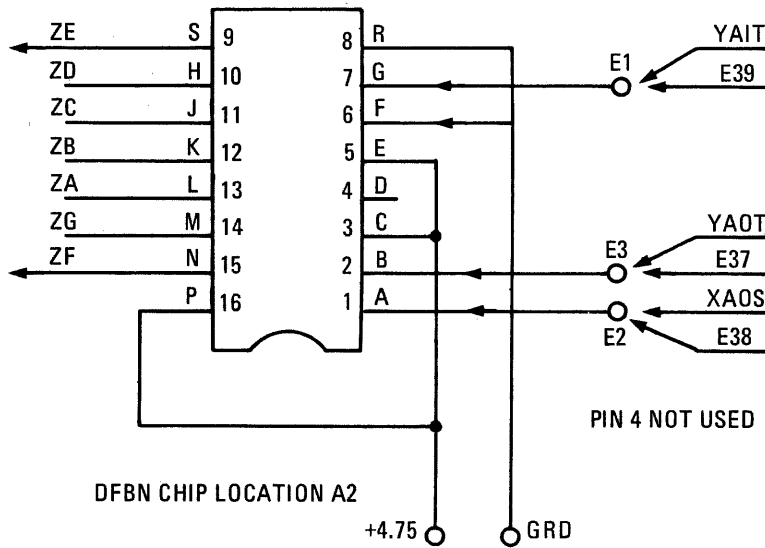


Figure 2-22. Decoder Input/Outputs.

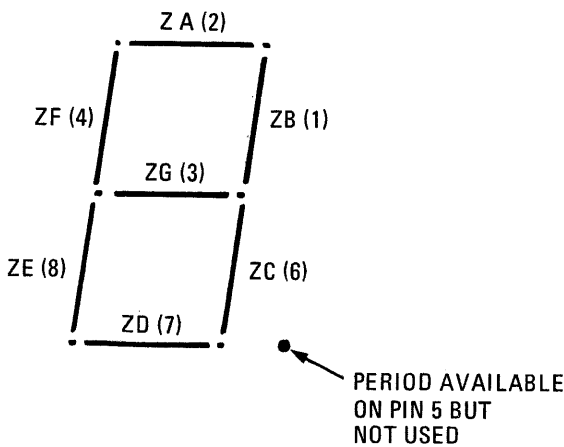


Figure 2-23. LED Display Bar Layout.

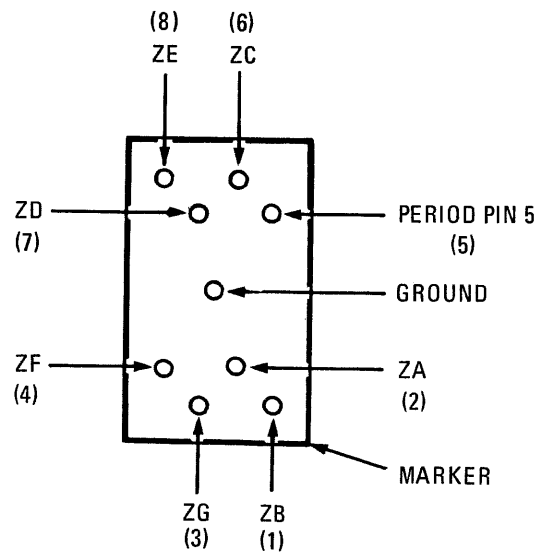


Figure 2-24. Display Element Pin Layout

Functional Detail

INTERLOCK RELAY ± 12

The purpose of the interlock relay K1 as shown in Figure 2-25, is to prevent ± 12 volts being accidentally applied to logic cards when the ± 12 switches are selected incorrectly. Early FCT models were not fitted with a 12 volt interlock relay K1, and it was possible to apply ± 12 volts before card insertion and therefore damage the logic elements. The introduction of a relay and another procedural step into the FCT operating instructions acts as a safeguard and a warning to the F.E.

Relay K1 circuit earth return is obtained from the common earth lines provided by a logic card when inserted into the backplane.

To energise relay K1, insert the card and operate the reset switch S6. The hold-on contacts 5 and 9 keeps relay K1 picked. The required ± 12 volts may be selected as instructed by the Card Test Data documentation. However, relay K1 remains picked through the hold-on contacts and card earth, until the card is removed from the backplane connector. Both ± 12v LED's will illuminate when selected by S44/S45 and independant of relay K1 condition. As shown in Figure 2-25, with S44/S45 off and K1 not picked the following backplane pins are connected to:

1. Y1L Y1L jack J32 YB4L logic.
2. Y1A Y1A jack J28 YB4A logic.
3. X1Z XA21 logic.

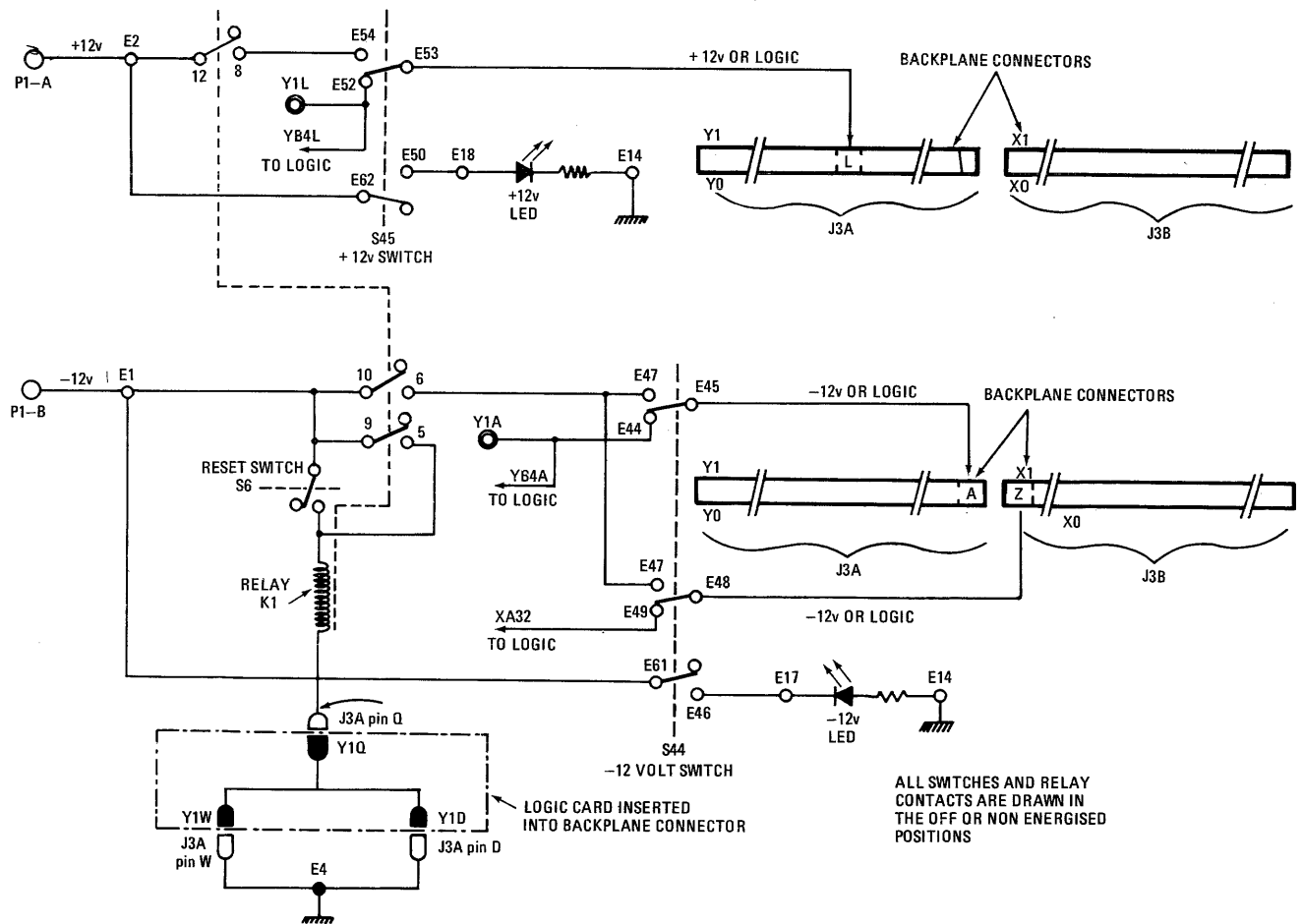


Figure 2-25. ± 12 Volt Interlock Relay

Functional Detail

RECYCLE LOGIC

The purpose of this logic as shown in Figure 2-26 and Figure 2-27, is to automatically simulate a manual clear-start pushbutton sequence. Recycle logic allows continuous Clear-Test cycles to occur for easier node counting. Node counter values are displayed for approximately 1 second during the clear phase of the following Clear-Test cycle.

With S5 selected to RECYCLE, the signal FRERUN will be true. Both RFBN's 2 and 3 are reset so SHIFT/ is also true. Pulse counter output T22, which signals end of

test, enables gate 1. Output from gate 1 sets both RFBN's 2 and 3 into the D-set mode and sets the lower stage of RFBN 1 true. Outputs from both RFBN's are connected together to produce the start pushbutton signal S02X and set the RFBN mode lines into the shift up mode. Successive clock pulses moves the start bit thru' the RFBN's in the shift up mode, as shown in Figure 2-27. Both RFBN's reset as the start bit moves out of the last stage. The pulse counter term T20 enables gate 4 to clear the node counter in preparation for the 1 second node count display during the next clear phase.

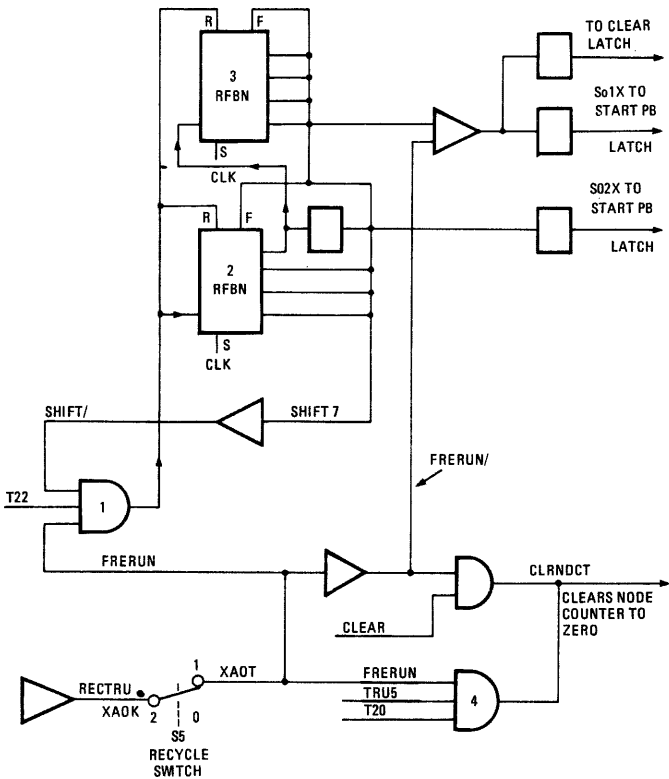


Figure 2-26. Recycle Logic

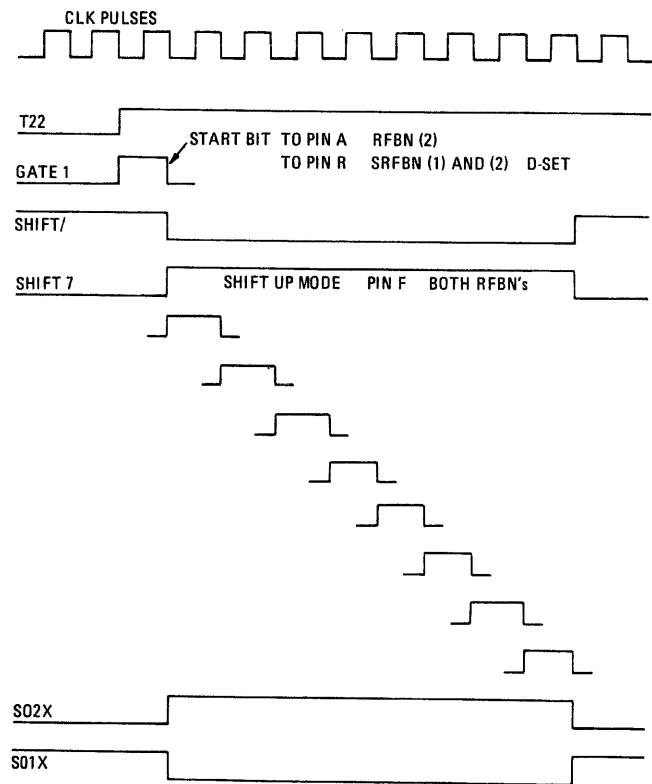


Figure 2-27. Recycle Logic Timing Diagram

Functional Detail

BACKPLANE PIN LOCATION

Schematic logic signals are related to backplane pins by means of a pin identification code. Backplane pins, as illustrated in Figure 2-28, indicates the co-ordinates for identifying any backplane pin. Details of the co-ordinates are as follows:

1. Card section X or Y.
2. Card zone A, B or C.
3. Card Row 0 thru' 7 except 2, 5 and 8.
4. Card pin A thru' Z except O.

Two examples from the operating panel schematic (also shown in Figure 3-6), illustrates the pin identification code.

Initial Pushbutton.

Switch S42 YA1V where Y = Section Y
 A = Zone A
 1 = Row 1.
 V = Pin V.

Schematic term = 1VY

Logic schematic CL, page 3 of 3 shows the input term 1VY to the pushbutton latch.

Selector Switch XO

Switch S29 XA1L where X = Section X
 A = Zone A.
 1 = Row 1.
 L = Pin L.

Schematic term = 1LX

Similarly the input term 1LX is shown on CL schematic page 3 of 3.

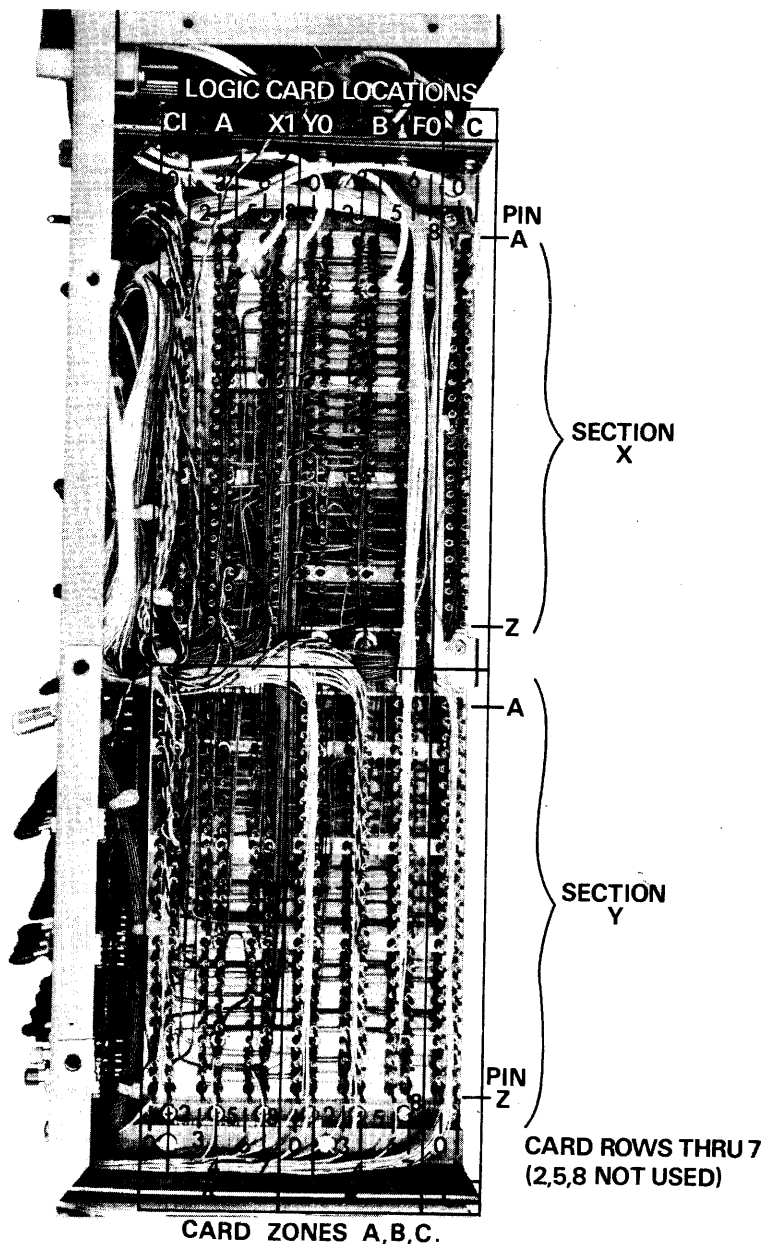


Figure 2-28. Backplane Pin Co-Ordinates.

SECTION 3

CIRCUIT DETAIL

CARD TESTER SCHEMATIC

This schematic shows the logic backplane connections between the following FCT sub-assemblies:

1. Frontplane Connectors
2. Backplane Connectors
3. Tester Output Jacks
4. Card Pin Jacks
5. Lamp Display Board
6. Switch Board
7. Logic voltage distribution and $\pm 12v$ interlock relay.

The card tester schematic E-22072250 is included in the Test and Field document package for the FCT and

is not shown in this manual. However, a brief explanation of each sub-assembly is given and the related diagrams may be cross referenced to schematic E-22072250.

FRONTPLANE CONNECTORS

Two 50 pin connectors J1 and J2 corresponding to frontplane connectors F1 and F0 respectively are shown in Figure 3-1. All signal lines are marked A thru Z (except 0) and each signal line has one adjacent ground line. All ground lines are strapped to terminal E4, whilst all signal line connections to the FCT logic backplane are identified by a 4 digit alpha-numeric code as shown in Section 2, Figure 2-28.

Example:

J2 pin A \rightarrow YB6A \rightarrow OAY (F0).

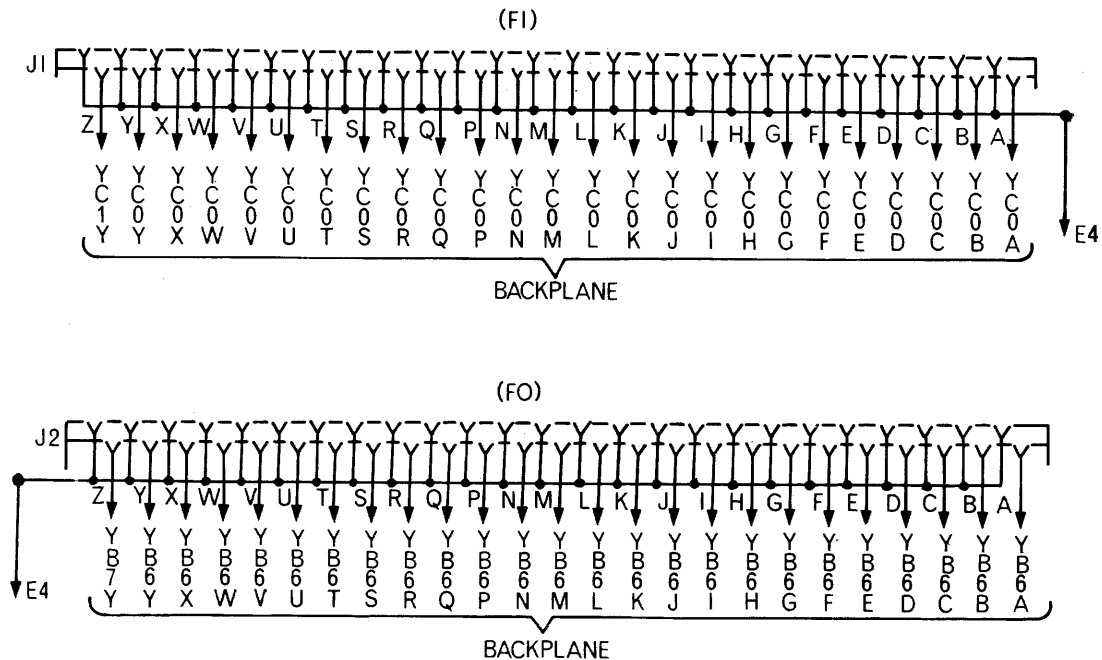


Figure 3-1. Frontplane Connectors

Circuit Detail

BACKPLANE CONNECTORS

Two 50 pin card connectors J3A and J3B are shown in Figure 3-2. Various logic signals are distributed from these connectors to one of the following destinations:

1. Direct connection to backplane
 i.e. Y1Y → YB4Y → YB1Y
 YB1Y → 1YY CARD Y1 → P60
2. Connection to backplane via the Tester Output Jack.
 i.e. Y1C → J29 → Y1C – Tester Output.
 J29 → YB4C → YB1C
 YB1C → 1CY – CARD Y1
3. Switched connection by switches S44 and S45 and 12 volt relay K1, between logic and ± 12 volts.

i.e. Y1L → E53 → S45 (off)

S45 off → E52 → YB4L (logic).

Alternatively:

Y1L → E53 → S45 (on)

S45 (on) → E54 → K1-8 (+12v).

4. Logic voltage +4.75v to J3B-Y0A/Y1A.
5. Logic voltage -2.00v to J3A-Y0Z/Y1Z
6. Clock signal X0W load switch S4, providing 3 switched clock load positions of zero, 12 and 18.
 i.e. X0W → S4-3 → XA4X (No load).
 X0W → XA4X → -2v x R2 (12 loads).
 X0W → XA4X → +4.75v x R1 (18 loads).
7. Common ground connections E4.

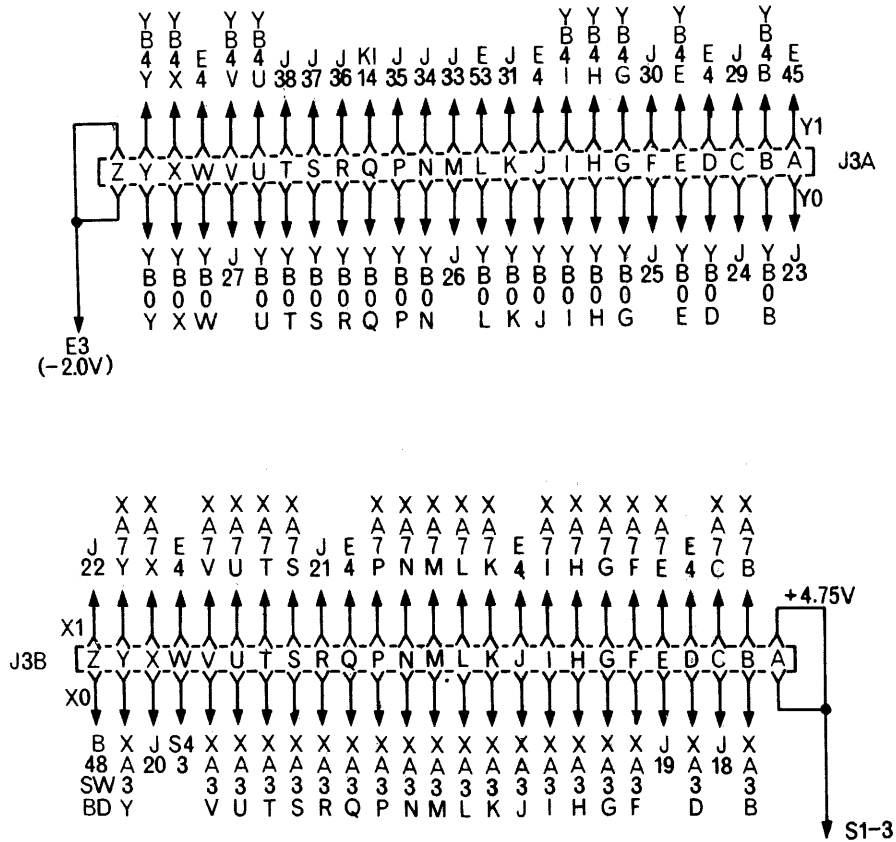


Figure 3-2. Backplane Connectors.

Circuit Detail

TESTER OUTPUT JACKS

Special output signals are generated by FCT logic and distributed by the tester output jacks as shown in Figure 3-3. Tester outputs are generated from:

1. Pulse counter logic.
2. Special clocks signals C0, CM and ERLY 20/40.
3. True signals TR1 thru TR3 and CLR.
i.e. TR (J55) → XA0N → ONX (Clock card).
ONX → TR1 Chip A3 CL 2 of 3.

CARD PIN JACKS

Card pin jacks are connected to selected pins of the two backplane connectors J3A and J3B, as shown in Figure 3-4. These 3 way signal junctions indicate:

1. Operating panel signal names,
i.e. J18 → X0C.
2. Connection to card backplane pins,
i.e. J18 → X0C (J3B).
3. Connection to FCT backplane logic,
i.e. J18 → XB3C.

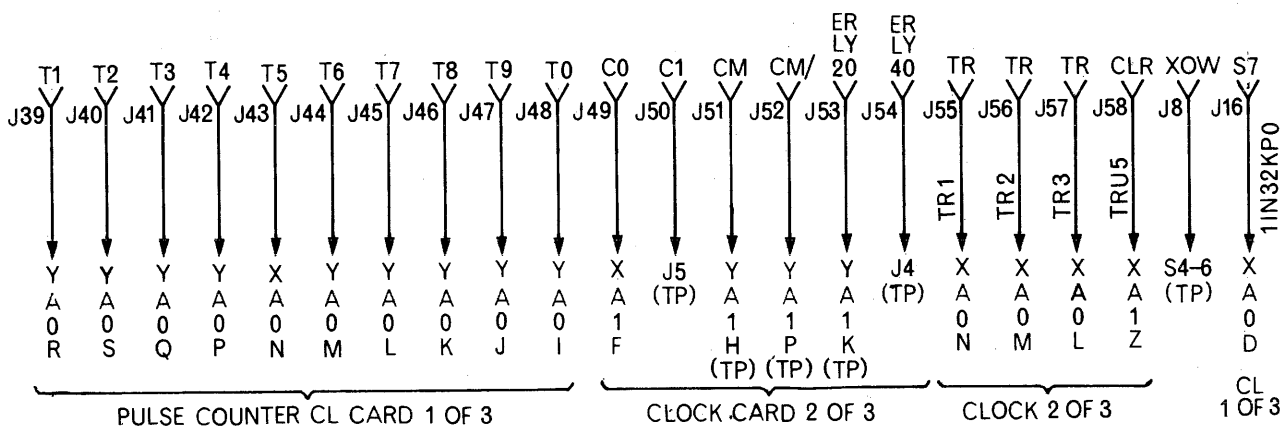


Figure 3-3. Tester Output Jacks.

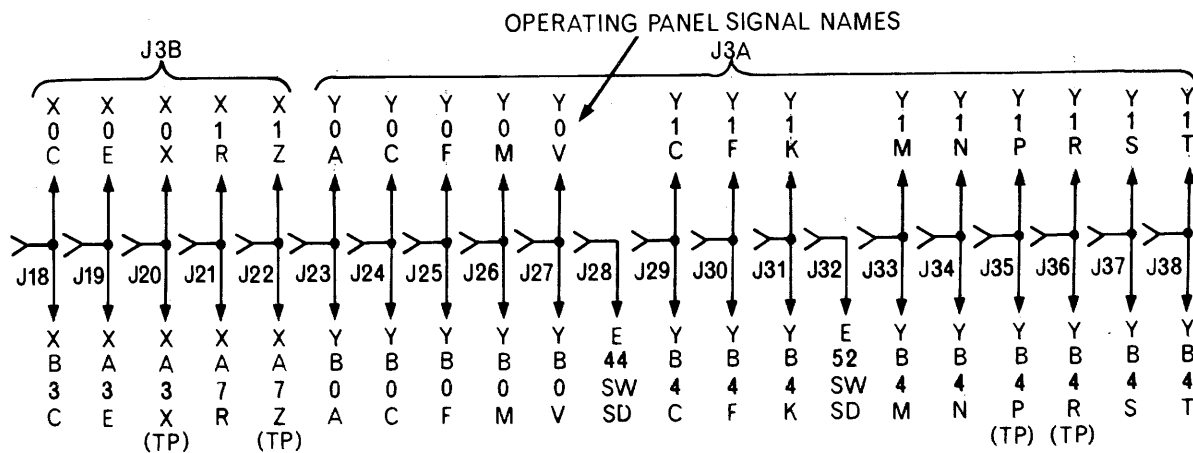


Figure 3-4. Card Pin Jacks

Circuit Detail

LAMP DISPLAY BOARD

Figure 3-5 shows a lamp display schematic that includes the following display logic:

1. Pin Display LED's (A thru Z), used to display the complete card signature.
2. Pulse Counter Decoder Chips (A2, A4, A7, A9).
3. Pulse Counter Display Element (A1, A3, A6, A8), used to display the partial card signature.
4. Pulse Counter Load Resistor Chips (A5, A10).

The component layout of a lamp display board is shown in Figure 5-8.

Decoder chip inputs E1 thru E12, are connected to the following points:

1. FCT backplane,
 - i.e. LT46 → 1TY (X1-2 of 2) → YA1T
 - YA1T → E1 → decoder A2.
2. Selected card pin display LED's (*)
 - i.e. LE105 (F0 - 1 of 2) → 0EX → XC0E
 - XC0E → E39 → E pin display LED
 - E39 → E1 → decoder A2.

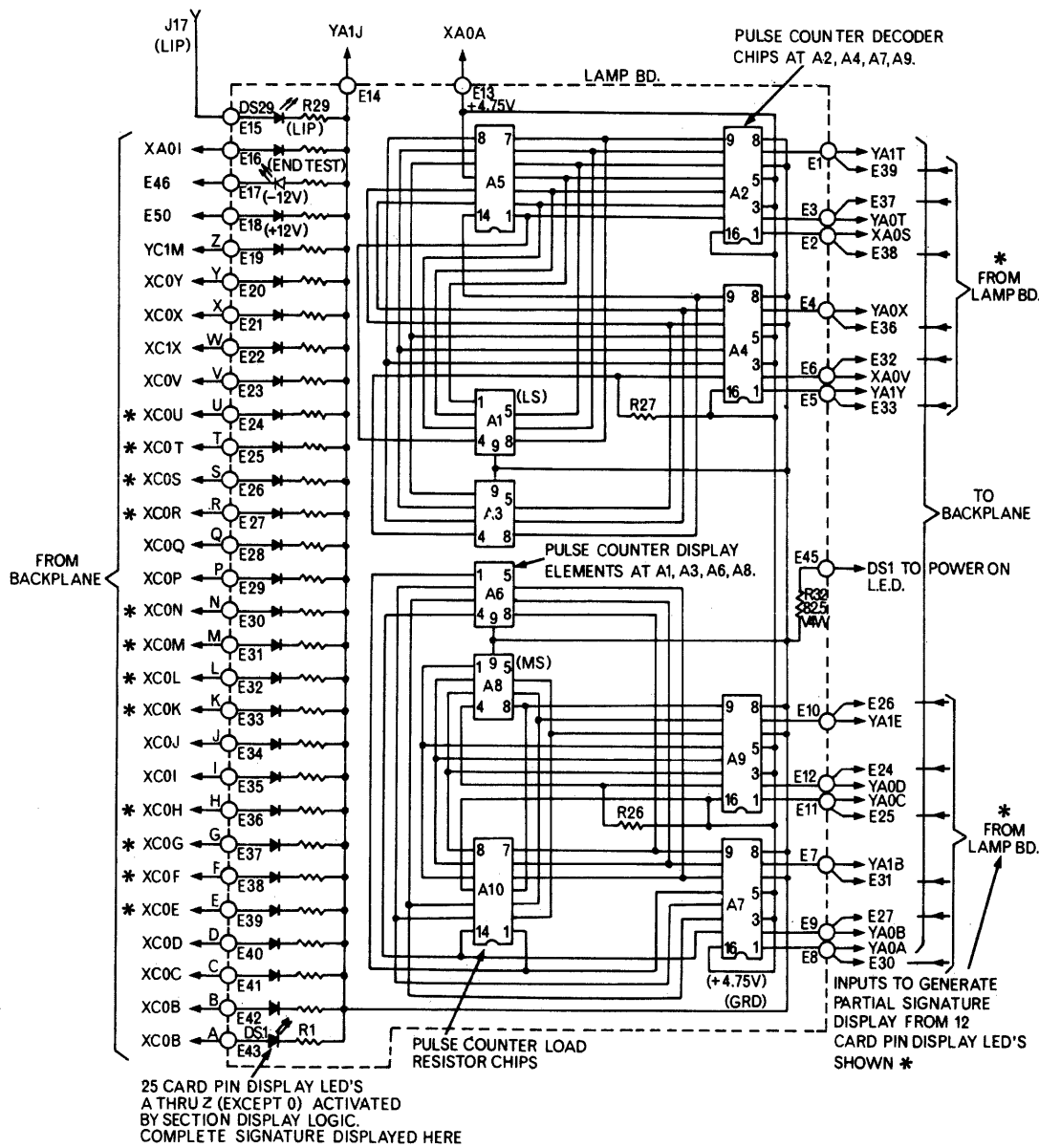


Figure 3-5. Lamp Display Board.

Circuit Detail

SWITCH BOARD

Figure 3-6 shows a switch board schematic and indicates the majority of operating panel switches. These switches distribute +4.75 volts to various backplane pins with destinations shown by the 4 digit alpha numeric code. The switch board component layout is shown in Figure 5-9

Clear Bus Switch Y0C (S32).

i.e. +4.75v → E32 → YB1K

YB1K → 1KY (Y0-1 of 2) → Y0CCON.0

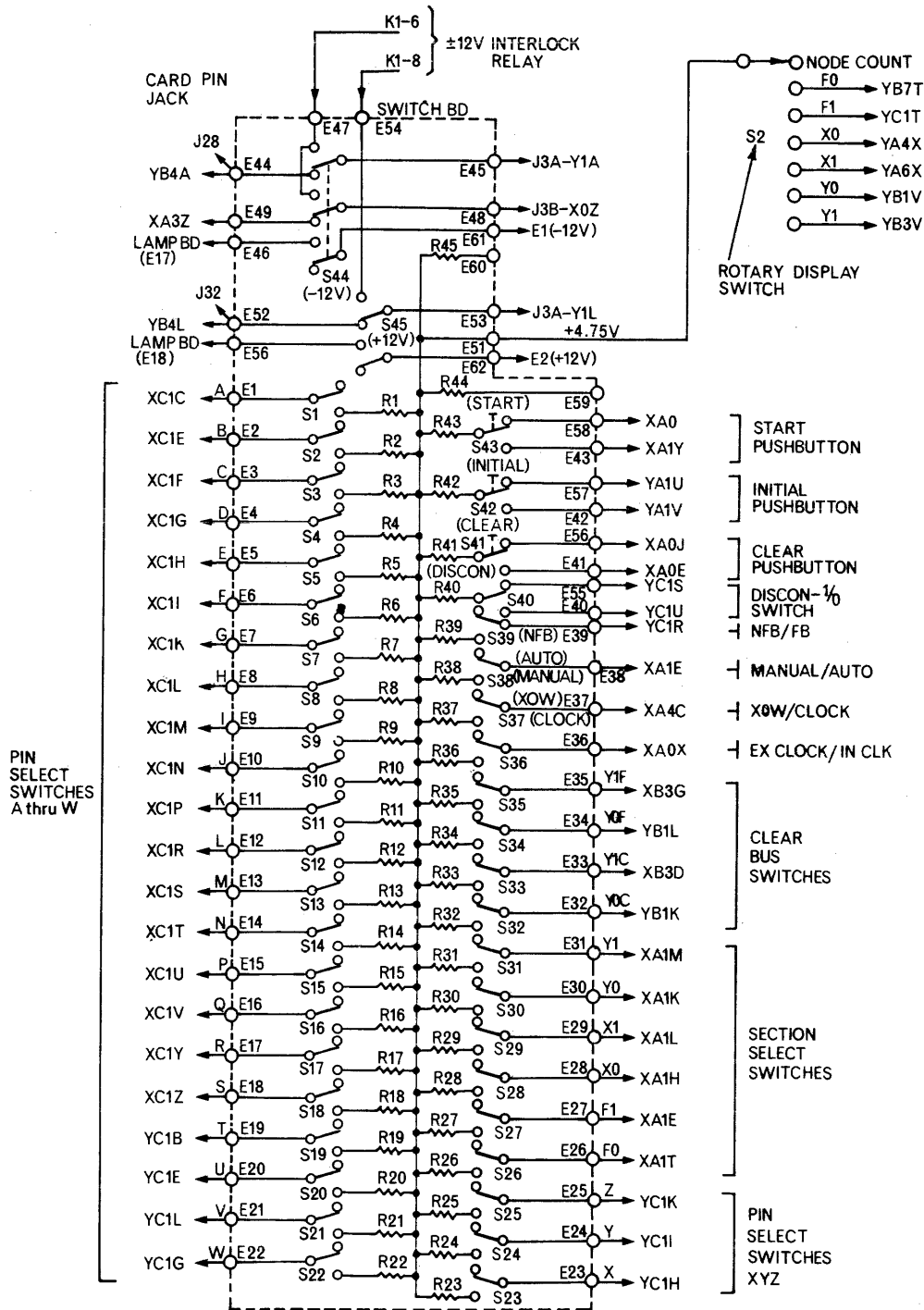


Figure 3-6. Switch Board

Circuit Detail

LOGIC VOLTAGE DISTRIBUTION

Field Card Tester

Distribution of logic voltages within the FCT is shown in Figure 3-7, which indicates:

1. Backplane voltage distribution.
2. Main input voltages and connector plug P1.
3. Capacitor board.
4. 12 volt interlock relay K1.
5. Fan motor.

The CR network strapped across S1 on the capacitor board eliminates inductance and prevents the system circuit breakers from tripping when S1 is actuated. The capacitor board and 12 volt relay mounting are shown in the electronic assembly, Figure 5-7.

TEST FIELD DOCUMENTS

The T and F document package supplied with the FCT comprises the following:

1. Logic Card Schematics.
2. Etched card artwork schematics. These schematics show the arrangement of etching for both solder and component sides.

3. Logic card signals and corresponding chip locations, sorted on logic name. The following elements indicate:
 - a. XXXX = Input or output pin.
 - b. XXXR = Load resistor.
 - c. XXXM = -2 volts.
 - d. XXXG = Logic ground.
 - e. XXXP = +4.75 volts.

4. Backplane name ordered circuit list. This shows logic signal names, backplane pin locations and wire wrap levels.

i.e. CLK . . . 0 = XA0B 2 () 2 XA4B

① ② ③ ④

- where
- ① indicates logic signal name
 - ② indicates backplane pin location with the FC prefix removed.
 - ③ indicates the wire wrap level and may be level 1 or 2.
 - ④ indicates wire pivot point.

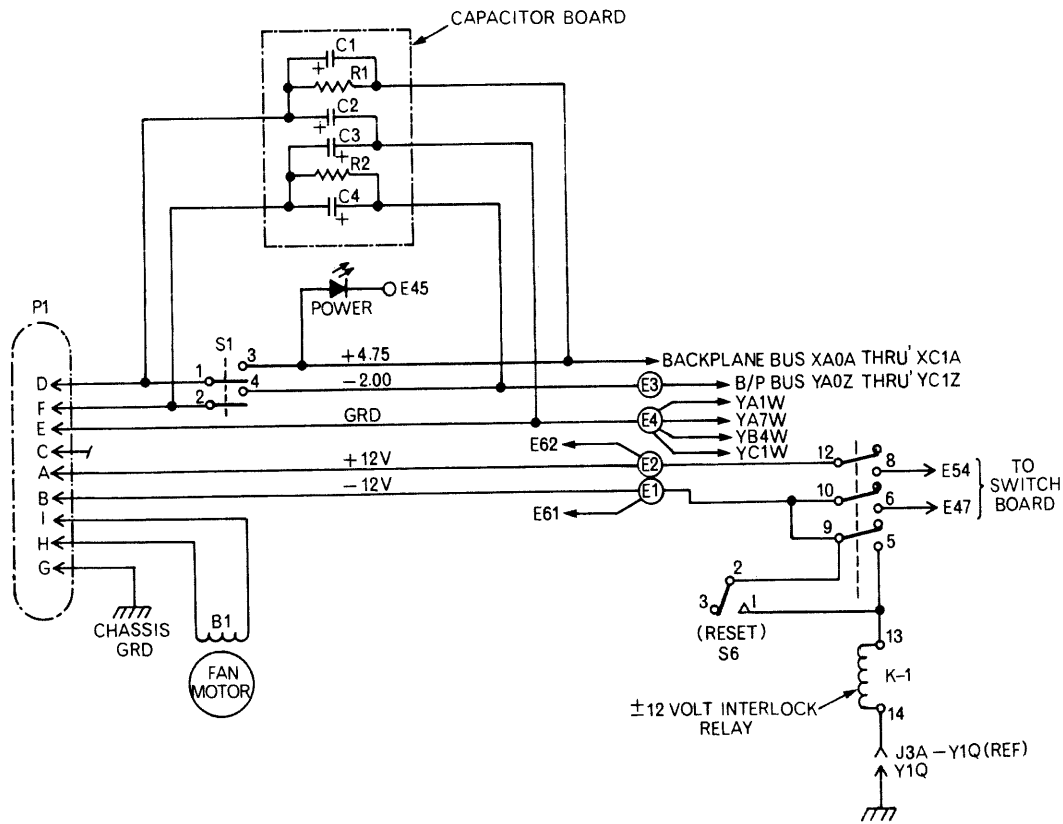


Figure 3-7. Logic Voltage Distribution.

SECTION 5

MAINTENANCE PROCEDURES

GENERAL

This section includes the following

1. Trouble shooting guide.
2. Component location and access instructions for:
 - a. Chassis.
 - b. Lamp Board.
 - c. Switch Board.
3. Component Parts list.

since it is composed of B1700 logic with no moving parts except for the cooling fan and switches.

But the following periodic checks are recommended:

COOLING FAN

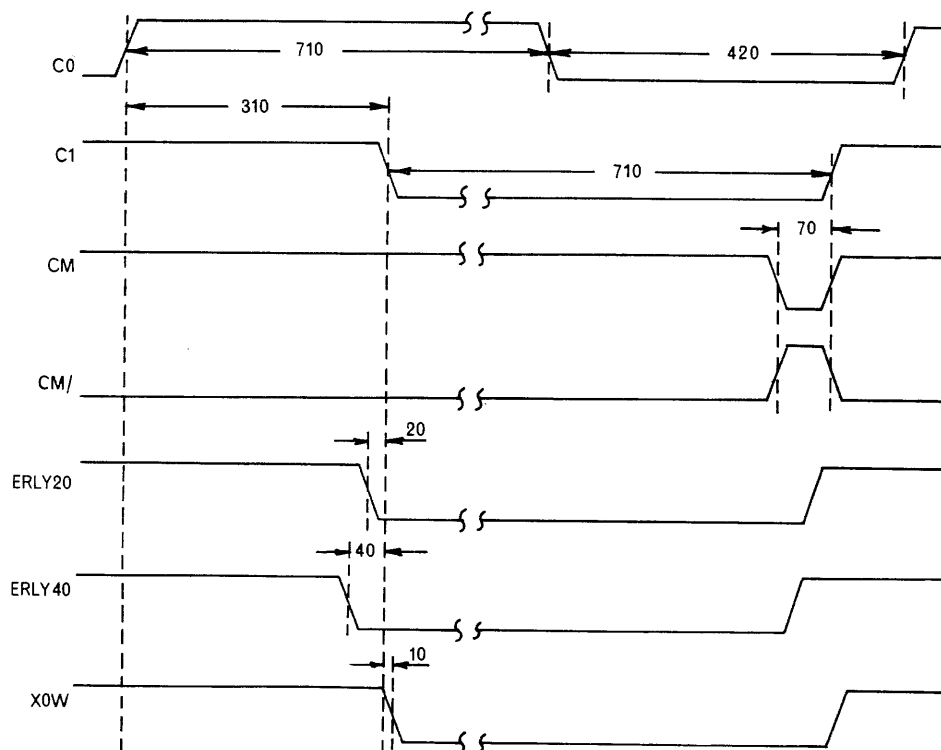
Check fan motor rotates freely without binding. Remove any paper debris etc. which would restrict air flow through the fan grill.

INTERNAL CLOCK FREQUENCY

Extend clock card (CL) on a standard B1700 logic card extender. Check clock waveform and frequency CLK.0 to that shown in Figure 5-1. Adjust potentiometer L6 on etched CL card or potentiometer K6 on wire wrap CL card.

MAINTENANCE GUIDE

The FCT will operate with a minimum of maintenance



ALL MEASUREMENTS IN NANoseconds
RISE & FALL TIMES ARE EXAGGERATED TO DEFINE MEASUREMENT POINTS

Figure 5-1. F.C.T. Clock Waveforms

Maintenance ProceduresTROUBLE SHOOTING GUIDE

The FE is recommended to follow the comprehensive trouble shooting guide as shown in the operation and test section of the Test and Field documents (T and F). Information contained in this section simply supplements the T and F guide.

GENERAL

The FCT logic cards develop signatures and node counts with the exception of the clock card (CL), in the same manner as B1700 system logic cards. Therefore logic faults on cards F0, F1, X0, X1, Y0 and Y1 can be diagnosed using another operational FCT.

However the FE can diagnose FCT logic faults without the aid of another FCT by correct interpretation and reference to the following:

1. T and F trouble shooting guide.
2. Knowledge of FCT theory of operation.
3. Switch panel tests.
4. Self check signatures and node counts.
5. Single shot clock modification.

CLOCK CARD WAVEFORMS

Check all waveforms as indicated in Figure 5-1. Only the CLK.0 signal is adjustable, and the remaining signals are delayed by standard B1700 DLCN delay elements on the CL card.

PULSE COUNTER TEST

Good signatures also depend upon a precise and repeatable number of clocks being applied to the card under test. Therefore, check the pulse counter waveforms and pulse duration by observing the tester outputs TEX01 thru' TEX10 at jacks J39 thru' J48, or at the backplane.

Figure 5-2, shows typical pulse counter waveforms and pulse widths. The frequency of T1 should be approximately 450 KHZ. Check that T2 frequency is exactly half that of T1. Check T1 thru T10, observing the frequency is divided by 2 at each successive test jack. Initialize the FCT and press start each time or alternatively select recycle in order to observe waveforms.

NODE COUNTER TEST

Accurate node counts depend upon the RFAN node counter adding up correctly. Therefore check the pulse widths of COUNT 1 thru COUNT 12 signals at the backplane. Typical node counter pulse widths and backplane pin locations are shown in Figure 5-3.

Initialize the FCT and press start each time or alternatively select recycle in order to observe waveforms.

SELF CHECK SIGNATURE

Execute a normal clear, initialize, start pushbutton sequence with no feedback, NFB and without a card inserted. Verify all self check signatures for word generator sections F0 thru Y1 correspond to correct values shown in the T and F operational and test section. An incorrect signature with NFB identifies the failing section of the word generator.

Repeat the clear, initialize and start sequence with feedback FB and again verify signatures against expected values shown in the T and F operational and test section.

Section Y1 of the word generator is shared by X0, X1 and Y0 sections. The logic relationship between section Y1 and the other sections is shown in Section 2, Figure 2-14 of this manual. The clock card CL also contains clear, clock and initial logic unique to each section. For example, the X0 section on the CL card is as follows:

- | | |
|-----------|-----------|
| 1. X0 CLK | 3. X0.INL |
| 2. CLR X0 | 4. X0 ON |

Therefore due to the relationship of the Y1 and CL card incorrect signatures will be developed over sections of the word generator. Figure 5-4 shows the relationship between incorrect signatures and faulty logic cards.

DISCONNECT LOGIC TEST

This simple switch panel test procedure checks the disconnect latch logic. A disconnect latch when set, effectively isolates the word generator output at the output buffer stage. Proceed as follows:

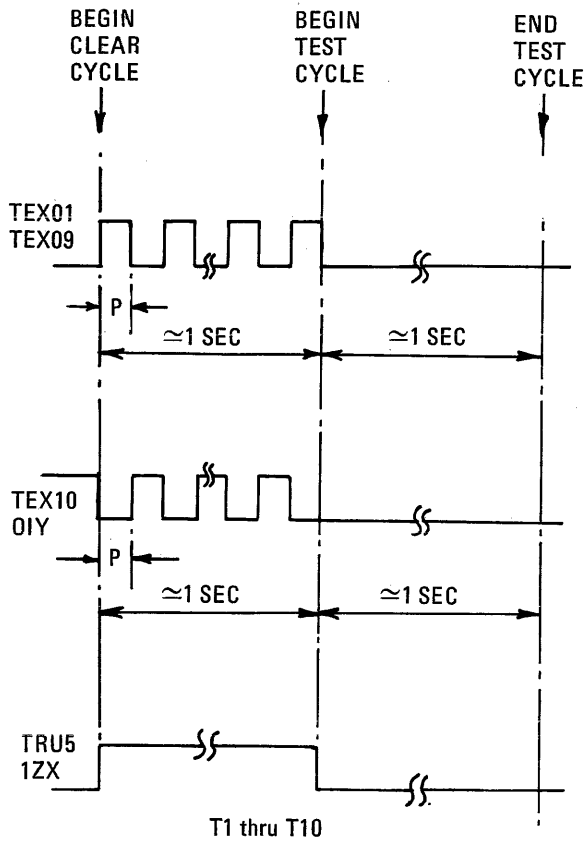
1. Set switch S40 to DISCONNECT
2. Set all pin select switches A thru Z down in the zero (0) position.
3. Set all section select switches F0 thru Y1 up in the set position.
4. Press INITIAL pushbutton, which generates one LFAN clock pulse to set the LFAN's.
5. Verify that all pulse counter signatures read 0000.
6. Verify that all card pin LED's are extinguished.

PIN SELECT LOGIC TEST

This procedure checks that all stages of the word generator can be set from the switch panel. The procedure is as follows:

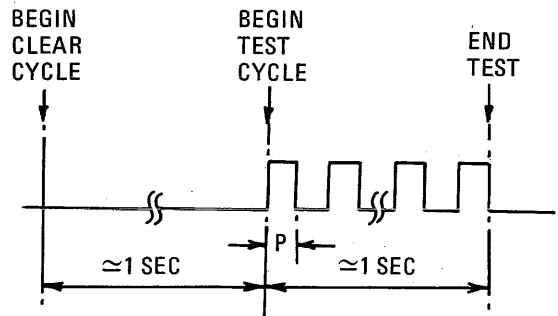
1. Set switch S40 to 1/0 position.
2. Set all pin select switches A thru Z up in the one (1) position.

Maintenance Procedures



Signal	Count	Pulse Period (P)
ORY	TEX01..0	1.1 μSec
OSY	TEX02..0	2.2 μSec
QQY	TEX03..0	4.4 μSec
OPY	TEX04..0	8.8 μSec
ONY	TEX05..0	18.0 μSec
OMY	TEX06..0	36 μSec
OLY	TEX07..0	72 μSec
OKY	TEX08..0	144 μSec
OJY	TEX09..0	288 μSec
OLY	TEX10..0	576 μSec

Figure 5-2. Pulse Counter Signals



Signal	Count	Pulse Period (P)
1TY	COUNT 1.0	1.1 μSec
0SX	COUNT 2.0	2.2 μSec
QTY	COUNT 3.0	4.4 μSec
0XY	COUNT 4.0	8.8 μSec
1YY	COUNT 5.0	18 μSec
OVX	COUNT 6.0	36 μSec
1BY	COUNT 7.0	72 μSec
0AY	COUNT 8.0	144 μSec
0BY	COUNT 9.0	288 μSec
1EY	COUNT 10.0	576 μSec
0CY	COUNT 11.0	1152 μSec
0DY	COUNT 12.0	2304 μSec

Figure 5-3. Node Counter Signals

		FAULTY LOGIC CARD						
		F0	F1	X0	X1	Y0	Y1	CL
INCORRECT SIGNATURE	F0	X						X
	F1		X					X
	X0			X			X	X
	X1				X		X	X
	Y0					X	X	X
	Y1						X	X

Figure 5-4. Relation Between Logic Card and Signature.

Maintenance Procedures

3. Set all section select switches F0 thru Y1 up in the set position.
4. Press INITIAL pushbutton to generate one RFBN clock pulse to set the RFBN stages of the word generator.
5. Verify the following pulse counter display values and corresponding card pin display signatures, as follows:

F0= 7777 display A thru' Z
 F1= 7777 display A thru' Z
 X0= 7777 display all except A
 X1= 7777 display all except ADJQW
 Y0= 7777 display all except Z.
 Y1= 7777 display all except DJQWZ

Twelve display lamps are not illuminated in this test because the corresponding output from the word generator stage are not connected to these lamps.

Also note that during this test procedure, 2 separate logical sequences occur as follows:

1. Set the corresponding RFBN stage via the switch panel.
2. Resets any disconnect LFAN latch condition set by a previous disconnect operation.

PULSE COUNTER TEST

This test procedure progressively checks all octal values and positions of the pulse counter. This is particularly useful when checking the octal decoder chip logic.

An incorrect pulse counter signature may occur even though the card under test and word generator logic are functioning correctly. Proceed as follows:

1. Set switch S40 to 1/0 position.
2. Set rotary switch S2 to F0 position.
3. Set section select switch F0 up
4. Set the required pin select switch (es) E thru U up and press the INITIAL pushbutton to generate the corresponding octal values as indicated as follows:

Check Units

Pin E = 0001
 F = 0002
 EF = 0003
 G = 0004
 GE = 0005
 GF = 0006
 GEF = 0007

Check Ten's

Pin H = 0010
 K = 0020
 HK = 0030
 L = 0040
 LH = 0050
 KL = 0060
 HKL = 0070

Check Hundred's

Pin M = 0100
 N = 0200
 MN = 0300
 R = 0400
 MR = 0500
 NR = 0600
 MNR = 0700

Check Thousand's

Pin S = 1000
 T = 2000
 ST = 3000
 U = 4000
 SU = 5000
 TU = 6000
 STU = 7000

SELF CHECK NODE COUNTS

With the FCT self check test feature and a correctly functioning pulse counter, it is possible to self check the backplane and frontplane pins.

Operating Procedure

1. Initialize the FCT.
2. Set switch S39 to NFB.
3. Set switch S5 to RECYCLE.
4. Check node counts and LED display for all backplane and frontplane pins.

Maintenance Procedures

Backplane Section X0

A	0 0 0 0	-
B	0 3 6 0	K L M N
C	0 1 5 4	G H L M
D	7 4 4 7	E F G L R S T U
E	7 3 4 0	L M N S T U
F	7 1 0 6	F G M S T U
G	1 1 1 6	F G H M S
H	6 5 1 3	E F H M R T U
I	1 3 3 4	G H K M N S
J	7 7 5 2	F H L M N R S T U
K	5 7 2 6	F G K M N R S U
L	6 1 5 3	E F H L M T U
M	6 1 1 0	H M T U
N	7 1 4 2	F L M S T U
P	6 7 5 2	F H L M N R T U
Q	0 0 5 3	E F H L
R	0 5 3 4	G H K M R
S	0 4 3 6	F G H K R
T	7 7 0 4	G M N R S T U
U	7 4 6 7	E F G K L R S T U
V	1 0 0 0	S
W	0 0 0 0	-
X	1 0 1 2	F H S
Y	7 5 3 7	E F G H K M R S T U
Z	6 4 0 4	G R T U

Backplane Section Y0

A	6 6 5 6	F G H L N R T U
B	0 6 6 4	G K L N R
C	6 2 1 1	E H N T U
D	2 0 2 5	E G K T
E	5 6 5 0	H L N R S U
F	7 0 5 1	E H L S T U
G	6 0 7 7	E F G H K L T U
H	0 4 3 1	E H K R
I	5 4 5 5	E G H L R S U
J	0 1 5 7	E F G H L M
K	1 3 3 5	E G H K M N S
L	0 1 5 1	E H L M
M	7 5 5 1	E H L M R S T U
N	6 4 0 1	E R T U
P	0 7 1 5	E G H M N R
Q	7 4 0 5	E G R S T U
R	7 7 6 6	F G K L M N R S T U
S	0 6 7 1	E H K L N R
T	7 2 6 5	E G K L N S T U
U	0 6 2 6	F G K N R
V	0 2 1 3	E F H N
W	0 4 2 4	G K R
X	0 6 3 3	E F H K N R
Y	6 6 3 6	F G H K N R T U
Z	0 0 0 0	-

Backplane Section X1

A	0 0 0 0	-
B	1 5 0 4	G M R S
C	7 5 6 6	F G K L M R S T U
D	0 0 0 0	-
E	0 3 4 7	E F G L M N
F	0 2 3 5	E G H K N
G	1 7 3 6	F G H K M N R S
H	0 5 4 4	G L M R
I	0 4 2 3	E F K R
J	0 0 0 0	-
K	6 5 2 0	K M R T U
L	0 4 0 1	E R
M	0 7 3 1	E H K M N R
N	0 0 0 6	F G
P	1 6 3 7	E F G H K N R S
Q	0 0 0 0	-
R	1 0 5 3	E F H L S
S	2 5 7 2	F H K L M R T
T	0 6 0 0	N R
U	0 2 6 3	E F K L N
V	0 4 3 4	G H K R
W	0 0 0 0	-
X	0 1 5 1	E H L M
Y	0 2 4 7	E F G L N
Z	0 0 5 0	H L

Backplane Section Y1

A	6 3 2 2	F K M N T U
B	5 6 0 4	G N R S U
C	7 3 4 3	E F L M N S T U
D	0 0 0 0	-
E	6 4 1 7	E F G H R T U
F	0 1 6 0	K L M
G	0 2 4 0	L N
H	0 3 1 3	E F H M N
I	7 6 0 3	E F N R S T U
J	0 0 0 0	-
K	1 2 5 4	G H L N S
L	6 5 7 6	F G H K L M R T U
M	0 4 0 2	F R
N	1 0 5 2	F H L S
P	0 0 3 0	H K
Q	0 0 0 0	-
R	6 4 6 6	F G K L R T U
S	7 0 6 5	E G K L S T U
T	6 4 0 1	E R T U
U	7 7 2 1	E K M N R S T U
V	6 2 5 0	H L N T U
W	0 0 0 0	-
X	1 5 0 5	E G M R S
Y	7 5 6 6	F G K L M R S T U
Z	0 0 0 0	-

Maintenance Procedures

Frontplane Section F0 and F1

A	0 4 2 4	G K R
B	7 5 2 2	F K M R ' S T U
C	7 6 3 5	E G H K N R S T U
D	1 3 3 6	F G H K M N S
E	7 5 6 7	E F G K L M R S T U
F	0 0 5 0	H L
G	0 1 5 6	F G H L M
H	0 3 2 5	E G K M N
I	7 1 3 0	H K M S T U
J	6 2 5 1	E H L N T U
K	7 6 4 4	G L N R S T U
L	1 0 1 2	F H S
M	7 5 1 2	F H M R S T U
N	7 6 4 2	F L N R S T U
P	0 6 6 3	E F K L N R
Q	0 4 2 4	G K P.
R	6 7 4 5	E G L M N R T U
S	7 5 7 5	E G H K L M R S T U
T	7 5 7 3	E F H K L M R S T U
U	5 5 6 5	E G K L M R S U
V	7 2 1 7	E F G H N S T U
W	0 1 0 3	E F M
X	0 7 3 4	G H K M N R
Y	0 2 0 0	N
Z	6 6 2 1	E K N R T U

Frontplane signal pins A thru' Z are located on the upper row of the F0/F1 connectors.

OUTPUT BUFFER CHECK

1. Set all Section Select switches UP. Set all Pin Select switches DOWN. Set disconnect I/O switch to DISCON. Depress INITIAL button. Set disconnect I/O SW to I/O. Set all PIN SELECT switches up. Depress INITIAL button. Card pin display should show 1's (ON) for all pins and for all rotary switch positions except:
X0A, X1A, D, J, Q, W, Y0Z, Y1D, J, Q, W, Z.
2. Using a voltmeter, measure the voltage output at the card backplane and frontplane connectors with the exception of the pins shown in paragraph 2a. Ensure the voltage is equal to or greater than 2.4 volts. A lower voltage usually indicates a failing output buffer or bad wire crimp.
- 2a. X0A, X1A are +4.75 volt inputs
X1D, J, Q, W are ground pins
Y1D, J, Q, W are ground pins
Y0Z, Y1Z are -2.0 volt inputs.

SINGLE SHOT CLOCK

Incorrect self-check signatures can result from either a faulty start bit INLQ or from a faulty exclusive-or AFAN element. A simple modification to the CL card enables

the FE to single step, clock by clock, through the Test phase and detect most logic faults by observation of the card pin LED display.

Modification Procedure

Modify the wire wrapped CL card as shown in Figure 5-5.

Add wires between E5H to G9R (INLN/Output)
G9S to L8C (EXT CLK.0)

Use spare inverter element at location G9.

Modify the etched CL card in the same way as shown in Figure 5-5, but use a different inverter element.

Add wires between E4H to E4R (INLN/Output)
E4S to L7C (EXT CLK.0)

Use spare inverter element at location E4.

This modification permits the INITIAL pushbutton to be used as an external single shot clock pulse.

Operating Procedure

Instructions to set up the FCT into the single shot mode is as follows:

1. Initialize the FCT.
2. Press clear, start and during the Test Phase, when the pulse counter reads 8888, set switch S38 to MANUAL.

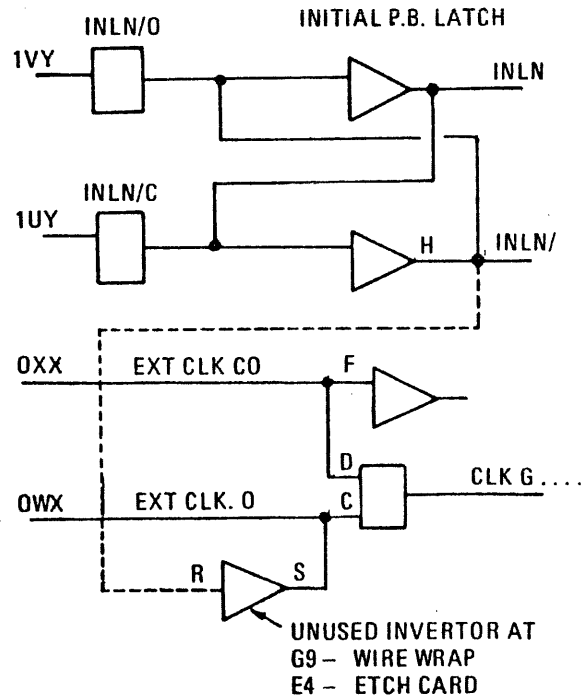


Figure 5-5. Single Shot Clock Modification

Maintenance Procedures

3. Set switch S40 to the 1/0 position.
4. Set all section select switches up.
5. Set all pin select switches down.
6. Press initial pushbutton to clear the word generator and LED display.
7. Select required section by rotary switch S2.
8. Select one pin select switch up.
9. Press INITIAL pushbutton to set the corresponding RFBN stage of the word generator section.
10. Set switch S36 to EX CLK.
11. Set switch S38 to AUTO.
12. Press INITIAL pushbutton for each single shot clock operation.

START BIT MODIFICATION INLQ

The single shot clock modification must be installed in conjunction with the INLQ modification.

Connect a temporary backplane jumper between INLQ at I1Y and EXT CLK0 at OXX on the CL card. This jumper freezes the clock sequence at the end of the Clear Phase immediately before the start bit INLQ is injected into the word generator.

Operating Procedure INLQ

1. Press clear and start pushbuttons with the operating panel switches in the normal position. The FCT will cycle through the Clear Phase and halt just before the INLQ start bit is injected.
2. Set switch S36 to EX CLK.
3. Press INITIAL pushbutton once and observe the LED display for each word generator section. The six INLQ start bits should be illuminated at the following switch positions and card pins:
 - a. F0 at pin B
 - b. F1 at pin B
 - c. Y0 at pin C
 - d. Y1 at pins C, F and R

Since INLQ lasts for two clocks, a second INITIAL pushbutton action will repeat the INLQ bit insertion and shift the first bit to the right. Repeated INITIAL pushbutton action shifts the bit patterns to the right, due to feedback, and is transferred to adjacent word generator sections. Cross refer to the word generator section layout shown in Section 2, Figure 2-14, of this manual.

NOTE

The temporary backplane jumper between I1Y and OXX on the CL card must be removed upon completion of trouble shooting procedures.

LED PIN POLARITY

Figure 5-6, shows the LED anode and cathode pin layout. Only the -12 volt LED is connected in reverse, as shown in Figure 4-5 terminal E17.

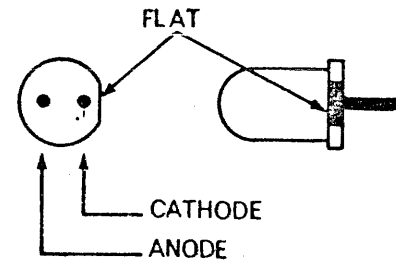


Figure 5-6. LED Pins.

RIN/LIN's

The FE is advised that the field card tester RIN/LIN's are issued under the B1700 system RIN series 3360.

LOCATION/ACCESS INSTRUCTIONS.

Figures 5-7 thru 5-9 are related to the following sub assembly component location and access instructions.
Electronics Assembly

1. Remove the cover.
2. Remove screws (7) from each side of the case.
3. Place FCT on its side with the handle uppermost.
4. Remove screws (4) from the bottom of the FCT.
5. Return FCT to its usual operating position and carefully lift the electronic assembly from the case.

Logic Card

1. Remove the card pin retainer.
2. Remove logic cards from the backplane connectors. Ensure cards are labelled correctly for later replacement. Logic cards CL, X0, X1, Y0 and Y1 are unique and cannot be interchanged. Only F0 and F1 logic cards are identical and may be interchanged.

Switch Assembly

1. Remove all switch locking nuts from the pushbuttons and switches on the operating panel side.
2. Remove switch assembly. It may be necessary to remove the large earth backplane lead for easier removal.

Lamp Board Assembly

1. Remove nuts (8) securing lamp board to electronic assembly.
2. Ensure LED's are not bent when replacing the lamp board.

End Panel Assembly

Access to the capacitor board, 12 volt relay and main on/off switch, backplane and frontplane connections are as follows:

1. Remove screws (3) from the operating panel side of electronic assembly.

Maintenance Procedures

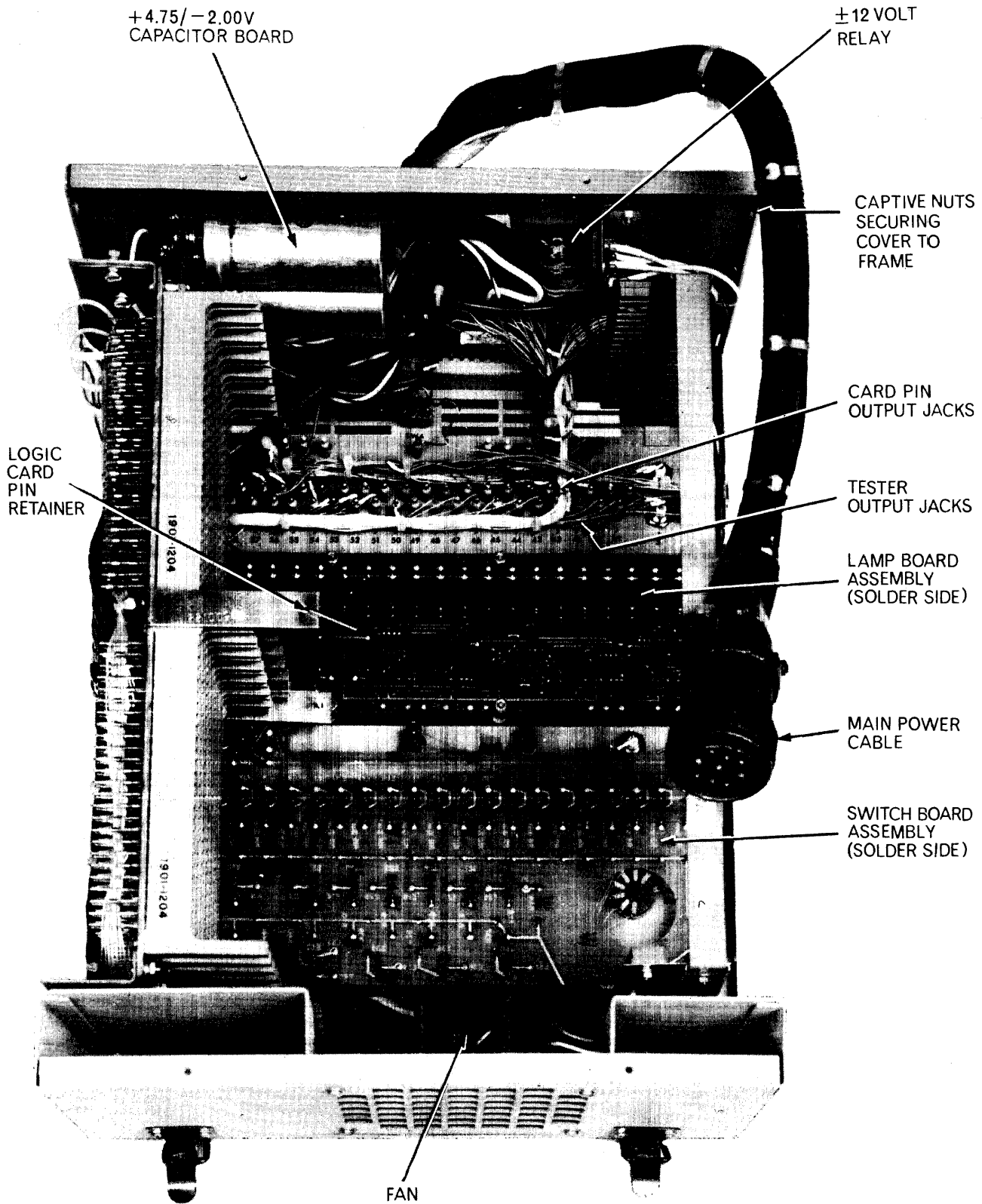


Figure 5-7. Electronic Assembly

Maintenance Procedures

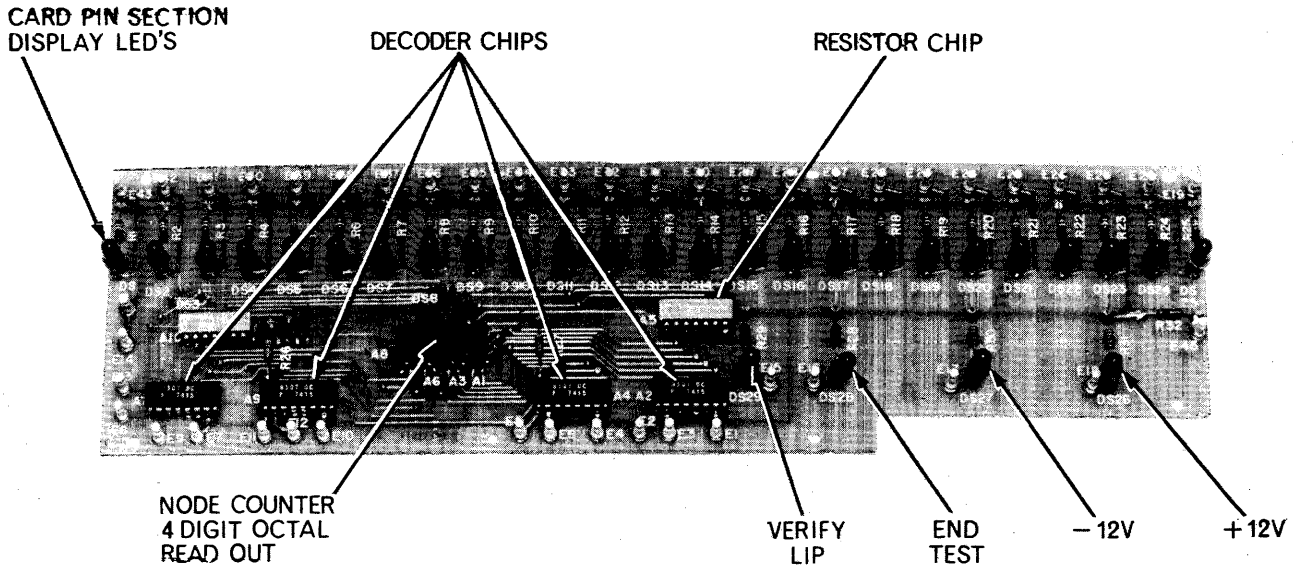


Figure 5-8. Lamp Display Board

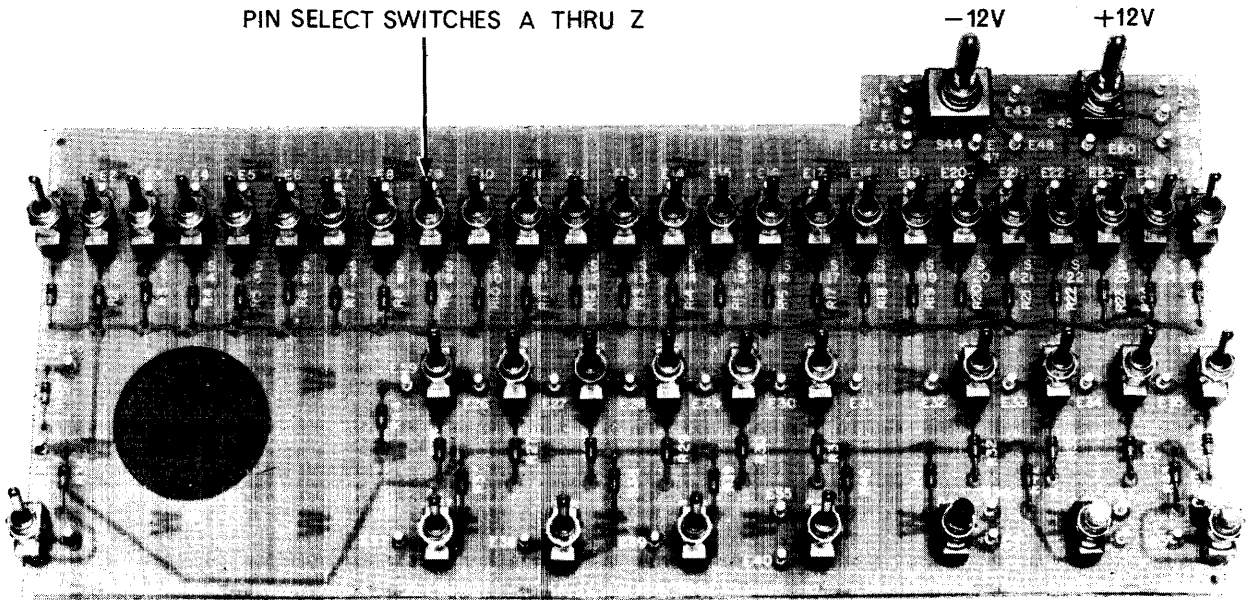
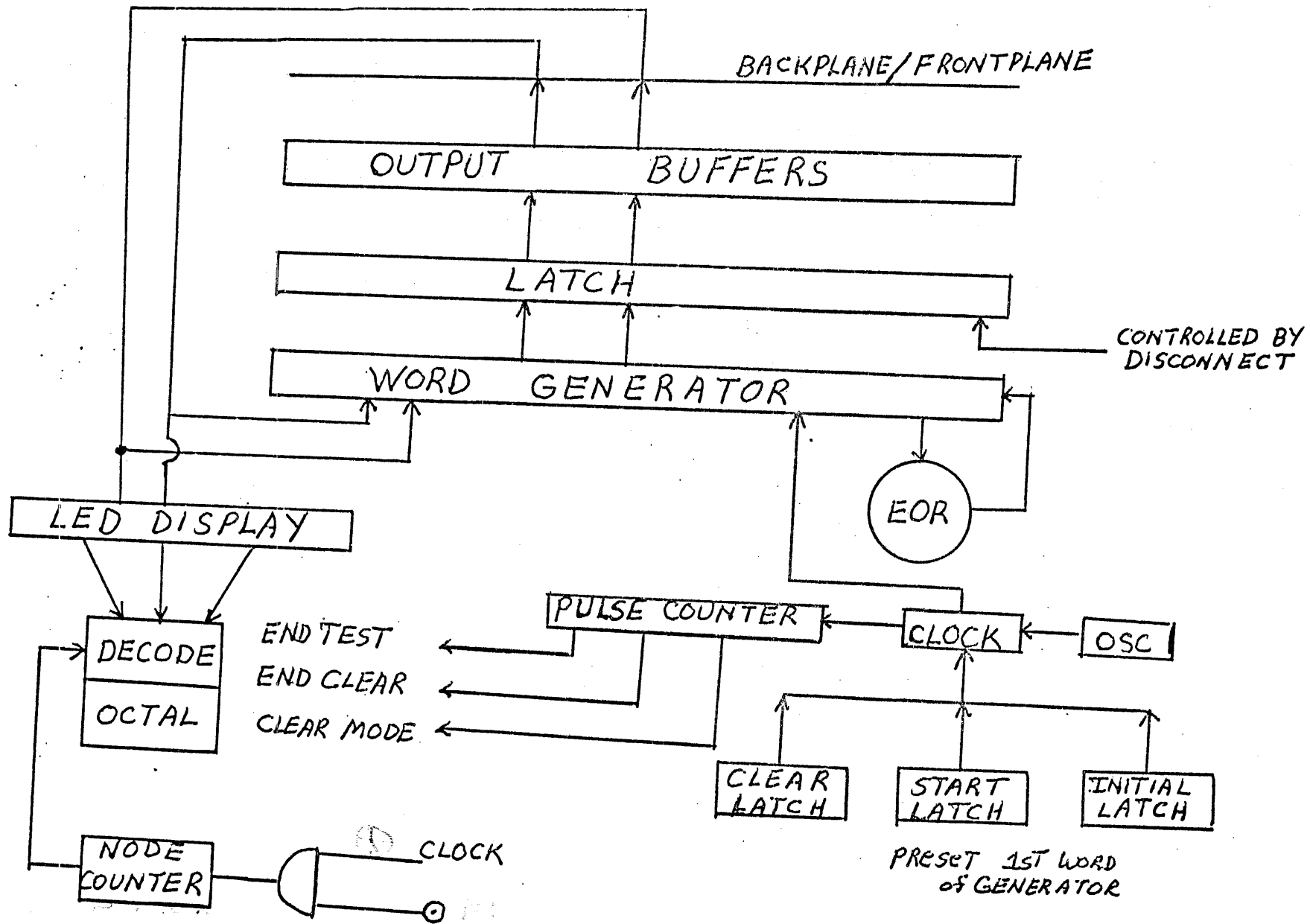
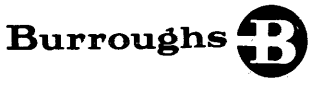


Figure 5-9. Switch Board Assembly.

Maintenance ProceduresCOMPONENT PART NUMBERS

1. Frontplane Connector, at F0, F1.
PN 2206 2087
2. Backplane double edge Connector, also for internal logic card connectors CL thru F1.
PN 1901 1204
3. Power On-Off Switch S1.
PN 2205 8432
4. Clock Load Switch S4.
PN 2012 3410
5. Ground Terminals,
Post: PN 2205 8978
Jack: PN 2206 6617
6. Card Pin and Tester Output Jacks.
PN 2205 8838
7. Coaxial Connector BNC
PN 2205 8358
8. D/TTL--CTL Switch S2
PN 2208 3796
9. Light Emitting Diodes (LED's) at, card pin display,
 ± 12 volts, power on, verify lip, end test.
PN 2300 6638
10. Pulse Counter Display Element.
PN 2205 7079
11. Display Decoder Chips.
PN 2205 8242
12. Decoder Load Resistor Chips (RPNN)
PN 2200 8320
13. Recycle/Normal Switch S5.
PN 2201 7875
14. Reset/12 volt Switch S6.
PN 2208 5047
15. + 12 volt Switch S45, 6 output pins.
PN 2206 6419
16. -12 volt Switch S44, 9 output pins.
PN 2206 6427
17. Pin Select Switches SPDT, also for section select, clear bus, external clock, XOW, manual NFB and DISCON.
PN 2201 7875
18. Rotary Display Switch S2
PN 2205 8291
19. Knob for Display Switch.
PN 1117 7326
20. Pushbuttons,
Clear: PN 1920 3231
Initial: PN 1920 3223
Start: PN 1920 3215
21. Fan, dual 50/60 cycle, 5 blade rotor
PN 2208 9262
22. Plastic Handle.
PN 2206 7862
23. Rubber Bumper, fitted to case.
PN 1103 2505
24. Rubber Bumper, fitted to cover.
PN 2206 7771
25. Burroughs Medallion.
PN 1128 5855 -
Spring Clip
PN 1907 7684
26. Self Locking Cable Strap, secures ribbon frontplane cables to cover, see Figure 1-13.
PN 2206 7821
27. Hinge-foot assembly, connects cover to case.
PN 2206 7912
28. Cover Latch assembly.
PN 2206 7888
29. ± 12 volt Relay.
PN 2208 5112





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