B 1700

80 COLUMN CARD READER CONTROL

Burroughs

FIELD ENGINEERING

TECHNICAL MANUAL

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GENERAL DESCRIPTION

The Card Reader Control consists of one standard B1700 card, located within either the I/O Base or an I/O Base Extension. The Card Reader used with this Control is the B9115-300CPM Reader or the B9116-600CPM Reader. These readers handle the standard 80 column card.

The Control is capable of translating the 12 bit (row) information read from the card into the code referred to as EBCDIC (Extended Binary Coded Decimal Interchange Code). If desired, the Control may perform a Binary read operation where each hole in a card column is translated as a one-bit and each non-hole as a zero-bit. In the case of the EBCDIC read, the Control performs a validity check and will insert the character "?" (Question Mark) in any column where an invalid character is found. The validity error will be reported to the Processor at the end of the read operation.

INTERFACE

The interface shown in Figure I-1 illustrates the control and data transfer lines between the Processor, Card Reader Control and the card read device. The interface between the Control and the Processor is via the Base Distribution Card in the I/O Base or via the Base Distribution Card and a Sub-Distribution Card (Extension) if the Card Reader Control is located within an I/O Base Extension. Refer to the I/O Base Technical Manual for details. The description of the Card Reader to Control interface is described within the glossary located in Section I of this manual.

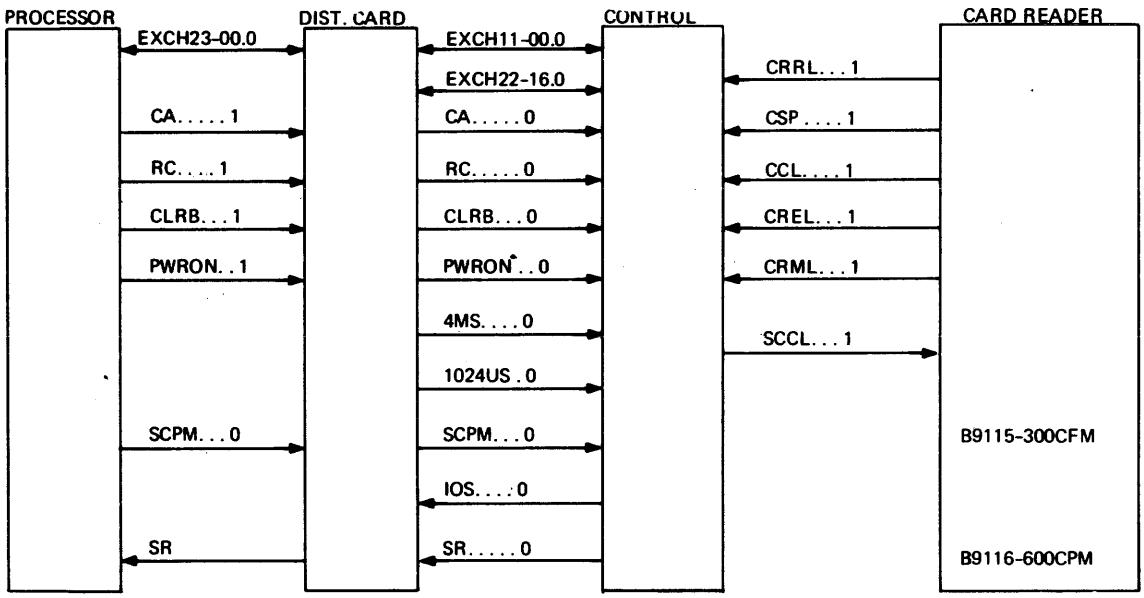


Fig. I-1 INTERFACE

GLOSSARY OF TERMS

REGISTERS AND COUNTERS

Command Register	The Command Register accepts all commands to all channels at CA (Command Active) time.
Command Variant Register	The Command Variant Register accepts all command variants to all channels at CA time and clears if the command at CA time is not a Command Variant.
OP Register	Accepts all OP Codes such as Read, Test or Pause when the Control is at Status Count 1 (STC01).
Input Register	The Input Register accepts all data which is to be stored in the MOS Buffer contained within the Control. The Input Register is a 12 bit register and accepts either 8 bit data from the Processor and Translator or accepts 12 bit data directly from the Card Reader.
100 Bit MOS Register	The 100 Bit MOS Register is 100 bits in length and 12 bits high (100 x 12). The register is a shift register and in order to shift and store data, two phase clock drivers are used.

Each shift and store operation requires four clock periods. (Refer to Figure II-7, 8).

Status Counter — (STC) The Status Counter sequences the Control Logic and counts from 00 thru 23. The status count is returned to the Processor during the RC portion of all commands except the Test Service Request and Transfer Out B commands.

Byte Counter — (BCNT) The Byte Counter is used to count the number of bytes either stored or read from the MOS Buffer in order to determine when an operation is to be terminated and a Service Request made.

Output Register — The Output Register is a 12 bit register and receives data read from the output section of the MOS Buffer. It is a temporary holding register for data to be transferred to the Processor.

INTERFACE (CONTROL/CARD READER)

CCL — CARD CYCLE LEVEL is true from the Card Reader upon sending a start card signal. CCL remains true for the entire read of the card.

CREL — CARD READER ERROR LEVEL is true from the Card Reader when an error has occurred in the read operation as a result of a failure in the Card Reader read circuits.

CRRL — CARD READER READY LEVEL is true when the Card Reader is ready for a read operation. ie. Power On, cards in the hopper and stacker is not full.

CR12L
CR11L
CR0L
CR1L
CR2L
CR3L
CR4L
CR5L
CR6L
CR7L
CR8L
CR9L — CARD READ LEVELS are twelve lines from the Card Reader which carry the column information from the Reader to the Control. Where a hole is detected the appropriate level is true and where a non-hole is detected, the appropriate level is false.

CSP — COLUMN STROBE PULSE is a 21 usec pulse from the Card Reader which occurs one time for each column read. It is this signal that indicates new data is available on the Card Read Lines.

SCCL — START CARD CYCLE LEVEL is a level from the Control to the Card Reader which will cause a card to be fed from the hopper to the read station and will go false upon reception of the first CSP from the Card Reader.

CONTROL MNEMONICS

BCNT — Byte Counter which counts number of bytes transferred from/to MOS Buffer.

CA — Command Active is true when the Processor is sending a command to one of the I/O Corttrols.

CH — Channel is true when the command sent at CA time is for the Card Reader Control as indicated by the Channel Number.

CHAF — Channel Active Flip-Flop is set to indicate that the command is for the Card Reader Control. Sets with CA*CH and resets at RC time.

CLTS — Clear and Test Status has been decoded on the Exchange Lines from the Processor.

CMR — Command Register used to store commands at CA time and reset with RC.

CODE8 — Code 8 refers to the translated EBCDIC data which has been read from the card.

CODE12 — Code 12 refers to the non-translated (binary) data read from the card.

CONTV/ — Control Variant Not refers to the fact that the command which is on the exchange lines from the Processor is not a Control Variants Command.

CONV — Control Variants Command has been decoded on the Exchange.

CRERF — Card Read Error Flip-Flop is set if a Read Error (CREL) has been detected by the reader and will be used to flag the error in the Result Descriptor.

CRRLPL	Card Reader Ready Leading Pulse Level is a pulse which is true when the Card Reader is first brought to the ready status.
CSPT	Column Strobe Pulse Trailing is a pulse developed within the Control as a result of CSP received from the Reader indicating data is available. CSPT is synchronized to the 4 usec bus.
EXCH	Exchange refers to the interface between the Control and the Processor which carries data to/from the Control.
ID	Identification refers to the unique identification assigned to the Card Reader Control which may be returned to the Processor during RC of a Test Status, Clear and Test Status or during the Result Descriptor of the Test-OP command for the Card Reader (010101).
INCSHF	Incomplete Shift is set to cause the data in the MOS Buffer to be right justified or may be set to allow the Shift Register Clock to run in order to count the BCNT for exit of the Pause or Test OPs.
IOS	I/O Send is enabled by the Control during the times which it is necessary for the Control to send data to the Processor.
NRDYF	Not Ready F/F is set to indicate a SCCL was sent to the reader and the reader is not ready.
OPREG	OP Code Register refers to the register where the OP Code is stored at STC01.
OR	Output Register is the register at the output of the MOS Buffer.
PAUSOP	Pause Operation is a Flip-flop set to indicate the OP-Code received at STC01 is a Pause OP.
PAUSOS	Pause One Shot is the output of a three bit-register indicating the pause duration of the Pause Op.
PH1DY	Phase One Delay is an output of the Shift Register (MOS Buffer) clock control. (Refer to Figure II-8).
PH2DY	Phase Two Delay is an output of the Shift Register (MOS Buffer) clock control. (Refer to Figure II-8).
RC	Response Complete is a signal received from the Processor and occurs on the second half of the command sequence (CA-RC).
READ12	Read 12 is true if the variant in the Read OP-Code indicate a 12 bit (Binary) read operation is to be performed by the control.
SCCF	Start Card Cycle Flip-Flop is set to produce Start Card Cycle Level (SCCL) to the Card Reader to initiate the reading of a card.
SERMSK	Service Mask refers to the bit returned to the Processor which corresponds to the Channel Number of the Card Reader Control if a Service Request has been made by the Control. SERMSK is returned with the Test Service Request Command at RC time.
SRF	Service Request Flip-Flop is set and indicates the Card Reader Control requires some type of service by the Processor ie. has data to be transferred.
STC	Status Count used to sequence the events which occur on the Test, Pause or Read operations.
TEST	Test refers to the TEST OP having been decoded.
TSR	Test Service Request indicates the Control Variant Command Test Service Request has been decoded by the Control.
TSTA	Test Status indicates the Control Variant command Test Status has been decoded by the Control.
VALE	Validity Error is true to indicate the eight bit data code which has been decoded by the control is not a valid code therefore transfer the character "?" will be transferred to the processor.
VALEF	Validity Error Flip-Flop is set if Validity Error (VALE) is true so that the error can be reported in the Result Descriptor.
WNOTRF	Wait on Not Ready is true if the variants in the Test OP indicate wait for the Card Reader to be in the Not Ready state before sending a Result Descriptor via a Service Request (SRF).

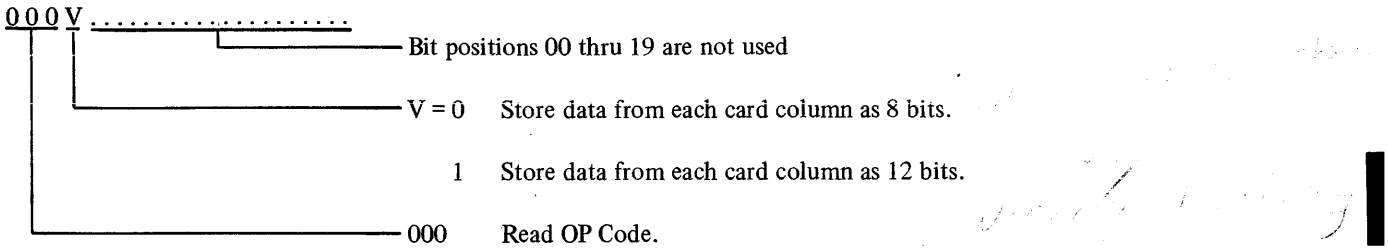
Functional Detail

I/O DESCRIPTION

The Card Reader Control is capable of executing one of three I/O Descriptors (also referred to as OP-Codes). EAch of the descriptors is 24-bits in length with the following variables:

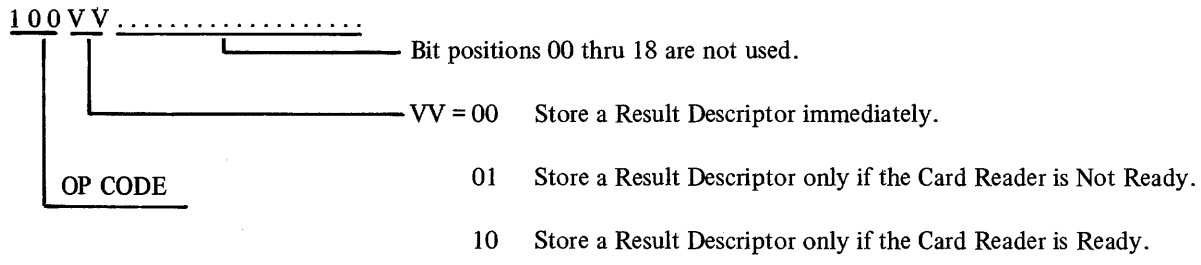
1. The three (3) most significant bits of the descriptor are decoded to represent the OP-Code.
2. V represents the Variant Bits.
3. (.) represents "Blank" bits with no significance; these bits should be set to zero.

READ OP



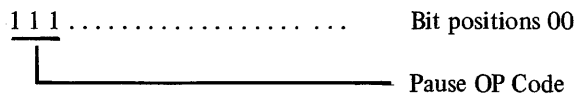
The READ-OP will read data from the Card Reader and store the data in a 100 x 12 MOS Buffer. The amount of data read will equal eighty columns of data. When the MOS Buffer is full, the Control will make a service request to the Processor and it is the function of the Processor to transfer the data from the buffer into Processor storage. The data read is either translated by the Control into an EBCDIC Code (8 Bit Data) or is transferred to the processor as 12 Bit Binary Data. Upon completion of the Read Operation, a Result Descriptor is returned to the Processor (See page 2 of this section).

TEST OP



The Test OP will test the Card Reader for the Not Ready Condition and return a Result Descriptor according to the variants. In addition to testing the status of the Reader, the Control returns the Control ID which is 010101 for the Card Reader Control described in this manual.

PAUSE OP



The Pause OP will insert a pause of approximately 8 milliseconds upon which time it will make a service request. Upon servicing the request, the Processor will receive the appropriate Result Descriptor from the Control.

I/O DESCRIPTOR TRANSFER TIMES

The 24 Bit I/O Descriptor is sent to the Control in three 8 Bit Bytes. The first Byte is sent at Status Count 01 (STC01), the second byte is sent at STC02 and the thired at STC03. Only the first byte has significance as it contains the OP-Code and variants. Refer to Figure II-1 for illustration of OP-Code transfer.

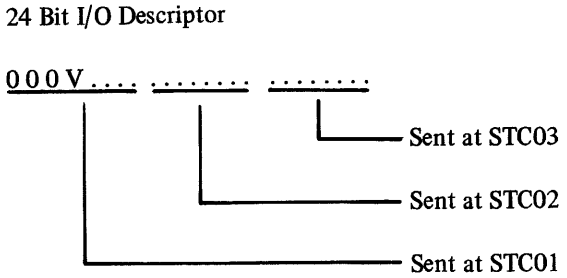


Fig. II-1 READ OP I/O DESCRIPTOR

RESULT INFORMATION

Upon completion of execution of the I/O Descriptors, a 24 bit Result Descriptor is available and is generated by the Control. The Processor (under software control) must transfer the Result Descriptor from the Control to the Processor. The information available in the 24 Bit Result Descriptor is as follows:

BIT	BUS POSITION	DESCRIPTION
1	23	Operation Completed
2	22	Exception Condition
3	21	Not Ready – operation not performed (Read & TEST)
4	20	Validity Error (READ)
5	19	Reserved
6	18	Reserved
7	17	Read Check (READ)
8-16	16-8	Reserved
17	7	Operation Completed
18-23	6-1	ID=010101 (TEST OP Only)
24	0	Reserved

RESULT DESCRIPTOR TRANSFER TIMES

The 24-bit Result Information is sent to the Processor by the Control in three 8-bit bytes. The first byte is sent at Status Count 21 (STC21), the second at STC22 and third at STC23.

BASIC DATA FLOW

Data read from the Card Reader is transferred to the Card Reader Control as 12 bit binary information. The strobe pulse for the data is supplied by the Reader and indicates one card column of data is available on the read lines. Each card column of data is stored in a 12 x 100 MOS Buffer within the Control. As each new card column is stored, the data in the buffer is shifted toward the right (Output Register) until the entire card has been read. Prior to being placed in the MOS

Functional Detail

Buffer the data may be translated and stored as 8-bit EBCDIC information rather than 12-bit binary information. A variant within the READ-OP specifies whether the translation is required. Figure II-2 illustrates this data flow.

When all 80 columns of the card have been read and stored in the manner described above, a Service Request is made and must be recognized by the Processor under software control. It is then a function of the Processor to send a series of commands to transfer the data from the MOS Buffer to the Output Register and subsequently be received by the Processor.

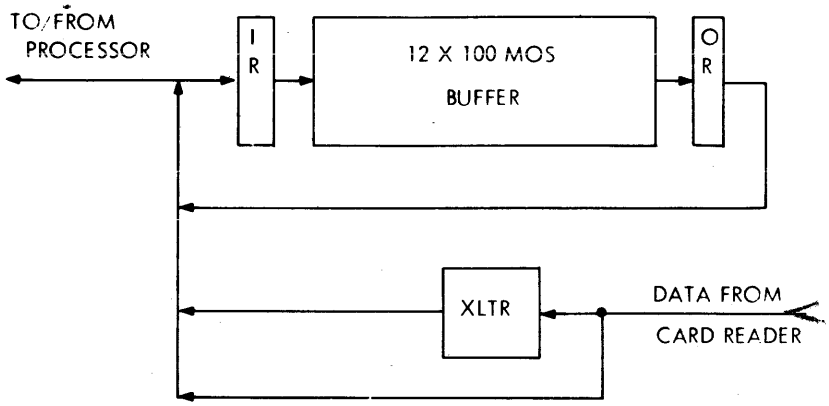


Fig. II-2

SIMPLIFIED FLOW

Each of the three OP-Codes (Read, Test and Pause) will cause a Status Counter in the Control to advance through a definite sequence of events. The Status Counter (STC) operation for the three Card Reader Control operations are shown in Figure II-3 with a description of each operation contained in the remaining pages of Section II of this manual.

TEST OP STC	PAUSE OP STC	READ OP STC
1	1	1
2	2	2
3	3	3
4	4	4
5	5	5
6	6	6
7	7	7
8	8	8
9	9	9
10	10	10
11	11	11
12	12	12
13	13	13
21	21	15
22	22	17
23	23	21
		22
		23

Fig. II-3 GENERAL FLOW FOR OP-CODES

Functional Detail

SIMPLIFIED FLOW OF TEST OPERATION

STC01 The Control is in the idle state at STC01. If the Card Reader Control is the Control which has been designated, the OP-Code which in this case will be a test is placed in the OP-Register. The variant bits will specify when a Service Request is to be made in order to complete the operation.

STC02 No Action

STC03 No Action

STC04 No Action

STC05 No Action

STC06 No Action

STC07 Receive Byte 1 of the Reference Address and temporarily store in the Input Register. Enable the MOS Buffer Clock Logic (See Figure II-7) and store Byte 1 of the Reference Address in the Buffer shifting the data presently in the Buffer to the right (No significant data contained in the Buffer at this time). Upcount the Byte Counter by one.

STC08 Receive Byte 2 of the Reference Address and store in the MOS Buffer shifting the previously received Byte 1 of the Reference Address to the right by one position (toward the Output Register). Upcount the Byte Counter by one. (BCNT=2)

STC09 Receive Byte 3 of the Reference Address and store in the Buffer shifting the previously received information to the right. Upcount the Byte Counter to BCNT=03.

STC10 Test the Card Reader according to the variants. If the Card Reader is in the condition specified by the variants or if the variants specify return a Result Descriptor regardless of the Card Reader Status, exit to Status Count 11. Before exiting to Status Count 11, set the Incomplete Shift (NCSHF) and shift the Reference Address which is contained in the Buffer until it is right justified.

STC11 Send Byte One of the Reference Address to the Processor when requested and shift the Buffer to the right by one. Reset the Service Request Flip-Flop which was set at Status Count 10.

STC12 Send Byte 2 of the Reference Address and shift the buffer to the right by one.

STC13 Send Byte 3 of the Reference Address to the processor and shift the buffer to the right by one place.

STC21 Send Result Descriptor Byte 1 which indicates operation complete, any exception conditions, status of the Card Reader and exit to STC22.

STC22 No Action

STC23 Send Result Descriptor Byte 3 to the Processor which contains a completion bit and the Control ID (010101). Clear all miscellaneous flip-flops and return the Control to STC01.

SIMPLIFIED FLOW PAUSE OPERATION

STC01 The Control is in the idle state at STC01. The OP-Code Byte One is received and placed in the OP Register. The OP being a Pause Operation, the Pause OP Flip-Flop is set.

STC02 No Action

STC03 No Action

STC04 No Action

STC05 No Action

STC06 No Action

During any of these No Action Status Counts if a 1024 usec pulse is received, the Pause One Shot is upcounted by one.

STC07 Receive Byte 1 of the Reference Address and temporarily store in the Input Register. Enable the MOS Buffer Clock Logic and store Byte 1 of the Reference Address in the Buffer. Upcount the Byte Counter by one (BCNT=01).

STC08 Receive Byte 2 of the Reference Address and store in the MOS Buffer shifting the previously receive Byte 1 of the Reference Address to the right by one position (toward the Output Register). Upcount the Byte Counter by one. (BCNT=02).

STC09 Receive Byte 3 of the Reference Address and store in the Buffer, shifting the previously received information to the right. Upcount the Byte Counter to BCNT=3.

STC10 With the operation a Pause each 1024 usec pulse upcounts the Pause One Shot until the entire delay has been imposed. Upon completion of the delay, set Incomplete Shift and right justify the Reference Address and exit to STC11.

STC11 When the Processor services the Service Request which was made at STC10, the Reference Address Byte one is sent to the Processor and the MOS Buffer is shifted to the right by one position.

STC12 Send Byte 2 of the Reference Address and shift the buffer to the right by one.
STC13 Send Byte 3 of the Reference Address and Shift the buffer to the right by one place.
STC21 Send Byte one of the Result Descriptor.
STC22 No Action
STC23 Clear all miscellaneous flip-flops and return the Control to STC01.

SIMPLIFIED FLOW READ OP

STC01 Receive the OP and store in the OP Register.
STC02 No Action
STC03 No Action
STC04 No Action
STC05 No Action
STC06 No Action
STC07 Receive Byte Two of the Reference Address and store in the MOS BUFFER. Upcount BCNT=01.
STC08 Receive Tyte Two of the Reference Address and store in the MOS BUFFER shifting previously received data to the right by one position. Upcount BCNT=02.
STC09 Receive Byte Three of the Reference Address and store in the MOS Buffer. Upcount the BCNT to three and start the card cycle.
STC10 Read 80 card columns of information and store in the MOS Buffer shifting the data to the right as each byte is received. If required translate the 12 bit data to EBCDIC or store as 12 bit binary data. Upcount the Byte Counter until all 80 columns of data have been read. Set the Incomplete Shift and justify the data contained in the buffer. Set the Service Request and exit to Status Count 11.
STC11 Send Reference Address Byte 1 to the Processor and reset the Service Request. Shift the data in the buffer to the right by one position.
STC12 Send Byte 2 of the Reference Address and shift the buffer to the right by one position.
STC13 Send Byte 3 of the Reference Address and shift the data in the MOS Buffer to the right.
STC15 Send 80 bytes of data to the processor, one byte at a time until the MOS Buffer is empty.
STC17 Send last byte of data to the processor.
STC21 Send Result Descriptor Byte One which contains any error conditions which may have occurred.
STC22 No Action.
STC23 Send Result Descriptor Byte 3, clear all miscellaneous flip-flops and go to idle Status Count (STC01).
NOTE: If during the read operation the Card Reader goes Not Ready the condition will be reported in the Result Descriptor. The data sent to the processor at STATUS COUNT 15 in this case would NOT be any good.

LOGIC DESCRIPTION

The following schematic diagrams with their associated descriptions show various sections of the logic contained within the CArd Reader Control. Also shown are various timing diagrams pertinent to the various operations.

COMMAND ACTIVE AND RESPONSE COMPLETE

Figure II-4 is a basic timing diagram showing the relationship of Command Active and Response Complete which are the result of Processor issued commands.

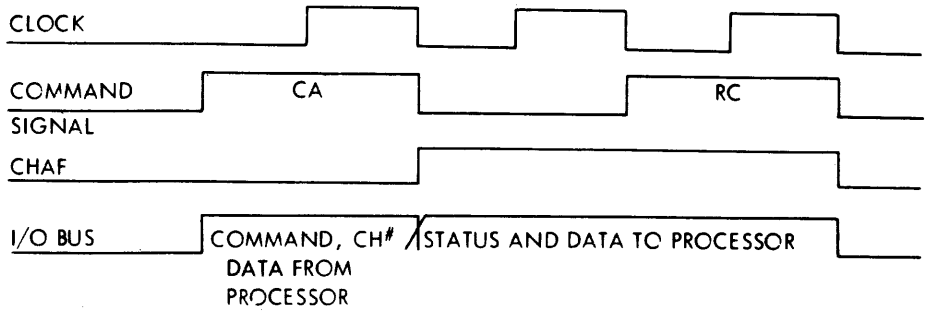


Fig. II-4 BASIC INTERFACE TIMING

Figure II-5 is a schematic diagram of the Command Register. Note that the command is placed in the register with each command that is received from the Processor (CMR EX=CA).

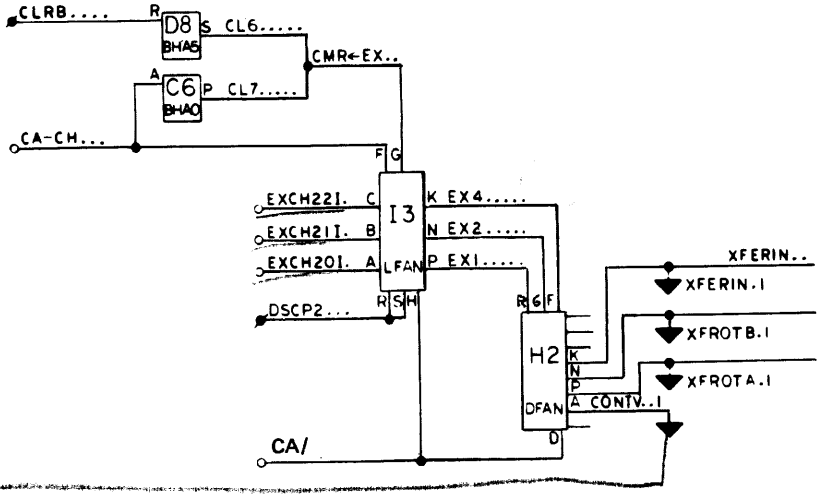


Fig. II-5 COMMAND REGISTER

CONTROL VARIANTS REGISTER

Figure II-6 is a schematic diagram of the Control Variants Register. At command Active time (CA) if the command is a Control Variants Command, the variants are set into this register. Those commands which are Control Variants commands are Test Service Request, Clear and Test Status and Test Status.

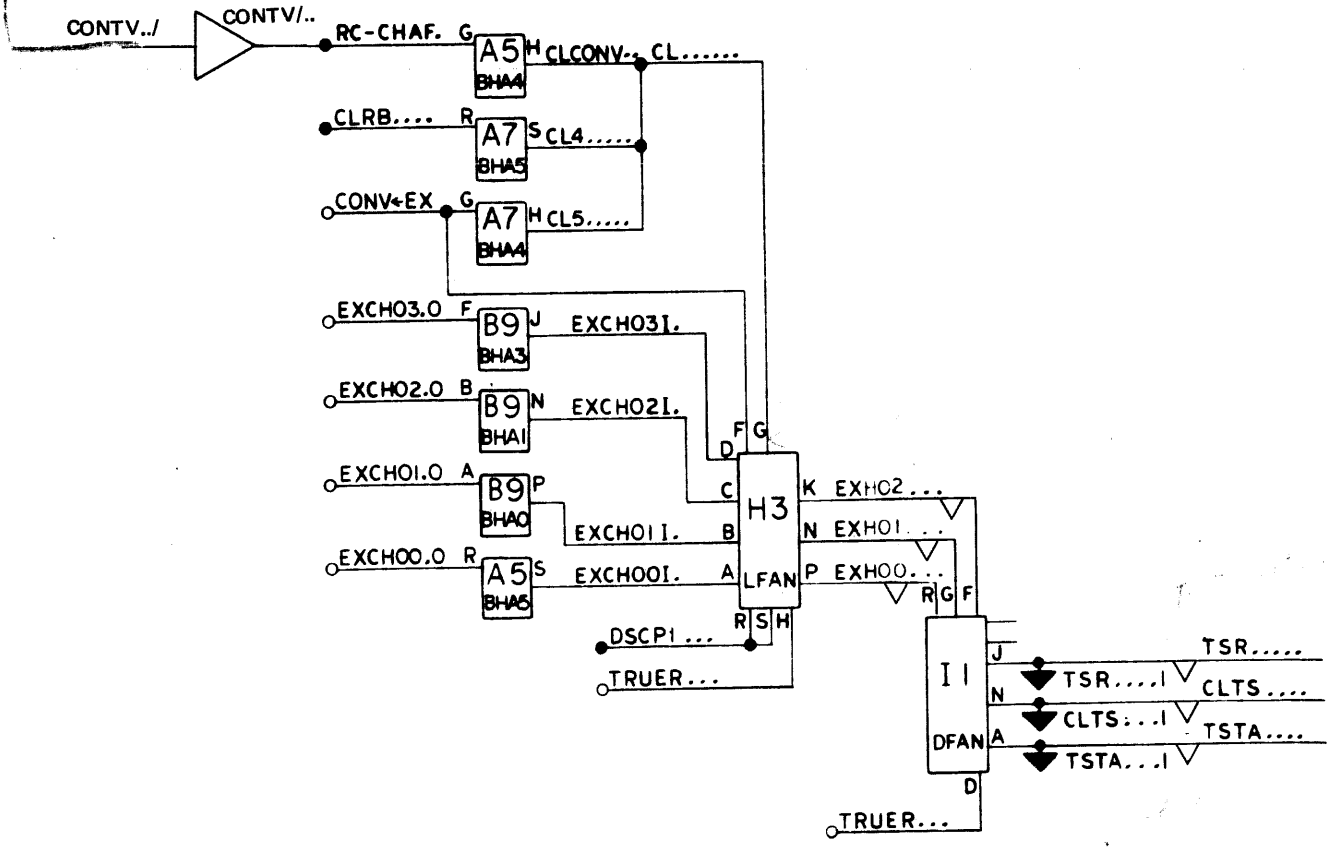


Fig. II-6 CONTROL VARIANTS REGISTER

Functional Detail

SHIFT REGISTER CONTROL

Figure II-7 is a schematic diagram of the MOS Buffer clock logic also referred to as Shift Register Control. It is the function of this logic to produce a clock to the MOS BUFFER to shift the contents of the Buffer and insert new data into the initial stage of the Buffer. Quiescently the term CTL-PH2. is true and PH1DY. . ., CTL-PH1. and PH2DY. . . are false. When either data is to be stored or if the buffer data is to be shifted, the term SHF (SHIFT) must come true. When SHIFT comes true the Four Bit Register element (RFBN) will be placed in the "D" set mode and when the clock occurs, PH2DY. . . sets and CTL-PH2. resets. PH2DY. . . through a buffer produces the term SHIFT UP (SHIFTUP.) which places the RFBN element in the shift mode. Each clock that occurs (Refer to Figure II-8) will shift the RFBN up until CTL-PH2. is true again at which time the RFBN is no longer in the shift mode. The term which started the sequence of events (SHF. . . . .) described above lasted for only one clock period and therefore the sequence of events terminates until SHF. . . . . is made true again by the logic. The four outputs of the Shift Register Control produced two clocks (MOS-PH1. and MOSPH2.) which will shift the contents of the MOS SHIFT BUFFER and store new data in the BUFFER.

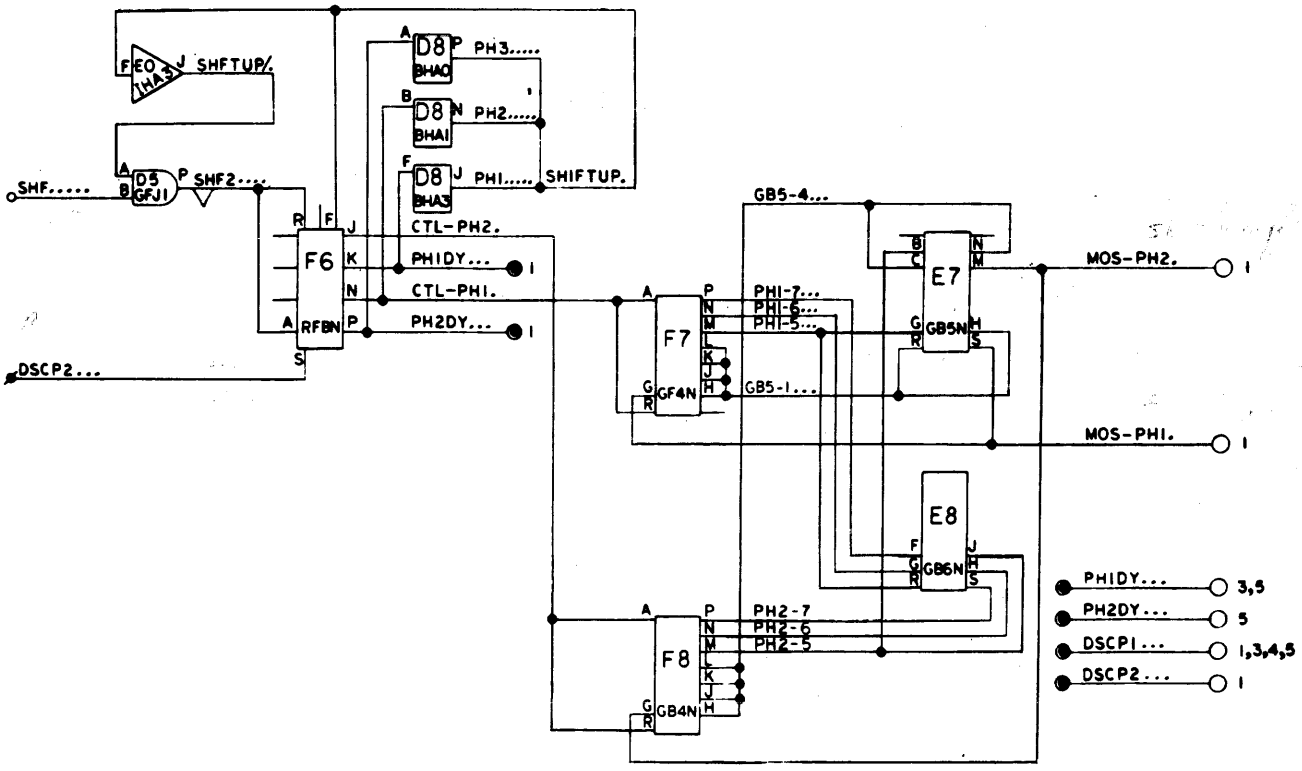


Fig. II-7 SHIFT REGISTER CONTROL LOGIC

COLUMN STROBE PULSE TRAILING

Figure II-9 shows the logic required for the development of the Column Strobe Pulse Trailing (CSPT) which is used by the Control to receive the information being read from the card. Column Strobe Pulse Trailing is developed as a result of the Column Strobe Pulse (CSP) received from the Card Reader. Figure II-10 is a timing diagram of CSPT. It should be noted that the duration of CSP is 21 usec and occurs once per card column at a rate of approximately 800 usec. The rate is NOT dependent upon the speed (399/600 CPM) of the Reader but is identical for both the B9115 and B9116 readers. The speed of the card through the read station is identical and the rate of the cards is dependent upon the delay or duration of time the card is in the hopper before being fed.

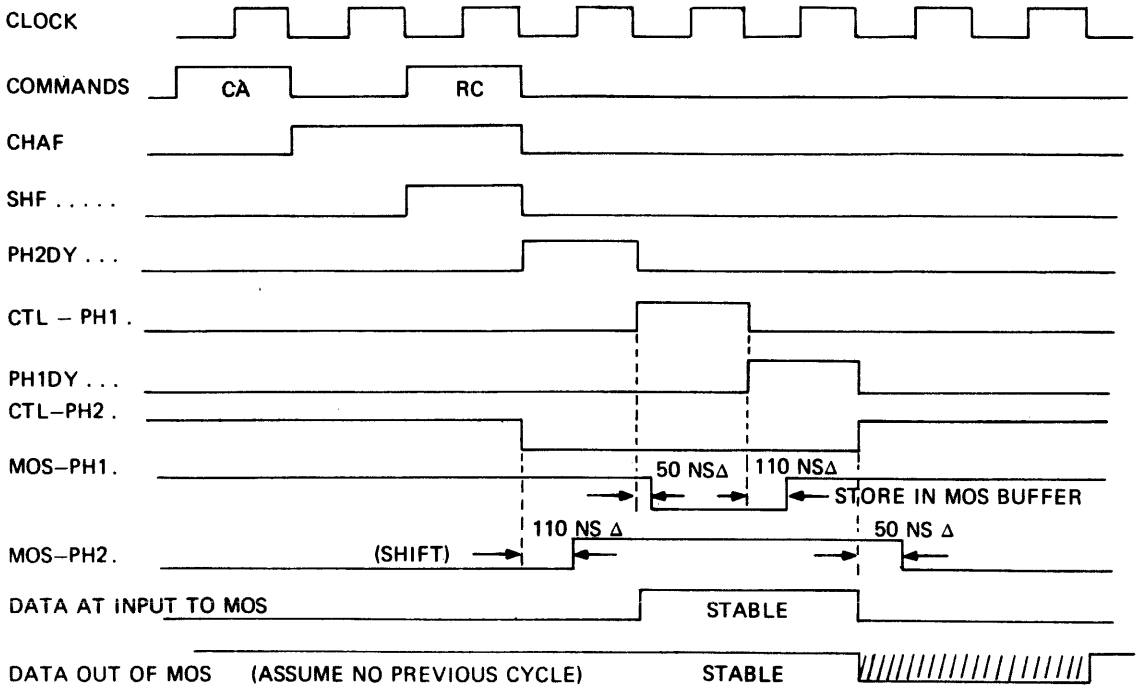


Fig. II-8 SHIFT REGISTER TIMING

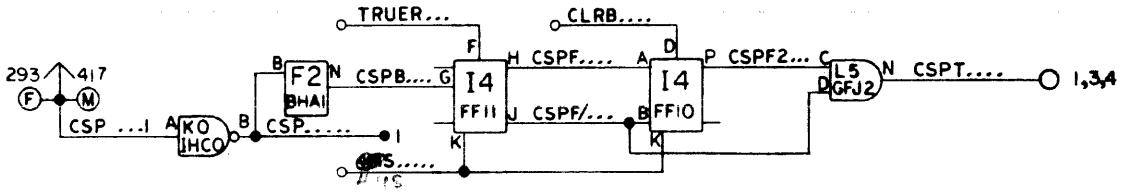


Fig. II-9 COLUMN STROBE PULSE TRAILING LOGIC

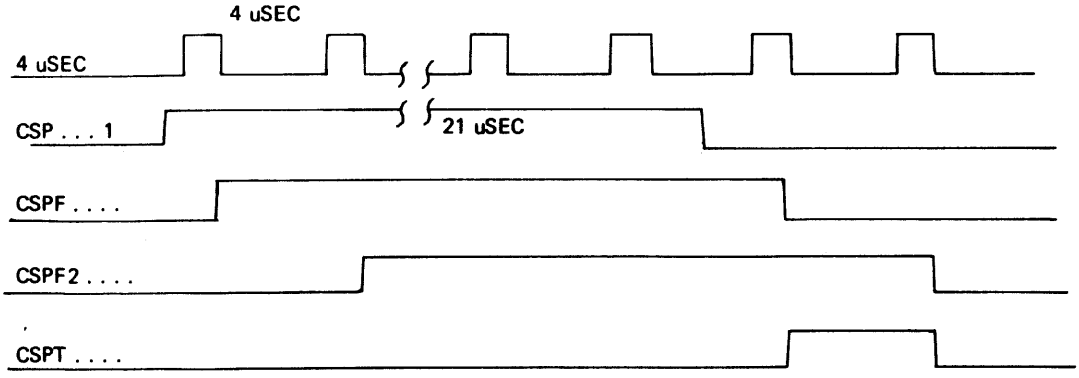


Fig. II-10 COLUMN STROBE PULSE TRAILING TIMING

Functional Detail

CARD READER DETAILED FLOW

CA (COMMAND ACTIVE)

CONV←EX	EXCH20I*EXCH21I/* EXCH22I/
CMR←EX	

With Command Active, if the Command is a Control Variants such as Test Status, Clear and Test Status or Terminate Data, the Exchange Lines 0 thru 3 are used to set the appropriate Control Variant in the Control Variants Register.

Command Active implies a command is on the Exchange Lines, therefore place the command in the Command Register. The Command Register indicates whether the command is a Transfer Out A, Transfer Out B, Transfer In or a Control Variants command.

RC (RESPONSE COMPLETE)

CRERF←0 IR←0 OR←0 VALEF←0 BCNT←0 STC←0 SRF←0 TEST←0 READ12←0	CHAF*CLTS
CHAF←0	

During the Response Complete portion of the two phase cycle , if this channel is active (CHAF) and the command received is a Clear and Test then the control is returned to the idle state with all miscellaneous flip-flops cleared in preparation for a new operation.

The Channel Active Flip-Flop is reset at the end of the two phase cycle (Command Active then Response Complete) to complete the cycle.

CONV←0	CONTV/

If the command in the Command Register is not a Control Variants Command then clear the Control Variants Register.

CA*CH

CHAF←1	
IR←EXCH	XFROTAD

With Command Active being true along with Channel (CH) the Channel Active Flip Flop is set. CH indicates that the command is for this channel. At Command Active time the channel address is on Exchange Lines 16 thru 19 and is compared to the Channel number which has been assigned (wired) to this channel.

If the Command is a Transfer Out A then the Exchange Lines 0 thru 7 which contains the data from the processor will be placed in the Input Register.

CHAF

EXCH←STC	XFROTB/*TSR/

During the data portion of the Response Complete which is indicated by Channel Active Flip-flop (CHAF) the Status Count is returned to the Processor unless the Command is a Transfer Out B or a Test Service Request in which other information is returned to the processor. Refer to description of commands in I/O Subsystem section of Processor Manual.

CHAF

EXCH←—ID	TSTA+CLTS	If the Processor has commanded either a Test Status or the Clear and Test Status Identification number (010101) is returned along with the status.
IOS←—1	TSR*CA/ +XFERIN	I/O Send is enabled on a Test Service Request or Transfer in Command to allow Data to be transferred from the I/O Control to the processor.
EXCH←—SERMSK	TSR*SRF	If the Command from the Processor is a Test Service Request and the Service Request Flip-Flop is set then the Service Request Mask is placed on the Exchange. The mask is a bit placed on the exchange which corresponds to the channel number.

STC01

OPREG←—EX	CA*CH*XFROTAD	With the Control at Status Count One and a Transfer Out Command is indicated for this channel then the contents of the exchange are placed in the Operation Register which will indicate if the operation is a Read OP, Pause OP, or Test OP.
PAUSOP←—1	CA*CH*XFROTAD *EXCH06I*EXCH07I	When the OP Code is received and bit 6 and 7 of the Exchange are true then the operation is a Pause Op.
STC+1	RC*CHAF*XFROTA	When the Processor completes the second half of the cycle the Status Count will be returned to the Processor and the Status Count upcounted.

STC (CAN OCCUR AT ANY STC)

STC+1	(STC02+STC03+STC04 +STC05+STC06)*RC* CHAF*XFROTA)	No Action is required for the Card Reader Control at Status Counts 2 thru 6 so with each CA and RC upcount the Status Counter.
PAUSOS+1	PAUSOP*1024us	With each 1024us pulse upcount the Pause OP Counter. This is used to insert the msec pause.
TEST←—0	PAUSOP	If the operation is a Pause OP, reset the Test Flip-Flop.

STC07

IR←—EXCH	CA*CH*XFROTAD	Place Byte One of the Reference Address in the Input Register.
STC+1	RC*CHAF*XFROTA	Upcount the Status Counter to Status Count Eight to receive Byte Two of the Reference Address.
PH2DY←—1	RC*CHAF*SFROTA	Phase2 Delay is set to initiate the Clock Generate which will place the contents of the Input Register in the MOS Buffer which in this case will result in the Reference Address Byte One being stored. Refer to Figure II-7 for a description of the clock and MOS Buffer.
BCNT+1	PH2DY	With PH2DY set upcount the Byte Counter which will count the number of Bytes stored in the MOS Buffer.

Functional Detail

STC08

IR←EXCH	CA*CH*XFROTAD	Place Byte Two of the Reference Address in the Input Register.
STC+1	RC*CHAF*XFROTA	Upcount the Status Counter to Status Count Nine to receive Byte Three of the Reference Address and start a Card Cycle if the operation is Read OP.
PH2DY←1	RC*CHAF*XFROTA	Phase 2 Delay is set to initiate the Clock Generator which will place Byte Two of the Reference Address in the MOS Buffer and shift Byte One of the Reference Address by one place toward the output register.
BCNT+1	PH2DY	Upcount the Byte Counter to reflect the fact that two bytes have been stored.

STC09

SCCF←1	CA*CH*XFROTAD *TEST/*PAUSOP/	If the operation is not a Test (TEST/) and not a Pause (PAUSOP/) then set the Start Card Cycle Flip-Flop as the operation is a Card Read.
IR←EXCH	CA*CH*XFROTAD	Receive Byte Three of the Reference Address and store in the Input Register.
STC+1 PH2DY←1	RC*CHAF*XFROTA	Upcount the Status Counter to Ten to perform the Operation specified and set PH2DY to store Byte 3 of the Reference Address and shift bytes 1 and 2.
BCNT+1	PH2DY	With PH2DY upcount the Byte Counter to reflect that three bytes have been stored in the MOS Buffer.

STC10

SCCF←0	CSPT+CRRLF/	The Start Card Cycle Flip-Flop is reset with the Column Strobe Pulse Trailing (CSPT) which is a result of a Column Strobe Pulse (CSP) received from the Reader and synchronized with the 4us bus. This indicates a card cycle has been initiated. If the card is not ready the F/F is reset also.
IR←CODE8	CSPT*READ12/*VALE/	With the receipt of the Column Strobe Pulse, data from one card column is available and if the operation is an EBCDIC read (READ12/) and a Validity Error does not exist (VALE/) then place the translated data (CODE8) into the Input Register.
IR←CODE12	CSPT*READ12	With the receipt of the Column Strobe Pulse and the operation is a Binary Read (READ12) then place the non-translated data (CODE12) into the Input Register.
IR←QM	CSPT*READ12/*VALE	If on the EBCDIC Read a Validity Error exists (VALE) force a question mark (?) bit configuration in the Input Register in place of the actual data read.

STC10

VALEF←1	CSPT*VALE	If a Validity Error occurred, set the Validity Error Flip-Flop to remember the error which will be reported at the time the Result Descriptor is sent to the Processor.
CRERF←1	CCLF*CREL	If a Card Read Cycle is in progress and a read error occurs, set the Card Read Error Flip-Flop to report the error at Result Descriptor time.
PH2DY←1	CSPT*CCLF*4us	With a Card Cycle (CCLF) and as each data column is received (CSPT, set PH2DY which will allow the data to be taken from the Input Register and stored in the MOS Buffer. In addition any previous data in the Buffer will be shifted toward the output section.
BCNT+1	PH2DY	When the new information is stored in the buffer, upcount the Byte Counter to reflect the number of bytes now stored in the buffer.
INCSHF←1	(SCCF/*CCLF/*PAUSOP/ *TEST/)	End of Card Read operation, justify the data in the buffer toward the output section by setting incomplete shift which allows the justify to occur.
	+(TEST/*PAUSOP/* CRRLF/)	Read OP was commanded but the Card Reader is Not Ready, shift in order to upcount the BCNT in order to exit to store the Result Descriptor.
	+(CCLF*CRRLPL)	If the Card Reader goes Not Ready in the middle of a Card Cycle (i.e., jam) and then when the reader is made ready, a pulse is produced (CRRLPL) which will allow the Incomplete Shift Flip-Flop to set and prevent the Control from hanging in STC10.
	+(TEST*READ12*CRRLF *4usec)	READ12 in the case of a Test OP indicates the variant is a 10 and therefore store a Result Descriptor and exit only if the Reader is Ready (CRRLF).
	+(TEST*WNOTRF* CRRLF/*4usec)	TEST OP and the variant is 01 indicating store the Result Descriptor if the Reader is Not Ready (CRRLF/).
	+(TEST*READ12/)* WNOTRF/*4usec)	TEST OP and the variant is 00 indicating store a Result Descriptor regardless of the status of the Reader.
	+(PAUSOP*PAUSOS/)	The operation is a Pause OP and PAUSOS/ indicates the pause period is over, therefore exit to store the Result Descriptor.
PH2DY←1	INCSHF*4usec	With Incomplete Shift (INCSHF) set and with each 4 usec pulse PH3DY is set which will initiate the sequence to justify the data in the MOS Buffer and upcount the Byte Counter (BCNT).
OR←BUFFER	BCNT100*4usec	With the Byte Counter equal to one hundred (100) take the contents of the Buffer (Reference Address Byte one) and place the data into the Output Register in order for the data to be sent to the Processor.

Functional Detail

STC10

INCSHF←0 STC+1 SRF←1 BCNT←02	BCNT101*PH1DY	With the Byte Counter equal to one hundred and one (101) and at PH1DY time of the clock, reset the Incomplete Shift, upcount the Status Counter to Eleven, set the Service Request Flip-Flop and set the Byte Counter to Two to indicate that Byte 2 of the Reference Address is the next byte to be obtained from the MOS Buffer.

STC11+STC12+STC13

EXCH←OR	CHAF*XFERIN	With the Processor sending a Transfer In Command as a result of recognizing the Service Request, the Output Register which contains either Byte 1, Byte 2 or Byte 3 of the Reference Address is placed on the Exchange Lines as data.
PH2DY←1	RC*CHAF*XFERIN	During the Response Complete portion of the Transfer In Command, PH2DY is set which will cause a new byte of data to be placed into the Output Register and the Byte Counter to be up-counted.
STC+1	RC*CHAF*XFERIN	Upcount the Status Counter and status will be sent to the Processor along with the Reference Address.
OR←BUFFER	RC*CHAF*XFERIN	The previous byte in the Output Register has been sent to the Processor, therefore place the next byte of data into the OR to be sent to the Processor.
BCNT+1	PH2DY	With each PH2DY, upcount the Byte Counter to reflect the number of bytes sent to the processor.
SRF←0	STC11*RC*CHAF* XFERIN	When the first Reference Address Byte is sent to the Processor, reset the Service Request Flip-Flop as the request has been recognized.

STC13

STC←21	RC*CHAF*XFERIN* (TEST+PAUSOP)	Neither a Test OP nor a Pause OP have data to be sent therefore exit to STC21 to start sending the Result Descriptor.
STC+2	RC*CHAF*XFERIN* TEST/*PAUSE/	Exit to Status Count 15 if the operation is a Read OP (Test/* PAUSE/) to send the data read to the processor.

STC15

OR←BUFFER PH2DY←1	RC*CHAF*XFERIN	Take the data from the MOS Buffer and place in the OUTPUT Register to send to the Processor. PH2DY is set to cause a shift of information so that at the appropriate time a new byte of data will be available at the output of the Buffer.
EXCH←OR	CHAF*XFERIN	Send the data contained in the Output Register to the Processor via the Exchange Lines.
BCNT+1	PH1DY	Upcount the Byte Counter to reflect the number of bytes sent to the Processor.
STC←17	RC*CHAF*XFERIN* BCNT83	Eighty bytes of data and three bytes of Reference Address have been read from the MOS Buffer, exit to Status Count 17 to transfer the last data byte to the Processor.

Functional Detail

STC17

EXCH←OR	CHAF*XFERIN	Place the last byte of data (Card Column 80) on the Exchange to the Processor.
STC←21	RC*CHAF*XFERIN	When the Processor sends the Transfer In Command to receive the last byte of data, exit to Status Count 21 to begin sending the Result Descriptor.

STC21

EXCH←RD	CHAF*XFERIN	Send Byte One of the Result Descriptor to the Processor.
STC+1	RC*CHAF*XFERIN	When Processor reads the Byte One, exit to Status Count 22 to send byte 2.

STC22

STC+1	RC*CHAF*XFERIN	No result information is tranferred to byte 2, exit to Status Count 23.

STC23

EX07←OC	CHAF*XFERIN	Transfer Additional Operation Complete Bit.
EXCH←ID	CHAF*XFERIN*TEST	Send ID number (010101) if the operation was a TEST.
STC←01 CRERF←0 VALEF←0 BCNT←0 TEST←0 READ12←0 PAUSOP←0 OR←0	RC*CHAF*XFERIN	End of operation, clear all miscellaneous flip-flops and return the Status Counter to 01 to await the new operation.

ADJUSTMENTS

There are no adjustments for the Card Reader Control.
Refer to I/O Base Section IV for clock adjustments.
Refer to Card Reader Control Section VI for determining the control channel number.

INTRODUCTION

The purpose of this section is to provide directions and aids in maintaining the 80 Column Card Reader Control.

PREVENTIVE MAINTENANCE

There is no preventive maintenance needed for the 80 Column Card Reader Control. Refer to the 80 Column Card Reader Manual for PM relating to the device.

SPECIAL MAINTENANCE TOOLS REQUIRED

80 Card Reader Control Confidence Routine
B1700 Field Card Tester
Tektronix 453A Oscilloscope or equivalent
Tripplet 630 VOM or equivalent
I/O Debug Routine

MAINTENANCE CONCEPT

B1700 controls are soft controls. No off-line capability is built into the control. The B1700 maintenance concept is centered around the use of test routines used in conjunction with the Field Card Tester. Hardware test points are provided for conventional troubleshooting.

TEST ROUTINES

CONFIDENCE ROUTINE

The 80 Column Control Confidence Routine checks the following:

1. Not Ready Condition
2. Binary Reads
3. EBCDIC Reads

RUN INSTRUCTIONS

The program listing provides Run Instructions.

RESULTS

Refer to Test Procedures to analyze the failure.

I/O DEBUG ROUTINE

General

Figure V-1 is a break down of the processor to I/O flow. In the case of the Card Reader it is strictly an input device.

The program listing calls for manually loading parameters such as device ID and the OP code.

TRACE AND STEP OPTION

As stated in the program listing, a number of program options are available. From a troubleshooting standpoint the two important options are Trace and Step.

The Trace option traces on the Line Printer the transfer's to and from the I/O base.

The Step option halts after each I/O transfer. The state of the exchange lines sent out to the I/O base and the state of the exchange lines coming back are displayed in two registers.

TEST PROCEDURES

Card Reader Control troubleshooting should follow these basic steps.

VISUAL CHECKS (Refer to 80 Column Control Section VI)

1. Assure that the control has been loaded into a valid one card control slot.
2. Assure that the cabling to the Card Reader is proper.
3. Assure that a channel jumper chip has been installed and that no two controls have the same channel number.

RUN CONFIDENCE ROUTINE

1. Before running the 80 Column Card Reader Confidence routine be assured that processor and memory are functioning properly. Run the processor and memory test routines.
2. Run the 80 Column Card Reader Confidence Routine (Refer to paragraph on Confidence Routine).

TYPES OF FAILURES FROM THE CONFIDENCE ROUTINE

1. Routine will not run.
2. Not Ready Section fails.
3. EBCDIC Read fails.
4. Binary read fails.
5. Confidence test passed.

DECISION

Refer to Figure V-2 and Figure V-3 for guidance in running the test routine and troubleshooting.

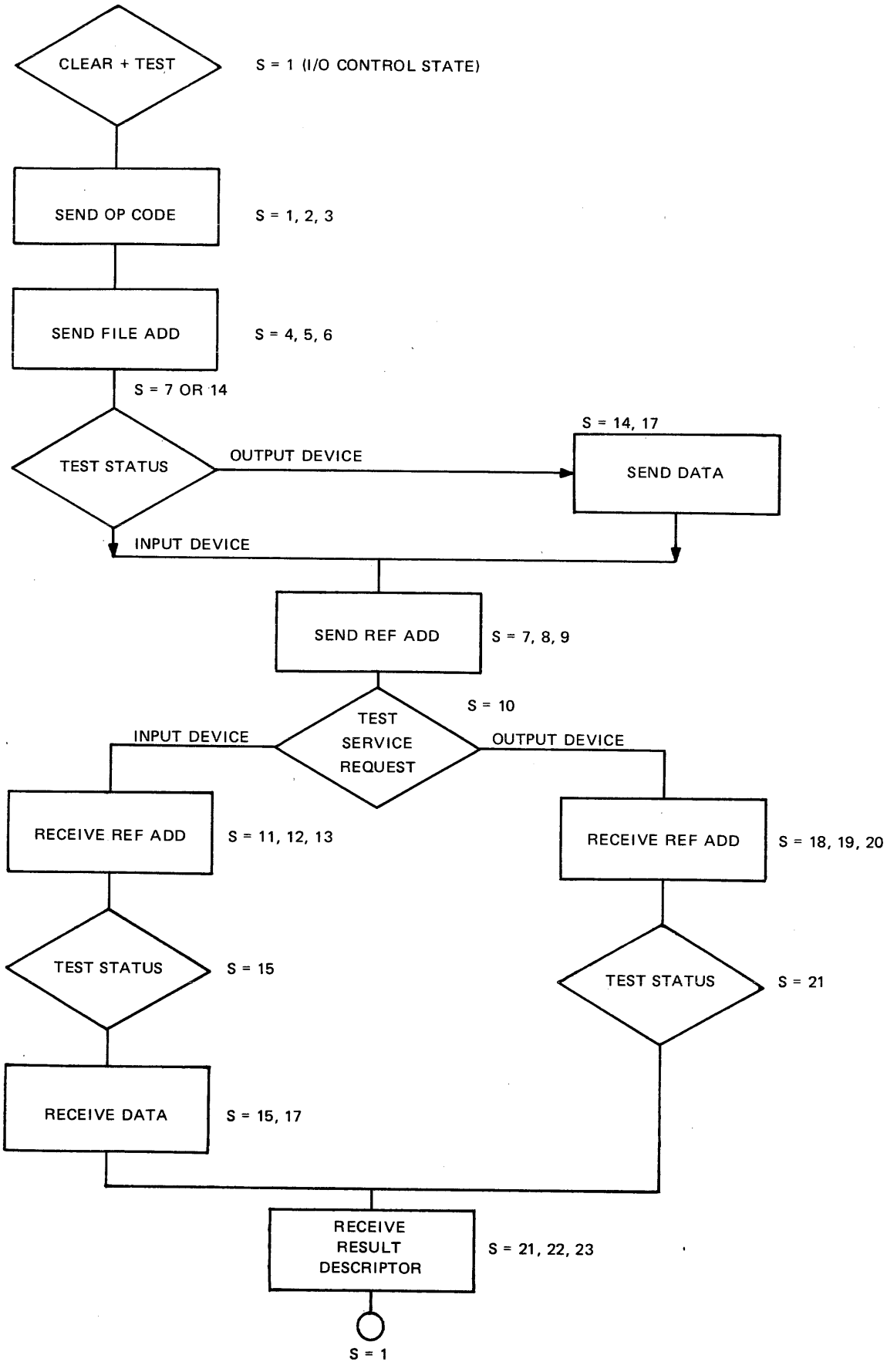


Fig. V-1 PROCESSOR TO I/O FLOW

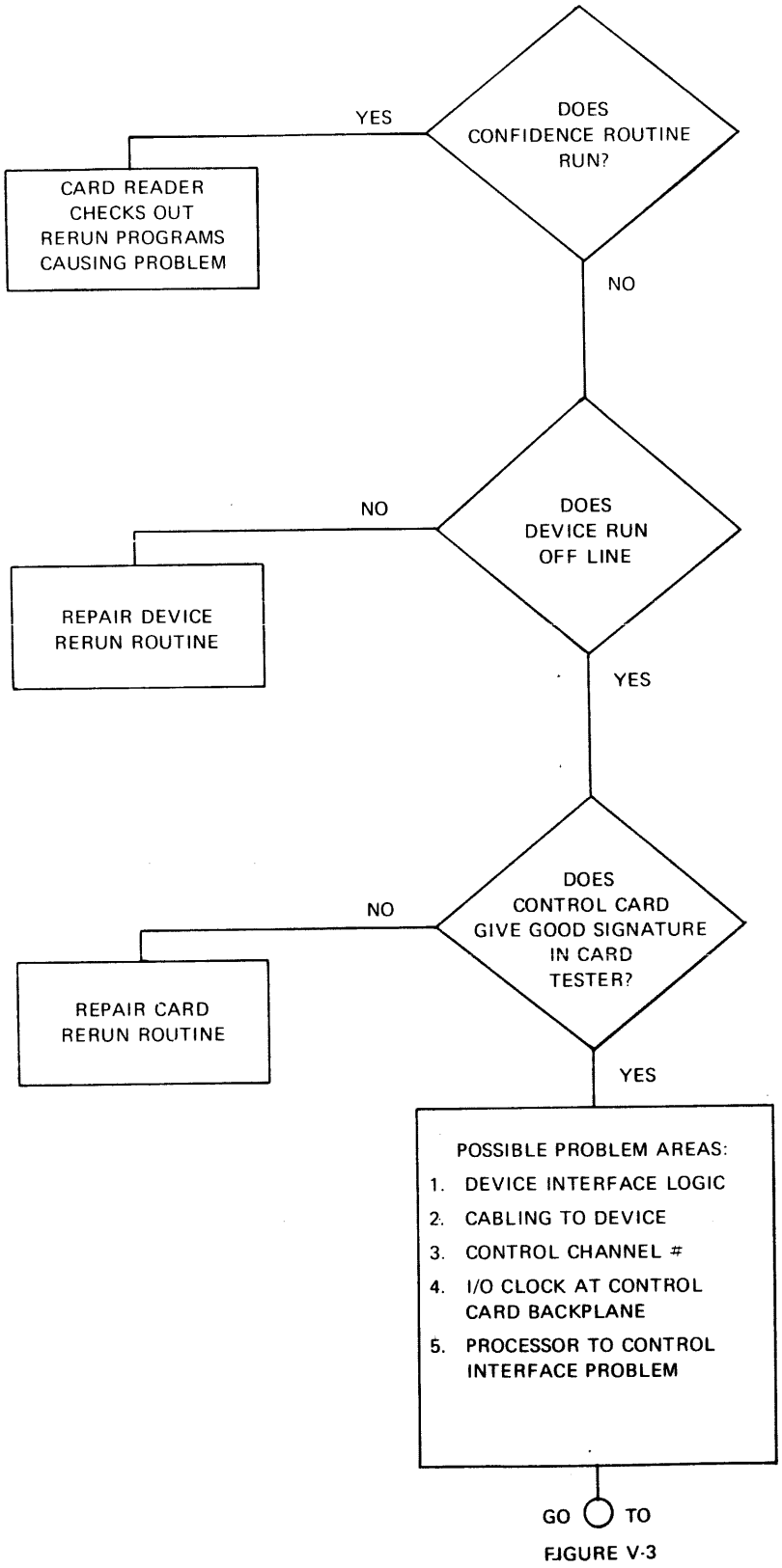


Fig. V-2 TROUBLESHOOTING PROCEDURE

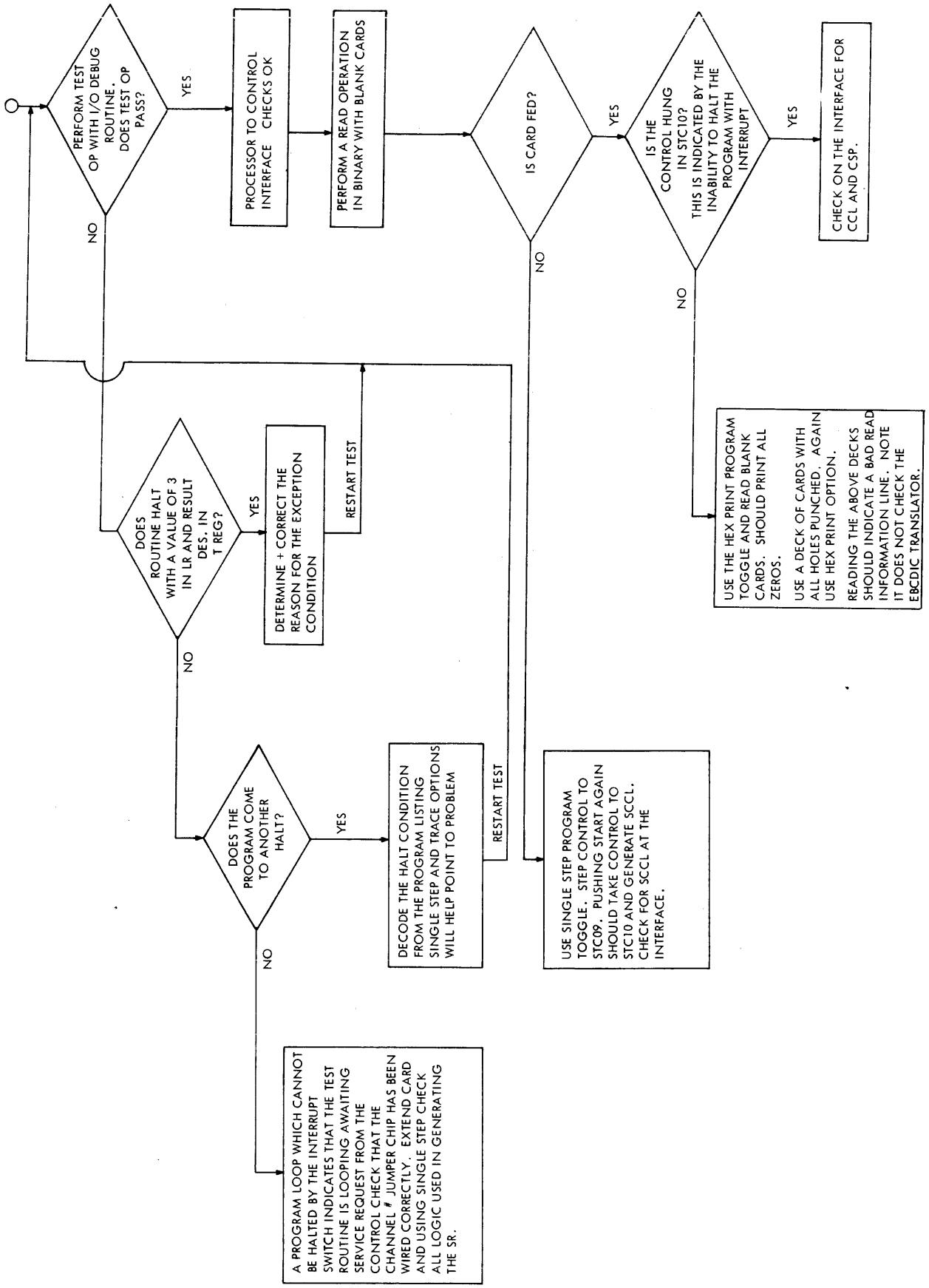


Fig. V-3 TROUBLESHOOTING FLOW CHART

HARDWARE TESTPOINTS

FRONTPLANE TESTPOINTS

$X Testpoints

A	STR1...1	I	RC-CHAF1	R	IREX3..1
B	STR2...1	J	TEST...1	S	IREX4..1
C	STR4...1	K	READ12.1	T	IREX5..1
D	STC8R..1	L		U	IREX6..1
E	STC16R.1	M		V	IREX7..1
F		N	IREX0..1	W	IREX8..1
G		P	IREX1..1	X	IREX9..1
H	CA.....1	Q	IREX2..1	Y	IREX10.1
				Z	IREX11.1

#X Testpoints

A	BC1....1	I	XFERIN.1	R	
B	BC2....1	J	XFROTB.1	S	CR12B..1
C	BC4....1	K	XFROTA.1	T	CR11B..1
D	BC8....1	L	CONTV..1	U	CR0B...1
E	BC16...1	M		V	CR9B...1
F	BC32...1	N	TSR....1	W	CR8B...1
G	BC64...1	P	TSTA...1	X	CR07B..1
H		Q	CLTS...1	Y	CR06B..1
				Z	CR05B..1

$Y Not Used

#Y Levels to Card Reader

A	SCCL...1	I	CR8L...1	R	CSP....1
B	CR1L...1	J	CR9L...1	S	
C	CR2L...1	K	CR0L...1	T	
D	CR3L...1	L	CR11L..1	U	CREL...1
E	CR4L...1	M	CR12L..1	V	CRCL...1
F	CR5L...1	N	CRRL...1	W	
G	CR6L...1	P	CCL....1	X	
H	CR7L...1	Q		Y	
				Z	

BACKPLANE TESTPOINTS

	Backplane 0		Backplane 1
	+4.75V	A	+4.75V
	EXCH00.0	B	EXCH01.0
	EXCH02.0	C	EXCH03.0
	EXCH04.0	D	grnd
	EXCH05.0	E	EXCH06.0
	EXCH07.0	F	EXCH08.0
	EXCH09.0	G	EXCH10.0
	EXCH11.0	H	EXCH12.0
X Connector	EXCH13.0	I	EXCH14.0
	EXCH15.0	J	grnd
	EXCH16.0	K	EXCH17.0
	EXCH18.0	L	EXCH19.0
	EXCH20.0	M	EXCH21.0
	EXCH22.0	N	EXCH23.0
	IR-EXCH0	P	
	4MS....0	Q	grnd
	4MS.....	R	
	32US...0	S	CL6....0
	1024US.0	T	
		U	
		V	
	SCPM...0	W	grnd
		X	
		Y	
	-12v...0	Z	STOCR...
		A	-12v....
		B	IOS....0
		C	CLRB...0
		D	grnd
	DSCP2..0	E	RC.....0
		F	CA.....0
	.....	G	SR.....0
	CA.....0	H	
Y Connector	CA/....0	I	PWRON..0
	DSCPL..0	J	grnd
		K	
		L	+12V...0
		M	SCCL...0
	CSPB...0	N	TESTER.0
	CRRLB..0	P	CCLB...0
	CRELB..0	Q	grnd
	CR12B..0	R	CR11B..0
	CROB...0	S	CRIB...0
	CR2B...0	T	CR3B...0
	CR4B...0	U	CR5B...0
	CR6B...0	V	CR7B...0
	CR8B...0	W	grnd
	CR9B...0	X	
		Y	
	.....-2V	Z	-2V.....

INTRODUCTION

This section provides information to install and check out an 80 Column Card Reader Control.

LOGIC PREPARATION

The processor communicates with an I/O Control by addressing the controls unique channel number. During a service request by a control the channel number is used to determine priority in the event two or more controls need service. Priority is determined by high order first. Channel number for a particular device will vary depending on system configuration.

CHANNEL NUMBER ADJUSTMENT

Jumper chip A9 should be wired to reflect the desired Card Reader channel number. Refer to I/O Base Section VI for typical system channel numbers and an example for wiring the jumper chip.

PHYSICAL INSTALLATION

The Card Reader Control Card will be installed in the I/O Base and cabled to the I/O Adapter Panel. The B9115/B9116 should be placed on a small table in close proximity to the other devices. Do not place the B9115/B9116 on the B9480 Disk Drive. The Card Reader is cabled to the I/O Adapter Panel.

CARD LOADING

The Card Reader Control Card is installed in a one card control slot or slot 1 of a two card control position. Refer to the I/O Base Section VI for definitions of the control slots.

CABLING

CONTROL TO I/O ADAPTER PANEL CABLING

Route the Card Reader Control Adapter cable from frontplane connector Y on the Card Reader Control Card to the I/O Adapter Panel. This ribbon cable should come down from the Control Card into the spring holder. Route left using the holder to contain the cable. Tie into bundle of other ribbon cables going to the adapter panel and route along side of these cables. Install the 50 pin Amp connector into the I/O Adapter Panel.

PERIPHERAL TO I/O ADAPTER PANEL CABLING

The Card Reader cable plugs into the I/O card inside the Card Reader. The card location is AABA6. The connector is installed with pin 1 to the top of the I/O Card.

To install the cable to the I/O card, remove the two L shaped cable brackets from the logic gate frame, install the cable and reinstall the two brackets to secure the cable to the I/O card.

The signal cable routes through the access hole in the rear of the machine adjacent to the power cord. Drop cable down to floor and route behind other devices. Bring cable into the console table through the trough at the end of the table. Route up to the I/O Adapter Panel and plug into the 50 pin receptacle. Coil extra cable length up and tie neatly.

ELECTRICAL INSTALLATION

AC POWER

Route the Card Reader AC cord alongside the previously laid Data cable. Insert through trough at the end of the table and plug into a standard power receptacle on the AC Power Distribution Assembly. Note that the Card Reader AC cable may not be long enough to reach depending on where the Card Reader is positioned. If this is the case use a 3 prong extender cord. Plugging into the system power prevents ground loops.

PERIPHERAL/CONTROL CHECKOUT

Upon completion of the Card Reader installation, run the confidence routine to assure proper operation.