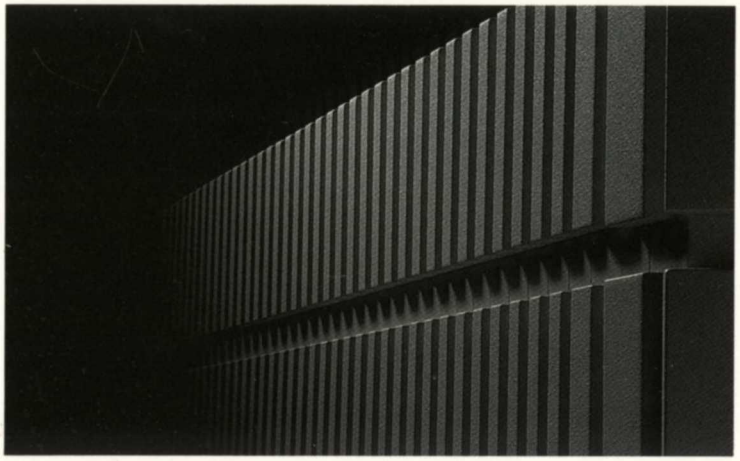
BiiN 20™ System
Technical Overview



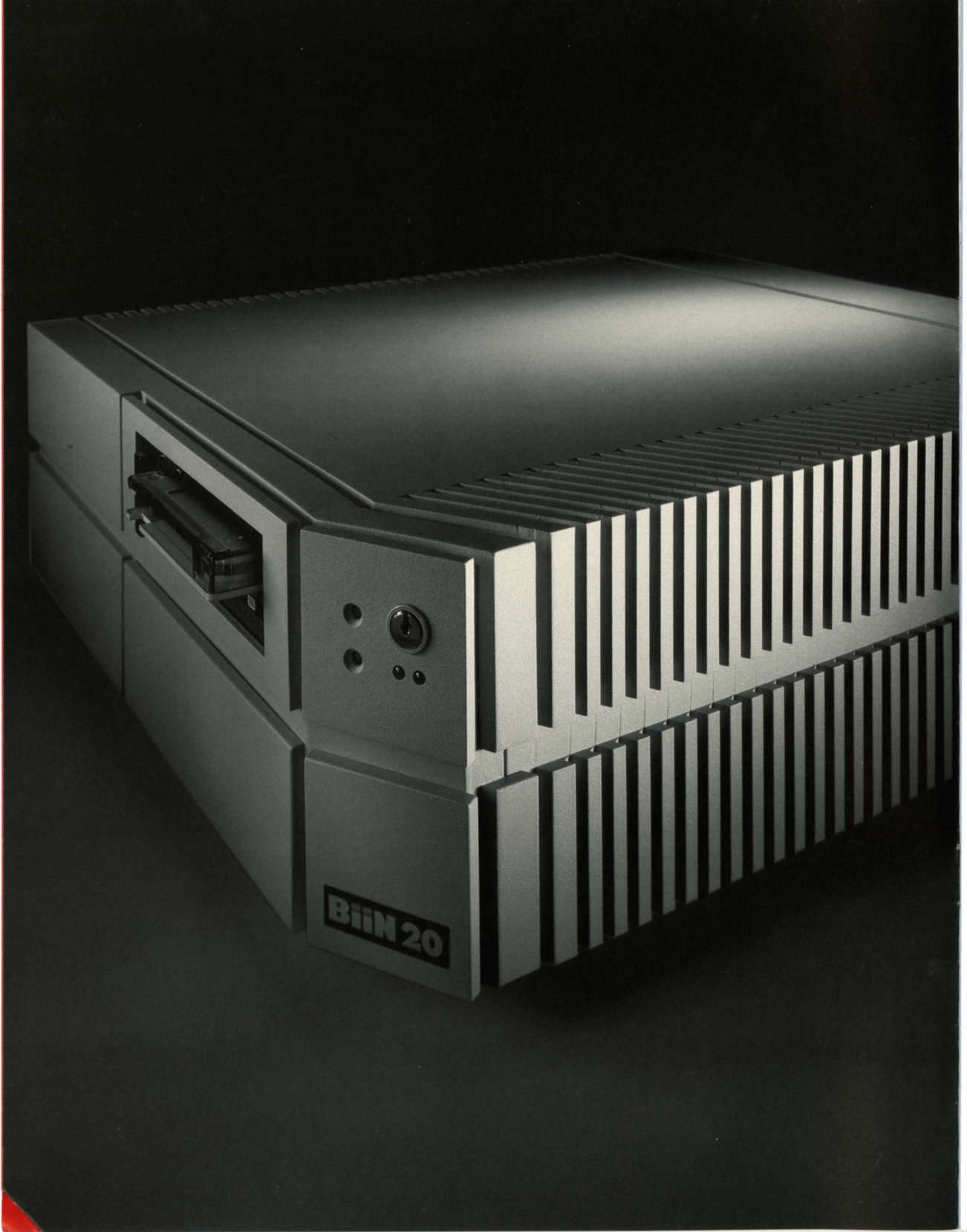
BiiN™

BiiN 20™ System Technical Overview

The BiiN 20™ system, the entry-level member of the BiiN family of computers, combines high performance and cost-effective processing in a desktop package, with upward software compatibility to any BiiN system. The BiiN 20™ system provides the choice of one or two-processor capability. I/O channels and memory capacity are easily expandable. By adding peripheral extension boxes, total disk mass storage capacities of over 1.7G bytes per disk channel are available. All configuration changes are completely transparent to users.

- **Hardware-Implemented Symmetric Multiprocessing:** The two processors access a common memory and automatically share a common workload for higher throughput.
- **Stable-Store Memory for High-Performance Transaction Processing:** Highly reliable battery-backed memory is used as a file cache to reduce both disk reads and writes.
- **Fine-Grained Protection for Security and Reliability:** VLSI-implemented object addressing promotes increased security and software reliability without sacrificing performance.
- **Expandable High-Speed I/O:** Specially designed intelligent channel processor is capable of transfer rates of up to 32M bytes per second and handles a variety of peripherals and communication interfaces.
- **Adherence to Industry Standards:** The BiiN 20™ system conforms to industry-recognized standards to connect to commonly available peripheral devices.
- **Software Compatibility:** Application programs can be run on any BiiN system without recompilation or relinking.

The BiiN 20™ system uses the extensible, multi-user, multitasking BiiN™ Operating System (BiiN/OS™) executive to provide reliable multiprocessing and secure distributed computing. The BiiN 20™ system provides a complete software support environment for fast program development, including five high-level languages, a complete set of programming tools, and a powerful relational database.



Symmetric Multiprocessing Architecture Provides Scalability

The processors and I/O channels directly access a common shared memory for powerful symmetric multiprocessing. Memory, I/O, and processing power are all extensible simply by adding the appropriate boards to the BiiN 20. This approach requires no software changes or complex system performance analysis and tuning as the number of processors changes. In addition, concurrent programming is made easier and more efficient by using shared memory.

To achieve efficient symmetric multiprocessing and concurrent programming, key facilities were designed into the VLSI processor and BiiN/OS. The processor implements low-level scheduling functions based on parameters set by the high-level BiiN/OS scheduler. Interprocess synchronization and communication are integrated with the processor scheduling, so that the processor can block one process and schedule another without BiiN/OS intervention. All processors in the computer share a queue of ready-to-run processes to automatically balance the workload.

Other features of the BiiN architecture include floating-point processing, independent I/O processing, and high data integrity. Fine-grained protection and reliability are achieved through an object-addressing mechanism that allow software modules to be grouped into a protected address space, accessible only through defined interfaces.

VLSI-Based Modules Offer Wide Range of Performance and Capabilities

The BiiN architecture divides the system into three basic modules: processor, memory, and I/O, as shown in Figure 1. To minimize space, the BiiN 20 processor board combines the processor and I/O processor modules. Additional memory and I/O capabilities are also provided by dedicated boards. The boards can be configured in several ways to meet the individual requirements of particular applications.

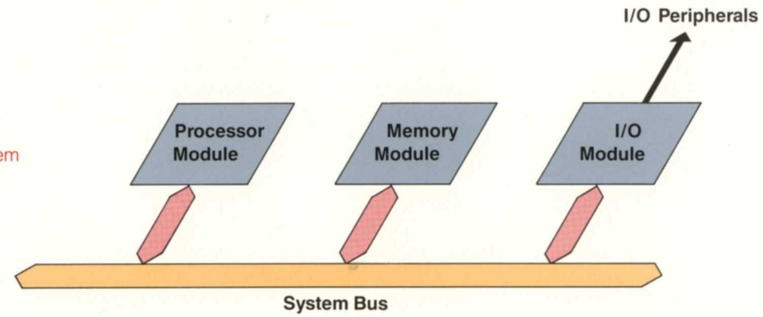


Figure 1: BiiN Modular, Extensible System Architecture

BiiN uses a comprehensive VLSI approach to build a balanced and modular computer architecture. BiiN implemented a separate VLSI component for each of the four functional blocks of a computer: processor, memory, bus, and I/O. The processor module uses the CPU for the computational engine and the Bus Exchange Unit (BXU) for the bus interface. The memory module uses the Memory Control Unit (MCU) for a memory controller and bus interface. The I/O module uses the Channel Processor (CP) as the I/O engine and the BXU for the bus interface. These components, specifically designed to implement the BiiN architecture, provide expansion of throughput by adding processor, memory, and I/O modules.

Implementing the BiiN architecture in VLSI reduces total chip count and interconnections to enhance system reliability. The BiiN 20 provides several functions that contribute to high reliability. These include a processor self-test, single-bit memory error correction (ECC), spare-bit replacement in memory arrays, and retry mechanism for bus errors.

High-Speed, Packetized System Bus Efficiently Handles Operations

The BiiN 20 employs an advanced bus to provide fast, efficient memory access for the processor and I/O modules. This synchronous, packetized bus contains 32 multiplexed address/data lines plus control lines, such as arbitration, clock and error signals. Designed to maximize throughput in a multiprocessing environment, the bus handles multiple requests from the processor and provides a message passing facility for processor-to-processor or processor-to-CP communications.

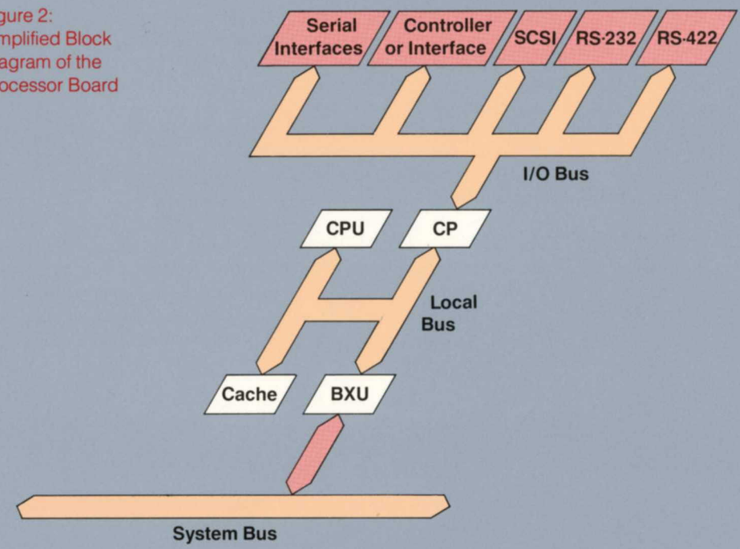
The bus provides an effective bandwidth of 40M bytes per second by implementing two techniques: burst transfers and packetizing. Burst transfers allow a packet from 1 to 16 bytes of information to be transferred in one bus transaction to minimize the number of memory accesses. Packetizing divides bus operations into request and reply packets to maximize bus usage. For example, the bus can handle another request while waiting for a reply from the previous request. The bus handles up to three outstanding request packets.

To provide high data integrity, the bus controllers perform parity checks on the data, address, and control signal transmissions. If a parity error is detected, the retry mechanism automatically performs the operation again.

High Performance Processor Board Features the Advanced 32-bit CPU, High-Speed Cache, and I/O Functionality

The BiiN 20 processor board combines the processor and I/O processor modules, as shown in Figure 2. The processor module performs all the computational and data processing tasks for the system and represents an independent processing unit that shares the system's computational load and system memory. The I/O processor module allows a variety of standard peripherals to connect to the system bus. The BiiN 20 can provide more I/O capabilities with the addition of an I/O processor board.

Figure 2: Simplified Block Diagram of the Processor Board



The advanced 32-bit BiiN CPU is the heart of the processor module. It incorporates not only many Reduced Instruction Set Computer (RISC) principles for computational performance, but also key data processing capabilities found in established architectures. The key data processing capabilities include the ability to access operands on any byte boundary and instructions for block data movement. To minimize component count and maximize performance, the CPU implements virtual address translation, floating-point operations, and a 512-byte instruction cache. The physical address space of the CPU is 4G bytes, and the virtual address space is 2^{58} bytes.

The CPU incorporates several performance features that are typical of RISC architectures, such as a large register set (16 local, 16 global, and four 80-bit floating-point registers) and an on-chip register cache that stores four sets of local registers for implementing a high-performance subprogram call/return mechanism. When memory access is necessary, the CPU can perform burst transactions that access up to four data words, with one word transferred per system clock cycle.

The CPU employs several other design techniques to enhance performance. The CPU overlaps memory accesses with computational operations using two mechanisms: write buffering and register scoreboarding. Write buffering allows a STORE instruction to complete execution as soon as the operand is transferred to the on-chip write buffer. Register scoreboarding permits instruction execution to continue while data is being fetched. These two mechanisms reduce the effect of memory latency and optimize execution speed. In addition, the CPU uses simple instruction formats to speed decoding of instructions. Many frequently used instructions are executed during single clock cycles, permitting maximum processor speed.

The BiiN CPU Takes a Step Beyond RISC

The BiiN CPU takes a step beyond RISC and traditional architectures by providing support for system functions, such as symmetric multiprocessing, object-oriented computing, and multitasking. Although many computer systems support symmetric multiprocessing, only the BiiN CPU embeds operating system mechanisms in VLSI to increase the efficiency and throughput of a multiprocessor system. Similarly, the BiiN CPU implements object addressing as the enabling technology for making BiiN/OS extensible, reliable, and secure, without sacrificing performance.

Processor Board Includes Write-Through Cache Memory and I/O Functionality

The processor module includes a write-through cache memory for intermediate storage of data and code fetched from system memory. The BXU contains the cache interface circuitry and maintains complete data coherency among caches on other processor boards. With cache memory, system throughput is enhanced by minimizing accesses to the system bus. The BXU also transfers information between the local bus of the CPU and the system bus, handles the system bus arbitration, and provides interprocessor communication and control.

The I/O portion of the processor board contains a CP (more details in the I/O Module section) and provides connections to I/O devices. It contains one RS-422 interface, one RS-232 interface, and one SCSI adapter for connections to peripherals. In addition, the board provides connections to BiiN controllers/interfaces and BiiN serial interface cards. For example, one of the following adapters, controllers, or interfaces and one of the following serial interfaces can be selected:

Adapters/Controllers/Interfaces

- ICA-30 Two-Line High Speed RS-422 Interface
- ICA-40 Ethernet/802.3 Controller

Serial Interfaces

- CSI-10 Four-Line RS-232 Interface
- CSI-20 Two-Line RS-232 and Two-Line RS-422 Interfaces
- CSI-30 Four-Line 20mA Current Loop Interface

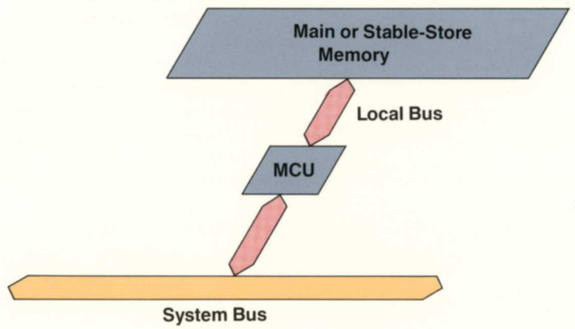
Memory Module Provides Reliable Operation with ECC and Spare-Bit Replacement

The BiiN 20 can accommodate multiple memory modules that can be added as needed for up to 32M bytes of total system memory. Each memory module has the following features:

- 8 or 16M bytes of random-access memory per module (with the capability to expand to 32M and 64M bytes with 4M-bit DRAMs)
- Built-in ECC on both data and address lines
- Diagnostic facilities that check ECC logic
- Spare-bit feature for on-line replacement of a failed DRAM component

One memory module is contained on one BiiN 20 memory board, as shown in Figure 3. The MCU controls the memory array, performs ECC, supports memory scrubbing, transfers information between memory and the system bus, and handles the system bus arbitration. Two memory boards can be combined to provide more system memory.

Figure 3:
Simplified Block Diagram of the Memory Board



File Cache Using Stable-Store Memory is the Key for High-Speed Transaction Processing

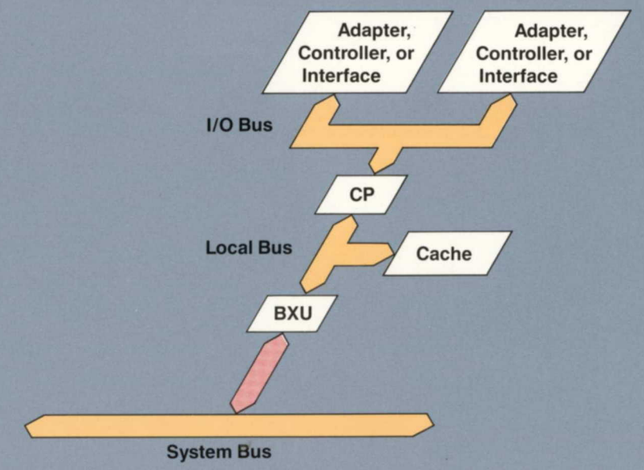
Up to 16M bytes of available memory can be used for stable-store memory, with the capability to expand to 64M bytes when 4M-bit DRAMs are available. Stable-store memory consists of highly reliable battery-backed memory that retains its contents in the event of a power failure or system crash. The stable-store memory is highly reliable due to a high-function memory controller integrated in the MCU, ECC checking, support for memory scrubbing, spare-bit replacement, and battery backup.

BiiN/OS uses stable-store memory to implement a file cache, which is the key mechanism for high-speed transaction processing. Other operating systems and database management systems implement a file cache with regular memory to reduce reads to disk. Since the BiiN file cache uses stable-store memory, BiiN/OS can—in addition to reducing disk reads—postpone and eliminate disk writes. Consequently, stable-store memory increases throughput by removing the disk as the I/O bottleneck.

I/O Processor Module Contains Intelligent Channel Processor for High Throughput

The I/O processor module allows a variety of standard peripherals to connect to the system, as shown in Figure 4. Operating independently, it performs complex I/O tasks without the need for constant direction from the processor module.

Figure 4:
Simplified Block Diagram of I/O Processor Board



The CP, a fully programmable device specially designed for communications and I/O, is capable of transfer rates of up to 32M bytes per second. Even more important, the CP can handle eight I/O tasks concurrently, even if each of the tasks requires a different I/O protocol. This feature allows the CP to move data quickly and efficiently between memory and a variety of peripheral devices. The CP contains a 512-byte register file for buffering data transfers and responds to interrupts with a worst-case latency of 250 nanoseconds. The CP communicates with the CPU using shared memory and interrupt messages.

The BXUs provide the interface to the system bus. To maintain a high data transfer rate, the BXUs can prefetch 32 bytes of data ahead of the CP and store it in an on-chip buffer. Thus, device underruns are effectively eliminated, even when the system bus is heavily utilized. Write-buffering in the BXUs provide the corresponding support and benefit for input data transfers.

The I/O processor board provides access for up to two connections to various adapters, controllers, and interface cards that mount on top of the I/O processor board. These cards offer a host of I/O capabilities, including standard interfaces for mass storage, communications, and networks. These interfaces support a variety of peripheral devices, such as disk drives, tape drives, terminals, modems, and printers.

The various adapters or controllers include the following:

Model Number	Description
ICA-20	Small Computer System Interface (SCSI) Adapter
ICA-30	Two-Line High-Speed RS-422 Interface with the capability of transmitting data at a rate of 1M bits per second.
ICA-40	Ethernet*/802.3 Controller

Initial Confidence Tests and On-Line Diagnostics Contribute to High Reliability

All systems include power-up diagnostics to detect potential problems before they occur. When a BiiN 20 is turned on, the CPU performs a self-test and a core integrity test. Next, basic confidence tests are run on all key system components, including the boot path, memory, cache, stable-store memory, system bus, I/O devices, and processors. Upon successful completion of the confidence tests, the system automatically initializes the VLSI components and builds a configuration table that records pertinent information, such as the number and types of boards and slot locations. If the initial confidence test identifies a faulty VLSI component, the component is removed from operation and the system is reconfigured, all within milliseconds.

The BiiN 20 supports on-line diagnostic tests that operate under BiiN/OS. The on-line diagnostic test consists of application-level programs that allow users to examine the status of system hardware, initiate utility programs to test specific configurations, and run diagnostic test programs. The on-line diagnostics provide high flexibility; they can be run in parallel to apply maximum stress, or be run serially to focus on a specific area, or be run using a combination of both.

Open System Standards Assure Interoperability

Adherence to industry standards allows the BiiN 20 to be easily connected to commonly available peripheral devices. The industry-recognized standards compatible with the BiiN 20 are shown in Table 1.

Table 1. List of Standards

Standard	Interface
ANSI	X3.131-1986 (SCSI)
EIA	RS-232-C, RS-449/422
CCITT	X.21, X.24/X.27, and X.150 V.21, V.22, V.22bis, V.23, V.24/V.28, V.25bis, V.26, V.26bis, V.26ter, V.27, V.27bis, V.27ter, V.29, V.32, and V.54
IEEE	802.3 LAN, (Ethernet Blue Book Version 2.0 LAN), 754 (Floating Point)
DoD	TCP/IP, FTP, TELNET, SMTP
SNA	3270, 3770, and LU 6.2, LU 0,1,2,3
ISO	Transport Class 4, FTAM, X.25

BiiN 20 Versatile Configurations Easily Expanded

The BiiN 20 offers versatile configurations that can be tailored to any application need in terms of processor, memory, or I/O requirements. For simplification, BiiN offers base system configurations, as shown in Table 2. These systems vary primarily in processor capability, with the 20/10 system using one processor and the 20/20 system using two processors. Each system supports up to 6 direct serial connections; one connection supports a high-speed RS-422 interface and five connections support an RS-232 interface.

Table 2. BiiN 20 Base System Configurations

Configuration	20/10	20/20
CPUs	1	2
Memory	16MB	16MB
Mass Storage		
Total Formatted Capacity	180MB	180MB
Number of Fixed-Disk Drives	1	1
Cartridge Tape	125/150MB	125/150MB
Communication Devices		
Ethernet/802.3	Yes	Yes
Serial Communication Interfaces	6	6

Related Products and Upgrade Kits Allow the BiiN 20 to Expand as the Applications Grow

Modular and incrementally expandable, the BiiN 20 offers many options that customize the system to specific requirements, as shown in Table 3. Mass storage can be expanded by connecting peripheral extension boxes; each SCSI adapter on the processor or I/O processor board supports up to seven SCSI peripherals. Each peripheral extension box accommodates up to two 320M-Bytes (formatted capacity) fixed-disk drives.

The one-processor BiiN 20 can easily be upgraded to two processors with the performance upgrade kit. Performance upgrade kits require no application software conversions, or costly reprogramming.

Table 3: The BiiN 20 Related Products

Add-In Boards	MEM-21 8M-Byte Main Memory Board
	MEM-22 16M-Byte Main Memory Board
	IOP-20 I/O Processor Board
I/O Adapters, Controllers, and Interfaces	ICA-20 SCSI Adapter
	ICA-30 Two-Line High-Speed RS-422 Interface
	ICA-40 Ethernet/802.3 Controller
Serial Interface	CSI-10 Four-Line RS-232 Interface
	CSI-20 Two-Line RS-232 and Two-Line RS-422 Interface
	CSI-30 20mA Current Loop Interface
Mass Storage (formatted capacity)	FDF-10 180M-Byte Fixed-Disk Drive
	CTU-10 125/150M-Byte Cartridge Tape Drive
Expanded Mass Storage (formatted capacity)	FDF-20 320M-Byte Fixed-Disk Drive
	EXB-20 Peripheral Extension Box
Upgrade Kit	PUG-22 One to Two Processors Upgrade Kit

The Extensible BiiN Operating System Provides Open Software Interface

To take full advantage of the hardware features, all BiiN systems offer the advanced BiiN/OS. This operating system features multi-user and multitasking operation; transaction processing support; flexible object-based protection of software modules; transparent distribution of operating system resources among system nodes; record structured files with multiple indexes; extensive communications support; and both a window-style user interface and a POSIX interface. Additional system support is provided by means of a database management system; a full complement of languages (including Ada, C, COBOL, FORTRAN, and Pascal); and a complete program development environment. Because of the modularity of the BiiN 20, software developed on any model within the family is transparently transferable to any other system in the family.

For more information, in North America call 1-800-252-BiiN. In Oregon call (503) 696-4800. In Europe, call (49) 911 5219 0. Or write BiiN, 2111 NE 25th Avenue, Hillsboro, Oregon 97124-5961.

BiiN 20 System Specification Summary

Table 4: The BiiN 20 Specifications

Category	Parameter	Specification
CPU	Cycle Time	62.5 ns
	32-Bit Registers	32
	80-Bit Registers	4
	Register Cache	4 sets of 16 32-bit Local Registers
	Instruction Cache	512 Bytes
	Linear Address Space	4G Bytes
	Virtual Address Space	2^{58} Bytes
	Multiplexed Address/Data Lines	32 plus a tag bit
	Floating Point Unit	IEEE 754 Standard
System Bus	Address/Data Lines	32 plus a tag bit
	Packet Size	1 to 16 Bytes
	Effective Bandwidth	40M Bytes per Second
	Parity Lines	2 per Word
	Bus Arbitration	Parallel, Overlapped
Memory	Total Capacity	32M Bytes
	Maximum Number of Boards	2
Mass Storage	System Chassis Capacity (One SCSI Disk Drive)	180M Bytes (Formatted)
	EXB-20 Peripheral Extension Box Capacity	640M Bytes (Formatted)
	Maximum Number of SCSI Disk Drives in the EXB-20	2
	Maximum Number of SCSI peripherals per SCSI bus	7 per processor or IOP-20 I/O Processor board
Communications	Terminal Connectivity	Up to 6 direct-connect serial lines. More available through Ethernet.
	Ethernet/802.3	Up to 2 Controllers
	High-Speed RS-422	Up to 4 Lines
Electrical	Voltage	110 VAC to 220 VAC
	Frequency	47 Hz to 63 Hz
	Maximum Power Consumption	320 Watts
	External Battery Input	8 VDC
Environment	Operating Temperature	10° to 35° C
	Non-Operating Temperature	–20° to 50° C
	Relative Humidity	20% to 80% (non-condensing)
System Enclosure	Size	5.5 inches (14 cm) high 17.5 inches (44.5 cm) wide 19.1 inches (48.6 cm) deep

Documentation

For more information on the BiiN 20, refer to the following manuals:

Getting Started with BiiN Systems
BiiN Hardware Subsystems Reference Manual
BiiN Hardware System Description
BiiN Diagnostics User's Guide
BiiN System Overview
BiiN Command Language Executive Guide
BiiN Commands Reference Manual
BiiN Operating System User's Guide
BiiN Operating System Reference Manual

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