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ABSTRACT and CONTENTS

All relationships between the ITP and other objects in the world are described.

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I. Introduction

The integral test processor (ITP) has the following interfaces with objects other than itself.

1) It shares a microprocessor with the microscheduler.

2) The microprocessor can be initialized by pushing some button. This operation clears the 0 register and sets BREAK to Ø.

3) The ITP has access to the main memory of the Ml.

4) The ITP can read or write the following devices of general interest to the system. In all cases, 24 bits are transferred between the microprocessor and the device using ALERT/POT/PIN.

R	System Switch Register and System Contol Register
W	System Lights and System Loadable Register
R	5 System Warning Registers

5) The ITP can read or write the following devices local to itself using ALERT/POT/PIN.

R	Flag Register
R	Teletype Input
R	Paper Tape Input
W	Teletype Output

More such devices may be added.

6) The ITP can send or receive STROBE and set or clear PROTECT like any other microprocessor.

7) The ITP can set the STEP and PROCEED flip-flops in both CPU's.

8) At times the microprocessor debugging logic may be connected. This is of interest to the processor as a whole and not particularly to the ITP.

Subsequent sections expand on each of these points.

II. Relations with the Microscheduler

The microscheduler (US) and the ITP share a microprocessor which will be called the microscheduler and test processor (UTP). The microcode in UTP divides its attention between US and ITP according to the following rules. The UTP has two non-exclusive modes.

<u>compute</u> mode, in which ITP instructions are executed

<u>schedule</u> mode, in which US requests are processed

Each mode may have one of three values: off, waiting, and on. When a mode is off, no activity involving that mode will take place unless it is turned on, either by an explicit instruction or request or by the system switches. When a mode is on, work is done. Schedule mode has priority so that whenever schedule mode is on the UTP will run in the US until all requests have been processed, and all scheduling done, at which time schedule mode will become waiting. STROBE sends schedule mode from waiting to on. When compute mode is on, UTP executes ITP instructions (except when temporarily diverted by schedule mode coming on.) UTP I/O can proceed, provided compute mode is not off. The occurrence of an I/O interrupt sends compute mode from waiting to on. The system failure (STROBE 2) latch forces compute mode on, as described in MPREC/W-30.

The possible changes in the values of modes are mentioned at appropriate points in this document and are summarized in Appendix I.

The values of modes are recorded in the MODE word as specified in Appendix I.

When the ITP sets a PROTECT, schedule mode is saved in the SSM bit and turned off. It is restored when the PROTECT is cleared. For this reason it is wise to set SSM when turning on schedule mode, to defend against accidental UNPROTECT's in the ITP.

III. Initialization

Initialization occurs when the O register is set to zero. When this happens the UTP proceeds as follows:

First test BREAK, which is set by the TP-driven breakpoint feature. If it is on, clear it and dump the state into core at location USSAVE in the format described in Appendix II. Then wait for location USBRKWAIT to become non-zero, reload the state and send control to the location found in USBRKADR. This procedure is designed to facilitate debugging of UTP and its microcode from an external test processor, which can set a break-point register which will set BREAK and initialize the UTP whenever the O register matches the breakpoint register.

If BREAK is off, this is a real initialization and not a break. Read the system control register (SCR). The bits of this register are listed in Appendix III and the correspondence between the names used here and numbers is given. The following steps are taken:

1) Test SELF-FILL. If off, go to step 2. Otherwise, set location ITPREL to the value INITREL and ITPBND to INITBND. Read paper tape until a non-blank frame is read. Pass over this frame. Then read 100B groups of 4 characters from the paper tape reader. Check each character for odd parity. Assemble the six low-order bits of the four characters into one 24-bit word:

Character in 4-Character group	Bits of Word
1	Ø - 5
2	6 - 11
3	12 - 17
4	18 - 23

Store the words in successive memory locations, starting at INITREL and ending at INITREL + 77B. Go to step 3. If a parity error or reader malfunction is detected, display the current reader input word in the lights, stop the reader and hang. Otherwise do not stop the reader.

2) Test COMPUTE. If off, go to step 4.

3) Turn off schedule mode. Then perform the ITP RESET sequence described below.

4) If we get to here, the ITP is not involved in the initialization, and compute mode is turned off. If CONTINUE is off, go to step 7.

5) This is a CPU-initiated restart. Read SCRMEM. Go to step 7 if CONTINUE is off in this word.

6) The CPU wanted the restart to take place without manual intervention. Go to step 9.

7) The restart is supposed to be controlled by SCR (either CONTINUE was off in SCR, meaning that the STOP button was pushed, or it was off in SCRMEM, meaning that the CPU intended to give control to the switches when it initiated the restart). Read SCR and loop until GO is on.

8) Store SCR in SCRMEM.

9) SCRMEM is now set up correctly for the other microprocessor to interpret. Send STROBE to AMC and CHIO. Wait for STROBE. Load state from SAVE area as is done after a break.

IV. RESET Sequence for ITP

the RESET sequence may be initiated by initialization of the UTP with COMPUTE or SELF-FILL set in SCR, by the failure level becoming high, or by a US request to start the ITP. It proceeds as follows:

1) Load the ITP's relocation register REL from location ITPREL.
2) Load the ITP's bounds register BOUND with max (4000B, contents of ITPBND).
3) Clear IOCTL.
4) Store P in relative 2 (i.e. 2 + REL).
5) Set P to 3
6) Turn compute mode on and start executing instructions in the usual way.

V. Memory References

The ITP program can make two kinds of references to the central memory of the M1. A relative reference is made at all times except when the address R to be used for the reference is the result of an indirection with the sign bit of the indirect word set. It references location R + REL. In this case R is never >37777B. If the instruction is a store, R<BOUND must also hold; if not, a trap occurs.

An absolute reference is the result of an indirection through a word with the sign bit set. In this case the effective address is

```
IAW (6-23)   if IAW (1) = Ø      (IAW is the
IAW (6-23)+X(6-23) if IAW(1) = 1  contents of the
                                  indirect word)
```

The whole central memory can be addressed absolutely in this way, and there are no restrictions on stores.

VI. POT/PIN

The ITP has access to the microprocessor ALERT/POT/PIN functions via two instructions which are implemented as follows:

```
    UPIN:    Z ← AR, ALERT
             PIN, Z ← E2, VCY;
             BR ← Z;
```

This instruction does an ALERT with A as argument and then PINs a word into B.

```
        UPOT:    Z ← AR, ALERT;
                 Z ← BR, POT;
```

This instruction does an ALERT with A as argument and then POTs a word from B. By using suitable device addresses, the ITP program can diddle all the registers. Note that the program may not assume that no ALERTs are given between program instructions, since an ALERT to read the flag register is part of instruction preparation. Nor may it assume that only a short time will elapse between instruction executions, unless schedule mode is off, since there are some US functions which may consume several milliseconds.

VII. System Registers

The UTP has access to nine system reigsters. These are:

Address	POT or PIN		Name
USRADR	PIN	SWR1	System warning register 1
USRADR+1	PIN	SWR2	System warning register 2
USRADR+2	PIN	SWR3	System warning register 3
USRADR+3	PIN	SWR4	System warning register 4
USRADR+4	PIN	SWR5	System warning register 5
USRADR+5	PIN	SSR	System switch register
USRADR+6	PIN	SCR	System control register
USRADR+7	POT	SLR	System loadable register
USRADR+8	POT	SSL	System sense lights

SSR and SWRS are stored in core, and SSL loaded from core, using locations SSRMEM, SWRSMEM and SSLMEM, about once every millisecond whenever schedule mode is not off. They are also directly accessible to the ITP program via POT/PIN.

VIII. ITP Input/Output

The input/output system for the ITP consists of a flag register and up to 23 devices, together with a word in the state called the input/output control word (IOCTL) which can be set by the program. For each bit in the flag register there is a corresponding device and an input/output pointer word and interrupt word. If the corresponding bit in IOCTL is set, the device is said to be enabled, if reset, disabled. For bit 23-i the pointer is at (relative) IOPTR+i, the interrupt word at IOINT+i+2.

On every instruction cycle if compute mode is on, and periodically when compute mode is waiting, the I/O system reads the flag register F and computes F AND IOCTL. It then scans this word, starting with bit 23, for a non-zero bit. If one is found, say bit i, I/O is done to that device. The exact procedure differs for input and output. Bit 2 of the pointer word determines which is to be done; it is set for output devices.

On input, a data word is read from the device and stored at the (relative) address given by $(\text{IOPTR+i})_{10-23}$. Then (IOPRT+i) is incremented unless bit Ø is set. Store protect is checked for the store.

On output, a word W is fetched from the (relative) address given by $(\text{IOPTR+i})_{10-23}$. If $(\text{IOPTR+i})_{1}=1$ and W=(IOPTR+i)+1, the IOCTL bit for the device is turned off and no output is done, i.e. this bit pattern serves as an end-of-buffer marker. Otherwise W is output to the device. (IOPTR+i) is incremented unless bit Ø is set, regardless of whether end of buffer is encountered.

After either input or output, $(\text{IOPTR+i})_{3}$ is checked. If it is on, a BRM* IOINT+i+2 is executed. This may change compute mode from waiting to on.

The flag register bits assigned so far are:

Bit	Device	POT/PIN Address
23	Paper tape reader	4B7+1
22	Teletype receiver	4B7+2
21	Teletype transmitter	4B7+4

The address of a device for UPOT or UPIN is a word which has all bits Ø except the sign bit and the device's flag register bit, which must be 1. The address of the flag register is 4B7.

Details on the format of data words for devices may be found in MSIOI/S-15.

IX. Microprocessor Communication

The ITP has an instruction, UPS, which can be used to send STROBEs and manipulate the protect system. It has three flavors:

STR: Send Q as a STROBE

PRO: Set the protects selected by Q. Turn off schedule mode, copying it into the saved schedule mode bit in MODE

UPR: Clear all protects and restore schedule mode from the saved bit.

APPENDIX I: Changes in UTP Modes

The mode word format is:

Bit	Content
Ø	Compute mode on
1	Compute mode waiting
2	Schedule mode on or waiting
3	Saved schedule mode bit

The possible transitions are

Mode	On	Wait	Off
Compute	Initialize UTP and self-fill or compute switch on Failure latch From wait on I/O interrupt		Initialize UTP and self-fill and compute switches off
Schedule	Initialize UTP and self-fill and compute switches off.		Initialize UTP, self-fill or compute switch on.
	From wait on STROBE From off when ITP unprotects and MODE [3] = 1	From on after work is done	From on when ITP protects

In addition, modes can be set arbitrarily by the ITP's XCA instruction or by the US's SETMODE request.

APPENDIX II: Format of USSAVE Area

The UTP saves its state in the following format starting at USSAVE when it breaks:

M

SK1 to SK31

RØ to R6

OS

Z

Q

APPENDIX III: Bits in System Control Register

Bit	Contents
Ø	GO
1	CONTINUE
2	Disk Start
3	Restart (if bit 2=1)
4-8	Starting address for disk save and system load area
9-21	Unused
22	COMPUTE
23	SELF-FILL

APPENDIX IV: Miscellaneous Parameters

Note: The formal authority for the assignment of absolute core locations is SYSP/W-15.

ITPREL	306B	INITREL	10000B
ITPBND	307B	INITEND	40000B
SWRSMEM			
SSRMEM			
SSLMEM			
USSAVE			
IOPTR	10B		
IOINT	40B		