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ABSTRACT and CONTENTS

This document specifies the special functions and branch conditions in the Data Communications Computer.

Branch Conditions

Ø	Never branch
1	Always branch
2	X=Ø
3	X≠Ø
4	X<Ø
5	X≥Ø
6	X>Ø
7	Y≥Ø
1Ø	Y<Ø
11	RØ<Ø
12	RØ≥Ø
13	X≤Ø
14	X= -1
15	X≠ -1
16	Z≥Ø
17	Z<Ø
2Ø	Always branch
21	Y∧7≠Ø (Y(15)∨Y(14)∨Y(13)=1)
22	BL=Ø
23	BL≠Ø
24	Y(15)=Ø
25	Y(15)≠Ø

Branch Conditions - 2

26	Attention latch 1 = Ø (also resets the latch)	
27	Undecoded	
3Ø	Undecoded	
31	Undecoded	
32	Special flag A = Ø	
33	Special flag A ≠ Ø	
34	Attention latch 2 = Ø	Also resets the latch
35	Attention latch 3 = Ø	
36	Attention latch 1 ≠ Ø	
37	Undecoded	
4Ø	Undecoded	
41	Undecoded	
42	Local memory parity error = 1 (resets the latch)	
43	Undecoded	
44	Undecoded	
45	Undecoded	

Special Conditions

Ø	No activity
1	LCY 1
2	LCY 2
3	LCY 3
4	LCY 4
5	LCY 8
6	LCY 12
7	Undecoded
1Ø	LCYØ
11	LCL Z (CCFZA)
12	LCH Z (CCFZB)
13	SKZ - Reference scratchpad with address in Z (SPFZ)
14	ALERT
15	POT
16	PIN
17	Undecoded
2Ø	Undecoded
21	Unusable
22	Undecoded
23	Undecoded
24	Undecoded
25	Undecoded

Special Conditions - 2

26	Reset T.U. (or other device attached to I/O connector)	
27	Undecoded	
3Ø	Set special flag A	Occurs at end of instruction
31	Reset special flag A	
32	Undecoded	
33	Undecoded	
34	Undefined	
35	Undecoded	
36	Undecoded	
37	Undecoded	
4Ø	Store	Memory Reference
41	Store	
42	Store	
43	Store	
44	Fetch	
45	Fetch	
47	Fetch	
6Ø	Undecoded	
61	Undecoded	
62	Undecoded	
64	Fetch	Memory Reference
65	Fetch	

Undefined means that the signal is brought off the card in the low true sense to be used as a special function if needed or, in the case of branch conditions, an input to the branch condition gate is brought to a pin for use if needed.

Undecoded means that the condition is presently not wired on the board.

Unusable means to avoid conflict with the TP's, this function is not used in the Model 1.

There exist two Always Branch conditions to reduce the number of diodes in the MC5 bit in the ROM.

Attention Latches operate as follows: They are set at the end of the global cycle with K2. They are cleared at the end of the interval in which branch is tested, unless the set exists simultaneously, in which case the latch is set. This means if the latch was set, the branch was unsuccessful and attention was sent, the latch will still be set at the end of the branch instruction.

Special Flag A is set and cleared with special function at the end of state A or state B depending on whether or not VCY is set.

Parity error latches are set upon receipt of an error and cleared upon branching, like the attention latches.

ALERT, POT, and PIN are discussed in MPPI/S-16, "Microprocessor Pot/Pin Interface."