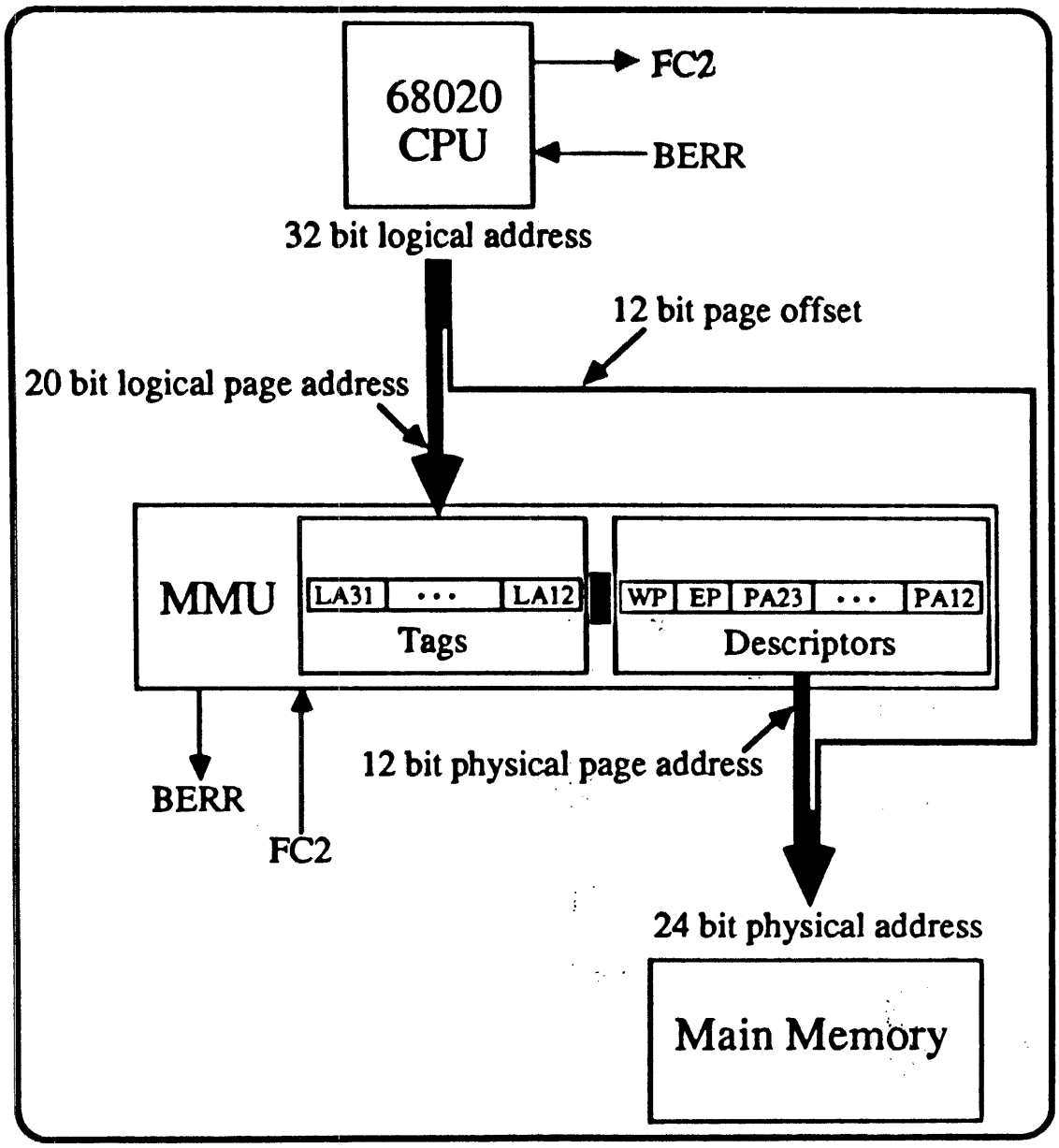
Introduction:

The Big Mac MMU is a memory management unit intended for use with the Motorola MC68020. The MMU features a 64 entry, fully associative cache that maps 4096 byte pages from the logical address bus of the MC68020 to the physical address bus of main memory. This allows a logical (virtual) memory space of 4 Gbytes; a maximum physical memory space of 16 Mbytes and a 256 Kbyte user working set. The MMU operates on the upper 20 bits of the logical address yielding the upper 12 bits of the phyical address. The lower 12 bits of the logical address bus are passed straight through to the physical address bus.



If the upper 20 bits of the logical address are contained in any of the 64 entries in the MMU, the upper 12 bits of the physical address are provided within 65ns. This permits the MMU to function without wait states. If the page is resident in the MMU, the access control bits associated with that page are also checked to see if write protection and or execute only protection is in effect.

If the upper 20 bits of the logical address are not contained in any of the 64 entries in the MMU, a Bus Error (BERR) signal will be asserted. This will suspend the execution of the instruction that caused the "miss", and system software can then load the MMU with the correct physical address of the page that caused the miss. The suspended instruction can then be restarted. If the logical address is contained in the MMU and a write protection or execute only protection violation is detected, a Bus Error is also generated.

Ten 16 bit status registers are implemented within the MMU to allow access to the following information: Page Accessed (status registers 0 through 3 for use in generating LRU info), Page Dirty (status registers 4 through 7), Exception Cause and MMU mode (status register 8) and Logical Address Latch (status register 9).

Operation:

Supervisor and user states are defined by the function code 2 bit (FC2) of the CPU (with FC2=1 --> supervisor and FC2=0 --> user).

The CPU and MMU combination operate with Supervisor state addresses always unmapped. User state can operate either mapped (by clearing the MODE bit in status register 8), or unmapped. The unmapped state is entered by setting the MODE bit in register 8. In the unmapped state the MMU presents logical address bits LA23 through LA12 directly to the physical address bits PA23 through PA12.

Independent of the mapping of User state, the registers of the MMU are accessible for reading or writing only from Supervisor state.

The registers LAR0 through LAR63 (located at byte offsets $00000 through $3F000) contain the logical addresses of the 64 pages to be mapped into the physical pages. The registers PAR0 through PAR63 (located at offsets $40000 through $7F000) contain the corresponding physical addresses and access protection bits. Setting WP = 1 will cause a

violation if a write is performed to the particular page. Setting EP =1 will cause a violation if anything other than a fetch (i.e. a read or write) is performed to the particular page.

Status registers 0 through 3 (located at byte offsets $80000 through $83000) contain the bits corresponding to page accesses made to the 64 physical pages defined by the physical address registers 0 through 64. Note the page addressed by PAR0 corresponds to bit 0 of status register 0 and the page addressed by PAR63 corresponds to bit 15 of status register 3. Any access to a physical memory page (while in mapped User state) will set the appropriate bit in the status registers 0 through 3. These status registers are intended for use by a Least Recently Used page replacement algorithm. (These registers can be periodically read by the CPU, any set bit increments its associated usage counter in main memory.) Writes to byte offset $80000 through $83000 can set and clear the bits in these registers individually, while a write operation to byte offset $84000 will clear all bits in status registers 0 through 3.

Status registers 4 through 7 (located at byte offsets $85000 through $88000) contain the bits corresponding to page writes made to the 64 physical pages defined by the physical address registers 0 through 63. Note the page addressed by PAR0 corresponds to bit 0 of status register 4 and the page addressed by PAR63 corresponds to bit 15 of status register 7. Any write to a physical memory page (while in mapped user state) will set the appropiate bit in these status registers 4 through 7. These status registers are intended for use in implementing a page replacement policy i.e. these registers reflect whether or not a page intended for replacement has been written to (ie. dirtied) since it was brought into mapped memory. Writes to byte offset $85000 through $88000 can set and clear the bits in these registers individually, while a write operation to byte offset $89000 will clear all bits in status registers 4 through 7.

Status register 8 (located at byte offset $8A000) contains the information necessary to determine the cause of an MMU exception; WP being set for violation of write protection and EP being set for violation of execute only protection (i.e. a write or a read that is not a fetch). It also contains the MMU mode bit and the index of the register that caused the access violation. The bits in the register are ordered to optimize the search for the exception cause by the use of the MC68020 BFFFO (bit field find first one) instruction. In the case of a translation miss, the cache address field will hold an undefined value. When the MMU mode bit is set to a 1, the MMU will be forced into the unmapped state, with the logical address bits LA23 through LA12 passed directly to the physical address

bits PA23 through PA12.

Status register 9 (located at byte offset $8B000) is the logical address latch which holds the logical address of the access violation. When a physical address register is written, the corresponding logical address register will be updated with the contents of the logical address latch.

Signal Summary:

Name	Type	Description
LA12-LA31	Input	Logical address used by the MMU for translation to physical addresses.
PA12-PA23	Output	Translated addresses
D12-D31 I/O	Data bus	
LAS	Input	Logical address strobe.
PAS	Output	Physical address strobe.
SIZE0,SIZE1	Input	Ignored by MMU.
DSACK0,DSACK1	Tristate	MMU drives both lines low when a status register is accessed.
PBR,PBG	Input	Ignored by MMU.
PBGACK	Input	When asserted the MMU will force all physical address and data outputs to tristate.
HALT	Input	Ignored by MMU.
RESET	Input	When asserted, forces the MMU into the unmapped mode.
DS	Input	Indicates valid data on data bus.
RMC	Input	Ignored by MMU.
CLK	Input	System clock.
BERR	Tristate	Driven low by the MMU when an exception occurs.
R/W	Input	Indicates read or write.
FC0,FC1,FC2	Input	CPU function codes (see MC68020 manual).
FC3	Input	Ignored by MMU.

BIG MAC MMU PROGRAMMER'S MODEL