1984 AppleBus File Server Interface

The 1984 File Server contains the following

- o 8MHz 68000 32 bit SuperMicroComputer
- o SCC Serial Communications Interface
- o 128K RAM
- o Interface to Apple Hard Disk Drive
- o Interface to Sony Floppy Disk Drive
- o Time of Day Clock

The Processor

A 8MHZ Motorola 68000 is used as the processor.

ROM

The File Server contains two sockets for two byte wide ROMS. These sockets will initially be configured for 2764 parts (16K bytes total), but may be configured for other ROMS.

ROM type	Total ROM size
2716	4K
2732	8K
2764	**16K**
27128	32K
27256	64K

Function	Address
ROM	000000-003FFF

RAM

The file server contains 128K bytes of parity RAM. This will be done by using 18 64K DRAM chips. An upgrade path for 1/2 Megabytes could will be provided for with the use of 256K DRAM parts.

Function	Address
RAM	FE0000-FFFFFF

Hard Disk I/O

The file server will have a hard disk interface. This interface is latches data and commands to be sent to the hard disk, as required by the Apple interface. All data read from from hard disk is read directly from the disk. The interface can be programmed to transfer data both with and without PSTRB. The interface also allows the control lines CRES, CMD/DATA, and R/W to be set by the software. In addition the line BSY, from the hard disk can be read directly, and optionally, used to generate an interrupt from. CRES is derived from the 68000's reset line.

Function	Address	
Data Port w/o PSTRB	200001	
Data Port w/ PSTRB	200003	
Read BSY	200005	Read
Reset CMD	200005	Write
Set CMD	200007	Write
Read PWM bit (diag)	200009	Read
Clear R/W	200009	Write
Read R/W bit	20000B	Read
Set R/W	20000B	Write
Read CMD bit	20000D	Read
Clear Disk Interrupt	20000D	Write

Sony Floppy Disk Drive

A Sony disc controller is provided. The controller contains an IWM chip to control the disk and transfer data. In addition, PWM circuitry is provided to control the speed of the Sony drive. This circuitry is almost identical to that of the Lisa 2. Refer to the IWM and Sony specifications for more detailed information.

Function	Address	
IWM chip accesses	40000x	
Re-sync PWM	100000	
SET SEL	20000F	READ
CLEAR SEL	20000F	WRITE

Time-of-Day Clock

The file server contains a MAC TOD clock chip to provide time and date information to the file server. The clock read accessed serially. Refer to the MAC clock chip specification for more information.

Function	Address	
Chip Enable	50000x	from SCC DTRB
Clock	50000x	from SCC enable
Data from Clock	50000x	to SCC DCDB
Data to Clock	20000x	from Par Port R/W

Serial Port I/O

The serial I/O is provided for by an SSC chip and misc logic. The two serial ports will look like the Lisa serial ports. One will contain additional control line for modems and the other will be a minimum port that can be used for AppleBus. Refer the the SSC and AppleBus specifications for more information.

Function	Address
SSC chip	50000x

Timer Interrupt

A 1 ms interrupt is provided in the File Server. This interrupt must be cleared in the interrupt handler by accessing the timer address.

Function	Address
Clear interrupt	300000

Address Summary

The addresses below are the address range for the following devices:

Device	Address	
ROM	000000 - 0FFFFF	
PWM	100000 - 1FFFFF	
ParPort	200000 - 2FFFFF	
Clear 1ms timer interrupt	300000 - 3FFFFF	
IWM	400000 - 4FFFFF	
SCC	500000 - 5FFFFF	
Reserved	600000 - 7FFFFF	
Clear Parity Error	800000 - BFFFFF	Read
RAM	C00000 - FFFFFF	

Note that many of the address spaces are very large and the specific device is repeated many times. In order to allow for compatibility of future systems alway address the lowest address set for each device, except for RAM, which starts at FFFFFF and goes down.

Interrupts

Device	Interrupt Level
NMI	7
Parity error	6
SCC	5
Par Port	4
Reseved	3
1 ms timer	2
Reseved	1