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TECHNICAL MANUAL FOR

DE-211/DE-291 DATA ELECTRONICS

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LIST OF EFFECTIVE PAGES

All pages are original through revision D, except for pages 5-1 through 5-26, which are revision E pages.

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF TABLES

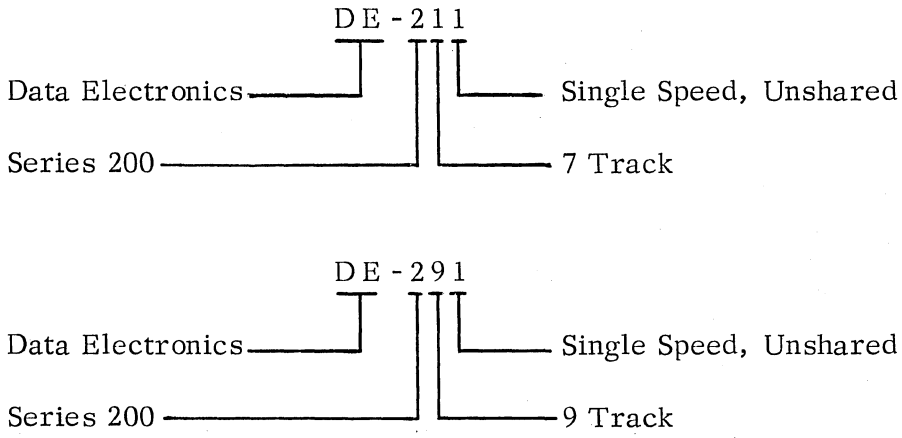
SECTION I
GENERAL DESCRIPTION

1-1. INTRODUCTION.

1-2. SCOPE.

This technical manual describes the installation, operation, theory of operation and maintenance of the DE-211 and the DE-291 Data Electronics.

1-3. MODEL DESIGNATIONS.



1-4. PURPOSE AND BASIC PRINCIPLES.

1-5. PURPOSE.

The Data Electronics card cage is wired, as shown on the Data Electronics Logic Diagram, to accommodate circuit board assemblies which provide the circuitry required to read, write, and check digital data. Seven-track tapes are bilaterally interchangeable with tapes prepared on IBM 729 tape transports. Nine-track tapes are bilaterally interchangeable with tapes prepared per ASCII specifications.

1-6. BASIC PRINCIPLES.

The card cage is wired to accommodate circuit boards which will read and write on either 7 or 9 tracks. Wiring is also included to accommodate circuit boards which will perform Vertical Parity Check, and Echo and Rate Checks.

Circuit board assemblies included in the card cage are determined by tape speed, bit packing density, number of tracks, error checking options, bidirectional read capability, and special features.

1-7. SPECIAL FEATURES.

The following special features (SF) are documented in Section VIII of this manual.

SF1: Special Positive Input/Output Levels (Dual Density).
SF2: Vertical Parity Generate (7 Track).
SF3: Vertical Parity Generate (9 Track).
SF4: Longitudinal Parity Check.
SF5: Longitudinal Check Character Generate.

Addenda, which include special logic diagrams, are prepared to document special features not included in this manual. Table 1-1 is a partial list of addenda.

TABLE 1-1
DATA ELECTRONICS ADDENDA

ADDENDUM	DESCRIPTION	LOGIC
3115501	Special Negative Input/Output Levels (Dual Density with Run/Stop Logic)	3115445
3115502	Tri-Density (Run/Stop Logic)	3115446
3115503	Read Only (Dual Density with Run/Stop Logic)	3115795
3115758	Longitudinal Check Character Generate (Tri-Density)	3115757
3118390	Special Negative Input/Output Levels (Tri-Density with Run/Stop Logic)	3118323

SECTION II
INSTALLATION

2-1. INTRODUCTION.

2-2. SCOPE.

This section provides information on unpacking, power requirements, installation and cabling. Input signal requirements and output signal characteristics are also described in this section.

2-3. UNPACKING.

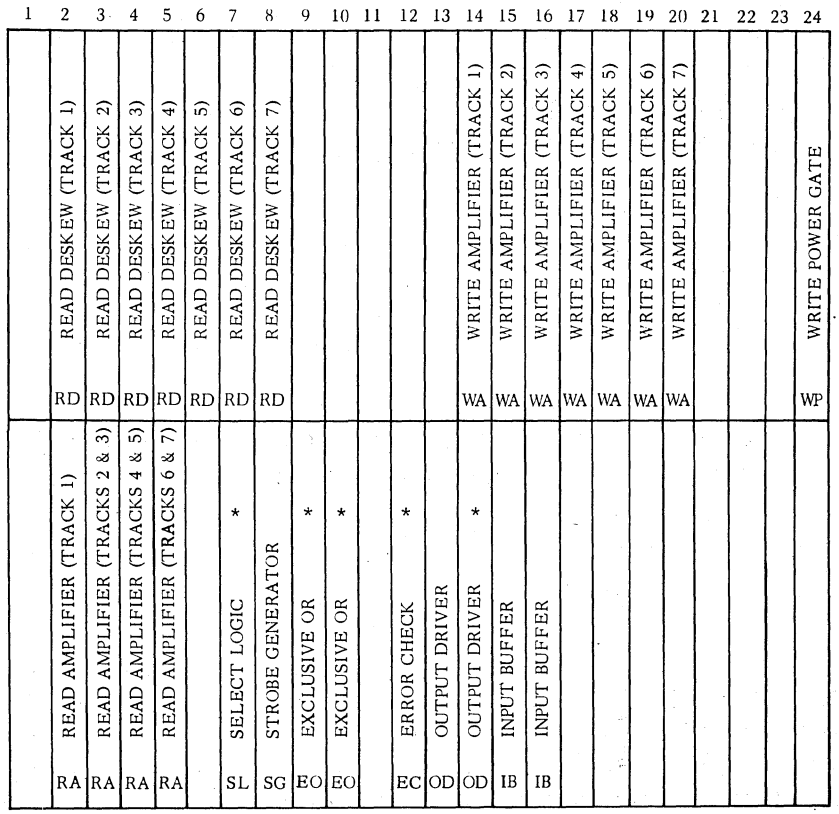
The Data Electronics is installed with the Ampex Tape Transport in the Tape Memory System enclosure. When no enclosure is supplied, the Data Electronics is shipped in custom designed crating. No special unpacking instructions are required. All equipment should be inspected for shipping damage prior to the application of power.

2-4. POWER REQUIREMENTS.

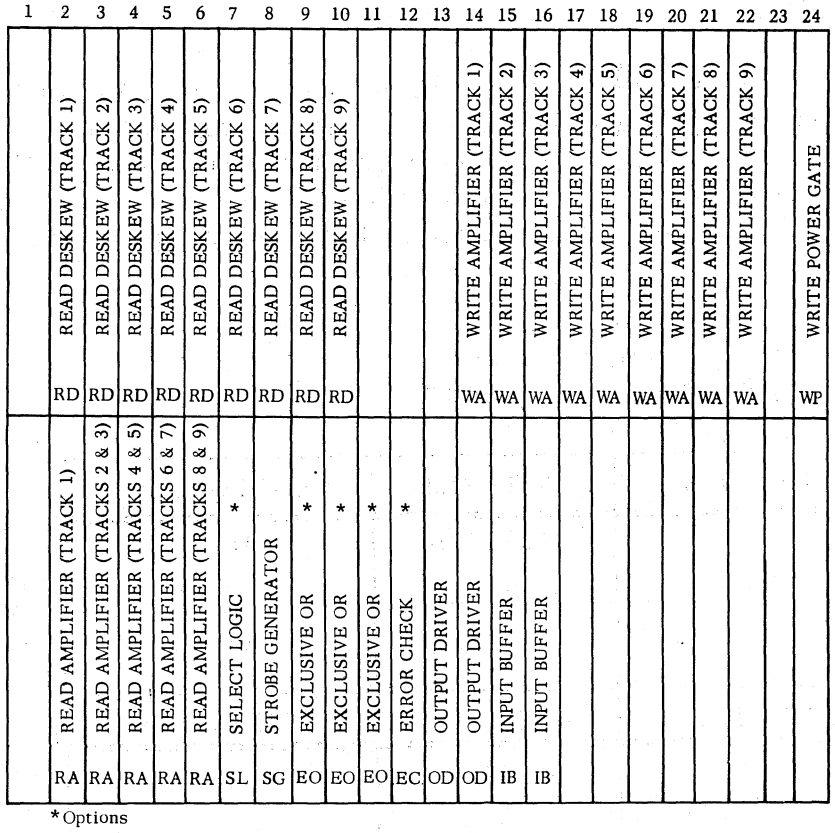
Power for the Data Electronics is supplied by the Ampex Logic Power Supply, which is a separate assembly. The power supply provides three regulated voltage outputs and two unregulated voltage outputs. The power supply requires a maximum input power of 345 watts with all outputs at the full load shown on Table 2-1. If the Ampex Logic Power Supply is not used, provision must be made to supply the voltages listed in Table 2-1 at the required current and regulation.

TABLE 2-1
POWER SUPPLY OUTPUT

REGULATED VOLTAGE	CURRENT	REGULATION
+12V	+4.5 Amp	1%
-12V	-5.0 Amp	1%
- 6V	±1.5 Amp	2%
UNREGULATED VOLTAGE	**CURRENT**	**REGULATION**
+24V	+0.1 Amp	10%
-24V	-0.1 Amp	10%



7-TRACK
DATA ELECTRONICS
(DE-211)



9-TRACK
DATA ELECTRONICS
(DE-291)

*Options

Figure 2-1
PCB Locations

2-5. INSTALLATION.

Typical Outline and Installation drawings are provided in the drawing sections of the Tape Transport technical manuals. Figure 2-1 shows typical printed circuit board (PCB) assembly locations for 7-track and for 9-track Data Electronics. Mnemonic designations, as shown on the Logic Diagram, are provided. Table 2-2 lists the coded designation which appears on the ejector tab of the PCB's and provides the part numbers according to basic tape speeds.

2-6. CABLING.

Cabling diagrams for TM-7211, TM-9211, and TM-11211 Tape Memory Systems are provided in the drawing sections of the tape transport technical manuals. The TM-11211 diagram is also used for TM-12211 systems. Inputs to the system and outputs from the system are connected to the Data Electronics via the connectors on the Input/Output Panel as shown in Tables 2-3 and 2-4, respectively. These inputs and outputs supersede those listed in the Tape Transport manual. Connections from the read heads are as shown in Table 2-5 and connections to the write heads in Table 2-6. Table 2-7 lists connections to the Tape Transport. Table 2-8 lists connections to the Logic Power Supply. Tables 2-3 through 2-8 are located at the end of this section.

2-7. INPUT SIGNAL REQUIREMENTS.

2-8. INPUT SIGNAL VOLTAGE LEVELS.

The following signal voltage levels apply to all input signals (the input impedance is 2300 ±115 ohms returned to -3.8 volts).

TRUE Level: -12 (+3, -13) volts

FALSE Level: 0.00 ±1.25 volts

NOTE

When non-standard input levels are provided, special Input Buffer PCBs and wiring changes are required.

2-9. INPUT SIGNAL TIMING.

In the following description of input signal timing, transition times are measured from the 10-percent point to the 90-percent point. Signal duration is measured from the 90-percent point of the leading-edge transition to the 10-percent point of the trailing-edge transition.

TABLE 2-2
PCB PART NUMBERS

CODE	DESCRIPTION	PART NO.
ECC*	Error Check	
	36/45 ips	3109872-10
	75 ips	3110558-10
	112.5/120/150 ips	3110031-10
EOA**	Exclusive OR	3107274-10
IBA	Input Buffer	3107258-10
ODA	Output Driver	3107259-10
RAB	Read Amplifier	
	36/45 ips	3107266-10
	75 ips	3109991-10
	112.5/120/150 ips	3110273-10 or 3118138-01
RDB***	Read Deskew (Read Fwd)	
	36/45 ips	3107269-10
	75 ips	3109475-10
	112.5/120/150 ips	3110004-10
RDC***	Read Deskew (Bidirectional)	
	36/45 ips	3109932-10
	75 ips	3109935-10
	112.5/120/150 ips	3109936-10
SGA	Strobe Generator	
	36/45 ips	3107057-10
	75 ips	3109994-10
	112.5/120 ips	3110003-10
	150 ips	3118218-01
SLB***	Select Logic-B	3111157-10
WAB	Write Amplifier	
	36/45 ips	3112363-10
	75 ips	3109572-10
	112.5/120/150 ips	3110002-10
WPD	Write Power Gate	3107268-10

*The Error Check (ECC) PCB is supplied for the Echo and Rate Check option.
**Two Exclusive OR (EOA) PCBs are supplied for the Vertical Parity Check option.
***Read Deskew (RDB) PCBs are replaced by Bidirectional Read Deskew (RDC) PCBs for bidirectional reading. Select Logic (SLB) is supplied for the bidirectional read option.

2-10. Write Data. (See Figure 2-2.) A minimum interval of 1.5 μsec is required between the 90-percent point of the Write Data leading-edge transition and the 10-percent point of the next Write Strobe leading-edge transition.

A minimum interval of 1.5 μsec is required between the 90-percent point of the Write Strobe trailing-edge transition and the 10-percent of the next Write Data leading-edge transition.

To write a series of ONE's, the Write Data input may be held at the TRUE level for the entire series.

2-11. Write Strobe. (See Figure 2-2.) The Write Strobe leading (and trailing) edge transition time shall not exceed 1.5 μsec.

The Write Strobe TRUE state must coincide with the Write Data TRUE (or FALSE) state for at least 2 μsec.

2-12. Write Reset. The Write Reset leading (and trailing) edge transition time shall not exceed 1.5 μsec.

The Write Reset signal must remain at the TRUE level for at least 1.5 μsec.

The Write Reset signal is used to write the longitudinal check character (LCC) at the end of each block of data. The LCC resets the NRZ1 write register.

A minimum interval of 10^6 μsec/data transfer frequency is required between the 90-percent point of the Write Reset trailing-edge transition and the 10-percent point of the next Write Strobe leading-edge transition.

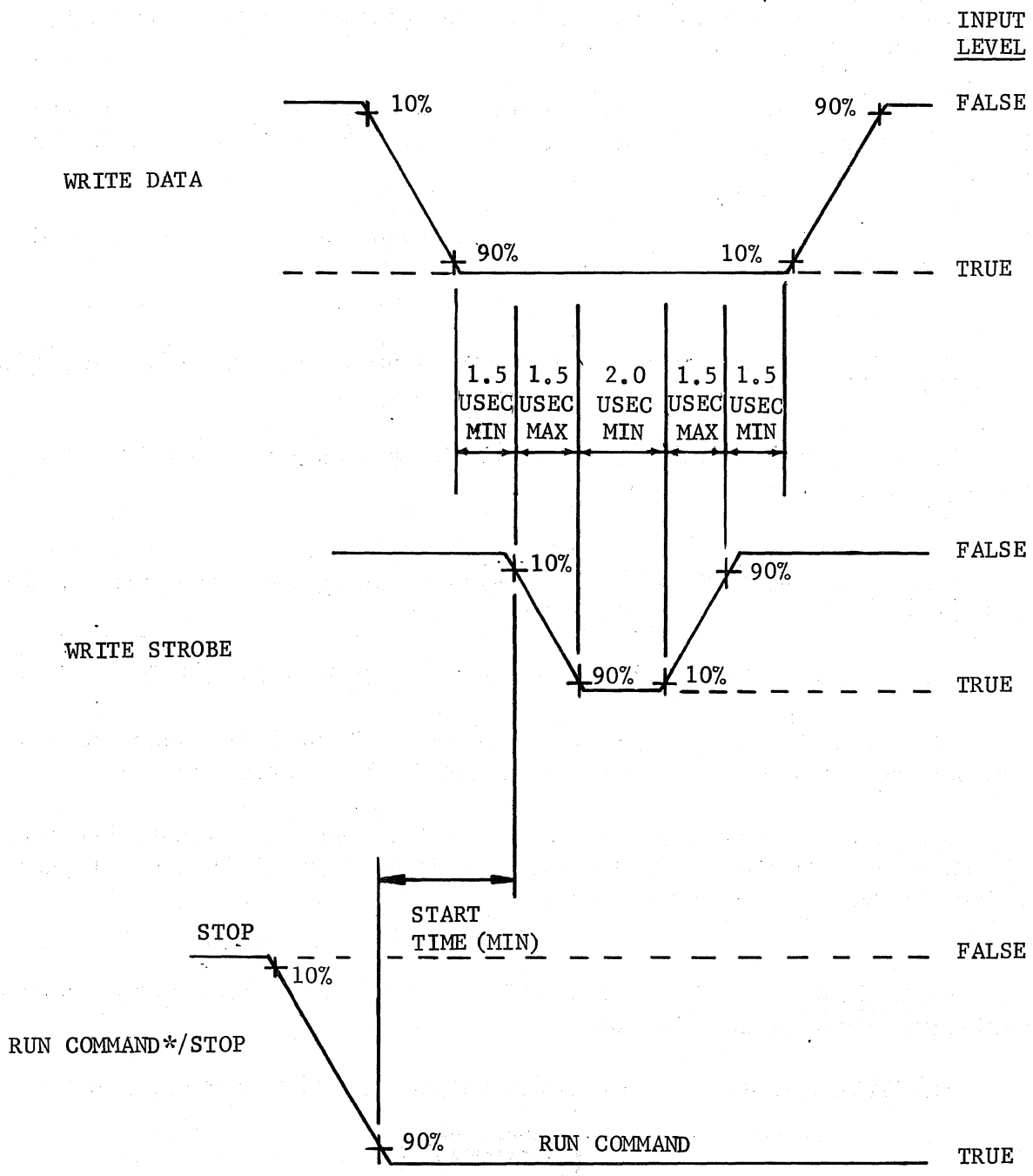
2-13. Write Permit. (See Figure 2-3.) The Write Permit leading (and trailing) edge transition time shall not exceed 5 μsec.

The Write Permit level shall not be changed while the tape is in motion.

CAUTION

Write Permit should be at the FALSE level during Reverse and Rewind operations.

2-14. Read Permit. The Read Permit leading (and trailing) edge transition time shall not exceed 5 μsec.



*Run Command is Run in Fwd/Rev-Run/Stop logic systems and Forward or Reverse in Fwd/Stop-Rev/Stop logic systems.

Figure 2-2
Timing Requirements for Write Data, Write Strobe, and Run/Stop Inputs

2-15. HI/LO Density. The HI/LO Density leading (and trailing) edge transition time shall be 5 μsec maximum. High density is selected by a TRUE level. The high/low density line selects the appropriate timing read circuits.

NOTE

This signal is normally supplied from the tape transport Operator Control Panel.

2-16. Odd/Even Parity. The Odd/Even Parity leading (and trailing) edge transition time shall not exceed 5 μsec. Odd parity is selected by a TRUE level. The Odd/Even Parity line is used to select odd or even Read Vertical Parity check.

2-17. Forward/Reverse. The Forward/Reverse leading (and trailing) edge transition time shall not exceed 5 μsec. (See Figure 2-3A.) The Forward mode is active when this line is at the TRUE level. Forward/Reverse transitions shall not occur while the tape is in motion.

A minimum interval of 5 μsec is required between a Forward/Reverse transition and the Run/Stop transition.

CAUTION

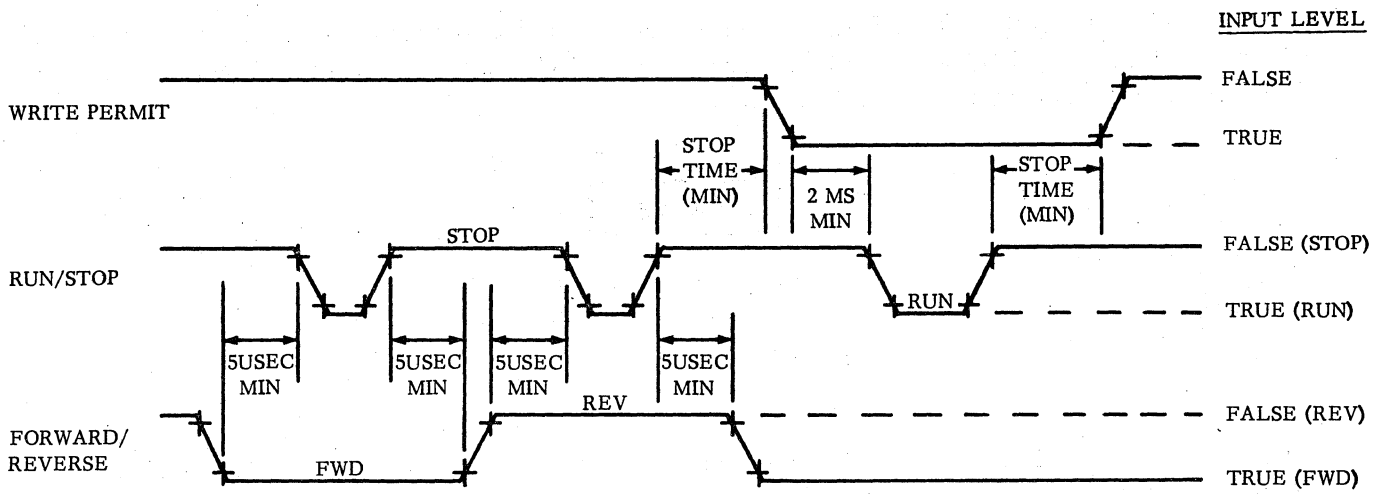
Write Permit should be at the FALSE level when tape is moving in the Reverse direction.

2-18. Run/Stop. The Run/Stop leading (and trailing) edge transition time shall not exceed 5 μsec. (See Figure 2-3B.) A TRUE level on this line sets the transport in the Run mode.

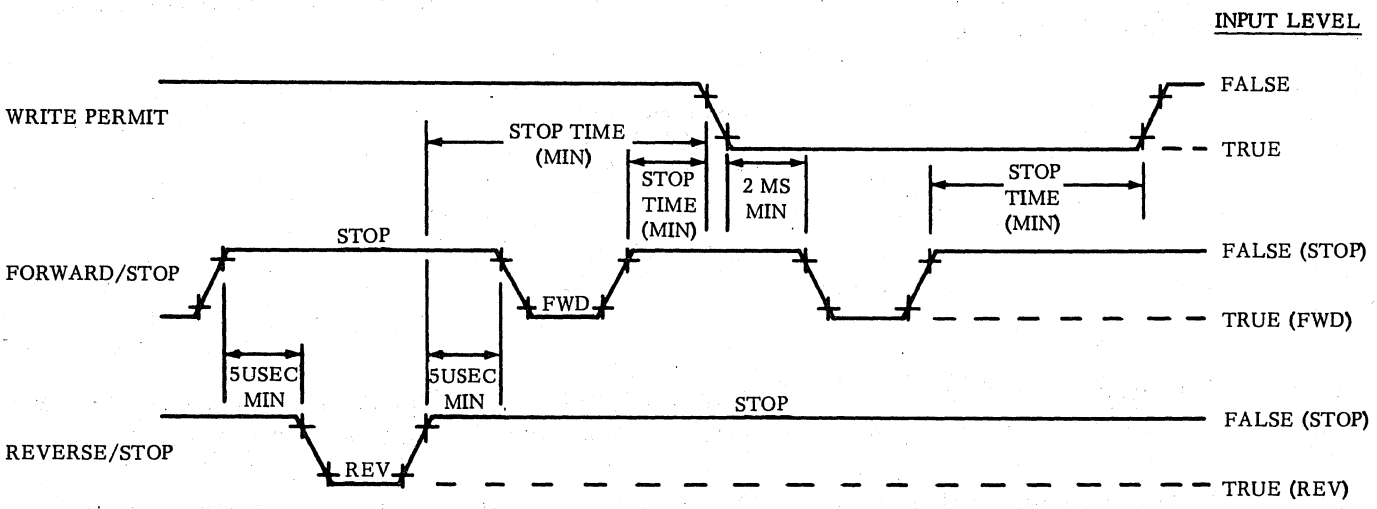
A minimum interval of 5 μsec is required between the Forward/Reverse transition and the Run command.

A minimum interval of 2.0 ms is required between a Write Permit transition and a Run command.

A minimum interval equal to the stop time (to allow tape motion to stop) is required between the 90-percent point of a Stop command transition and a Write Permit transition.



A. Forward/Reverse-Run/Stop Logic



B. Forward/Stop-Reverse/Stop Logic

Figure 2-3
Timing Requirements for Write Permit, Forward/Reverse, Run/Stop, Forward/Stop, and Reverse/Stop Inputs

2-19. Forward/Stop (Option). The Forward/Stop leading (and trailing) edge transition time shall not exceed 5 μsec. (See Figure 2-3B.) The Forward mode is active when this line is at the TRUE level.

A minimum interval of 2.0 ms is required between a Write Permit transition and a Forward command.

A minimum interval equal to the stop time (to allow tape motion to stop) is required between the 90-percent point of a Stop command transition and a Write Permit transition.

2-20. Reverse/Stop (Option). The Reverse/Stop leading (and trailing) edge transition time shall not exceed 5 μsec. (See Figure 2-3B.) The Reverse mode is active when this line is at the TRUE level. A minimum interval equal to the stop time (to allow tape motion to stop) is required between the 90-percent point of a stop command transition and a Write Permit transition.

CAUTION

Write Permit should be at the FALSE level when tape is moving in the Reverse direction.

2-21. Rewind. The Rewind leading (and trailing) edge transition time shall not exceed 5 μsec. The Rewind signal shall remain at the TRUE level for at least 5 μsec. Rewind operation is initiated by the negative-going transition.

2-22. Rewind and Lockout. The Rewind and Lockout leading (and trailing) edge transition time shall not exceed 5 μsec. The Rewind and Lockout signal shall remain at the TRUE level for at least 5 μsec. Rewind and lockout operation is initiated by the negative-going transition.

2-23. OUTPUT SIGNAL CHARACTERISTICS.

2-24. OUTPUT SIGNAL VOLTAGE AND CURRENT LEVELS.

TRUE Level: -11.5 (+2.5, -0.5) volts; 5 ma maximum from the load

FALSE Level: 0.00 ±1.25 volts; 5 ma maximum to the load

NOTE

When non-standard output levels are provided, special Output Driver PCBs and wiring changes are required.

2-25. OUTPUT SIGNAL TIMING.

In the following description of output signal timing, transition times are measured from the 10-percent point to the 90-percent point. Signal duration is measured from the 90-percent point on the leading edge transition to the 10-percent point on the trailing edge transition. Maximum leading edge displacement between Read Data, Read Clock, and Vertical Parity Error outputs is 0.3 μsec maximum.

The trailing edge transition times may be affected by the external load circuits.

2-26. Read Data. The Read Data leading edge transition time is 0.30 μsec maximum. The trailing edge transition time is 0.30 μsec. Signal duration is from 0.9 μsec minimum to 1.5 μsec maximum.

2-27. Read Clock. The Read Clock leading edge transition time is 0.30 μsec maximum. The trailing edge transition time is 0.30 μsec. Signal duration is from 0.9 μsec minimum to 1.5 μsec maximum.

2-28. Vertical Parity Error (Option). The Vertical Parity Error leading edge transition time is 0.30 μsec maximum. The trailing edge transition time is 0.30 μsec maximum. Signal duration is from 0.9 μsec minimum to 1.5 μsec maximum.

2-29. Write Check Error (Option). The Write Check Error leading edge transition time is 0.30 μsec maximum. The trailing edge transition time is 0.30 μsec maximum. Signal duration is from 0.5 μsec minimum to 5.3 μsec maximum.

2-30. Write Enable Status. Three lines are provided to indicate the state of the write permit relay on the Data Electronics Write Power Gate PCBA. When a file-protect condition exists, the write permit relay is deenergized and the Write Enable Status (C) line is connected to the Write Enable Status (NC) line. When a write enable condition exists, the write permit relay is energized and the Write Enable Status (C) line is connected to the Write Enable Status (NO) line.

2-31. LP Error (Special Feature). The LP Error leading edge transition time is 0.30 μsec maximum. The trailing edge transition time is 0.3 μsec maximum. A TRUE level pulse on the LP Error line indicates that a longitudinal parity error was detected in the last data block read.

2-32. TAPE TRANSPORT STATUS OUTPUTS.

Tape transport status output levels are -11.5 (+2.5, -0.5) volts (5 ma maximum from the load) and 0.00 ±1.25 volts (5 ma maximum to the load) for TRUE and FALSE, respectively, unless otherwise indicated. The status outputs are active in the remote mode only.

2-33. Beginning-of-Tape (BOT). A TRUE level on the BOT line indicates that the BOT tab is being sensed by the photosense assembly.

2-34. End-of-Tape (EOT). A TRUE level on the EOT line indicates that the EOT tab is being sensed by the photosense assembly.

2-35. High/Low Density Status. The High/Low Density Status line acknowledges the density select level. A TRUE level indicates that high density has been selected. A FALSE level indicates that low density has been selected.

2-36. Ready. A TRUE level on the Ready line indicates that all tape transport interlocks are closed and the transport is ready for remote operation.

2-37. Rewinding. A TRUE level on the Rewinding line indicates that the rewind operation is being performed.

2-38. Unit Select. A TRUE level on the Unit Select line indicates that the tape transport has been selected by a TRUE level at the Select input (when a single tape transport is used, the Select line is returned to -12 volts in the Data Electronics, thus providing a TRUE Select level at all times).

2-39. Select and Remote Indicator. This line is driven by a line driver returned to ground. The line driver must be terminated with an indicator lamp returned to -12 volts (this is normally done by an indicator lamp in the Operator Control Panel of the Tape Transport). When so terminated, the line driver output is 0.0 ±1.5 volts when the Unit Select status line is at the TRUE level; the line driver output is 125 ohms returned to ground when the Unit Select status line is at the FALSE level.

TABLE 2-3
SYSTEM INPUT CONNECTIONS
(TYPICAL)

INPUT/OUTPUT PANEL CONNECTOR J4 PIN NO.	INPUT SIGNAL	DATA ELECTRONICS CONNECTOR J5 PIN NO.
e	Fwd/Rev (or Rev/Stop)	26
l	Odd/Even Parity	24
f	Rewind Command	28
Z	Rewind and Lockout	27
d	Read Permit	10
Y	Run/Stop (or Fwd/Stop)	25
c	Write Permit	21
X	Write Reset	9
W	Write Strobe	8
C	Write Track 1	1
D	Write Track 2	2
E	Write Track 3	3
F	Write Track 4	4
M	Write Track 5	5
N	Write Track 6	6
P	Write Track 7	7
R	Write Track 8	22
S	Write Track 9	23
G	Spare	31
j	Spare	39
k	Spare	40
A	Ground	11
B	Ground	12
H	Ground	13
J	Ground	14
K	Ground	15
L	Ground	16
T	Ground	17
U	Ground	18
V	Ground	19
a	Ground	35
b	Ground	36
g	Ground	29
h	Ground	30
m	Shield Ground	20

TABLE 2-4
SYSTEM OUTPUT CONNECTIONS
(TYPICAL)

INPUT/OUTPUT PANEL CONNECTOR J5 PIN NO.	OUTPUT SIGNAL	DATA ELECTRONICS CONNECTOR J4 PIN NO.
W	Beginning-of-Tape	21
X	End-of-Tape	22
e	High/Low Density Status	25
R	Read Clock	8
C	Read Track 1	1
D	Read Track 2	2
E	Read Track 3	3
F	Read Track 4	4
M	Read Track 5	5
N	Read Track 6	6
P	Read Track 7	7
G	Read Track 8	9
d	Read Track 9	10
Z	Ready	24
Y	Rewinding	23
k	Unit Select	32
l	Select and Remote Indicator	33
h	Vertical Parity Error*	27
c	Write Check Error*	29
V	Write Enable Status (C)	38
b	Write Enable Status (NC)	40
a	Write Enable Status (NO)	39
j	Spare (or LP Error**)	28
f	Spare	26
A	Ground	11
B	Ground	12
H	Ground	13
J	Ground	14
K	Ground	15
L	Ground	16
S	Ground	17
T	Ground	18
U	Ground	19
g	Ground	31
m	Shield Ground	20

*Spare when option is not supplied.
**With Longitudinal Parity Check special feature.

TABLE 2-5
DATA ELECTRONICS TO READ HEAD INTERCONNECTIONS

DATA ELECTRONICS J1 PIN NO.	READ HEAD J1 PIN NO.	SIGNAL DESCRIPTION
2	A	Read Track 1
12	D	Read Track 1
23	H	Read Track 2
33	L	Read Track 2
4	P	Read Track 3
14	T	Read Track 3
25	W	Read Track 4
35	Z	Read Track 4
6	a	Read Track 5
16	X	Read Track 5
27	U	Read Track 6
37	R	Read Track 6
8	M	Read Track 7
18	J	Read Track 7
29	E	Read Track 8
39	B	Read Track 8
21	C	Read Track 9
31	F	Read Track 9
9	c	Head Ground
22	--*	Shield Ground

*Shield ground terminated at the read head with lug E1, which is attached to chassis ground near the read head.

TABLE 2-6
DATA ELECTRONICS TO WRITE HEAD INTERCONNECTIONS

DATA ELECTRONICS J7 PIN NO.	WRITE HEAD J2 PIN NO.	SIGNAL DESCRIPTION
2	A	Write Track 1
12	D	Write Track 1
22	--	Shield Ground 1
23	H	Write Track 2
33	L	Write Track 2
13	--	Shield Ground 2
4	P	Write Track 3
14	T	Write Track 3
24	--	Shield Ground 3
25	W	Write Track 4
35	Z	Write Track 4
15	--	Shield Ground 4
6	a	Write Track 5
16	X	Write Track 5
26	--	Shield Ground 5
27	U	Write Track 6
37	R	Write Track 6
17	--	Shield Ground 6
8	M	Write Track 7
18	J	Write Track 7
28	--	Shield Ground 7
29	E	Write Track 8
39	B	Write Track 8
19	--	Shield Ground 8
21	C	Write Track 9
31	F	Write Track 9
11	--	Shield Ground 9
20	b	Erase Head Power
30	d	Erase Head Return
40	--	Shield Ground Erase Head
10	S	Write Power (Head CT)
9	c*	Head Ground
--	--**	Common Shield

*Head ground also terminated at the write head with lug E1, which is attached to chassis ground near the write head.

**Common shield terminated at the write head with lug E2, which is attached to terminal E2 near the write head.

TABLE 2-7
DATA ELECTRONICS TO TAPE TRANSPORT INTERCONNECTIONS

DATA ELECTRONICS J6 PIN NO.	SIGNAL DESCRIPTION	TM-7/TM-9 J10 PIN NO.	TM-11/TM-12 CONTROL ELECTRONICS J4 PIN NO.
6	Beginning-of-Tape (-)	6	11
8	End-of-Tape (-)	8	12
1	Forward/Reverse (-/+)*	1	14
7	High/Low Density (-/+)	7	7
19	High/Low Density Status (-/+)	19	3
10	Ready (-)	10	2
4	Rewind and Lockout (-)	4	9
3	Rewind Command (-)	3	8
9	Rewinding (-)	9	1
2	Run/Stop (-/+)**	2	15
5	Select (-)	5	4
18	Select and Remote Indicator (+)	18	6
14	Unit Select (-)	14	5
15	Write Enable Switch/Relay (C)	15	18
16	Write Enable Switch/Relay (NC)	16	17
17***	Write Enable Switch/Relay (NO)	17	19
11	Ground	11	13
12	Ground	12	16
13	Ground	13	10
20	Shield Ground	20	20

*Reverse/Stop (-/+) when Fwd/Stop-Rev/Stop logic is supplied.
**Forward/Stop (-/+) when Fwd/Stop-Rev/Stop logic is supplied
***Pin 17 of J6 is returned to ground in the Data Electronics

TABLE 2-8
DATA ELECTRONICS TO POWER SUPPLY INTERCONNECTIONS

DATA ELECTRONICS TS1 TERMINAL NO.	LOGIC POWER SUPPLY TS1 TERMINAL NO.	VOLTAGE
1	6	+12 VDC (Regulated)
2	8	Ground
3	10	-6 VDC (Regulated)
4	12	Ground
5	2	-12 VDC (Regulated)
6	4	Ground
7	13	+24 VDC (Unregulated)
8	14	Ground
9	15	-24 VDC (Unregulated)
10	16	Ground

SECTION III
OPERATION

3-1. INTRODUCTION.

This section briefly describes the operation of the Data Electronics.

3-2. OPERATING MODES.

The Data Electronics is capable of operating in three different modes: write check, write only, and read only. The operating mode is determined by the level of the Read Permit and Write Permit input signals.

3-3. WRITE CHECK MODE.

In the Write Check Mode, information is read immediately after it is written. To operate in the Write Check Mode, Write Permit and Read Permit inputs must be TRUE.

3-4. WRITE ONLY MODE.

In the Write Only Mode, information is written but reading does not occur. To operate in the Write Only Mode, Write Permit input must be TRUE and Read Permit input must be FALSE.

3-5. READ ONLY MODE.

In the Read Only Mode, information is read, but writing does not occur. To operate in the Read Only Mode, Read Permit input must be TRUE and Write Permit input must be FALSE.

3-6. WRITE SIGNAL CONDITIONING.

Writing of data is accomplished on seven (or nine) tracks. In the following description of write signal conditioning, the operation of only one track is discussed. Each input signal is conditioned by an input buffer.

3-7. WRITE DATA. (See Figure 3-1.)

Data is written when the Write Data input is strobed through an AND gate by the Write Strobe and fed, via an OR gate, to the Write Deskew single-shot delay. Write Head gap-to-gap static skew is compensated for by the single-shot delay. The deskewed Write Data signal is fed to the write register. Write Permit is comprised of the ANDed Write Permit and Run inputs. The write register controls the direction of current flow in the write head.

3-8. WRITE POWER.

When the Write Permit signal is TRUE and a Write Enable Ring is in place, power is supplied to the Write and Erase Heads through the Write Power Gate.

3-9. WRITE RESET.

The Write Reset signal is ANDed with the Set status output of the NRZ Write Register and is then fed to the NRZ Write Register flip-flops via the OR gate and the single-shot delay. The Write Reset line is used to write the Longitudinal Check Character (LCC) at the end of each block of data. The LCC is used to reset the NRZ register, resulting in an even number of flux reversals (ONEs) in each track of the block.

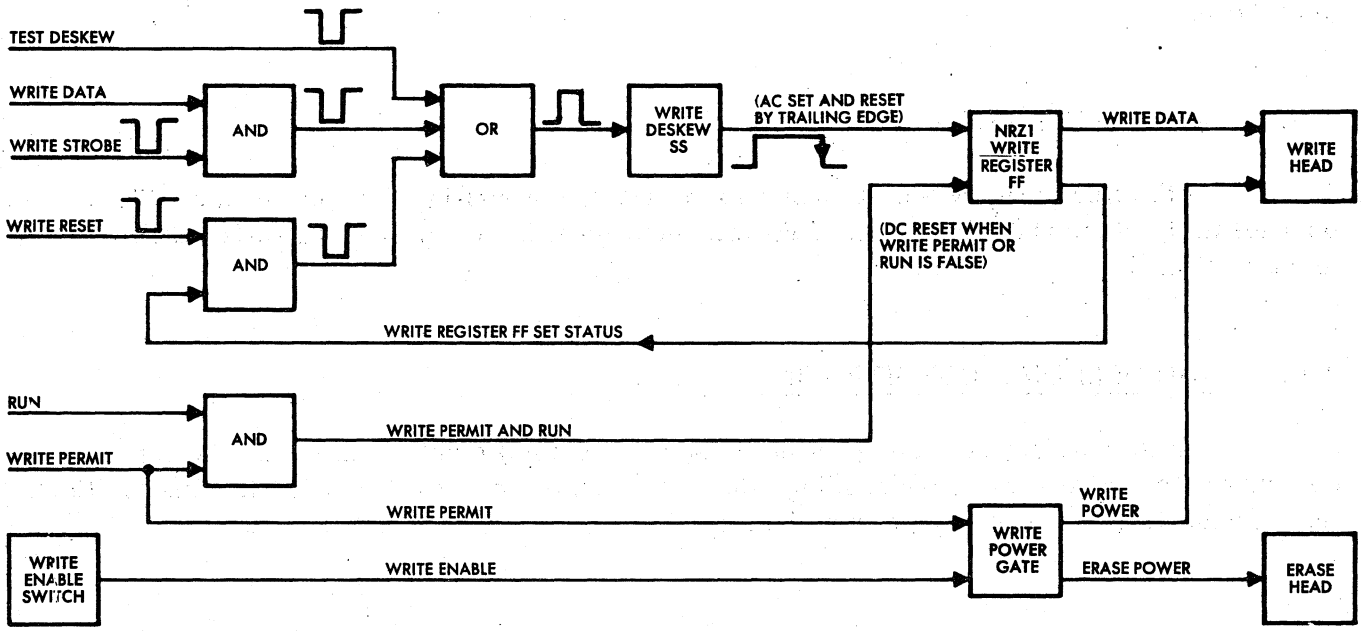


Figure 3-1
Write Signal Conditioning, Block Diagram

3-10. READ SIGNAL CONDITIONING.

Reading of data is accomplished on seven (or nine) tracks. In the following description of read signal conditioning, only one track is discussed.

3-11. READ DATA. (See Figure 3-2.)

The signals from the Read Head are amplified by the Read Amplifier and fed to the peak detector circuit on the Read Deskew PCBA. The peak detector generates positive pulses, corresponding in time to the peaks of the analog Read Head signals. The peak detector clipping level is established as a function of Write Permit.

The Read Data from the peak detector is fed to the Read Deskew single-shot delay. Read head gap-to-gap static skew is compensated for by the single-shot delay. The deskewed Read Data signal is fed to the Read Register. Bi-directional Read Deskew circuits are available as an option.

When a Read Permit signal is present, the Read register assembles the deskewed Read Data signals within each character frame and drives the data output drivers.

3-12. STROBE GENERATION.

The Strobe Generator provides the Strobe signal for the Read Data and Read Parity Error AND gates, and the Read Clock signal to the Read Clock output driver.

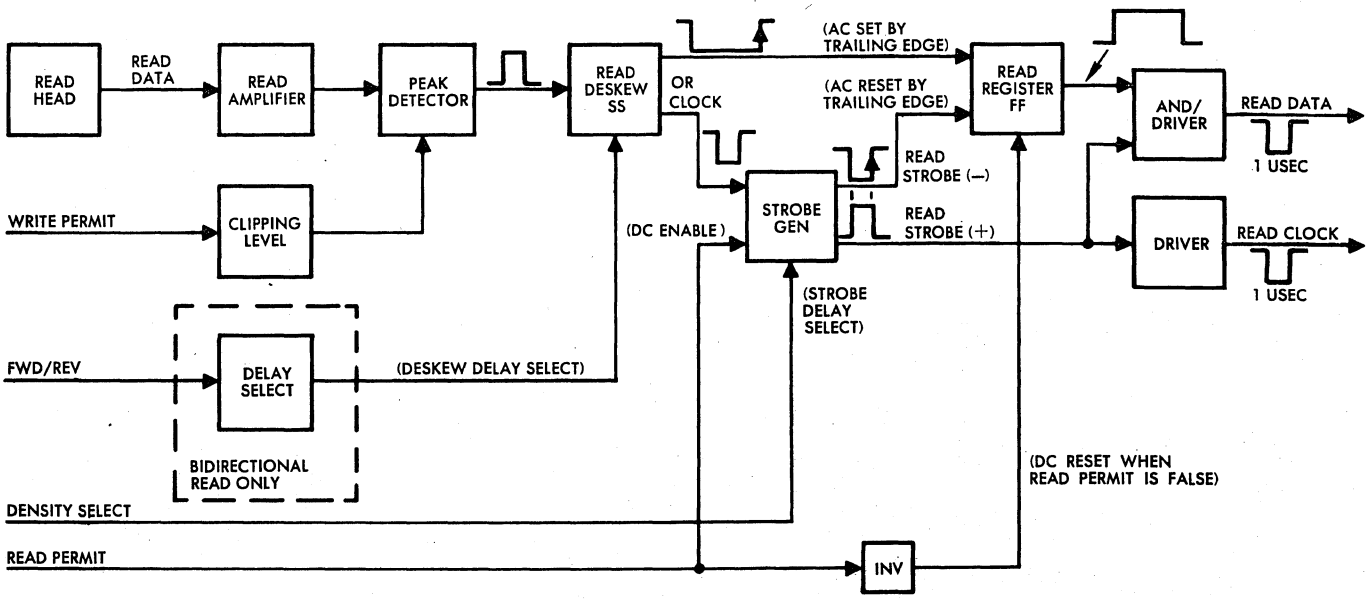


Figure 3-2
Read Signal Conditioning, Block Diagram

3-13. ERROR CHECKING.

3-14. VERTICAL PARITY CHECK.

The vertical parity check circuits generate an Error signal when the parity of the read register does not correspond to the status of the Odd/Even Parity input. In the Read Only Mode, the Error output is provided at the Vertical Parity Error output. In the Write Check Mode, the error indication is provided at the Vertical Parity Error output and at the Write Check Error output

3-15. RATE CHECK.

The rate check circuit generates a Write Check Error output when the time interval between successive characters is below a design threshold.

3-16. ECHO CHECK.

In ORed Clock systems, at least one Write Amplifier flip-flop must change state after each Write Strobe. The echo check circuits generate a Write Check Error output when none of the Write Amplifiers change state after receipt of a Write Strobe.

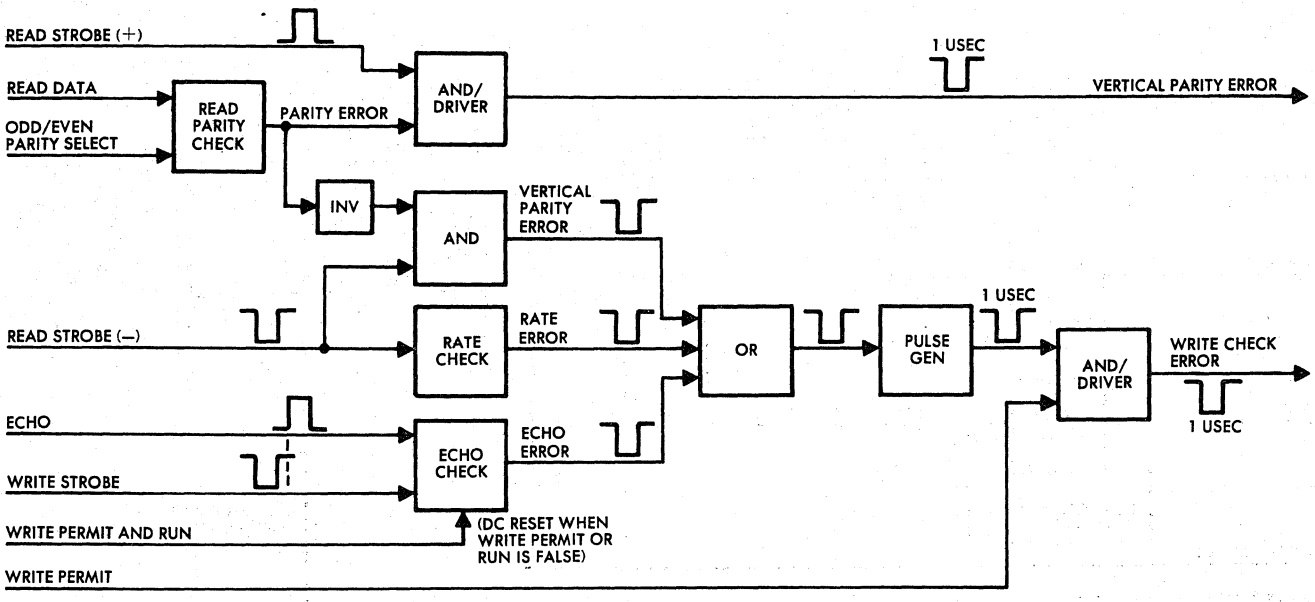


Figure 3-3
Error Check Circuits, Block Diagram

SECTION IV
THEORY OF OPERATION

4-1. INTRODUCTION.

This section includes the theory of operation of the data electronics and an introduction to the graphic symbols used in the logic diagrams. The theory of operation description comprises input/output interface, write logical sequence, read logical sequence, and error check functions.

4-2. LOGIC DIAGRAMS.

The data electronics logic diagrams are located at the end of Section VII. Graphic symbols used in the logic diagrams comply with Military Standard MIL-STD-806B, except that squares and rectangles are used interchangeably for special circuits.

4-3. Logic Element Identification. Identification of a logic element is accomplished by the graphic symbol and the notations within and adjacent to the symbol. (See Figure 4-1.) The mnemonic (top) designation within the symbol identifies the printed circuit board (PCB) type. The alphanumeric (bottom) designation within the symbol identifies the physical location of the PCB in the data electronics card cage. Dashed lines indicate internal connections on the PCB. Numbers adjacent to the logic element indicate the PCB pin number for the connecting signal line.

4-4. State Indicators. A state indicator (small circle) at the input to any logic element indicates that the relatively-low level of the input signal activates that function of the logic element. A state indicator at the output of any logic element indicates that the output level of the activated function is relatively low.

4-5. Signal Callouts. Signal callouts in the data electronics logic diagrams show the TRUE (active) state of the signal. Write Permit (-) indicates that Write Permit is TRUE when the Write Permit (-) signal is relatively low. Read Strobe (+) indicates

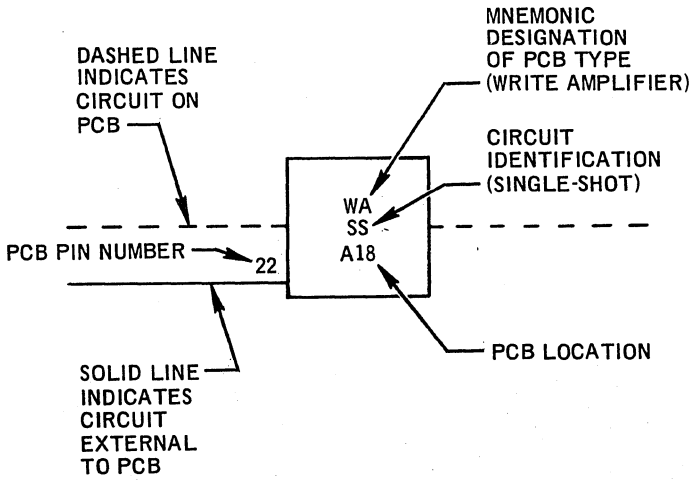


Figure 4-1
Typical Logic Symbol

that Read Strobe is TRUE when the Read Strobe (+) signal is relatively high. Run/Stop (-/+) indicates Run (-) is TRUE when the Run/Stop (-/+) signal is relatively low and Stop (+) is TRUE when the signal is relatively high.

4-6. Signal Flow Direction. Direction of signal flow is indicated by logic symbol orientation. Inputs to a circuit are from the left and outputs are from the right.

Signal flow other than from left to right is indicated by directional arrowheads on the signal lines.

4-7. INPUT/OUTPUT INTERFACE.

4-8. GENERAL.

Most of the signals used in the data electronics logic circuits are binary. Where binary levels are used, one of the two levels is a 0.0 ±0.5 volt level. The second level is generally a -6 volt level. In some circuits, -12 volt, +6 volt, or +12 volt levels are used. When the binary levels are 0 and -6 or 0 and -12; the 0 volt level is relatively high and is therefore termed positive (+), the -6 volt and -12 volt levels are relatively low and are therefore termed negative (-). When the binary levels are 0 and +6 or 0 and +12; the 0 volt level is relatively low and is therefore termed negative (-), the +6 volt and +12 volt levels are relatively high and are therefore termed positive (+).

Input buffers are used in the input interface to condition the system input signals to the logic levels required by the data electronics circuits. Output drivers are used in the output interface to condition the data electronics output signals to the levels required for the system output signals.

4-9. INPUT BUFFERS (TYPICAL).

The system input line to each input buffer is returned to ground through a line terminating resistor. Each system input signal level is compared with a fixed reference voltage in transistor gate circuits on the input buffer PCB. When the level of an input signal exceeds the gate threshold level established by the reference voltage, the output of the input buffer circuit is switched from one binary logic level to the other. When the system input signal level falls below the gate threshold level, the output of the input buffer is switched back to the other binary logic level. The input buffers provide high-noise-immunity inputs for the system.

The conditioned outputs from the input buffers are applied to the data electronics logic circuits.

4-10. OUTPUT DRIVERS (TYPICAL).

The output drivers for the data electronics are located on the output driver PCB assemblies. NAND gate/drivers are used in each output driver circuit. The NAND gates provide for read strobe control of the system read data outputs and for inhibit of other system outputs when required. The NAND gates are enabled by relatively-high level (or open circuit) inputs.

4-11. WRITE LOGIC SEQUENCE.

4-12. WRITE DATA.

A TRUE (low level) Write Data signal at pin 12 of the write amplifier data input AND gate enables the AND gate. A Write Strobe pulse coincidental with the TRUE Write Data signal produces a negative-going pulse at the output of the AND gate. The negative-going pulse is applied through a NOR gate to the input of the Write Deskew single-shot delay. The positive-going pulse from the NOR gate triggers the single-shot delay, which produces a positive-going pulse. The width of the single-shot delay pulse is adjustable and is set to compensate for the gap-to-gap misalignment (static skew) of the write heads.

The negative-going trailing edge of the single-shot delay pulse triggers the Write Register flip-flop and the flip-flop changes state. When the flip-flop changes state, the direction of current flow through the write head is reversed, which causes the polarity of the head magnetic flux to reverse. The flux polarity change is impressed on the tape and is interpreted as a logical ONE during the read function.

4-13. WRITE RESET.

The Write Reset signal is used to reset the Write Register flip-flops and to generate the LPC character. The Write Register flip-flops are in the reset state at the start of each block of write data. If an odd number of data bits are written on any one track, that Write Register flip-flop is in the set state after the last data bit of the block is written. A low level status signal from the set flip-flop enables the Write Amplifier reset AND gate. The Write Reset pulse produces a negative-going pulse at the output of the reset AND gate. The negative-going pulse is applied through the NOR gate to the input of the Write Deskew single-shot delay and causes a ONE to be written as previously described for the Write Data input. The Write Register flip-flop is then in the reset state.

The reset of the flip-flops generates the LCC which provides an even number of data bits in each track of a data block.

4-14. WRITE REGISTER DC RESET.

The Write Permit signal input is inverted and NANDed with the inverted Run/Stop signal input (or with the inverted Fwd/Stop signal input in Fwd/Stop-Rev/Stop logic systems). The NAND gate is located on the strobe generator PCB. When either the Write Permit signal or the Run/Stop (or Fwd/Stop) signal is at the FALSE (high) level, the output of the NAND gate is at the low level. The low level output from the NAND gate DC resets the Write Register flip-flops and holds the flip-flops in the reset state.

4-15. TEST DESKEW.

A negative-going Test Deskew pulse train applied at test point TP1 of the Data Electronics is applied through the Write Amplifier NOR gates to the inputs of the Write Deskew single-shot delays. The pulses cause all ONEs to be written as previously described for the Write Data input. The Test Deskew input is used during off-line Write Deskew adjustment procedures. The Write Reset and the Write Strobe inputs must be FALSE when the Test Deskew input is used.

4-16. WRITE HEAD POWER.

Write Head Power is furnished by the Write Power Gate. When the Write Permit input is at the TRUE level and a write enable ring is in place in the file reel, +10 volt power is supplied to the write heads from the write power gate PCB through pins 28, 29, and 30. The write power relay on the write power gate PCB is energized when the write enable ring is sensed by the write enable switch assembly on the tape transport.

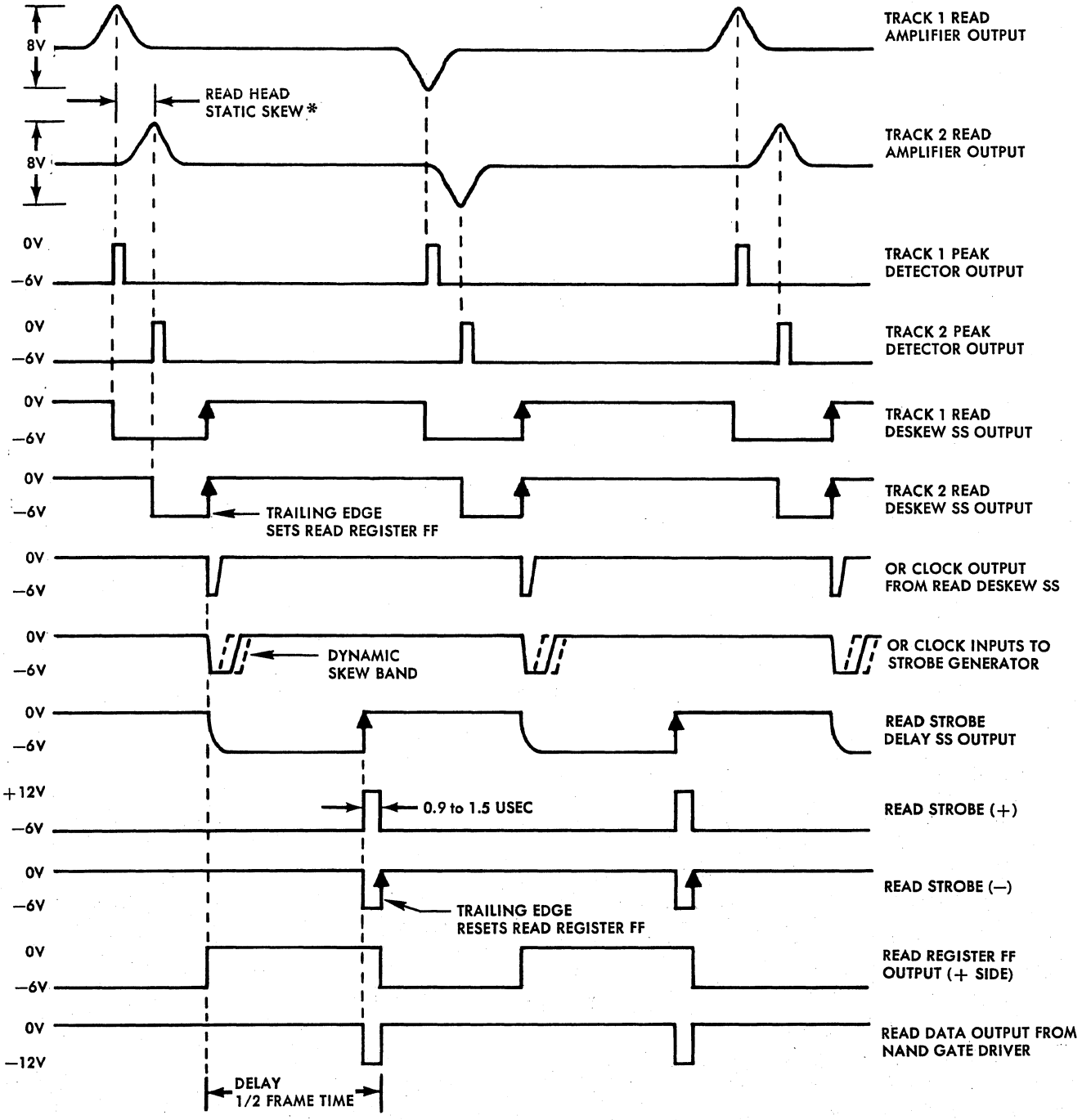
4-17. READ LOGICAL SEQUENCE.

4-18. READ PERMIT.

Read Permit TRUE enables the read strobe generator circuits. Read Permit FALSE DC resets the read register flip-flops and holds the flip-flops in the reset state.

4-19. READ DATA. (See Figure 4-2.)

Flux transitions (written ONEs) on the tape are sensed by the read heads as bipolar analog Read Data signals. The Read Data signals from each read head are amplified in a three-stage differential voltage amplifier on the associated read amplifier PCB assembly and then applied to a differential voltage amplifier on the associated read deskew PCB assembly.



*The read amplifier data outputs are caused by flux reversals on the tape which are sensed by the read heads. Flux reversals on the tracks are written coincidentally; the time displacement shown (read head static skew) is caused by gap-to-gap misalignment of the read heads.

Figure 4-2
Read Deskew Timing

The differential output from the amplifier on the read deskew PCB assembly is clipped in a clipping stage at the input of the peak detector circuit. The clipping level is established by the clipping bias generated on the strobe generator PCB assembly and is selected by the Write Permit signal. The clipping bias level is higher when Write Permit is TRUE.

The clipped analog Read Data signal is applied to the peak detector circuit which produces a positive-going pulse at the positive or negative peaks of the signal. The leading edge of the peak detector output pulse is coincident with the detected peak. The positive-going pulse triggers the Read Deskew single-shot delay, which produces a negative-going pulse. The width of the single-shot delay pulse is adjustable and is preset to compensate for the gap-to-gap misalignment (static skew) of the read heads. Two pulse widths are set for bidirectional read systems; the forward deskew pulse width is selected when the Forward/Reverse (or Forward/Stop) input is TRUE, the reverse deskew pulse width is selected when the Forward/Reverse (or Forward/Stop) input is FALSE.

The positive-going trailing edge of the single-shot delay pulse sets the Read Register flip-flop and the Read Data output at pin 32 of the read deskew PCB goes to the TRUE (high) level. The Read Data output is applied to one input of a NAND gate driver circuit and enables the NAND gate. A Read Strobe (+) pulse coincidental with the TRUE Read Data signal produces a negative-going pulse at the output of the NAND gate driver. The negative-going pulse is a TRUE Read Data output representing a ONE sensed from the tape.

The Read Register flip-flop is reset by the positive-going trailing edge of the Read Strobe (-) pulse.

4-20. READ STROBE.

The Read Strobe (+) and Read Strobe (-) pulses are generated on the strobe generator PCB assembly. The positive-going trailing edge of each Read Deskew single-shot delay pulse is coupled through an associated inverter driver stage to produce a negative-going OR Clock pulse. The OR Clock pulses are applied to one common input of an AND gate on the strobe generator PCB. The other input to the AND gate is the Read Permit signal. When Read Permit is at the TRUE (low) level, the OR Clock pulses are passed through the AND gate. The first OR Clock pulse through the AND gate triggers the Read Strobe single-shot delay, which produces a negative-going pulse. The width of the single-shot delay pulse is adjustable and is preset to approximately one-half the character frame time, less the read strobe pulse time. Two single-shot delay pulse widths are preset: one for the high density packing rate, the other for the low density packing rate. Selection of the pulse width is accomplished by switching circuits on the write power gate PCB. When the HI/LO Density line is at the low level, the High Density pulse width is selected. When the HI/LO Density line is at the high level, the Low Density pulse width is selected.

The positive-going trailing edge of the Read Strobe single-shot delay pulse is coupled to a pulse generator circuit which then generates the positive-going Read Strobe (+)

pulse. The pulse width of the Read Strobe (+) pulse is approximately one microsecond. The Read Strobe (+) pulse is inverted through an inverter stage to produce the Read Strobe (-) pulse.

4-21. ERROR CHECK OPTIONS.

Error check options consist of Vertical Parity Check, Rate Check, and Echo Check. (See The Data Electronics Logic Diagrams in Section VII.)

4-22. VERTICAL PARITY CHECK.

Vertical Parity is checked during both Read Only and Write Check modes of operation by a continuous frame-by-frame check of the contents of the read register. A parity-select level from the customer selects either odd or even parity check. Odd parity requires an odd number of logical ONEs be recorded in every character frame. Even parity requires an even number of logical ONEs in every character frame. A Vertical Parity Error exists when an extra (or missing) logical ONE is detected.

Numerical values in parenthesis in the following circuit description refer to 9-track systems. The Odd/Even Parity Select line and the complementary outputs of the Read Register flip-flops are applied to the inputs of the parity checking circuit on the Exclusive OR PCB assembly. Eight Exclusive OR gates are used for 7-track systems, nine for 9-track systems. Each gate compares two inputs and produces a high level output when the logic levels of the inputs are dissimilar. Seven (or nine) Read Data (-) lines from the Read Register flip-flops and the Odd/Even Parity Select line are applied to four (or five) of the Exclusive OR gates. The outputs of the four gates are applied in pairs to the following two Exclusive OR gates, the outputs of which are compared by a single gate. The output of the single gate is compared in a final Exclusive OR gate with a fixed low level input (in 9-track systems, the output of the fifth input Exclusive OR gate is compared with the output of the single gate in the final Exclusive OR gate). The output of the final gate is ANDed with the Read Strobe (+) pulse in a NAND gate driver. If a vertical parity error is sensed, a negative-going Vertical Parity Error pulse is produced at the output of the NAND gate driver and is transmitted to the customer via the system output connector.

4-23. RATE CHECK.

Rate Check is performed only during the Write/Check mode. A Rate error pulse is generated when the interval between successive Read Strobe (-) pulses decreases to

$$0.67 \frac{1}{(\text{tape speed in ips})\,(\text{high bit packing density})}$$

The Rate Check circuit is located on the error check PCB and operates in the following manner. (See Figures 4-3 and 4-4.) The Read Strobe (-) pulse triggers single-shot delay A which produces a negative-going pulse. The positive-going trailing edge of the single-shot delay A pulse triggers single-shot delay B, which produces a negative-going pulse. The next arriving Read Strobe (-) pulse retriggers single-shot delay A and also is ANDed with the output of single-shot delay B. If the Read Strobe (-) pulse and the output pulse from single-shot delay B are coincident, a rate error pulse is generated.

4-24. ECHO CHECK.

An Echo output is generated by each Write amplifier whenever the amplifier changes state and reverses the Write head coil current. The Echo output is a positive-going pulse derived from the induced EMF generated by the Write head inductance when the write head coil current reverses.

In ORed Clock systems, the data that is written must cause at least one head driver to change state in each frame. The Echo output of each Write amplifier is ORed with the Echo outputs of all other Write amplifiers to generate an ORed Echo output. The ORed Echo output occurs if any Write amplifier changes state during the frame interval. If no ORed Echo occurs during the frame, a malfunction in the Write circuits is indicated and an Echo error pulse is generated by the Echo Check circuits.

The Echo error pulse is generated in the following manner. (See Figures 4-5 and 4-6.) The Write Strobe triggers the single-shot delay and the leading edge of the single-shot delay pulse sets the flip-flop. The Write Strobe holds the AND gate FALSE for the strobe duration to prevent any output from the AND gate during the period that the single-shot delay and flip-flop are going TRUE. The AND gate is also held FALSE by the single-shot delay pulse for the duration of its delay. The Echo input must occur sometime after the Write Strobe and within the duration of the single-shot output. The Echo input resets the flip-flop. If no Echo input occurs, the flip-flop remains set at the end of the single-shot delay pulse and the output of the AND gate goes TRUE, indicating an Echo Error.

4-25. WRITE/CHECK ERROR.

The Vertical Parity Check output, Rate Check output, and Echo Check output are ORed together. The occurence of any error triggers a pulse generator circuit, which produces a negative-going 1 microsecond error pulse. The error pulse is ANDed with Write Permit. If the Write Permit is TRUE, a negative-going Write Check Error pulse is produced at the output of the AND gate driver and is transmitted to the customer via the system output connector.

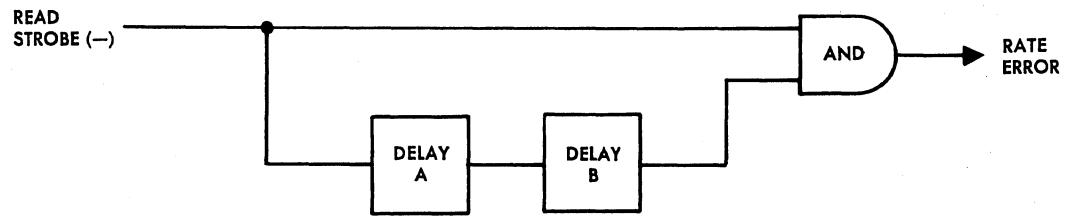


Figure 4-3
Rate Error Check, Block Diagram

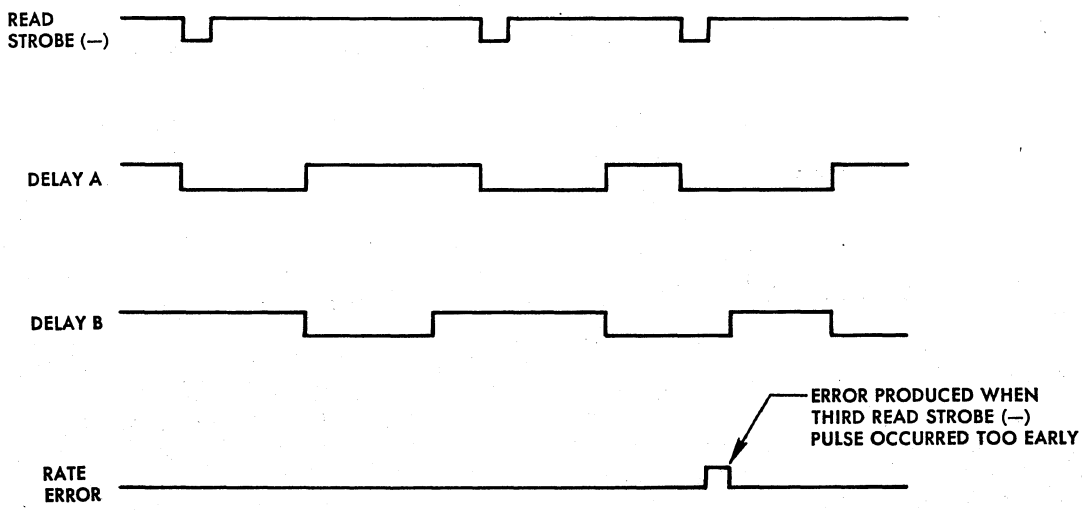


Figure 4-4
Rate Error Timing

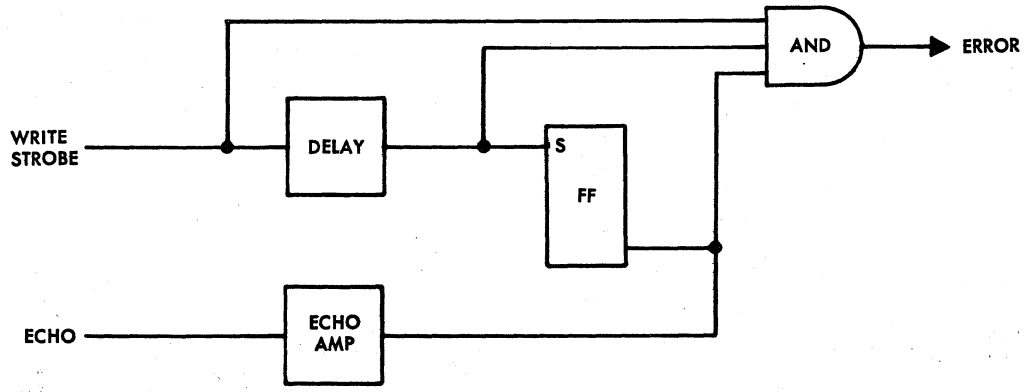


Figure 4-5
Echo Check, Block Diagram

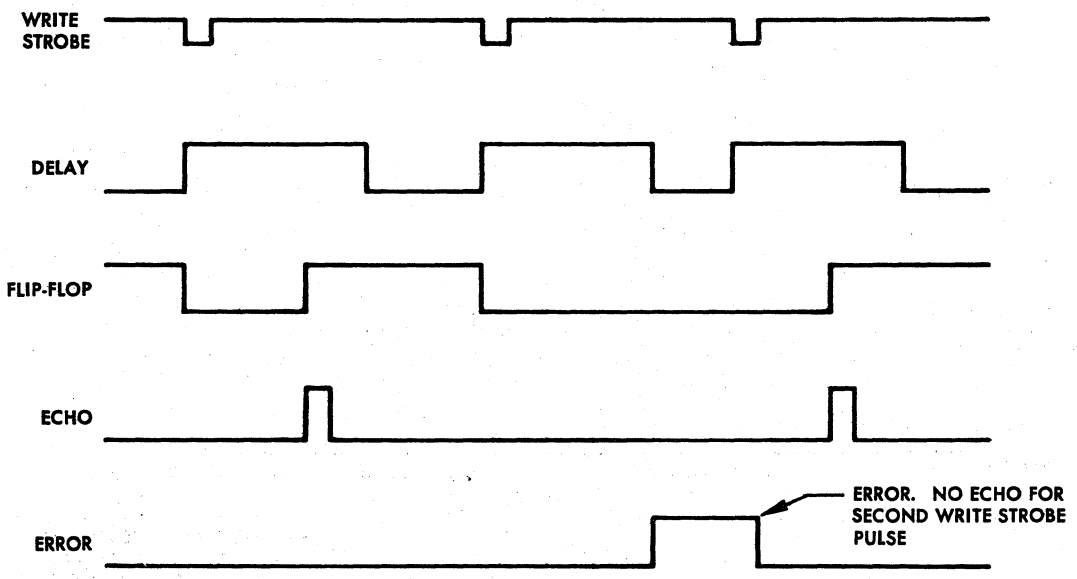


Figure 4-6
Echo Check Timing

SECTION V
MAINTENANCE

5-1. INTRODUCTION.

This section contains adjustment procedures and troubleshooting techniques for the data electronics. Tape transport maintenance is included in the Tape Transport technical manual.

5-2. TEST EQUIPMENT.

Table 5-1 lists the required test equipment.

TABLE 5-1
REQUIRED TEST EQUIPMENT

EQUIPMENT	RECOMMENDED TYPE OR EQUIVALENT
Voltmeter	Hewlett-Packard HP 412A
Alignment Master Tape	Ampex 750-238
Oscilloscope	Tektronix 535
Preamplifier	Tektronix CA
Square Wave Generator	Hewlett-Packard HP 211

5-3. ADJUSTMENT SCHEDULE.

Adjustments are made by Ampex prior to the shipment of equipment. Further adjustments are not normally required unless components are interchanged or replaced. Verify adjustments every 500 hours of operation to maintain maximum data reliability.

5-4. ADJUSTMENT PROCEDURES.

Tape transport and power supply adjustments must be verified before data electronics adjustments are made. Due to the interrelationship between circuit functions, data electronics adjustments must be made in the following sequence.

1. Clipping Level
2. Read Deskew
3. Write Check
4. Write Deskew
5. Read Strobe Delay
6. Rate Check Reference Time*

CAUTION

An insulated blade screwdriver is recommended for making adjustments to prevent accidental shorting of components.

The following preliminary checks should be made before any read deskew, write deskew, or read strobe adjustments are made. Verify that the tape path is clean and free of any restrictions to tape movement. TM-11 and TM-12 tape transports only: In new installations or where the tape guides have been replaced, ensure that the top flanges (caps) on the spring-loaded tape guides are in contact with the center sleeves of the guides. If the attaching screws of the top flanges must be tightened to bring the flanges in contact with the sleeves, a torque driver should be used and the screws tightened to 2.5 to 3.0 inch-pounds of torque.

If adjustments are to be made off line, use Alternate Adjustment Procedure. (Refer to paragraph 5-11.)

5-5. CLIPPING LEVEL.

The bias setting adjustment on the Strobe Generator card determines the clipping level. In the Read Only Mode, the clipping level is set at 20 percent. In the Write Check Mode, the clipping level is set at 40 percent. These percentages refer to the base-to-peak amplitude of the signal into the peak detector.

Step 1: Connect the voltmeter negative lead to pin B8-32 (clip level output) and the positive lead to TS1-3 (-6 volt reference).

*Required only when the optional write check circuits are used in the data electronics.

Step 2: With power ON, select Remote Mode at the Operator control panel (OCP). When the REMOTE indicator goes ON, the system is ready for operation.

Step 3: Set the Write Permit input to the TRUE level.

Step 4: Adjust R9 (bottom potentiometer) on the strobe generator (SG) PCB at B8 to obtain +1.40 ±0.05 volts between B8-32 and TS1-3, as indicated on the voltmeter. (See Figure 5-1 for potentiometer location.)

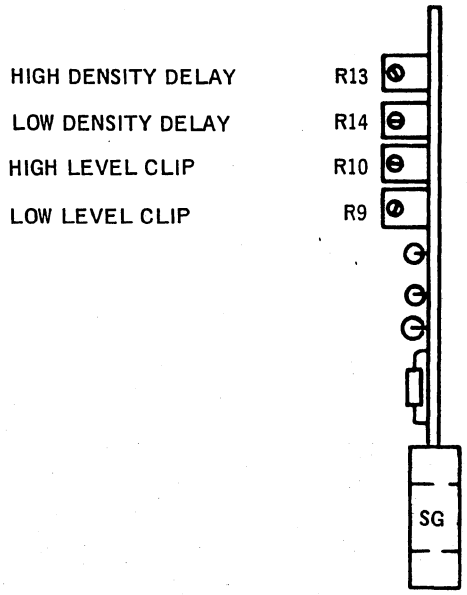


Figure 5-1
Clip Level and Strobe Delay Potentiometers

Step 5: Set the Write Permit input to the FALSE level.

Step 6: Adjust R10 (second-from-bottom potentiometer) on SG to obtain +0.60 ±0.02 volts between B8-32 and TS1-3, as indicated on the voltmeter.

Step 7: Repeat Steps 3 through 6 to ensure that the level has not changed. This completes the clipping level adjustment.

Step 8: Disconnect the voltmeter.

5-6. READ DESKEW.

The read deskew adjustment is made using a skew alignment master tape (Ampex No. 750-238). The skew correction is accomplished by setting the delay time of each read deskew single-shot so that the trailing edges of the delay pulses are coincident. A reference track is selected and the trailing edge of the center track (track 5 in 9-track systems, track 4 in 7-track systems) read deskew delay pulse is aligned with the trailing edge of the selected reference track read deskew delay pulse. The center track is then used as the reference track during the read deskew adjustment. A preliminary read-amplifier-gain check is made to ensure that the read amplifier output signal amplitude is adequate for use during the setting of the read deskew single-shot delay times. Steps 3 through 6 pertain to the preliminary read-amplifier-gain adjustment. Steps 7 through 26 pertain to the read forward deskew adjustment. Steps 27 through 41 pertain to the read reverse deskew adjustment and are applicable to bidirectional-read systems only.

Where two potentiometer or test point references are given in an adjustment procedure, the reference not in parenthesis pertains to 9-track systems and the reference in parenthesis pertains to 7-track systems.

Step 1: Set the Write Permit input to the FALSE level and load the alignment master tape on the transport (ensure that the reel does not contain a write enable ring). Verify that the FILE PROTECT indicator on the OCP is ON.

CAUTION

Write power must be disabled to prevent accidental erasure of the master tape. Disabling is accomplished by the procedures of Step 1.

Step 2: Select Remote Mode at the OCP. When the REMOTE indicator goes ON, the system is ready for operation.

Step 3: Connect an oscilloscope to observe the read signal at pin 12 of the track 1 read deskew (RD) PCB at A2. Set the vertical sensitivity of the oscilloscope to 2 v/cm.

Step 4: Run the tape forward. Adjust the oscilloscope horizontal sweep rate as required to observe the read signal envelope (sweep rate approximately 50 μsec/cm for a tape speed of 75 ips).

Step 5: Adjust 2R11 (top potentiometer) on the read amplifier (RA) PCB at B2 to obtain a read signal amplitude of 6 to 8 volts peak-to-peak, as indicated on the oscilloscope. This completes the preliminary read-amplifier-gain adjustment for read data track 1.

Step 6: Repeat Steps 3 through 5 for each of the remaining read data tracks. Refer to Table 5-2 for the read amplifier adjustment and test point locations. See Figure 5-2 for the read amplifier PCB locations. Refer to Table 5-3 for the location of the read deskew PCB assemblies.

Step 7: Connect the channel A input of the oscilloscope to observe the read signal at pin 12 of the track 1 read deskew (RD) PCB at A2.

Step 8: Connect the channel B input of the oscilloscope to observe the read signal at pin 12 of the track 2 read deskew (RD) PCB at A3.

Step 9: Separate the base lines of the two signals displayed on the oscilloscope.

Step 10: Determine which of the two data bits displayed on the oscilloscope is occurring last. (In the example shown in Figure 5-3, the track 2 read data bit occurs later than the track 1 read data bit.) The track in which the data bit is occurring last is used as the comparison track for the next step.

NOTE

Figure 5-3 illustrates the hypothetical timing relationship between the amplified read data outputs of each track in a 7-track system; a 9-track system would have two additional amplified read data outputs. The relationship shown is for example only, the actual time at which each bit occurs is determined by the gap-scatter of the read heads in the system being adjusted.

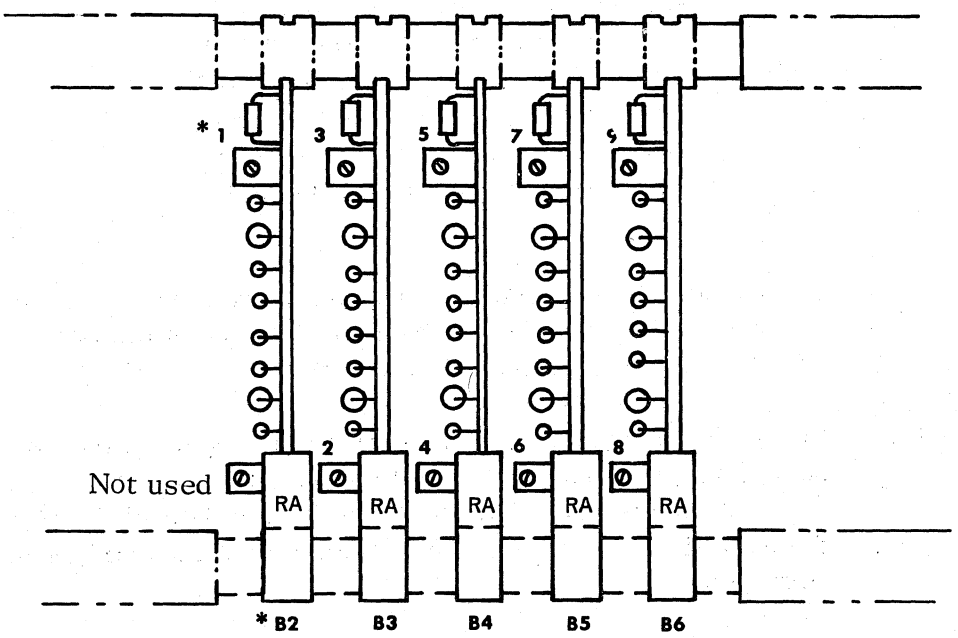
Step 11: Connect the oscilloscope to observe the read signal at pin 12 of the track 3 read deskew PCB at A4 and at pin 12 of the comparison track read deskew PCB selected in Step 10.

Step 12: Determine which of the two data bits displayed on the oscilloscope is occurring last. (In the example shown in Figure 5-3, the track 2 read data bit occurs later than the track 3 read data bit.) The track in which the data bit is occurring last is used as the comparison track for the next step.

TABLE 5-2
READ AMPLIFIER ADJUSTMENTS

TRACK	*OSCILLOSCOPE CONNECTION	POTENTIOMETER	
		LOCATION	REF DES
1	A2-12	B2 top	2R11
2	A3-12	B3 bottom	1R11
3	A4-12	B3 top	2R11
4	A5-12	B4 bottom	1R11
5	A6-12	B4 top	2R11
6	A7-12	B5 bottom	1R11
7	A8-12	B5 top	2R11
8	A9-12	B6 bottom	1R11
9	A10-12	B6 top	2R11

*Read Amplifier adjustments are observed on Read Deskew PCBs.



*Read Track and PCB Designations for Reference Only

Figure 5-2
Read Amplifier Adjustments

Step 13: Repeat Steps 11 and 12 for the remaining read data tracks to determine which data bit of the character is occurring last. Refer to Table 5-3 for the location of the read deskew PCB assemblies. (In the example shown in Figure 5-3, track 2 would be used as the comparison track until the read data bits of tracks 2 and 5 are compared. The track 5 read data bit occurs later than the track 2 read data bit, thus track 5 would be used as the comparison track for track 6. The track 6 read data bit occurs later than the track 5 read data bit, thus track 6 would be used as the comparison track for track 7. The track 6 read data bit occurs later than the track 7 read data bit, thus the track 6 read data bit of the character occurs last in the example.) The track in which the data bit is occurring last is used as the selected reference track for the next step.

Step 14: Connect the channel B input of the oscilloscope to observe the negative-going read deskew delay pulse at pin 34 of the selected reference track read deskew PCB.

Step 15: Adjust R25 (top potentiometer) on the selected reference track read deskew PCB so that the read deskew delay pulse is at the 20-percent point of the delay range, as indicated on the oscilloscope. (See Figure 5-4 for potentiometer location.) For example; if the minimum delay time obtained by adjusting R25 fully counterclockwise is 10 μsec and the maximum delay time obtained by adjusting R25 fully clockwise is 25 μsec, 20-percent of the 15-μsec delay range is 3 μsec, thus the delay time is set to 13 μsec (10 μsec minimum plus 3 μsec for 20-percent of the delay range).

Step 16: Connect pin 34 of the selected reference track read deskew PCB to the external trigger input of the oscilloscope.

Step 17: Set the oscilloscope for external (-) trigger.

Step 18: Connect the channel A input of the oscilloscope to observe the negative-going read deskew delay pulse at pin 34 of the center track read deskew PCB at A6 (A5).

Step 19: Superimpose the base lines of the two signals displayed on the oscilloscope.

Step 20: Adjust R25 (top potentiometer) on A6 (A5) to superimpose the trailing-edge of the center-track deskew delay pulse on the trailing-edge of the selected reference track read deskew-delay pulse. The trailing-edge of the center-track pulse will appear on the oscilloscope as a jitter band; the jitter band should be centered over the stable trailing-edge of the selected reference track pulse.

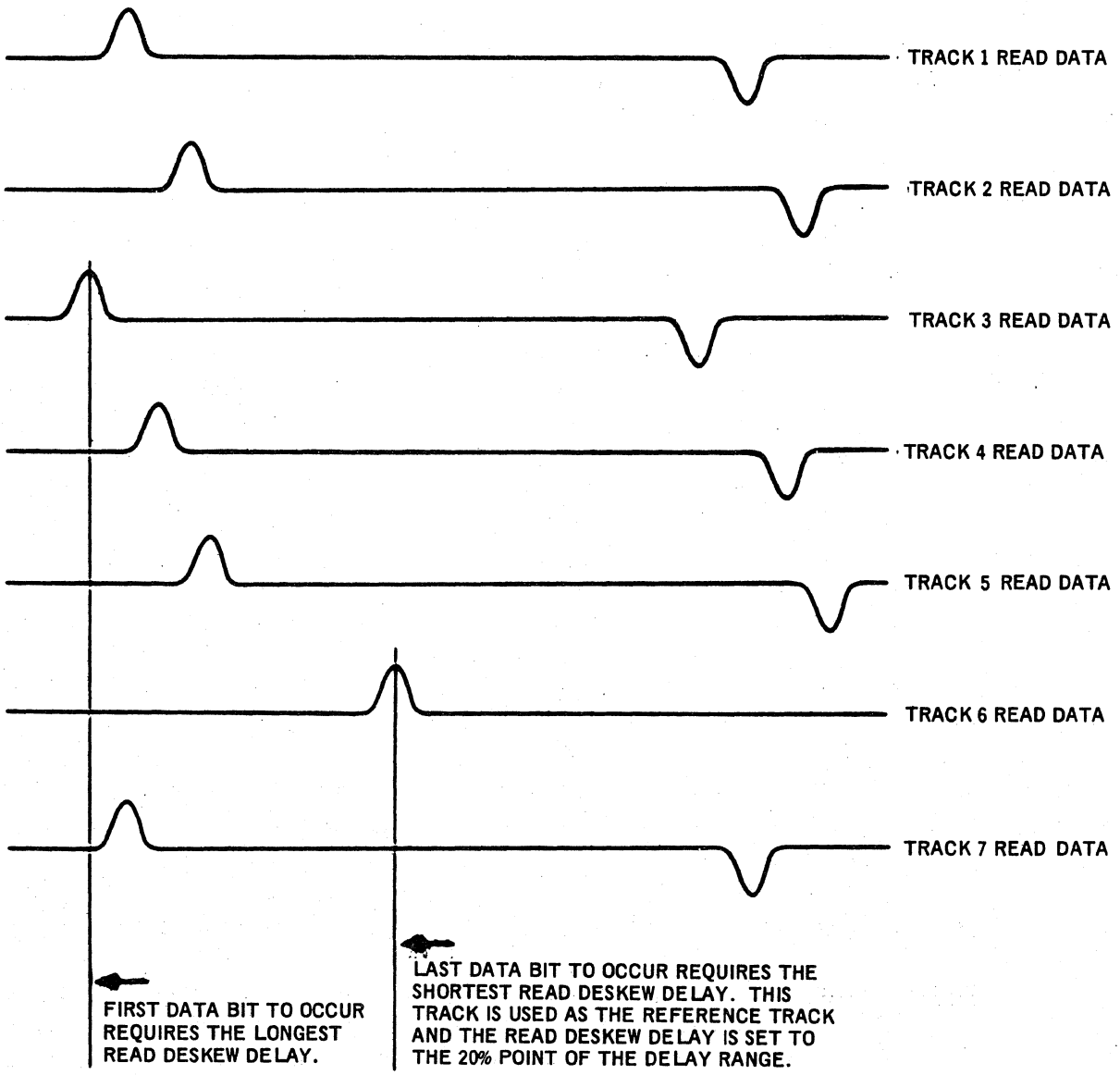


Figure 5-3
Read Deskew Reference Track Selection
(Example Only)

TABLE 5-3
READ DESKEW PCB LOCATION

TRACK	LOCATION
1	A2
2	A3
3	A4
4	A5
5	A6
6	A7
7	A8
8	A9*
9	A10*

*9-track system only.

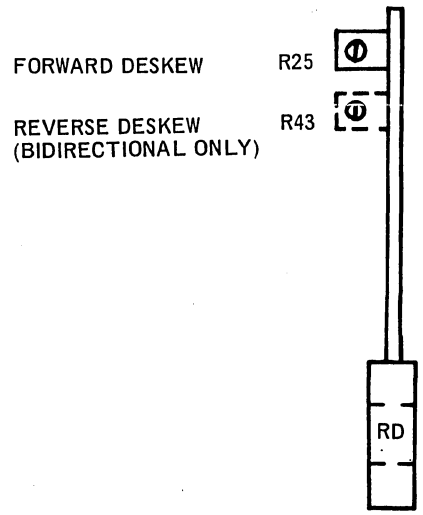


Figure 5-4
Read Deskew Potentiometer Location

Step 21: Disconnect the external trigger input to the oscilloscope from pin 34 of the selected reference track read deskew PCB and connect to pin 34 of the center track read deskew PCB.

Step 22: Connect the channel B input of the oscilloscope to observe the track 1 read deskew delay pulse at pin 34 of the read deskew PCB at A2.

Step 23: Adjust R25 (top potentiometer) on A2 to superimpose the trailing-edge (jitter band) of the track 1 read deskew delay pulse on the trailing edge of the center track read deskew delay pulse.

Step 24: Adjust the read forward deskew delay times for the remaining tracks by following the procedures of Steps 22 and 23. Refer to Table 5-3 for the location of the read deskew PCB assemblies.

Step 25: When the read forward deskew delay times of all tracks have been set, connect the channel B input of the oscilloscope to observe the OR'ed Clock signal at pin 35 of any read deskew PCB. The jitter band of the OR'ed Clock signal should not exceed 2 μsec*. If the jitter band exceeds 2 μsec*, repeat Steps 16 through 25.

Step 26: When the read forward deskew adjustments are completed, stop the tape. If the data electronics contains bidirectional-read circuits, proceed to Step 27. If the data electronics contains unidirectional-read circuits, the read deskew adjustment is completed. Disconnect the oscilloscope, unload the master tape from the transport, and remove the extender board.

*For 75 ips tape speed only. For other tape speeds, the jitter band change is inversely proportional to the tape speed change. For example, the jitter band is approximately 4 μsec at 36 ips.

Step 27: Set the oscilloscope for internal trigger.

Step 28: Repeat Steps 7 through 13, except run the tape in the reverse direction, to determine which data bit of a character is occurring last. The track in which the data bit is occurring last is used as the selected reference track for the next step.

Step 29: Connect the channel B input of the oscilloscope to observe the negative-going read deskew delay pulse at pin 34 of the selected reference track read deskew PCB.

Step 30: Adjust R43 (bottom potentiometer) on the selected reference track read deskew PCB so that the read deskew delay pulse is at the 20-percent point of the delay range, as indicated on the oscilloscope. (See Figure 5-4 for potentiometer location.) For example, if the minimum delay time obtained by adjusting R43 fully counterclockwise is 10 μsec and the maximum delay time obtained by adjusting R43 fully clockwise is 25 μsec, 20-percent of the 15-μsec delay range is 3 μsec, thus the delay time is set to 13 μsec (10 μsec minimum plus 3 μsec for 20-percent of the delay range).

Step 31: Connect pin 34 of the selected reference track read deskew PCB to the external trigger input of the oscilloscope.

Step 32: Set the oscilloscope for external (-) trigger.

Step 33: Connect the channel A input of the oscilloscope to observe the negative-going read deskew delay pulse at pin 34 of the center track read deskew PCB at A6 (A5).

Step 34: Superimpose the base lines of the two signals displayed on the oscilloscope.

Step 35: Adjust R43 (bottom potentiometer) on A6 (A5) to superimpose the trailing-edge of the center-track read deskew delay pulse on the trailing-edge of the selected reference track read deskew delay pulse. The trailing edge of the center-track pulse will appear on the oscilloscope as a jitter band; the jitter band should be centered over the stable trailing-edge of the selected reference track pulse.

Step 36: Disconnect the oscilloscope external trigger input from pin 34 of the selected reference track read deskew PCB and connect to pin 34 of the center track read deskew PCB.

Step 37: Connect the channel B input of the oscilloscope to observe the track 1 read deskew delay pulse at pin 34 of the read deskew PCB at A2.

Step 38: Adjust R43 (bottom potentiometer) on A2 to superimpose the trailing-edge (jitter band) of the track 1 read deskew delay pulse on the trailing edge of the center track read deskew delay pulse.

Step 39: Adjust the read reverse deskew delay times for the remaining tracks by following the procedures of Steps 37 and 38. It is not necessary to re-adjust the read deskew delay time of the selected reference track. Refer to Table 5-3 for the location of the read deskew PCB assemblies.

Step 40: When the read reverse deskew delay times of all tracks have been set, connect the oscilloscope to observe the OR'ed Clock signal at pin 35 of any read deskew PCB. The jitter band of the OR'ed Clock signal should not exceed 2 μsec*. If the jitter band exceeds 2 μsec*, repeat Steps 31 through 40.

Step 41: When the read reverse deskew adjustments are completed, stop the tape and disconnect the oscilloscope. Unload the master tape from the transport.

5-7. WRITE CHECK.

The Write Check procedures are performed with the system performing the write and read function. The write permit and read permit levels must be set TRUE and the transport placed in the Remote Mode of operation. Select high density on the OCP. Verify that the write operation is being performed by checking the write amplifiers.

Step 1: Install the write enable ring. Load a scratch-pad tape on the transport. Set the Write Permit and Read Permit inputs TRUE. Write all ONEs at the high density rate.

Step 2: Connect the oscilloscope to observe the signal at pin 34 of the track 1 write amplifier at A14. A voltage spike of approximately 10 volts should occur for every other current transition through the write head.

Step 3: Connect the oscilloscope to observe the signal at pin 30 of the track 1 write amplifier. A voltage spike of approximately 10 volts should occur for every other current transition through the write head.

Step 4: Repeat the procedures of Steps 2 and 3 for the remaining tracks. Refer to Table 5-4 for the location of the write amplifier PCB assemblies.

*For 75 ips tape speed only. For other tape speeds, the jitter band change is inversely proportional to the tape speed change. For example, the jitter band is approximately 4 μsec at 36 ips.

5-8. WRITE DESKEW.

The write deskew adjustment is made while reading the tape as a series of ONEs is being written. The skew correction is accomplished by setting the delay time of each write deskew single-shot. (The write deskew single-shots are located on the write amplifier PCB assemblies.) A reference track is selected and the trailing edge of the center track (track 5 in 9-track systems, track 4 in 7-track systems) read deskew delay pulse is aligned with the trailing edge of the selected reference track read deskew delay pulse. The center track is then used as the reference track during the write deskew adjustment. The read amplifier gain is adjusted to ensure that the read amplifier output is normal for write check operation before setting the write deskew single-shot delay times. Steps 6 through 8 pertain to the read amplifier gain adjustment. Refer to Table 5-4 for the location of the write amplifier PCB assemblies and see Figure 5-5 for the location of the write deskew potentiometer.

Where two potentiometer or test point references are given in an adjustment procedure, the reference not in parenthesis pertains to 9-track systems and the reference in parenthesis pertains to 7-track systems.

Step 1: Load a new, blank tape (or a blank tape known to be in good condition) on the tape transport, with a write enable ring in place on the reel.

Step 2: Set the Write Permit, Read Permit, Select, and all Write Data inputs to the TRUE level.

Step 3: Select Remote Mode at the OCP. When the REMOTE indicator goes ON, the system is ready for operation.

Step 4: Program the tape transport to run the tape forward.

TABLE 5-4
WRITE AMPLIFIER PCB LOCATION

TRACK	LOCATION
1	A14
2	A15
3	A16
4	A17
5	A18
6	A19
7	A20
8	A21*
9	A22*

*9-track system only.

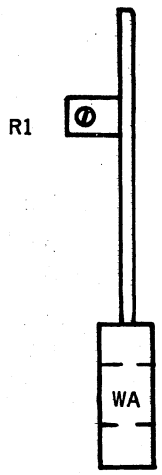


Figure 5-5
Write Deskew Potentiometer Location

Step 5: Write all ONEs at the normal density rate (the Write Strobe period is 16.67 μsec for an 800 cpi density at a tape speed of 75 ips).

Step 6: Connect an oscilloscope to observe the read signal at pin 12 of the track 1 read deskew PCB at A2. Set the vertical sensitivity of the oscilloscope to 2 v/cm. Adjust the oscilloscope horizontal sweep rate as required to observe the read signal envelope (sweep rate approximately 50 μsec/cm for a tape speed of 75 ips).

Step 7: Adjust 2R11 (top potentiometer) on the read amplifier (RA) PCB at pin 32 to obtain a read signal amplitude of 8 volts peak-to-peak, as indicated on the oscilloscope. This completes the read amplifier gain adjustment for read data track 1.

Step 8: Repeat Steps 6 and 7 for each of the remaining read data tracks. Refer to Table 5-2 for the read amplifier adjustment and test point locations. See Figure 5-2 for the location of the read amplifier PCB assemblies. Refer to Table 5-3 for the location of the read deskew PCB assemblies.

Step 9: Set the oscilloscope controls for DC vertical input, 2 v/cm vertical sensitivity, 1 μsec/cm horizontal sweep rate, and internal (+) trigger.

Step 10: Connect the channel A input of the oscilloscope to observe the negative-going write deskew delay pulse at test point TP1 of the track 1 write amplifier PCB at A14.

Step 11: Adjust potentiometer R1 on A14 so that the write deskew delay pulse is at the 20-percent point of the delay range, as indicated on the oscilloscope. (See Figure 5-5 for potentiometer location.) For example; if the minimum delay time obtained by adjusting R1 fully counterclockwise is 10 μsec and the maximum delay time obtained by adjusting R1 fully clockwise is 25 μsec, 20-percent of the 15-μsec delay range is 3 μsec, thus the delay time is set to 13 μsec (10 μsec minimum plus 3 μsec for 20-percent of the delay range).

Step 12: Connect test point TP1 of the track 1 write amplifier to the external trigger input of the oscilloscope.

Step 13: Set the oscilloscope for external (-) trigger.

Step 14: Connect the channel B input of the oscilloscope to observe the negative-going write deskew delay pulse at test point TP1 of the track 2 write amplifier PCB at A15.

Step 15: Superimpose the base lines of the two signals displayed on the oscilloscope.

Step 16: Adjust R1 on A15 to superimpose the trailing edge of the track 2 write deskew delay pulse on the trailing edge of the track 1 write deskew delay pulse. The trailing edge of the track 2 pulse will appear on the oscilloscope as a jitter band; the jitter band should be centered over the stable trailing edge of the track 1 pulse.

Step 17: Connect the channel B input of the oscilloscope to observe the write deskew delay pulse at test point TP1 of the track 3 write amplifier PCB at A16.

Step 18: Adjust potentiometer R1 on A16 to superimpose the trailing-edge (jitter band) of the track 3 write deskew delay pulse on the trailing edge of the track 1 write deskew delay pulse.

Step 19: Adjust the write-deskew delay times for the remaining tracks by following the procedures of Steps 17 and 18. Refer to Table 5-4 for the location of the write amplifier PCB assemblies.

Step 20: Connect the channel A input of the oscilloscope to observe the read signal at pin 12 of the track 1 read deskew (RD) PCB at A2.

Step 21: Connect the channel B input of the oscilloscope to observe the read signal at pin 12 of the track 2 read deskew (RD) PCB at A3.

Step 22: Separate the base lines of the two signals displayed on the oscilloscope.

Step 23: Determine which of the two data bits displayed on the oscilloscope is occurring last. (In the example shown in Figure 5-3, the track 2 read data bit occurs later than the track 1 read data bit.) The track in which the data bit is occurring last is used as the comparison track for the next step.

NOTE

Figure 5-3 illustrates the hypothetical timing relationship between the amplified read data outputs of each track in a 7-track system; a 9-track system would have two additional amplified read data outputs. The relationship shown is for example only, the actual time at which each bit occurs is determined by the gap-scatter of the write heads in the system being adjusted. (The gap-scatter of the read heads is compensated for by the read deskew adjustment.)

Step 24: Connect the oscilloscope to observe the read signals at pin 12 of the track 3 read deskew PCB at A4 and at pin 12 of the comparison track read deskew PCB selected in Step 23.

Step 25: Determine which of the two data bits displayed on the oscilloscope is occurring last. (In the example shown in Figure 5-3, the track 2 read data bit occurs later than the track 3 read data bit.) The track in which the data bit is occurring last is used as the comparison track for the next step.

Step 26: Repeat Steps 24 and 25 for the remaining read data tracks to determine which data bit of the character is occurring last. Refer to Table 5-3 for the location of the read deskew PCB assemblies. (In the example shown in Figure 5-3, track 2 would be used as the comparison track until the read data bits of tracks 2 and 5 are compared. The track 5 read data bit occurs later than the track 2 read data bit, thus track 5 would be used as the comparison track for track 6. The track 6 read data bit occurs later than the track 5 read data bit, thus track 6 would be used as the comparison track for track 7. The track 6 read data bit occurs later than the track 7 read data bit, thus the track 6 read data bit of the character occurs last in the example.) The track in which the data bit is occurring last is used as the selected reference track for the next step.

Step 27: Connect the channel B input of the oscilloscope to observe the negative-going read deskew delay pulse at pin 34 of the selected reference track read deskew PCB.

Step 28: Connect pin 34 of the selected reference track read deskew PCB to the external trigger input of the oscilloscope.

Step 29: Set the oscilloscope for external (-) trigger.

Step 30: Connect the channel A input of the oscilloscope to observe the negative-going read deskew delay pulse at pin 34 of the center track read deskew PCB at A6 (A5).

Step 31: Superimpose the base lines of the two signals displayed on the oscilloscope.

Step 32: Adjust potentiometer R1 on the center track write amplifier PCB at A18 (A17) to superimpose the trailing edge of the center-track read deskew delay pulse on the trailing edge of the selected reference track read deskew delay pulse. The trailing edge of the center-track pulse will appear on the oscilloscope as a jitter band; the jitter band should be centered over the stable trailing edge of the selected reference track pulse.

Step 33: Disconnect the oscilloscope external trigger input from pin 34 of the selected reference track read deskew PCB and connect to pin 34 of the center track read deskew PCB.

Step 34: Connect the channel B input of the oscilloscope to observe the track 1 read deskew delay pulse at pin 34 of the read deskew PCB at A2.

Step 35: Adjust potentiometer R1 on the track 1 write amplifier PCB at A14 to superimpose the trailing edge (jitter band) of the track 1 read deskew delay pulse on the trailing edge of the center track read deskew delay pulse.

Step 36: Adjust the write deskew delay times for the remaining tracks by following the procedures of Steps 34 and 35. It is not necessary to readjust the write deskew delay time of the selected reference track. Refer to Tables 5-3 and 5-4 for the location of the read deskew and write amplifier PCB assemblies, respectively.

CAUTION

Do not change the read deskew delay adjustments. An alignment master tape must be used to set the read deskew delay adjustments.

Step 39: When the write deskew delay times have been set, the write deskew adjustment is complete. Stop the tape and disconnect the oscilloscope. Unload the tape from the transport.

5-9. READ STROBE DELAY.

The read strobe delay adjustment is made while reading the tape as a series of ONEs is being written at the required data transfer rate. Two read strobe delay times are set: one for high density packing, the other for low density packing. Steps 9 through 11 pertain to the strobe delay time adjustment for high density packing, Steps 12 through 14 pertain to the strobe delay time adjustment for low density packing.

The read strobe delay adjustment procedure includes read strobe delay adjustments for density/speed combinations of 800 cpi at 75 ips and 556 cpi at 75 ips. Refer to Table 5-5 for the read strobe delays required at other density/speed combinations.

Step 1: Load a new, blank tape (or a blank tape known to be in good condition) on the tape transport, with a write enable ring in place on the reel.

TABLE 5-5
READ STROBE DELAY TIME*

DENSITY	36 IPS	45 IPS	75 IPS	112.5 IPS	120 IPS	150 IPS
200 cpi	69 μsec	56 μsec	33 μsec	22.0 μsec	29.0 μsec	16.7 μsec
556 cpi	25 μsec	20 μsec	12 μsec	8.0 μsec	7.0 μsec	6.0 μsec
800 cpi	17 μsec	14 μsec	8 μsec	5.5 μsec	5.2 μsec	4.0 μsec

*Read Strobe Delay Time = 1/2 Character Frame Period

Step 2: Set the Write Permit, Read Permit, Select, and all Write Data inputs to the TRUE level.

Step 3: Select Remote Mode at the OCP. When the REMOTE indicator goes ON, the system is ready for operation.

Step 4: Connect the channel A input of an oscilloscope to observe the negative-going OR Clock signals at pin 10 of the strobe generator PCB at B8.

Step 5: Connect pin 10 of B8 to the external trigger input of the oscilloscope.

Step 6: Connect the channel B input of the oscilloscope to observe the positive-going Read Strobe (+) pulse at pin 24 of B8.

Step 7: Set the oscilloscope controls for DC vertical input, 2 v/cm vertical sensitivity, 1 μsec/cm horizontal sweep rate, external (-) trigger, and chopped channel display.

Step 8: Program the tape transport to run the tape forward.

Step 9: Select high density operation at the OCP.

Step 10: Write all ONEs at the high density rate (the Write Strobe period is 16.67 μsec for an 800 cpi density at a tape speed of 75 ips).

Step 11: Adjust R13 (top potentiometer) on B8 to obtain a read strobe delay of 8 μsec* between the leading edge of the first OR Clock signal and the trailing edge of the following Read Strobe (+) pulse, as indicated on the oscilloscope. The timing relationship of the two signals is shown in Figure 5-6. See Figure 5-1 for potentiometer location.

Step 12: Select low density operation at the OCP.

*For 800 cpi at 75 ips. Refer to Table 5-5 for the read strobe delay required at other density/speed combinations.

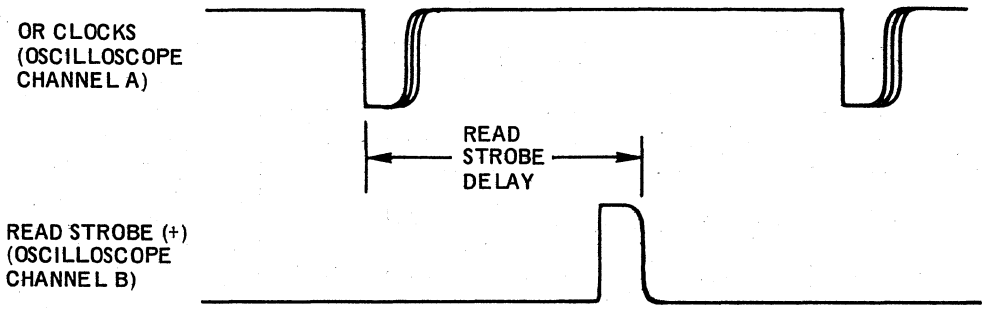


Figure 5-6
Read Strobe Delay Timing

Step 13: Write all ONEs at the low density rate (the Write Strobe period is 24 μsec for a 556 cpi density at a tape speed of 75 ips).

Step 14: Adjust R14 (second-from-top potentiometer) on B8 to obtain a read strobe delay of 12* μsec between the leading edge of the OR Clock signal and the trailing edge of the following Read Strobe (+) pulse, as indicated on the oscilloscope. This completes the read strobe delay adjustment.

NOTE

Systems Operating at 150 IPS.

Under worst case program conditions at 150 IPS, the cumulative timing errors introduced by dynamic skew and instantaneous speed variation (ISV) can cause a read register flip-flop set (OR Clock leading edge) and the read register reset (Read Strobe trailing edge) conditions to occur simultaneously or almost simultaneously. These conflicting commands to the read register flip-flop can cause a read data error. The following read strobe delay adjustment should be used if the read strobe timing is causing read data errors.

Connect the oscilloscope to observe the OR Clock and Read Strobe pulses. (Use the worst case program that produced the read data errors.) Adjust the read strobe delay as required to provide a guardband of approximately 1 μsec between the Read Strobe pulse and the nearest OR Clock pulse.

Step 15: Stop the tape and disconnect the oscilloscope. Unload the tape from the transport.

*For 556 cpi at 75 ips. Refer to Table 5-5 for the read strobe delay required at other density/speed combinations.

5-10. RATE CHECK REFERENCE TIME.

The rate check reference time adjustment is made while reading the tape as a series of ONEs is being written at the required data transfer rate. An error signal is produced when the interval between successive read strobe pulses is less than approximately 67-percent of the nominal interval.

The rate check reference time adjustment procedure includes rate check reference time adjustments for the density/speed combination of 800 cpi at 75 ips. Refer to Table 5-6 for the rate check reference time required at other density/speed combinations.

TABLE 5-6
RATE CHECK REFERENCE TIME*

DENSITY	36 IPS	45 IPS	75 IPS	112.5 IPS	120 IPS	150 IPS
556 cpi	33 μsec	27 μsec	16 μsec	11.0 μsec	10.9 μsec	8.0 μsec
800 cpi	23 μsec	19 μsec	11 μsec	7.4 μsec	6.9 μsec	5.6 μsec

*Rate Check Reference Time = 2/3 Character Frame Period.

Step 1: Load a new, blank tape (or a blank tape known to be in good condition) on the tape transport, with a write enable ring in place in the reel.

Step 2: Set the Write Permit, Read Permit, Select, and all Write Data inputs to the TRUE level.

Step 3: Select Remote Mode at the OCP. When the REMOTE indicator goes ON, the system is ready for operation.

Step 4: Connect the channel A input of an oscilloscope to observe the negative-going Read Register Reset (-) pulse at pin 23 of the error check PCB at B12.

Step 5: Connect pin 23 of B12 to the external-trigger input of the oscilloscope.

Step 6: Connect the channel B input of the oscilloscope to observe the negative-going rate error delay B pulse at pin 27 of the error check PCB at B12.

Step 7: Set the oscilloscope controls for DC vertical input, 2 v/cm vertical sensitivity, 2 μsec/cm horizontal sweep rate, external (-) trigger, and chopped channel display.

Step 8: Program the tape transport to run the tape forward.

Step 9: Select high density operation at the OCP.

Step 10: Write all ONEs at the high density rate (the Write Strobe period is 16.67 μsec for an 800 cpi density at a tape speed of 75 ips).

Step 11: Adjust potentiometer R12 on B12 to obtain a rate check reference time of 11 μsec* between the leading edge of the Read Register Reset (-) signal and the trailing edge of the following rate error delay B pulse, as indicated on the oscilloscope. The timing relationship of the two signals is shown in Figure 5-7. This completes the rate check reference time adjustment.

Step 12: Stop the tape and disconnect the oscilloscope. Unload the tape from the transport.

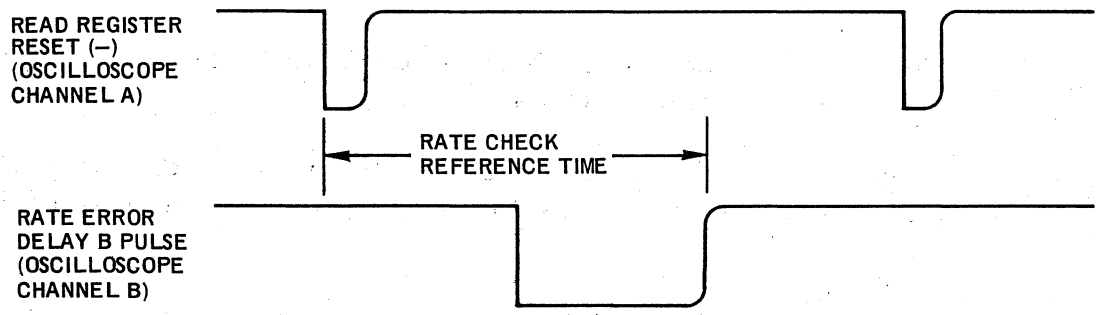


Figure 5-7
Rate Check Reference Timing

*For 800 cpi at 75 ips. Refer to Table 5-6 for the rate check reference time required at other density/speed combinations.

5-11. ALTERNATE ADJUSTMENT PROCEDURE.

The alternate adjustment procedure may be used to make off-line adjustments. The tape transport must be in the LOCAL mode when making off-line adjustments.

5-12. GENERAL.

The output of a square-wave generator may be applied to test points TP1 and TP2 (TP2 is ground) to write a series of ONEs on all tracks. Verify transport and power supply adjustments. Sequence of off-line adjustments are the same as listed in paragraph 5-4.

CAUTION

To prevent accidental damage to external equipment, disconnect the input at connector J5 of the data electronics.

5-13. Clipping Level. The clipping level is adjusted in the manner described in paragraph 5-5. The input buffer PCB at B16 is extracted from B16 to simulate a Write Permit TRUE signal.

5-14. Read Deskew. The read deskew adjustments are as described in paragraph 5-6. For a read forward only system, ensure that -12 volts (TRUE) is at pin 21 of the read deskew PCB. For a bidirectional read system, connect -12 volts to pin 26 of J5 on the data electronics before performing forward deskew adjustment. For reverse deskew adjustment, remove the -12 volts from pin 26 of J5 and connect 0 volts to pin 26.

CAUTION

Ensure that the square-wave generator is terminated with the correct load resistance.

5-15. Write Check. The write check and write deskew adjustments are made in the manner described in paragraphs 5-7 and 5-8, with the following exceptions.

Connect a square-wave generator to TP1 and TP2 on the data electronics assembly. Simulate Write Permit and Run/Stop TRUE by removing the input buffer PCB from B16. Set the frequency of the square-wave generator according to Table 5-7. Adjust the output amplitudes for 0 and -12 volts. For a bidirectional read system, connect -12 volts to pin 26 of J5 on the data electronics.

5-16. Read Strobe Delay and Rate Check Reference Time. The read strobe delay and rate check reference time adjustments are made in the manner described in paragraphs 5-9 and 5-10, with the following exceptions. The square-wave generator is connected as described in paragraph 5-15. The generator frequencies required to simulate the bit density are listed in Table 5-7.

TABLE 5-7
TEST DESKEW INPUT REQUIREMENT
(SYSTEM DATA TRANSFER RATE)

DENSITY	36 IPS	45 IPS	75 IPS	112.5 IPS	120 IPS	150 IPS
200 cpi	7.2 kHz	9.0 kHz	15.0 kHz	22.5 kHz	24.0 kHz	30.0 kHz
556 cpi	20.0 kHz	25.0 kHz	41.7 kHz	62.5 kHz	66.7 kHz	83.4 kHz
800 cpi	27.8 kHz	36.0 kHz	60.0 kHz	90.0 kHz	96.0 kHz	120.0 kHz

5-17. TROUBLESHOOTING PROCEDURE.

The data electronics circuits are on plug-in type printed circuit boards (PCBs). The troubleshooting charts, Tables 5-9 and 5-10, facilitate the isolation of the malfunctioning PCB. The location and function of each PCB is shown in Figure 2-1.

The Theory of Operation in Section IV, the Printed Circuit Descriptions in Section VI, and the logic diagram in Section VII provide the information required for more extensive troubleshooting.

Check the equipment for evidence of damage, that no wires are disconnected, and that the PCBs are firmly seated in the connector at the proper location.

5-18. PRELIMINARY TESTS.

Establish that the input signals controlling the data electronics are as required. Table 5-8 lists the input function, the signal requirement, and the test point. These tests are made at the output of the buffer amplifiers. Should the input signals not be as required, the possibility of a malfunctioning input buffer PCB exists. A check may be made by exchanging the PCB at B16 with the PCB at B15. Use an oscilloscope to make all tests. Refer to the logic diagram in Section VII while performing all tests.

A write operation cannot be performed unless at least one Write Data input line is TRUE. The input data may be coincident with the Write Strobe pulse or may be held in the TRUE condition by a continuous -9 to -25 volt level. Removing the input buffer PCB at B15 will have the effect of conditioning tracks 1 through 8 to write all ONEs.

To determine that the write operation is being performed, connect the oscilloscope input lead to pin 24 of any write amplifier PCB at A14 through A22. A 10-volt spike should be present. The repetition rate is a function of the Write Strobe rate.

The read function is controlled by the read permit level and the strobe generator. Should no data output be present, determine if data is being read by any of the read tracks by checking the OR Clock pulse at pin 10 of the strobe generator PCB at B8. A negative-going pulse should be observed. The repetition rate will be determined by the data transfer frequency. Should the test confirm that data is being read by the read heads, but no data is being presented to the outputs, investigate the condition of the Read Permit line at pin 9 of the write power gate PCB at A24. The level of read permit at this point must be 0 volts. Should the level not be 0 volts, replace the write power gate. The Read Strobe and the Read Register Reset pulses must be present at pins 24 and 22 of the strobe generator PCB at B8; the Read Strobe pulse is positive-going, the Read Register Reset pulse is the inverse of the strobe pulse. Should the signals not be as indicated in the preceding test, replace strobe generator B8.

TABLE 5-8
INPUT SIGNALS

INPUT FUNCTION	TEST POINT	SIGNAL
Write Reset	B16-14	0V
Write Permit	B16-20	-12V
Write Strobe	B16-22	-12V pulses
Read Permit	B16-26	-12V
Run/Stop (or Fwd/Stop)	B16-28	-12V

5-19. TROUBLESHOOTING TABLES.

Troubleshooting Tables 5-9 and 5-10 may be used as a guide to further investigate any malfunction existing in the data electronics.

TABLE 5-9
WRITE SECTION TROUBLESHOOTING PROCEDURE

MALFUNCTION	FAILURE INDICATION	REMEDY
1. No head driver output on any track as measured at pins 30 and 34 of PCBs A14 through A22	A. Input Buffer output at B16-20 is at 0 volts	Replace PCB B16
	B. Output of Write Power Gate at pins A24-28, -29, and -30 is at 0 volts	Verify that Write Enable Ring is in place. If ring is in place and the malfunction still exists, replace PCB A24
	C. Write Register Reset output at B8-30 is +12 volts when Write Permit at B8-28 and Run at B8-20 are at -6 to -12 volts	Replace PCB B8
	D. Either a constant 0 volts or a constant -12 volts Write Strobe signal at B16-22	Replace PCB B16
2. No head driver output on a particular track as measured at pins 30 and 34 of PCBs A14 through A22	A. Write Data output from the input buffer of the malfunctioning track remains at 0 volts when ONEs are being written on that track	Replace the PCB corresponding to the malfunctioning track
	B. Input to the Write Amplifier is negative and the Write Strobe is present, but no output at pins 30 and 34 of the Write Amplifier	Replace Write Amplifier PCB associated with the malfunctioning track (A14 through A22)

TABLE 5-10
READ SECTION TROUBLESHOOTING PROCEDURE

MALFUNCTION	FAILURE INDICATION	REMEDY
1. No output on any track as measured at the output of the output drivers	A. Read Permit output at B16-26 is at 0 volts	Replace PCB B16
	B. Read Register DC Reset at A24-9 is at -6 volts	Replace PCB A24
	C. OR Data input at B8-10 remains at a constant -6 volts	One of the Read Deskew Boards A2 through A10 is malfunctioning. Replace malfunctioning PCB.
	D. Read Permit is negative at B8-12 and an OR Data signal is present at B8-10 but no Read Strobe pulse at B8-24 or no Read Register Reset output at B8-22	Replace PCB B8
	E. Read Amplifier output of 6 to 8 volts peak-to-peak at pins 12 and 14 of A2 through A10 but no OR Data output at pin 35 of A2 through A10. Clipping Level input at pins 24 of A2 through A10 at -10 volts or greater	Decrease clipping level (refer to paragraph 5-5). If clipping level will not decrease, replace PCB B8
	F. No Read Register Reset output at B8-22 or no Read Strobe at B8-24 when OR data is present at B8-10. Both High and Low Density Select at B8-34 and B9-35 are at a voltage other than -12 volts	Replace PCB A24.

TABLE 5-10
READ SECTION TROUBLESHOOTING PROCEDURE
(Continued)

MALFUNCTION	FAILURE INDICATION	REMEDY
2. No output from a particular track at the output of the Output Driver	A. No Read Amplifier output at pins 12 and 14 of the Read Deskew boards of the malfunctioning track	Adjust Read Amplifier of malfunctioning track. (Refer to paragraph 5-8.) If malfunction is not corrected, replace Read Amplifier board and adjust. If malfunction still exists, replace Read Deskew board of malfunctioning track
	B. No output at pin 32 of the Read Deskew board of the malfunctioning track, but 6 to 8 volts peak-to-peak measured at pins 12 and 14 of that PCB	Replace Read Deskew PCB of the malfunctioning track
	C. No output signal from the output driver of the malfunctioning track even though both inputs to the output driver are TRUE	Replace PCB B13 or B14

SECTION VI
CIRCUIT DESCRIPTIONS

6-1. INTRODUCTION.

This section contains detailed circuit descriptions of typical printed circuit board assemblies used in the data electronics. The circuit descriptions are in alphabetical sequence by mnemonic coded designation. Schematic diagrams and assembly drawings are located in Section VII.

TABLE 6-1
LIST OF CIRCUIT DESCRIPTIONS

CODE	CIRCUIT DESCRIPTION	SCHEMATIC
ECC	Error Check	3109873
EOA	Exclusive OR	3104452
IBA	Input Buffer	3107038
ODA	Output Driver	3107043
RAB	Read Amplifier	3107118
RDB	Read Deskew	3107253
RDC	Read Deskew, Bidirectional	3109930
SGA	Strobe Generator	3107058
SLB	Select Logic	3111158
WAB	Write Amplifier	3112345
WPD	Write Power Gate	3107128

1. GENERAL DESCRIPTION.

This card contains the circuits required to perform the Write Check function.

2. THEORY OF OPERATION.

The Write Check function checks the read-after-write data for Parity, Rate and Echo errors. The outputs of the Parity, Rate and Echo check circuits are ORed together such that a Write Check error is generated at the card output if either a Parity, Rate or Echo error is generated.

Parity. The Parity input is ANDed with the Read Register Reset by the AND gate made up of R17 and CR10. The Read Register Reset pulse occurs simultaneously with the Read Clock. The output of the AND gate drives diode CR13, which is an input to the OR gate driving Q6.

Rate Check. The Rate Check circuit checks the period between successive Read Register Reset pulses and generates an output from the AND gate made up of CR11, CR12, and R18 whenever the period between Reset pulses decreases beyond an adjustable threshold. The Rate circuit operates as follows.

A negative Register Reset pulse turns Q1 ON, forcing the single-shot SS-1 (Q2 and Q3) to trigger. At the end of single-shot SS-1's delay, the single-shot SS-2 (Q4 and Q5) is set. The output of SS-2 is ANDed with the next arriving Register Reset pulse. The sum of the delays of SS-1 and SS-2 is adjusted by potentiometer R12 to give a total delay of 0.67 (1/upper Data Transfer frequency). Under normal conditions the next arriving Register Reset pulse will not coincide with the output of SS-2 and the AND gate will give no output. If the tape speed was slow at the time of writing such that the distance between frames was decreased to 0.67 (normal frame time) or less, then coincidence will occur at the AND gate and a Rate Error will be indicated.

Echo Check. The Echo Check circuit verifies that at least one Head Driver changes state after each Write Strobe. The Echo Check circuit operates as follows.

The flip-flop made up of transistors Q16 and Q17 is held reset at all times that the Write Amplifiers are reset. This is done by the Write Register DC Reset input at pin 19. When writing, the Write Register DC Reset is FALSE and the flip-flop is no longer forced reset. The Write Strobe input at pin 11 causes the single-shot (SS-3), made up of Q10 and

2. THEORY OF OPERATION. (Continued)

Q11 to trigger. The output of SS-3 is inverted by the inverter made up by Q12. The flip-flop is set by the single-shot at the moment that the single-shot triggers. The input to the AND gate at CR26 is held FALSE for the duration of the delay of SS-3.

The Echo outputs from the Write Amplifiers arrive at pin 15 before the delay of SS-3 ends, and the first arriving Echo resets the flip-flop. If there is no Echo input after a Write Strobe, the flip-flop remains set and at the end of the delay of SS-3, the flip-flop output coincides with the output of the inverter, made up of Q12, and an Echo Error output is generated by the AND gate.

OR Gate. The outputs from the Parity, Rate and Echo AND gates drive the OR gate made up of CR13, CR14, and CR29. This gate drives the circuit made up of Q6 and Q7 which limits the duration of the Write Check Error output pulse. Resistor R24 and diode CR16 make up an AND gate ANDing the Write Permit with the Write Check Error output. Q8 makes up the inverter that repowers the Write Check output.

3. OPERATIONAL CHARACTERISTICS.

FUNCTION	UP LEVEL	DOWN LEVEL
Write Permit	0 ±0.5 volt	-12 volts
Parity	0 ±0.5 volt	-12 volts
Read Register Reset	0 ±0.5 volt	-6 volts most positive
Write Strobe	0 ±0.5 volt	-6 volts
Write Register DC Reset	+12 volts	Open circuit
Echo	+5 volt transition	
Write Check Error	0 ±0.5 volt	-12 volts

4. POWER REQUIREMENTS.

VOLTAGE	CURRENT
+12 VDC ±3%	20 ma
-12 VDC ±3%	78 ma
- 6 VDC ±4%	16 ma

1. GENERAL DESCRIPTION.

This card contains four independent logic elements. Two of the elements require external termination. Each element performs an Exclusive OR function. Electrically, the output assumes UP level only when the polarities of the two inputs are dissimilar.

2. TRUTH TABLE.

INPUT 1	INPUT 2	OUTPUT
-6	-6	-6
-6	0	0
0	-6	0
0	0	-6

3. THEORY OF OPERATION.

Diodes CR1 and CR2 comprise an OR gate. Diodes CR3 and CR4 comprise an AND gate. Transistors Q1 and Q2 are inverters.

Two 0 volt inputs forward bias CR1 and CR2 which conduct and place a positive voltage on the base of Q1 (with respect to the emitter), causing Q1 to cut off. Diodes CR3 and CR4 are back biased and 0 volt appears at the anode of CR6. With Q1 cut off, CR6 is forward biased and conducts, placing 0 volt on the base of Q2. Transistor Q2 is cut off and -6 volts appears at the output.

Zero volt at Input 1 and -6 volts at Input 2 will cause the following sequence of events. Diode CR1 is forward biased and conducts, causing CR2 to be back biased, placing 0 volt on the base of Q1 and causing Q1 to cut off. Diode CR4 is forward biased and conducts, causing CR3 to be back biased and placing -6 volts on the anode of CR6. With Q1 cut off, CR6 is forward biased and conducts, placing -6 volts on the base of Q2. Transistor Q2 conducts and 0 volt appears at the output. When the input voltages are reverse, (-6 volts at Input 1 and 0 volt at Input 2), the circuit action is the same except that diodes CR2 and CR3 conduct and CR1 and CR4 are cut off.

Two -6 volt inputs reverse bias CR1 and CR2 which drives the base of Q1 negative and Q1 conducts. Diodes CR3 and CR4 are forward biased and conduct, placing -6 volts on the anode of CR6. With Q1 conducting and CR6 back biased, the base of Q2 goes positive. Transistor Q2 cuts off and -6 volts appears at the output.

4. OPERATIONAL CHARACTERISTICS

FUNCTION	INPUT		OUTPUT	
	UP LEVEL	DOWN LEVEL	UP LEVEL	DOWN LEVEL
Voltage	0.0V to -0.5V	-5V to -13V	0.0V to 0.5V	-5.7V to -6.7V
Current	5.4 ma max	1 ma max at -6.3V	13.5 ma max	1 ma max
Rise Time			150 ns max*	
Fall Time			1100 ns max*	
Delay	750 ns max** Signal Propagation Delay			

*With 220 pf load returned to ground or 390 pf returned to ground in parallel with 430 ohms returned to -6 volts.

**Total delay of 4 circuits in series.

5. POWER REQUIREMENTS.

VOLTAGE	CURRENT
+12 VDC ±3%	11 ma max
-12 VDC ±3%	60 ma max
- 6 VDC ±4%	6.8 ma max

1. GENERAL DESCRIPTION.

This card contains eight identical, independent input buffer circuits. Each circuit provides a non-inverted output and has an input noise rejection of approximately 5 volts.

2. THEORY OF OPERATION.

With 0 volt input, Q1 conducts and -6 volts appears at the collector of Q1. Q2 is driven into saturation by base current via R4. With Q2 conducting, the output is zero.

With -12 volts input, Q1 is reverse biased and cut off. The base of Q2, through R4, goes positive, driving Q2 to cutoff. With Q2 cut off, the output is -12 volts.

3. OPERATIONAL CHARACTERISTICS.

FUNCTION	INPUT		OUTPUT	
	HIGH LEVEL	LOW LEVEL	HIGH LEVEL	LOW LEVEL
Voltage	0.00 ±1.25V	-12 ±12V	0.5V max	-12V thru 2.7K ±10%
Current	2.6 ma max	4.7 ma max	30 ma max	-12V thru 2.7K ±10%
Rise Time			100 ns max	
Fall Time			500 ns max	

4. POWER REQUIREMENTS.

VOLTAGE	CURRENT
+12 VDC ±3%	+40 ma max
-12 VDC ±3%	-40 ma max
- 6 VDC ±4%	+56 to -19 ma max

1. GENERAL DESCRIPTION.

Eight identical output driver circuits are mounted on this card. Each circuit provides a two-way gating function.

2. TRUTH TABLE.

INPUT 1	INPUT 2	OUTPUT
HIGH	HIGH	LOW
HIGH	LOW	HIGH
LOW	HIGH	HIGH
LOW	LOW	HIGH

3. THEORY OF OPERATION.

During the following discussion, a 2K output load is assumed. When both inputs are at the high level of zero volts, the input to the base of Q1 becomes positive. Q1 is cut off. When Q1 cuts off, the base of Q2 goes negative. Q2 conducts and functions as an emitter follower until the output reaches approximately -12 volts.

When either one or both inputs are at the low level of -6 volts, the input to the base of Q1 goes negative and Q1 conducts. The base of Q2 goes positive with respect to emitter of Q2 and Q2 cuts off. The output is zero volts.

4. OPERATIONAL CHARACTERISTICS.

FUNCTION	INPUT		OUTPUT	
	HIGH LEVEL	LOW LEVEL	HIGH LEVEL	LOW LEVEL
Voltage	0V to -1V	-5V to -12V	0V to -1V	-12 ±2V
Current	350 μa max	1.5 ma max at -6V	5 ma max	5 ma max

3. POWER REQUIREMENTS.

VOLTAGE	CURRENT
+12 VDC ±3%	5.5 ma max
-12 VDC ±3%	55.0 ma max

1. GENERAL DESCRIPTION.

This card contains two independent and identical circuits. Each circuit is a three-stage, variable gain, linear differential preamplifier.

2. THEORY OF OPERATION.

The inputs to the differential preamplifiers are direct coupled to the Read Heads. The first stage, made up of Q1 and Q2, is a typical differential amplifier. The collectors of Q1 and Q2 are capacitively coupled to the second differential stage, made up of Q3 and Q4. A gain potentiometer, R11, is connected between the collectors of Q3 and Q4 to provide a variable gain adjustment. The second state output is capacitively coupled to the third stage made up of Q5 and Q6. Third stage output of Circuit Number 1 appears at pins 14 and 16. Output of Circuit Number 2 appears at pins 22 and 24.

The differential input impedance is from 7K minimum to 15K maximum across the input terminals. Input voltages are from 12 mv to 24 mv peak-to-peak differentially.

To measure gain, band pass, and output amplitude, the Read Amplifier board must be loaded with the Read Deskew board, assembly 3107252-10. Gain is 310 minimum at the maximum setting of potentiometer R11. Band pass is from 90 cps minimum to 35KC maximum with gain set to maximum. The output amplitude is 3.7 volts peak-to-peak minimum without limiting.

3. POWER REQUIREMENTS.

VOLTAGE	CURRENT
+12 VDC ±3%	10 ma max
-12 VDC ±3%	10 ma max

1. GENERAL DESCRIPTION.

This card contains one stage of a differential amplifier, a clipping circuit, a peak detector, a deskew single-shot, and a skew register flip-flop.

2. THEORY OF OPERATION.

The differential input from pins 8 and 10 is applied to the differential amplifier made up of Q1 and Q2. The output of the amplifier is summed with the Clipping Bias input from pin 16, and appears at the bases of Q3 and Q4. Q3 and Q4 form a full-wave rectifier with power gain. The amplitude of the Rectifier output is a function of the Clipping Bias input and appears at the base of emitter follower Q5. Q5 is directly coupled to Q6 and Q7. When the input to Q5 goes positive, Q5 drives the bases of Q6 and Q7 positive. Q6 conducts, charging capacitor C11, and Q7 cuts off. Capacitor C11 reaches maximum charge at the peak of the input waveform at the base of Q6. Following the peak of the waveform, the voltage begins to drop. C11 is charged to the peak voltage and holds the emitter of Q6 to that level. When the voltage at the base of Q6 drops, the base-emitter junction becomes back biased and Q6 cuts off. At the moment Q6 cuts off, the collector of Q6 goes positive, turning on emitter follower Q8. As input to the base of Q7 drops, Q7 begins to conduct and fully discharges C11 when the input waveform reaches zero. The circuit is then prepared for the next positive-going signal. When Q8 conducts, Q9 also conducts, causing Q10 to conduct. When Q10 conducts, a positive signal is fed via CR4 and C12 into the single-shot made up of Q11 and Q12. The output of the single-shot goes negative for the duration of its time delay. The single-shot time delay is dependent on the RC network of C13, R25, and R26. At the end of the time delay, the collector of Q12 goes positive, causing Q13 to conduct. The collector of Q13 goes negative, generating an OR Clock output at pin 35. At the time the collector of Q12 goes positive, the read register flip-flop made up of Q14 and Q15 is set. The flip-flop is later AC reset by a positive-going pulse from AC Reset input, pin 24. The flip-flop may also be forced to reset by a Skew Register DC Reset input from pin 26 through R37. The flip-flop output appears at pins 30 and 32.

3. POWER REQUIREMENTS.

VOLTAGE	CURRENT
+12 VDC ±3%	16 ma max
-12 VDC ±3%	40 ma max
- 6 VDC ±4%	80 ma max

1. GENERAL DESCRIPTION.

This card contains one stage of a differential amplifier, a Clipping circuit, a peak detector, a deskew single-shot, and a skew register flip-flop. The deskew single-shot provides two adjustable deskew delays, which are selected by applying +12 volts at one of two inputs.

2. THEORY OF OPERATION.

The Differential input from pins 8 and 10 is applied to the differential amplifier made up of Q1 and Q2. The output of the amplifier is summed with the Clipping Bias input from pin 16, and appears at the bases of Q3 and Q4. Q3 and Q4 form a full-wave rectifier with power gain. The amplitude of the Rectifier output is a function of the Clipping Bias input and appears at the base of emitter follower Q5. Q5 is directly coupled to Q6 and Q7. When the input to Q5 goes positive, Q5 drives the bases of Q6 and Q7 positive. Q6 conducts, charging capacitor C11, and Q7 cuts off. Capacitor C11 reaches maximum charge at the peak of the input waveform at the base of Q6. Following the peak of the waveform, the voltage begins to drop. C11 is charged to the peak voltage and holds the emitter of Q6 to that level. When the voltage at the base of Q6 drops, the base-emitter junction becomes back biased and Q6 cuts off. At the moment Q6 cuts off, the collector of Q6 goes positive, turning on emitter follower Q8. As input to the base of Q7 drops, Q7 begins to conduct and fully discharges C11 when the input waveform reaches zero. The circuit is then prepared for the next positive-going signal. When Q8 conducts, Q9 also conducts, causing Q10 to conduct. When Q10 conducts, a positive signal is fed via CR4 and C12 into the single-shot made up of Q11 and Q12 The output of the single-shot goes negative for the duration of its time delay. The single-shot time delay is dependent on the RC network of C13, R25, and R26 when -12 volts is applied at pin 21, or C13, R43 and R26 when -12 volts is applied at pin 20. Diodes CR16 and CR17 isolate the two inputs. At the end of the time delay, the collector of Q12 goes positive, causing Q13 to conduct. The collector of Q13 goes negative, generating an OR Clock output at pin 35. At the time the collector of Q12 goes positive, the read register flip-flop made up of Q14 and Q15 is set. The flip-flop is later AC reset by a positive-going pulse from AC Reset input, pin 24. The flip-flop may also be forced to reset by a Skew Register DC Reset input from pin 26 through R37. The flip-flop output appears at pins 30 and 32.

3. POWER REQUIREMENTS.

VOLTAGE	CURRENT
+12 VDC ±3%	16 ma max
-12 VDC ±3%	40 ma max
- 6 VDC ±4%	80 ma max

1. GENERAL DESCRIPTION.

This card contains four separate circuits. These circuits generate the Read Strobe, AC Read Register Reset signal, a Write Register DC Reset signal, and a Clipping Level output.

2. THEORY OF OPERATION.

Read Strobe and Read Register AC Reset. The Read Strobe circuit generates a Read Strobe and a Read Register AC Reset output at the time of the arrival of the first OR Clock input. The OR Clock (-) and Read Permit (-) inputs are fed to an AND gate comprised of CR1, CR2, and R20. The output of the gate goes negative, driving the base of Q6 negative, and Q6 conducts. The collector of Q6 goes positive, the OR Clock output at pin 14 goes positive, and a positive spike is coupled to the collector of Q7 through diode CR5 and capacitor C6. Q7 is the first transistor in a three-transistor flip-flop made up of Q7, Q8, and Q9. The positive pulse arriving at the collector of Q7 triggers the single-shot and the collector of Q9 goes negative for the duration of the single-shot delay. At the end of the delay, the collector of Q9 goes positive. This positive-going transition is coupled through CR12 and charges C11. When C11 is charged, the base of Q10 goes positive and Q10 cuts off. (Q10 remains cut off until capacitor C11 discharges to a level which causes the base of Q10 to go negative.) The period in which Q10 is cut off is approximately 1.5 μs. While Q10 is cut off, Q11 cuts off, and the collector of Q11 goes positive causing the Read Strobe output at pin 24 to go positive. The collector of Q11 remains positive for the period of time Q10 is cut off. When the collector of Q11 goes positive, Q12 cuts off and the collector of Q12 goes negative. When Q10 conducts, Q11 conducts and the Read Strobe output at pin 24 goes negative. The negative transition of the Read Strobe is the trailing edge of the Read Strobe pulse. When the collector of Q11 goes negative, Q12 conducts and the collector of Q12 goes positive. The positive transition of Q12 is the Read Register AC Reset signal, and appears at pin 22.

The single-shot in the preceding paragraph operates in the following manner. When a positive pulse is coupled into the collector of Q7, this pulse is also seen at the base and emitter of emitter follower Q8 and charges C8. When C8 is charged, the base of Q9 goes positive, and Q9 is cut off. Q7 is forced into conduction and the collector of Q7 drops to ground potential. The emitter of Q8 also falls to approximately ground and completes the charge cycle of C8. Capacitor C8 then begins a slow discharge through R28, R31, and R13 or R14. Resistors R13 and R14 are selected externally to change the time delay range. R13 is selected in high density. R14 is selected in low density. When C8 is discharged to a point where the base of Q9 goes negative, Q9 conducts and the single-shot delay has ended. Emitter follower Q8 totally discharges C8 through diode CR10 and resistors R30 and R29.

2. THEORY OF OPERATION. (Continued)

Write Register DC Reset. The Write Register Reset signal is a composite of the Run and Write Permit input signals. The Run and Write Permit are ANDed in the following manner. The collector of Q2 is normally negative. If Run or Write Permit inputs are positive, the collector of Q2 goes positive. With Write Permit input at pin 28 negative and Run input at pin 20 positive, Q1 is cut off and the collector of Q1 goes positive. Q13 is conducting. The collector of Q13 goes negative. CR19 is back biased and isolates the collector of Q13 from the collector of Q1. Q2 is conducting. The collector of Q2 goes to +12 volts and appears at output pin 30.

With the Run input negative and Write Permit input positive, Q13 is cut off and Q1 is conducting. The collector of Q1 goes negative. Diode CR19 becomes forward biased and lowers the collector voltage of Q13 to -6 volts. Q2 conducts and +12 volts appears at the collector of Q2 and at output pin 30.

With both Run and Write Permit inputs negative, Q1 and Q13 are cut off. The collector of Q13 rises to a value more positive than the emitter of Q2, driving Q2 to cutoff. The output at pin 30 is negative.

Clipping Level. The Clipping Level circuit provides a negative clipping bias voltage for the Read Deskew circuits. This bias voltage may be varied from approximately -6 to -9 volts. In normal operation, a higher clipping level is required in the Write Mode than that used in the Read Mode. The Clipping Level circuit automatically provides a higher clipping level when the circuit is in the Write Mode.

Transistor Q4 functions as an emitter follower and provides a low impedance voltage source to the output at pin 32. Q4 is driven by the voltage divider network comprised of trim pots R9 and R10, resistor R8, and zener diode VR1. A maximum output of approximately -9 volts is required. This output is obtained by placing VR1 in series with -6 volts to give approximately -9 volts between the anode of VR1 and ground.

When Write Permit (-) is TRUE, Q1 is cut off, causing Q3 to be cut off. With Q3 cut off, the voltage at the base of Q4 may be varied from approximately -6 volts to -9 volts by varying trim pot R9. When Write Permit (-) is FALSE, Q1 and Q3 conduct. The collector of Q3 goes to -6 volts. The voltage at the base of Q4 may then be adjusted between -6 volts and the voltage present at the slider of R9.

3. POWER REQUIREMENTS.

VOLTAGE	CURRENT
+12 VDC ±3%	86 ma max
-12 VDC ±3%	100 ma max
- 6 VDC ±4%	30 ma max
+24 VDC ±15%	3 ma max

1. GENERAL DESCRIPTION.

This card contains six independent circuits as follows: two Input Buffers, one Output Driver, one Inverter, one Hi/Lo Density Select Driver, and one Deskew and Amplifier Select Driver.

2. THEORY OF OPERATION.

Input Buffers. The input to Buffer #1 is at pin 12 and the output is at pin 15. The input to Buffer #2 is at pin 13 and the output is at pin 16. The Input Buffer circuits are identical. Only Input Buffer #1 is described.

With 0 volts input, Q5 conducts and -6 volts appears at the collector of Q5. Q6 is driven into saturation by base current via R14. With Q6 conducting, the output is zero.

With -12 volts input, Q5 is reverse biased and cuts off. The base of Q6, through R14, goes positive, driving Q6 to cutoff. With Q6 cut off, the output is -12 volts.

Output Driver. The Output Driver circuit has two inputs at pins 18 and 19, and an output at pin 17. The theory of operation is as follows.

During the following discussion, a 2K output load is assumed. When both inputs are at the high level of zero volts, the input to the base of Q14 becomes positive. Q14 is cut off. When Q14 cuts off, the base of Q15 goes negative. Q15 conducts and functions as an emitter follower until the output reaches approximately -12 volts.

When either one or both inputs are at the low level of -6 volts, the input to the base of Q14 goes negative and Q14 conducts. The base of Q15 goes positive with respect to emitter of Q15 and Q15 cuts off. Output is zero volts.

Inverter. The Inverter circuit has an input at pin 9 and an output at pin 10. The theory of operation is as follows.

When Read Permit input is -12 volts, Q9 is biased to cutoff and the output is 0 volts. When Read Permit input is 0 volts, Q9 is conducting and the output is -6 volts.

2. THEORY OF OPERATION. (Continued)

Density Select Driver. The Density Select Driver input is at pin 25 and the outputs are at pins 21 and 23. The theory of operation is as follows.

The Density Select Driver input is controlled by a pushbutton on the OCP. When the input at pin 25 is 0 volts (Low Density), Q10 and Q11 are cut off. High Density output at pin 23 is open circuit. Q12 and Q13 are conducting and Low Density output at pin 21 is -12 volts.

When the input at pin 25 is -12 volts (High Density), Q10 and Q11 are conducting. High Density output at pin 23 is -12 volts. Q12 and Q13 are cut off and Low Density output at pin 21 is open circuit.

Deskew and Amplifier Select Driver. The Deskew and Amplifier Select Driver input is at pin 27 and the Deskew Select outputs are at pins 29 and 31, and Amplifier Select outputs are at pins 32 and 33.

The theory of operation is as follows. An input of -12 volts causes Q1 and Q2 to conduct and Q3 and Q4 to cut off. When Q2 is conducting, the outputs at pins 31 and 32 are driven to approximately -12 volts by transistor Q2.

When Q4 is cut off, the output at pin 29 goes to +12 volts and the output at pin 33 is isolated from pin 29 by back biased diode CR5.

An input of 0 volts causes Q1 and Q2 to cut off and Q3 and Q4 to conduct. When Q4 is conducting, the outputs at pins 29 and 33 are driven to approximately -12 volts by transistor Q4. The output at pin 31 goes to +12 volts and the output at pin 32 is isolated from pin 31 by back biased diode CR2.

3. OPERATIONAL CHARACTERISTICS.

CIRCUIT	PARAMETER	INPUT		OUTPUT	
		HIGH LEVEL	LOW LEVEL	HIGH LEVEL	LOW LEVEL
Input Buffer	Voltage	0.00 ±1.25V	-12 ±2V	0.5V max	-12V thru 2.7K ±10%
	Current	2.6 ma max	4.7 ma max	30 ma max	-12V thru 2.7K ±10%
	Rise Time	100 ns		100 ns	
	Fall Time		100 ns		500 ns max
Output Driver	Voltage	0V to -1V	-5V to -12V	0V to -1V	-12 ±2V
	Current	350 μa max	1.5 ma max at -6 volts	5 ma max	5 ma max
Density Select	Voltage	-0.5V most negative	-5.5V least negative	0.3V more positive than -12V supply	Open circuit
Read Permit	Voltage	-0.5V most negative	-5.5V least negative	+0.5V max	-6.0 ±0.5V
Deskew & Amplifier Select	Voltage Deskew	0.00 ±1.25V	-9V to -25V	+12V with no load	-12V
	Voltage Amplifier Select	0.00 ±1.25V	-9V to -25V	0.0 ±0.8V with no load	-12V

1. GENERAL DESCRIPTION.

This card contains the input gating, deskew single-shot and the write head driver flip-flop.

2. THEORY OF OPERATION.

When Write Data input is coincident with the Write Strobe input for a period of 2 μsec, the Write Data signal is fed through OR diode CR7 to the base of Q2. Transistor Q2 conducts and the collector of Q3 is placed at ground.

Capacitor C7 charges, causing Q4 to cut off and allowing Q3 to conduct. After capacitor C7 discharges, Q4 conducts again. The discharge time of C7 is based on the time constant of C7, R1 (or R2) and R12. The discharge time determines the deskew delay time and can be varied by adjusting potentiometer R2. When the dual speed option is used, potentiometer R1 is used.

With Q4 conducting, Q5 conducts and a negative input is fed to the trigger flip-flop Q7 and Q8. The steering diodes CR18 and CR26 gate the input pulse to the proper transistor, causing the flip-flop to change state.

Assuming the flip-flop is in the reset state, Q6 and Q7 are conducting, Q8 and Q9 are cut off. Diode CR18 is forward biased and CR26 is reverse biased. The collector output of Q6 is at ground and that of Q9 is near +10 volts.

When a negative set pulse arrives at C10 and C11, the pulse through C11 is applied to reverse biased CR26, producing no change. The pulse through C10 is conducted through forward biased CR18 to the base of Q7, cutting Q7 off. When Q7 cuts off, Q6 turns off and opposite state transistors Q8 and Q9 turn on.

When Q8 and Q9 conducts, a ground is provided through the emitter-collector path to output B, pin 30. Simultaneously, the Q6 collector voltage rises to a positive voltage and is applied to output A, pin 34. Each voltage polarity change at the outputs A and B causes a current reversal in the write coil, producing a written ONE on the tape. The positive voltage is also conducted through CR21 to the Echo output, pin 24, for optional Write Check Error usage.

A positive signal at DC Reset input pin 26 causes CR19 to be forward biased, applying a positive potential to the base of Q7. Q7 is forced into conduction. A negative signal at pin 26 causes CR19 to be back biased and disconnects this input.

2. THEORY OF OPERATION. (Continued)

Write Reset input at pin 10 is combined with the Reset output of the flip-flop via Q1 and is handled in the same manner as data, except that a Write Strobe input is not required.

Test Deskew is an input provided for use in the system alignment procedures. Test signals are handled in the same manner as data, except that no other inputs are required.

3. POWER REQUIREMENTS.

VOLTAGE	CURRENT
+12 VDC ±3%	14 ma max
-12 VDC ±3%	14 ma max
- 6 VDC ±4%	8 ma max

1. GENERAL DESCRIPTION

This card contains three independent circuits.

The Write Power Gate provides power to the write amplifiers when Write Permit is TRUE and when the Write Enable relay has been energized.

The Read Permit inverter inverts and amplifies the Read Permit signal.

The Density Select driver applies voltage to the density potentiometers located on the Read Deskew Assembly (3107252).

2. THEORY OF OPERATION.

Write Power Gate. When input 1 or 2 is -12 volts, Q1 is biased to cutoff. With Q1 cut off, Q2 is driven into saturation by positive base current through R3. When Q2 conducts, the base of Q3 goes to approximately +3 volts causing Q3 to conduct. With Q3 conducting, the voltage at the base of Q4 goes to approximately +3 volts, causing Q4 to conduct. When Q4 conducts, the output, through pins 7 and 1 of K1, is at +10 volts. Relay K1 is energized when the External File Protect switch is closed.

When input 1 or 2 is 0 volts, Q1 conducts and -6 volts appears at the base of Q3, driving it to cutoff. With Q2 cut off, the base of Q3 goes to +15 volts. As Q3 is conducting, approximately +15 volts appears at the base of Q4, driving it to cutoff. The output is 0 volts.

Read Permit Inverter. When Read Permit input is -12 volts, Q9 is biased to cutoff, and the output is +12 volts. When Read Permit input is 0 volts, Q9 is conducting and the output is -6 volts.

Density Select Driver. The Density Select Driver input is controlled by a pushbutton on the OCP. When input at pin 11 is 0 volts (Low Density), Q5 and Q6 are cut off. High Density output at pin 16 is open circuit. Q7 and Q8 are conducting and Low Density output at pin 17 is -12 volts.

2. THEORY OF OPERATION. (Continued)

Erase Head Driver. Whenever the Write Power Gate is on, current is supplied to the Erase Head through R19. The current is 100 milliamperes nominal.

When input at pin 11 is -12 volts (High Density), Q5 and Q6 are conducting. High Density output at pin 16 is -12 volts. Q7 and Q8 are cut off and Low Density output at pin 17 is open circuit.

3. OPERATIONAL CHARACTERISTICS.

CIRCUIT	INPUT		OUTPUT	
	HIGH LEVEL	LOW LEVEL	HIGH LEVEL	LOW LEVEL
Write Power Gate	0.0V to -0.5V	-5.70V to -12.36V	+11V to +12V	0.0V to -1.5V
Density Select	-0.5V most negative	-5.5V least negative	0.3V more positive than -12V supply	Open circuit
Read Permit	-0.5V most negative	-5.5V least negative	0.5V max	-6.0 ±0.5V
Write Enable Relay	11.64V min at 100 ma max		+11V to +12V	0.0V to -1.5V

4. POWER REQUIREMENTS.

VOLTAGE	CURRENT
+12 VDC ±3%	2 ma max
-12 VDC ±3%	103 ma max
- 6 VDC ±4%	13 ma max
+24 VDC ±15%	30 ma max
-24 VDC ±15%	5 ma max

SECTION VII
DRAWINGS

7-1. INTRODUCTION.

Printed circuit board schematics and assembly drawings are included in this section and are located in alphabetic order by the mnemonic code, as shown on Table 7-1.

The master part selector drawings show the standard PCB assemblies used for the various versions of the data electronics. Drawing 3124744 covers the TM-7 series, drawing 3124745 covers the TM-9 series, and drawing 3124746 covers the TM-11/TM-12 series. The part number of the standard data electronics assembly (with or without the echo, rate, or vertical parity check options) is 3115771-10. The part number of a data electronics assembly containing one or more of the special features (special positive input/output levels, vertical parity generate, longitudinal parity check, and longitudinal check character generate) is 3115770- followed by a two digit version number which is determined by the version table on the master part selector drawing. For example, part number 3115770-01 identifies a data electronics assembly wired for bidirectional read (run/stop logic); standard input/output levels; echo, rate, and vertical parity checking; and 7-track vertical parity generate.

Two sets of logic diagrams are located at the end of this section. Logic Diagram 3112457 is for standard DE-211 (7-track) and DE-291 (9-track) systems which use Forward/Reverse and Run/Stop commands. Logic Diagram 3115496 is for standard systems which use Forward/Stop and Reverse/Stop commands.

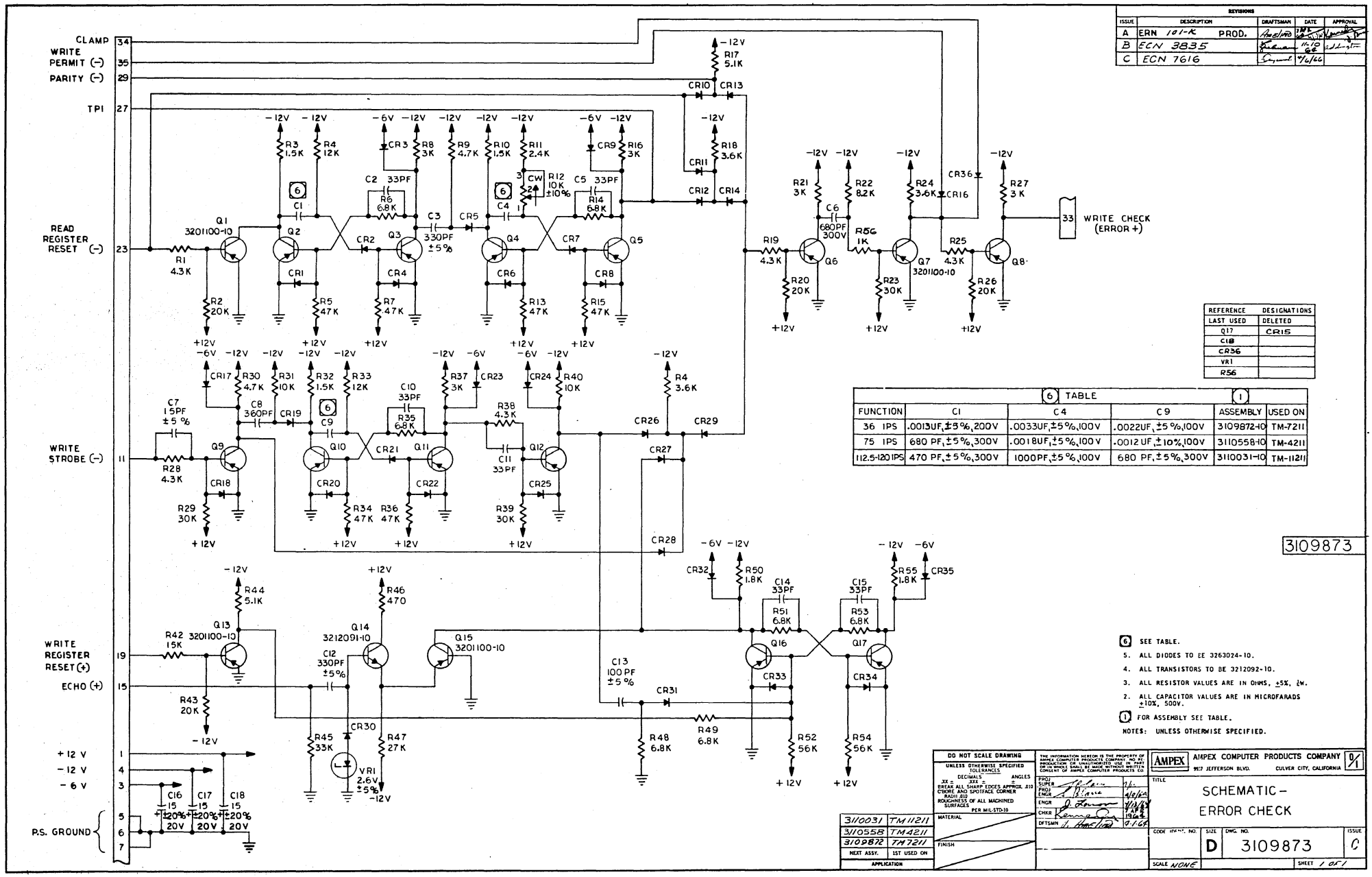
TABLE 7-1
LIST OF DRAWINGS

CODE	DESCRIPTION	SCHEMATIC	ASSY DWG
ECC	Error Check	3109873	3109915
EOA	Exclusive OR	3104452	3107274
FFB*	Flip-Flop	3104541	3107275
IBA	Input Buffer	3107038	3107251
IBT*	Input Buffer	3118175	3118174
LGB*	LCC Generator	3116076	3116075
LPB*	LPC Timing -B	3116088	3116087
ODA	Output Driver	3107043	3107255
ODL*	Output Driver	3118184	3118183
ODM*	Output Driver	3118166	3118165
PRB*	Long. Parity Reg -B	3116083	3116100
RAB	Read Amplifier	3107118	3107270
RDB	Read Deskew	3107253	3107273
RDC	Read Deskew, Bidirectional	3109930	3109933
SGA	Strobe Generator	3107058	3107276
SLB	Select Logic	3111158	3111157
WAB	Write Amplifier	3112345	3112347
WPD	Write Power Gate	3107128	3107272

*Required for special features. Refer to Section VIII.

MISCELLANEOUS DRAWINGS

DESCRIPTION	DWG NO.
Master Part Selector	
Std TM-7 Series	3124744
Std TM-9 Series	3124745
Std TM-11/TM-12 Series	3124746
Card Location Chart (DE-211/DE-291)	3124747
Logic Diagram, DE-211 Data Electronics	
(Fwd/Rev-Run/Stop)	3112457
(Fwd/Stop-Rev/Stop)	3115496



REVISIONS				
ISSUE	DESCRIPTION	DRAFTSMAN	DATE	APPROVAL
A	ERN 101-K PROD.			
B	ECN 3835			
C	ECN 7616			

REFERENCE DESIGNATIONS	
LAST USED	DELETED
Q17	CR15
C18	
CR36	
VR1	
R56	

(6) TABLE (1)

FUNCTION	C1	C4	C9	ASSEMBLY	USED ON
36 IPS	.0013UF, ±5%, 200V	.0033UF, ±5%, 100V	.0022UF, ±5%, 100V	3109872-10	TM-7211
75 IPS	680 PF, ±5%, 300V	.0018UF, ±5%, 100V	.0012 UF, ±10%, 100V	3110558-10	TM-4211
112.5-120 IPS	470 PF, ±5%, 300V	1000PF, ±5%, 100V	680 PF, ±5%, 300V	3110031-10	TM-11211

3109873

(6) SEE TABLE.

5. ALL DIODES TO EE 3263024-10.
4. ALL TRANSISTORS TO BE 3212092-10.
3. ALL RESISTOR VALUES ARE IN OHMS, ±5%, ¼W.
2. ALL CAPACITOR VALUES ARE IN MICROFARADS ±10%, 500V.

(1) FOR ASSEMBLY SEE TABLE.

NOTES: UNLESS OTHERWISE SPECIFIED.

3110031	TM11211
3110558	TM4211
3109872	TM7211
NEXT ASSY.	1ST USED ON
APPLICATION	

DO NOT SCALE DRAWING

UNLESS OTHERWISE SPECIFIED TOLERANCES
DECIMALS .XX ± .010 .XXX ± .005
ANGLES ±1°
BREAK ALL SHARP EDGES APPROX. .010 CHORE AND SPOTFACE CORNER RADII .010
ROUGHNESS OF ALL MACHINED SURFACES PER MIL-STD-10

MATERIAL

FINISH

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PROJ SUPR		
PROJ ENGR		4/6/66
ENGR		7/7/66
CHKR		7/8/66
DFTSMN		9/1/66

AMPEX COMPUTER PRODUCTS COMPANY
9937 JEFFERSON BLVD. CULVER CITY, CALIFORNIA

TITLE: SCHEMATIC - ERROR CHECK

CODE IDENT. NO.	SIZE	DWG. NO.	ISSUE
	D	3109873	C

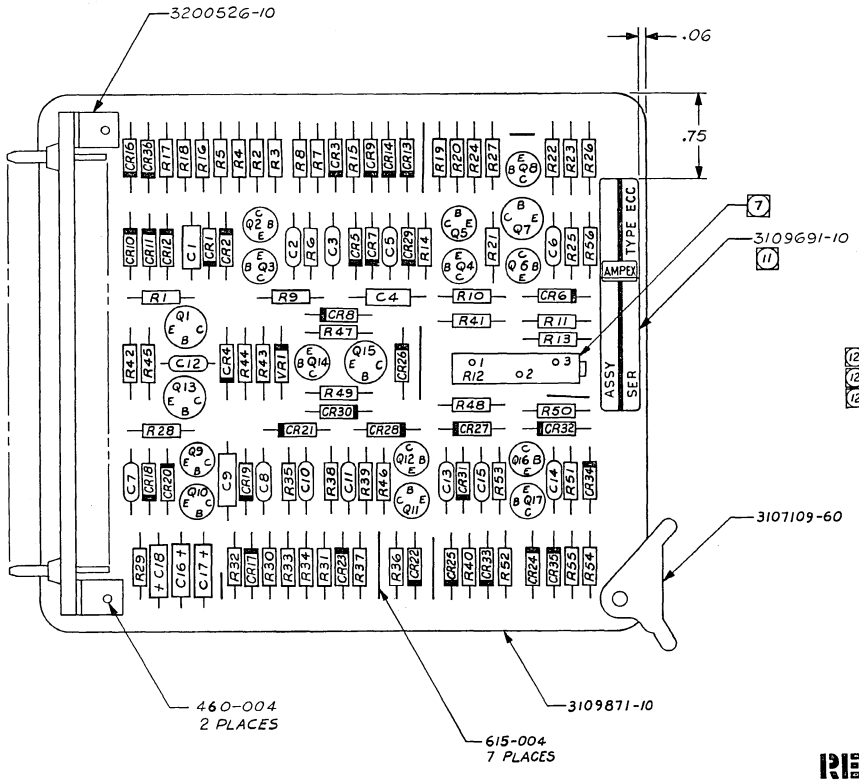
SCALE NONE SHEET 1 OF 1

B/M REFERENCE TABLE

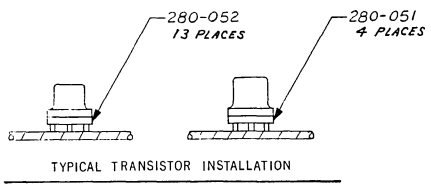
ASSEMBLY	FUNCTION	USED ON	COMPONENTS		
			PART A	PART B	PART C
3109872-10	36 IPS	TM-7211	033-168	035-422	035-421
3110558-10	75 IPS	TM-4211	034-930	033-082	035-757
3110031-10	112.5-120 IPS	TM-11211	034-214	034-950	034-930

REVISIONS

ISSUE	DESCRIPTION	DATE	DRAFTSMAN	DATE	APPROVAL
A	ERN 101-K PROD REL	4/7/66	ANDELINO	4/7/66	KENNEDY
B	ECN	8/3/66	ANDELINO	8/3/66	Gough
C	ECN 3835	11/10/66	UNDERMAN	11/10/66	Gough
D	ECN 7016	4/11/67	Andelino		



PART NO.	REFERENCE DESIGNATION	PART NO.	REFERENCE DESIGNATION
3201100-10	Q1, Q13, Q15, Q7	041-412	R9, R30
3212091-10	Q14	041-413	R6, R14, R35, R48, R49, R51, R53
3212092-10	Q2, Q3, Q4, Q5, Q6, Q8, Q9, Q10, Q11, Q12, Q16, Q17	041-428	R46
		041-430	R3, R10, R32
3263024-10	CR1 THRU CR14, CR16 THRU CR36	041-434	R50, R55
013-461	VR1	041-482	R4, R33
034-177	C13	041-483	R47
034-212	C3, C12	041-495	R22
034-535	C7	041-508	R2, R20, R26, R43
034-491	C2, C5, C10, C11, C14, C15	041-518	R45
034-496	C8	041-519	R52, R54
034-519	C6	041-550	R8, R16, R21, R27, R37
037-990	C16, C17, C18	041-561	R17, R44
041-408	R31, R40	041-570	R11
041-409	R42	041-571	R18, R24, R41
041-411	R5, R7, R13, R15, R34, R36	041-584	R1, R19, R25, R28, R38
12 PART A	C1	041-612	R23, R29, R39
12 PART B	C4	041-410	R56
12 PART C	C9	044-197	R12



TYPICAL TRANSISTOR INSTALLATION

REFERENCE

12 INSTALL PARTS 'A' THRU 'C' PER TABLE I.

11 MARK PART NO. AND NAMEPLATE INFORMATION PER MIL-STD-130.

10. PART NO. TO BE AS SHOWN ON B/M.

9. SEAL PRINTED CIRCUIT SIDE ONLY WITH HUMISEAL TYPE 1B15 COLUMBIA TECH. CORP. OR EQUIV.

~~8 MARK POT REF NO'S, .12 HIGH CHARACTERS, COLOR WHITE, PER MIL-STD-130. DO NOT IMPRESSION STAMP~~

7 TRIMPOTS NOT TO BE SUBMERGED IN WATER.

6. COMPONENT DESIGNATIONS ARE FOR REF. ONLY.

5. PLUS SIGN ON CAPACITOR INDICATES POSITIVE.

4. HEAVY LINE ON DIODES INDICATES CATHODE.

3. ASSEMBLE PER PRODUCTION PRACTICES MANUAL.

2. FOR ASSEMBLY SPECIFICATION SEE 3109874.

1. FOR SCHEMATIC SEE 3109873.

NOTES:

DO NOT SCALE DRAWING
UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES: DECIMALS XX± XXX± ANGLES ±
BREAK ALL SHARP EDGES APPROX. .010. C'BORE AND SPOTFACE CORNER RADII APPROX. .010.
ROUGHNESS OF ALL MACHINED SURFACES ✓ PER MIL-STD-10
MATERIAL

3110031	TM-11211
3110558	TM-4211
3109872	TM-7211
NEXT ASSY.	1ST USED ON
APPLICATION	

FINISH

DWG NO 3109915

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PROJ ENGR	S. BLANK	9/13/66
ENGR	T. CARSON	9/13/66
CHKR	KENNEDY	9/9/66
DFTSMN	V. ANDELINO	3/24/66

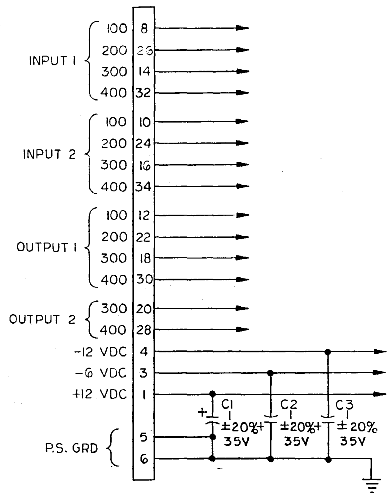
AMPEX COMPUTER PRODUCTS DIVISION
P.O. BOX 329, CULVER CITY, CALIF.

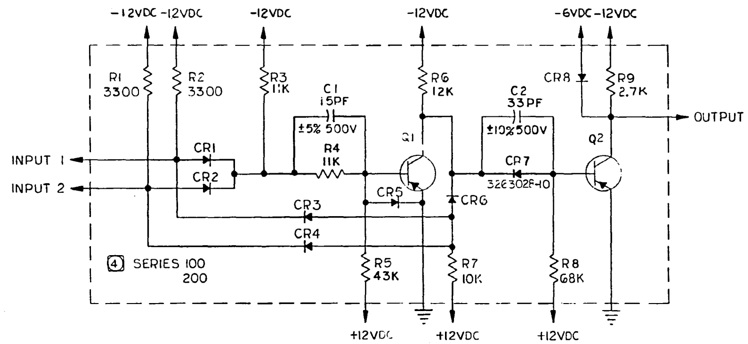
TITLE
CIRCUIT BOARD ASSY
ERROR CHECK

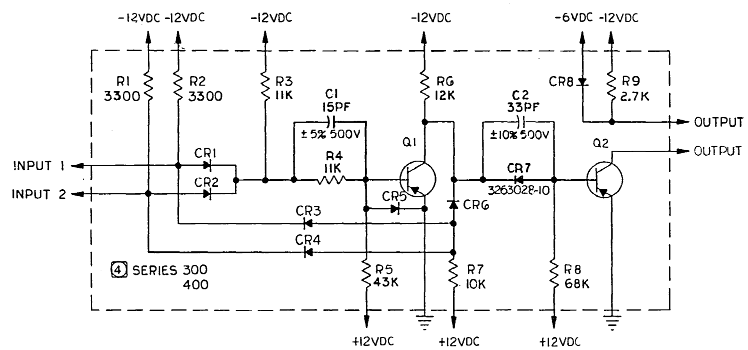
SIZE D | CODE IDENT. NO. 09150 | DWG. NO. 3109915

SCALE 2:1 | SHEET 1 OF 1

ISSUE	DESCRIPTION	DRAFTSMAN	DATE	APPROVAL
REVISIONS				
A	[illegible]	HB	[illegible]	[illegible]
B	ECN 3149	[illegible]	[illegible]	[illegible]
C	ECN 8061	[illegible]	[illegible]	[illegible]







5. ALL TRANSISTORS TO BE 3212092-10.
4. REF DESIGNATIONS ARE ABBREVIATED PER MIL-STD-16. PREFIX THE PART DESIGNATION WITH THE SUBASSEMBLY DESIGNATION.
3. ALL DIODES TO BE 3263024-10.
2. ALL RESISTORS IN OHMS ±5%, 1/4W.
1. ALL CAPACITORS IN MICROFARADS

NOTES: UNLESS OTHERWISE SPECIFIED

REQD.	PART NO.	DESCRIPTION	REFERENCE	ZONE	ITEM
LIST OF MATERIAL					

DO NOT SCALE DRAWING

UNLESS OTHERWISE SPECIFIED TOLERANCES
DECIMALS .XX ± .03 .XXX ± .010; ANGLES ± 1/2°
BREAK ALL SHARP EDGES APPROX .010
C'BORE AND SPOTFACE CORNER RADII .010
ROUGHNESS OF ALL MACHINED SURFACES ✓ PER MIL-STD-10

MATERIAL

FINISH

NEXT ASSY.	1ST USED ON
3102978	DE-100
APPLICATION	

FORM 2402-107 REV. 9-61

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PROJ SUPER / PROJ ENGR / ENGR / CHKR / DFTSMN [illegible signatures] 9-2-62

7103-254

AMPEX COMPUTER PRODUCTS COMPANY
9937 JEFFERSON BLVD. CULVER CITY, CALIFORNIA

TITLE: SCHEMATIC, EXCLUSIVE OR TYPE P

CODE INDENT. NO.	SIZE	DWG. NO.	ISSUE
	D	3104452	C

SCALE NONE

REVISIONS				
ISSUE	DESCRIPTION	DRAFTSMAN	DATE	APPROVAL
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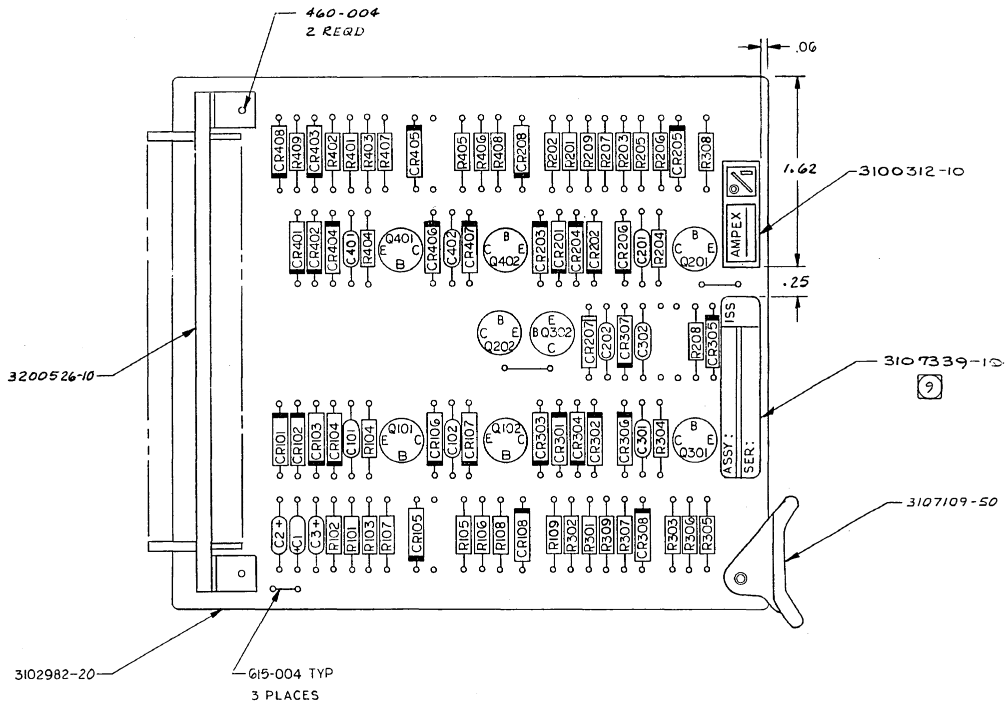
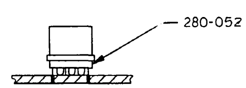
B	ECN 8061	[illegible]	[illegible]	[illegible]



PART NO.	QTY.	COMPONENT DESIGNATION
3212092-10	8	Q101,102,201,202,301,302,401,402
3263024-10	28	CR101 THRU 106,108,301 THRU 306, 308,CR201 THRU 206,208,401 THRU 406,408
3263028-10	4	CR107,207,307,407
034-491	4	C102,202,302,402
034-963	4	C101,201,301,401
037-058	3	C1,2,3
041-407	8	R101,102,201,202,301,302,401,402
041-408	4	R107,207,307,407
041-415	4	R108,208,308,408
041-482	4	R106,206,306,406
041-562	4	R105,205,305,405
041-442	4	R109,209,309,409
041-748	8	R103,104,203,204,303,304,403,404

3107274



TYPICAL TRANSISTOR INSTALLATION

9. MARK PART NO. AND NAMEPLATE INFORMATION PER MIL-STD-130.
8. PART NO. TO BE 3107274-10.
7. SEAL PRINTED CIRCUIT SIDE ONLY WITH HUMI-SEAL TYPE 1B15, COLUMBIA TECH. CORP., OR EQUIV.
6. HEAVY LINE ON DIODE INDICATES CATHODE.
5. PLUS SIGN ON CAPACITOR INDICATES POSITIVE.
4. COMPONENT DESIGNATIONS ARE FOR REFERENCE ONLY.
3. ASSEMBLE PER MANUFACTURING PRACTICE MANUAL
2. FOR ASSY SPECIFICATION SEE 3104624.
1. FOR SCHEMATIC SEE 3104452

NOTES:

REQD.	PART NO.	DESCRIPTION	REFERENCE	ZONE	ITEM

LIST OF MATERIAL

FORM 2602-107 REV. 9-61

DO NOT SCALE DRAWING

UNLESS OTHERWISE SPECIFIED TOLERANCES
DECIMALS .XX ± .03 .XXX ± .010 ANGLES ± 1/2°
BREAK ALL SHARP EDGES APPROX. .010
C'BORE AND SPOTFACE CORNER RADII .010
ROUGHNESS OF ALL MACHINED SURFACES ✓ PER MIL-STD-10

MATERIAL

FINISH

THE INFORMATION HEREON IS THE PROPERTY OF AMPEX COMPUTER PRODUCTS COMPANY. NO REPRODUCTION OR UNAUTHORIZED USE IN PART OR IN WHOLE SHALL BE MADE WITHOUT WRITTEN CONSENT OF AMPEX COMPUTER PRODUCTS CO.

PROJ SUPER	[illegible]
PROJ ENGR	[illegible]
ENGR	[illegible]
CHKR	[illegible]
DFTSMN	[illegible]

AMPEX COMPUTER PRODUCTS COMPANY
9937 JEFFERSON BLVD. CULVER CITY, CALIFORNIA

TITLE CIRCUIT BOARD ASSY- EXCLUSIVE OR TYPE P

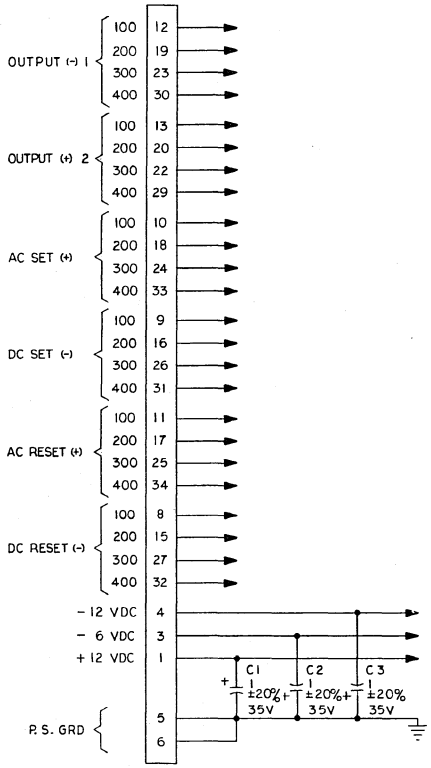
CODE INDENT. NO.	SIZE	DWG. NO.	ISSUE
	D	3107274	B

SCALE 2/1

NEXT ASSY.	1ST USED ON
3107280	TM-7211

APPLICATION

REVISIONS				
ISSUE	DESCRIPTION	DRAFTSMAN	DATE	APPROVAL
A	[illegible]	[illegible]	[illegible]	[illegible]
B	ECN 00572	[illegible]	1-25-65	[illegible]
C	ECN 1877	Butterworth	7/8/69	[illegible]
D	ECN 3143	Butterworth	[illegible]	[illegible]
E	ECN 3631	[illegible]	[illegible]	[illegible]



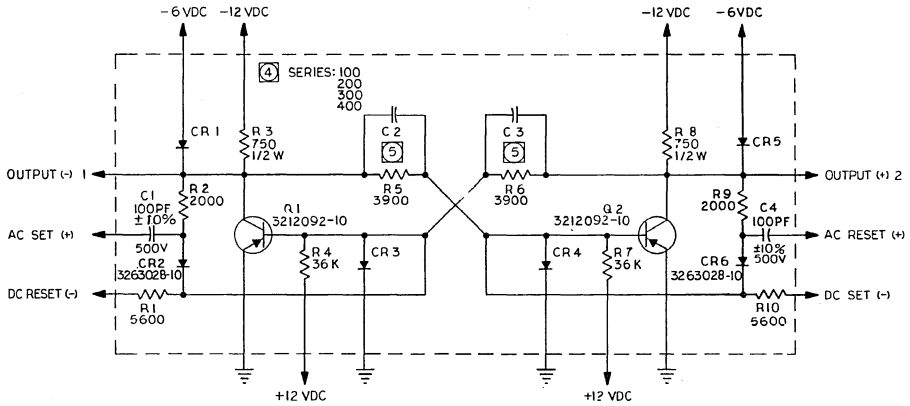


TABLE I 5	
ASSY NO.	C2 & C3
3102970-10	33PF ±10%, 500V
3107275-10	33PF ±10%, 500V
3109115-10	15PF ± 5%, 500V
3111790-10	NONE

5 SEE TABLE I.

4 REF. DESIGNATIONS ARE ABBREVIATED PER MIL-STD-16. PREFIX THE PART DESIGNATION WITH THE SUBASSEMBLY DESIGNATION.

3. ALL DIODES TO BE 3263024-10.
2. ALL CAPACITORS IN MICROFARADS.
1. ALL RESISTORS IN OHMS ±5%, 1/4 W.

NOTES: UNLESS OTHERWISE SPECIFIED

REQD.	PART NO.	DESCRIPTION	REFERENCE	ZONE	ITEM

LIST OF MATERIAL

DO NOT SCALE DRAWING

UNLESS OTHERWISE SPECIFIED TOLERANCES. DECIMALS XX ± .03 XXX ± .010 ANGLES ± 1/2° BREAK ALL SHARP EDGES APPROX. .010 C'BORE AND SPOTFACE CORNER RADII .010 ROUGHNESS OF ALL MACHINED SURFACES √ PER MIL-STD-10

FORM 2602-107 REV. 9-65

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AMPEX 0/1 AMPEX COMPUTER PRODUCTS COMPANY
9937 JEFFERSON BLVD. CULVER CITY, CALIFORNIA

PROJ	[illegible]
SUPER	[illegible]
PROJ ENGR	[illegible]
ENGR	[illegible]
CHKR	[illegible]
DFTSMN	[illegible]

TITLE: SCHEMATIC, FLIP-FLOP, TYPE P

3109115	TM-4122
3102970	TM-4111
NEXT ASSY.	1ST USED ON
APPLICATION	

MATERIAL

FINISH

7103-252

CODE IDENT. NO. 91662

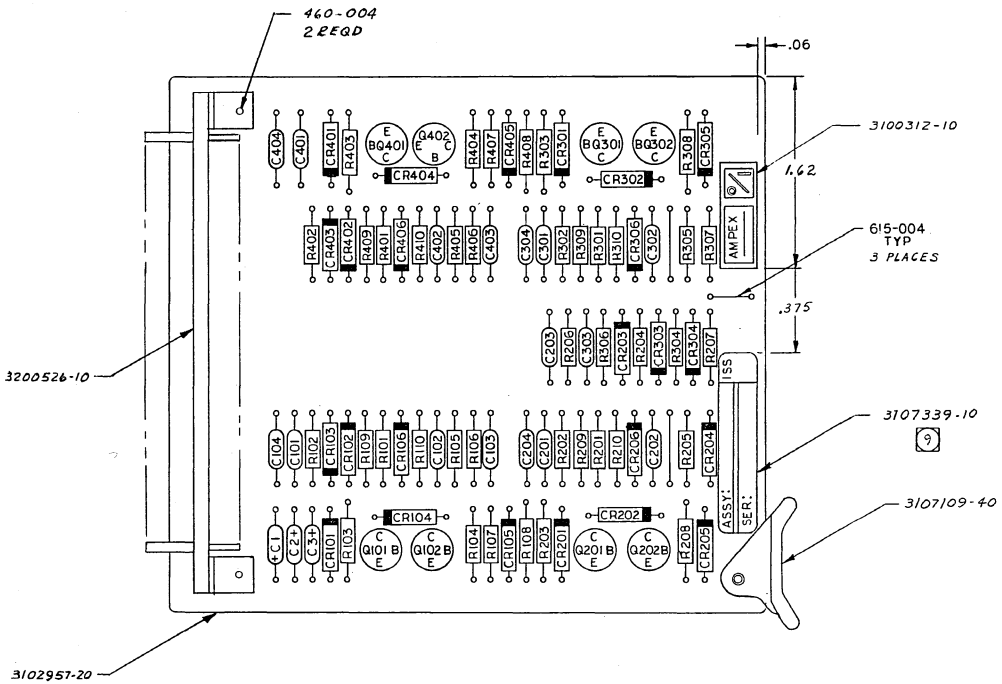
SIZE D

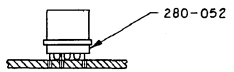
DWG. NO. 3104541

ISSUE E

SCALE NONE

REVISIONS				
ISSUE	DESCRIPTION	DRAFTSMAN	DATE	APPROVAL
A	[illegible]	[illegible]	[illegible]	[illegible]





TYPICALL TRANSISTOR INSTALLATION

PART NO.	QTY.	COMPONENT DESIGNATION
3263024-10	16	CR101,103,104,105,201,203,204, 205,301,303,304,305,401,403,404, 405
3212092-10	8	Q101,102,201,202,301,302,401,402
037-058	3	C1,2,3
034-491	8	C102,103,202,203,302,303,402,403
034-417	8	C101,104,201,204,301,304,401,404
041-007	8	R103,108,203,208,303,308,403,408
041-560	8	R102,109,202,209,302,309,402,409
041-511	8	R105,106,205,206,305,306,405,406
041-507	8	R101,110,201,210,301,310,401,410
041-751	8	R104,107,204,207,304,307,404,407
3263028-10	8	CR102 THRU 402, CR106 THRU 406

3107275

(9) MARK PART NO. AND NAMEPLATE INFORMATION PER MIL-STD-130

8. PART NO. TO BE 3107275-10
7. SEAL PRINTED CIRCUIT SIDE WITH HUMI-SEAL TYPE 1B15 COLUMBIA TECH. CORP OR EQUIVALENT.
6. HEAVY LINE ON DIODE INDICATES CATHODE.
5. PLUS SIGN ON CAPACITOR INDICATES POSITIVE.
4. COMPONENT DESIGNATIONS ARE FOR REFERENCE ONLY.
3. ASSEMBLE PER MANUFACTURING PRACTICE MANUAL.
2. FOR ASSY SPEC SEE 3104604
1. FOR SCHEMATIC SEE 3104541.

NOTES:

REQD.	PART NO.	DESCRIPTION	REFERENCE	ZONE	ITEM

LIST OF MATERIAL

FORM 2603-107 REV. 9-61

DO NOT SCALE DRAWING

UNLESS OTHERWISE SPECIFIED TOLERANCES:
DECIMALS ANGLES
XX ± .03 XXX ± .010 ± 1/2°
BREAK ALL SHARP EDGES APPROX .010
C'BORE AND SPOTFACE CORNER RADII .010
ROUGHNESS OF ALL MACHINED SURFACES
√ PER MIL-STD-10

MATERIAL

FINISH

3107280	TM-7211
NEXT ASSY.	1ST USED ON
APPLICATION	

THE INFORMATION HEREON IS THE PROPERTY OF AMPEX COMPUTER PRODUCTS COMPANY. NO REPRODUCTION OR UNAUTHORIZED USE IN PART OR IN WHOLE SHALL BE MADE WITHOUT WRITTEN CONSENT OF AMPEX COMPUTER PRODUCTS CO.

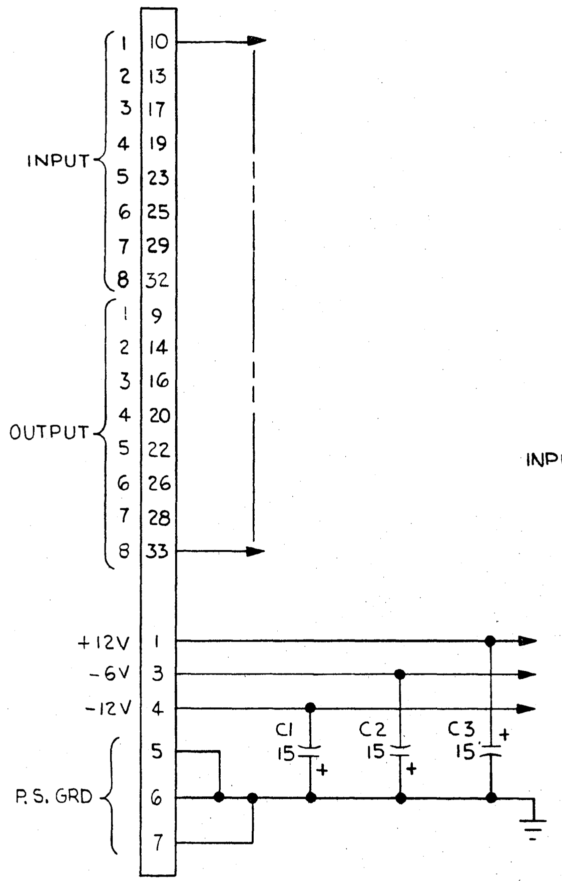
PROJ SUPER	[illegible]	4/6/64
PROJ ENGR	[illegible]	4/16/64
ENGR		4/16/64
CHKR	[illegible]	5/MAR 1964
DFTSMN	[illegible]	3-4-64

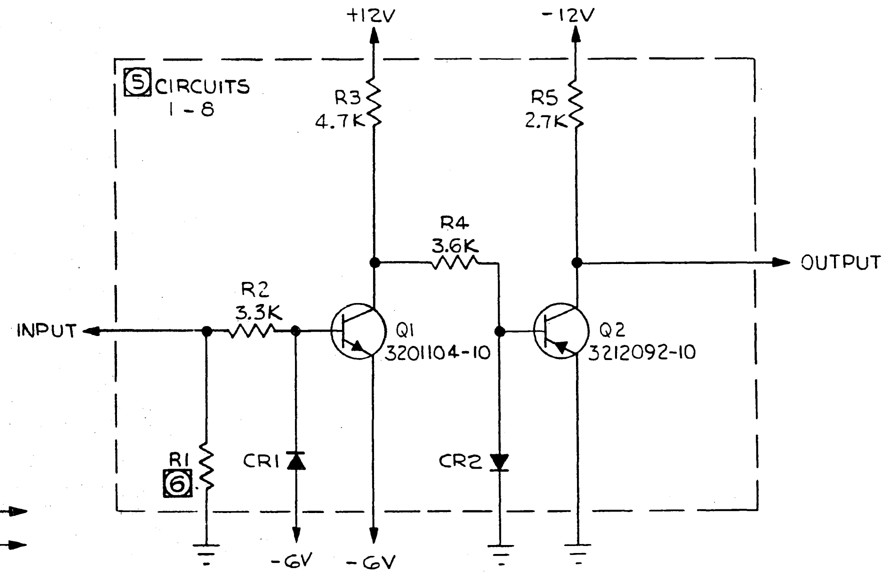
AMPEX 0/1 AMPEX COMPUTER PRODUCTS COMPANY
9937 JEFFERSON BLVD. CULVER CITY, CALIFORNIA

TITLE
CIRCUIT BOARD ASSY—
FLIP-FLOP, TYPE P

CODE IDENT. NO. | SIZE | DWG. NO. | ISSUE
SCALE 2:1 | D | 3107275 | A

REVISIONS					
ISSUE	DESCRIPTION	DATE	DRAFTSMAN	DATE	APPROVAL
D	ECN 911-AN REDRAW	10-29-65	[illegible]	10-29-65	[illegible]
E	ECN 5051	4-11-66	L.C.	4-11-66	[illegible]
F	ECN 5912	8/17/66	[illegible]	[illegible]	[illegible]





DWG. NO. 3107038

TABLE I

ASSEMBLY	USED ON	COMPONENT R1	
3107037-10	DE 200	7.5 K	
3107258-10	DE 200	7.5 K	
3118156-01	TM 12213 WE	36 K	
3118279-01	DE-212 (EAI)	270Ω	

6 SEE TABLE I

5 PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. PREFIX THE REFERENCE DESIGNATION WITH THE CIRCUIT NUMBER FOR COMPLETE DESIGNATION.

4. ALL DIODES TO BE 3263024-10.
3. ALL RESISTOR VALUES ARE IN 1/4W ±5%.
2. ALL CAPACITOR VALUES ARE IN MICROFARADS, 20V ±20%.
1. FOR ASSEMBLY SEE TABLE I.

NOTES: UNLESS OTHERWISE SPECIFIED.

NEXT ASSY.	1ST USED ON
SEE TABLE	—

APPLICATION

DO NOT SCALE DRAWING

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

TOLERANCES: DECIMALS .XX ±.03 .XXX ±.010; ANGLES ±1/2°

BREAK ALL SHARP EDGES APPROX. .010. C'BORE AND SPOTFACE CORNER RADII APPROX. .010. ROUGHNESS OF ALL MACHINED SURFACES —— PER MIL-STD-10 ✓

MATERIAL

FINISH

THE INFORMATION HEREON IS THE PROPERTY OF AMPEX COMPUTER PRODUCTS DIVISION. NO REPRODUCTION OR UNAUTHORIZED USE IN PART OR IN WHOLE SHALL BE MADE WITHOUT WRITTEN CONSENT OF AMPEX COMPUTER PRODUCTS DIV.

PROJ SUPER	S. Blane	8-15-64
PROJ ENGR	S. Blane	8-15-64
ENGR	[illegible]	3/6-66
CHKR	R.B. Taylor	8-15-63
DFTSMN	[illegible]	4-6-63

AMPEX COMPUTER PRODUCTS DIVISION P.O. BOX 329, CULVER CITY, CALIF.

TITLE

SCHEMATIC-INPUT BUFFER

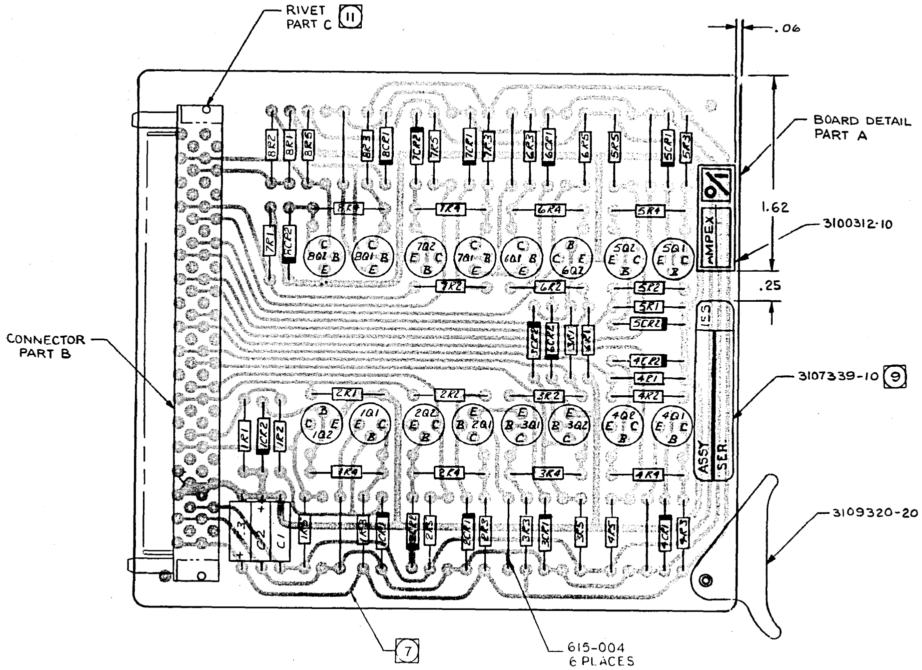
SIZE C | CODE IDENT. NO. 09150 | DWG. NO. 3107038

SCALE NONE | SHEET 1 OF 1

REVISIONS				
ISSUE	DESCRIPTION	DRAFTSMAN	DATE	APPROVAL
A	E N 3.. 31 [illegible]	[illegible]	[illegible]	[illegible]
B	ECN 911-76	[illegible]	[illegible]	[illegible]
C	ECN 911-AN PROD	[illegible]	3-3-64	[illegible]
D	ECN 5051	S. Aramaki	4/11/66	[illegible]
E	ECN 5912	Aramaki	9/17/66	

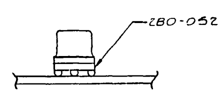
TABLE I

B/M REFERENCE TABLE		
ASSEMBLY	USED ON	PART D
3107037-10	DE-200	041-520
3107258-10	DE-200	041-520
3118156-01	TM-12213 BTL WE	041-751
3118279-01	DE-212(BAI)	041-503



PART NO.	REFERENCE DESIGNATION
3201104-10	1Q1 THRU 8Q1
3212092-10	1Q2 THRU 8Q2
37[illegible]024-10	1CR1 THRU 8CR1, 1CR2 THRU 8CR2
037-990	C 1,2,3
041-407	1R2 THRU 8R2
041-442	1R5 THRU 8R5
041-412	1R3 THRU 8R3
12 PART D	1R1 THRU 8R1
041-571	1R4 THRU 8R4

REFERENCE



TYPICAL TRANSISTOR INSTALLATION

12. INSTALL PART D PER TABLE I.
11. RIVET, PART C USED ONLY WITH 3200526-10.
10. SEAL PRINTED CIRCUIT SIDE ONLY WITH HUMI-SEAL TYPE 1B15, COLUMBIA TECH CORP OR EQUIV.
9. MARK PART NO AND NAMEPLATE INFORMATION PER MIL-STD-130.
8. PART NO. TO BE AS SHOWN ON TABLE I.
7. CIRCUITRY ON FARSIDE.
6. PLUS SIGN ON CAPACITOR INDICATES POSITIVE.
5. COMPONENT DESIGNATIONS ARE FOR REFERENCE ONLY.
4. ASSEMBLE PER MANUFACTURING PRACTICE MANUAL.
3. HEAVY LINE ON DIODE INDICATES CATHODE.
2. FOR PRODUCT SPECIFICATION SEE 3107039.
1. FOR SCHEMATIC SEE 3107038.

NOTES: UNLESS OTHERWISE SPECIFIED

REQD.	PART NO.	DESCRIPTION	REFERENCE	ZONE	ITEM

NEXT ASSY.	1ST USED ON
3107258	TM7211
3107037	TM7211
310725[illegible]	TM7212
310[illegible]	[illegible]
APPLICATION	

DO NOT SCALE DRAWING

UNLESS OTHERWISE SPECIFIED TOLERANCES
DECIMALS .XX ± .03 .XXX ± .010 ANGLES ± 1 2°
BREAK ALL SHARP EDGES APPROX. .010
C'BORE AND SPOTFACE CORNER RADII .010
ROUGHNESS OF ALL MACHINED SURFACES ✓ PER MIL-STD-10

MATERIAL

FINISH

FORM 2602-107 REV. 9 61 — LIST OF MATERIAL

THE INFORMATION HEREON IS THE PROPERTY OF AMPEX COMPUTER PRODUCTS COMPANY. NO REPRODUCTION OR UNAUTHORIZED USE IN PART OR IN WHOLE SHALL BE MADE WITHOUT WRITTEN CONSENT OF AMPEX COMPUTER PRODUCTS CO.

PROJ SUPER	[illegible]	5/6/[illegible]
PROJ ENGR		
ENGR	[illegible]	[illegible]
CHKR	[illegible]	[illegible]
DFTSMN	[illegible]	4-27-[illegible]

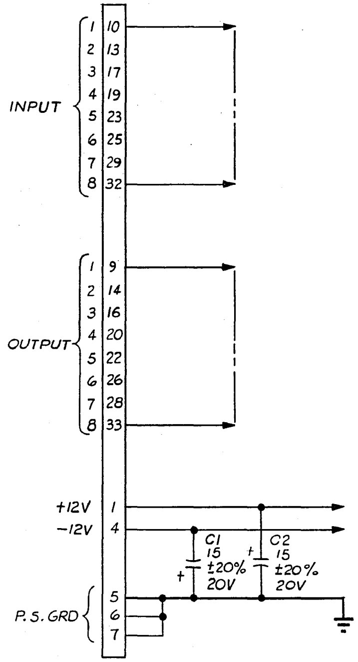
AMPEX COMPUTER PRODUCTS COMPANY
9937 JEFFERSON BLVD. CULVER CITY, CALIFORNIA

TITLE: CIRCUIT BOARD ASSEMBLY- INPUT BUFFER

CODE INDENT. NO. | SIZE D | DWG. NO. 31[illegible] | ISSUE E

SCALE 2/1

REVISIONS					
ISSUE	DESCRIPTION	DATE	DRAFTSMAN	DATE	APPROVAL
B	ECN 9827 CONT	4-26-68	H. Brozo	4/29/68	



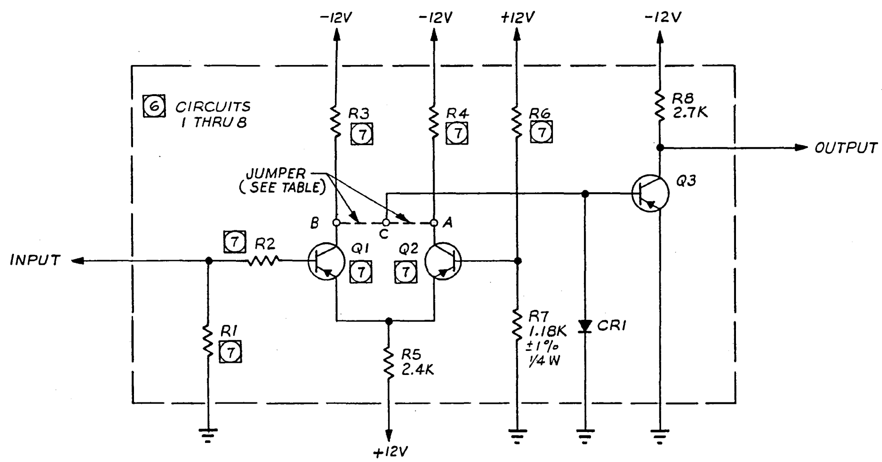


TABLE I

ASSEMBLY NO.	INPUT LEVEL	COMPONENTS						
		R1	R2	R3	R4	R6	Q1 & Q2	JUMPER
3118170-01	+3/0V	4.7K	470 Ω	JUMPER	7.5K	8.25K,±1%	014-505	POSITION A TO C
3118171-01	+6/0V	10K	2.7K		↑	3.57K,±1%	014-505	
3118172-01	+9/0V	10K	4.7K			1.91K,±1%	014-505	
3118173-01	+12/0V	10K	4.7K		↓	1.91K,±1%	3212053-10	
3123922-01	+6/0V	2.4K	2.7K		7.5K	3.57K±1%	014-505	
3118227-01	0/+3V	OPEN	470 Ω	7.5K	JUMPER	8.25K±1%	014-505	POSITION B TO C
3118228-01	0/+6V	↑	2.7K	↑		3.57K±1%	014-505	
3118229-01	0/+9V	↓	4.7K	↓		1.91K±1%	014-505	
3118230-01	0/+12V	OPEN	4.7K	7.5K		1.91K±1%	3212053-10	

7. SEE TABLE.
6. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. PREFIX THE REFERENCE DESIGNATION WITH THE CIRCUIT NUMBER FOR COMPLETE DESIGNATION.
5. ALL TRANSISTORS TO BE 3212092-10.
4. ALL DIODES TO BE 3263024-10.
3. ALL RESISTOR VALUES ARE IN OHMS, ±5%, 1/4W.
2. ALL CAPACITOR VALUES ARE IN MICROFARADS.
1. FOR ASSEMBLY SEE TABLE I.
NOTES:

3123922	AUTONETICS
SEE TABLE	DE-200
NEXT ASSY.	1ST USED ON
APPLICATION	

DO NOT SCALE DRAWING
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
DECIMALS TOLERANCES ANGLES
.XX± — .XXX± — ± —
BREAK ALL SHARP EDGES APPROX. .010. C'BORE AND SPOTFACE CORNER RADII APPROX. .010.
ROUGHNESS OF ALL MACHINED SURFACES — PER MIL-STD-10 ✓
MATERIAL
FINISH

THE INFORMATION HEREON IS THE PROPERTY OF AMPEX COMPUTER PRODUCTS DIVISION. NO REPRODUCTION OR UNAUTHORIZED USE IN PART OR IN WHOLE SHALL BE MADE WITHOUT WRITTEN CONSENT OF AMPEX COMPUTER PRODUCTS DIV.

PROJ SUPER
PROJ ENGR /N S [illegible]
ENGR
CHKR
DFTSMN [illegible] 6/20/66

AMPEX COMPUTER PRODUCTS DIVISION P.O. BOX 329, CULVER CITY, CALIF.

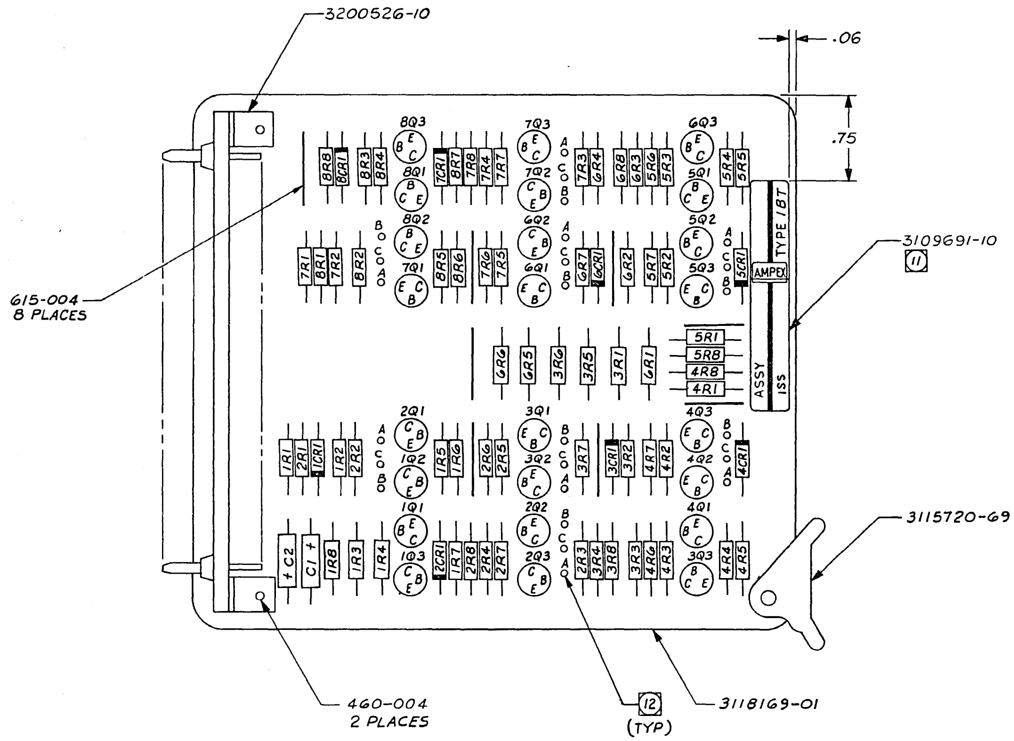
TITLE SCHEMATIC — INPUT BUFFER -T (POSITIVE LOGIC)

SIZE D | CODE IDENT. NO. 09150 | DWG. NO. 3118175
SCALE NONE | SHEET 1 OF 1

ISSUE	DESCRIPTION	DATE	DRAFTSMAN	DATE	APPROVAL
B	ECN 9827 CONT	9/26/68	[illegible]		

TABLE I

ASSEMBLY NO.	INPUT LEVEL	PART A	PART B	PART C	PART D	PART D	PART F	JUMPER
		COMPONENTS						
3123922-01	+6/0V	041-570	041-442	JUMPER	041-520	048-047	014-505	POSITION A TO C
3118170-01	+3/0V	041-412	041-428		041-520	042-431	014-505	
3118171-01	+6/0V	041-408	041-442		041-520	048-047	014-505	
3118172-01	+9/0V	041-408	041-412		041-520	042-422	014-505	
3118173-01	+12/0V	041-408	041-412		041-520	042-422	3212053-10	
3118227-01	0/+3V	NOT USED	041-428	041-520	JUMPER	042-431	014-505	POSITION B TO C
3118228-01	0/+6V	↕	041-442	041-520		048-047	014-505	
3118229-01	0/+9V		041-412	041-520		042-422	014-505	
3118230-01	0/+12V	NOT USED	041-412	041-520		042-422	3212053-10	



PART NO.	REFERENCE DESIGNATION
3263024-10	1CR1 THRU 8CR1
037-068	C1, C2
041-570	1R5 THRU 8R5
041-442	1R8 THRU 8R8
048-391	1R7 THRU 8R7
3212092-10	1Q3 THRU 8Q3
PART A	1R1 THRU 8R1
PART B	1R2 THRU 8R2
PART C	1R3 THRU 8R3
PART D	1R4 THRU 8R4
PART E	1R6 THRU 8R6
PART F	1Q1 THRU 8Q1, 1Q2 THRU 8Q2

12 FOR JUMPER POSITIONS SEE TABLE I.

11 MARK PART NO. AND NAMEPLATE INFORMATION PER MIL-STD-130.

10. PART NO. TO BE AS SHOWN ON TABLE I.

9. SEAL PRINTED CIRCUIT SIDE ONLY WITH HUMISEAL TYPE 1B15 COLUMBIA TECH. CORP. OR EQUIV.

~~8. MARK POT REF NO's. .12 HIGH CHARACTERS, COLOR WHITE, PER MIL-STD-130. DO NOT IMPRESSION STAMP.~~

~~7. TRIMPOTS NOT TO BE SUBMERGED IN WATER.~~

6. COMPONENT DESIGNATIONS ARE FOR REF. ONLY.

5. PLUS SIGN ON CAPACITOR INDICATES POSITIVE.

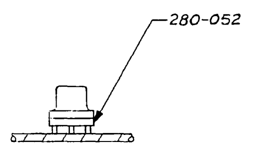
4. HEAVY LINE ON DIODES INDICATES CATHODE.

3. ASSEMBLE PER AMPEX STANDARDS.

2. FOR PERF SPECIFICATION SEE 3118176.

1. FOR SCHEMATIC SEE 3118175.

NOTES:



TYPICAL TRANSISTOR INSTALLATION

REFERENCE

DO NOT SCALE DRAWING
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: DECIMALS .XX ± .05 .XXX ± .010; ANGLES ± 1/2°
BREAK ALL SHARP EDGES APPROX. .010. C'BORE AND SPOTFACE CORNER RADII APPROX. .010. ROUGHNESS OF ALL MACHINED SURFACES PER MIL-STD-10
MATERIAL
FINISH

NEXT ASSY.	1ST USED ON
3123922	AUTONETICS
SEE TABLE	DE-200

APPLICATION

DWG. NO. 3118174

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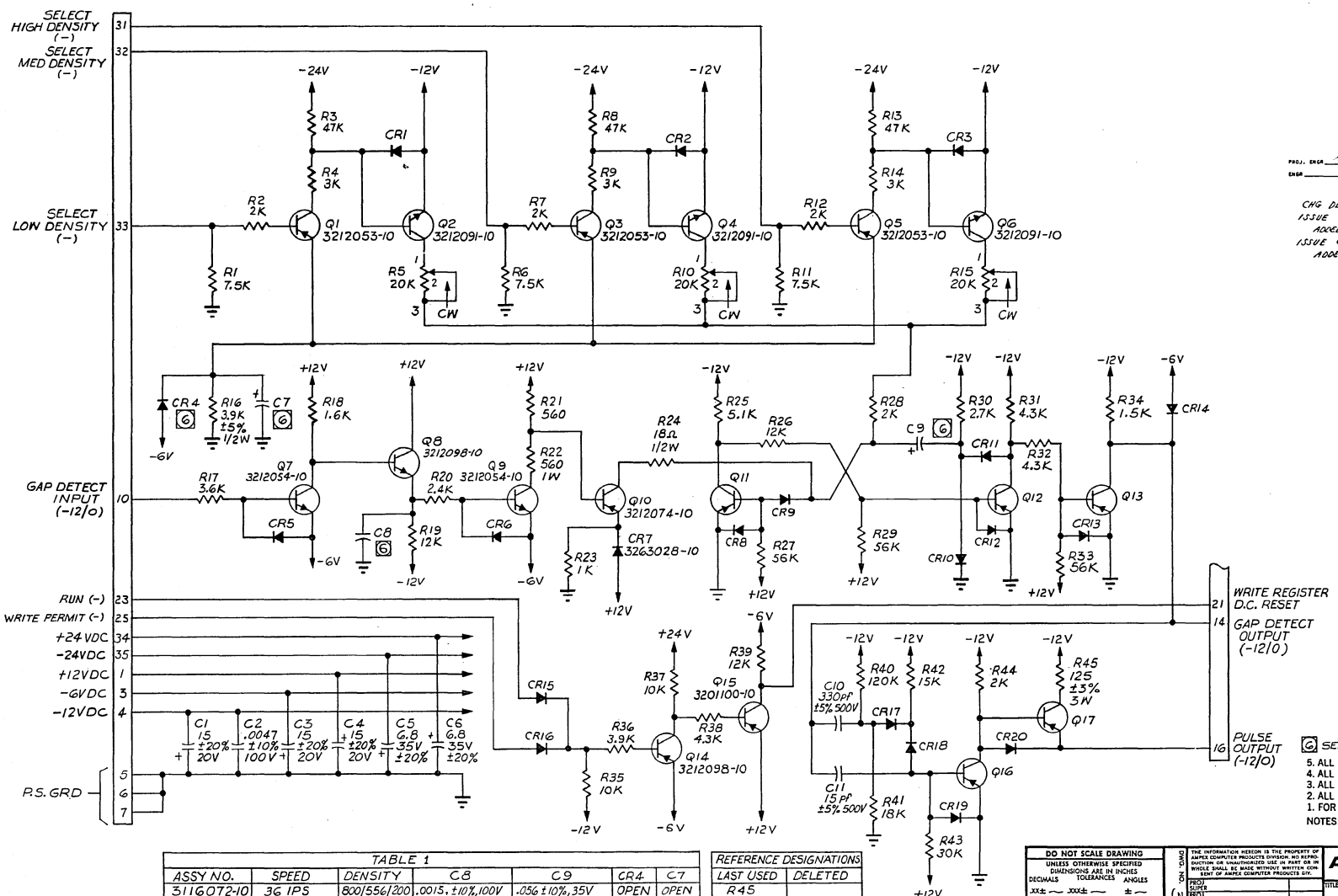
PROJ SUPER
PROJ ENGR [illegible]
ENGR
CHKR
DFTSMN [illegible] 6/27/66

AMPEX COMPUTER PRODUCTS DIVISION P.O. BOX 329, CULVER CITY, CALIF.

TITLE: CIRCUIT BOARD ASSY—INPUT BUFFER -T (POSITIVE LOGIC)

SIZE D | CODE IDENT. NO. 09150 | DWG. NO. 3118174

SCALE 2:1 | SHEET 1 OF 1



REVISIONS					
ISSUE	DESCRIPTION	DATE	DRAFTSMAN	DATE	APPROVAL

ISSUE C

PROJ. ENGR J.M.

ENGR

CHG DESCRIPTION
ISSUE B
ADDED ASSY 3116142-10 TO TABLE I.
ISSUE C
ADDED ASSY 3118152-01 TO TABLE I.

TABLE 1

ASSY NO.	SPEED	DENSITY	C8	C9	CR4	C7
3116072-10	36 IPS	800/556/200	.0015, ±10%, 100V	.056 ±10%, 35V	OPEN	OPEN
3116073-10	112.5/150 IPS	800/556/200	330pf ±5%, 500V	.015 ±10%, 35V	OPEN	OPEN
3116074-10	7.5 IPS	800/556/200	.0047 ±10%, 100V	.22 ±5%, 35V	OPEN	OPEN
3116142-10	56-75 IPS	800/556/200	470pf, ±5%, 300V	.027 ±10%, 35V	OPEN	OPEN
3118152-01	60 IPS	556/200	470 pf, ±5%, 300V	.047 ±10%, 35V	OPEN	OPEN

REFERENCE DESIGNATIONS	
LAST USED	DELETED
R45	
Q17	
CR20	
C11	

G SEE TABLE 1.

5. ALL TRANSISTORS TO BE 3201209Z-10.
4. ALL DIODES TO BE 3263024-10.
3. ALL RESISTOR VALUES ARE IN OHMS, ±5%, 1/4W.
2. ALL CAPACITOR VALUES ARE IN MICROFARADS.
1. FOR ASSEMBLY SEE TABLE 1.

NOTES: UNLESS OTHERWISE SPECIFIED.

DO NOT SCALE DRAWING
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES DECIMALS .xx ± .xxx ± ANGLES ±
BREAK ALL SHARP EDGES APPROX. .010. C'BORE AND SPOTFACE CORNER RADII APPROX. .010. ROUGHNESS OF ALL MACHINED SURFACES PER MIL-STD-10
MATERIAL
FINISH
SEE TABLE TM 7211
NEXT ASSY. 1ST USED ON
APPLICATION

DWG. NO. 3116076

THE INFORMATION HEREON IS THE PROPERTY OF AMPEX COMPUTER PRODUCTS DIVISION. NO REPRODUCTION OR UNAUTHORIZED USE IN PART OR IN WHOLE SHALL BE MADE WITHOUT WRITTEN CONSENT OF AMPEX COMPUTER PRODUCTS DIV.

PROJ SUPER
PROJ ENGR
ENGR
CHKR
DFTSMN Sujimoto 11-9-65

AMPEX COMPUTER PRODUCTS DIVISION P.O. BOX 328, CULVER CITY, CALIF.

TITLE
SCHEMATIC-
LCC GENERATOR-B

SIZE D | CODE IDENT. NO. 09150 | DWG. NO. 3116076

SCALE ~ | SHEET 1 OF 1

ISSUE	DESCRIPTION	DATE	DRAFTSMAN	DATE	APPROVAL

REVISIONS

ISSUE C

PROJ. ENGR

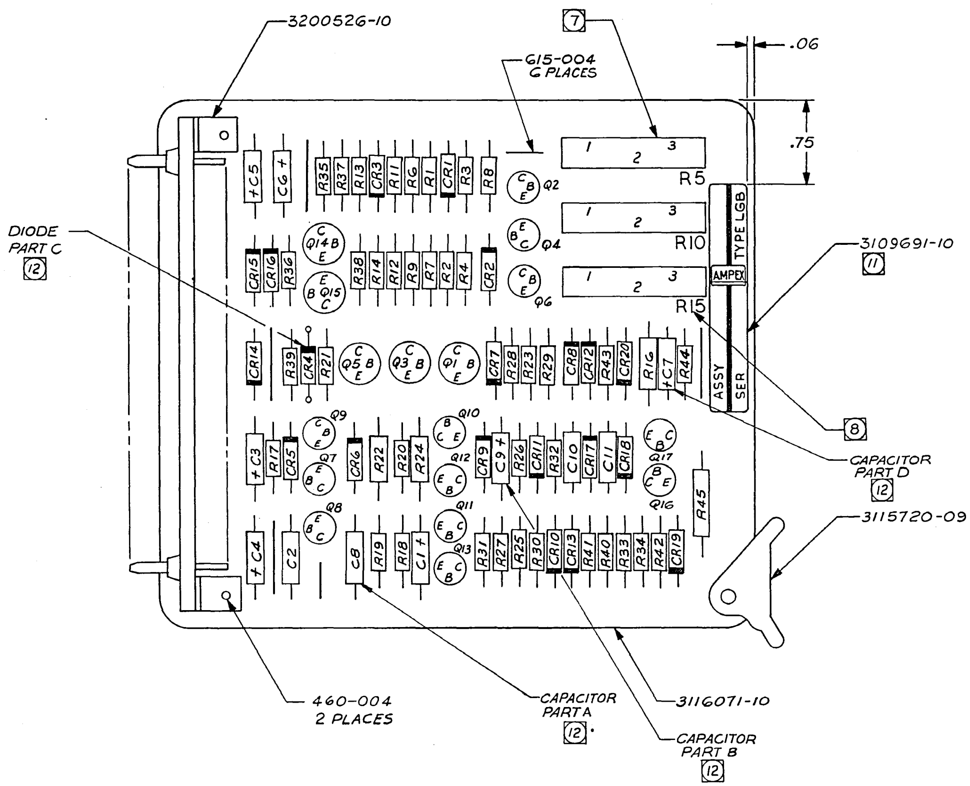
ENGR

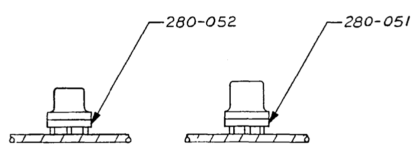
CHANGE DESCRIPTION

ISS 'B' ADDED ASSY 3116142-10
ISS 'C' ADDED ASSY 3118152-01

TABLE I

B/M REFERENCE TABLE						
ASSY NO.	SPEED	DENSITY	PART A	PART B	PART C	PART D
3116072-10	36 IPS	800/556/200	035-509	037-465	NOT USED	NOT USED
3116073-10	112.5/150 IPS	800/556/200	034-212	037-344	NOT USED	NOT USED
3116074-10	7.5 IPS	800/556/200	035-989	037-454	NOT USED	NOT USED
3116142-10	56-75 IPS	800/556/200	034-214	037-343	NOT USED	NOT USED
3118152-01	60 IPS	556/200	034-214	037-273	NOT USED	NOT USED





TYPICAL TRANSISTOR INSTALLATION

PART NO.	REFERENCE DESIGNATIONS	PART NO.	REFERENCE DESIGNATIONS
3201100-10	Q15	041-430	R34
3212053-10	Q1, Q3, Q5	041-436	R41
3212054-10	Q7, Q9	041-442	R30
3212074-10	Q10	041-482	R19, R26, R39
3212091-10	Q2, Q4, Q6	041-484	R40
3212092-10	Q11, Q12, Q13, Q16, Q17	041-497	R21
3212098-10	Q8, Q14	041-511	R36
3263024-10	CR1-CR3, CR5, CR6, CR8-CR20	041-519	R27, R29, R33
3263028-10	CR7,	041-520	R1, R6, R11
034-212	C10	041-411	R3, R8, R13
034-963	C11	041-560	R2, R7, R12, R28, R44
035-989	C2	041-561	R25
037-071	C5, C6	041-570	R20
PART A	C8	041-571	R17
037-990	C1, C3, C4	041-584	R31, R32, R38
041-408	R35, R37	041-612	R43
041-409	R42	041-595	R24
041-410	R23	044-313	R5, R10, R15
041-550	R4, R9, R14	047-302	R45
PART B	C9	047-891	R22
PART C	CR4	041-437	R18
PART D	C7		
041-303	R16		

12. INSTALL PARTS A THRU D PER TABLE I.

11. MARK PART NO. AND NAMEPLATE INFORMATION PER MIL-STD-130.

10. PART NO. TO BE AS SHOWN ON TABLE I.

9. SEAL PRINTED CIRCUIT SIDE ONLY WITH HUMISEAL TYPE 1B15 COLUMBIA TECH. CORP. OR EQUIV.

8. MARK POT REF. NO's. .12 HIGH CHARACTERS, COLOR WHITE, PER MIL-STD-130. DO NOT IMPRESSION STAMP.

7. TRIMPOTS NOT TO BE SUBMERGED IN WATER.

6. COMPONENT DESIGNATIONS ARE FOR REF. ONLY.

5. PLUS SIGN ON CAPACITOR INDICATES POSITIVE.

4. HEAVY LINE ON DIODES INDICATES CATHODE.

3. ASSEMBLE PER PRODUCTION PRACTICES MANUAL.

2. FOR ASSEMBLY SPECIFICATION SEE 3116077.

1. FOR SCHEMATIC SEE 3116076.

NOTES:

REFERENCE

SEE TABLE	TM-7211
NEXT ASSY.	1ST USED ON
APPLICATION	

DO NOT SCALE DRAWING

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

DECIMALS TOLERANCES ANGLES

.XX± .03 .XXX± .010 ± 1/2°

BREAK ALL SHARP EDGES APPROX. .010. C'BORE AND SPOTFACE CORNER RADII APPROX. .010. ROUGHNESS OF ALL MACHINED SURFACES —— PER MIL-STD-10 ✓

MATERIAL

FINISH

DWG. NO. 3116075

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PROJ SUPER

PROJ ENGR

ENGR

CHKR

DFTSMN Fujimoto 12-5-65

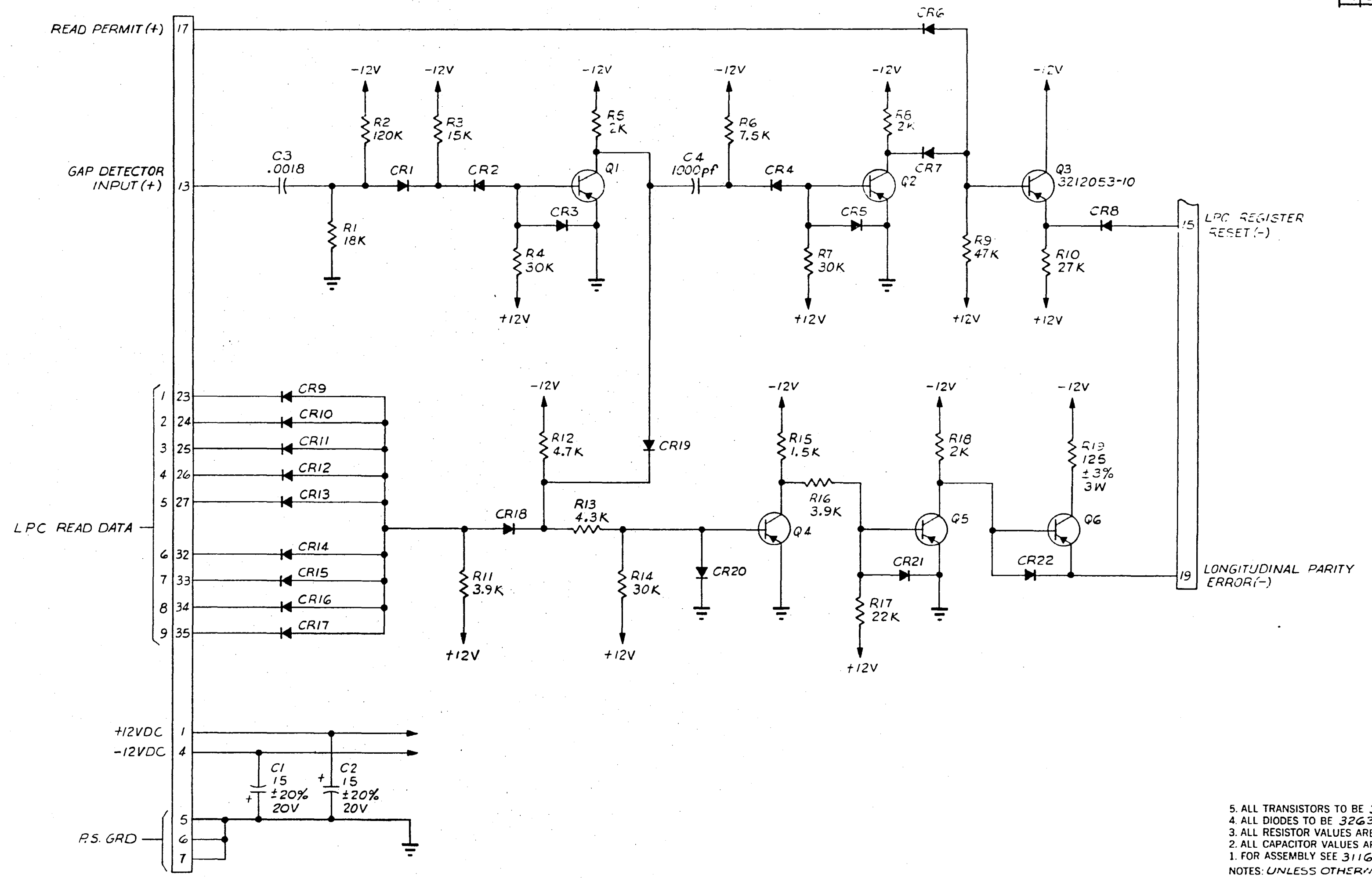
AMPEX COMPUTER PRODUCTS DIVISION P.O. BOX 329, CULVER CITY, CALIF.

TITLE CIRCUIT BOARD ASSY-LCC GENERATOR —B

SIZE	CODE IDENT. NO.	DWG. NO.
D	09150	3116075

SCALE 2:1 SHEET 1 OF 1

REVISIONS					
ISSUE	DESCRIPTION	DATE	DRAFTSMAN	DATE	APPROVAL
A	ERN [illegible] RFCD	[illegible]	[illegible]	[illegible]	[illegible]



REFERENCE DESIGNATIONS	
LAST USED	DELETED
C4	
CR22	
R19	
Q6	

5. ALL TRANSISTORS TO BE 3212092-10.
4. ALL DIODES TO BE 3263024-10.
3. ALL RESISTOR VALUES ARE IN OHMS ±5%, 1/4W.
2. ALL CAPACITOR VALUES ARE IN MICROFARADS ±5%, 100V.
1. FOR ASSEMBLY SEE 3116087.
NOTES: UNLESS OTHERWISE SPECIFIED.

DO NOT SCALE DRAWING
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
DECIMALS .XX± .XXX± TOLERANCES ANGLES ±
BREAK ALL SHARP EDGES APPROX. .010. C'BORE AND SPOTFACE CORNER RADII APPROX. .010.
ROUGHNESS OF ALL MACHINED SURFACES PER MIL-STD-10
MATERIAL
FINISH

3116087	TM-7211 (I.D.)
NEXT ASSY.	1ST USED ON
APPLICATION	

DWG. NO. 3116088

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PROJ SUPER / PROJ ENGR / ENGR / CHKR / DFTSMN

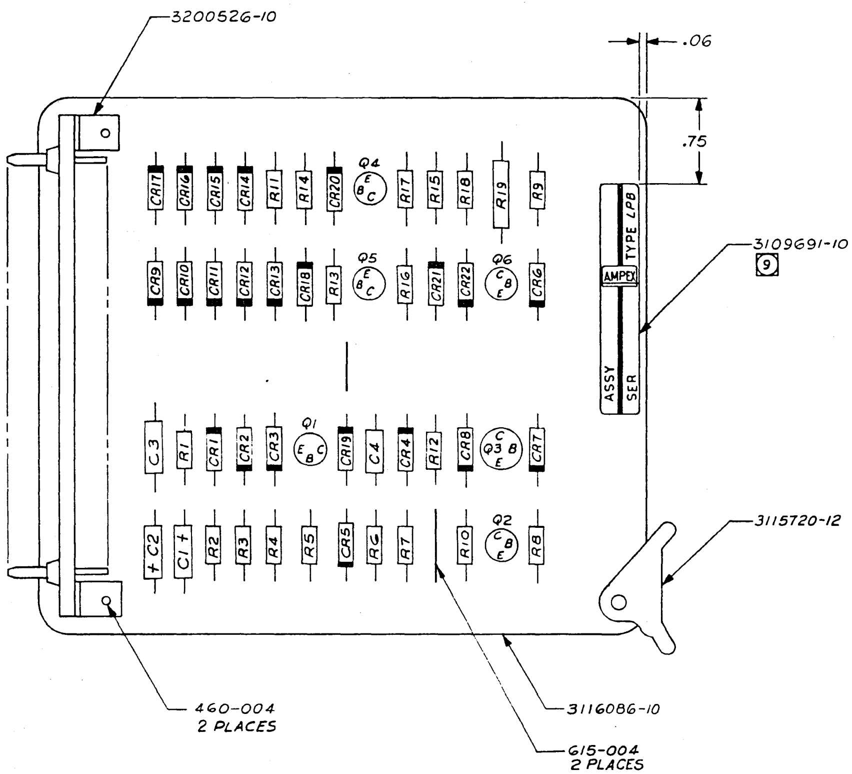
AMPEX COMPUTER PRODUCTS DIVISION P.O. BOX 329, CULVER CITY, CALIF.

TITLE: SCHEMATIC- LPC TIMING -B

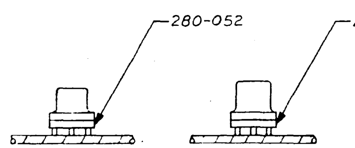
SIZE D | CODE IDENT NO 09150 | DWG NO 3116088

SCALE NONE | SHEET OF

REVISIONS					
ISSUE	DESCRIPTION	DATE	DRAFTSMAN	DATE	APPROVAL
A	ERN 106-CJ PROD.	12/21/65	Fujimoto	12/21/65	[illegible]



PART NO.	REFERENCE DESIGNATIONS	PART NO.	REFERENCE DESIGNATIONS
3212053-10	Q3	041-430	R15
3212092-10	Q1, Q2, Q4, Q5, Q6	041-436	R1
3263024-10	CR1 THRU CR22	041-483	R10
033-082	C3	041-484	R2
034-950	C4	041-511	R11, R16
037-990	C1, C2	041-520	R6
041-406	R17	041-560	R5, R8, R18
041-409	R3	041-584	R13
041-411	R9	041-612	R4, R7, R14
041-412	R12	047-302	R19



TYPICAL TRANSISTOR INSTALLATION

9. MARK PART NO. & NAMEPLATE INFORMATION PER MIL-STD-130.
8. PART NO. TO BE 3116087-10.
7. SEAL PRINTED CIRCUIT SIDE ONLY WITH HUMI-SEAL TYPE IB15 COLUMBIA TECH. OR EQUIV.
6. COMPONENT DESIGNATIONS ARE FOR REF. ONLY.
5. PLUS SIGN ON CAPACITOR INDICATES POSITIVE.
4. HEAVY LINE ON DIODES INDICATES CATHODE.
3. ASSEMBLE PER PRODUCTION PRACTICES MANUAL.
2. FOR ASSEMBLY SPECIFICATION SEE 3116089.
1. FOR SCHEMATIC SEE 3116088.

NOTES:

FINAL B/M	TM-T211(1D)
NEXT ASSY.	1ST USED ON
APPLICATION	

DO NOT SCALE DRAWING
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
DECIMALS TOLERANCES ANGLES
.XX ± .05 .XXX ± .010 ± 1/2°
BREAK ALL SHARP EDGES APPROX. .010. C'BORE AND SPOTFACE CORNER RADII APPROX. .010.
ROUGHNESS OF ALL MACHINED SURFACES —— PER MIL-STD-10 ✓
MATERIAL
FINISH

DWG. NO. 3116087

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PROJ SUPER		
PROJ ENGR	[signature]	21 DEC 65
ENGR	" "	" "
CHKR	S. Arumoki	12/21/65
DFTSMN	Fujimoto	12-1-65

AMPEX COMPUTER PRODUCTS DIVISION P.O. BOX 329, CULVER CITY, CALIF.

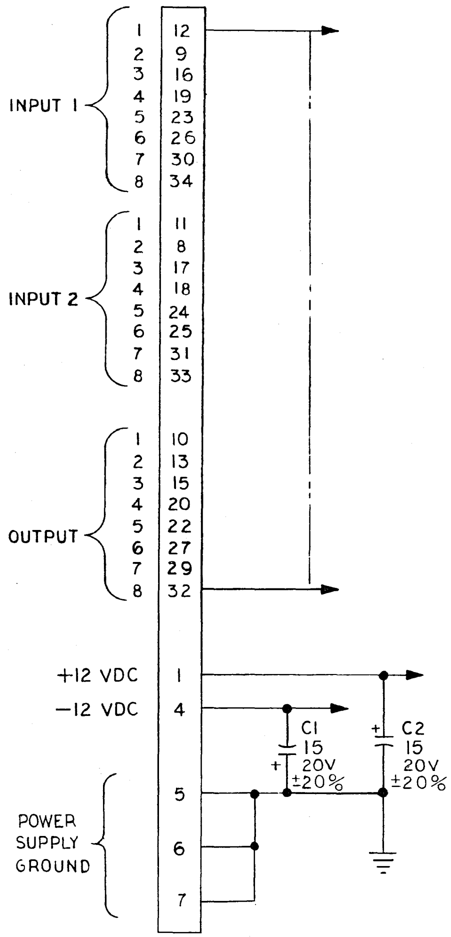
TITLE: CIRCUIT BOARD ASSY— LPC TIMING —B

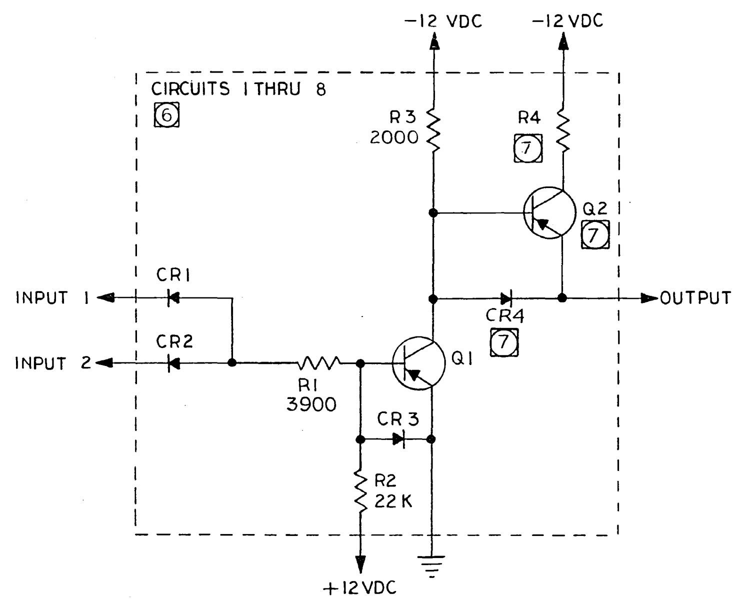
SIZE	CODE IDENT. NO.	DWG. NO.
D	09150	3116087
SCALE 2:1		SHEET 1 OF 1

REVISIONS				
ISSUE	DESCRIPTION	DRAFTSMAN	DATE	APPROVAL
A	ECN 800-54 DEV. PRO.(x-c)	B. Herr	8-23-63	
B	ECN 911-31		[illegible]	
C	ECN 911-AN PROD.		3-3-64	
D	ECN 8732	H Bravo	2-26-68	
E	ECN 8747	H Bravo	3-12-68	

TABLE I

ASSEMBLY	COMPONENTS		
	Q2	CR4	R4
3107042-10	3212092-10	3263024-10	125Ω±3% 3W
3107259-10	3212092-10	3263024-10	125Ω±3% 3W





8. FOR REF ASSY SEE 3107255
7 SEE TABLE I
6 PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. PREFIX THE DESIGNATING NUMBER WITH THE CIRCUIT NUMBER FOR COMPLETE DESIGNATION.
5. ALL DIODES TO BE 3263024-10.
4. ALL TRANSISTORS TO BE 3212092-10.
3. ALL RESISTOR VALUES ARE IN OHMS, 1/4W,±5%.
2. ALL CAPACITOR VALUES ARE IN MICROFARADS.
1. FOR ASSEMBLY SEE TABLE I

NOTES: UNLESS OTHERWISE SPECIFIED

NEXT ASSY.	1ST USED ON
3107042	TM-5
3107259	TM 7211
3107042	TM 7211
3107259	TM7212

APPLICATION

REQD.	PART NO.	DESCRIPTION	REFERENCE	ZONE	ITEM

LIST OF MATERIAL

DO NOT SCALE DRAWING

UNLESS OTHERWISE SPECIFIED TOLERANCES
DECIMALS .XX ± .03 .XXX ± .010 ANGLES ± 1/2°
BREAK ALL SHARP EDGES APPROX. .010
C'BORE AND SPOTFACE CORNER RADII .010
ROUGHNESS OF ALL MACHINED SURFACES ✓ PER MIL-STD-10

MATERIAL

FINISH

FORM 2602-107 REV. 9-61

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AMPEX COMPUTER PRODUCTS COMPANY
9937 JEFFERSON BLVD. CULVER CITY, CALIFORNIA

PROJ SUPER		
PROJ ENGR		
ENGR		
CHKR		8-15-63
DFTSMN	B. Herr	4-22-63

TITLE
SCHEMATIC — OUTPUT DRIVER

CODE INDENT. NO. | SIZE C | DWG. NO. 3107043 | ISSUE E

SCALE NONE

REVISIONS				
ISSUE	DESCRIPTION	DRAFTSMAN	DATE	APPROVAL
A	ECN 911-31 DEV. PROD.	[illegible]	11-[illegible]	[illegible]
B	ECN 911 AN PROD.	[illegible]	3-5-68	[illegible]
C	ECN 8732	W Brant	2-26-68	[illegible]
D	ECN 8747	W Brant	3-18-68	[illegible]
E	ECN 9076	W Brant	4-10-68	[illegible]

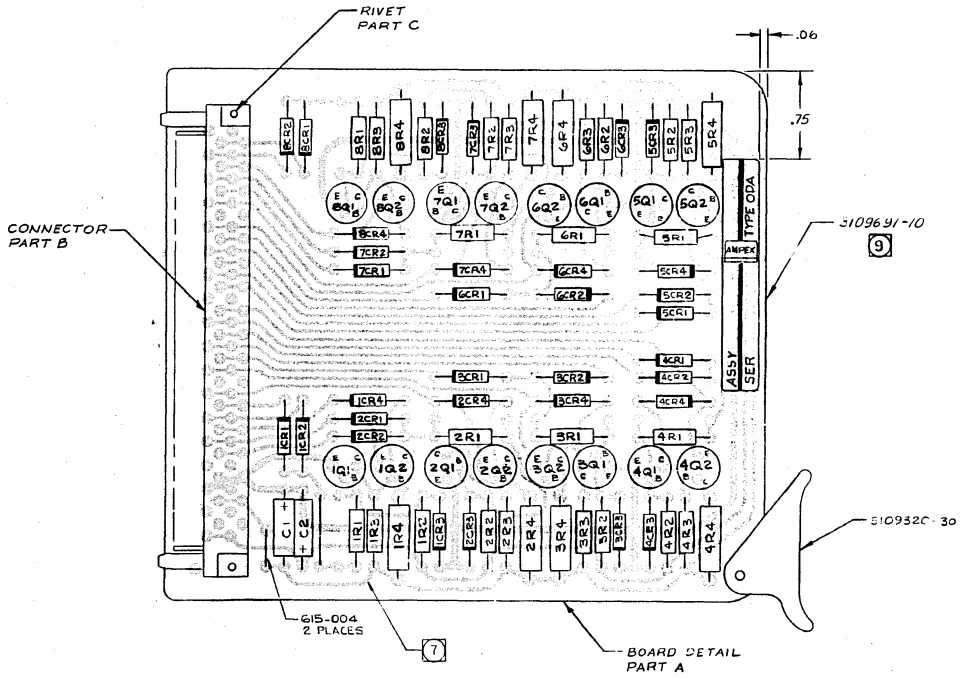

TABLE I

ASSEMBLY	PART A	PART B	PART C	PART D	PART E	PART F
3107042-10	3107041-10	3200504-10	NOT USED	3212092-10	3263024-10	047-302
3107259-10	3107041-20	3200526-10	460-004	3212092-10	3263024-10	047-302

REFERENCE

PART NO.	REFERENCE DESIGNATION
3212092-10	1Q1 THRU 8Q1
3263024-10	1CR1 THRU 8CR1, 1CR2 THRU 8CR2, 1CR3 THRU 8CR3
037-900	C1, C2
041-406	1R2 THRU 8R2
041-511	1R1 THRU 8R1
041-560	1R3 THRU 8R3
12 PART F	1R4 THRU 8R4
12 PART D	1Q2 THRU 8Q2
12 PART E	1CR4 THRU 8CR4

12 INSTALL PART A THRU F PER TABLE I

~~11 RIVET, PART C USED ONLY WITH 3200526-10~~

10 SEAL PRINTED CIRCUIT SIDE ONLY WITH HUMI-SEAL TYPE 1B15, COLUMBIA TECH CORP OR EQUIV.

9 MARK PART NO. AND NAMEPLATE INFORMATION PER MIL-STD-130.

8. PART NO. TO BE AS SHOWN IN BILL OF MATERIAL

7 CIRCUITRY ON FARSIDE

6. PLUS SIGN ON CAPACITOR INDICATES POSITIVE

5. COMPONENT DESIGNATIONS ARE FOR REFERENCE ONLY

4. ASSEMBLE PER *AMPEX STANDARDS*

3. HEAVY LINE ON DIODE INDICATES CATHODE

2. FOR *PERF* SPECIFICATION SEE 3107044

1. FOR SCHEMATIC SEE 3107043

NOTES: UNLESS OTHERWISE SPECIFIED

TYPICAL TRANSISTOR INSTALLATION

3107042	TM7211
3107259	TM7211
3107259	TM7212
3107042	TM5
NEXT ASSY.	1ST USED ON
APPLICATION	

REQD.	PART NO.	DESCRIPTION	REFERENCE	ZONE	ITEM
		FORM 2502-107 REV. 9-61 LIST OF MATERIAL			

DO NOT SCALE DRAWING

UNLESS OTHERWISE SPECIFIED TOLERANCES: DECIMALS XX ± .03 XXX ± .010 ANGLES ± 1/2° BREAK ALL SHARP EDGES APPROX .010 C'BORE AND SPOTFACE CORNER RADII .010 ROUGHNESS OF ALL MACHINED SURFACES √ PER MIL-STD-10

MATERIAL

FINISH

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PROJ SUPER	[illegible]	3/68
PROJ ENGR	[illegible]	4/11/68
ENGR	[illegible]	5/6/68
CHKR	[illegible]	5/8/68
DFTSMN	B. [illegible]	4-23-68

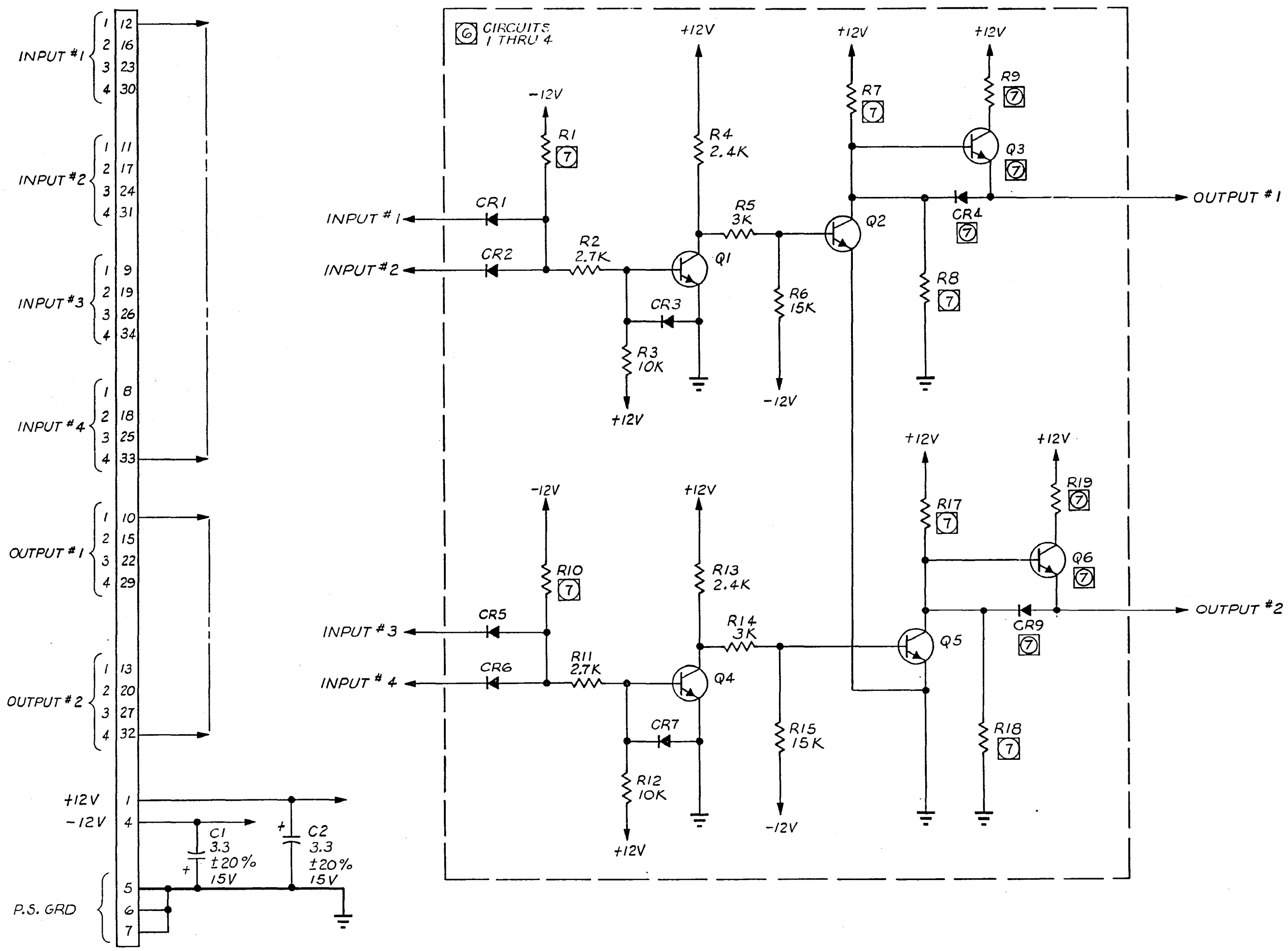
AMPEX AMPEX COMPUTER PRODUCTS COMPANY 9937 JEFFERSON BLVD. CULVER CITY, CALIFORNIA

TITLE: CIRCUIT BOARD ASSEMBLY OUTPUT DRIVER

CODE IDENT. NO. | SIZE D | DWG. NO. 3107255 | ISSUE D

SCALE 2/1

REVISIONS					
ISSUE	DESCRIPTION	DATE	DRAFTSMAN	DATE	APPROVAL
B	ECN 5936 PROD REL	8/23/66			
C	ECN 8008				
D	ECN 7200	12-16-66	REISS		
E	ECN 5553	8-17-66			
F	ECN 7884			9/26/67	



8. FOR REF ASSY SEE 3118183.
7 SEE TABLE 1
6 PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. PREFIX THE REFERENCE DESIGNATION WITH THE CIRCUIT NUMBER FOR COMPLETE DESIGNATION.
5. ALL TRANSISTORS TO BE 3201104-10.
4. ALL DIODES TO BE 3263028-10.
3. ALL RESISTOR VALUES ARE IN OHMS, ±5%, 1/4W.
2. ALL CAPACITOR VALUES ARE IN MICROFARADS.
1. FOR ASSEMBLY SEE TABLE 1.
NOTES:

TABLE 1

ASSEMBLY	OUTPUT LEVEL	COMPONENTS (CKT 1 THRU 4)					
		R1 & R10	R7 & R17	R8 & R18	R9 & R19	Q3 & Q6	CR4 & CR9
3118179-01	+3/0	OPEN	6.19K ±1%, 1/4W	2.74K ±1%, 1/4W	125 ±3% 3W	3201104-10	3263024-10
3118180-01	+6/0	OPEN	2.21K ±1%, 1/4W	2.74K ±1%, 1/4W	125 ±3% 3W	3201104-10	3263024-10
3118181-01	+9/0	OPEN	1.82K ±1%, 1/4W	7.5K ±1%, 1/4W	125 ±3% 3W	3201104-10	3263024-10
3118182-01	+12/0	OPEN	2K ±5%, 1/4W	OPEN	125 ±3% 3W	3201104-10	3263024-10
3118292-01	+4/0	OPEN	5.49K ±1%, 1/4W	2.74K ±1%, 1/4W	125 ±3% 3W	3201104-10	3263024-10
3119498-01	+8/0	OPEN	3.01K ±1%, 1/4W	7.5K ±1%, 1/4W	125 ±3% 3W	3201104-10	3263024-10
3119588-01	+5/0	OPEN	2.74K ±1%, 1/4W	2K ±1% 1/4W	125 ±3% 3W	3201104-10	3263024-10
3123873-01	+6/0	OPEN	1.2K ± 1% 1/4W	1.2K ± 1% 1/4W	OPEN	OPEN	JUMPER

NEXT ASSY.	1ST USED ON
SEE TABLE	

APPLICATION

DO NOT SCALE DRAWING
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
DECIMALS TOLERANCES ANGLES
.XX± — .XXX± — ± —
BREAK ALL SHARP EDGES APPROX. .010. C'BORE AND SPOTFACE CORNER RADII APPROX. .010. ROUGHNESS OF ALL MACHINED SURFACES — PER MIL-STD-10 ✓
MATERIAL
FINISH

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PROJ SUPER
PROJ ENGR
ENGR
CHKR
DFTSMN 6/15/66

AMPEX COMPUTER PRODUCTS DIVISION
P.O. BOX 329, CULVER CITY, CALIF.

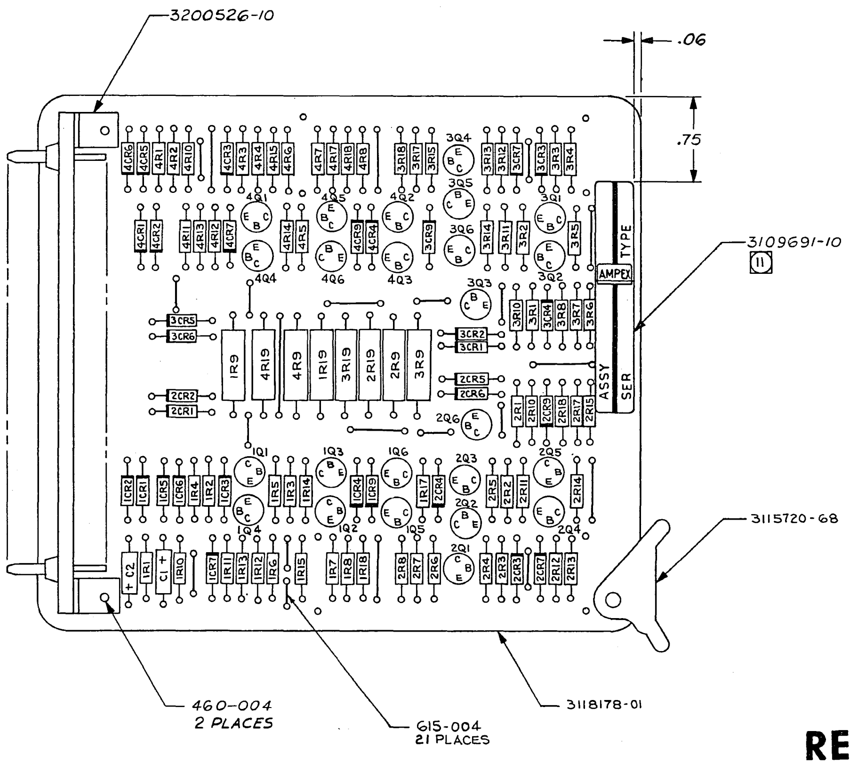
TITLE SCHEMATIC — OUTPUT DRIVER -L (NON-INV POSITIVE OUTPUT)

SIZE D | CODE IDENT. NO. 09150 | DWG. NO. 3118184
SCALE NONE | SHEET 1 OF 1

B/M REFERENCE TABLE

ASSEMBLY	OUTPUT LEVEL	PART A	PART B	PART C	PART D	PART E	PART F
3118179-01	+3/0	NOT USED	042-881	048-186	047-302	3201104-10	3263024-10
3118180-01	+6/0	NOT USED	042-423	048-186	047-302	3201104-10	3263024-10
3118181-01	+9/0	NOT USED	042-460	042-430	047-302	3201104-10	3263024-10
3118182-01	+12/0	NOT USED	041-560	NOT USED	047-302	3201104-10	3263024-10
3118292-01	+4/0	NOT USED	057-540	048-186	047-302	3201104-10	3263024-10
3119498-01	+8/0	NOT USED	042-866	042-430	047-302	3201104-10	3263024-10
3119588-01	+5/0	NOT USED	042-426	048-052	047-302	3201104-10	3263024-10
3123873-01	+6/0	NOT USED	042-517	042-517	OPEN	OPEN	JUMPER

REVISIONS					
ISSUE	DESCRIPTION	DATE	DRAFTSMAN	DATE	APPROVAL
B	ECN 5936 PROD REL	8/23/66	[illegible]	[illegible]	[illegible]
C	ECN 8008	[illegible]	[illegible]	[illegible]	[illegible]
D	ECN 7200	[illegible]	RE1[illegible]	[illegible]	[illegible]
E	ECN 5553	8-17-67	H. Brodo	8/18/67	[illegible]
F	ECN 7884	[illegible]	[illegible]	[illegible]	[illegible]

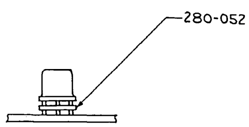


PART NO.	REFERENCE DESIGNATION
3201104-10	1Q1 THRU 4Q1, 1Q2 THRU 4Q2, 1Q4 THRU 4Q4, 1Q5 THRU 4Q5,
(12) PART F	1CR4 THRU 4CR4, 1CR9 THRU 4CR9
3263028-10	1CR1 THRU 4CR1, 1CR2 THRU 4CR2, 1CR3 THRU 4CR3, 1CR5 THRU 4CR5, 1CR6 THRU 4CR6, 1CR7 THRU 4CR7,
041-408	1R3 THRU 4R3; 1R12 THRU 4R12
041-409	1R6 THRU 4R6; 1R15 THRU 4R15
041-442	1R2 THRU 4R2; 1R11 THRU 4R11
041-550	1R5 THRU 4R5; 1R14 THRU 4R14
041-570	1R4 THRU 4R4, 1R13 THRU 4R13
(12) PART E	1Q3 THRU 4Q3, 1Q6, THRU 4Q6
(12) PART D	1R9 THRU 4R9; 1R19 THRU 4R19
(12) PART A	1R1 THRU 4R1; 1R10 THRU 4R10
(12) PART B	1R7 THRU 4R7; 1R17 THRU 4R17
(12) PART C	1R8 THRU 4R8; 1R18 THRU 4R18
037-056	C1, C2

12. INSTALL PART A, B, C, D, E, & F PER B/M REFERENCE TABLE.
11. MARK PART NO. AND NAMEPLATE INFORMATION PER MIL-STD-130.
10. PART NO. TO BE AS SHOWN ON TABLE.
9. SEAL PRINTED CIRCUIT SIDE ONLY WITH HUMISEAL TYPE 1B15 COLUMBIA TECH. CORP. OR EQUIV.
8. ~~MARK POT REF. NO's. .12 HIGH CHARACTERS, COLOR WHITE, PER MIL-STD-130. DO NOT IMPRESSION STAMP.~~
7. ~~TRIMPOTS NOT TO BE SUBMERGED IN WATER.~~
6. COMPONENT DESIGNATIONS ARE FOR REF. ONLY.
5. PLUS SIGN ON CAPACITOR INDICATES POSITIVE.
4. HEAVY LINE ON DIODES INDICATES CATHODE.
3. ASSEMBLE PER PRODUCTION PRACTICES MANUAL.
2. FOR PERF SPECIFICATION SEE 3118185
1. FOR SCHEMATIC SEE 3118184.

NOTES:

REFERENCE



TYPICAL TRANSISTOR INSTALLATION

SEE TABLE	DE-200
NEXT ASSY.	1ST USED ON
APPLICATION	

DO NOT SCALE DRAWING
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
DECIMALS TOLERANCES ANGLES
.XX± .XXX± ±
BREAK ALL SHARP EDGES APPROX. .010. C'BORE AND SPOTFACE CORNER RADII APPROX. .010.
ROUGHNESS OF ALL MACHINED SURFACES —— PER MIL-STD-10 ✓
MATERIAL
FINISH

DWG. NO. 3118183

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PROJ SUPER	[illegible]	8/30/66
PROJ ENGR		
ENGR	[illegible]	[illegible]
CHKR	[illegible]	8/25/66
DFTSMN	Chatzke	6/27/66

AMPEX COMPUTER PRODUCTS DIVISION P.O. BOX 329, CULVER CITY, CALIF.

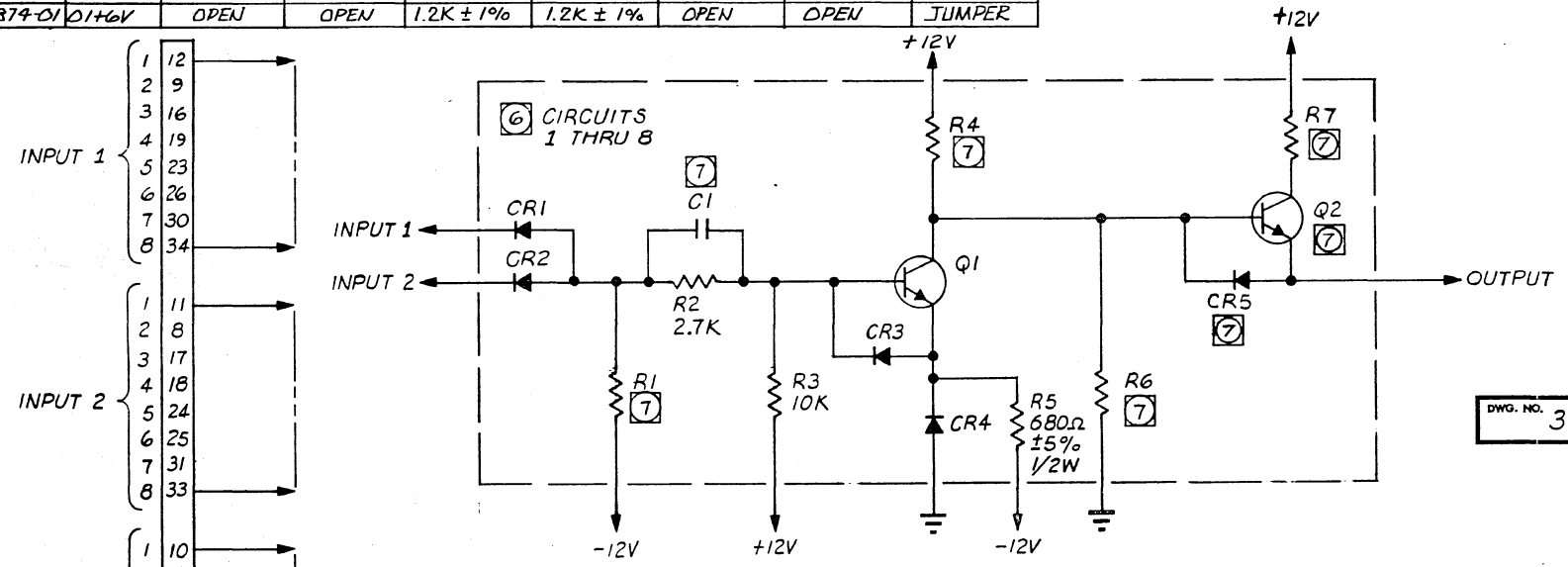
TITLE CIRCUIT BOARD ASSY-OUTPUT DRIVER-L

SIZE	CODE IDENT. NO.	DWG. NO.
D	09150	3118183
SCALE 2:1		SHEET 1 OF 1

TABLE I

ASSY NO.	OUTPUT LEVEL	COMPONENTS						
		C1	R1	R4	R6	R7	Q2	CR5
3118161-01	0/+3V	OPEN	OPEN	619K, ±1%	2.74K ± 1%	125 ± 3% 3W	3201104-10	3263024-10
3118162-01	0/+6V	OPEN	OPEN	2.21K, ±1%	2.74K, ±1%	125 ± 3% 3W	3201104-10	3263024-10
3118163-01	0/+9V	OPEN	OPEN	1.82K, ± 1%	7.5K, ± 1%	125 ± 3% 3W	3201104-10	3263024-10
3118164-01	0/+12V	OPEN	OPEN	2K	OPEN	125 ± 3% 3W	3201104-10	3263024-10
3118293-01	0/+4V	OPEN	OPEN	4.22K, ±1%	2.74K, ±1%	125 ± 3% 3W	3201104-10	3263024-10
3119497-01	0/+8V	OPEN	OPEN	3.01K, ±1%	7.5K, ± 1%	125 ± 3% 3W	3201104-10	3263024-10
3119589-01	0/+5V	OPEN	OPEN	2.74K ± 1%	2K ± 1%	125 ± 3% 3W	3201104-10	3263024-10
3123874-01	0/+6V	OPEN	OPEN	1.2K ± 1%	1.2K ± 1%	OPEN	OPEN	JUMPER

REVISIONS					
ISSUE	DESCRIPTION	DATE	DRAFTSMAN	DATE	APPROVAL
B	ECN 5942 PROD REL	8/28/66	Jujimoto	9/30/66	Hough
C	ECN 7200	12/16/66	REISS	11/20/67	Hough
D	ECN 5553	8-17-67	H BROOD	9/18/67	W Burk
E	ECN 7884	9-18-67	Jms	9/22/67	Hough
F	ECN 8642	12/21/67	H Brood	1/4/67	Wilson



DWG. NO. 3118166

8. FOR REF ASSY SEE 3118165
7. SEE TABLE 1.
6. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. PREFIX THE REFERENCE DESIGNATION WITH THE CIRCUIT NUMBER FOR COMPLETE DESIGNATION.
5. ALL TRANSISTORS TO BE 3201104-10.
4. ALL DIODES TO BE 3263028-10.
3. ALL RESISTOR VALUES ARE IN OHMS, ±5%, 1/4W.
2. ALL CAPACITOR VALUES ARE IN MICROFARADS.
1. FOR ASSEMBLY SEE TABLE 1.

NOTES:

DO NOT SCALE DRAWING
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
DECIMALS TOLERANCES ANGLES
.XX± —— .XXX± —— ± ——
BREAK ALL SHARP EDGES APPROX. .010. C'BORE AND SPOTFACE CORNER RADII APPROX. .010.
ROUGHNESS OF ALL MACHINED SURFACES —— PER MIL-STD-10 ✓
MATERIAL
FINISH

SEE TABLE	DE-200
NEXT ASSY.	1ST USED ON
APPLICATION	

THE INFORMATION HEREON IS THE PROPERTY OF AMPEX COMPUTER PRODUCTS DIVISION. NO REPRODUCTION OR UNAUTHORIZED USE IN PART OR IN WHOLE SHALL BE MADE WITHOUT WRITTEN CONSENT OF AMPEX COMPUTER PRODUCTS DIV.

PROJ		7/20/66
SUPER		
PROJ ENGR		8/29/66
ENGR		8/30/66
CHKR		9/9/66
DFTSMN		6/15/66

AMPEX COMPUTER PRODUCTS DIVISION
P.O. BOX 329, CULVER CITY, CALIF.

TITLE: SCHEMATIC — OUTPUT DRIVER — M (INV. POSITIVE OUTPUT)

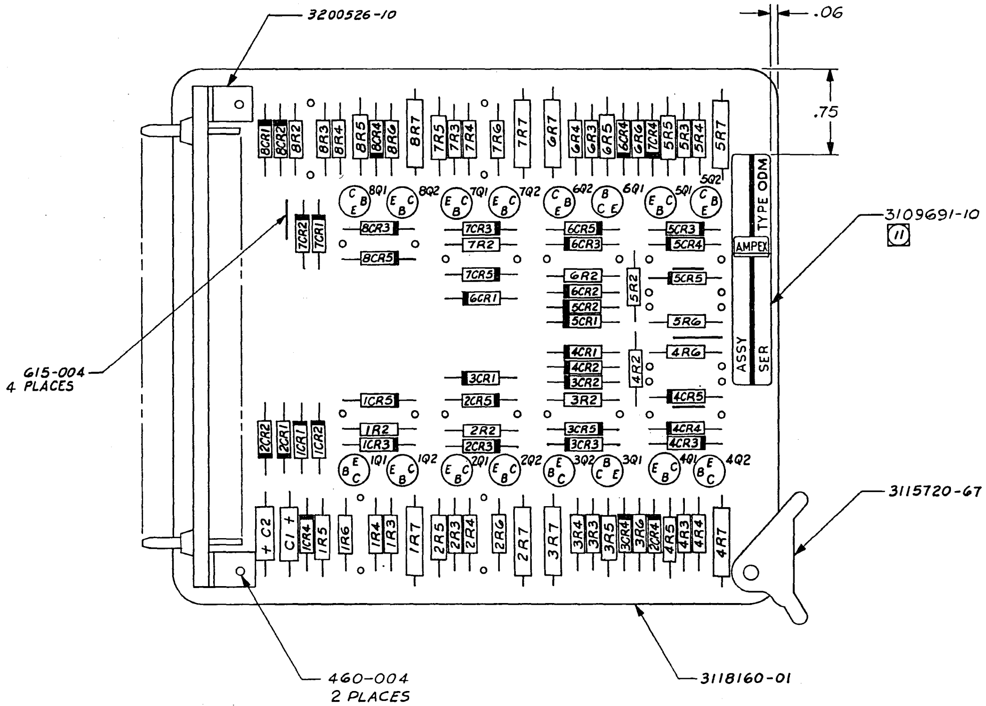
SIZE	CODE IDENT. NO.	DWG. NO.
C	09150	3118166

SCALE NONE SHEET 1 OF 1

REVISIONS					
ISSUE	DESCRIPTION	DATE	DRAFTSMAN	DATE	APPROVAL
B	ECN 5942 PROD REL	8/26/66	[illegible]	8/x/66	[illegible]
C	ECN 7200	12/15/66	REISS	[illegible]	[illegible]
D	ECN 5553	8-17-67	H Bravo	8/18/67	[illegible]
E	ECN 7884	[illegible]	[illegible]	[illegible]	[illegible]

TABLE I

ASSEMBLY NO.	OUTPUT LEVEL	COMPONENTS						
		PART A	PART B	PART C	PART D	PART E	PART F	PART G
3118161-01	0/+3V	NOT USED	NOT USED	042-881	048-186	047-302	3201104-10	3263024-10
3118162-01	0/+6V	↕	↕	042-423	048-186	047-302	3201104-10	3263024-10
3118163-01	0/+9V			042-460	042-430	047-302	3201104-10	3263024-10
3118164-01	0/+12V	NOT USED	NOT USED	041-560	NOT USED	047-302	3201104-10	3263024-10
3118293-01	0/+4V	NOT USED	NOT USED	042-873	048-186	047-302	3201104-10	3263024-10
3119497-01	0/+8V	NOT USED	NOT USED	042-866	042-430	047-302	3201104-10	3263024-10
3119589-01	0/+5V	NOT USED	NOT USED	042-426	048-052	047-302	3201104-10	3263024-10
3123874-01	0/+6V	NOT USED	NOT USED	042-517	042-517	OPEN	OPEN	JUMPER



	PART NO.	REFERENCE DESIGNATION
	3201104-10	1Q1 THRU 8Q1,
12	PART G	1CR5 THRU 8CR5
	3263028-10	1CR1 THRU 8CR1, 1CR2 THRU 8CR2 1CR3 THRU 8CR3, 1CR4 THRU 8CR4
	037-068	C1, C2
	041-408	1R3 THRU 8R3
	041-442	1R2 THRU 8R2
12	PART C	1R4 THRU 8R4
12	PART D	1R6 THRU 8R6
	041-343	1R5 THRU 8R5
12	PART E	1R7 THRU 8R7
12	PART A	1C1 THRU 8C1
12	PART B	1R1 THRU 8R1
12	PART F	1Q2 THRU 8Q2

12 INSTALL PARTS 'A THRU G' PER TABLE I.

11 MARK PART NO. AND NAMEPLATE INFORMATION PER MIL-STD-130.

10. PART NO. TO BE AS SHOWN ON TABLE I.

9. SEAL PRINTED CIRCUIT SIDE ONLY WITH HUMISEAL TYPE 1B15 COLUMBIA TECH. CORP. OR EQUIV.

~~8. MARK POT. REF. NO's. .12 HIGH CHARACTERS. COLOR WHITE, PER MIL-STD-130. DO NOT IMPRESSION STAMP.~~

~~7. TRIMPOTS NOT TO BE SUBMERGED IN WATER.~~

6. COMPONENT DESIGNATIONS ARE FOR REF. ONLY.

5. PLUS SIGN ON CAPACITOR INDICATES POSITIVE.

4. HEAVY LINE ON DIODES INDICATES CATHODE.

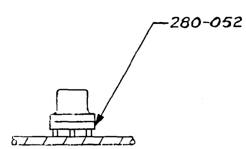
3. ASSEMBLE PER PRODUCTION PRACTICES MANUAL.

2. FOR PERF SPECIFICATION SEE 3118167

1. FOR SCHEMATIC SEE 3118166.

NOTES:

REFERENCE



TYPICAL TRANSISTOR INSTALLATION

SEE TABLE	DE-200
NEXT ASSY.	1ST USED ON
APPLICATION	

DO NOT SCALE DRAWING

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

DECIMALS TOLERANCES ANGLES

.XX ± .05 .XXX ± .010 ± 1/2°

BREAK ALL SHARP EDGES APPROX. .010. C'BORE AND SPOTFACE CORNER RADII APPROX. .010. ROUGHNESS OF ALL MACHINED SURFACES ——— PER MIL-STD-10 ✓

MATERIAL

FINISH

DWG. NO. 3118165

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PROJ SUPER	[illegible]	3/2/66
PROJ ENGR	[illegible]	[illegible]
ENGR	[illegible]	[illegible]
CHKR	[illegible]	[illegible]
DFTSMN	[illegible]	5/26/66

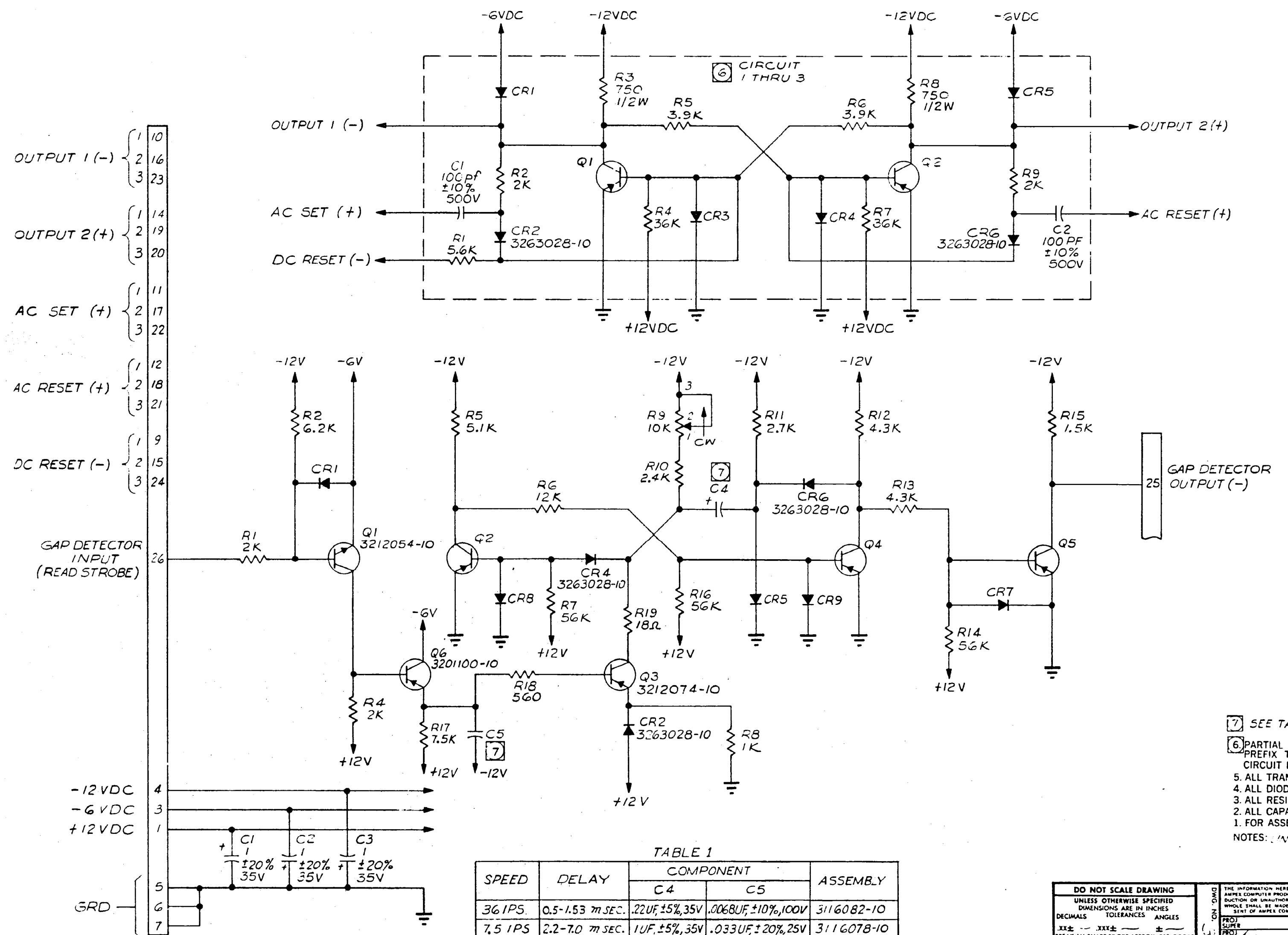
AMPEX COMPUTER PRODUCTS DIVISION P.O. BOX 329, CULVER CITY, CALIF.

TITLE CIRCUIT BOARD ASSY— OUTPUT DRIVER -M (INV. POSITIVE OUTPUT)

SIZE	CODE IDENT. NO.	DWG. NO.
D	09150	3118165

SCALE 2:1 SHEET 1 OF 1

REVISIONS					
ISSUE	DESCRIPTION	DATE	DRAFTSMAN	DATE	APPROVAL
A	ERN 106-CH PROD	7/65			
B	ECN 4B14	12/28/65			



-6VDC
-12VDC
6 CIRCUIT 1 THRU 3
CR1
R3 750 1/2W
R5 3.9K
R6 3.9K
R8 750 1/2W
CR5
OUTPUT 1 (-)
OUTPUT 2 (+)
C1 100pf ±10% 500V
R2 2K
Q1
Q2
R9 2K
AC SET (+)
R4 36K
CR3
CR4
R7 36K
AC RESET (+)
R1 5.6K
CR2 3263028-10
CR6 3263028-10
C2 100 PF ±10% 500V
DC RESET (-)
+12VDC
OUTPUT 1 (-)
OUTPUT 2 (+)
AC SET (+)
AC RESET (+)
DC RESET (-)
GAP DETECTOR INPUT (READ STROBE)
-12V
-6V
R2 6.2K
CR1
R1 2K
Q1 3212054-10
R5 5.1K
R6 12K
Q2
CR8
CR4 3263028-10
R7 56K
+12V
R9 10K
CW
R10 2.4K
7
C4
R19 18Ω
R16 56K
R11 2.7K
CR6 3263028-10
CR5
CR9
R12 4.3K
R13 4.3K
Q4
R15 1.5K
Q5
CR7
R14 56K
GAP DETECTOR OUTPUT (-)
Q6 3201100-10
R4 2K
R17 7.5K
R18 560
C5
Q3 3212074-10
CR2 3263028-10
R8 1K
-12VDC
-6VDC
+12VDC
C1 1 ±20% 35V
C2 1 ±20% 35V
C3 1 ±20% 35V
GRD

REFERENCE DESIGNATIONS	
LAST USED	DELETED
C5	
1C2 THRU 3C2	
CR9	CR3
1CR6 THRU 3CR6	
Q6	
1Q2 THRU 3Q2	
R19	R3
1R9 THRU 3R9	

7 SEE TABLE 1.

6 PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. PREFIX THE REFERENCE DESIGNATION WITH THE CIRCUIT NUMBER FOR COMPLETE DESIGNATION.

5. ALL TRANSISTORS TO BE 3212092-10.
4. ALL DIODES TO BE 3263024-10.
3. ALL RESISTOR VALUES ARE IN OHMS 1/4W, ±5%.
2. ALL CAPACITOR VALUES ARE IN MICROFARADS.
1. FOR ASSEMBLY SEE TABLE.

NOTES: UNLESS OTHERWISE SPECIFIED.

TABLE 1

SPEED	DELAY	COMPONENT		ASSEMBLY
		C4	C5	
36 IPS.	0.5-1.53 m SEC.	.22UF, ±5%, 35V	.0068UF, ±10%, 100V	3116082-10
7.5 IPS	2.2-7.0 m SEC.	1UF, ±5%, 35V	.033UF, ±20%, 25V	3116078-10
75 IPS	0.35-0.85 mSEC	0.1UF, ±5%, 35V	0.01UF, ±10%, 100V	3116161-10
112/150 IPS	0.18-0.55 m SEC	.068UF, ±5%, 50V	.0068UF, ±10%, 100V	3116162-10

NEXT ASSY.	1ST USED ON
3116078	TM-9212
3116082	TM-7211(1D)

APPLICATION

DO NOT SCALE DRAWING

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

DECIMALS TOLERANCES ANGLES .XX± — .XXX± — ± —

BREAK ALL SHARP EDGES APPROX .010. C'BORE AND SPOTFACE CORNER RADII APPROX .010. ROUGHNESS OF ALL MACHINED SURFACES — PER MIL-STD-10 ✓

MATERIAL

FINISH

DWG. NO. 3116083

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PROJ SUPER
PROJ ENGR
ENGR
CHKR
DFTSMN

AMPEX COMPUTER PRODUCTS DIVISION P.O. BOX 329, CULVER CITY, CALIF.

TITLE SCHEMATIC—LONGITUDINAL PARITY REGISTER-B

SIZE	CODE IDENT. NO.	DWG. NO.
D	09150	3116083

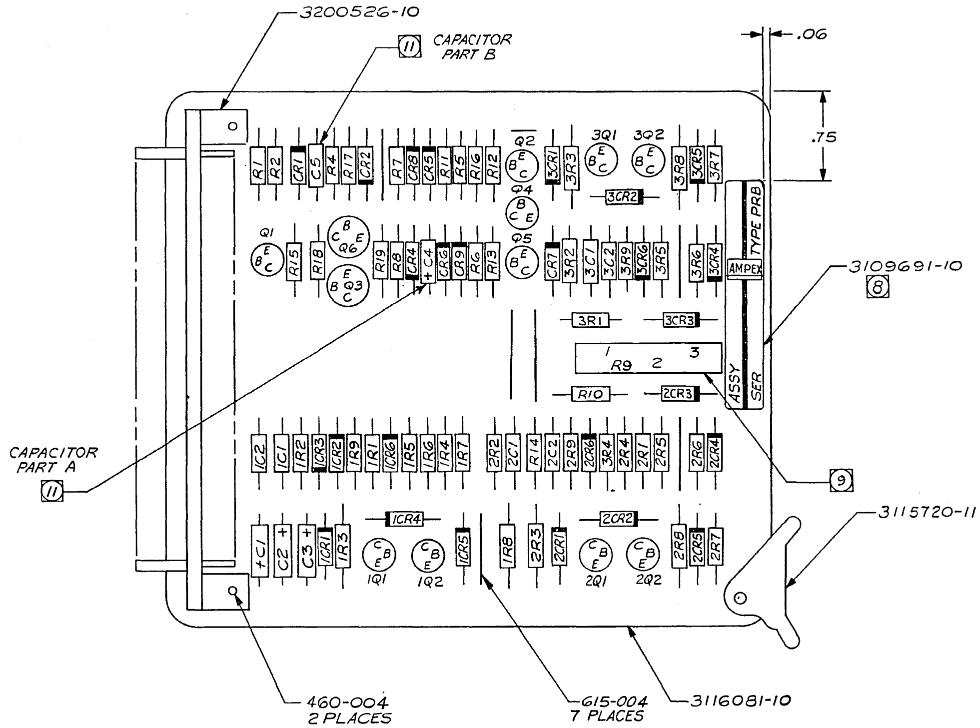
SCALE —

SHEET 1 OF 1

REVISIONS				
ISSUE	DESCRIPTION	DRAFTSMAN	DATE	APPROVAL
A	ECN 4814 PROD REL	Aramaki	11/16/65	[illegible]

TABLE I

B/M REFERENCE TABLE				
ASSY NO.	SPEED	DELAY	PART A	PART B
3116082-10	36 IPS	0.5-1.53 mSEC.	037-454	030-195
3116078-10	7.5 IPS	2.2-7.0 mSEC.	037-455	030-294
3116161-10	75 IPS	.35-.85 mSEC.	037-453	035-219
3116162-10	112/150 IPS	.18-.55 mSEC.	033-100	035-568

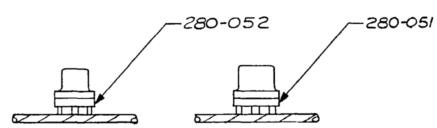


PART NO	REFERENCE DESIGNATIONS
3201100-10	Q6
3212074-10	Q3
3212054-10	Q1
3212092-10	Q2, Q4, Q5, 1Q1, 1Q2, 2Q1, 2Q2, 3Q1, 3Q2
3263024-10	CR1, CR5, CR7, 1CR1, 2CR1, 3CR1, 1CR3, 2CR3, 3CR3, 1CR4, 2CR4, 3CR4, 1CR5, 2CR5, 3CR5, CR8, CR9
3263028-10	CR2, CR4, CR6, 1CR2, 2CR2, 3CR2, 1CR6, 2CR6, 3CR6
PART A	C4
034-417	1C1, 1C2, 2C1, 2C2, 3C1, 3C2
037-058	C1, C2, C3
041-007	1R3, 2R3, 3R3, 1R8, 2R8, 3R8
041-410	R8
041-430	R15
041-442	R11
041-482	R6
041-497	R18
041-507	1R1, 2R1, 3R1
041-511	1R5, 2R5, 3R5, 1R6, 2R6, 3R6
041-519	R7, R14, R16
041-538	R2
041-560	R1, R4, 1R2, 2R2, 3R2, 1R9, 2R9, 3R9
041-561	R5
041-570	R10
041-584	R12, R13
041-751	1R4, 2R4, 3R4, 1R7, 2R7, 3R7
044-197	R9
041-520	R17
041-547	R19
PART B	C5

3116100

(11) INSTALL PT. 'A' & 'B' PER TABLE 1.
10. SEAL PRINTED CIRCUIT SIDE ONLY WITH HUMI-SEAL TYPE 1B15, COLUMBIA TECH CORP OR EQUIV.
(9) TRIMPOT NOT TO BE SUBMERGED IN WATER.
(8) MARK PART NO. AND NAMEPLATE INFORMATION PER MIL-STD-130.
7. PART NO. TO BE AS SHOWN ON B/M.
6. COMPONENT DESIGNATIONS ARE FOR REF. ONLY.
5. PLUS SIGN ON CAPACITOR INDICATES POSITIVE.
4. HEAVY LINE ON DIODES INDICATES CATHODE.
3. ASSEMBLE PER PRODUCTION PRACTICES MANUAL.
2. FOR ASSEMBLY SPECIFICATION SEE 3116084.
1. FOR SCHEMATIC SEE 3116083.
NOTES: UNLESS OTHERWISE SPECIFIED.

REFERENCE



TYPICAL TRANSISTOR INSTALLATION

DO NOT SCALE DRAWING

UNLESS OTHERWISE SPECIFIED TOLERANCES
DECIMALS .XX ± .03 .XXX ± .010 ANGLES ± 1/2°
BREAK ALL SHARP EDGES APPROX .010
C'BORE AND SPOTFACE CORNER RADII .015
ROUGHNESS OF ALL MACHINED SURFACES PER MIL-STD-10

MATERIAL

FINISH

SEE TABLE	TM-7211 (1D)
NEXT ASSY.	1ST USED ON
APPLICATION	

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PROJ SUPER
PROJ ENGR [illegible]
ENGR [illegible]
CHKR Aramaki
DFTSMN [illegible] 10-8-65

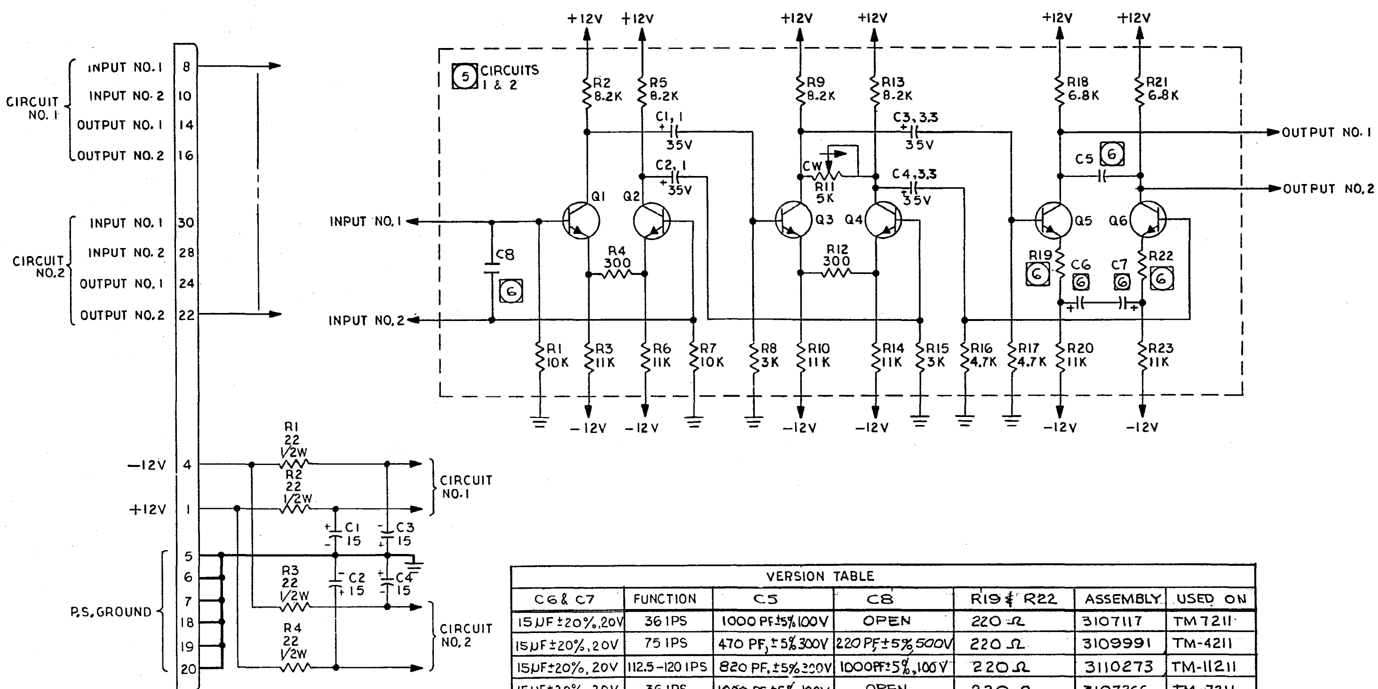
AMPEX COMPUTER PRODUCTS COMPANY
9937 JEFFERSON BLVD. CULVER CITY, CALIFORNIA

TITLE
CIRCUIT BOARD ASSY-
LONGITUDINAL PARITY REGISTER-B

CODE IDENT. NO. | SIZE D | DWG. NO. 3116100 | ISSUE A

SCALE 2:1 | SHEET 1 OF 1

REVISIONS				
ISSUE	DESCRIPTION	DRAFTSMAN	DATE	APPROVAL
A	ECN 911-47 DEV. PRO.(AXCH)	[illegible]	11/21/63	[illegible]
B	ECN 911-AH PROD.	[illegible]	[illegible]	[illegible]
C	ECN 3570	[illegible]	[illegible]	[illegible]
D	ECN 3963	Matzke	1-27-65	[illegible]
E	ECN 4291	[illegible]	5-5-65	[illegible]
F	ECN 4544	Aromaki	9/15/65	[illegible]
G	ECN 4657	Matzke	11/11/65	[illegible]
H	ECN 4984	[illegible]	2/10/66	[illegible]
J	ECN 5016	[illegible]	3/19/66	[illegible]
K	ECN 5086	[illegible]	4/28/66	[illegible]
L	ECN 7003	Aromaki	9/18/66	[illegible]



VERSION TABLE						
C6 & C7	FUNCTION	C5	C8	R19 & R22	ASSEMBLY	USED ON
15µF ±20%, 20V	36 IPS	1000 PF ±5% 100V	OPEN	220 Ω	3107117	TM7211
15µF ±20%, 20V	75 IPS	470 PF, ±5% 300V	220 PF ±5%, 500V	220 Ω	3109991	TM-4211
15µF ±20%, 20V	112.5-120 IPS	820 PF, ±5% 300V	1000PF ±5%, 100V	220 Ω	3110273	TM-11211
15µF ±20%, 20V	36 IPS	1000 PF ±5% 100V	OPEN	220 Ω	3107266	TM-7211
15µF ±20%, 20V	7.5 IPS	.0047 µF ±10% 100V	OPEN	100 Ω	3113334	TM-7211
70µF $^{-15}_{+20}$%, 15V	7.5 IPS	.0047µF ±10%, 100V	OPEN	100 Ω	3116066	TM 7211 INTERSTATE
15µf, ±20%, 20V	150 IPS	OPEN	OPEN	220 Ω	3116187	TM-12211 (AGBL)
15µf, ±20%, 20V	112.5/120/150 IPS	360PF, ±5%, 500V	270PF, ±5%, 500V	220 Ω	3118138	TM11211 MANDRELL

3107118

6 FOR VALUE SEE VERSION TABLE.

5 PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. PREFIX THE DESIGNATING NUMBER WITH THE CIRCUIT NUMBER FOR COMPLETE DESIGNATION.

4. ALL TRANSISTORS TO BE 3212091-10.

3. ALL RESISTOR VALUES ARE IN OHMS, 1/4 W, ± 5%.

2. ALL CAPACITOR VALUES ARE IN MICROFARADS, -20 V ± 20%.

1. FOR ASSEMBLY SEE TABLE.

NOTES: UNLESS OTHERWISE SPECIFIED.

DO NOT SCALE DRAWING

UNLESS OTHERWISE SPECIFIED TOLERANCES
DECIMALS .XX ± .XXX ± ANGLES ±
BREAK ALL SHARP EDGES APPROX. .010
C'BORE AND SPOTFACE CORNER RADII .010
ROUGHNESS OF ALL MACHINED SURFACES PER MIL-STD-10

MATERIAL

FINISH

SEE TABLE

NEXT ASSY. | 1ST USED ON

APPLICATION

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PROJ SUPER [illegible] 3/6/?
PROJ ENGR [illegible]
ENGR [illegible]
CHKR [illegible]
DFTSMN [illegible] 11/6/63

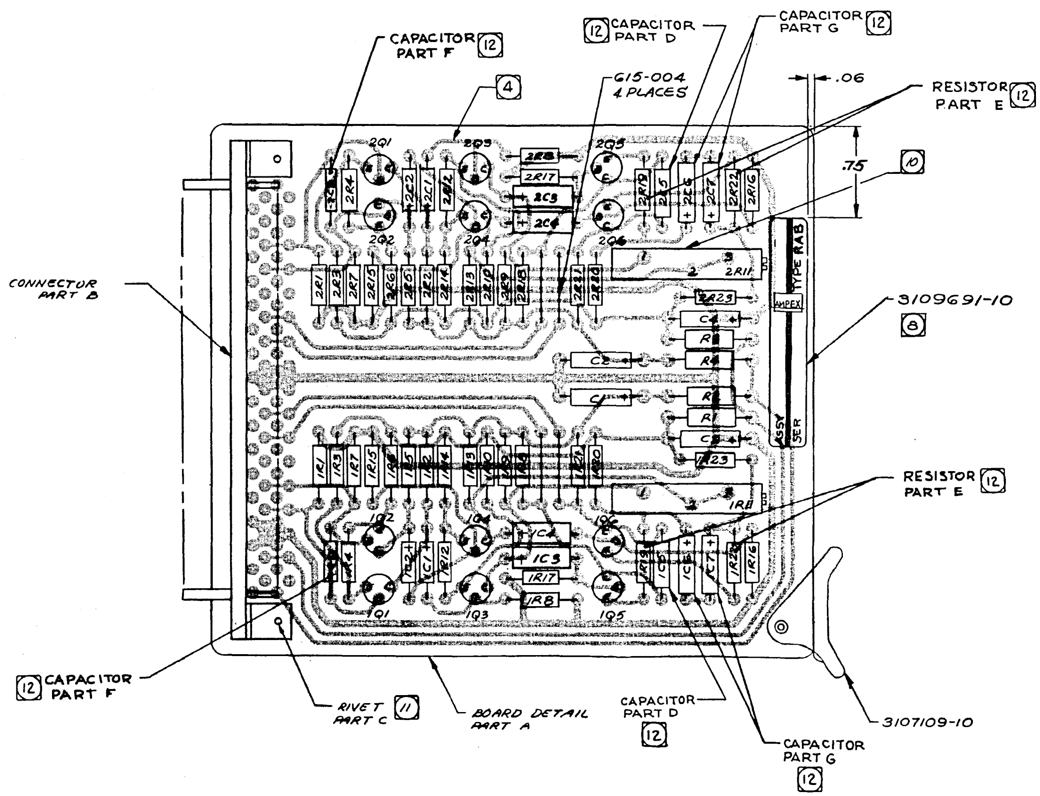
AMPEX COMPUTER PRODUCTS COMPANY
9937 JEFFERSON BLVD. CULVER CITY, CALIFORNIA

TITLE
SCHEMATIC - READ AMPLIFIER UNSHARED

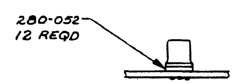
CODE IDENT. NO. | SIZE D | DWG. NO. 3107118 | ISSUE L

SCALE NONE | SHEET 1 OF 1

REVISIONS				
ISSUE	DESCRIPTION	DRAFTSMAN	DATE	APPROVAL
A	ECN 911-47 DEV. PRO(AXCI)	Kuratani	[illegible] 63	Anderson
B	ECN 911-AH PROD.	[illegible]	3-6	[illegible]
C	ECN 3594	[illegible]	[illegible]	[illegible]
D	ECN 3858	Kuratani	11/24/[illegible]	[illegible]
E	ECN 3963	Matzke	1/27/65	[illegible]
–	ECN 4291	[illegible]	5-7-65	Gough
G	ECN 4657	Matzke	11/[illegible]	Gough
H	ECN 4984	[illegible]	2/18/66	Gough
J	ECN 5016	[illegible]	3/19/66	[illegible]
K	ECN 5086	[illegible]	4/28/66	[illegible]



PART NO.	REFERENCE DESIGNATION
3212091-10	1Q1 THRU 1Q6, 2Q1 THRU 2Q6
PART D	1C5, 2C5
037-994	1C1, 1C2, 2C1, 2C2
037-990	C1 THRU C4,
041-408	1R1, 2R1, 1R7, 2R7
041-413	1R18, 2R18, 1R21, 2R21
PART E	1R19, 2R19, 1R22, 2R22
041-550	1R8, 2R8, 1R15, 2R15
041-495	1R2, 2R2, 1R5, 2R5, 1R9, 2R9, 1R13, 2R13
041-421	R1 THRU R4
041-569	1R4, 2R4, 1R12, 2R12
041-748	1R3, 2R3, 1R6, 2R6, 1R10, 2R10, 1R14, 2R14, 1R20, 2R20, 1R23, 2R23
044-366	1R11, 2R11
041-412	1R16, 2R16, 1R17, 2R17
037-176	1C3, 1C4, 2C3, 2C4
PART F	1C8, 2C8
PART G	1C6, 2C6, 1C7, 2C7



TYPICAL TRANSISTOR INSTALLATION

TABLE I

ASSEMBLY	USED ON	PART D	PART E	PART F	PART G
3107117-10	TM 7211	034-950	041-416	NOT USED	037-990
3109991-10	TM 4211	034-214	041-416	034-240	037-990
3110273-10	TM 11211	034-283	041-416	034-950	037-990
3107266-10	TM 7211	034-950	041-416	NOT USED	037-990
3113334-10	TM 7211	035-989	041-419	NOT USED	037-990
3116066-10	TM 7211 INTERSTATE	035-989	041-419	NOT USED	037-478
3116187-10	TM-12211 (AGBL)	NOT USED	041-416	NOT USED	037-990
3118138-[illegible]	TM-11211 MANDRELL	034-934	041-416	034-319	037-990

3107270

10 TRIMPOT NOT TO BE SUBMERGED IN WATER

9 SEAL PRINTED CIRCUIT SIDE ONLY WITH HUMI-SEAL TYPE 1B15, COLUMBIA TECH CORP OR EQUIV

8. MARK PART NO. AND NAMEPLATE INFORMATION PER MIL-STD-130.

7. PART NO. TO BE AS SHOWN IN BILL OF MATERIAL.

6. PLUS SIGN ON CAPACITOR INDICATES POSITIVE.

5. COMPONENT DESIGNATIONS ARE FOR REFERENCE ONLY.

4. CIRCUITRY ON FARSIDE.

3. ASSEMBLE PER MANUFACTURING PRACTICE MANUAL.

2. FOR ASSEMBLY SPECIFICATION SEE 3107119.

1. FOR SCHEMATIC SEE 3107118.

NOTES:

12 INSTALL PARTS D,E,F

11 RIVET, PART C USED ONLY WITH 3200826-10.

REFERENCE

273

SEE TABLE	
NEXT ASSY.	1ST USED ON
APPLICATION	

DO NOT SCALE DRAWING

UNLESS OTHERWISE SPECIFIED TOLERANCES
DECIMALS .XX ± .XXX ± ANGLES ±
BREAK ALL SHARP EDGES APPROX .010
C'BORE AND SPOTFACE CORNER RADII .010
ROUGHNESS OF ALL MACHINED SURFACES PER MIL-STD-10

MATERIAL

FINISH

THE INFORMATION HEREON IS THE PROPERTY OF AMPEX COMPUTER PRODUCTS COMPANY. NO REPRODUCTION OR UNAUTHORIZED USE IN PART OR IN WHOLE SHALL BE MADE WITHOUT WRITTEN CONSENT OF AMPEX COMPUTER PRODUCTS CO.

PROJ SUPER	[signature]	3/6/4
PROJ ENGR	[signature]	3/6/4
ENGR	[signature]	3/6/64
CHKR	C. Anderson	[illegible] 63
DFTSMN	L. Kuratani	11/6/63

AMPEX COMPUTER PRODUCTS COMPANY
9937 JEFFERSON BLVD. CULVER CITY, CALIFORNIA

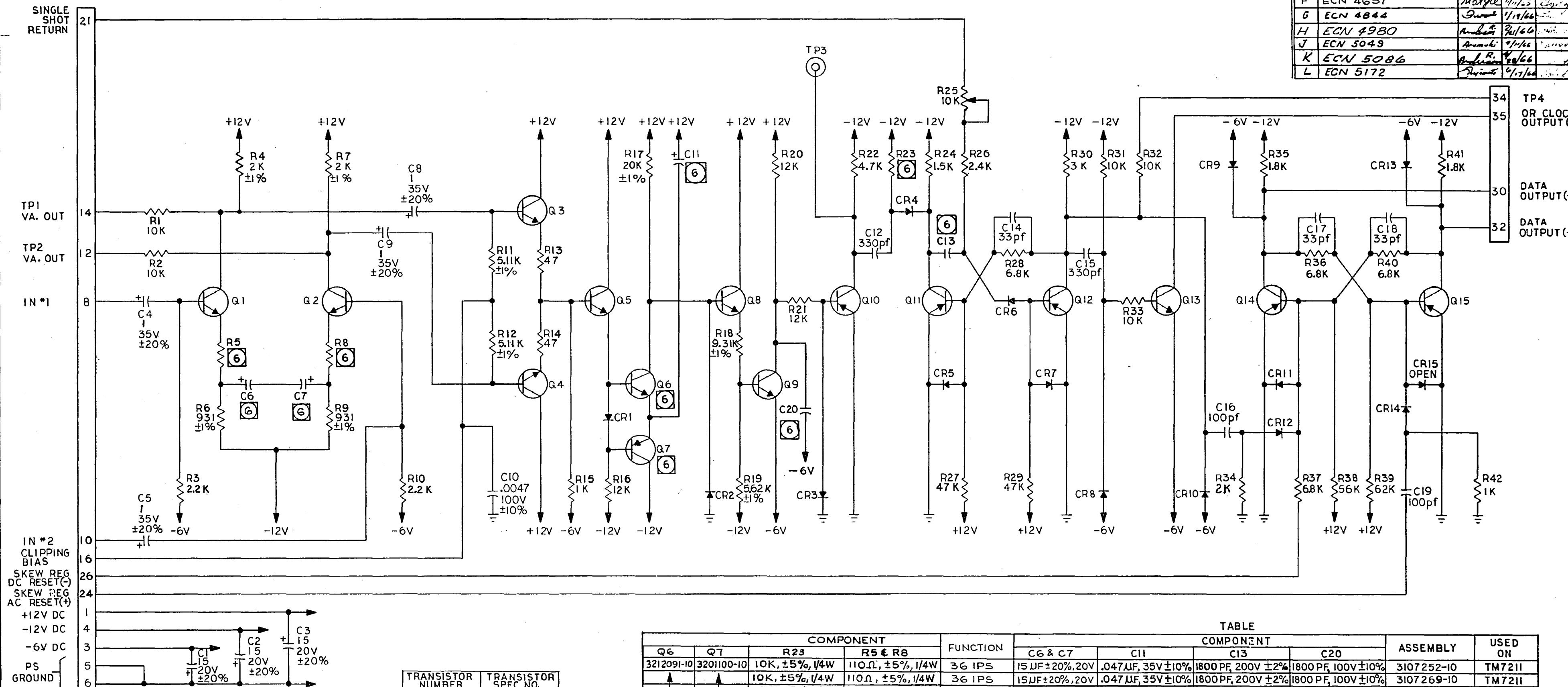
TITLE: CIRCUIT BOARD ASSEMBLY-READ AMPLIFIER UNSHARED

CODE IDENT. NO.	SIZE	DWG. NO.	ISSUE
	D	3107270	K

SCALE 2:1 SHEET 1 OF 1

REVISIONS				
ISSUE	DESCRIPTIONS	DRAFTSMAN	DATE	APPROVAL
M	ECN 5772	[illegible]	7/21/66	[illegible]
N	ECN 7659	[illegible]	3/2/67	Allington
P	ECN 7959	[illegible]	6/26/67	[illegible]
R	ECN 9913	H Bravo	5-24-68	[illegible]

REVISIONS				
ISSUE	DESCRIPTION	DRAFTSMAN	DATE	APPROVAL
A	[illegible] DEV PRO(X-A CH)	Kurstani	[illegible]	[illegible]
B	[illegible]	[illegible]	[illegible]	[illegible]
C	ECN 311-AM PROD.	Matzke	[illegible]	[illegible]
D	[illegible]	[illegible]	5-5-65	[illegible]
E	ECN 4612	Fujisat	10-22-65	[illegible]
F	ECN 4657	Matzke	11/1/65	[illegible]
G	ECN 4844	[illegible]	1/19/66	[illegible]
H	ECN 4980	Anderson R.	2/21/66	[illegible]
J	ECN 5049	Aramaki	4/11/66	[illegible]
K	ECN 5086	Anderson R.	4/28/66	[illegible]
L	ECN 5172	Fujisat	6/17/66	[illegible]



TRANSISTOR NUMBER	TRANSISTOR SPEC NO.
Q1, 2	3212091-10
Q3, 4	3201117-10
Q5	3212098-10
Q8, 9, 13	3201104-10
Q10, 11, 12, 14, 15	3212092-10

TABLE

COMPONENT				FUNCTION	COMPONENT				ASSEMBLY	USED ON
Q6	Q7	R23	R5 & R8		C6 & C7	C11	C13	C20		
3212091-10	3201100-10	10K, ±5%, 1/4W	110Ω, ±5%, 1/4W	36 IPS	15 µF ±20%, 20V	.047 µF, 35V ±10%	1800 PF, 200V ±2%	1800 PF, 100V ±10%	3107252-10	TM7211
↕	↕	10K, ±5%, 1/4W	110Ω, ±5%, 1/4W	36 IPS	15 µF ±20%, 20V	.047 µF, 35V ±10%	1800 PF, 200V ±2%	1800 PF, 100V ±10%	3107269-10	TM7211
		2K, ±5%, 1/4W	220Ω, ±5%, 1/4W	75 IPS	15 µF ±20%, 20V	.022 µF, 35V ±20%	910 PF, 100V ±2%	270 PF, ±5%, 500V	3109475-10	TM4211
		2K, ±5%, 1/4W	220Ω, ±5%, 1/4W	112.5-150 IPS	15 µF ±20%, 20V	.015 µF, 35V ±10%	560 PF, 300V ±2%	270 PF, ±5%, 500V	3110004-10	TM11211
3212091-10	3201100-10	10K, ±5%, 1/4W	110Ω, ±5%, 1/4W	7.5 IPS	15 µF ±20%, 20V	.47 µF, 35V ±20%	1800 PF, 200V ±2%	.0047 PF 100V ±10%	3113333-10	TM7211
3212081-10	014-364	10K, ±5%, 1/4W	110Ω, ±5%, 1/4W	7.5 IPS	70 µF +75/-20 %, 15V	.22 µF, 35V, ±10%	.01 UF, 100V ±10%	.0047 PF, 100V ±10%	3116055-10	TM 7211 INTERSTATE
3212091-10	3201100-10	2K, ±5%, 1/4W	220Ω, ±5%, 1/4W	120 IPS	15 µF, ±20%, 20V	.015 µF, 35V, ±10%	910 PF, 100V, ±2%	270 PF, ±5%, 500V	3118153-01	TM-11241
3212091-10	3201100-10	2K, ±5%, 1/4W	110Ω ±5%, 1/4W	45 IPS	15 µF, ±20%, 20V	.022 µF, 35V, ±20%	910 PF, 100V ±2%	270 PF, ±5%, 500V	3123847-01	TM7211

6 SEE TABLE.
5. CR3 THRU CR14 TO BE 3263024-10.
4. CR1 AND CR2 TO BE CD458
3. ALL RESISTOR VALUES ARE IN OHMS, 1/4W, ±5%.
2. ALL CAPACITOR VALUES ARE IN MICROFARADS, ±10%, 500V.
1. FOR ASSEMBLY SEE TABLE.

NOTES: UNLESS OTHERWISE SPECIFIED

DO NOT SCALE DRAWING

UNLESS OTHERWISE SPECIFIED TOLERANCES
DECIMALS .XX ± .XXX ± ANGLES ±
BREAK ALL SHARP EDGES APPROX. .010
C'BORE AND SPOTFACE CORNER RADII .010
ROUGHNESS OF ALL MACHINED SURFACES PER MIL-STD-10

MATERIAL

FINISH

THE INFORMATION HEREON IS THE PROPERTY OF AMPEX COMPUTER PRODUCTS COMPANY. NO REPRODUCTION OR UNAUTHORIZED USE IN PART OR IN WHOLE SHALL BE MADE WITHOUT WRITTEN CONSENT OF AMPEX COMPUTER PRODUCTS CO.

PROJ / SUPER / PROJ ENGR / ENGR

CHKR [illegible] 12-11-?

DFTSMN L. Kurstani 9/4/63?

SEE TABLE

NEXT ASSY. | 1ST USED ON

APPLICATION

AMPEX — AMPEX COMPUTER PRODUCTS COMPANY
5337 JEFFERSON BLVD. CULVER CITY, CALIFORNIA

TITLE

SCHEMATIC — READ DESKEW, UNSHARED

CODE IDENT. NO. | SIZE D | DWG. NO. 3107253 | ISSUE R

SCALE NONE | SHEET 1 OF 1

DIETERICH-POST CLEARPRINT 1000H-4 FORM 2608-387 REV. 11-62

TABLE I

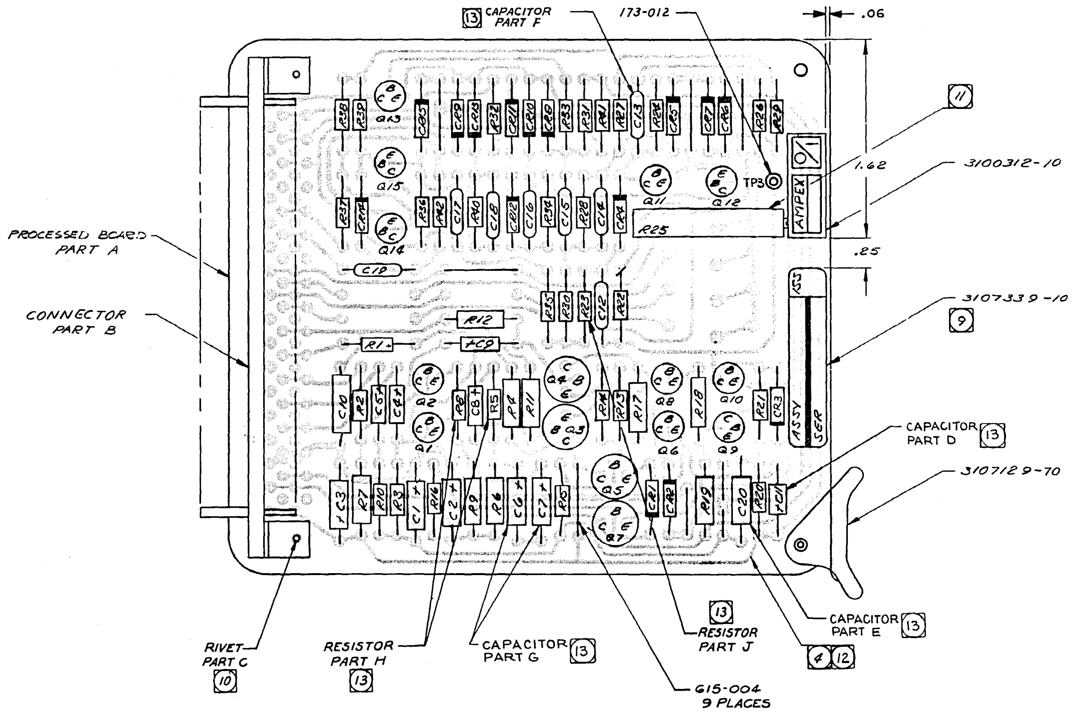
PART K	PART L	ASSEMBLY	FUNCTION	PART D	PART E	PART F	PART G	PART H	PART J
3212091-10	3201100-10	3107252-10	36 IPS	037-273	035-510	033-147	037-990	041-736	041-408
↕	↕	3107269-10	36 IPS	037-273	035-510	033-147	037-990	041-736	041-408
		3109475-10	75 IPS	037-034	034-319	034-278	037-990	041-396	041-560
		3110004-10	112.5-150 IPS	037-344	034-319	034-350	037-990	041-396	041-560
3212091-10	3201100-10	3113333-10	7.5 IPS	037-043	035-989	033-147	037-990	041-736	041-408
3212081-10	014-364	3116055-10	7.5 IPS	037-217	035-989	035-219	037-478	041-736	041-408
3212091-10	3201100-10	3118153-01	120 IPS	037-344	034-319	034-278	037-990	041-396	041-560
3212091-10	3201100-10	3123847-01	45 IPS	037-034	034-319	034-278	037-990	041-736	041-560

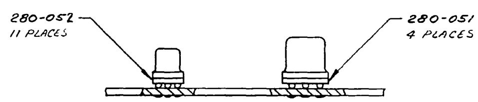
REVISIONS

ISSUE	DESCRIPTION	DRAFTSMAN	DATE	APPROVAL
B	ECN 911-32 REDRAWN	[illegible]	[illegible]	[illegible]
C	ECN 911-AM PROD.	Motzke	3/5/4	[illegible]
D	ECN [illegible]	[illegible]	[illegible]	[illegible]
E	ECN 4612	[illegible]	10-22-65	[illegible]
F	ECN 4657	Motzke	11/1/65	[illegible]
G	ECN 4844	[illegible]	1/20/66	[illegible]
H	ECN 4980	[illegible]	2/21/66	[illegible]
J	ECN 5049	Aramaki	9/11/66	[illegible]
K	ECN 5086	[illegible]	9/30/66	[illegible]
L	ECN 5172	[illegible]	6/17/66	[illegible]
M	ECN 5772	Aramaki	7/27/66	[illegible]
N	ECN 7320	Aramaki	1/22/67	[illegible]
P	ECN 7659	[illegible]	5/2/67	Addington
R	ECN 7959	[illegible]	6/26/67	Addington

PART NO.	REFERENCE DESIGNATIONS
PART J	R23
PART K	Q6
041-753	R39
NOT USED	CR15

PART NO.	REFERENCE DESIGNATIONS
041-414	R3,10
PART L	Q7
3201104-10	Q8,9,13
3212091-10	Q1,2
3212092-10	Q10,11,12,14,15
3212098-10	Q5
3201117-10	Q3,4
3263024-10	CR3 THRU CR14
3263028-10	CR1,2
034-417	C16,19
034-491	C14,17,18
034-493	C12,15
PART D	C11
035-989	C10
PART E	C20
PART F	C13
037-990	C1,2,3
041-408	R1,2,31, 32,33
041-410	R15,42
041-411	R29,27
041-412	R22
041-413	R28,34,36,37,40
041-425	R13,14
041-430	R24
041-434	R35,41
041-482	R16,20,21
048-175	R17
041-519	R38
041-550	R30
041-570	R26
037-994	C8,9,4,5
PART H	R5,8
042-429	R19
048-051	R6,9
048-052	R4,7
048-053	R18
042-877	R11,12
044-197	R25
PART G	C6, C7





TYPICAL TRANSISTOR INSTALLATION

REFERENCE

13. INSTALL PARTS D,E,F,G,H,J,K & L PER TABLE I.
12. SEAL PRINTED CIRCUIT SIDE ONLY WITH HUMI-SEAL TYPE 1B15, COLUMBIA TECH. CORP. OR EQUIVALENT.
11. TRIMPOT NOT TO BE SUBMERGED IN WATER.
10. RIVET PART "C" USED ONLY WITH 3200526-10.
9. MARK PART NO. AND NAMEPLATE INFORMATION PER MIL-STD-130.
8. PART NO. TO BE AS SHOWN IN BILL OF MATERIAL.
7. HEAVY LINE ON DIODE INDICATES CATHODE.
6. PLUS SIGN ON CAPACITOR INDICATES POSITIVE.
5. COMPONENT DESIGNATIONS ARE FOR REFERENCE ONLY.
4. CIRCUITRY ON FARSIDE.
3. ASSEMBLE PER MANUFACTURING PRACTICES MANUAL.
2. FOR ASSEMBLY SPECIFICATION SEE 3107254.
1. FOR SCHEMATIC SEE 3107253.

NOTES:

REQD.	PART NO.	DESCRIPTION	REFERENCE	ZONE	ITEM

LIST OF MATERIAL

NEXT ASSY.	1ST USED ON
3118153	TM-11241
3116055	TM 7211
3110004	TM 11211
3107269	TM 7211
3107252	TM7211

APPLICATION

DO NOT SCALE DRAWING

UNLESS OTHERWISE SPECIFIED TOLERANCES
DECIMALS .XX ± .03 .XXX ± .010 ANGLES ± 1/2°
BREAK ALL SHARP EDGES APPROX. .010
C'BORE AND SPOTFACE CORNER RADII .010
ROUGHNESS OF ALL MACHINED SURFACES √ PER MIL-STD-10

MATERIAL

FINISH

FORM 2602-107 REV. 9-61

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PROJ SUPER	[signature]	3/4/64
PROJ ENGR	[signature]	3/4/64
ENGR	[signature]	3/11/64
CHKR	K. BRINKMAN	12/21-63
DFTSMN	L. KURATANI	11/7-63

AMPEX 0/1 AMPEX COMPUTER PRODUCTS COMPANY
9937 JEFFERSON BLVD. CULVER CITY, CALIFORNIA

TITLE CIRCUIT BOARD ASSY-READ DESKEW UNSHARED

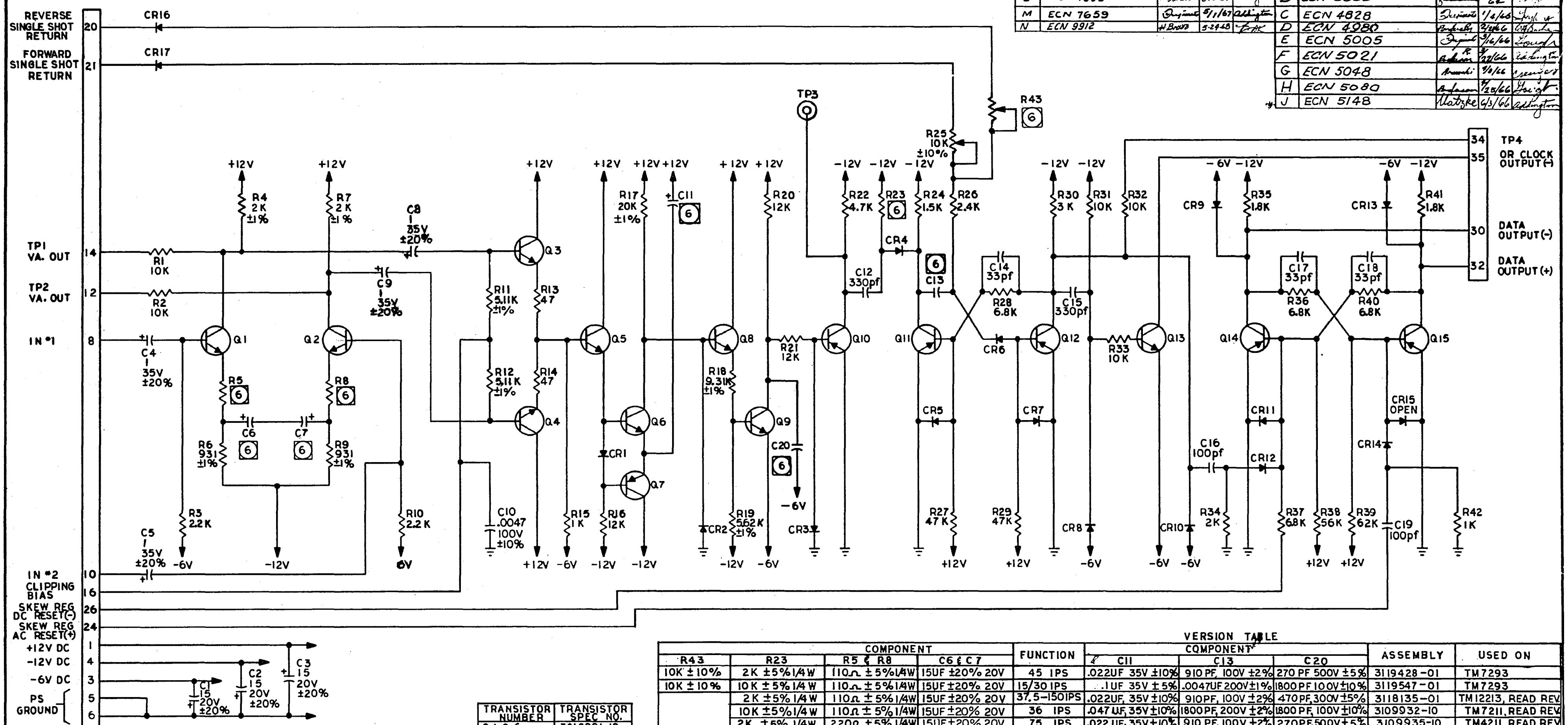
CODE INDENT. NO. | SIZE D | DWG. NO. 3107273 SHEET 1 OF 1 | ISSUE R

SCALE 2:1

RDB

ISS	DESCRIPTION	DFTSM	DATE	APRVL
K	ECN 7121	ER	11-11-66	[illegible]
L	ECN 7392	H. Bravo	2-10-67	[illegible]
M	ECN 7659	[illegible]	5/1/67	[illegible]
N	ECN 9912	H. Bravo	5-24-68	[illegible]

ISSUE	DESCRIPTION	DRAFTSMAN	DATE	APPROVAL
A	ERN [illegible] PROD.	[illegible]	[illegible]	[illegible]
B	ECN 3835	[illegible]	11-10-64	[illegible]
C	ECN 4828	[illegible]	1/4/66	[illegible]
D	ECN 4980	[illegible]	2/2/66	[illegible]
E	ECN 5005	[illegible]	3/16/66	[illegible]
F	ECN 5021	[illegible]	3/22/66	[illegible]
G	ECN 5048	[illegible]	4/1/66	[illegible]
H	ECN 5080	[illegible]	4/28/66	[illegible]
J	ECN 5148	Matzke	6/3/66	[illegible]



VERSION TABLE

COMPONENT R43	COMPONENT R23	COMPONENT R5 & R8	COMPONENT C6 & C7	FUNCTION	COMPONENT C11	COMPONENT C13	COMPONENT C20	ASSEMBLY	USED ON
10K ±10%	2K ±5% 1/4W	110Ω ±5% 1/4W	15UF ±20% 20V	45 IPS	.022UF 35V ±10%	910 PF, 100V ±2%	270 PF 500V ±5%	3119428-01	TM7293
10K ±10%	10K ±5% 1/4W	110Ω ±5% 1/4W	15UF ±20% 20V	15/30 IPS	.1UF 35V ±5%	.0047UF 200V ±1%	1800 PF 100V ±10%	3119547-01	TM7293
10K ±10%	2K ±5% 1/4W	110Ω ±5% 1/4W	15UF ±20% 20V	37.5-150 IPS	.022UF, 35V ±10%	910PF, 100V ±2%	470 PF, 300V ±5%	3118135-01	TM12213, READ REV
	10K ±5% 1/4W	110Ω ±5% 1/4W	15UF ±20% 20V	36 IPS	.047 UF, 35V ±10%	1800PF, 200V ±2%	1800 PF, 100V ±10%	3109932-10	TM7211, READ REV
	2K ±5% 1/4W	220Ω ±5% 1/4W	15UF ±20% 20V	75 IPS	.022 UF, 35V ±10%	910 PF, 100V ±2%	270PF, 500V ±5%	3109935-10	TM4211, READ REV
	2K ±5% 1/4W	220Ω ±5% 1/4W	15UF ±20% 20V	112.5-150 IPS	.015 UF, 35V ±10%	560 PF, 300V ±2%	270 PF, 500V ±5%	3109936-10	TM11211, READ REV
	10K ±5% 1/4W	110Ω ±5% 1/4W	70UF $^{-15\%}_{+20\%}$ 15V	10-100 IPS	.47UF, 35V ±10%	.01UF, 100V ±10%	.0047UF, 100V ±10%	3116107-10	TM7293 READ REV
	10K ±5% 1/4W	110Ω ±5% 1/4W	15 UF ±20% 20V	30 IPS/1 INCH	.047 µF, 35V., ±10%	.0047 µF, 200V., ±1%	1800 PF, 100V., ±10%	3118154-01	TM9241 READ REV.
20K ±10%	10K ±5% 1/4W	110Ω ±5% 1/4W	15 µF ±20%, 20V	10/20 IPS	.1 µF, 35V, ±5%	.0047 µF, 200V ±1%	3300PF, 100V ±5%	3118198-01	TM7293

TRANSISTOR NUMBER	TRANSISTOR SPEC NO.
Q1,2,6	3212091-10
Q3,4	3201117-10
Q5	3212098-10
Q7	3201100-10
Q8,9,13	3201104-10
Q10,11,12,14,15	3212092-10

6. SEE VERSION TABLE.
5. CR3 THRU CR14, CR16 & CR17 TO BE 3263024-10.
4. CR1 AND CR2 TO BE CD458
3. ALL RESISTOR VALUES ARE IN OHMS, 1/4W, ±5%.
2. ALL CAPACITOR VALUES ARE IN MICROFARADS, ±10%, 500V.
1. FOR ASSEMBLY SEE VERSION TABLE.

NOTES: UNLESS OTHERWISE SPECIFIED

DO NOT SCALE DRAWING

UNLESS OTHERWISE SPECIFIED TOLERANCES
DECIMALS .XX ± .XXX ± ANGLES ±
BREAK ALL SHARP EDGES APPROX .010
C'BORE AND SPOTFACE CORNER RADII .010
ROUGHNESS OF ALL MACHINED SURFACES PER MIL-STD-10

MATERIAL

FINISH

NEXT ASSY.	1ST USED ON
APPLICATION	

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PROJ SUPER / PROJ ENGR / ENGR / CHKR / DFTSMN

AMPEX — AMPEX COMPUTER PRODUCTS COMPANY
9937 JEFFERSON BLVD. CULVER CITY, CALIFORNIA

TITLE
SCHEMATIC - READ DESKEW, BI-DIRECTION

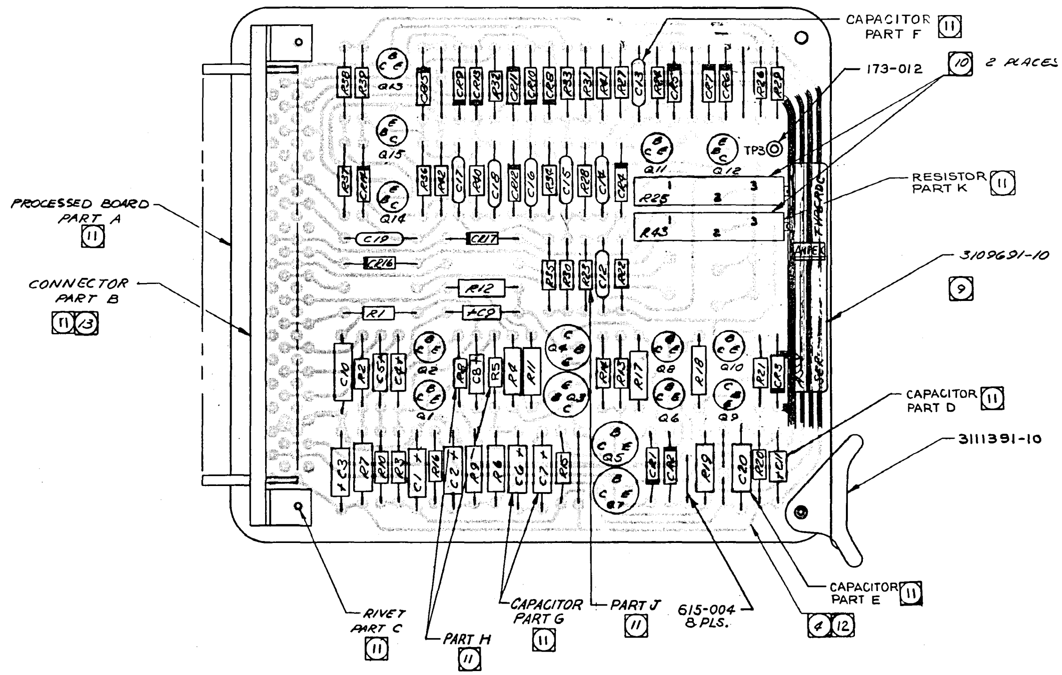
CODE IDENT. NO.	SIZE	DWG. NO.	ISSUE
	D	3109930	N

SCALE NONE — SHEET 1 OF 1

TABLE I

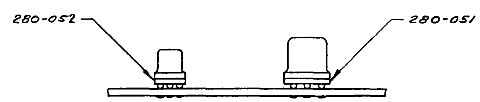
BIM REFERENCE TABLE											
ASSEMBLY	FUNCTION	PART A	PART B	PART C	PART D	PART E	PART F	PART G	PART H	PART J	PART K
3119547-01	15/30 IPS	3107046-20	3200526-10	460-004	037-453	035-510	055-128	037-990	041-736	041-408	044-197
3109932-10	36 IPS	3107046-20	3200526-10	460-004	037-273	035-510	033-147	037-990	041-736	041-408	044-197
3109935-10	75 IPS	3107046-20	3200526-10	460-004	035-839	034-319	034-278	037-990	041-396	041-560	044-197
3109936-10	112.5-150 IPS	3107046-20	3200526-10	460-004	037-344	034-319	034-350	037-990	041-396	041-560	044-197
3116107-10	10-100 IPS	3107046-20	3200526-10	460-004	037-097	035-989	035-219	037-478	041-736	041-408	044-197
3118135-01	37.5-150 IPS	3107046-20	3200526-10	460-004	035-839	034-214	034-278	037-990	041-736	041-560	044-197
3118154-01	30 IPS / 1 INCH	3107046-20	3200526-10	460-004	037-273	035-510	055-128	037-990	041-736	041-408	044-197
3118198-01	10/20 IPS	3107046-20	3200526-10	460-004	037-453	035-422	055-128	037-990	041-736	041-408	044-313
3119428-01	45 IPS	3107046-20	3200526-10	460-004	035-839	034-319	034-278	037-990	041-736	041-560	044-197

REVISIONS				
ISSUE	DESCRIPTION	DRAFTSMAN	DATE	APPROVAL
A	ERN 110-A PROD.	[illegible]	4-30-64	[illegible]
B	ECN 4392	[illegible]	6-21-64	[illegible]
C	ECN 3755	Matzke	7-12-63	[illegible]
D	ECN 4828	[illegible]	1/4/66	[illegible]
E.	ECN 4980	R. [illegible]	2/21/66	[illegible]
F	ECN 5005	[illegible]	3/16/66	[illegible]
G	ECN 5021	ANDERSON	3/22/66	Addington
H	ECN 5048	Aramaki	4/8/66	[illegible]
J	ECN 5080	[illegible]	4/25/66	[illegible]
K	ECN 5148	Matzke	6/3/66	Addington
·L	ECN 7121	REISS	11-18-66	Addington
M	ECN 7320	Aramaki	1/23/67	Addington
N.	ECN 7392	H. Bravo	2-13-67	Addington
P	ECN 7659	[illegible]	3/1/67	Addington
R	ECN 9912	H. Bravo	5-24-68	[illegible]



PART NO.	REFERENCE DESIGNATION
3201100-10	Q7
3201104-10	Q8, 9, 13
3212091-10	Q1, 2, 6
3212092-10	Q10, 11, 12, 14, 15
3212098-10	Q5
3201117-10	Q3, Q4
3263024-10	CR3 THRU CR14, CR16, CR17
013-599	CR1, CR2
034-417	C16, C19
034-491	C14, C17, C18
034-493	C12, C15
PART D	C11
041-414	R3, R10
PART K	R43
041-753	R39
NOT USED	CR15
041-560	R34

PART NO.	REFERENCE DESIGNATION
035-989	C10
PART F	C13
PART E	C20
037-990	C1, 2, 3
041-408	R1, 2, , 31, 32, 33
041-410	R15, 42
041-411	R29, 27
041-412	R22
041-413	R28, 36, 37, 40
041-425	R13, 14
041-430	R24
041-434	R35, 41
041-482	R16, 20, 21
048-175	R17
041-519	R38
041-550	R30
041-570	R26
037-994	C8, 9, 4, 5
PART H	R5, 8
042-429	R19
048-051	R6, 9
048-052	R4, 7
048-053	R18
042-877	R11, 12
044-197	R25
PART G	C6, C7
PART J	R23



TYPICAL TRANSISTOR INSTALLATION

REFERENCE

13 TP1 @ CONNECTOR PIN 14. TP2 @ PIN 12.

12 SEAL PRINTED CIRCUIT SIDE ONLY WITH HUMI-SEAL TYPE 1B15, COLUMBIA TECH. CORP. OR EQUIVALENT.

11 INSTALL PARTS A THRU K PER TABLE I.

10 TRIMPOT NOT TO BE SUBMERGED IN WATER.

9 MARK PART NO. AND NAMEPLATE INFORMATION PER MIL-STD-130.

8. PART NO. TO BE AS SHOWN ON TABLE

7. HEAVY LINE ON DIODE INDICATES CATHODE.

6. PLUS SIGN ON CAPACITOR INDICATES POSITIVE.

5. COMPONENT DESIGNATIONS ARE FOR REFERENCE ONLY.

4 CIRCUITRY ON FARSIDE.

3. ASSEMBLE PER MANUFACTURING PRACTICES MANUAL.

2. FOR ASSEMBLY SPECIFICATION SEE 3107254.

1. FOR SCHEMATIC SEE 3109930.

NOTES:

REQD.	PART NO.	DESCRIPTION	REFERENCE	ZONE	ITEM

LIST OF MATERIAL

FORM 2602-107 REV. 9-62

NEXT ASSY.	1ST USED ON
3118154	TM-9241
3118135	TM12213
3116107	TM 7293
3109935	TM4211, R-R
3109936	TM4211, R-R
3109932	TM7211, R-R

APPLICATION

DO NOT SCALE DRAWING

UNLESS OTHERWISE SPECIFIED TOLERANCES
DECIMALS .XX ± .03 .XXX ± .010 ANGLES ± 1/2°
BREAK ALL SHARP EDGES APPROX. .010
C'BORE AND SPOTFACE CORNER RADII .010
ROUGHNESS OF ALL MACHINED SURFACES ✓ PER MIL-STD-10

MATERIAL

FINISH

THE INFORMATION HEREON IS THE PROPERTY OF AMPEX COMPUTER PRODUCTS COMPANY. NO REPRODUCTION OR UNAUTHORIZED USE IN PART OR IN WHOLE SHALL BE MADE WITHOUT WRITTEN CONSENT OF AMPEX COMPUTER PRODUCTS CO.

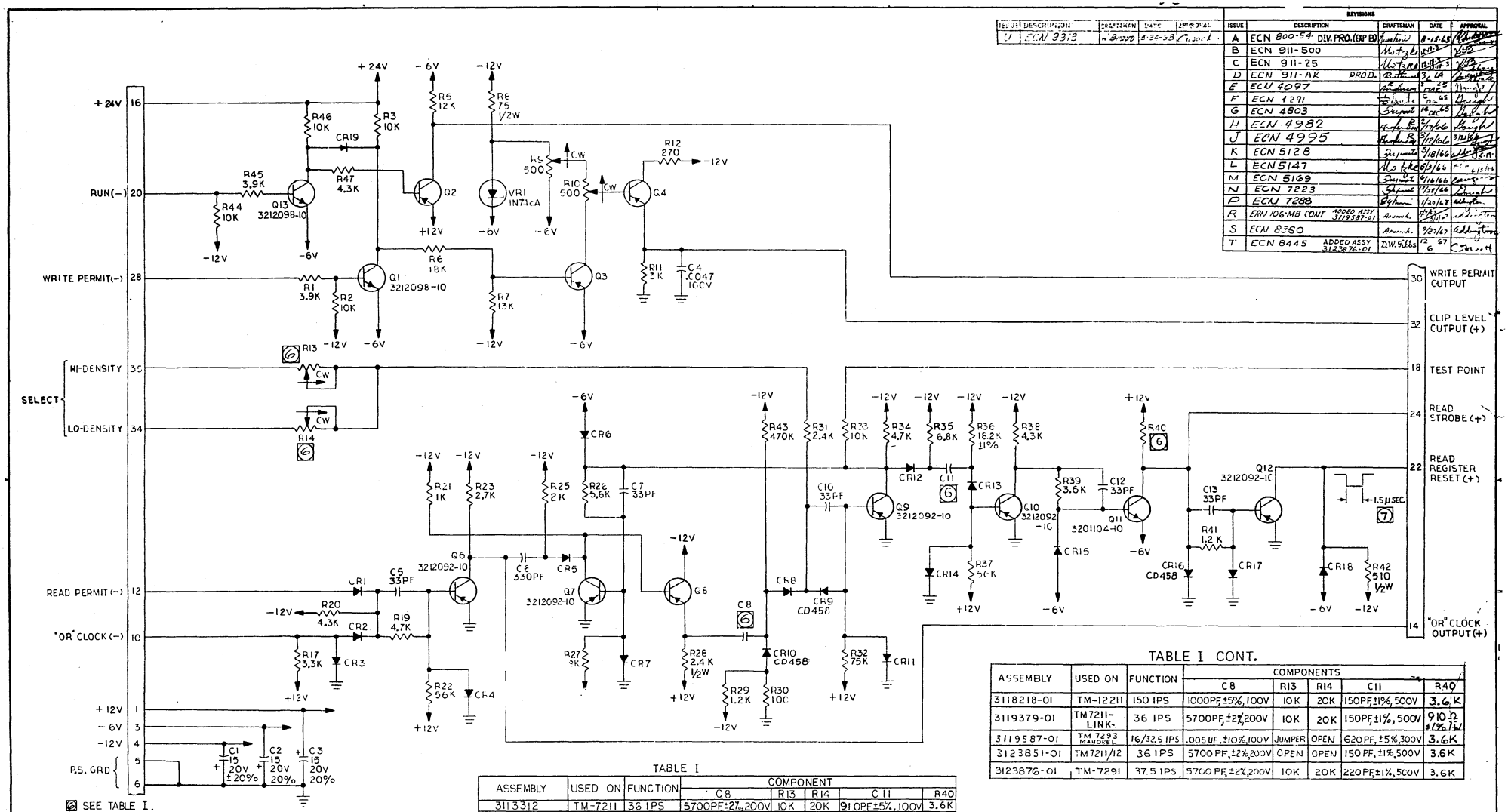
PROJ SUPER	[illegible]	5/4/64
PROJ ENGR	[illegible]	5/4/64
ENGR	[illegible]	5/4/64
CHKR	[illegible]	4-30-64
DFTSMN	V. Aceline	4-22-64

AMPEX 0/1 AMPEX COMPUTER PRODUCTS COMPANY
9937 JEFFERSON BLVD. CULVER CITY, CALIFORNIA

TITLE CIRCUIT BOARD ASSY - READ DESKEW, BI-DIRECTION

CODE INDENT. NO. | SIZE D | DWG. NO. 3109933 | ISSUE R

SCALE 2:1



ISSUE	DESCRIPTION	DRAFTSMAN	DATE	APPROVAL
T	ECN 8445 ADDED ASSY 3123876-01	D.W. Stiles	12 6 67	

ISSUE	DESCRIPTION	DRAFTSMAN	DATE	APPROVAL
A	ECN 800-54 DEV. PRO. (EXP BD)		8-15-65	
B	ECN 911-500			
C	ECN 911-25			
D	ECN 911-AK PROD.			
E	ECN 4097			
F	ECN 4291			
G	ECN 4803			
H	ECN 4982			
J	ECN 4995			
K	ECN 5128			
L	ECN 5147			
M	ECN 5169			
N	ECN 7223			
P	ECN 7288			
R	ERN 106-M8 CONT ADDED ASSY 3119587-01			
S	ECN 8360			
T	ECN 8445 ADDED ASSY 3123876-01	D.W. Stiles	12 6 67	

TABLE I

ASSEMBLY	USED ON	FUNCTION	COMPONENT C8	R13	R14	C11	R40
3113312	TM-7211	36 IPS	5700PF±2%,200V	10K	20K	91 OPF±5%,100V	3.6K
3107057	TM-7211-12	36 IPS	5700PF±2%,200V	10K	20K	150PF±1%,500V	
3113186	TM 7211	7.5 IPS	.033±2%, 200V	10K	20K	150PF±1%,500V	
3109994	TM 4211	75 IPS	2800PF±2%,200V	10K	20K	150PF±1%,500V	
3110003	TM 1121	112.5-120IPS	1800PF±2%,200V	10K	20K	150PF±1%,500V	
3107277	TM 7211	36 IPS	5700PF±2%,200V	10K	20K	150PF±1%,500V	
3112412	DE 213	75 IPS	.0022±10%, 100V	JUMPER	OPEN	150PF±1%,500V	
3113187	TM 7211	15 IPS	.015±2%, 200V	10K	20K	150PF±1%,500V	
3116102	TM 7211 INTERSTATE	7.51PS	.033±2%,200V	10K	20K	620PF±5%,300V	
3116164	TM 9241	30 IPS	5700PF,±2%,200V	10K	20K	.0022uF±10%,100V	
3118123	TM-7293	10/20 IPS	.01 ±5%, 100V	JUMPER	OPEN	620PF±5% 300V	
3118189-01	DE-213	7.5/15/30 IPS	5700PF,±2%,200V	JUMPER	OPEN	150PF,±1%,500V	3.6K

TABLE I CONT.

ASSEMBLY	USED ON	FUNCTION	COMPONENTS C8	R13	R14	C11	R40
3118218-01	TM-12211	150 IPS	1000PF±5%,100V	10K	20K	150PF±1%,500V	3.6K
3119379-01	TM7211-LINK-	36 IPS	5700PF,±2%,200V	10K	20K	150PF,±1%,500V	910Ω ±(3%) 1/2W
3119587-01	TM 7293 MANDREL	16/32.5 IPS	.005 UF, ±10%,100V	JUMPER	OPEN	620PF, ±5%,300V	3.6K
3123851-01	TM7211/12	36 IPS	5700 PF, ±2%,200V	OPEN	OPEN	150 PF, ±1%,500V	3.6K
3123876-01	TM-7291	37.5 IPS	5700 PF, ±2%,200V	10K	20K	220PF,±1%,500V	3.6K

[6] SEE TABLE I.

5. ALL DIODES TO BE 3263024-10.
4. ALL TRANSISTORS TO BE 3201100-10.
3. ALL RESISTOR VALUES ARE IN OHMS, 1/4W, ±5%.
2. ALL CAPACITOR VALUES ARE IN MICROFARADS, 500V, ±10%.
1. FOR ASSEMBLY SEE TABLE.

NOTES: UNLESS OTHERWISE SPECIFIED

[7] RESET PULSE 8.0μs. WIDE ON 3113312; 4.5μs WIDE ON 3116102

DO NOT SCALE DRAWING

UNLESS OTHERWISE SPECIFIED TOLERANCES
DECIMALS XX ± XXX ±
ANGLES ±
BREAK ALL SHARP EDGES APPROX. .010
CROSS AND SPOTFACE CORNER RADII .010
ROUGHNESS OF ALL MACHINED SURFACES PER MIL-STD-10
MATERIAL
FINISH

THE INFORMATION HEREON IS THE PROPERTY OF AMPEX COMPUTER PRODUCTS COMPANY, INC. ITS REPRODUCTION OR UNAUTHORIZED USE IN ANY MANNER WHATSOEVER WITHOUT THE WRITTEN CONSENT OF AMPEX COMPUTER PRODUCTS CO.

PROJ
SUPER
PROJ ENGR
ENGR
CHKR P. Anderson 9/15/65
DFTSMN

AMPEX COMPUTER PRODUCTS COMPANY
9937 JEFFERSON BLVD. CULVER CITY, CALIFORNIA

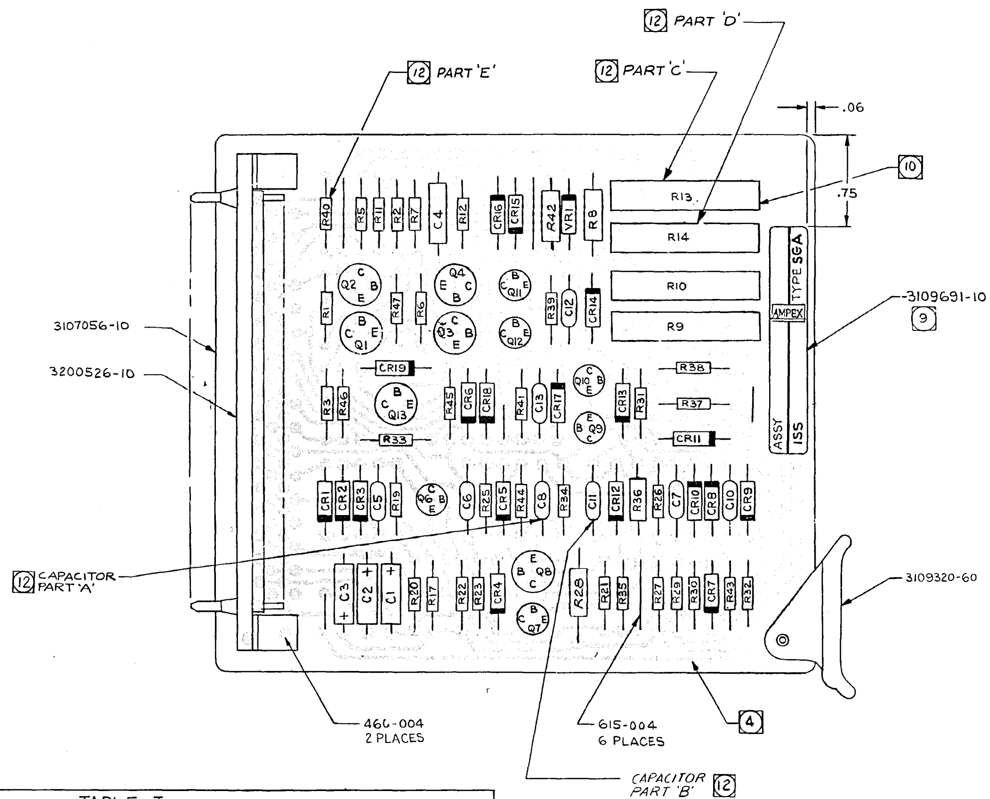
TITLE
SCHEMATIC—
STROBE GENERATOR

CODE IDENT. NO.	SIZE	DWG. NO.	ISSUE
	D	3107058	U

SCALE NONE SHEET 1 OF 1

DIETERICH-POST CLEARPRINT 1088H-8 FORM 2603-107 REV. 11-62

REVISIONS				
ISSUE	DESCRIPTION	DRAFTSMAN	DATE	APPROVAL
A	ECN 911-AK PROD.	Butterworth	3/6/64	[illegible]
B	ECN 3849	Natzke	64	[illegible]
	[illegible] 4097	[illegible]	[illegible]	[illegible]
D	ECN 4803	[illegible]	14 DEC 65	[illegible]
E	ECN 4982	[illegible]	2/17/66	[illegible]
F	ECN 5169	[illegible]	6/16/66	[illegible]
G	ECN 7003	E. REISS	9/15/66	
H	ECN 7223	[illegible]	12/28/66	[illegible]
J	ECN [illegible]8	[illegible]	1/19/67	Addington
K	ECN 8360	[illegible]	9/21/67	Addington
L	ECN 8445	D.W. Sibbs	12 6 67	[illegible]
M	ECN 9913	H. Bravo	5-24-68	[illegible]

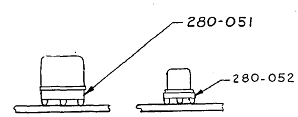


PART NO.	REFERENCE DESIGNATIONS
041-503	R12
041-507	R26
041-511	R1,45
041-512	R43
041-516	R8
041-519	R22,37
041-549	R7
041-550	R11
041-571	R39
041-570	R31
PART E	R40
041-573	R32
041-584	R20,38,47
041-419	R30
042-803	R36
PART C	R13
044-202	R9,10
PART D	R14
041-316	R28
041-440	R29,41
041-404	R42
041-560	R25

PART NO.	REFERENCE DESIGNATIONS
3201100-10	Q2,3,4,8
3201104-10	Q11
3212092-10	Q6,7,9,10,12
3212098-10	Q1,13
3263024-10	CR1 THRU 8, CR11 THRU 15, CR17,18,19
013-599	CR9,10,16
013-166	VR1
PART A	C8
034-491	C5,7,10,12,13
034-493	C6
PART B	C11
035-989	C4
037-990	C1,2,3
041-407	R17
041-408	R2,3, .33,44,46
041-410	R21
041-412	R19,34
041-413	R35
041-415	R27
041-436	R6
041-442	R23
041-482	R5

TABLE I

B/M REFERENCE TABLE					USED ON	
ASSY	PART 'A'	PART 'B'	PART 'C'	PART 'D'		PART 'E'
3107057	033-146	034-220	044-197	044-523	TM-7211	041-571
3109994	035-832	034-220	↑	↑	TM-4211	↑
3110003	033-147	034-220			TM-11211	
3107277	033-146	034-220			TM-7211	
3113312	033-146	034-217			TM-7211	
3116102	033-276	034-228			TM-7211-INTERSTATE	
3116164	033-146	035-988	↓	↓	TM-9241	
3118218	034-950	034-220	044-197	044-523	TM-12211	↓
3113186	033-276	034-220	044-197	044-523	EAI-TM-7211	041-571
3119379	033-146	034-220	044-197	044-523	TM 7211 LINK	047-472
3123851-01	033-146	034-220	NOT USED	NOT USED	TM 7211/12	041-571
3123876-01	033-146	034-225	044-197	044-523	TM-7291 MARSHALL	041-571



TYPICAL TRANSISTOR INSTALLATION

REFERENCE

12 INSTALL PER TABLE I.

11. SEAL PRINTED CIRCUIT SIDE ONLY WITH HUMI-SEAL TYPE 1B15, COLUMBIA TECH. CORP., OR EQUIV.

10 TRIMPOTS NOT TO BE SUBMERGED IN WATER.

9 MARK PART NO. AND NAMEPLATE INFORMATION PER MIL-STD-130.

8. PART NO. TO BE AS SHOWN ON B/M.

7. HEAVY LINE ON DIODE INDICATES CATHODE.

6. PLUS SIGN ON CAPACITOR INDICATES POSITIVE.

5. COMPONENT DESIGNATIONS ARE FOR REFERENCE ONLY.

4. CIRCUITRY ON FARSIDE.

3. ASSEMBLE PER AMPEX STANDARDS

2. FOR PERF SPECIFICATION SEE 3107059.

1. FOR SCHEMATIC SEE 3107058.

NOTES:

REQD.	PART NO.	DESCRIPTION	REFERENCE	ZONE	ITEM

LIST OF MATERIAL

DO NOT SCALE DRAWING

UNLESS OTHERWISE SPECIFIED TOLERANCES
DECIMALS .XX ± .03 .XXX ± .010 ANGLES ± 1/2°
BREAK ALL SHARP EDGES APPROX. .010
C'BORE AND SPOTFACE CORNER RADII .010
ROUGHNESS OF ALL MACHINED SURFACES ✓ PER MIL-STD-10

MATERIAL

FINISH

SEE TABLE	
NEXT ASSY.	1ST USED ON
APPLICATION	

FORM 2602-107 REV. 9-61

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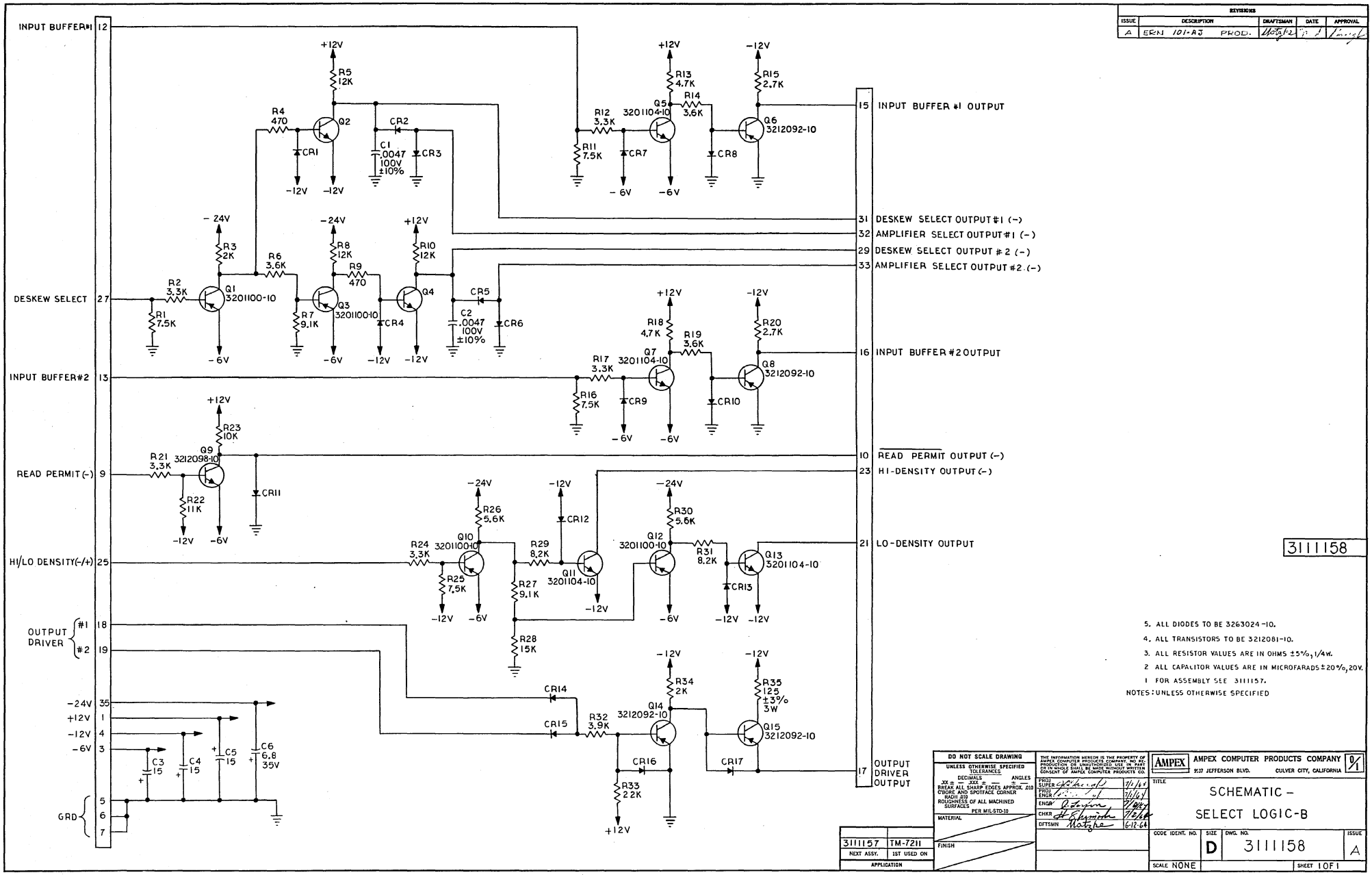
PROJ SUPER	S. Blanc	3/6/64
PROJ ENGR	S. BLANC	3/15/63
ENGR	J. Zanoni	3/6/64
CHKR	C ANDERSON	3-15-63
DFTSMN	J. BUTTERWORTH	6-24-63

AMPEX 0/1 AMPEX COMPUTER PRODUCTS COMPANY
9937 JEFFERSON BLVD. CULVER CITY, CALIFORNIA

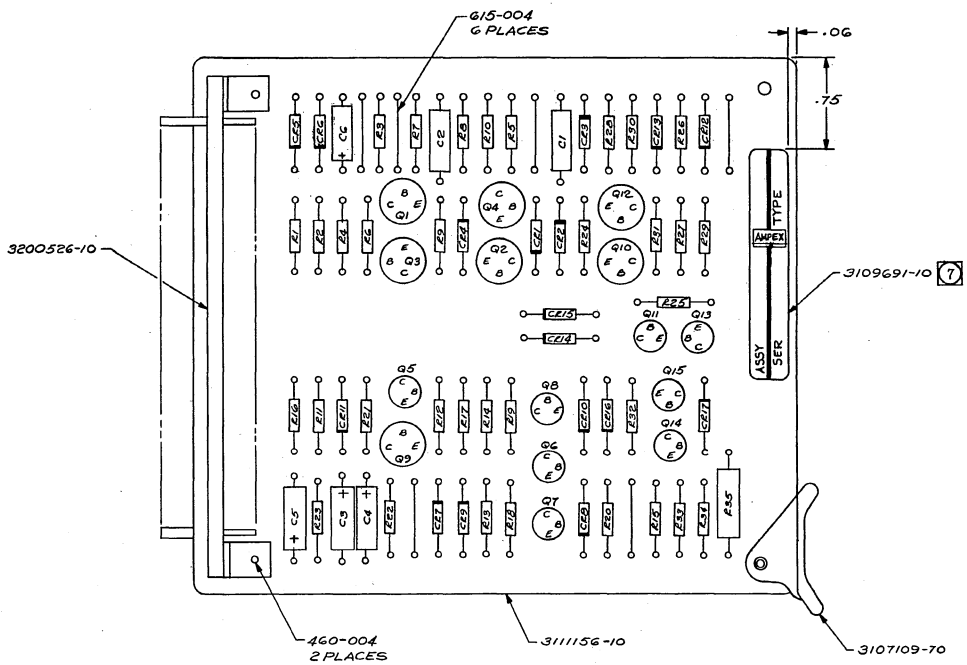
TITLE: CIRCUIT BOARD ASSEMBLY— STROBE GENERATOR

CODE INDENT. NO.	SIZE	DWG. NO.	ISSUE
	D	3107276	M

SCALE 2/1

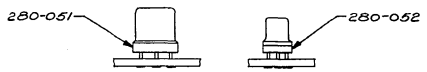

INPUT BUFFER#1
12
+12V
R5
12K
R4
470
Q2
CR2
CR1
C1
.0047
100V
±10%
CR3
-12V
-12V
R12
3.3K
Q5
3201104-10
R13
4.7K
R14
3.6K
R15
2.7K
Q6
3212092-10
R11
7.5K
CR7
CR8
-6V
-6V
15
INPUT BUFFER #1 OUTPUT
31
DESKEW SELECT OUTPUT #1 (-)
32
AMPLIFIER SELECT OUTPUT #1 (-)
29
DESKEW SELECT OUTPUT #2 (-)
33
AMPLIFIER SELECT OUTPUT #2 (-)
DESKEW SELECT
27
-24V
R3
2K
R6
3.6K
R8
12K
R9
470
R10
12K
R2
3.3K
Q1
3201100-10
Q3
3201100-10
Q4
CR5
R1
7.5K
R7
9.1K
CR4
C2
.0047
100V
±10%
CR6
-6V
-6V
-12V
-12V
INPUT BUFFER#2
13
+12V
R18
4.7K
R19
3.6K
R20
2.7K
R17
3.3K
Q7
3201104-10
Q8
3212092-10
16
INPUT BUFFER #2 OUTPUT
R16
7.5K
CR9
CR10
-6V
-6V
+12V
R23
10K
Q9
3212098-10
R21
3.3K
READ PERMIT (-)
9
R22
11K
CR11
-12V
-6V
10
READ PERMIT OUTPUT (-)
23
HI-DENSITY OUTPUT (-)
-24V
R26
5.6K
-12V
CR12
-24V
R30
5.6K
HI/LO DENSITY(-/+)
25
R24
3.3K
Q10
3201100-10
R29
8.2K
Q11
3201104-10
Q12
3201100-10
R31
8.2K
Q13
3201104-10
21
LO-DENSITY OUTPUT
R25
7.5K
R27
9.1K
CR13
-12V
-6V
-12V
-12V
-12V
-6V
R28
15K
OUTPUT DRIVER #1
18
#2
19
CR14
CR15
-12V
-12V
R34
2K
R35
125
±3%
3W
R32
3.9K
Q14
3212092-10
Q15
3212092-10
CR16
CR17
R33
2.2K
+12V
17
OUTPUT DRIVER OUTPUT
-24V
35
+12V
1
-12V
4
-6V
3
C3
15
C4
15
C5
15
C6
6.8
35V
GRD
5
6
7
3111158
5. ALL DIODES TO BE 3263024-10.
4. ALL TRANSISTORS TO BE 3212081-10.
3. ALL RESISTOR VALUES ARE IN OHMS ±5%, 1/4W.
2 ALL CAPACITOR VALUES ARE IN MICROFARADS ±20%, 20V.
1 FOR ASSEMBLY SEE 3111157.
NOTES: UNLESS OTHERWISE SPECIFIED
REVISIONS
ISSUE
DESCRIPTION
DRAFTSMAN
DATE
APPROVAL
A
ERN 101-AJ PROD.
DO NOT SCALE DRAWING
UNLESS OTHERWISE SPECIFIED TOLERANCES
DECIMALS XX ± XXX ±
ANGLES °
BREAK ALL SHARP EDGES APPROX. .010
C'BORE AND SPOTFACE CORNER RADII .010
ROUGHNESS OF ALL MACHINED SURFACES PER MIL-STD-10
MATERIAL
FINISH
APPLICATION
3111157
TM-7211
NEXT ASSY.
1ST USED ON
PROJ
SUPER
PROJ
ENGR
ENGR
CHKR
DFTSMN
7/1/64
7/1/64
7/1/64
7/1/64
6-12-64
AMPEX
AMPEX COMPUTER PRODUCTS COMPANY
9937 JEFFERSON BLVD. CULVER CITY, CALIFORNIA
TITLE
SCHEMATIC –
SELECT LOGIC-B
CODE IDENT. NO.
SIZE
D
DWG. NO.
3111158
ISSUE
A
SCALE NONE
SHEET 1 OF 1

REVISIONS				
ISSUE	DESCRIPTION	DRAFTSMAN	DATE	APPROVAL
A	ERN 101-AJ PROD.	[illegible]	7/1/69	[illegible]



PART NO.	REFERENCE DESIGNATION
3201100-10	Q1,Q3,Q10,Q12
3201104-10	Q5,Q7,Q11,Q13
3212081-10	Q2,Q4
3212092-10	Q6,Q8,Q14,Q15
3212098-10	Q9
3263024-10	CR1 THRU CR17
035-989	C1,C2
037-095	C6
037-990	C3,C4,C5
041-406	R33
041-407	R2,R12,R17,R21,R24
041-408	R23
041-409	R28
041-412	R13,R18
041-428	R4,R9
041-442	R15,R20
041-482	R5,R8,R10
041-495	R29,R31
041-507	R26,R30
041-511	R32
041-514	R7,R27
041-520	R1,R11,R16,R25
041-560	R3,R34
041-571	R6,R14,R19
047-302	R35
041-748	R22

3111157



TYPICAL TRANSISTOR INSTALLATION

8. SEAL PRINTED CIRCUIT SIDE ONLY WITH HUMI-SEAL TYPE 1B15 COLUMBIA TECH. CORP. OR EQUIVALENT.
7. MARK PART NO. AND NAMEPLATE INFORMATION PER MIL-STD-130.
6. PART NO. TO BE 3111157-10.
5. PLUS SIGN ON CAPACITOR INDICATES POSITIVE.
4. HEAVY LINE ON DIODE INDICATES CATHODE.
3. ASSEMBLE PER PRODUCTION PRACTICES MANUAL.
2. FOR ASSEMBLY SPECIFICATION SEE 3111159.
1. FOR SCHEMATIC SEE 3111158.

NOTES:

DO NOT SCALE DRAWING
UNLESS OTHERWISE SPECIFIED TOLERANCES
DECIMALS ANGLES
XX ± .03 XXX ±
BREAK ALL SHARP EDGES APPROX. .010
C'BORE AND SPOTFACE CORNER RADII .010
ROUGHNESS OF ALL MACHINED SURFACES PER MIL-STD-10
MATERIAL
FINISH

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PROJ SUPER.	[illegible]	7/1/69
PROJ ENGR.	[illegible]	7/1/69
ENGR.	[illegible]	7/1/69
CHKR.	[illegible]	7/1/69
DFTSMN.	[illegible]	7/1/69

FINAL ASSY.	TM-7211
NEXT ASSY.	1ST USED ON
APPLICATION	

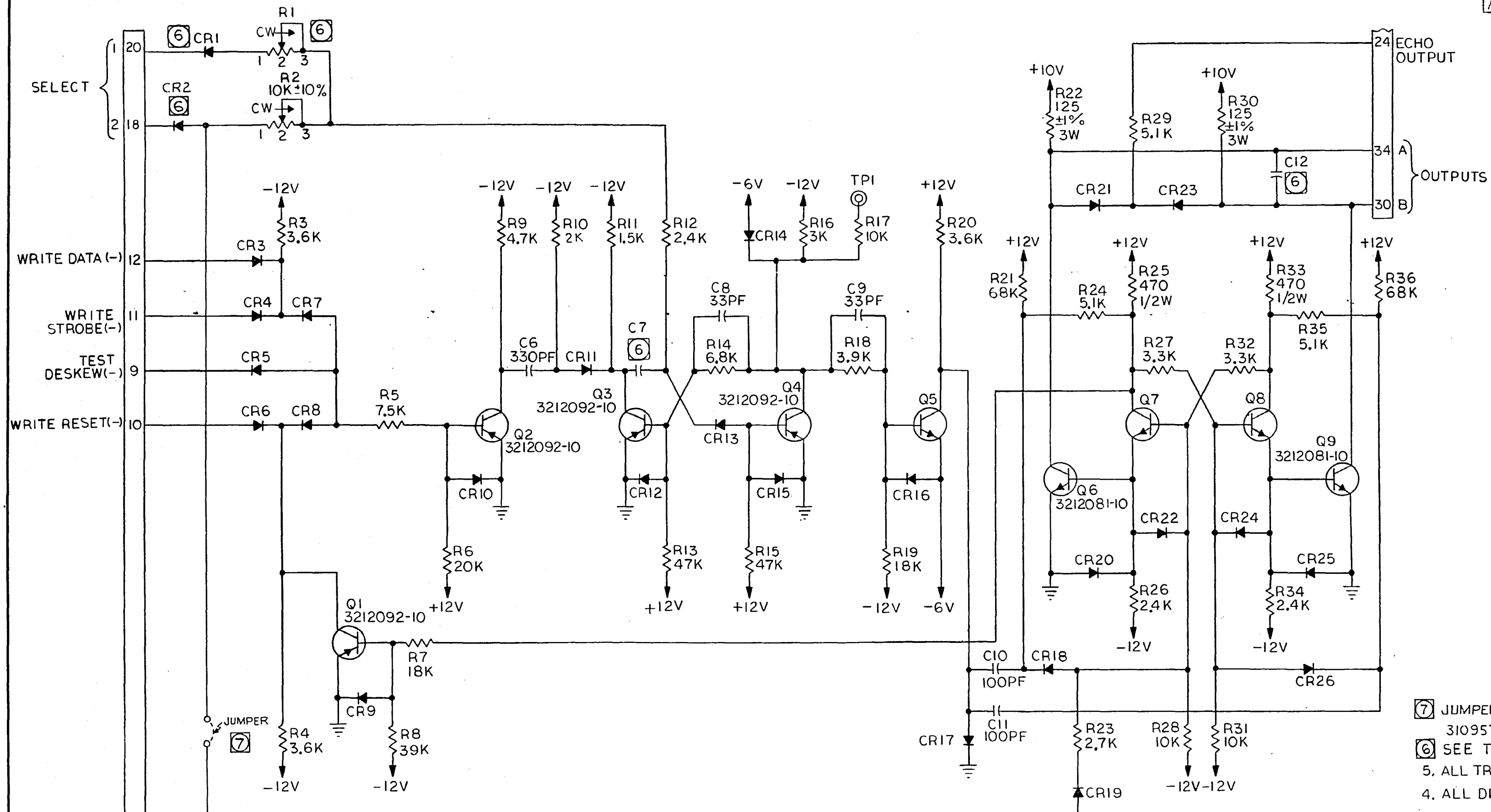
AMPEX COMPUTER PRODUCTS COMPANY
9937 JEFFERSON BLVD. CULVER CITY, CALIFORNIA

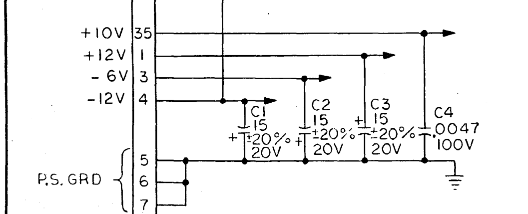
TITLE
CIRCUIT BOARD ASSY-
SELECT LOGIC-B

CODE IDENT. NO.	SIZE	DWG. NO.	ISSUE
	D	3111157	A

SCALE 2/1 SHEET 1 OF 1

REVISIONS				
ISSUE	DESCRIPTION	DRAFTSMAN	DATE	APPROVAL
K	EWN 106-MB CONT ADD ASSY 3119586-01	[illegible]	5/3/67 5/4/67	[illegible]
L	ECN 8830	H. Brown	8-1-67 9-1-67	[illegible]
M	ECN 9313	H. Brown	5-24-68	[illegible]





REFERENCE DESIGNATION	
LAST USED	DELETED
R36	
CR26	
C12	
Q9	

3112345

7 JUMPER TO BE USED ON ASSEMBLY 3112363-10, 3109572-10, 3110002-10 & 3123869-01

6 SEE TABLE I.

5. ALL TRANSISTORS TO BE 3201104-10.

4. ALL DIODES TO BE 3263024-10.

3. ALL RESISTOR VALUES ARE IN OHMS, 1/4W, ±5%.

2. ALL CAPACITOR VALUES ARE IN MICROFARADS, ±10%, 500V.

1. FOR ASSEMBLY SEE TABLE I.

NOTES: UNLESS OTHERWISE SPECIFIED

TABLE I

ASSEMBLY	FUNCTION	C7	C12	R1	CR1	CR2	SINGLE SPEED	DUAL SPEED
3123869-01	10 IPS	.0047 ±10%, 100V	NOT USED	10K ±10%	CD458	CD458	X	
3119586-01	16/32.5 IPS	.0022 UF, ±10%, 100V	NOT USED	10K, ±10%	CD458	CD458		X
3112363-10	36-54 IPS	1800PF ±2%, 200V	NOT USED	NOT USED	NOT USED	NOT USED	X	
3109572-10	54-90 IPS	910PF ±5%, 100V	↑	NOT USED	NOT USED	NOT USED	X	
3110002-10	90-120 IPS	620PF ±5%, 300V		NOT USED	NOT USED	NOT USED	X	
3112364-10	36-54 IPS	1800PF ±2%, 200V		10K ±10%	CD458	CD458		X
3112344-10	54-90 IPS	910 PF ±5%, 100V		10K ±10%	↑	↑		X
3112365-10	90-150 IPS	620 PF ±5%, 300V	↓	10K ±10%				X
3113131-10	105/52.5 IPS	1500 PF ±10%, 100V	NOT USED	10K ±10%	↓	↓		X
3118121-01	10-20 IPS	.0047 ± 10%, 100V	NOT USED	10K, ± 10%	CD458	CD458		X

SEE TABLE	DE-200
NEXT ASSY.	1ST USED ON
APPLICATION	

DO NOT SCALE DRAWING

UNLESS OTHERWISE SPECIFIED TOLERANCES DECIMALS .XX ± .XXX ± ANGLES ± BREAK ALL SHARP EDGES APPROX. .010 C'BORE AND SPOTFACE CORNER RADII .010 ROUGHNESS OF ALL MACHINED SURFACES PER MIL-STD-10

MATERIAL

FINISH

THE INFORMATION HEREON IS THE PROPERTY OF AMPEX COMPUTER PRODUCTS COMPANY. NO REPRODUCTION OR UNAUTHORIZED USE IN PART OR IN WHOLE SHALL BE MADE WITHOUT WRITTEN CONSENT OF AMPEX COMPUTER PRODUCTS CO.

PROJ SUPER
PROJ ENGR
ENGR [illegible] 8-1-67
CHKR
DFTSMN H. Nitrao 12-20-?

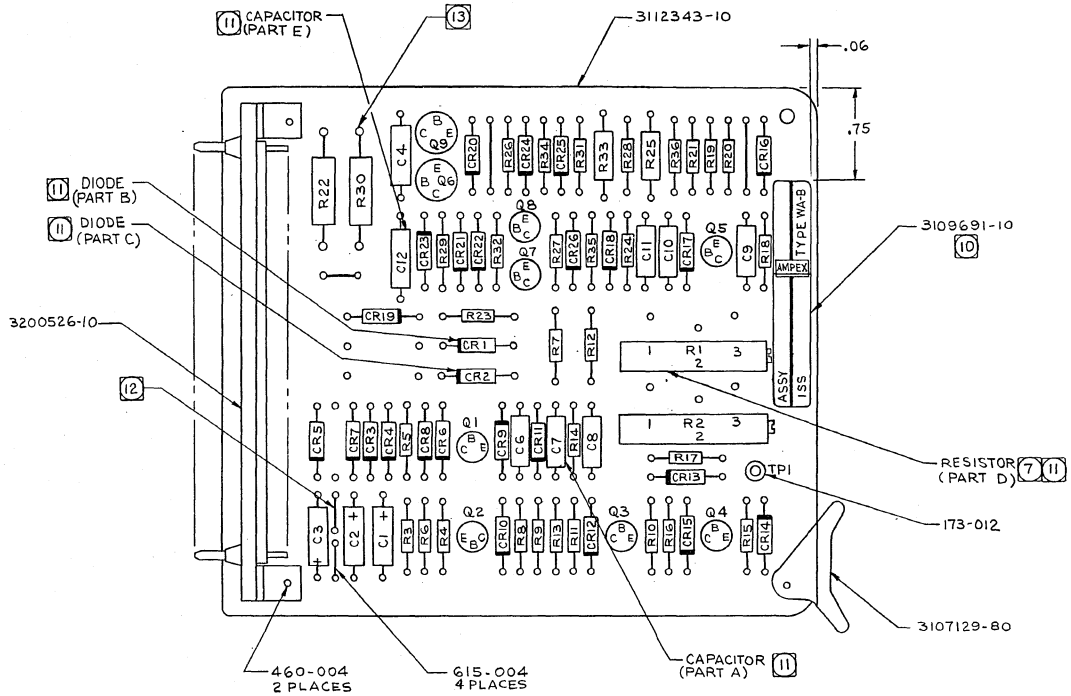
AMPEX COMPUTER PRODUCTS COMPANY 9937 JEFFERSON BLVD. CULVER CITY, CALIFORNIA

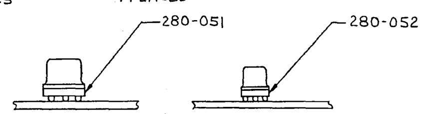
TITLE SCHEMATIC— WRITE AMPLIFIER-B

CODE IDENT. NO.	SIZE	DWG. NO.	ISSUE
	D	3112345	M

SCALE NONE SHEET 1 OF 1

REVISIONS				
ISSUE	DESCRIPTION	DRAFTSMAN	DATE	APPROVAL
G	ECN 4454 PROD. RELEASE	[illegible]	7-2-65	[illegible]
H	ECN 4522	Matzke	8/30/65	[illegible]
J	ECN 4995	Anderson	3/18/66	[illegible]
K	ECN 5084	Anderson	4/27/66	Allington
L	ECN 5151	Matzke	6/6/66	Allington
M	ERN 106-MB CONT ADDED 3119586	Arsanski	5/3/67 5/4/67	Allington
N	ECN 7931	L. Etchison	6/19/67	Allington
P	ECN 8230	H. Brown	8-1-67	Allington
R	ECN 9913	H. Brown	5-24-68	Cusack





TYPICAL TRANSISTOR INSTALLATION

PART NO.	REFERENCE DESIGNATION	PART NO.	REFERENCE DESIGNATION
041-442	R23	3201104-10	Q5, Q7, Q8
041-443	R8	3212081-10	Q6, Q9
041-511	R18	3212092-10	Q1, Q2, Q3, Q4
041-520	R5	3263024-10	CR3 THRU CR26
041-571	R3, R4, R20	PART B	CR1
041-550	R16	PART A	C7
041-561	R24, R29, R35	034-417	C10, C11
041-570	R12, R26, R34	034-491	C8, C9
		034-493	C6
041-508	R6	035-989	C4
041-415	R21, R36	037-990	C1, C2, C3
044-197	R2	041-336	R25, R33
047-340	R22, R30	041-407	R27, R32
PART C	CR2	041-408	R17, R28, R31
PART D	R1	041-411	R13, R15
PART E	C12	041-412	R9
041-560	R10	041-413	R14
		041-430	R11
		041-436	R19, R7

(13) INSTALL R22 & R30 PER PRODUCTION PRACTICES MANUAL, SECTION 7 HE2-5, FIGURE 10, HIGH WATTAGE RESISTOR SPACING.

(12) INSTALL JUMPER ONLY ON ASSEMBLY 3112363-10, 3109572-10, 3110002-10 & 3123869-01

(11) INSTALL PARTS A,B,C,D,E PER TABLE I.

3112347

(10) MARK PART NO. & NAMEPLATE INFORMATION PER MIL-STD-130.

9. PART NO. TO BE AS SHOWN ON TABLE I.

8. SEAL PRINTED CIRCUIT SIDE ONLY WITH HUMI-SEAL TYPE IB15 COLUMBIA TECH. CORP. OR EQUIV.

(7) TRIMPOTS NOT TO BE SUBMERGED IN WATER.

6. PLUS SIGN ON CAPACITOR INDICATES POSITIVE.

5. HEAVY LINE ON DIODE INDICATES CATHODE.

4. COMPONENT DESIGNATIONS ARE FOR REFERENCE ONLY.

3. ASSEMBLE PER AMPEX STANDARDS.

2. FOR PERF SPECIFICATION SEE TABLE I.

1. FOR SCHEMATIC SEE 3112345.

NOTES:

REFERENCE

TABLE I

	B/M REFERENCE TABLE					ASSEMBLY SPECIFICATION
ASSEMBLY	PART A	PART B	PART C	PART D	PART E	
3123869-01	035-989	013-599	013-599	044-197	NOT USED	3113154
3112363-10	033-147	NOT USED	NOT USED	NOT USED	NOT USED	3112346
3109572-10	034-386	NOT USED	NOT USED	NOT USED	NOT USED	
3110002-10	034-228	NOT USED	NOT USED	NOT USED	NOT USED	
3112364-10	033-147	013-599	013-599	044-197	NOT USED	
3112344-10	034-386	013-599	013-599	044-197	NOT USED	
3112365-10	034-228	013-599	013-599	044-197	NOT USED	
3113131-10	035-509	013-599	013-599	044-197	NOT USED	3113154
3118121-01	035-989	013-599	013-599	044-197	NOT USED	3113154
3119586-01	035-988	013-599	013-599	044-197	NOT USED	3113154

SEE TABLE I	DE-200
NEXT ASSY.	1ST USED ON
APPLICATION	

DO NOT SCALE DRAWING

UNLESS OTHERWISE SPECIFIED TOLERANCES
DECIMALS .XX ±.03 .XXX ±.010 ANGLES ± —
BREAK ALL SHARP EDGES APPROX .010
C'BORE AND SPOTFACE CORNER RADII .010
ROUGHNESS OF ALL MACHINED SURFACES PER MIL-STD-10

MATERIAL

FINISH

THE INFORMATION HEREON IS THE PROPERTY OF AMPEX COMPUTER PRODUCTS COMPANY. NO REPRODUCTION OR UNAUTHORIZED USE IN PART OR IN WHOLE SHALL BE MADE WITHOUT WRITTEN CONSENT OF AMPEX COMPUTER PRODUCTS CO.

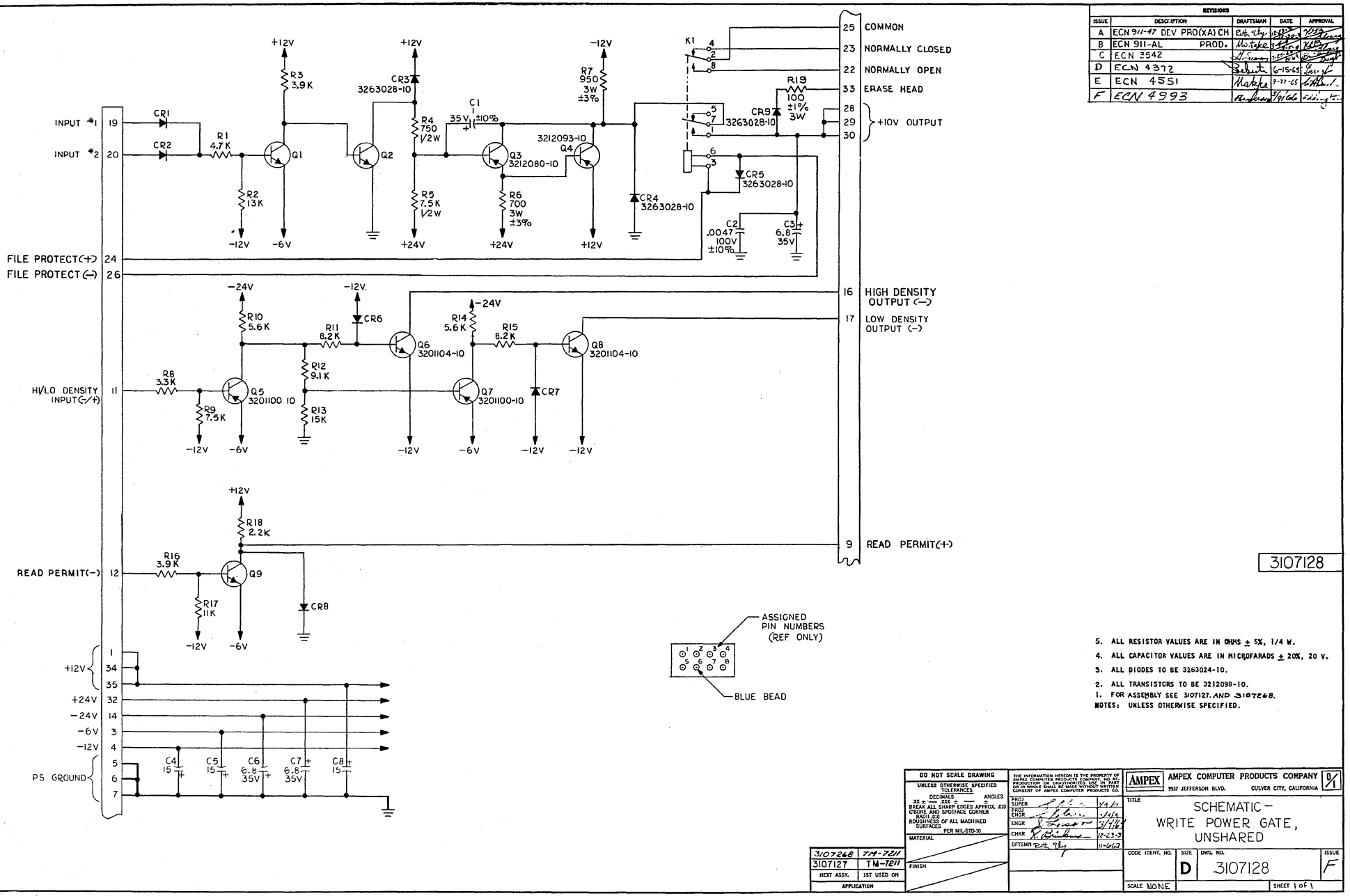
PROJ SUPER	[illegible]	7/[illegible]/65
PROJ ENGR	[illegible]	7/[illegible]/65
ENGR	[illegible]	7/[illegible]/65
CHKR	[illegible]	7/20/65
DFTSMN	M. Matzke	1-6-65

AMPEX COMPUTER PRODUCTS COMPANY
9937 JEFFERSON BLVD. CULVER CITY, CALIFORNIA

TITLE: CIRCUIT BOARD ASSY- WRITE AMPLIFIER-B

CODE IDENT. NO. | SIZE D | DWG. NO. 3112347 | ISSUE R

SCALE 2:1 | SHEET 1 OF 1



REVISIONS				
ISSUE	DESCRIPTION	DRAFTSMAN	DATE	APPROVAL
A	ECN 911-47 DEV PRO(XA) CH			
B	ECN 911-AL PROD.			
C	ECN 3542			
D	ECN 4372		6-15-65	
E	ECN 4551		8-22-65	
F	ECN 4993		9/9/66	

3107128

5. ALL RESISTOR VALUES ARE IN OHMS ± 5%, 1/4 W.
4. ALL CAPACITOR VALUES ARE IN MICROFARADS ± 20%, 20 V.
3. ALL DIODES TO BE 3263024-10.
2. ALL TRANSISTORS TO BE 3212098-10.
1. FOR ASSEMBLY SEE 3107127 AND 3107268.

NOTES: UNLESS OTHERWISE SPECIFIED.

DO NOT SCALE DRAWING

UNLESS OTHERWISE SPECIFIED TOLERANCES

DECIMALS XX ± — XXX ± — ANGLES ±

BREAK ALL SHARP EDGES APPROX. .010 CBORE AND SPOTFACE CORNER RADII .010 ROUGHNESS OF ALL MACHINED SURFACES PER MIL-STD-10

MATERIAL

FINISH

APPLICATION

3107268	TM-7211
3107127	TM-7211
NEXT ASSY.	1ST USED ON

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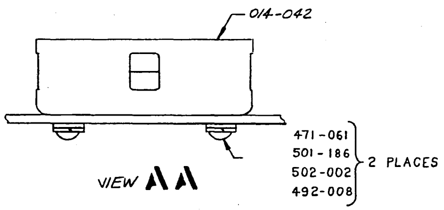
PROJ SUPER		9/1/66
PROJ ENGR		9/1/66
ENGR		9/7/66
CHKR		12-23-3
DFTSMN		11-66

AMPEX COMPUTER PRODUCTS COMPANY
9937 JEFFERSON BLVD. CULVER CITY, CALIFORNIA

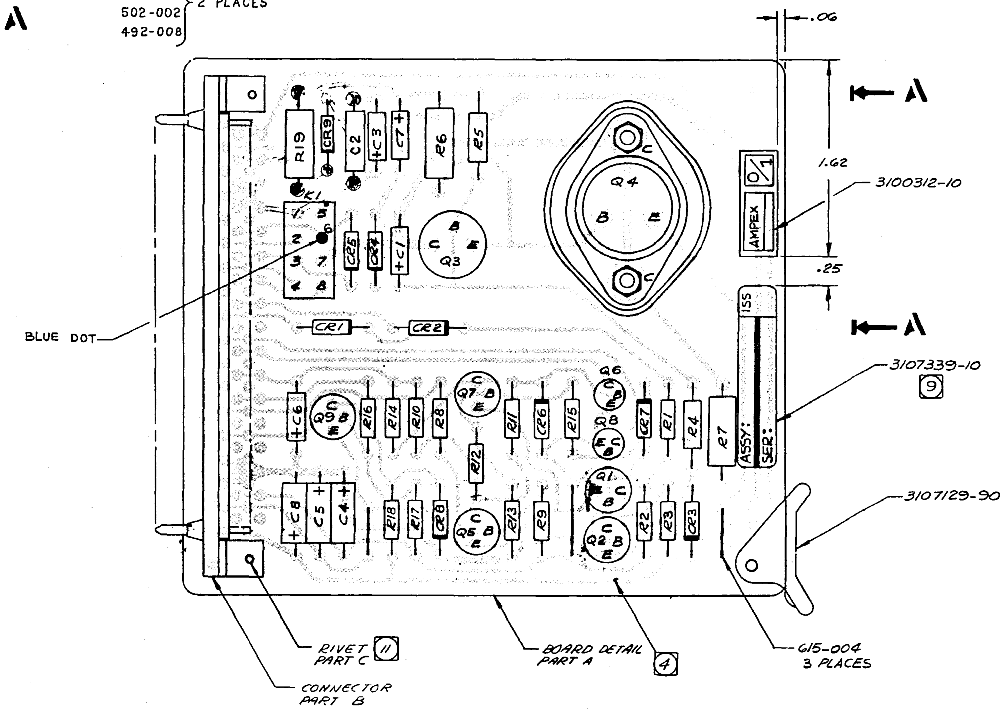
TITLE: SCHEMATIC — WRITE POWER GATE, UNSHARED

CODE IDENT. NO.	SIZE	DWG. NO.	ISSUE
	D	3107128	F

SCALE NONE SHEET 1 OF 1



REVISIONS				
ISSUE	DESCRIPTION	DRAFTSMAN	DATE	APPROVAL
A	ECN 911-A / DEV PRO (X-A) CH	[illegible]	[illegible]	[illegible]
B	ECN 911-AL PROD.	Matzke	[illegible]	[illegible]
C	ECN 3542	[illegible]	[illegible]	[illegible]
D	ECN 3750	Matzke	[illegible]	[illegible]
E	ECN 4377	[illegible]	[illegible]-15-65	[illegible]
F	ECN 4551	Matzke	[illegible]	[illegible]
G	ECN 7082	Reiss	10/12/66	[illegible]

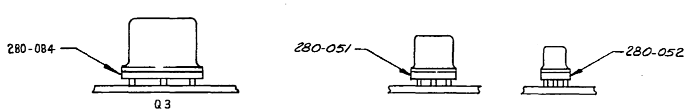


PART NO.	REFERENCE DESIGNATIONS
3201100-10	Q5,7
3201104-10	Q6,8
3212080-10	Q3
3212093-10	Q4
3212098-10	Q1,2,9
3263024-10	CR1,2,6,7,8
3263028-10	CR3,4,5,9
035-989	C2
037-095	C3,6,7
037-265	C1
037-990	C4,5,8
041-007	R4
041-361	R5
041-407	R8
041-414	R18
041-409	R13
041-412	R1
041-495	R11,15
041-507	R10,14
041-511	R3,16
041-514	R12
041-520	R9
041-549	R2
041-748	R17
047-408	R6
047-632	R7
020-233	K1
047-764	R19

3107272

11. RIVET, PART C USED ONLY WITH 3200526-10.
10. PART NO. TO BE AS SHOWN IN BILL OF MATERIAL.
9. MARK PART NO. AND SERIAL NO. PER MIL-STD-130.
8. SEAL PRINTED CIRCUIT SIDE ONLY WITH HUMI-SEAL TYPE 1B15 COLUMBIA TECH. CORP., OR EQUIVALENT.
7. PLUS SIGN ON CAPACITOR INDICATES POSITIVE.
6. COMPONENT DESIGNATIONS ARE FOR REFERENCE ONLY.
5. ASSEMBLE PER MANUFACTURING PRACTICES MANUAL.
4. CIRCUITRY ON FAR SIDE.
3. HEAVY LINE ON DIODE INDICATES CATHODE.
2. FOR ASSEMBLY SPECIFICATION SEE 3107121.
1. FOR SCHEMATIC SEE 3107128.

NOTES:



TYPICAL TRANSISTOR INSTALLATION

REFERENCE

3107268	TM-7211
3107127	TM-7211
NEXT ASSY	1ST USED ON
APPLICATION	

DO NOT SCALE DRAWING

UNLESS OTHERWISE SPECIFIED TOLERANCES
DECIMALS .XX ± .03 .XXX ± .010 ANGLES ± 1/2°
BREAK ALL SHARP EDGES APPROX. .010
C'BORE AND SPOTFACE CORNER RADII .010
ROUGHNESS OF ALL MACHINED SURFACES ✓ PER MIL-STD-10

MATERIAL

FINISH

FORM 2602-107 REV. 9 61

THE INFORMATION HEREON IS THE PROPERTY OF AMPEX COMPUTER PRODUCTS COMPANY. NO REPRODUCTION OR UNAUTHORIZED USE IN PART OR IN WHOLE SHALL BE MADE WITHOUT WRITTEN CONSENT OF AMPEX COMPUTER PRODUCTS CO.

PROJ SUPER	[illegible]	[illegible]
PROJ ENGR	[illegible]	[illegible]/63
ENGR	[illegible]	3/4/64
CHKR	K. [illegible]	12-23-3
DFTSMN	Jansten	12/18-3

LIST OF MATERIAL

AMPEX COMPUTER PRODUCTS COMPANY
9937 JEFFERSON BLVD. CULVER CITY, CALIFORNIA

TITLE CIRCUIT BOARD ASSY— WRITE POWER GATE, UNSHARED

CODE INDENT. NO.	SIZE	DWG. NO.	ISSUE
SCALE 2/1	D	3107272	G

GROUP A - BASIC CONFIGURATION			
CODE	PART NO.	DESCRIPTION	QTY
A136	3124725-02	HORIZONTAL, W/LOGO, W/ D.E.	1
A146	3124725-03	HORIZONTAL, W/O LOGO, W/D.E	1
A236	3124725-04	VERTICAL, W/LOGO, W/D.E.	1
A246	3124725-05	VERTICAL, W/O LOGO, W/D.E.	1
A135	3124725-06	HORIZONTAL, W/LOGO, W/O D.E.	1
A145	3124725-07	HORIZONTAL, W/O LOGO, W/O D.E.	1
A235	3124725-08	VERTICAL, W/ LOGO, W/O D.E.	1
A245	3124725-09	VERTICAL, W/O LOGO, W/O D.E.	1

GROUP B - REEL RETAINERS			
CODE	PART NO.	DESCRIPTION	QTY
B1	3113100-10	IBM HOLD DOWN KNOB	1
	3101267-10	FIXED TAKE UP REEL	1
B2	3113100-10	IBM HOLD DOWN KNOB	2
	3108273-30	EMPTY REEL	1

GROUP C - HEADS			
CODE	PART NO.	DESCRIPTION	QTY
C1	3119337-01	7 CH. W/O ERASE	1
C2	3118430-01	7 CH. W/ ERASE	1
C3	3118429-01	9 CH. W/ERASE (STD. IBM WIRING)	1
⊖ C4	3118429-02	9 CH. W/ERASE (SPECIAL IBM WIRING)	1

GROUP D - MOTION COMMAND				
CODE	PART NO.	DESCRIPTION	LOCAT.	QTY
D1	3119598-01	PCBA, RUN/STOP	J4	1
D2	3119529-01	PCBA, FWD/STOP	J4	1

GROUP E - CABINET			
CODE	PART NO.	DESCRIPTION	QTY
E1	3110719-10	LO BOY CABINET	1
E2	3111257-10	19" VERTICAL CABINET	1
E4	———	NO CABINET	—

GROUP F - VERTICAL HINGE			
CODE	PART NO.	DESCRIPTION	QTY
F1	3109889-10	VERTICAL HINGE ASSY	1
F2	———	NO VERTICAL HINGE	—

GROUP G - TAPE SPEED				
CODE	PART NO.	DESCRIPTION	LOCAT.	QTY
G1	3119593-01	PCBA, REEL SERVO 36 IPS	J7	1
	3107097-10	PCBA, CAPSTAN SERVO 36 IPS	J6	1
G2	3119594-01	PCBA, REEL SERVO 45 IPS	J7	1
	3112170-10	PCBA, CAPSTAN SERVO 45 IPS	J6	1

GROUP H - INPUT LEVELS					
CODE	LEVELS TRUE	LEVELS FALSE	PART NO.	QTY	LOCATION
H1	-12	0	3107258-10	2	B15, B16
H2	+3	0	3118170-01	3	B15
H3	+6	0	3118171-01		
H4	+9	0	3118172-01		
H5	+12	0	3118173-01		B16
H6	0	+3	3118227-01		
H7	0	+6	3118228-01		
H8	0	+9	3118229-01		B22
H9	0	+12	3118230-01		

GROUP J - OUTPUT LEVELS					
CODE	LEVELS TRUE	LEVELS FALSE	PART NO.	QTY	LOCATION
J1	-12	0	3107259-10	*2	B13, B14
J2	+3	0	3118179-01	*2	B13, B14
			3118161-01	1	B23
J3	+4	0	3118292-01	*2	B13, B14
			3118293-01	1	B23
J4	+5	0	3119588-01	*2	B13, B14
			3119589-01	1	B23
J5	+6	0	3118180-01	*2	B13, B14
			3118162-01	1	B23
J6	+8	0	3119498-01	*2	B13, B14
			3119497-01	1	B23
J7	+9	0	3118181-01	*2	B13, B14
			3118163-01	1	B23
J8	+12	0	3118182-01	*2	B13, B14
			3118164-01	1	B23
J9	0	+3	3118161-01	*2	B13, B14
			3118179-01	1	B23
J10	0	+4	3118293-01	*2	B13, B14
			3118292-01	1	B23
J11	0	+5	3119589-01	*2	B13, B14
			3119588-01	1	B23
J12	0	+6	3118162-01	*2	B13, B14
			3118180-01	1	B23
J13	0	+8	3119497-01	*2	B13, B14
			3119498-01	1	B23
J14	0	+9	3118163-01	*2	B13, B14
			3118181-01	1	B23
J15	0	+12	3118164-01	*2	B13, B14
			3118182-01	1	B23

GROUP K - STD. DATA ELECT., WRITE W/UNIDIRECTIONAL READ							
CODE	DESCRIPTION	PART NO.	SPEED	QTY 7CH	QTY 9CH	LOCATION 7 CH	LOCATION 9 CH
K1	WRITE POWER GATE	3107268-10	ALL	1	1	A24	A24
	STROBE GENERATE	3107057-10	36 & 45	1	1	B8	B8
	READ AMP	3107266-10	36 & 45	4	5	B2 THRU B5	B2 THRU B6
	WRITE AMP	3112363-10	36 & 45	7	9	A14 THRU A20	A14 THRU A22
	READ DESKEW	3107269-10 3123847-01	36 45	7	9	A2 THRU A8	A2 THRU A10

GROUP K - STD. DATA ELECT., WRITE W/ BIDIRECTIONAL READ							
CODE	DESCRIPTION	PART NO.	SPEED	QTY 7CH	QTY 9CH	LOCATION 7 CH	LOCATION 9 CH
K2	WRITE POWER GATE	3107268-10	ALL	1	1	A24	A24
	STROBE GENERATE	3107057-10	36 & 45	1	1	B8	B8
	READ AMP	3107266-10	36 & 45	4	5	B2 THRU B5	B2 THRU B6
	WRITE AMP	3112363-10	36 & 45	7	9	A14 THRU A20	A14 THRU A22
	READ DESKEW	3109932-10 3119428-01	36 45	7	9	A2 THRU A8	A2 THRU A10
	SELECT LOGIC	3111157-10	ALL	1	1	B7	B7

GROUP L - DATA ELECTRONICS OPTIONS								
CODE	OPTION	PCBA DESCRIPTION	PART NO.	SPEED	QTY 7CH	QTY 9CH	LOCATIONS 7 CH	LOCATIONS 9 CH
L1	NO OPTIONS	———	———	—	—	—	———	———
L2	ECHO & RATE	ERROR CHECK	3109872-10	36 & 45	1	1	B12	B12
L3	VERT. PARITY CHK	EXCLUSIVE OR	3107274-10	ALL	2	3	B9, B10	B9, B10, B11
L4	VERT. PARITY GEN.	EXCLUSIVE OR	3107274-10	ALL	2	2	A11, A12	A11, A12
L5	LONGIT. PARITY GEN.	LONG. PARITY GEN.	3116072-10	36 & 45	1	1	A13	A13
L6	LONGIT PARITY CHECK	LONG. PARITY REG.	3116082-10	36 & 45	1	1	B19	B19
		LPC TIMING	3116087-10	ALL	1	1	B20	B20
		FLIP FLOP	3107275-10	ALL	1	2	B17	B17, B18

3115770 - SELECT PROPER VERSION

USED W/CODES	OPTION OR FEATURE	55	01	02	03	04	05	06	07	08	09	10	13	15	17	20	22	24	25	30	31	32	33	36	37	38	39	40	41	43	46	48	49	50	56	60		
K1	UNIDIRECTIONAL READ								X			X		X		X			X	X	X	X	X	X	X	X	X	X	X	X		X	X		X	X		
K2 W/01	BIDIRECTIONAL READ W/RUN/STOP	X	X	X	X		X	X		X	X		X				X	X													X			X				
K2 W/02	BIDIRECTIONAL READ W/ FWD/STOP					X									X																							
H1, J1	-12 LEVELS	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X								X			X	X			X		
H2 TO H9 & J2 TO J15 W/01	POSITIVE LEVELS W/RUN/STOP																						X	X	X	X	X			X	X			X				
H2 TO H9 & J2 TO J15 W/02	POSITIVE LEVELS W/ FWD/STOP																					X						X							X			
L2	ECHO & RATE	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
L3	VERTICAL PARITY CHECK	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
L4	VERTICAL PARITY GEN. 7 CH.		X				X	X	X				X	X	X	X				X						X				X								
L4	VERTICAL PARITY GEN. 9 CH.			X						X								X						X				X	X			X	X	X				
L5	LONGITUDINAL PARITY GEN.						X				X		X			X	X	X	X	X	X			X	X	X		X		X		X	X	X	X			
L6	LONGITUDINAL PARITY CHECK				X			X		X	X	X	X	X	X	X			X					X			X	X		X			X	X				

⊖ WITH ITEM C4 INCLUDE ADDENDUM 3123716-01

* ONLY 1 REQD IF 7 CH. NO OPTIONS, OR 7 CH. & OPTION L4, OR L5 OR BOTH, & NO OTHER OPTIONS

NOTE: FOR TRI DENSITY SUBSTITUTE STROBE GENERATOR 3114894-10, & ADD DENSITY CONTROL 3115632-10 IN B21. FOR DATA C.C. SEE DWG 3115770

REVISIONS					
ISSUE	DESCRIPTION	DATE	DRAFTSMAN	DATE	APPROVAL
B					

NEXT ASSY.	1ST USED ON
APPLICATION	

DO NOT SCALE DRAWING
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: DECIMALS .XX± .XXX± ANGLES ±
BREAK ALL SHARP EDGES APPROX. .010. C'BORE AND SPOTFACE CORNER RADII APPROX. .010. ROUGHNESS OF ALL MACHINED SURFACES ——— PER MR-STD-10 ✓
MATERIAL
FINISH

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PROJ / SUPER / PROJ ENGR
ENGR A. WATSON 9/2/68
CHKR
DFTSMN [signature] 9/2/68

AMPEX COMPUTER PRODUCTS DIVISION P.O. BOX 329, CULVER CITY, CALIF.

TITLE MASTER PART SELECTOR, STD. TM-707, 709, 7211, 7291

SIZE D CODE IDENT. NO. 09150 DWG. NO. 3124744

SCALE SHEET

GROUP A-BASIC CONFIGURATION			
CODE	PART NO.	DESCRIPTION	QTY
A136	3124730-02	HORIZONTAL, W/LOGO, W/D.E.	1
A146	3124730-03	HORIZONTAL, W/O LOGO, W/D.E.	1
A236	3124730-04	VERTICAL. W/LOGO, W/D.E.	1
A246	3124730-05	VERTICAL, W/O LOGO, W/D.E	1
A135	3124730-06	HORIZONTAL, W/LOGO, W/O D.E.	1
A145	3124730-07	HORIZONTAL, W/O LOGO, W/O D.E.	1
A235	3124730-08	VERTICAL, W/LOGO, W/O D.E.	1
A245	3124730-09	VERTICAL, W/O LOGO, W/O D.E.	1

GROUP B - REEL RETAINERS			
CODE	PART NO.	DESCRIPTION	QTY
B1	3113100-10	IBM HOLD DOWN KNOB	1
	3101267-10	FIXED TAKE UP REEL	1
B2	3113100-10	IBM HOLD DOWN KNOB	2
	3108273-30	EMPTY REEL	1

GROUP C - HEADS			
CODE	PART NO.	DESCRIPTION	QTY
C1	3112686-10	7 CH. W/O ERASE	1
C2	3112442-10	7 CH. W/ERASE	1
C3	3112443-10	9 CH. W/ERASE (STD. IBM WIRING)	1
⊖ C4	3112443-20	9 CH. W/ERASE (SPECIAL IBM WIRING)	1

GROUP D - MOTION COMMAND				
CODE	PART NO.	DESCRIPTION	LOCAT.	QTY
D1	3119598-01	PCBA, RUN/STOP	J4	1
D2	3119529-01	PCBA, FWD/STOP	J4	1

GROUP E - CABINET			
CODE	PART NO.	DESCRIPTION	QTY
E1	3110719-10	LO BOY CABINET	1
E2	3111257-10	19" VERTICAL CABINET	1
E4	———	NO CABINET	—

GROUP F - VERTICAL HINGE			
CODE	PART NO.	DESCRIPTION	QTY
F1	3109889-10	VERTICAL HINGE ASSY	1
F2	———	NO VERTICAL HINGE	—

GROUP G — TAPE SPEED	
CODE	DESCRIPTION
G3	TAPE SPEED PCBA'S INCLUDED IN GROUP A

GROUP H - INPUT LEVELS					
CODE	LEVELS TRUE	LEVELS FALSE	PART NO.	QTY	LOCATION
H1	-12	0	3107258-01	2	B15, B16
H2	+3	0	3118170-01	3	B15
H3	+6	0	3118171-01		
H4	+9	0	3118172-01		B16
H5	+12	0	3118173-01		
H6	0	+3	3118227-01		
H7	0	+6	3118228-01		B22
H8	0	+9	3118229-01		
H9	0	+12	3118230-01		

GROUP J - OUTPUT LEVELS					
CODE	LEVEL TRUE	LEVEL FALSE	PART NO.	QTY	LOCATION
J1	-12	0	3107259-10	*2	B13, B14
J2	+3	0	3118179-01	*2	B13, B14
			3118161-01	1	B23
J3	+4	0	3118292-01	*2	B13, B14
			3118293-01	1	B23
J4	+5	0	3119588-01	*2	B13, B14
			3119589-01	1	B23
J5	+6	0	3118180-01	*2	B13, B14
			3118162-01	1	B23
J6	+8	0	3119498-01	*2	B13, B14
			3119497-01	1	B23
J7	+9	0	3118181-01	*2	B13, B14
			3118163-01	1	B23
J8	+12	0	3118182-01	*2	B13, B14
			3118164-01	1	B23
J9	0	+3	3118161-01	*2	B13, B14
			3118179-01	1	B23
J10	0	+4	3118293-01	*2	B13, B14
			3118282-01	1	B23
J11	0	+5	3119589-01	*2	B13, B14
			3119588-01	1	B23
J12	0	+6	3118162-01	*2	B13, B14
			3118180-01	1	B23
J13	0	+8	3119497-01	*2	B13, B14
			3119498-01	1	B23
J14	0	+9	3118163-01	*2	B13, B14
			3118181-01	1	B23
J15	0	+12	3118164-01	*2	B13, B14
			3118182-01	1	B23

STD DATA ELECT., WRITE W/UNIDIRECTIONAL READ							
CODE	DESCRIPTION	PART NO.	SPEED	QTY 7CH	QTY 9CH	LOCATION 7 CH	LOCATION 9 CH
K1	WRITE PWR GATE	3107268-10	ALL	1	1	A24	A24
	STROBE GENERATE	3109994-10	75	1	1	B8	B8
	READ AMP	3109991-10	75	4	5	B2 THRU B5	B2 THRU B6
	WRITE AMP	3109572-10	75	7	9	A14 THRU A20	A14 THRU A22
	READ DESKEW	3109475-10	75	7	9	A2 THRU A8	A2 THRU A10

STD DATA ELECT., WRITE W/BIDIRECTIONAL READ							
CODE	DESCRIPTION	PART NO.	SPEED	QTY 7CH	QTY 9CH	LOCATION 7 CH	LOCATION 9 CH
K2	WRITE PWR GATE	3107268-10	ALL	1	1	A24	A24
	STROBE GENERATE	3109994-10	75	1	1	B8	B8
	READ AMP	3109991-10	75	4	5	B2 THRU B5	B2 THRU B6
	WRITE AMP	3109572-10	75	7	9	A14 THRU A20	A14 THRU A22
	READ DESKEW	3109935-10	75	7	9	A2 THRU A8	A2 THRU A10
	SELECT LOGIC	3111157-10	ALL	1	1	B7	B7

GROUP L - DATA ELECTRONICS OPTIONS								
CODE	OPTION	PCBA DESCRIPTION	PART NO	SPEED	QTY 7CH	QTY 9CH	LOCATION 7 CH	LOCATION 9CH
L1	NO OPTIONS	———	———	——	—	—	———	———
L2	ECHO & RATE	ERROR CHK.	3110558-10	36 & 45	1	1	B12	B12
L3	VERT. PARITY CHK.	EXCLUSIVE OR	3107274-10	75	2	3	B9, B10	B9, B10, B11
L4	VERT. PARITY GEN.	EXCLUSIVE OR	3107274-10	75	2	2	A11, A12	A11, A12
L5	LONG. PARITY GEN.	LONG. PARITY GEN.	3116142-10	75	1	1	A13	A13
L6	LONG. PARITY CHECK	LONG. PARITY REG	3116161-10	75	1	1	B19	B19
		LPC TIMING	3116087-10	ALL	1	1	B20	B20
		FLIP FLOP	3107275-10	ALL	1	2	B17	B17, B18

3115770 - SELECT PROPER VERSION

USED W/CODES	OPTION OR FEATURE	55	01	02	03	04	05	06	07	08	09	10	13	15	17	20	22	24	25	30	31	32	33	36	37	38	39	40	41	43	46	48	49	50	56	60		
K1	UNIDIRECTIONAL READ								X			X		X		X			X	X	X	X	X	X	X	X	X	X	X	X		X	X		X	X		
K2 W/D1	BI DIRECTIONAL READ W/RUN/STOP	X	X	X	X		X	X		X	X		X				X	X													X			X				
K2 W/D2	BI DIRECTIONAL READ W/FWD/STOP					X									X																							
H1, J1	-12 LEVELS	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X								X			X	X			X		
H2 TO H9 & J2 TO J15 W/D1	POSITIVE LEVELS W/RUN/STOP																						X	X	X	X	X			X	X			X				
H2 TO H9 & J2 TO J15 W/D2	POSITIVE LEVELS W/FWD/STOP																					X						X							X			
L2	ECHO & RATE	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
L3	VERTICAL PARITY CHECK	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
L4	VERTICAL PARITY GEN. 7 CH		X				X	X	X				X	X	X	X				X						X				X								
L4	VERTICAL PARITY GEN. 9 CH			X						X								X						X				X	X			X	X	X				
L5	LONGITUDINAL PARITY GEN						X				X		X			X	X	X	X	X	X			X	X	X		X		X		X	X	X	X			
L6	LONGITUDINAL PARITY CHECK				X			X		X	X	X	X	X	X	X			X					X			X	X		X			X	X				

⊖ WITH ITEM C4 INCLUDE ADDENDUM 3123716-01

* ONLY ONE REQUIRED IF 7 CH. NO OPTIONS, OR 7 CH & OPTION L4 OR L5 OR BOTH, & NO OTHER OPTIONS.

NOTE: FOR TRI DENSITY SUBSTITUTE STROBE GENERATOR 3114897-10, AND ADD DENSITY CONTROL 3115632-10 IN B21. FOR DATA CC. SEE DWG 3115770

REVISIONS					
ISSUE	DESCRIPTION	DATE	DRAFTSMAN	DATE	APPROVAL
B					

NEXT ASSY.	1ST USED ON
APPLICATION	

DO NOT SCALE DRAWING
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
DECIMALS TOLERANCES ANGLES
.XX± .XXX± ±
BREAK ALL SHARP EDGES APPROX. .010. C'BORE AND SPOTFACE CORNER RADII APPROX. .010.
ROUGHNESS OF ALL MACHINED SURFACES —— PER MIL-STD-10 ✓
MATERIAL
FINISH

THE INFORMATION HEREON IS THE PROPERTY OF AMPEX COMPUTER PRODUCTS DIVISION. NO REPRODUCTION OR UNAUTHORIZED USE IN PART OR IN WHOLE SHALL BE MADE WITHOUT WRITTEN CONSENT OF AMPEX COMPUTER PRODUCTS DIV.

PROJ SUPER
PROJ ENGR
ENGR Dulatson 5-3-68
CHKR
DFTSMN [signature] 5-1-68

AMPEX COMPUTER PRODUCTS DIVISION P.O. BOX 329, CULVER CITY, CALIF.

TITLE MASTER PART SELECTOR STD. TM-907, 909, 9211, 9291

SIZE D | CODE IDENT. NO. 09150 | DWG. NO. 3124745
SCALE | SHEET

REVISIONS					
ISSUE	DESCRIPTION	DATE	DRAFTSMAN	DATE	APPROVAL
B					

GROUP A - BASIC CONFIGURATION - TM 11

CODE	PART NO.	DESCRIPTION	QTY
A236	3118770-02	VERTICAL, W/LOGO, W/ D.E.	1
A246	3118770-02	VERTICAL (REMOVE LOGO) W/D.E.	1
A235	3118770-03	VERTICAL, W/LOGO, W/O D.E.	1
A245	3118770-03	VERTICAL, (REMOVE LOGO) W/O D.E.	1

GROUP A - BASIC CONFIGURATION - TM 12

CODE	PART NO.	DESCRIPTION	QTY
A236	3118770-06	VERTICAL, W/LOGO, W/ D.E.	1
A246	3118770-06	VERTICAL, (REMOVE LOGO) W/D.E.	1
A235	3118770-07	VERTICAL, W/LOGO, W/O D.E.	1
A245	3118770-07	VERTICAL, (REMOVE LOGO), W/O D.E.	1

GROUP B - REEL RETAINERS

CODE	PART NO	DESCRIPTION	QTY
B1	3113100-10	IBM HOLD DOWN KNOB	1
	3101267-10	FIXED TAKE UP REEL	1
B2	3113100-10	IBM HOLD DOWN KNOB	2
	3108273-30	EMPTY REEL	1

GROUP C - HEADS - TM-11

CODE	PART NO.	DESCRIPTION	QTY
C1	3110206-30	7 CH. W/O ERASE	1
C2	3110213-30	7 CH. W/ERASE	1
C3	3112721-20	9 CH. W/ERASE (STD. IBM WIRING)	1
⊖ C4	3112721-50	9 CH. W/ERASE (SPECIAL IBM WIRING)	1

GROUP C - HEADS - TM-12

CODE	PART NO.	DESCRIPTION	QTY
C1	3110206-50	7 CH. W/O ERASE	1
C2	3110213-50	7 CH. W/ ERASE	1
C3	3112721-40	9 CH. W/ERASE (STD. IBM WIRING)	1
⊖ C4	3112721-60	9 CH. W/ERASE (SPECIAL IBM WIRING)	1

GROUP D - MOTION COMMAND

CODE	PART NO.	DESCRIPTION	LOCAT.	QTY
D1	3107082-10	PCBA. RUN / STOP	J4	1
D2	3112360-10	PCBA, FWD / STOP	J4	1

GROUP E - CABINET

CODE	PART NO.	DESCRIPTION	QTY
E3	3112647-10	24" VERTICAL CABINET	1
E4	———	NO VERTICAL HINGE	1

GROUP G - TAPE SPEED

CODE	DESCRIPTION
G3 THRU G6	TAPE SPEED PCBA'S INCLUDED IN GROUP A

GROUP H - INPUT LEVELS

CODE	LEVELS TRUE	LEVELS FALSE	PART NO.	QTY	LOCATION
H1	-12	0	3107258-10	2	B15, B16
H2	+3	0	3118170-01	3	B15
H3	+6	0	3118171-01		
H4	+9	0	3118172-01		
H5	+12	0	3118173-01		B16
H6	0	+3	3118227-01		
H7	0	+6	3118228-01		B22
H8	0	+9	3118229-01		
H9	0	+12	3118230-01		

GROUP J - OUTPUT LEVELS

CODE	LEVELS TRUE	LEVELS FALSE	PART NO.	QTY	LOCATION
J1	-12	0	3107259-10	*2	B13, B14
J2	+3	0	3118179-01	*2	B13, B14
			3118161-01	1	B23
J3	+4	0	3118292-01	*2	B13, B14
			3118293-01	1	B23
J4	+5	0	3119588-01	*2	B13, B14
			3119589-01	1	B23
J5	+6	0	3118180-01	*2	B13, B14
			3118162-01	1	B23
J6	+8	0	3119498-01	*2	B13, B14
			3119497-01	1	B23
J7	+9	0	3118181-01	*2	B13, B14
			3118163-01	1	B23
J8	+12	0	3118182-01	*2	B13, B14
			3118164-01	1	B23
J9	0	+3	3118161-01	*2	B13, B14
			3118179-01	1	B23
J10	0	+4	3118293-01	*2	B13, B14
			3118292-01	1	B23
J11	0	+5	3119589-01	*2	B13, B14
			3119588-01	1	B23
J12	0	+6	3118162-01	*2	B13, B14
			3118180-01	1	B23
J13	0	+8	3119497-01	*2	B13, B14
			3119498-01	1	B23
J14	0	+9	3118163-01	*2	B13, B14
			3118181-01	1	B23
J15	0	+12	3118164-01	*2	B13, B14
			3118182-01	1	B23

GROUP K - STD PCBA'S UNIDIRECTIONAL READ

CODE	DESCRIPTION	PART NO.	SPEEDS	QTY 7CH	QTY 9CH	LOCATIONS 7 CH	LOCATIONS 9 CH
K1	WRITE POWER GATE	3107268-10	ALL	1	1	A24	A24
	STROBE GENERATOR	3109994-10	75	1	1	B8	B8
		3110003-10	112.5/120				
		3118218-01	150				
	READ AMPLIFIER	3109991-10	75	4	5	B2 THRU B5	B2 THRU B6
		3110273-10	112.5/120				
		3118138-01	150				
	WRITE AMPLIFIER	3109572-01	75	7	9	A14 THRU A20	A14 THRU
		3110002-10	112.5 120/150				
	READ DESKEW	3109475-10	75	7	9	A2 THRU A8	A2 THRU A10
		3110004-10	112.5 120/150				

GROUP K - STD PCBA'S BIDIRECTIONAL READ

CODE	DESCRIPTION	PART NO	SPEEDS	QTY 7CH	QTY 9CH	LOCATIONS 7 CH	LOCATIONS 9 CH
K2	WRITE POWER GATE	3107268-10	ALL	1	1	A24	A24
	STROBE GENERATOR	3109994-10	75	1	1	B8	B8
		3110003-10	112.5/120				
		3118218-10	150				
	READ AMPLIFIER	3109991-10	75	4	5	B2 THRU B5	B2 THRU B6
		3110273-10	112.5/120				
		3118138-10	150				
	WRITE AMPLIFIER	3109572-10	75	7	9	A14 THRU A20	A14 THRU A22
		3110002-10	112.5 120/150				
	READ DESKEW	3109935-10	75	7	9	A2 THRU A8	A2 THRU A10
		3109936-10	112.5 120/150				
	SELECT LOGIC	3111157-10	ALL	1	1	B7	B7

GROUP L - DATA ELECTRONICS OPTIONS

CODE	OPTION	PCBA DESCRIPTION	PART NO.	SPEED	QTY 7CH.	QTY 9CH	LOCATIONS 7 CH.	LOCATIONS 9 CH.
L1	NO OPTIONS	——	——	—	—	—	——	——
L2	ECHO AND RATE	ERROR CHECK	3110558-10	75	1	1	B12	B12
		ERROR CHECK	3110031-10	112.5 120/150				
L3	VERT. PARITY CHK	EXCLUSIVE OR	3107274-10	ALL	2	3	B9, B10	B9, B10, B11
L4	VERT. PARITY GEN	EXCLUSIVE OR	3107274-10	ALL	2	2	A11, A12	A11, A12
L5	LONGITUDINAL PARITY GENERATE	LONG. PAR. GEN	3116142-10	75	1	1	A13	A13
		LONG. PAR. GEN	3116073-10	112.5 120/150				
L6	LONGITUDINAL PARITY CHECK	LONG. PAR. REG.	3116161-10	75	1	1	B19	B19
		LONG. PAR. REG.	3116162-10	112.5 120/150				
		LPC TIMING	3116087-10	ALL	1	1	B20	B20
		FLIP FLOP	3107275-10	ALL	1	2	B17	B17, B18

3115770 - SELECT PROPER VERSION

USED WITH CODES	OPTION OR FEATURE	55	01	02	03	04	05	06	07	08	09	10	13	15	17	20	22	24	25	30	31	32	33	36	37	38	39	40	41	43	46	48	49	50	56	60		
K1	UNIDIRECTIONAL READ								X			X		X		X			X	X	X	X	X	X	X	X	X	X	X	X		X	X		X	X		
K2 W/ D1	BI-DIRECTIONAL READ W/RUN/STOP	X	X	X	X		X	X		X	X		X				X	X													X			X				
K2 W/D2	BI-DIRECTIONAL READ W/FWD/STOP					X									X																							
H1, J1	-12 LEVELS	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X								X			X	X			X		
H2 TO H9 & J2 TO J15 W/D1	POSITIVE LEVELS W/RUN / STOP																						X	X	X	X	X			X	X			X				
H2 TO H9 & J2 TO J15 W/D2	POSITIVE LEVELS W/ FWD/ STOP																					X						X							X			
L2	ECHO & RATE	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
L3	VERTICAL PARITY CHECK	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
L4	VERTICAL PARITY GEN. 7 CH		X				X	X	X				X	X	X	X				X						X				X								
L4	VERTICAL PARITY GEN. 9 CH			X						X								X						X				X	X			X	X	X				
L5	LONGITUDINAL PARITY GEN.						X				X		X			X	X	X	X	X	X			X	X	X		X		X		X	X	X	X			
L6	LONGITUDINAL PARITY CHECK				X			X		X	X	X	X	X	X	X			X					X			X	X		X			X	X				

⊖ WITH ITEM C4 INCLUDE ADDENDUM 3123716-01

* ONLY ONE REQUIRED IF 7 CHANNEL NO OPTIONS OR 7 CHANNEL AND OPTION L4 OR L5 OR BOTH AND NO OTHER OPTIONS.

NOTE: FOR TRI DENSITY SUBSTITUTE ONE OF THE FOLLOWING STROBE GENERATORS. 75 IPS 3114897-10, 112.5 OR 120 IPS 3115626-10, 150 IPS 3118278-01, AND ADD DENSITY CONTROL 3115632-10 IN B21. FOR DATA C.C. SEE DWG. 3115770

NEXT ASSY.	1ST USED ON
APPLICATION	

DO NOT SCALE DRAWING

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

TOLERANCES: DECIMALS .XX± .XXX± ANGLES ±

BREAK ALL SHARP EDGES APPROX. .010. C'BORE AND SPOTFACE CORNER RADII APPROX. .010. ROUGHNESS OF ALL MACHINED SURFACES —— PER MIL-STD-10 ✓

MATERIAL

FINISH

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PROJ SUPER		
PROJ ENGR		
ENGR	D. Watson	5-3-68
CHKR		
DFTSMN	[signature]	5-1-68

AMPEX COMPUTER PRODUCTS DIVISION P.O. BOX 329, CULVER CITY, CALIF.

TITLE: MASTER PART SELECTOR STD. TM-1107, 1109, 11211, 11291 STD. TM-1207, 1209, 12211, 12291

SIZE	CODE IDENT. NO.	DWG. NO.
D	09150	3124746
SCALE		SHEET

REVISIONS

ISSUE	DESCRIPTION	DATE	DRAFTSMAN	DATE	APPROVAL
A	106-RY	2/29/68	Jw	2/29/68	Addington

Slot	A	B
1		
2	RD READ DESKEW (TRACK 1)	RA READ AMPLIFIER (TRACK 1)
3	RD (TRACK 2)	RA (TRACKS 2 & 3)
4	RD (TRACK 3)	RA (TRACKS 4 & 5)
5	RD (TRACK 4)	RA (TRACKS 6 & 7)
6	RD (TRACK 5)	RA *READ AMPLIFIER (TRACKS 8 & 9)
7	RD (TRACK 6)	SL SELECT LOGIC
8	RD (TRACK 7)	SG STROBE GENERATOR
9	RD *READ DESKEW (TRACK 8)	EO ΦEXCLUSIVE OR
10	RD *READ DESKEW (TRACK 9)	EO ΦEXCLUSIVE OR
11	EO +EXCLUSIVE OR	EO Φ*EXCLUSIVE OR
12	EO +EXCLUSIVE OR	EC ERROR CHECK
13	PG LONG. PARITY GENERATE	OD OUTPUT DRIVER
14	WA WRITE AMPLIFIER (TRACK 1)	OD OUTPUT DRIVER
15	WA (TRACK 2)	IB INPUT BUFFER
16	WA (TRACK 3)	IB INPUT BUFFER
17	WA (TRACK 4)	FF FLIP FLOP
18	WA (TRACK 5)	FF *FLIP FLOP
19	WA (TRACK 6)	PR LONG. PARITY REGISTER
20	WA (TRACK 7)	LP LPC TIMING
21	WA *WRITE AMPLIFIER (TRACK 8)	DC DENSITY CONTROL
22	WA *WRITE AMPLIFIER (TRACK 9)	IB △INPUT BUFFER
23		OD △OUTPUT DRIVER
24	WP WRITE POWER GATE	

DWG. NO. 3124747

* ADDITIONAL LOCATIONS FOR 9 TRACK QUANTITIES

\+ VERTICAL PARITY GENERATE OPTION

Φ VERTICAL PARITY CHECK OPTION

△ LOCATION OF ADDITIONAL PCBA REQD WITH POSITIVE LOGIC LEVELS

DO NOT SCALE DRAWING
UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES
DECIMALS .XX± .XXX± ANGLES ±
BREAK ALL SHARP EDGES APPROX. .010. C'BORE AND SPOTFACE CORNER RADII APPROX. .010.
ROUGHNESS OF ALL MACHINED SURFACES — PER MIL-STD-10 ✓
MATERIAL
FINISH

NEXT ASSY. | 1ST USED ON
APPLICATION

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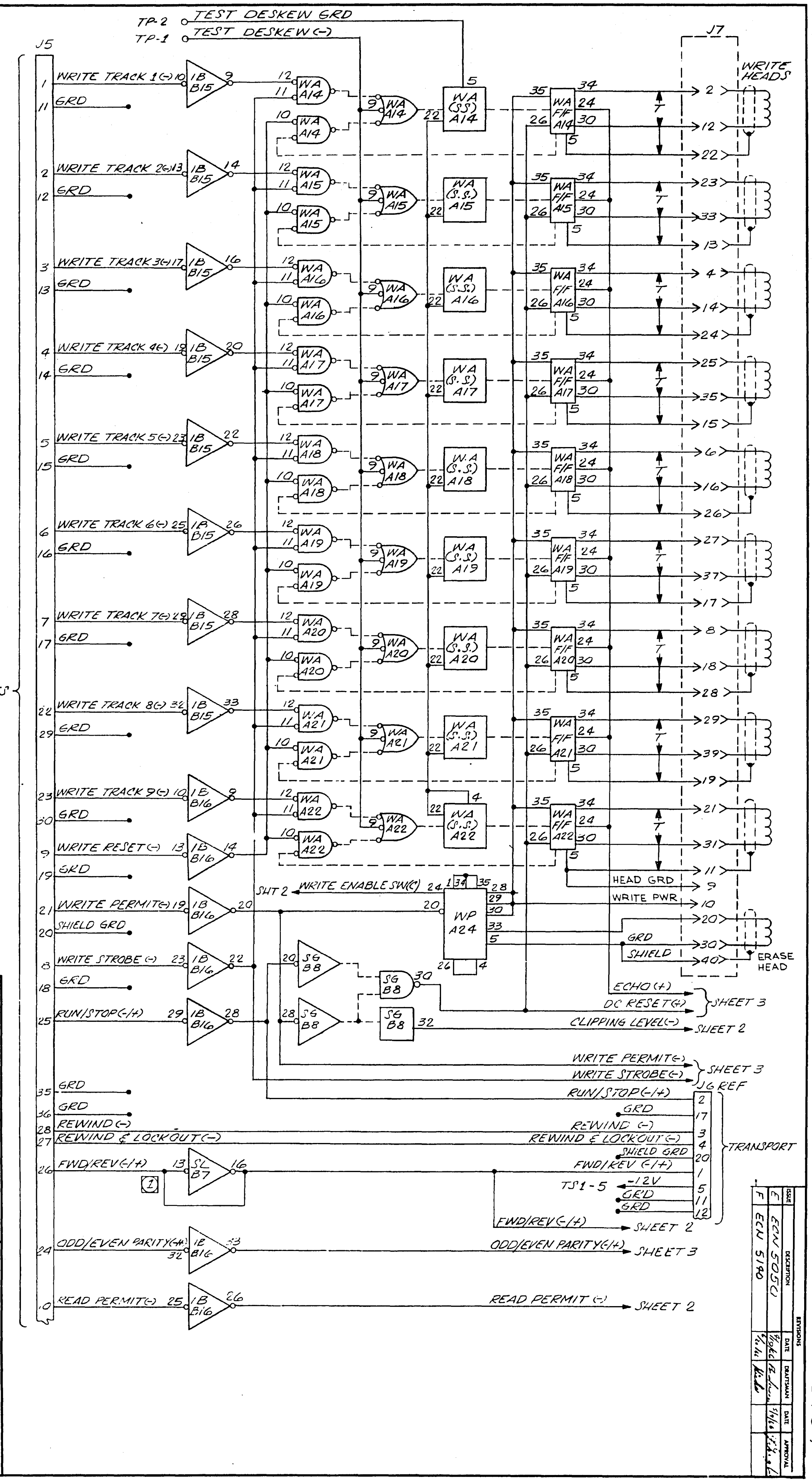
PROJ SUPER
PROJ ENGR Addington 7/28/68
ENGR [signature] 2/13/68
CHKR
DFTSMN

AMPEX COMPUTER PRODUCTS DIVISION P.O. BOX 329, CULVER CITY, CALIF.

TITLE CARD LOCATION CHART DATA ELECTRONICS DE-211, DE-291

SIZE C | CODE IDENT. NO. 09150 | DWG. NO. 3124747
SCALE | SHEET



TP-2 TEST DESKEW GRD
TP-1 TEST DESKEW (-)
J5
J7
WRITE HEADS
WRITE TRACK 1(-)
WRITE TRACK 2(-)
WRITE TRACK 3(-)
WRITE TRACK 4(-)
WRITE TRACK 5(-)
WRITE TRACK 6(-)
WRITE TRACK 7(-)
WRITE TRACK 8(-)
WRITE TRACK 9(-)
GRD
WRITE RESET(-)
WRITE PERMIT(-)
SHIELD GRD
WRITE STROBE (-)
RUN/STOP(-/+)
CUSTOMER INPUTS
REWIND (-)
REWIND & LOCKOUT(-)
FWD/REV(-/+)
ODD/EVEN PARITY(-/+)
READ PERMIT(-)
SHT 2 WRITE ENABLE SW(C)
WP A24
HEAD GRD
WRITE PWR
SHIELD
ERASE HEAD
ECHO (+)
DC RESET(+)
SHEET 3
CLIPPING LEVEL(-)
SHEET 2
WRITE PERMIT(-)
WRITE STROBE(-)
SHEET 3
RUN/STOP(-/+)
J6 REF
TRANSPORT
TS1-5
-12V
FWD/REV (-/+)
SHEET 2
ODD/EVEN PARITY(-/+)
SHEET 3
READ PERMIT (-)
SHEET 2

NOTES:
1. ON READ FWD ONLY SYSTEMS B7 IS OMITTED & JUMPERS B7-31 TO B7-4 AND B7-13 TO B7-16 ARE ADDED.
2. FOR UNSTROBED OUTPUTS REMOVE WIRE FROM B13-31 TO B13-34. ADD WIRE FROM B13-31 TO B13-5.

NEXT ASSY.	1ST USED ON
315770	TM-7211
312460	TM-7211

APPLICATION

DO NOT SCALE DRAWING

REVISIONS				
ISSUE	DESCRIPTION	DATE	DRAFTSMAN	APPROVAL
E	ECN 5050			
F	ECN 5190			

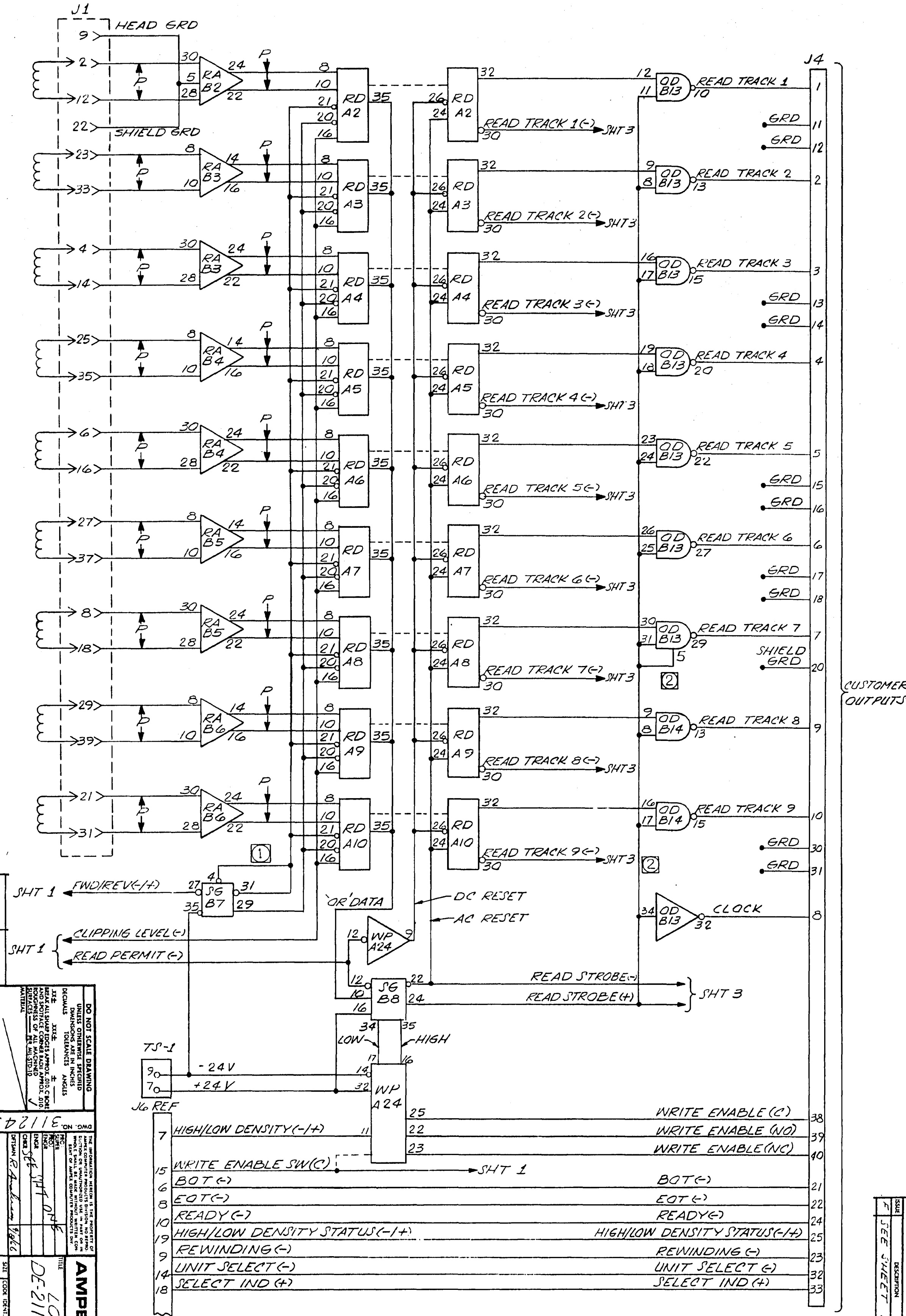
AMPEX COMPUTER PRODUCTS DIVISION P.O. BOX 329, CULVER CITY, CALIF.

TITLE: LOGIC DIAGRAM- DF-211 DATA ELECTRONICS

SIZE: D CODE IDENT. NO.: 09150 DWG. NO.: 312457

SCALE: NONE SHEET 1 OF 3

312457


J1
HEAD GRD
SHIELD GRD
RA B2
RA B3
RA B4
RA B5
RA B6
RD A2
RD A3
RD A4
RD A5
RD A6
RD A7
RD A8
RD A9
RD A10
OD B13
OD B14
READ TRACK 1
READ TRACK 2
READ TRACK 3
READ TRACK 4
READ TRACK 5
READ TRACK 6
READ TRACK 7
READ TRACK 8
READ TRACK 9
READ TRACK 1(-) SHT 3
READ TRACK 2(-) SHT 3
READ TRACK 3(-) SHT 3
READ TRACK 4(-) SHT 3
READ TRACK 5(-) SHT 3
READ TRACK 6(-) SHT 3
READ TRACK 7(-) SHT 3
READ TRACK 8(-) SHT 3
READ TRACK 9(-) SHT 3
GRD
SHIELD GRD
J4
CUSTOMER OUTPUTS
SHT 1 FWD/REV(-/+)
SG B7
'OR' DATA
DC RESET
AC RESET
WP A24
CLOCK
SHT 1 CLIPPING LEVEL(-)
READ PERMIT(-)
SG B8
READ STROBE(-)
READ STROBE(+)
SHT 3
LOW
HIGH
TS-1
-24V
+24V
J6 REF
HIGH/LOW DENSITY(-/+)
WRITE ENABLE SW(C)
SHT 1
WRITE ENABLE (C)
WRITE ENABLE (NO)
WRITE ENABLE (NC)
BOT(-)
EOT(-)
READY(-)
HIGH/LOW DENSITY STATUS(-/+)
REWINDING(-)
UNIT SELECT(-)
SELECT IND(+)

SEE SHT ONE — NEXT ASSY. — USED ON — APPLICATION

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DWG. NO. 3112457

DFTSMN R. A. [illegible] 9/66

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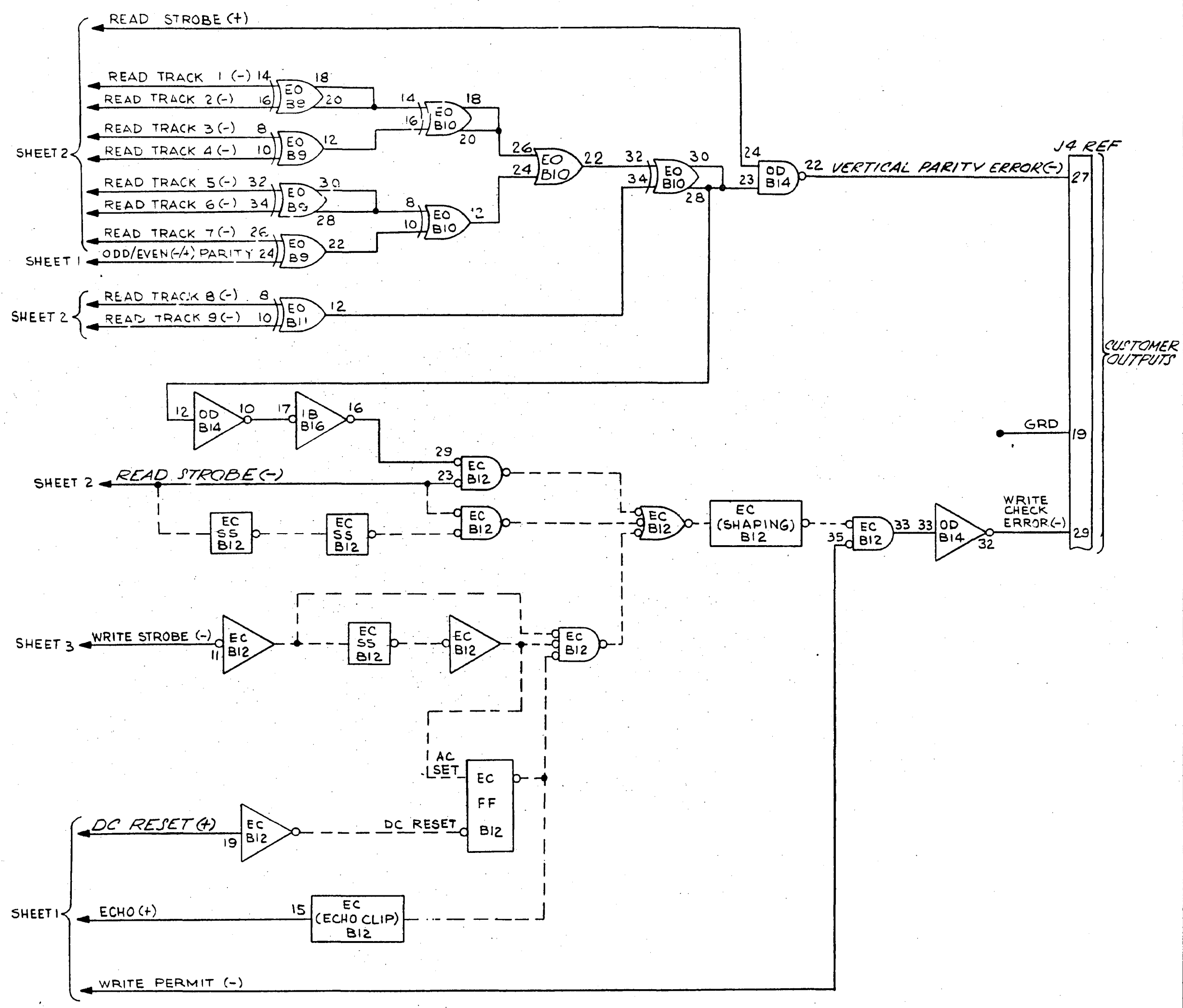
TITLE: LOGIC DIAGRAM- DE-211 DATA ELECTRONICS

SIZE D — CODE IDENT. NO. 09150 — DWG. NO. 3112457

SCALE NONE — SHEET 2 OF 3

REVISIONS

ISSUE	DESCRIPTION	DATE	DRAFTSMAN	DATE	APPROVAL
F	SEE SHEET 1				


READ STROBE (+)
READ TRACK 1 (-)
READ TRACK 2 (-)
READ TRACK 3 (-)
READ TRACK 4 (-)
READ TRACK 5 (-)
READ TRACK 6 (-)
READ TRACK 7 (-)
ODD/EVEN (-/+) PARITY
READ TRACK 8 (-)
READ TRACK 9 (-)
SHEET 2
SHEET 1
SHEET 2
EO B9
EO B10
EO B11
OD B14
VERTICAL PARITY ERROR (-)
J4 REF
CUSTOMER OUTPUTS
GRD
OD B14
IB B16
SHEET 2
READ STROBE (-)
EC B12
EC SS B12
EC (SHAPING) B12
WRITE CHECK ERROR (-)
SHEET 3
WRITE STROBE (-)
AC SET
EC FF B12
DC RESET (+)
DC RESET
SHEET 1
ECHO (+)
EC (ECHO CLIP) B12
WRITE PERMIT (-)

ISSUE	DESCRIPTION	DRAFTSMAN	DATE	APPROVAL
F	SEE SHEET 1			

SEE SHEET 1

NEXT ASSY. | 1ST USED ON

APPLICATION

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MATERIAL

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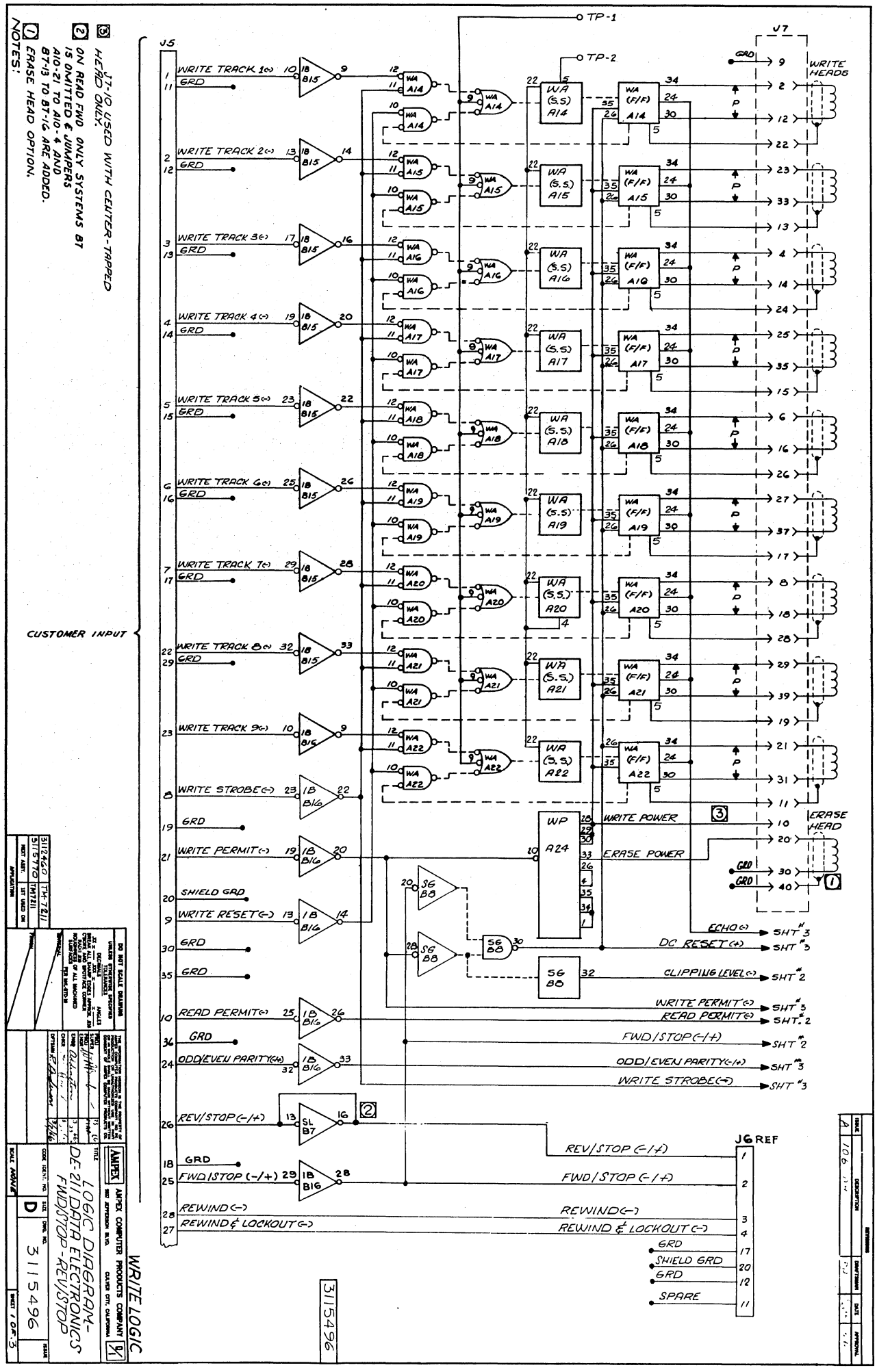
ERROR CHECK OPTION

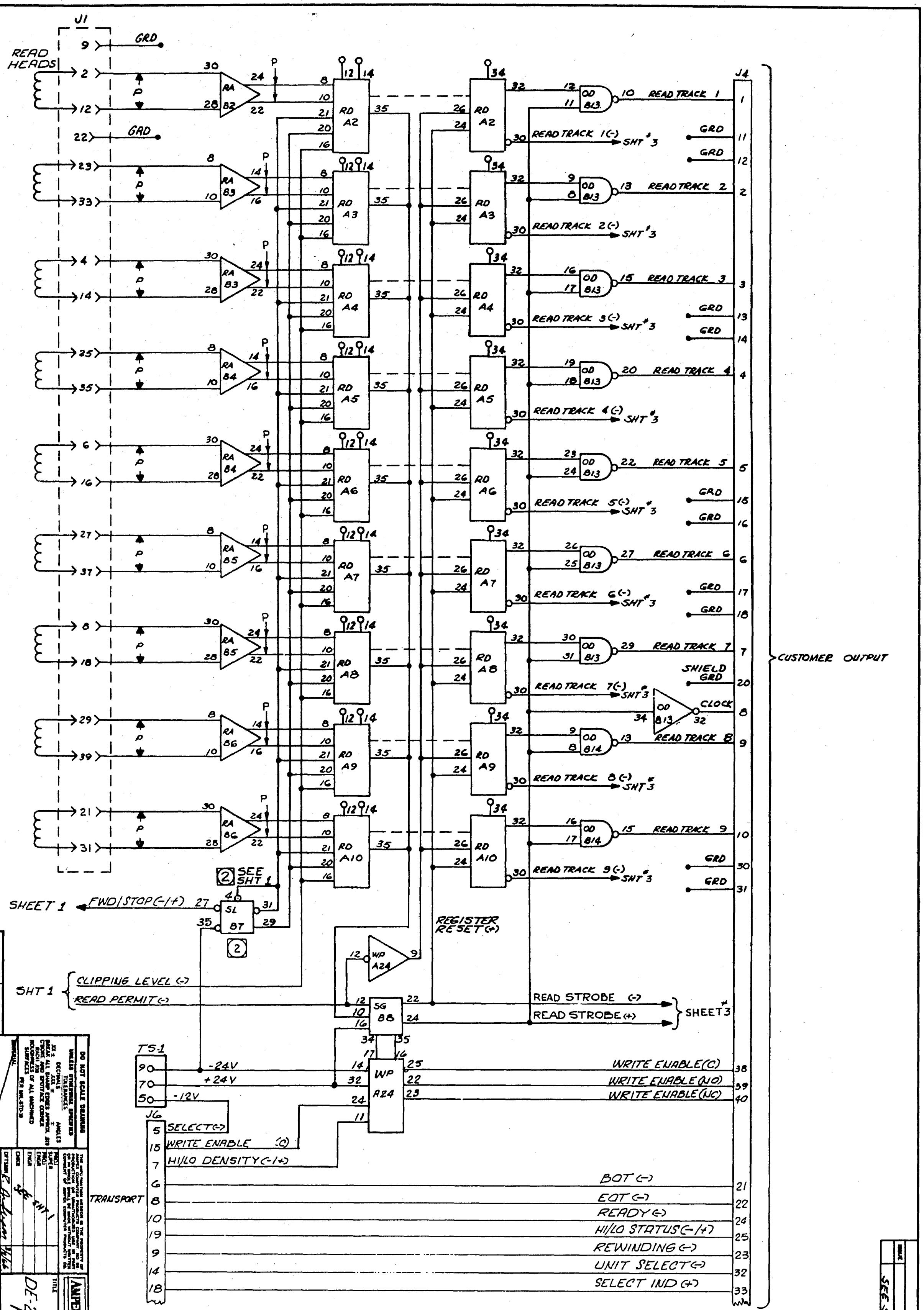
TITLE LOGIC DIAGRAM- DE-21 DATA ELECTRONICS

SIZE D | DWG. NO. 3112457 | ISSUE F

SCALE NONE | SHEET 3 OF 3

3112457


NOTES:
1. ERASE HEAD OPTION.
2. ON READ FWD ONLY SYSTEMS BT 15 OMITTED & JUMPERS A10-21 TO A10-4 AND B7-13 TO B7-16 ARE ADDED.
3. J7-10 USED WITH CENTER-TAPPED HEAD ONLY.
CUSTOMER INPUT
J5
J7
TP-1
TP-2
WRITE TRACK 1(-)
WRITE TRACK 2(-)
WRITE TRACK 3(-)
WRITE TRACK 4(-)
WRITE TRACK 5(-)
WRITE TRACK 6(-)
WRITE TRACK 7(-)
WRITE TRACK 8(-)
WRITE TRACK 9(-)
WRITE STROBE(-)
WRITE PERMIT(-)
SHIELD GRD
WRITE RESET(-)
READ PERMIT(-)
ODD/EVEN PARITY(+/-)
REV/STOP(-/+)
FWD/STOP(-/+)
REWIND(-)
REWIND & LOCKOUT(-)
GRD
WRITE HEADS
ERASE HEAD
WRITE POWER
ERASE POWER
ECHO(-)
DC RESET(+)
CLIPPING LEVEL(-)
WRITE PERMIT(-)
READ PERMIT(-)
FWD/STOP(-/+)
ODD/EVEN PARITY(-/+)
WRITE STROBE(-)
REV/STOP(-/+)
FWD/STOP(-/+)
REWIND(-)
REWIND & LOCKOUT(-)
J6 REF
GRD
SHIELD GRD
GRD
SPARE
WRITE LOGIC
DE-211 DATA ELECTRONICS
FWD/STOP-REV/STOP
AMPEX COMPUTER PRODUCTS COMPANY
3115496


J1
READ HEADS
GRD
RA
RD
OD
READ TRACK 1
READ TRACK 2
READ TRACK 3
READ TRACK 4
READ TRACK 5
READ TRACK 6
READ TRACK 7
READ TRACK 8
READ TRACK 9
READ TRACK 1(-)
READ TRACK 2(-)
READ TRACK 3(-)
READ TRACK 4(-)
READ TRACK 5(-)
READ TRACK 6(-)
READ TRACK 7(-)
READ TRACK 8(-)
READ TRACK 9(-)
SHT # 3
J4
CUSTOMER OUTPUT
SHIELD GRD
CLOCK
SEE SHT 1
SHEET 1
FWD/STOP(-/+)
SL
REGISTER RESET(+)
WP
SHT 1
CLIPPING LEVEL (-)
READ PERMIT(-)
SG
READ STROBE (-)
READ STROBE (+)
SHEET 3
TS-1
-24V
+24V
-12V
J6
SELECT(-)
WRITE ENABLE (C)
HI/LO DENSITY(-/+)
TRANSPORT
WRITE ENABLE(C)
WRITE ENABLE(NO)
WRITE ENABLE(NC)
BOT(-)
EOT(-)
READY(-)
HI/LO STATUS(-/+)
REWINDING(-)
UNIT SELECT(-)
SELECT IND(+)

SEE SHEET 1

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READ LOGIC

LOGIC DIAGRAM-
DE-21 DATA ELECTRONICS
FWD/STOP-REV/STOP

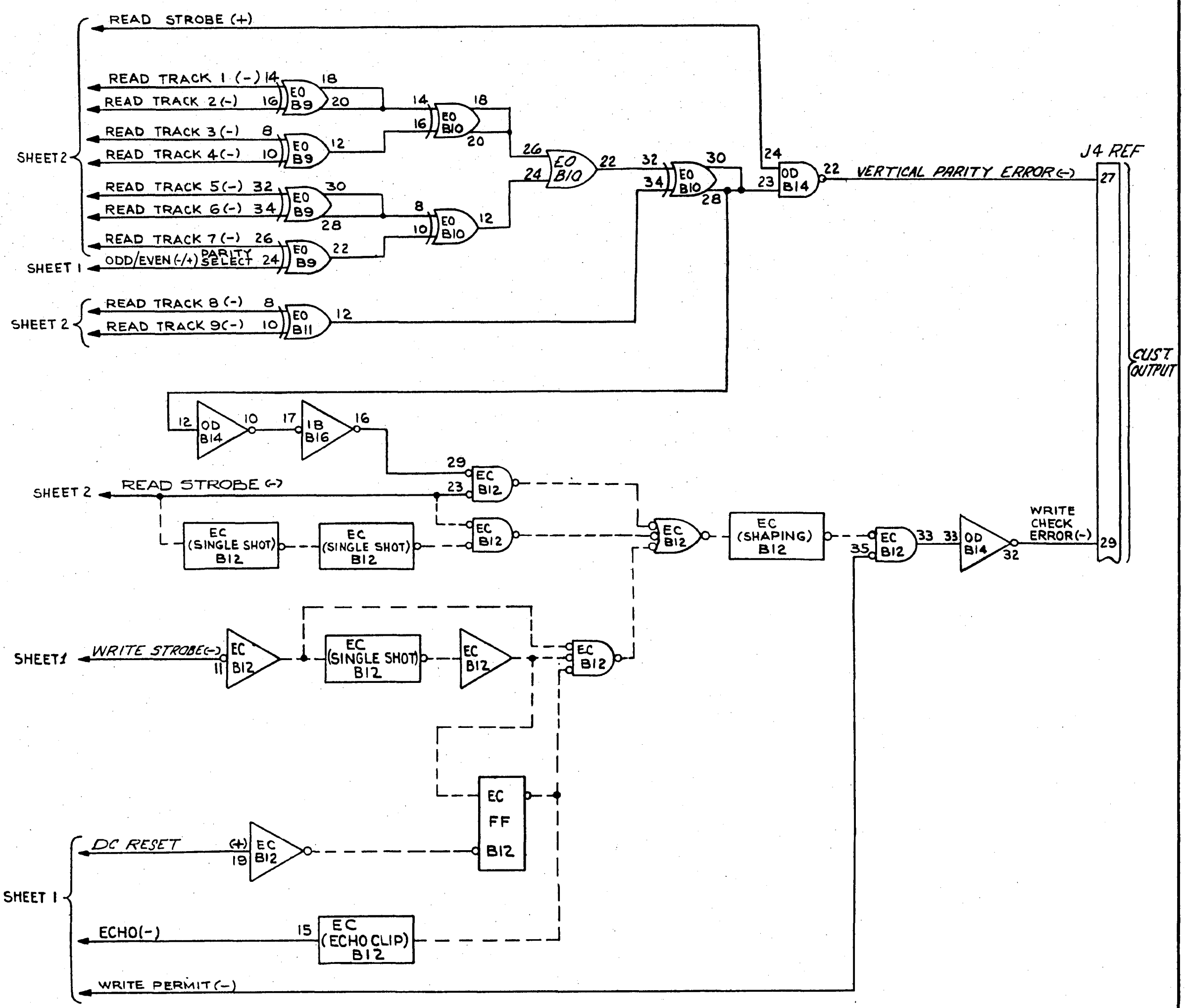
D 3115496

SCALE NONE

SHEET 2 OF 3

3115496

SEE SHEET 1



SEE SHEET I

NEXT ASSY. | 1ST USED ON
APPLICATION

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MATERIAL

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TITLE LOGIC DIAGRAM- DF-211 DATA ELECTRONICS FWD/STOP-REV/STOP

SIZE D DWG. NO. 3115496

SCALE NONE SHEET 3 OF 3

ISSUE | DESCRIPTION | REVISIONS | DRAFTSMAN | DATE | APPROVAL

SEE SHEET I

3115496

SECTION VIII
SPECIAL FEATURES

8-1. INTRODUCTION.

This section documents the changes made in the data electronics to provide the special features listed in Table 8-1. The special feature descriptions are in alphanumeric sequence by the codes listed in Table 8-1. Schematic diagrams and assembly drawings of the PCB assemblies listed in the special feature descriptions are located in Section VII. The logic diagrams applicable to each special feature are located with the special feature description.

TABLE 8-1
DATA ELECTRONICS SPECIAL FEATURES

CODE	DESCRIPTION
SF1	Special Positive Input/Output Levels (Dual Density)
SF2	Vertical Parity Generate (7 Track)
SF3	Vertical Parity Generate (9 Track)
SF4	Longitudinal Parity Check
SF5	Longitudinal Check Character Generate

SPECIAL FEATURE (SF1)
SPECIAL POSITIVE INPUT/OUTPUT LEVELS
(DUAL DENSITY)

INTRODUCTION.

The standard Input Buffer and Output Driver printed circuit board (PCB) assemblies in the data electronics are replaced with special PCB assemblies in systems which require positive input/output levels. The data electronics assembly is wired as shown in the applicable data electronics logic diagram (3118315 for run/stop logic, 3118325 for forward/stop logic).

GENERAL DESCRIPTION.

The signal levels for the input buffers and the output drivers are selected to meet the system requirements. Table 1 lists typical IBT input buffers used at the various input levels. Table 2 lists typical output drivers used at the various output levels. The ODL and ODM output driver PCB assemblies are used for both 0 volt FALSE and 0 volt TRUE system outputs. When the system output is 0 volts FALSE, ODL output driver PCB assemblies are used in locations B13 and B14 of the data electronics and an ODM output driver PCB is used in location B23. When the system output is 0 volts TRUE, ODM output driver PCB assemblies are used in locations B13 and B14 and an ODL output driver PCB is used in location B23.

DRAWINGS.

The schematic diagrams and assembly drawings of the PCB assemblies are located in Section VII. The logic diagrams are located at the end of this special feature description.

APPLICABLE PRINTED CIRCUIT BOARD DRAWINGS

CODE	DESCRIPTION	SCHEMATIC	ASSY DWG
IBT	Input Buffer	3118175	3118174
ODL	Output Driver	3118184	3118183
ODM	Output Driver	3118166	3118165

LOGIC DIAGRAM

DE-211 Data Electronics, Positive Levels	
Run/Stop	3118315
Forward/Stop	3118325

The logic diagrams are intended for use with systems using either a positive TRUE level and a negative or ground FALSE level or a positive FALSE level and a negative or ground TRUE level. For this reason, state indicators have been omitted from the input buffer inputs and the output driver outputs. State indicators for all other signal levels are as shown in the logic diagram.

TABLE 1
POSITIVE LEVEL INPUT BUFFERS

CODE	LEVEL (VOLTS)		PART NO.	SCHEMATIC	ASSY DWG
	TRUE	FALSE			
IBT	+3	0	3118170-01	3118175	3118174
↑	+6	0	3118171-01	↑	↑
	+9	0	3118172-01		
	+12	0	3118173-01		
	0	+3	3118227-01		
	0	+6	3118228-01		
↓	0	+9	3118229-01	↓	↓
IBT	0	+12	3118230-01	3118175	3118174

TABLE 2
POSITIVE LEVEL OUTPUT DRIVERS

CODE	LEVEL (VOLTS)		PART NO.	SCHEMATIC	ASSY DWG
	TRUE*	FALSE*			
ODL	+3	0	3118179-01	3118184	3118183
ODM			3118161-01	3118166	3118165
ODL	+4	0	3118292-01	3118184	3118183
ODM			3118293-01	3118166	3118165
ODL	+5	0	3119588-01	3118184	3118183
ODM			3119589-01	3118166	3118165
ODL	+6	0	3118180-01	3118184	3118183
ODM			3118162-01	3118166	3118165
ODL	+8	0	3119498-01	3118184	3118183
ODM			3119497-01	3118166	3118165
ODL	+9	0	3118181-01	3118184	3118183
ODM			3118163-01	3118166	3118165
ODL	+12	0	3118182-01	3118184	3118183
ODM			3118164-01	3118166	3118165

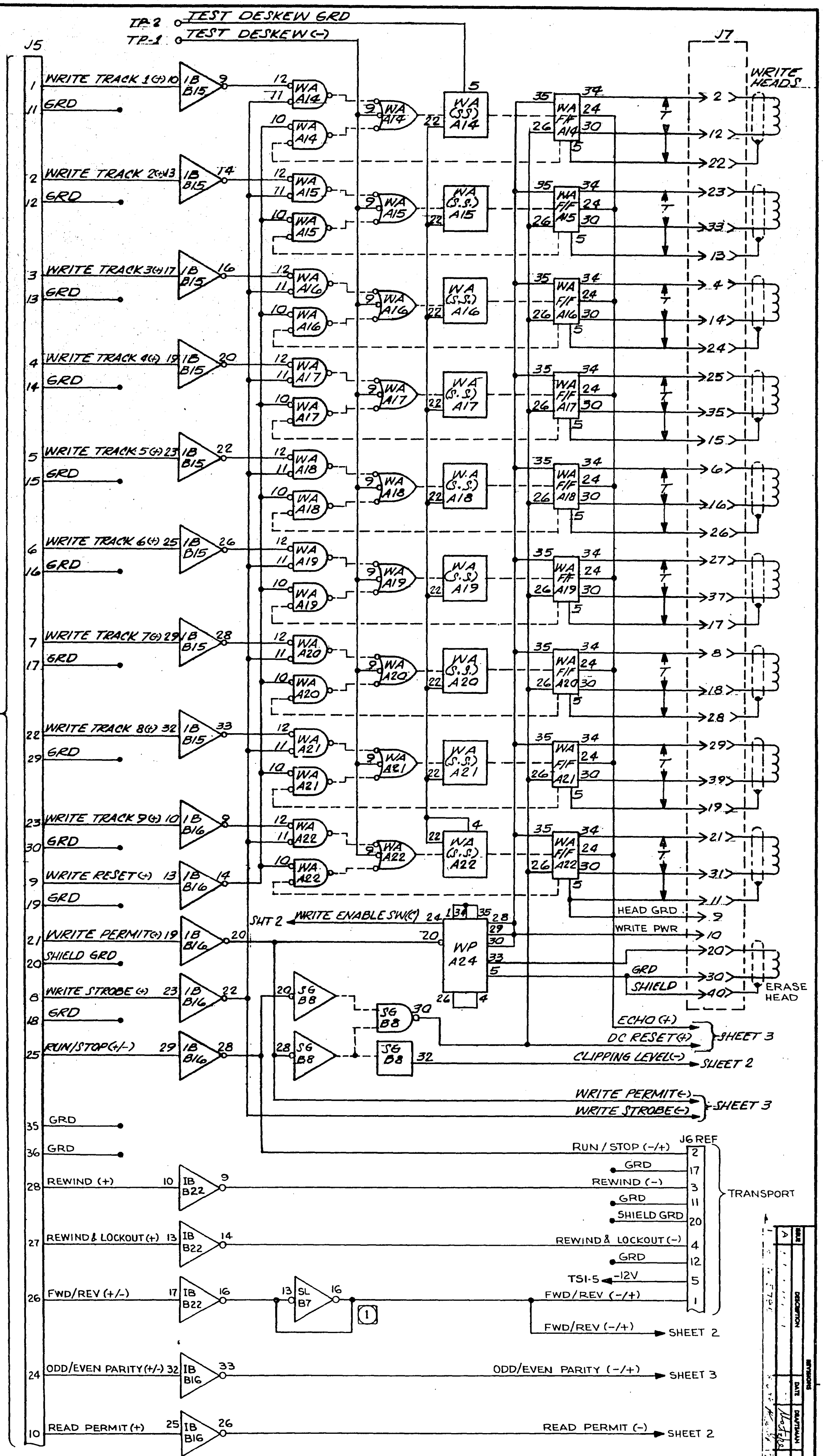
*The same PCB assemblies are also used for
0 volt TRUE and positive voltage FALSE output levels.

NOTES:

1. ON READ FWD ONLY SYSTEMS B7 IS OMITTED & JUMPERS B7-31 TO B7-4 AND B7-13 TO B7-16 ARE ADDED.

2. FOR UNSTROBED OUTPUTS REMOVE WIRE FROM B13-31 TO B13-34. ADD WIRE FROM B13-31 TO B13-5.

3. OPTION.



TP-2 TEST DESKEW GRD
TP-1 TEST DESKEW (-)
J5
J7
WRITE HEADS
CUSTOMER INPUTS
WRITE TRACK 1(+)
WRITE TRACK 2(+)
WRITE TRACK 3(+)
WRITE TRACK 4(+)
WRITE TRACK 5(+)
WRITE TRACK 6(+)
WRITE TRACK 7(+)
WRITE TRACK 8(+)
WRITE TRACK 9(+)
WRITE RESET(+)
WRITE PERMIT(+)
SHIELD GRD
WRITE STROBE (+)
RUN/STOP(+/-)
GRD
WRITE ENABLE SW(+)
SHT 2
HEAD GRD
WRITE PWR
SHIELD
ERASE HEAD
ECHO (+)
DC RESET(+)
SHEET 3
CLIPPING LEVEL(-)
SHEET 2
WRITE PERMIT(-)
WRITE STROBE(-)
SHEET 3
RUN / STOP (-/+)
J6 REF
REWIND (+)
REWIND (-)
SHIELD GRD
TRANSPORT
REWIND & LOCKOUT (+)
REWIND & LOCKOUT (-)
TSI-5
-12V
FWD/REV (+/-)
FWD/REV (-/+)
FWD/REV (-/+)
SHEET 2
ODD/EVEN PARITY (+/-)
ODD/EVEN PARITY (-/+)
SHEET 3
READ PERMIT (+)
READ PERMIT (-)
SHEET 2
REVISIONS

NEXT ASSY.	1ST USED ON
315770	DE-211

APPLICATION

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DWG. NO. 318315

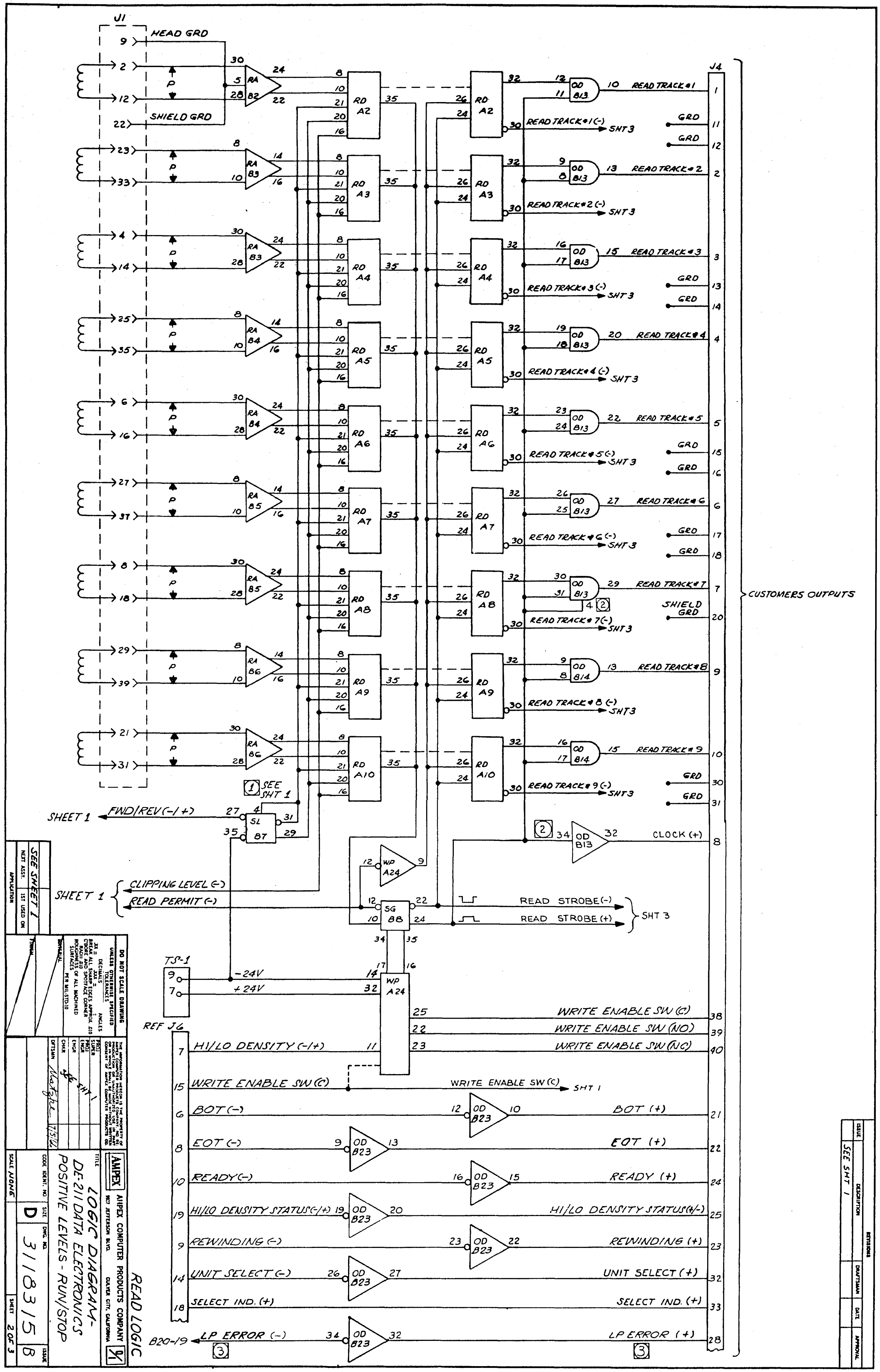
AMPEX

LOGIC DIAGRAM-
DF-211 DATA ELECTRONICS
POSITIVE LEVELS-RUN/STOP

SIZE D 09150 318315

SCALE NONE

SHEET 1 OF 3


J1
HEAD GRD
SHIELD GRD
J4
CUSTOMERS OUTPUTS
READ TRACK #1
READ TRACK #2
READ TRACK #3
READ TRACK #4
READ TRACK #5
READ TRACK #6
READ TRACK #7
READ TRACK #8
READ TRACK #9
READ TRACK #1 (-) SHT 3
READ TRACK #2 (-) SHT 3
READ TRACK #3 (-) SHT 3
READ TRACK #4 (-) SHT 3
READ TRACK #5 (-) SHT 3
READ TRACK #6 (-) SHT 3
READ TRACK #7 (-) SHT 3
READ TRACK #8 (-) SHT 3
READ TRACK #9 (-) SHT 3
GRD
SHIELD GRD
CLOCK (+)
SHEET 1
FWD/REV (-/+)
SEE SHT 1
CLIPPING LEVEL (-)
READ PERMIT (-)
READ STROBE (-)
READ STROBE (+)
SHT 3
TS-1
-24V
+24V
REF J6
WRITE ENABLE SW (C)
WRITE ENABLE SW (NO)
WRITE ENABLE SW (NC)
HI/LO DENSITY (-/+)
WRITE ENABLE SW (C)
WRITE ENABLE SW (C) SHT 1
BOT (-)
BOT (+)
EOT (-)
EOT (+)
READY (-)
READY (+)
HI/LO DENSITY STATUS (-/+)
HI/LO DENSITY STATUS (+/-)
REWINDING (-)
REWINDING (+)
UNIT SELECT (-)
UNIT SELECT (+)
SELECT IND. (+)
SELECT IND. (+)
B20-19
LP ERROR (-)
LP ERROR (+)
SEE SHEET 1
NEXT ASSY
1ST USED ON
APPLICATION
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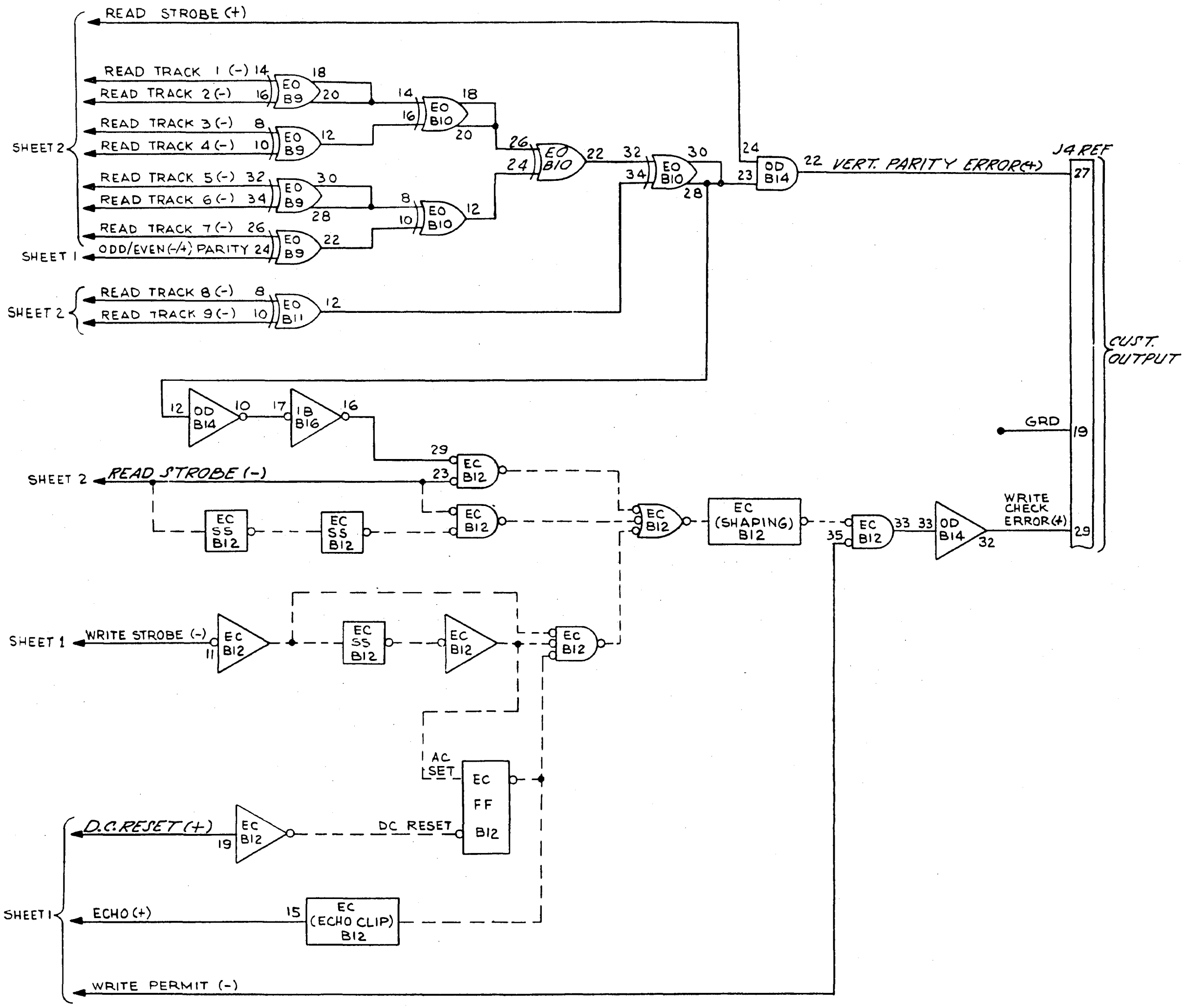
AMPEX
AMPEX COMPUTER PRODUCTS COMPANY
READ LOGIC
LOGIC DIAGRAM-
DE-211 DATA ELECTRONICS
POSITIVE LEVELS-RUN/STOP
SCALE NONE
D
B
SHEET 2 OF 3
REVISIONS
SEE SHT 1


READ STROBE (+)
READ TRACK 1 (-)
READ TRACK 2 (-)
READ TRACK 3 (-)
READ TRACK 4 (-)
READ TRACK 5 (-)
READ TRACK 6 (-)
READ TRACK 7 (-)
ODD/EVEN (-/+) PARITY
READ TRACK 8 (-)
READ TRACK 9 (-)
SHEET 2
SHEET 1
SHEET 2
EO B9
EO B10
EO B11
OD B14
VERT. PARITY ERROR(+)
J4 REF
CUST. OUTPUT
GRD
OD B14
IB B16
SHEET 2
READ STROBE (-)
EC B12
EC SS B12
EC (SHAPING) B12
OD B14
WRITE CHECK ERROR(+)
SHEET 1
WRITE STROBE (-)
AC SET
EC FF B12
D.C. RESET (+)
DC RESET
SHEET 1
ECHO (+)
EC (ECHO CLIP) B12
WRITE PERMIT (-)

ERROR CHECK OPTION

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TITLE
LOGIC DIAGRAM-
DE-21 DATA ELECTRONICS
POSITIVE LEVELS-RUN/STOP

CODE IDENT. NO.	SIZE	DWG. NO.	ISSUE
	D	311831 5	B

SCALE NONE — SHEET 3 OF 3

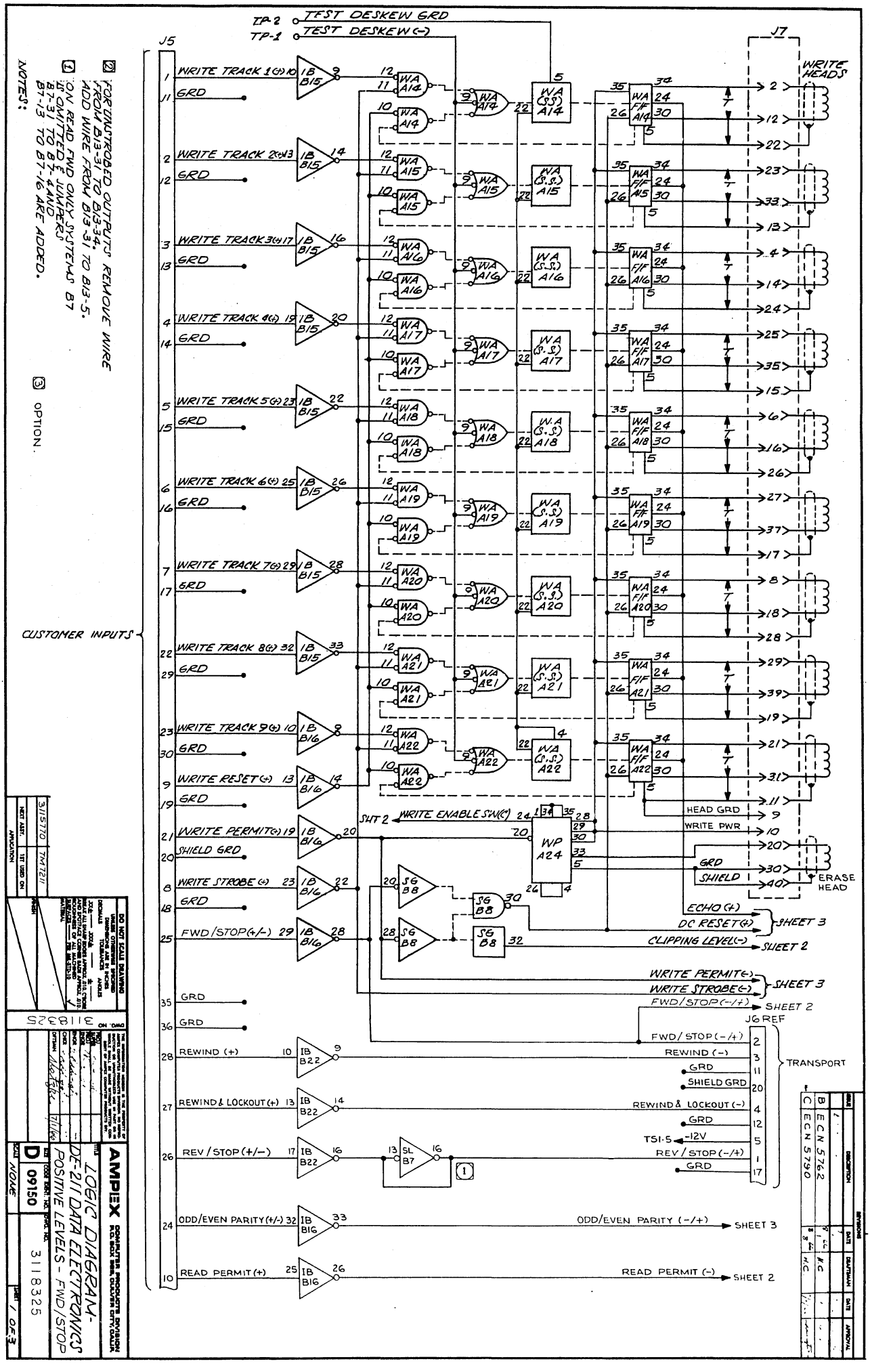
DO NOT SCALE DRAWING

NEXT ASSY.	1ST USED ON
SEE SHEET I	

APPLICATION

REVISIONS: SEE SHEET 1

311831 5



NOTES:

1. FOR UNUTROBED OUTPUTS, REMOVE WIRE FROM B13-31 TO B13-34. ADD WIRE FROM B13-31 TO B13-5.
2. ON READ FWD ONLY SYSTEMS B7 B7-31 IS OMITTED & JUMPERS B7-13 TO B7-16 ARE ADDED.
3. OPTION.

REVISIONS				
REV	DESCRIPTION	DATE	DRAFTSMAN	DATE
B	ECN 5762	8/1/69	R.C.	
C	ECN 5790	8/8/69	R.C.	

NEXT ASSY.	3115770		
APPLICATION	1ST USED ON	TM7211	

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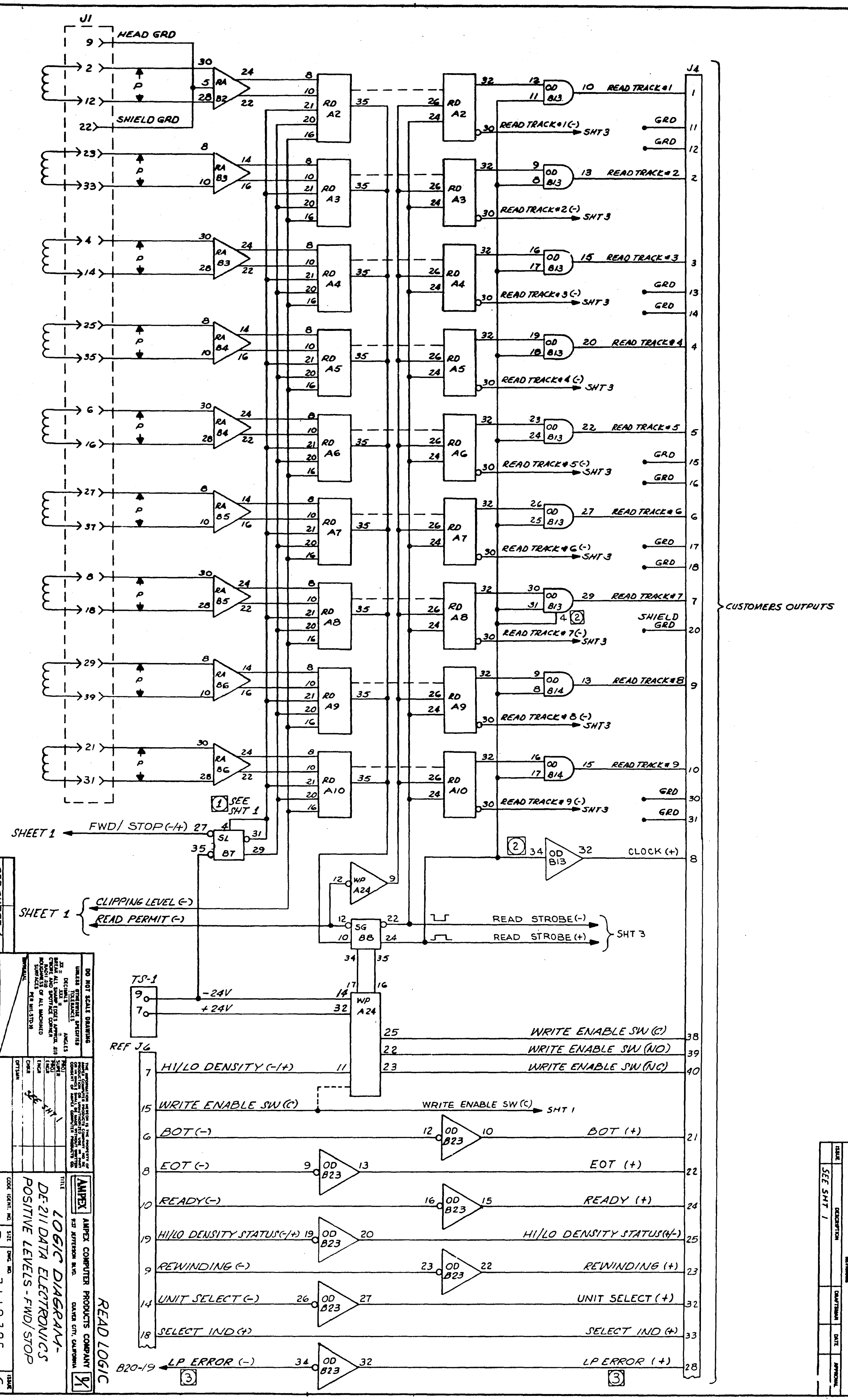
LOGIC DIAGRAM-DE-211 DATA ELECTRONICS POSITIVE LEVELS - FWD/STOP

SIZE D | CODE IDENT. NO. 09150 | SHEET 1 OF 3

DWG. NO. 3118325

SCALE NONE


J1
HEAD GRD
SHIELD GRD
J4
READ TRACK #1
READ TRACK #2
READ TRACK #3
READ TRACK #4
READ TRACK #5
READ TRACK #6
READ TRACK #7
READ TRACK #8
READ TRACK #9
READ TRACK #1 (-) SHT 3
READ TRACK #2 (-) SHT 3
READ TRACK #3 (-) SHT 3
READ TRACK #4 (-) SHT 3
READ TRACK #5 (-) SHT 3
READ TRACK #6 (-) SHT 3
READ TRACK #7 (-) SHT 3
READ TRACK #8 (-) SHT 3
READ TRACK #9 (-) SHT 3
SHIELD GRD
CUSTOMERS OUTPUTS
SEE SHT 1
SHEET 1
FWD/ STOP (-/+)
CLOCK (+)
CLIPPING LEVEL (-)
READ PERMIT (-)
READ STROBE (-)
READ STROBE (+)
SHT 3
TS-1
-24V
+24V
REF J6
HI/LO DENSITY (-/+)
WRITE ENABLE SW (C)
WRITE ENABLE SW (NO)
WRITE ENABLE SW (NC)
WRITE ENABLE SW (C) SHT 1
BOT (-)
BOT (+)
EOT (-)
EOT (+)
READY (-)
READY (+)
HI/LO DENSITY STATUS (-/+)
HI/LO DENSITY STATUS (+/-)
REWINDING (-)
REWINDING (+)
UNIT SELECT (-)
UNIT SELECT (+)
SELECT IND (+)
B20-19
LP ERROR (-)
LP ERROR (+)

SEE SHEET 1

NEXT ASSY. | USED ON | APPLICATION

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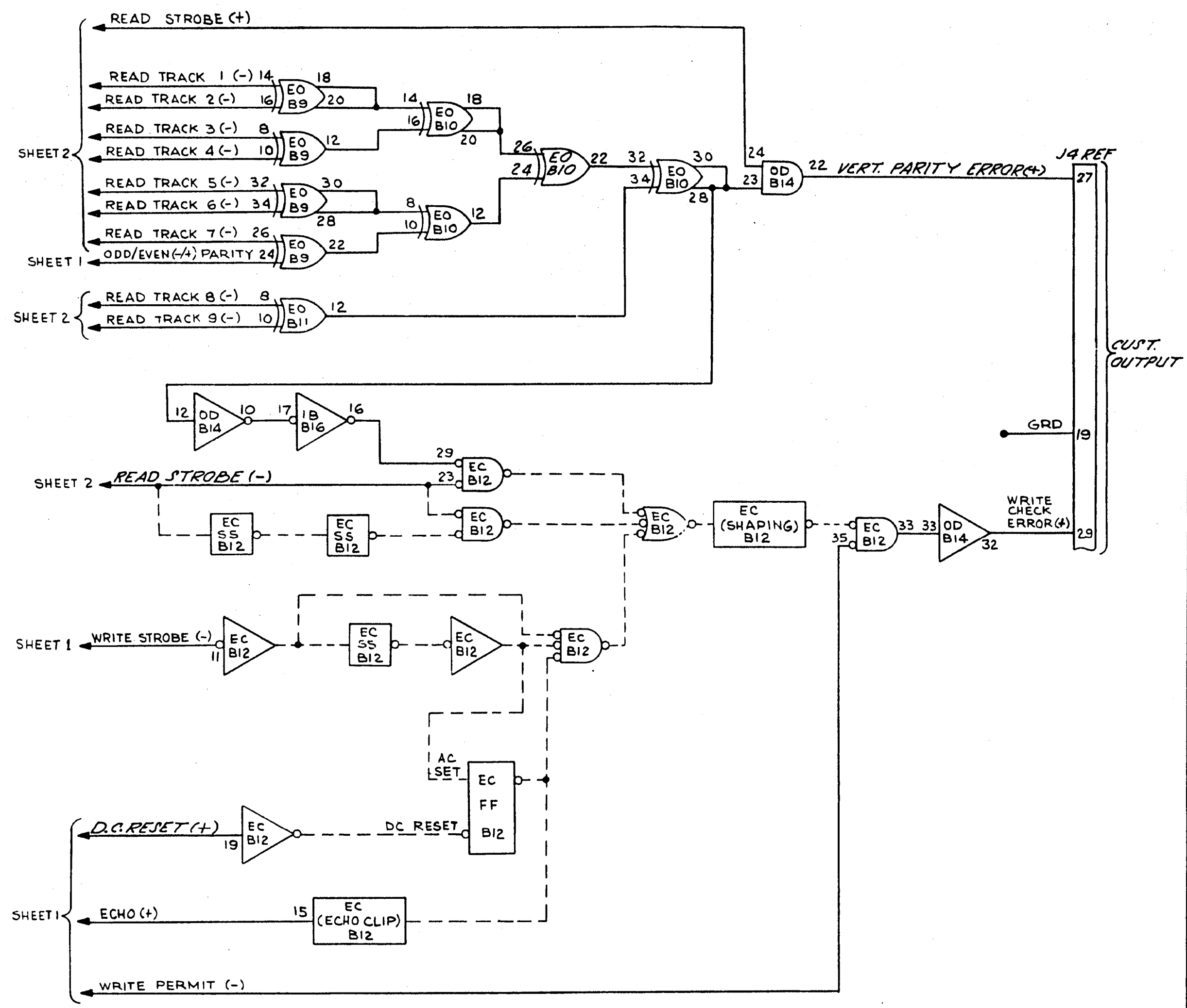
READ LOGIC

LOGIC DIAGRAM-
DE-211 DATA ELECTRONICS
POSITIVE LEVELS-FWD/STOP

SIZE D | DWG. NO. 3118325 | ISSUE C

SCALE NONE | SHEET 2 OF 3

SEE SHT 1



READ STROBE (+)
SHEET 2
READ TRACK 1 (-) 14
READ TRACK 2 (-) 16
READ TRACK 3 (-) 8
READ TRACK 4 (-) 10
READ TRACK 5 (-) 32
READ TRACK 6 (-) 34
READ TRACK 7 (-) 26
SHEET 1
ODD/EVEN (-/+) PARITY 24
EO B9
EO B10
EO B11
SHEET 2
READ TRACK 8 (-) 8
READ TRACK 9 (-) 10
OD B14
VERT. PARITY ERROR (+)
J4 REF
CUST. OUTPUT
GRD
IB B16
EC B12
SHEET 2
READ STROBE (-)
EC SS B12
EC (SHAPING) B12
WRITE CHECK ERROR (+)
SHEET 1
WRITE STROBE (-)
AC SET
EC FF B12
D.C. RESET (+)
DC RESET
SHEET 1
ECHO (+)
EC (ECHO CLIP) B12
WRITE PERMIT (-)

DE-211 LOGIC DIAGRAM, POSITIVE LEVELS, FWD/STOP (3 OF 3)

ERROR CHECK OPTION

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TITLE: LOGIC DIAGRAM- DE-211 DATA ELECTRONICS POSITIVE LEVELS-FWD/STOP

SIZE: D
DWG. NO. 3118325
ISSUE: C
SCALE: NONE
SHEET 3 OF 3

DO NOT SCALE DRAWING

SEE SHEET 1

318325

ISSUE	DESCRIPTION
	SEE SHEET 1

SPECIAL FEATURE (SF2)
VERTICAL PARITY GENERATE
(7 TRACK)

INTRODUCTION.

The vertical parity generate special feature provides a vertical parity bit (Write Data 7) to write track 7 of the data electronics. Odd or even parity is selected by the Odd/Even Parity select line.

GENERAL DESCRIPTION.

Exclusive-OR printed circuit board (PCB) assemblies (3107274-10) are inserted into locations A11 and A12 of the data electronics assembly. Four exclusive-OR circuits are provided on each of the PCB assemblies. The data electronics assembly is wired, and the logic elements operate, as shown in vertical parity generate logic diagram 3114921.

OPERATION.

The level of the Odd/Even Parity select line determines whether the parity bit supplied to write track 7 will generate odd or even parity. The parity bit is derived in the same manner as the vertical parity error output. Refer to the description of the vertical parity check circuit and the exclusive-OR circuit description for more details of circuit operation.

DRAWINGS.

The schematic diagram and assembly drawing of the Exclusive-OR PCB are located in Section VII. The logic diagram is located at the end of this special feature description.

APPLICABLE PRINTED CIRCUIT BOARD DRAWING

CODE	DESCRIPTION	PART NO.	SCHEMATIC	ASSY DWG
ECC	Exclusive-OR	3107274-10	3104453	3107274

LOGIC DIAGRAM

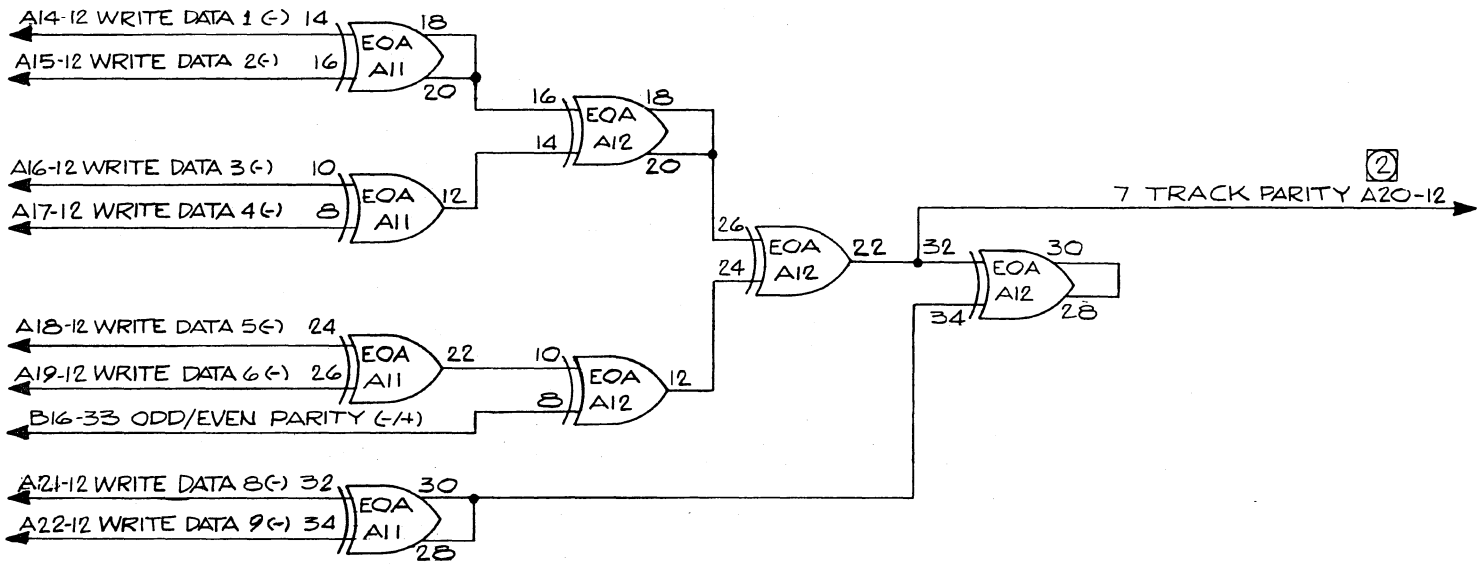
Vertical Parity Generate (7 Track) 3114921

REVISIONS				
ISSUE	DESCRIPTION	DRAFTSMAN	DATE	APPROVAL

PROTOTYPE ISSUE A

PROJ. ENGR 8-13-65

ENGR 8-13-65



2 A20-12 TO B15-28 IS DELETED.

1. THIS DIAGRAM TO BE USED IN CONJUNCTION WITH DATA ELECTRONICS LOGIC DIAGRAM WHEN VERTICAL PARITY GENERATE IS SELECTED.

NOTES:

DO NOT SCALE DRAWING

UNLESS OTHERWISE SPECIFIED TOLERANCES
DECIMALS ANGLES
.XX ± — .XXX ± — ± —
BREAK ALL SHARP EDGES APPROX. .010
C'BORE AND SPOTFACE CORNER RADII .010
ROUGHNESS OF ALL MACHINED SURFACES PER MIL-STD-10

MATERIAL

FINISH

3113340	DE-200
NEXT ASSY.	1ST USED ON
APPLICATION	

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ENGR		
CHKR		
DFTSMN R. Anderson	12 SEP 65	

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0/1

TITLE
LOGIC DIAGRAM-
VERT. PARITY GENERATE
7 TRACK

CODE IDENT. NO.	SIZE	DWG. NO.	ISSUE
	C	3114921	

SCALE NONE SHEET 1 OF 1

SPECIAL FEATURE (SF3)
VERTICAL PARITY GENERATE
(9 TRACK)

INTRODUCTION.

The vertical parity generate special feature provides a vertical parity bit (Write Data 4) to write track 4 of the data electronics. Odd or even parity is selected by the Odd/Even Parity select line.

GENERAL DESCRIPTION.

Exclusive-OR printed circuit board (PCB) assemblies (3107274-10) are inserted into locations A11 and A12 of the data electronics assembly. Four exclusive-OR circuits are provided on each of the PCB assemblies. The data electronics assembly is wired, and the logic elements operate, as shown in vertical parity generate logic diagram 3115766.

OPERATION.

The level of the Odd/Even Parity select line determines whether the parity bit supplied to write track 4 will generate odd or even parity. The parity bit is derived in the same manner as the vertical parity error output. Refer to the description of the vertical parity check circuit and the exclusive-OR circuit description for more details of circuit operation.

DRAWINGS.

The schematic diagrams and assembly drawings of the Exclusive-OR PCB are located in Section VII. The logic diagram is located at the end of this special feature description.

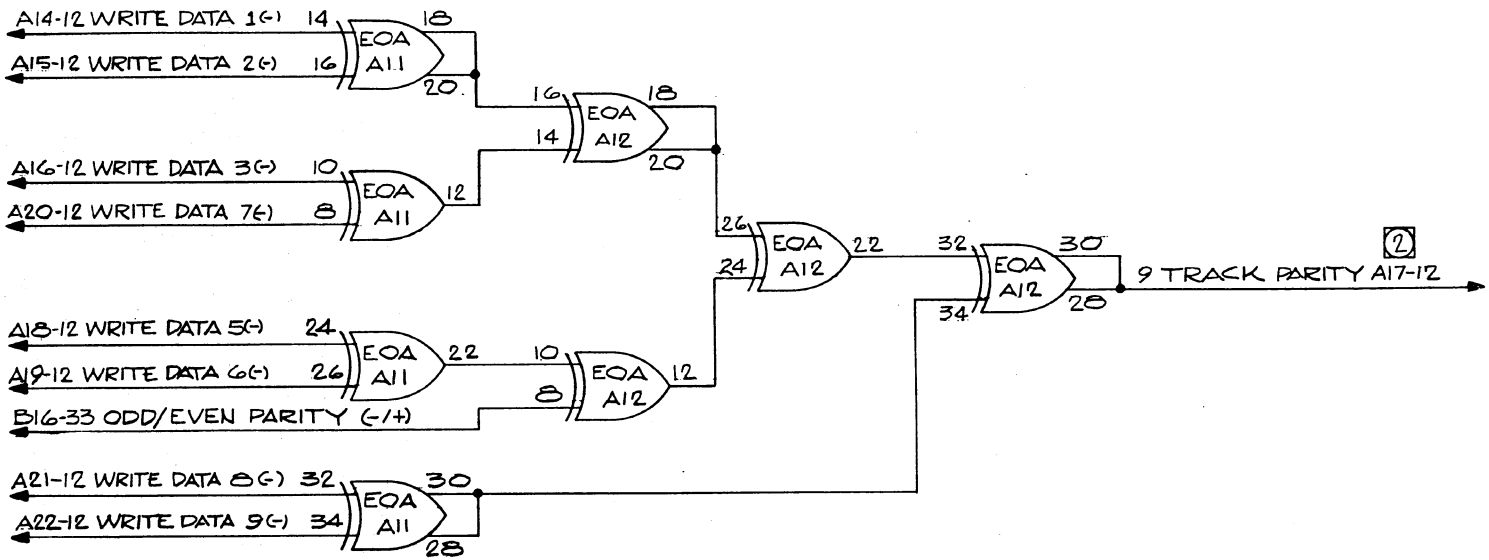
APPLICABLE PRINTED CIRCUIT BOARD DRAWING

CODE	DESCRIPTION	PART NO.	SCHEMATIC	ASSY DWG
ECC	Exclusive-OR	3107274-10	3104453	3107274

LOGIC DIAGRAM

Vertical Parity Generate (9 Track) 3115766

REVISIONS				
ISSUE	DESCRIPTION	DRAFTSMAN	DATE	APPROVAL
A	106-DH	RA	3 23 LL	



2 A17-12 TO B15-20 IS DELETED.

1. THIS DIAGRAM TO BE USED IN CONJUNCTION WITH DATA ELECTRONICS LOGIC DIAGRAM SHEET 1 WHEN VERTICAL PARITY GENERATE IS SELECTED.

NOTES:

DO NOT SCALE DRAWING

UNLESS OTHERWISE SPECIFIED TOLERANCES

DECIMALS XX ± ___ XXX ± ___ ANGLES ± ___

BREAK ALL SHARP EDGES APPROX .010
C'BORE AND SPOTFACE CORNER RADII .010
ROUGHNESS OF ALL MACHINED SURFACES PER MIL-STD-10

MATERIAL

FINISH

FINAL ASSY	TM-7211
NEXT ASSY.	1ST USED ON
APPLICATION	

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DFTSMN	R. Anderson	1/26/66

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TITLE

LOGIC DIAGRAMS- VERT. PARITY GENERATE 9 TRACK

CODE IDENT. NO.	SIZE	DWG. NO.	ISSUE
	C	3115766	

SCALE NONE SHEET 1 OF 1

SPECIAL FEATURE (SF4)
LONGITUDINAL PARITY CHECK

INTRODUCTION.

The longitudinal parity check feature is added to the data electronics by the addition of special printed circuit board (PCB) assemblies and wiring, as shown in the longitudinal parity check logic diagram.

GENERAL DESCRIPTION.

A flip-flop circuit is provided for each read track. Four flip-flops are provided on the Flip-Flop (FF) PCB at data electronics card cage location B17. Three flip-flops are provided on the Longitudinal Parity Register (PR) PCB at B19. Two additional flip-flops are provided on the Flip-Flop (FF) PCB at B18 for tracks 8 and 9. A gap detector circuit, adjusted to six character frame periods (at the lowest character rate) is also provided on the Longitudinal Parity Register PCB. The remaining circuitry required for longitudinal parity check is provided on the LPC Timing (LP) PCB at B20.

OPERATION.

While data is being read, the gap detector on PR at B19 is held on by the read strobe pulse train. The flip-flops (at B17, B19, and B18) are toggled by each read data bit and act as a read register. When longitudinal parity exists in a block of data, all of the flip-flops will be in the reset state following the LPC character and no LP error pulse is generated. When a longitudinal parity error occurs in a block of data, one of the flip-flops will be in the set state following the LPC character and a negative level is applied to the nine-input OR gate on LP at B20. The negative level output from the OR gate enables the LP error NAND gate on LP. The gap detector times out approximately six character frame periods after the LPC character is read and produces a positive-going output transition. The gap detector output is differentiated on LP to produce a negative-going LPC strobe pulse. The LPC strobe pulse is NANDed with the negative-level error output from the OR gate and produces a negative-going LP Error pulse output from the system. The positive-going trailing edge of the LP strobe pulse causes a negative-going LPC Register Reset pulse to be generated on LP and the flip-flops are reset to enable the longitudinal parity check circuit for the next block of data.

ADJUSTMENT.

To check or adjust for the six character frame period, an oscilloscope must be used to measure the timing delay between the leading edge of the last read strobe pulse and the positive-going trailing edge of the gap detector output pulse (at pin 25 of B19); adjust potentiometer R9 to obtain the time delay period listed in Table 1 for the applicable density/speed combination.

TABLE 1
LPC TIMING DELAY
(SIX CHARACTER PERIOD)

DENSITY	36 IPS	45 IPS	75 IPS	112.5 IPS	120 IPS	150 IPS
200 cpi	833 µsec	667 µsec	400 µsec	267 µsec	250 µsec	200 µsec
556 cpi	300 µsec	240 µsec	144 µsec	96 µsec	90 µsec	72 µsec
800 cpi	208 µsec	167 µsec	100 µsec	67 µsec	63 µsec	50 µsec

DRAWINGS.

The schematic diagrams and assembly drawings of the PCB assemblies are located in Section VII. The logic diagram is located at the end of this special feature.

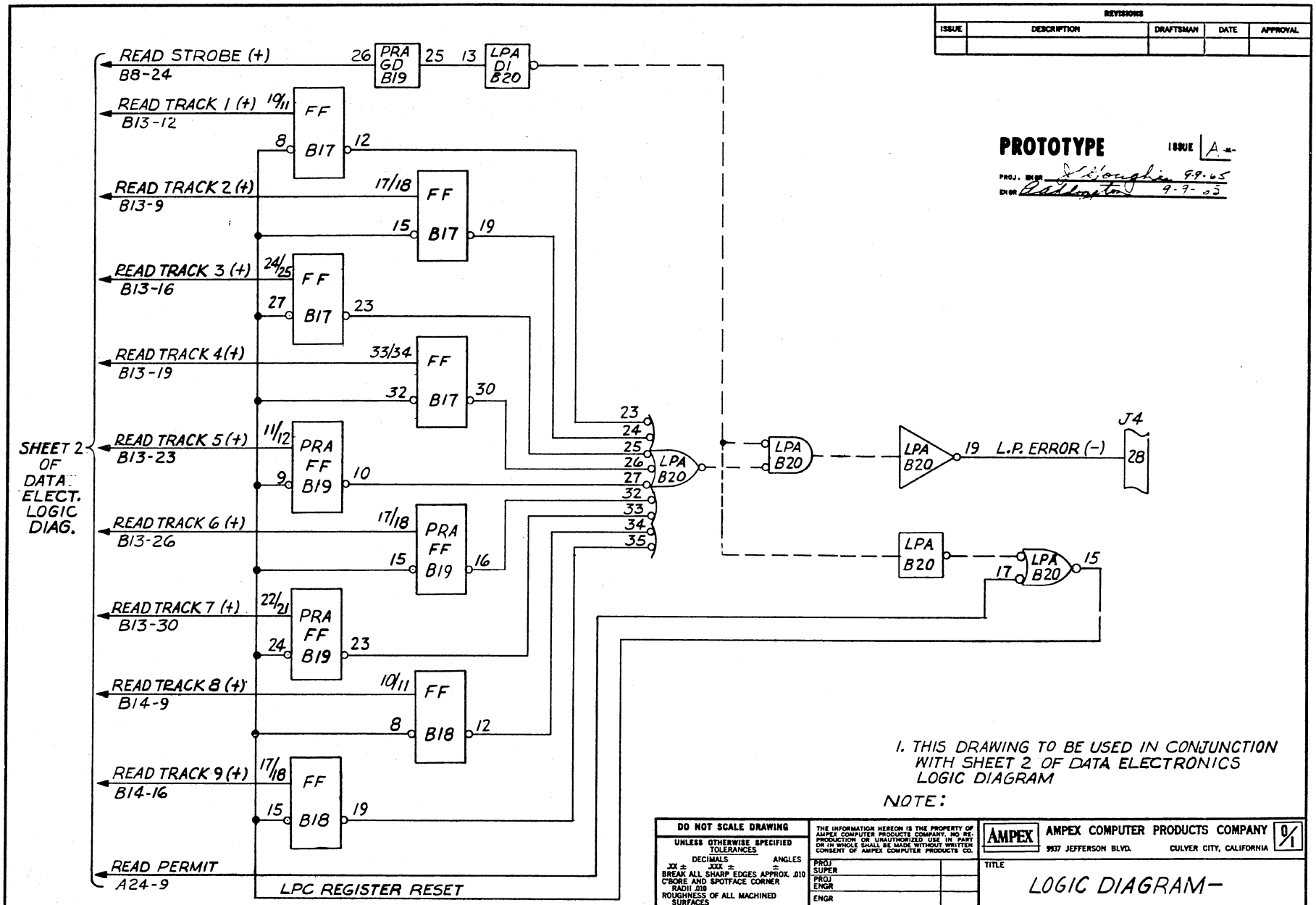
APPLICABLE PRINTED CIRCUIT BOARD DRAWINGS

CODE	DESCRIPTION	PART NO.	SCHEMATIC	ASSY DWG	LOCATION
FFB	Flip-Flop	3107275-10	3104541	3107275	B17, B18*
LPB	LPC Timing -B	3116087-10	3116088	3116087	B20
PRB	Long. Parity Reg -B		3116083	3116100	B19
	36/45 Ips	3116082-10			
	75 Ips	3116161-10			
	112.5/120/150 Ips	3116162-10			

LOGIC DIAGRAM

Longitudinal Parity Check 3114904

*Not required in 7-track systems.


READ STROBE (+)
B8-24
26
PRA GD B19
25
13
LPA DI B20
READ TRACK 1 (+)
B13-12
19/11
FF B17
8
12
READ TRACK 2 (+)
B13-9
17/18
FF B17
15
19
READ TRACK 3 (+)
B13-16
24/25
FF B17
27
23
READ TRACK 4 (+)
B13-19
33/34
FF B17
32
30
SHEET 2 OF DATA ELECT. LOGIC DIAG.
READ TRACK 5 (+)
B13-23
11/12
PRA FF B19
9
10
READ TRACK 6 (+)
B13-26
17/18
PRA FF B19
15
16
READ TRACK 7 (+)
B13-30
22/21
PRA FF B19
24
23
READ TRACK 8 (+)
B14-9
10/11
FF B18
8
12
READ TRACK 9 (+)
B14-16
17/18
FF B18
15
19
READ PERMIT
A24-9
LPC REGISTER RESET
23
24
25
26
27
32
33
34
35
LPA B20
LPA B20
LPA B20
19
L.P. ERROR (-)
J4
28
LPA B20
LPA B20
17
15
REVISIONS
ISSUE
DESCRIPTION
DRAFTSMAN
DATE
APPROVAL
PROTOTYPE
ISSUE A
PROJ. ENGR
ENGR
9-9-65
9-9-65
1. THIS DRAWING TO BE USED IN CONJUNCTION WITH SHEET 2 OF DATA ELECTRONICS LOGIC DIAGRAM
NOTE:
DO NOT SCALE DRAWING
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DECIMALS
ANGLES
BREAK ALL SHARP EDGES APPROX. .010
C'BORE AND SPOTFACE CORNER RADII .010
ROUGHNESS OF ALL MACHINED SURFACES PER MIL-STD-10
MATERIAL
FINISH
NEXT ASSY.
TM 7211
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APPLICATION
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CHKR
DFTSMN Fujimoto 7-13-65
AMPEX COMPUTER PRODUCTS COMPANY
9937 JEFFERSON BLVD.
CULVER CITY, CALIFORNIA
0/1
TITLE
LOGIC DIAGRAM—
LONGITUDINAL PARITY CHECK
CODE IDENT. NO.
SIZE
C
DWG. NO.
3114904
ISSUE
SCALE —
SHEET 1 OF 1

SPECIAL FEATURE (SF5)
LONGITUDINAL CHECK CHARACTER GENERATE

INTRODUCTION.

The longitudinal check character generate special feature provides an internally generated Write Reset signal which causes a longitudinal check character (LCC) to be written. Changes to the data electronics for this special feature includes the addition of an LCC Generator (LG) printed circuit board (PCB) assembly at location A13 in the data electronics card cage and additional wiring as shown in the LCC Generate logic diagram.

GENERAL DESCRIPTION.

The absence of a Write Strobe input for the equivalent of four character frame periods is interpreted as the end of a block of data. A Write Reset pulse is generated at this time by the LCC generate circuit and the write registers of the data electronics are reset, causing the LCC to be written on the tape. Two adjustments are provided; one for low density LCC generate timing, the other for high density LCC generate timing. The delay time is selected by the level of the Hi/Low Density select signal.

OPERATION.

The Write Strobe pulse input to the gap detector circuit causes timing capacitor C9 to be charged on receipt of the first Write Strobe pulse and with each succeeding pulse. When no Write Strobe pulses occur for approximately four character frame periods at the selected density/speed combination, timing capacitor C9 discharges and the gap detector produces a positive-going output transition. The gap detector output is differentiated on LG to produce a negative-going Write Reset pulse which resets the write register flip-flops on tracks which have had an ODD number of ONEs written. The LCC is written on the tape when the flip-flops are reset.

Two delay times are preset for the gap detector. When the Hi/Low Density select input to LG is at 0 volts (low density select), Q3 is biased on by the fixed -6 volt level applied at pin 32 of LG. When Q3 conducts, Q1 and Q5 are held cut off by the -7 volt level established at the common emitters by current flow through Q3 (the bases of Q1 and Q5 are at 0 volts, thus the base-to-emitter voltages are positive and establish the cut off condition). When Q1 and Q5 are cut off, Q2 and Q6 are also cut off, effectively removing delay adjustment potentiometers R5 and R15 from the gap detector timing circuit. Transistor Q4 is biased on by Q3 and provides a return to -12 volts (through delay adjustment potentiometer R10) for timing capacitor C9. Potentiometer R10 is adjusted to provide a delay of approximately four character frame periods at the low-density/speed rate. When the Hi/Low Density select input to LG is at -12 volts (high density select), Q5 is biased on. When Q5 conducts, Q1 and Q3 are cut off by the -7 volt level established at the common emitters by current flow through Q5 (the bases of Q1 and Q3 are at 0 volts and -6 volts, respectively, thus the base-to-emitter voltages are

positive and establish the cut off condition). When Q1 and Q3 are cut off, Q2 and Q4 are also cut off, effectively removing delay adjustment potentiometers R5 and R10 from the gap detector timing circuit. Transistor Q6 is biased on by Q5 and provides a return to -12 volts (through delay adjustment potentiometer R15) for timing capacitor C9. Potentiometer R15 is adjusted to provide a delay of approximately four character frame periods at the high-density/speed rate.

ADJUSTMENT.

To check or adjust for the four character frame period, an oscilloscope must be used to measure the timing delay between the leading edge of the last Write Strobe pulse and the leading edge of the Write Reset pulse at pin 16 of A13. For low density, adjust potentiometer R10 to obtain the time delay period listed in Table 1 for the applicable low-density/speed combination; for high density, adjust potentiometer R15 to obtain the time delay listed for the applicable high-density/speed combination.

TABLE 1
LCC GENERATE DELAY
(FOUR CHARACTER PERIOD)

DENSITY	36 IPS	45 IPS	75 IPS	112.5 IPS	120 IPS	150 IPS
200 cpi	556 µsec	444 µsec	267 µsec	178 µsec	167 µsec	133 µsec
556 cpi	200 µsec	160 µsec	96 µsec	64 µsec	60 µsec	50 µsec
800 cpi	139 µsec	111 µsec	67 µsec	44 µsec	42 µsec	33 µsec

DRAWINGS.

The schematic diagram and assembly drawing of the PCB are located in Section VII. The logic diagram is located at the end of this special feature.

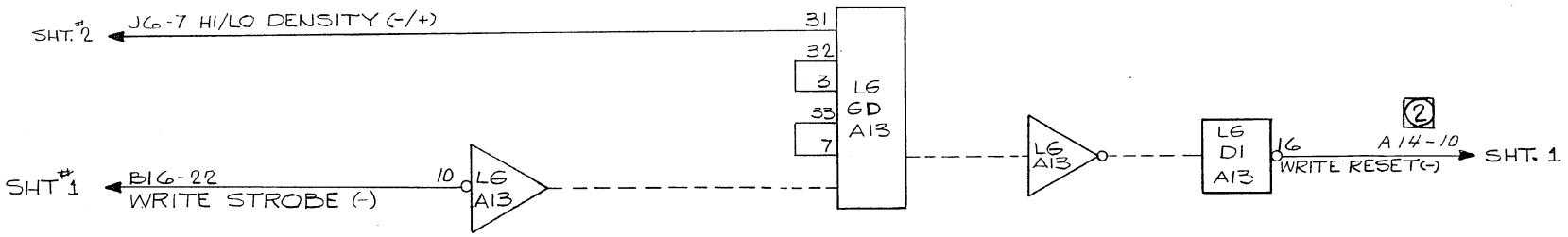
APPLICABLE PRINTED CIRCUIT BOARD DRAWINGS

CODE	DESCRIPTION	PART NO.	SCHEMATIC	ASSY DWG
LGB	LCC Generator -B		3116076	3116075
	36/45 Ips	3116072-10		
	75 Ips	3116142-10		
	112.5/120/150 Ips	3116073-10		

LOGIC DIAGRAM

LCC Generate (Dual Density)	3115776

REVISIONS					
ISSUE	DESCRIPTION	DATE	DRAFTSMAN	DATE	APPROVAL
A	ECN 10[illegible]	2, 66	R.A.	2, 66	[illegible]
B	ECN 9988	12/28/66	[illegible]	[illegible]	[illegible]



DWG. NO. 3115776

(2) EXTERNAL WRITE RESET B16-14 TO A22-10 TO BE REMOVED.

1. THIS DRAWING TO BE USED IN CONJUNCTION WITH SHEETS 1 & 2 OF DATA ELECTRONICS LOGIC DIAGRAMS.

DO NOT SCALE DRAWING
UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ANGLES
.XX± —— .XXX± —— ± ——
BREAK ALL SHARP EDGES APPROX. .010. C'BORE AND SPOTFACE CORNER RADII APPROX. .010.
ROUGHNESS OF ALL MACHINED SURFACES —— PER MIL-STD-10 ✓
MATERIAL
FINISH

FINAL ASSY TM 7211
NEXT ASSY. | 1ST USED ON
APPLICATION

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ENGR	[illegible]	12-31-66
CHKR	[illegible]	12-31-66
DFTSMN	R. Anderson	12/15/65

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P.O. BOX 329, CULVER CITY, CALIF.

TITLE: LOGIC DIAGRAM-
LCC GENERATE "B"
DUAL DENSITY

SIZE	CODE IDENT. NO.	DWG. NO.
C	09150	3115776

SCALE NONE | SHEET 1 OF 1